SENTRY VII

SENTRY VII

PRODUCT DESCRIPTION

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FAIRCHILD
SYSTEMS TECHNOLOGY
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

PROPOSAL FOR A SENTRY VII TEST SYSTEM

FIGURES

SECTION 1

SENTRY VII SPECIFICATION

1.0 SYSTEM DESCRIPTION

The Fairchild Systems Technology Sentry VII is a universal test system, designed to operate in a multitude of environments to meet a multitude of testing needs. For the engineer, the Sentry VII combines over 50 man-years of sophisticated software development and high-speed hardware technology with an extensive customer-feedback loop, resulting in a powerful yet flexible characterization and analysis tool. For the Quality Control Engineer, Shmoo plots, histograms, delta measurements, extensive datalogging and data manipulation are part of the standard Sentry software; environmental changers and handlers are readily interfaced to the high speed test head to aid in component evaluation.

The Sentry VII hardware is modularly designed to enable each customer to select that configuration which best suits his present needs.

Basically, the system permits expansion in various test areas solely through the addition or selection of different test stations. The basic building block (the FST-2 computer with 32K 24-bit word memory), the Video Keyboard Terminal, and other peripherals, have been designed to control and operate up to 2 test stations.

The extensive number of software routines available to the user combined with the ability to transfer data to and from an 18 megabit disc, gives the Sentry an unparalleled ability within the device characterization and data analysis field. This ability includes plots of mathematical functions, parametric distributions, three-dimensional distributions (commonely referred to as composite SHMOOs) and matrices with various X and Y parameters.

The Sentry VII test station electronics combined with the High Speed Test Controller provide the capability to do functional test at a 5 or 10MHz rate, DC parametric tests at rates up to 300 tests/second. These tests are performed at the programmed rate by inputting data to the DUT and comparing its outputs with expected values. These inputs and output values are stored in a local memory in the High Speed Controller. An optional hardware pattern generator is also available for the generation of DUT inputs and outputs.

The basic Sentry VII system includes a 5 or 10 MHz 30-pin test station. The test stations of the Sentry include true universal capability for all active test pins. Each test pin under software control may be assigned as an Input Driver, Output Comparator, Input Clock, Bias Supply, Load, or Input/Output Pin. The precision measurement unit may be connected to any device pin to measure or datalog the voltage/current parametric characteristics of the device under test.

The local memory is a specialized processor which consists of bipolar random access memory, control registers, and instruction set. One local memory channel is assigned to each DUT pin. By using RAMs for local memory, the FST-2 computer can update the functional patterns in local memory while testing is going on at the programmed rate.

Under standard system software control, local memory can be segmented into major

and minor loops with separate start and stop addresses and loop counts. With the Sequence Processor, the Sentry further condenses long test patterns for optimum use of local memory by modifying register definitions on-the-fly, nesting subroutines up to 16 deep, and doing clock-bursts. The Sentry VII Pattern Processor for testing large scale memory chips also makes maximum use of local memory, by offering independent X- and Y-addressing, split-cycle timing, topological scrambling, hardwired data equations, and pseudo-random data generation.

Several registers within the High Speed Controller allow control of each DUT pin while testing at the programmed rate. Two pairs of mask and I/O definition registers allow changing of DUT pin I/O definition and "care"/"don't care" conditions "on the fly". Another register controls selection of the input reference voltage pair to the DUT inputs; up to four pairs of input reference voltages are available for selection by this register. Other registers control data driver mode definitions, record failures and invert data patterns.

Output data of the device under test is checked via the high speed comparator for level and polarity and with the stored expected output pattern and sequence of the local memory associated with that pin.

The test instruction set for control of the bias and reference supplies, the system control registers, the timing generators, local memory and pin electronics, as well as the functional pattern, are stored as part of the device test program on the disc and in the FST-2 computer. The local memory instruction set, the timing generator conditions and the Precision Measurement Unit (PMU) conditions as well as the bias supply conditions are under complete control of the user's device program.

The Sentry VII is focused on the testing and data analysis requirements for state-of-the art devices. The system is organized to perform that task. The Sentry VII includes three hardware groups, which are:

1. Peripherals
2. Central Control Console
3. High Speed Test Station Group

1.1 System Peripherals and External Interfaces

The system software supports any combination of available peripherals and External Interfaces. Peripheral equipment available with the system includes a video keyboard terminal, magnetic tape unit, high speed or medium speed line printer, card reader and disc. External interfaces include a Data Set interface and an Instrumentation Bus interface. All peripherals are referenced by name in software; therefore, additional peripherals may be utilized with no basic operational change.

1.1.1 Data Set Interface

The Data Set interface is available to provide a communications Link to data processing facilities. This link may be used for down loading test programs from a host CPU or up loading test result data to the host for storage, in-depth statistical analysis, and user defined graphic reports.

The Data Set interface is fully compatible to EIA standard RS232C and Bell System 202S operating discipline. Data is transmitted asynchroneously in ASCII or packed Binary at switch selectable data rates of 110 -9600 Baud. A Communication link may be established in a local null-modem configuration when the host CPU is adjacent to Sentry test system. If the host CPU is remote, the Data Set interface may be used with a Bell System 202S Data Set to establish a 1200 BAUD communications link over dial-up facilities. Data integrity is assured by cross-parity error checking on all messages. If an error is detected in any message, the message is automatically retransmitted and verified.

1.1.2 Instrumentation Bus Interface

The Instrumentation Bus Interface is an external interface which, like the Data Set interface, is an industry standard interface providing greater system flexibility. The Instrumentation Bus interface is available to communicate with external instrumentation compatible to ANSI/IEEE Standard 488-1975 "Digital Interface for Programmable Instrumentation."

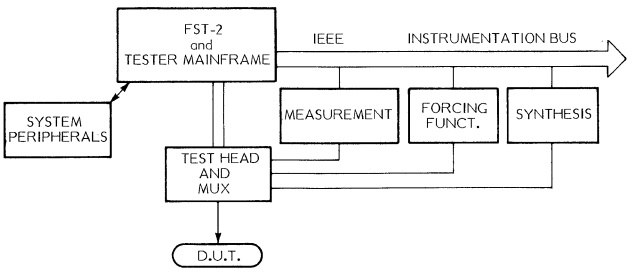
The Bus functions of Talker, Listener, and Controller may be invoked by the operator from the VKT keyboard or by a FACTOR program. Up to 14 external instruments may be connected to the Bus and programmed directly through the Instrumentation Bus Interface.

This interface option is fully compatible to the IEEE Standard and will, therefore, support any instrument which is likewise compatible. The Instrumentation Bus Interface is highly recommended for Sentry VII Tester applications requiring auxiliary instrumentation above and beyond basic tester capabilities. Wafetek, Dana, Fluke, Systron Donner, Tektronix, Hewlett-Packard, and Fairchild presently manufacture instrumentation in compliance to the Standard. An abbreviated list of the instrument functions available include:

- Frequency Synthesizers
- Signal Generators
- Counters
- Multimeters
- Crosspoint Matrix Controllers
- Word Generators
- Function Generators
- Capacitance Bridges
- Pulse Generators
- UHF/VHF Test Sets
- Programmable Filters
- Programmable Calibrators

As can be seen, the variety of instrumentation which can be configured in Sentry VII automatic test applications is not limited to the resources of one supplier, nor is custom built interfacing required before it can be used.

The following diagram illustrates a typical application.



The FACTOR statement and format to communicate with instruments on the bus is as follows:

EXEC IB (FUNCTION, UNIT, ARRAY, ERROR):

where the parameters are:

Function→function code
- 0 = reset
- 1 = write ASC11
- 2 = read ASC11
- 3 = write variable
- 4 = read variable
- 5 = wait for SRQ
- 6 = addressed or universal command

Unit→a constant or variable name representing the unique address of an instrument and the bus.

Array→an array name of the data to be transferred to the addressed instrument or the area for the received data to be stored.

Error→a code returned from the BI program in the event the requested operation cannot be performed correctly.

This literal operand structure allows you to program instruments on the Bus in their own language and translate retrieved data into FACTOR compatible form transparently.

1.1.3 Video Keyboard Terminal (VKT)

The Video Keyboard Terminal consists of a keyboard and a CRT display; it is the primary man-machine interface. The VKT operates much like a conventional teletype, except with greater ease, convenience, quietness, and speed.

Program statements and system control commands entered on the keyboard are transmitted to the computer and simultaneously displayed on the VKT display. Programs and system control commands already stored in the computer can also be displayed on the VKT.

The video display provides a visual record of all keyboard operations and displays all test programs on call, all test station registers, and test results for both function and parametric testing. The unit is also used to edit test programs.

CHARACTER REPERTOIRE:

63 USASCII alphanumeric characters, space and one special symbol

DATA TRANSMISSION RATE:

9600 baud (when used with the Sentry systems)

KEYBOARD:

Solid state with teletype key arrangement

1.1.4 Disc Memory

The system operates with a fast, fixed head disc memory to provide instant access to any test program in the user's device library, to remove core size restrictions, and to store the operating system software and complete system diagnostic and self-check programs.

This unit is an extension of the main core-memory. It has one rotating disc, and uses the one head per-track principle. The unit is self-contained, requiring only an external ac power source and external input/output control.

STORAGE CAPACITY:

737,280 24-bit words

TRANSFER RATE:

113,000 words/second

AVERAGE ACCESS TIME:

17 msec

DISC ROTATION SPEED:

1745 RPM

1.1.5 Card Reader

The card reader provides a fast, convenient and flexible means of loading test programs.

The unit reads 80-column, punched, data processing cards, column-by-column. The card reader operates in a remote mode in response to commands from the computer. Data is transferred from the cards via the card reader, and transmitted as electrical pulses to the FST-2 computer.

CARD STORAGE: 500 cards maximum
CARD READING RATE: 400 cards/minute

1.1.6 Line Printers

Medium Speed Line Printer

The medium speed line printer is available for applications requiring printed test data.

This is a medium speed impact printer that uses a 5 x 7 dot matrix to generate each character. The printer uses sprocket-fed paper and can be adjusted to any paper width between 4 inches and 14-7/8 inches. It will print up to 132 columns when full-width paper is used, and it can produce an original plus four legible copies.

CHARACTER SET:

USASCII - 63 characters plus space

PRINTING STRUCTURE:

132 char./line
60 lines/minute
(132 char./line)
200 lines/minute (approximately 16.5 char./line)

CHARACTER STRUCTURE:

5 x 7 dot matrix 10 point type equiv.

PAPER DIMENSIONS:

Standard fanfold, edge punched adjustable to maximum of 14-7/8 in. with 11 in. between folds

High Speed Line Printer

The high speed line printer is also available for applications requiring large quantities of printed test data. This unit is similar to the medium speed line printer, except that it is a drum printer and the print speed is 480 cps.

CHARACTER SET:

USASCII - 63 char. plus space

PRINTING STRUCTURE:

80 char./line, 6 lines/in.

PRINTING SPEEDS:

356 lines/min. for 80 char.
460 lines/min. for 60 char.
650 lines/min. for 40 char.
1110 lines/min. for 20 char.

PAPER DIMENSIONS:

Standard fanfold, edge punched 4 in. to 9-5/16 in. wide with 11 in. between folds.

1.1.7 Magnetic Tape Drive

The magnetic tape drive provides fast means of loading system software and device test programs. Tape speed is 24 inches/second (ips) for both the normal read and write operations. The rewind and fast forward speed is 150 ips. Recording density is 800 bits/inch (bpi), with a 9-track, ASCII format that is IBM-compatible. Tape dimensions are 1/2 inch x 1.5 mil x 2400 feet on a 10-1/2 inch reel (IBM or NAB).

1.2 CENTRAL CONTROL CONSOLE

The Central Control Console Mainframe houses the Computer, RVS's, DPS's, PMU, and High Speed Controller, all in one cabinet.

1.2.1 FST-2 Computer

The nucleus of the Sentry family is Fairchild's FST-2 general purpose 24-bit word computer which controls the complete system. Using FACTOR, an English-like test program language, the computer transmits control data, and receives subsystem status reports, interrupt requests and test data. Figure 1-1 is a photograph of a FST-2 25 x 8K semiconductor memory module.

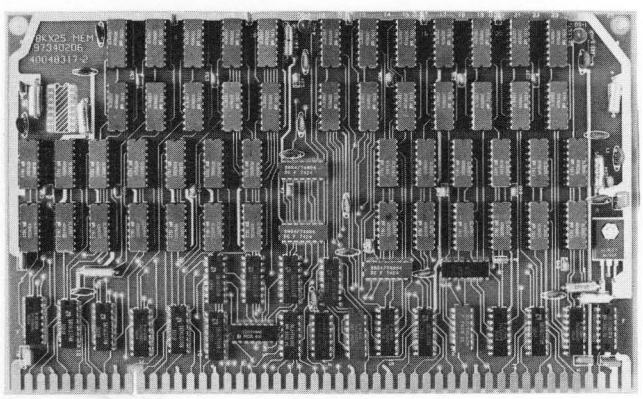


Figure 1-1. FST-2 Semiconductor Memory (25x8K) PCB

The FST-2 Computer is a general purpose digital computer and consists of three subsystems: central processing unit (CPU), memory, and interface.

Controls are available on the test station panel for controlling the FST-2 during normal operation.

An additional set of controls is located on the CPU behind the left panel mainframe cabinet. These controls are primarily for maintenenace personnel and are not normally used by the test system operator.

This maintenance panel (see Figure 1-2) provides all controls and indicators for the FST-2. The switch register provides a means of manually setting up a 24-bit word. The contents of various working registers may be displayed on the lamps above the switches. In the bottom right hand corner are located in the main computer switches; i.e., START, STOP, etc.

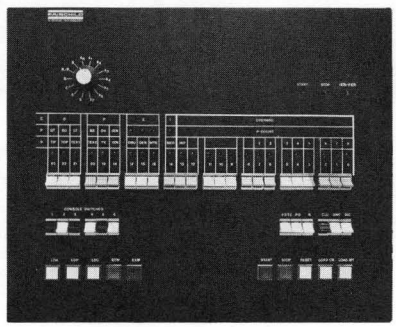


Figure 1-2. FST-2 Computer Maintenance Panel

The computer uses semiconductor memory. A minimum memory subsystem is 32K 25-bit words (bit 25 is memory parity) and can be expanded in increments of 16K words up to 196,608 words. Operating in a Direct Memory Access mode, the computer minimizes test execution time by direct loading of local memory. By increasing CPU memory capacity to 32K and greater, test throughput improvement factors of two (2) or more can be obtained.

The A memory and B memory data buses are interfaced to the memory and primarily used for transmitting functional test data at memory speeds to the tester. Both of these memory buses may be in operation at the same time.

The basic configuration for the FST-2 is shown in Figure 1-3a.

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FST-2 features are as follows:

1. 24-bit data word
2. 1.75 microsecond memory-cycle time
3. 32K of semiconductor storage, expandable in 16K modules up to 196K.
4. Dual memory-access via two memory buses
5. Random direct memory access, stored by/retrieved at 571,000 words per second per memory bus
6. Separate interface control between memory modules and CPU or tester
7. Interrupt sub-system for communications and data transfer between CPU and peripheral units via accumulator bus
8. 16 external interrupt channels and a maximum of 64 memory interrupt locations
9. 7 index register for address modification available to programmer and a relocation register
10. Indirect addressing for most instructions
11. A six-bit operation code for the following types of instructions:
    - load and store
    - arithmetic
    - logical operations
    - register and state
    - conditional and unconditional branch
    - transfer-control
    - shift
    - input/output

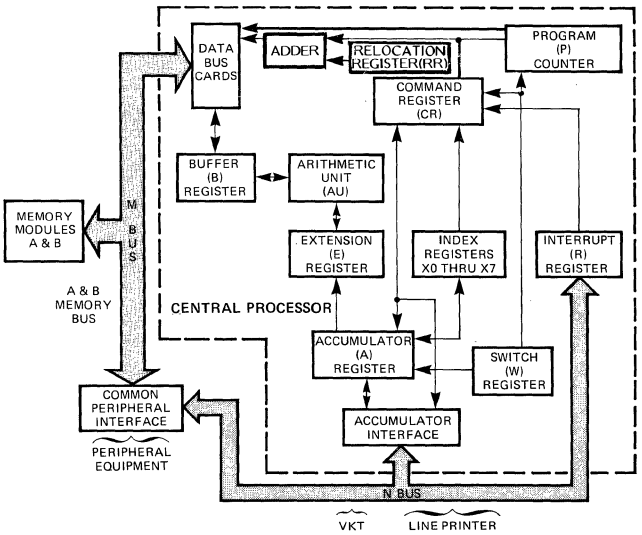


Figure 1-3a. FST-2 Simplified Block Diagram

1.2.2 Reference Voltage Supplies

The Reference Voltage Supplies (RVS's) provide the "1" and "0" logic levels to the drivers and detectors. The system is supplied with up to five pairs of RVS supplies contained on 5 boards (one pair per board). The driver RVS's are designated E0/E1, EA0/EA1, EB0/EB1 and EC0/EC1. The comparator reference supplies are designated S1 and S0.

1.2.3 Digital Programmable Supplies

The mainframe also contains up to three Digital Programmable Supplies (DPS). These supplies provide both programmable voltages and programmable currents to the High Speed Test Station for parametric testing.

Digitally Programmable Supplies (DPS's) provide the necessary bias supplies to activate the DUT when connected externally at the load board. The supplies can be programmed to force a voltage with a programmable current trip. The DPS can be programmed to any pin(s) on the DUT load board through a buffer driver on the pin electronics card with a drive capability of ±100 mA, per pin. Also the DPS's can be connected directly to the load board to provide drive capabilities of ± 1 amp. Section 1.3.1 (Pin Electronics) provides complete specifications of the DPS when buffered and channeled through the pin electronics.

The DPS is programmable in two ranges and polarity. A third range is optional. Magnitude is contained in 10 bits, range is contained in 2 bits and sign is contained in 1 bit. The specifications of this section apply when the DPS's are brought to the test head through the load board rather than through the pin electronics.

Voltage Force or Voltage Trip

Range	Max Load	Resolution	Accuracy % of Value
1 ±0 to ±2.04V	± 1 amp	2 mV	***
2 ±0 to ±10.23V*	± 1 amp	10 mV	0.1%± 1
3 ±0 to ±40.92V*	± 1 amp	40 mV	0.1% ± 1 bit

Regulation: No load to full load ±20 millivolt**

Time Response: Settling to 1% in 1 millisecond
Overshoot 1% of step value change into resistive load

Current Trip Out: See DPT (Digitally Programmed current trip detector)

*Relative to chassis ground
**When force/sense is tied at the load board.
*** Range 1 is optional (see 1.2.6)
No voltage trip/current trip in range 1

The DPT is programmable in two ranges and acknowledges current flow direction according to the polarity of the Device Power Supply (DPS). The value of the trip level is stored in a 12-bit binary register.

Current Trip or Force

Range	Max Load	Least Significant Digit	Acurracy % of Value
Bit 11 = 1	0-1 amp (magnitude)	1 mA	±1.5% ± 2 bits
Bit 11 = 0	0-0.1 amp (magnitude)	0.1 mA	±1.5% ± 2 bits

Bit 12 = 1 indicates trip if current programmed value.

Bit 12 = 0 indicates trip if current programmed value.

Response Time: Tracks supply load with no greater than 1 microsecond delay. Trip is automatically inhibited for 3 ms during forcing changes.

Trip level activates system interrupt.

1.2.5 Precision Measurement Unit (PMU)

The Precision Measurement Unit (PMU) is an instrument which, under program control can be connected to an individual pin of the device under test (DUT) for the purpose of making a quantitative voltage or current measurement at that point. This unit is used for DC parametric or DC GO/NO-GO testing. The PMU is also capable of applying (forcing) a precise program, specified voltage or current to any desired pin of the DUT. In practice, these two operations are performed simultaneously; i.e., a voltage is applied, and a measurement is made of the resulting current flow, or, alternatively a current is forced, and the voltage is measured. The use of the PMU voltage clamp offers the user protection from over voltage due to programming errors, or voltage compliance problems.

The PMU can also be used to make a variety of internal measurements within the test system itself, such as measuring test head analog reference voltages and functional test voltages, as well as voltages at certain of the test points located on the printed circuit cards within the system. This is done automatically during system self-check under the control of diagnostic programs. Thus the PMU is also a trouble-shooting aid at the user's disposal for purposes of system maintenance.

The operation of the PMU is controlled mainly by the contents of four registers:

PPS (Precision Power Supply) register
DCT (DC Trip) register
PSL (Precision Sense Level) register
PA (Pin Address) register

The PPS register holds the information determining the value of the voltage (or current) to be forced. This includes polarity, range, magnitude, and whether the forced quantity is voltage or current.

The DCT Register is used to hold the information fed into a DAC which is part of the circuitry for the analog-to-digital conversion of the measured current (or voltage). When this conversion is made the measured quantity is contained in this register in digital form. Polarity, range, and magnitude information are also present.

The PSL register is used to hold the information establishing the operating range for voltage or current measurements by the PMU, and specifying whether it is indeed current or voltage that is to be measured. The PSL register also holds the information specifying voltage clamp values. These values are upper and/or lower limits on the allowable voltage at the PMU output; i.e., at the pin of the DUT. This provides protection for the device under test. For example, a programming error may cause the PPS register to specify a harmfully high voltage to be applied to the pin of the DUT. In this case the voltage clamp circuit, programmed with limit values held in the PSL register, provides the required compensation within the voltage feedback loop, so that the PMU output voltage does not violate these limits, and thus the device is protected.

The PA register holds the information controlling the connection of the PMU to the appropriate pin of the DUT or to the appropriate internal mode within the test system. The bits of the PA register are the pin address.

The PMU is a precision, digitally programmed, forcing and sensing unit with 10 bits for magnitude, 2 bits for range, 1 bit for polarity, and 1 bit for voltage or current. Maximum capacitive loading is 01.1μf. Recommended calibration check period is one month.

Voltage Clamp Table

PSL	Volts Low Range (PSL=0)	Volts High Range (PSL5=0)
4 3 2 1 0		
1 0 0 0 0	± 1.5	±3
1 0 0 0 1	± 4.5	±4
1 0 0 1 0	± 7.5	-15
1 0 0 1 1	±10.5	-21
1 0 1 0 0	-13.5	-27
1 0 1 0 1	-16.5	-33
1 0 1 1 0	-19.5	-39
1 0 1 1 1	-22.5	-45
1 1 0 0 0	-25.5	-51
1 1 0 0 1	-28.5	-57
1 1 0 1 0	-31.5	-63
1 1 0 1 1	-34.5	-69
1 1 1 0 0	-37.5	-75
1 1 1 0 1	-40.5	-81
1 1 1 1 0	-43.5	-87
1 1 1 1 1	-46.5	-93

Notes:

1. PSL4 = 0, no clamp
2. Voltage clamp values are with respect to TCOM.
3. The clamp values are slightly lower, if a small current is forced (less than 10 least significant counts of any current ranges).

1.2.6 2V/2mV RVS-DPS-PMU Option

The 2V/2mV optional capability on the Sentry provides increased voltage resolution for low voltage technologies (TTL, ECL, and I^2L). The optional 2V/2mV range is incorporated into the RVS and DPS, and the 1V/1mV range of the PMU is changed to 2V/2mV.

1.2.7 High Speed Controller

The circuitry that controls the digital data originating from the CPU memory is contained within the high speed controller.

The controller provides up to eight timing generators (two for strobe and six for clock and data timing); five generators are standard and may be used for clocks or strobes.

The basic system allows complete functional testing at a 5MHz data rate or a 10 MHz dat rate at either the wafer probe or final test level. The system also performs DC parametric testing (stress, leakage, continuity) at a rate up to 300 tests per second in addition to AC measurement.

The station controller provides the Precision Measurement Unit (PMU) which may be used for stress, leakage, parameter, and loading measurement and subsequent datalogging. The PMU is also the primary instrument for system self-check reference.

The station controller also provides up to 4096 bit local memory pattern depth for functional testing; the basic station controller provides 30 x 2048 bits and this is expandable to a maximum of 60 x 4096 bits.

10MHz pin electronics cards in each test station are required for operation 10 MHz. The standard test station can be operated up to 5MHz. The standard test station can be operated up to 5MHz or 10MHz with the 10MHz controller. The 10MHz controller provides enable latches which allow the system to continue testing after a "fail" and provides the accumulated pin failures at the end of a test cycle. Also an external sync capability is provided to allow testing of "self-timing" devices.

One test station controller is allowed per system. The controller may have up to two high speed test stations, and these test stations may be 5 or 10 MHz.

The high speed registers, local memory, PMU, and timing generators are multiplexed sequentially between the test stations. The test stations contain high speed driver switches and comparators which are to be connected to the DUT. Further, any pin in the test head has the capability to be programmed as:

REFERENCE VOLTAGE (RVS), 2V/2mV OPTION

The RVS is a programmable Reference Voltage Supply with 10 bits force magnitude, 2 bits for range, 1 bit for polarity.

Range	Forcing Range	Resolution	Accuracy (1% of programmed value)
1	0 to ±2.046V	2mV	.1% ±2mV
2	0 to ±10.23V	10mV	.1% ±10mV
3	0 to ±30.72V	40mV	.1% ±40mV

SYSTEM NOISE/REPEATABILITY: ±10mV max. (Allowed in Internal Node Check)

DIGITALLY PROGRAMMED POWER SUPPLY (D.P.S.), 2V/2mV OPTION

The DPS is a Programmed Power Supply with 10 bits for magnitude, 2 bits for ranges, 1 bit for polarity, 2V/2mV option (Range 1) is added to Voltage Forcing Mode only.

VOLTAGE FORCING

Range	Forcing Range	Resolution	Accuracy (% of programmed value)
1*	0 to ±2.046V	2mV	.1% ±2mV
2	0 to ±10.23V	10mV	.1% ±10mV
3	0 to ±40.92V	40mV	.1% ±40mV

SYSTEM REPEATABILITY/NOISE: ±10mV max. (Allowed in Internal Node Check)
*No voltage trip/current trip in RANGE 1

PMU SPECIFICATIONS

FORCE VOLTAGE/MEASURE CURRENT

Range	Forcing Range	Resolution	Rise Time* (10-90%) (All Measuring Ranges)	Accuracy (% of Programmed Value)	Overshoot* (% of Programmed Value) (All Measuring Ranges)
1	0 to ±1.023V	1 mV	100 μs	±.3% ±4 mV	< 15%
2	0 to ±10.23V	10 mV	200 μs	±.15% ±10 mV	< 5%
3	0 to -40.92V	40 mV	400 μs	±.15% ±40 mV	< 1%
4	0 to -102.30V	100 mV	600 μs	±.15% ±100 mV	< 1%

Regulation: No load to full load of the current range < ±40 mV/100 mA.

Leakage: The PMU measurement system leakage resistance shall not be less than 2000 MΩ to system ground at less than 50% relative humidity and 25°C ambient temperature at the station inlet (leakage current increases 0.5 nA/V). (Leakage error is additive to listed specifications.)

Tester Common: TCOM: -11V ± 3 mV

Repeatability: For 100 consecutive measurements, ±4 counts when forcing or measuring in the 1V or 1 μA ranges, ±1 count in all remaining ranges.

Range	Measuring Range	Least Significant Bit	Voltage Compliance	Accuracy*** (% of Measured Value)	TOPSY Required Measurement Delay** (in msec) Forcing Ranges 1/2/3/4 Typical Value	5 MHz Max Value	10 MHz Max Value
0	0 to ±1.023 μA	1 nA	-93.0V	±.5% ±10 nA	4/5/20/40	10/15/50/100	10/15/50/120
1	0 to ±0.1023 mA	0.1 μA	-93.0V	±.15% ±200 nA	0/0/0.5/1	0/0/1/2	1/1/1.5/3
2	0 to ±10.23 mA	10 μA	-93.0V	±.15% ±20 μA	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3
3	0 to ±102.3 mA	100 μA	-93.0V	±.2% ±200 μA	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3

FORCE CURRENT/MEASURE VOLTAGE

Range	Forcing Range	Least Significant Bit	Rise Time* (10-90%) (All Measuring Ranges) 1 (1V)	2 (10V)	3 (40V)	4 (100V)	Voltage Compliance	Accuracy*** (% of Programmed Value)	Overshoot* (% of Measuring Ranges) 1/2/3/4
0	0 to ±1.023 μA	1 nA	700 μs	5 ms	20 ms	45 ms	-93.0V	±.5% ±10 nA	20/5/3/3
1	0 to ±0.1023 mA	0.1 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±200 nA	20/5/3/3
2	0 to ±10.23 mA	10 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±20 μA	20/5/3/3
3	0 to ±102.3 mA	100 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±200 μA	20/5/3/3

Range	Measuring Range	Least Significant Bit	Accuracy (% of Measured Value)	TOPSY Required Measurement Delay**—ms Forcing Ranges 0/1/2/3 Typical Value	5 MHz Max Value	10 MHz Max Value
1	0 to ±1.023V	1.0 mV	±.3% ±4 mV	3/0/0/0	8/0.5/0.5/0.5	8/0.5/0.5/0.5
2	0 to ±10.23V	10 mV	±.15% ±20 mV	20/0/0/0	35/1/1/1	48/1/1/1
3	0 to -40.92V	40 mV	±.15% ±40 mV	80/2/1/0	130/6/2/2	190/6/2/2
4	0 to -102.30V	100 mV	±.15% ±100 mV	190/5/2/2	270/13/5/5	480/13/5/5

The measuring circuit will provide automatic down ranging to the range of best resolution when AUTO range is specified.

Programmable Clamp: Positive Clamp: -0.7V to +9V; Negative Clamp: +0.7V to -Vc; Symmetrical Clamp: ±Vc
Vc Programmable (see Voltage Clamp Table): ±10% ±1 V accuracy.

*With R_L = Voltage range/current range and slewing from 0 to 50% of the range.

**When forcing current Range 0/Range 1/Range 2/Range 3 or forcing voltage in Range 1/Range 2/Range 3/Range 4, respectively and slewing from 0 to 50% of the range and a resistive load equal to the voltage range/current range. This delay gives accuracies within 0.6% of full scale compared to the value measured in manual mode (static). The programmed delay is in parallel to a fixed hardware delay of about .5 msec.

***For longer delay (1 sec), ±.5% ±5 nA accuracy can be achieved on 1 μA range.

PMU SPECIFICATIONS, 2V/2mV OPTION

FORCE VOLTAGE/MEASURE CURRENT

Range	Forcing Range	Resolution	Rise Time* (10-90%) (All Measuring Ranges)	Accuracy (% of Programmed Value)	Overshoot* (% of Programmed Value) (All Measuring Ranges)
1	0 to ±2.046V	2 mV	100 μs	±.3% ±8 mV	< 15%
2	0 to ±10.23V	10 mV	200 μs	±.15% ±10 mV	< 5%
3	0 to -40.92V	40 mV	400 μs	±.15% ±40 mV	< 1%
4	0 to -102.30V	100 mV	600 μs	±.15% ±100 mV	< 1%

Regulation: No load to full load of the current range < ±40 mV/100 mA.

Leakage: The PMU measurement system leakage resistance shall not be less than 2000 MΩ to system ground at less than 50% relative humidity and 25°C ambient temperature at the station inlet (leakage current increases 0.5 nA/V). (Leakage error is additive to listed specifications.)

Tester Common: TCOM: -11V ±3 mV

Repeatability: For 100 consecutive measurements, ±4 counts when forcing or measuring in the 1V or 1 μA ranges, ±1 count in all remaining ranges.

Range	Measuring Range	Least Significant Bit	Voltage Compliance	Accuracy*** % of Measured Value)	TOPSY Required Measurement Delay** (in msec) Forcing Ranges 1/2/3/4 Typical Value	5 MHz Max Value	10 MHz Max Value
0	0 to ±1.023 μA	1 nA	-93.0V	±.5% ±10 nA	4/5/20/40	10/15/50/100	10/15/50/120
1	0 to ±0.1023 mA	0.1 μA	-93.0V	±.15% ±200 nA	0/0/0.5/1	0/0/1/2	1/1/1.5/3
2	0 to ±10.23 mA	10 μA	-93.0V	±.15% ±20 μA	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3
3	0 to ±102.3 mA	100 μA	-93.0V	±.2% ±200 μA	0/0/0.5/1.5	0/0/1.5/3	0/0/1.5/3

FORCE CURRENT/MEASURE VOLTAGE

Range	Forcing Range	Least Significant Bit	Rise Time* (10-90%) (All Measuring Ranges) 1 (1V)	2(10V)	3(40V)	4(100V)	Voltage Compliance	Accuracy*** (% of Programmed Value)	Overshoot* (% of Measuring Ranges) 1/2/3/4
0	0 to ±1.023 μA	1 nA	700 μs	5 ms	20 ms	45 ms	-93.0V	±.5% ±10 nA	20/5/3/3
1	0 to ±0.1023 mA	0.1 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±200 nA	20/5/3/3
2	0 to ±10.23 mA	10 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±20 μA	20/5/3/3
3	0 to ±102.3 mA	100 μA	110 μs	250 μs	500 μs	800 μs	-93.0V	±.15% ±200 μA	20/5/3/3

Range	Measuring Range	Least Significant Bit	Accuracy (% of Measured Value)	TOPSY Required Measurement Delay**—ms Forcing Ranges 0/1/2/3 Typical Value	5 MHz Max Value	10 MHz Max Value
1	0 to ±2.046V	2 mV	±.3% ±8 mV	3/0/0/0	8/0.5/0.5/0.5	8/0.5/0.5/0.5
2	0 to ±10.23V	10 mV	±.15% ±20 mV	20/0/0/0	35/1/1/1	48/1/1/1
3	0 to -40.92V	40 mV	±.15% ±40 mV	80/2/1/0	130/6/2/2	190/6/2/2
4	0 to -102.30V	100 mV	±.15% ±100 mV	190/5/2/2	270/13/5/5	480/13/5/5

The measuring circuit will provide automatic down ranging to the range of best resolution when AUTO range is specified.

Programmable Clamp: Positive Clamp: -0.7V to +9V; Negative Clamp: +0.7V to -Vc; Symmetrical Clamp: ±Vc
VC Programmable (see Voltage Clamp Table: ±10% ±1 V accuracy.

Capacitive Loading: .01 μf maximum.

*With R_L = Voltage range/current range and slewing from 0 to 50% of the range.

**When forcing current Range 0/Range 1/Range 2/Range 3 or forcing voltage in Range 1/Range 2/Range 3/Range 4, respectively and slewing from 0 to 50% of the range and a resistive load equal to the voltage range/current range. This delay gives accuracies within 0.6% of full scale compared to the value measured in manual mode (static). The programmed delay is in parallel to a fixed hardware delay of about .5 msec.

***For longer delay (1 sec), ±.5% ±5 nA accuracy can be achieved on 1 μA range.

1. Clock channel
2. Data input channel
3. Detector output channel
4. Bias or power supply channel
5. Input/Output channel

Digital Interface. The test station controller derives control information and data via the mainframe instruction register, multiplex control, and test station control (TSC) register.

Analog Interface. Analog buffers in the high speed test controller fan out the RVS and DPS voltages to up to two test stations where high speed driver switching between two voltage levels and output comparisons per pin are obtained within 4 inches of the DUT.

Pipelining. During functional testing, test patterns proceed synchronously through several stages of logic, such as local memory, formatter, pin electronics, strobe registers, etc. A sequencer controls the orderly flow of information through this pipeline. It controls startup and shutdown of test and ensures proper test execution in various modes such as external sync mode, match mode, etc. The operation of the pipeline in general is transparent to the user; timing relationships, strobe regions, mask and I/O changes etc., are not changed with changes in the test rate.

1.2.8 High Speed Registers

There are several high speed registers in the high speed controller sub group for control formatting and timing of local memory data input and output to the DUT. These registers provide selection of a per-pin basis.

DA/DB Registers. There are two I/O definition registers, DA and DB, which allow for changing of Input/Output definition of any DUT pin "on-the-fly"; i.e., at the programmed functional test rate.

MA/MB Registers. There are two mask definition registers, MA and MB, which allow for changing "care-don't care" conditions on any DUT pin "on-the-fly"; i.e., at the programmed functional test rate. A "care" condition enables a defined output pin (defined by DA or DB, or by I/O MODE) to be compared to the expected output state which is stored in local memory. A "don't care" condition disables a comparison of a DUT output with any expected value. These registers allow masking all outputs while the DUT is in some undefined state and then switching on the fly to the specified Input/Output definition once the device has been initalized.

Enable IMask allows the programmer to specify whether or not a pin in an input mode is an automatic "don't care." IMASK gives an alternate mask control saving local memory space since an I/O definition word also controls the mask and a corresponding mask definition word is not necessary for pins changing I/O mode.

I/O Mode. Independent of the DA/DB register definitions, pin W can have its I/O definition supplied by the F data (stored in local memory) of the pin adjacent to W. For this operation, the system operates in a mode called I/O MODE. This allows completely independent changing of the I/O definition of up to 15 pins with each test pattern. The I/O Mode for pin W can change within 50 nsec of T0 (test cycle start) or after a programmed delay depending on the timing generator programmed to the adjacent controlling pin.

When the system runs in this mode and a pin W is defined as an input pin, fail data on the pin are automatically disabled; i.e., for each test pattern that defines the pin W as an input, the device output seen at this pin is a "don't care".

I/O definition of pin W by pin X F data is done under control of the chaining register, in a fashion identical to the "Chain 2 Mode". "Chaining" and I/O Mode are mutually exclusive modes of operation.

I/O Mode 3. In the I/O Mode, the input/output definition of a pin is identical to the functional data of an adjacent controlling pin. In I/O Mode 3, the controlling pin's functional data controls the I/O definition of 3 pins. The list shows which pins can be controlling pins and which can be controlled pins.

Controlling pin	2	6	10	14	17	21	25	29	32	36	40	44	47	51	55
Controlled pin, in I/O Mode (Pin W)	1	5	9	13	16	20	24	28	31	35	39	43	46	50	54
Controlled pins in I/O Mode 3	1	5	9	13	16	20	24	28	31	35	39	43	46	50	54
	3	7	11	15	18	22	26	30	33	37	41	45	48	52	56
	4	8	12		19	23	27		34	38	42		49	53	57

Chaining. When a sequence of test patterns is executed in the Chain 4 Mode, each memory access generates four test patterns by using the memory data of the four chained pins in sequence and applying them to the surviving pin. Non-chained pins repeat the same test pattern four times. Example: if pins 5,6,7, and 8 are chained and pins 9, 10,11, and 12 are not, the memory word A generates the four patterns indicated in Figure 1-3b. The Chain 2 Mode generates two patterns from each memory word in an analogous fashion.

Pattern No.	Pin No. 5	9	10	11	12
1	A5	A9	A10	A11	A12
2	A6	A9	A10	A11	A12
3	A7	A9	A10	A11	A12
4	A8	A9	A10	A11	A12

Figure 1-3b. Chaining

In the Chain 4 and Chain 2 Modes, each chainable group of pins can either be chained or not chained, independent of all other groups. The 15-bit chaining register controls which groups are chained. The maximum number of Chain 2 pins is 15; i.e., 15 groups of Chain 2's. The maximum number of Chain 4 pins is 12; i.e., 12 groups of Chain 4's.

Chained "Surviving" pin	1	5	9	13	16	20	24	28	31	35	39	43	46	50	54
Pin chained to it in "chain 2" mode	2	6	10	14	17	21	25	29	32	36	40	44	47	51	55
Pin chained to it in "chain 4" mode	2	6	10	–	17	21	25	–	32	36	40	–	47	51	55
	3	7	11	–	18	22	26	–	33	37	41	–	48	52	56
	4	8	12	–	19	23	27	–	34	38	42	–	49	53	57
Rank	1				2				3				4		

Chain 2 or Chain 4 Mode is available if SIZE is 1024. Only Chain 2 Mode is available when 1024 SIZE 2048. When the size of the local memory has been defined by the FACTOR statement 'Set Page SIZE', then a mode bit is set to a '1' when the SIZE is 1024 and is set to a '0' when the SIZE is 1024. That means the length of the program cannot exceed the SIZE as specified regardless of the actual memory size of the system. Note: Chaining cannot be used with SPM.

MUX Mode. In the MUX mode, the waveforms of 2 pins, X and Y, are ORed together and appear on pin X. Pins X and Y come in 16 pairs.

Pin X	1	2	3	4	5	6	7	8	31	32	33	34	35	36	37	38
Pin Y	16	17	18	19	20	21	22	23	46	47	48	49	50	51	52	53

Address multiplexing means that both X and Y signals of an address appear on one line (or pin electronics) in a time-multiplexed fashion. For example, X0 - 1 appears on Pin 1 for the first 50 nsec and, 20 nsec later, the Y0 = 1 appears for 50 nsec on the same Pin 1. This means that in 120 nsec, an address (X0 = 1, Y0 = 1 in this example) has been presented to the DUT on one single line.

XOR Register. This register allows the data to an input pin to be exclusive ORed with TG data in order to apply worst case waveforms to the DUT.

RZ Register. This register defines whether an input pin operates in the RZ (return to zero) or NRZ (non-return to zero) mode.

Invert Functional Data Register. In the RZ or NRZ mode, functional data can be inverted on a per pin basis; thus the waveshape is converted to return-to-one in the RZ mode.

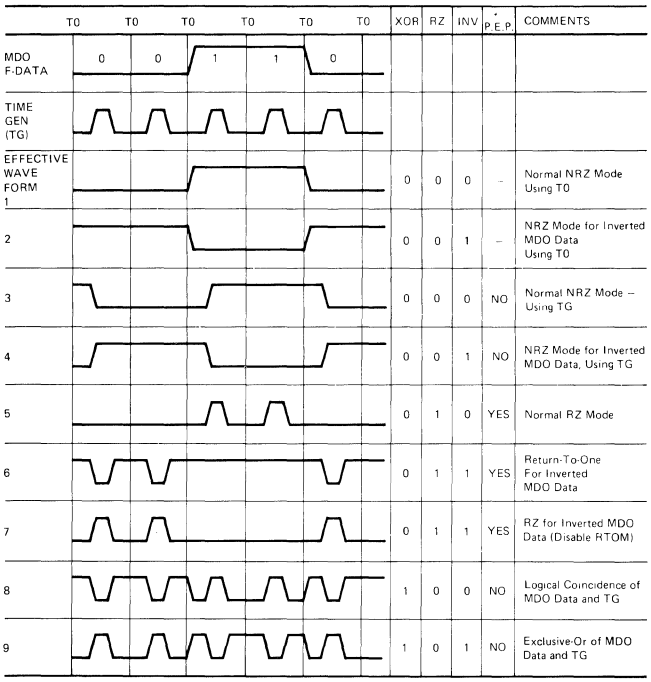
ST Register. This register allows for selection of one or two comparator strobe timing generators (TG7, TG8). Each timing generator is programmable for delay and width so that different outputs can be tested after allowing for different propagation delay times. It is possible to enable a double strobe also, whereby both TG7 and TG8 are used to control the periods when data is sampled.

TG1,2,3 Registers. These registers allow for selection of one of six timing generators, no timing generator (data appearing at T_0), or the "or" -ing of TG1 and TG2 for double pulse mode.

C Register. This register stores "FAIL" information based on comparisons between expected output values stored in local memory and the actual output value from the DUT. The register also shows which pin(s) "failed".

Additional Registers. In addition to the above registers, the controller has several

other registers which allow for selection of data/clock voltage levels, output comparison voltage levels, DPS select control, local memory address control, etc.



* P.E.P. = Pulse Exceeding Period Allowed

Figure 1-4. Waveforms

1.2.9 Local Memory Operation

Under normal functional test execution, functional testing proceeds by reading sequentially all local memory words from a start address S to a last address L. This may include looping back from L to address 0 (major loop), traversing this major loop N times. The test sequence may also include a minor loop between address J and K which is traversed M times. Addresses, S,J,K,L and counts M, N are programmable. Maximum count is 4096.

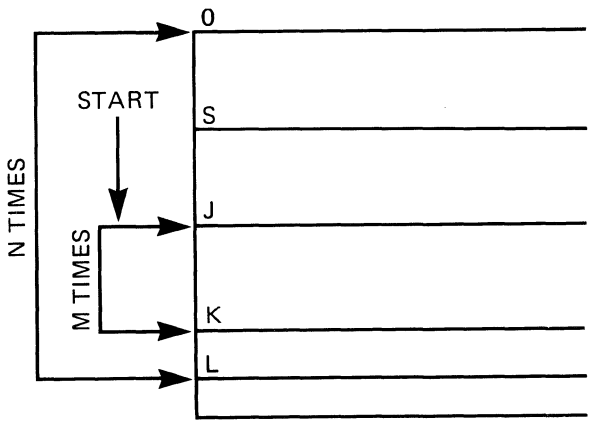


Figure 1-5. Major/Minor Loops

The tester will leave the normal test mode, generate an interrupt and become idle when address L is reached and major loop counter N is zero - this signals successful completion of a test - or when a test pattern fails and its address is larger than the address contained in the IF (Ignore Fail) register, signalling failure of a test.

Continuous Loop Mode. This mode is identical to normal test execution except that testing will stay continuously in either the minor or the major loop when it encounters them. Loop counters will not be decremented. While in the loop, the mainframe can read or write words in local memory. This mode is terminated under program control, by executing an ENABLE TEST MOMENTARY statement.

Momentary Mode. Execution of an ENABLE TEST MOMENTARY statement causes the continuous mode to terminate. When the minor loop K address is next encountered, test execution will proceed on to address K+1 rather than jump back to address J.

Match Mode. In this mode the tester stays continuously in the minor loop as long as each test generates a failure. On the first pass ("match") the test sequence branches to address Ø and leaves the match mode.

When in Match Mode, the test rate is constant throughout the entire functional test sequence; i.e., there is no Dummy Test Time. Minimum programmable period is 800 nsec. TG7 (Delay + Width) $\leqslant$ period - 600 nsec. During the 'search for match' only TG7 is enabled. TG8 is automatically disabled while searching for a match.

Sync Signal. A BNC connector supplies a sync pulse which is generated whenever a specified statement or local memory location is executed.

Enable Latches. Once this mode is entered and test enabled, functional test will not be terminated regardless of the number of failures which have occurred until local memory reaches location L. The C register stores failures of all pins during functional test and will not be cleared during the functional test. The C register may be cleared only if the DISABLE LATCH has been programmed and/-or it is followed by a functional test and

during the functional test no failure has occurred.

Enable Test Ifail. The External Sync Mode allows the Sentry System to perform Functional Test at a rate determined by the DUT. An external clock signal is brought into the Time Base via pin 1.

When external sync mode is programmed, the period must be in range ∅, and until the first functional data pattern appears at the DUT all timing generators will be disabled.

Logic levels of the External Sync signal must be compatible with other outputs on the DUT or level shifters are required at the Performance Board to provide the appropriate levels.

When Match Mode is not programmed, the minimum test period is 200 nsec.

External Sync Alternate. With External Sync Alternate, the timing generators are not disabled during the first functional test. This mode is for use with devices that give an external sync pulse at a known time, so that the period is not shorter than the delay or width of any timing generators which are programmed.

External Sync Match Mode. When the External Sync Circuit operates in Match Mode, the minimum test period is 800 nsec. Test data arrives at the DUT typically 560 nsec after the External Sync signal. For Match Mode, allowable programmed strobe time for Strobe 7 (delay + width) $\leq$ period -600 nsec (Figure 1-6).

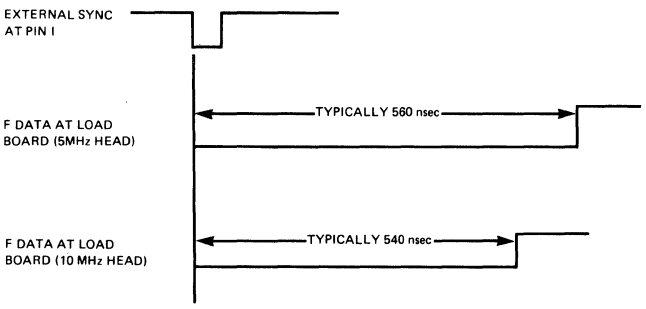


Figure 1-6. External Sync Timing

In this mode the tester stays continuously in the minor loop as long as each test generates a failure. On the first pass ("match") the test sequence branches to address ∅ and leaves the match mode. As long as the tester stays in a match mode, each test pattern is executed at a minimum rate of 800 nsec (Figs. 1-7 and 1-8).

1. Min. Period = 800 nsec
2. TG7 Delay + Width Period - 600 nsec
3. During "Search for Match", only TG7 is enabled
4. TG8 will be enabled immediately upon a match

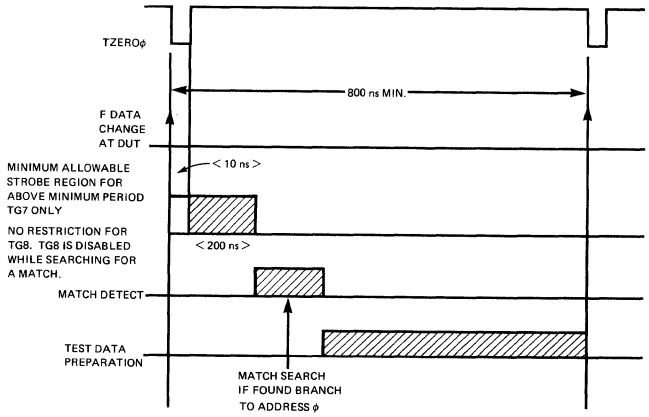


Figure 1-7. Normal Match Mode

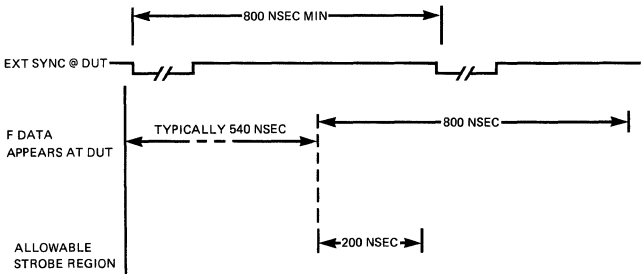


Figure 1-8. External Sync Match Timing

1.2.10 Timing Generators (TG'S)

Eight timing generators are available and provide synchronization and timing for single or multiphase clock devices. These TG's also provide fail strobe and data timing for functional testing. If no timing generator is programmed, the start of test period pulse (TO) is used for data timing.

Test Rate Period

100 nsec to 40 msec in four ranges

Pulse Width or Delay

10 nsec to 10 msec in four ranges
Resolution: $\pm$0.16 nsec (in Range 0)

		10 MHz	
	Range	Full Scale	Programming Resolution
Test Rate Period	ϕ	20 μsec	10 nsec
	1	400 μsec	100 nsec
	2	4 msec	1 μsec
	3	40 msec	10 μsec
Pulse width or delay	ϕ	10 μsec	0.16 nsec
	1	100 μsec	100 nsec
	2	1 msec	1 μsec
	3	10 msec	10 μsec

Conditions for above:
Pulse width $\leq$ period
Pulse delay $\leq$ period
Pulse delay + width $\leq$ 2 periods

Accuracy of Programmed Value
Maximum: 0.5 nsec

Strobes. For those generators used as strobes, the strobe window equals the duration of its programmed width (10 nsec to 5 msec). For 5 MHz test stations, the allowable strobe window is 20 nsec from the leading edge of TØ to 35 nsec from the completion of the period. For 10 MHz test stations, the allowable strobe region is 10 nsec from the leading edge of Tϕ to 10 nsec from the completion of the period. The above times exclude the use of I/O switching.

Double Pulse in RZ Mode. If a pin is in the RZ mode, and it is connected to "TG12" via the FACTOR program, the logical OR of timing generators TG1 and TG2 will be used as the effective timing input to this pin. See Figure 1-9.

Accuracy of Double Pulse Mode. Pulse rise and fall at DUT are delayed by 1 ECL gate ($\approx$2 ns) with respect to a reference frame established by Tϕ and all other timing generators.

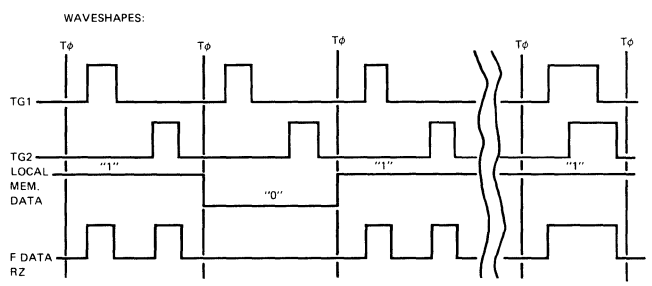


Figure 1-9. Double Pulse in RZ Mode

Pulse Exceeding Period. Use in conjunction with TG1 through TG6 only. If a pin is in the RZ mode it can be driven by a timing generator whose pulse delay + width exceeds one period (but is less than 2 periods). See Figure 1-10.

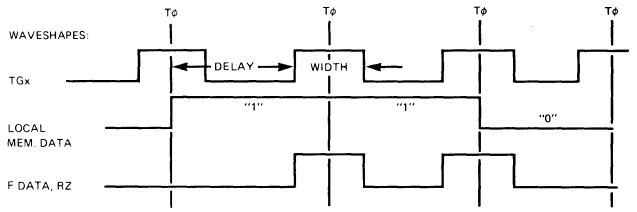


Figure 1-10. Pulse Exceeding Period

1.3 HIGH SPEED TEST STATION

Each test station (5 or 10MHz) contains a test head assembly with test head pin electronics. The pin electronics are the final link between the Sentry VII and the Device Under Test (DUT). Pin Electronics provide pin drivers and detector functions to each pin of the DUT and access to the DC testing and performance board.

The compact test head is designed for optimal device testing. Each pin electronics card is located in a "carousel" configuration that provides less than 4 inches of lead length to each DUT pin. The assembly will accommodate up to 30 pin cards to service up to 60 DUT pins. Each pin electronics card can function as data input driver, clock driver, device power supply, and data output comparator. Inputs can be switched to outputs within one data period; no pin swap boards are needed.

Test heads function with manual tests, wafer probers, or automatic device handler/chambers. This flexibility provides maximum device throughput with optimum data correlation between wafer test and final test.

1.3.1 Pin Electronics

The pin electronics circuitry is designed to function in any one of five possible modes completely under program control to provide the user a system that can be easily programmed to a specific application:

1. Data Mode
2. Clock Mode
3. Output Mode
4. Input/Output Mode
5. Power Supply Mode

Functionally the pin electronics receives two types of digital data. Low speed control data that establishes the modes of operation and high speed functional data that establishes conditions to be met in that particular mode.

In addition to the digital data, the pin electronics receives two types of analog data from the reference voltage supplies. The first type (E0, E1) establishes the "one" and "zero" logic levels that are to be forced in the clock and data modes. The second (S1, S0) establishes the voltage levels for sensing at the detector.

The pin electronics provides a forcing voltage to the element under test/or compares an output from the element with S1 or S0 reference and sends digital data that represents the results of the comparison back to the pin control II logic to be processed.

The pin electronics also provides a low impedance path to the pin for parametric measurements by the precision measurement unit.

A functional block diagram of pin electronics inputs and outputs is presented in Figure 1-11.

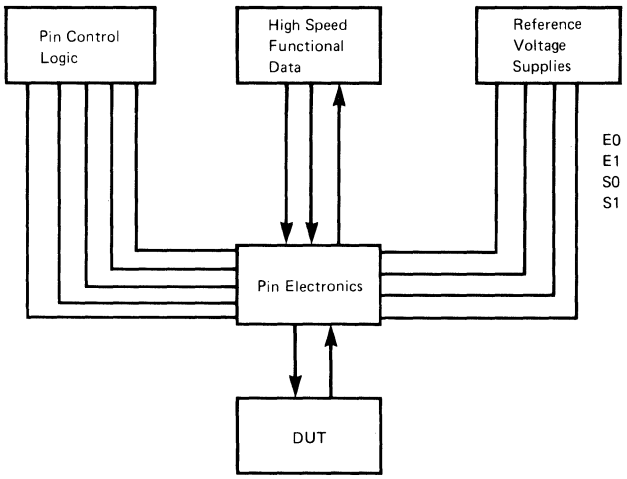


Figure 1-11. Functional Block Diagram of Pin Electronics Inputs and Outputs

DATA DRIVERS AND CLOCK MODES

Drivers: As measured into a standard of 1M in parallel with 50 pF* for data or 100 pF(for clock drivers, located three inches from the pin electronics output unless otherwise specified.

Output: 10 MHz: +6V to -16V (22V p-p).

Amplitude: 5 MHz: +6V to -30V (36V p-p).

Accuracy: 10 MHz: ±0.8% ±15mV (10V range), ±0.08%, ±25 mV (40V range) DC at 23°C ±1°C for 7 hours.
±75mV (≤ 3.75V signal) and ±2% (>3.75 V signal) relative to the steady state value at 50 nsec from start time of voltage slew into an impedance of > 1MΩ shunted by 10pF.* Steady-state is achieved ≥ 1 msec after starting time of voltage slew.

5 MHz: +-0.08% +25mV DC at 23°C ±1°C ambient for 7 hours.
±75mV (≤ 3.75V signal) and ±2% (>3.75-V signal) relative to the steady state value at 50 nsec from start time of voltage slew into an impedance of >1MΩ shunted by 10pF.* Steady-state is achieved ≥ 1 msec after starting time of voltage slew.

Resolution: ±10mV in low range (+6V to -10.23V)
±40mV in high range (+6V to -30V for 5MHz, +6V to -16V for 10MHz).

Stability: 10 MHz: For a change in ambient temperature of ±7°C from 23°C for a period of 30 days, the maximum drift is ±.1% ±15mV in addition to the accuracy spec.

*Load capacitance plus scope probe capacitance equals noted pF.

	5 MHz:	For a change in ambient temperature of ±7°C from 23°C for a period of 30 days, the maximum drift is ±.1% ±25mV in addition to the accuracy spec.
Reference Voltage Input:	Data Drivers: One of two pairs of reference supplies: E1, E0, EB1, EB0 Clock Drivers: One of two pairs of reference supplies: EA0, EA1, EC0, EC1	
Voltage Slew Rate:	10 MHz:	>1.5V/nsec at 20V p-p into 10 pF* in parallel with 1 MΩ . >1V/nsec at 20V p-p into 100 pF.* Measured at the 50% level.
	5 MHz:	Clock Mode. >1V/ns typical,. 7V/ns minimum for a voltage change of 30V, measured at the 50% point into a capacitive load ⩽200 pF.
	5 MHz:	Data Drive Mode. 1V/ns typical, .7V/ns minimum for a voltage change of 30V measured at the 50% point into a capacitive load of 100 pF on the acceptance test performance board.
Rise/Fall Time (10-90%)	10 MHz:	<10nsec at 5V p-p, <20 nsec at 20V p-p (10 pF* load).
	5 MHz:	Clock Mode. < 40 nsec at 30V p-p (10pF load, 20 nsec at 10V p-p (200 pF load). Data Drive Mode. 40ns at 30V p-p (10pF load) 20 nsec at 10V p-p (100 pF load).
Overshoot/ Undershoot:	10 MHz:	⩽100 mV at 5V p-p, ⩽300 mV at 20V p-p (10pF load).
	5 MHz:	Clock Mode. ⩽300 mV at 20V p-p with a 100 to 300 pF capacitive load. Data Drive Mode. ⩽300 mV at 20V p-p with a 10 to 200 pF load.
Minimum Pulse Width:	10 MHz:	20 nsec at 5V p-p (measured at the 50% points).
	5 MHz:	50nsec at 20V p-p (measured at the 50% points).
Skew:	10 MHz:	Adjustable to <±1 nsec on both edges at 5V p-p using common reference supplies. Measured with no load and at the 50% level.
	5 MHz:	±5nsec. This means a range of 10nsec or les between the slowest and fastest pin. Skew from pin to pin with E1 = 0, E0 = -16V for both edges measured at the -8V point with 10 MΩ ‖ 7pF load, TG1 used.
Source Resistance:	10 MHz:	47Ω ±6Ω for ⩽100mA DC in data mode. 30Ω ±5Ω for <100mA DC in clock mode.
	5 MHz:	50Ω max. for <100 mA DC in data mode. 33Ω max. for <100 mA DC in clock mode.
Load Current:	±100mA DC (data or clock mode), ±200mA peak for < 100ns.	

*Load capacitance plus scope probe capacitance equals noted pF.

Dissipation Limitation of Driver: 800 mW maximum.

I/O Switching: Switching from an input to an output or vice versa shall occur within 50 nsec at the beginning of the cycle (for data pins only).

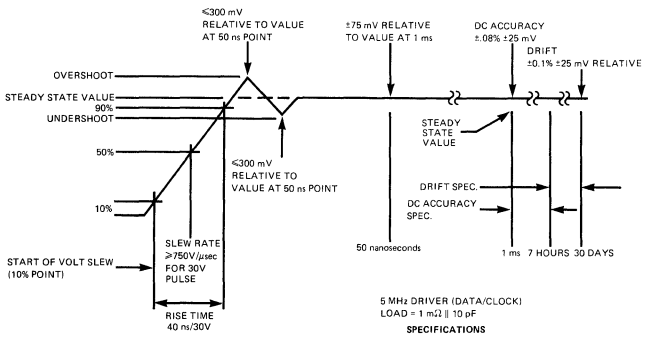


Figure 1-12. 5 MHz Data Drive Mode

COMPARATOR (10 MHz/5 MHz)

Input Amplitude: 10 MHz:+6V to -16V (22V p-to-p)
5 MHz:+6V to -27V (33V p-to-p)

Accuracy of Threshold Voltage: (10 MHz) +0.08% ±10 mV, (5MHz) ±0.08% ±30mV at 23°C ±1°C ambient for 7 hours.

Resolution of Threshold Voltage:
5MHz: 10mV in low range (+6 to -10.23V)
40 mV in high range (+6 to -27V)
10 MHz: 10mV in low range (+6 to -10.23V)
40 mV in high range (+6 to -16V)

Stability of Threshold Voltage: The maximum drift is ±.1% ±25mV (5MHz), ±1% ±15mV (10MHz) in addition to the accuracy specification, for a change in ambient temperature of ±7°C from 23°C for a period of 30 days.

Comparator Hysteresis:
10 MHz: ≤10 mV p-p (pin Electronics Board only).
5 MHz: ≤40 mV p-p typical about threshold level.

Capacitive Loading:
10 MHz: <25pF (typically 20 pF) as output only, <45pF (typically 40 pF) as an I/O in the output state (exclusive of load board) at 0V in.
5 MHz: <25pF (typically 17 pF) as an I/O in the output only pin, <35-pF as an I/O pin in the output state, exclusive of load board at 0V in.

Input Bias Current:
10 MHz: <100nA from +6V to -12V increasing monotonically to <2μA at -16V.
5 MHz: ≤5nA for +6V to -14V, ≤100nA for -14V to -20V, ≤1μA for -20V to -30V

Response Time (10MHz): For step inputs (tr < 1 nsec) from .5 to 5V, the propagation time through the comparator will increase by 3.5nsec when the reference voltage is changed from the 10% to the 90% level of the input signal.

Slew Rate (10MHz): >1.2V/nsec (negative going edge limitation only). Does not affect propagation time for input signals moving slower than 1.2V/ns.

Change in propagation time of one comparator with a change in input polarity or amplitude (10MHz): 10 MHz: <±2nsec measured with the reference voltage set to the 50% level of the inptut pulse for amplitudes between .5V and 20V p-p, except when slewing rate limited.

Skew among comparators for identical input: 10 MHz: <±2nsec, when the reference level is between 10% and 90% of the input signal for amplitudes between .5V and 20V.

*Load capacitance plus scope probe capacitance equals noted pF.

5 MHz: Skew between comparators from pin to pin measured with a voltage going from -16V to -14V, with the sense level at -15V, Source resistance equals 50 Ω. Measurement is made using strobe generator #7. ±3nsec - this means a range of 6nsec or less between the slowest and fastest pin.

Threshold Voltage Input: One pair of Reference Voltage Supplies S0/S1.

Protection: Safe input voltage: +11V to-23V (10MHz) or -34V (5MHz) relative to TCOM. Voltages outside this range are clamped by diodes at the driver and comparator provided the current is limited to < 200mA. No damage will occur if a pin is shorted to the chassis (+11V), to a voltage programmed through any other PE board, or to the PMU. DPSs, however, when wired directly to the load board can provide ±1 ampere. This is potentially damaging to the PE so in no case should a DPS supply be directly connected to a PE pin. In an output mode, no harm shall occur if a pin using an RVS source is shorted to the chassis (system ground) or a voltage of -45V relative to system ground.

Mask: Using an additional local memory channel, one of two mask registers can be gated with the comparator with each functional test. If the channel contains a 0, then mask register MA will be used, and conversely, if it is a 1, mask register MB will then be used. This allows up to two masks to be used for any given data channel and mask selection can change at the beginning of each test period.

Strobes: One or two strobe patterns may be selected by each pin. The strobe patterns have programmable width and delay. Also the strobes may be ORed together to create a composite strobe pattern. Failures may be detected any time during the strobe window.

In order to select a double strobe, Strobe B must be selected; therefore, some pins may be Strobe A and other the composite strobe pattern.

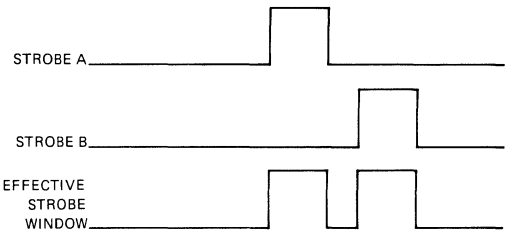


Figure 1-13. Strobe Patterns

Minimum Strobe Width: 10 nsec

Allowable Strobe Region:
- 10MHz: From 10ns after T_o 10ns before the next T_o for input signals with zero rise and fall times.
- 5 MHz: From 10ns after T_o to 35ns before the next T_o.

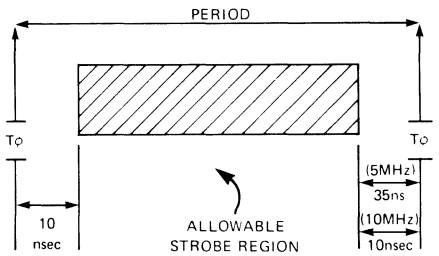


Figure 1-14. Allowable Strobe Region

POWER SUPPLY MODE

This mode uses the driver as a supply thus allowing the use of the DPS reference sup-

plies as bias (100 mA, steady state). The four available reference supplies are Tester Common, DPS1, DPS2, and DPS3.

Impedance:	3 maximum (typically 1)
Load Current:	100 mA
Format:	Input Pin
Voltage:	+6 to -30V relative to Tester Common (5 MHz test stations). +6 to -16V relative to Tester Common (10 MHz test stations).

The standard DPS supplies are brought to the test head and are available at the load board for connection to the Device Under Test when currents up to 1 amp or large positive voltage are required. Amplitudes of +51V to -29V relative to Tester Common (TCOM) are possible with this connection.

NOTE

The DPS supply output is offset from Tester Common by +11V when used directly at the test head (not via the pin electronics).

Reference Select Logic. Four for data driver*, E0, E1, EB0, EB1; two for comparators S1, S0; four for clock*, EA0, EA1, EC0, EC1; four for bias supplies/ground, DPS1, DPS2, DPS3, and TCOM.

*A data driver may be used as a clock driver by definition of the RZ register. A clock pin may conversely be changed into a data pin by definition of the RZ register.

I/O Switching. Provisions are made to allow switching (via spare local memory channel) from an input to an output or vice versa within 50 nsec, at the beginning of the cycle. Data pins only.

1.3.2 Interfacing Test Head

HANDLER INTERFACING

It is possible to interface the test head electronics to one of three types of handlers.

Wafer Prober -- up to 60 pins with provision for external components and pin routing
Manual or Automatic Package Handler
Environmental Automatic Package Handler

The modularity of the Sentry VII allows ease of interfacing the test head to any of the three above handlers or wafer probers, but specifications remain essentially a function of interface design. F.S.T. offers three logic interfaces as standard but will additionally consider and advise the customer or any handler or prober not included in the F.S.T. library.

PERFORMANCE BOARD GROUP

There are a number of performance board types available for interfacing the test station to the device under test.

Passive components may be connected to a device via the performance board to provide a load on the output. For certain device types, with open collectors, for example, a load is required for proper logic functioning. Active components may also be used for special pulse shaping or logically combining tester signals or other like purposes. Typically, passive or active components are connected to the relay side of the pin rather than the force side. The components may then be connected or disconnected under program control.

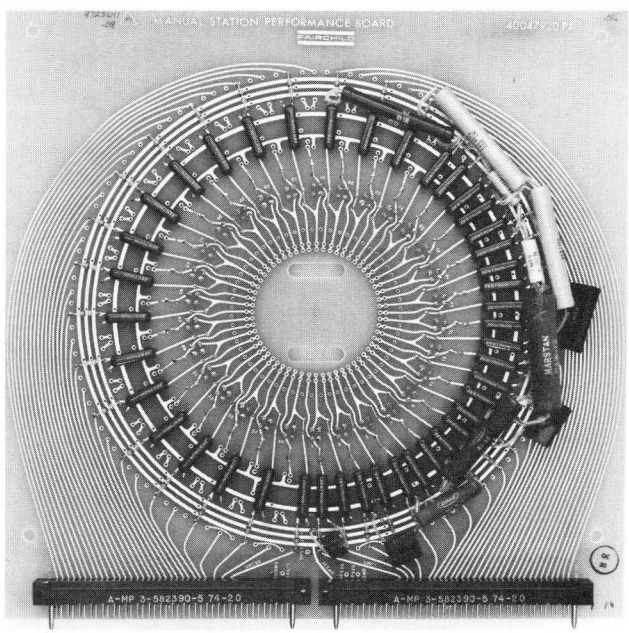


Figure 1-15. Solid Core Performance Board (Model 8345)

The solid center performance board is used for manual insertion testing. Typically this board is used to mount device sockets that are not of the Textool type. The perfor-

mance board artwork is designed to accommodate one relay for each pin of the tester. Individual control lines for each relay are provided which enable the user to load the device under program control.

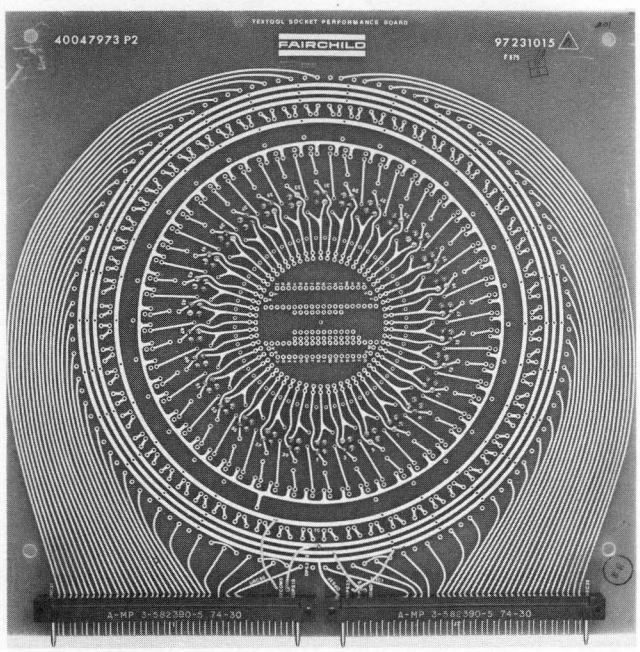


Figure 1-16. Solid Center Performance Board with Pin Patterns for Textool Sockets

This solid center performance board is also used for manual insertion testing; this board has the same functions as the solid center board described above with the addition of a pin pattern design that accommodates 14, 16, 18, 24, and 40 pin Textool sockets. Note: Textool is a trademark for test sockets.

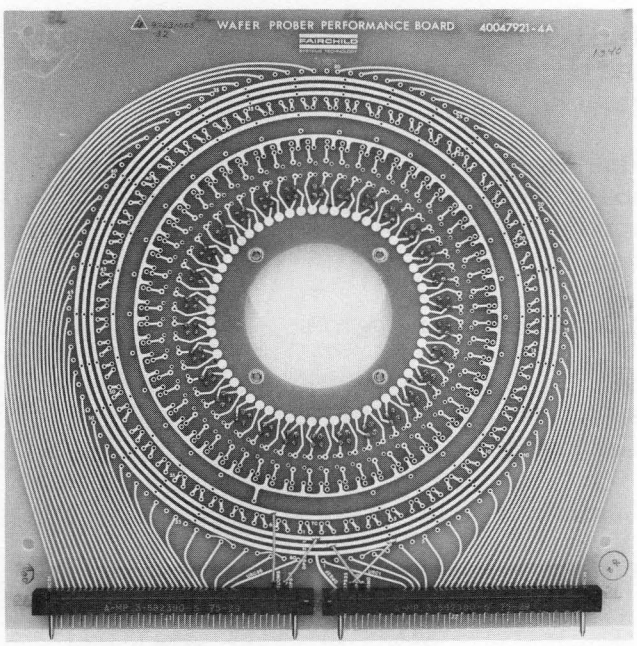


Figure 1-17. Hollow Center Performance Board

This hollow center performance board is used with automatic handling equipment where the test station carousel hinges away from the test fixture. Electrical contact is made between the performance board and probe card/contractor via a pinless contact ring (Figure 1-18). The hole in the center of the performance board allows the viewing of the wafer through optics centered above the test station carousel. When the test station carousel is positioned away from the handling equipment, a small device under test (DUT) circuit card can be mounted on the performance board for manual insertion testing. This performance board can often accommodate several devices by simply changing the DUT board for the device to be tested. (See Figures 1-10 and 1-20).

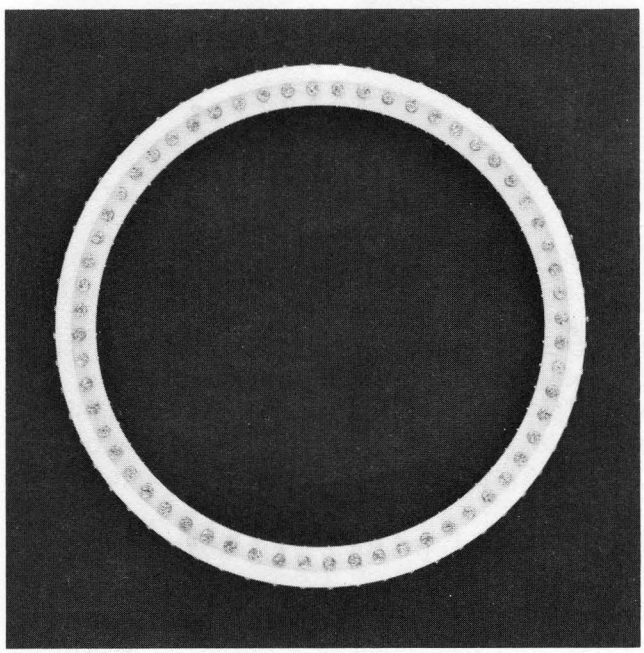


Figure 1-18. Pinless Contact Ring

The hollow center performance board artwork is designed to accommodate one relay for each pin of the tester. Individual control lines for each relay are provided which enable the user to load the device under program control.

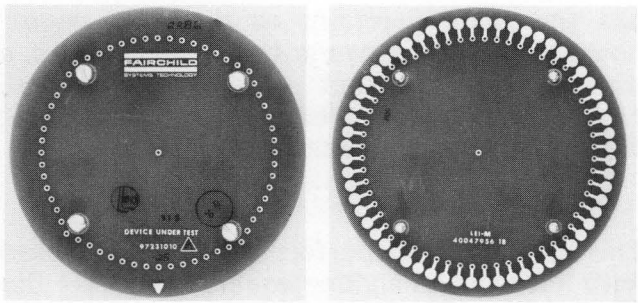


Figure 1-19. Blank DUT Board Top and Bottom

This printed circuit board is used with the hollow center performance board via the pinless contact ring. The hollow center performance board is to contain any sepcialized circuitry required. The user can drill the mounting holes for his unique socket and wire the socket to the appropriate DUT contact pads that have a one-to-one correspondence to the tester pins. A limited number of components can be placed on the DUT board itself.

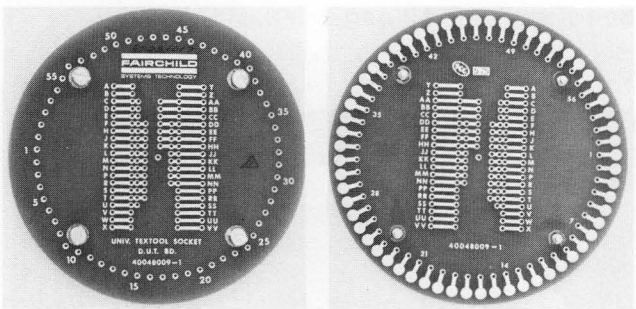


Figure 1-20. DUT Board With Pin Pattern For Textool Sockets Top and Bottom

This DUT board is used in the same manner as the blank DUT board described above. It provides the same functions with the addition of a pin pattern design that accommodates 14, 16, 18, 24, and 40 pin Textool sockets.

The universal performance board assembly for Sentry VII Test Head consists of two boards: a base board and a performance board. The electrical connection between the two boards is made with the pinless contact ring assembly. The ground connection between the two boards is made through four gold plated locating studs which are mechanically secured and soldered to the base board ground plane. The studs are offset to provide proper keying to the performance board. They also limit the height of pinless contact ring compression.

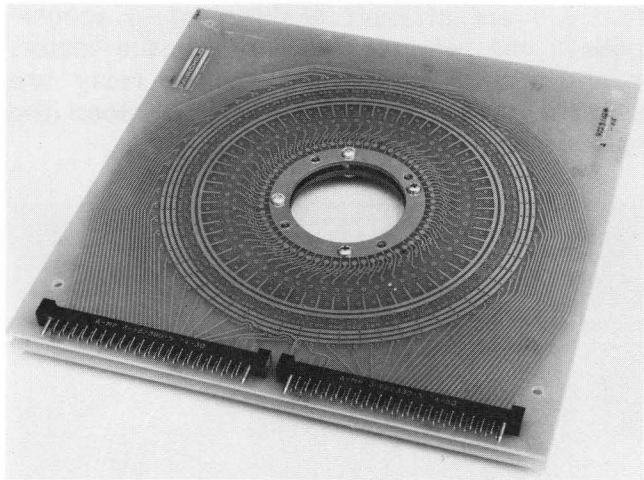


Figure 1-21. Universal Performance Board Assembly

The base board consists of four ground studs and connectors that mate with the Pin Electronics boards. In normal operation the base board is permanently installed on the test head and secured by the four thumb nuts. The pinless contact ring is located on top of the base board by three dowels. The performance board provides the same functions as the standard solid center performance board.

The only modification required for this operation is to increase the test station table top about 3/8 inch higher from the frame due to the added height of the extra board and pinless contact rings; this can be accomplished by a few special brackets.

The performance board adds typically 5 pF to the pin capacitance specifications from pin to ground.

The capacitance between pins without load board is 1.5 pF typical. The load board addition to the capacitance between pins is typically 1.5 pF.

1.3.3 Displays/Indicators

Each test station has sufficient controls/indicators to display the following information: (see Figure 1-22)

Controls

START	Initiates program execution
RESET	Stops program execution; resets the program, tester displays and registers

MANUAL (MAN)	Initiates Manual Mode in which one tester statement or instruction is executed each time the station START pushbutton is pressed
ADVANCE (ADV)	When in MANUAL mode, this switch initiates START pulse at a repetition rate of three per second
Indicators	
ON LINE	Indicates that particular station is enabled and has control
DC PASS/ FAIL	Indicates results of DC tests
DYNAMIC PASS/FAIL	Indicate results of functional tests
END OF TEST (E.O.T.)	Indicates end of test execution
EXTERNAL INTERFACE REG. (EIR)	Indicates contents of the ten least significant bits of the external interface register
POWER FAIL	Indicates when station and controller power is on. Flashes if a power failure occurs in any of the controller power supplies.

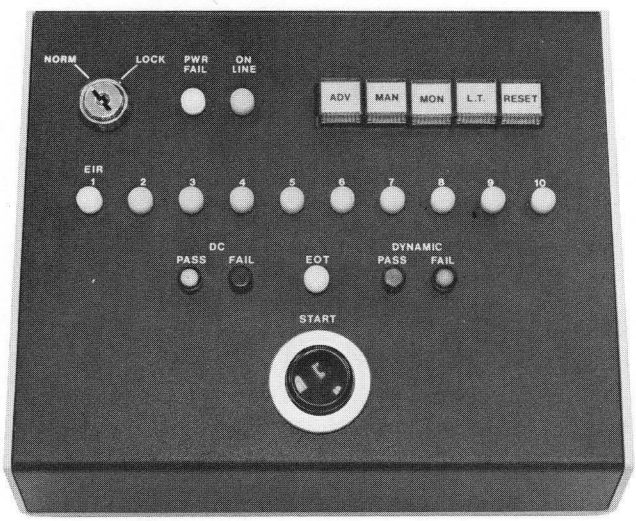


Figure 1-22. Test Station Control/Display Unit

1.4 SEQUENCE PROCESSOR (SPM) FOR SEQUENTIAL DEVICES

The Sequence Processor meets a large number of key requirements for testing modern complex devices and anticipates the needs for testing microprocessors, communications, and other devices which are evolving. The Sentry VII Sequence Processor provides enhanced capabilities for testing devices that require flexible input/output control of individual pins, long functional test patterns and sequences, high speed, and an absence of data breaks.

The ability to execute a large number of commands at a full 10 MHz data rate reduces the amount and hence cost of high speed memory required and greatly eases the quantity and cost of programming.

Local Memory is already capable of operating at up to a 10 MHz rate and of storing 4096 60-bit patterns of functional test and compare data. The Sequence Processor augments the Sentry High-Speed Local Memory by adding a control word to the Local Memory functional data word for memory address control, I/O control, and mask control.

Physically, the Sequence Processor is a multiprocessor with a high-speed TTL microcode store. The microcode store contains up to 4096 words of 16-bit microcode, and the multiprocessor has two other main sections: the address control section and the timing section.

The large number of Sequence Processor options for real-time control of I/O definition, masking, and timing eases application to different device classes; devices having wide I/O buses and variable I/O groups may be handled as easily as devices having fixed pin assignments.

The address control and timing sections of the Sequence Processor fetch and interpret the microcode command from Local Memory at the same time as a 60-pin wide field of functional and compare date is fetched from the Local Memory's functional data store.

1.4.1 Microcode Commands To Modify Test Pattern Sequence

Microcode commands allow efficient reuse and modification of data already in local

memory. Ordinarily, functional testing proceeds by reading sequentially all local memory words from a start address to a last address. This sequential test execution may be altered by the following microcode commands:

Clock Burst. A clock burst is basically a loop confined to one pattern at one memory location; this pattern is repeated a specified number of times. If the DUT requires repetitive data in its test sequence, the clock burst command is used. (SET FC n, where n is the number of times the test pattern is repeated.) Each functional pattern can be repeated up to 4096 times, and each clock burst is variable in count from one SET FC to the next.

Subroutine Call. Set F. . . . . - LCALL sub, where sub is the name of a subroutine, allows you to branch out of sequential order to a subroutine.

Subroutine Definition and Loop Count. Use of the subroutine loop is largely for execution of often-used sequences. Looping on a group of patterns is allowed in a subroutine loop and the loop will be traversed until the loop count is exhausted before the subroutine return is taken. A subroutine loop can be called from any portion of local memory and can contain any other patterns or commands, including other subroutine calls. In fact, subroutines may call subroutines and nest up to 16 levels deep.

LSUBR sub NORMAL n; SET F . . . . .; defines a subroutine called sub and says it is to be repeated n times; n can be 1 to 4096. (Normal indicates that this is a normal test, without match mode, continuous loop mode, sync mode, etc.)

The return address and loop count are stored in hardware push down stacks; thus, after completion of the requested number of subroutine loops, the tester returns to the next pattern in the sequence it was running before it branched to the subroutine.

Unconditional Jump. Unconditional jumps are a way of linking sequences in local memory. Because the jump-to location may be changed from the system CPU, the entire sequence may be reordered with one statement. In addition, jumps may be inserted under keyboard controls to allow looping for debug purposes. (SET F . . . . . — LGOTO label, where label is a local memory location.)

1.4.2 Microcode Commands to Modify Registers

Register load commands are part of the Sequence Processor for on-the-fly reassignment of pin I/O definitions, care/don't care masking, and pin timing.

Input/Output Definition. There are two I/O definition registers, DA and DB, which allow for changing the Input/Output definition of any DUT pin. Ordinarily, DA and DB are preloaded by the system computer and selected on-the-fly by the two extra control channels in Local Memory.

With the Sequence Processor, these registers may be controlled by using the function data field of Local Memory to load the I/O registers in response to a microcode command. LSET DA/DB . . . . is the microcode command to change DA or DB on-the-fly. In addition to selecting DA or DB on-the-fly, you can modify DA or DB at a 10 MHz rate (subject to cycle steal).

Care/Don't Care Masking Registers, MA and MB, can also be modified on-the-fly with microcode command LSET MA/MB *subject to cycle steal).

Waveform Control. The commands LSET XOR, LSET RZ, and LSET STROBE change the Exclusive- or, Return-to-zero, and strobe select registers on-the-fly. Because these functions are not pipelined (see Section 1.2.7) some care must be exercised in useage.

Pin Timing. The command LCGEN TGn allows reassignment of timing generators to pins on-the-fly. As with LSET XOR, this function is not pipelined and special rules apply.

1.4.3 Microcode Commands to Modify Testing

There are occasions when local memory data must be changed before it can be re-used. For this purpose, the multiprocessor uses its local memory alteration commands in conjunction with the system's invert functional data register. This invert register can invert functional data on a pin-by-pin basis. The invert register can be set on-the-fly by LSET.

Changes to the invert register can be done simultaneously with a subroutine call, thus causing the subroutine to produce different patterns each time it's called. In fact, the invert register may even be changed within the called subroutine. LSET IX changes the invert register and executes a test; LSET IX may have a subroutine call (LCALL) attached to it.

1.4.4 Microcode Commands to Modify Local Memory

CONTINUOUS LOOP MODE

There are two Sequence Processor instructions which put the system in a continuous loop; either instruction will inhibit all fails. LSUBR sub CONTIN n defines the start address of the continuous subroutine sub. When the loop count n is exhausted and ENABLE TEST MOMENT[1] has been executed, address control returns to the calling address plus one. With SET FC CONTIN, the F pattern is repeated continuously until the execution of ENABLE TEST MOMENT[1], which will then advance the local memory to the current address plus one.

While in the loop, the mainframe can write words in local memory; continuous loop mode allows alteration of Local Memory from the CPU memory without stopping Local Memory. When continuous loop mode is entered, a hardware function causes the start-up of the DMA channel from CPU memory, and alteration of Local Memory proceeds. This form of local memory alteration causes no timing disturbance in the test since testing is going on continuously during alteration.

Continuous Loop Mode is also beneficial to the user doing manual analysis.

1.4.5 Conditional Jump (Match)

A form of conditional branch or branch on match is appropriate when the device being tested cannot be initialized and legitimate testing can begin only when a particular output pattern or group of patterns appears. For example, the leading or trailing edge of some signal or a particular bit sequence must be found before testing can begin. In Match Mode, testing continues until the desired condition is found.

A match is defined as a test or a series of tests whose result matches an expected pattern.

With the Sequence Processor, matching may be done in any loop, either clock burst or subroutine. Thus it is possible to test devices which require repeated matching or which receive a certain input sequence during match.

In any type of match search, should the match not occur within the programmed loop count of the burst or subroutine, a hardware fail interrupt will be forced since the device is presumed inoperative.

Regular Match and Alternate Match. LSUBR sub MATCH n defines the start of a match subroutine. A match within the subroutine will cause a branch to the calling address plus one. If the expected pattern or patterns cannot be matched within the loop count n, the local memory controller will cause a hardware trip and set the fail flag.

SET FC MATCH n seeks a match by repeating the same F pattern to the DUT; n serves as a burst count beyond which the test sequence is terminated and fail interrupt is set. Upon a successful match, local memory address will advance to the next location.

With regular match mode, the test rate can be programmed up to 1.25 MHz. Alternate match mode can be done at the maximum speed of the machine (10 MHz) except that branching always lags the successful match by six extra cycles.

Sequential Match. A sequential match is defined by a desired pass/fail sequence. The Sequence Processor's match-to-a- sequence capability allows it to find leading or trailing edges without ambiguity and to find pulses of specified widths. SET Q XXXXXXXXXXXX is used in conjunction with the ENABLE TEST MATCH/AMATCH statement to search for a sequential match on a pass/fail pattern. The "search pins" enabled are defined by one of the mask registers. The pass/fail data is transferred after each test from the C register into the C-save register. When a match is found, the contents of C-save match the contents of the Q register and control is

[1] Momentary Mode

passed to the subroutine calling address plus one or the FC+1. The sequential match mode is reset when a sequential match occurs or by a SET Q 0.

IGNORE FAIL BY COUNT AND DATALOG

To create a full picture of device characteristics and failures, the Sequence Processor has ignore failure commands, commands that allow testing to continue after a failure. The count of failures to be datalogged can be up to 8,388,609.

DATALOG FCT m COUNT STATXX enables the datalogger to log failures until m+1 is exhausted or the test ends. Use of the DATALOGGER and the FACTOR command SET IFAIL N together allows the user to specify whether datalogging is to begin at a specific memory location, at a test sequence start location, after a specific number of local memory tests, or at the first local memory test.

Failures can be logged by local memory location number or by test sequence number. Because of the numerous opportunities to reuse Local Memory locations, the capture of fail information must receive special treatment; a failure at a particular memory location may not be of significance in itself. Therefore, provision has been made to log not only the memory location of a fail, but also the total test count since the initiation of the functional sequence. This feature allows the failure always to be pinpointed, even though it is deep within a complex sequence.

1.4.6 Manual Analysis With the Sequence Processor

Manual analysis is a software program that enhances the user's ability to debug his test plan with maximum efficiency.

SYNC ON N COUNT generates a sync pulse at the Nth test of a sequence. N must be between 0 and 37777777B. Under Manual Analysis, the user has the ability to read and write the following SPM registers:

Start Register (SA)
Return Address Register (RA)
Clock Burst Count (FC)
Loop Count Stack (LCS)
Loop Counter (LC)
Stack Address (STAM)
Ignore Fail Register #2 (IF2)

1.4.7 Sequence Processor Diagnostic (SPDG)

The diagnositc package supplied with each Sequence Processor Module is a system of assembly language and FACTOR programs to test all functions of the SPM. SPDG assumes that TVFY, the Sentry VII system diagnostic, has been successfully run.

SPDG is divided into nine tests. The operator may pause or loop on each or any detected error inside a test. At the completion of each test, a message is output to inform the operator whether the test passed or failed.

The first test checks for correct local memory terminations.

The second test contains six subtests to verify individual local memory commands; each of these subtests are run in both internal and external clock mode.

The third test, the clock burst test, causes local memory to execute a SET FC command and verifies the time to execute the command.

The fourth test causes the local memory processor to execute a program that nests 16 levels deep and exits on an error. When it exits, the contents of the stack, loop counter, and stack pointer are verified. If the results are correct, all ones, all zeroes, and two checkerboard patterns are flushed through the stack and loop stack.

The fifth test verifies loop entry and exit timing by causing local memory to execute a program that nests 16 levels and terminates normally. When the program terminates, a timer value is checked.

The sixth test verifies escape from continuous loop mode via the enable test momentary command. The test also verifies escape from a continuous clock burst.

The seventh test modifies local memory while the local memory processor is executing a continuous loop and verifies the contents of local memory upon termination.

The eighth test causes a series of clock burst commands to be executed in match mode with only the last one causing a match. At termination, the time and termination ad-

dress are checked. A match loop is executed next and the termination address checked. Finally, a sequential match is checked in normal and alternate mode. This test is run in internal sync mode and then in external sync mode.

The ninth test attempts to force errors by executing sequences of commands in XOR, MUX, IMASK, and AMATCH modes. Match mode is used with clock bursts, match loops, and sequential match loops. Inside these loops, the masks and I/O pin definitions are changed.

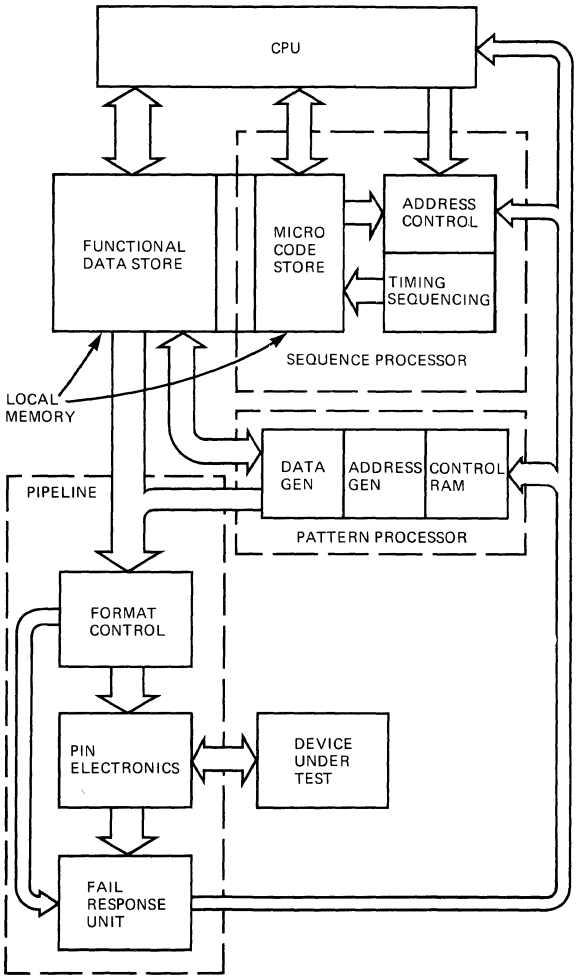


Figure 1-23. Sequence Processor and Pattern Processor with Local Memery and Pipeline

1.5 PATTERN PROCESSOR (PPM) FOR MEMORIES

The Sentry VII Pattern Processor was developed for evaluating large-scale memory chips with competitive cell patterns that must be fully verified and where each individual cell must be verified.

The Pattern Processor with the Sentry VII enables a memory device (RAM, ROM, shift register) to undergo pattern testing of its memory matrix, parametric testing of its DC characteristics, and additional functional testing from local memory all in one test sequence.

Physically, the Pattern Processor is a microprocessor. It has three high-speed ECL RAMs and six X- Y-coordinate registers. It works in conjunction with the Sentry VII Local Memory and fits into the testing pipeline.

The user controls and directs the Pattern Processor with microprograms. Each microprogram is accessed and executed from a FACTOR program (much like subroutines are called, except microprograms execute faster and more efficiently). Because the microprograms are separate, name modules, the same microprogram can be called from several FACTOR programs for efficient use of system resources.

Utility programs like CREATE, DELETE, EDIT, and FDUMP (all part of DOPSY utility software) simplify microprogram creation for the user.

Even though microprograms are initially stored on the disc, they are accessible quickly because up to ten microprogram modules may be stored in the FST-2 core memory and quickly transferred via DMA to the Pattern Processor when needed.

The user writes microprograms with three types of programming instructions:

Assembler Directives
Definition Instructions
Microinstructions

1.5.1 Assembler Directives

Assembler Directives give the Pattern Processor Assembler information for converting a source microprogram into a microprocessor executable program.

Directive	Mnemonic
Define an address generator block	AGEN
Define a data generator block	DGEN
Define the end of program file	END
Define the start of a program module	PGMID

1.5.2 Definition Instructions

Definition instructions are used to initialize the registers which are used to perform pattern testing; the instructions provide the set-up information necessary for execution of the microprogram.

Instruction	Mnemonic	
Load Hold Register pair	HLDm	(Xm), (Ym)
Load Delta Register pair	DELm	(Xm), (Ym)
Load Maximum Register	MAX	(XMAX), (YMAX)
Load Refresh Count Register	RFC	integer
Load Chip Select	CSEL	integer
Load Storage Address Register	ORG	integer
Load Shift Data Register	SHFD	integer
Load Data RAM	DATA	n1,n2,n3,n4
Load Topological RAM	TOPO	(X),(Y)
Load Mask for X coordinate	MASKX	integer
Load Mask for Y coordinate	MASKY	integer
Disable/Enable Data Extension	DEX	0/1

The Pattern Processor has ten registers for X and Y. Three holding registers are for the initial X- and Y-values, (three values each). Three delta registers contain the amount by which X and Y are to be incremented or decremented. One limit register holds the maximum X and Y values, the values that define the size of the memory under test. Three index registers are the working registers for X and Y values.

1.5.3 Microinstructions

There are two types of microinstructions: address generation and data generation. The Pattern Processor's highspeed ECL Control RAM stores these microinstructions, and each 44-bit word in the Control RAM is either an address generator word or a data generator word.

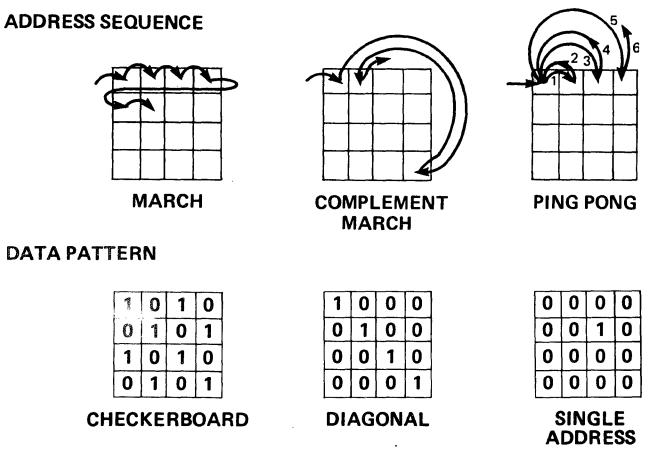


Figure 1-24. Major Attributes of a Memory Test Pattern

The microword eliminates pattern generation overhead, and the result is decreased test time and increased throughput, fewer program steps and lower programming costs, and pattern generation flexibility.

The Control Ram is 64 words long, and microprograms big enough to handle today's memories take but half of the microprogram space available in the Control RAM. The PPM can handle a memory with up to 16 9X,8Y address lines, 18 data in lines, 18 data out lines, a read control, a write control, 3 power supplies, and four chip select lines at a 100ns cycle time (10 MHz test rate).

ADDRESS GENERATION

Address generation instructions define and control the execution of a sequence pattern. They update the coordinate registers, execute read-write operations on the memory under test, compare coordinate registers, and control the execution sequence by branching.

In a microword coded to generate an address one microword can perform 20 operations simultaneously: specifying a branch condition, a branch address, read, or write; enabling or disabling chip select; inverting data; incrementing, decrementing, or loading any one or all of the three pairs of X and Y registers; and determining which of the three pairs of X and Y registers is to be applied to the DUT and also to be used as the address from which the Data In and Data Out are generated.

Address generation flexibility comes, in part, from the Pattern Processor's six registers for storing X- and Y-coordinate values. The independence of the set of X-coordinates and the set of Y-coordinates from each other greatly simplifies programming array-oriented patterns, and the three pairs of X- and Y-coordinate working registers greatly increase the addressing combinations in a pattern test sequence.

Patterns like the "Butterfly" are easily implemented on the Pattern Processor because of the independent X- and Y-addressing. In the Butterfly, each test cell is surrounded by a spiral address sequence. After traversing all X- and Y- address sequences, the test cell is moved typically along a diagonal.

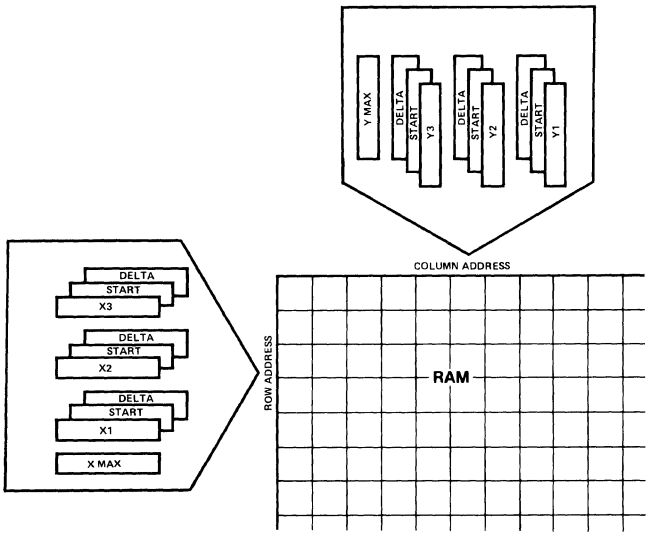


Figure 1-25. Address Generation Registers in the Pattern Processor

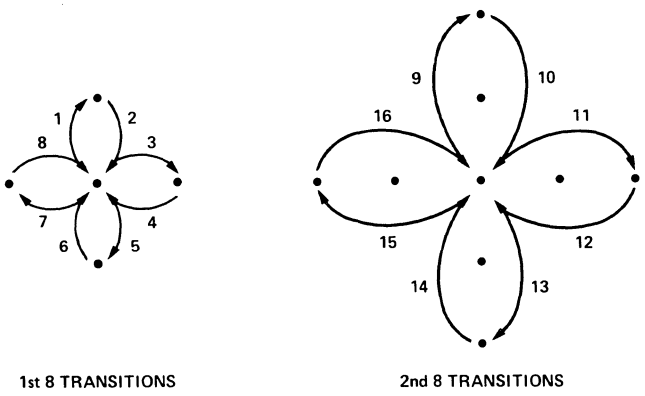


Figure 1-26. The "Butterfly" Pattern, Showing the First 16 Address Transitions

The following address generator instructions directly control the X-Y register values:

Instruction	Mnemonic	
Increment index register by	INC	Xm
delta value	INC	Ym
Decrement index register by	DEC	Xm
delta value	DEC	Ym
Load index register with	L	Xm
holding value	L	Ym

Address generation flexibility can also be seen clearly in the read-write operations.

For instance, W writes a data pattern into a cell of the memory under test. The location of this cell is indicated by the coordinate values (Xm, Yn) in the working registers. WI writes the binary complement of a data pattern into the cell indicated by the coordinate values in the working registers. Not only can the user write the binary complement of the data pattern, he can also write into the location defined by the binary complement of the X- and Y-values (-Xm, -Yn) in the working registers.

Instruction	Mnemonic	
Write	W	±Xm, ±Yn
Write Invert	WI	±Xm, ±Yn
Read	R	±Xm, ±Yn
Read-Modify-Write	RW	±Xm, ±Yn
Read-Modify-Write Invert	RWI	±Xm, ±Yn
Operate	OP	±Xm, ±Yn
Operate Invert	OPI	±Xm, ±Yn

Split-cycle timing allows intermixed read, write, and read-modify-write cycles without timing compromise. Split-cycle timing lets the system user test read cycles to stringent limits. ENABLE SPLIT is a FACTOR statement that enables tests to be executed at the APERIOD (Alternate Test Rate) during the read cycle. This alternate test rate can be 100 nsec to 40 msec. The alternate timing generator (ATG4) is used with the alternate test rate during non-write cycles.

The capability to split test rate and pulse width between read and write test cycles - i.e., to use different values - enables the user to test memories with different read and write cycle times without trying the test to the longer cycle. Moreover, cycle splitting is done on-the-fly.

In conjunction with register changing and binary complement capabilities, address generator words also are capable of comparisons, branching, ship selection, and programmable refresh.

Instruction	Mnemonic	
Compare Equal (fld1)=(fld2)	CE	fld1,fld2
Compare Greater than (fld1)>(fld2)	CG	fld1,fld2
Disable/Enable Chip Select	CHPS	0/1
Disable/Enable Refresh	RFEN	0/1

CE and CG compare the contents of one register to another. If equal, CE sets a hardware indicator to "true." If the first is greater than the second, CG sets a hardware indicator to "true." These "trues" could trigger a branch to elsewhere in the program.

CHPS enables or disables chip selection; when enabled, memory testing is confined to memory devices with the proper chip select combination.

Asynchronous/Synchronous Refresh Timing. The size of the refresh interval is set by a definition instruction as a multiple of 10 usec and can be set from 10 usec to 650 msec. The refresh counter counts asynchronously with the test rate. The pattern program proceeds in its own sequence until a refresh interrupt occurs at which time a programmed refresh pattern sequence may be executed. RFEN enables or disables the programmable refresh interrupt. When enabled, refresh is allowed at any point in the pattern. A synchronous refresh may be simply programmed and executed at the desired time by using a subroutine call.

TOPOLOGICAL SCRAMBLER

The second RAM in the Pattern Processor is the 256 words by 16 bits Topological RAM. For memories where device pin order and array location aren't one-for-one, the Topological RAM stores address scrambling data to make your test sequences what you want them to be; i.e., the Topological RAM translates a generated address to the actual geometrical address on the DUT. The Topological RAM is loaded via TOPO X-data, Y-data where x- and y-data are positive values and less than 377 (octal). To use the Topological Scrambler (RAM), the simple instruction SCRM 1 enables and starts the process. Note that, even though data patterns are generated as a function of address, they are independent of the initial address sequence and, thus, the user can scramble the x- and y-coordinates and leave the patterns intact.

DATA GENERATION

Data generation instructions are used to define and select data patterns in one of three ways:

- Selecting one of 15 different data equations without requiring software intervention.
- Using the Data RAM for logic combinations of selected data equations
- Using the Shift Data Register in repeating mode or to generate pseudo-random data.

Data Equations. There are four sets (from 0 to 3) of hardwired data equations in the Pattern Processor. The user can select a data equation (DE) or a data equation with its outcome inverted to its binary complement value (IDE). The basic equations selectable under program control are shown in Figure 1-29.

Each set corresponds to one of the four primary data channels to the memory under test (via the pipeline). If, for example, the user is testing a 256 x 4 memory, he can program a different data pattern into each of the four channels of the memory under test. (Figure 1-28.)

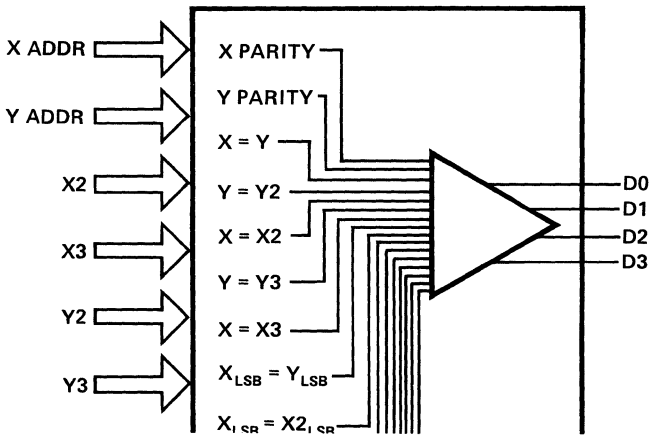


Figure 1-27. Generation and Selection of Data Equations

Logic Combinations of Data Equations. The Pattern Processor Data RAM extends the basic data generator by providing the capability of making any logic combination of the basic equations listed in the preceding table.

For example, the equation $X = X_2$ represents a single row bar at the programmed value of X_2. The equation $X = X_3$ represents a single row bar at the programmed value of X_3. (Note that both X_2 and X_3 are changeable under program control at test speeds without breaks in testing.) With the Data RAM, the user can program the equation $(X = X_2) + (X = X_3)$ which is a double row bar.

Combinations of up to four logic equations can be accomplished with the Data RAM; i.e., combinations like (Equation 1) + (Equation 2) · (Equation 3) + (Equation 4).

Select-Number	DE0	DE1	DE2	DE3
0	(X Parity) XPAR	(Y Parity) YPAR	(Diagonal) X=Y	(Checkerboard) X=YL
1	(Diagonal) X=Y	(Diagonal) X=Y	X=X2	(Row Bar) X=X2L
2	(Spiral) X=Y+X2	X=X2	Y=Y2	(Column Bar) Y=Y2L
3	X=X2	X=X3	SHIFT2	SHIFT3
4	X=X3	Y=Y2		
5	Y=Y2	Y=Y3		
6	Y=Y3	0		
7	(All Zeros) 0	SHIFT1		
8	(Y Parity) YPAR			
9	(Checkerboard) X=YL			
10	(Row Bars) X=X2L			
11	(Column Bars) Y=Y2L			
12	(Row Bars) X=X3L			
13	(Column Bars) Y=Y3L			
14	(One Pattern) (X=X2) • (Y=Y2)			
15	(Random Pattern) SHIFT0			

Data Generation Instruction		Mnemonic
Normal Data Equations	DEn	select-number
Invert Data Equations	IDEn	select-number
Select subfield in Data RAM	RMUX	integer (0 to 3)
Enable/Disable Data Shifter	LSHFT	1/0
Enable/Disable Random Mode	RNDM	1/0
Enable/Disable Data RAM	DRAM	1/0
Enable/Disable Topological Scrambler	SCRM	1/0
Reset Hardware FLAG and Invert Data	RST	
No (Null) operation	NOP	
Halt and branch to own address	HALT	

NOTE: The X and Y are the working registers.

L means that the least significant bit of the working register is compared to the least significant bit of the specified register.

Figure 1-28. Data Equations

The Data RAM is implemented with four 16-word by 4-bit memories that are user-programmed to create the desired logic combinations. Programming is accomplished via a definition instruction: DATA (n1),(n2),(n3),(n4) where n1, n2, n3, and n4 are four-bit octal numbers that load into the respective 16 x 4 bit RAM memories.

To load the Data RAM, an ORG statement positions the Storage Address Register to the desired word in the RAM; DRAM enables access to the Data RAM; and the RMUX instruction specifies which of the four-bit patterns is desired.

Use of the Shift Data Register allows deviations from the hardwired data equations. Data generation via the Shift Data Register provides repeating or pseudo-random patterns.

LSHFT 1 enables the Shift Register. If, with the RNDM instruction, the user selects operation mode 0, the shifter generates data that repeats every 16 cycles. This is done by the end-around shift of the contents of the 16-bit shift register with each bit being shifted one place from lowest to highest order bit.

If the user selects RNDM mode 1, the shifter generates pseudo-random data that repeats every 2^{16} -1 cycles. Each bit is shifted one place as before. Then Bit 0 is inverted and Exclusive-ORed with Bit 15. The resulting binary value is held as reserve to be shifted into the lowest order bit for the next data pattern generation.

BRANCH INSTRUCTIONS

Branch instructions alter the execution sequence of the microprogram loaded into the Control RAM. They can be part of either an address or a data generator word and give the user even greater flexibility in altering test sequences and patterns.

Instruction	Mnemonic
Branch on True	BT label
Branch on Not-True	BNT label
Branch and save return	BSR label
With BSR, the current Control RAM address plus one is saved in the Return Address register; then an unconditional branch is executed to the location specified in the instruction.	
Branch return	BRT label
Branch unconditional	BRU label
Branch on FLAG	BOF label

1.5.4 Manual Analysis

Manual Analysis of the memory under test is facilitated by five key commands: PAUSE, STOP, LOOP, READ, and WRITE.

STOP, in conjunction with PAUSE, stops testing within a specific microprogram at a particular location in the Control RAM.

The LOOP command allows looping between address 0 of the Control RAM and the address specified in the loop command.

READ allows the specified tester hardware register to be read and displayed immediately or at the next station pause. WRITE causes the tester hardware register specified to have the data written into it immediately or on the next station pause.

1.5.5 Datalogging

The DATALOG command collects and reports memory failures in the memory under test.

/. DATALOG FCT m COUNT STATXX

Where m is the additional number of failures (besides the very first one) to be datalogged and where COUNT specifies that failures are datalogged by the test count of the tests that failed (rather than by datalogging failures by the local memory addresses a which the failures occurred); m can be as large as 8 million.

The printout for memory failures includes the statement number which initiated PPM operation; the test count of the test that failed; the X-coordinate value of the failure location in memory under test; the Y-coordinate value of the failure location; the failure data in binary; the expected data in binary; the function (type of test executed) that caused the failure (R or RW); and the value of the chip select enabled.

1.5.6 Pattern Processor Diagnostic (PPOD)

The diagnostic package supplied with each Pattern Processor is composed of eight sub-programs to verify the Pattern Processor. Execution of PPOD assumes that the system has passed all tests in TVFY, the Sentry VII system diagnostic package.

The user can use PPOD three ways:

- Auto-execution of the entire verification with a printed system status.
- Individual-execution of each sub-program.
- Burn-in/repeated execution of the entire verification sequence at a requested repetition rate.

Console switch options give the diagnostic user even greater control, allowing halting on failures, cycling current tests, even walking through the sub-program step-by-step.

FUNCTIONAL PPOD SUB-PROGRAMS

- Register read/write test
- Control RAM memory test, including:
  RAM counter increment test,
  RAM reset test,
  Read/write test, and
  Walking 1 test (address Test).

- Address generator test, including:
  Stop address test,
  Index data transfer test,
  Index delta transfer test,
  Index compare/branch test, and
  Subroutine/flag branch test.

- Data generator test, including:
  Checkboard walk test and
  Chip select and X/Y mask test.

- Data out test

- Alternate TG4/Period delay and width test

- Topological RAM memory test, including:
  RAM Counter Increment Test,
  RAM Reset Test,
  Read/Write Test, and
  Address Test

- Data RAM memory test, including:
  RAM Counter Increment Test,
  RAM Reset Test,
  Read/Write Test, and
  Address Test

TESTER PIN ASSIGNMENTS (FIXED)

Pin	Function	Pin	Function
1	XO	31	DI4 (=0)
2	X1	32	DO4 (=0)
3	X2	33	DI5 (=1)
4	X3	34	DO5 (=1)
5	X4	35	DI6 (=2)
6	X5	36	DO6 (=2)
7	X6	37	DI7 (=3)
8	X7	38	DO7 (=3)
9	Write (selects test rate and timing generator)	39	DI8 (=0)
10	Read	40	DO8 (=0)
11	DI0	41	DI9 (=1)
12	DO0	42	DO9 (=1)
13	DI1	43	Spare
14	DO1	44	Spare
15	CS1	45	DI10 (=2)
16	YO	46	DO10 (=2)
17	Y1	47	DI11 (=3)
18	Y2	48	DO11 (=3)
19	Y3	49	DI12 (=0)
20	Y4	50	DO12 (=0)
21	Y5	51	DI13 (=1)
22	Y6	52	DO13 (=1)
23	Y7	53	DI14 (=2)
24	CS2	54	DO14 (=2)
25	CS3	55	DI15 (=3)
26	CS4	56	DO15 (=3)
27	DI2	57	DI16 (=0)
28	DO2	58	DO16 (=0)
29	DI3	59	DI17 (=1)
30	DO3	60	DO17 (=1)

NOTE: Pins 31-60 can be used as data pins for memories with up to 18 data lines by enabling Data Extension.

SECTION II

SYSTEM SOFTWARE

2.0 SYSTEM SOFTWARE

Software is at the heart of any test system, and Fairchild has devoted a large amount of its total manpower and capital resources to develop powerful and highly usable software in support of Sentry hardware.

A substantial portion of this resource is dedicated to the established customer base, over 350 Sentry users. Fairchild recognizes that software deficiencies will exist in any software package. To overcome deficiencies, Fairchild regularly issues new revisions of the software, enhancing system versatility and correcting any known deficiencies; we welcome customer feedback.

2.1 SYSTEMS SOFTWARE

Systems software is the internal set of resident programs and procedures. The Sentry VII system software is disc-resident until the desired routine is called automatically or by the operator from the control console (the Prime Input Device at that time).

Systems software is used by the central processor to control the system hardware elements and associated peripherals, the test program sequences, the test data, and and the files themselves.

Information flow between the major system elements is illustrated in Figure 2-1. In addition to the standard peripherals, a Communication Link and General Purpose Instrument Port are included.

The General Purpose Instrument Port is compatible with the IEEE/488 - 1975 Standard Digital Interface for Programmable Instruments. Sentry utility software provides a convenient means for programming up to 15 instruments.

The Communications Link is RS232C Compatible with Baud Rates up to 9600. The Sentry System Software is designed using a Message and Line Protocol including error detection, which links the Sentry to the Fairchild INTEGRATOR hos processor. The link may be either hardwired or connected via telecommunications equipment. Incorporation of this Communications Link allows the Sentry to Data Log to the INTEGRATOR as well as to utilize the mass storage of INTEGRATOR for up-load and down-load of test plans, source files and ALLINK files. For specific information related to the INTEGRATOR, refer to Fairchild's INTEGRATOR Product Description.

Through the use of Sentry VII system software, it is possible to load the system, perform various tests on the DUT, obtain go-no-go results, and to perform diagnostics. Test results may be printed out, recorded on the disc memory or on magnetic tape, or displayed on a video keyboard terminal; or a combination of these, depending on the peripheral equipment selected for use.

Systems software is supplied as object material on 9-track 800 bpi magnetic tape with CPU and peripheral diagnostics in source and object on magnetic tape.

Standard systems software is delivered as an integral part of each hardware system at no extra cost, and undergoes a complete verification by our field engineering staff upon system installation. Each software element has been written, debugged, and fully documented for ease of understanding and control.

The modularity of the systems architecture allows the user to expand his operating system as required to fit his test applications without changing the resident executive software. The test programs are automatically relocated and packed in memory and disc as they are entered or deleted, so the operator does not need to assign memory locations or keep a directory on what is in memory or on disc.

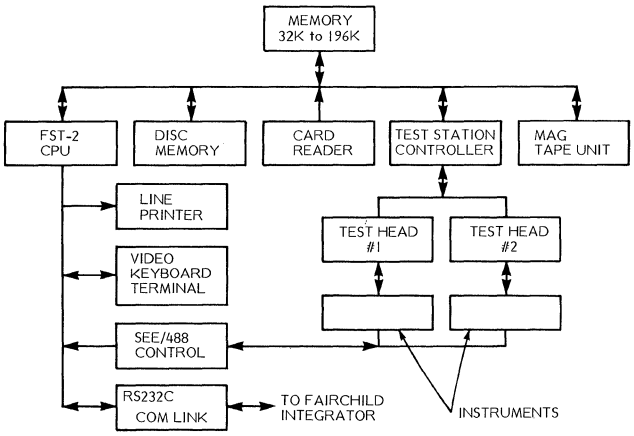


Figure 2-1. System Information Flow

The automatic test program packing is a result of dynamic core allocation capability. As test programs are entered into the memory, they are automatically packed in memory address sequence. When a test program is removed from the memory, the test programs following it are automatically moved with the memory to fill the vacant memory space. All vacant memory spaces are therefore, always in adjacent memory addresses and not scattered through the memory. This provides test program protection as no test programmer executive module can be removed or overlayed with a second program.

2.1.1 Data Management Routines

The Sentry software provides the capability for fully debugged data management operations. A full range of arithmetic computation routines are possible with the Sentry. While testing is performed, the computer can manipulate that data to produce histograms (including maximum, minimum, mean, standard deviation), floating point calculation, after mapping, Boolean expressions, etc. This provides instant data analysis capability so that changes can readily be assimilated by the test or evaluation engineer for immediate response or action while normal testing continues.

Additional datalog features include dynamic datalog of high speed MOS memories, shift registers and encoders; selection of the desired data on a pass/fail per test, per device or per nth device basis; datalog to any I/O device including VKT, line printer, magnetic tape, and disc. The Sentry VII FACTOR programming language permits, by its structure, enhancements or the addition of special features to the already extensive datalog capabilities.

Programming the Sentry VII is in an English-like language similar to FORTRAN or Algol-60. The Sentry language is called FACTOR (Fairchild Algorithmic Compiler-Tester ORiented). FACTOR provides Algorithmic Compiler-Tester ORiented). FACTOR provides two basic types of statements: (1) arithmetic and logical control statements, such as those which normally comprise procedural languages; (2) test control statements which set up and execute functional/parameter tests. The Sentry VII compiler assists the programmer in the development of his FACTOR test program by indicating syntax errors committed, the entry of overlong statements, etc. Thus, programming time is minimized because the effort is focused on the actual testing rather than on "grammatical" errors. Assembly language programs can be used also with the Sentry VII to minimize test program core usage and overhead time; users of the Sentry VII can be trained in Assembly Language programming and can either write their own programs or work with Fairchild system in program development.

2.1.2 DOPSY

Two operating systems, supplied with the system, must be resident in the disc memory before actual device testing can be performed: DOPSY (the Disc Operating System) and TOPSY (the Tester Operating System).

DOPSY is a programming system that consists of an assembler, compiler, diagnostic, file system, system loader, and extensive library routines that operate under the control of a DOPSY Monitor. In other words, DOPSY facilitates job control, loading, core allocation and input/output functions. DOPSY organization is shown in Figure 2-2.

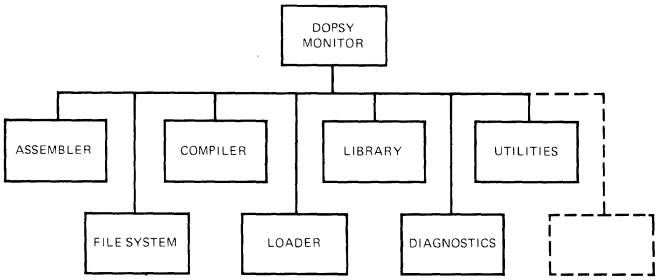


Figure 2-2. DOPSY Organization

The majority of core memory used by DOPSY for maintaining the disc and file processing are available to the users. Figure 2-3 illustrates how space is allocated on the disc. Of the five areas on the disc, only the first two - the core buffer and the skeleton monitor - are fixed in size.

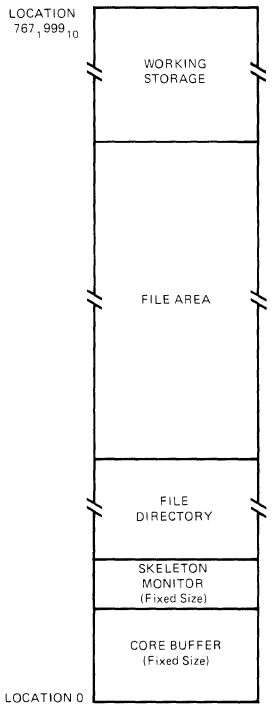


Figure 2-3. Disc Sector Allocations

The kinds of files that the system processes are called STRING, DATA, OBJECT, and COREIMAGE.

STRING files may be generated with CREATE or EDIT programs. STRING files are used as input to the compiler, assembler, and as control procedures.

OBJECT files are formed from one or more OBJECT files via the CREATE operation. These files, as the name implies, are an image of core memory for quick loading and execution. Figure 2-4 illustrates core memory allocation when the DOPSY monitor is in core. User programs may use all of core from octal location 220 to octal location 37,777.

DATA files are FACTOR test program files generated by compiling a STRING file. These files contain data which is directly executed by the tester and interpretive data which is executed by TOPSY.

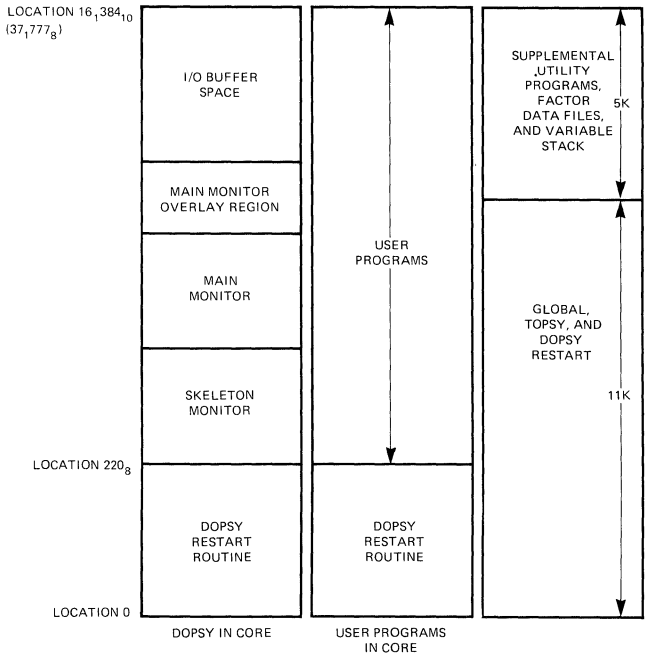


Figure 2-4. Core-Memory Allocations

2.1.3 TOPSY

TOPSY is designed to aid the user's interactions with the test system and to supplement the capabilities of the hardware. TOPSY is a programming system comprised of a Command Processor, Arithmetic Statement Processor, Interpreter, Datalogger, and Manual Analysis that operate under the control of the TOPSY Monitor. A compiler translates FACTOR programs to a code in a format executable by TOPSY. The TOPSY Monitor analyzes the user test plan instruction-by-instruction, calls the routines necessary for execution of the program instructions, and initiates the Direct Memory Access (DMA) Mode for the system.

Effective management of CPU memory resource is required to maximize test system throughput (Device Tested per Second). TOPSY is organized such that it accesses

FACTOR DATA files from Disc only when necessary - thus minimizing data transfer times. The memory management algorithm automatically determines available memory size and adjust its paging scheme (if paging is required) optimally. This allows the User to optionally add CPU memory as dictated by throughput requirements without any changes to his FACTOR or system programs - providing total growth compatibility.

Memory allocation while in the TOPSY mode is illustrated in Figure 2.5. To further enhance memory management, Utility Programs (ALLINK's) can access a 4K Buffer located in upper memory. In addition, multiple Utilities (ALLINK's) can reside in the FILE storage area.

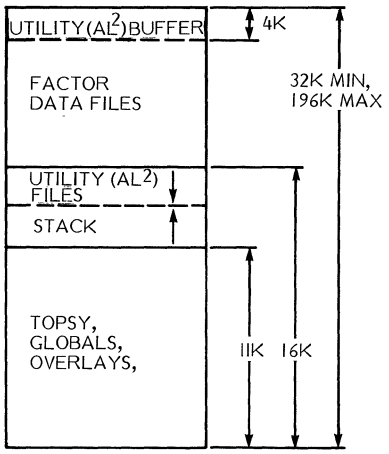


Figure 2-5. TOPSY Mode Memory Allocation

TOPSY is capable of multiplexing four test stations in an ordered sequence (4D, 4C, 4B, 4A). Manual, monitor, or automatic operation can be independently exercised at each test station/head. To maximize efficiency from a system viewpoint, control is given to the next station in sequence whenever TOPSY cannot execute the net test of the presently active test sequence; i.e., a pause, end of test or terminal error.

2.1.4 Diagnostics

Extensive diagnostic software is provided as standard with all Sentry systems. The diagnostic software is designed to assist the customer in calibration, verification, and maintenance of the Sentry VII. With it, the performance of the entire system is measured or exercised for value, timing or function. The Diagnostics perform both macro and micro functions by defining a general malfunction area for one part of the system, peripherals or the interface, while pinpointing relay or other key component problems non the pin electronic cards. All elements of the test system, the CPU, memory, long and short registers, timing generators, drivers, comparators, certain relays, the Precision Measurement Unit (PMU), the peripherals, and the peripheral interface are systematically examined by the Diagnostics. The PMU is used, after its self-check with a standard resistor, to measure the various parts of the system for DC accuracy, not just functional verification.

At the request of the operator, selected portions of the Diagnostics can be exercise; they can verify the operation characteristics, accuracy, tolerances, and limits of the tester hardware itself to establish confidence in the performance and condition of the hardware elements as well as assure the functional operation of the system architecture. The diagnostic package provides programs to completely check out the mainframe, the computer, the test station, and all system peripherals.

Use of the diagnostics is simple and can be performed by an unskilled operator.

A powerful set of diagnostic software, taking from two to fifteen minutes to run, has direct impact on profit and loss for every customer since failure modes are readily identified and rapidly corrected; thus, wasted manpower and dollar losses due to production slow downs are minimized, with a resulting favorable impact on dollar savings.

2.2 SUPPLEMENTAL SOFTWARE

2.2.1 Device Test Program Software

Plant applications engineers generate programs and applications notes to assist you in the programming of especially difficult or tricky devices. Field applications engineers are available also to assist new customers in system use, generate test programs, application routines, explain new or special system features, and to generally assist you with troublesome device testing.

Device test programs currently in our catalogue library may be purchased, complete

with the required performance board, device specification and system configuraton. The Applications Department will be glad to quote any devices which you may wish programmed.

Device programs available cover virtually every class of semiconductor in all current functional product types: bipolar MSI/SSI, MOS static or dynamic MSI/SLI (PMOS, NMOS, CMOS), memories (RAMs, ROMs, PROMs), calculator chips, watch circuits, low power devices, microprocessors, opto electronic devices, linear components, and micrologic.

For the Sentry Series, Fairchild Systems Technology has developed device test programs for RAMs from Mostek, AMS, TI, FSC, Intel, AMI, and Signetics; for shift registers from Signetics, AMI, and RCA; for Harris flipflops; for microprocessors from Intel, Signetics, Motorola, AMI, Monolithic Memories, Toshiba, and Intersil; and for other devices from FSC, RCA, and Western Digital. Also there are modular programs available allowing the use of one performance board for the entire 7400 Series of TTL devices - total functional and DC test programs can be completed and debugged in 30 minutes.

These test programs are placed in peripheral storage by the operator using the appropriate media and may then be called into the system's central processor to enable the test system to apply specific parametric and functional testing parameters to the particular device under test. Test program media depends on the system peripherals specified in the particular configuration. The standard medium is 9-track 800 pbi source magnetic tape. However, test program packages are delivered in the particular medium - punched card, paper tape, magnetic tape, microfiche, etc. - appropriate to the user's specific hardware.

Applications support is available to every F.S.T. test system user and supplements the standard test programs and utilities. New devices, more pins, changed circuits, technical requirements evolving constantly, new management data, reformatted process control data - all these special situations may call for new, special-purpose software beyond the standard, available modules and packages. Custom software from Fairchild Systems Technology is available on special request, estimated to your testing needs.

2.2.2 Utility Software

A broad range of utility software packages and subroutines are available for users of Fairchild test systems. For both simple and quick system usage, the user loads these routines to the system disc. These routines may be divided conveniently into the following general categories:

General Purpose Utilities
Pattern Generation
FACTOR Enhancement
Peripheral Control Routines

GENERAL PURPOSE UTILITIES

COPJOB copies files from disc to magnetic tape (self-loading) for efficient file transfer from system to system and reloads into disc without operator intervention or action.

COPMBT is similar to COPJOB, but creates a fully blocked magnetic tape at approximately a 20:1 saving in tape use and time to read/write.

CHANGE edits string files by changing every occurrence of a given character string into any other given character string, thus speeding and simplifying creating or altering new or existing FACTOR programs.

LMLOAD transfers functional test data between local memory and disc files at run time and greatly reduces compile time.

LMSAVE is used with microprocessor test generation programs for transferring functional test data between local memory and disc files, converting floating point numbers to octal or hexadecimal, converting microprocessors opcodes to their mnemonics for printing on an output device.

PATTERN GENERATION UTILITIES

ROMPAT. Given a ROM with known good inputs, this package generates a functional pattern for testing subsequent ROMs of the same type - with sequential, complementary, or random-address generation. Automatic function eliminates human error and saves engineering time.

ROMPONG executes a ping-pong type test on a ROM to test access times using a simple FACTOR calling sequence, thus greatly reducing programming time and effort.

RAMPAT generates N and N^2 functional test patterns for RAMs from an extensive library of patterns and SHMOO plots with fail matrices for datalogging results. when used with LMTSF, it can generate patterns for inclusion in other test programs.

PGLOG datalogs failures in program using the hardware pattern generator (enabled or disabled during test), thus supplementing the standard datalogging capability of the hardware.

CSETF. An algorithmetic pattern generator of SET F data, it creates SET F data and writes it to disc for later use.

FACTOR ENHANCEMENTS

GLOBS extends the number of system global variables.

LOGREG reads and writes contents of long registers and logs them to the primary system output device (terminal or line printer).

PERIPHERAL CONTROL ROUTINES

FMTAP controls the magnetic tape unit from a FACTOR program, including rewinding tape, skipping files (forward or backward), reading/writing large arrays, and writing EOF marks.

EXTERNAL INSTRUMENT CONTROL

IBUS allows Instruments which meet the IEEE/488-1975, "Standard Digital Interface for Programmable Instruments", to be controlled from within a FACTOR program. The instrument may be a Talker or a Listener thus providing a means for the User to interface his own devices to the Sentry in a straightforward manner.

COMPLETE UTILITY PACKAGE

A complete package of utility programs for the Sentry VII is available, or the programs may be purchased separately as needed.

2.2.3 Special Software Products

LEAD

Microprocessor testing has in the past faced the test engineer with the horrendous task of generating functional test patterns and sequences in the thousands. The Fairchild Systems' LEAD method reduces the huge task of finding the optimum test for microprocessors and the associated truth table to the simple task of specifying the diagnostic test an the device characteristics.

With LEAD, a reference microprocessor is placed in the test socket of the Sentry VII; the LEAD generator/monitor executes a diagnostic program written in the microprocessor's own language and the Sentry VII learns all the microprocessor responses and stimuli. This learned information (a truth table of functional test sequences) is stored in the system disc memory for later use. In conjunction with the learning process, the Sentry VII printer prints out a program map that cross-references microprocessor data, opcodes, and addresses to the learned functional truth table.

```
STAT1D        TEST PLAN  GEN8P          SN       2

8080 TRUTH TABLE GENERATION                 PAGE   1

PAGE LOCAL   CPU   READ WRITE   OPCODE  STACK   A/F   B/C   D/E   H/L
     MEM     PROG  DATA DATA            PNTR    REGS  REGS  REGS  REGS
     ADDR    CNTR

   1 0111  0000  00C3         JMP     0000  0002  0000  0000  0000
   1 0115  0001  0050
   1 0120  0002  0000
   1 0123  0050  00FB         EI      0000  0002  0000  0000  0000
   1 0127  0051  003A         LDA     0000  0002  0000  0000  0000
   1 0133  0052  0013
   1 0136  0053  0000
   1 0141  0013  0002
   1 0144  0054  0021         LXI H   0000  0202  0000  0000  0000
   1 0150  0055  0014
   1 0153  0056  0000
   1 0156  0057  0007         RLC     0000  0202  0000  0000  0014
   1 0162  0058  0086         ADD M   0000  0402  0000  0000  0014
   1 0166  0014  0005
   1 0171  0059  0032         STA     0000  0906  0000  0000  0014
   1 0175  005A  0015
   1 0200  0058  0000
   1 0203  0015        0009
   1 0206  005C  00F3         DI      0000  0906  0000  0000  0014

GENERATION COMPLETE
```

Figure 2-6. Program Map

Next the learned truth table is used by a device test program. This device test program can be one designed for engineering evaluation, production test, or diagnostic purposes; all the device programs can use the same learned truth table stored on disc.

After executing a device test program and using the learned truth table, the characterization data is analyzed and correlated with

the expected data. This is the LEAD method: Learn, Execute, and Diagnose.

The Sentry VII user can purchase from Fairchild System the LEAD generator/monitor for the microprocessor he wishes to test on the Sentry VII. This generator/monitor is the program that interprets the diagnostic program, creates the learned truth table, and prints the program map correlating microprocessor information an functional test sequences.

The Sentry VII user writes his own microprocessor diagnostic program in the microprocessor's own language.

Microprocessor test programs are also available from Fairchild for engineering evaluation or production test. Depending on the user's needs, these programs provide failure analysis data - shmoo plots showing the interaction of two parameters, functional and parametric test results showning both expected and actual data, and yield analysis reports showing quantity tested, passed, and failed plus which tests failed - and manual analysis options for greater flexibility in testing and analysis.

FAIRTEST

Boeing Computer Services markets FAIRTEST, a computer-aided test generation system which produces functional tests for digital logic subassemblies.

FAIRTEST is available as a remote batched service, enabling customers to rent a terminal and FAIRTEST time, or may be purchased outright with all documentation and support provided.

Contact Boeing Computer Services, 1101 San Antonio Rd., Suite 314, Mountain View, CA 94043, (415) 964-8555.

SECTION III

ENVIRONMENTAL REQUIREMENTS

3.0 ENVIRONMENTAL REQUIREMENTS

Even though the Sentry VII test system can operate in a temperature range of $+5^{\circ}C$ to $+30^{\circ}C$ ($+60^{\circ}F$ to $86^{\circ}F$) with a relative humidity level of 5 to 50%, non-condensing, Fairchild Systems recommends an optimum temperature of $23^{\circ}C$ ($73^{\circ}F$) and a relative humidity level of 35%. This optimum environment provides the largest buffer in terms of system operation, accuracy, and guard band repeatability.

Deviations from the recommended environment, in either direction, for sustained periods will expose the system to possible malfunction. Deviations of 24 hours or more will permit cards, magnetic tape, paper, and electronic components to reach steady-state conditions and, thus, prolong return to the optimum design point.

High relative humidity levels may cause condensation, improper feeding of cards and paper, leakage which interferes with low current measurements, plus operator discomfort. Low humidity levels tend to increase the possibility of static charges which may cause intermittent interference with precision measurements.

Since moisture and foreign particle contamination tends to degrade precision high speed test equipment performance overtime, it is recommended that routine maintenance be performed to provide maximum instrumentation margins and sustained high levels of system performance.

It also recommended that automatic air conditioning be provided at the site for maximum system availability.

Sentry VII Air Conditioning Requirements. To allow for heat produced by personnel, instruments, and the Sentry VII, use six tons of air conditioning to cool the Sentry VII installation site; use more if there is other machinery or equipment in the area.

The following is a calculation for partial air conditioning requirements:

Since a Sentry VII with three test heads draws approximately 115 amperes total current,

$$\text{Power} = (115\ A)(115VAC) = 13.225 \times 10^{3}\ VA$$

The heating, ventilation, and air conditioning required is approximately 0.4 tons per kilowatt. $(13.225)(0.4) = 5.29$ tons

SECTION IV

POWER REQUIREMENTS

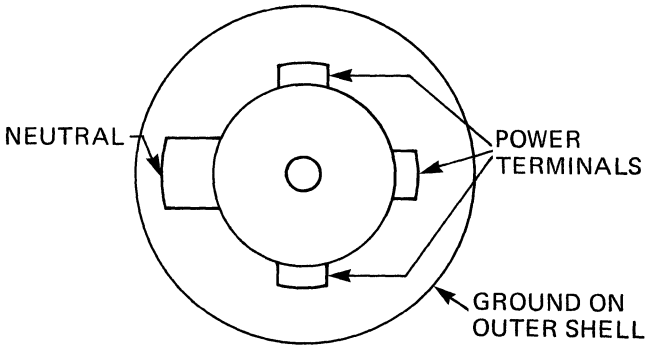
4.0 POWER REQUIREMENTS

All peripherals - test station as well as VKT, line printer, card reader, magnetic tape unit, etc. - are powered from the Sentry II Mainframe, and two power sources come with the system for this purpose.

Each of the two cables supplied is 5-wire, 3-phase, Y-connected, 208 VAC, with 30 Amp per phase. Each of the two cables has ground, neutral, and three phases of 115 VAC (5 wires). The cables are rubber-covered, 5-wire, 10 gauge, 600V rated. The cables are terminated with a Hubbell #25414 connector on the mainframe end.

These main power cables are delivered with connectors on only the mainframe end to facilitate connection to any type of customer power source. Hardwiring into a 30A per phase breaker box is the usual practice.

The mainframe end of the cable (connector end) can be checked for proper source power. To do this, the user measures 208 VAC from any power terminal to any other power terminal and measures 115 VAC from neutral to any power terminal.



HUBBELL 25414 CONN.

The Sentry VII user provides power to the Sentry VII. This power should be provided by a separate power line and should be physically removed from high emissive sources. Power input must comply with specifications; line variations in frequency and voltage to approximately $\pm 5\%$ can be tolerated without damage to the system, but operating performance may be affected, depending on the extent of voltage and frequency excursions.

Also, the user should have a 30 amp circuit breaker per phase (six in all) for the two power sources required by the Sentry VII.

SECTION V

SPACE REQUIREMENTS, MECHANICAL DESCRIPTION, FLOOR PLANS, AND ACCENT PANEL COLORS

5.0 SPACE REQUIREMENTS

Figure 5-2 shows a floor plan for the Sentry VII with one test station.

Sentry VII Mainframe. The central, control console consists of a single bay with side panels on each 44-inch (110 cm) side that are removable for servicing or maintenance of the internal electronics.

The magnetic tape unit, housed in the central console, is accessed by a hinged door that has a swing-out radius of 30 inches (75 cm). The swing door on the opposite side of the central console covers the computer, memory, and I/O and has a swing-out radius of 20 inches (50 cm).

Three feet (90 cm) of access space should be left around the entire machine for maintenance access.

Test Station. The test station is a single bay 35"x35"x35" (67.5 cm x 67.5 cm x 675 cm).

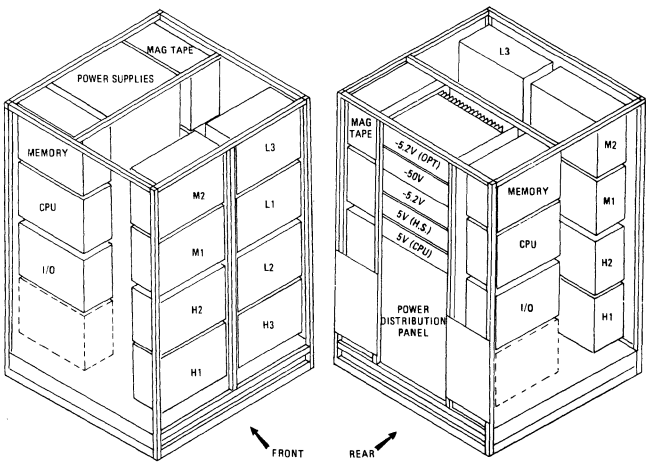


Figure 5-1. Sentry VII Module Locations

Within the test station is the pin electronics carousel designed to function as a manual station or with a wafer prober or automatic or environmental handler station. It can contain up to 30 pin electronic cards (60 pins) placed radially in a package configuration 16" (40 cm) wide by 15" (37.5 cm) deep by 9" (22.5 cm) high.

The display and control panel is mounted in a portable box that can be placed at any location on the table top of the test station to suit the operator's convenience. The box is 9" (22.5 cm) wide by 7" (17.5 cm) deep by 3" (7.5 cm) high.

Peripherals. The VKT, card reader, and line printers all require tables so that they are at a convenient height for use by the operator. A table area beside the VKT is useful for writing and for holding listings, information to be entered, run sheets, etc. Sentry VII customers may supply their own tables or order accessory tables (model number 8358) from FST.

The fixed-head disc is a free-standing unit 23" (58 cm) wide by 24" (61 cm) deep. Three feet should be left at the front and the sides of the disc console to allow for easy operator use of the disc and to accommodate maintenance personnel.

5.1 FLOORING AND CABLING

Although not absolutely necessary, the user may implement a 6"-8" (15-20 cm) raised floor for the installation site. With a raised floor, peripheral and power cables external to the mainframe are run under the floor to eliminate hazardous clutter. With or without a raised floor, test station cables are run

through the cable duct included with each system.

Cable Length Mainframe to Test Head. Although the physical length of the shortest cable that connects the high speed controller is 15 feet (5MHz station) or 10 feet (10 MHz), the actual usable length is 10 feet (5 MHz) or 5 feet (10 mHz) due to cable routing in the test station.

5.2 EQUIPMENT WEIGHT

The approximate weight for the main items of the Sentry VII are as follows:

Mainframe: 2,000 pounds (907 Kg)
Test Station: 300 pounds (136 (Kg)
30 pounds for the pin electronics
Test Station: 300 pounds (136 (Kg)
30 pounds for the pin electronics carousel and 4 pounds for the display and control panel
Cable Duct Assembly:100 pounds (45 Kg)
Disc: 220 pounds (100 Kg)
Card Reader: 45 pounds (20 Kg)
VKT: 40 pounds (18 Kg)
Line Printer: 230 pounds (104 Kg)
Wafer Handler: 350 pounds (159 Kg)

5.3 ACCENT PANEL COLORS

The Sentry VII accent panels can be ordered in one of five colors to suit your facility's color scheme; see the next page for color swatches:

Blue (Federal Standard #15180)
Gold (Federal Standard #33434)
Orange (Federal Standard #32544)
Red (Federal Standard #31136)
Dark Grey (Federal Standard #26134)

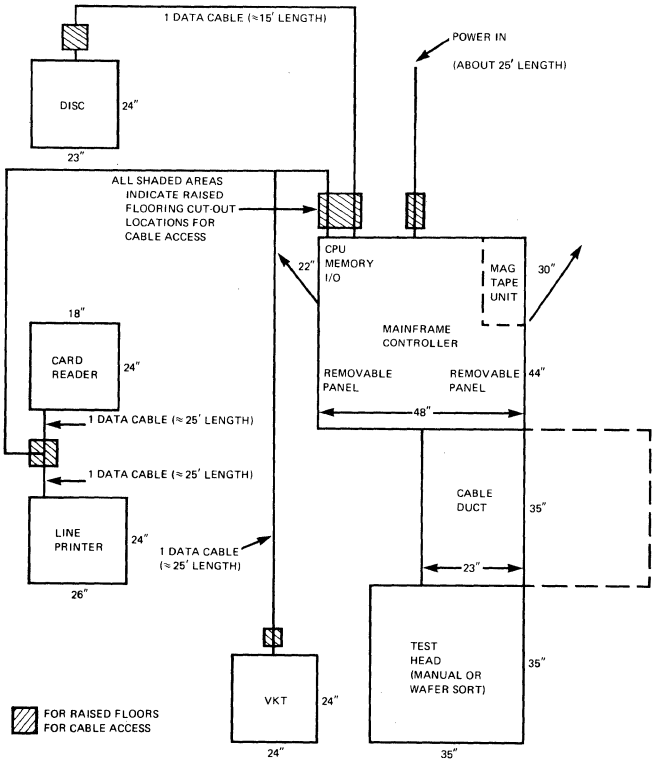


Figure 5-2. Typical Sentry VII Floor Plan with One Test Station

SECTION VI

RECOMMENDED MEASUREMENT EQUIPMENT AND SPARE PARTS

6.1 MEASURING INSTRUMENT RECOMMENDATIONS

We recommend that the Sentry system user gather the following list of instruments for use at system installation time and for subsequent device program debugging.

Oscilloscopes:

- o Tektronix 7904 or equivalent
- o Two Tektronix 7A11 High Frequency Pre-amplifiers or equivalent
- o Two Tektronix 7B92 Dual Time Base or equivalent
- o Two Tektronix P6054A matched oscilloscope probes

Digital Voltmeter:

- o 6-digit Integrating DVM with 1 volt resolution and .01% accuracy

Volt-Ohm-Meter:

- o Simpson 260 VOM or equivalent

6.2 SPARE PARTS

Fairchild Systems Technology offers parts to its customers as another means of achieving maximum product utilization. Customers may purchase on a piece part or spares kit basis or use the repair or exchange programs.

The Sentry VII Basic Spare Parts Kit contains those components and circuit board types which are located in several positions throughout the system. For example, there are two "tester" pins of electronics on one Pin Electronics (P.E.) card and three tester pins of electronics on one Pin Control 2 board; thus, a 30-pin system with one test head would have 15 P.E. cards and 10 Pin Control 2 cards.

The Supplemental Spare Parts Kit contains those printed circuit board types which are the most complex and probably the most difficult to troubleshoot should the need arise.

They are offered to minimize repair time for personnel who are not intimately knowledgeable of the machine at the device level. Test system user maintenance personnel also have telephone assistance available from either the FST local Field Service office or from FST Technical Support in San Jose when necessary to aid in rapidly localizing a problem to the board level.

RECOMMENDED SPARE PARTS KIT
SENTRY II
BASIC

Quantity	Part Number	Description
1	97166001	2 Bit Slice PCB
1	97230101	Pin Control 1 PCB
1	97230109	Analog Ref. Supply
1	97234303	Pin Control 2 PCB
1	97230341	Local Memory PCB (512 x 16)
1	97230313	Timing Gen. PCB
2	97231041*	10 MHz P.E. PCB
10	05036850	Relay, 225-4-1A
2	05036860	Relay, 450-4-1C
2	05037100	Relay, 551-4-1A
2	05037110	Relay, W/16
3	05906001	PMU Relay 9121-1C-05
3	05907001	Relay, 766070565
10	05903103**	Relay, 1317-4-1A 10 MHz P.E. PCB
5	05037080	Relay, 766060375
5	12014570	Lamp, 5V
1	81006400	Fan, Pamotor
1	81006060	Fan, Muffin

*Substitute 97231023 5MHz Pin Electronic Board when ordering for 5 MHz test head. For either 5 or 10 MHz, we recommend two boards for every 60 pins.

**Kit excludes 05903103 when ordered for 5 MHz test head

SENTRY VII - PATTERN PROCESSOR SPARE PARTS KIT

Quantity	Part Number	Description
1	97234301	Data Out PCB
1	97234401	Datalog Buffer PCB
1	97234402	Load Control A PCB
1	97234403	Clock A PCB
1	97360101	Control Address PCB
1	97360104	Control Data PCB
1	97360107	Reg. Compare PCB
1	97360111	Address MUX PCB
1	97360112	Data MUX PCB
1	97360113	Data RAM PCB
1	97360114	Pipeline PCB
1	97360127	Topological Scrambler PCB
1	97360109	Index Register

SENTRY VII - SEQUENCE PROCESSOR SPARE PARTS KIT

Quantity	Part Number	Description
1	97234310	Rank 8 Memory PCB
1	97234312	Mem. Add. B PCB

Under the FST Repair Program, customer-owned units are repaired for a percentage of the current board sale price. Restrictions are placed upon the age of the boards and their reparability in order to be eligible for the program.

RECOMMENDED SPARE PARTS KIT SENTRY VII SUPPLEMENTAL

Quantity	Part Number	Description
1	97166108	CPI #3 PCB
1	97166109	CPI #1 and #2 PCB
1	97340806	XDL Counter PCB
1	97340805	Phase Loop Counter PCB
1	97206007	T-Counter PCB
1	97230107	PMU Analog 1 PCB
1	97230108	PMU Analog 2 PCB
1	97234309	Sequencer PCB
1	97234306	Status and Mode PCB
1	97234302	Dual Test Rate Gen. PCB
1	97234304	Mem. Add. D PCB
1	97234305	Mem. Add. C PCB
1	97234307	Clock 1 PCB
1	97234308	Clock 2 PCB
1	97234313	Time Base PCB
1	97234314	Timing Ref. Distr. PCB
1	97234311	Mem. Add. A PCB
1	97206110	RVS PCB
1	97206103	RVS PCB
1	97206104	DPS PCB
1	97206105	1 Amp Buffer PCB

The Exchange Program relieves customers of critical situations as soon as possible on current production boards. The customer can obtain a board on an "as available" delivery basis prior to Fairchild receiving the bad board. The customer pays full price for the new board and then is credited a percentage of the bad board's current sell price.

SECTION VII

FST SUPPORT CAPABILITIES

7.0 SUPPORT CAPABILITIES

Fairchild Systems Technology is committed to a complete systems approach for all products. Each Sentry system sold is complemented with complete hardware and software documentation. You, as our customers, have access to a software and applications staff to solve your system needs. A well-trained field service organization has spare-stocking offices worldwide. And system training courses are scheduled year round for customer staffs in both programming and maintenance.

Briefly, the Sentry VII is the most extensive and capable hardware and software test system on the market today. And the total support in service, training, applications and documentation collectively is unmatched in the industry.

7.1 DOCUMENTATION

With each Sentry VII system comes a complete documentation package for both hardware and software. The documentation shipped depends on the system configuration.

7.1.1 General Information/Operating Instructions

Sentry VII Operation Manual (npn)
Sentry Systems Users Handbook (67095476)
Systems Coverage (schematics) for High Speed Controller
Systems Coverage (systems schematics), Volumes 1 and 2
Log Book (6709531) for field service entries
Bound Volume of Customer Specifications for Sentry VII, 10 MHz Pin Electronics, and 1 Nanosecond Option

7.1.2 Sequence Processor/Pattern Processor Documentation

SPM/PPM Hardware Description (67095609)
Sequence Processor Programming Reference, Users Manual, and Diagnostics (67095589)
PPM Microprogram Library Reference Manual (67095703)
Pattern Processor Programming Reference, Users Manual, and Diagnostics (67095583)

7.1.3 Test Generation Documentation

PROGRAMMING

FACTOR Manual (npn)
Sentry System Register Format Manual (67095504)
FST-2 Computer Product Description 67095701
Software Utilities Manual (67095661)
Assembly Language Subroutine Manual (67095658)

7.1.4 Systems Maintenance Documentation

Sentry Series Preventive Maintenance Manual (67095618)
CPU and Peripheral Diagnostics Manual (67095570)
Tester Diagnostic Manual TVFY (67095501)

7.1.5 Hardware Description Documentation

COMPUTER AND PERIPHERALS

Sentry VII Hardware Manual (npn)
VKT Manual Card Reader Manual
Magnetic Tape Unit Manual
Disc Schematics
Disc Technical Manual
Line Printer Manual

TEST HEAD

Sentry 5 MHz Pin Electronics Reference Manual (67095549)
Sentry 10 MHz Pin Electronics Reference Manual (67095612)
Prober Interface Board Manual (67095473)

TESTER CONTROLLER/ANALOG SYSTEM

Precision Measurement Unit (PMU) Manual (67095457)
Sentry 610 Controller Manual (67095611)

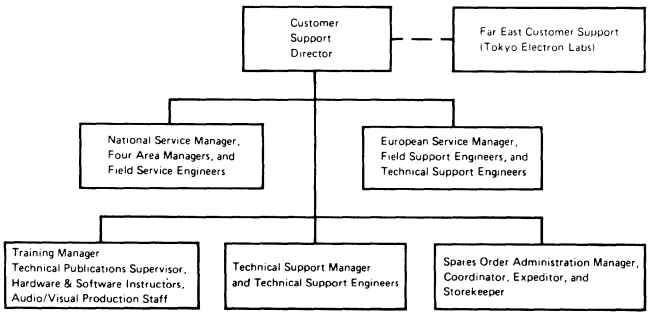
7.1.6 Pattern Generator Option Documentation

Sentry VII Pattern Generator Description (67095480)
Pattern Generator Option, FACTOR Manual Supplement (67095475)

7.2 CUSTOMER SUPPORT

The Fairchild Systems Technology Customer Support organization provides after sale support to FST customers through a worldwide field engineering group and a training group located at the FST San Jose headquarters facility.

Customer Support at Fairchild Systems encompasses an inplant technical support group, a spare parts ordering group, a repair/exchange group, maintenance and programming training, a European service organization, and four-division United States service group.



7.2.1 FIELD SERVICE

Fairchild maintains a world-wide field service engineering group for system maintenance and testing support to the customer. Factory-trained resident field engineers are strategically located throughout the world to provide on-site maintenance support. The office that will service your system is located at:

For off-hours service, call (408) 998-0123.

Complete on-site service is provided for 90 days after completion of the system installation at the customer's facility under the standard system warranty. Service after the 90 day free service period may be contracted for as a maintenance agreement.

FIELD SERVICE CREDENTIALS

Field Service engineers come to Fairchild with different backgrounds, but they all are well trained in electronic theory; mechanical timing, motion, and adjustment; tester maintenance and repair; computer maintenance and repair; and diagnostic programming. The average Fairchild Systems field service engineer has been with FST five years. He is kept up-to-date weekly on system changes, both hardware and software plus new product developments, by the technical support group in the plant. He returns to the plant periodically for additional training on all aspects of Fairchild systems.

SERVICE/MAINTENANCE CONTRACTS

As a customer of Fairchild Systems, you have your choice of a variety of service: fixed price maintenance, resident field engineer standby plans, extended coverage plans, extended travel plans, and response improvement on-call service. These types of service allow you to pick the most suitable arrangement for your testing system or systems and for operations at your facility.

Under a Fixed Price Maintenance Agreement, you pay a flat monthly fee, based on the size and complexity of your system, and, for this fee, you receive automatically system software revisions, a monthly calibration service,

scheduled preventive maintenance, automatic incorporation of Field Change Notices, plus free parts and labor. An FST maintenance agreement affords you the assurance that your FST products will be continuously maintained in top operating condition at a known and budgeted cost. The standard fixed price maintenance agreement covers on-call service eight hours per day, five days per week excluding holidays. If you wish multiple shift coverage (16 or 24 hours/day, five to seven days/week), Fairchild offers you an Extended Coverage Plan. Response time for extended coverage plans will be within four hours following a request for remedial maintenance.

In addition, FST offers a Standby Plan that can be incorporated in the Fixed Price Maintenance Agreement. This plan guarantees availability of FST service personnel within four hours.

Normal travel factored into the basic monthly maintenance prices covers travel with 100 miles of the FST service office. If your system is located more than 100 miles from the FST service office, FST offers you an Extended Travel option where a fixed monthly charge covers travel time to your location.

If you have several large systems in critical operations, you may wish to have a field service engineer resident at your testing facility. The Resident Field Engineer Contract provides you with on-site coverage one shift, five days per week (excluding holidays), with one resident engineer. Working hours may be adjusted to fit your requirements. The cost of a resident field service engineer is a fixed price per month, plus parts and portal-to-portal relocation (where applicable).

FST also offers a Response Improvement On-Call Service that guarantees response time will be within 24 hours. The charge for this type of on-call service is a flat rate per occurrence plus parts, materials, labor, travel expenses, and the miscellaneous expenses of lodging and meals.

Customers who prefer to employ Fairchild Systems Technology service on a time-and-materials basis may request service, parts, and labor as they need them. This arrangement provides maintenance serivce as required at an hourly rate. Travel time is also charged at the applicable hourly rate. All parts and material are charged at established catalog prices. The customer is also charged miscellaneous expenses of lodging, meals, car rental, mileage, and transportation charges such as airfare. This on-call service is, however, recommended for customers who have their own maintenance capability or whose sense of urgency, in terms of response time for service, is not critical. (While it is Fairchild's policy to respond as quickly as possible to all requests, service contract commitments receive priority.)

7.2.2 Spare Parts

FST offers to its customers spare parts kits (Section VI) to speed system repair. FST also offers a PC board repair/ exchange program to relieve the customer of a critical situation as soon as possible on current production boards.

7.2.3 Training

Included in the purchase price of your Sentry VII are 18 training credits - each credit equals one man-week of training in San Jose at the FST training center - including all manuals, schematics, and systems hands-on training required. We recommend attending courses during the months preceding system delivery so that you are ready to fully use your Sentry VII as soon as it is installed.

Fairchild Systems Technology offers you three ways of training: on-site training at your facility, classroom training at the FST training center in San Jose, or video tapes and cassettes for use wherever you choose.

FST instructors are well-versed in device testing, computer technologies, programming, and education techniques. Each instructor has areas of specialized training as well as a general background in other course areas.

Courses are tentatively scheduled over six-month periods and courses are added to and deleted from the schedule according to customer requirements. Video tapes and cassettes are available for rental or purchase year round.

ON-SITE TRAINING

Fairchild instructors will travel to customer facilities to train groups of employees. On-site training is cost effective when groups of students need to travel a long distance for training and when personnel to be trained are needed daily for a resource in their own facility.

The price for a Fairchild instructor teaching at your facility is $3,000 per week for one-weeked courses and $2,500 per week for courses two weeks or longer, plus the instructor's expenses (room accommodations, meals, travel to and from your facility) for twelve students or fewer. For more than twelve students, add $100 per week per student. The cost includes instruction as well as standard course materials (manuals, schematics, listings, etc.) for each student. Requests for on-site training should be handled through the Fairchild field sales offices.

TRAINING AT THE FST TRAINING FACILITY

The training center is at the heart of the new FST main plant in San Jose. When the building was designed, modern training facilities were designed in right from the start. Each of the three classrooms can accommodate from 1 to 12 students. Chalkboards are large and well-lit for easy viewing from anywhere in the room. Screens and projection equipment are available for audio/visual tape presentations. Large table areas make note-taking and referring to course material easy. Each room is well insulated, air conditioned, and acoustically tiled, so noise and temperature variations do not interfere with the learning process.

In addition to the classrooms, there is a modern industrial TV studio for preparing or viewing video tapes and a learning center for independent study. Plus, there are additional rooms for student use in reviewing the day's material. A hands-on lab is right next door to the classrooms, and a Sentry system is available for students to practice programming techniques during regular classroom hours or after hours.

Classes range from one to eight weeks in length. Each training credit included in the price of your system is equivalent to one student class week. These training credits are sufficient to bring you up to speed on your Sentry VII system. Additional courses are available at $300/week per student tuition to help you further refine your skills and your use of the Sentry VII.

A complete set of training materials and documentation is included in the course price for each student. Additional sets may be purchased for $100 per class documentation package (or $75 each in quantities of ten or greater).

VIDEO TAPE AND CASSETTE TRAINING

Video tapes and cassettes are ideal for armchair training. When your operation changes personnel, video tapes are a fast way to bring new personnel up to speed. You can use your own video playback equipment or rent the equipment from Fairchild for as long as needed.

Video tapes sell for $200 per reel and rent for $10/day/reel ($50/week/reel). The video tape playback unit and monitor rents for $50/day ($250/week). Prices are FOB San Jose, California, and apply from date of receipt to date shipped back. Transportation and insurance both ways are the customer's responsibility.

PROGRAMMING COURSES

The Sentry VII Programming Course is an intensive three week course of instruction segmented into two parts: two weeks of basic Sentry programming, and one week of programming the SPM and PPM.

The subject matter includes testing philosophies; system hardware and software capabilities; interfacing the component-to-be-tested to the tester; description and function of system controls and indicators; an overview of the Disc Operating System (DOPSY) and Tester Operating System (TOPSY) and detailed user description of associated keyboard commands and error messages for both; an overview of system utility routines; a detailed explanation of FACTOR programming capabilities, rules, syntax, statement definitions, and examples; an overview of TVFY, the Sentry Tester Verification Program; plus analysis of sample FACTOR programs written for testing and data reduction.

At the completion of this three week course, the student will be able to initialize and communicate with the test system; load and execute system programs such as DOPSY and TOPSY, Utilities (e.g., Editor), and the Tester Verification Program (TVFY); write FACTOR language test programs; interpret and correlate test data. The student demonstrates the attainment of the stated course objectives by the satisfactory completion of all homework, lab assignments, and a written end of course examination.

Prerequisites: Students from your company should have a general knowledge of semiconductor testing concepts as well as the ability to read and interpret semiconductor device specifications sheets. Experience in programming in FORTRAN or ALGOL is helpful, but not mandatory. Credits Required: Three credits or $900 per student.

MAINTENANCE COURSES

FST-2 Computer Subsystem. This is a three-week theory of operation course, a lecture session with laboratory time, providing the student with a detailed knowledge of the Central Processing Unit registers, memory, peripherals, and common peripheral interfaces, instruction timing, and machine language programming. The student will study the hardware physical locations, interconnections, modes of operation, and timing. Studies include analysis of the system's electrical schematics.

The third week theory of operation course is a lecture session with laboratory time providing the student with a detailed knowledge of interconnections, modes of operation, and timing for the peripheral controllers, video keyboard, line printer, magnetic tape unit disc, and card reader. Studies incude analysis of electrical schematics.

Prerequisites: Senior Technician level or equivalent experience with digital logic and general purpose computers. Credits Required: Three credits or $900 per student.

Sentry Tester System Maintenance and Diagnostics. This course is the second in the series of three-week theory of operation courses, lecture sessions, plus laboratory (hands-on) time. The student studies the hardware, physical locations, interconnections, modes of operation, and timing of the Sentry mainframe, the CPI (Common Peripheral Interface), M1/M2, Mux/Ref Module, High Speed Station Controller, Low Speed Module, High Speed Module, High Speed Test Head, Control and Display Panels, and the one nanosecond high resolution timing option. Studies include analysis of the system's electrical schematics.

Prerequisites: Senior technician level or equivalent experience with digital logic, analog circuits, and general purpose computers. Prior attendance at FST-2 Computer System Maintenance course is recommended. Sentry VII Tester System Maintenance. Credits Required: Three credits or $900 per student.

Sentry VII/Pattern Processing Module Maintenance is a one-week theory of operation course covering the Pattern Processor on the Sentry VII. This course includes practical hands-on laboratory time as well as illustrated classroom lectures. Prerequisites: Attendance at the Sentry and Sentry VII Tester Maintenance and Diagnostic Courses. Credits Required: One credit or $300 per student.

VIDEO TAPE LIBRARY

The following tapes and cassettes are available for your use:

Sentry VII Basic Programming (9 reels)

FST-2 CPU Theory of Operation (11 reels)

FST-2 Peripherals Theory of Operation (10 reels)

FST-2 Assembly Language Programming (8 audio cassettes)

TRAINING SCHEDULE

Available on request.

SECTION VIII

RELATED EXPERIENCE

8.0 RELATED EXPERIENCE

Fairchild Camera and Instrument Corporation is a diversified, international company with capabilities in electronics components, systems and equipment. The company maintains manufacturing facilities in five states and eight foreign countries, and a worldwide sales and distribution network.

The Systems Technology Division is an international operation engaged in designing, developing and producing automatic test systems for semiconductor devices, components, electronics subsystems and systems. The Division's headquarters and main manufacturing plant are located in San Jose, California, U.S.A. This modern, 140,000 square foot facility is supported by a network of sales and service offices in the United States, Canada, Europe and Asia and by selected manufacturer's representatives in these areas.

The Division, formed in 1965, was initially called Instrumentation Division. The operation expanded its test system product line and in 1969 changed its name to Fairchild Systems Technology.

Early product developments included the 500 transistor/diode tester in 1963, and its second-generation counter-part - the 600 transistor/diode tester - in 1967. Fairchild Systems introduced an integrated circuit tester, the 4000 series, in 1964. This was followed by the 5000 series of complex circuit testers introduced in 1968 and the first computer-controlled CI tester system, the 5000C, introduced in 1969. With its high throughput rates, high-speed analog-to-digital converter and versatile software package, the 5000C continues to serve a substantial segment of the test market.

In March of 1970, Fairchild Systems introduced the first computer-controlled, modularized, expandable test system product line, called the Sentry series. These third-generation systems are designed to test complex MSI/LSI integrated circuits, electronic subsystems and systems.

Fairchild Systems Technology has installed nearly 2000 automatic test systems to customers throughout the world, including companies such as IBM, NCR, National Semi, Delco, Bell Labs, Aeronutronics Ford, AMS, Western Electric, RCA, AMI Univac, Burroughs, Teletype, Control Data, Intel, Signetics, Intersil, Litton Industries, Lockheed, General Dynamics, U.S.Air Force and U.S. Navy. Activities are continually expanding and the Division is developing new equipment and systems responsive to changing technical requirements.

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SECTION IX

SENTRY VII ACCEPTANCE PROCEDURES

9.0 SENTRY VII ACCEPTANCE PROCEDURES

System conformance to this acceptance procedure for the Sentry VII constitutes the method by which System Performance and Acceptance are verified. The System Acceptance tests are run prior to system shipment and at system installation. Items of this Acceptance Procedure are as follows:

A. Inventory/verify all items to be shipped (except those specifically approved to be shipped later).

- Record serial numbers of major modules.
- Verify that documentation sets are available.
- Verify software components are available by entering // FDUMP' .PSLIP' LP
- Verify software components are on disc by entering // SET DIF' .PSLIP'

B. Verify CPU and CPU memory by executing:

- INSF2 - CPU Instruction Check
- MEMF2 - Memory Diagnostic
- INDFX2 - Index Register Diagnostic
- ATXF2 - Index Register Diagnostic
- PYRF2 - Pyramid Adder Check
- RELF2 - Relative Memory Address

C. Verify Peripheral Operation by executing the following diagnostics:

- Disc - QDISC
- Mag. Tape - MGTDIA
- Card Reader - CRDIA
- Line Printer - appropriate line printer diagnostic
  LPDIA - High-Speed Line Printer
  LSDIA - Low-Speed Line Printer
- Video Keyboard Terminal - TTYDI

D. Verify system performance with the Sentry VII Tester Verification Program (TVFY), which self-tests in the integrity of data paths, functions, and D.C./Dynamic accuracies of the Sentry VII. This program accounts for tolerances of both the Self-Stimulus and Measurement Accuracy Specifications of the system. The Sentry Diagnostic Manual (FST Part Number 67095501) describes the tests performed and the method of operation. The tests included in this program are as follows:

TEST 1

Mainframe Short Register Test. All short registers are exercised with floating ones and zeroes with crosstalk tests.

TEST 2

Mainframe Time Delay Test. All time delay registers are tested for correct time delay.

TEST 3

Station Controller Long Register Test. All long registers are exercised with floating ones and zeroes with crosstalk tests.

TEST 4

Local Memory Test. The local memory is exercised with checkerboard, checkerboard complement, all ones, all zeroes, and address test.

TEST 5

Memory Control Test. The memory control hardware is tested by executing minor and major loop.

TEST 6

Local Memory Cycle Steal. The local memory is tested for the ability to alter locations while in a continuous loop test.

TEST 7

Loop Counter Test. The major and minor loop counters are tested to ensure proper operation.

TEST 8

Test Head Leakage Test. All tester pins are tested for leakage and comparator bias current.

TEST 9

PMU Test. The precision measurement unit is tested for D.C. and dynamic accuracy in all force and sense ranges.

TEST 10

PMU Clamp and relay driver test. The PMU clamp is verified at various voltage levels. All odd utility drivers from pin 31 to pin 59 are tested.

TEST 11

I/O switch and I/O mode Test. Each pin is tested for correct I/O switch operation in DA/DB modes and in IOMODE/-IOMD3.

TEST 12

Internal Node Test. All RVS's and DPS's are tested for D.C. accuracy at the internal node.

TEST 13

Test Head D.C. Test. The D.C. accuracy of the functional drivers is tested.

TEST 14

Driver Impedance Test. The output impedance of all drivers is tested at full-rated current.

TEST 15

Pin Electronics Function Test. The drivers and comparators are tested functionally to verify dynamic accuracy and functional fail logic.

TEST 16

Pin Control II Test. Ignore fail, chain 2, chain 4, ignore fail by count, XOR, MUX, IMASK, RTO mode are verified.

TEST 17

Timing Generator Assignment Test. All possible combinations of timing generator and pin assignments are tested to verify the decoder logic and utility relay performance.

TEST 18

Timing Generator Delay and Width Test. Each timing generator delay and width counter is tested in all ranges.

TEST 19

MATCH MODE TEST. The match mode function is tested in a functional program to ensure that a match condition is detected correctly.

TEST 20

LATCH MODE TEST. The latch mode function is tested to ensure that the comparator register will accumulate fail data while the latch is enabled.

TEST 30

Burn-In Test Repeated at Requested Rep Rate. All tests, 1 through 20, are exercised during each cycle of burn-in. Summary printout indicates results.

DPSTT

Device Power Supplies tested for current and voltage trips.

DCMP

D.C. comparator Test. The D.C. trip points of each pin are measured to verify the comparator.

E. To further ensure system performance, exercise the system in its operating mode by executing standard FST device programs on each test head without any failures. The two programs to be executed incorporate both N and N^2 functional patterns.

If the system is configured without the Hardware Pattern Generator Option, test it with the N1103 MOS 1K x 1 Dynamic RAM (5/10 MHz Stations) and the R93410 TTL 256 x 1 TTL RAM device test programs.

Both programs include Checkerboard, Column Bar, Row Bar, Diagonal, and Ping Pong patterns. "N1103" also has Walking One, Walking Zero, Checkerboard Complement, and Diagonal Complement patterns. "R93410" also has Solid, Parity, Shift, Chip Select Access Time, and Write Recovery Time patterns.

"N1103" runs DC tests for input leakage, output leakage, and IDD and IBB current tests. "R93410" runs DC tests for input clamp voltage, input low current, input high current, output low voltage, and output leakage.

If the system is configured with the Hardware Pattern Generator Option, verify Pattern Generator operation using PDIAG and two device test programs: P1103 (5/10 MHz) and H93410 TTL 256 x 1 RAM.

"P1103" includes Checkerboard, Checkerboard Complement, Column Bar, Row Bar, Diagonal, Diagonal Complement, Walking One, Walking Zero, and Pingpong patterns. It also does the DC parametric tests for input leakage, output leakage, and IDD and IBB current.

"H93410" includes Solid, Checkerboard, Column Bar, Row Bar, Diagonal, Parity, Shift, Pin Pong, Chip Select Access Time, and Write Recovery Time patterns. It also does the DC parametric tests for input clamp voltage, input low current, input high current, output low voltage, and output leakage.

F. To verify pin driver skew specifications execute the FACTOR program SKEW6.

Use a high-frequency oscilloscope with one pin as reference and visually check the remaining tester pins for skew relative to the reference pins.

Load the FACTOR program SKEW6 with /. LOAD 'SKEW6' STATn where n is the station 1A-4D. Push test station start and select Option 4 (all pins as data drivers) to cause the test to begin. The procedure will be in local memory loop such that system skew can be measured on each test head.

Obtain an oscilloscope with a bandwidth 200 MHz. Verify oscilloscope sweep by using 100MHz clock. Verify skew by connecting the two probes to the same pin and noting any skew or amplitude different. Use adapter plus 97239939.

Place Probe #1 on Tester Pin 2 Output and sync the scope off this input. A performance board is not used in this procedure.

Sequentially, place Probe #2 on 20 pins (selected by customer) recording the time different between the 50% point of the pin being checked. Check both rise and fall. A signal different is positive if the tested signal preceeds the reference signal and negative if the tested signal is delayed from the reference signal. Record all measurements. The difference between the slowest and fastest pins must be 2ns for 10MHz stations and 10ns for 5MHz stations.

Push Test Station Start to change E0 to -16V and E1 to +6V and verify slew rate is 1.5V/ns for 10MHz stations. For a 5MHz station, verify that slew rate is .75V/ns for a 36V change.

Repeat test with Option 1 (all pins as clock drivers). Use the same 20 pins as before. Load pins with 100 pf. with E0 at -16V and E1 at +6V, verify that the slew rate is greater than 1V/ns for 10MHz stations and greater than .75V/-ns for 5MHz stations.

Repeat test with Option 1 (all pins as clock drivers). Use the same 20 pins as before. Load pins with 100 pf. with E0

at -16V and E1 at +6V, verify that the slew rate is greater than 1V/ns for 10MHz stations and greater than .75V/-ns for 5MHz stations.

For 10MHz stations, check that overshoot/ undershoot on all pins is 100mV for 5V p-p and 300mV for 22V p-p. Check both for data and clock mode. (Data Mode Load, 50pf; Clock Mode Load, 100pf) Use the same 20 pins as before. For 5MHz stations check that overshoot/undershoot on all pins is 300mV for 20V p-p. Check for both Data and Clock Mode using 50pf and 100pf loads respectively.

Check for minimum pulse widths at the 50% points. On a 10MHz test station, minimum pulse width should be 20 ns for a 5V peak-to-peak pulse (-2.5V to +2.5V) and 30 ns for a 22V peak-to-peak pulse (+6V to -16V). One a 5MHz test station, minimum pulse width should be 50 ns for a 20V peak-to-peak pulse (0 to -20V).

G. To test the Pattern Processor (PPM), run the Pattern Processor Diagnostic (PPOD) in Mode C (repeated execution) with a repitition rate of one second for a minimum of ten times. The tests included in this program are as follows:

TEST 1

Read/write the registers associated with PPM.

TEST 2

Test the PPM Control RAM.

TEST 3

Test the address generator which provides the X/Y coordinate addressing.

TEST 4

Test the data generator X and Y parity generators and address comparators.

TEST 5

Test the address and data signals at the test heads.

TEST 6

Test the alternate TG4.

TEST 7

Test the topological RAM memory.

TEST 8

Test the data RAM memory.

TEST 9

Test the Data RAM address, shifter, and pseudo shifter modes.

Execute the Pattern Processor device program P93410 with Load Board 97231028 with Option 5 selected (repeated execution) for a minimum of 10 times. Patterns included in the P93410 are Spiral Complement March, Diagonal March, Checkerboard Complement March, Ping-Pong, Checkerboard Complement March with Refresh, and Checkerboard Complement March with Data Extension.

H. To test the Sequence Processor (SPM), execute the Sequence Processor Diagnostic (SPDG) in Mode R (all tests with internal sync, then all tests with external sync) for a minimum of ten times. The TVFY load board must be mounted for this test. (Mode RL can also be used to give summary on the line printer.)

TEST 1

Terminate Test. Tests for correct local memory termination.

TEST 2

Test each of the local memory commands: LGOTO, LCALL, LEND, LSET, LSETI, LSETIX.

TEST 3

Clock Burst Test.

TEST 4

Loop Counter, Stack, and Stack Pointer Test.

TEST 5

Multi-Level Loop Test.

TEST 6

Continuous Mode Test.

TEST 7

Local Memory Modification Test.

TEST 8

Match Mode Test.

TEST 9

Sequence of Commands Test.

Execute Sequence Processor device program S2533. Select Test Number 0 (all tests) and Option 2 (loop). Use a known good device and load board 97231028. The following tests are included within program S2533:

- Clock Burst Normal.
- Clock burst match by count, DC time, and sequential match of 12.
- Clock burst mix.
- 16 levels of normal subroutines.
- Match mode subroutine by command DC time.

SECTION X

TERMS AND CONDITIONS

10.0 ORDER ACCEPTANCE

These Terms and Conditions of Sale apply to all quotations made and purchase orders accepted by Seller. Acceptance of Buyer's order is on the express condition that these Terms and Conditions of Sale govern. Any other terms and conditions or any changes in these Terms and Conditions of Sale are specifically rejected unless agreed to in writing by Seller's contract administrator.

Prices quoted for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.

10.1 TERMS OF PAYMENT

Domestic (United States)

The equipment will be deemed accepted upon performance by seller of the FST Standard system acceptance procedures at the FST Facility. All invoices are due and payable within thirty (30) days of such acceptance. No discounts are authorized. In the event that installation at the Buyer's facility is not accomplished within thirty (30) days after acceptance at FST unless same is due solely to Seller's failure to act, the Buyer agrees to pay 80% of total amount of the invoice and the remaining 20% shall be paid immediately after installation. Installation at the Buyer's facility shall be deemed accomplished upon completion of FST's standard installation procedures.

If the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may required full or partial payment in advance. In the event of the bankruptcy or insolvency of the Buyer, or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for cost and profit for items so cancelled.

Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payment therefore shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based upon the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer. The seller reserves the right to ship to its order and make collection by sight draft with bill of lading attached

International

All Quotations are made and Orders are accepted on the basis of establishment of an irrevocable letter of credit in United States Dollars available by sight draft upon presentation of copies of the Commercial Invoice, required U.S. Export license(s), Packing List, and Bill(s) of Lading indicating delivery to the appropriate carrier/forwarder.

10.2 F.O.B. POINT

All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon delivery of material to carrier at shipping point in good condition, the carrier acting as Buyer's agent.

Unless instructions from Buyer specify the method of shipment to be used, the Seller will exercise his own discretion, and material will be shipped uninsured. Seller reserves the right to make partial shipments by purchase order line item and invoice therefore.

10.3 DELIVERY

Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any reprocurement costs, consequential or special damages, nor for delay or non-delivery due to acts of God or other causes beyond its reasonable control. In the event of any such delay, the date of delivery shall be deferred for a period equal to the time lost by reason of delay.

10.4 TAXES

The amount of any tax applicable to the products covered by this order or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer. In lieu thereof, the Buyer shall provide a tax exemption certificate acceptable to the taxing authorities.

10.5 PATENTS

The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, Seller shall defend any suit or proceedings brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same. Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing product, or remove said and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof.

10.6 ASSIGNMENT

The Buyer shall not assign his order or any interest herein or any rights thereunder without the prior written consent of Seller.

10.7 WARRANTY

Seller warrants equipment of its manufacture against defective materials or workmanship for a period of one year from date on which Seller determines the installation to be complete.

Seller warrants spare parts of its manufacture against defective materials or workmanship for a period of 30 days from date of shipment.

Buyer's remedies are as follows:

a. Large Systems - repair on-site for 90 days after installation, repair or replacement of defective subassemblies or components returned to FST's factor for the balance of the warranty period.
b. All other Products - repair or replacement of subassemblies or components returned to FST's factor within the warranty period.

This warranty does not extend to expendable items such as lamps, fuses, etc., or mechanical parts failing from normal usage. In the case of accessories not manufactured by Seller, Seller's liability is limited to whatever warranty is extended by the manufacturer and is transferable. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE. In no event shall Seller be liable for consequential or special damages.

10.8 CANCELLATION

Orders placed under a Government prime or subcontract and so identified to Seller may be terminated for convience in accordance with the applicable provisions of ASPR, only in the event of termination of Buyers contract and to the extent this order is directly affected. No other orders may be cancelled without prior agreement between the parties.


FAIRCHILD
SYSTEMS TECHNOLOGY
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION