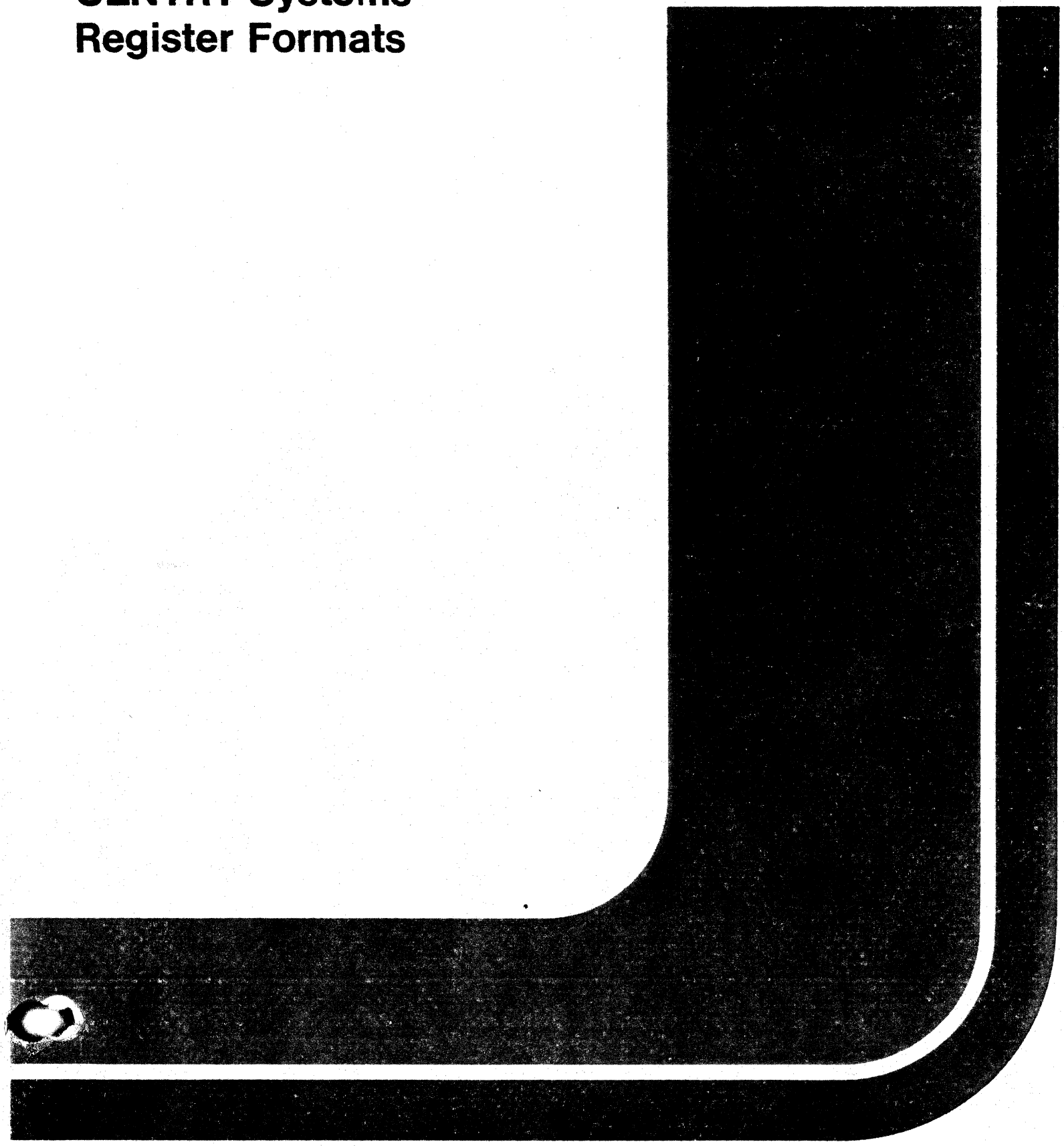
FAIRCHILD

Test Systems Group

SENTRY Systems
Register Formats



SENTRY Systems
Register Formats

Publication Number 67095504

June 1976 Revision 3

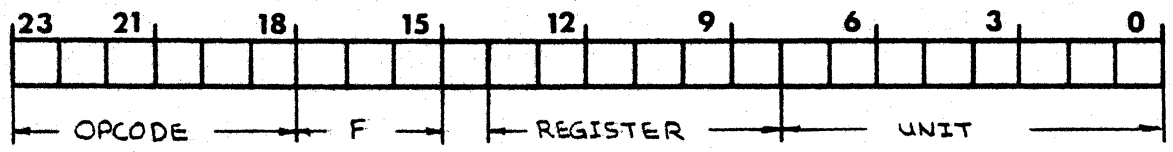
SHORT REGISTER ASSIGNMENT

REGISTER	SYMBOL	NAME	USED BY SYSTEM	USED BY STATION
01	MR	MODE	X	
02	SR	STATUS	X	
03	I	INSTRUCTION	X	
04	MAR	MEMORY ADDRESS	X	
05	TSC	TEST STATION CONTROL	X	
06	--			
07	--			
10	CBC	CLOCK BURST COUNTER		X
11	TD	TIME DELAY		X
12	--			
13	--			
14	IND	INSTRUCTION # DISPLAY	X	
15	INC	INSTRUCTION # COMPARE	X	
16	--			
17	--			
20	--			
21	DPS1	DIG. POWER SUPPLY 1		X
22	DPS2	DIG. POWER SUPPLY 2		X
23	DPT3	TRIP REGISTER 3		X
24	DPS3	DIG. POWER SUPPLY 3		X
25	DPT2	TRIP REGISTER 2		X
26	DPT1	TRIP REGISTER 1		X
27	--			
30	--			
31	--			
32	E1	VOLTAGE REF. SUPPLY		X
33	E0	VOLTAGE REF. SUPPLY		X
34	S1	VOLTAGE REF. SUPPLY		X
35	S0	VOLTAGE REF. SUPPLY		X
36	EA1	VOLTAGE REF. SUPPLY		X
37	EA0	VOLTAGE REF. SUPPLY		X
40	--			
41	--			
42	EB1	VOLTAGE REF. SUPPLY		X
43	EB0	VOLTAGE REF. SUPPLY		X
44	EC1	VOLTAGE REF. SUPPLY		X
45	EC0	VOLTAGE REF. SUPPLY		X
46	SA1	VOLTAGE REF. SUPPLY		X
47	SA0	VOLTAGE REF. SUPPLY		X

I) REGISTER SHORT

II) S-100 THRU S-600 SHORT REGISTERS

III) FORMAT



OPCODE - COMPUTER OPCODE WHICH CAUSES I/O
= 06 SPU FST1 INSTRUCTION

F - FUNCTION
0 = NO OPERATION
2 = REGISTER SPECIAL
4 = WRITE
6 = READ

REGISTER - SPECIFIES 1 OF 64 UNIQUE SHORT REGISTERS

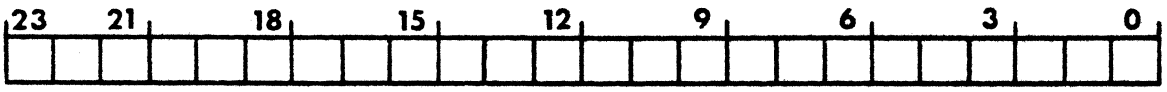
UNIT - THE UNIT ADDRESS OF THE TESTER
= 120B

IV) NOTES
1.) DELAY - REGISTER DEPENDENT
2.) SPECIAL - REGISTER DEPENDENT
3.) THE FORMATS GIVEN FOR THE SHORT REGISTERS IS THE CONFIGURATION OF THE ACCUMULATOR (FST1 A-REGISTER) WHEN A SPU FUNCTION IS EXECUTED.

I) REGISTER 01 MR

II) S-100 THRU S-600 MODE REGISTER

III) FORMAT



R/W	SPARE	B15
R/W	PASS	B14
R/W	FUNCTION FAIL	B13
R/W	TRIP FAIL	B12
R/W	FUNCTION TEST SUS	B11
R/W	DMCRS	B10
W	DMA START	B9
W	FORCE SYNC	B8
W	FORCE STROBE	B7
R/W	STROBE INHIBIT	B6
R/W	ENABLE C LATCH	B5
R/W	NEGATIVE LOGIC	B4
R	AUTO TEST	B3
R	MONITOR MODE	B2
W	RESET LONG REG	B1
W	RESET SHORT REG	B0

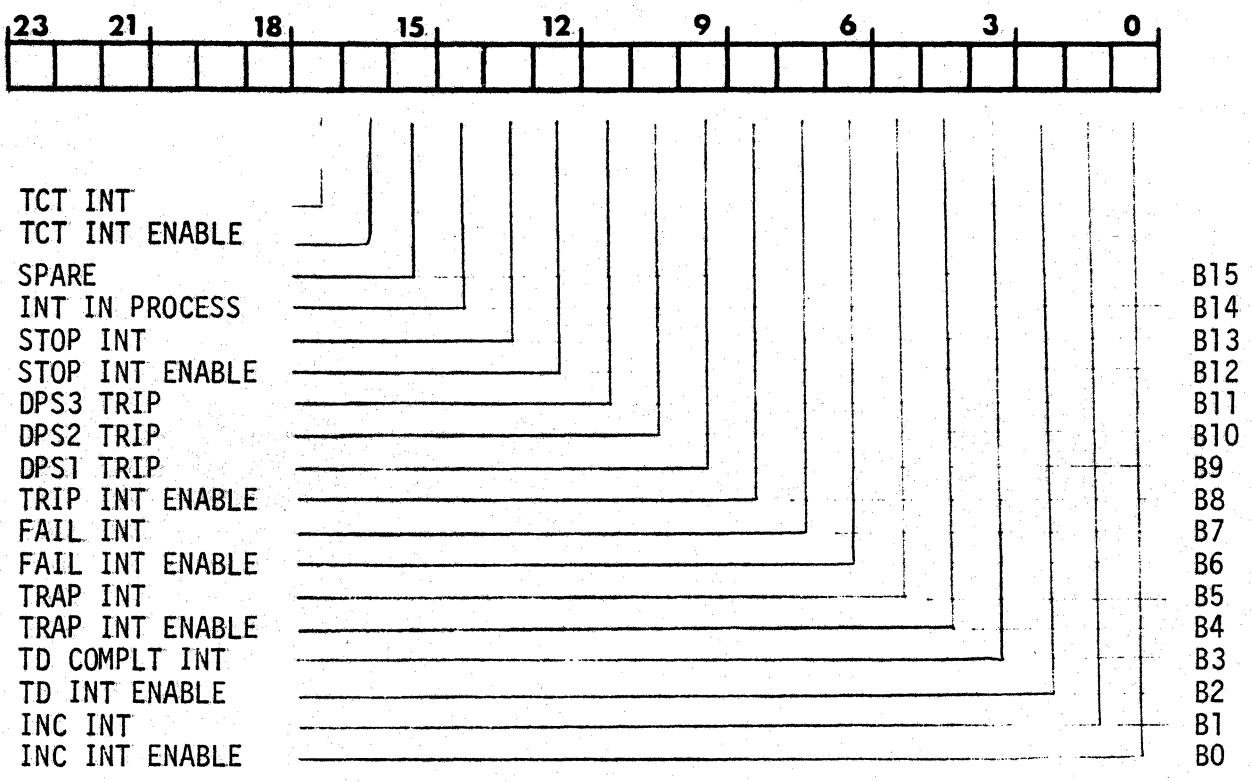
IV) NOTES

1.) DELAY - N/A
2.) MODE SPECIAL CLEAR THE REGISTER
3.) WRITTEN DUE TO THE FACTOR STATEMENTS
   a.) SET LOGIC POS/NEG B4
   b.) ENABLE LATCHES B5
   c.) ENABLE/DISABLE COMPARATORS B6
   d.) FORCE STROBE B7
   e.) FORCE CLOCK B8

I) REGISTER 02 SR

II) S-100 THRU S-600 STATUS REGISTER

III) FORMAT



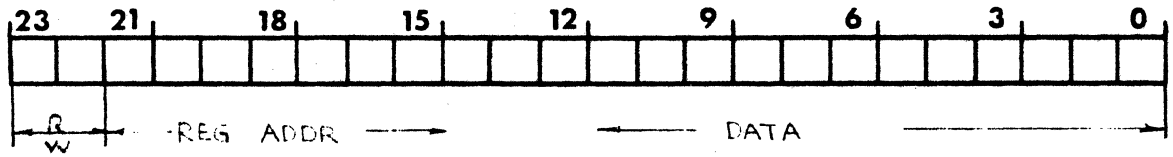
IV) NOTES

1.) DELAY - N/A
2.) STATUS SPECIAL CLEARS B0-B13
3.) THIS REGISTER IS THE INTERRUPT ENABLE AND INTERRUPT SENSE REGISTER.
4.) TRIP CANNOT SET B9-B11 UNLESS DELAY IS COMPLETE

I) REGISTER 03 IR

II) S-100 THRU S-600 INSTRUCTION REGISTER

III) FORMAT



R/W - READ/WRITE COMMUNICATION CODE
00 = WRITE & HOLD B0 - B14
01 = WRITE & EXECUTE BØ - B14
10 = READ BØ - B14

REGISTER ADDRESS - THE ADDRESS OF THE DESIRED LONG REGISTER

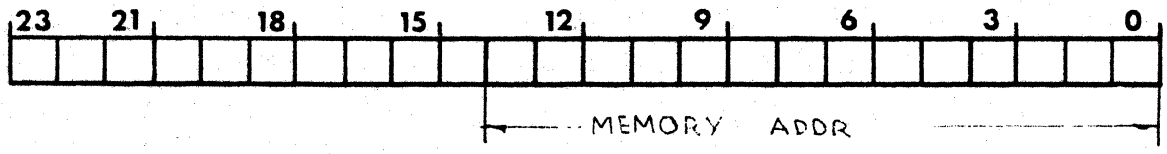
DATA - UP TO 15 BITS OF REGISTER DEPENDENT INFORMATION

IV) NOTES
1.) DELAY - REGISTER DEPENDENT
2.) SPECIAL - N/A
3.) THIS REGISTER IS A BUFFER BETWEEN MEMORY AND THE LONG REGISTERS VIA THE 'B' DATA BUS AND THE CPI
4.) WRITE AND EXECUTE IN DMA MODE ADVANCES INSTRUCTION NUMBER COUNTER (IND) AND WAITS FOR TESTER NOT BUSY.

I) REGISTER 04 MAR

II) S-100 THRU S-600 MEMORY ADDRESS REGISTER

III) FORMAT



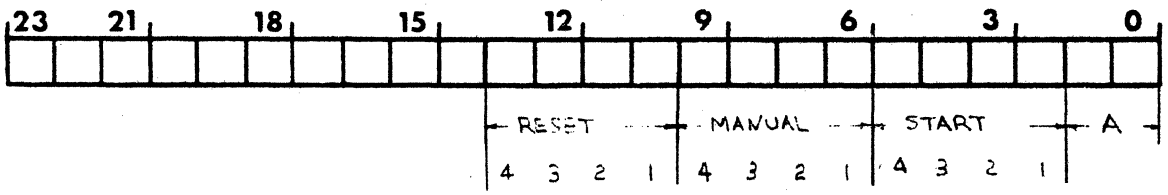
MEMORY ADDRESS - THE CPU MEMORY ADDRESS FROM WHICH WORDS ARE TO BE SENT TO THE TESTER VIA DMA $8192 \leq MAR \leq 16383$

IV) NOTES
1.) DELAY - N/A
2.) SPECIAL - N/A
3.) DMA RATE = 1.75 (1 + N) μs, N = NUMBER OF WORDS
4.) MAR IS AUTOMATICALLY UPDATED.

I) REGISTER 05 TSC

II) S-100 THRU S-600 TEST STATION CONTROL REGISTER

III) FORMAT



RESET, MANUAL, START - FROM CONSOLE PUSHBUTTONS
FOR TEST STATIONS 1, 2, 3, and 4

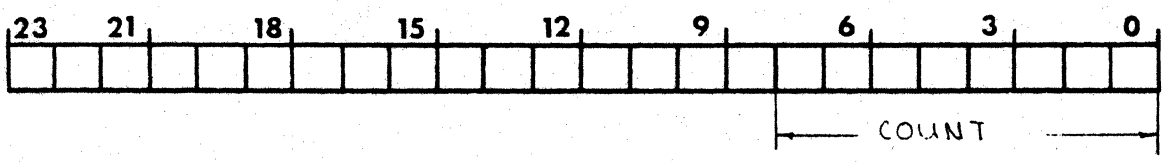
A - STATION ADDRESS
00 = STATION 1
01 = " 2
10 = " 3
11 = " 4

IV) NOTES
1.) DELAY - 3 DLS
2.) SPECIAL - N/A
3.) RESET AND START ARE WRITABLE ONLY BY ADDRESSING THE ASSOCIATED STATION

I) REGISTER 10 CBC

II/ S-100/200 CLOCK BURST COUNTER REGISTER

III) FORMAT



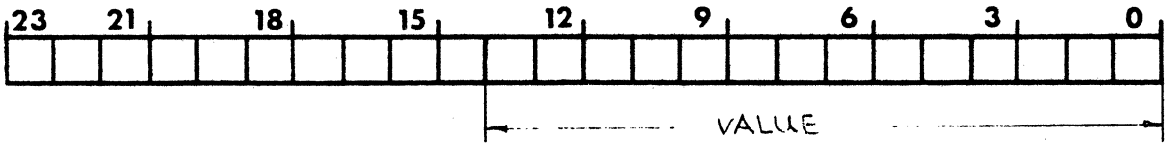
COUNT - THE NUMBER OF CLOCK SYNCS GENERATED PER FUNCTION TEST.

IV) NOTES
1.) DELAY - N/A
2.) SPECIAL - N/A
3.) GENERATED BY THE FACTOR STATEMENT
a.) SET CLOCK (INTP)

I) REGISTER 11 TD

II) S-100 THRU S-600 TIME DELAY REGISTER

III) FORMAT



VALUE $0 \leq$ VALUE $\leq$ 16383

DURING DMA FOR FUNCTIONAL TEST DELAY
BØ = 0.35µs F.S. = 5.734ms

INTERPRETIVELY FOR DC DELAY
BØ = 0.35ms F.S. = 5.734s

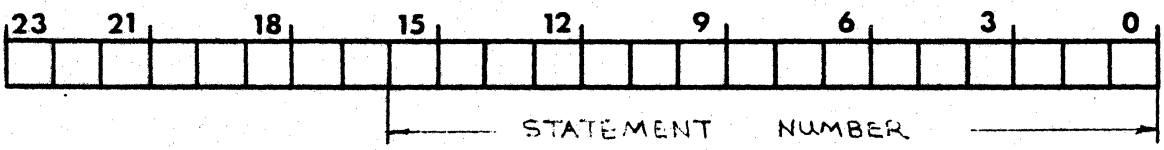
IV) NOTES
1.) DELAY - N/A
2.) TD SPECIAL STARTS THE DELAY COUNTDOWN
3.) GENERATED BY THE FACTOR STATEMENTS.
a.) SET DELAY (INTP)
b.) SET DELAY, DC (INTP)
4.) TIME DELAY COUNTDOWN IS STARTED BY:

a.) SET F
b.) ENABLE TRIPI
c.) FORCE VOLTAGE/CURRENT
d.) FORCE PMU
e.) ENABLE TRIPV
f.) MEASURE NODE
g.) FORCE E(X)0/1
h.) SET S0/S1
i.) FORCE VF
j.) FORCE DELAY
k.) FORCE IF

I) REGISTER 14 IND

II) S-100 THRU S-600 INSTRUCTION NUMBER DISPLAY COUNTER

III) FORMAT



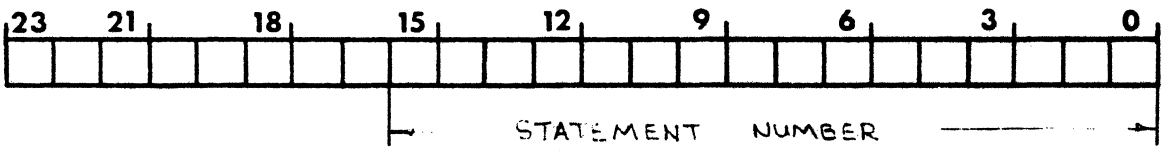
STATEMENT NUMBER - THE SEQUENTIAL NUMBER OF THE FACTOR STATEMENT UNDER EXECUTION

IV) NOTES
1.) DELAY - N/A
2.) SPECIAL - INCREMENTS THE COUNTER ONE
3.) IS ALSO INCREMENTED IN DMA WHEN B23 & 22 = 01, WRITE AND EXECUTE, ARE SET
4.) SOFTWARE LIMITED TO 15 BITS

I) REGISTER 15 INC

II) S-100 THRU S-600 INSTRUCTION NUMBER COMPARE &
SYNC ON STATEMENT NUMBER

III) FORMAT



STATEMENT NUMBER - THE FACTOR STATEMENT AT WHICH A COMPARE
INTERRUPT OR SYNC PULSE OCCURS

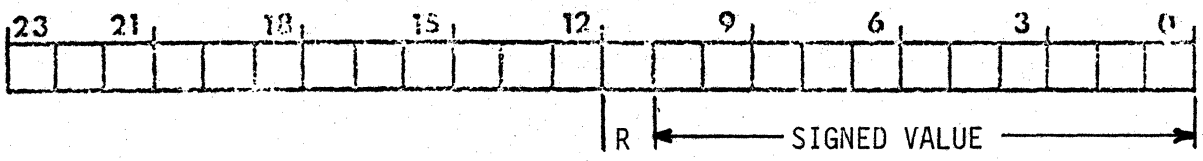
IV) NOTES
1.) DELAY - N/A
2.) SPECIAL - N/A
3.) A COMPARE INTERRUPT IS GENERATED IF THE INC INTERRUPT
IS ENABLED, ELSE A SYNC PULSE OCCURS.

I) REGISTER 21, 22, 24 DPS

II) S-100 THRU S-600 DIGITALLY PROGRAMMED POWER SUPPLIES

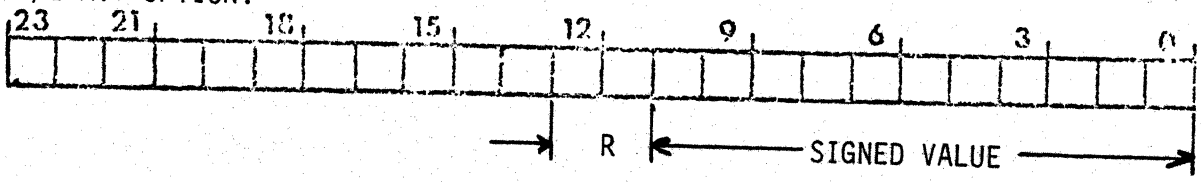
III) FORMAT

STANDARD:



R - RANGE	LSB	F.S.
Ø =	10 MV	±10 V
1 =	40 MV	±40 V

2V/2 MV OPTION:



R - RANGE	LSB	F.S.
Ø1 =	2 MV	± 2 V
1Ø =	10 MV	±10 V
11 =	40 MV	±40 V

SIGNED VALUE - -1024 VALUE 1023

THE VALUE OF THE VOLTAGE BEING FORCED OR THE VOLTAGE TRIP POINT.

IV. NOTES

1) DELAY - 3 DLS
2) SPECIAL - DISCONNECTS THE SUPPLY (NO DELAY IS INITIATED).
3) MUST BE USED IN CONJUNCTION WITH THE DPT REGISTERS
4) DPS1 = REGISTER 21
   DPS2 = REGISTER 22
   DPS3 = REGISTER 24

5) GENERATED BY THE FACTOR STATEMENTS

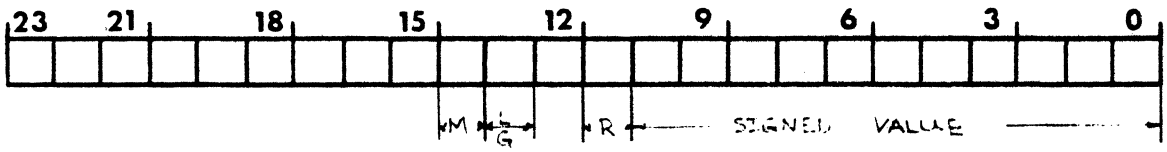
a) FORCE VF (X)
b) ENABLE TRIPV (X)

6) DPS W CONNECTS THE UNIT TO THE LOAD BOARD.

I) REGISTER 23, 25, 26 DPT

II) S-100 THRU S-600 DPS TRIP REGISTERS

III) FORMAT



M - MODE
0 = VOLTAGE FORCE/CURRENT TRIP
1 = CURRENT FORCE/VOLTAGE TRIP

L/G - LESS THAN/GREATER THAN
0 = LESS THAN
1 = GREATER THAN

R - RANGE	LSB	F.S.
0 =	100μa	100ma
1 =	1ma	1A

SIGNED VALUE - $-1024 \leq \text{VALUE} \leq 1023$
THE VALUE OF THE CURRENT BEING FORCED OR THE CURRENT TRIP POINT

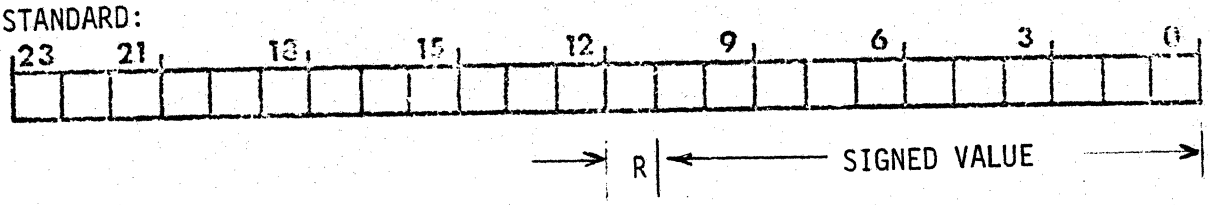
IV) NOTES
1.) DELAY - 3 DLS
2.) SPECIAL - N/A
3.) MUST BE USED IN CONJUNCTION WITH THE DPS REGISTERS
4.) DPT1 = REGISTER 26
5.) DPT2 = " 25
DPT3 = " 23
5.) GENERATED BY THE FACTOR STATEMENTS.
a.) FORCE IF(x)
b.) ENABLE TRIP (x)

I) REGISTER 32-37, 42-47 RVS

II) S-100 THRU S-600 REFERENCE VOLTAGE SUPPLIES

III) FORMAT

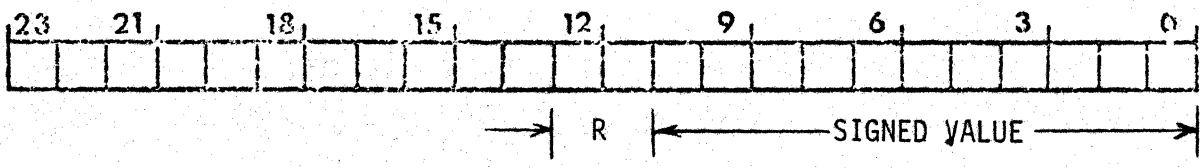
STANDARD:



R - RANGE	LSB	F.S.
Ø =	10 MV	±10 V
1 =	40 MV	±40 V

R - RANGE	LSB	F.S.
Ø =	10 MV	± 10 V
1 =	40 MV	± 40 V

2V/ 2MV OPTION:



R - RANGE	LSB	F.S.	
Ø1 =	2 MV	±2 V	(max 6V - hardware
10 =	10 MV	±10 V	(max 30V - hardware)
11 =	40 MV	±40V	

SIGNED VALUE - -1024 VALUE 1023

THE VALUE OF THE VOLTAGE BEING FORCED

IV) NOTES

1) DELAY - 1 DLS
2) SPECIAL - N/A
3) GENERATED BY THE FACTOR STATEMENTS
   a) FORCE E (X) Ø / 1
   b) SET SØ / S1, SA Ø / SA1

LONG REGISTER ASSIGNMENT

REGISTER	SYMBOL	FUNCTION	USED BY SYSTEM	S-100/200	S-500/600
000-003	RZ	RETURN TO ZERO			X
010-013	ST	STROBE			X
020-027	DA	INPUT PIN DEF.		X	X
030-033	DB	ALT. INPUT PIN DEF.			X
040-047	MA	MASK PIN CARE		X	X
050-053	MB	ALT. MASK PIN CARE			X
060-077	F	FUNCTION		X	X
100-107	S	PRIMARY/ALT. SELECT		X	X
110-113	TG1	TG PIN ADDR 2^0			X
120-127	C/I	C/I COMPARE STORAGE/INVERT REG	X		
130-133	TG2	TG PIN ADDR 2^1			X
140-147	R	UTILITY RELAY		X	X
150-153	TG3	TG PIN ADDR 2			X
160	PA	PMU PIN ADDR		X	X
161	SID	SOCKET ID		X	
162	SND	STATEMENT # DISPLAY	X		
163	CS/TR	CLOCK & STROBE/TEST RATE		X	X
164	PPS	PMU FORCE		X	X
165	PSL	PMU SENSE/CLAMP		X	X
166	EIR	EXTERNAL INTERFACE	X	X	X
167	STSC	SLAVE TSC	X		
170	BMA	BUFFER MEMORY ADDR	X		X
171	DCT	PMU DC COMPARE		X	X
172	CH	CHAINING			X
173	MODE	STATUS & MODE A/B/C/D/LRAX	X	X	X
174	PG	PATTERN GENERATOR			X
175	PW	TG PULSE WIDTH			X
176	PD	TG PULSE DELAY			X
177	PPA	POWER PIN ADDR			X
177	V	TG VERNIER			X

NOTE: A REGISTER is considered to be used by the SYSTEM when a FUNCTION is not station dependent. This occurs when the REGISTER must be READ or WRITTEN due to:

1.) The REGISTER is not on the SYSTEM Reset line and must be preset, by software, to some value.
2.) When the FUNCTION is not directly related to a FACTOR statement; e.g. EIR must be written at each manual STEP, PAUSE, and EOT.
3.) When the REGISTER must be READ to supply information to the software for control or information.

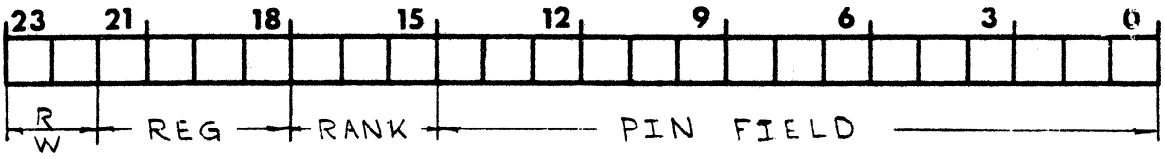
LONG REGISTER PARTICULARS

REGISTER	SYMBOL	MODE			DELAY GENERATED
		SYSTEM	DMA	INTP	
000-003	RZ		X		0
010-013	ST		X		0
020-027	DA		X		1 DLS
030-033	DB		X		1 DLS
040-047	MA		X		0
050-053	MB		X		0
060-077	F		X	X	TD
100-107	S		X	X	.5 DLS
110-113	TG1		X		0
120-127	C/I	X			0
130-133	TG2		X		0
140-147	R		X		1 DLS
150-153	TG3		X		0
160	PA		X	X	1 DLS
161	SID			X	1 DLS
162	SND	X			0
163	CS			X	0
163	TR			X	0
164	PPS		X	X	1 DLS
165	PSL		X	X	1 DLS
166	EIR	X		X	1 DLS
167	STSC	X			1 DLS
170	BMA	X	X	X	0
171	DCT		X	X	0
172	CH			X	0
173	MODE	X			0
174	PG			X	0
175	PW			X	0
176	PD			X	1 DLS
177	PPA		X		1 DLS
177	V			X	1 DLS

I) REGISTER 000-157 OVERVIEW

II) S-100 thru S-600 PIN DEFINITION REGISTERS

III) FORMAT



R/W - READ/WRITE COMMUNICATION CODE
- 00 = WRITE BØ-B14 AND HOLD
- 01 = WRITE BØ-B14 AND EXECUTE
- 10 = READ BØ-B14

REG - REGISTER ADDRESS

RANK - A GROUP OF 15 PINS
- 0 = PINS 1-15
- 1 = PINS 16-30
- 2 = PINS 31-45
- 3 = PINS 46-60
- 4 = PINS 61-75
- 5 = PINS 76-90
- 6 = PINS 91-105
- 7 = PINS 106-120

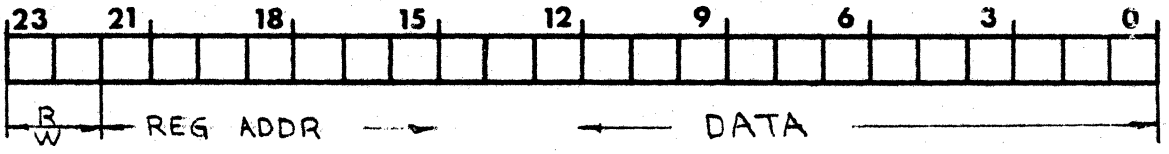
PIN FIELD BØ = PINS 1/16/31/46 etc.
B1 = PINS 2/17/32/47 etc.
etc.
B14 = PINS 15/30/45/60 etc.

IV) NOTES
1.) DELAY - DEPENDENT ON REGISTER ADDRESS
2.) THESE REGISTERS ARE NORMALLY WRITTEN IN DMA MODE
3.) A WRITE & EXECUTE CAUSES IND (14) TO BE INCREMENTED, A WRITE & HOLD DOES NOT.
4.) S-200, $0 \leq$ RANK ≤ 7 FOR 120 PIN CAPABILITY
5.) S-100/500/600 $0 \leq$ RANK ≤ 3 FOR 60 PIN CAPABILITY

I) REGISTER 160-177 OVERVIEW

II) S-100 THRU S-600 SPECIFIC FUNCTION REGISTERS

III) FORMAT



R/W - READ/WRITE COMMUNICATION CODE
  00 = WRITE BØ-B14 AND HOLD
  01 = WRITE BØ-B14 AND EXECUTE
  10 = READ BØ-B14

REGISTER ADDRESS
  NORMALLY B21-B15 (REGISTER + RANK = ADDRESS)
  IN OTHER CASES, B14 THRU B12 ARE USED AS REGISTER ADDRESS
  EXTENSION TO PROVIDE MULTIPLE SUB-REGISTERS

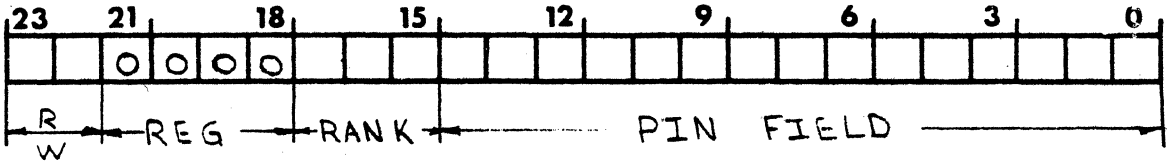
DATA-REGISTER DEPENDENT INFORMATION

IV) NOTES
1.) DELAY - DEPENDENT ON REGISTER ADDR

I) REGISTER 00 RZ

II) S-500/600 RETURN TO ZERO REGISTER

III) FORMAT



RANK - $0 \leq \text{RANK} \leq 3$

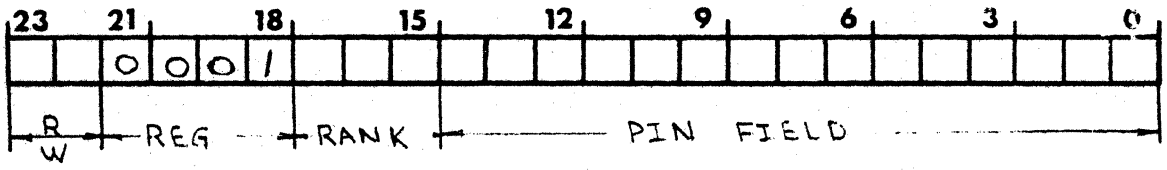
PIN FIELD BØ = PIN 1/16/31/46
0 = NRZ
1 = RZ

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET RZ binary pattern (DMA)
b.) CONN CLK pin list (DMA)

I) REGISTER 01 ST

II) S-500/600 TG8 STROBE SELECT REGISTER

III) FORMAT



RANK - $0 \leq RANK \leq 3$

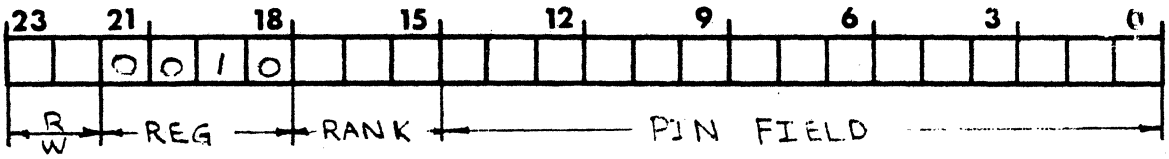
PIN FIELD BØ = PIN 1/16/31/46
0 = TG7
1 = TG8

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET STROBE binary pattern (DMA)

I) REGISTER 02 D,DA

II) S-100 thru S-600 INPUT/OUTPUT PIN DEFINITION REGISTER

III) FORMAT



RANK S-100/500/600 $0 \leq RANK \leq 3$
S-200 $0 \leq RANK \leq 7$

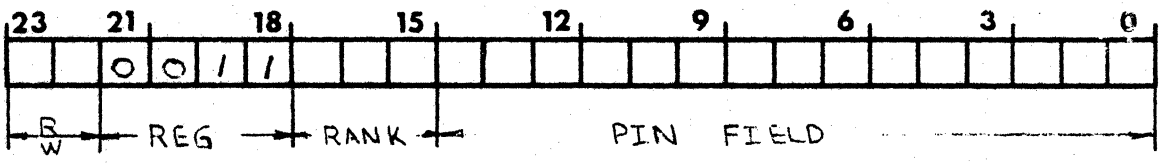
PIN FIELD BØ = PIN 1/16/31/46
0 = OUTPUT PIN
1 = INPUT PIN

IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED by the FACTOR statements
a.) SET D binary pattern S-100/200 (DMA)
b.) SET DA binary pattern S-500/600 (DMA)

I) REGISTER 03 DB

II) S-500/600 ALTERNATE INPUT/OUTPUT PIN DEFINITION REGISTER

III) FORMAT



RANK $0 \leq RANK \leq 3$

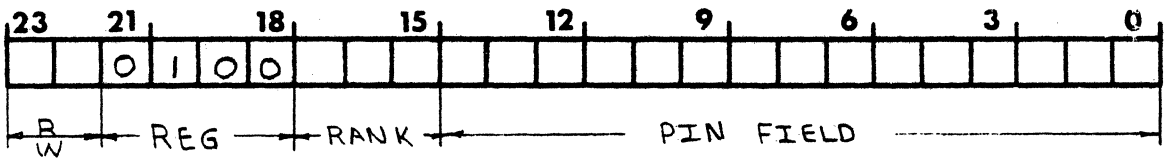
PIN FIELD BØ = PIN 1/16/31/46
0 = OUTPUT PIN
1 = INPUT PIN

IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED by the FACTOR statement
a.) SET DB binary pattern (DMA)

I) REGISTER 04 M,MA

II) S-100 THRU S-600 MASK PIN CARE/DONT CARE REGISTER

III) FORMAT



RANK S-100/500/600 $0 \leq RANK \leq 3$
S-200 $0 \leq RANK \leq 7$

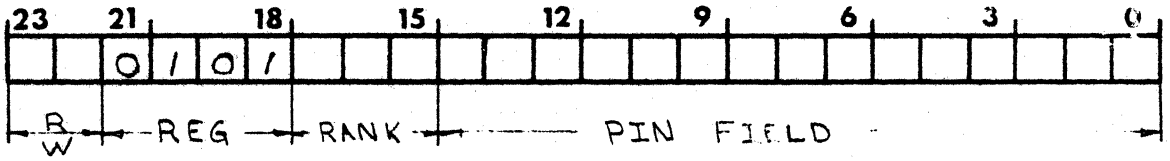
PIN FIELD BØ = PIN 1/16/31/46
0 = DONT CARE
1 = CARE

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
a.) SET M binary pattern S-100/200 (DMA)
b.) SET MA binary pattern S-500/600 (DMA)

I) REGISTER 05 MB

II) S-500/600 ALTERNATE MASK PIN CARE/DONT CARE REGISTER

III) FORMAT



RANK $0 \leq \text{RANK} \leq 3$

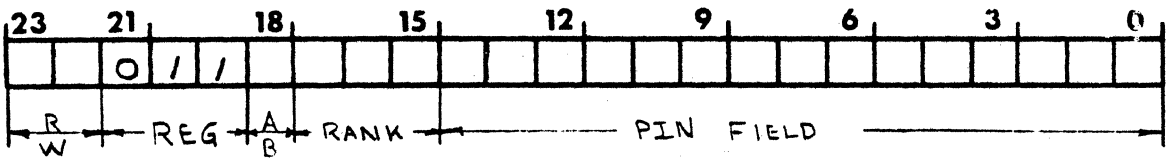
PIN FIELD BØ = PIN 1/16/31/46
0 = DONT CARE
1 = CARE

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
a.) SET MB binary pattern (DMA)

I) REGISTER 06 F

II) S-100 thru S-600 FUNCTIONAL TEST PATTERN

III) FORMAT



S-100/200 BIT 18 = Ø

S-500/600

A/B MA/MB DA/DB REGISTER SELECTION
FOR RANK = 0
0 = DA
1 = DB
FOR RANK = 1
0 = MA
1 = MB

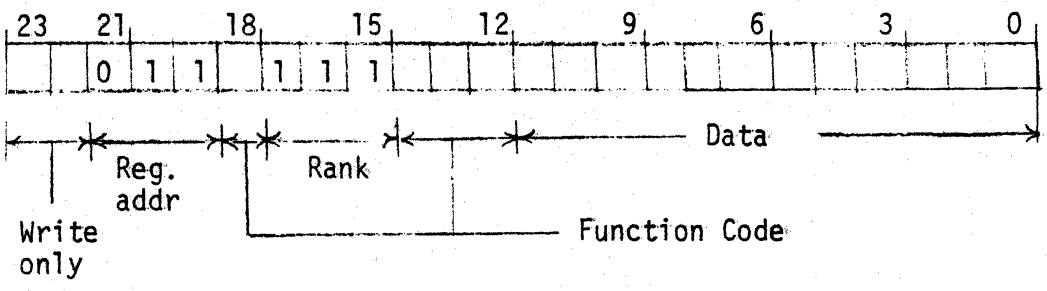
PIN FIELD BØ = PIN 1/16/31/46
0 = LOGIC 0
1 = LOGIC 1 in conjunction with the definition Register D
D = Ø = EXPECTED OUTPUT
D = 1 = FORCING FUNCTION

IV) NOTES
1.) DELAY - 700ns + SET DELAY exp
2.) GENERATED by the FACTOR statement
a.) SET F binary pattern (DMA)
b.) SET FI binary pattern S500/600 (INTP)

I) REGISTER 067 F- RANK 8

II) S-670 (Sequence Processor Option)

III) FORMAT



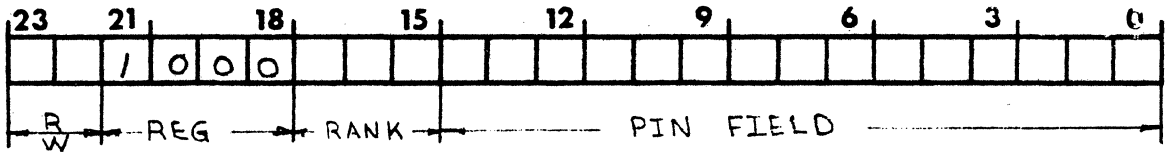
Func Code	Data	Factor Statement
00		NOT ALLOWED
01	4 (OPCODE OF INVERT REG.)	LSET IX
02		SPARE
03	OPCODE OF REGISTERS	LOADING REGISTERS ON-THE-FLY
	1 (STROBE REG.)	LSET STROBE
	2 (RZ REG.)	LSET RZ
	3 (XOR REG.)	LSET XOR
	4 (INVERT REG.)	LSET I
	5 (TGA0 REG.)	LCGEN
	6 (TGA1 REG.)	LCGEN
	7 (TGA2 REG.)	LCGEN
	10 (DB)	LSET DB
	11 (DA)	LSET DA
	12 (MB)	LSET MB
	13 (MA)	LSET MA
04	LOCAL MEMORY ADDR.	SET F - LCALL
05	LOCAL MEMORY ADDR.	LSET IX - LCALL
06	LOCAL MEMORY ADDR.	SET F -LGOTO
07	LOCAL MEMORY ADDR.	SET F - LEND
10	LOOP COUNT	LSUBR (NORMAL)
11	LOOP COUNT	LSUBR MATCH
12	LOOP COUNT	LSUBR CONTIN
13		SPARE
14	CLOCK BURST COUNT	SET FC (NORMAL)
15	CLOCK BURST COUNT	SET FC MATCH
16	ALL ONE'S	SET FC CONTINUOUS
17		SPARE

These are all DMA instructions.

I) REGISTER 10 S

II) S-100 thru S-600 PRIMARY/ALTERNATE DATA/CLOCK RVS SELECTOR

III) FORMAT



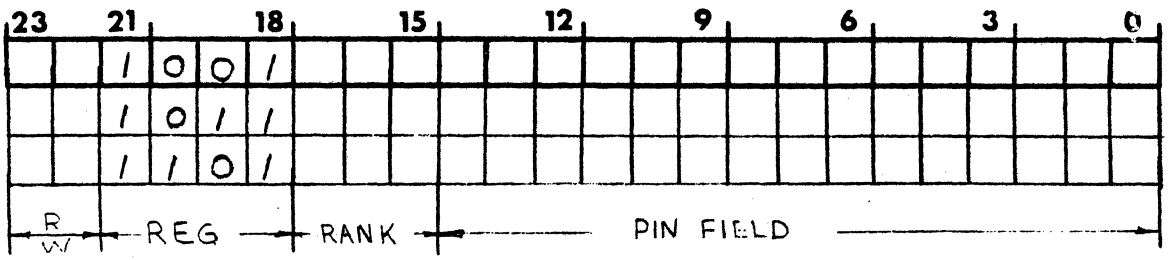
PIN FIELD BØ = PIN 1/16/31/46
0 = SELECT PRIMARY DATA/CLOCK REFERENCE PAIRS
1 = SELECT ALTERNATE DATA/CLOCK REFERENCE PAIRS

IV) NOTES
1.) DELAY - .5DLS
2.) GENERATED BY THE FACTOR STATEMENT
a.) SET S BINARY PATTERN (DMA)
b.) SET SI BINARY PATTERN S-500/600 (INTP)

I) REGISTER 11, 13, 15 TGAØ, TGA1, TGA2

II) S-500/600 TIMING GENERATOR PIN ADDRESS REGISTERS

III) FORMAT



RANK $\leq$ 0 $\leq$ RANK 3

PIN FIELD BØ = PIN 1/16/31/46
READING VERTICALLY

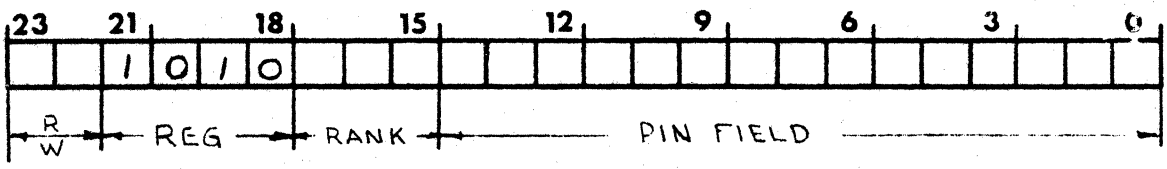
TGA2	A1	AO	
0	0	0	NO TIMING GENERATOR ASSIGNED
0	0	1	TG1
0	1	0	TG2 THRU
1	1	0	TG6
1	1	1	OR OF TG 1 AND TG 2

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
a.) CGEN TG(x) pin list (DMA)

I) REGISTER 12 C/INVERT

II) S-100 THRU S-600 FUNCTIONAL COMPARE STORAGE REGISTER
FUNCTIONAL DATA INVERT REGISTER

III) FORMAT



READ:
PIN FIELD BØ = PIN 1/16/31/46--ETC
0 = FUNCTIONAL TEST PASS
1 = FUNCTIONAL TEST FAIL

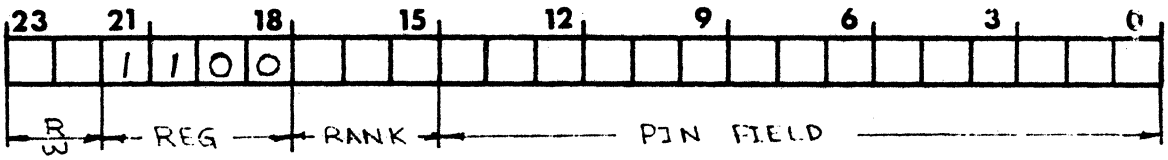
WRITE:
PIN FIELD BØ = PIN 1/16/31/46--ETC
0 = F DATA NORMAL
1 = F DATA INVERTED

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the SYSTEM in D/L

I) REGISTER 14 R

II) S-100 THRU S-600 UTILITY RELAY REGISTER

III) FORMAT



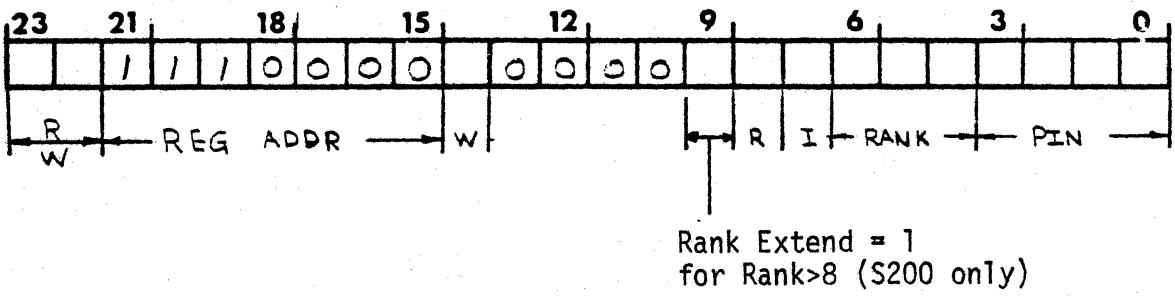
PIN FIELD BO = PIN 1/16/31/46
0 = UTILITY RELAY OPEN
1 = UTILITY RELAY CLOSE

IV) NOTES
1.) DELAY - 1DLS
2.) GENERATED by the FACTOR statement
a.) SET R binary pattern (DMA)

I) REGISTER 160 PA

II) S-100 THRU S-600 NEW PMU PIN ADDRESS REGISTER

III) FORMAT



W = WRITE PROTECT
= Ø B8 - B13 ARE WRITE PROTECTED
= 1 BØ - B7 ARE WRITE PROTECTED

R = RELAY (CONNECT DRIVER AND PMU)
= Ø DISABLE RELAY - DISCONNECTION
= 1 ENABLE RELAY - CONNECTION

I = INTERNAL NODE
= Ø NOT INTERNAL NODE
= 1 THE VALUE OF BØ - B7 IS AN INTERNAL NODE

RANK, ONE OF EIGHT 15 PIN GROUPS

PIN , 1 - 15 pin #/RANK SPECIFIED
RANK Ø, PIN Ø = PMU - PIN DISCONNECTION

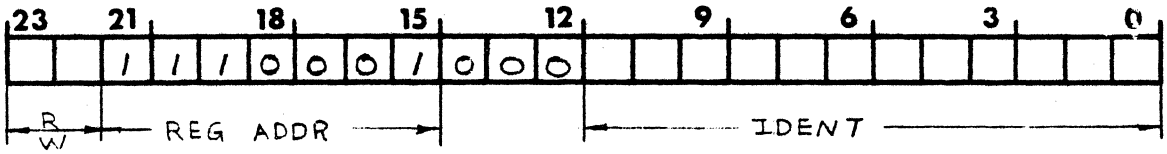
IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED by FACTOR statements:
a.) GPMU PIN exp. (DMA & INTP)
b.) XPMU PIN (DMA)
c.) ENABLE/DISABLE RELAY (DMA)
d.) MEASURE NODE # (INTP)

3.) THIS REGISTER IS DUPLICATED IN THE MAINFRAME FOR INTERNAL NODES

I) REGISTER 161 SID

II) S-100/200 - SOCKET IDENTIFICATION

III) FORMAT - READ ONLY



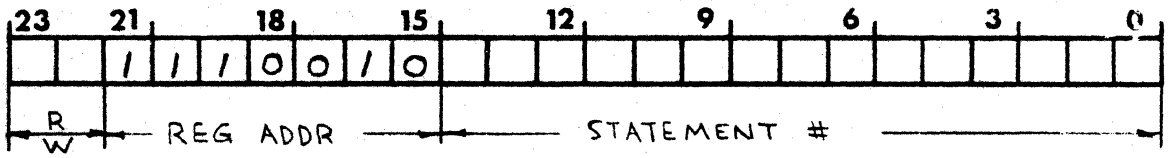
IDENT - IS THE HARD WIRED VALUE ON THE LOAD BOARD

IV) NOTES
1.) DELAY - 1 DLS
2.) A READ is GENERATED by the FACTOR statement
a.) SOCKET ID number (INTP)

I) REGISTER 162 SND

II) S-100/200 - STATEMENT NUMBER DISPLAY

III) FORMAT



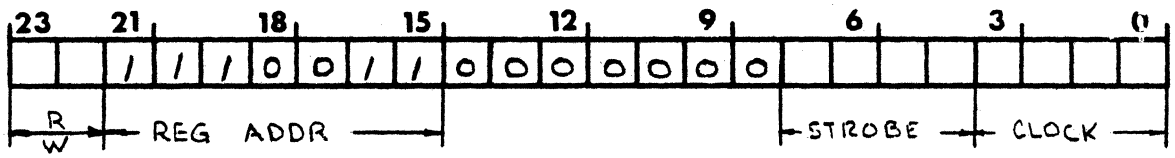
STATEMENT # IS A FULL 15 BITS - 32K

IV) NOTES
1.) DELAY - N/A
2.) A WRITE is GENERATED by the SYSTEM AT
a.) EACH MANUAL STEP
b.) EACH PAUSE
c.) END OF TEST

I) REGISTER 163 CS, TR

II) S-100/200 CLOCK & STROBE REGISTER
S-500/600 FUNCTIONAL TEST RATE REGISTER

III) FORMAT - S-100/200 CLOCK & STROBE



STROBE B4 = TESTER PIN 1
B5 = TESTER PIN 2
B6 = TESTER PIN 3
B7 = TESTER PIN 4

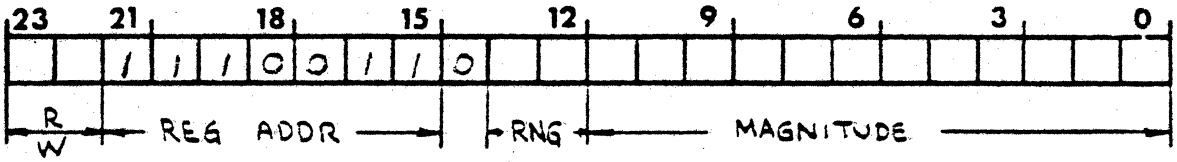
CLOCK BØ = TESTER PIN 1
B1 = TESTER PIN 2
B2 = TESTER PIN 3
B3 = TESTER PIN 4

IV) NOTES
1.) DELAY - N/A
2.) GENERATED BY FACTOR STATEMENTS
a.) ENABLE CLOCK binary pattern (INTP)
b.) ENABLE STROBE binary pattern (INTP)
3.) B8 - B14 UNUSED AND NOT DECODED
4.) COMPARATORS MUST BE DISABLED WHEN STROBE IS ENABLED.
5.) THE CLOCK ADDRESS BITS ARE ANDed WITH THE FIRST FOUR BITS OF THE F REGISTER TO GENERATE CLOCK SYNC SIGNALS.

I) REGISTER 163 CS, TR

II) S-100/200 CLOCK & STROBE REGISTER
S-500/600 FUNCTIONAL TEST RATE REGISTER

III) FORMAT - S-500/600 FUNCTIONAL TEST RATE



RNG = RANGE (10ns for 10MHz) (20ns for 10 MHz)

00 = RNGØ	BØ = 20ns	FS = 80µs
01 = RNG1	BØ = 100ns	FS = 400µs
10 = RNG2	BØ = 1µs	FS = 4ms
11 = RNG3	BØ = 10µs	FS = 40ms

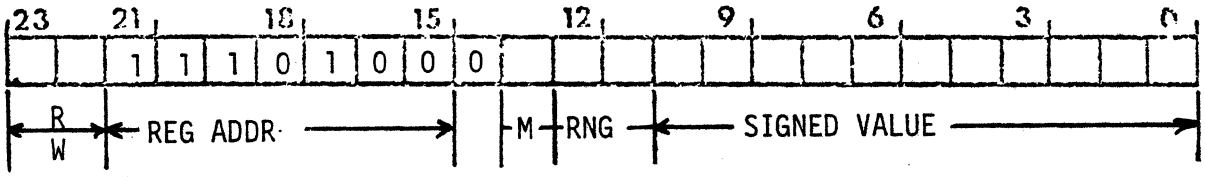
MAGNITUDE - 12 BIT POSITIVE VALUE
$1 \leq$ VALUE ≤ 4095

IV) NOTES
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENT
a.) SET PERIOD exp. (INTP)
3.) B14 UNUSED
4.) MINIMUM VALUE FOR RANGE Ø IS 200ns (5 MHz)
5.) MINIMUM VALUE FOR RANGE Ø IS 100ns (10 MHz)

I) REGISTER 164 PPS

II) S-100 THRU S-600 NEW PMU FORCE (PRECISION POWER SELECT) REGISTER

III) FORMAT



M - MODE

Ø = CURRENT FORCE

1 = VOLTAGE FORCE

RNG - RANGE	B12-11	LSB	FULL SCALE
CURRENT RANGE	Ø (00)	1na	±1μa
	1 (01)	100na	±100μa
	2 (10)	10μa	±10ma
	3 (11)	100μa	±100ma
VOLTAGE RANGE	1 (01)	1mv	±1v(STANDARD)
	1 (Ø1)	2mv	±2v (for the 2V/2MV OPTION)
	2 (10)	10mv	±10v
	3 (11)	40mv	±40v
	4 (00)	100mv	+ or - 100v
SIGNED VALUE	-1024 ≤ V ≤ + 1023		

IV) NOTES

1.) DELAY - 1 DLS to 5 ms

2.) GENERATED BY THE FACTOR STATEMENTS
   a.) FORCE VOLTAGE EXP. (DMA & INTP)
   b.) FORCE CURRENT EXP. (DMA & INTP)
   c.) FORCE PMU EXP. (INTP)

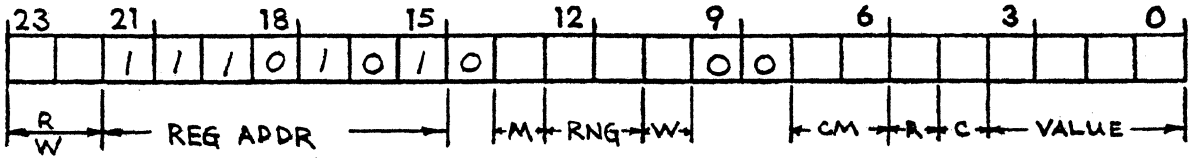
d.) SET PMU FORCEI/V (INTP)
e.) MEASURE NODE # (INTP)

3.) VOLTAGE RANGE 4 EXISTS FOR S-500/600 ONLY

I) 165 PSL

II) S-100 THRU S-600 NEW PMU PRECISION SENSE LEVEL REGISTER

III) FORMAT



M - SENSE MODE - READ ONLY (SET BY PPS)
0 = CURRENT SENSE
1 = VOLTAGE SENSE

RNG - SENSE RANGE		B12-11	LSB	FULL SCALE
CURRENT SENSE RANGE	Ø	(00)	1na	±1μa
	1	(01)	100na	±100μa
	2	(10)	10μa	10ma
	3	(11)	100μa	100ma
VOLTAGE SENSE RANGE	1	(01)	1mv	±1v (STANDARD)
	1	(01)	2mv	2v (FOR THE 2v/2mv)
	2	(10)	10mv	±10v
	3	(11)	40mv	±40v
	4	(00)	100mv	+ or - 100v

W - WRITE LOCKOUT

= 0 B8 - B13 ARE WRITE PROTECTED
= 1 BØ - B7 ARE WRITE PROTECTED

CM - VOLTAGE CLAMP MODE
= 00 SYMMETRICAL (SYM)
= 01 POSITIVE (POS)
= 10 NEGATIVE (NEG)

C - CLAMP ON/OFF INDICATOR
0 = OFF
1 = ON

VALUE - ONE OF 16 CLAMP VALUES

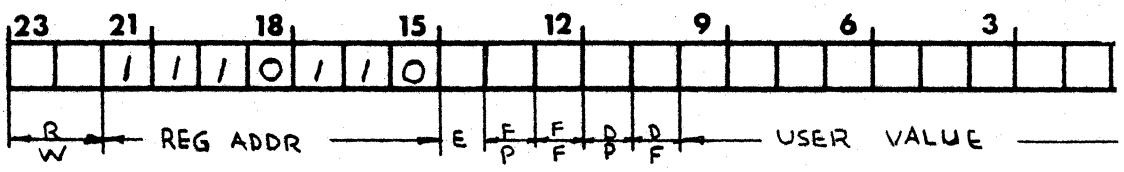
IV) NOTES

1.) DELAY - 1 DLS to 5ms
2.) GENERATED BY FACTOR STATEMENTS
    a.) MEASURE (VALUE/NODE) (INTP)
    b.) SET PMU SENSE (INTP)
    c.) SET CLAMP (DMA)
    d.) SET DCT LT/GT EXP (DMA)
3.) VOLTAGE RANGE 4 EXISTS FOR S-500/600 ONLY
4.) B13 IS READ ONLY AND IS THE COMPLIMENT OF THE MODE BIT (B13) WRITTEN TO THE PPS REGISTER.

I) REGISTER 166 EIR

II) S-100 THRU S-600 EXTERNAL INTERFACE REGISTER

III) FORMAT



E- END OF TEST
1 = EOT

F/P, 1 = FUNCTIONAL TEST PASS
F/F, 1 = FUNCTIONAL TEST FAIL
D/P, 1 = DC/TRIP TEST PASS
D/F, 1 = DC/TRIP TEST FAIL

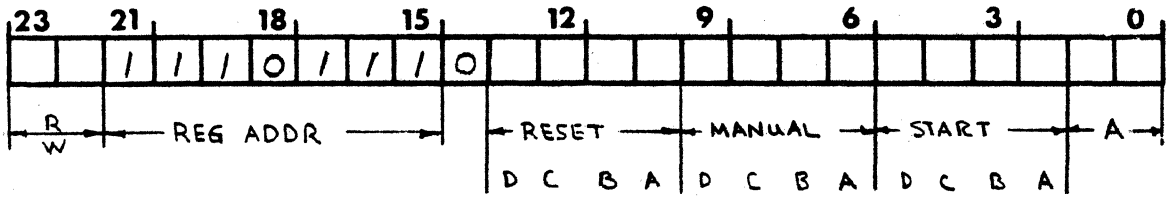
USER VALUE - USER WRITTEN EXTERNAL INFORMATION

IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED BY THE FACTOR STATEMENT
a.) WRITE (EIR) BINARY PATTERN (INTP)
3.) ALSO WRITTEN BY THE SYSTEM AT
a.) Each manual step
b.) EACH PAUSE
c.) END OF TEST

I) REGISTER 167 STSC

II) S-100 THRU S-600 MUX SLAVE TEST STATION CONTROL REGISTER

III) FORMAT



RESET, MANUAL, START - FROM CONSOLE PUSHBUTTONS
FOR TEST HEADS A, B, C, D

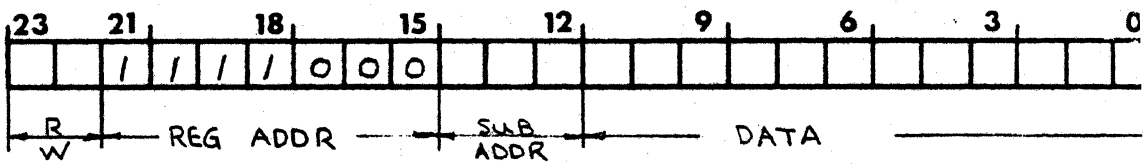
A - SUB-STATION ADDRESS
00 = HEAD A
01 = HEAD B
10 = HEAD C
11 = HEAD D

IV) NOTES
1.) DELAY - 1 DLS
2.) SYSTEM GENERATED
3.) THIS REGISTER IS DIRECTED TO 1 OF 4 MAIN STATION BY WRITING THE TEST STATION CONTROL REGISTER (TSC)
4.) WRITING A SUB-STATION ADDRESS PUTS THAT TEST HEAD ON-LINE.

I) REGISTER 170 BMA

II) S-500/600 BUFFER MEMORY ADDRESS REGISTERS

III) FORMAT



SUB-ADDRESS, THIS REGISTER IS DIVIDED INTO 8 SUB-REGISTERS OF 12 BITS EACH

SUB-ADDRESS

Ø	-	S ,	TEST START ADDRESS; MAD, DELAYED MEMORY ADDR
1	-	M ,	MINOR LOOP COUNT
2	-	N ,	MAJOR LOOP COUNT
3	-	MCS,	MAIN FRAME ACCESS
4	-	J ,	MINOR LOOP START ADDRESS
5	-	K ,	MINOR LOOP END ADDRESS
6	-	L ,	MAJOR LOOP AND TEST END ADDRESS
7	-	IF ,	IGNORE FAIL ADDRESS

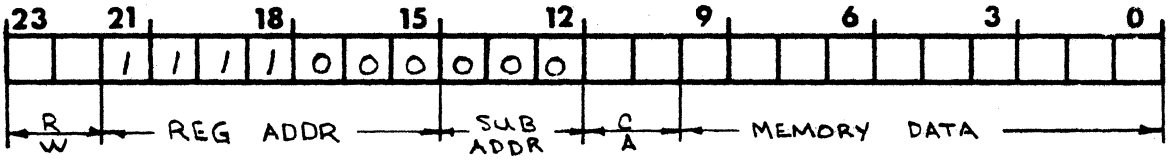
IV) NOTES

1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENTS
   a.) SET START exp (DMA & INTP)
   b.) AT exp (DMA & INTP)
   c.) SET MINOR (DMA & INTP)
   d.) SET MAJOR (DMA & INTP)
   e.) ENABLE TEST (DMA & INTP)
3.) GENERATED BY THE SYSTEM
4.) THESE REGISTERS ARE NOT ON THE SYSTEM RESET LINE.
5.) FOR THOSE REGISTERS WHICH PERMIT CHAIN ADDRESSING, THE APPROPRIATE BITS IN REGISTER SAMB (1734) MUST BE SET TO PROVIDE THE CHAIN FUNCTION.

I) REGISTER 1700 BMA - S, MAD

II) S-500/600 LOCAL MEMORY TEST START REGISTER (WRITE)
DELAYED MEMORY ADDR (READ)

III) FORMAT



C/A - CHAIN ADDRESS
00 = NO CHAIN ADDRESS
10 = CHAIN TWO ADDRESS
11 = CHAIN FOUR ADDRESS

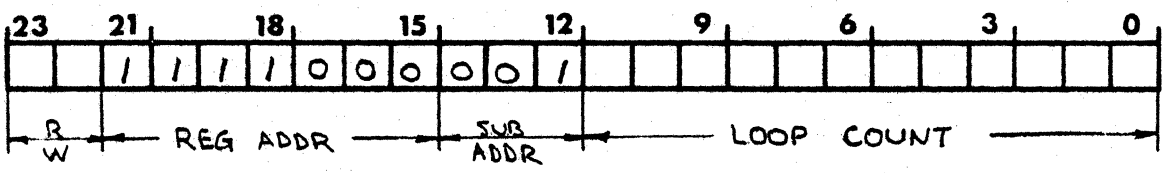
MEMORY ADDRESS
WRITE - TEST START ADDRESS IN LOCAL MEMORY
READ - LOCAL MEMORY LOCATION ON WHICH FUNCTIONAL EXECUTION STOPPED, PASS OR FAIL

IV) NOTES
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENTS
a.) SET START exp (DMA & INTP)
b.) ENABLE TEST (DMA & INTP)
3.) SYSTEM GENERATED BY DYNAMIC D/L
4.) THIS REGISTER IS NOT HARDWARE RESTORED.

I) REGISTER 1701 BMA - M

II) S-500/600 LOCAL MEMORY MINOR LOOP COUNT REGISTER

III) FORMAT



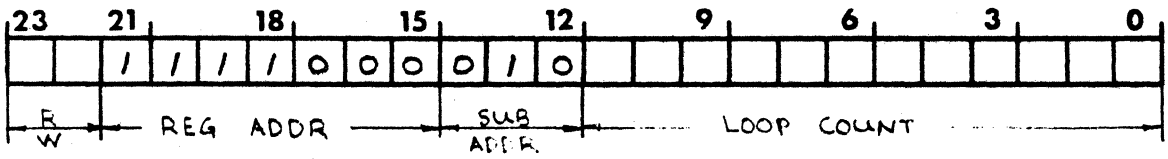
LOOP COUNT - THE NUMBER OF JUMPS FROM K TO J
$0 \leq \text{COUNT} \leq 4095$

IV) NOTES
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENT
a.) SET MINOR (DMA & INTP)

I) REGISTER 1702 BMA-N

II) S-500/600 LOCAL MEMORY MAJOR LOOP COUNT REGISTER

III) FORMAT



LOOP COUNT - THE NUMBER OF JUMPS FROM L to Ø

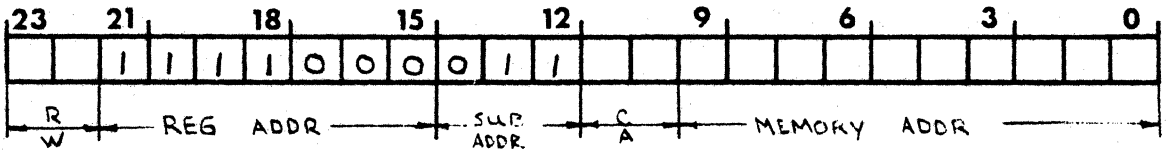
$0 \leq \text{COUNT} \leq 4095$

IV) NOTES
1) DELAY - N/A
2) GENERATED BY the FACTOR statement
a.) SET MAJOR (DMA & INTP)
3) THIS REGISTER IS NOT HARDWARE RESTORED

I) REGISTER 1703 BMA-MCS

II) S-500/600 LOCAL MEMORY MAIN FRAME ACCESS

III) FORMAT - WRITE ONLY



C/A = CHAIN ADDRESS
= 00 - NO CHAIN ADDRESS
= 10 - CHAIN TWO ADDRESS
= 11 - CHAIN FOUR ADDRESS

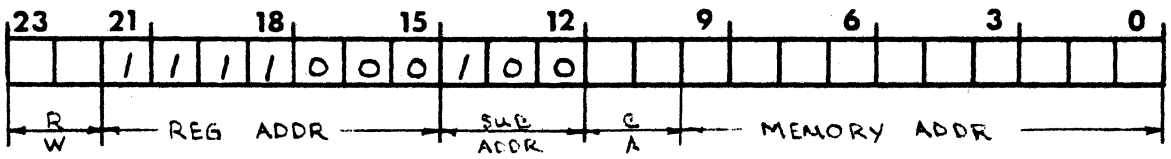
MEMORY ADDRESS -
DEFINES LOCAL MEMORY ADDRESS TO WHICH SUCCEEDING FUNCTIONAL PATTERNS (SET F's) WILL BE LOADED

IV) NOTES
1) DELAY - N/A
2) GENERATED by the FACTOR Statements
a.) AT exp (DMA & INTP)
b.) ENABLE TEST (DMA)
3) WRITE ONLY

I) REGISTER 1704 BMA-J

II) S-500/600 LOCAL MEMORY MINOR LOOP START ADDRESS

III) FORMAT



C/A - CHAIN ADDRESS
00 - NO CHAIN ADDRESS
10 - CHAIN TWO ADDRESS
11 - CHAIN FOUR ADDRESS

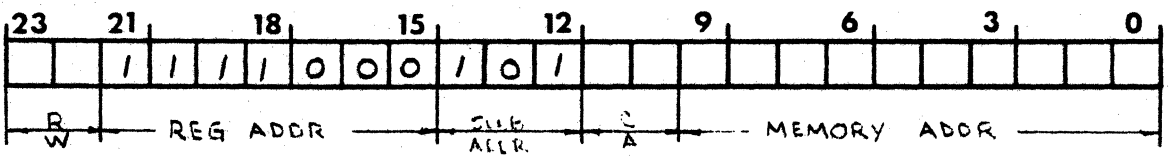
MEMORY ADDRESS -
DEFINES THE MINOR LOOP START ADDRESS
WITHIN LOCAL MEMORY.

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET MINOR (DMA & INTP)

I) REGISTER 1705 BMA-K

II) S-500/600 LOCAL MEMORY MINOR LOOP END ADDRESS

III) FORMAT



C/A - CHAIN ADDRESS
00 - NO CHAIN ADDRESS
10 - CHAIN TWO ADDRESS
11 - CHAIN FOUR ADDRESS

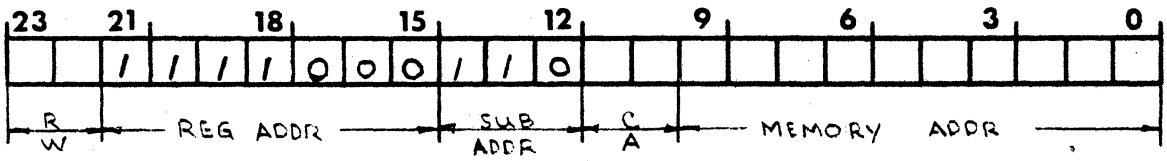
MEMORY ADDRESS
DEFINES THE MINOR LOOP END ADDRESS
WITHIN LOCAL MEMORY

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET MINOR (DMA & INTP)

I) REGISTER 1706 BMA-L

II) S-500/600 LOCAL MEMORY MAJOR LOOP END ADDRESS & TEST END ADDRESS

III) FORMAT



C/A - CHAIN ADDRESS
00 - NO CHAIN ADDRESS
10 - CHAIN TWO ADDRESS
11 - CHAIN FOUR ADRRESS

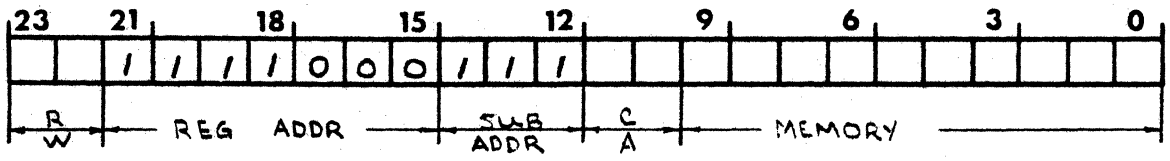
MEMORY ADDRESS
DEFINES THE MAJOR LOOP END OR TEST
END ADDRESS WITHIN LOCAL MEMORY

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
a.) SET MAJOR (DMA & INTP)
b.) ENABLE TEST (DMA)

I) REGISTER 1707 BMA-IF

II) S-500/600 LOCAL MEMORY IGNORE FAIL REGISTER OR PATTERN GENERATOR ENABLE REGISTER

III) FORMAT



C/A - CHAIN ADDRESS
- 00 - NO CHAIN ADDRESS
- 10 - CHAIN TWO ADDRESS
- 11 - CHAIN FOUR ADDRESS

MEMORY ADDRESS

1.) FAILS ARE IGNORED UP TO AND INCLUDING THE LOCAL MEMORY ADDRESS SPECIFIED IF B8 IS ALSO SET IN REGISTER SAMA (1730)

2.) DEFINES THE ADDRESS AT WHICH THE PATTERN GENERATOR IS ENABLE IF B3 IS ALSO SET IN REGISTER SAMB (1734)

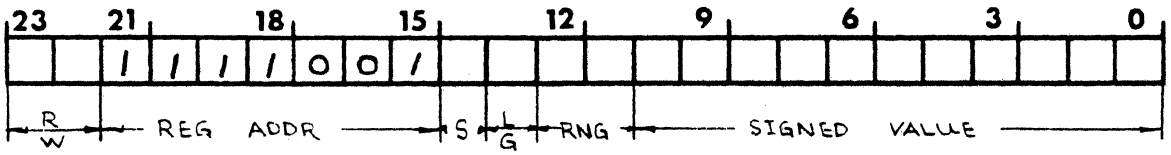
IV) NOTES

1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
   a.) SET PGENE exp (INTP)
   b.) ENABLE TEST
3.) GENERATED by system for DYNAMIC D/L

I) REGISTER 171 DCT

II) S-100 THRU S-600 NEW PMU HARDWARE COMPARE REGISTER

III) FORMAT



S - DC STROBE
1 = CAUSE A STROBE ALSO WRITE LOCKOUT OF BØ-B13

L/G - LESS THAN / GREATER THAN
0 - LESS THAN
1 - GREATER THAN

RNG - RANGE (SENSE) READ ONLY
SET BY WRITING SENSE RANGE IN PSL (165) REGISTER

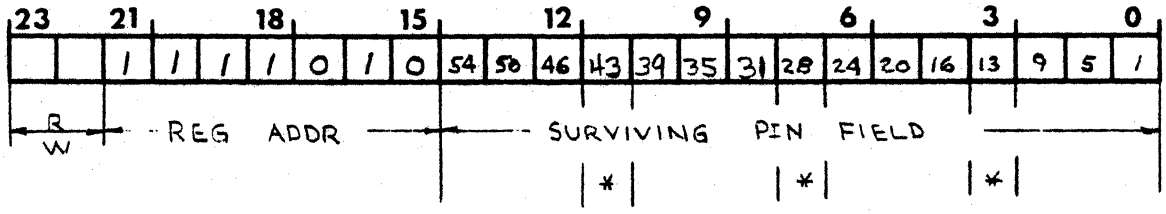
SIGNED VALUE - PASS/FAIL LIMIT

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET DCT LT/GT exp.
3.) A DC strobe also occurs on a READ

I) REGISTER 172 CH

II) S-500/600 CHAINING REGISTER

III) FORMAT



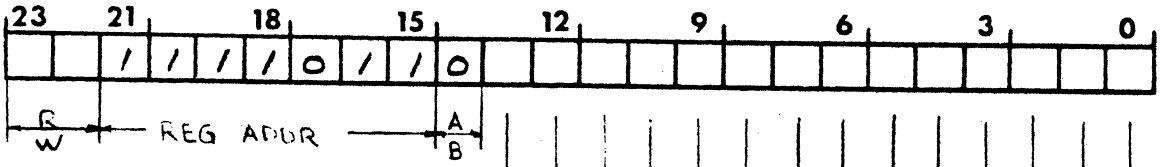
SURVIVING PIN FIELD
THESE ARE THE PINS TO WHICH THE NEXT ASCENDING PINS ARE CHAINED
CHAIN TWO - ALL THOSE SHOWN
CHAIN FOUR - ALL THOSE SHOWN EXCEPT THOSE INDICATED BY THE *

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET CHAIN TWO/FOUR binary pattern (DMA)
b.) SET IOMODE pin list (INTP)

I) REGISTER 173 SAMA (173Ø)

II) S-100 THRU S-600 STATUS AND MODE REGISTER A

III) FORMAT



R/W	CONTINUOUS LOOP MODE	B13
R/W	ENABLE FAIL IN CONT. LOOP	B12
R	MEMORY SIZE B	B11
R	MEMORY SIZE A	B10
R/W	RANK LOAD MODE	B9
R/W	ENABLE IGNORE FAIL	B8
R/W	DC FAIL INTERUPT ENABLE	B7
R/W	FC FAIL INTRUPT ENABLE	B6
R	DC FAIL	B5
R	FC FAIL	B4
R	CONTINUOUS LOOP STATE	B3
R/W	MOMENTARY MODE	B2
R/W	MATCH MODE, NO MATCH	B1
R/W	BSY/BUSY	BØ

IV) NOTES

1) DELAY - N/A
2) GENERATED by the FACTOR statements
   a.) ENABLE TEST BØ & B6
   b.) ENABLE TEST CONTINUOUS BØ, B6, & B13
   c.) ENABLE TEST MOMENTARY BØ, B2, & B6
   d.) ENABLE TEST MATCH BØ, B1, & B6
3) LOCAL MEMORY SIZE

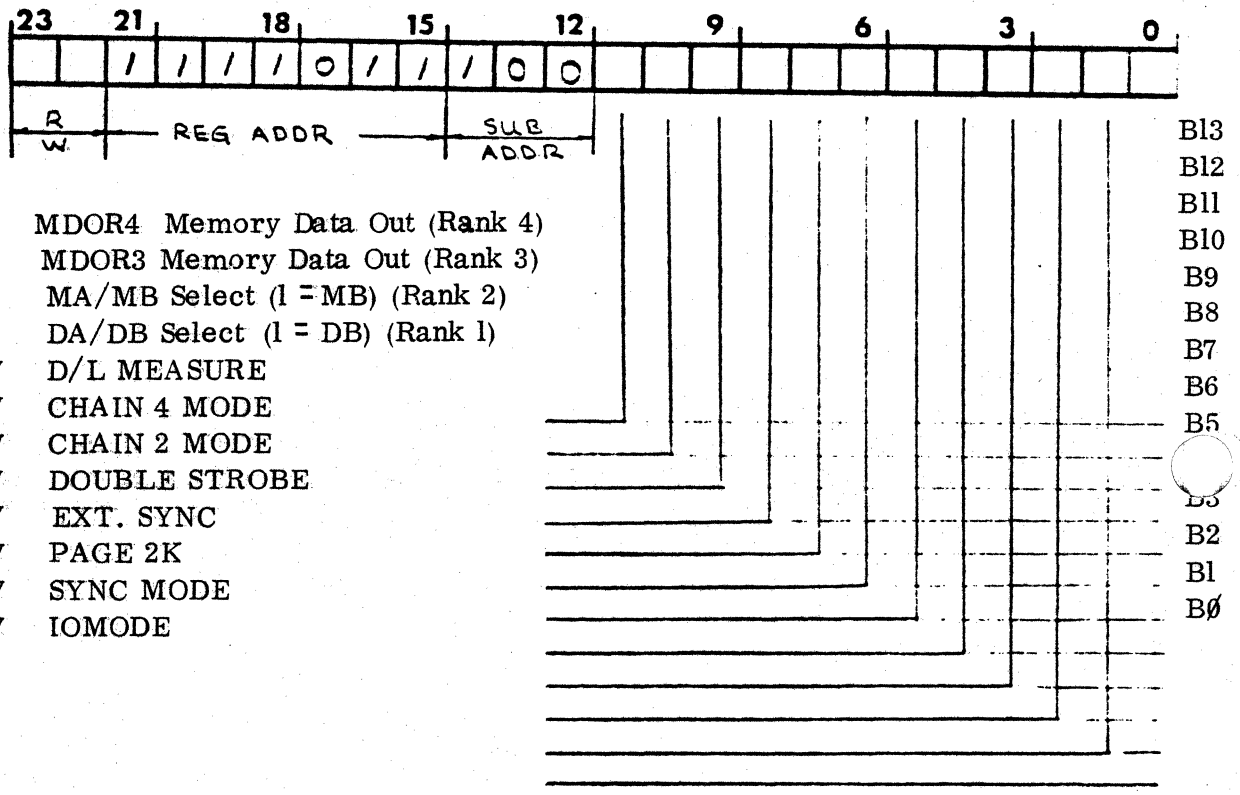
(B2(SAMC)	B10	B11	5MHz	10MHz
1	1	1	256	512
1	0	1	512	1024
1	0	0	1024	2048
0	0	0	N/A	4096

4) MATCH MODE SENSE
   BØ & B1 = 1 = STILL IN MATCH MODE
   BØ OR B1= Ø = MATCH MODE REQUESTED AND NO MATCH FOUND
5) BØ WRITE BSY (LOCAL MEMORY GO)
   READ BUSY (TESTER BUSY)

I) REGISTER 173 SAMB (1734)

II) S-100 THRU S-600 STATUS AND MODE REGISTER B

III) FORMAT



R	MDOR4 Memory Data Out (Rank 4)
R	MDOR3 Memory Data Out (Rank 3)
R	MA/MB Select (1 = MB) (Rank 2)
R	DA/DB Select (1 = DB) (Rank 1)
R/W	D/L MEASURE
R/W	CHAIN 4 MODE
R/W	CHAIN 2 MODE
R/W	DOUBLE STROBE
R/W	EXT. SYNC
R/W	PAGE 2K
R/W	SYNC MODE
R/W	IOMODE

IV) NOTES

1.) DELAY - N/A

2.) GENERATED by the FACTOR statements

a.) ENABLE DOUBLE STROBE — B4

b.) SET CHAIN TWO/FOUR — B5 & B6

c.) SET PGENE exp — B3

3.) SYSTEM GENERATED BY

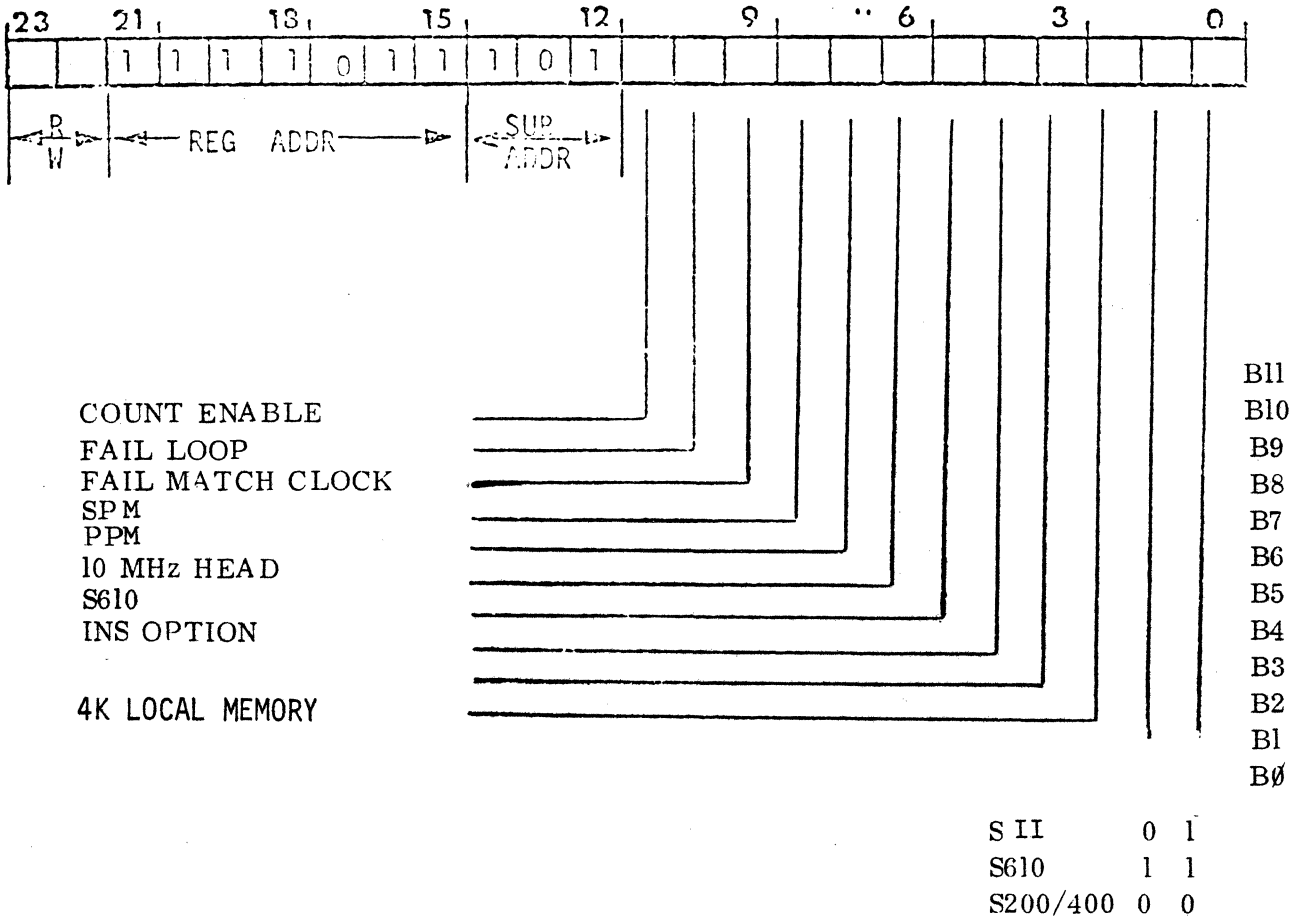
a.) /. DATALOG MEASURE — B7

b.) CHECK STATION TYPE — BØ

I) REGISTER 173 SAMC (1735)

II) S-100 THRU S-600 STATUS AND MODE REGISTER C

III) FORMAT



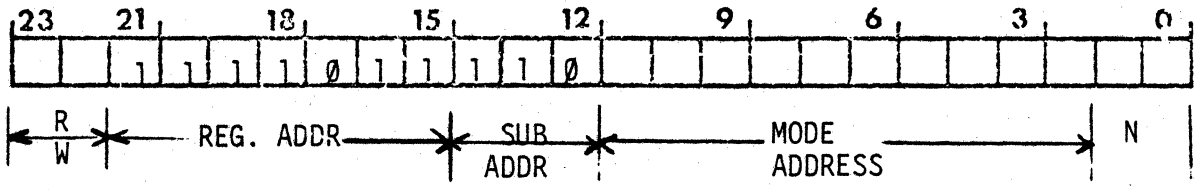
IV) NOTES

1) BITS 0,1,2,3,4,5,6,7,8, and 9 ARE READ ONLY
2) BIT 11 IS WRITE AND READ. (S II and up)
3) BIT 1Ø ON WRITE IS FAIL LOOP ENABLE.
   ON READ IS FAIL MATCH LOOP.

I) REGISTER 173 SAMD (1736)

II) S-600 ONLY STATUS AND MODE REGISTER D

III) FORMAT



MODE ADDR	DESCRIPTION	INVOKED BY:
Ø	Data	
1	Data Spare	
2	PPO Programmed Stop	/. STOP ON/OFF (Analysis)
3	PPO Programmed Loop	/. LOOP ON/OFF (Analysis)
4	Split Cycle Mode	ENABLE/DISABLE SPLIT (DMA)
5	Load Alternate Timing Registers	SET APERIOD (INTP) SET ATG4 WIDTH/DELAY (INTP)
6	PPO - Local Memory Address Mode	
7	PPO Data Bit Extension	DEX 1/Ø (RASM) (DMA)
10	Disable Return To One	ENABLE/DISABLE RTO (DMA)
11	Enable Muxing of F Data	ENABLE/DISABLE MUXMODE (DMA)
12	1 Conditioning PIN vs 3 Controlled Pins	SET IOM3 (INTP)
13	Mask Input Pins	ENABLE/DISABLE IMASK (DMA)
14	SPO	SET PAGE, SPO (INTP)
15	Alternate Match Mode	ENABLE TEST AMATCH (INTP)
16	P4K (SAMD 71)	SET PAGE 4096

17	SPM Momentary	ENABLE TEST MOMENTARY in an SPM program (DMA)

N = 1 for setting the respective mode.
= Ø for resetting the respective mode.

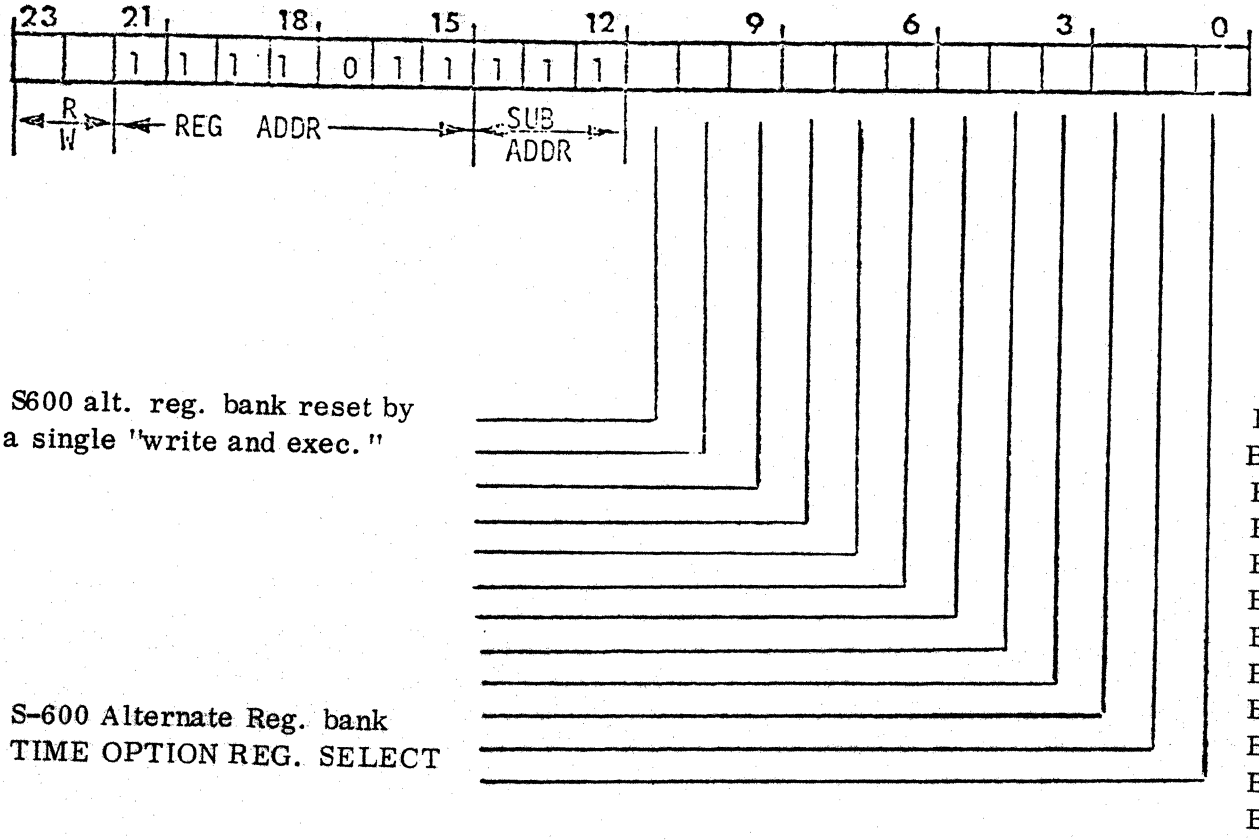
IV) NOTES

1) None of the modes are readable.
2) Mode addresses from 20 to 77 and 121 to 1777 are unassigned.
3) Bit 1 is unused and must be set to Ø.
4) Mode addresses 100 to 120 are reserved for use by C.P.E.

I) REGISTER 173 LRAX (1737)

II) S-600 ONLY LONG REGISTER ADDRESS EXTEND (SAM-E)

III) FORMAT



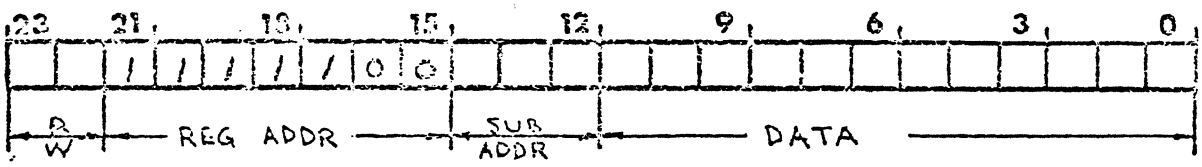
① S-600 Alternate Reg. bank TIME OPTION REG. SELECT

① SELECT AND HOLD

I) REGISTER 174 PG

II) S-500/600 PATTERN GENERATOR REGISTERS

III) FORMAT



SUB-ADDRESS, THIS REGISTER IS DIVIDED INTO 5 SUB-REGISTERS OF 12 BITS EACH.

SUB-ADDRESS DATA

Ø - THE DATA FIELD CONTAINS THE MEMORY INSTRUCTION TO EXECUTE AND GOES TO THE PG MEMORY ADDRESS SPECIFIED BY THE PCNTR

1 - PG MEMORY ADDR COUNTER PCNTR
2 - DEVICE MEMORY SIZE -1, 2"-1, N=# OF ADDR LINES
3 - FUTURE OPTION, DEVICE MEMORY SIZE
4 - DEVICE PIN FUNCTION

REGISTER READ FUNCTION

SUB-ADDRESS

Ø - (M), P: CONTENTS OF PG MEMORY AS DEFINED BY THE PCNTR

2 - CONTENTS OF COUNTER A

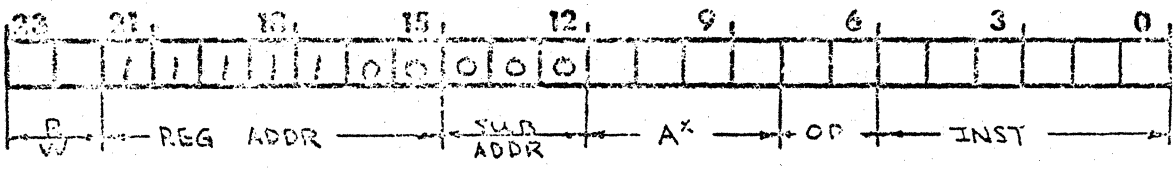
3 - CONTENTS OF COUNTER B

1,4 - ARE NOT READABLE.

I) REGISTER 1740 PG-MIL

II) S-500/600 PATTERN GENERATOR MEMORY INSTRUCTION LOAD

III) FORMAT



A^X - UPPER 4 BITS (2^{12}-2^{15}) OF COUNTER A, (READ ONLY)

OP - OPCODE
- 00 - GENERAL FUNCTION
- 01 - READ/WRITE PATTERN
- 10 - CONDITIONAL BRANCH
- 11 - UNCONDITIONAL BRANCH

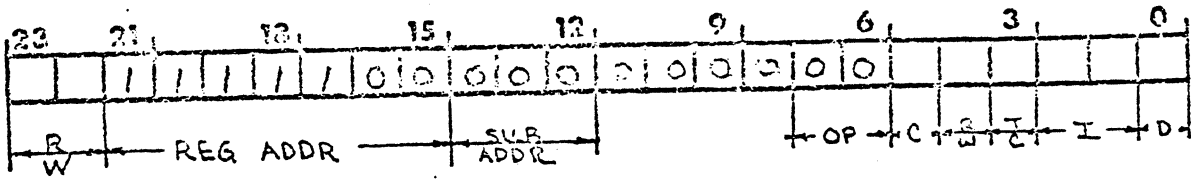
INST - THE PARTICULAR INSTRUCTION FOR EACH OPCODE

IV) NOTES
1) DELAY - N/A

I) REGISTER 1740 PG-MIL OPCODE

II) S-500/600 PATTERN GENERATOR MEMORY INSTRUCTION LOAD

III) FORMAT OPCODE Ø, READ/WRITE ZERO/ONE



C - COUNTER SELECT

0 = COUNTER A
1 = COUNTER B

R/W - READ/WRITE FUNCTION

0 = PERFORM A READ
1 = PERFORM A WRITE

T/C - TRUE/COMPLEMENT ADDRESSING SELECT

0 = TRUE
1 = COMPLEMENT

I - FUNCTION ITERATION SELECT

00 = 1 ITERATION, NO COUNTER INCREMENT
01 = 1 ITERATION, COUNTER INCREMENT
10 = UP TO N-1 ITERATIONS WITH COUNTER INCREMENT
11 = UP TO N ITERATIONS WITH COUNTER INCREMENT

D - DATA TO READ/WRITE FROM/TO DEVICE UNDER TEST

0 = LOGICAL Ø
1 = LOGICAL 1

IV) NOTES

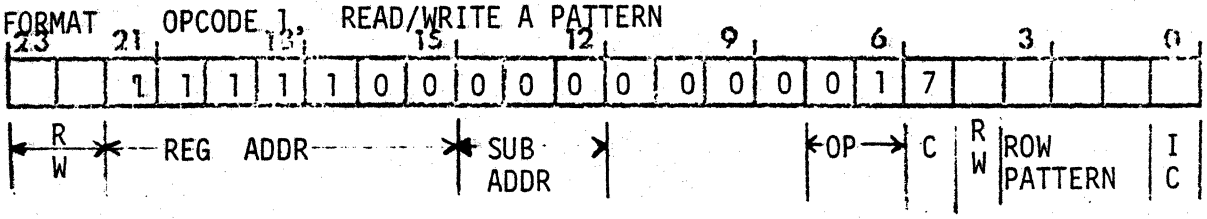
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENT

a) RD/WR ZERO/ONE

I) REGISTER 1740 PG-MIL OPCODE 1

II) S-500/600 PATTERN GENERATOR MEMORY INSTRUCTION LOAD

III) FORMAT OPCODE 1, READ/WRITE A PATTERN



R/W - READ/WRITE FUNCTION
0 = READ
1 = WRITE

T/C - TRUE/COMPLEMENT
0 = TRUE
1 = COMPLEMENT

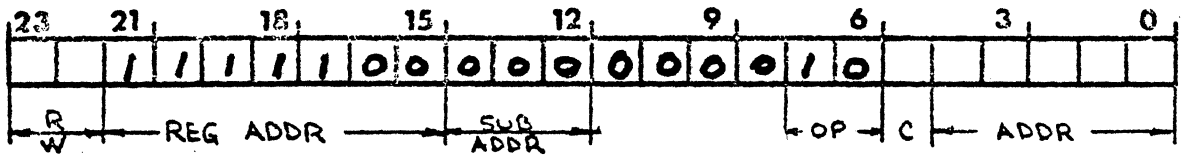
ROW PATTERN = 001 = CHECKERBOARD
011 - DIAGONAL

IV) NOTES
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENT
a) RD/WR CHECK/NCHECK
b) RD/WR DIAG/NDIAG

I) REGISTER 1740 PG-MIL OPCODE 2

II) S-500/600 PATTERN GENERATOR MEMORY INSTRUCTION LOAD

III) FORMAT OPCODE 2, CONDITIONAL BRANCH



C - COUNTER TO TEST SELECT

0 = COUNTER A
1 = COUNTER B

ADDR - PATTERN GENERATOR MEMORY ADDRESS TO BRANCH TO WHEN THE CONDITION FAILS.
0 ≥ ADDR ≤ 31

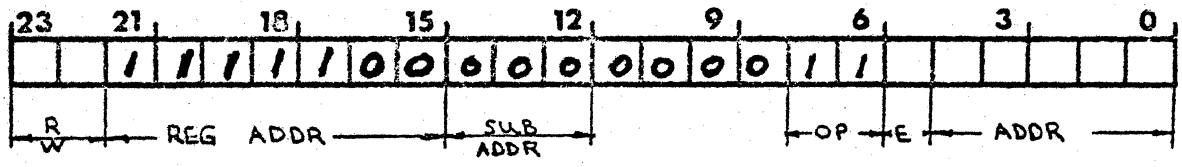
IV) NOTES

1.) DELAY - N/A
2.) GENERATED by the FACTOR statements
   a.) BRANCH UNLESS A=B TO HERE ± n/n
   b.) BRANCH UNLESS B=N TO HERE ±n/n
3.) FOR COUNTER A selection
   TEST A =B; for A ≠ B, GO TO (ADDRESS) ELSE
   GO TO P + 1
4.) FOR COUNTER B selection
   TEST B = N: FOR B ≠ N, GO TO (ADDRESS) ELSE
   GO TO P + 1

I) REGISTER 1740 PG - MIL OPCODE 3

II) S-500/600 PATTERN GENERATOR MEMORY INSTRUCTION LOAD

III) FORMAT OPCODE 3, UNCONDITIONAL BRANCH



E - BRANCH/EXIT SELECT

0 = UNCONDITIONAL BRANCH TO ADDRESS
1 = TERMINATE PATTERN GENERATOR EXECUTION
AND SET RESTART ADDRESS =ADDR

ADDR - PATTERN GENERATOR MEMORY ADDRESS
$0 \leq \text{ADDR} \leq 31$

IV) NOTES

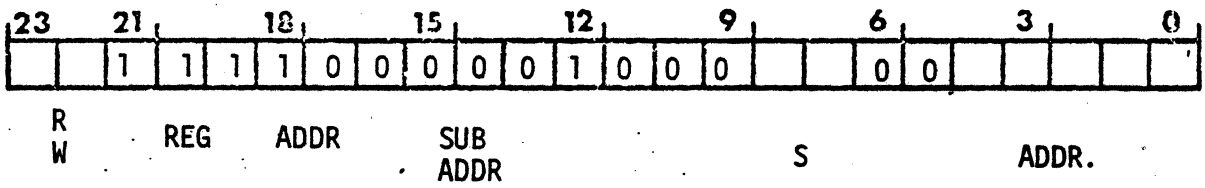
1.) DELAY - N/A
2.) GENERATED BY THE FACTOR STATEMENTS

a) BRANCH (TO/RESET) (HERE ± N/N)

I) REGISTER 1741 PG-PCNTR

II) S-500/600 PATTERN GENERATOR MEMORY PROGRAM COUNTER

III) FORMAT



S - DEFINES PATTERN GENERATOR START CRITERIA

00- DISABLE PATTERN GENERATOR EXECUTION

01- START EXECUTION AT LOCAL MEMORY LOCATION m WHEN THE ADDRESS M-1 CONTAINS 1 FOR PIN 30; REMAINS ENABLED UNTIL DISABLED.

10- START EXECUTION AT THE LOCAL MEMORY START ADDRESS S AS SOON AS ENABLE TEST IS ISSUED. AFTER COMPLETION, PATTERN GENERATOR IS DISABLED AUTOMATICALLY. ADDR - PATTERN GENERATOR MEMORY ADDRESS AT WHICH EXECUTION WILL BEGIN; MUST BE IN THE RANGE OF 0-31.

IV) NOTES

1.) DELAY - N/A

2.) GENERATED BY THE FACTOR STATEMENTS

a.) PGEN LOAD ADDR

b.) PGEN START

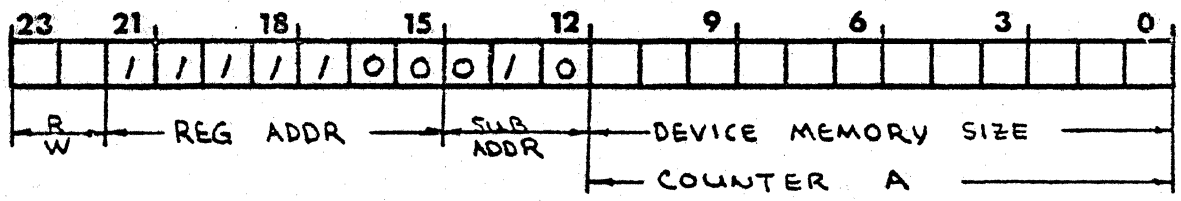
c.) ENABLE/DISABLE PGEN

3) THE PROGRAM MEMORY COUNTER AUTOMATICALLY INCREMENTS AT INSTRUCTION LOAD TIME AND EXECUTION TIME.

I) REGISTER 1742 PG-SIZE

II) S-500/600 PATTERN GENERATOR DEVICE ARRAY SIZE

III) FORMAT



DEVICE MEMORY SIZE - PROGRAMMED SIZE OF MEMORY ARRAY UNDER TEST. EACH BIT CORRESPONDS TO A DEVICE ADDRESS STAGE AND IS THEREFORE ACTUALLY SIZE-1 (2^n-1). VALID SIZE 1 SIZE 4096

COUNTER A -THE VALUE OF COUNTER A ON A READ

IV) NOTES

1.) DELAY - N/A

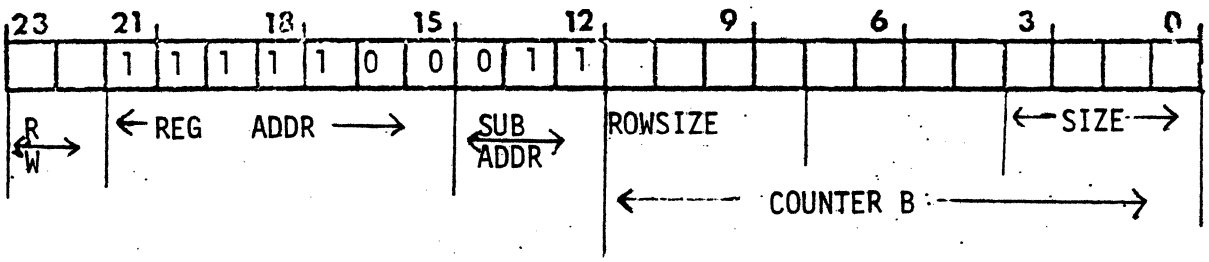
2.) GENERATED by the FACTOR statement

a.) SET PGEN1 rw, size, rowsize

I) REGISTER 1743 PG-XSIZE

II) S-500/600 PATTERN GENERATOR DEVICE ARRAY SIZE EXPANSION

III) FORMAT



XSIZE - An extension of register 1742. This is the upper 4 bits (2^{15} - 2^{12}) of device memory size.

ROWSIZE - ROWSIZE SELECT (4.2^n)

0 = Rowsize of 4
1 = Rowsize of 8
2 = Rowsize of 16
3 = Rowsize of 32
4 = Rowsize of 64
5 = Rowsize of 128
6 = Rowsize of 256
7 = Rowsize of 512

COUNTER B - Contents of Counter B when the Pattern Generator stops after completion - Read only

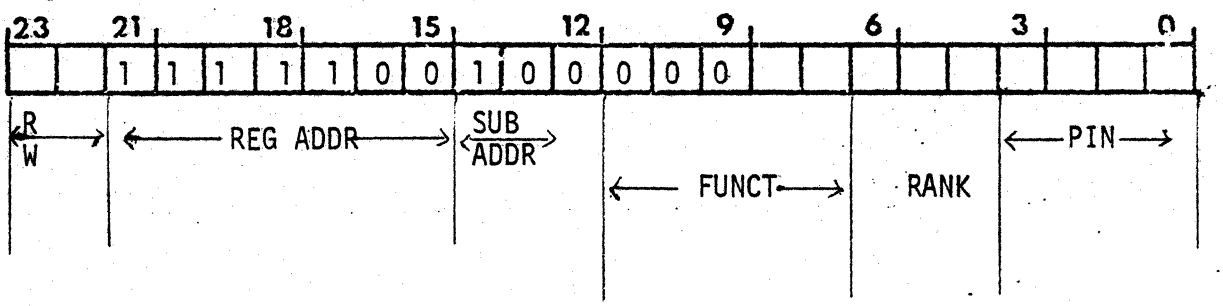
IV) NOTES

1.) DELAY - N/A
2.) GENERATED by the FACTOR STATEMENT
   a) SET PGEN1 RW, Size, Rowsize

I) REGISTER 1744 PG-PS

II) S-500/600 PATTERN GENERATOR PIN SCRAMBLER CONTROL

III) FORMAT



RANK 000 = RANK 1, PINS 1 - 15
001 - RANK 2, PINS 16 - 30
010 = RANK 3, PINS 31 - 45
011 = RANK 4, PINS 46 - 60

PIN = 1 - 15, Ø IS A NOP

FUNCT = PIN FUNCTION
= 0 = DEVICE PIN ADDR LINE Aø
= 1 = DEVICE PIN ADDR LINE A1
= 2 = DEVICE PIN ADDR LINE A2
= 3 = DEVICE PIN ADDR LINE A3
= 4 = DEVICE PIN ADDR LINE A4
= 5 = DEVICE PIN ADDR LINE A5
= 6 = DEVICE PIN ADDR LINE A6
= 7 = DEVICE PIN ADDR LINE A7
= 8 = DEVICE PIN ADDR LINE A8
= 9 = DEVICE PIN ADDR LINE A9
=10 = DEVICE PIN ADDR LINE A10
=11 = DEVICE PIN ADDR LINE A11
=12 = DATA PIN = TRUE DATA PIN
=13 = DEVICE READ/WRITE PIN
=14 = $\overline{\text{DATA}}$ PIN = COMPLEMENT DATA PIN
=15 = NOT USED

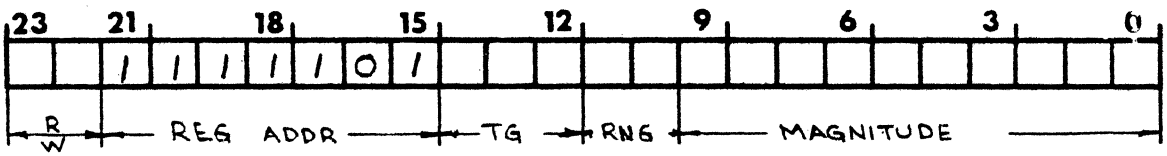
=23 = POWER PIN, GROUND PIN, CHIP SELECT COMPLEMENT, PIN 30 of TESTER

IV) Generated by the FACTORY statements
a) SET PGENA/PGEND/PGENDN/PGENC/PGENCN
b) SET PGEN1

I) REGISTER 175 PW

II) S-500/600 TIMING GENERATOR PULSE WIDTH REGISTER

III) FORMAT



TG - TIMING GENERATOR
0 = TG8
1 = TG1 THRU
7 = TG7

RNG - TIMING GENERATOR WIDTH RANGE

B11-B10		LSB	FULL SCALE
00	RNG0	10ns	10µs
01	RNG1	100ns	100µs
10	RNG2	1µs	1ms
11	RNG3	10µs	10ms

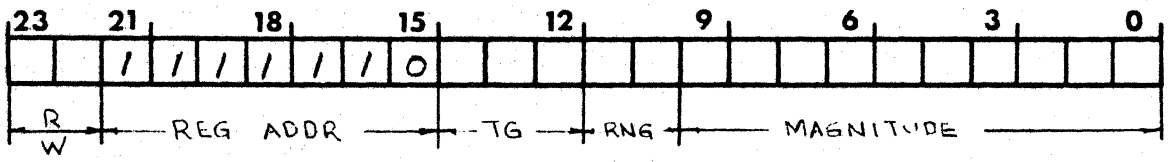
MAGNITUDE - $1 \leq$ VALUE ≤ 1023

IV) NOTES
1.) DELAY - N/A
2.) GENERATED by the FACTOR statement
a.) SET TG(x) WIDTH exp. (INTP)

I) REGISTER 176 PD

II) S-500/600 TIMING GENERATOR PULSE DELAY REGISTER

III) FORMAT



TG - TIMING GENERATOR
0 = TG8
1 = TG1 THRU
7 = TG7

RNG - TIMING GENERATOR PULSE DELAY RANGE

B11-B10		LSB	FULL SCALE
00	RNG0	10ns	10µs
01	RNG1	100ns	100µs
10	RNG2	1µs	1ms
11	RNG3	10µs	10ms

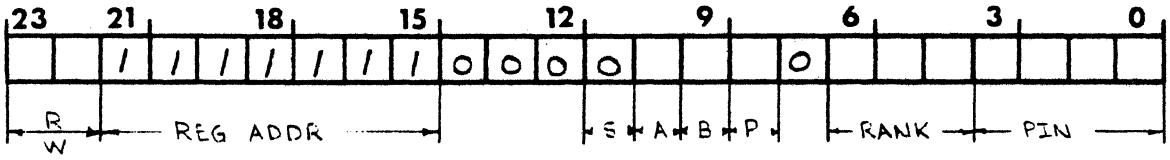
MAGNITUDE - $1 \leq$ VALUE ≤ 1023

IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED BY THE FACTOR STATEMENT
a.) SET TG(x) DELAY exp (INTP)

I) REGISTER 177 PPA, V

II) S-500/600 POWER PIN ADDRESS, TIMING GENERATOR VERNIER

III) FORMAT - POWER PIN ADDRESS



S - REGISTER SUB-ADDR Ø = PPA REGISTER
A (PRSA), B (PRSB), AND P FORM 60 3-BIT REGISTERS

ABP	CONNECTION
000	DATA REFERENCE PAIR
001	TCOM
010	CLOCK REFERENCE PAIR
011	DPS2
101	DPS1
111	DPS3

RANK - SELECTS 15 PIN GROUPS, $0 \leq$ RANK ≤ 3

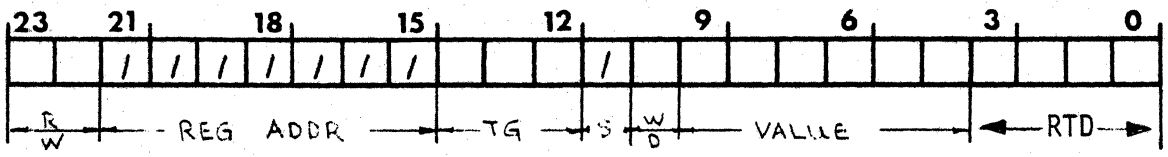
PIN - 1 OF 15 PIN #'s, PIN = Ø IS ILLEGAL

IV) NOTES
1.) DELAY - 1DLS
2.) GENERATED BY THE FACTOR STATEMENTS
a.) CONN CLK pin list (DMA)
b.) CONN DPS1/2/3/TCOM pin list (DMA)
c.) XCON PIN pin list (DMA)

I) REGISTER 177 PPA, V

II) S-500/600 POWER PIN ADDRESS, TIMING GENERATOR VERNIER

III) FORMAT - TIMING GENERATOR DELAY/WIDTH VERNIER



TG - TIMING GENERATOR
0 = TG8
1 = TG1 THRU
7 = TG7

S = REGISTER SUB-ADDRESS
1 = VERNIER REGISTER

W/D - WIDTH/DELAY
0 = WIDTH VERNIER
1 = DELAY VERNIER

VALUE - 6 BIT VERNIER VALUE
B4 = 160ps FS = 10ns

RTD = ROUND TRIP DELAY FOR TG7 AND TG8 LSB = 1ns, FS = 9 ns

IV) NOTES
1.) DELAY - 1 DLS
2.) GENERATED BY THE FACTOR STATEMENT
a.) SET TG(x) DELAY/WIDTH EXP. (INTP)
3.) RTD APPEARS ONLY IN TG1 DELAY REGISTER. THE VALUE IS READ ONLY AND IS HARDWIRED FOR EACH SYSTEM.

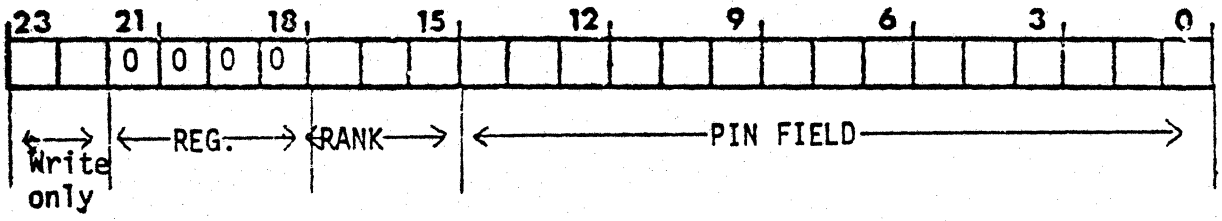
LONG REGISTER ASSIGNMENT IN ALTERNATE BANK

REG. ADDR	SYMBOL	FUNCTION	S670	SPO	PPO	S1200
000-007	XOR	EXCLUSIVE OR	X			
020-027	CRO	COMPARATOR RELAY OPEN				X
060	DR1	DATA READOUT #1			X	
062	DR2	DATA READOUT #2			X	
100	TOPO	TOPOLOGICAL SCRAMBLER			X	
102	HLD1/IR1	HOLD/INDEX REG			X	
104	HLD2/IR2	HOLD/INDEX REG			X	
106	HLD3/IR3	HOLD/INDEX REG			X	
110	MAX/CMP	MAXIMUM/COMPARE			X	
112	DEL1	DELTA REG.			X	
114	DEL2	DELTA REG.			X	
116	DEL3	DELTA REG.			X	
120	CD1	CONTROL RAM			X	
122	CD2	CONTROL RAM			X	
124	CA	CONTROL RAM			X	
126	SD/CRA	SHIFT DATA/EXEC ADDR			X	
130	DRAM	DATA RAM			X	
132	CSMD	CHIP SELECT & MASK			X	
134	SSA	STOP & STORAGE ADDR			X	
136	RFC	REFRESH COUNT			X	
140-147		RESERVED FOR USE BY C.P.E.				
1700	SA	START ADDR	X			
1701	RA	RETURN ADDR		X		
1703	FC	CLOCK BURST		X		
1704	LCS	LOOP COUNT STACK		X		
1705	LC	LOOP COUNT		X		
1706	STAM	STACK ADDR		X		
1707	IF2	IGNORE FAIL #2	X			
1710	OL	SEQUENTIAL LENGTH		X		
1711	Q	SEQUENTIAL PATTERN		X		
1740	LMI	LOCAL MEMORY INST.		X		

I) REGISTER ØØ EXCLUSIVE - OR REGISTER - XOR

II) S-670 ALTERNATE BANK

III) FORMAT



RANK - Ø $\leq$ RANK $\leq$ 7

PIN FIELD BØ = PIN 1/16/31/46/61/76/91/106

Ø = NOT SELECTED FOR EXCLUSIVE - OR FUNCTION

1 = SELECTED FOR XOR FUNCTION BETWEEN F-DATA AND TG

IV) NOTES

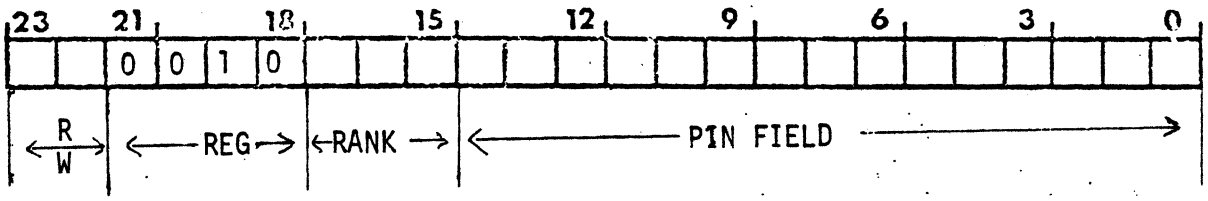
1) GENERATED BY THE FACTOR STATEMENT SET XOR (DMA)

#) OTHER REGISTERS MAY BE USED WITH XOR REGISTERS SUCH AS INVERT.

I) REGISTER Ø2 COMPARATOR RELAY OPEN - CRO

II) S-1200 ALTERNATE BANK (120 Pin Option)

III) FORMAT



RANK - Ø ≤ RANK ≤ 7

PIN FIELD BØ = PIN 1/16/31/46/61/76/91/106

Ø = COMPARATOR RELAY CLOSED

1 = COMPARATOR RELAY OPENED FOR THE PIN

IV NOTES

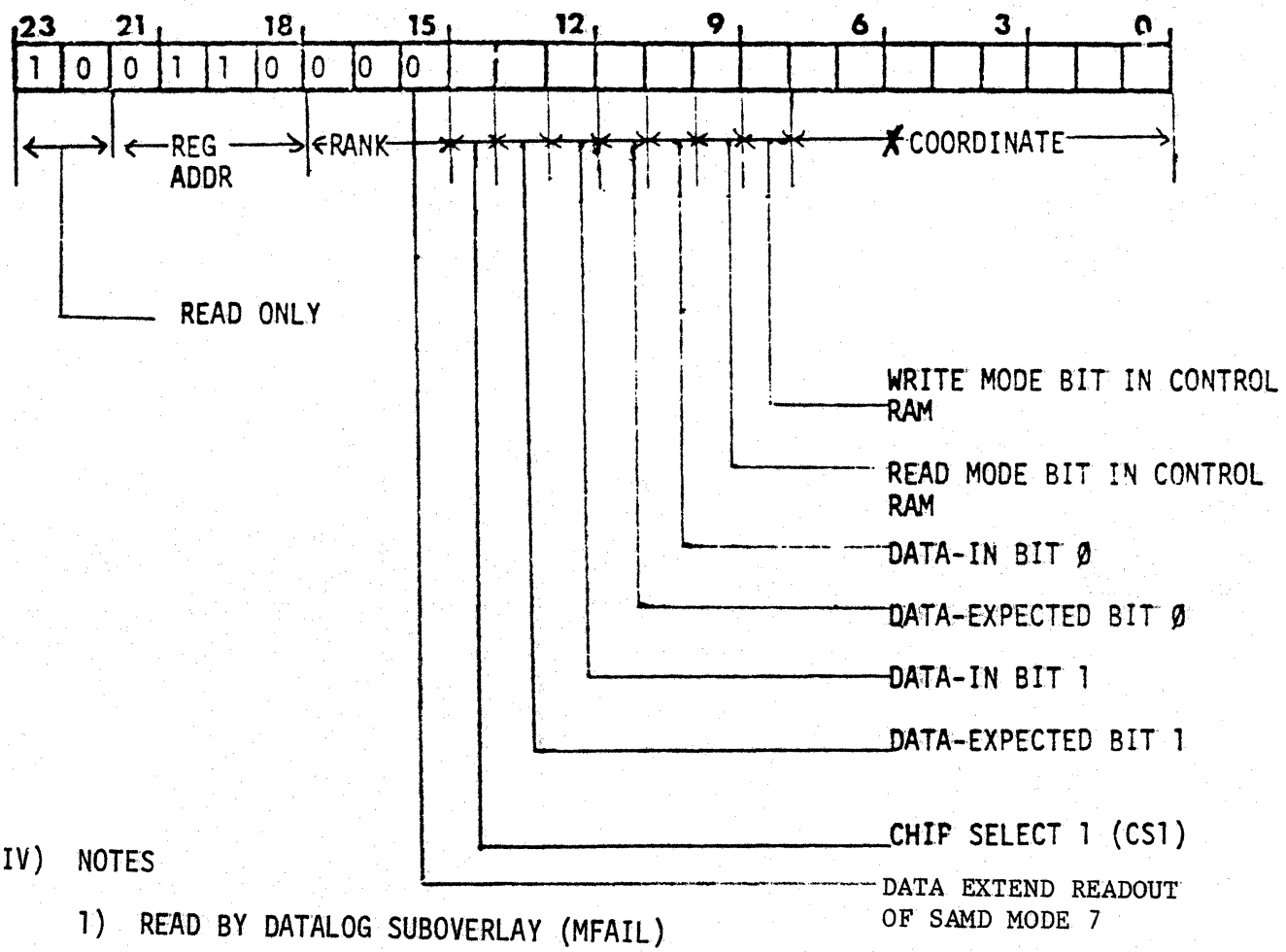
1) GENERATED BY THE FACTOR STATEMENT:

SET CRO BINPAT (DMA)

I) REGISTER 6Ø DATA READOUT #1 - DR1

II) S-II ALTERNATE BANK (PPM)

III) FORMAT



IV) NOTES

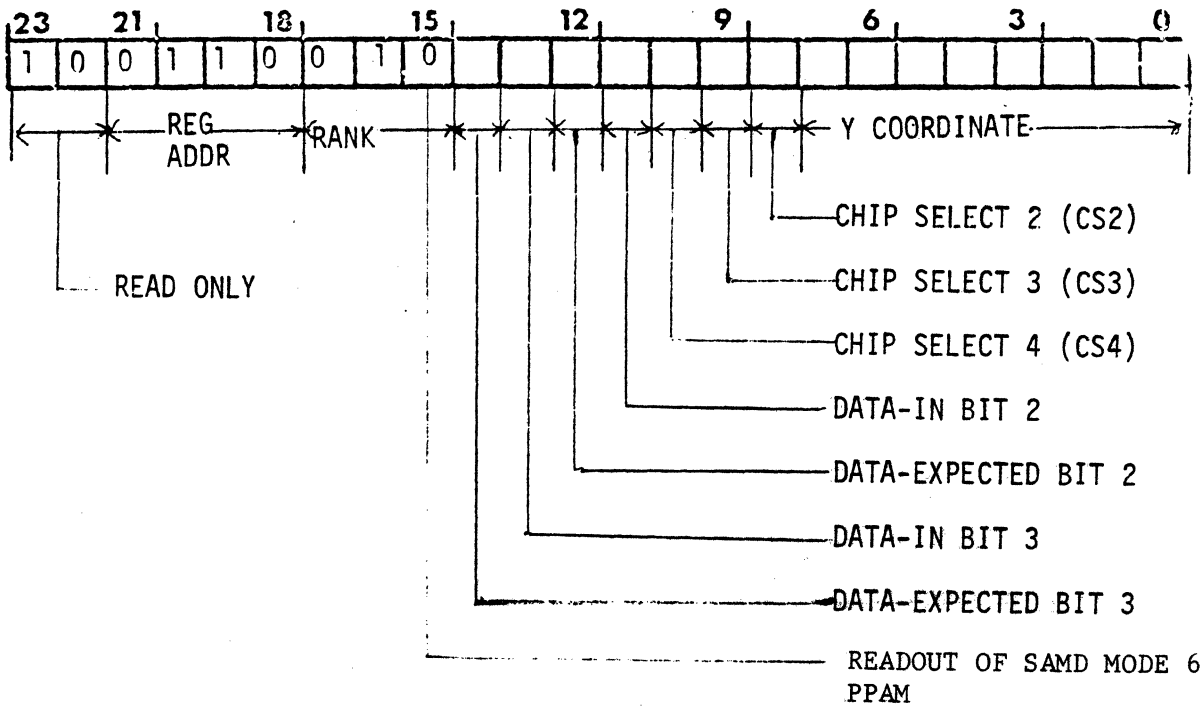
1) READ BY DATALOG SUBOVERLAY (MFAIL)

2) USED TOGETHER WITH DATA READOUT #2 (Ø62)

I) REGISTER 62 DATA READOUT #2 - DR2

II) S-II ALTERNATE BANK (PPM)

III) FORMAT



IV) NOTES

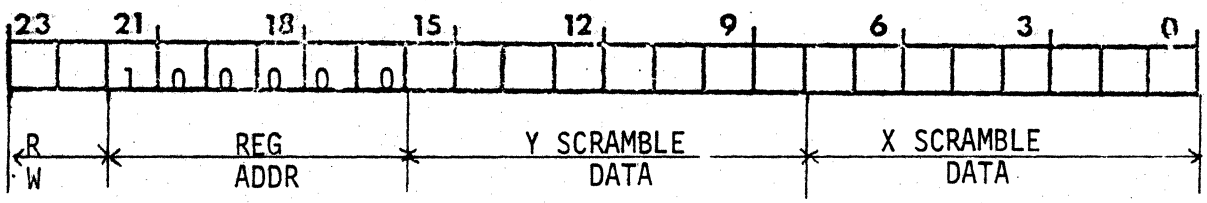
1) READ BY DATALOG SUBOVERLAY (MFAIL)

2) USED TOGETHER WITH DATA READOUT #1 (Ø6Ø)

I) REGISTER 1ØØ TOPOLOGICAL SCRAMBLER - TOPO

II) S- 670 ALTERNATE BANK (PPO)

III) FORMAT



IV) NOTES

1) GENERATED BY THE PPO ASSEMBLY INSTRUCTION, TOPO (DMA)

2) USAGE OF THE TOPOLOGICAL SCRAMBLER IS ENABLED/DISABLED BY THE PPO ASSEMBLY INSTRUCTION, SCRM. (DMA)

3) IT IS FOR BOTH READ AND WRITE

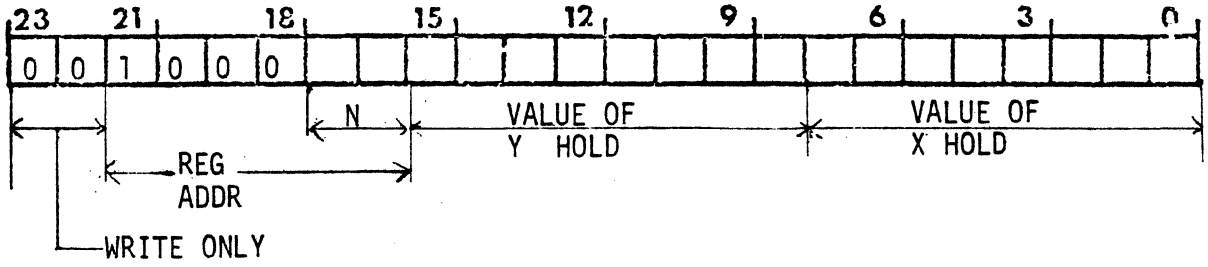
4) THE DATA CONTAINED IN A READ/WRITE OF THE REGISTER IS LOCATED IN THE TOPOLOGICAL SCRAMBLER MEMORY AT AN ADDRESS DEFINED BY THE STORAGE ADDRESS IN THE SSA REGISTER.

I) REGISTER 102, 104, 106 HOLD REGISTERS-HLD1/2/3, INDEX REGISTERS-IR1/2/3

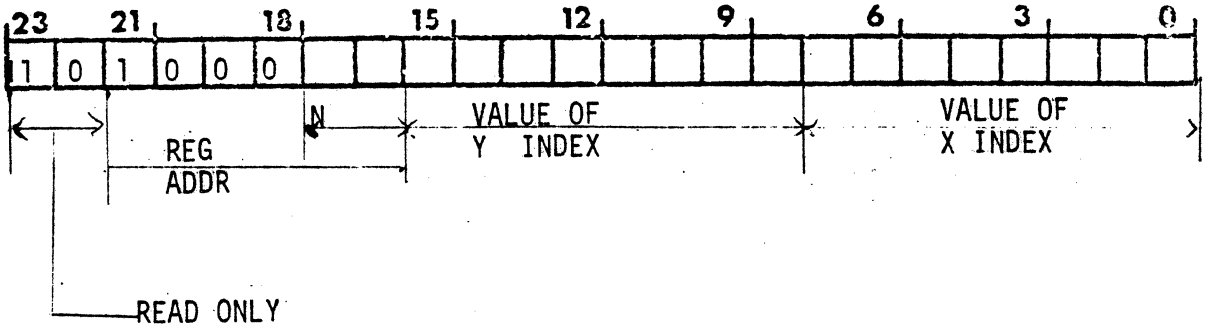
II) S-670 ALTERNATE BANK (PPO)

III) FORMAT

WRITE: HOLD REGISTERS



READ: INDEX REGISTERS



N : Y/X register designation

- 01 for Y1/X1 selection
- 10 for Y2/X2 selection
- 11 for Y3/X3 selection

IV) NOTES

1) N = 00 IS NOT APPLICABLE

2) WRITE TO THE HOLD REGISTERS IS GENERATED BY THE PPO ASSEMBLY INSTRUCTIONS, HLD1, HLD2, and HLD3 (DMA)

3) READING THE INDEX REGISTERS IS DONE BY ANALYSIS COMMAND READ IR1/IR2/IR3.

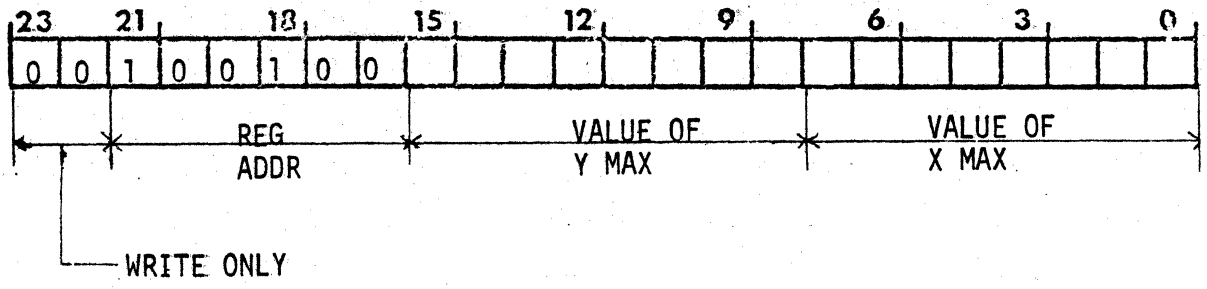
4) THE HOLD AND THE INDEX REGISTERS ARE RELATED BY THE PPO ASSEMBLY INSTRUCTION, L, WHICH LOADS THE INDEX REGISTER WITH THE CONTENT IN THE CORRESPONDING HOLD REGISTER.

I) REGISTER 11Ø MAXIMUM REGISTER - MAX, COMPARE ADDR - CMP

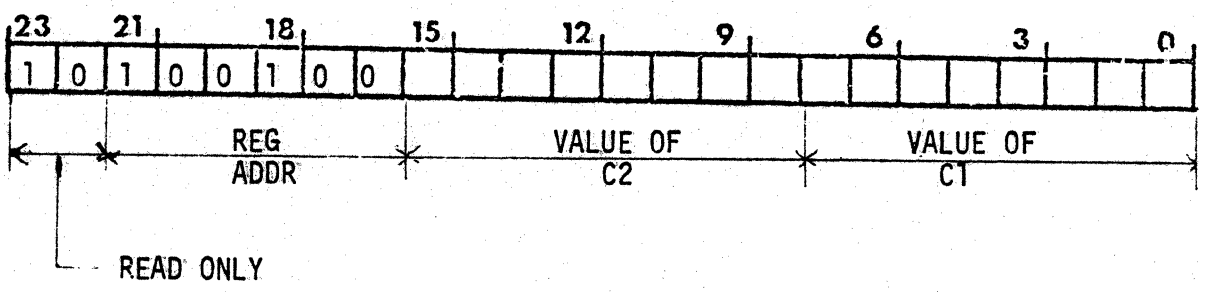
II) S-670 ALTERNATE BANK (PPO OPTION)

III) FORMAT

WRITE: MAXIMUM REGISTER



READ: COMPARE ADDRESS REGISTER



IV) NOTES

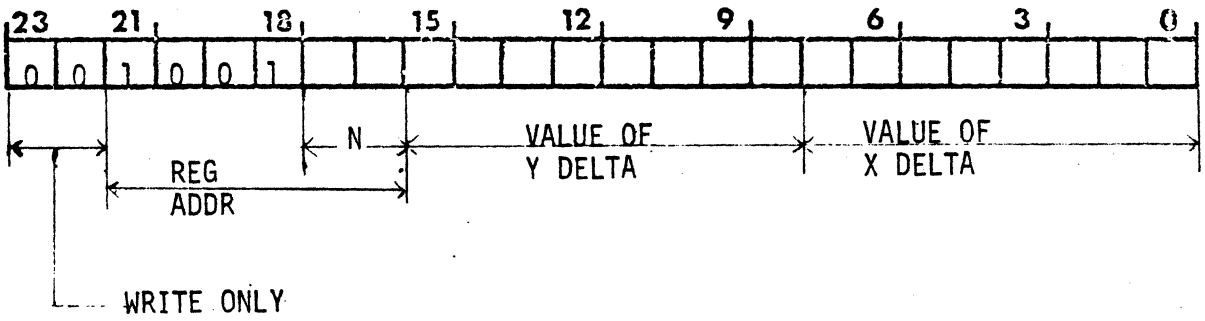
1) WRITE TO THE MAX REGISTER IS GENERATED BY THE PPO ASSEMBLY INSTRUCTION, MAX (DMA).

2) READ FROM THE COMPARE ADDRESS REGISTER IS DONE BY THE ANALYSIS COMMAND, READ CMP.

I) REGISTER 112, 114, 116 DELTA REGISTERS - DEL1/2/3

II) S-670 ALTERNATE BANK (PP0)

III) FORMAT



N : Y/X Register Designation

Ø1 for Y1/X1 selection
1Ø for Y2/X2 selection
11 for Y3/X3 selection

IV) NOTES

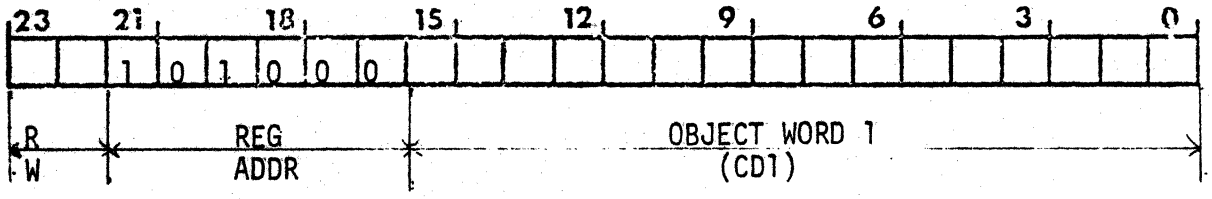
1) N = ØØ IS NOT APPLICABLE

2) GENERATED BY THE PP0 ASSEMBLY INSTRUCTIONS, DEL1, DEL2, and DEL3. (DMA)

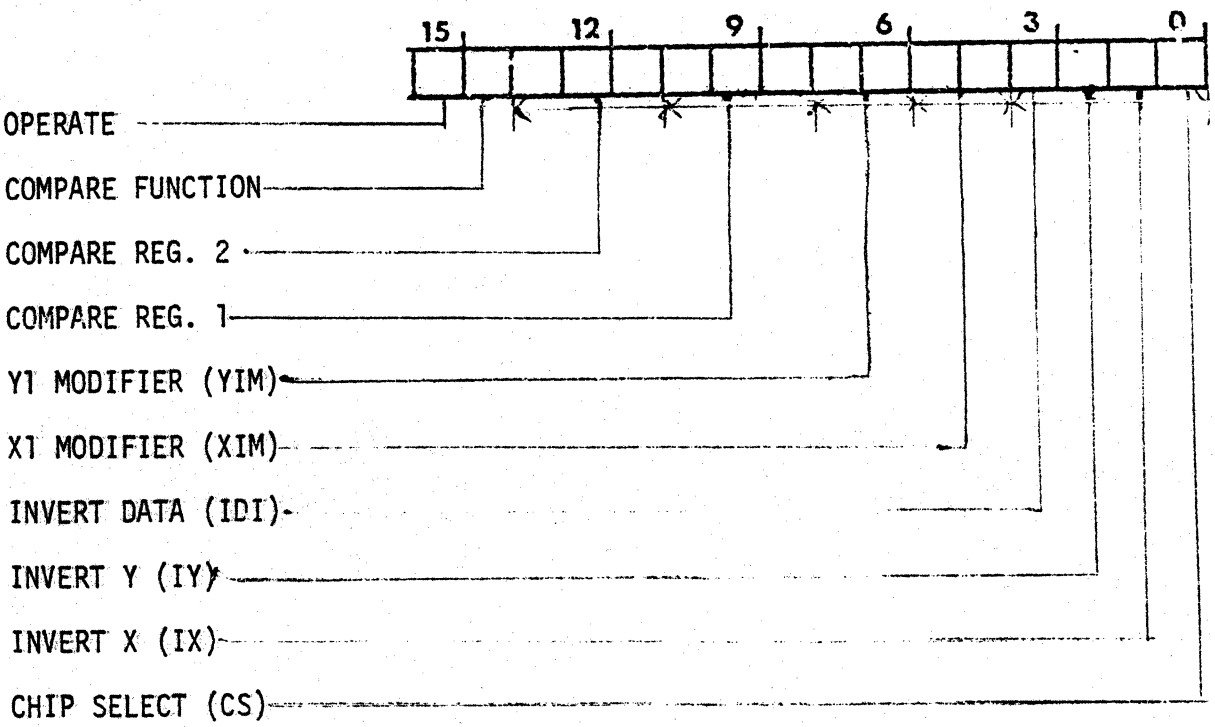
I) REGISTER 12Ø CONTROL RAM REGISTER - CD1

II) S-670 ALTERNATE BANK (PPO)

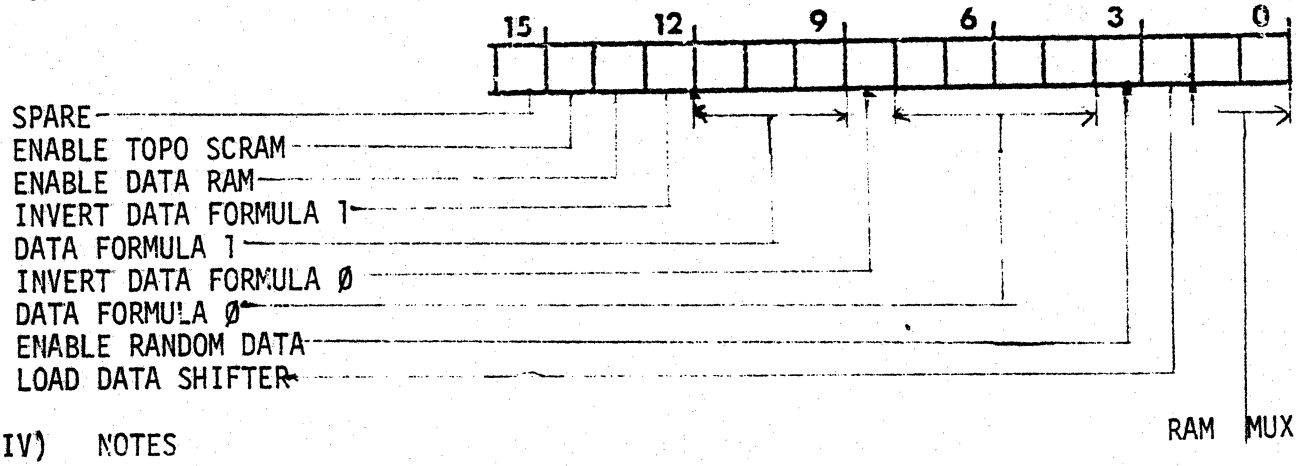
III) FORMAT



FOR AN ADDRESS GENERATOR WORD, CD1 IS AS FOLLOWS:



FOR A DATA GENERATOR WORD, CD1 IS AS FOLLOWS.



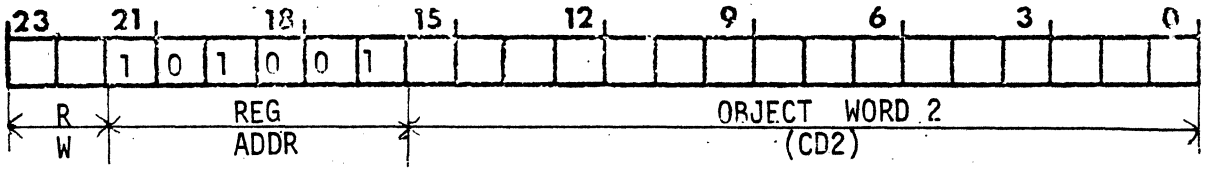
IV) NOTES

1) GENERATED BY PPO ASSEMBLY INSTRUCTIONS (DMA)
2) SEE NOTE 2 ON REG. 122 - CONTROL CA

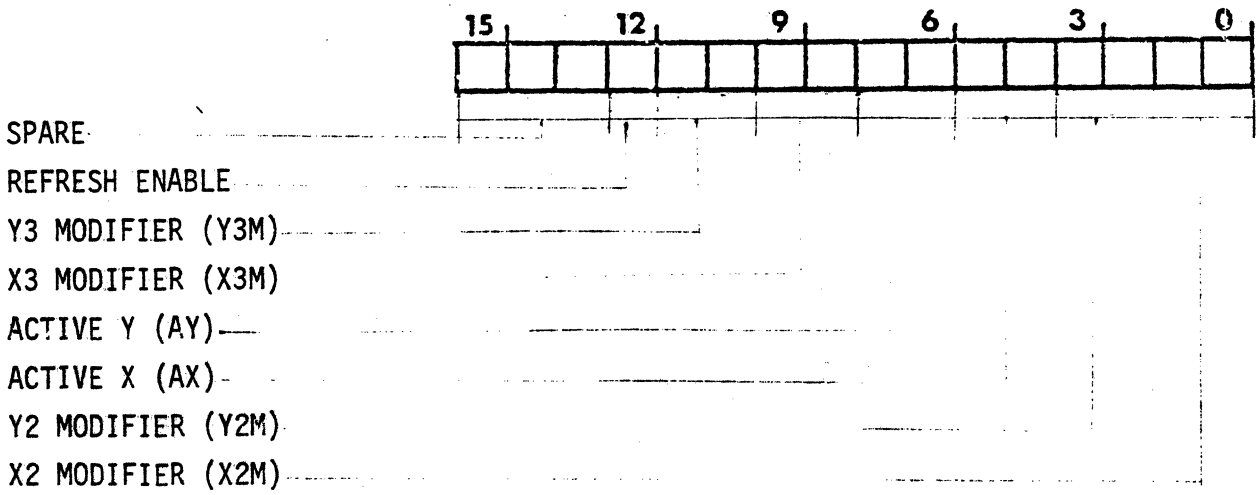
I) REGISTER 122 CONTROL RAM REGISTER - CD2

II) S-670 ALTERNATE BANK (PPO)

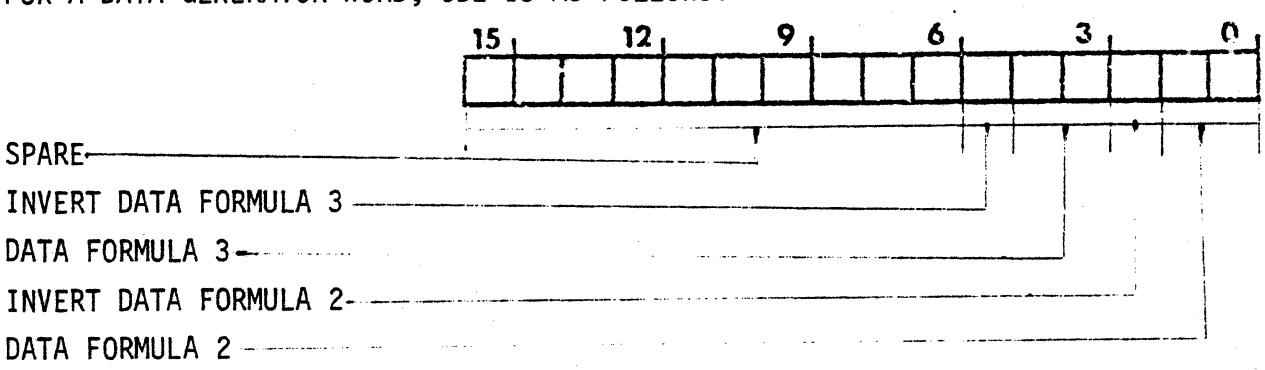
III) FORMAT



FOR AN ADDRESS GENERATOR WORD, CD2 IS AS FOLLOWS:



FOR A DATA GENERATOR WORD, CD2 IS AS FOLLOWS:



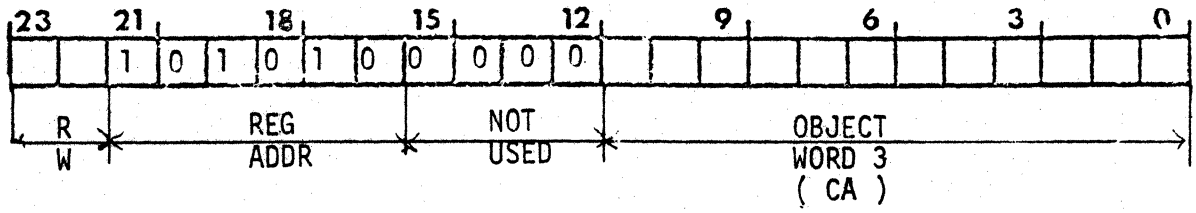
IV) NOTES

1) GENERATED BY PPO ASSEMBLY INSTRUCTIONS (DMA)
2) SEE NOTE ON REG. 122 - CONTROL RAM CA

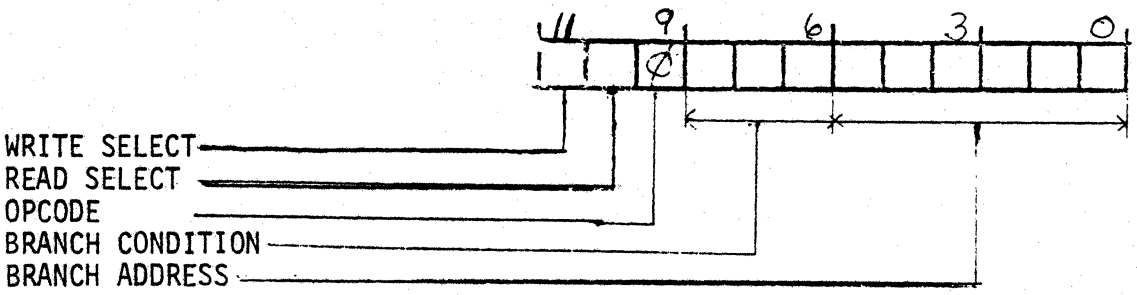
I) REGISTER 124 CONTROL RAM REGISTER - CA

II) S-II ALTERNATE BANK (PPM)

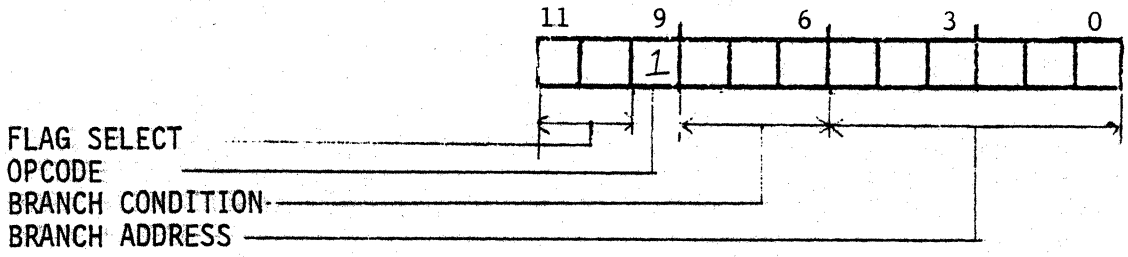
III) FORMAT



FOR AN ADDRESS GENERATOR WORD, CA IS AS FOLLOWS



FOR A DATA GENERATOR WORD, CA IS AS FOLLOWS



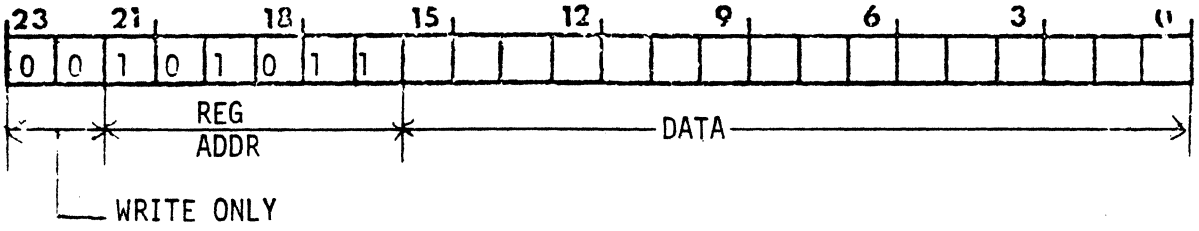
IV) NOTES

1) GENERATED BY PPO ASSEMBLY INSTRUCTIONS (DMA)
2) THIS REGISTER IS PART OF A 64 WORDS X 44 BIT CONTROL MEMORY. THE OTHER 2 PARTS OF THE 44 BIT WORDS ARE CD1 AND CD2. FOR WRITING INTO THE MEMORY, THE STORAGE ADDRESS REGISTER (#134) HAS TO BE SET UP FIRST. AFTER CA IS WRITTEN THE STORAGE ADDRESS REGISTER IS AUTOMATICALLY INCREMENTED.

I) REGISTER 126 SHIFT DATA REGISTER - SD.

II) S-670 ALTERNATE BANK (PPO)

III) FORMAT



IV) NOTES

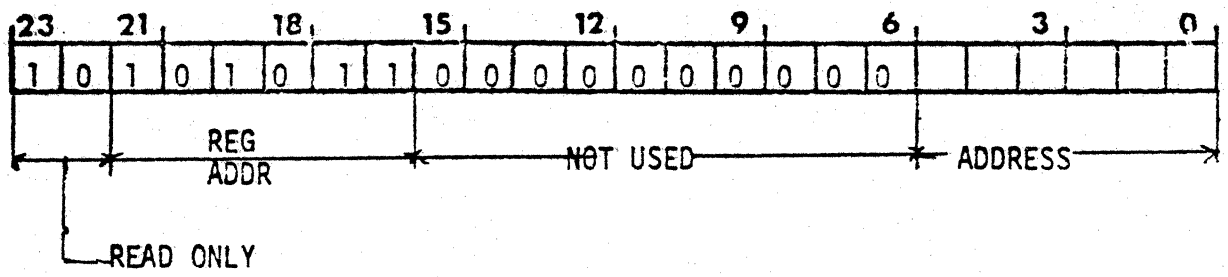
1) GENERATED BY THE PPO ASSEMBLY INSTRUCTION, SHFD. (DMA)

2) USED IN ACCORDANCE WITH THE PPO ASSEMBLY INSTRUCTION, RNDM

I) REGISTER 126 RAM EXECUTION ADDRESS REGISTER - CRA

II) S-670 ALTERNATE BANK (PPO)

III) FORMAT



IV) NOTES

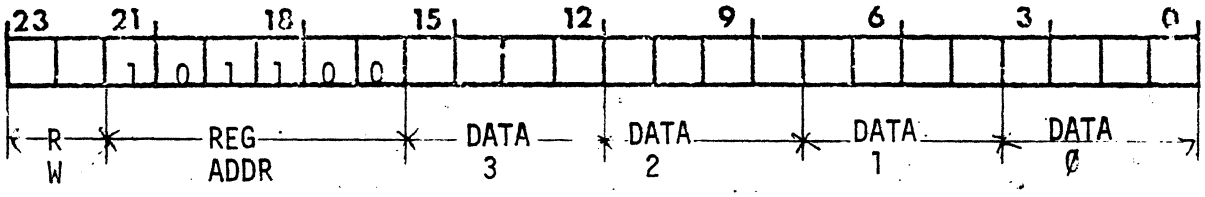
1) INVOKED ONLY BY THE ANALYSIS COMMAND, READ CRA

2) THIS IS THE ADDRESS COUNTER OF THE CONTROL RAM USED DURING MICROPROGRAM EXECUTION.

I) REGISTER 130 DATA RAM - DRAM

II) S-670 ALTERNATE BANK (PPO)

III) FORMAT



IV) NOTES

1) GENERATED BY THE PPO ASSEMBLY INSTRUCTION DATA. (DMA)

2) USAGE OF THE DATA RAM IS ENABLED/DISABLED BY THE PPO ASSEMBLY INSTRUCTION, DRAM. (DMA)

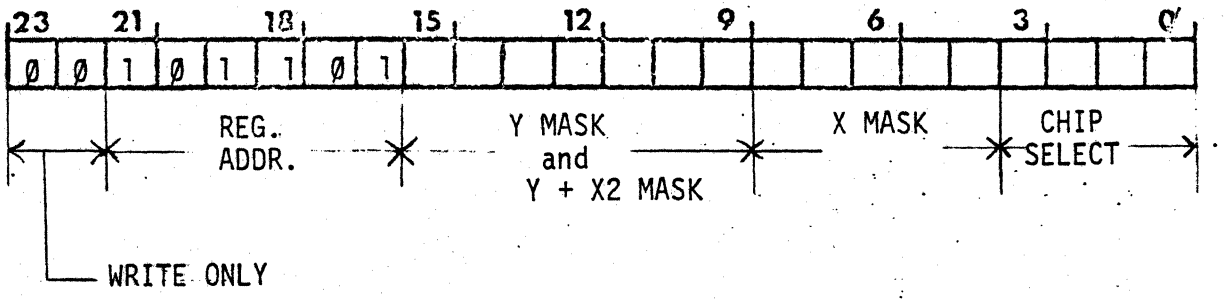
3) IT IS FOR BOTH READ AND WRITE.

4) THE DATA CONTAINED IN A READ/WRITE OF THE REGISTER IS LOCATED IN THE DATA RAM AT AN ADDRESS DEFINED BY THE STORAGE ADDRESS IN THE SSA REGISTER.

I) REGISTER 132 CHIP SELECT AND ADDRESS MASK - CSMD

II) S-670 ALTERNATE BANK (PPO)

III) FORMAT



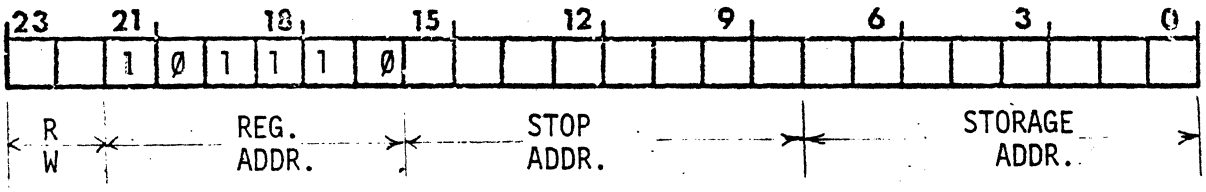
IV) NOTES

1.) GENERATED BY THE PPO ASSEMBLY INSTRUCTIONS CSEL, MASKX, MASKY. (DMA)

I) REGISTER 134 STOP ADDR. AND STORAGE ADDR. - SSA

II) S-670 ALTERNATE BANK (PPO)

III) FORMAT



IV) NOTES

1) THE STORAGE ADDRESS IS SET BY THE PPO ASSEMBLY INSTRUCTION, ORG. (DMA)

2) THE STOP ADDRESS IS SET BY THE ANALYSIS COMMAND, STOP ON. (INTP)

3) THE STORAGE ADDRESS CONTROLS THE ACCESSED LOCATION OF A TOPOLOGICAL RAM, A DATA RAM AND A CONTROL RAM. IT IS AUTOMATICALLY INCREMENTED AFTER WRITING INTO REGISTERS:

124 CONTROL RAM-CA PART

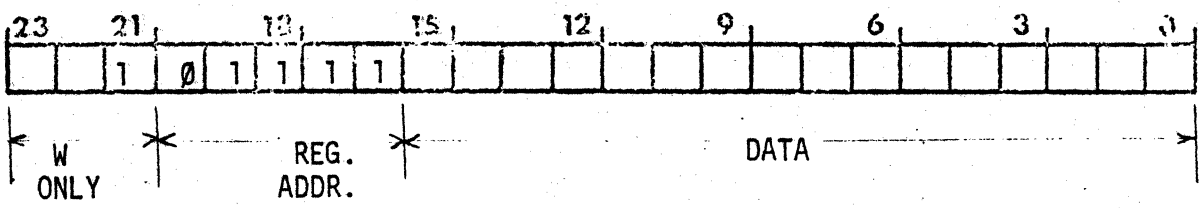
100 TOPOLOGICAL SCRAMBLER

130 DATA RAM

I) REGISTER 136 REFRESH COUNT REGISTER - RFC

II) S-670 - ALTERNATE BANK (PPO)

III) FORMAT



DATA IS A MULTIPLE OF 10 USECS, I.E. WHEN DATA IS 5, A REFRESH TIME OF 50 USECS IS PROGRAMMED.

IV) NOTES

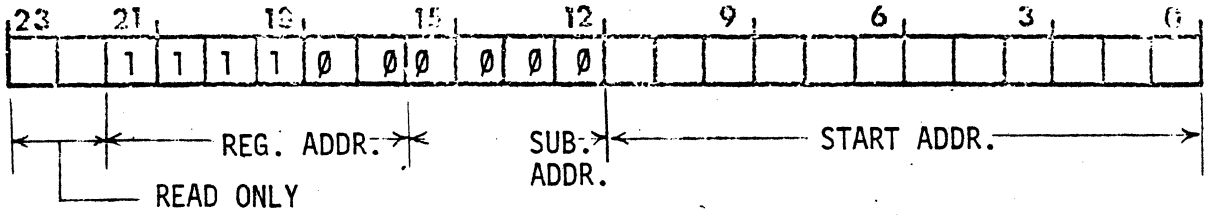
1) GENERATED BY THE PPO ASSEMBLY INSTRUCTION, RFC. (DMA)

2) ITS USAGE IS ENABLED/DISABLED BY THE PPO ASSEMBLY INSTRUCTION, RFEN. (DMA)

I) REGISTER 17ØØ START ADDRESS REGISTER - SA

II) S-67Ø ALTERNATE BANK

III) FORMAT



START ADDRESS IS THE TEST START ADDRESS IN LOCAL MEMORY.

IV) NOTES

1) READ BY ANALYSIS COMMAND

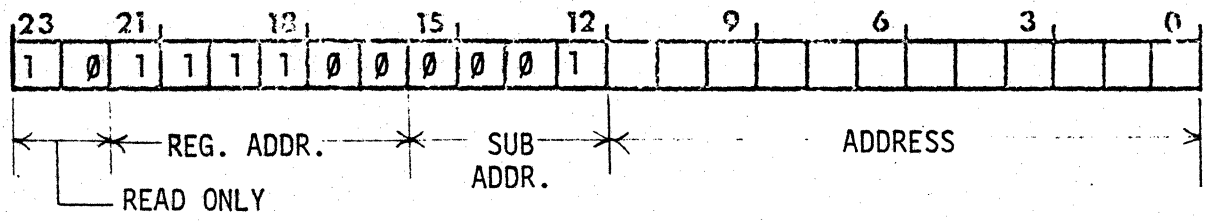
/. READ SA

2) ONLY BITS 1Ø to Ø ARE USED.
BIT 11 IS RESERVED FOR FUTURE EXPANSION.

I) REGISTER 17Ø1 RETURN ADDRESS REGISTER - RA

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



ADDRESS IS THE ADDRESS TO RETURN TO FROM AN INNER NESTED LEVEL TO THE OUTER LEVEL. IT IS USED IN CONJUNCTION WITH THE STAC REGISTER WHICH IS USED TO SPECIFY THE STACKED LEVEL WANTED BY LEVEL COUNT.

IV) NOTES

1) READ BY ANALYSIS COMMAND:

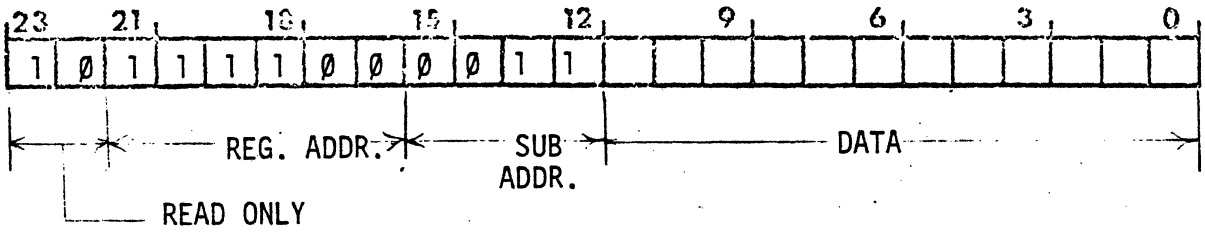
```
/. READ  RA
```

2) BITS 1Ø to Ø ARE VALID.
BIT 11 IS RESERVED FOR FUTURE EXPANSION.

I) REGISTER 17Ø3 CLOCK BURST REGISTER - FC

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



DATA IS THE REPETITION COUNT OF EXECUTING AN F DATA TESTING.
MAGNITUDE: $2 \leq \text{DATA} \leq 4096$
TO GET TRUE VALUE, SUBTRACT 2 FROM THE READ-VALUE.
THEN PERFORM A ONE'S COMPLEMENT (X OR WITH ALL 1'S)

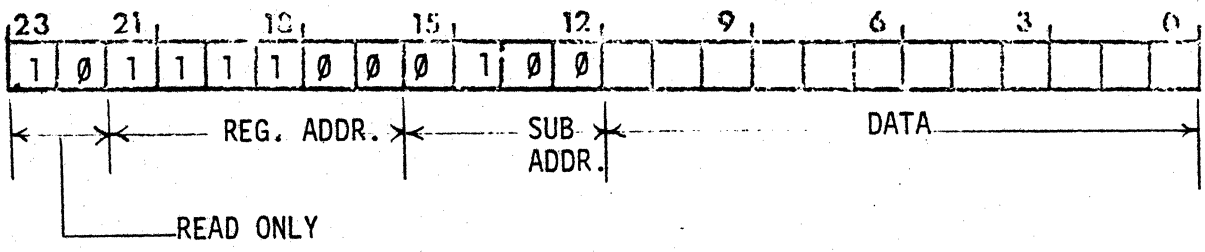
IV. NOTES

1) READ BY ANALYSIS COMMAND:
/. READ FC

I) REGISTER 1704 LOOP COUNT STACK REGISTER - LCS

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



DATA REPRESENTS THE LOOP COUNT VALUE OF A NESTED LEVEL. IT IS USED IN CONJUNCTION WITH THE STAM REGISTER WHICH SELECTS THE LEVEL NUMBER (FROM Ø TO 17B).

DATA ITSELF IS A TWO'S COMPLEMENT OF THE LOOP COUNT VALUE, E.G., LOOP COUNT VALUE OF 1 GENERATES A 7777B IN THE DATA FIELD OF THIS REGISTER.

IV. NOTES

1) A ZERO VALUE IN DATA IS NOT ALLOWED.

2) IN A CONTINUOUS LOOP, DATA IS ALL 1'S.

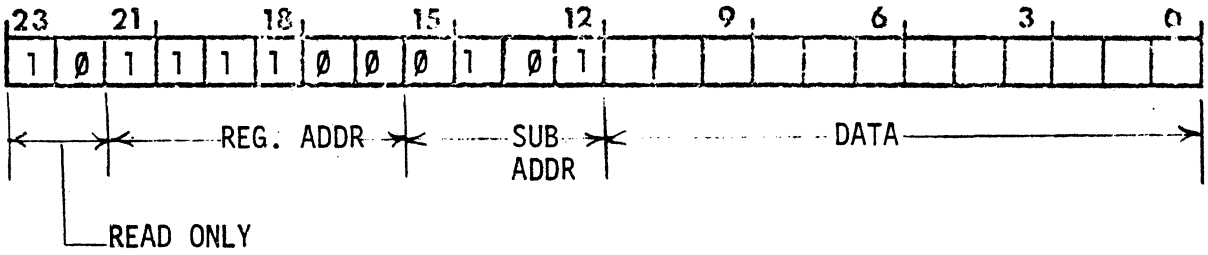
3) READ VIA ANALYSIS COMMAND:

/. READ LCS

I) REGISTER 17Ø5 LOOP COUNT REGISTER - LC

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



IV. NOTES

1) READ VIA THE ANALYSIS COMMAND

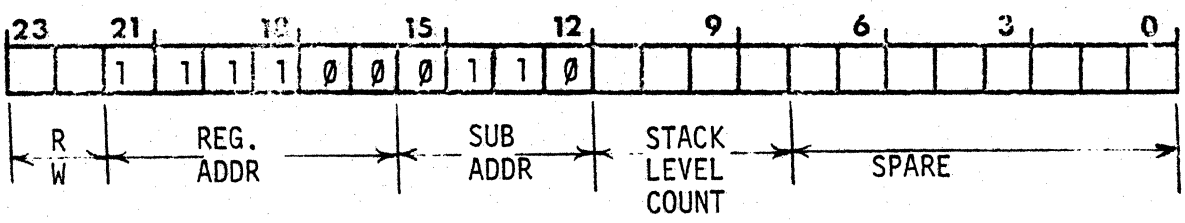
/. READ LC

2) DATA REPRESENTS THE NUMBER OF TIMES LOOPING WITHIN THE CURRENT NEST LEVEL.

I) REGISTER 17Ø6 STACK ADDR - STAM

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



STACK LEVEL COUNT: RANGES FROM Ø TO 17B.

INCREMENTS BY 1 WHEN ENTERING INTO AN INNER LEVEL OF NESTING.

DECREMENTS BY 1 WHEN EXITING OUT OF AN INNER LEVEL OF NESTING INTO AN OUTER LEVEL.

IV) NOTES

1) READ AND WRITE VIA THE ANALYSIS COMMAND

/ READ STAM

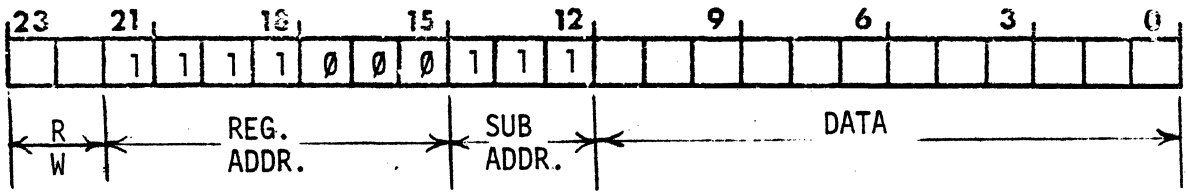
AND

/ WRITE STAM

I) REGISTER 17Ø7 IGNORE FAIL REGISTER #2 - IF2

II) S-670 ALTERNATE BANK (PPO/SPO)

III) FORMAT



IV) NOTES

1) USED IN CONJUNCTION WITH THE STANDARD IF REGISTER (17Ø7 IN THE STANDARD BANK).

2) CONTAINS THE MORE SIGNIFICANT HALF OF A TEST COUNT UP TO WHICH FUNCTIONAL FAILURES ARE TO BE IGNORED.

3) IT IS NOT INTENDED FOR A LOCAL MEMORY ADDRESS.

4) IT IS USED ONLY WHEN B11 (COUNT ENABLE) IN SAMC IS SET.

5) GENERATED BY FACTOR STATEMENT:

```
SET IFAIL, COUNT;
```

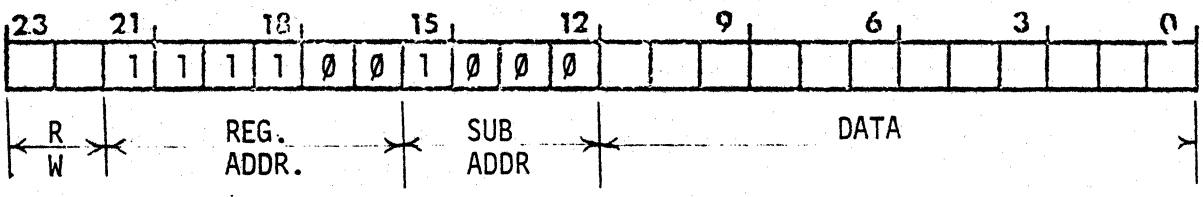
6) INVOKED BY DATALOG COMMAND:

```
/. DATALOG FCT COUNT
```

I) REGISTER 1710 SEQUENTIAL LENGTH REGISTER - QL

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



DATA REPRESENTS THE LENGTH OF A SEQUENTIAL PATTERN.

MAGNITUDE $1 \leq DATA \leq 14B$

IV) NOTES

1) GENERATED BY THE FACTOR STATEMENT:

SET Q (INTP)

2) USED IN CONJUNCTION WITH THE Q REGISTER (1711 IN ALTERNATE BANK).

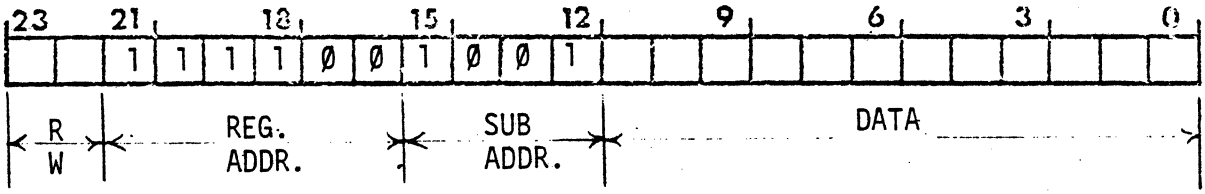
3) INVOKED BY THE FACTOR STATEMENT:

ENABLE TEST MATCH/AMATCH;

I) REGISTER 1711 SEQUENTIAL PATTERN REGISTER - Q

II) S-670 ALTERNATE BANK (SPO)

III) FORMAT



DATA REPRESENTS A SERIES OF PASS/FAIL CONDITIONS OF TESTS. B11 REPRESENTS 1ST TEST OF THE SERIES.

IV) NOTES

1) GENERATED BY THE FACTOR STATEMENT:

SET Q (INTP)

2) USED IN CONJUNCTION WITH THE QL REGISTER (171Ø IN ALTERNATE BANK).

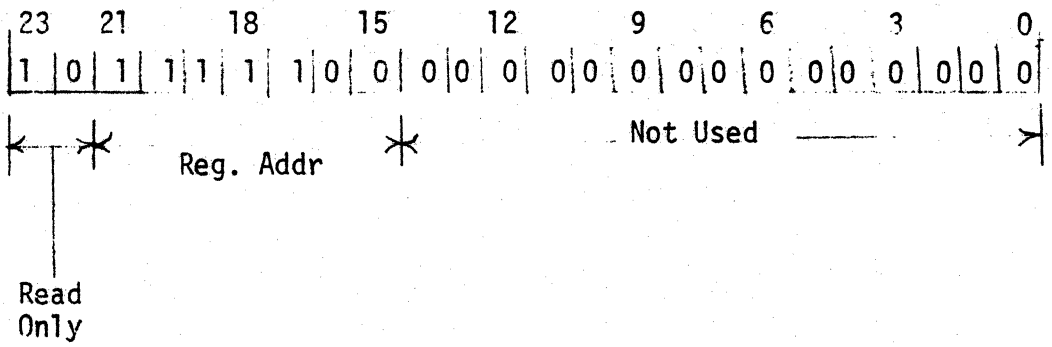
3) INVOKED BY THE FACTOR STATEMENT:

ENABLE TEST MATCH/AMATCH;

I) REGISTER 174Ø LOCAL MEMORY INSTRUCTION

II) S-670 ALTERNATE BANK (SEQUENCE PROCESSOR OPTION)

III) FORMAT



The format of the read-out data is similar to that for the F-RANK 8 (SPO) register except that bit 18 in F-RANK 8 will become bit 15 in in the LMI register.

IV) NOTES

Access to local memory instruction is performed as follows:

Writing local memory instruction = Write F-RANK8 in the standard bank.

Reading local memory instruction = Read LMI in the alternate bank

Analysis command is /. READ LMI nnnnB

Where nnnnB is the octal address of the local memory location to be read.

Feedback Form

Please send us your comments. They will help us produce better publications for you. We are interested in comments on accuracy, completeness, organization, clarity, audience suitability, illustrations, and detail level. If you choose to identify yourself (lower left), we will acknowledge your comments. All comments are confidential, FTSG property.

Optional

Name _____

Title _____

_____

Address _____

_____

_____

Phone _____

Telex _____

Publications Department Use Only

P/N 67095504

Rev 3 Date 6/76

_____

_____

_____

_____

_____

_____ _____ _____ _____

Technical Reviewer Date Response Sent Date

FAIRCHILD Test Systems Group

STAPLE

STAPLE

No Postage
Necessary If
Mailed In The
United States

Business Reply Mail
First Class Permit No. 5699 San Jose, California

Postage Will Be Paid By

Fairchild Test Systems Group
Technical Publications
1725 Technology Drive
San Jose, Ca. 95110