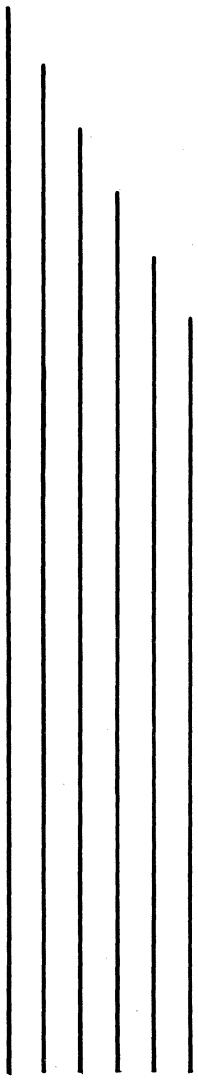
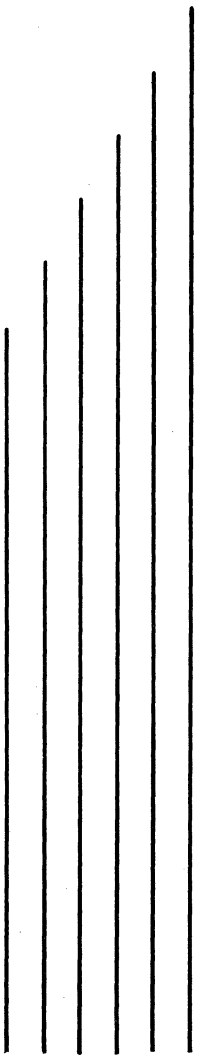
Sentry 100

Hardware Manual





FAIRCHILD

SYSTEMS TECHNOLOGY

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Sentry 100

Hardware Manual

Part Number 67095483
Issued: June,1973

FAIRCHILD
SYSTEMS TECHNOLOGY

Table of Contents

		Page
PREFACE		
SECTION I	GENERAL INFORMATION	1-1
1.0	GENERAL DESCRIPTION	1-1
1.1	SYSTEM HARDWARE DESCRIPTION	1-2
1.1.1	System Control Panel	1-4
1.1.2	System Power Modules	1-4
1.1.3	FST-1 Computer	1-4
1.1.4	Tester Controller	1-8
1.1.5	Test Station	1-8
	Pin Electronics	1-8
	Precision Measurement Unit	1-8
	Load Boards	1-10
	Power Supply Decoupling	1-10
	Input Bias Voltage	1-10
	MOS Input Pin Stressing	1-10
	Clocking	1-10
	Output Pin Loading	1-10
	EUT Connection	1-11
1.2	FUNCTIONAL DESCRIPTION	1-11
SECTION II	FUNCTIONAL DESCRIPTION	2-1
2.0	SYSTEM BLOCK DIAGRAM	2-1
2.1	REGISTERS & DATA BUSSES	2-3
2.2	COMPUTER & TESTER DATA FLOW	2-5
2.2.1	Peripheral Data Bus	2-6
2.2.2	Short Register Data Bus	2-6
2.2.2.1	Short Register Descriptions	2-7
	Register Address	2-7
	Mode Register (01)	2-8
	Status Register (02)	2-10
	Memory Address Register, MAR (04)	2-11
	Clock Burst Counter Register (10)	2-12
	Time Delay Register (11)	2-12
	Instruction Number Compare Register (14)	2-12
	Instruction Number Display Register (15)	2-13
	Data Buffer	2-13
	Test Station Control Register (05)	2-13
	Instruction Register (03)	2-13
	Quad 16 Bit Registers	2-14

Table of Contents (Continued) Page

2.2.3 Long Register Data Bus 2-15
2.2.3.1 Long Register Descriptions 2-16

. D Register (Input/Output Definition Register) 2-17
M Register (Mask Register) 2-17
F Register (Function Register) 2-17
S Register (Select Reference Register) 2-17
C Register (Comparison Register) 2-17
R Register (Relay Register) 2-18
PA Register (Pin Address Register) 2-19
SID Register (Socket Identification Register) 2-19
SND Register (Statement Number Display Register) 2-20
CS Register (Clock & Strobe Register) 2-20
PPS Register (Precision Power Supply Register) 2-20
PSL Register (Precision Sense Level Register) 2-20
EIR Register (External Interface Register) 2-21
DCT Register (DC Trip Register) 2-21

2.3 INDIVIDUAL BOARD DESCRIPTIONS 2-22
2.3.1 CPI 1 and CPI 2 (97166109 2-22
2.3.2 CPI 3 (97166108) 2-24
2.3.3 Register Address A (97340803) 2-24
2.3.4 Status Register A (97340804) 2-27
2.3.5 Mode Register (97206005) 2-30
2.3.6 Phase Loop Counter (97206006) 2-33
2.3.7 XDL Counter A (97340806) 2-35
2.3.8 T Count A (97206007) 2-39
2.3.8.1 Time Delay Counter 2-39
2.3.8.2 Clock Burst Counter 2-39
2.3.8.3 Instruction Number Display Counter 2-40
2.3.8.4 Instruction Number Counter 2-40
2.3.8.5 Readout Logic 2-40
2.3.9 Quad 16 Bit Register 2-40

Type 1 (97206008) 2-41
Type 2 (97206009) 2-41
Type 3 (97206010) 2-41
Statement Number Display Register 2-43
Clock, Sync, and Strobe Register 2-43
Socket Identification Register 2-45
External Interface Register 2-45

2.3.10 Data Buffer (97206002) 2-45
2.3.11 Dual Multiplex Control (97236101) 2-47
2.3.12 Instruction Register (97206102) 2-49
2.3.13 Control 1 A (97340807) 2-50
2.3.14 Line Receiver II (97206113) 2-53

Table of Contents (Continued) Page

2.3.15 T-Line Driver (97206206) 2-53
2.3.16 Reference Voltage Supply (97206110)(97206103) 2-53
2.3.17 Digitally Programmed Supply (97206104) 2-59
2.3.18 1 Amp Buffer (97206105) 2-64
2.3.19 Line Reference Voltage (97206111) 2-64
2.3.20 Analog Multiplexer (97209601) 2-65
2.3.21 Line Receiver (97206107) 2-65
2.3.22 15 Bit Decoder (97341603) 2-65

120 Bit Register Decoder 2-66
Pin Address Register 2-66
PMU Addressing 2-66
Internal Node Decoding 2-66
Clock Relay Decoding 2-68
Connect Voltage Conditioner 2-68

2.3.23 120 Bit Decoder (97200101) 2-68

Long Register Decoding Logic 2-68
Sync and Strobe Logic 2-70
Fail Set Logic 2-70

2.3.24 PEST Register (97201902) 2-71
2.3.25 Pin Control Logic (97200103) 2-71

Long Register Two-Bit Slices 2-74
Lamp Display Logic 2-74
Pass-Fail Set Logic 2-74

2.3.26 EUT Interface (97200104) 2-75
2.3.27 Decoupling Board (97200110) 2-75
2.3.28 Monitor Control (97340801) 2-76
2.3.29 Power Supply Alarm (97204601) 2-76

SECTION III THEORY OF OPERATION 3-1

3.1 TESTER OPERATING AND INSTRUCTION MODES 3-1
3.1.1 Operating Modes 3-1

SPU and DMA Instructions 3-2
Short Register Loading 3-5
Short Register Addressing and Loading 3-5
DPS and RVS Addressing 3-9
Data Buffer Interface Operation 3-9
Long Register Loading and DMA Mode 3-9
DMA Instructions 3-13

3-14

Table of Contents (Continued) Page

3.2 DETAILED THEORY OF OPERATION 3-14

Input Pins 3-17
Output Pins 3-17
Tester Strobe 3-18
Digitally Programmed Supplies (DPS) 3-18
Clock Burst Counter 3-18
Test Station Control Panel 3-18
Rank Fail Indicators 3-20
Long Register Data Display 3-20
External Interface Register (EIR) Display 3-20
Statement Number Readout 3-20
Pass/Fail Indicators 3-20

3.2.1 SPU MODE 3-21

Typical SPU Instruction 3-21
Read TSC (06602520B) 3-21
Write TSC (06402520B) 3-27
Write DPS1 (06410520B) 3-29
SPU Instruction to MAR 3-30

3.2.2 DMA MODE 3-31
3.2.2.1 DMA Sequence 3-31

Common Transitions 3-33
Read or Trap 3-33
Write to F Register 3-33
Write to non-F Registers 3-34
CPI Control 3-34
Function Test Suspended 3-35

3.2.3 PROGRAMMABLE VOLTAGE SUPPLIES 3-36

Reference Voltage Supplies 3-36
Digitally Programmable Supplies 3-37

3.2.4 PMU - PRECISION MEASUREMENT UNIT 3-38

INTRODUCTION 3-38

Functions 3-38
Basic Operating Modes 3-38
Control 3-40

Table of Contents (Continued) Page

OPERATION

Analog Circuits 3-41
Forcing and Measuring Circuits 3-41
Voltage Clamp Circuit 3-44
Control Circuits
PPS (Precision Power Supply) Register 3-47
DCT (DC Trip) Register 3-48
PLS (Precision Sense Level) Register 3-50
PA (Pin Address) Register 3-51

DETAILED CIRCUIT DESCRIPTIONS 3-52

Analog #1A Board (Refer to schematic 97341605-04) 3-52
Basic Forcing Loop and Sensing Circuitry 3-52
100mA Buffer Amplifier 3-53
MOS Switches 3-54
DAC 1 & DAC 2 (Forcing and Measuring DAC's) 3-54
Ground Buffer 3-55
Current Range Relays 3-55

Analog #2A Board (Refer to schematic 97341604-04) 3-56
40 Volt Follower 3-56
Voltage Clamp Circuit 3-58
Miscellaneous Relays 3-58

PMU Control Board (Refer to schematic 97230104-04) 3-59
PPS Register 3-59
DCT Register 3-60
PSL Register 3-61
Current Range Relay Drivers 3-61

List of Illustrations

		Page
Figure 1-1	S100 Test System	1-3
Figure 1-2	S100 Test System Control Panel	1-5
Figure 1-3	FST-1 Computer Control Panel	1-7
Figure 1-4	FST-1 Computer Simplified Block Diagram	1-9
Figure 1-5	S100 Simplified Block Diagram	1-12
Figure 1-6	S100 Simplified (Digital)	1-14
Figure 2-1	S100 Simplified Block Diagram	2-2
Figure 2-2	Tester CPI, Detailed Block Diagram	2-23
Figure 2-3	Register Address Simplified Block Diagram	2-25
Figure 2-4	Status Register Simplified	2-28
Figure 2-5	Mode Register Simplified	2-31
Figure 2-6	Phase Loop Counter Simplified	2-34
Figure 2-7	XDL Counter Flowchart	2-37
Figure 2-8	Quad 16-Bit Register	2-42
Figure 2-9	Data Buffer Simplified	2-46
Figure 2-10	Multiplex Control	2-48
Figure 2-11	Control 1A Simplified	2-51
Figure 2-12	Function Test, Signal Flowpath	2-55
Figure 2-13	Driver RVS Simplified	2-56
Figure 2-14	Detector RVS Simplified	2-56
Figure 2-15	RVS Simplified Block Diagram	2-57
Figure 2-16	D/A Converter Ladder Network	2-58
Figure 2-17	Simplified Op Amp	2-59
Figure 2-18	Simplified DPS Supply (V_F I Trip)	2-60
Figure 2-19	Simplified DPS Supply (I_F V Trip)	2-61
Figure 2-20	Line Reference Voltage Simplified	2-63
Figure 2-21	Pin Control Logic Simplified	2-72
Figure 2-22	S100 System Block Diagram (Sheet 1 of 3)	2-77
Figure 2-22	S100 System Block Diagram (Sheet 2 of 3)	2-78
Figure 2-22	S100 System Block Diagram (Sheet 3 of 3)	2-79
Figure 3-1	TOPSY Flowchart	3-6
Figure 3-2	Simplified Multiplex Control	3-7
Figure 3-3	Register Address Simplified	3-8
Figure 3-4	Control 1 Simplified	3-10
Figure 3-5	Quad 16 Bit Register Simplified	3-11
Figure 3-6	Data Buffer Simplified	3-12
Figure 3-7	Test Station Detailed Block Diagram, Pin 1 (Typical)	3-15
Figure 3-8	120 Bit Decoder Simplified Diagram	3-16
Figure 3-9	Test Station Control Panel Logic Diagram	3-19
Figure 3-10	SPU Instruction Logic	3-22
Figure 3-11	SPU Instruction Timing	3-26
Figure 3-12	DMA Timing Time Delay And Clockburst	3-32
Figure 3-13	PMU Simplified Block Diagram	3-39

List of Illustrations (Continued)

		Page
Figure 3-14	PMU Simplified Schematic Diagram	3-42
Figure 3-15	Voltage Clamp Circuit Simplified Schematic Diagram	3-45
Figure 3-16	40V Follower Simplified	3-57

List of Tables

Table 2-1	Long Registers	2-4
Table 2-2	Short Registers	2-4
Table 2-3	Short Registers Loaded by Peripheral Data Bus	2-6
Table 2-4	Mode Register Bit Description	2-8
Table 2-5	Status Register Bit Description	2-10
Table 2-6	Function of D, M, F, S, C, & R Registers	2-18
Table 2-7	Clock, Sync, and Strobe Register, Word Format	2-44
Table 2-8	EIR Word Format	2-44
Table 2-9	15-Bit Register Decoding	2-67
Table 2-10	Pin Address Format	2-67
Table 2-11	Long Register Decoding	2-69
Table 2-12	D, M, F, S, C, & R Register Functions	2-73
Table 3-1	SPU Instruction, Typical Format	3-3
Table 3-2	DMA Instruction, Typical Format	3-4
Table 3-3	Typical SPU Read Instruction	3-23
Table 3-4	Typical SPU Write Instruction	3-28
Table 3-5		3-36
Table 3-6	Voltage and Current Ranges	3-43
Table 3-7	Voltage Clamp Values	3-46
Table 3-8	Voltage And Current Range Bit Format	3-47
Table 3-9	PPS Register	3-49
Table 3-10	DCT Register	3-49
Table 3-11	PSL Register	3-49
Table 3-12	PA Register	3-49

Preface

This manual is intended to provide the reader with an appreciation of and in-depth familiarity with the tester portion of the Sentry 100 system -- its construction, organization, and operation -- from a hardware point of view.

Section I provides a general overall discussion of the S100 test System. This places the test system in the correct frame of reference with regard to the CPU memory and peripherals and will enable the reader to fully appreciate the following discussions on the tester.

Section 2 presents the basic system organization, showing how data is transferred along the three principal data buses -- peripheral data bus, short register data bus, and long register data bus. Each register in the tester is discussed, in a manner which shows its function in the system, the information contained therein, and how that register is loaded from or read into one of the three data buses. A set of individual printed circuit board descriptions is provided, showing for each board its function in the system, the main input and output signals, and the circuitry contained on that board.

Section 3 presents the tester operation. The operating modes -- Manual and Automatic -- and the instruction modes -- SPU and DMA -- are defined and explained.

Next, the detailed SPU and DMA instruction sequences are discussed, to provide an understanding of how the user-specified device testing algorithms are set up and run under program control. Finally, a complete description is given of the operation and circuitry of the PMU (Precision Measurement Unit).

FRONTISPIECE S-100 TEST SYSTEM

FAIRCHILD
SYSTEMS TECHNOLOGY

Section I
General Information

1.0 GENERAL DESCRIPTION

The Sentry 100 Computer Controlled Test System provides the capability to test virtually all digital networks with up to 60 pins.

The system design is oriented to production testing of:

Wafers or discrete packages
Static MOS, or
Bi-Polar Integrated Circuits
- using small to large scale integration (SSI, MSI, LSI)
- using any technology (ECL, CML, CTL, TTL, DTL, RTL)

The S-100 system can also test other digital networks such as arrays and printed circuit cards.

The general purpose S-100 system software and hardware is driven by test plans programmed by the user, or, if desired, supplied by Fairchild. The system software utilizes a background/foreground approach which allows test plan creation, compilation, editing, etc., to be performed in the background mode while testing is in process in the foreground mode.

The system provides the capability to classify and bin integrated circuits according to a master test plan and up to 16 individual test specifications. Failure counters identified by the test type and device pin can be defined, when requested, in order to allow various problems in the manufacturing process to be detected easily and quickly. Histograms of related device test results can be created when requested. Also, the results of all tests or certain sets of tests (such as all fails) can be logged. Analysis aids are provided to simplify test plan development.

The Sentry 100 System performs two basic types of tests; functional tests (that determine whether the circuit performs the intended logic operations), and precision parametric tests (that determine whether component parameters meet specifications).

Functional tests are performed by forcing programmed logic levels on all input pins of the Element-Under-Test and comparing all

device outputs with the expected logic levels previously programmed. In functional testing, all device input pins are driven in parallel and all device output pins are tested in parallel after a programmed interval of time.

Parametric tests allow a voltage or current to be measured at any pin of the Element-Under-Test while forcing a current or voltage, respectively at that pin. The Precision Measurement Unit can force or sense voltages or currents which are positive or negative. This allows device parameters such as voltage levels of an output pin, input leakage current, etc., to be measured under desired load conditions. The functional testing capability of the system is generally used in conjunction with parametric testing in order to force the device into the desired state.

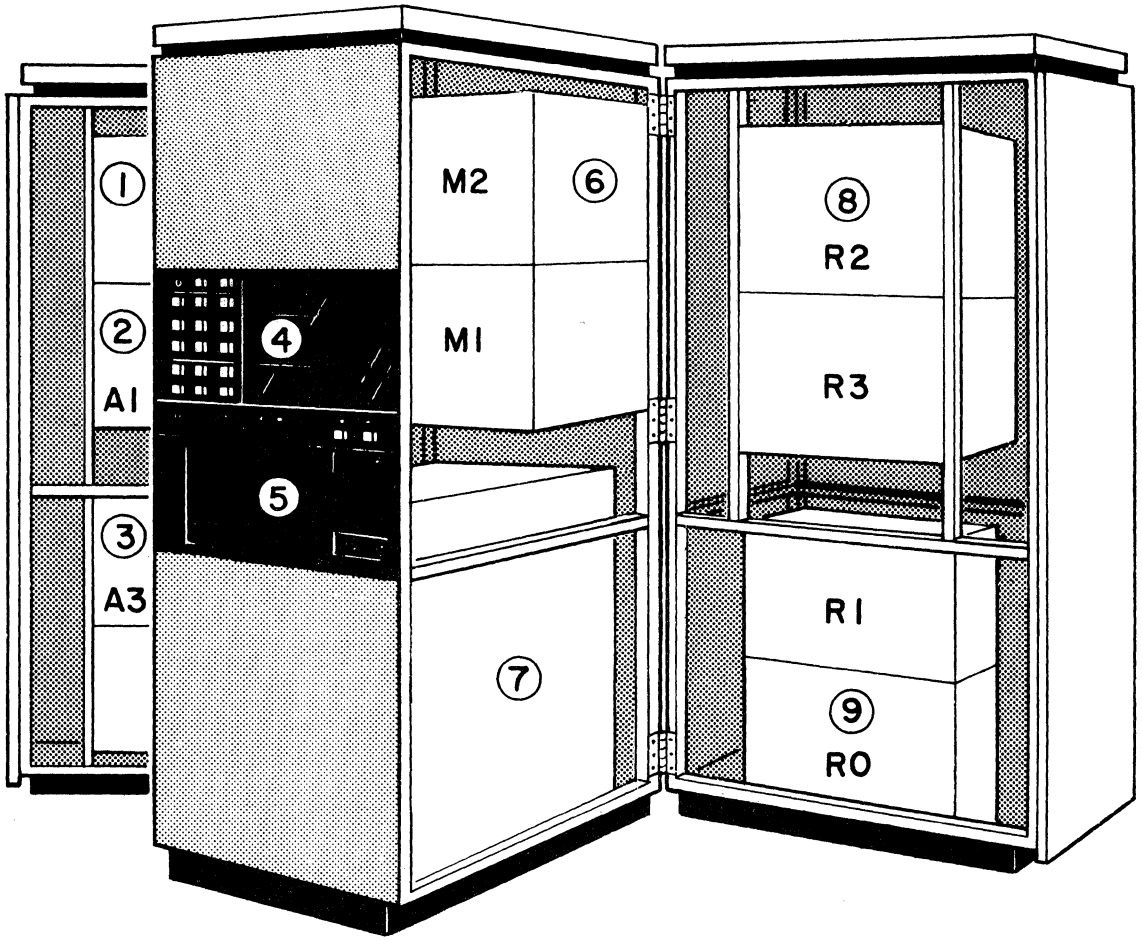
The Precision Measurement Unit may be connected to internal system nodes so that quantities such as the actual output voltages and load currents of the programmable Device Power Supplies or the functional logic levels actually generated by the Reference Voltage Supplies can be measured. This allows device power consumption to be calculated, and also allows system calibration to be checked by the system itself.

The maximum test rate of the system is 286,000 functional tests per second or approximately 875 D.C. tests per pin per second. The maximum number of tests that can be performed on a single element is virtually unlimited if subroutines or loops are used.

1.1 SYSTEM HARDWARE DESCRIPTION

The basic Sentry 100 System consists of a single bay enclosing system power modules, the FST-1 computer, the tester controller, and the test station. A Teletype unit is supplied in addition to the basic mainframe. Optional peripheral items such as the VKT, tape cassette unit, line printer and submultiplex test stations are packaged independently to maximize system modularity.

Figure 1-1 is an illustration of the system with the side doors opened. The following paragraphs describe the functions of the various components of the system.



1. MEMORY
2. CENTRAL PROCESSING UNIT
3. INPUT/OUTPUT MODULE
4. CONTROL PANEL
5. TESTER INTERFACE
6. MULTIPLEXER
7. POWER MODULE
8. 30-PIN MODULE PINS 31-60
9. 30-PIN MODULE PINS 1-30

FIGURE 1-1. S100 TEST SYSTEM

1.1.1 System Control Panel

Controls and displays are separated into two areas. One provides the operator with station START and RESET pushbutton controls, and displays the pass/fail status of the element under test and the end-of-test status. The second area provides computer, tester operating mode, statement advance, register display, and indicator test controls. It also displays computer status, tester register contents, and the current program statement number.

Register Selector pushbuttons allow the operator to select various registers or the rank fail indicator whose contents will be displayed by a row of 15 register display lamps. There are four ranks to each register. By appropriate combination of rank selector and register selector the status of all 60 pins can be displayed.

The rank fail indicator illuminates, if selected, when a pin of a certain rank fails. The register contents may then be displayed on the register display lamps to determine which pin has failed. This type of display is useful while debugging prototype designs and during test program verification.

A numerical display of the test statement number which is currently in the tester is also provided. This is extremely valuable for program verification when the tester is in the manual mode and is being single stepped. It is always updated with the number of the last FACTOR statement executed when the test pauses. A detailed view of the system control panel is shown in figure 1-2.

1.1.2 System Power Modules

The power modules are contained in the lower central section of the bay. Should one or more of the modules fail, an audible and visual alarm is generated. The modules are mounted so that all potentiometer controls are available for adjustment.

1.1.3 FST-1 Computer

The FST-1 is a general-purpose digital computer located in the left door frame. Sufficient controls are available on the test station panel to control the FST-1 during normal operation.

The FST-1 Computer consists of three subsystems; the central processing unit (A1), memory (A0), and interface (A3). Provisions are made for two memory modules each providing 8,192

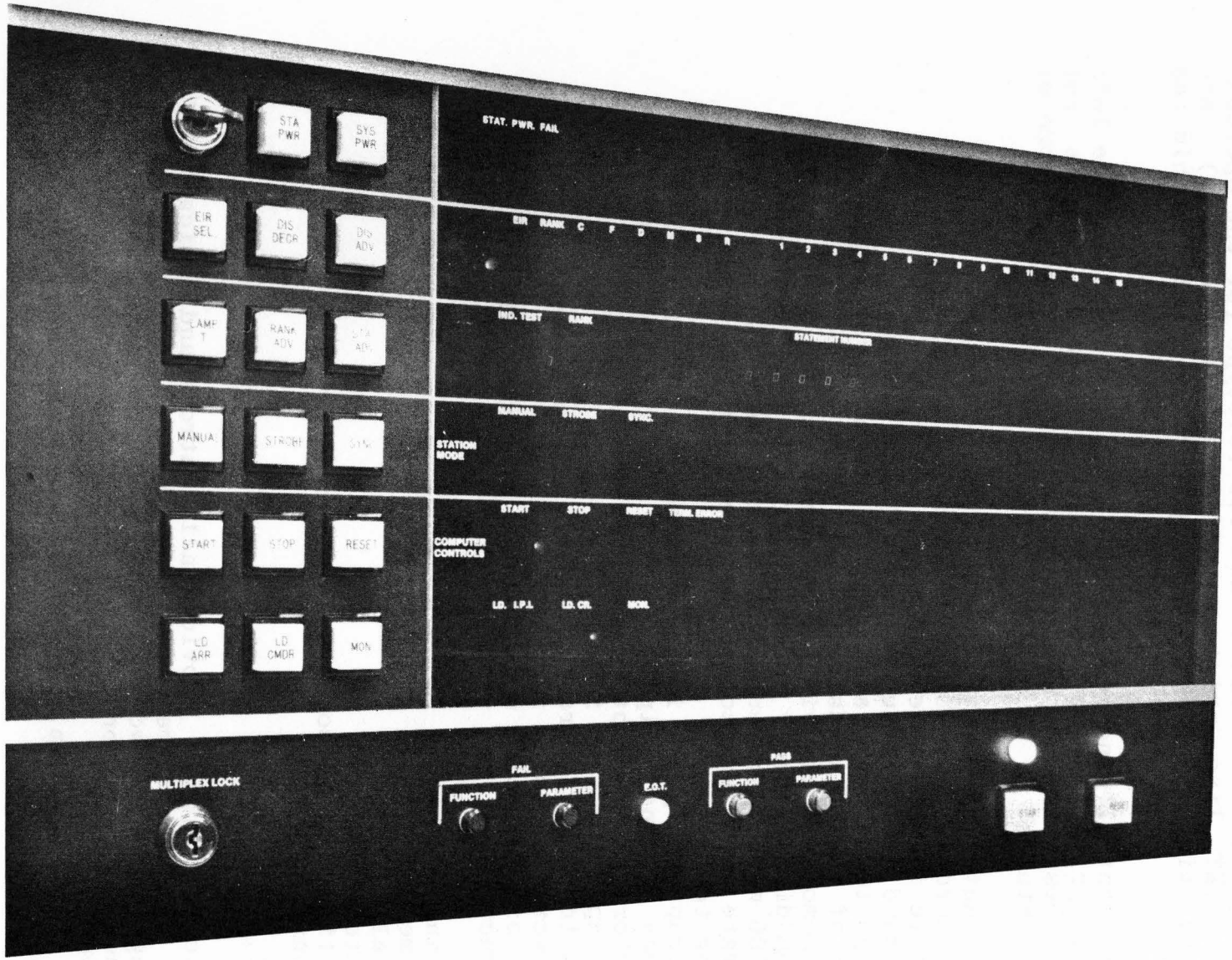


FIGURE 1-2. S-100 TEST SYSTEM CONTROL PANEL

word locations; they are positioned directly above the CPU. The interface module (A3) does not exist in the case of the S-100 system. Interface between the FST-1 and the tester is accomplished via three interface cards located in the M2 module. Interface between the FST-1 and the teletype (or the optional peripherals VKT line printer and tape cassette unit) are accomplished via interface cards physically located within the CPU module.

The FST-1 control panel (Figure 1-3) is located behind the left panel and is primarily for maintenance personnel; it is not normally accessible to the operator. Listed below are some of the FST-1 features:

(1) 24-bit data word
(2) 1.75 microsecond memory-cycle time
(3) Magnetic ferrite-core memory
(4) 8192-word memory modules
(5) Options to comprise a maximum of two memory modules, a total of 16,384 words per CPU
(6) Dual memory-access via two memory buses
(7) Random direct memory access, stored or retrieved at 571,000 words per second per memory bus
(8) Separate interface control between memory modules and CPU or tester
(9) Interrupt subsystem for communications and data transfer between CPU and peripheral units via accumulator bus
(10) 16 external interrupt channels and a maximum of 63 interrupt locations in memory
(11) Seven index registers for address modification
(12) Indirect addressing for most instructions
(13) A six-bit operation code for the following types of instructions:

load and store
arithmetic
logical operations
register and state
conditional and unconditional branch (transfer-of-control)
shift
input/output

The maintenance panel provides all controls and indicators for the FST-1. The switch register provides a means of manually setting up a 24-bit word. The up position represents a binary '1' and the down position a binary '0'. The contents of various working registers may be displayed on the lamps above the switches. In the bottom right hand corner are located the main computer switches; i.e., START, STOP, etc.

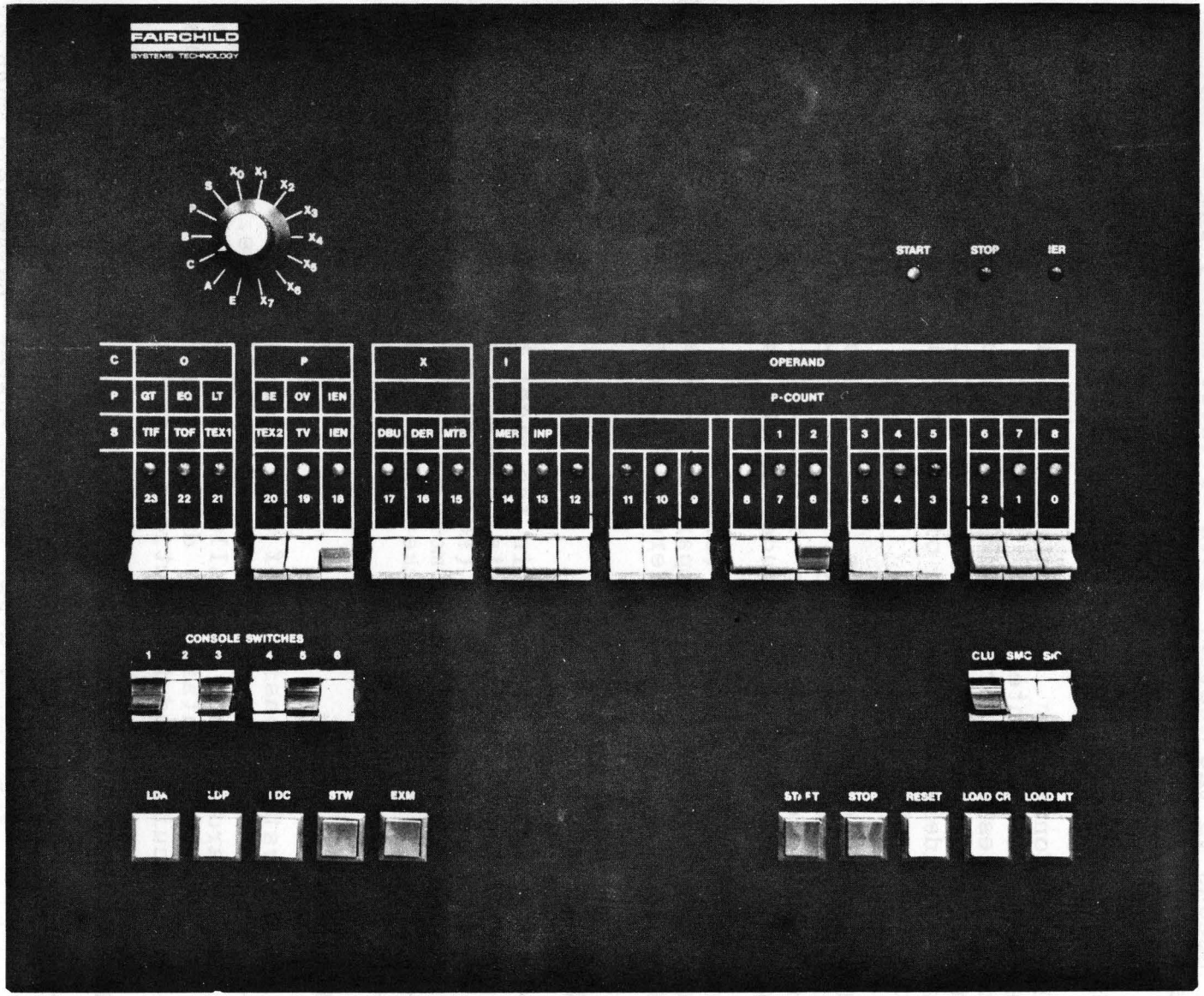


FIGURE 1-3. FST-1 COMPUTER CONTROL PANEL

The basic configuration for the FST-1 is shown in Figure 1-4. The A memory and B memory data buses are interfaced to the memory and are primarily used for transmitting functional test data at memory speeds to the tester. Both of these memory buses may be in operation at the same time.

1.1.4 Tester Controller

The Tester Controller is mounted on the backplane in the upper rear section of the center bay. The tester controller contains the computer/tester interface (M2) and various control and status registers. The controller contains such functions as initiation of hardware delays, execution of functional tests directly from the computer memory, etc.

The programmable Device Power Supplies and Reference Voltage Supplies are also mounted in the tester controller (M1). The output of these supplies is furnished to the test station in analog form. The supplies included in the basic system are:

One Device Power Supplies (DPS1)
One Pair of Functional Comparator Reference Supplies (S0, S1)
One Pair of Functional Reference Voltage Supplies (E0, E1)

1.1.5 Test Station

The Test Station is mounted in the right hand door frame. The lower backplane, where the Precision Measurement Unit is mounted, is present in all systems (R0). The upper backplane (R2) is present only in systems having more than 30 pins. On standard systems, one load board socket and input/output connector is provided for each backplane.

Pin Electronics

A minimum system consists of sufficient EUT Interface and Pin Control Logic circuit boards to drive 16 pins. Adding an additional card of each type allows an additional two pins to be used. These cards contain the driver amplifiers, comparators, and logic circuits used in functional testing.

Precision Measurement Unit

A Precision Measurement Unit is provided to measure the DC characteristics of the device-under-test. This type of testing is essential for specifying semiconductor parameters such as saturation voltage, input leakage, etc. The Precision Measurement Unit is capable of forcing a voltage or current on

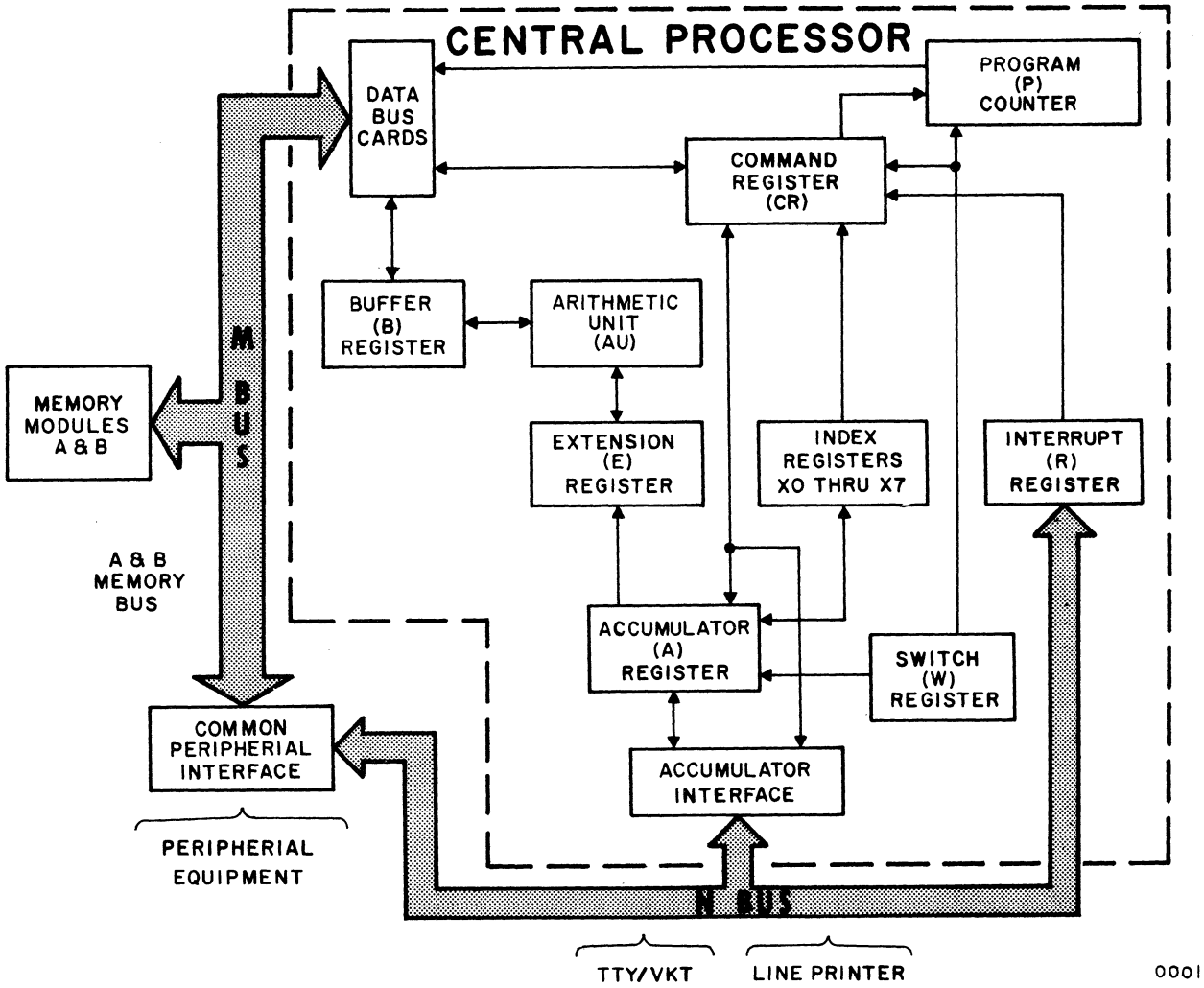


FIGURE 1-4. FST-1 COMPUTER SIMPLIFIED BLOCK DIAGRAM

any tester pin. The Precision Measurement Unit also is capable of measuring internal analog reference voltages and power supply voltages and currents for system self-checks. Measurements are made with a high-speed comparator with a 0.1% accuracy and resolution for voltages from 1 millivolt to 40 volts and currents from 1 nanoampere to 100 milliamperes. System software provides analog to digital conversion for data logging.

Load Boards

User designed load boards (or a performance board in the case of a sub multiplex station) allow unique requirements for a device or family of devices to be accomodated. The load board may be hardwired or switched under program control using the utility relay for each pin. The following list is typical of the hardware functions that may be implemented on the load board or performance board:

Power Supply Decoupling

Device power supply pins can be decoupled by connecting a capacitor in series with a utility relay. If it is necessary to perform a precision leakage test on the device supply pin, the utility relay can be opened prior to connecting the precision measurement unit to the device pin.

Input Bias Voltage

Unused power supplies can be connected to device input pins via utility relays to provide bias voltages. Up to two optional reference voltage supplies may be connected.

MOS Input Pin Stressing

Low-energy pulses can be applied to MOS input pins by connecting the user supplied pulse source to input pins via the utility relays. Control for the pulse source is derived from one of the external registers.

Clocking

An active circuit may be used to provide device clocking with pulse shaping if desired.

Output Pin Loading

Output pins can be loaded by either of the following methods:

(a) Connect a resistive load in series with the functional test driver and the device output pin (the functional

test level detector is also connected to the device output pin to allow concurrent GO/NO-GO testing). The load current for VOH/VOL is provided by switching the driver reference between EA1 and EA0 according to the output bit in the F register.

(b) Connect a resistive load to the device output pin in series with a utility relay and one of the programmable power supplies. Load current is then applied when the power supply is programmed to the appropriate voltage level.

EUT Connection

A connector for each backplane is mounted on pylons such that the connectors are positioned over a work surface when the right hand door of the system is closed. Each connector provides both force and sense connections for each tester pin. A mating connector may be used as a mount for a test socket for devices of less than 30 pins or connected via a cable to a remote socket, or a handler, or wafer prober, etc. Force and sense for each pin are tied together as close to the Element Under Test as practical so that line resistance does not affect measurement accuracy.

The system side of the connectors is wired to the load board sockets and the EUT Interface circuit boards.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-5 is a simplified block diagram of the Sentry 100 tester circuitry associated with one pin. A minimum system consists of circuitry for 16 pins. Driver/detector circuits are added in groups of 2 up to a maximum of 60 pins. The driver and detector permits each pin to be operated as an input pin, an output pin, both, or neither, depending upon programming of the registers.

The system provides two pairs of analog input references so that the programmer has the flexibility of choosing between two levels. One of the two input analog buses is selected by the 'S' register. Depending upon the excitation bit in the 'F' register, the driver is gated to produce a voltage equal to either the '1' or '0' level of the pair selected by the 'S' register.

If the device pin is an input pin, a '1' bit in the 'D' register closes relay R1. The output of the driver is applied to the pin of the DUT. If the device pin is an output pin, a '0' bit in the 'D' register opens relay R1. The pin of the DUT is now connected only to the input of the detector. The detector also receives an input level proportional to the expected output. If the device

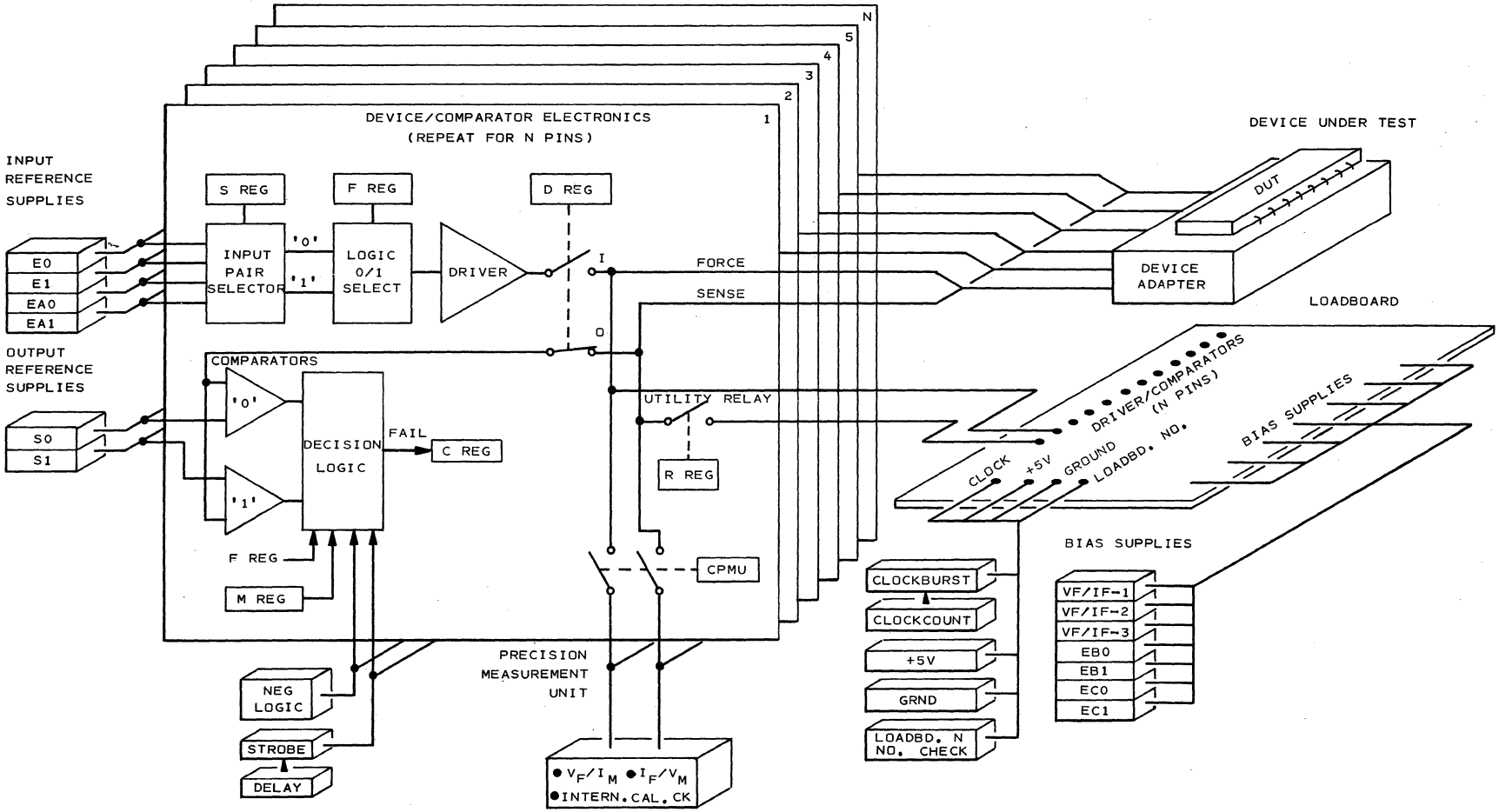


FIGURE 1-5 S100 SIMPLIFIED BLOCK DIAGRAM

pin is an output, the expected output is compared with the actual output of the pin. If the inputs are within the programmed limits, the detector will provide a '0' output that is interpreted as a pass condition. If no comparison exists, the detector will provide a '1' output that is interpreted as a fail condition.

The detectors are always connected to the sense line through relay R0 except when the PMU is addressed to that pin. The level on a pin can therefore be sensed whether it is an input pin or an output pin.

The detector also receives an input from the M register (mask register). If the programmer is interested in the output, the 'M' register is programmed as a '1'. The '1' condition enables the detector to make the comparison between the actual output and the expected output. If the programmer is not interested in the output level of the pin the 'M' register is programmed as a '0'. The '0' condition inhibits the output of the detector. The 'C' register and the function test fail output will indicate a pass.

Figure 1-6 is a simplified block diagram of the digital portion of the tester. Interface between the FST-1 computer and the tester is provided by the CPI cards, which also contains the memory address register (MAR). Various other working registers are enterfaced to the peripheral data buss and to the long and short register data busses. Details of the operation and function of these registers are contained in the following sections.

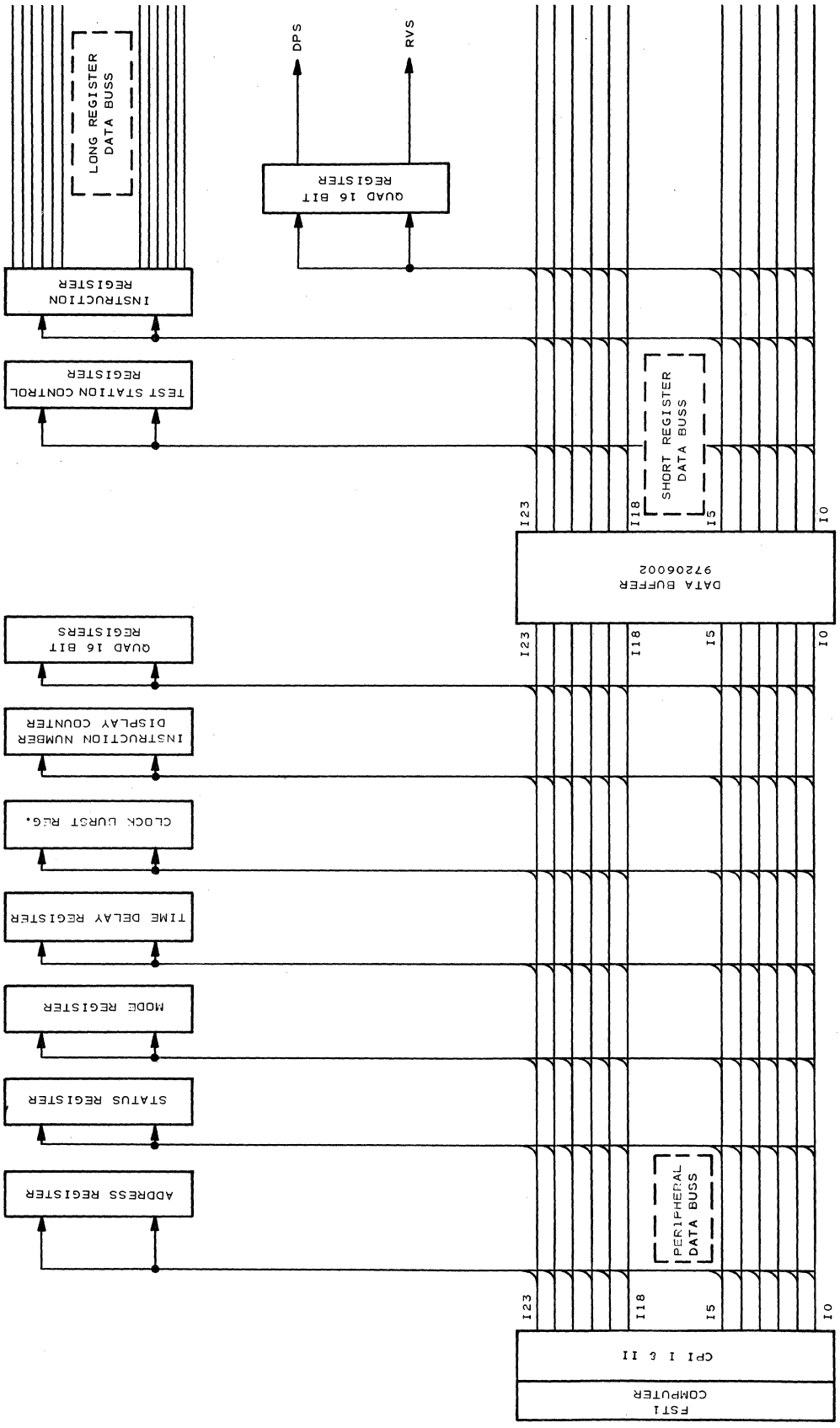


FIGURE 1-6. S100 SIMPLIFIED (DIGITAL)

Section II
Functional Description

2.0 SYSTEM BLOCK DIAGRAM

A simplified block diagram of the S100 system is shown in Figure 2-1. The computer and I/O peripherals are not represented on this diagram. The possibility for analog multiplexing to four test stations is indicated.

Figure 2-22 is a more detailed system block diagram. In this figure the computer and I/O peripherals are represented, and a single test station is detailed as a typical case. The system as shown in this figure is composed of four major blocks -- I/O Peripherals, Computer, Mainframe, and Test Station. The Computer block includes the CPU (Central Processing Unit), Core Memory, Computer Control Panel, I/O CPI's (Common Peripheral Interface), and Tester CPI.

The Mainframe Block contains all Short Registers and their associated logic circuitry, as well as the RVS and DPS power supplies. Also shown are the three 24-bit data buses (Peripheral Data Bus, Short Register Data Bus, and Long Register Data Bus). The functions of these registers and buses are discussed in detail in Section 2.2 below. The overall function of the Mainframe block is to control the operation of the Test Station(s) in accordance with the programmed information resident in Computer Core Memory.

The Test Station block contains all long registers and pin electronics, including the PMU (Precision Measurement Unit).

In the S100 System, the Computer, Mainframe, and one Test Station are all physically housed in a single console. With a submux option (8438, 8439), up to four test stations may be accomodated, housed at remote locations.

Within each major block, dotted lines enclose individual printed circuit boards. Separate descriptions for each of these boards are presented in Section 2.3.

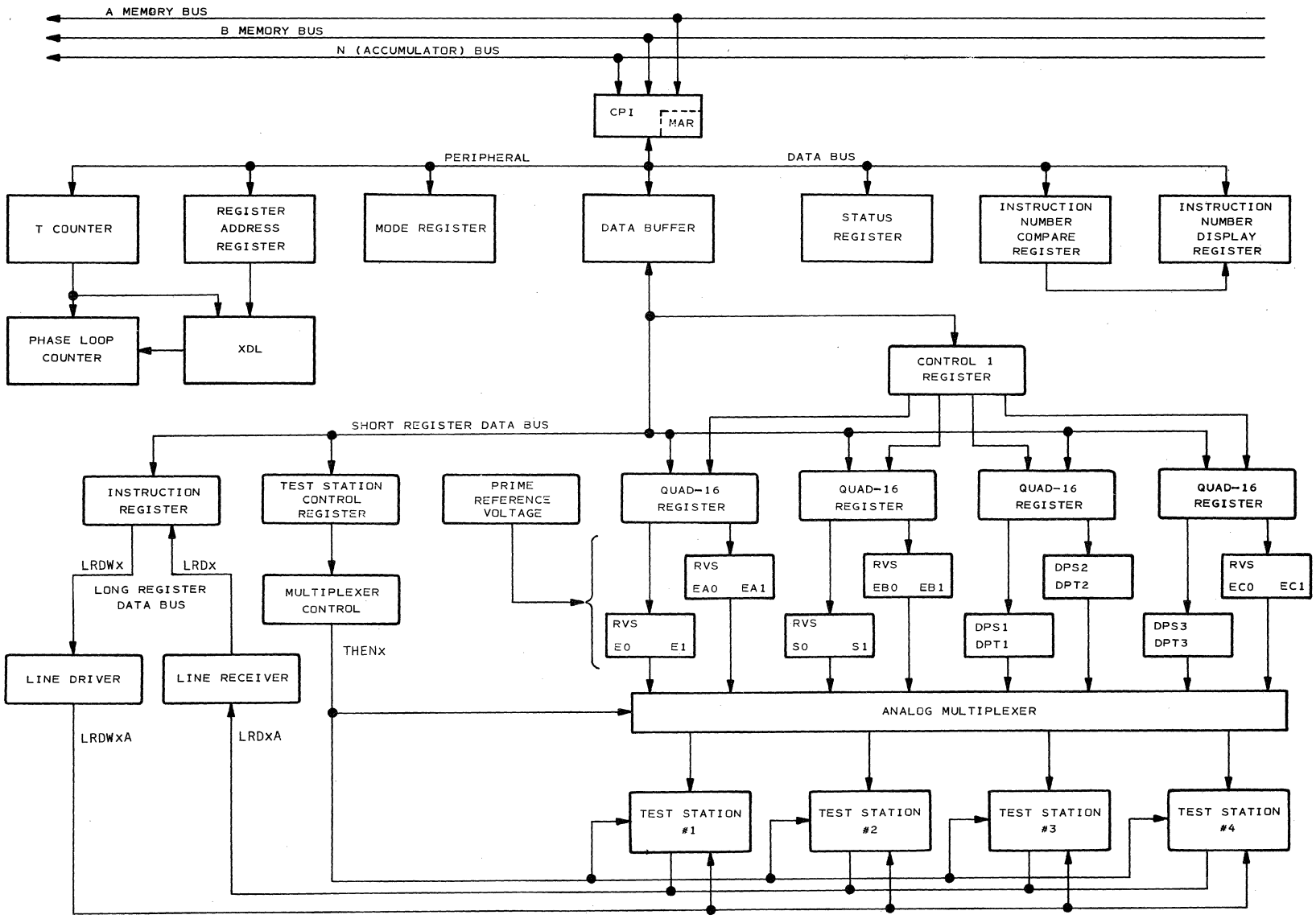


FIGURE 2-1. S100 SIMPLIFIED BLOCK DIAGRAM

2.1 REGISTERS & DATA BUSSES

The registers in the S100 system are grouped into two categories -- short registers and long registers. Table 2-2 lists the short registers and table 2-1 lists the long registers. There are two groups of short registers. The first group is used for tester control. The second group controls the programmable dc power supplies which provide the functional logic level test voltages to the test station. There are also two groups of long registers, the variable length (D, M, F, S, C, and R) registers, and the fixed length special registers.

All short registers are programmed by SPU instructions. Depending on the SPU data control field, NO OP, WRITE, READ, or SPECIAL operations may be performed. SPECIAL operations are defined for each individual short register; the other operations are self explanatory.

DMA write instructions are applied to the peripheral data bus, through the data buffer, through the instruction register, through the line driver board to the line receiver board in the test station. The DMA write instructions are routed from the line receiver to the pin control boards where they are applied to the D, M, F, S, C, and R registers, or they are routed to the special registers. The instructions applied to the pin control D, M, F, S, C, and R registers are used to control the application of functional test stimuli and monitoring of functional test responses by the EUT interface boards.

The functional test logic level voltages are generated by A/D converters, controlled by the contents of the corresponding short registers. These voltages are applied through the analog mux cable card directly to the EUT interface boards or the load (performance) boards. These programmable voltages are then applied to the pins under test, used as comparison references, or applied to load boards, in accordance with the specific D, M, F, S, C, and R commands to the pin control boards. Certain special test registers control the dc parametric testing by the PMU (precision measurement unit). The dc parametric voltages developed by the PMU are applied to the EUT interface cards prior to application to the DUT (device under test).

TABLE 2-1. LONG REGISTERS

REGISTER NAME	NUMBER
D	020-207
M	040-047
F	060-067
S	100-107
C	120-127
R	140-147
PA	160
SID	161
SND	162
CS	163
PPS	164
PSL	165
EIR	166
DCT	171

TABLE 2-2. SHORT REGISTERS

REGISTER NAME	NUMBER
	Tester Control
Register Address	N/A*
Mode	01
Status	02
MAR	04
CBC (P/O T COUNTER)	10
TDC (P/O T COUNTER)	11
INC (P/O QUAD 16)	14
IND (P/O TCOUNTER)	15
Instruction	03
TSC (P/O MUX CTL)	05
	Programmable RVS and DPS Control
EA0 (P/O QUAD 16)	37
EA1 (P/O QUAD 16)	36
E0 (P/O QUAD 16)	33
E1 (P/O QUAD 16)	32
EB0 (P/O QUAD 16)	42
EB1 (P/O QUAD 16)	43
S0 (P/O QUAD 16)	35

TABLE 2-2. SHORT REGISTERS (Continued)

REGISTER NAME	NUMBER
S1 (P/O QUAD 16)	34
DPS1 (P/O QUAD 16)	21
DPT1 (P/O QUAD 16)	26
DPS2 (P/O QUAD 16)	22
DPT2 (P/O QUAD 16)	25
EC0 (P/O QUAD 16)	45
EC1 (P/O QUAD 16)	44
DPS3 (P/O QUAD 16)	24
DPT3 (P/O QUAD 16)	23

*The register address card is not addressed by an SPU command, but is always on line to the P bus. The register address in turn enables the mode (01), status (02), I (03), MAR (04), TSC (05) and the control 1. Control 1 in turn enables quad 16 registers (37), (36), (33), (32), (42), (43), (35), (34), (21), (26), (22), (25), (45), (44), (24), and (23). The CBC (10), TDC (11), INC (14), and IND (15) registers are enabled by the XDL counter card as a result of AR0 through AR5 signals.

2.2 COMPUTER & TESTER DATA FLOW

The main data flow between the computer, the computer core memory, and the peripheral CPI's takes place on three 24-bit data buses, as shown in Figure 2-1. These are:

1. N Bus (Accumulator Bus)

2. A Memory Bus

3. B Memory Bus

The main data flow within the tester takes place on three 24-bit data buses, which are:

1. Peripheral Data Bus (PDB)

2. Short-Register Data Bus (SRDB)

3. Long-Register Data Bus (LRDB)

2.2.1 Peripheral Data Bus

Instructions are transferred from the computer's accumulator bus, the A memory bus, or the B memory bus, under the control of the CPI 3 board, through the CPI 1 and the CPI 2 boards, through the tester 24-bit peripheral data bus, to the register address register, the status register, the mode register, and the data buffer boards.

Once the tester is addressed by the computer, 24-bit instructions with a unit address of 120 can be transferred from the accumulator bus through the CPI 1 and the CPI 2 cards to the tester peripheral data bus. The tester peripheral data bus transfers this information through the data buffer card to the short register data bus, which can be regarded as an extension of the peripheral data bus. The data buffer card, placed between the peripheral data and the short register data buses, extends the drive (fan-out) capabilities of the peripheral data bus.

The peripheral data bus (P data bus) transfers information to the short registers listed in Table 2-3.

TABLE 2-3. SHORT REGISTERS LOADED BY PERIPHERAL DATA BUS

REGISTER	NUMBER
Register Address	N/A
Mode	01
Status	02
MAR (P/O CP1 I and CPI 2)	04
CBC (P/O "T" CTR)	10
TDCR (P/O "T" CTR)	11
INC	14
IND (P/O "T" CTR)	15
Data Buffer	N/A

2.2.2 Short Register Data Bus

The short register data bus (SRDB) applies data to certain short registers, which are a fixed number of bits in length and receive information from the peripheral data bus through the data buffer. They communicate tester status (mode and interrupt information) and control digital-to-analog subsystems by means of four quad 16 bit registers. These short registers are:

REGISTER	NUMBER
Test Station Control Register (TSC)	05
Instruction Register (I)	03
Quad 16 Bit Registers	See Table 2-2

2.2.2.1 Short Register Descriptions

A general description of each register follows. For a more detailed functional flow discussion, refer to the SPU detailed descriptions or DMA detailed decriptions presented later in this manual.

Register Address

The register address board receives and stores the programmed register address issued during phase time T4 of a computer SPU command.

The short register address is loaded from bits 8-13 of the P data bus when select device (SELDEV) is on. SELDEV is generated on the CPI 3 board, when the tester address 120B is decoded at time T4. During times T5 and T1, these six bits are decoded to generate one of 64 possible addresses. Then at time T2, bits 8 through 13 are cleared and the register is preset for the next SPU command.

Some short register addresses are decoded on this card (I, memory address, mode, status, and TSC registers). The signals generated are load memory address register (LMARD/), read memory address register (PRMAR/), gate I to S (GITS/), clear status register (CSTAT/), status load (STATL/), read status register (RSTAT), clear mode register (CMODE/), write mode register (WMODE), read mode register (RMODE), write test station control register (WTSC/), and read TSC (RTSC/). In addition to the six register address bits which are loaded from bits 8 through 13 of the SPU word, bits 16 and 17, which contain read/write control instructions, are also loaded into the register address board. Bit 17 is called NXFR (accumulator data transfer) and bit 16 is called PTN (P-to-N bus transfer). Their read/write function is as follows:

X17 NXFR	X16 PTN	
0	0	NO-OP (No-operation)
0	1	Special (no data transfer)
1	0	Write
1	1	Read

Additional address decoding is done on the XDL board (time delay, clock burst, instruction number display, and instruction number compare registers) and control 1 card (DPS1, DPS2, DPS3, DPT1, DPT2, DPT3, E0, E1, EA0, EA1, EB0, EB1, EC0 and EC1 registers). Of the possible 64 addresses, 25 are utilized (including two NO-OP addresses consisting of all 1's and all 0's). The command interrupt flip-flop is lcoated on this board and is discussed in the status register description.

Mode Register (01)

The mode register is a 16-bit register that uses 14 bits and includes 2 spares. Table 2-4 describes the function of each mode register bit.

TABLE 2-4. MODE REGISTER BIT DESCRIPTION

BIT	FUNCTION	READ	WRITE
0	Resets the short registers while WMODE is true.		X
1	Resets the long registers while WMODE is true.		X
2	Indicates monitor display lamp on.		
3	Indicates automatic mode.	X	
4	Sets the negative logic mode of operation. This must be programmed in the FACTOR program and causes the tester to look for the opposite logic signal in the C register, which is normally set up for positive true logic.	X	X
5	Selects the latch-C mode of operation. The latch-C mode permits the C register to accumulate function test failures.	X	X
6	Sets the strobe inhibit mode. This mode inhibits the strobe C signal that would	X	X

TABLE 2-4. MODE REGISTER BIT DESCRIPTION (Continued)

BIT	FUNCTION	READ	WRITE
	otherwise enable the pass/fail data from each function test to be strobed into the C register.		
7	Generates a C-register strobe.		
8	Generates a train of sync pulses, the period of which is determined by the present count in the time delay register.		X
9	Sets the DMA mode of operation which enables long register instructions (long-register data block) to be loaded into long registers from memory.		X
10	Indicates that the last instruction in DMA mode was to set a non-F register (D, M, R, or S).	X	X
11	Indicates that a function test suspended signal has occurred. Function test suspended is the condition achieved in the DMA mode when a function test failure has occurred and a new instruction has been read from memory and is pending.	X	X
12	Indicates that a trip failure has occured, i.e., that one of the DPS power supplies has reached its programmable or fixed current trip point.	X	X
13	Indicates that a failure has occurred in one of the function tests on the unit under test.	X	X
14	Not used.	X	X
15	Spare	X	X

NOTE

A special SPU command (bit 16 = 1, bit 17 = 0) written to the mode register clears the mode register.

Status Register (02)

The status register receives enabling signals from bits 0-14 of the P data bus. The status register records the state of the six tester interrupts. If the interrupt is enabled, the status register gates the address of the appropriate interrupt subroutine. The six tester interrupts are:

1. Stop: the stop bit is set by pressing RESET on the test station or by a computer reset signal.

2. Instruction Number Compare: this bit is generated whenever the present executing instruction number compares with a number previously loaded into the system by the operator.

3. Trap: the trap bit is set whenever the last long register instruction of any DMA long register data block is decoded. This bit causes the tester to reset the DMA mode of operation.

4. Delay Complete: this bit indicates that a fixed or programmed delay has been executed and the computer is now ready to execute the remaining program.

5. DC Trip: the trip bit will be set if a programmed power supply exceeds its predetermined trip value in voltage or current mode.

6. Fail: the fail bit will be set if any functional test on the DUT fails, or if the PMU measurement exceeds the programmed limit.

Table 2-5 describes the function of each status register bit.

TABLE 2-5. STATUS REGISTER BIT DESCRIPTION

BIT	FUNCTION	READ	WRITE
0	Instruction number compare interrupt enable signal, which allows the tester to respond to the instruction number compare interrupt signal.	X	X
1	Instruction number compare interrupt, which indicates that the instruction number comparison has been reached. This condition	X	X

TABLE 2-5. STATUS REGISTER BIT DESCRIPTION(Continued)

BIT	FUNCTION	READ	WRITE
	occurs when the IND counter and the INC register hold the same number.		
2	Delay complete interrupt enable signal.	X	X
3	Delay complete interrupt. Indicates that the time delay counter has completed its count. This interrupt is used only for programmed DC delays.	X	X
4	Trap interrupt enable signal.	X	X
5	Trap interrupt bit, which is set upon completion of long-register data block loading while in the DMA mode.	X	X
6	Fail interrupt enable signal.	X	X
7	Fail interrupt resulting from a functional test failure.	X	X
8	Trip interrupt enable signal.	X	X
9, 10, & 11	Bits 9, 10 and 11 are the DPS1 trip, DPS2 trip and DPS3 trip, respectively. In each case bit 8 must be set to allow either the programmable or the fixed trip from DPS1, 2 or 3 to cause an interrupt in the computer.	X X X X	X X X X
12	Stop interrupt enable signal.	X	X
13	Stop interrupt signal, which halts the tester program when bit 12 has been set.	X	X
14	Common bit from all of the interrupts, which indicates that some interrupt is pending and that the program is not to continue until the interrupt has been processed.	X	

Memory Address Register, MAR (04)

The memory address register points to the address of the next DMA instruction, and is contained on the CPI 1 and CPI 2 boards.

An instruction may be written into or read from the memory address register. The memory address register stores and updates the memory address of the long-register data block, whenever the tester goes into the DMA mode. The memory address register is 14 bits long.

Clock Burst Counter Register (10)

The clock burst count register is an eight-bit register and counter used to generate a programmable number of clock pulses for conditioning a device for testing. The number of pulses in the programmable clock burst is controlled by programming the time delay register. The computer can read all eight bits in order to determine the count stored in the register, as well as write the programmed value.

Time Delay Register (11)

The time delay register accommodates 14 read/write bits, which represent a value of functional test or DC test time delay to be generated by certain tester instructions.

For functional tests, the least significant bit of the time delay register represents 350 nanoseconds, and full scale is 5.734 milliseconds.

The phase loop counter triggers the time delay counter when a set F instruction is executed. A Time Delay Special SPU command triggers the counter for DC delays. For DC tests the least significant bit represents 0.35 milliseconds, and the full scale value is 5.734 seconds.

Instruction Number Compare Register (14)

This register is loaded with the statement or instruction number on which a tester stop or pause is desired. The instruction number compare register utilizes 16 read/write bits, which represent the test instruction number. The test set can be programmed to pause or stop whenever the number in the INC register and the number in the instruction display counter are the same. Also, a sync pulse (brought to a front panel jack) may be generated at the same time, which is useful for troubleshooting and for semi-manual operation.

Instruction Number Display Register (15)

The instruction number display register, which works in conjunction with the instruction number compare register, utilizes 16 read/write bits. These bits represent the number of the test instruction being executed.

Data Buffer

The data buffer is not a register, but provides the gain required to extend the fan-out capabilities of the P data bus. This buffer has a 24-bit, parallel capacity (the same as the P data bus) and can be written through to the short-register data bus or read from the short-register data buss to the P data bus.

Test Station Control Register (05)

The test station control register is located on the multiplex control board and is used to generate Start, Reset, and Manual signals, and to select the desired main station.

The test station control register is loaded from bits 0 through 13. Bits 0 and 1 are used as the main station address. Bits 2 through 5 are read-only. Bits 2 through 5 provide Start request signals from the main test stations. Bits 6 through 9 are read-only, and provide Start request signals from the main test stations when in the manual mode. In the S100 system, there is one test station. Bits 10 through 13 are read-only and provide the Reset request signals from the test stations.

Instruction Register (03)

The instruction register is a buffer between memory and the long registers, which are located in the test station. At any given time it contains 24 bits of information. Bits 0 through 14 contain pin information for 15 pins (1 through 15 or 16 through 30 or 31 through 45, etc.) depending upon rank address.

Bits 15 through 18 are the rank address, which can be rank 0 through 7. Bits 19, 20 and 21 are the register address for the F, M, R, C, D, or S registers, and bits 22 and 23 are the long-register read/write control bits. The instruction register is used in the DMA mode. It may also be read or written, as any other short register.

Quad 16 Bit Registers - RVS and DPS Power Supply Control.

The digitally programmed power supply addresses are 21, 22 and 24 for DPS1, DPS2 and DPS3, respectively. The DPS's utilize bits 0 through 9 for the voltage magnitude, with bit 0 as the least significant bit. Bit 10 is the polarity bit, bit 11 is the range bit. There are two ranges, a low range and a high range. An SPU Special command to a DPS power supply disconnects that power supply and shuts it off. An SPU Write command to a DPS register connects that power supply.

The current trip register addresses are 26, 25 and 23 for DPT1, DPT2 and DPT3, respectively. There are 14 bits used to program the trip modes for the DPS power supplies. To set a current trip point, bits 0 through 9 of the DPT registers are programmed for current magnitude, bit 10 is the polarity of the current trip, bit 11 is the range. There are two ranges. Bit 13 specifies whether the current value is less than or greater than the value programmed in bits 0 through 9. Bit 14 in the trip register indicates whether it is to be a voltage force or current force condition.

The reference voltage supplies are controlled by registers E1 (32), E0 (33), S1 (34), S0 (35), EA1 (36), EA0 (37), EB1 (42), EB0 (43), EC1 (44) and EC0 (45) (all 12-bit registers). Bits 0 through 11 are used to program the reference voltage power supplies to the selected range, polarity, and magnitude for application to the EUT interface card. Bits 0 through 9, as above, are the voltage magnitude. Bit 10 of the reference voltage supply register is the polarity bit. Bit 11 is the range bit, with two ranges available.

The control 1 board receives AR0 through AR5 address signals from the register address board, which originated as bits 8-13 of an SPU command. The control 1 board decodes these address codes and applies them to the appropriate quad 16 bit register. The control 1 board also initiates the correct fixed delay associated with that address and, in the case of a DPS, closes the output relays to connect the DPS to the load board.

The fixed time delay counter is located on the execute delay loop counter board (XDL counter). The fixed time delay counter is actuated by signals 1DLS or 3DLS, which are generated when a reference voltage supply or DPS bias supply is programmed. Signal 1DLS (560-usec delay) is generated whenever a reference voltage supply is programmed. The 3DLS (1.792-msec delay) is generated when a DPS bias supply is programmed. These delays are necessary to allow the relays in the supplies to close and the voltage outputs to reach the programmed value. All fixed delay times are as follows:

.5DLS	=	280 usec
1DLS	=	560 usec
3DLS	=	1.792 msec

2.2.3 Long Register Data Bus

The long-register data bus (LRDB) applies data to the registers in the test station. Bits 15 through 21 of the I register are used as addressing codes and are applied to test station decoding logic (120 pin decoder and 15 pin decoder boards) which enables the correct long register. Bits 0 through 14 are applied to the long-register data bus and loaded into the enabled long register.

All long registers are loaded with information from the long-register data bus, which originates at the outputs of the instruction register. Data being transferred from the computer to the instruction register during a device test program is normally controlled by the direct memory access (DMA) mode of operation. It is true that an SPU command appearing on the P data bus could address and load data into the instruction register, but this procedure is normally used only in diagnostic programs designed to check the system for correct operation, and for software A/D conversions. The instruction register applies bits 19 through 23 to decoding logic in the system. Bits 19-23 of any 24-bit functional control word contain the address of the long register to be accessed and whether the instruction is to write into, or read from the register. There are two other functions of bits 22 and 23:

1. Determine whether or not to execute the test immediately or wait until the next word is transferred from memory.

2. To detect the trap bits used to indicate the last 24-bit function word of a long register data block. These signals and address codes are wired to the phase loop counter board.

The phase loop counter receives data from the I register decoding logic and from the execute delay loop (XDL) board. The phase loop counter controls system timing in the DMA mode. It fetches the long register instruction from memory, gates it to the I register, decodes the address and the read, write and hold, trap, and write and execute functions. The phase loop counter then initiates tester activities dependent on the register address and the read, write and hold, trap, and write and execute functions.

2.2.3.1 Long Register Descriptions

There are two groups (refer to Table 2-1) of long registers. The first group is comprised of the D, S, M, F, C, and R registers. The second group is comprised of special registers as follows:

REGISTER	NO.	FUNCTION
Pin Address (PA)	160	Addresses the precision measuring unit to any tester pin or to an internal node.
Socket Identification (SID)	161	Reads a hardwired address on a load board for FACTOR program comparison.
Statement Number Display (SND)	162	Contains the statement number to be displayed on the test station control panel.
Precision Power Supply (PPS)	164	Controls the forcing output of the precision measurement unit.
Precision Sense Level (PSL)	165	Controls the measuring circuitry of the precision measurement unit.
External Interface (EIR)	166	May be used to display test results and to control external functions.
Slave TSC (STSC)	167	Duplicates TSC register functions for Sub-Mux system.
D.C. Trip (DCT)	171	Contains PMU GO/NO-GO limit.

Bits 0-14 of the DMA instruction are applied to the D, M, F, S, C, and R registers, or to the special registers as applicable. The D, M, F, S, C, and R registers are contained in the pin control cards. Bits 15 through 18 are applied to the 15 bit decoder board, and bits 19 through 23 are applied to the 120 bit decoder board.

The main function of the 120 bit decoder board is to decode bits 19 through 21 of each instruction word and provide a D, S, M, F, C, or R enable to the pin control cards, as applicable for that word. The main function of the 15 bit decoder board is to decode

bits 15 through 18 of each instruction word and provide a 0, 1, 2, 3, 4, 5, 6, or 7 rank enable, as applicable for that word.

For each pin, the tester provides a voltage conditioner (driver), two level detectors (comparators), a utility relay, and one bit from each of six control registers, D, F, S, C, M, and R. A general description of each register follows. For a more detailed functional flow discussion, refer to the SPU detailed descriptions and DMA detailed descriptions presented later in this section.

D Register (Input/Output Definition Register)

Each bit of the D register controls the connection of the voltage conditioner associated with its pin. A one valued bit connects the voltage conditioner, driving the pin of the device under test and thereby treating it as an input pin, and a zero disconnects the voltage conditioner. Level detectors remain connected during function testing.

M Register (Mask Register)

Each bit of the M register enables setting a one into the corresponding bit of the C register. A one in the M register allows setting of the C register to one, while a zero inhibits this. A one therefore determines that the device under test pin is to be monitored.

F Register (Function Register)

The F register contains desired function test patterns for the device under test inputs and expected function patterns out. A one valued bit in the F register connects its associated voltage conditioner input to the E1 or EA1 reference supply and is compared with the level detector outputs. A zero connects the voltage conditioner input to E0 or EA0 and again is compared with level detector outputs.

S Register (Select Reference Register)

Each bit of the S register controls the connection of the voltage conditioner inputs to the E0-E1 or EA0-EA1 reference supplies. A one valued bit selects the EA0-EA1 pair, a zero the E0-E1 pair.

C Register (Comparison Register)

Each bit of the C register is set to one if its associated pin is in the wrong state and if the M register enables the comparison. The wrong state is determined by the content of the corresponding

F register bit, the level detector outputs and the negative logic control from the mode register. When any C register bit is set to one, a function test failure is assumed. The C register is normally reset before each function test, but the reset can be inhibited by the enable C latches bit from the mode register, allowing accumulation of failure data.

R Register (Relay Register)

Each bit of the R register controls the utility relay of the corresponding DUT pin. A one closes the relay, a zero opens it. The utility relays are provided to allow connection of DPS's, RVS's, loads, clock drivers, etc., to the device under test.

TABLE 2-6. FUNCTION OF D, M, F, S, C, AND R REGISTERS

REGISTER	FUNCTION
D	Input/Output Pin Definition Register - defines each tester pin as an input or an output pin. A logical 1 signifies input, and a logical 0 signifies output for the associated tester pin.
M	Mask Register - controls the care/don't care condition for each tester pin. A logical 0 (don't care) inhibits the comparison operation for that particular pin, while a logical 1 (care) enables the comparison operations.
F	Function Register - represents the input forcing logic for those pins programmed as inputs and the expected output response for those pins programmed as outputs in the D register.
S	Select Reference Register - selects which set of reference supplies are to be used by the functional test driver for each tester pin. A logical 0 selects the E0/E1 reference supplies, while a logical 1 selects the EA0/ EA1 reference supplies.
C	Comparison Register - this register stores the GO/NO-GO results of a comparison between the actual outputs of a device and the expected outputs. A logical 1 signifies a comparison

TABLE 2-6. FUNCTION OF D, M, F, S, C, AND R REGISTERS (CONTINUED)

REGISTER	FUNCTION
	failure while a logical 0 signifies a pass condition.
R	Utility Relay Register - controls the utility relays, one per tester pin. A logical 1 signifies a closed relay, while a logical 0 signifies an open relay. The utility relays can be used for such functions as connecting a load resistor for an output pin to a programmable power supply.

PA Register (Pin Address Register)

The pin address register is programmed by eight bits of information. The pin address register addresses the relay driver logic on each EUT interface card, closing the relay on the pin to be measured. This relay attaches the addressed pin to the PMU bus. Internal system nodes may also be programmed. For example, the PMU is able to monitor the voltage output or the load current for each DPS. It is also able to monitor the output of any one of the reference voltage supplies. Bits 0 through 3 of the pin address register select the test head pin or the internal node pin. Bits 4 through 6 of the pin address register select one of eight ranks (0 through 7). Bit 7 represents the internal node address, and bit 8 selects connection to a voltage conditioner.

SID Register (Socket Identification Register)

The socket identification register is a 12-bit, read-only long register. The input to the socket identification register comes from the load board that is plugged into the test station. The load board has jumper connections wired by the user, which enable the load board to be identified by the tester to insure proper selection for the device under test. The information is read from the load board and transferred immediately, by the long register data bus, to the accumulator bus. The computer then compares the socket identification code to the identification code in the particular FACTOR program.

SND Register (Statement Number Display Register)

The statement number display register is located on the test head control panel and consists of four type 9300 four-bit shift registers. The SND register is 15 bits long and has read and write capability. The SND register drives light emitting diodes to display the statement number, whenever the tester is in the manual mode of operation. In the automatic mode of operation it displays the end statement number. The statement number display register is interfaced to the instruction number display register with software under TOPSY control. It is updated whenever the sequence pauses, or whenever the software updates the statement display register.

CS Register (Clock and Strobe Register)

The clock and strobe register controls the enabling and generation of clock sync pulses. Bits 0, 1, 2, and 3 enable sync 1, 2, 3, 4, and disconnect the EUT functions of pins 1, 2, 3, and 4 from the device under test. Bits 4, 5, 6, and 7 are ANDed with the first four bits of the F register, and control generation of the sync 1, 2, 3, and 4 signals, which may be used to control clock drivers or other special signal generators for the DUT.

PPS Register (Precision Power Supply Register)

The precision power supply register contains the necessary bits to control the forcing function of the precision measurement unit (PMU). The PMU is a precision programmable power supply and measuring circuit, used for dc parametric tests and for system checkout. Bits 0 through 9 of the PPS register contain the magnitude of the forced value, from a minimum of 1 millivolt up to 40.92 volts, and from a minimum of 1 nanoampere up to 102.3 millamperes. Bit 10 selects polarity. Bits 11 and 12 provide four separate ranges, range 0, 1, 2 and 3. Bit 13 indicates whether it is to be a voltage force or a current force condition.

PSL Register (Precision Sense Level Register)

The PSL register is used to hold the information establishing the operating range for voltage or current measurements by the PMU, and specifying whether it is current or voltage that is to be measured. The PSL register also holds the information specifying voltage clamp vlaues. These values are upper and/or lower limits on the allowable voltage at the PMU output -- i.e., at the pin of the device under test.

Bits 0-3 of the PSL register specify the magnitude of the voltage clamp level. Bit 4 is the clamp enable bit. Bit 5 is not used in the S-100 system. Bits 6 and 7 specify, respectively, positive and negative clamp. Bits 8 and 9 are not used. Bit 10, range enable, is for data protection in the PSL register. If bit 10 is a 1, the sensing ranges (bits 11 and 12) can be programmed, and the clamp data (bits 0-7) is protected. If bit 10 is a 0, the voltage clamp can be programmed, and the range data is protected. Bits 11 and 12 determine the voltage or current sensing (measuring) range. Bit 13 specifies whether the measurement is a current or a voltage. Bit 13 of the PSL register is constrained to be the complement of bit 13 of the PPS register.

EIR Register (External Interface Register)

The external interface register is a 15-bit register that is used to display the test results and control optional external equipment. Bits 0 through 9 are available to the programmer to be used at his discretion. Bits 10 through 14 are defined by the system itself, where bit 10 controls the PARAMETER TEST FAIL lamp, bit 11 controls the PARAMETER TEST PASS lamp, bit 12 controls the FUNCTIONAL TEST FAIL lamp, bit 13 the FUNCTIONAL TEST PASS lamp, and bit 14 controls the EOT (end of test) lamp on the front panel). All 15 bits have both read and write capability.

DCT Register (DC Trip Register)

This 15-bit register holds the information used in the DC parametric voltage (or current) measuring process. Bits 0-9 and polarity bit 10 are fed to PMU DAC 2 to establish an analog comparison reference into the comparator. Bits 11 and 12 duplicate the corresponding bits of the PSL register, establishing the voltage (or current) range for measuring. Bits 13 and 14 are used in connection with DC GO/NO-GO testing. Bit 13=1 means "greater than"; bit 13=0 means " less than". Thus it is possible to specify (using bits 0-13) pass and fail thresholds for the measured voltage or current. This DC GO/NO-GO testing is carried out in direct memory access mode. When a GO/NO-GO measurement is executed, a DC strobe signal samples the comparator output. A failure generates a DC fail signal, which causes a functional test interrupt. A comparator fail signal during a strobe sets bit 14, while a comparator pass signal during a strobe resets this bit.

The DCT register is also used in the course of making a quantitative DC parametric (voltage or current) measurement. In this case, a software routine carries out an algorithm of successive approximations in bits 0-9 of the DCT register, until

the PMU DAC 2 output matches the corresponding measured quantity at the comparator input. In this way an A/D conversion is effected in about 350 microseconds.

2.3 INDIVIDUAL BOARD DESCRIPTIONS

The descriptions given below present each of the printed circuit boards from a functional point of view. The principal input and output signals are listed, and the overall function within the system is described. The circuitry found on the particular board and its main operations are discussed.

The sequence of these board descriptions follows the layout of Figure 2-22 the System Block Diagram, which the reader may use as a reference.

2.3.1 CPI 1 and CPI 2 (97166109)

The CPI 1 and CPI 2 boards are identical to each other and in conjunction with the CPI 3 board, form the common peripheral interface for the tester.

Each CPI board is specialized for a particular controller (peripheral address) by option plugs on the end of the board. The logic on the CPI boards decodes the peripheral address data on bits 0 through 7 of an SPU instruction and also provides bus-to-bus gating when enabled by the applicable signal from the CPI 3 board. The CPI 1 board transfers bits 0-7 and bits 16-19 between the peripheral data bus and the accumulator bus, or between the A and B memory buses and the peripheral data bus. The CPI 2 board transfers bits 8-15 and bits 20-23 between the peripheral data bus and the accumulator bus, or between the A and B memory buses and the peripheral data bus. The CPI 1 and the CPI 2 boards also contain memory address registers used to store the current memory address of direct memory access (DMA) data blocks.

The following signals are the main gating signals associated with the CPI 1 and the CPI 2 boards: write peripheral (WBP), read peripheral (RBP), write memory (WMB), read memory (RMB), device code 1 (DEVCO 1), device code 2 (DEVCO 2), and select device (SELDEV).

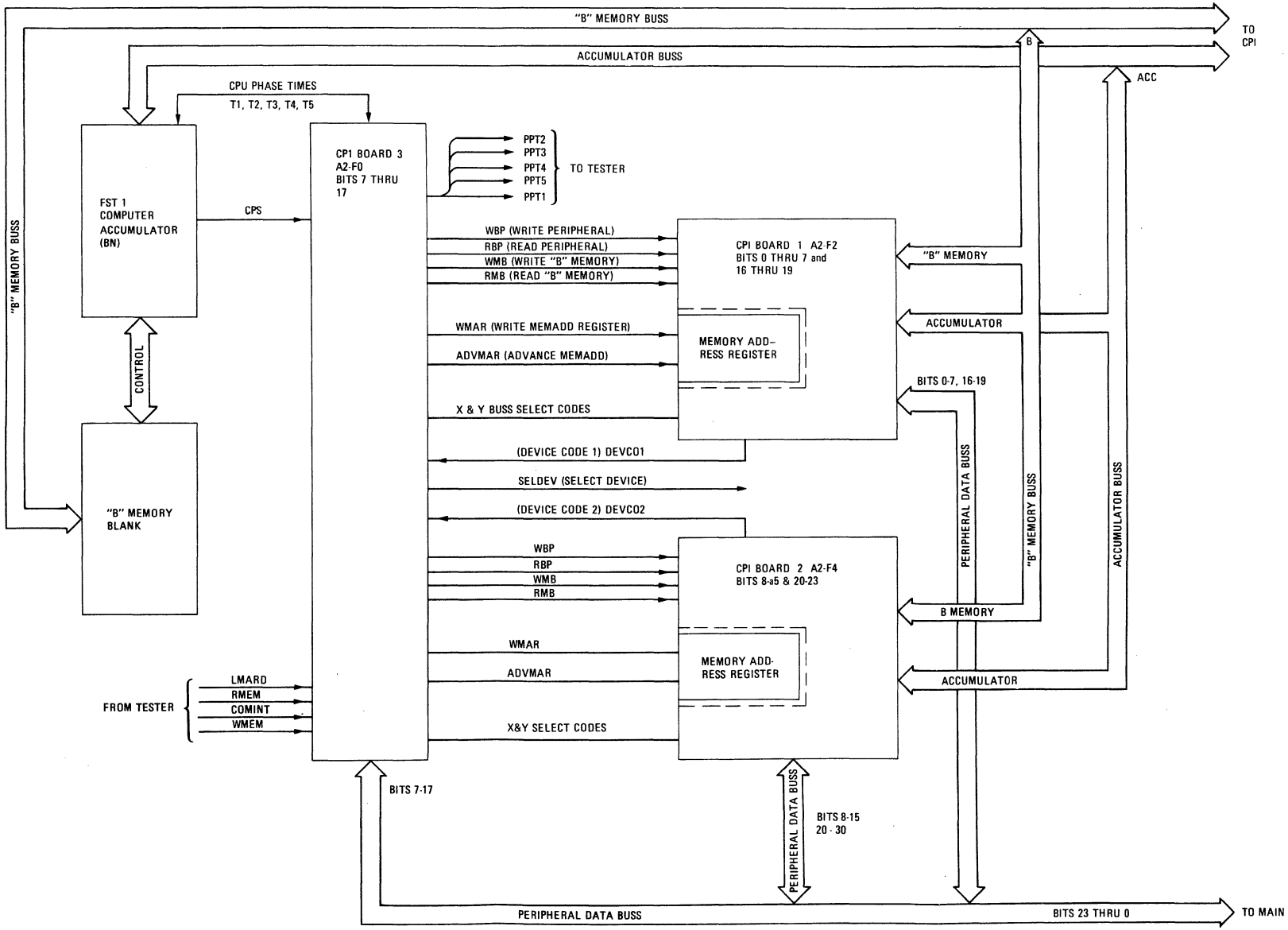


FIGURE 2-2. TESTER CPI, DETAILED BLOCK DIAGRAM

2.3.2 CPI 3 (97166108)

The CPI 3 board, in conjunction with the CPI 1 and the CPI 2 boards, forms the common peripheral interface for the tester. At computer phase time T4, the PS signal from the computer is ANDed with the DEVCO 1 signal from CPI 1 board to generate the SELDEV signal in the CPI 3 board. The SELDEV signal is applied to the CPI 1 and the CPI 2 boards to enable the transfer of data between the P data bus and the accumulator or between the P data bus and memory.

The CPI 3 board also generates write peripheral (WBP), read-peripheral (RBP), write memory (WMB), read memory (RMB), and write B memory from accumulator (WBNB). The SELDEV signal is also applied to the register address board in the tester where it gates bits 8 through 13, 16, and 17 from the peripheral data bus to the inputs of the register address storage elements.

2.3.3 Register Address A (97340803)

The basic logic function of the register address board is to receive and store the register address issued during phase time T4 of a select peripheral unit (SPU) command.

The short register address is loaded from bits 8-13 (six bits) of the P data bus when the select device (SELDEV) signal is on. SELDEV is generated on the CPI 3 board when tester address 120B is decoded at time T4. During time T5 and T1, these six bits are decoded to generate one of 64 possible register addresses. Then, at time T2, the six bits are cleared and the register readied for the next SPU command.

The short register addresses decoded on this board are the instruction (IRAD), the memory (MARAD), the mode (MODRAD), the status (STATRAD), and the TSC (TSCRAD) register addresses.

The signals generated are as follows:

1. Load Memory Address Register (LMARD/)

2. Read Memory Address Register (PRMAR/)

3. Gate I to S (GITS/)

4. Clear Status Register (CSTAT/)

5. Status Load (STATL/)

6. Read Status Register (RSTAT)

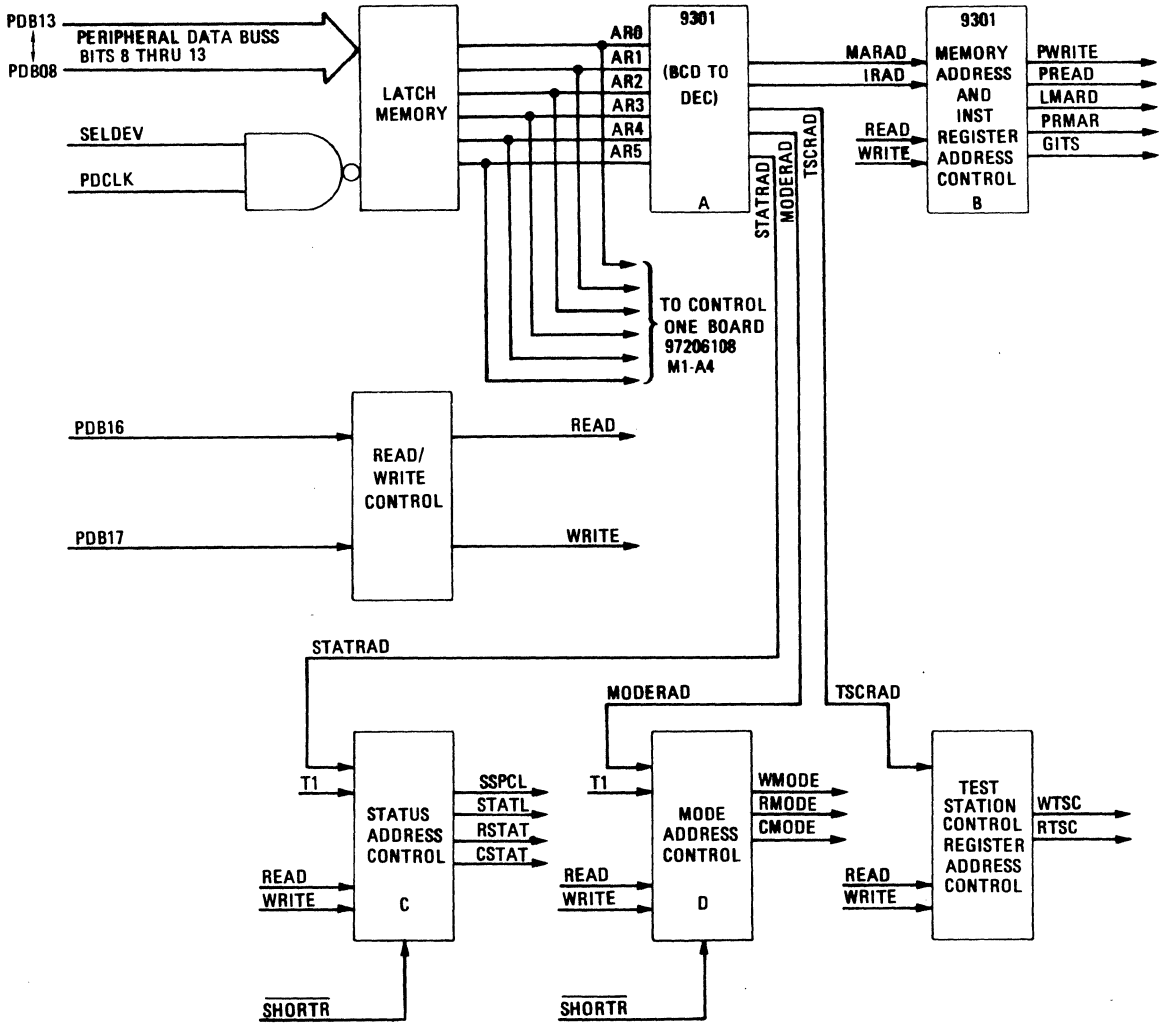


FIGURE 2-3. REGISTER ADDRESS SIMPLIFIED BLOCK DIAGRAM

7. Clear Mode Register (CMODE/)

8. Write Mode Register (WMODE)

9. Read Mode Register (RMODE)

10. Write Test Station Control Register (WTSC)

11. Read TSC (RTSC)

Two bits from SPU word positions 16 and 17, called NXFR (accumulator data transfer) and PTN (P to N bus transfer), are stored on the CPI 3 board. The table below gives their function in relation to short register operations.

NXFR	PTN	
0	0	No-op
0	1	Special (no data transfer)
1	0	Write
1	1	Read

Other address decoding is done on the XDL board (time delay, clock burst, instruction number display, and instruction number compare registers) and control 1 board (DPS1, DPS2, DPS3, DPT1, DPT2, DPT3, E0, E1, EA0, EA1, EB0, EB1, EC0 and EC1 registers). Twenty-five of the possible 64 addresses are utilized (including two no-op addresses of all 1's and all 0's).

The command interrupt flip-flop is located on this board and is discussed in the status register description.

The control signals for the instruction register are implemented here. The I register forms a buffer between the memory and test station. When executing a long register instruction with an SPU command, the I register is addressed and IW/ goes low. This generates CPI (clock pulse I), and gates S to I. At the end of time T1, flip-flop F4 pin 10 is set and the execute I command (EIC), goes high. At the end of T2, EIC is reset and EIC2 is set. EIC2 remains high until the end of time T4. If the I register is loaded with a 'read long register' instruction, then I23=1 and I22=0. Then CPI is generated to load the I register with the returning data from the test station (GLTI).

In the direct memory access mode, when memory access is granted (MACG), GSTI and CPI are generated at time T1 to load the I register from memory. Transmittal of data from the I register to the long register bus (GITL), is executed by the phase loop logic.

Set interrupt in process (SINP), loads bit 14 of the status register. This bit is located on the CPI 3 board.

2.3.4 Status Register A (97340804)

The status register board records the status of the six tester interrupts. It also contains the logic for gating the address of the appropriate interrupt subroutine. Some of the interrupt control logic that is on the register address board and the CPI boards is also covered in this discussion.

The six tester interrupts are stop, instruction number compare, trap, delay complete, functional fail, and dc trip. Each interrupt can be enabled or disabled under program control by turning on the appropriate enable bit in the status register. An example of an interrupt process follows. Let bit 0 (compare enable) of the status register be on. When the contents of the instruction number display (IND) counter equal that of the instruction number compare (INC) register, then CMPS from the T counter board sets bit 1 of the status register (CMP) at the appropriate time of the phase loop count. With CMP and CMPEN now both on CMPA is generated if the signals SODA/ (E5-pin 11) and DOTOFA/ (E4-pin 8) are high. The compare interrupt has lowest priority and the signals SODA and DOTOFA inhibit the compare (CMPA) interrupt if any higher-priority interrupts are on. CMPA turns on the interrupt request (IREQ) signal, via gate C6-pin 8. CMP and CMPEN also generate functional test interrupt (FTINT) by gates C3-pin 11 and E4-pin 6. FTINT resets the phase loop counter to phase 0 and clears DMA.

On the register address board, IREQ and phase 0 set the command interrupt (COMINT) flip-flop at the end of phase time T2. On the CPI 3 board, assume that the interrupt arm instruction, PON, has set INA. When COMINT goes high, the CPI 3 board logic determines if the tester has highest interrupt priority. If highest priority is acknowledged, the PIA flip-flop is set. This sets the interrupt-in-process (INP) flip-flop (bit 14) of the status register. This flip-flop is located on the CPI 3 board. With INP on, the interrupt address is gated to the P data bus by GTINAD. Thus, the interrupt address for the compare interrupt, octal 20, is gated to the P data bus, and the CPI 3 board logic transfers this data to the accumulator bus during phase time T5.

The PIA signal resets the COMINT flip-flop on the register address board at the beginning of T5. While interrupt-in-process (INP) is on, IREQ also stays on. The interrupt subroutine must reset the status register. This may be accomplished by a status special command which generates clear status register (CSTAT) on the register address board. After

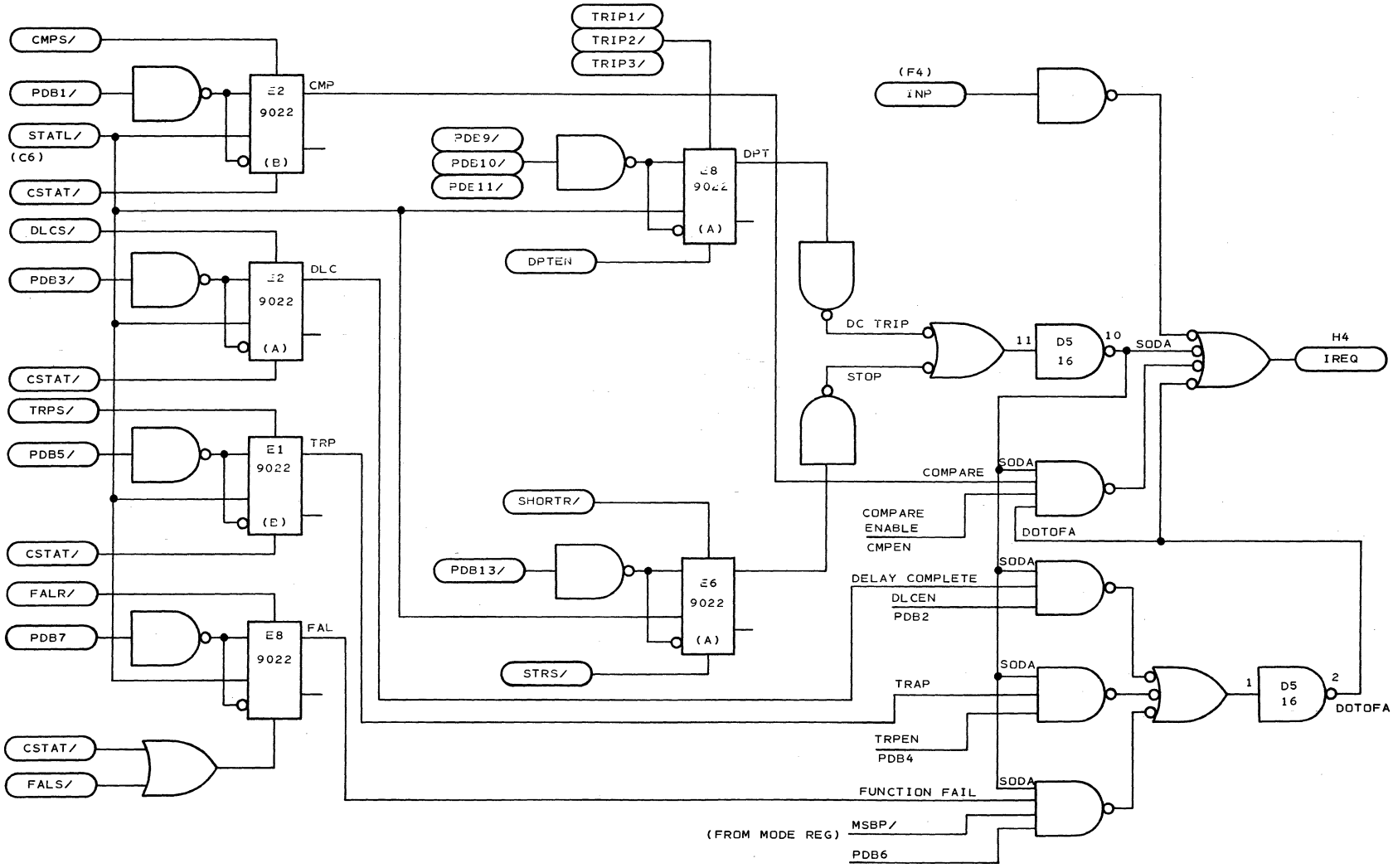


FIGURE 2-4. STATUS REGISTER SIMPLIFIED

clearing the status register, the software may then re-enable the appropriate interrupts (however, the stop enable bit is not cleared by CSTAT).

Now consider bits 2 and 3, the delay complete enable (DLCEN) and the delay complete (DLC) interrupt, respectively. The DLC interrupt can be set only if the tester is not in DMA mode. If DLCEN is set, then at the end of a time delay, DLCS can set DLC. Then DLCA is set if SODA/ = 1. (SODA = stop or dc trip interrupt.) This means that DLC has a lower priority than the stop or the dc trip interrupts because SODA inhibits DLCA. DLCA also generates DOTOFA which turns on IREQ and inhibits the compare (CMPA) interrupt. Thus, DLCA has a higher priority than CMPA. IREQ again starts the interrupt sequence and eventually GTINAD gates the DLCA address to the P data bus. This address is octal 13.

Bits 4 and 5 of the status register are the trap enable (TRPEN) and the trap bits, respectively. When both of these are set, TRPA is generated. TRPA also sets DOTOFA and IREQ. TRPA is inhibited by SODA just as DLCA was. The trap interrupt address is octal 14.

BITS 6 and 7 are the functional fail enable (FALA) and the functional test interrup (FTINT), respectively. While FTINT stops the phase loop counter and resets DMA, FALA generates DOTOFA and IREQ. The fail interrupt address is octal 15. Also, the FTINT inhibits the CMPA interrupt. On the other hand, SODA inhibits FTINT. Note that the trap, the functional fail and the delay complete interrupts all have the same level of priority. However, since it is not possible for more than one of them to occur at the same time, no confusion in interrupt address can result.

The dc trip interrupt enable (DPTEN) is bit 8. There are three digitally programmable power supplies, each with a programmable current/voltage trip point monitor, called TRIP1, TRIP2, and TRIP3. If DPTEN = 0, the three trip bits (9, 10, and 11) cannot be set. When DPTEN = 1, when a trip occurs, the appropriate bit will be set when either DMA is off or during phase 5 or X7. If monitor and strobe are on, the trips are inhibited. If one of the trips occurs, then DPT and DPTEN are set and enable DPTA and FTINT. The dc trip and the stop interrupts have the highest priority, so SODA inhibits all other interrupts. The trip interrupt address is octal 16.

The stop interrupt (STPA) bit is bit 13, and stop enable is bit 12. Once the stop enable bit is written on, status special cannot clear this bit. It must be written to 0, or CPU reset will clear it. A short register reset will automatically set the

stop bit. With stop and stop enable on, STPA occurs, which turns on IREQ and also inhibits all other interrupts. Start (STR), bit 14, is the complement of the stop bit. STR must be on to enable the phase loop counter. The stop bit will automatically be cleared when the TSC register on the multiplex control board is written. Thus a normal test sequence may begin by writing into the TSC register with the test station address. At the end of the test program, a short register reset, under program control, is generated by the mode register board, which sets the stop interrupt, and transfers control to the stop interrupt subroutine. Bit 15 of the status register is a spare bit.

All 16 bits of the status register may be read or written. The-signal RSTAT gates the contents of the register to the P data bus and WSTAT enables the register inputs to accept data from the P data bus. RSTAT, WSTAT and CSTAT are generated on the register address board.

2.3.5 Mode Register (97206005)

This 16-bit register contains several miscellaneous control functions. The following discussion details the operation of each bit. The mode register address is decoded on the register address board, where write mode (WMODE), read mode (RMODE), and clear mode (CMODE) are generated.

The Mode Register generates the following signals--long register reset (LRESET), short register reset (SRESET), negative logic mode (NEG L), latch C register (LTC), strobe C register (STROBE), sync pulse (SYNC), direct memory access (DMA), and functional test suspended (FTS).

Bit 0 ANDed with WMODE generates the short register reset (SRESET) under software control. This allows all of the short registers (registers driven from the P, or short register, data bus) to be cleared under program control. The only exception is the test station control (TSC) register, on the multiplex control board, and the stop enable bit of the status register.

Bit 1 ANDed with WMODE generates the long register reset (LRESET). This allows the long registers of the test station to be cleared under program control. Bits 0 and 1 are write only bits.

Bits 2 and 3 can be read only. Bit 2, with RMODE on, indicates whether the monitor switch on the monitor control panel is on or off. This bit will be a 1 when the monitor switch is on. Bit 3, with RMODE on, indicates whether the tester is in automatic or

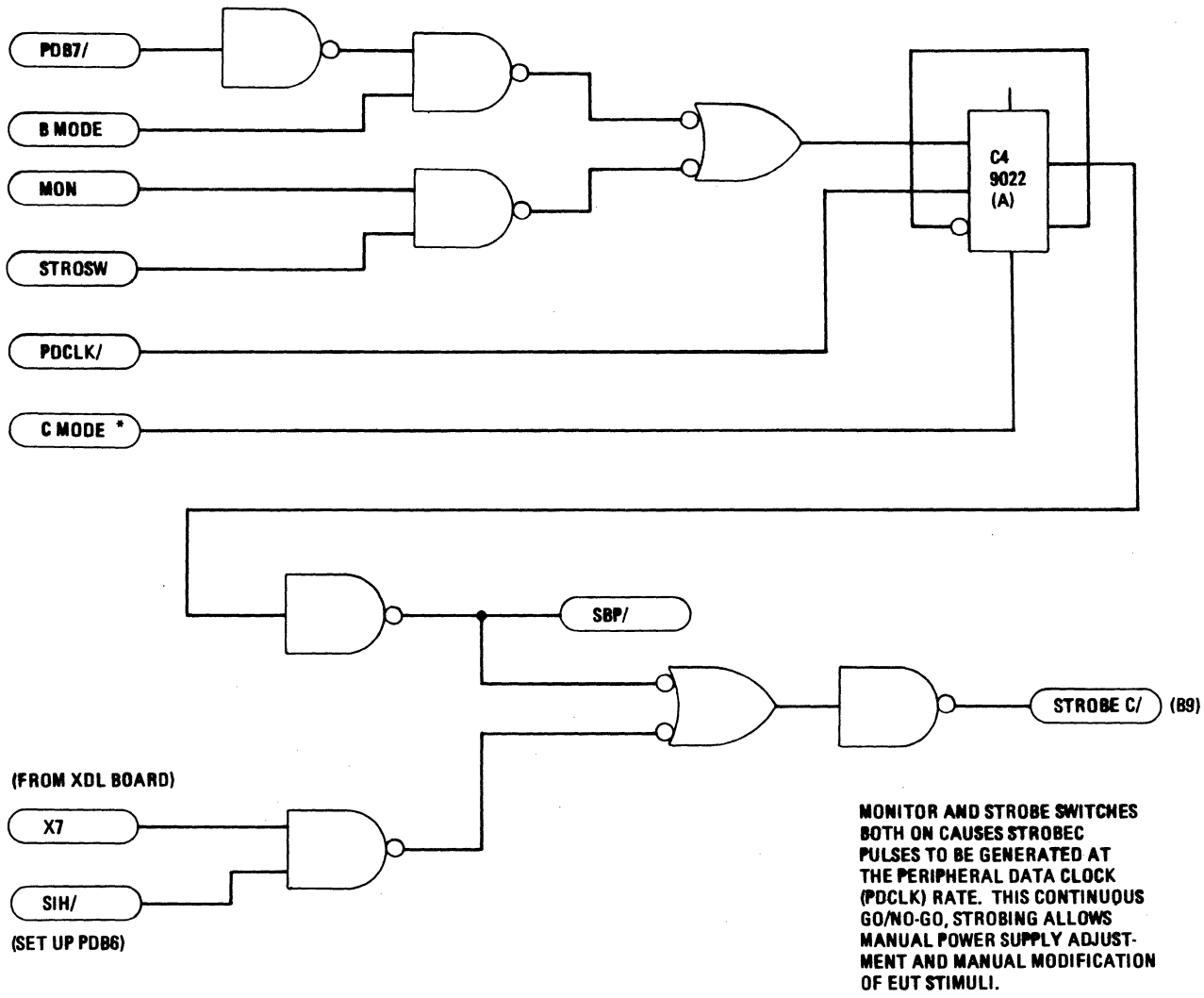


FIGURE 2-5. MODE REGISTER SIMPLIFIED

manual mode. This bit will be a 1 when the test station is in automatic mode.

Bit 4 can be read or written. This bit stores the negative-logic-mode (NEGL) command. With this bit on, NEGL will alter the pass/fail logic decisions at the test station. With NEGL = 0, positive logic decisions are made.

Bit 5 can be read or written. It stores the latch-C-register (LTC) command. With LTC = 0, the C register is cleared before the functional comparators are strobed. In this mode, the C register contains the failures of the last test executed. With LTC = 1, the C register is not cleared prior to strobing (see the XDL schematic). Hence, the C register accumulates failures on pins during the entire test sequence, or that portion of testing during which LTC = 1. Any pin that failed one or more times during a test pattern is so indicated on the C register display.

Bit 6 also can be read or written. This bit causes the strobe of the comparators to be inhibited. When SIH = 1 the strobe C pulse will not be generated at the end of the execute delay loop.

Bit 7 can be writton only. With bit 7 and WMODE on, a strobe C pulse is generated by flip-flop C4-pin 6. The pulse width is equal to the period between the system clock pulses. The strobe pulse strobes the functional comparators even if strobe inhibit (SIH) is on.

Bit 8 of the mode register can be written only. This bit generates a synchronization pulse. Writing this bit sets flip-flop D3-pin 10 and starts the time delay counter (TDCRB). When the time delay is completed (TDCC = 1), the flip-flop is reset. Therefore, the width of the sync pulse (SNP) is equal to the value in the time delay register. Also, at the completion of the time delay, the gate-all-sync-pulses (GASP) signal is generated on the XDL board. delay register. This signal enables clock lines 1 through 4.

Bit 9 can be written only. When this bit is set, the tester begins testing in the direct memory access mode. The tester is then under control of the phase loop and XDL counters. Return to CPU control is accomplished by resetting this DMA bit. Three reset lines are used. PHS2B resets DMA when a functional test interrupt occurs. DMARA resets DMA when an interrupt occurs after phase 5. DMARB resets DMA when a trap instruction occurs.

Bit 10 is a spare and can be read or written.

Bit 11 can be read or written. It is set when a functional test failure occurs if a new functional test has already been loaded

into the master side of the F register. This is possible when the programmed time delay is longer than two memory cycles. Since the phase loop controller has a built-in overlap of test execution and memory fetch, the next instruction may already by loaded before strobing the comparators for the previous instruction. This functional test suspended bit is automatically cleared when the DMA mode is resumed after processing the functional fail routine.

Bits 12, 13, and 14 can be read or written, but are not mutually exclusive.

Bit 14 is the pass bit. It is automatically set by gate A8-pin 6 when the C register is strobed if the functional test passes and bits 12 and 13 are not on. If a functional test fails then FALS/ goes on and sets bit 13, the functional fail bit. Also, the pass bit is cleared by FALS/. If a dc trip occurs and the trip interrupt is enabled, DPTA goes high and sets bit 12, the dc fail bit, while resetting the pass bit. Once a functional failure occurs in automatic mode, bit 13 remains on and bit 14 remains off. However, in manual mode a strobe pulse, bit 7, clears the fail bit and sets the pass bit if the current test passes. That is, in manual mode, the pass and fail bits reflect the outcome of the current test. A start command (STRS) at the beginning of a test also sets the pass bit and clears both fail bits.

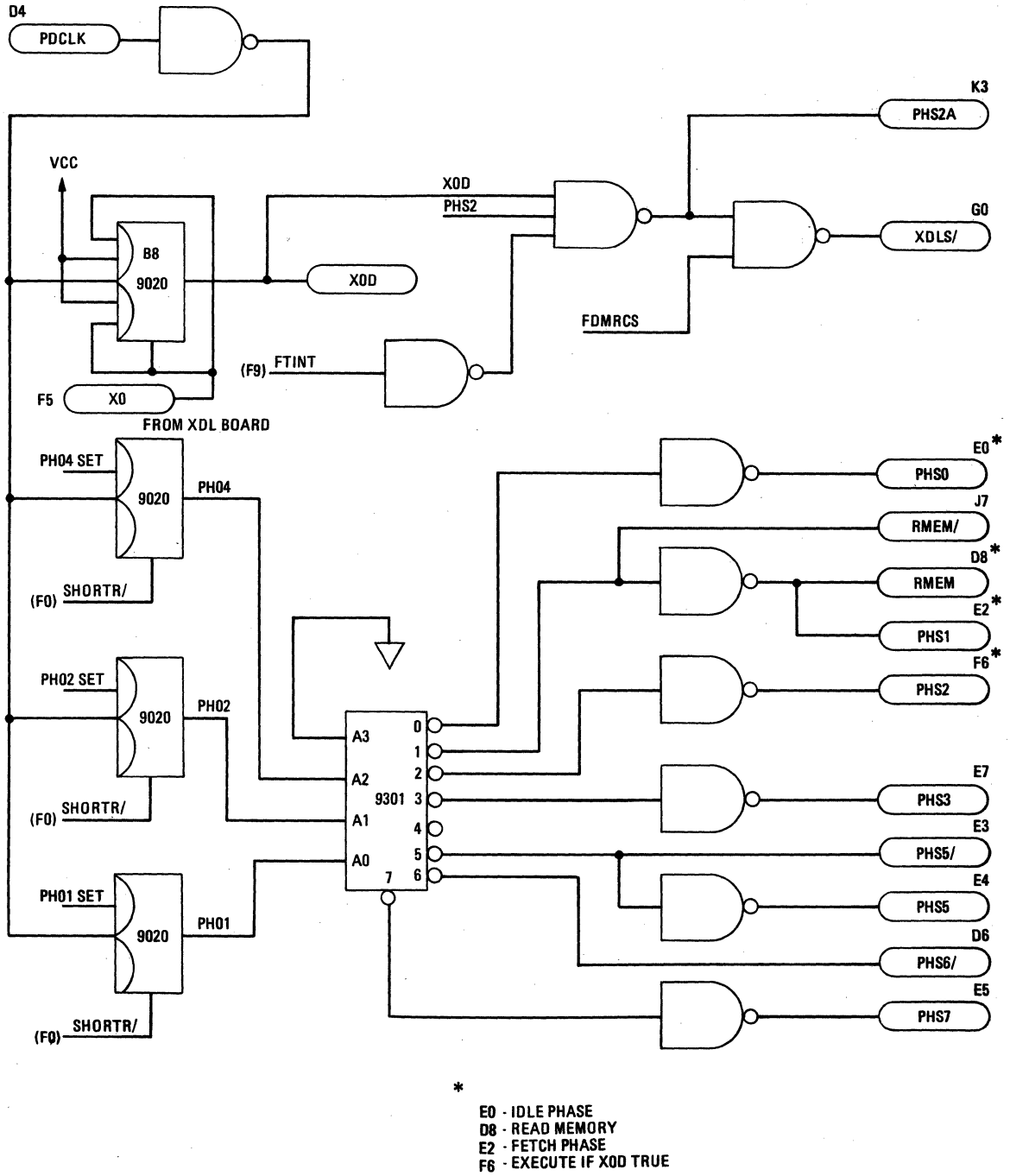
Bit 15 is a spare bit and can be read or written.

2.3.6 Phase Loop Counter (97206006)

The Phase Loop Counter has the functions of controlling the transfer of information from the Instruction Register to the long registers, and, with the CPI, controlling the DMA transfer from memory to the Instruction Register.

Figure 2-6 is a simplified diagram of the Phase Loop Counter A board. The three flip-flops, PH01, PH02, and PH04, comprise a counter having 8 states, which are decoded to generate PHS0 through PHS7 (PHS4 is not used). The counter has several possible sequences, depending on the long register address, the command held in bits I23 and I22 of the Instruction Register, the FTS and DMA bits of the Mode Register, the STR, FTINT, and IREQ signals generated by the Status Register, and the DLY and XO signals generated in the XDL Counter.

The Boolean equations for the phase state outputs PHS0 through PHS7 are as follows:



*
E0 - IDLE PHASE
D8 - READ MEMORY
E2 - FETCH PHASE
F6 - EXECUTE IF XOD TRUE

FIGURE 2-6. PHASE LOOP COUNTER SIMPLIFIED

```
PHS0 = PHS2 FTINT XOD
PHS0 = PHS7 (DMARA+DMARB)XOD
PHS1 = PHS0 STR DMA IREQ/ FTS/
PHS1 = PHS3 WRHOL F
PHS1 = PHS2 FTINT/ XOD
PHS1 = PHS5 FTINT/ DLY/
PHS1 = PHS2 STR DMA IREQ/ FTS/
PHS2 = PHS3 WRHOL (D+R+M+C+S)
PHS2 = PHS0 STR DMA IREQ/ FTS
PHS2 = PHS3 WREX F
PHS2 = TRPS = PHS3 TRAP FTS
PHS3 = PHS1 MACG T1
PHS5 = PHS6
PHS6 = PHS2 WREX (D+R+M+C+S)
PHS7 = PHS2 FTINT/ XOD DMARB
PHS7 = PHS5 FTINT DLY/ XOD
```

In all, there are 5 conditions of interest, leading to 4 count sequences. The phase count transitions are discussed in detail under "DMA Sequence", in the detailed theory of operation (Section 3).

2.3.7 XDL Counter A (97340806)

The execute delay loop (XDL) counter provides the following capabilities:

1. Execute delay loop

2. Hardware automatic time-delay generator

3. Miscellaneous logic functions to augment the T counter logic.

Refer to sections B1 and C1 of the XDL schematic. Assume that the counter flip-flops D4 and D5 are in the 000 state so the decoder E5 output 0 is low (state X0). Upon receipt of XDLS the start XDL flip-flop D4-pin 6 is set and the XDL counter advances to X1. X1 generates three functions: 1) gate master to slave (GMTS) (see phaseloop counter schematic), 2) increment IND counter (gate F7-pin 1), and 3) time delay counter (gate D3-pin 1) and clock burst counter parallel entry (T counter gate C3-pin 9), along with their respective clock pulses to load the counters with new data. The XDL counter then advances to X3 by setting flip-flop D5-pin 10. The counter remains in X3 until TDCC goes high. Then the counter goes to X7 if CBCC/ is low or to X2 if CBCC/ is high. While in X3, TDCCPS is generated (gate D3-pin 10) to increment the time delay counter every 0.35 microseconds (system clock rate). If CBCC/ is low, the C register will be

reset (CRRA/) unless latch C is on (LTC/ low) in the mode register. Assume that the clock burst count is not complete and the counter advances to X2 by clearing flip-flop D4-pin 6. Since CBCC/ is high, one sync pulse will be enabled by gate F4-pin 11. The clock burst counter will be incremented (gate C4-pin 13). Again the time delay counter will be reset with the inverted data in the time delay register (gate D3-pin 1). The XDL counter advances to state X6 by setting flip-flop D5-pin 6. Here it again waits for the time delay count complete (TDCC) signal. The time delay counter is incremented by gate D3-pin 12 while TDCC/ is high. If the clock burst count is not complete, gate C4-pin 8 clears flip-flop D5-pin 6 and the XDL counter returns to state X2. If CBCC is high, gate B5-pin 8 will clear the C register if latch C is not on. Then gate C5-pin 8 will set flip-flop D4-pin 6 and the XDL counter will advance to state X7.

At X7 strobe C is generated on the mode register board (unless strobe inhibit is on). Strobe C in turn enables FALS which is high if any pin failed. FALS sets the FAL bit of the status register. Also, X7 enables the dc trip set line on the status register board to record any of the three dc trips. The same is also true for the compare set signal. It is acknowledged during X7 if the instruction number equals the number in the INC register. Immediately following state X7 the XDL counter returns to the starting point (X0) where it awaits an XDLS signal. An XDLS may also be set because the phase loop can fetch the next instruction from memory faster than the XDL loop processes the preceding instruction, if either the time delay or clock burst counters have a value greater than five.

Refer to sections A3, B3, and C3 of the XDL schematic. The delay counter uses five type 9316 four-bit binary counters. One of the four delay start signals (0.5DLS/, 1DLS/, 3DLS/, or 5DLS/) resets the first three 9316 counters to zero, sets one of the four corresponding R/S latches, and sets flip-flop D4-pin 10, which sets tester busy (TBSY). When the binary count reaches an appropriate value, the R/S latch is reset. If no other latches are set, the flip-flop D4-pin 10 is cleared, thus removing TBSY. TBSY is gated through the CPI 2 board to status bit eight. It is up to the software to perform a status test to check TBSY if an instruction is time-delay-dependent. The signal DLY/, which is functionally the same as TBSY/ for the delays generated by the hardware mentioned above, goes to the phase loop counter and forces a wait-for-delay whenever the D or the R register is exercised. At the conclusion of the delay, a DLCS pulse is generated, which sets a delay complete bit in the status register. With a T1 repetition period of 1.75 microseconds, the delays are: 0.5DLS-280 uS, 1DLS-560 uS, 3DLS-1.792 mS, and 5DLS-2.688 mS.

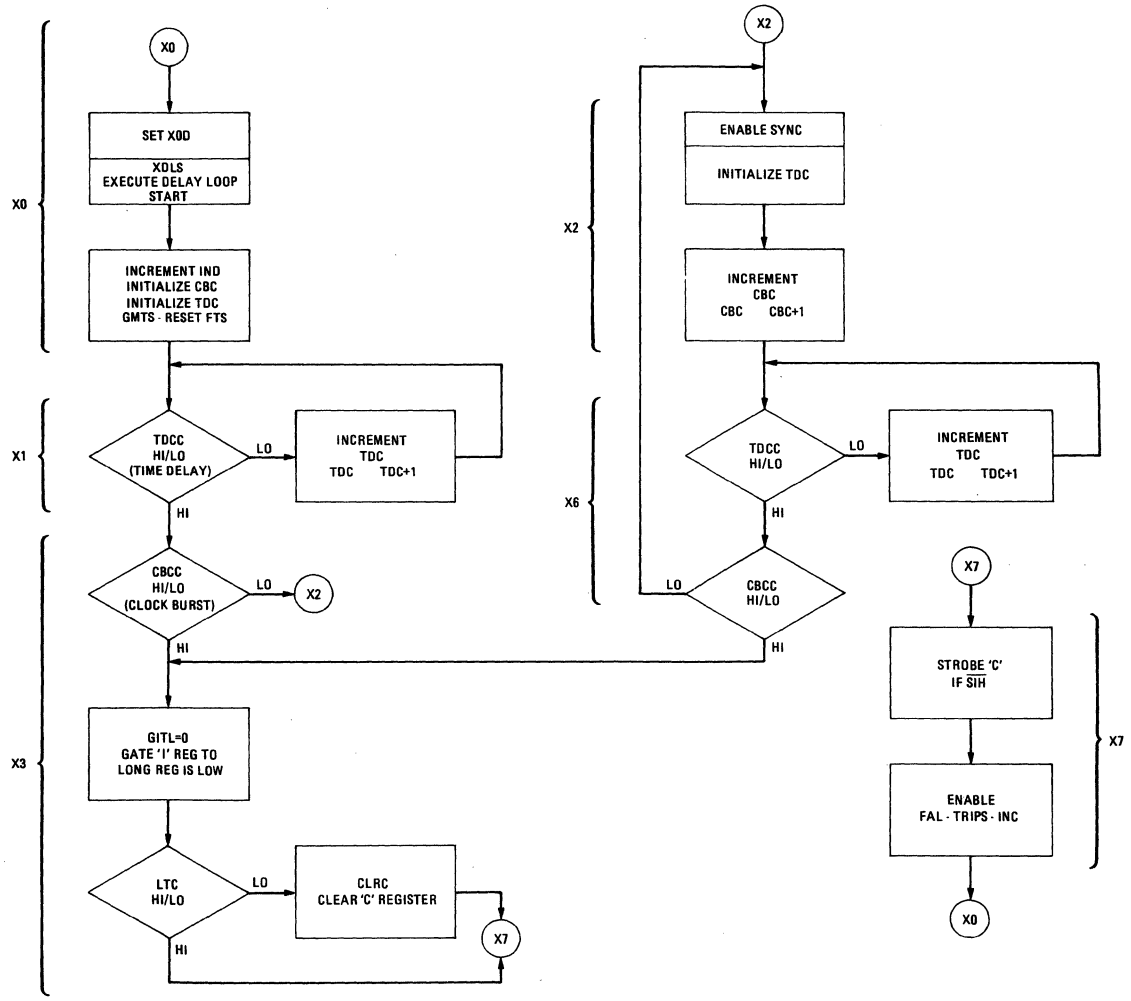


FIGURE 2-7. XDL COUNTER FLOWCHART

The last two type 9316 counters continue frequency division of T1 down to the order of 3 Hz, for use by the manual mode advance feature. When the advance button at the test station control panel is pressed, advance counter reset (AVCR) is generated on the multiplex control board and resets the last two 9316 counters. When the state of the counters reaches the point where all three inputs to gate A5-pin 6 are high (as determined by jumpers S1 and S5), advance start (ASTRS) is generated. The repetition rate of ASTRS will be from one to five starts per second, depending on the jumper wiring shown on the XDL schematic.

An extended time delay is generated by the counter in section C2 of the XDL schematic. This counter divides the frequency of pulses going to the time delay counter on the T counter board by 1000. The extended, or dc, time delay count is initiated by a time delay special instruction (gate D7-pin 6). This sets flip-flop C7-pin 10 and releases the reset line to the counter (B7, B8 and C7-pin 6). The counter divides the frequency of T1 (T1 is one fifth the system clock frequency) by two and then by ten twice using the two 9310 decade counters. The output/frequency of TDCI is 1/200 of T1, or 1/1000 of PDCLK.

The six short register address bits (AR0-AR5) are decoded by F8, the type 9301 decoder. It generates the addresses for the time delay register (TDRA), clock burst register (CBRA), instruction number compare register (INCA), instruction number display counter (INDA), and four unused addresses A12, A13, A16, and A17.

The remaining logic on the board is for the clocks to the counters, and the Boolean equations for the clocks are as follows:

```
TDRCPE = TDRCB + TDRA.SSPCL + SNP.TDCC + X1 + X2

TDCCPS = CLK.(TDRCPE + (TDCI + X3 + X6 + SNP).TDCC/)

CBCCPS = CLK.(X1 + TDCC.X2.CBCC/)

CBRCPS = T1.PWRITE.CLK.CBRA

TDRCPS = T1.PWRITE.CLK.TDRA

INCRCPS = T1.PWRITE.CLK.INCA

INDCCPS = CLK.(INDCPE + INDI + X1 + PHS6)

INDCPE = T1.PWIRTE.INDA

INDI   = T1.SSPCL.INDA
```

RPDBA = TDRA + INCA + CBRA

GASP = SNP.TDCC

2.3.8 T Count A (97206007)

The T counter provides the following:

1. A 14-bit counter and storage register for the programmable tester time delay.

2. An eight-bit counter and register for the programmable tester clock burst.

3. A 16-bit counter for the instruction number display.

4. A 16-bit comparator for comparing the IND (instruction number display) count with the contents of the INC register.

5. Logic for reading the IND, the TDR, and the CBR registers.

2.3.8.1 Time Delay Counter

A 14-bit register contains the value of the time delay desired.- This register is loaded from the inverted contents of the P data bus upon receipt of TDRCPS/ from the XDL board. A time delay is initiated when the signal TDRCEPE/ from the XDL board causes the inverted contents of the time delay register to be loaded into the time delay counter. Time delay counter clock pulses from the board increment the contents of the binary time delay counter. When all 14 bits are logical 1's, the signal time delay count complete (TDCC) goes high signifying the completion of the desired time delay. For example, let the TDR be loaded with some number 'N/'. At the beginning of the time delay, the TDC is loaded with 'N/', the complement of N. Now, TDCC goes high when the contents of the TDC are all ones. Therefore, it takes (37777B-N/ N) TDCCPS/ pulses. The frequency of TDCCPS/ determines the ratio of the time delay to N. The XDL circuitry determines this frequency, which is either 2.86 MHz for functional test time delays or 2.86 kHz for parameter test time delays. Hence, the maximum time delay can be 5.73405 milliseconds or 5.73405 microseconds. The resolution of the time delay would be 0.35 microseconds.

2.3.8.2 Clock Burst Counter

The clock burst counter (CBC) functions exactly the same as the time delay counter but is only eight bits in length. CBRCPS/ is

generated on the XDL board and loads the clock burst register with inverted data from the P data bus. During period X1 in the execute delay loop (XDL) the clock burst counter is loaded with inverted data from the register. CBCC (clock burst count complete) will go low and remain low until the CBC has all ones.

2.3.8.3 Instruction Number Display Counter

The instruction number display (IND) counter is a 16-bit binary counter. The counter may be preset when INDCPE/ is low. The count will be incremented as each functional test or parametric test is executed in the direct memory access (DMA) mode by the pulse INDCCPS/. Other test instructions not in DMA mode will utilize an IND Special command for this purpose. At the end of the test program, the instruction number is written into the statement number display (SND) register at the test station console.

2.3.8.4 Instruction Number Counter

In order to interrupt testing at some predetermined point in the test program, a 16-bit instruction number comparator is used. The first 12 bits of the INC register are on the type 1 quad 16 bit register board and the remaining four bits are on the T counter board. When the contents of the INC register equal the contents of the IND counter, the signal compare set (CMPS) goes high. This signal sets the compare flip-flop on the status register.

2.3.8.5 Readout Logic

Outputs of the IND counter, the TD register and the CB register are ANDed with their respective addresses and then ORed together to form the signals RPDB0 to RPDB11, which go to the type 1 quad 16 bit register board for readout.

2.3.9 Quad 16 Bit Register

The quad 16 bit register board is a universal register board. That is, it can have as many as four 16-bit-word registers, but also be tailored to have fewer registers and fewer bits per word. Each different configuration has a unique part number, but still carries the basic name, "quad 16 bit register board". There are three types of this board used in the test set:

TYPE	NO. OF REGISTERS	BITS PER REGISTER	SCHEMATIC
1	1	12	97206008-04
2	4	12	97206009-04
3	4	16	97206010-04

Type 1 (97206008)

In the tester interface unit (A2) a type 1 board is used as the INC (instruction number compare) register. It is also used to read the signals RPDB0 through RPDB11 onto the P data bus.

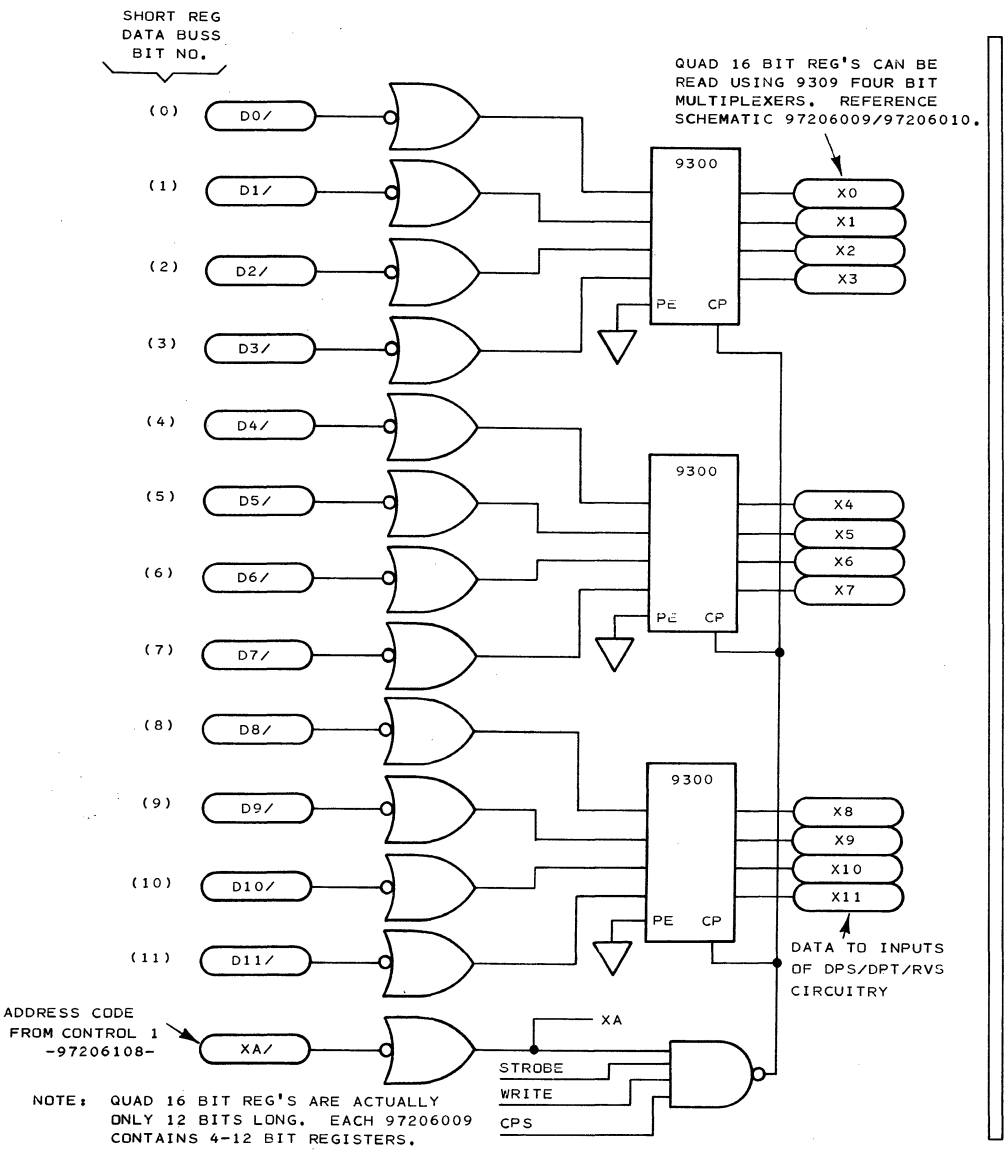
Except for the quantity of registers and the word length, each register functions in the same manner. Each board contains the logic necessary to perform write, store, and read operations on each register. Separate read/write address and reset lines are provided for each register. Each bit of each register is accessible in the true state at the printed circuit board I/O connector. Each register can be read over the wired-OR network which is driven by type DTuL 994 gates. Because of the wired-OR read/write circuit, the data is written and read with complementary logic. For example, to load (write into) register X, data is present on the I/O data bus. The X address (XA/) goes low, the write command (WRITE/) goes low, and the clock line (CP/) makes a high-low-high transistion. A zero (low) on the data bus loads a 1 (high) into the corresponding bit of the register. The registers consist of MSI-TTuL 9300 four-bit registers operated in the parallel entry mode. The register outputs have a CCSL drive factor of 10/100. The contents of a selected register may be read onto the data bus by enabling the register address to go low along with READ/. The register contents are then gated through the 9309 dual four-bit multiplexer to the type 944 output gates.

Type 2 (97206009

In the MUX reference subassembly, four type 2 quad 16 bit register boards are used to store the data for the RVS and DPS supplies. Each board stores four 12-bit words. The first 10 bits (0 through 9) are data, the eleventh bit is the sign, and the twelfth bit is the range for each individual supply.

Type 3 (97206010)

The type 3 quad 16 bit register board contains the logic necessary for writing, storing, and reading three individual 16-



INPUT SIGNAL	DESCRIPTION
CPS	CLOCK PULSES GENERATED BY THE COMPUTER - (EVERY 350NS)
D0/	SHORT REG. DATA BUSS (BIT 0)
D1/	SHORT (BIT 1)
D2/	SHORT (BIT 2)
D3/	SHORT (BIT 3)
D4/	SHORT (BIT 4)
D5/	SHORT (BIT 5)
D6/	SHORT (BIT 6)
D7/	SHORT (BIT 7)
D8/	SHORT (BIT 8)
D9/	SHORT (BIT 9)
D10/	SHORT (BIT 10)
D11/	SHORT (BIT 11)
XA/	DECODED REG ADDRESS CODE BITS 8-13 OF SPU COMMAND.
STROBE	SIGNAL NAME ACTUALLY 'CPT1WS'. (CLOCK PULSE - T1-WRITE SHORT REG)
WRITE/	SWRITE/ FROM DATA BUFFER TO ALLOW WRITING TO SHORT REG. DATA BUSS.

FIGURE 2-8. QUAD 16-BIT REGISTER

bit data words and for reading only, one 16-bit data word. The full 16-bit capability is not used, however, on any of the four registers. In test station module R0, the type 3 quad 16 bit register board has the following register assignments.

REGISTER NAME	MNE-MONIC	LENGTH (NO. OF BITS)	TYPE
Statement Number Display	SND	15	Read/Write
Clock, Sync, and Strobe	CSR	8	Read/Write
Socket Identification	SID	12	Read Only
External Interface A	EIRA	15	Read/Write

Statement Number Display Register

This 15-bit register is a holding register for the nixie display on the test head control panel. The octal code for executable software commands is stored in this register. For example, when the program has the command 'PAUSE ON FAIL', the SND register contains the statement number of the step in which the failure occurred. This in turn is displayed by the nixie tubes so that the operator can begin to analyze the failure.

Clock, Sync, and Strobe Register

This eight-bit register is a holding register for the signals Strobe Enable and Clock Address as shown in Table 2-7.

The strobe enable signals are routed to the 120 bit decoder board where they are ANDed with F register bits. (See schematic 97200101-04). The equation for generating a strobe is: STROBE = CSR4.F0.X7 + CSR5.F1.X7 + CSR6.F2.X7 + CSR7.F3.X7. This shows that a strobe pulse is generated whenever the phase loop counter is in phase 7 and coincidence exists between F pattern and strobe enable bits.

The clock address bits go to both the 120 bit and the 15 bit decoder boards. On the 120 bit decoder board, the clock address bits are ANDed with F register bits, sync enable, and the system clock. When coincidence exists between these signals, a sync pulse is generated.

TABLE 2-7. CLOCK, SYNC, AND STROBE REGISTER, WORD FORMAT

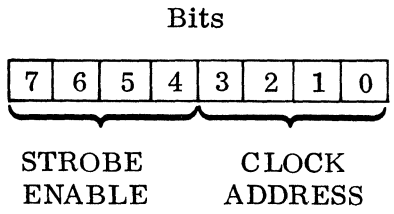
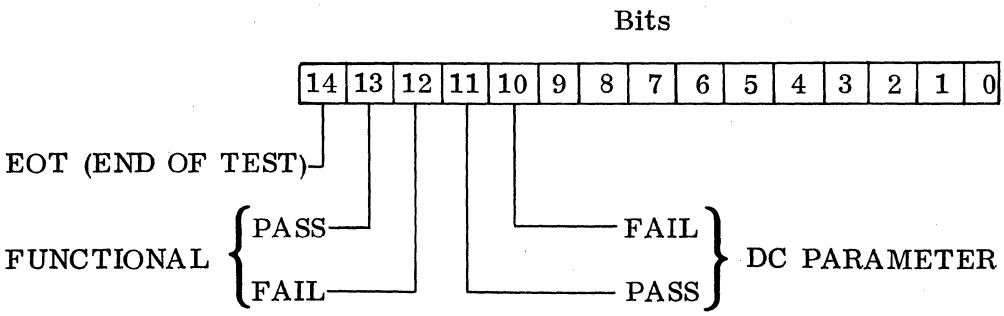


TABLE 2-8. EIR WORD FORMAT



On the 15 bit decoder board, the clock address bits are ANDed with decoded pin address bits to generate the clock relay (CRLY) signals (see schematic 97341603).

Socket Identification Register

The input to this read-only register is a hardwired, 12-bit bus that originates at the RO load baord. Here the operator can hardwire a 12-bit code to identify a particular load board. At the beginning of each program, the SID register is interrogated to determine whether or not the correct load board is inserted for the device under test.

External Interface Register

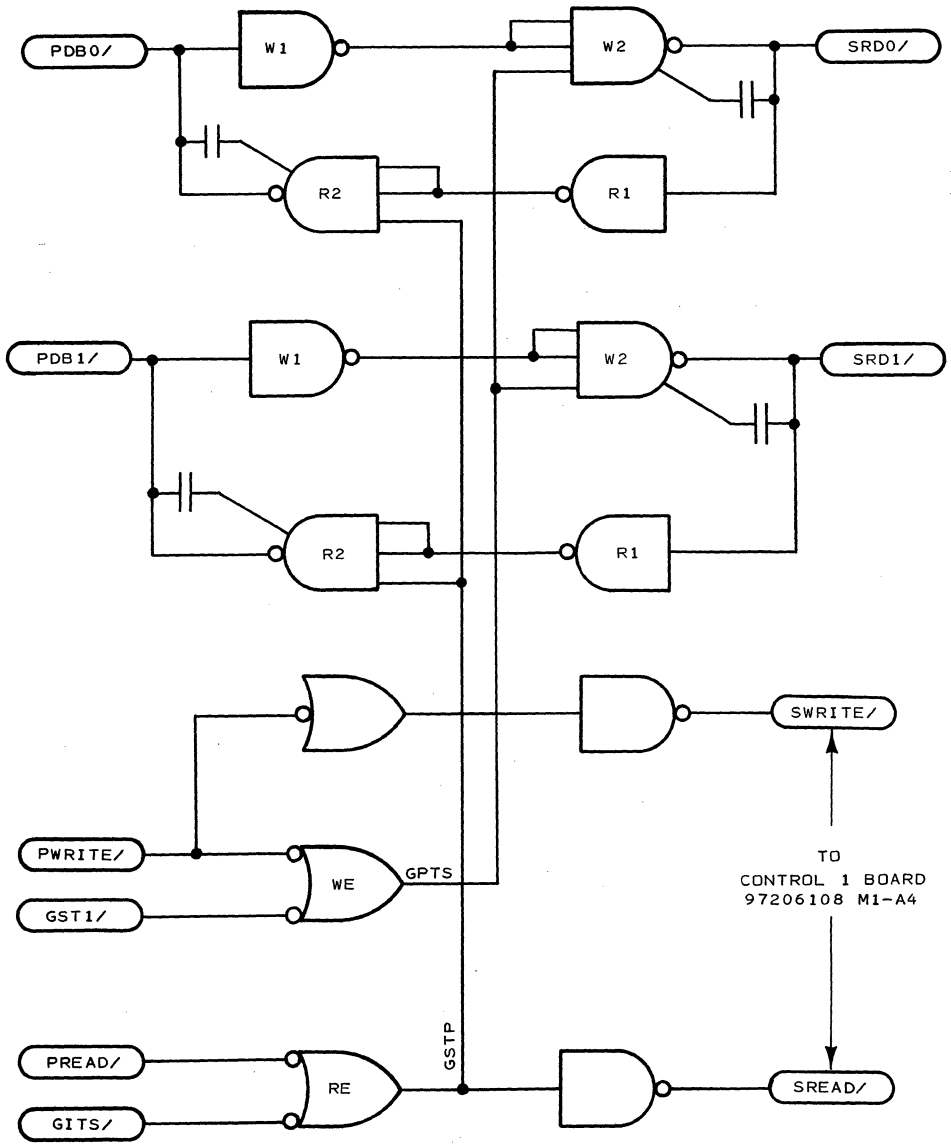
This 15-bit read/write register is assigned the function of communicating to external handling equipment. The bits of this register are applied to plug J4 of the convenience panel. The word format is shown in Table 2-8.

2.3.10 Data Buffer (97206002)

The data buffer contains the logic that transmits and receives data between the 24-bit P data bus and the short register data bus. These two buses are logically equivalent. Because the CPI boards have limited bus drive capability, the data buffer is used to amplify the capacity of the P data bus. Each output is capable of driving 14 wired OR loads (registers).

The status, the mode, the INC and the TD, CBC, and IND registers are driven from the P data bus. The instruction, E0, E1, EA0, EA1, S0, S1, DPS1, DPT1, DPS2, DPT2, DPS3, DPT3, EB0, EB1, EC0, EC1 and the TSC registers are on the short register bus. All of these registers are located on backplane of the reference and multiplex unit. The data buffer also drives the 8-foot cable connecting backplanes A2 and M2.

Signals from the register address board, PWRITE or GATE-S-TO-I,- enable data transmission from the P data bus to the short register bus. SWRITE/ equals PWRITE/ and is compensated for the data buffer time delay. The signals PREAD or GATE-I-TO-S enable data transmission from the short register bus to the P data bus. PREAD/ or GITS/ equals SREAD/. All 24 bits are driven by power gates to both buses. Pull-up resistors are selected to match the various loading requirements of each bit.



INPUT SIGNAL	DESCRIPTION
GITS/	GATE INSTRUCTION REG. TO SHORT REG. (READ ENABLE)
GSTI/	GATE SHORT REG. TO INSTRUCTION REG. (WRITE ENABLE)
PDB0/	PERIPHERAL DATA BUSS BIT ZERO
PDB1/	PERIPHERAL DATA BUSS BIT ONE
PWRITE/	PERIPHERAL WRITE (SPU OR 24 BIT FTW CONTAINING WRITE BITS)
PREAD/	PERIPHERAL READ

FIGURE 2-9. DATA BUFFER SIMPLIFIED

2.3.11 Dual Multiplex Control (97236101)

The dual multiplex control board contains the logic circuitry for station addressing, manual control and reset control. The test station control (TSC) register forms the primary interface to the multiplex control software.

Bits 0 and 1 of the TSC register can be read or written. These two bits form the station address as shown in the table below.

TSC 1	TSC 0	STATION NUMBER
0	0	1
0	1	2
1	0	3
1	1	4

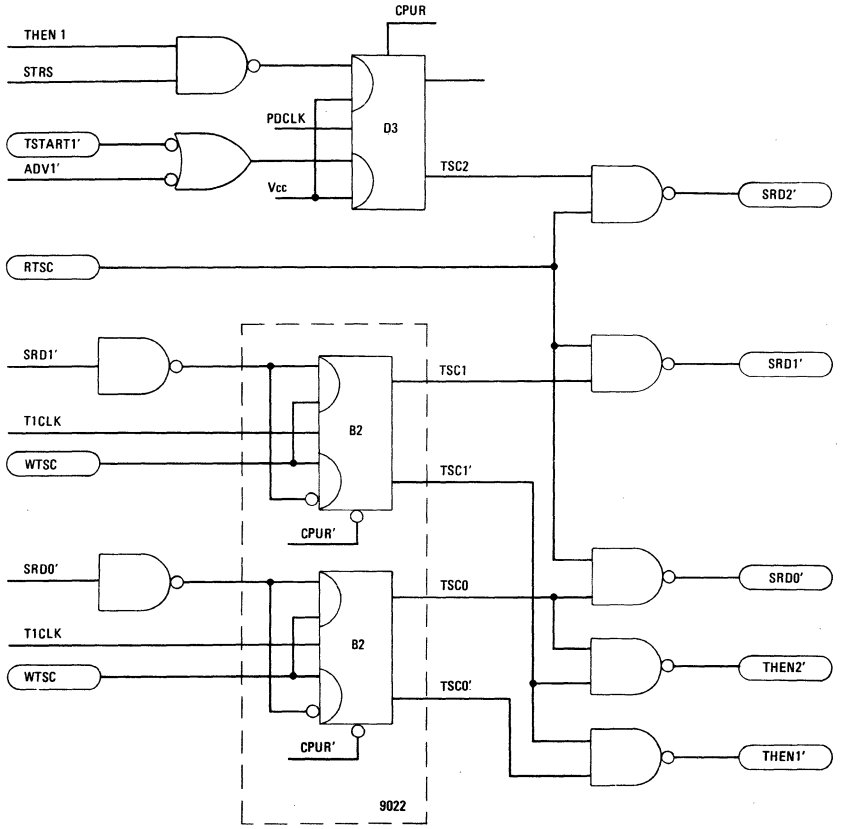
When writing into the TSC register, flip-flop C1 generates a start set (STRS/) pulse which clears the stop bit of the status register. The outputs of bits 0 and 1 are decoded by gate B1-pin 6 to give the station address THEN4 (test head enable 4).

Bits 2 through 5 can be read only. They accept start request commands (TSTART) from the stations and store the request. When the multiplex software reads the TSC register, it processes the start request information, handling stations in the cyclic order 4-3-2-1-4. When a start request is acknowledged, and the TSC register is loaded with the station address, the corresponding start request bit is cleared by STRS and THEN (gate F3 or C3).

Bits 6 through 9 can be read only. They indicate when the station is in manual mode. Also, when the station is in manual mode, the manual signal is high (gate B8-pin 8).

Bits 10 and 13 can be read only. When the reset switch is pressed on the test station, then TRESET sets a corresponding bit in the TSC register, which applies a signal to software controller the next time the TSC register is read. This causes various software control flags to be cleared. Also, if the station is on line when the reset is used, then short register reset (SHORTR/), is generated and clears all mainframe registers. The next time the station is addressed, the reset bit will be cleared. Software reset of the test station long registers is controlled by gates A6 and A7. Also, a CPU reset clears the test station.

A logic comparator, gate A1, generates analog reset (ANLGR) and clears all registers controlling the digital-to-analog converters. This occurs when the test station address is changed. The end result is that when the analog multiplexer



SIGNAL	DESCRIPTION
ADV1'	ADVANCE PUSH BUTTON SIGNAL USED TO ADVANCE TO NEXT STATEMENT WHILE IN MANUAL TEST MODE.
CPUR	COMPUTER RESET
PDCLK	PERIPHERAL DATA CLOCK
TRSC	READ TEST STATION CONTROL REG.
SRD0'	SHORT REGISTER DATA BIT 0
SRD1'	SHORT REGISTER DATA BIT 1
SRD2'	SHORT REGISTER DATA BIT 2
STRS	START SET-USED TO RESET THE TEST START
THEN1'	TEST HEAD ENABLE STATION ONE
THEN2'	TEST HEAD ENABLE STATION TWO
TSC0	TEST STATION CONTROL BIT 0
TSC1	TEST STATION CONTROL BIT 1
T1CLK	CPU T1 AND PDCLK 'ANDED' TOGETHER

FIGURE 2-10. MULTIPLEX CONTROL

relays switch from one station to another, the supplies are all at 0 volts and the relays will be switched without current on their contacts. When rewriting the same station address, a frequent occurrence if only one station is testing or in manual mode, no ANLGR occurs and thus the supplies may be maintained at their programmed values. This capability is not used in a system using one test station.

In manual mode, when the advance button is pressed and the station is on line, the signal AVCR/ goes high. This signal goes to the XDL board where a frequency divider generates a 3-Hz pulse train (ASTRS). The signal ASTRS/ in turn generates a start request pulse (ADV) for the test station via flip-flop D6. Hence when the advance button is pressed, continuous start commands are generated at the rate of three per second. This enables rapid scanning of poritions of a program and yet allows visual observation of the step number display or pass/fail indicators.

2.3.12 Instruction Register (97206102)

The instruction register board is located in the reference and multiplex unit. This logic forms a buffer memory between the FST1 core memory and the test station. Data from the computer is fed to the P data bus and routed to the reference and multiplex unit by the data buffer board by way of the short register data (SRD) bus. Logic on the register address boards provides the control signals for the I register.

Data transmitted from the computer accumulator to the test head while not in the direct memory access (DMA) mode arrives at the I register on the SRD bus and GATE-S-TO-I enables the type 9005 gates. Subsequently CLOCK-PULSE-I loads the 24-bit I register. Then the signal GATE-I-TO-L enables the type 9002 gates, which transmit long register data write commands (WRITE = CPU to test station, READ = test station to CPU). The LRDW signals are routed to the multiplexer line drivers which transmit the long register data to the test station. The nine higher-order bits (I15-I23) are address and control bits for long register operations and are write only.

Data transmission from the test station to the FST1 computer is initiated by first writing into the I register a command which has bit I23 high and bit I22 low. Then, logic on the register address board will generate GATE-L-TO-I and a CPI pulse to load the I registers via the multiplexer line receivers. The CPU then reads the I register, setting GATE-I-TO-S, which enables the type 944 gates. Logic controlling CPI, forces an I register clear at time T5 and loads it at the end of phase time T1. In the DMA mode, the I register is loaded at the end of phase time T2.

2.3.13 Control 1 A (97340807)

The control 1 board is used on the mainframe of the Sentry 400 system. It has the following five functions:

1. Decodes the addresses for the three DPS's.

2. Decodes the address for 10 RVS's.

3. Generates time delay trigger signals when either an RVS or DPS is addressed.

4. Provides storage and gating for bits 14 and 13 of the DPS's (i.e., the V/I and the DPTGOL bits plus the DPS trip logic).

5. Decodes the address of internal nodes, which can then be monitored by the precision measurement unit (PMU).

The DPS addresses are decoded by IC's C1 and A3 (9301's) from the six address lines AR0/, AR1/, AR2/, AR3, AR4, and AR5. The addresses decoded are as follows:

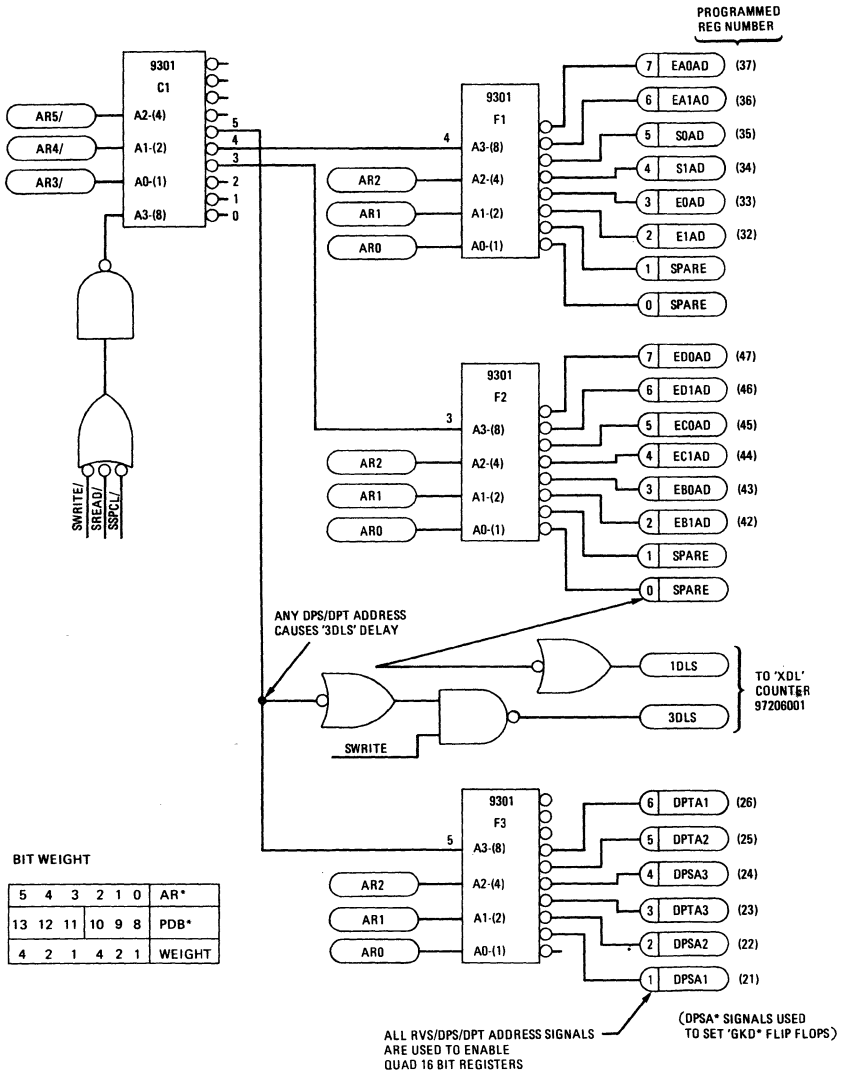
DPT1	26	DPS1	21
DPT2	25	DPS2	22
DPT3	23	DPS3	24

Gates E2 and B2 enable the addressing only when there is an SWRITE/, SPREAD/ or an SSPCL/. C1 decodes the second digit for the DPS's as well as the second digit for the RVS's. A3 decodes the first digit for the DPS's. F1, and F2 decode the first digit (units) for the RVS's. The address codes for the RVS's are as follows:

E1	32	EA0	37
E0	33	EB1	43
S1	34	EB0	42
S0	35	EC1	44
EA1	36	EC0	45

Both DPS and RVS decoding generate a trigger signal for a time delay. The DPS's generate 3DLS/ when writing. The RVS's generate 1DLS/ when addressed.

Three identical circuits on this board generate the DPS functions DPTV/1 (i.e., voltage or current forcing signal and DPTGOL, the greater or less-than bit for current or voltage tripping). Typical of the three circuits, element C5 (9020) provides the storage for the two bits. Element B7 enables reading the information back into the short register bus when enabled by SPREAD/. The flip-flops on IC's A1 and A4 provide the trip logic



BIT WEIGHT

5	4	3	2	1	0	AR*
13	12	11	10	9	8	PDB*
4	2	1	4	2	1	WEIGHT

INPUT SIGNAL	DESCRIPTION
AR0	ADDRESS BIT ZERO SET BY PDB8
AR1	PDB9
AR2	PDB10
AR3/	PDB11
AR4/	PDB12
AR5/	PDB13
SREAD	SHORT REGISTER READ SIGNAL.
SSPCL	SHORT SPECIAL-ADDRESSING SIGNAL USED FOR SPECIAL FUNCTIONS.
SWRITE	SHORT REGISTER WRITE SIGNAL.

FIGURE 2-11. CONTROL 1A SIMPLIFIED

when any DPS is set. Pin 7 of A4 becomes a 0 and it remains a 0 until delay complete (DLCS/) occurs approximately 3 uS later. When pin 7 of A4 goes high the trip gate is enabled and if a valid trip is to occur, the TRIP/, signal is set low and sets a DPT latch in the status register. Note that the inhibit F/F (A4, pin 7) is common to all TRIP/ signals. Pin 10 of A4 enables a trip to occur when a DPT supply is written. If DPT1 is not written, pin 10 of A4 remains low and no trips would occur.

The DPS's have sense circuits which monitor current drain and generate a signal for overcurrent conditions set at approximately 1.5A. If comparator A1 or comparator B1 signals indicate this overcurrent condition, the two flip-flops on element A1 provide the disconnect logic for the DPS's. When GKD is low, the force and sense lines of the DPS are open. GKD is set high when the DPS is selected at the end of the delay, when DLCS/ is high. GKD may go low if comparator A goes low or comparator B goes high.

Since the current trips are bipolar, a less-than, greater-than bit is required to control the trip level. C5-pin 6 provides this control. COMPC/1 generates the trigger level. C5-pin 6 is a logical 1 for greater-than, and a logical 0 for less-than trips. For a trip, therefore, COMPC/1 and C5-pin 6 must be equal for B5-pin 6 to be high and make TRIP1/ low when the trip is enabled by the other two previously described signals.

On page two of the control 1 board schematic, another function is shown--the internal node decoding. Internal nodes are defined as all the reference voltage current trip supplies. Storage for addressed bits is implemented on D7 and D9 (9300's). E6, E7, and E8 (9301's) are the actual decoders. The pin address is stored from the long register data bus LRD0 through LRD7 with the address information on LRA1/, LRA2/, LRA4/, LRR1/, LRR2/, and LRR4/. This has write capability only. The addresses of the internal nodes are as follows:

NODE NUMBER		
OCTAL	DECIMAL	DESCRIPTION
200	128	S1
201	129	S0
202	130	E1
203	131	E0
204	132	EA1
205	133	EA0
206	134	EB1
207	135	EB0
210	136	EC1
211	137	EC0

OCTAL	DECIMAL	DESCRIPTION
214	140	DPS1
215	141	DPS2
216	142	DPS3
217	143	DPT1
220	144	DPT2
221	145	DPT3

2.3.14 Line Receiver II (97206113)

The line receiver II board forms the receiver half of a line-driver/line-receiver transmission of a line-driver/line-receiver transmission path. As on the line driver, a package enables a section of the board for multiplexing purposes. There are sevemal lines on this board that are not multiplexed. These are:

INPUT	OUTPUT
D5	E3
F8	G9
E9	H1

All of the outputs of the line receiver board can be wired-OR tied, except E9 and H0 when a type 9009 device is used for a clock line.

2.3.15 T-Line Driver (97206106)

The T line driver board forms the transmitter half of a line-driver/line-receiver transmission path. In the test set, the board drives up to 50 feet of twisted-pair cable and can drive as many as 44 individual lines. For multiplexing purposes, the board is divided into sections that are enabled by package D.9.

2.3.16 Reference Voltage Supply (97206110) (97206103)

The reference voltage supplies provide the "1" and "0" logic levels to the drivers and detectors. There are two types of RVS supplies as individualized by distinctive part numbers above. The difference between the supplies is that the 97206110 supply gain is one eighth that of the 97206103. The 97206110 supply is used to provide the RVS supply to the drivers on the DUT board which contains a preamplifier with a gain of 8:1. The 97206103 supply is used to provide the RVS supply to the detectors. The detectors do not contain any preamplifier and therefore a gain of 8:1 is required.

The system is supplied with six RVS supplies contained on 3 boards (2 per board). The driver RVS's are designated E0/E1 and EA0/EA1. The detector supplies are designated S1 and S0. The driver supplies are programmed such that one pair provides the drive voltage for the current test and the next pair are programmed waiting for the next test.

Figure 2-12 shows the signal flow path between the drivers, detectors and the RVS supplies. Figure 2-13 illustrates the driver RVS supply providing one eighth the input voltage, with the voltage conditioner preamplifier providing a gain of 8:1. Figure 2-14 illustrates the detector RVS supply providing a gain of 1:1.

Figure 2-15 is a simplified block diagram of an RVS. The programmed value is provided thru a quad 16 bit register to the input of a digital to analog converter. The D/A converter is the current summing type 10 bits plus sign (two's complement). The output of the DAC is fed to the noninverting input of an operational amplifier. The output is then fed to a buffer amplifier capable of driving 60 milliamps at $\pm$30 volts which is then fed to the pin of the DUT. The feed back loop for the operational amplifier is provided by the sense line which contains a feed back risistor and two gain adjustment potentiometers, one for each of the two ranges. The sense line can also be switched to the precision measurement unit for monitoring purposes.

Figure 2-16 is a schematic diagram of the D/A converter. The circuit formed by Q2-11, Q13-22 and Q34-33 constitutes a switch for the 2^9 bit. When the 2^9 bit is a "1" level the circuit will conduct and place R_{IN} as the input resistor to the op amp. Similarly any combination of bits for bit 2^0-2^9 will cause the various resistors to be placed in parallel to provide the appropriate value for the input resistor. Since the ladder network has 10 switches the voltage output may be varied into 1023 discrete voltage levels.

Figure 2-17 illustrates a simplified op amp whose output is determined by the formula $V_{OUT} = \frac{R_F}{R_{IN}} \times V_{IN}$

In the RVS circuit R_F is a constant depending upon the range selected. V_{IN} is a constant 5.12 volts provided by the prime reference supply (to be discussed later). V_{OUT} is therefore varied by changing the value of R_{IN} by means of the D/A ladder network in accordance with the programmed input (10 bits plus sign).

The sign of the voltage is change in the following manner. In figure 2-16 the circuit formed by Q1, Q12 and Q23 is controlled

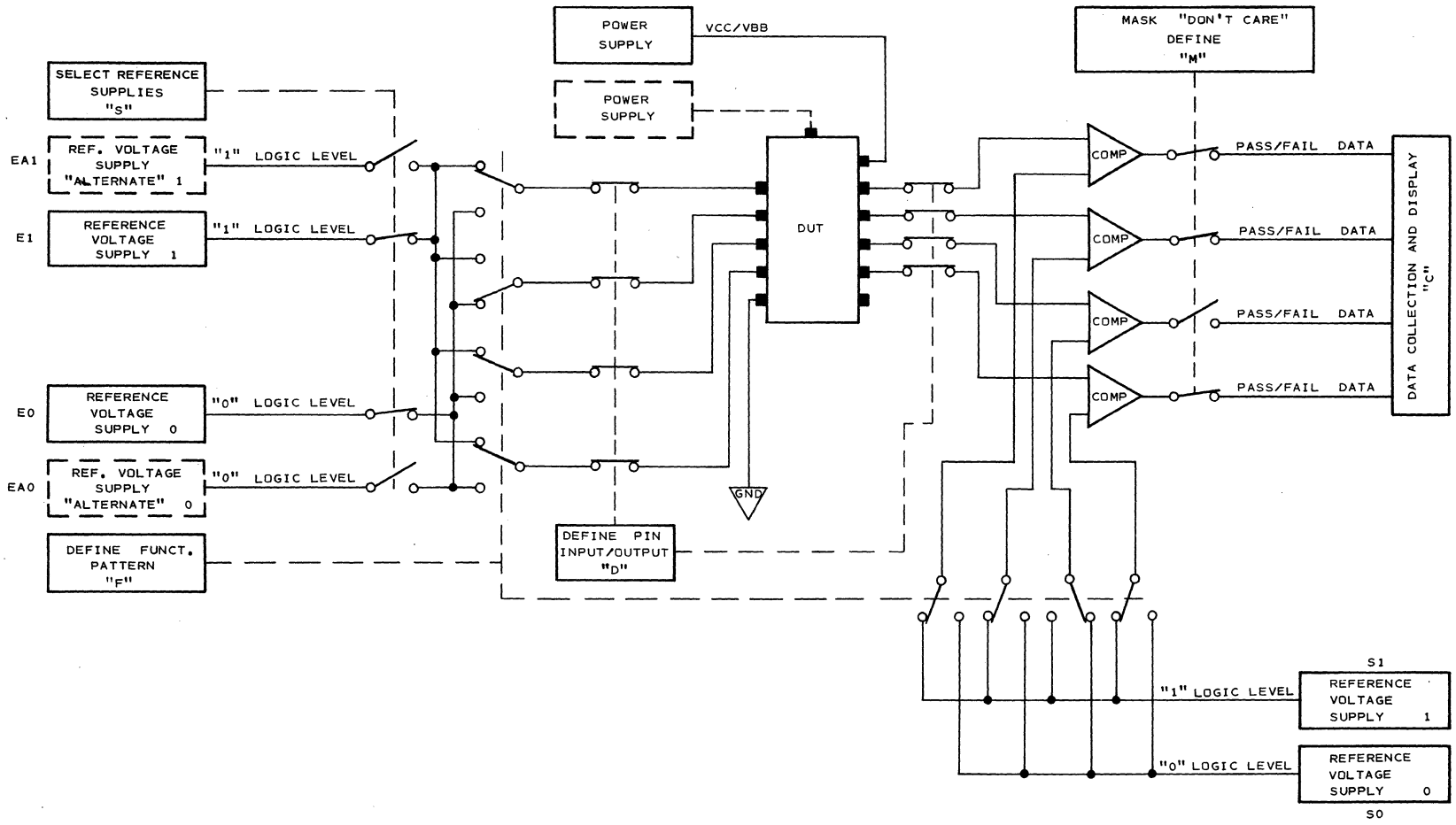


FIGURE 2-12. FUNCTION TEST, SIGNAL FLOWPATH

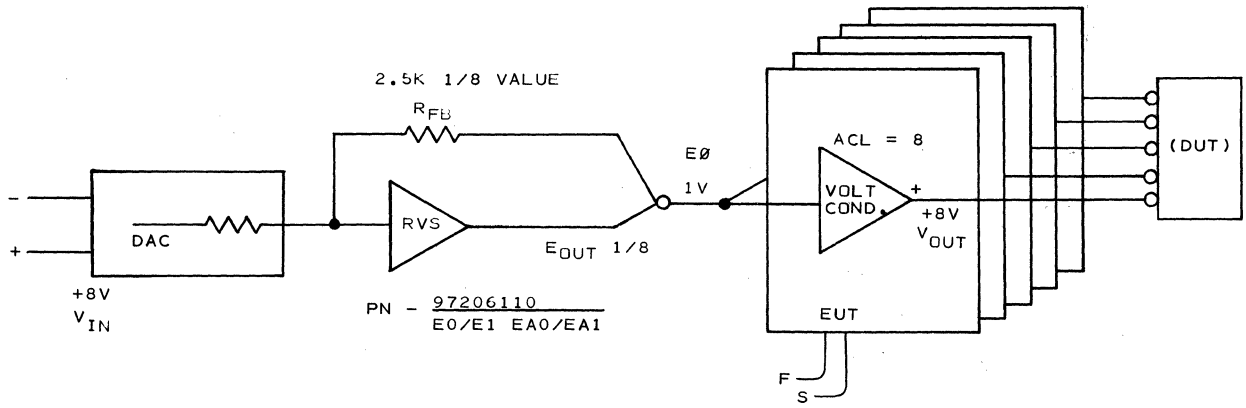


FIGURE 2-13. DRIVER RVS SIMPLIFIED

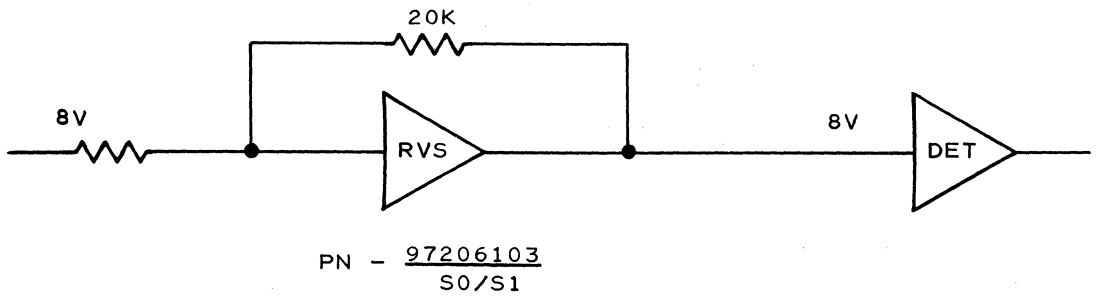


FIGURE 2-14. DETECTOR RVS SIMPLIFIED

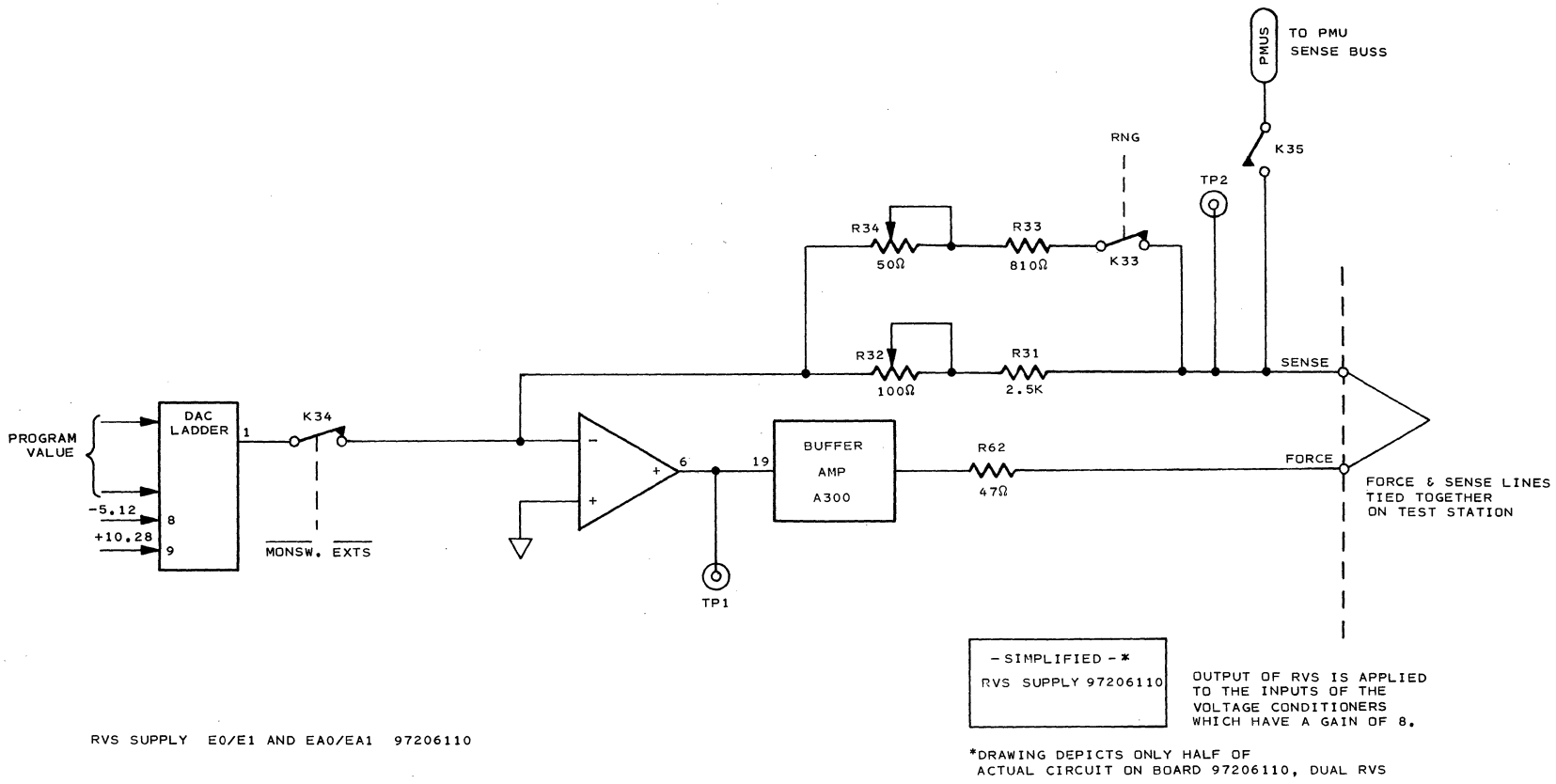


FIGURE 2-15. RVS SIMPLIFIED BLOCK DIAGRAM

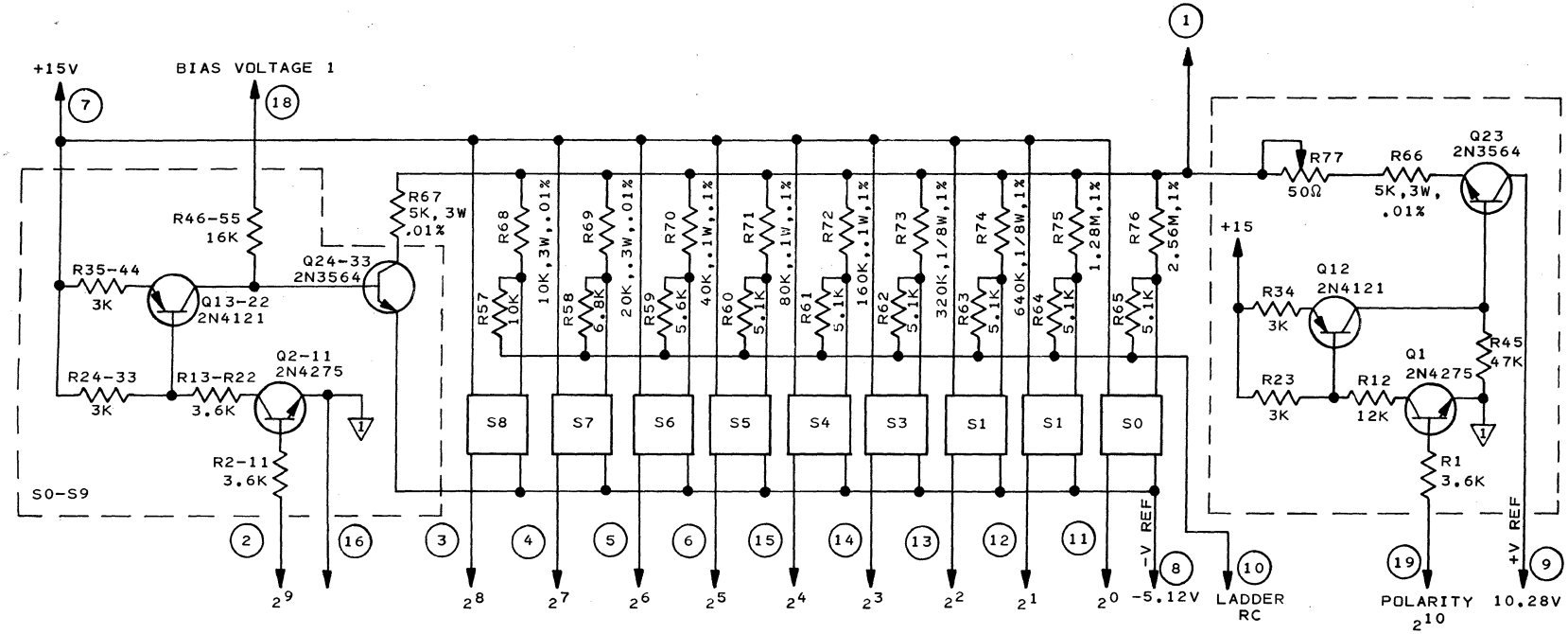


FIGURE 2-16. D/A CONVERTER LADDER NETWORK

FAIRCHILD
SYSTEMS TECHNOLOGY

by the polarity bit. If the polarity bit is zero the circuit is inoperative and V_{OUT} is a plus value. If the polarity bit is "1" (negative) the circuit will conduct and place the - 10.24 reference supply in opposition to the 5.12 reference supply to provide a voltage with a negative polarity. When a negative polarity is indicated the software automatically changes the input to the D/A converter in order to provide the correct value for the output.

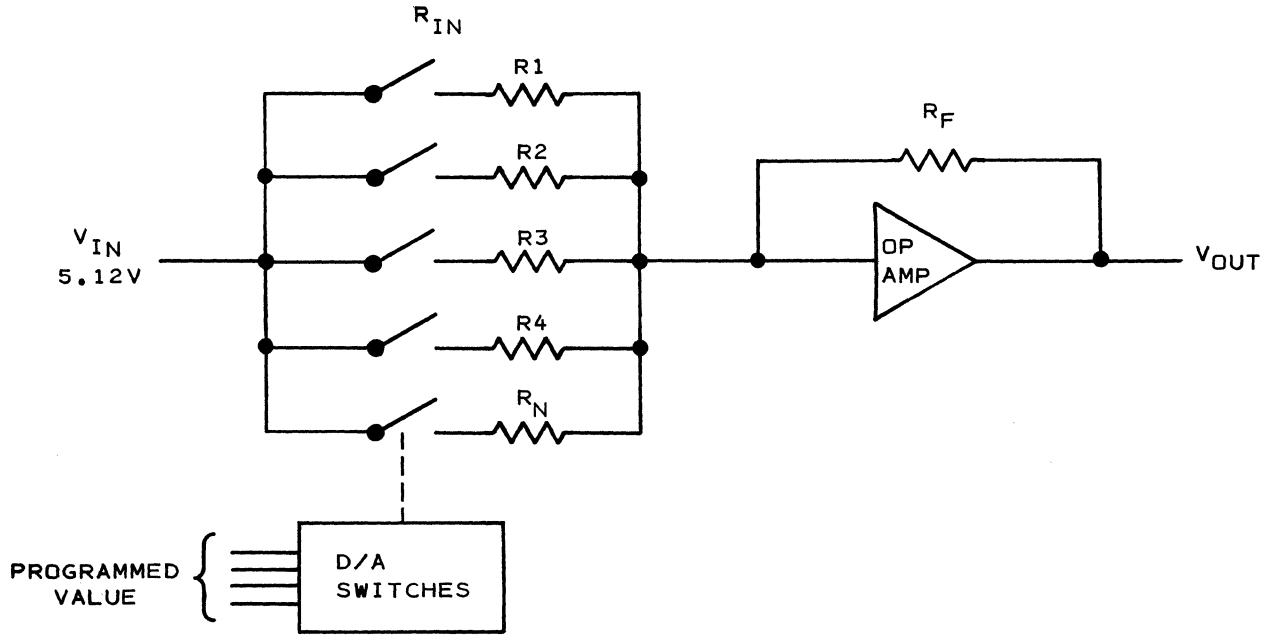


FIGURE 2-17. SIMPLIFIED OP AMP

2.3.17 Digitally Programmed Supply (97206104)

Digitally programmable supplies are connected directly to the device load board to provide the necessary bias supplies to activate the DUT. The supplies can be programmed to force a voltage with a programmable current trip, or to force a current with a programmable voltage trip.

Figure 2-18 and 2-19 illustrate the two configurations. The illustrations are similar to the RVS shown in figure 2-15 and function in a similar manner. Differential amplifier A1 is connected across the current sensing resistors on the 1 amp buffer board. The output of A1 is fed to a comparator A6 along with the programmed trip value.

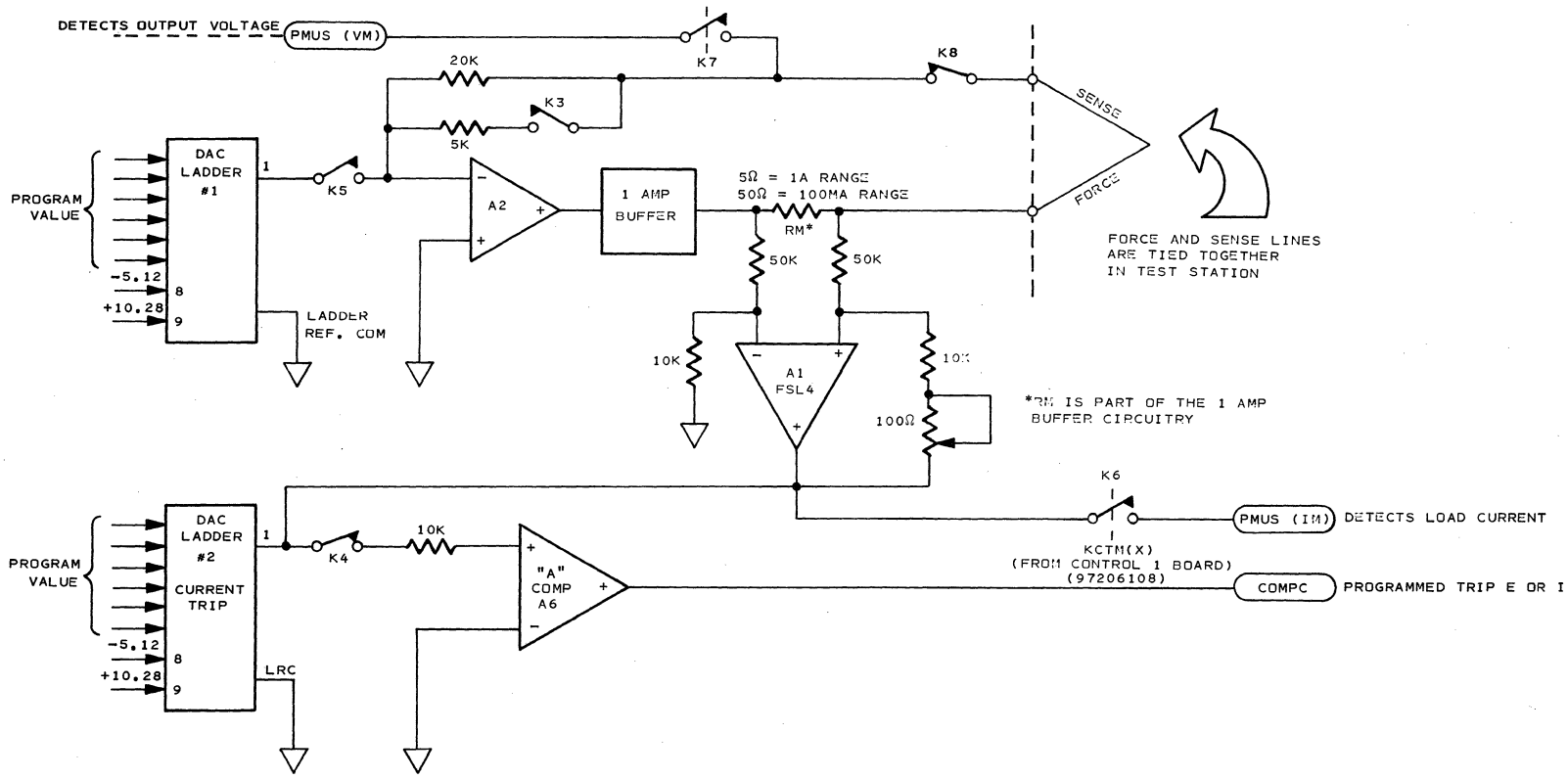


FIGURE 2-18. SIMPLIFIED DPS SUPPLY (V_F I TRIP)

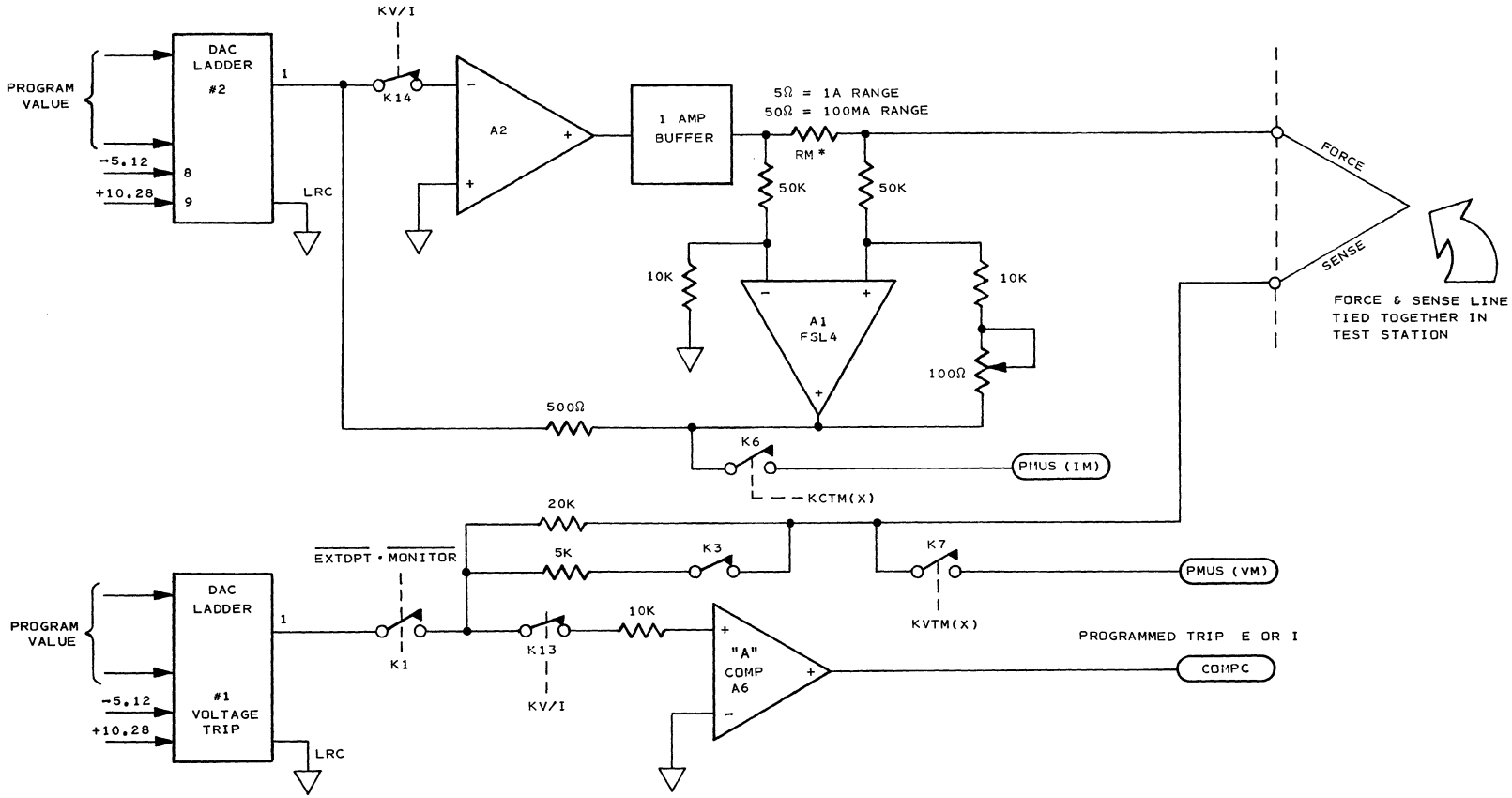


FIGURE 2-19. SIMPLIFIED DPS SUPPLY (I_F V TRIP)

The following discussions provide further details of the digital power supplies and can be found in the DPS schematic diagram (97206104).

The gain of amplifier A2, connected in the current summing mode, may be changed by closing K3; both ranges have vernier gain adjustments and a zero offset adjustment.

The force and sense lines are brought out for remote sensing, and K7 allows the sense line to be multiplexed to the PMUS bus and therefore be monitored by the precision measurement unit. The force line has two resistors in series with it, R26 and R27 (1 amp buffer board) with K3 enabling R26. These resistors allow monitoring of the output current at two range levels.

The three comparators (A4, A5, and A6) perform the following functions: A4 and A5 generate digital signals which disable the 1-amp buffer when its output current is greater than 1.5 amperes. It essentially provides hardware protection for the supply. A4 protects the amplifier for positive, and A5 for negative overcurrents. A6 is a discrete component comparator with high gain and stable input. It compares the current level programmed on the current trip ladder network to the current level sensed at pin F4. The outputs of the comparators A4 and A5 are digital levels that control circuitry which disables K4 and K8 and turns off the supply.

Differential amplifier A1 is connected across the current sensing resistors on the 1 amp buffer board. It generates a voltage which is proportional to the current being drawn by R19, R20, R21, and R22. These circuit elements, in conjunction with K10, K11, K12, are used to adjust the gain for the different range combinations. R23 adjusts the zero offset. Buffer amplifier A3 is a non-inverting, uA741 with the inputs protected for overvoltage. K1 or K2 allows the ladder network or the buffer amplifier, respectively, to be connected to the input of A2.

The switches K1-K12 are single pole and shielded. Their functions are as follows: K1 and K2 are controlled by the signal EXTDPS. The signal MONSW/ inhibits K1, K2 switching. When EXTDPS is true, K2 is closed and the signal generated by A3 is enabled into the summing junction of A2 or A6 depending on whether K5 or K15 is closed. When K2 is open, K1 is closed and the signal at the summing junction of the ladder is the enabled signal.

K3 controls the range of the DPS. When DPSRING is true K3 is closed and the low range is enabled. With K3 open, the high range is enabled. Relays K4 and K5 are enabled in parallel with K13 and K14. These relays are controlled by KV/1, and when this

signal is false, K4 and K5 are closed and the mode of operation is voltage forcing, current measuring. When K4 and K5 are open and K14 and K15 are closed, the mode of operation is current forcing, voltage measuring. Relay K6 enables the output of differential amplifier A1 to be connected to PMUS for monitoring purposes. Relay K7 connects the output of the DPS supply. Relay K8 is controlled by GKD and is part of a disconnect function. It breaks the sense line in the DPS board. The same signal on the 1 amp buffer board disconnects the force line. Relays K10, K11, and K12 control resistors that enable common mode gain error adjustment. Relay K125 enables the adjustment for full scale, high range common mode, low range, DPT. Relay K11 enables the adjustment for DPS full scale low range and DPT high range. K10 enables the adjustment for plus full scale high range on DPS and full scale low range on DPT.

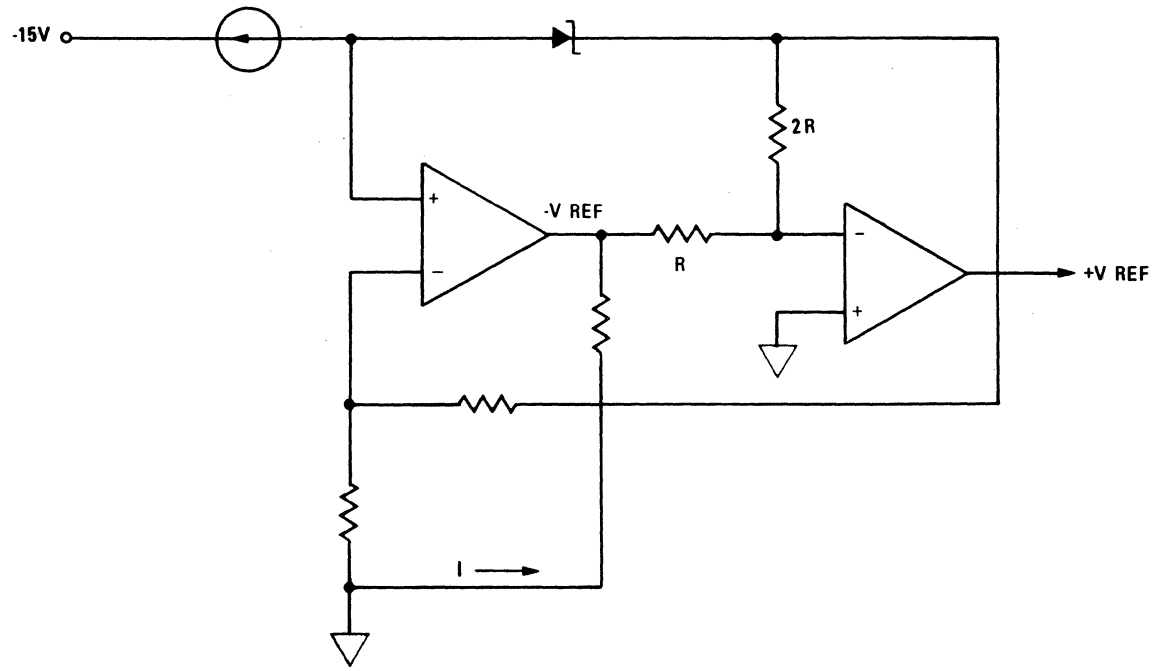


FIGURE 2-20. LINE REFERENCE VOLTAGE SIMPLIFIED

2.3.18 1 Amp Buffer (97206105)

The 1 amp buffer board is an X11 non-inverting amplifier, which is used in conjunction with DPS' board 97206104 to form the DPS assembly. This buffer gives a total current capability for the supply of ±1.5 amperes.

When the input Vo(x) goes more positive, the voltage across R4 increases, since Q1A is turning off and Q1B is turned on harder. Since the voltage across R4 is increasing, Q5 is turning off, which in turn turns Q4 and Q6 less on, and Q2 and Q3 are turned on harder, making the output voltage V1AO(x) more positive.

The output of the amplifier is fed back into the positive input by R15, and since the open loop gain is large, which determines that the two inputs of the amplifier are at essentially the same potential, the output voltage is therefore determined by the feedback resistors. The output is current limited by resistors R12 and R13 and relay K1. Relay K2 controls the power dissipation of the amplifier. Relays K1, K2, and K3 are closed, the amplifier is in the high current range, and is capable of driving 1.5 amperes. With the relays open, the maximum current is 1.5 milliamperes. Resistors R26 and R27, in series with the Force (x) output, monitor the current being drawn from the DPS assembly. Relay K4 enables the amplifier to disconnected from its load. Diodes CR4 and CR5 provide short circuit protection.

2.3.19 Line Reference Voltage (97206111)

The line reference voltage board has two functions:

1. It provides the positive and the negative reference voltages.

2. It provides isolation by means of a buffer amplifier.

Amplifiers A1 and A2 and their associated buffers in conjunction with the temperature controlled zener CR3 generate the reference voltages (see Figure 2-7). Current limiting of 60 milliamperes on the negative supply and 30 milliamperes on the positive supply protect both buffer amplifiers. Resistor R17 gives the negative supply the ability to drive additional loads by allowing the -V ref output of the amplifier to sink a current equal to

$$I_{R17} = \frac{15\ (-Vref)}{R17}$$

plus the current limit of the amplifier. This buffer amplifier cannot be used as a current source since it normally must be a 50-mA source for R17 when no load is applied.

Amplifier A3 and its buffer provides the other function on this board. It is used on the test set in the gain-of-1, noninverting configuration. It provides a buffer for the reference common which is connected at the input. The output is used to drive the ladder RC.

2.3.20 Analog Multiplexer (97209601)

The function of the analog multiplexer board (refer to schematic 97209601-04) is to multiplex the mainframe to up to four test stations. There is one board for each station. The board is composed of nine relays and one relay driver.

The driver is turned on by signal THENX/ (test head enable barred). The relays connect the DPS's (1, 2, 3), RVS's (EA1, EA0, E1, E0, EB1, EB0, EC1, EC0, S1, S0), PMU sense, and REFCOM from the mainframe to the selected test station.

2.3.21 Line Receiver (97206107)

The line receiver board forms the receiver half of a line driver/line-receiver transmission path. Just as on the line driver, a package enables a section of the board for multiplexing purposes. There are several lines on this board that are not multiplexed. These are:

INPUT	OUTPUT
D5	E3
F8	G9
E9	H1

All of the outputs of the line receiver can be tied together into a wired-OR function except E9 and H0 when a type 9009 IC is used for a clock line.

2.3.22 15 Bit Decoder (97341603)

The 15 Bit Decoder board contains the following discrete circuits:

1. Address decoder for several 15-bit registers.
2. Pin address register.
3. PMU address decoder.

4. Internal node decoder.

5. Clock relay decoder.

6. Connect voltage conditioner circuit.

120 Bit Register Decoder

The 120 bit decoder board utilizes logic combinations of bits 19, 20, and 21 to generate D, M, F, S, C, and R enable signals. The two long-register address codes that are not used on the 120 bit decoder board (see description of 19 bit decoder board) are 000 and 111. Table 2-9 shows the decoding structure developed for the 15 bit decoder board, using 111 as a decode enable.

Pin Address Register

This 12-bit register is a buffer register that holds information for the following functions:

1. Precision measuring unit pin connection (PMU Addressing)

2. Internal node decoding

3. Clock relay control

4. Connect voltage conditioner

PMU Addressing

The PMU address decoding structure utilizes an 8-4-2-1 binary code for pin decoding as well as rank decoding. In one sense, the PMU decoding is partially done on the 15 bit decoder board and completed on the EUT boards where there is coincidence between the signals RANK and PIN. The pin address register format is shown in Table 2-10.

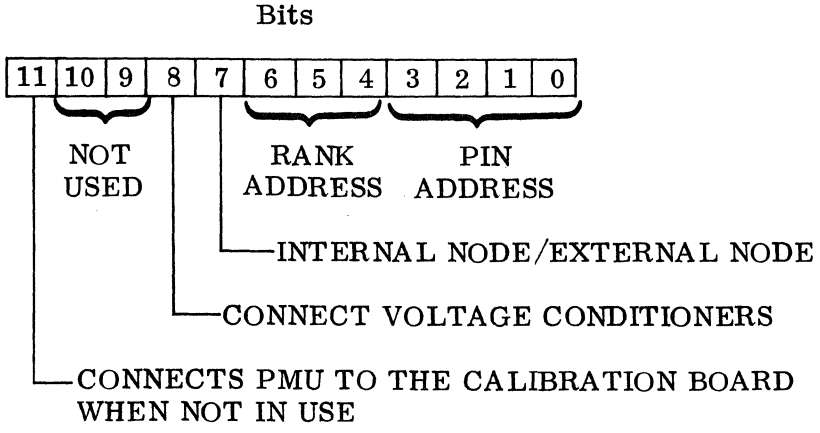
Internal Node Decoding

The internal nodes are the nodes dedicated to the internal power and reference supplies of the test set. This allows the PMU to be addressed to these node points, and thereby gives the test set a self-diagnostic capability. Note that bit 11 of the pin address register is hardwired to a logical 1 at the register input. This allows the PMU to be connected to the calibration load board via the CALAD signal when the system is reset.

TABLE 2-9. 15-BIT REGISTER DECODING

BITS			REGISTER ADDRESSED	BITS			
21	20	19		18	17	16	15
1	1	1	Pin Address Register	0	0	0	0
1	1	1	SIDRAD	0	0	0	1
1	1	1	SNDRAD	0	0	1	0
1	1	1	CSRAD	0	0	1	1
1	1	1	PPSRAD	0	1	0	0
1	1	1	PSLRAD	0	1	0	1
1	1	1	EIRAAD	0	1	1	0

TABLE 2-10. PIN ADDRESS FORMAT



Whenever the pin address register is written into, that is, when the PMU is being used, the CALAD signal is removed unless specifically addressed by the lower order bits of the register.

Clock Relay Decoding

This circuit, generating the signals CRLY0/ through CRLY3/ (clock relay pins 0 through 3), gives the user an opportunity under program control to connect external black boxes to one of the first 4 pins of the test system. These signals are used in conjunction with the sync signals. The CRLY/ signals may be used to close an external relay, and the sync signals to start and stop the black box generator.

Connect Voltage Conditioner

This circuit allows the user to connect the PMU to a device pin in one of two ways. Either the voltage conditioner (pin driver) is connected to the device under test before the PMU is connected, or the voltage conditioner is connected to the device under test after the PMU is connected. These modes of operation are often referred to as make-before-break or break-before-make modes.

2.3.23 120 Bit Decoder (97200101)

The 120 bit decoder board consists of three distinct circuits:

1. Long-Register Decoding Logic

2. Sync and Strobe Logic

3. Fail Set Logic

Long Register Decoding Logic

Two ranks of long-register control signals are decoded by this board; therefore, one 120 bit decoder board is needed for each 30 tester I/O pins. Table 2-11 depicts how the long register data bits are decoded. Bits 18 through 15 form the rank address in binary 8-4-2-1 code. Bits 21 through 19 form the long-register address and are assigned arbitrarily.

Notice that the rank decoding is done on the backplane rather than on the PC board. This allows one board type to be used for all ranks with a hardwired coding scheme (see schematic). To reflect their specific function and binary coding, the above

TABLE 2-11. LONG REGISTER DECODING

REGISTER	BITS			RANK	BITS			
	21	20	19		18	17	16	15
D	0	0	1	0	0	0	0	0
M	0	1	0	1	0	0	0	1
F	0	1	1	2	0	0	1	0
S	1	0	0	3	0	0	1	1
C	1	0	1	4	0	1	0	0
R	1	1	0	5	0	1	0	1
Special Registers (See 15-Bit Decoder Card)	1	1	1	6	0	1	1	0
				7	0	1	1	1

long-register data bits are often referred to by the following names:

BIT	NAME	FUNCTION
15	LRR1	Long Register Rank 1's digit
16	LRR2	2's digit
17	LRR4	4's digit
18	LRR8	8's digit
19	LRA1	Long Register Address 1's digit
20	LRA2	2's digit
21	LRA4	4's digit

There is one asynchronous signal in the decoding logic called GMTS (gate master to slave). This signal transfers 120 bits of data from the master side of the F and S registers simultaneously, so that all of the tester pin drivers change state at the same time.

Sync and Strobe Logic

The sync circuit allows the user to generate up to four synchronous sync pulses under program control. The logical function of this circuit is to give the user a sync pulse whenever F.CSR=1. The strobe circuit allows the user to strobe the 'C' register for pass/fail information under program control. Again, as in the sync circuit, the function is to strobe the 'C' register whenever F.CSR=1.

Fail Set Logic

This circuit is one large 16-input OR gate. Whenever a fail condition occurs within two ranks, the signal TFALS/ is generated. This signal is joined in a wired-OR circuit with the TFALS/ signals from the other ranks; therefore, whenever a fail condition occurs on any pin the mainframe is notified of the event.

See Section 3.2.3 for these board descriptions:

PMU CONTROL (97230104)
PMU ANALOG 1A (97341605)
PMU ANALOG 2A (97341604)

2.3.24 PEST Register (97201902)

The PEST register board provides four different functions as follows:

1. Multiplex function which consists of eight type 9309 IC's. Four groups of 16 bits of information can be transferred to the output depending on the combination coding of S0 and S1. Only one group of 16 bits can be transferred at a time.

2. Parallel entrance, serial transfer function which consists of four type 9300 IC's. When PE is low, 16 bits of information from multiplex enter the 9300's by clock pulse. When the PE is high, all the 16 bits of information previously clocked into 9300's, will be serially transferred out by 16 clock pulses.

3. One-out-of-ten decoder function. The binary code (bit weights 1, 2, and 4) from 97201906 enter a type 9301 IC, are decoded into seven different signals, and go through a buffer output.

4. Inverter function. Signals from 97201906 are inverted by type 9016 and type 9009 IC's. The 9009's are inverter-buffers which can handle higher load currents than the 9016's.

2.3.25 Pin Control Logic (97200103)

Each pin control board (Figure 2-21 contains a complete set of control logic for 2 tester I/O pins. Therefore; the board is a two-bit slice of each long register. The term long register refers to the specific D, M, F, S, C, and R registers in the test set that may be as long as 120 bits (one bit per tester I/O pin) or as short as 1 bit. Table 2-12 lists the D, M, F, S, C, and R registers and gives a brief description of each register function. Figure 2-8 shows that the pin control board consists of four major circuits:

1. A two-bit slice of each long register

2. Long-register read logic

3. Lamp display logic

4. Pass-fail set logic.

The second listed circuit, whose operation is self-evident in the schematic, will not be discussed.

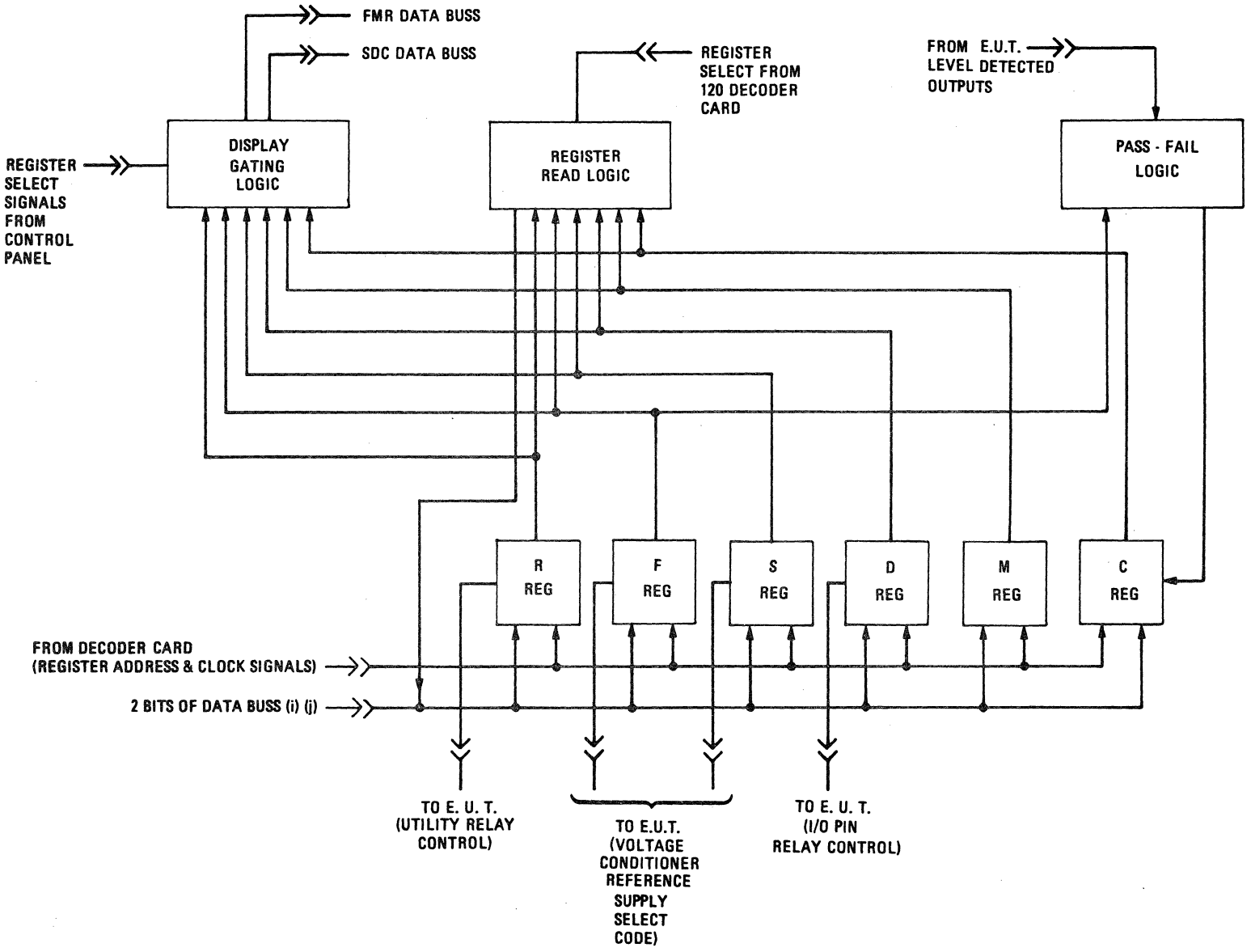


FIGURE 2-21. PIN CONTROL LOGIC SIMPLIFIED

TABLE 2-12. D, M, F, S, C, AND R REGISTER FUNCTIONS

REGISTER NAME	SYMBOL	FUNCTION
DEFINE	D	Defines each tester I/O pin as input/output. 1 = input, 0 = output.
MASK	M	Provides logical care/don't care condition for pass/fail signals of each tester I/O pin. 1 = care, 0 = don't care.
FUNCTION	F	Performs a dual function depending upon whether a tester pin is defined as an input pin or an output pin. a. For tester input pins, the register provides the expected logical 1 or 0 for the pass/fail circuit. b. For tester output pins, the register provides one-half of a two-bit binary code that selects one of four reference supply voltages that can be gated to the element under test.
SELECT	S	See part b of f register.
COMPARE	C	Provides storage of pass/fail status for each tester I/O pin.
UTILITY	R	Provides direct utility relay control. 1 = relay closed, 0 = relay open.

F	S	Reference Selected
0	0	E0
1	0	E1
0	1	EA0
1	1	EA1

Long Register Two-Bit Slices

All of the long registers except the C register are standard holding registers for the functions shown in Table 2-16. Therefore, only the C register will be discussed here.

The primary function of the C, or compare, register is to store pass-fail data of each tester pin. After each functional pattern is executed and the appropriate programmed time delay has lapsed, the C register is strobed to log the pass-fail condition of each pin (0 = pass, 1 = fail). The information in the C register can either be datalogged or ignored. Normally, the pass-fail data that results from the Mth F pattern is held until after the (M+1)st F pattern is executed. If the latch C function is not invoked, the C register is first cleared, then strobed, to log in the pass-fail information of the (M+1)st F pattern. When latch C is invoked, the clear C signal is inhibited. Therefore, in this mode of operation, once a failure has occurred on a particular pin it is never forgotten. This allows gross sorting of devices in the automatic test mode of system operation where the only interest is whether a device passes all functional tests or not.

Lamp Display Logic

The control signals for this circuit come from the pushbutton switches on the test station control panel. The control signals are the following:

1. GFD = Gate F to Display
2. GSD = Gate S to Display
3. GCD = Gate C to Display
4. GDD = Gate D to Display

Pass-Fail Set Logic

The Pass-Fail Set circuit receives the following input signals:

1. LD0 The level detector output with S0 as a reference.
2. LD1 The level detector output with S1 as a reference.
3. F The true function register bit.
4. F/ The complement function register bit.
5. M The true mask register bit.

6. TNEGL/ Negative logic.

7. STRBC/ Strobe C.

The level detectors used in the test set generate a logical 0 whenever the input voltage is greater than the reference supply voltage. For positive logic a logical 1 must be above S1 and a logical 0 must be below S1.

2.3.26 EUT Interface (97200104)

The EUT (element under test) interface board contains two voltage conditioner modules and four level detector modules. One voltage conditioner and two level detectors comprise the force and sense functions for one tester pin. Therefore, one EUT interface board drives two tester pins.

In addition to the force and sense electronics, the board decodes pin control logic signals to open and close appropriate relays to connect forcing and sensing signals to and from (respectively) the device under test. The relay equations are:

K9 + K10 (Utility Relay): Close = R bit

K1 + K5 (Level Detector Relay): Open = PMU Relay Closed + CRLY/(Low)

(K6 . K8) + (K2 . K4) (PMU Relays): Close = PMU addressed (Rank . Pin)

(K3 + K7) (Voltage Conditioner Relays): Open = CRLY/ (Low) + TD (Low) + PMU addressed . CVC/ (High)

2.3.27 Decoupling Board (97200110)

The primary function of this board is to filter the reference voltage supplies (E0, E1, EA0, EA1). In addition, the board contains fuses that are used in conjunction with zener diodes to protect the MOS-FET analog switches located on each pin driver module. Ordinarily, the RVS voltages are restricted to -3.75 volts $\leq$Vref$\leq$3.75 volts, but should a supply fail, the reference voltage can go to $\pm$48 volts. For this reason, the reference voltage lines are fuse-and-zenerer-diode protected. Note that reference supplies S0 and S1 are not fused, since they have a $\pm$30 volt operating range in the system.

2.3.28 Monitor Control (97340801)

The monitor control board consists of several independent interface circuits used to display data on the front panel. There are three latch circuits for SYNC, STROBE and MONITOR switches; one reference voltage circuit which generates voltage for manual reference power supplies; and operational amplifier to amplify the E0, E1, EA0 and EA1 reference voltages by a factor of 8 in order to display them properly on the front panel dvm; a power alarm circuit which produces an audible alarm when any dc power supply fails.

2.3.29 Power Supply Alarm (97204601)

The power supply alarm board consists of a summing amplifier, an oscillator, and two drivers. Its purpose is to monitor up to four dual power supplies and four 5-volt power supplies, and generate a modulated signal when any of the supplies fail or exceed predetermined voltage limits.

A1 is a summing amplifier, with inputs R1 through R8. The output is bucked against plus and minus 15 volts in such a way that when the output of the amplifier exceeds its circuit voltage for an alarm, A2(10) goes high. A2(8), A2(6) and A2(1) form an oscillator which drives Q1 and Q2. The collector of Q1 and Q2 can be used to drive a lamp or an alarm buzzer.

Diodes CR6, CR7 and CR8 are connected to the input of A2(10) so that when one of those supplies fail, the oscillator is enabled. A dual supply alarm is generated when +V and -V differ enough to generate an error current, which when multiplied by the feedback resistor R9, generates a voltage on the output of A1 which triggers the oscillator. Note that if plus or minus 15 volts, or the plus 5 volts that drives the gate fails, an alarm condition will be generated.

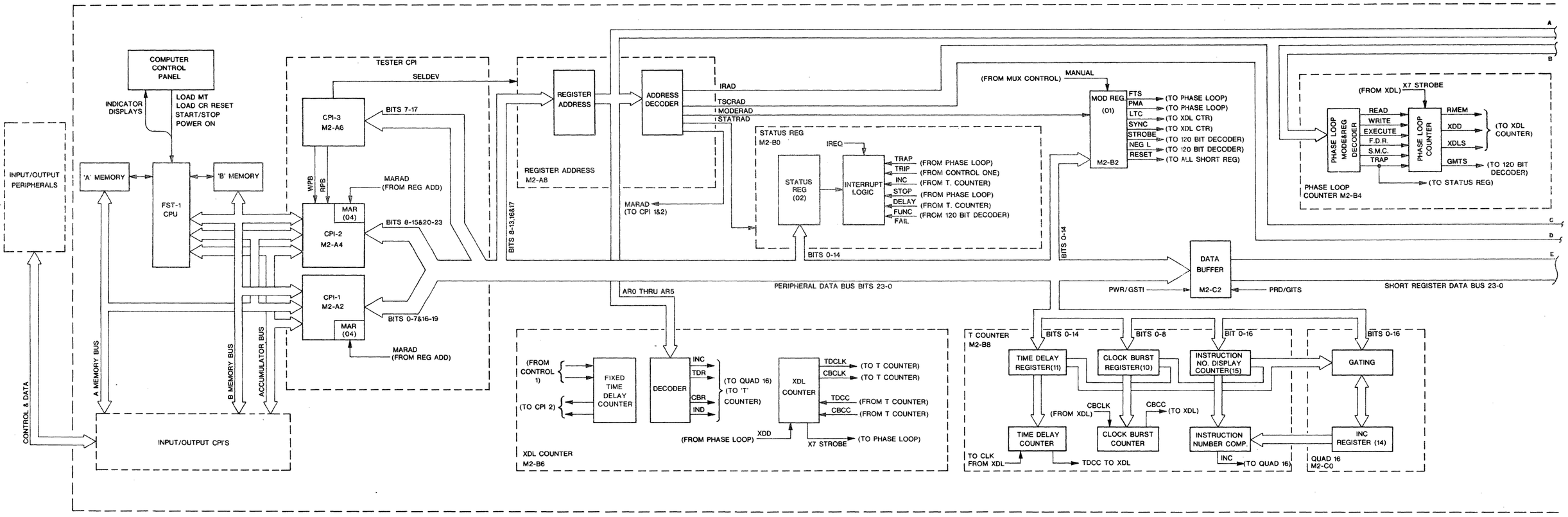


FIGURE 2-22. S100 SYSTEM BLOCK DIAGRAM (Sheet 1 of 3)

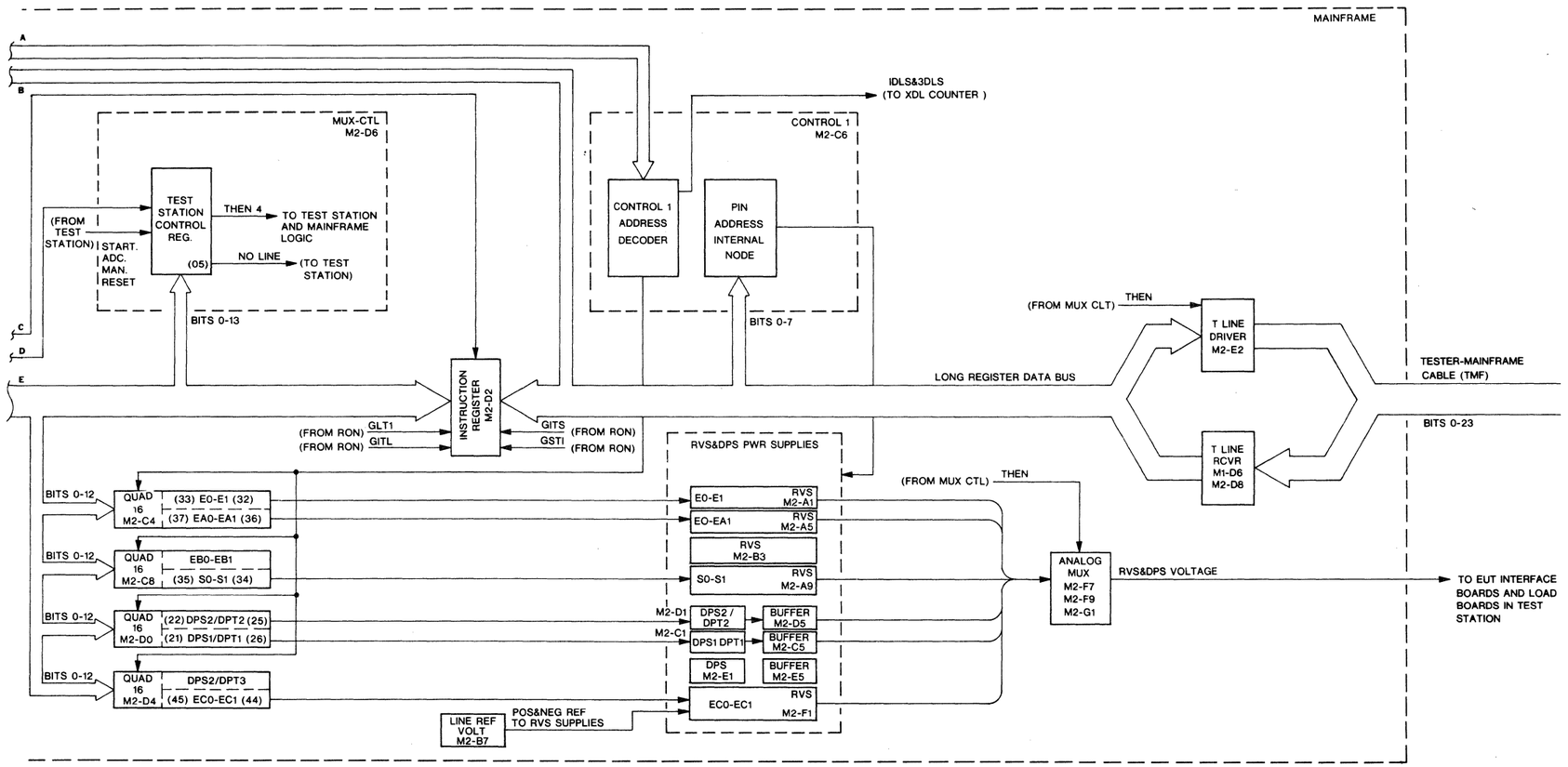


FIGURE 2-22. S100 SYSTEM BLOCK DIAGRAM (Sheet 2 of 3)

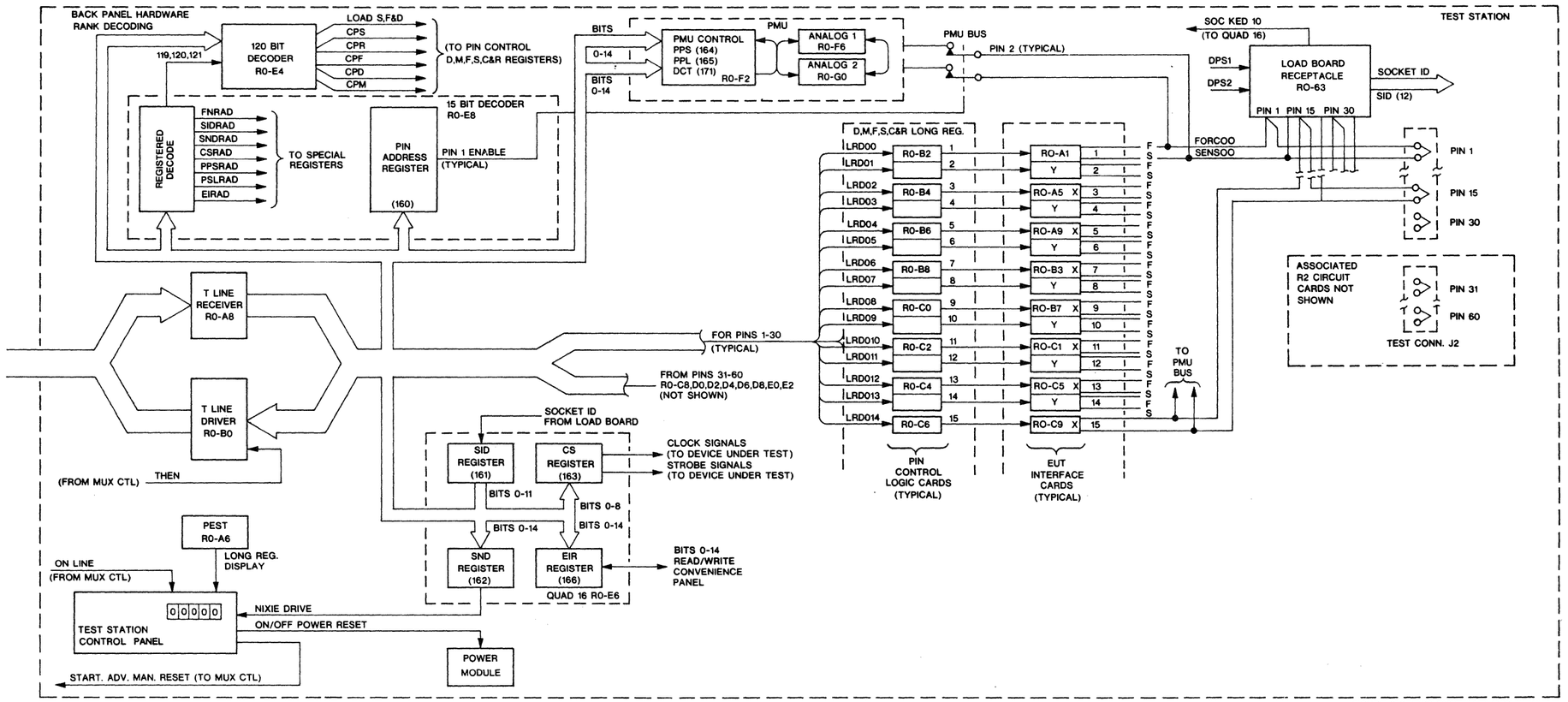


FIGURE 2-2, S100 SYSTEM BLOCK DIAGRAM

FIGURE 2-22. S100 SYSTEM BLOCK DIAGRAM (Sheet 3 of 3)

Section III
Theory of Operation

3.1 TESTER OPERATING AND INSTRUCTION MODES

3.1.1 Operating Modes

The test set has two modes of operation, selected from the test station control panel:

1. Automatic Mode

2. Manual Mode

The automatic mode of operation enables the programmed test statements to be automatically executed by pressing the START pushbutton. Through the use of certain programming statements, the program may be interrupted when a functional failure occurs or at a pre-determined statement number. In this event, the START pushbutton must be pressed again to restart the program.

The automatic mode allows all programmed tests on a device under test (DUT) to be performed by the actuation of one pushbutton. Pressing the START pushbutton on the test station enables the test set to automatically perform all statements of the program; datalog as required; print terminal errors when applicable; or continue testing until the END statement of the test program has been decoded.

The manual mode of operation enables the tester to execute the assigned test program one instruction at a time. The manual mode is selected by pressing the MAN pushbutton. From then on a single instruction will be executed each time the START pushbutton is pressed. The manual mode is used primarily for test program checkout.

The manual mode allows execution of one statement at a time in order to facilitiate device troubleshooting. The use of the ADV pushbutton on the test station control panel allows the program to run automatically, but at a very slow rate. Whenever the ADV pushbutton is released, the tester will stop on the statement it is currently executing. The manual mode permits the observance of the programmed instructions, in order to determine how the device under test is responding to the programmed stimuli.

System troubleshooting may be facilitated by using the manual mode.

SPU and DMA Instructions There are two instruction modes possible within either of the two operating modes. They are the select peripheral unit (SPU) and the direct memory access (DMA) modes. The SPU mode provides for initial test program setup, including the selection of logic level voltages (E0-E1, etc.) for use during a specific test. Following the SPU setup instructions, the tester assumes control and is linked directly to memory in order to receive DMA instructions. The DMA sequence contains specific instructions for use of previously SPU-programmed voltages as stimuli or comparator references. The DMA instructions are separated by the computer into blocks for direct application to the tester. There are two different types of DMA instructions, which are as follows:

1. Functional Logic Test

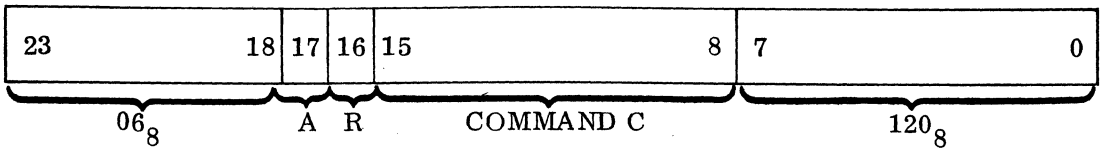
2. DC Parametric Test (PMU - precision measurement unit)

Normally, the functional logic test or the dc parametric test is executed in the DMA mode, although it is possible to perform these tests in the slower SPU mode. The formats for the SPU and the DMA instructions is given in table 3-1 and table 3-2, respectively.

The DMA instruction is a method of transferring programmed data from core memory, in the computer, directly to the test station registers without excessive delay. On the other hand, several SPU instructions are required to address and load a register. Loading data into a forcing supply, (e.g., FORCE VF1), is a non-DMA operation. SPU commands are required to first address the VF supply register and then to write into the register. During this time the computer is servicing the tester and cannot perform other functions. To initiate DMA operation, the computer first sets up the test system with SPU commands, and then turns the loading of the data over to the tester logic. The computer is then free to process data, make decisions on the basis of test results, and process fail or other interrupts.

TABLE 3-1. SPU INSTRUCTION, TYPICAL FORMAT

PART I. During a computer cycle, SPU format selects a specific tester short register at computer phase time T5 (see SPU detailed timing discussion in this section).

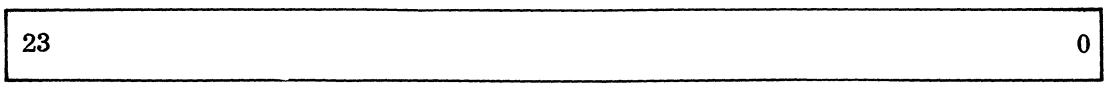


BITS	FUNCTION
23-18	06_8 specifies SPU instruction
17-16	A and R bit pattern specifies read, write, special, or no-operation
15-8	Typically, contains address of applicable tester short register
7-0	120_8 specifies tester as the addressed peripheral

SHORT REGISTER LISTING

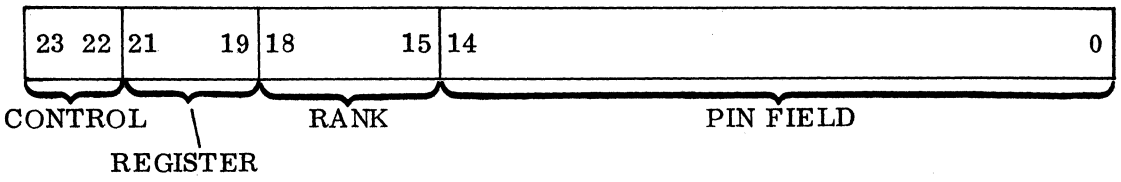
REGISTER	OCTAL ADDRESS	REGISTER	OCTAL ADDRESS
Mode	01	DPT2	25
STATUS	02	DPT1	26
Instruction	03	E1	32
MAR	04	E0	33
TSC	05	S1	34
CBC	10	S0	35
TDC	11	EA1	36
INC	14	EA0	37
IND	15	EB1	42
DPS1	21	EB0	43
DPS2	22	EC1	44
DPT3	23	EC0	45
DPS3	24		

PART II. Once a specific short register is selected at time T5, 24 bits of new data, previously stored in computer register A (accumulator) or from memory, is transferred to the selected short register at phase time T1 (see SPU detailed timing discussion in this section).



24 DATA BITS

TABLE 3-2. DMA INSTRUCTION, TYPICAL FORMAT



CONTROL			REGISTER ADDRESS BITS				RANK OR SPECIAL REGISTER ADDRESS BITS				
BIT 23	BIT 22	CONTROL	BIT 21	BIT 20	BIT 19	NAME	BIT 18	BIT 17	BIT 16	BIT 15	RANK OR SPECIAL REGISTER NAME
0	0	WRITE & HOLD	0	0	0	NOT USED	0	0	0	0	0
0	1	WRITE & EXECUTE	0	0	1	D	0	0	0	1	1
1	0	READ	0	1	0	M	0	0	1	0	2
1	1	TRAP	0	1	1	F	0	0	1	1	3
			1	0	0	S	0	1	0	0	4
			1	0	1	C	0	1	0	1	5
			1	1	0	R	0	1	1	1	6
			1	1	1	SPECIAL REGISTER DEFINED BY RANK BITS	1	0	0	0	7
							0	0	0	0	PA
							0	0	0	1	SID
							0	0	1	0	SND
							0	0	1	1	C&S
							0	1	0	0	PPS
							0	1	0	1	PSL
							0	1	1	0	EIR

if the TSC register is read. Under TOPSY monitor control, the computer repeatedly interrogates the TSC register by issuing an SPU command addressing the TSC register. When the SPU command addresses the TSC register with the proper read code, the station select request bits will be read into the computer and serviced individually beginning with test station 4, then 3, then 2, and finally station 1 (3, 2, and 1 not used in this system). For this reason, systems having only one station are normally configured with the test station connected to test station 4 multiplex cables. This configuration reduces the multiplex selection process time for the computer. Once the computer has received the select request bits from the TSC register, it can issue another SPU command to enable the test station, closing the multiplex relays. A flow chart of the TOPSY monitor and station scanning sequence is shown on Figure 3-1. A simplified logic diagram of the multiplex control board is shown in Figure 3-2, showing the operator's test start request, and the computer read and the computer write actions that take place during and after a test start request.

Short Register Loading The short registers of the test are loaded, as the FACTOR program dictates, in a non-DMA mode of operation. As an example, consider the FACTOR statement:

```
FORCE VF1 5.0, RNG2
```

The TOPSY interpreter generates an SPU command which addresses the tester common peripheral interface (CPI) channel. Table 2-1 provides a breakdown of the typical SPU instruction. Bits 0 through 7 of the 24-bit word accomplish this addressing task at computer phase time T4. Also during this time, the status of the system is gated back to the accumulator bus (BN bus) via bits 20 through 23. Also during this time, the status of the system is gated back to the accumulator bus (PN bus) via bits 20 through 23.

At computer phase time T4, bits 8-13, 16, and 17 are gated from the accumulator bus to the peripheral data bus and applied to the register address board (Figure 3-3). At computer phase time T5, bits 8-13, 16, and 17 are stored in shift registers located on the register address board. These bits generate the address signals to enable the short registers, including the quad 16 bit short registers which provide range, polarity, and magnitude data to the RVS's and DPS's.

Short Register Addressing and Loading Refer to Table 2-2 for a listing of the short registers. The short registers consist of two groups. One group is comprised of the registers loaded from

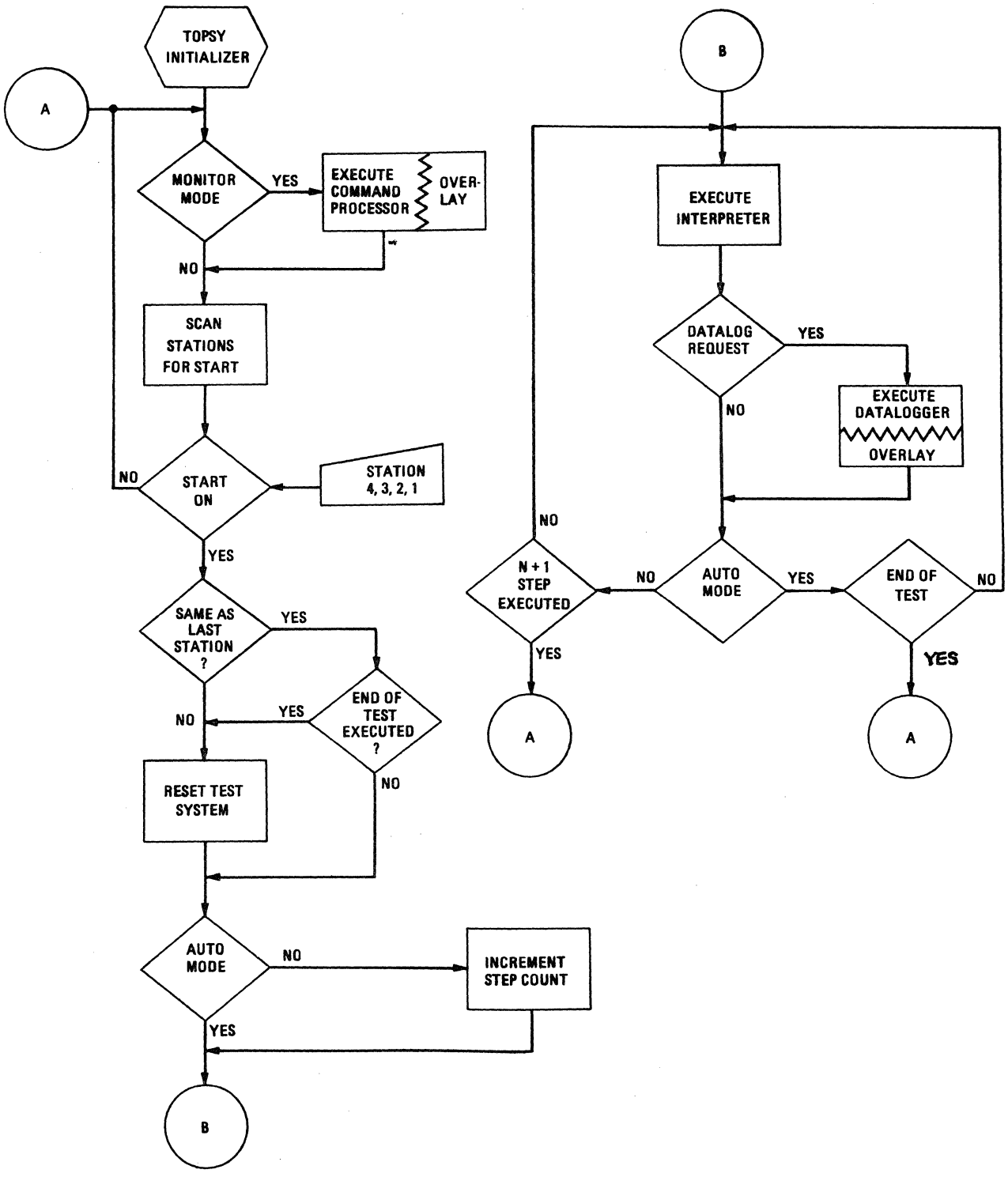
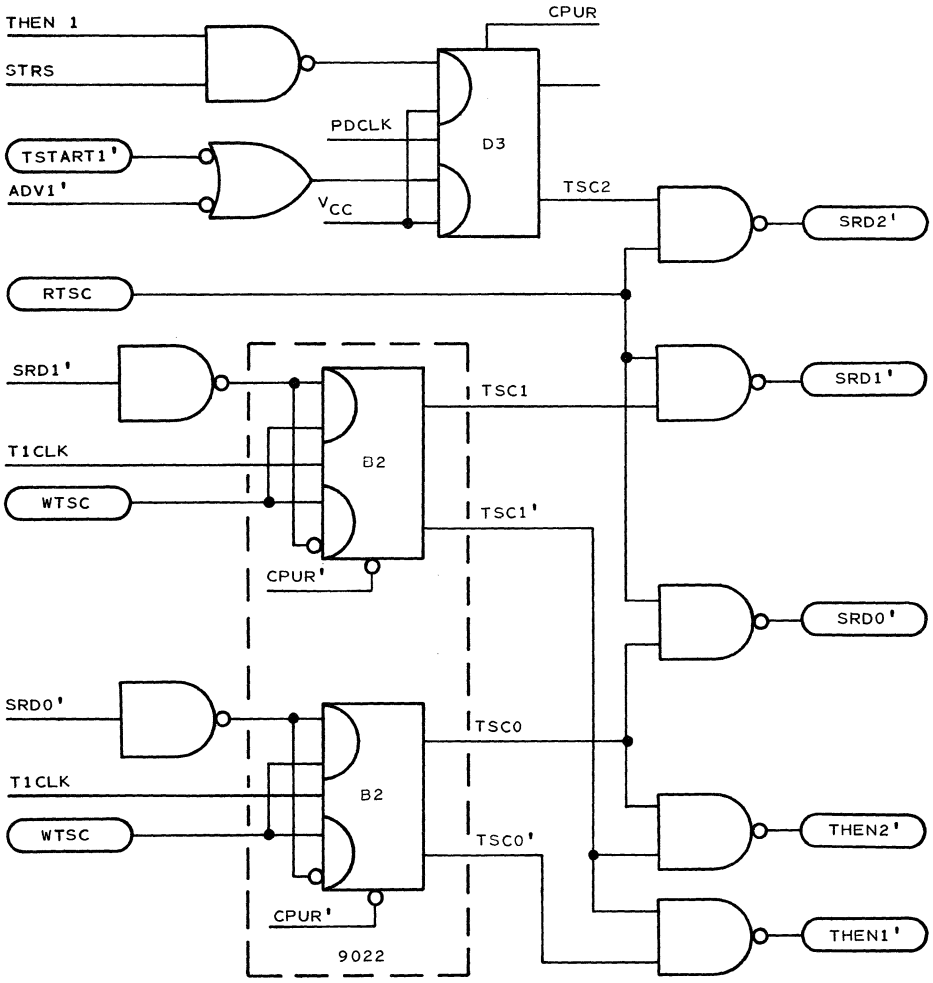


FIGURE 3-1. TOPSY FLOWCHART



SIGNAL	DESCRIPTION
ADV1'	ADVANCE PUSH BUTTON SIGNAL USED TO ADVANCE TO NEXT STATEMENT WHILE IN MANUAL TEST MODE.
CPUR	COMPUTER RESET
PDCLK	PERIPHERAL DATA CLOCK
RTSC	READ TEST STATION CONTROL REG.
SRD0'	SHORT REGISTER DATA BIT 0
SRD1'	SHORT REGISTER DATA BIT 1
SRD2'	SHORT REGISTER DATA BIT 2
STRS	START SET-USED TO RESET THE TEST START
THEN1'	TEST HEAD ENABLE STATION ONE
THEN2'	TEST HEAD ENABLE STATION TWO
TSC0	TEST STATION CONTROL BIT 0
TSC1	TEST STATION CONTROL BIT 1
T1CLK	CPU T1 AND PDCLK 'ANDED' TOGETHER

FIGURE 3-2. SIMPLIFIED MULTIPLEX CONTROL

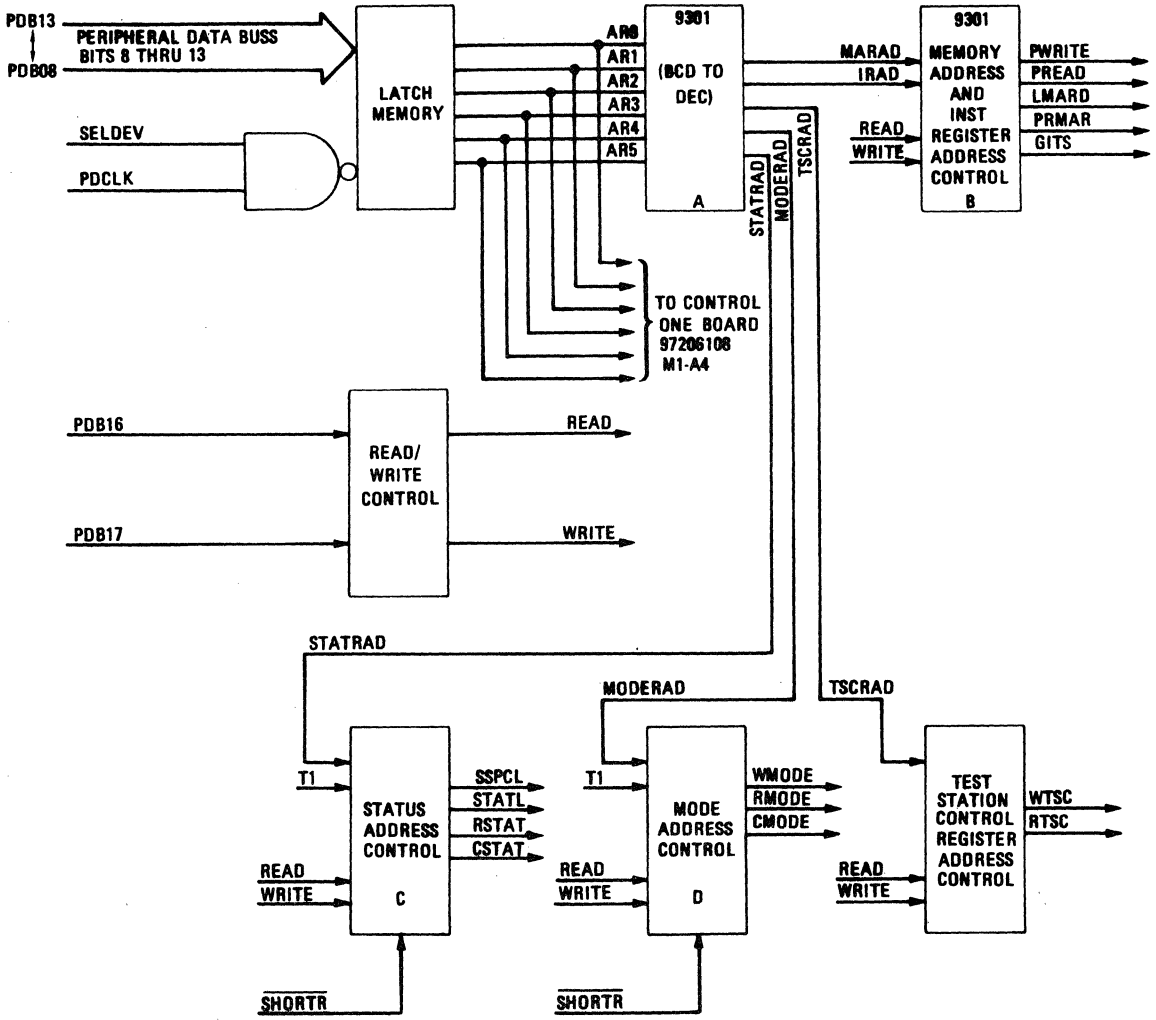


FIGURE 3-3. REGISTER ADDRESS SIMPLIFIED

the P data bus. The second group is comprised of the registers loaded from the data buffer output, which is the short-register data bus. These short registers store the programmed information which controls the digitally programmed supplies and reference voltage supplies, and are located on four quad 16 bit register boards. Each quad 16 bit register board contains four 12-bit registers.

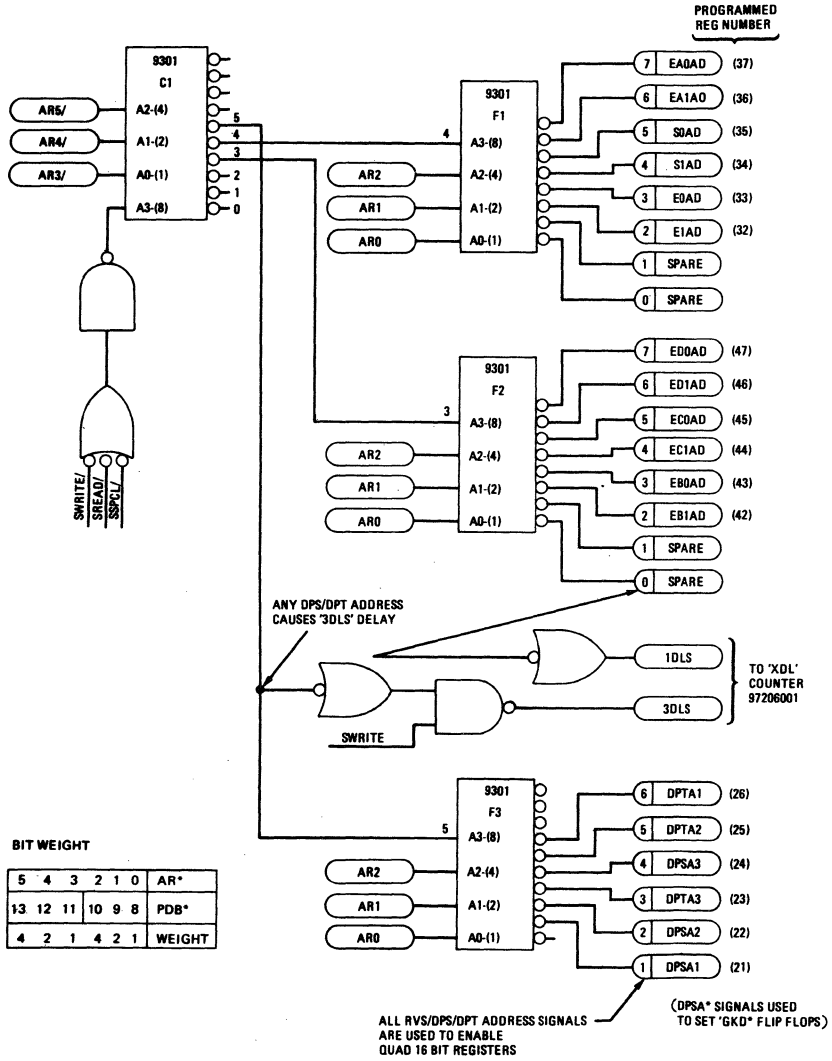
DPS and RVS Addressing The DPS and RVS address codes are generated on the control 1 board (Figure 3-4). For example, consider the DPS1 address code for register 21, refering to Figure 3-5 for the following discussion.

The 12-bit register used to control DPS1 is loaded in parallel with bits 0 through 11 (SRD0-SRD11) from the short-register data bus. The bits from the data bus are inverted and applied to the parallel inputs of the register, which is clocked when the address code and the necessary write signal, strobe signal, and clock pulse are ANDed together. The parallel enable input on the register is always grounded, or enabled. As soon as the data is loaded into the register, it is available at the output pins and wired directly to the DPS1 power supply board. The short register just loaded can be read back by generating the necessary read signal and the register address code. The stored information from the addressed register is then applied to the short register data bus. The information is then read into the computer via the data buffer, the peripheral data bus, and the computer CPI.

Data Buffer Interface Operation The signals RWRITE, PREAD, GSTI, and GITS are used to enable the data buffer to read and write between the P and the S data buses. These read/write control signals are generated from the register address as a result of correct register address codes, and the proper read/write bits (16 and 17) from the computer during the program run time.

Figure 3-6 is a simplified logic diagram of the data buffer board. It shows all the read/write control signals and two typical bits of the 24 bits processed by the data buffer. All 24 bits are processed by the data buffer in the same manner as the two depicted in the simplified logic diagram.

Long Register Loading and DMA Mode The outputs of the I register constitute the long-register data bus. Therefore, any information passing through the I register, to be loaded into a register in the test station module, is considered to be long-

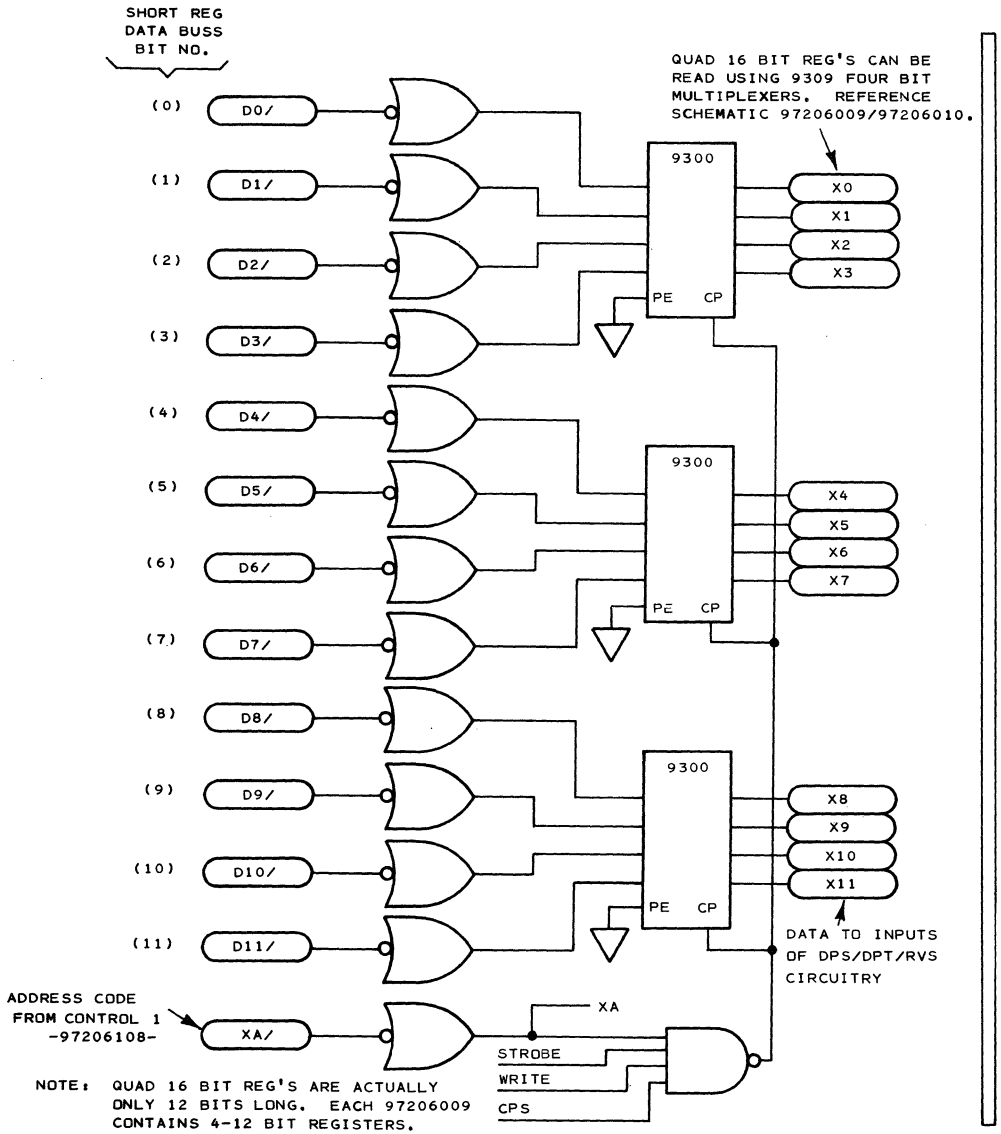


BIT WEIGHT

5	4	3	2	1	0	AR*
13	12	11	10	9	8	PDB*
4	2	1	4	2	1	WEIGHT

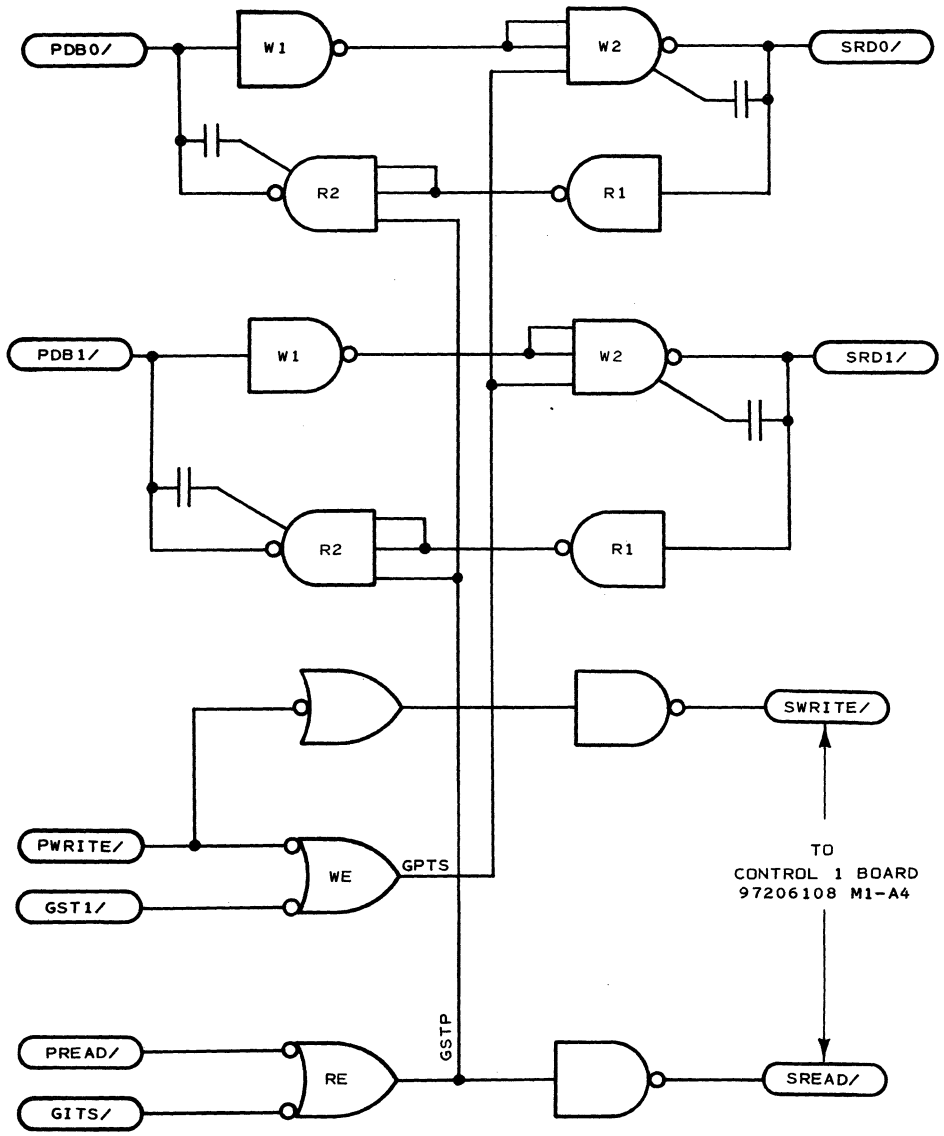
INPUT SIGNAL	DESCRIPTION
AR0	ADDRESS BIT ZERO SET BY PDB8
AR1	PDB9
AR2	PDB10
AR3/	PDB11
AR4/	PDB12
AR5/	PDB13
SREAD	SHORT REGISTER READ SIGNAL.
SSPCL	SHORT SPECIAL-ADDRESSING SIGNAL USED FOR SPECIAL FUNCTIONS.
SWRITE	SHORT REGISTER WRITE SIGNAL.

FIGURE 3-4. CONTROL 1 SIMPLIFIED



INPUT SIGNAL	DESCRIPTION
CPS	CLOCK PULSES GENERATED BY THE COMPUTER - (EVERY 350NS)
D0/	SHORT REG. DATA BUSS (BIT 0)
D1/	SHORT (BIT 1)
D2/	SHORT (BIT 2)
D3/	SHORT (BIT 3)
D4/	SHORT (BIT 4)
D5/	SHORT (BIT 5)
D6/	SHORT (BIT 6)
D7/	SHORT (BIT 7)
D8/	SHORT (BIT 8)
D9/	SHORT (BIT 9)
D10/	SHORT (BIT 10)
D11/	SHORT (BIT 11)
XA/	DECODED REG ADDRESS CODE BITS 8-13 OF SPU COMMAND.
STROBE	SIGNAL NAME ACTUALLY 'CPT1WS'. (CLOCK PULSE - T1-WRITE SHORT REG)
WRITE/	SWRITE/ FROM DATA BUFFER TO ALLOW WRITING TO SHORT REG. DATA BUSS.

FIGURE 3-5. QUAD 16 BIT REGISTER SIMPLIFIED



INPUT SIGNAL	DESCRIPTION
GITS/	GATE INSTRUCTION REG. TO SHORT REG. (READ ENABLE)
GSTI/	GATE SHORT REG. TO INSTRUCTION REG. (WRITE ENABLE)
PDB0/	PERIPHERAL DATA BUSS BIT ZERO
PDB1/	PERIPHERAL DATA BUSS BIT ONE
PWRITE/	PERIPHERAL WRITE (SPU OR 24 BIT FTW CONTAINING WRITE BITS)
PREAD/	PERIPHERAL READ

FIGURE 3-6. DATA BUFFER SIMPLIFIED

register data. Refer to Table 2-1 for a listing of the long registers.

The long registers may be loaded with data by either SPU or DMA instructions. An SPU instruction (Table 3-1) may be issued by the TOPSY controller to enable the tester CPI logic and address the I register. Once the I register is addressed, the data is loaded into it. The I register applies the 24-bit instruction to the long-register data bus. Once the long registers are enabled, the data is transferred from the I register to the addressed long registers. Once an instruction is resident in the addressed long registers, it may be executed. Separate SPU commands are necessary for each instruction. To reduce the execution time and increase the rate of testing, instructions to the long register are normally DMA instructions.

DMA Instructions Direct memory access (DMA), 24-bit instructions (Table 3-2) allow the software controller, TOPSY, to set aside the instructions intended for the long registers, and to group them into long-register data blocks. Once the grouping occurs, only the address of the location at which the group is stored is retained in the program. As the program is executed, under TOPSY control, the short-register instructions are loaded and executed using the SPU commands and normal addressing techniques. When a long-register instruction is decoded it causes TOPSY to configure the system logic to receive information directly from the memory and transfer it to the long registers. Bypassing the normal SPU commands and timing permits the execution of the long-register instructions at a very fast rate, at the same time freeing the computer for other duties.

The first step in initiating the DMA mode is for TOPSY to generate an SPU command to load the memory address register (MAR) with the address of the long register data block. The MAR is located in the tester common peripheral interface (CPI) logic, on the CPI 1 and CPI 2 boards.

TOPSY then clears the register address board, and loads the address of the status register with a second SPU command. The trap enable bit is written into the status register to enable the DMA mode to reset after the last long register instruction has been executed. Another SPU command is then issued, which changes the register address board's decoded address from the status register address to the mode register address. TOPSY then writes the DMA mode bit (bit 9) into the mode register. This action sets the DMA mode and transfers the long register loading control to the phase loop counter logic. The setting of the DMA bit on the mode register causes the phase loop counter to be set to phase one. The phase loop counter in turn generates a read

memory (RMEM) signal which allows the system to read long-register instructions directly from memory, under the timing control of the phase loop counter.

The phase loop counter sequentially fetches instructions from memory and loads them into the I register, where they are stored. The I register outputs the data to decoders, which decode the long-register address and rank code to enable the correct register. The address signals, along with the system clock, allow the data to be transferred to the master side of the addressed long register. After the last instruction necessary to perform a test is loaded into the master side of the addressed long register, the execute signal causes the information to be transferred to the slave side of the registers where it is immediately executed.

The phase loop counter fetches the next long-register instruction during the execution time of the previous instruction. The previous instruction, being executed, is then under the control of the execute delay loop counter. The phase loop counter fetches and loads the next long-register instruction into the master side of the register. Each register that is addressed is loaded, and as soon as the execute delay loop (XDL) counter has executed the previously loaded statement, the XDL counter turns control over to the phase loop counter until the next execute command is decoded. Then the XDL counter again assumes control and executes the statements just loaded. When the last instruction of a long-register data block is decoded, a trap condition will exist (the TOPSY controller will have previously generated the proper trap bits). This enables the system to reset the DMA mode of operation, after the last long-register instruction is decoded, loaded and executed.

3.2 DETAILED THEORY OF OPERATION

Refer to Figures 3-7. The left side of Figure 3-7 depicts the instruction (I) register which contains the storage elements for a single 24-bit data word used to control the test head pin functions. The instructions are transferred to the test station via the I register in the direct memory access (DMA) mode. The FACTOR statements, SET D, SET R, SET M, SET S, and SET F are applied individually to the I register. The control bits, I22 and I23, decode the functions write-and-hold, write-and-execute, read, or trap. These control bits are wired to the phase loop counter, which generates the necessary control signals to control the DMA flow of data to the test station. Bits 19 through 21 are decoded in the 120 bit decoder board (Figure 3-8), and initiate the required long-register enabling signals. Bits 15 through 18 are also decoded (15 bit decoder board of test station), and

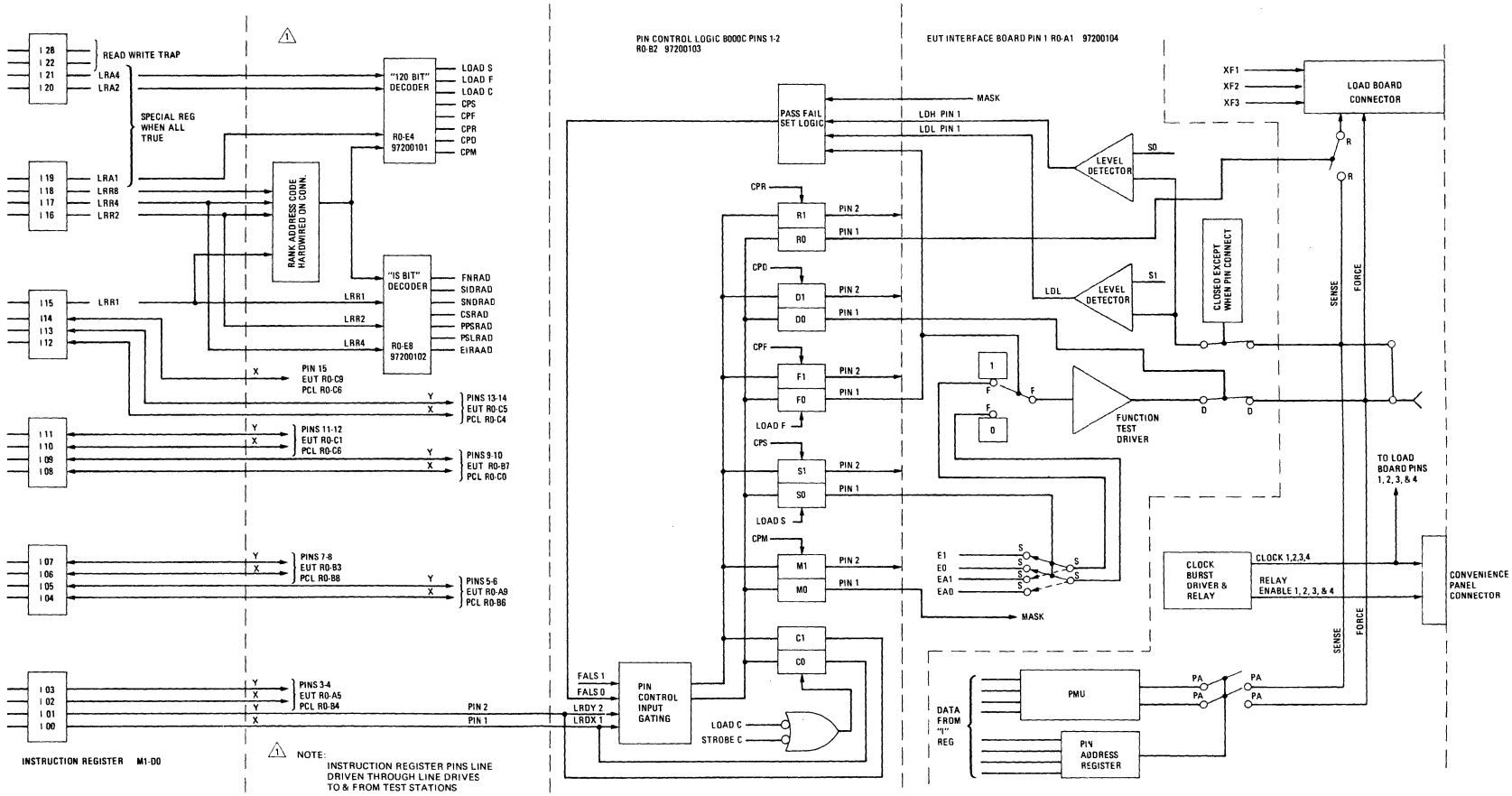


FIGURE 3-7. TEST STATION DETAILED BLOCK DIAGRAM, PIN 1 (TYPICAL)

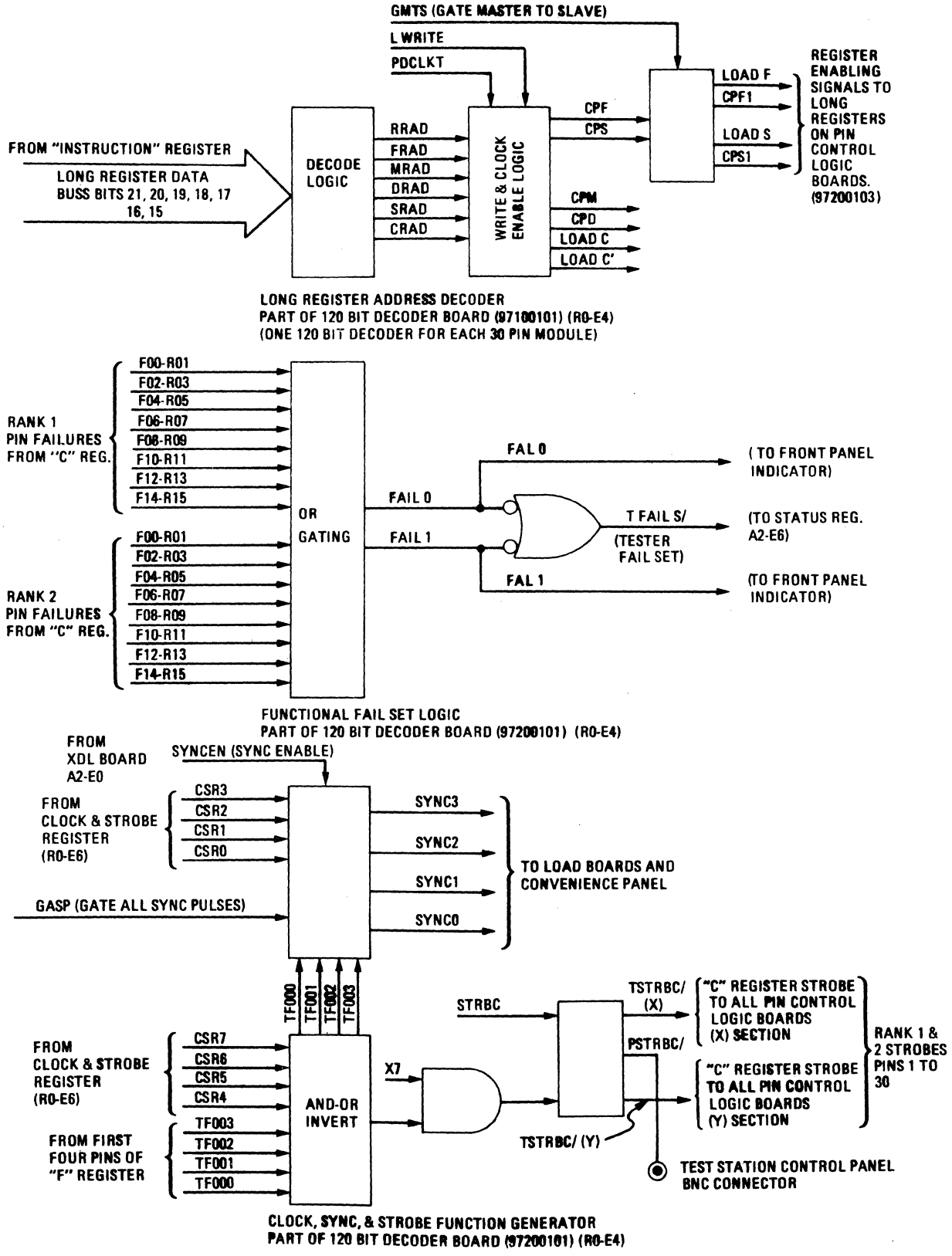


FIGURE 3-8. 120 BIT DECODER SIMPLIFIED DIAGRAM

provide the rank signals necessary to enable the correct rank of pins. The 60 test head pins are divided into four ranks (ranks 0 through 3) of 15 pins each. Data is loaded into the long registers on a rank-by-rank basis. The address of the rank to be loaded is determined by the 15 bit decoder board. Bits 0 through 14 are data bits. Each bit controls a function of one pin. Bit 0 corresponds to pin 1, bit 1 to pin 2, etc. If the decoded instruction in the I register is a set D instruction, the 15 bits of data (bits 0-14) are simultaneously loaded into all D registers of the addressed rank. The D registers, as in the case of all long registers, consist of a single flip-flop per pin of the test station. Each EUT (element under test) interface board controls two pins. If any bit in the D register is set true, that is, to a logical 1, the corresponding relay on an EUT interface board closes, connecting the function test driver to the force line of that pin. That makes the pin an input pin. The sense line (input to the level detector) is always connected, except when the PMU measuring circuit is programmed to that pin by the pin address register.

Input Pins . The D register defines input pins as pins which may be set to a logical 1 or 0. The F register selects the logic level to be driven to the unit under test. The F register is loaded with a set F instruction utilizing the 120 bit and the 15 bit decoder boards. The F register consists of a single flip-flop per pin. The 120 flip-flops of the F register are located on pin control boards, two per board except for every eighth board which has only one of the two flip-flops wired into the F register (since each rank has 15 pins, the sixteenth flip-flop in each group of eight pin control boards is not used). The pin control boards control the EUT interface boards. Each EUT interface board controls two pins on the test head. Setting any bit of the F register to a logical 1 forces the corresponding pin to a high level. Setting that bit to a logical 0 forces the pin to a low level.

Output Pins The D register defines output pins as a D register set of bits at a logical 0 level. When a pin is not defined as an input pin, it automatically becomes an output pin. The output pin connections from the test head sockets and load board connections are wired to the EUT interface boards, through an input relay controlled by the pin address register. This relay is normally closed, unless the PMU is programmed to that pin. The output pins are also wired to one of two inputs on the line detector modules location on the EUT interface board. The second input of the level detector modules has a dual reference power supply (RVS) applied to it. The RVS is programmed to provide an accurate logical 1 or 0 level. The output of the device under

test (DUT) is applied to the level detector module and compared to the programmed logic level of the RVS. The F register is utilized to specify whether a logical 1 or 0 level is expected on the output pin. When set to a logical 1, a bit in the F register specifies an expected logical 1 level output from the corresponding DUT pin; when set to a logical 0, that bit specifies an expected logical 0 from the DUT pin. The S0 and S1 RVS's are used as the expected output level references and are selected by the F register bit function. The outputs of the level detectors are applied to decision making logic and to the C register.

Tester Strobe The tester strobe is generated in the mainframe by the execute delay loop (XDL) board. The strobe signal is generated during the execution of SET F instructions. The strobe is used as a clock pulse for the C register elements. The strobe may be delayed by programming.

Digitally Programmed Supplies (DPS) The DPS's are multiplexed to the test station and are used as Vcc, Vbb, Vee, and bias supplies. The DPS's are not programmable to a pin, but are connected to the DUT pin by jumper wires on the test station load board. The utility relay, located on the EUT interface board may be used to switch the DPS during the test program.

Clock Burst Counter The clock burst generator is a signal gating circuit located on the 120 bit decoder board. A series, or pattern, of four clock pulses may be programmed by utilization of the clock and strobe (CS) register located in the test station. The outputs of the clock register are gated with the tester strobe signal to generate sync signals. The sync signals are then imposed on the first four pins (1-4) of the test station and used for device clock pulses. Additional wiring may be required to properly connect the test socket to the DUT.

Test Station Control Panel The test station control panel (Figure 3-9) contains the START (automatic mode), the MAN (manual mode), the ADV (manual-mode advance), and the RESET (test station reset) pushbuttons. It also contains an ON LINE indicator, that lights when the test station is selected by the multiplex unit, and an EOT indicator that lights when a FACTOR program END statement is decoded. In addition, the panel contains indicators, readouts, register selector pushbuttons, and status indicators described in the following paragraphs.

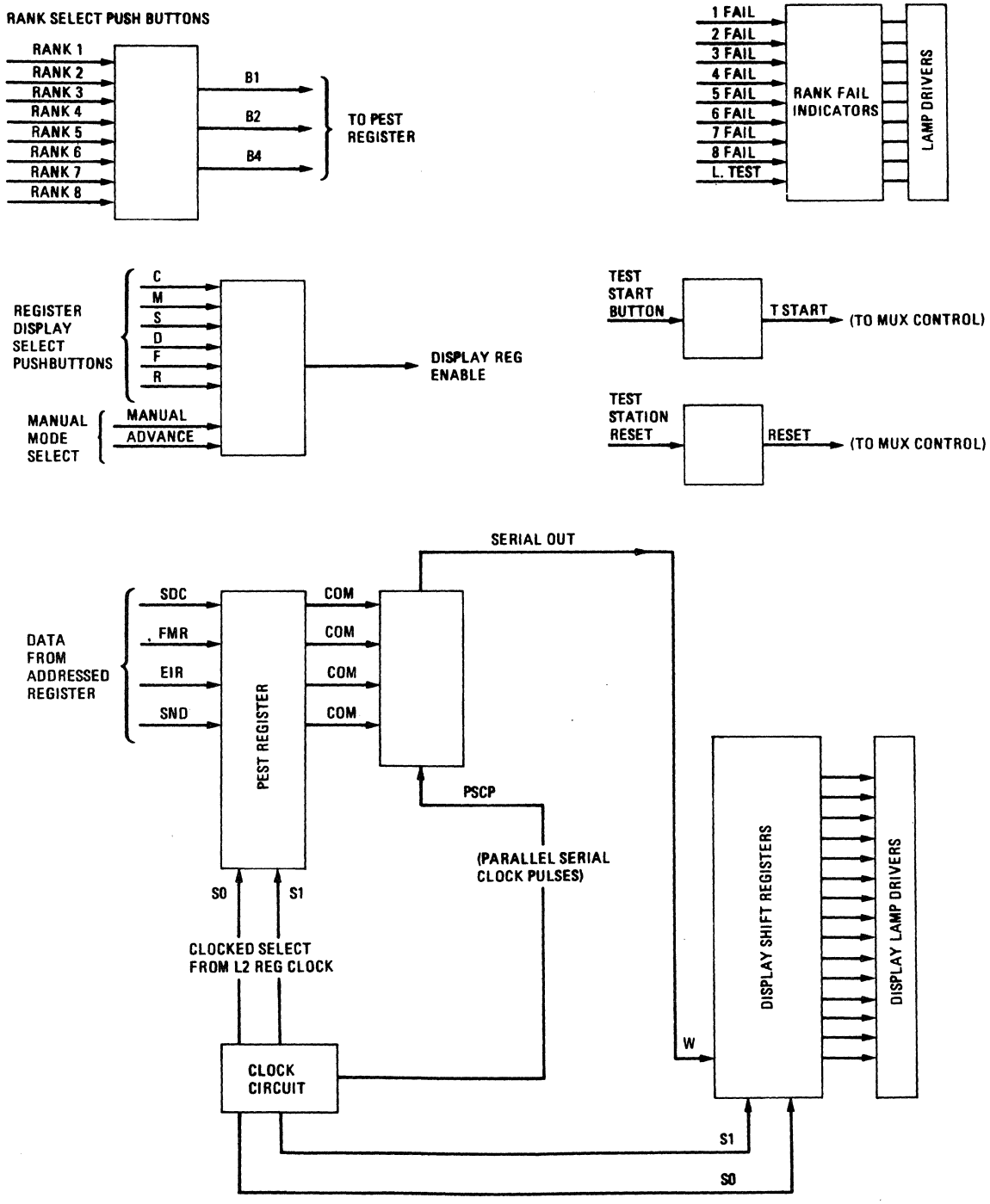


FIGURE 3-9. TEST STATION CONTROL PANEL LOGIC DIAGRAM

Rank Fail Indicators The RANK FAIL Indicators light whenever a functional test failure occurs. A specific indicator lights for the rank in which the failure occurred. The corresponding RANK SELECTOR pushbutton (located directly below the lighted indicator) may then be pressed to select that 15-bit slice of the C register (pass-fail data) for display to determine on which pin of the DUT a functional failure occurred. The procedure to display the information is described in the following paragraph. To perform this rank-and-pin failure determination procedure, the test station must be in manual mode.

Long Register Data Display In the manual test mode, the contents of the long registers may be displayed on the test station control panel, 15 bits at a time. First the desired RANK SELECTOR pushbutton is pressed to select a 15-bit slice of a long register (corresponding to a rank of 15 pins); then the desired REGISTER SELECTOR pushbutton (or two of them) are pressed to select the applicable long register(s). The lamps to the right of the pushbuttons will then indicate the logic level state of each flip-flop of the selected 15-bit slice of the selected long register(s). Only two long registers may have a 15-bit slice displayed at any one time. The upper set of indicators can display the selected slice of the S, the D, or the C register. At the same time, the lower set can display the selected slice of the F, the M, or the R register.

External Interface Register (EIR) Display The external interface register outputs are monitored on the 10-lamp EXTERNAL REGISTER display on the test station control panel to give category information, if programmed in the test sequence. This permits the categorization of devices or units into several pass or fail categories.

Statement Number Readout A STATEMENT NUMBER readout (neon tubes) displays the number of the FACTOR program statement being executed. In the automatic test mode the readout is not updated until the end of the test program. In manual test mode it is updated after each statement is executed.

Pass/Fail Indicators The test station control panel also contains four pass/fail indicators, located on either side of the EOT indicator. To the left are the FUNCTIONAL TEST PASS and the FUNCTIONAL TEST FAIL indicators; to the right are the PARAMETER TEST PASS and the PARAMETER TEST FAIL indicators.

3.2.1 SPU MODE

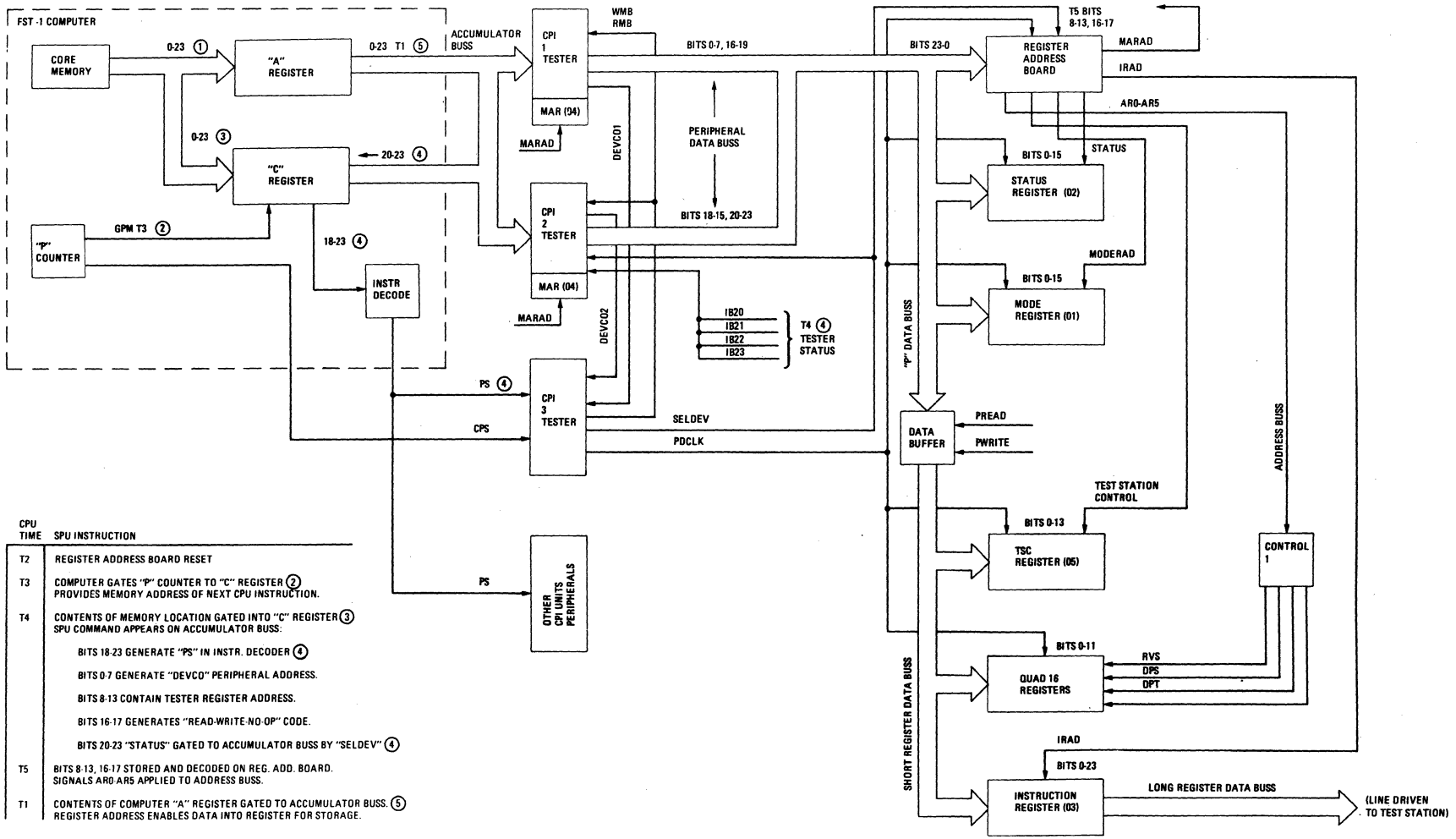
Registers connected to the peripheral data bus or to the short-register data bus are programmed by SPU instructions. For example, the status register, the mode register, the register address board, the test station control register, the instruction register, and the quad 16 bit register board are programmed by SPU instructions.

Each SPU instruction is performed within a single computer cycle. The computer cycle consists of five phases -- T2, T3, T4, T5, and T1. The computer cycle is considered to start at T2 and to proceed through T3, T4, T5, and T1. At the completion of a cycle at T1, the next cycle starts at T2.

Typical SPU Instruction The operation of the tester during the SPU instruction cycle is best described by considering a typical SPU instruction sequence (Figure 3-10). A typical SPU read instruction format is given in Table 3-3.

The first SPU instruction in a standard TOPSY program is normally one to read out of the TSC register, which allows the computer to check whether or not the tester is available. If the tester is available, the next SPU instruction is normally one to write into the TSC register to select the multiplex logic and associated relays required to connect the mainframe to the test station. Next, the desired RVS and DPS control registers are selected. Following this the MAR's in the CPI 1 and CPI 2 boards are selected to enable loading of the DMA location. Then the instruction register is enabled, in order to transfer DMA instructions to the long registers. The status and the mode registers are addressed, in case of interrupts. For DMA operations, the trap enable bit must be loaded into the mode register. The functions of the instruction register, the mode register, the status register, the MAR, and the XDL counter are described in greater detail in the DMA instruction timing discussion which follows this SPU timing discussion. The timing for all SPU instructions is similar to that for the typical read TSC and write TSC instructions which are described in the following paragraphs.

Read TSC (06602520B) The computer, under TOPSY monitor control, continually checks the status of the tester, for a start request signal. For example, when the START pushbutton on the test station control panel is pressed, a test start signal is generated on the L2 test station control panel and applied to the multiplex control board, setting a flip-flop in the test station control register. This flip-flop remains set until read by the



CPU TIME	SPU INSTRUCTION
T2	REGISTER ADDRESS BOARD RESET
T3	COMPUTER GATES "P" COUNTER TO "C" REGISTER ② PROVIDES MEMORY ADDRESS OF NEXT CPU INSTRUCTION.
T4	CONTENTS OF MEMORY LOCATION GATED INTO "C" REGISTER ③ SPU COMMAND APPEARS ON ACCUMULATOR BUSS: BITS 18-23 GENERATE "PS" IN INSTR. DECODER ④ BITS 0-7 GENERATE "DEVCO" PERIPHERAL ADDRESS. BITS 8-13 CONTAIN TESTER REGISTER ADDRESS. BITS 16-17 GENERATES "READ-WRITE-NO-OP" CODE. BITS 20-23 "STATUS" GATED TO ACCUMULATOR BUSS BY "SELDEV" ④
T5	BITS 8-13, 16-17 STORED AND DECODED ON REG. ADD. BOARD. SIGNALS AR0-AR5 APPLIED TO ADDRESS BUSS.
T1	CONTENTS OF COMPUTER "A" REGISTER GATED TO ACCUMULATOR BUSS. ⑤ REGISTER ADDRESS ENABLES DATA INTO REGISTER FOR STORAGE.

FIGURE 3-10. SPU INSTRUCTION LOGIC

TABLE 3-3. TYPICAL SPU READ INSTRUCTION

COMPUTER CONTROL PANEL	OCTAL VALUE CPU CTL PANEL	0			6			6			0			2			5			2			0		
	BIT WEIGHT CPU CTL PANEL	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1
	BIT NO.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BINARY		0	0	0	1	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
TESTER LOGIC	BIT NO.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BIT WEIGHT, TESTER LOGIC	4	2	1	4	2	1	4	2	1	X	4	2	1	4	2	1	2	1	4	2	1	4	2	1
	OCTAL VALUE, TESTER LOGIC	0			6			6			X	0			5			1			2			0	
	SPU INSTRUCTION GROUPING	OP CODE						FTCN			TESTER REG.							UNIT ADDRESS								
	TYPICAL SPU INSTRUCTION TO TESTER	SPU						READ			TSC							TESTER								

computer under TOPSY monitor control. The read TSC instruction sequence is described in the following steps:

1. At time T2 (computer phase time T2), the register address board is reset (Figure 3-10). With the register address board reset, it is ready for the next SPU instruction.

2. At time T3, a gate memory to computer P counter (GPM) signal occurs, gating the computer P counter to the computer C register to provide the core memory address for the next computer (CPU) instruction.

3. At time T4 the contents of the computer C register are gated to the accumulator bus (BN bus). Bits 18-23 are decoded by the instruction decode circuitry and generate the peripheral select (PS) signal.

   a. The PS signal is applied to all peripheral CPI units. However, 120B bits 0 through 7 code is only acceptable to the tester CPI. Tester CPI 1 and CPI 2 boards decode the 120B address bits 0 through 7 to generate signal device code 1 (DEVCO 1) and signal device code 2 (DEVCO 2), respectively. The DEVCO 1 signal is ANDed with the PS signal on the CPI 3 board to generate select device (SELDEV).

   b. If there is no higher priority pending, the SELDEV signal is applied to the CPI 1 and CPI 2 boards where it gates the peripheral status from the P data bus to the accumulator bus. The peripheral status is determined from the IB16, IB17, IB18, and IB19 signals, which are gated into the bit 20 through 23 positions, respectively, of the accumulator bus. At this time, the computer monitors these bit positions on the accumulator to check whether or not the tester is available.

   c. The SELDEV signal is used by the CPI 3 board to generate WBP (write to peripheral bus) or WBNB (write to BN bus). The signals WBP and WBNB enable the transfer of data through the CPI 1 and CPI 2 boards in either of two directions, to the P buss, or to the BN bus, respectively. The SELDEV signal is connected by permanent jumper wires to the CPI 2 board, where it gates signals IB16, IB17, IB18, and IB19 into the bit 20 through 23 positions on the accumulator (BN) bus. The IB16 through IB19 signals, applied to the bit 20 through 23 positions of the BN bus, contain the status of the tester peripheral. Bit 20 is signal VCCT, a power monitor signal from the monitor control panel

circuitry. If signal VCCT is untrue, power has been lost, and therefore the BE (bit equal) indicator on the computer control panel lights, indicating that the tester peripheral is not available. Bit 21 corresponds to signal DMA (direct memory access) from the mode register. The DMA signal is connected by permanent jumper wires to the CPI 2 board. When the DMA signal is true, it indicates that the tester is busy or in use by lighting the LT (less than) indicator on the computer control panel. Bit 22 is a signal from the status register called IREQ (interrupt request). When this bit is true, it indicates that an interrupt is awaiting service. This interrupt action (bit 22 true) lights EQ (equal) indicator. Bit 23 is set by the TSBY (tester busy) signal generated as a result of a fixed time delay on the execute delay loop counter (XDL board). When the TSBY signal is untrue, the tester peripheral is ready for service or in the idle state. Also, during computer time T4, signal SELDEV is applied to the register address board, where it gates bits 8 through 13, 16, and 17 to the inputs of the address storage elements.

d. By the completion of time T4, the SPU instruction has accomplished the following:

   1) Selected the tester peripheral (bits 0-7)

   2) Generated peripheral select signal PS (bits 8-23)

   3) Read status of tester peripheral (bits 20-23)

   4) Applied tester register address information to inputs of register address board (bits 8-13, 16, and 17)

   5) Enabled BN bus to P bus or P bus to BN bus using SELDEV signal.

4. At time T5 the computer generates another CPS signal. (The CPS signal is generated once each phase time.) The CPS signal is wired to the CPI 3 board and generates the PDCLK (peripheral data clock) signal. The PDCLK signal is generated at T5 only if the tester was determined to be available by the computer when it read tester status on bits 20 through 23 at time T4. If the tester is available at time T5, the PDCLK signal is applied to the register address, enabling bits 8 through 13, 16, and 17 to be stored and decoded. The AR0 through AR5 signals generated by the

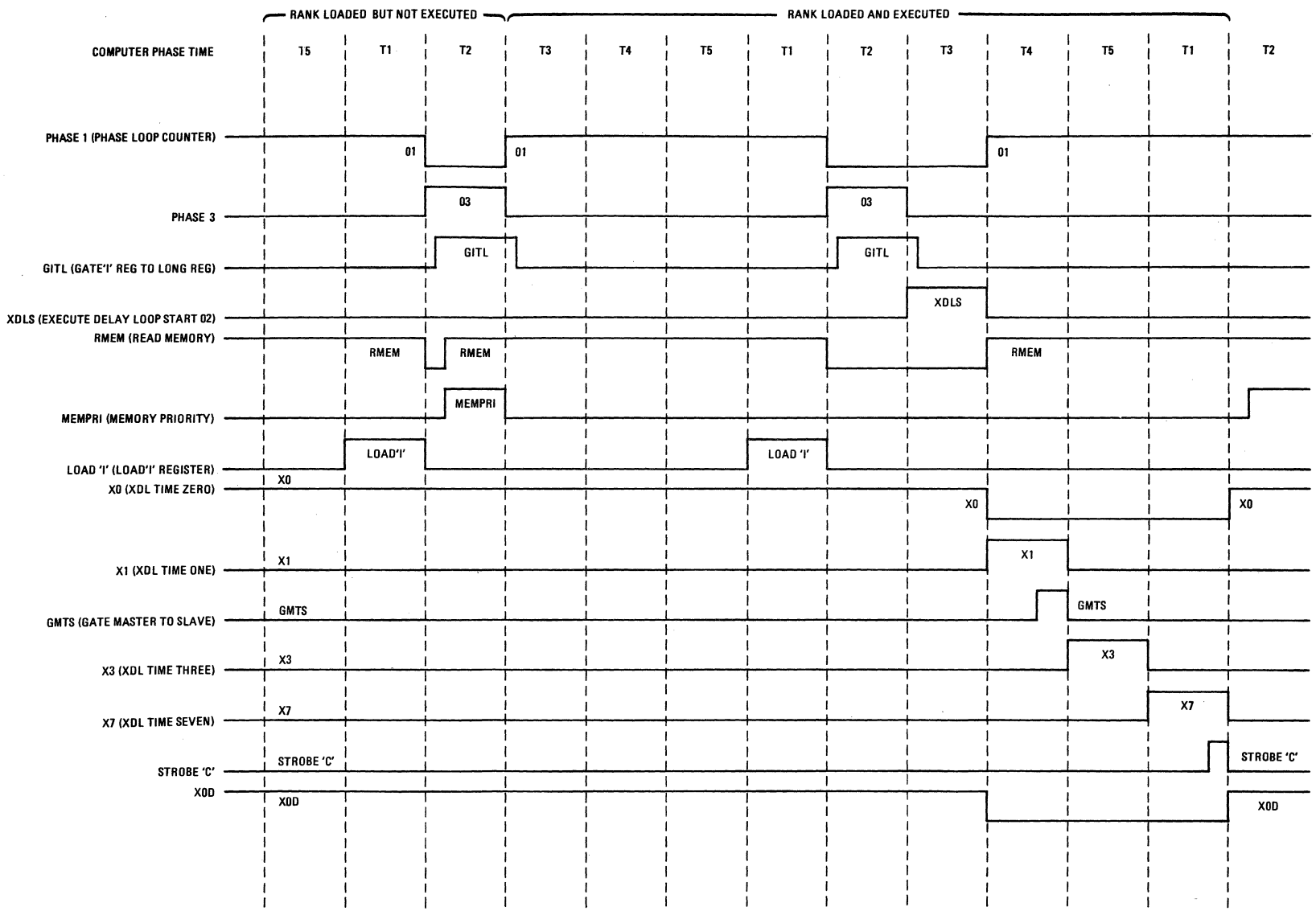


FIGURE 3-11. SPU INSTRUCTION TIMING

FAIRCHILD SYSTEMS TECHNOLOGY

register address board form the desired address pattern to enable the selected quad 16 bit register board or the applicable enabling signal from the register address board which is applied to the TSC, the I, the mode, the status, or the memory address register. After the desired short register is enabled at T5, it is ready to transmit or receive data at the ensuing phase time, T1. In this example the TSC register is enabled to transmit data (to be read by the computer).

5. At time T1, another PDCLK clock signal is generated. At time T1, for this example, the 13 bits of data in the enabled TSC register are clocked onto the short-register data bus, through the data buffer, onto the P data bus, through the CPI 1 and CPI 2 boards, onto the accumulator bus, and into the A register. If this SPU instruction was a write instruction, then at T1 the PDCLK signal clocks the data into the addressed register. This data in the A register during a write instruction is the 24 bits of information which had been stored during a previous computer cycle in the A register. At time T1, this data is gated from the A register onto the BN bus, through the CPI 1 and CPI 2 boards, onto the P data bus, and into the enabled tester short register.

Write TSC (06402520B) The TOPSY monitor must next address the TSC register in a write mode to enable the multiplex control board to generate the signals required to connect the digital and the analog multiplex buses to the test station. The write TSC instruction is the same as the read TSC instruction except that bit 16 is now true. The instruction sequence is described in the following steps:

1. Time T2. Same as for read TSC.

2. Time T3. Same as for read TSC.

3. Time T4. Same as for read TSC.

4. Time T5. Same as for read TSC, except in this example the TSC register is enabled to receive (to be written into by the computer).

5. Time T1. At time T1, another PDCLK signal is generated. This PDCLK signal clocks the data into the addressed register. This data consists of the 24 bits of information which had been stored during a previous computer cycle in the A register. At time T1, this data is gated from the A register on to the accumulator bus, through the CPI 1 and

TABLE 3-4. TYPICAL SPU WRITE INSTRUCTION

COMPUTER CONTROL PANEL	OCTAL VALUE CPU CTL PANEL	0			6			4			1			0			5			2			0		
	BIT WEIGHT CPU CTL PANEL	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1
	BIT NO.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BINARY		0	0	0	1	1	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0
TESTER LOGIC	BIT NO.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BIT WEIGHT, TESTER LOGIC	4	2	1	4	2	1	4	2	1	X	4	2	1	4	2	1	2	1	4	2	1	4	2	1
	OCTAL VALUE, TESTER LOGIC	0			6			4			X	2			1			1			2			0	
	SPU INSTRUCTION GROUPING	OP CODE						FTCN			TESTER REG.							UNIT ADDRESS							
	TYPICAL SPU INSTRUCTION TO TESTER	SPU						WRITE			DPS1							TESTER							

CPI 2 boards, onto the P data bus, and into the enabled tester short register. For the next SPU write instruction, which is started at time T2, the entire sequence previously described for an SPU instruction is repeated. Before an SPU write instruction is stored in the C register, a 24-bit data word must be fetched and stored in the A register. This fetch operation requires a complete T2, T3, T4, T5, T1 computer cycle. Once the desired data instruction is stored in the A register, another SPU write instruction may be executed in the same manner as previously described. An SPU read instruction does not require prior storage of a data word in the A register. Of course, the A register must be available for storing the data read at time T1, depending on the particular computer programming. In this example, bits 16 and 17 of the write instruction, along with the TSC register address, initiate a write TSC register (WTSC/) signal which enables the test head enable information contained in short-register data bus bits 0 and 1 to be clocked into dual flip-flop B2 (at CPU time T1). The output information is encoded to create test head enable station 4 signal (THEN4) to connect the mainframe multiplex to the test station.

Write DPS1 (06410520B) With the test station connected to the mainframe as a result of the write TSC instruction described in the previous paragraph, the tester is now ready for the programming of the RVS and DPS supplies described in the following steps:

1. The WTSC/ signal from the register address board is also used on the multiplex control board to set flip-flop C1 (type 9000 J-K flip-flop), which generates an STRS/ (start set) signal. This signal is generated at the T1 PDCLK time which is when the THEN4 signal was generated. (CPU time T1.)

2. The STRS/ signal is sent to the status register where it resets flip-flop E6, generating signal STP/ (stop) and STR (start). Signal STR (start) is sent to the phase loop counter to control phase timing.

3. Following the test head addressing and enabling signals during CPU times T5 and T1, the TOPSY program then locates the test program and prepares to load and execute. During computer time T2 the register address board is cleared. The next instruction to be sent to the tester is then resident in the C register of the computer. The TOPSY monitor scans the instruction, interpreting the coding and preparing to transfer it to the tester.

4. Once the test station multiplex has been enabled, and the necessary relays, line drivers and line receivers have connected the test station to the mainframe and to the computer control, normal testing can continue under TOPSY control. Typically, in any FACTOR program, there are statements used to control analog power supplies, which are used to provide input reference voltage levels for a logical 0 and a logical 1, and biasing and Vcc voltages for the DUT test. The analog supplies, digitally programmed power supplies, and their associated current trip points, are programmed using SPU commands. A typical method of loading information into one of the power supplies is as follows: Assume that the statement, FORCE VF1 to 5V in Range 2, was one of the first statements in a typical FACTOR program, and this information is intended to cause DPS1 to go to a 5-volt logic level signal at some specific current level.

5. If the next instruction is not a long register (D, M, F, S, C, or R) instruction, another SPU command must be issued to address the register to which the data is to be transferred. This non-DMA mode of operation does not require the use of the I register. If the instruction (Example: FORCE VF1 500E-2) is intended for a register which is accessed from the short-register data bus, the SPU command generated by the TOPSY monitor will include the unit address of the Tester (120B), and the address of the VF1 supply register which is to be loaded with data.

6. An example of an SPU command used to address the tester and the DPS1 to load data into the DPS1 register is given in Table 3-4. An SPU command addressing the tester (120B), then a DPS (21B) transfers the information from the accumulator bus to the P data bus, through the CPI 1 and CPI 2 boards, and then to the short-register data bus via the data buffer board. The DPS is loaded from a single Quad 16 bit register board. The address of the DPS is generated on the control 1 board. The DPS receives 12 bits of information in parallel from the short-register data bus. The DPS is energized as soon as the Quad 16 bit register board completes the loading operation. All short registers are loaded in the non-DMA mode by an individual SPU command.

SPU Instruction to MAR The computer software issues an SPU instruction to address the memory address register (MAR) located on the CPI 1 and the CPI 2 boards. Once addressed, the memory address of the long-register data block is loaded into the MAR. This provides a local memory location counter and storage element for the phase loop counter.

SPU Instruction to Status Register. During the next computer cycle time, another SPU instruction is issued and decoded, addressing the status register. During time T1 of this SPU command, bit 4 of the status register is set. Bit 4 is the trap enable bit for the tester. During the program run time, the trap bits are inserted into the last long register instruction of the current long-register data block. When the last instruction is executed, the trap bits (I23-I22) are decoded and gated with bit 4 (the trap enable bit of the status register) to generate an interrupt. This interrupt initiates a reset of the DMA oepration.

SPU Instruction to Mode Register. A third SPU instruction issued by the computer addresses the mode register, and at time T1 the data instruction sets bit 9 of the mode register. Bit 9 is the DMA mode bit that enables the system to be controlled by the phase loop counter and XDL counter.

3.2.2 DMA MODE

Data is transferred to the long registers during a test sequence by means of direct memory access (DMA). The programmed information destined for the test station long registers is set aside in memory as a long-register data block. The starting memory address of the data block is retained in the actual program. Statements which set F, R, M, D, S, and C registers are the infromation words programmed for DMA operations. During DMA operation the tester is controlled by the phase loop counter and the execute delay loop (XDL) counter. The computer is then released to perform other duties such as datalog, process error or failure information, and monitor system and peripheral status. Prior to entering the DMA mode the computer must issue several SPU commands to configure the system for direct memory access operation, which is the tester's fastest operating mode. Typical SPU instructions were discussed previously in SPU Mode.

3.2.2.1 DMA Sequence

Execution of the DMA instruction sequence is carried out under the control of the Phase Loop Counter. In all, the Phase Loop Counter has the functions of controlling the transfer of information from the Instruction Register to the long registers, and, with the CPI, controlling the DMA transfer from memory to the Instruction Register.

During the following discussion, the reader may refer to the Phase Loop Counter A schematic, drawing number 97340805-04.

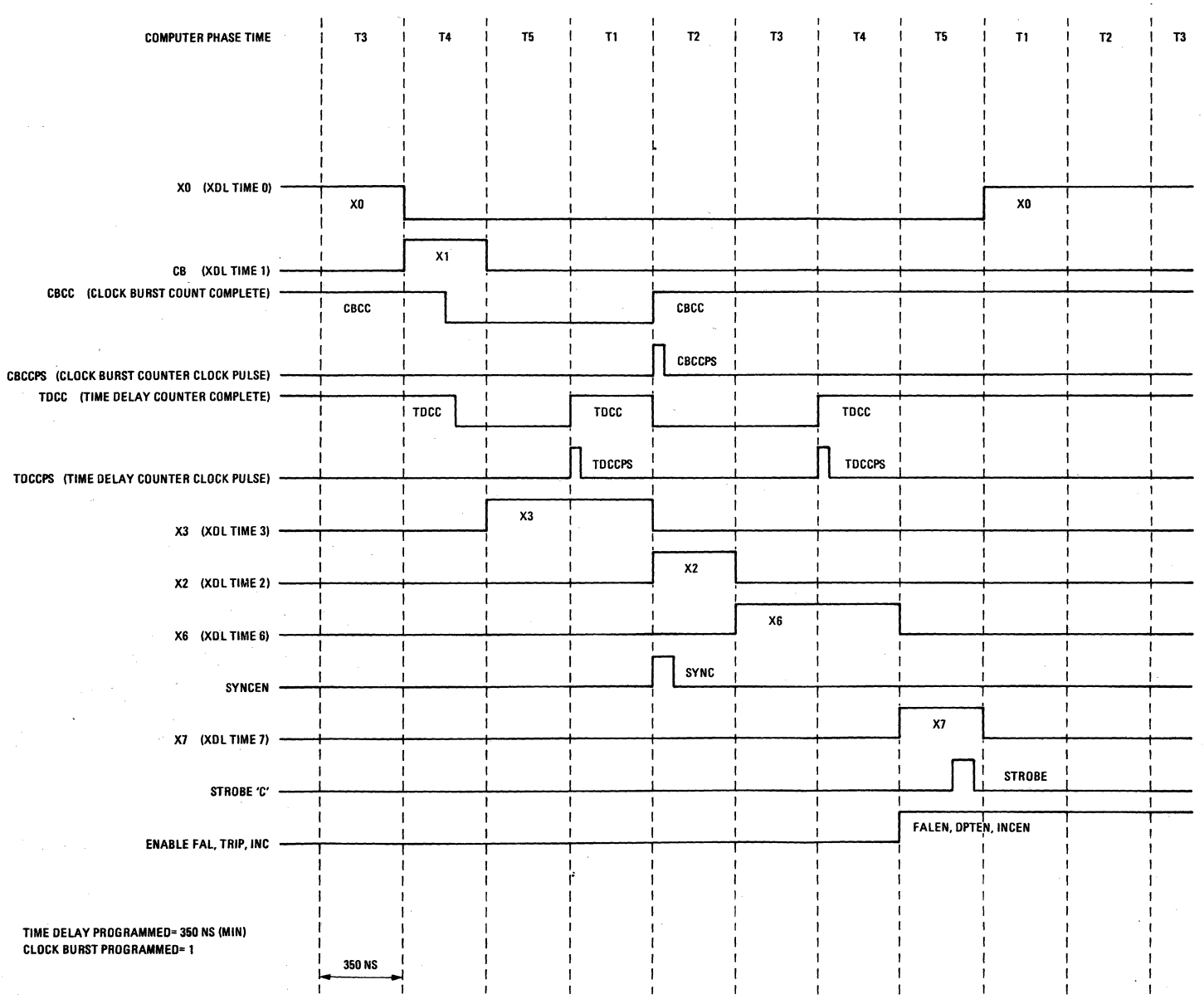


FIGURE 3-12. DMA TIMING TIME DELAY AND CLOCKBURST

FAIRCHILD
SYSTEMS TECHNOLOGY

Table 3-5 relates the internal signal names used here to the generating gate or flip-flop location.

The Phase Loop Counter consists of three flip-flops named PH01, PH02 and PH04. The eight states are decoded and named PHS0 through PHS7 (PHS4 is not used). The counter has several possible sequences depending on the long register address, the command held in bits I23 and I22 of the Instruction Register, the FTS and DMA bits of the Mode Register, the STR, FTINT and IREQ signals generated by the Status Register, and the DLY and X0 signals generated in the XDL counter. In all, there are five conditions of interest, leading to four count sequences. The count transitions common to the five sequences will be discussed first, then the conditional transitions.

Common Transitions PHS0 is the off state, during which no DMA transfers are made. Transition from PHS0 to PHS1 occurs when the condition STR DMA IREQ/ FTS/ is true, where STR is the Status Register start bit, DMA is the Mode Register DMA control bit, IREQ/ is a signal indicating that no tester interrupts are pending, and FTS/ is the Mode Register Function Test Suspended bit. (Another transition from PHS0 to PHS2 with FTS is implemented, but no longer used. This will be discussed later for the sake of completeness.) PHS1 is held until the CPI indicates that memory access is granted, MACG, at time T1. At that time, a word from memory is written into the Instruction Register and PHS3 is entered. Exit from PHS3 depends on I23, I22, and whether long register F is addressed.

Read or Trap Read or Trap commands are identified by I23. If I23 is true, the TRP bit of the Status Register is set by the signal TRPS (during PHS3) and PHS2 is entered. PHS2 is held until the XDL counter indicates that a previous function test is completed. When the X0 state of the XDL counter occurs, the flip-flop XOD is set, giving a one clock period delay, which allows time for a function test failure to generate the function test interrupt request FTINT. If FTINT/ is true (no function test failure occurred), and XOD is true, DMA is reset by DMARB and PHS7 is entered. The transistion from PHS7 occurs immediately and is to PHS0. If the signal FTINT is true with XOD in PHS2, DMA is reset by PHS2B and PHS0 is entered. This transition is independent of any other conditions.

Write to F Register If the word held in the Instruction Register contains a write and hold command, indicated by I23/ I22/, to the F register, the latch GITL is set and the signal LWRITE is generated during PHS3. The transition from PHS3 is to

PHS1, when GITL is reset. GITL gates the contents of the Instruction Register to the long register data bus; LWRITE controls the transfer from the long register data bus to the long register addressed.

If the Instruction Register holds a write and execute (I23/ I22) to the F register, GITL is set and LWRITE is generated as above, but the transition from PHS3 is to PHS2. Again PHS2 is held until XOD becomes true. If FTINT/ is true at that time PHS1 is entered and the signal XDLS, which starts the XDL counter, is generated. Note that function test patterns are loaded into the F register master while a function test previously loaded is being executed. This is possible because the F and S registers are master-slave types. This feature not only speeds testing, but simplifies control of the test rate.

Write to non-F Registers During a write and hold to any long register other than F, PHS2 is entered from PHS3. When XOD and FTINT/ are true, GITL is set, LWRITE is generated, and PHS1 is entered. PHS1 again resets GITL.

Write and execute to a non-F long register is similar to write and hold, except that the transition from PHS2 is to PHS6. PHS6 initiates hardware delays, depending on the register addressed (see below), and resets GITL. The transition from PHS6 is to PHS5 and is unconditional. PHS5 is held until the signal DLY/ becomes true, indicating that the hardware delays have timed out. If FTINT/ is true at that time, PHS1 is entered. If FTINT is true, PHS7 is entered, DMA is reset by DMARA, then PHS0 is entered. (The transition from PHS7 to PHS0 is conditional on XOD. PHS7, however, cannot be entered unless XOD is true.)

PHS6 may initiate one of three delays, depending on the register addressed. The signal .5DLS is generated and starts a 280 usecond delay, if the S register is addressed. Another signal, 1DLS, is generated and starts a 560 usecond delay, if the D, R, PA, SID, PPS, PSL, EIR, STSC, or DCT registers are addressed. If the PPS or PSL registers are addressed, the signal TDCR is generated along with 1DLS. TDCR starts the programmed DC delay.

CPI Control The Phase Loop Counter A board generates the signal RMEM which requests the CPI to perform a DMA read. RMEM is reset the following T1 time if DMA/ is true, or if MACG is true and the word read from memory is anything other than write and hold to the F register. RMEM thus allows a continuous DMA transfer when loading the master side of the F register, but forces a DMA interruption of at least one memory cycle in any other case.

Miscellaneous Functions. A number of miscellaneous functions are implemented on the Phase Loop Counter A board providing the means of controlling non-DMA data transfers to the long registers, and generation of the signals CLRI (clear the Instruction Register) and GMTS (gate-master-to-slave for the two master-slave long registers, F and S).

When an SPU write to the I register instruction is executed, two signals, EIC and EIC1, are generated on the Register Address board. EIC occurs immediately after the Instruction Register write, EIC1 occurs one clock period later. Both are one clock period wide. On the Phase Loop Counter A board, EIC sets GITL and EIC1 generates LWRITE. EIC1 will generate 1DLS if the Instruction Register holds a write and execute to any of the registers associated with 1DLS in the DMA mode. EIC1 is delayed one clock period by the flip-flop GITLR, which resets the GITL latch.

GMTS is generated by GITLR if the Instruction Register holds a write and execute command, or by the X1 state of the XDL counter, or by PHS6 if the S register is addressed.

The Instruction Register is cleared with CLRI by the clock pulse that occurs during T1 time if the signal MACG is false, indicating that no memory access has been granted.

Function Test Suspended Tester expansion and development has obsoleted the Function Test Suspended function, which is now performed by system software. It is, however, implemented in the Phase Loop Counter A board and is discussed below.

As mentioned earlier, the master of the F register may be reloaded while the function defined by the F register slave is tested. Thus the F master register holds the function test following the current test at the time a failure is detected. If this condition occurs, the signal FTSS is generated and sets the FTS bit of the Mode Register. FTSS is generated at PHS2 time, if FTINT, and XOD are true, and if the Instruction Register holds a write to the F register command.

The transition from PHS0 is to PHS1 if the condition STR DMA IREQ/ FTS is true. During PHS2 the XDL counter is started, then PHS1 is entered. State X1 of the XDL counter resets FTS if STR, DMA, and IREQ/ are true. If FTS is true the transitions from PHS0 to PHS2 to PHS1 are forced and not dependent on the contents of the Instruction Register.

TABLE 3-5

Name	Package-Pin	Schematic Page-Area	
CLR1/	A1-8	2	B-1
DMARA/	F5-12	1	A-3
DMARB/	C3-11	2	C-2
FTSR/	D8-8	2	A-2
FTSS/	D5-8	1	A-2
GITL	C5-8	1	A-2
GITLR	D4-10	1	C-2
GMTS	B4-8	1	C-2
LWRITE	A4-6	1	B-2
PH01	A7-6	2	B-2
PH02	A7-10	2	B-2
PH04	D4-6	2	C-2
PHS0-7	E4	2	B-1, C-1
PHS2B/	F5-8	1	A-3
RMEM	B1-6	2	A-2
TDCR/	A3-8	1	B-2
TRPS/	F7-11	2	A-2
XDLS/	D5-6	1	A-2
XOD	B8-6	2	C-2
5DLS/	C3-6	1	C-2
1DLS/	A3-6	1	C-2

3.2.3 PROGRAMMABLE VOLTAGE SUPPLIES

There are two types of programmable voltage supplies; reference voltage supplies (RVS's) and digitally programmable supplies (DPS's).

Reference Voltage Supplies The function drive reference and the level detection reference RVS's are identical except for a difference in gain due to different amplifier feedback resistors. These supplies are energized under program control. There are five sets of RVS's which are the following:

RVS TYPE	FUNCTION DRIVE REFERENCE		LEVEL DETECTION REFERENCE		
Designation	E0-E1	EA0-EA1	S0-S1	EB0-EB1	EC0-EC1

RVS TYPE	FUNCTION DRIVE REFERENCE		LEVEL DETECTION REFERENCE	
Control Register	(33)(32)	(37)(36)	(35)(34)(43)(42)	(45)-(44)

Each RVS printed circuit board consists of two independent but identical digital-to-analog converters. The digital-to-analog converter is the current summing type, 10 bits plus sign (two's complement), with a current summing output amplifier which has two gain ranges. Each amplifier may be switched from the ladder network into the output of a non-inverting amplifier which is driven externally. The output amplifiers have remote sense feedback, which may be switched to enable either one of two output ranges. Each sense line may be switched into a common point which enables the monitoring of either supply by the PMU. For further information, refer to the RVS (97206103 and 97206110) porition of the section on printed circuit board theory.

Digitally Programmable Supplies There are three DPS's in the tester. The supplies are mounted on printed circuit boards, each having an associated 1-amp buffer circuit mounted on separate boards.

The DPS supplies are energized under program control. The supplies may be programmed to force a voltage or current, with programmable voltage or current trip circuitry to interrupt the system if the actual value exceeds the programmed value. The supplies can be programmed in either polarity in two voltage and two current ranges.

Each DPS has the following circuits: Two D/A ladder networks, 10 bits plus sign, two's complement. A two-range amplifier, (1 amp buffer board) for 1-amp drive capability. Three comparators, used for monitoring the output current level. A differential amplifier, with high common mode voltage capability, used to convert the output current level into a voltage level. A buffer amplifier that enables the use of a high impedance external voltage source, to replace the programmed voltage. Analog switches and drivers necessary to perform the logic functions of the assembly.

The ladder networks consist of 10 switches each. When the voltage ladder is programmed for a specific voltage, the current ladder may be programmed for a current trip and vice versa. Amplifier A2, together with the 1-amp buffer, provides the output voltage or current. The gain of the amplifier when connected in the current summing mode may be changed by closing K3. Both

ranges have gain adjustments R5 and R6 and zero offset adjustment R9.

Sense lines provide for remote sensing. Relay K7, when energized, connects the sense line to the PMU bus for monitoring by the precision measurement unit. The force line has two current sensing resistors in the 1 amp buffer board that allow monitoring of the output current at two range levels. A differential amplifier is connected across the current sensing resistors on the lamp buffer board. It generates a voltage that is proportional to the current being drawn. For further information, refer to the DPS (97206104) and the 1-Amp Buffer (97206105) portion of the section on printed circuit board descriptions.

3.2.4 PMU - PRECISION MEASUREMENT UNIT

INTRODUCTION

Functions

The Precision Measurement Unit (PMU) is an instrument which, under program control, can be connected to an individual pin of the device under test (DUT), for the purpose of making a quantitative voltage or current measurement at that point. This is useful during DC parametric or DC GO/NO-GO testing. The PMU is also capable of applying (forcing) a precise program-specified voltage or current to any desired pin of the DUT. In practice, these two operations are performed simultaneously--i.e., a voltage is applied, and a measurement is made of the resulting current flow; or, alternatively, a current is forced, and the voltage is measured.

The PMU can also be used to make a variety of internal measurements within the test system itself, such as measuring test head analog reference voltages and functional test voltages, as well as voltages at certain of the test points located on the printed circuit cards within the system. This is done automatically during system self-check under the control of diagnostic programs. Thus the PMU is also a troubleshooting aid at the user's disposal for purposes of system maintenance.

Basic Operating Modes

Figure 3-13 is a simplified block diagram of the PMU forcing and measuring circuitry. The positions of switches SW1 and SW2 implement the choice of operating mode.

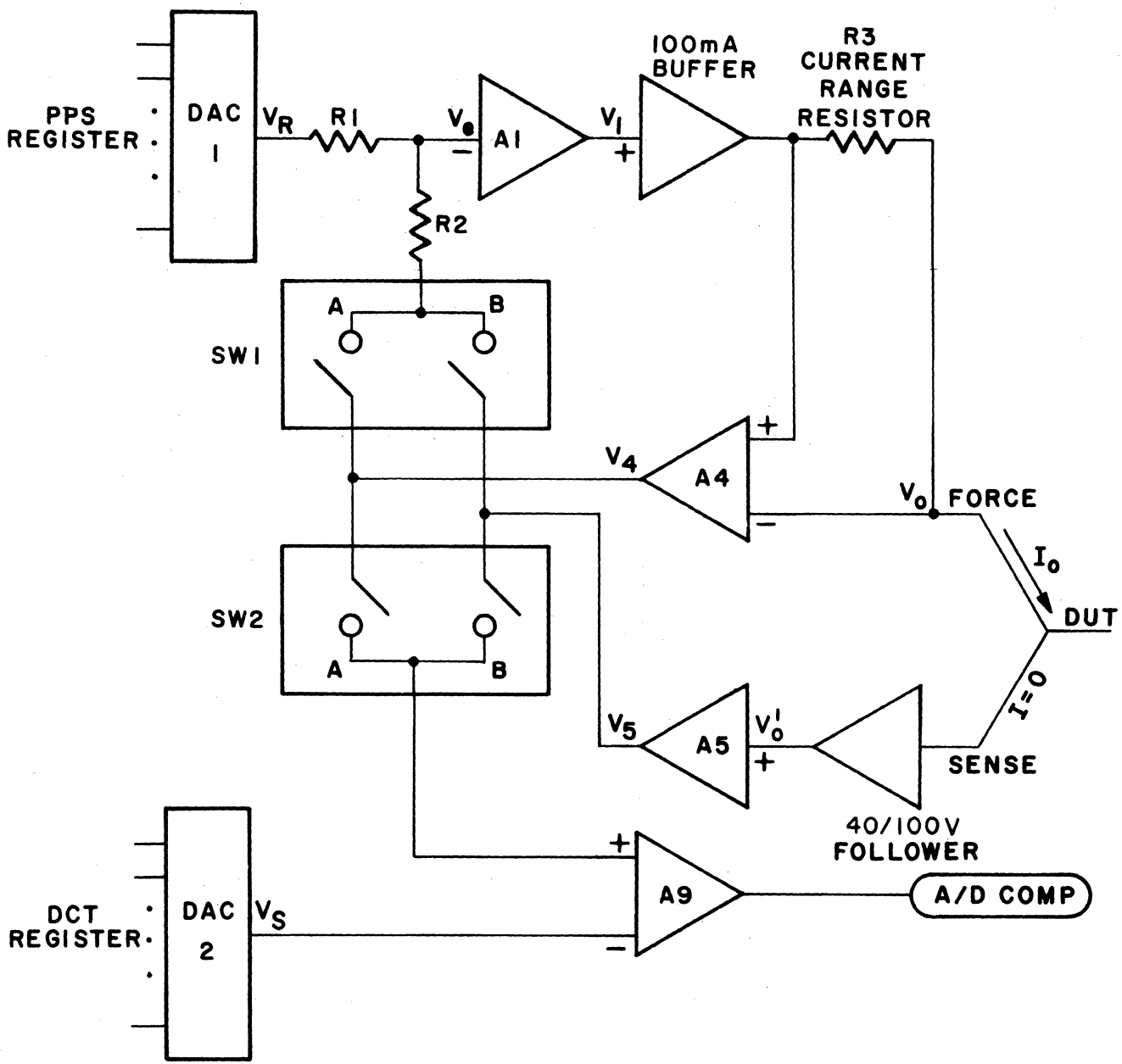


FIGURE 3-13. PMU SIMPLIFIED BLOCK DIAGRAM

When the PMU is to be used in the voltage forcing-current measuring mode, switches SW1-B and SW2-A are closed. The closure of SW1-B completes a voltage feedback loop, so that the voltage sensed by the 40 volt follower is fed back to the open-loop summing amplifier A1. The input of A1 is the voltage VR, which is the output of DAC 1, a digital-to-analog converter whose inputs are determined by the test program. The net result is that a stable PMU output voltage Vo is produced, which is proportional to VR. The ratio of the two, Vo/VR, is determined by the gain of amplifier A5, which is also program controlled. Thus the gain of A5 serves to establish the output voltage range (in practice A5 may be an active amplifier or a simple resistive voltage divider, depending on the voltage range selected).

The concurrent closure of SW2-A completes a current measuring circuit. The output voltage V4 of the differential amplifier A4 is proportional to the current flow Io into the DUT, by the simple relation V4=Io.R3. V4 then becomes one input to the comparator A9. The other input to A9 is VS, the output of DAC 2. A software routine, using the output of A9 as a control signal, adjusts the inputs to DAC 2 until V4 and VS are equal. This produces a quantity proportional to Io in digital form in the DCT register, which can be read out as part of the datalogging process.

Operation in the current forcing-voltage measuring mode is accomplished in a similar manner, by closing switches SW1-A and SW2-B. The closure of SW1-A completes a "current feedback loop", in which V4 must be equal in magnitude to VR. Since, however, V4 is proportional to Io, the net result is the production of a stable PMU output current, proportional to VR, which drives (or loads) the DUT, as set forth in the program. The ratio of the two, VR/Io, is the value of the current range resistor R3, which is switched in under program control to select the appropriate current range.

The concurrent closure of SW2-B completes a voltage measuring circuit, by connecting the output of amplifier A5 to one input of comparator A9. As above, a software routine adjusts the inputs to DAC 2 until V5 and VS are equal, such that a quantity proportional to Vo is retained in the DCT register.

Control

The operation of the PMU is controlled mainly by the contents of four registers, named as follows:

PPS (Precision Power Supply) register
DCT (DC Trip) register

PSL (Precision Sense Level) register
PA (Pin Address) register

The exact information content and bit configuration for each of these registers will be explained later. The following paragraphs describe the main functions of each register.

The PPS register holds the information determining the value of the voltage (or current) to be forced. This includes polarity, range, magnitude, and whether the forced quantity is voltage or current.

The DCT register is used to hold the information fed into DAC 2 during the course of the analog-to-digital conversion of the measured current (or voltage) value, as explained above. When this conversion is complete, the measured quantity is contained in this register in digital form. Polarity, range, and magnitude information are also present.

The PSL register is used to hold the information establishing the operating range for voltage or current measurements by the PMU, and specifying whether it is indeed current or voltage that is to be measured. The PSL register also holds the information specifying voltage clamp values. These values are upper and/or lower limits on the allowable voltage at the PMU output--i.e., at the pin of the DUT. This provides protection for the device under test. For example, a programming error may cause the PPS register to specify a harmfully high voltage to be applied to the pin of the DUT. In this case the voltage clamp circuit, programmed with limit values held in the PSL register, provides the required compensation within the voltage feedback loop, so that the PMU output voltage does not violate these limits, and thus the device is protected.

The PA register holds the information controlling the connection of the PMU to the appropriate pin of the DUT, or to the appropriate internal node within the test system. The bits of the PA register constitute the pin address.

OPERATION

Analog Circuits

Forcing and Measuring Circuits

Figure 3-14 is a simplified schematic of the basic forcing feedback loop and measuring circuit, serving as a reference for the following descriptions. Table 3-6 below, lists the voltage and current ranges available.

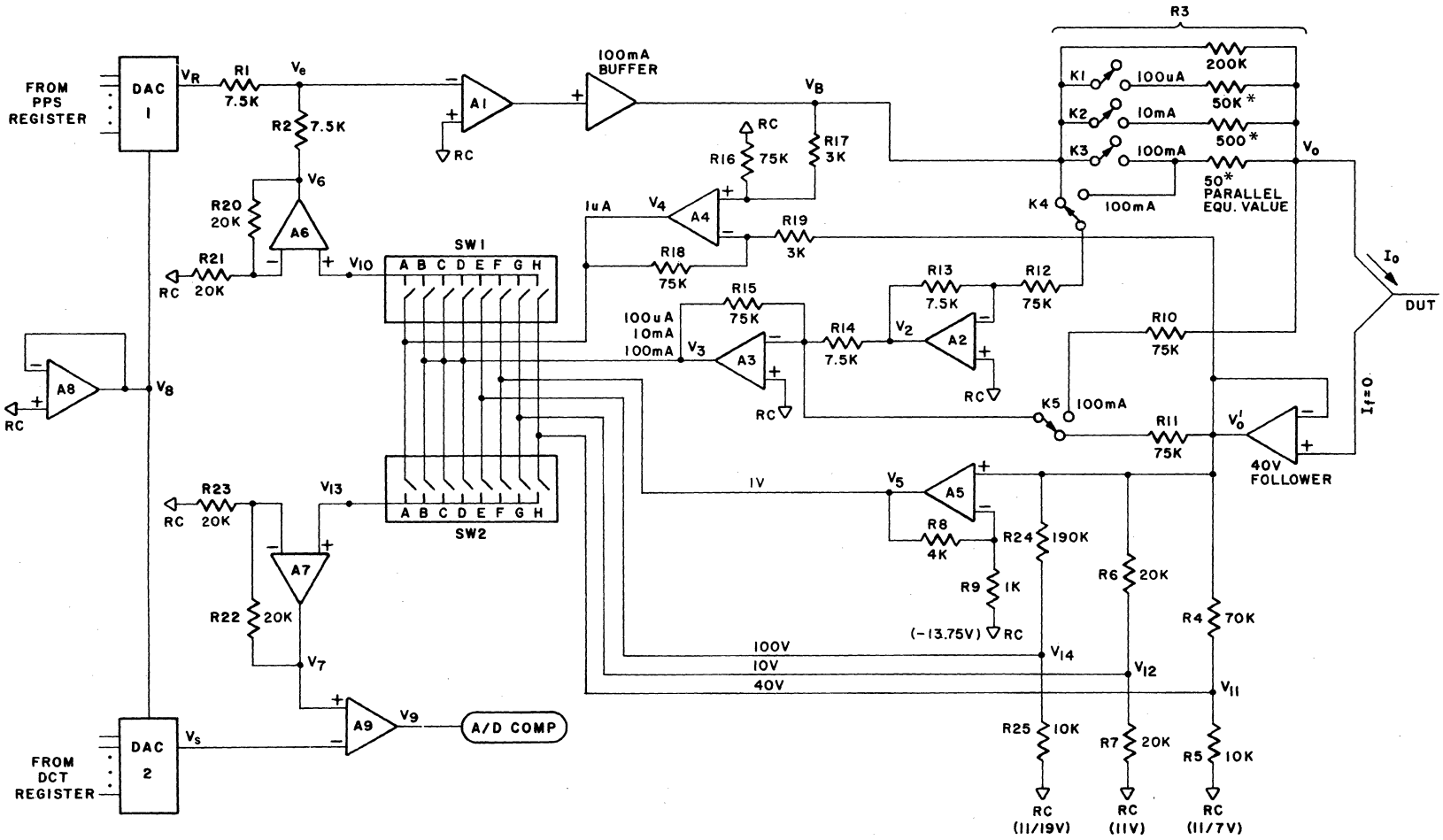


FIGURE 3-14. PMU SIMPLIFIED SCHEMATIC DIAGRAM

TABLE 3-6. VOLTAGE AND CURRENT RANGES

Range #	Voltage	Current
0	--	1uA
1	1V	100uA
2	10V	10mA
3	40V	100mA

DAC 1 and DAC 2 both have full scale outputs of 10 volts. A1 is an operational amplifier with open loop voltage gain on the order of 10^5 (100 dB); Ve, then, may be considered equal to zero. Since R1=R2, therefore, V6=-VR.

How the voltage ranges are established, can be demonstrated by tracing the voltage gain from the PMU output Vo to amplifier A6 output V6. Vo' is the output of the 40 volt follower, which is a unity gain non-inverting amplifier having a very high (10^{12} ohms) input impedance. Thus Vo'=Vo.

When the 10 volt range is selected, the voltage divider formed by R6 and R7 is used. In that case, V12=(R7/(R6+R7))Vo'=Vo/2. When the appropriate switch (SW1-G) is closed, V10=V12. Finally, the gain of the non-inverting amplifier A6 is given by V6=((R20+R21)/R21)V10=2V10. Thus by substitution V6=Vo, from which it follows that the PMU output Vo has the same value (although opposite in polarity) as the DAC 1 output VR, thereby establishing the 10 volt PMU output range.

In exactly the same manner, when switch SW1-H is closed, V10=V11, and V11 = (R5/(R4+R5))Vo'=Vo/8, therefore, V6=Vo/4, so that the 40 volt range is established in this case.

When SW1-F is closed, V10=V5. V5, however, is the output of the non-inverting amplifier A5, the gain of which is given by V5=((R8+R9)/R9)Vo'=5Vo. Thus V6=2V10=2V5=10Vo, which establishes the 1 volt range.

Since the gain of A7, given by V7=((R22+R23)/R23)V13=2V13 is the same as the gain of A6, and DAC2, like DAC1, has a full scale output of 10 volts, it can be seen that the voltage ranges for measuring are the same as those for forcing. The only difference is simply that the appropriate legs of SW2 are closed, rather than SW1 , so that the voltage information is fed to the comparator A9, rather than closing the voltage feedback loop into A1.

Current forcing ranges are determined by the positions of switches K1-5 and SW1-A,B,C,or D. When a current range of 100uA, 10mA, or 100mA is chosen, SW1-B,C, or D is respectively closed,

and in all three cases V10=V3. A2 and A3 together act as a differential amplifier, where V2=-(R13/R12)VB=-VB/10 and V3=-(R15/R14)V2-(R15/R11)Vo'=-10V2-Vo'=VB-Vo. Hence V6=2(VB-Vo).

VB-Vo is related to the PMU output current Io by the relation VB-Vo=Io.R3, so that V6=2Io.R3. Substituting the values of R3 switched in by K1, K2, and K3, we have:

V6=2Io.50K	= 100,000Io	(100uA range)
V6=2Io.500	= 1000Io	(10mA range)
V6=2Io.50	= 100Io	(100mA range)

As before, V6, like DAC 1 output VR, has a full-scale range of 10 volts. The resistance values listed above for R3 are the equivalent parallel resistances of the resistor switched in by K1, K2, or K3, and the 200K resistor that is always in place.

The 1uA range is implemented when switch SW1-A is closed. This sets V10=V4, connecting the input of A6 to the output of differential amplifier A4. Therefore, V4=(R16/R17)VB-(R18/R19)Vo=25(VB-Vo), and V6=50(VB-Vo). Substituting VB-Vo=Io.R3, it follows that V6=50x200KxIo=10x10^6 Io. Since V6, again, is 10 volts full scale, the range of Io is 1uA.

The preceding paragraphs describe the establishment of the ranges for current forcing. The ranges for current measurement are the same. This is due to the fact that the gain of amplifier A7 is the same as that of A6, and the output range of DAC 2 is the same as that of DAC 1. In the case of current measuring the output of A3 (or A4) is switched by SW2 through A7 to the comparator A9, rather than by SW1 through A6 to complete the feedback loop at the input of A1.

Further aspects of this circuitry will be discussed in the section on detailed circuit descriptions. This discussion examines the various loading effects, the choice of voltage sampling points, and the purpose and structure of the 100 mA buffer and 40 volt follower.

Voltage Clamp Circuit

This circuit provides protection for the device under test, by setting up limits for the PMU output voltage Vo. These limits can be selected under program control, according to the configuration of bits in the PSL register.

Figure 3-15 is a simplified schematic, showing how the voltage clamp circuit modifies the basic voltage (or current) forcing feedback loop to accomplish this voltage limiting action. The

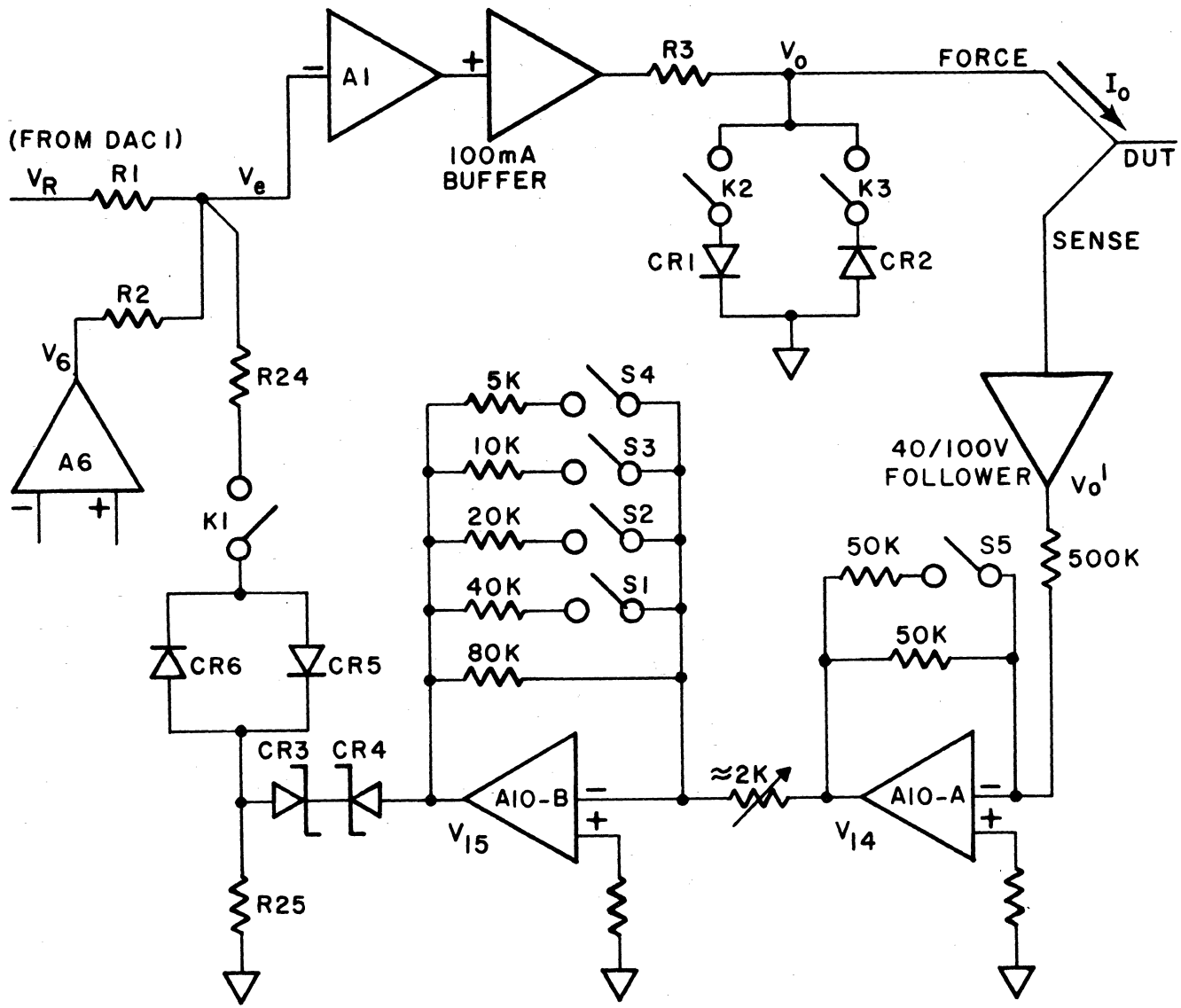


FIGURE 3-15. VOLTAGE CLAMP CIRCUIT SIMPLIFIED SCHEMATIC DIAGRAM

signal path from DAC 1 output VR and amplifier A6 output V6, through A1, the 100mA buffer, R3, the DUT, and the 40 volt follower is part of the basic forcing feedback loop. The remaining circuitry shown in Figure 3 is unique to the voltage clamp circuit.

The actual voltage clamp values depend on the characteristics of the zener diodes CR3 and CR4, and the gain of amplifiers A10-A and A10-B. The clamp circuit operates when the "clamp enable" relay K1 is closed, and when the voltage V15 exceeds about ± 6 volts (that is, less than -6 volts or more than +6 volts). The values of Vo corresponding to !6 volts at V15 are inversely proportional to the gain of A10-B, which depends in turn on the position of the clamp magnitude relays S1, S2, S3, and S4. For example, when all four relays are open, only the 80K ohms feedback resistor remains across A10-B. Thus V15=-40xV14 and V14=-Vo'/10, so that Vo=V15/4=$\pm$6/4 volts; hence the clamp limits on Vo are $\pm$1.5 volts.

Values of Vo outside this range do not occur, since the additional feedback through A10-A and A10-B provides enough current into the summing junction Ve at the input of A1, to maintain Vo at the limiting value.

Higher clamp values are set by closing relays S1, S2, S3, and S4 according to the configuration of the corresponding four bits (VLT1-4) in the PSL register. The clamp values are a linear function of this four-digit binary number. The actual numerical values are given in the following table.

TABLE 3-7. VOLTAGE CLAMP VALUES

VLT 4	3	2	1	Clamp Value (Volts)
0	0	0	0	$\pm$1.5
0	0	0	1	$\mp$4.5
0	0	1	0	$\mp$7.5
0	0	1	1	$\mp$10.5
0	1	0	0	$\mp$13.5
0	1	0	1	$\mp$16.5
0	1	1	0	$\mp$19.5
0	1	1	1	$\mp$22.5
1	0	0	0	$\mp$25.5
1	0	0	1	$\mp$28.5
1	0	1	0	$\mp$31.5
1	0	1	1	$\mp$34.5
1	1	0	0	$\mp$37.5
1	1	0	1	$\mp$40.5

Tolerances are ±1 volt ±10% of the value specified.

The clamp operation also provides a choice of "positive", "negative", or "symmetrical" clamp. These are defined by the following allowed voltage ranges:

positive clamp	-0.7 volts to +Vc
negative clamp	-Vc to +0.7 volts
symmetrical clamp	-Vc to +Vc

where Vc are the values given in Table 3-7 above.

Positive and negative clamp are implemented by closing relays K3 or K2, respectively, according to the values of bits 6 and 7 in the PSL register. Symmetrical clamp occurs with both K3 and K2 open.

Control Circuits

PPS (Precision Power Supply) Register

This register holds the information determining the value of the voltage (or current) to be forced. Fourteen bits are used, according to the following format:

Bits 0-9 and the polarity bit 10 are fed to DAC 1 to determine the value of VR (see Figure 2). The (binary) 10 place accuracy of bits 0-9 provides a resolution of 0.1% of full scale. Bit 10 is a zero for positive polarity, one for negative.

Bits 0-10 are in two's complement coding, as illustrated by the following examples:

```
0111111111 = +FS (full scale)
0000000001 = +LSB (least significant bit)
0000000000 = 0
1111111111 = -LSB
1000000000 = -(FS+LSB)
```

Bits 11 and 12 determine the voltage (or current) forcing range as follows:

TABLE 3-8 - VOLTAGE AND CURRENT RANGE BIT FORMAT

Range	Bit 12	Bit 11	Voltage	Current
0	0	0	--	1uA
1	0	1	1V	100uA

TABLE 3-8 - VOLTAGE AND CURRENT RANGE BIT FORMAT (Continued)

Range	Bit 12	Bit 11	Voltage	Current
2	1	0	10V	10mA
3	1	1	40V	100mA

This range information, together with bit 13, which selects voltage or current forcing (1=voltage forcing, 0 = current forcing), then controls the position of the switches SW1 (Figure 2) and (in the case of current forcing) relays K1 through K5.

DCT (DC Trip) Register

This register holds the information used in the voltage (or current) measuring process. Fifteen bits are present, in the following format:

Bits 0-9 and polarity bit 10 are fed to DAC 2 to establish an analog comparison reference into the comparator A9 (Figure 2). As with the PPS register, a resolution of 0.1% of full scale is available.

Bits 11 and 12 duplicate the corresponding bits of the PSL register, which in turn hold the information establishing the voltage (or current) range for measuring. The definitions of the four ranges used are the same as listed under "PPS Register" above.

Bits 13 and 14 are used in connection with DC GO/NO-GO testing. Bit 13 is defined by:

1 = Greater than (GT)
0 = Less than (LT)

Thus it is possible to specify (using bits 0-13) pass and fail thresholds for the measured voltage or current. This DC GO/NO-GO testing is carried out in Direct Memory Access mode. When a GO/NO-GO measurement is executed, a DC strobe signal samples the comparator (A9, Figure 2) output. A failure generates a DC fail signal, which causes a functional test interrupt.

A comparator fail signal during a strobe sets a latch (LRD14/=0) at bit 14, while a comparator pass signal during a strobe resets this latch (LRD14/=1).

TABLE 3-9. PPS REGISTER

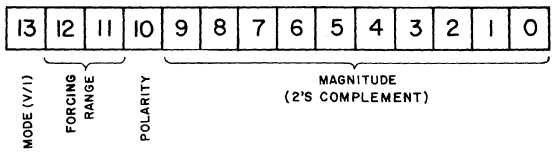


TABLE 3-10. DCT REGISTER

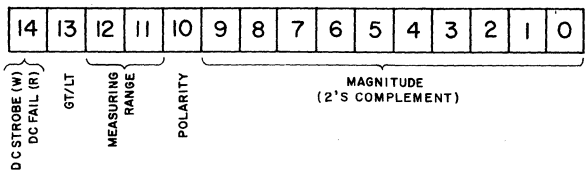


TABLE 3-11. PSL REGISTER

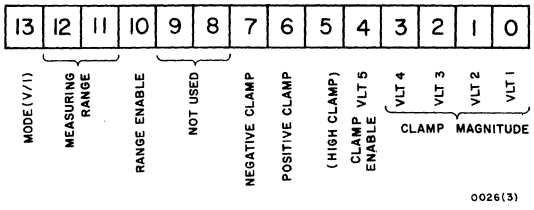
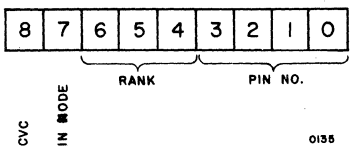


TABLE 3-12. PA REGISTER



The DCT register is also used in the course of making a quantitative DC parameter (voltage or current) measurement. In this case, a software routine carries out an algorithm of successive approximations, based on the comparator output condition as feedback around DAC 2. The execution time of such a software A/D conversion is about 350 microseconds.

This software routine performs 11 iterations -- one for the sign, and one for each of the 10 magnitude bits. The DCT register is initially loaded with all zero's. Then, depending on whether the comparator output corresponds to a pass or fail, the sign bit is set to zero or one. Next, each of the magnitude bits, in descending order of significance, is set to a zero or one. This is accomplished by an addition or subtraction of a one in each bit position, depending on whether the comparator indicates pass or fail. The quantitative effect of each such addition or subtraction is one-half that of the previous operation, hence the term "successive approximations".

PSL (Precision Sense Level) Register

This register is used for setting up sense (measuring) range conditions and voltage clamp values. Fourteen bits are arranged in this register as follows:

Bits 0-3 select the clamp magnitudes as given in Table 2 in the analog circuits section above. Bit 4, clamp enable, if it is a one, closes relay K1 (Figure 3), connecting the clamp circuit into the feedback loop.

Bits 6 and 7 select positive, negative, or symmetrical clamp, as defined in the section on the voltage clamp circuit above, and shown in the following table.

Clamp	Bit 6	Bit 7
Positive	0	1
Negative	1	0
Symmetrical	0	0

The range enable, bit 10, has two functions. If bit 10 is a one, the sensing ranges (bits 12 and 11) can be programmed, and the clamp data (bits 0-7) is protected. If bit 10 is a zero, the voltage clamp can be programmed, and the range data is protected.

Bits 12 and 11 determine the sensing (measuring) range, with values according to Table 3 under "PPS Register" above.

Bit 13 determines whether the measurement is a current or a voltage. Bit 13=1 is defined as a voltage measurement, while with bit 13=0, current is sensed. Bit 13 of the PSL register is constrained to be the complement of bit 13 in the PPS register. Thus, in effect, when voltage is forced, current is measured, and when current is forced, voltage is measured.

PA (Pin Address) Register

This register holds the information addressing the specific pin of the test head (or internal node) to which the PMU is connected. Nine bits are present, according to the following format:

This provides a capability such that DUT's up to 120 pins can be tested, as far as pin addressing is concerned (the actual number of pins depends on the system and option selected). These pins are arranged in up to 8 ranks of 15 pins each. Bits 4-6 select which of the 8 ranks is addressed; bits 0-3 select one of the 15 pins within that rank. Since the four bits 0-3 provide 16 bit configurations, and only 15 are used, there is one combination left over. This is the 0000 address, and is used for "XPMU", a position to which the PMU is switched when not in use.

Bit 7 (In Node) is a 0 for all pin addresses. When bit 7 is a 1, the PMU is connected to specified internal nodes. The same 7 bits, 0 - 6, that are used to specify all pin addresses, are used to specify all internal node addresses. All internal nodes can therefore be considered as starting with address 128 in the pin address register.

Bit 8 (CVC), when equal to one, is used to connect the functional test driver and the PMU to the same test head pin at the same time, in response to the ENABLE RELAY statement. Bit 8 can be set only if bit 14 is a one (LRD14/=0), whereas bits 0-7 can be set only if bit 14 is a zero (LRD14/=1).

The components of the pin address register are located on the 15 Bit Decoder Board. For the sake of completeness, however, its function is described here as part of the PMU operation.

DETAILED CIRCUIT DESCRIPTIONS

Analog #1A Board (Refer to schematic 97341605-04)

Basic Forcing Loop and Sensing Circuitry

The operation of this feedback loop is discussed in the section on analog circuit operation above. This section discusses some of the factors regarding the choice of components.

An important consideration is that the response of the feedback loop should be as fast as possible, so that the PMU output voltage (or current) can faithfully follow the DAC 1 output without overshoot. Thus the use of fast (high slew rate) operational amplifiers is dictated.

Amplifier A6 is a particularly fast op amp, which has a high input impedance and a low input bias current. The main function of A6 is to isolate the switching network S1 from the summing resistor R6 at the input of A1. The switches are a solid state MOS type having a resistance of about 1000 ohms when turned on. The low input bias current into A6 assures a low current through S1 and thus a negligible voltage drop across S1. This in turn helps assure the accuracy of the feedback portion of the basic forcing loop.

Amplifier A7 serves a similar function to A6, but with regard to the switches S2 and the comparator A9. The speed requirement is not as critical as A6. Therefore, a general purpose op amp (uA 741) is used.

A4 is a discrete op amp module with very high slew rate and common mode rejection ratio. It is connected as a differential amplifier, the gain of which is determined by the ratio of the feedback and input resistors, as mentioned in the analog circuits operation section above. The relatively high (closed loop) gain (25) of this amplifier is required because of the low (1 uA full scale) current being measured, and the moderate (200K ohms) value of R13. R13 must not be too high, since a high value would result in a long RC time constant and hence a slow response of the feedback loop. The high gain of A4 results in significant amplification of noise on the 1uA range; therefore, a low-pass filter is inserted, composed of R70, C8, and R45.

A2 and A3 together form a differential amplifier (as stated in the analog circuit operation section). The use of two low voltage IC op amps provides a high common mode rejection ratio and a high common mode range. The speed requirements on A2 and A3 are not as stringent as those on A4. This is true because the speed of the feedback loop is jointly a function of amplifier

slew rate and the value of the current sampling resistors (R13, R14, R15, R16). For the 1uA range, a larger value of R13 (200K ohms) is required, to the detriment of the response time. To compensate for this, A4 must be especially fast, hence the necessity to build A4 as a single amplifier, from discrete components. For the higher current ranges (100uA, 10mA, 100mA), this resistance (R14, R15, or R16) is lower, and hence A2/A3 can be slower. Both A2 and A3 are low input bias current types (uA777), to avoid offset voltage errors at the outputs of A2 and A3. In practice, this means an error of less than 5mV, (the LSB value at the points V3 and V4.)

100mA Buffer Amplifier

The 100mA buffer is used to increase the current and voltage capability of the forward loop. This buffer circuit has an open loop gain of about 65 db; internal negative feedback brings the closed loop gain down to a factor of about 11. Since A1 is capable of 10 volts output, the 100mA buffer can provide as much as 110 volts output, as far as gain is concerned. The actual output voltage available depends on the power supply voltages used. The power supply voltage is +48 and -48 volts, and the output voltage can range from 0 to $\pm$44 volts.

The 100mA buffer circuit is current limited and short-circuit proof. Two current ranges are provided. A 160mA limit is in effect on the 100mA sensing range, when the relays K201 and K202 are closed. When these relays are open (i.e., on the 10mA, 100uA, and 1uA ranges), a 16mA limit is held. The purpose of this current limiting to 16mA is to protect the current sampling resistor R15 from excessive power dissipation, during voltage forcing operations when the 10mA current measuring range is selected. The current limiting is controlled by CR204, R208, and R209 on the positive side, and by CR205, R217, and R220 on the negative side.

A 6db/octave frequency response is incorporated to assure that the buffer is unconditionally stable. The dominant pole is controlled by the RC time constant of C203 and R213, and provides a corner frequency of about 2 kHz.

The 100mA buffer has a very high slew rate, greater than that of A1. This is necessary because the voltage swing at the 100mA buffer output is 11 times as much as that at the output of A1.

MOS Switches

The use of solid state MOS switches for S1 and S2, rather than relays, offers several advantages. Speed of operation is greater, so that voltage and current range changes can be made in less time. Also, the reliability is better.

Each of the switches S1 and S2 must be capable of switching the maximum analog signal voltages which may at any time be present at its terminals. Thus, to find the required switch rating, we need to examine the signals at test points TP9, TP10, TP11, TP13, and TP14. Each of these test points has a voltage range of $\pm$5 volts full scale when actually used in the forcing loop or measuring circuit. However, voltages considerably in excess of 5 volts (in some cases as much as 20 volts) would appear at some of these test points under certain selections of forcing and/or measuring ranges, if no action were taken to prevent this. For this reason zener diode pairs CR15/16, CR13/14, CR19/20, CR9/10, and CR11/12 are used to limit these voltages to about 5.8 volts. This gives no interference with normal operation, but does protect the MOS switches. The particular switches chosen are DG503 (Fairchild Part No. 26904802), which have a $\pm$10 volt analog signal rating.

The DG503 is a single pole, 8-position switch with a built-in 3 bit decoder. The necessary input is provided for S1 by bits 11, 12, and 13 of the PPS register, and for S2 by bits 11, 12, and 13 of the PSL register. However, the logic levels needed to drive these switches are low level (less than 0.6 volts) and high level (greater than 8.5 volts). Since these are not the standard tester logic levels, special measures must be taken to convert them. This is accomplished by the 7406 hex inverter G6, with open collector output, and a +10 volt pullup provided by Q1, CR31, R10, and R11.

DAC 1 and DAC 2 (Forcing and Measuring DAC's)

Cycom CY2235 digital-to-analog converters are used for DAC 1 and DAC 2. These are 12 bit DAC's, which are used to provide 10 significant bits plus sign. The DAC's are manufactured to use offset binary inputs, whereas the information in the PPS and DCT registers is in two's complement coding. Therefore, inverters are used at certain of the DAC 1 and DAC 2 inputs to effect the conversion. The DAC 1 output has a negative sign relative to the PMU output, while the DAC 2 output is positive in that respect. This explains the fact that 10 inverters are needed (for the 10 significant bits) at the DAC 1 input, while for DAC 2 only 1 inverter (for the polarity bit) is required. Note also that the least significant bit (bit 16) is tied high for DAC 1 and low for

DAC 2. In DAC1 the LSB is tied to +5V, providing an LSB offset to compensate for the difference between the offset binary and two's complement coding.

The DAC's have their own internal reference voltage, a settling time of 20 usec to half LSB value, and a gain accuracy within 0.1%.

Ground Buffer

It is important that the reference common (RC) between boards (and particularly between the system ground and the PMU board) carry no significant amount of current, if it is to serve as a reliable 0 volt standard. DAC 1 and DAC 2, however, deliver up to 70mA each to their ground. For this reason, the ground buffer circuit is included, to provide a current return path and isolate the ground current from the RC, while maintaining a high impedance to the RC line itself.

This buffer circuit consists of a general purpose op amp (A8) in a voltage follower connection, with a high current capability discrete current buffer (Q2, Q3, Q4) in the output. The voltage gain is equal to unity with an output current capability of 200mA.

Because of this ground buffer, the DAC analog ground always maintains the same potential as RC, regardless of the bit configuration at the DAC inputs. This assures accuracy of the PMU forcing and measuring functions.

Current Range Relays

Since the PMU output voltages can be as high as $\pm$40 volts, mercury film relays are used in the current range relay circuits K1 - K5. The mercury film relays used in this circuit provide a mean time to first failure of about 250 million operations. Moreover, these relays have a very clean closure characteristic, free from relay contact bounce and contact noise. Thermal noise across the contact junction is also much less than with reed relays.

This type of relay is driven by a pulse with 3 milliseconds minimum pulse width (supplied by a one-shot on the PMU control board). The relay itself contains two coils and a ring shaped ferrite magnet. A pulse applied to the set coil transfers the moving contact, which then latches in position, without the need for a holding current. A pulse applied to the reset coil returns the moving contact to its original position.

Relays K1, K2, and K3 switch, in a mutually exclusive manner (for example, when K1 is closed K2, K3 are open), the current range resistors for the 100uA, 10mA, and 100mA scales, respectively. Relays K4 and K5 also switch at the same time as K3. The purpose of K4 is to bypass the contact resistance of K3, allowing a more accurate current forcing and measuring on the 100mA range. For the same reason, relay K5 is used to bypass the resistance of the force and sense lines to the DUT.

Analog #2A Board (Refer to schematic 97341604-04)

40 Volt Follower

This circuit is shown extending from the PMU sense line to the point marked Vo'. The purpose of this circuit is to provide a unity gain amplifier with voltage follower configuration in the PMU sensing line, by using an op amp with a very high input impedance. This enables an accurate measurement of the voltage on the PMU sense line coming from the DUT, free from errors introduced by the loading effects which would be present if the sensing circuitry drew any significant amount of input current. This is particularly important when the PMU is used in the voltage forcing/current measuring mode. The high input impedance in this case assures that the measured current through R3 (Figure 2) is equal to the current into the DUT.

Another purpose of this circuit is to provide a low impedance source to drive the shield on the PMU force/sense lines. This assures that the PMU shield has the same potential as the PMU force/sense lines, and thus reduces the effect of capacitive loading.

Figure 3-16 below, shows a simplified equivalent circuit for this 40 follower.

The FET input operational amplifier A1026 is used with a floating power supply composed of two 15 volt zener diodes. The output is taken from the zener center tap, connected as a voltage follower. Under these conditions, the input impedance is the product of the A1026 input impedance and the 40V follower open loop gain (approximately 10^{15} ohms). In practice, however, the common-mode impedance of the A1026 itself, about 10^{12} ohms, is predominant, so that 10^{12} ohms is the effective loading on the PMU sense line itself.

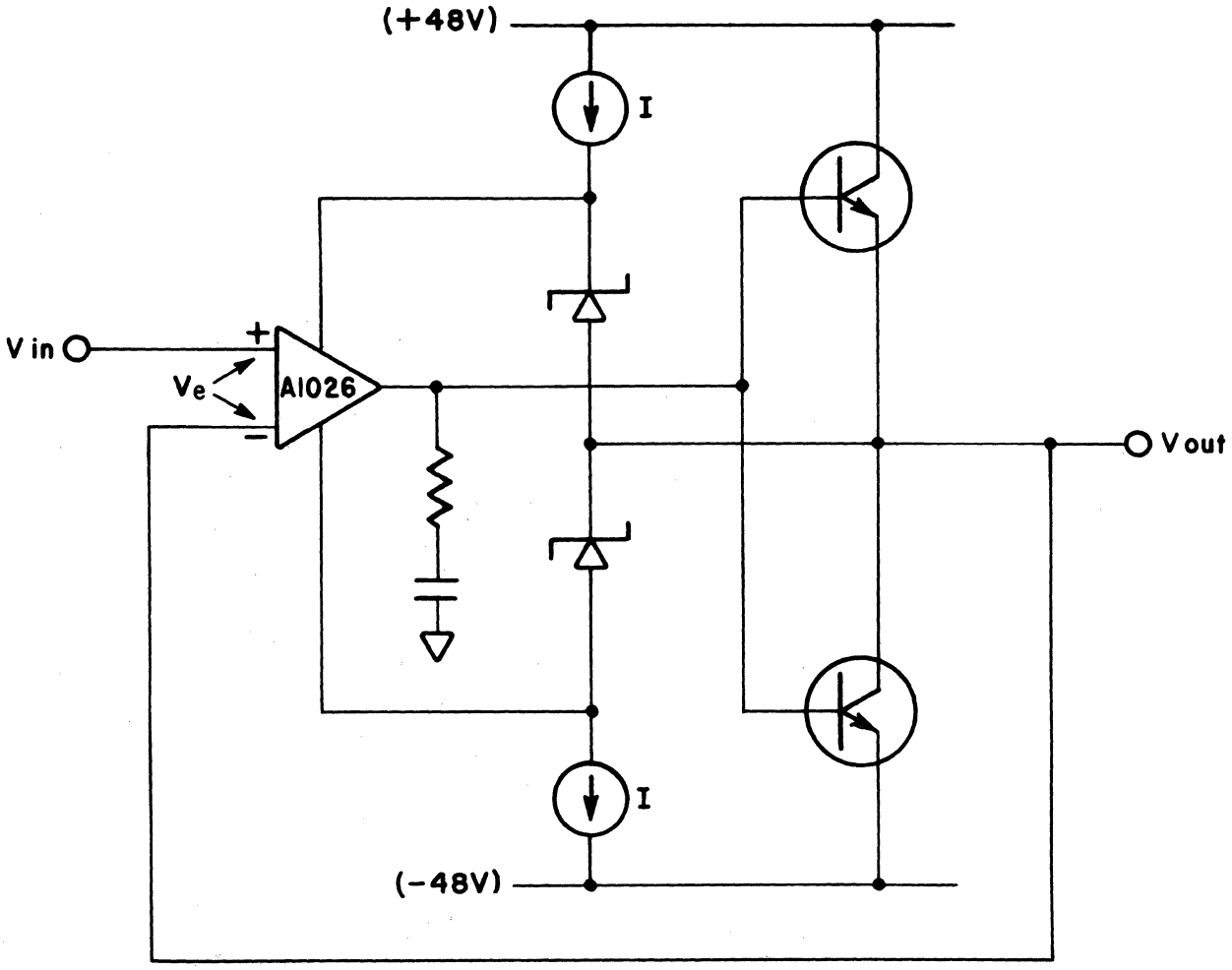


FIGURE 3-16. 40V FOLLOWER SIMPLIFIED

Voltage Clamp Circuit

The basic voltage clamp operation is described in the analog circuit operation section above. This section discusses the function of some of the major components.

R212 is used in connection with the zener diodes CR201 and CR202, to assure that enough current is drawn through the zeners to give a square characteristic. R212 also provides a path for the leakage current of CR201 and CR202, to maintain the accuracy of the programmed voltage when the programmed value is near the clamped value. The relatively low resistance of R212 necessitates further decoupling of this load from the summing junction of A1, in order to maintain accuracy. For this reason, the diodes CR203 and CR204 are included. The forward bias voltage of these diodes is about 0.3 volts. Thus when the clamp voltage is not exceeded, the diodes are both reverse biased and present essentially an open circuit. When the clamp voltage is exceeded, that is, when the programmed voltage exceeds the clamp voltage, then the output of A201-B will exceed about ± 6 volts (greater than +6 or less than -6 volts). The zeners will then conduct, and current will flow through R212. When the voltage drop across R212 exceeds ± 0.3 volts, current will flow through CR203 or CR204.

For a positive clamp, CR203 conducts, CR201 is zenered, and CR202 is forward biased, while for a negative clamp, CR204 conducts, CR201 is forward biased, and CR202 is zenered.

Capacitor C205 increases the stability (preventing oscillation) at low values of current through the zeners. This occurs when the programmed voltage and the clamp voltage are approximately equal.

Capacitor C202 prevents oscillation of A201-B. It is selected as small as possible while still stopping oscillation. In this way the high speed of the clamp feedback circuit is maintained.

Capacitor C201 also speeds up the operation of the clamp feedback circuit, thus preventing a spike into the DUT when the programmed output voltage exceeds the clamp value.

Miscellaneous Relays

Six reed relays are used on this board, driven by the three (944) dual four-input NAND gates QA2, QA3, and QA4. The respective functions of these relays are described below.

K13 is the voltage clamp enable. It is controlled by bit 4 (VLT5) of the PSL register (described under Control Circuits above). When bit 4=1, relay K13 is closed, connecting the voltage clamp circuit (through diodes CR203 & CR204 and resistor R214) into the feedback loop at the summing junction of A1 (PMU Analog #1A board).

K11 and K10 implement the positive, negative and symmetrical clamp options (see Analog Circuits above). These relays are controlled by bits 6 and 7 of the PSL register. When positive clamp is programmed, K10 is closed, K11 open; when negative clamp is programmed, K11 is closed, K10 open. Symmetrical clamp corresponds to both K11 and K10 open.

K9 connects resistor R30 as a load for the PMU, when the PMU is not connected to any DUT pin or when the system is in reset condition. K9 is closed when the PMU is in current forcing mode, and open when the PMU is in voltage forcing mode, such that there is no load when voltage is forced. R30 has a very low value (10 ohms), and its purpose is to prevent voltage saturation of the PMU output, in case of programming errors.

K12 is closed when the PMU is used for internal node measurements. It is controlled by bit 7 of the PA register, such that when bit 7=1, relay K12 is closed. This connects the PMU sense circuitry to "MPMUSNSE", which is in turn switched to various internal nodes under the control of PA register bits 0-6.

PMU Control Board (Refer to schematic 97230104-04)

PPS Register

This register has 14 bits (named PPSLD0-9, PPSPOL, PPSRNG0, PPSRNG1, and PPSV/I), which are held in the 9308 dual four-bit latches E5 and A5. The PPSLD3 bit, as an example, is "written" into the PPS register from the long register data buss, or "read" out of the PPS register onto the long register data buss, in the following manner.

In the write operation, the data for PPS bit 3 first appears as LRD03/ on the long register data buss. After being inverted by the 9016 inverter D2-2, it appears at pin 4 of E5, the input of the latch for bit 3. When pins 2 and 3 of E5 are both low, this data is transferred to the output, and appears as PPSLD3 at pin 5 of E5. This occurs when PPSA is high, and WRITE/ and CPS/ are both low, to enable the read operation.

The read operation occurs as a transfer of the PPSLD3 data from pin 6 to pin 1 of the MSI 9309 dual four-input multiplexer F3.

This occurs when S0 is low and S1 is high--i.e., when PSLA is low and PPSA is high. The data is then inverted by F2-6 and passed onto the long register data buss as LRD03/, provided that F2-2 is high--i.e., READ/ is low (note that F2-1 is automatically high since PPSA is high), to enable the read operation.

DCT Register

This register has 15 bits (named DCT0-9, DCTPOL, PSLRNG0, PSLRNG1, DCTG/LT, and DC STROBE/DC FAIL). DCT0-9, DCTPOL, and DCTG/LT are held in the 9308 latches F5-A, B5-B, and D5-B (the suffix A refers to pins 1-11 of the 9308, while B refers to pins 13-23). Bits 11 and 12 (RNG0 and RNG1) of the DCT register have no provision for a write operating, since they are identical with those of the PSL register. Thus separate latches need not be used. Proper response to the DCT register read instruction is insured by the connection of pins 4 and 5 of F4, and pins 11 and 12 of A4. Bit 14 serves a dual function of DC STROBE when written and DC FAIL when read. This will be discussed in more detail later in this section.

The DCT2 write and read operations between the long register data buss and the DCT register can be traced as follows: In the write operation, the data for DCT bit 2 first appears as LRD02/ on the long register data buss. After being inverted by D2-4, it appears at pin 6 of F5, the input of the latch for bit 2. When pins 2 and 3 of F5 are both low, this data is transferred to the output, and appears as DCT 2 at pin 7 of F5. This occurs when LRD14/ and DCTA are both high, and WRITE/ and CPS/ are both low.

The read operation occurs as a transfer of the DCT2 data from pin 12 to pin 15 of F3. This occurs when S0 and S1 are both low--i.e., when PSLA and PPSA are both low. The data is then inverted by F2-8 and passed onto the long register data buss as LRD02/, provided that F2-12 is high (READ/ is low) and that F2-13 is high (DCTA is high).

Bit 14 serves a number of functions. During a write operation (WRITE/ and CPS/ low), when DCTA is high, LRD14/ in the high state gates data into the 9308 latches in the DCT register. When LRD14/ goes low (DCTA still high), C2-2 goes high and D3-12 goes low, which brings C3-11 high and produces the DC STROBE. This gates PASS/FAIL data from D1-6 into the DC FAIL flip-flop. DC STROBE is also produced when A1-9 and A1-10 are both high--i.e., when READ/ is low and DCTA is high.

The output of the DC FAIL flip-flop is inverted by A3-6 and gated onto the long register data buss as LRD14/, when READ/ is low and DCTA is high. This explains why bit 14 of the DCT register is

said to be the DC FAIL signal when read, and DC STROBE when written.

PSL Register

This register has 14 bits (named VLT1-5, VLT40V, POSCLP, NEGCLP, SPARE 1, SPARE 2, PSLRGN, PSLRNG0, PSLRNG1, and PSLV/I). The function of each bit is explained in the "Operation" section above. The first 8 bits (0-7, through NEGCLP) are held in the 9308 latches F5-B and B5-A. Bit 8, SPARE 1 (TA4), tied to ground, is read only. Bit 9, SPARE 2, though presently not used, is held in D5-A. RANGE ENABLE (PSLRGN), PSLRNG0, and PSLRNG1 are also held in D5-A. PSLRGN, bit 10, is write only, but the PSL read operation brings out TA4 onto LRD10, which is therefore always read low. Bits 11 and 12 are PSLRNG0 and PSLRNG1, respectively. Bit 13, PSL V/I, does not have a separate latch, but is taken from bit 13 of the PPS register and inverted by C1-6 (i.e.--PSL bit 13 is the complement of PPS bit 13). Thus bit 13 in the PSL register is not affected during PSL write operations.

The VLT5 bit (PSL bit 4) write and read operations between the long register data buss and the PSL register can be traced as follows: In the write operation, the data for VLT5 first appears as LRD04/ on the long register data buss. After being inverted by C2-10, it appears at pin 6 of B5, the input of the latch for bit 4. When pin 2 and 3 of B5 are both low, this data is transferred to the output, and appears as VLT5 at pin 7 of B5. This occurs when PSLA is high, and WRITE/ and CPS/ are both low.

The read operation occurs as a transfer of the VLT5 data from pin 11 to pin 15 of B3. This occurs when S1 is low and S0 is high--i.e., when PPSA is low and PSLA is high. The data is then inverted by B2-8 and passed onto the long register data buss as LRD04/, provided that B2-12 is high--i.e., that READ/ is low (note that B2-13 is automatically high since PSLA is high).

Current Range Relay Drivers

The functions of the current range relays are described above under Analog #1 board. Signals for switching these relays are generated on the PMU Control board by the circuitry shown on page 2 of the PMU Control schematic. The logic shown is mainly for the purpose of decoding bits 11, 12, and 13 of the PPS register (PPSRNG0, PPSRNG1, and PPSV/I), and bits 11, 12, and 13 of the PSL register (PSLRNG0, PSLRNG1, and PSL V/I).

When PPSV/I is high, PSLV/I is automatically low, and the PMU operates in voltage forcing/current measuring mode. The current

range information from PSLRNG0 and PSLRNG1 is then gated through C6-6 (range 3) to set flip-flop C7-B to operate relays K3, K4, and K5; through D6-6 (range 2) to set C7-A to close relay K2; through C6-8 (range 1) to set E7-B to close relay K1; or (in the case of range 0), no relays are closed.

Similarly, when PPSV/I is low, PSL V/I is automatically high, and the PMU operates in current forcing/voltage measuring mode. In this case the current range information from PPSRNG0 and PPSRNG1 is decoded and used to close relays K1-5 accordingly.

The coincidence gates D-7 and F-7 are connected to the flip-flops in such a way as to detect when a relay change occurs, in which case one of the 3 points F7-6, D7-8, or D7-6 will make a high-low-high transistion. This causes B7-6 to go low-high-low, and starts the one-shot A7, which generates a pulse of 4.2 milliseconds (typical) width. While the one-shot is on, A7-8 is high and A7-6 is low. This brings A3-8 low, and generates a tester busy signal TBSY/. B7-8 is brought high, which enables the entire set of relay drivers for 4.2 msec, thereby generating the 4.2 msec pulses into the relays--set or reset according to the outputs of the flip-flops E7 and C7.

Also shown on this page is the comparator interface logic. The A/D COMP signal comes from the comparator on the Analog #1A board, while the DCTG/LT is from bit 13 of the DCT register. The circuit composed of D4-2, F6-2, A6-6, A6-8, and A6-3 is an exclusive OR function, which generates a PASS signal according to the truth table shown. This PASS signal then goes to pin D1-5 (page 1), and is used in conjunction with the DCSTROBE to generate the DC FAIL data for DCT bit 14.