SENTRY

DISC INTERFACE MANUAL

FAIRCHILD
SYSTEMS TECHNOLOGY
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

DISC INTERFACE MANUAL

Fairchild Systems Tech.
1725 Technology Drive
San Jose, California 95110

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FAIRCHILD
SYSTEMS TECHNOLOGY

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BURROUGHS 9370/6 DISC MANUAL	
OR	
ALPHA DATA INC. AD9370 DISC MEMORY MANUAL.	
The manual to be used will depend on disc that the system has tied to it.	

1.0 INTRODUCTION

The FST-1 Disc Control Unit (DCU) in conjunction with the disc provides the FST-1 with a large data base. See Table 1.0.1 for size. The maximum transfer rate of the data is 113,000 words per second with each word containing 24 bits of data.

The organization of the DCU is such that the data is word-string oriented and little attention need be given to data blocking by the user. The disc is addressed by track with 80 segments per track and 48 words per segment. This gives a total of 3840 words per track. The track and segment addresses are Binary Coded Decimal information and are supplied only once per word-string as an origin. The DCU is interfaced to the FST-1 Central Processor and Memory through a Common Peripheral Interface (CPI). Refer to diagram on page 1.0.2 for details.

TABLE 1.0.1

Disc Type	Number of Tracks	Total Word Capacity
Burroughs B-9370/6	200 (000-199)	768,000
Alpha Data AD9370	192 (000-191)	737,280

REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPROVAL
1	REL PER EN # 2890	SBO	2-24-70	

DISC

LINE RECEIVERS 8

LINE DRIVERS 9

LINE RECEIVERS 8

LINE DRIVERS 9

WI 1-6

RI1-4 → B1

RI1-6

PARITY GENERATOR AND COMPARATOR
PX1-6
PCMP
8

FCLP
INDX
SACP
LPCP
SURL & OTHERS

DISC SYNC LOGIC
IM
BTR
SNF, PR
5

RI1-6

C REGISTER
C0-C5 | C6-C11 | C12-C17 | C18-C23
6 | 7

CLOCK GATING LOGIC
3

TRACK ADDRESS COUNTER (B.C.D.)
NBTA, TA200
4

BITS 8-16

BITS 0-7

SEGMENT ADDRESS COUNTER (B.C.D.)
NBSA, SCO, CK
5

END WORD COUNTER
EWC1L
EWC2
4

BITS 0-14

B3 → RI1-4

SEGMENT ADDRESS MATCH
SAMC
5

MODE CONTROL LOGIC
BSST
I
SGSH
WR
BSY.
DMT
IOP
1

MEMORY REQUEST LOGIC
MRR
MQ
2

SEGMENT WORD COUNTER (BINARY)
SWC2
SWC4-7, SWC4B
4

BITS 0-23

QUARTER WORD RING COUNTER
D1, D2, D3, D4
4

B REGISTER
B0-B11 | B12-B23
6 | 7

INSTRUCTION DECODE
1

STATUS LOGIC
DNR
DPERR
DOV
TAOV
DCBERR
DDS
2

INITIALIZATION PHASE RING COUNTER
I0, I1, I2, I3, I4, I5
4

BITS 0-23

BITS 16, 17

BITS 0-2, 23

95206000-20 | 1

PERIPHERAL DATA BUSS

COMMANDS

IB20-23

DISC COMMON PERIPHERAL INTERFACE
DEVICE CODE -070
INTERRUPT PRIORITY - B
INTERRUPT ADDRESS -07
MEMORY PRIORITY -5

DISC P.C. BOARDS

1	DISC CONTROL A
2	DISC CONTROL B
3	DISC INTERFACE C
4	D.C.I. ADDRESS
5	DISC SYNC - DISC SYNC
6	CHANNEL TIME-OUT & MEMORY REQUEST
7	CHANNEL TIME-OUT & MEMORY REQUEST
8	PARITY GENERATOR
9	LINE DRIVERS

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION

REFERENCE DRAWINGS | NEXT ASSY | MDL

MATERIAL | TREATMENT | FINISH

TOLERANCES AND NOTES UNLESS OTHERWISE SPECIFIED
DECIMAL ANGLES
X ± .1 ± 2°
XX ± .03
XXX ± .010

⊥ PERPENDICULAR
∥ PARALLEL
⊙ CONCENTRIC
— FLAT OR STRAIGHT-
✓ SURFACE ROUGHNESS

BREAK ALL SHARP EDGES .010 MAX DO NOT SCALE THIS DRAWING

NEXT ASS'Y | MODEL FST-1

DRAWN RS 2-19-70
CKD
MECH. ENGR. 2/24/70
ELEC. ENGR.
MFG 3-2-70
PROJ. ENGR.

FAIRCHILD SYSTEMS TECHNOLOGY

TITLE
DISC CONTROL UNIT

SIZE D | NO. 95206000-20

SCALE | SHEET 1 OF 1 | REV 1

1.0.2

2.0 THEORY OF OPERATION

This section is a brief discussion of DCU operations. For a detailed analysis, refer to the logic flow diagram of Appendix 3.0.

The DCU is an extension of main memory. Large (or small) data blocks may be rapidly transferred to or from core memory through a direct memory access channel in the CPI. To program the DCU for a data transfer, a 3 word Data Control Block (DCB) must be stored in memory. Before issuing a SPU data transfer instruction (RD,ARD, or WRIT),the Accumulator must be loaded with the address of the first word of the DCB. The SPU will transfer that address to the DCU which then fetches the 3 words of the DCB to initialize itself for the data transfer. As a buffered I/O controller, the DCU will "control itself" until the operation is complete and an interrupt has been issued.

Data Control Block

The Data Control Block for the DCU has 3 words. The first word is the Block Length (i.e., number of words to be transferred), in binary format. The second word is the File Origin (i.e., starting address in core memory for the data transfer), also in binary format. The third word is the Disc Address (i.e., the starting track and segment address on the disc) which must be in B.C.D. format.

Disc Addresses

The Disc is addressed in Binary Coded Decimal format for

both tracks and segments. The disc is sectioned with "N" tracks (See Table 1.0.1) and 80 segments per track (00 through 79). Refer to Figure 4.0.1 in Appendix 4.0 for detailed information on Disc Data Organization.

For data transfers to or from the disc that are longer than one segment or even one track, the DCU will automatically increment the disc address so that the user need not be concerned with addresses other than the origin.

Initialization Phase

The DCU Initialization Phase (I) begins with the accepting of the SPU data transfer command. The Initialization Phase is used to fetch the information in the DCB. A minimum of 5 memory cycle times are required to complete this phase and each of these cycle times constitute a subphase In.

The first I phase is I0. I0 is not a complete computer cycle but is true until the next T5 time to provide synchronization at which time the I counter is advanced to I1.

During I1 the DCB address (which is on the Accumulator Buss, BN) is loaded into the CPI Memory Address Register (MAR) through the PDB buss with signal LMARD and a request to read from that address is initiated (RMEM). If no errors occur and memory access is granted (MACG), the I counter is advanced to I2 at T5 time.

During I2 the first word of the DCB, Block Length, is loaded into the End Word Counter (EWC) at T1 time, the MAR is advanced, and a new request to read from memory is initiated. If no errors

occur and memory access is granted, the I counter is advanced to 13 at T5 time.

During 13 the second word of the DCB,File Origin, is temporarily stored in the B register, the MAR is advanced, and a new request to read from memory is initiated. If no errors occur and memory access is granted, the I counter is advanced to 14 at T5 time.

During 14 the third word of the DCB, Disc Address, is stored in the Track and Segment Address Counters, the contents of the B register is transferred to the MAR which now has the memory address of the file origin. If, at this time, the SPU was a WRIT, a memory request to read the first data word from memory is initiated.

Nothing occurs during 15 unless the SPU was a WRIT. For a WRIT the first data word is stored in the B register and the MAR is incremented. At the end of 15 the DCU enters the Segment Search Phase.

Segment Search Phase

The Segment Search Phase (SGSH) is no longer synchronous with the CPU; the main timimg now comes from the disc clocks.

In the SGSH phase the DCU has a disc address in the Track and Segment Address Counters which it is trying to find on the disc. The Track Address portion goes directly to the disc where that track is selected. To find the correct Segment Address, the DCU has the ITSL line (Information Track Select) false so that segment address characters (2 per segment, lower order decade then higher order decade) will be presented to it on the RInL lines (Read lines).

At the Segment Address transfer time (SACP), the DCU will compare its address with the ones coming from the disc until it gets an exact comparsion of both decades (SAMC) at which time it enters the Data Transfer Phase. If the desired segment is not found in something less than 2 revolutions of the disc, the DCU will abort with the error, Segment Not Found (SNFD).

Data Transfer Phase

When the DCU has found the proper segment, it will signal the disc that data transfers are ready to begin by making the ITSL line true and by setting the WISL line true for write or false for read. The basic timing here is the FCLP (File Character Clock Pulse) which exists for each 6 bit character transferred and the FCLP deriviatives, RCP1 and RCP2.

The buffer register to the disc is the C register which transfers 6 bit characters to or from the disc for write or read respectively. A Quarter Word Counter with phases D1, D2, D3, and D4 counts the number of 6 bit characters per 24 bit computer word. At the end of the fourth count (D4), the C register is refilled from the B register if the operation is a write or the C register is transferred to the B register if the operation is a read. The B register operates synchronously with the CPU for transfers of 24 bit words to or from core memory.

Also at the end of D4, two other counters are changed. The Segment Word Counter (SWC) is incremented and the End Word Counter (EWC) is decremented. The Segment Word Counter is keeping track

of the place in the segment; legal counts are 0 through 47 for data and 48 for a 6 bit longitudinal parity character.

The End Word Counter which was loaded with the Block Length, is keeping track of how far the data transfer has proceeded. It must decrement with each word transferred so the DCU will know when to stop requesting memory access.

During the data transfers as a segment or track address boundry is passed, the DCU will always increment the Track and Segment Address Counters as long as the EWC is not zero. One exception to this is when there is no more space on the disc; this will cause a disc overflow error (DOVF).

If, during a segment transfer the EWC goes to zero, which means the file is exhausted before the number of words in the segment is exhausted, the DCU will switch modes from Read or Write to Read without Transfer or Write without Transfer respectively. The Read without Transfer and Write without Transfer involve no word transfers between the DCU and memory. This control state is required at the end of the segment cycle in order to provide the proper character checking and/or parity generation to occur. The segment transfers are cyclic and will not be terminated or will not terminate the DCU until both the Segment Word Counter and the End Word Counter of the file are exhausted.

There are no code translations in the data written on the disc. Data is written and read on the disc exactly as it is presented.

Parity

Parity checking for the DCU is accomplished as follows. In writing a file on the disc, a parity character is generated for each segment used. The parity is a 6 bit odd longitudinal parity character computed from the 6 bit data characters written on the disc. It is written in the 49th word (SWC48) of each segment. When reading a file from the disc, parity is again computed as the characters are transferred to the DCU. When the previously written parity character is read, it is compared with the new parity character (PCMP) and the two must be the same or the DCU will halt with an error (DPERR).

Interrupts

If the DCU has been enabled for interrupts (PON), it will issue an interrupt (COMINT) when a data transfer operation is completed. If an error occurs during a data transfer operation, the DCU will halt and generate an interrupt. The error is held in the Status Register for interrogation by the software.

DCU Status

Whenever an error occurs in the DCU, the error is stored in the Status Register(Refer to Appendix 7.0) and classification of the error is gated to the IB buss (Refer to Appendix 8.0 and 9.0). The IB buss can be interrogated with STST and ETST command forms of the SPU. The Status Register can be interrogated by a RDS command; resetable errors will be cleared by this action. The current Track and Segment Address may also be interrogated by an ARDS command.

Disc Maintenance Segment

Each track on the disc has a maintenance segment addressed as segment 80. By using the NORMTST switch in the DCU and the diagnostic SPARWRIB, data transfers to and from the disc may be checked without destroying valid user data on the disc.

3.0 LOGIC PARTIONING

This section is provided as an explanation of the DCU logic in its manufactured form (i.e., breakdown is by P.C. board). Each separable block of logic is discussed in reference to the function it performs.

3.1 COMMON PERIPHERAL INTERFACE

The DCU uses a standard Common Peripheral Interface (CPI) specialized by adapter plugs to the DCU device code, interrupt address, interrupt priority, and memory priority. The CPI, which is comprised of 3 boards, is used to interface the DCU to the memory busses and the CPU. Two of the boards are identical (except for adapters) and contain the Memory Address Register (MAR), buss to buss gating, and the option logic for specialization. The third board is used for buss control, interrupt functions, partial command decode, and common peripheral logic functions.

The communication between the DCU and the CPI is accomplished with various control lines and the Peripheral Data Buss (PDBnn). Note: Each peripheral controller and its CPI have a private PDB buss. Although the PDB buss for all controllers has the same name, these busses are not physically tied together.

For a more comprehensive explanation of the CPI, refer to the CPI Manual.

If additional copies of the CPI manual and the CPI logic schematics are available, insert them here for a complete set of documentation of the DCU subsystem.

3.2 DISC CONTROL A

The Disc Control A board is used for instruction decode and Disc mode control logic. Indicator lamps are provided on this board so that the 8 mode functions may be visually checked by maintenance personnel.

Instruction Decode

The Instruction Decode network decodes all valid commands for the DCU. A list of the DCU commands is available in Appendix 6.0. Bits 16 and 17 of the PDB are gated at SELDEV2 time to determine if there will be an information transfer on the accumulator buss (BNnn). If PDB17/ is low there will be a buss transfer. If PDB16/ is low the transfer will be from the DCU to the CPU; if it is high the transfer will be from the CPU to the DCU.

Mode Control Flip-Flops

I - The Initialization Phase flip-flop is true whenever the DCU is being initialized for data transfers.

SGSH - The Segment Search flip-flop is true after Initialization and during the address search of the disc. It will also be true during a track change operation.

WR - The Write/Read flipflop is used to hold the DCU in the proper state during the entire current operation. Normally this ff is in the RESET (Read) condition.

BSY - The Busy flip-flop is true during a data transfer operation from start of initialization until the last word is transferred if no errors occur.

DMT - The Disable Memory Transfers flip-flop is used to inhibit memory transfers during a Read without Transfer or a Write without Transfer operation.

IOP - The Interrupt Upon Termination of OPeration flip-flop is used to store the condition that interrupts are enabled and that a data transfer operation has started. Once set, IOP will stay true until the interrupt is serviced.
Note: The interrupt will not be issued (COMINT) until the present operation is completed (not BUSY) or an error occurs (SERR).

BSST - The Busy Status flip-flop is true whenever the DCU is Busy or an interrupt in pending (IOP).

<u>One-Shots</u>

SAI - The Segment Address Inhibit one-shot is used to provide an inhibit signal whenever an error exists and for at least one clock phase after the error has been corrected.

3.3 DISC CONTROL B

The Disc Control B board is used for the disc Status Register, indicator buss status (IBnn), and memory request logic.

Status Register

DNR - Disc not ready, data transfers cannot be made at this time.

DPERR - Disc Parity Error

INA - Interrupts are enabled (from CPI).

INTINH/- Interrupt inhibit switch (for debugging).

MPRO/- Memory protect switch (located on CPI 3 for debugging).

NORMTST - Normal / test switch (test disc segment 80).

DOV - Data overflow, DCU could not get access to memory in time.

TAOV - Track Address Overflow, the disc is full.

DCBERR- DCB Error, illegal memory or disc address has occured.

IOP - Interrupt pending.

SNFD - Segment not found.

WRINH/- Write to disc inhibit switch (for debugging).

DWINH/- Write to disc inhibit switch (located in disc for program protection).

ERR - An error has occured in the DCU.

Indicator Buss, IBnn

The IB gates classification of DCU status to the control panel indicators GT,EQ,LT, and BE.

For a STST command the response is gated by SPUR1 to the IB as follows: IDLE, IDLERR, BSST, and DNR respectively.

For the ETST command, the response is gated to the IB by SPUR2 as follows: TAOV, DPERR, DOV, DCBERR respectively.

Memory Request Logic

The memory request logic is centered around the two flip-flops Memory Request (MQ) and Memory Request Resync (MRR). MQ operates synchronously with the core memory and MRR operates synchronously with the disc. Together they manage the flow of data through the DCU.

Miscellaneous Logic

Also on this board is the flip-flop Disc Data Select (DDS) which controls the Information Track Select (ITSL) and Write/ Read Select (WISL) lines to the disc.

3.4 DISC CONTROL C

The primary purpose of the Disc Control C board is the generation of clock and gating signals for the general purpose boards of the DCU; the Character Buffer boards, the Disc Counter board, and the Parity Logic board.

There are 4 switches on this board which are used in debugging; NORMTST for testing maintenance segment 80, WRINH to inhibit writing on the disc, INTINH to inhibit interrupts, and ERR to inhibit error interrupts.

There is also a 4 stage one-shot string which generates two short clocks (RCP1 and RCP2) from the disc character clock (FCLP).

3.5 D.C.U. COUNTERS

The Disc Counter board is used for 5 of the counters required in disc operations. The design of this board is such that the degree of specialization for disc requirements is minimal. All specialized inputs to the counters (clocks, data enable signals, and clear signals) are generated external to this board. Each counter is a separate piece of logic with no on-board connections to the other counters.

Track Address Counter

The Track Address counter is a two decade plus one bit counter in 8-4-2-1 BCD code. The counter may be parallel loaded from an external buss or its contents may be written to that buss. The counter outputs are also directly available to the backplane. Decode logic is included to detect a non-BCD format (NBTA) and counter overflow (TA200).

Quarter Word Ring Counter

The Quarter Word Ring Counter is used to count the characters per word transferred to or from the disc (CPU 24 bit words are written on the disc as four 6-bit characters). The signal KLRQWC will set the first stage (D1) and reset all others. With each clock pulse (CPQWC), a "ONE" is shifted around the ring to the next stage.

End Word Counter

The End Word Counter is used to count the number of words that are to be transferred. It must count down with each word

transferred. Since the 9316 devices used will only count up, a complementing scheme is used to simulate a down counter. The complement of the Block Length is loaded into the counter by loading from the inverted PDB buss. With each clock pulse, the counter is incremented until the counter is all ONES. Since the original count was complemented, this state is in effect all ZEROS. At this state the signal EWCZ indicates that all the required words have been transferred. The signal EWC1L will be true when there are one or less words yet to be transferred. The total count capability is 16 bits binary. The two highest bits are tied to Vcc in the DCU configuration for the FST-1.

Segment Word Counter

The Segment Word Counter is a binary counter used to count the number of words in each disc segment. Each segment will hold 48 data words plus 1 parity character. Decoded signals are SWCZ for the first data word, SWC47 for the last data word, and SWC48 for the parity character.

Initialization Phase Counter

The Initialization Phase Counter is used to count the five CPU cycles required to initialize the DCU for a data transfer operation. The signal KLRIPC will set the first stage and reset all others. With each clock pulse (CPIPC), a "ONE" is shifted around the ring to the next stage. Note: The state 10 is used to signify that although the Initialization Phase may have begun, the first data transfer cycle has not.

3.6 DISC SYNC LOGIC

The Disc Sync Logic board is used to synchronize data and address transfers between the DCU and the disc.

Segment Address Counter

The Segment Address Counter is a two decade BCD counter which is used to hold or increment the desired disc segment address. The counter may be loaded from the PDB buss and its contents may be written to the PDB buss. Format detection logic is included to detect a non-BCD address (NBSA), an address greater than 80, or addressing segment 80 in the Normal mode.

Segment Counter Overflow logic (SCO) is provided for two cases. For normal operations data can be written on segments 0-79 and SCO will become true on segment 79 so that the track address will be incremented after writing the parity character for 79. For test purposes the input NORMTST will be low and data can be written (or read) on the maintenance segment (segment 80).

Segment Address Match

To synchronize segment addresses with the disc, the Segment Address Counter outputs are compared with current disc segment addresses which are available on the Read lines (R11-4) during a segment search phase (SGSH). If the lower order decade of the address matches, the flip-flop SAM will be set. If the higher order decade also is a match, SAM will remain set, otherwise it will be reset. If the entire segment address is a match at compare

time (CMP), then SAMC/ will be low.

Index Mark Synchronization

When an index mark signal (INDX) is received from the disc, a one-shot network is triggered to signal its presence (DSTRT). This signal is used to (1) trigger a second one-shot which will "lockout" any extraneous pulses on the INDX line until that region of the disc is passed, and (2) resync the disc with the CPU in flip-flops Index Mark (IM) and Index Mark Resync (IMR). Refer to Figure 4.0.6 in Appendix 4,0 for a better understanding of this logic.

Also included here is the Beginning of Track (BTR) and Segment Not Found (SNFD) flip-flops. SNFD will be true if the desired segment is not found in something less than two complete revolutions of the disc.

Address Presence

The Address Presence flip-flop (ADP) is used to indicate when a segment address is present on the RI lines. A three state binary counter uses this condition in generating the comparison signals to the Segment Address Match flip-flop (SAM). Those signals are GRS1 (gate results of lower order segment decade comparison), GRS10 (gate results of higher order segment decade comparison), and CMP (compare strobe of SAM).

Parity Character Timing

The longitudinal parity character strobe pulse (LPCP) is delayed and shaped in a one-shot network to provide reliable timing.

3.7 DISC CHARACTER BUFFER

The Disc Character Buffer is a 12 bit double rank register used in the FST-1 DCU. Two boards of this type are required in each DCU for FST-1 -- DCU communications. The lower rank of the character buffer is the B register which communicates with the CPI through the Peripheral Data Buss (PDB) in 24 bit parallel data transfers. The upper rank of the character buffer is the C register which communicates with the disc in 6 bit character parallel transfers.

During a Read-from-Disc operation, 6 bit characters are presented to the 6 LSB (least significant bits) of the C register. As each character is presented to the 6 LSB, the preceding character is transferred to the next 6 higher order bits until a complete 4 character (24bit) word is formed in C. This is then transferred to the B register and then the FST-1 core memory.

During a Write-to-Disc operation a 24 bit word is loaded into the B register from the FST-1 (PDB). This word is then transferred to the C register where 6 bit characters are written to the disc from the 6 MSB (most significant bits). With each character transferred the 6 MSB are replaced by the next 6 lower order bits of the C register. (Note: The connections to allow the inter-register character transfers of the C register are made on the backplane so that any size character desired can be formed; e.g., Cn is tied to WCn+6).

Although not used in the DCU application additional inputs

and outputs are provided which allow serial entry and exit of the B and C registers.

Possible register transfers which can be made with the Character Buffer board are:

B reg. to C reg. - parallel

C reg. to B reg. - parallel

B reg. to PDB - parallel

PDB to B reg. - parallel

Backplane to C reg. - parallel

C reg. to Backplane - parallel

B reg. to Backplane - parallel

C reg. to Backplane - serial

Backplane to C reg. -serial

B reg. to Backplane - serial

Backplane to B reg. -serial

3.8 DISC PARITY LOGIC

The Disc Parity Logic board is used to generate and check longitudinal parity (odd) on the 6 bit characters transferred between the DCU and the disc. Also on this board are the line receivers for all signals coming from the disc.

Parity Generator

To generate parity in the write mode, the parity generator is first set all ONES using KLRPX. WP/ will be a low so that the generator can sample each character as it appears in the 6 MSB of the C register CPPX. The effect of this is that each flip-flop in PX will count the number of ones in that bit position of each data character written to the disc. While writing data characters, GCWI/ will be low. At the end on each disc segment, GCWI/ will be high, but PR and GPXWI/ will be high and low, respectively. This condition will cause the contents of PX to be written on the disc as the parity character. In each bit position of PX there will be a ONE if the number of ONES sampled from the data characters was even so that the sum total in that bit position will be odd. If the number of ONES sampled was odd, then the PX bit will be a zero.

Note: The true state on the PX bits has been defined as the normal RESET output because there is no direct SET input on the 9020 flip-flops.

To generate parity for checking in the read mode, R11-6 are sampled instead of C18-23.

Parity Comparator

At the end of a segment in the read mode, the disc parity character on the RI lines is compared with PX using exclusive OR gates to generate PCMP/.

Line Receivers

Line receivers are provided for all lines coming from the disc. A 100 ohm termination is provided and positions are available for filter capacitors.

3.9 LINE DRIVER BOARD

The Line Driver board is used to provide high current drivers for 25 interface signals. The drivers are separated into four groups of 7-6-6-6 to provide different gating schemes. In the DCU the gating functions GATEA,B,C,D are tied to Vcc on the backplane. For DCU applications, a diode is provided in the driver output to allow the signals to go below ground. This is required to match the CTL interface levels in the disc.

4.0 DIAGNOSTICS

The operating instructions for the disc diagnostics can be found in the Sentry CPU and Peripheral Diagnostics Manual, part number 67095570.

APPENDIX I.0

DISC CONTROL UNIT

MNEMONICS

ADP-(ff) Segment Address Presence, an address is available for comparison on the RI lines.

Bn- B Register bit n (n=0,11)

BSERI- B Register serial input (not used in DCU).

BSERO- B Register serial output (not used in DCU).

BSST-(ff) Busy status (DCU busy or interrupt pending).

BSY-(ff) DCU is busy

BTR-(ff) Beginning of track

Cn- C Register bit n (n=0,11).

CDIO- Command DCU do I/O operation.

CDXF- CPI control decode data transfer.

CLEAR- CPU reset signal.

CMP- Compare time for SAM.

COMINT- Command an interrupt.

CONA- CPI control decode "A".

CONB- CPI control decode "B".

CONC- CPI control decode "C".

COND- CPI control decode "D".

CONE- CPI control decode "E".

CPB- Clock pulse to B register.

CPC- Clock pulse to C register.

CPDPE- Clock pulse to Disc Parity Error.

CPEWC- Clock pulse to End Word Counter.

CPIPC- Clock pulse to Initialization Phase Counter.

CPQWC- Clock pulse to Quarter Word Counter.

CPSAC- Clock pulse to Segment Address Counter.

CPSAM- Clock pulse to Segment Address Match.

CPSWC- Clock pulse to Segment Word Counter.

CPTAC- Clock pulse to Track Address Counter.

CSERI- C Register serial input (not used in DCU).

CSERO- C Register serial output (not used in DCU).

CTST- CPI control decode test instruction.

Dn- Quarter Word Ring Counter phase n.

DCBERR-(ff) Data Control Block error.

DDS-(ff) Disc data select.

DMT-(ff) Disable memory transfers.

DNR-(ff) Disc not ready.

DOV-(ff) Data overflow, DCU could not access memory in time.

DRDY- Disc is ready.

DSTRT- Disc, start of track origin.

ERR- Error in DCU.

EWCn- End Word Counter, bit n.

EWCIL- End Word Counter equals one or less.

EWCZ- End Word Counter equals zero.

FCLP- Read (or write) charcter clock pulse (from disc).

GBC- Gate B register to C register.

GBP- Gate B register to P buss.

GCB- Gate C register to B register.

GCnCn6- Gate C register bit n to bit n+6.

GCWI- Gate the 6 M.S.B. of C to the disc write lines.

GCPS- Gate clock pulse to Segment Address Counter.

GPB- Gate P buss to B register.

GPEWC- Gate P buss to End Word Counter.

GPTASA- Gate P buss to Track Address and Segment Address Counters.

GPXWI- Gate the Parity Generator to the disc write lines.

GRSI- Gate results of lower order decade of segment address comparison to SAM.

GRSIO- Gate results of higher order decade of segment address comparison to SAM.

GTASAP- Gate Track Address and Segment Address Counters to P buss.

I-(ff) Initialization Phase Mode.

In- Initialization Phase n.

IBnn- Indicator Buss bit nn (nn=20,21,22,23).

IDLE- DCU not busy.

IDLERR- DCU idle with error.

IM-(ff) Index mark presence.

IMR-(ff) Index mark resync.

INA- CPI interrupts enabled.

INDX- Index pulse (from disc).

INTINH- Interrupts are inhibited (switch).

IOP-(ff) Interrupt upon termination of operation.

ITA- Increment track address

KLRB- Clear B register.

KLREWC- Clear End Word Counter.

KLRIPC- Clear Initialization Phase Counter.

KLRPX- Clear Parity Generator.

KLRQWC- Clear Quarter Word Counter.

KLRS- Clear Segment Address Counter.

KLRSTAT- Clear Status Register.

KLRSWC- Clear Segment Word Counter.

KLRTAC- Clear Track Address Counter.

KSAM- Clear Segment Address Match.

KSAMI- Clear Segment Address Counter.

LDnn- Line driver nn (nn=1-25).

LMARD- Load Memory Address Register from P buss (to CPI).

LPn- Lamp circuit n (n=1-8).

LPC- Longitudinal parity character clock pulse (buffered).

LPCP- longitudinal parity character clock pulse (from disc).

LPDC- Delayed longitudinal character parity clock pulse.

LSAC- Lower order decade of Segment Address Counter.

MACG- Memory access granted (from CPI).

MOVF- Memory overflow (from CPI).

MQ-(ff) DCU memory request.

MQROR- Memory request "OR".

MRR-(ff) Memory request resync.

MSAC- Higher order decade of Segment Address Counter.

NBSA- Non BCD segment address.

NBTA- Non BCD track address.

NORMTST- Normal/test switch, test segment80.

OPIPR- Operation in progress.

PCMP- Parity character comparison output.

PDBnn- Peripheral Data Buss bit nn (nn=00-23).

PDCLK- Peripheral delayed clock.

PECLK- Peripheral early clock.

PIA- Priority interrupt acknowledged (from CPI).

PNBSY- Peripheral Data Buss busy (to CPI).

PPTn- Peripheral Phase time n.

PR-(ff) Parity character time.

PXn-(ff) Parity Generator bit n (n=1-6).

RCP1,2- Delayed character clock pulses 1 and 2.

RDST- Read Status Register to P buss.

RESET- Control panel "RESET" switch.

RIn- Disc read data lines (n=1-6).

RMEM- Read memory (to CPI).

RP- Read data from disc for parity checking.

RQM- Conditions for request for memory exist.

Sn- Segment Address Counter bit n.

SACP- Segment Address Clock Pulse (from disc).

SAI- Segment address decode inhibit one-shot.

SAM-(ff) Segment Address Match.

SAMC- Segment Address Match Compares.

SCO- Segment Address Counter Overflow.

SERR- Some error in DCU.

SELDEV- Select this device (from CPI).

SGSH-(ff) Segment Search phase of DCU.

SK-(ff) Suppress count of Segment Address Counter in test mode.

SNFD-(ff) Segment not found.

SPUR1- Gate SPU command response type 1 (STST) to IBnn.

SPUR2- Gate SPU command response type 2 (ETST) to IBnn.

SS1-(ff) Status request state 1.

SS2-(ff) Status request state 2.

SWCnn- Segment Word counter count nn.

SWCZ- Segment Word Counter equals zero.

TAnn- Track Address Counter bit nn.

TA200- Track Address Counter count 200 (illegal).

TAOV-(ff) Track Address overflow.

TSL- Information track select (to disc).

VALDAT- Valid data (to CPI).

WCnn- Write C Register bit nn.

WIn- Write data lines (to disc).

WMEM- Write memory (to CPI).

WP- Write data to disc and generate parity.

WR-(ff) Write/Read control.

WRINH- Write to disc inhibit switch.

WS- Write select (to disc).

DISC CONTROL UNIT

LOGIC EQUATIONS

NOTE: (#) Denotes a direct input to flipflops.

(↑) Denotes SET conditions.

(↓) Denotes RESET conditions.

ADP↑ = (PDCLK).SAI/.SACP.SGSH

ADP↓ = (PDCLK).(SGSH+CMP)

+(#) CLEAR

BSST↑ = (PDCLK).BSY.IOP/

BSST↓ = (PDCLK).BSY/.IOP/

+(#) CLEAR

BSY↑ = (PDCLK).CDIO.IOP/

BSY↓ = (PDCLK).I/.(SERR+(MQROR.WR/.SWCZ.BSY.EWCZ.DI))

+(#) (CLEAR+(WR.LPCP.SWCZ.I/.BSY.EWCZ.DI))

BTR↑ = (PDCLK).I/.IM.BSY

BTR↓ = (PDCLK).SGSH/.(BSY/+EWCZ+SCO)

+(#) CLEAR

CDIO = SPUA.SPUR/.CDXF.(RD+ARD+WRIT)

CLEAR = RESET

COMINT = IOP.INTINH/.(BSY/+ERR)

CPB = GPB.PECLK+GCB.RCP2

CPC = RCPI.(GBC+GCnCn6)

CPDPE = PR.RCPI+BSY/.PECLK

CPEWC = GPEWC.PECLK+OPIPR.EWCZ/.SWC48/.RCP2.(WR/.D4+WR.DI)

CPIPC = PECLK.I.(IO+PPT5(MACG+I4))

```
CPQWC = RCP2.SWC48/.TSL

CPSAC = GPTASA.PECLK+LPC.SCO/.1/.SK/.SGSH/

CPSAM = ADP.RCP1

CPSWC = OP1PR.D4.SWC48/.RCP2

CPTAC = GPTASA.PECLK+1TA.INDX

DCBERR↑= (PDCLK).BSY.(15.(NBTA+NBSA)+SWCZ.11/.MQ.MOVF+EWCZ.13)

DCBERR↓= (PDCLK).KLRSTAT

          +(#) CLEAR

DDS↑= (#) SAMC

DDS↓= (WR.LPDC+RCP1.WR/.SWC48).(EWCZ+1TA)

       +(#) CLEAR

DMT↑= (PDCLK).(BSY/+SERR+(EWCZ.1/))

       +(#) CLEAR

DMT↓= (PDCLK).BSY/.1OP/.(RD+WR1T)

DNR↑= (PDCLK).DRDY/

DNR↓= (PDCLK).DRDY

       +(#) CLEAR

DOV↑= (PDCLK). MOVF/.RQM.MQ

DOV↓= (PDCLK).KLRSTAT

       +(#) CLEAR

DPERR↑= PCMP/.D1.WR/.OP1PR.(CPDPE)

DPERR↓= (CPDPE). KLRSTAT

         +(#) CLEAR

DRDY = SURL (from disc)

DSTRT = INDX + 100 nsec.

ERR = SERR.(ERROR SWITCH NORMAL)

GBC = WR.(EWCZ/.D4+BSY.SGSH.D1.MRR/)
```

```
GBP = I4.PPT2+MACG.WR/.I/.PPT5

GCB = WR/.D4.SGSH/

GCnCn6 = SGSH/.I/.SWC48/.(WR/+WR.D4/)

GCWI = WR.SWC48/

GPB = PPTI.MACG.(I3+WR.I/)

GPEWC = I2.PPTI

GPTASA = I4.PPTI

GPXWI = WR.SWC48

GTASAP = SS2.PPTI.BSY/

I↑= (PDCLK).IOP/.BSY/.CDIO

I↓= (PDCLK).(SERR+PPT5.I5.(MACG+WR/))
     +(#) CLEAR

IB20 = SPURI.DNR+SPUR2.DCBERR

IB2I = SPURI.BSST+SPUR2.DOVF

IB22 = SPURI.IDLERR+SPUR2.DPERR

IB23 = SPURI.IDLE+SPUR2.TAOVF

IDLE = DNR/.SERR/.BSST/

IDLERR = BSST/.SERR

IM↑= (PDCLK).IMR.IM/

IM↓= (PDCLK).(IM.IMR+IMR/)
      +(#) CLEAR

IMR↑= (PDCLK).IM.IMR/
       +(#) DSTRT

IMR↓= (PDCLK).IM.IMR
       +(#) CLEAR
```

```
IOP↑= (PDCLK).BSY.INA
IOP↓= (PDCLK).(PIA+INA/.BSY/)
      +(#) CLEAR
ITA = SCO.NORMTST.OPIPR
KLRB = DMT.I/.RCP2.MQROR/
KLREWC = BSY/
KLRIPC = CLEAR + I/
KLRPX = RCP1.D1.SWCZ
KLRQWC = BSY/
KLRS = CLEAR+BSY.I/IM.SGSH/
KLRSTAT = CLEAR+CD10+BSY/.SS1.PPT2
KLRSWC = BSY/+SWC48.LPDC
KLRTAC = CLEAR
KSAM = CLEAR+KSAM1
KSAM1 = ADP/.PECLK
LMARD = 11.PPT1+14.PPT2
MQ↑= (PDCLK).RQM.BSY
MQ↓=(PDCLK).MACG.PPT5
      +(#) BSY/
MQROR = MRR+MQ+MACG
MRR↑= (RCP1).(DMT/.I/.SGSH/.SWC48/.(WR/.D4+WR.D1.EWC1L))
MRR↓= (#) MQ.PPT2+CLEAR
NBSA = S80.(S40+S20) + S8.(S4+S2) + S80.(S1+S2+S4+S8) + S80.NORMTST
NBTA = TA80.(TA40+TA20) + TA8.(TA4+TA2)
```

```
OPIPR = BSY.I/.SGSH/
PDB00/= GBP.B00+GTASAP.S1+RDST.DNR+(CPI SOURCE)
PDB01/= GBP.B01+GTASAP.S2+RDST.DPERR+(CPI SOURCE)
PDB02/= GBP.B02+GTASAP.S4+RDST.INA+(CPI SOURCE)
PDB03/= GBP.B03+GTASAP.S8+RDST.INTINH/+(CPI SOURCE)
PDB04/= GBP.B04+GTASAP.S10+RDST.MPRO/+(CPI SOURCE)
PDB05/= GBP.B05+GTASAP.S20+RDST.NORMTST+(CPI SOURCE)
PDB06/= GBP.B06+GTASAP.S40+RDST.DOV+(CPI SOURCE)
PDB07/= GBP.B07+GTASAP.S80+RDST.TAOV+(CPI SOURCE)
PDB08/= GBP.B08+GTASAP.TA1+RDST.DCBERR+(CPI SOURCE)
PDB09/= GBP.B09+GTASAP.TA2+RDST.IOP+(CPI SOURCE)
PDB10/= GBP.B10+GTASAP.TA4+RDST.SNFD+(CPI SOURCE)
PDB11/= GBP.B11+GTASAP.TA8+RDST.WRINH/+(CPI SOURCE)
PDB12/= GBP.B12+GTASAP.TA10+RDST.DWINH/+(CPI SOURCE)
PDB13/= GBP.B13+GTASAP.TA20+(CPI SOURCE)
PDB14/= GBP.B14+GTASAP.TA40+(CPI SOURCE)
PDB15/= GBP.B15+GTASAP.TA80+(CPI SOURCE)
PDB16/= GBP.B16+GTASAP.TA100+(CPI SOURCE)
PDB17/= GBP.B17+(CPI SOURCE)
PDB18/= GBP.B18+(CPI SOURCE)
PDB19/= GBP.B19+(CPI SOURCE)
PDB20/= GBP.B20+(CPI SOURCE)
PDB21/= GBP.B21+(CPI SOURCE)
PDB22/= GBP.B22+(CPI SOURCE)
PDB23/= GBP.B23+RDST.ERR+(CPI SOURCE)
```

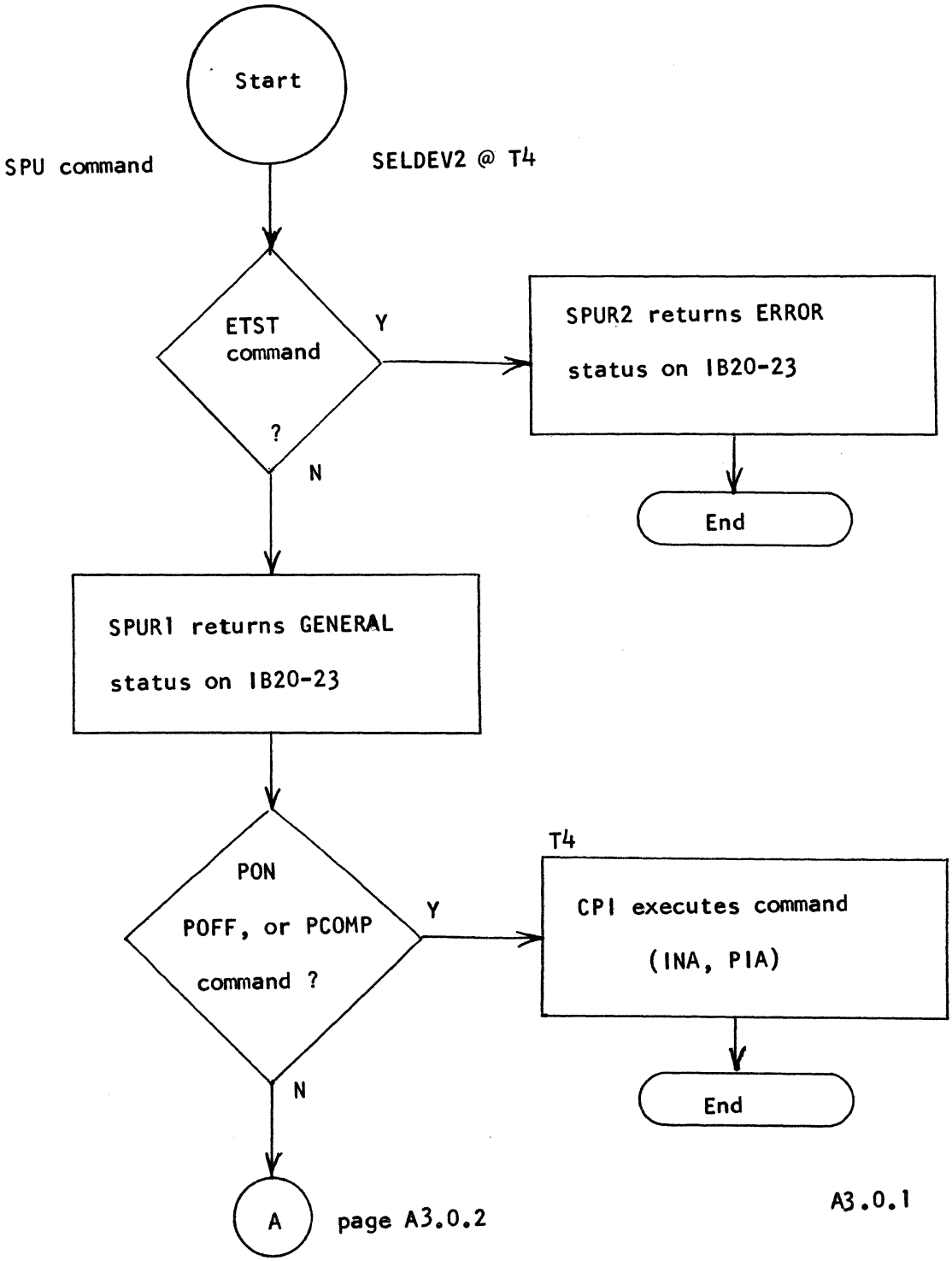
```
PNBSY = VALDAT/

PR↑ = (RCP1).SWC47.D4

PR↓ = (RCP1).(SWC48+BSY/)
      +(#) BSY/

PXn↑ =(CPPX).PR/.PXn/.(WP.Ci+RP.RIn)
      +(#) KLRPX              (n=1-6,i=18-23)

PXn↓ = (CPPX).PR/.PXn.(WP.Ci+RP.RIn)              (n=1-6,i=18-23)

RDST = SS1.PPT1.MQ/.MACG/

RMEM = (MQ+MACG).(1+WR)

RP = WR/.SGSH/.1/

RQM = PPT1.(MRR+11+12+13+15.WR.EWCZ/)

SAM↑ = (CPSAM).LSAC.GRS1

SAM↓ = (CPSAM).MSAC/.GRS10
       +(#) KSAM

SAMC = SAM.CMP

SCO = NORMTST.SM79+NORMTST/.SM80

SERR = DPERR+DOV+TAOV+DCBERR+SNFD+BSY.DNR

SGSH↑ = (PDCLK).PPT5.15.(MACG+WR/)
        +(#) 1/.ITA.EWCZ/.IM

SGSH↓ = (PDCLK).SERR
        +(#) (CLEAR+BSY/+SAMC)

SK↑ = (LPC).NORMTST/.SCO

SK↓ = (#) BSY/

SNFD↑ = (PDCLK).BTR.IM

SNFD↓ = (#) KLRSTAT
```

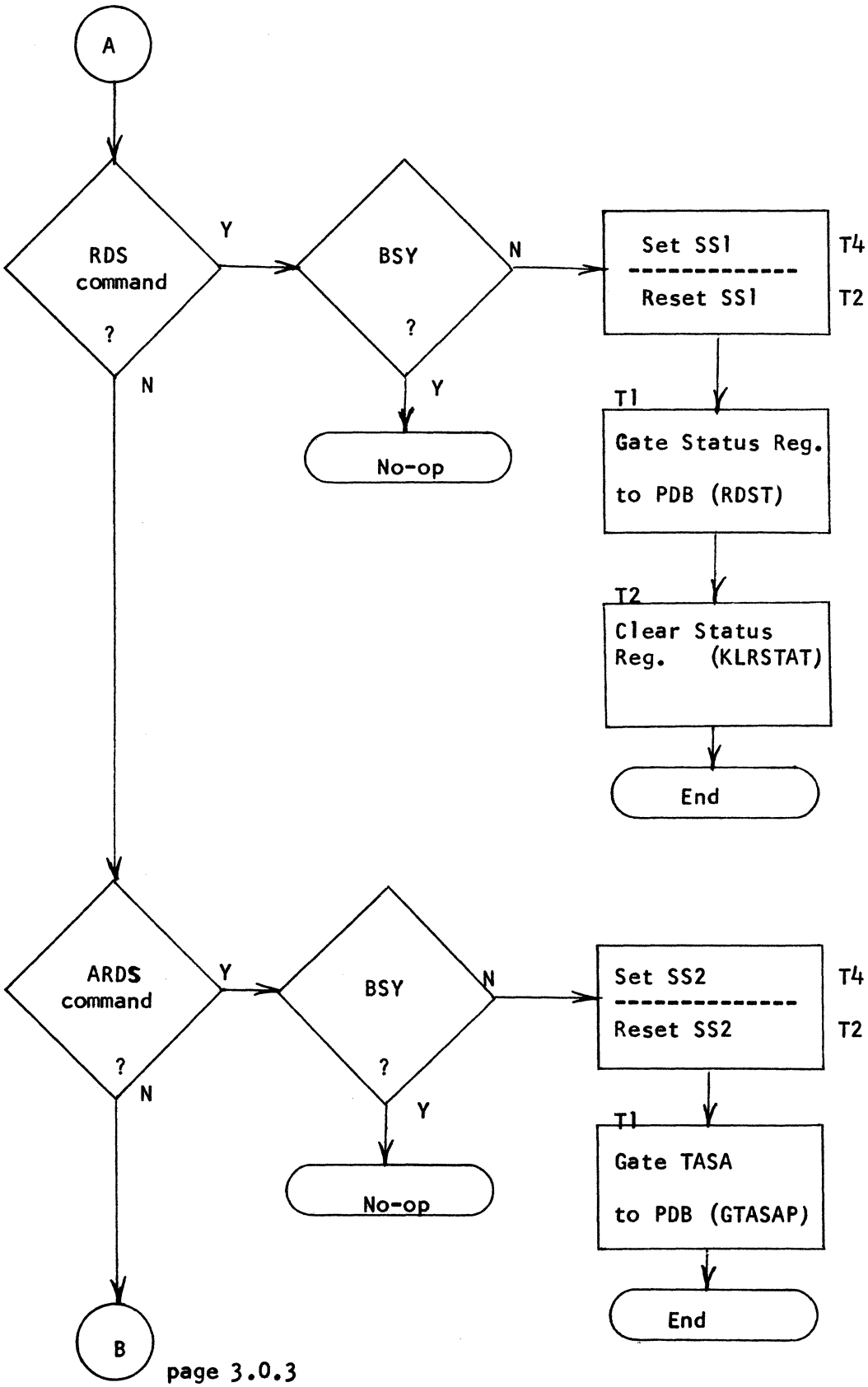
```
SPUR1 = CTST.CONB.COND

SPUR2 = SPUR1/.SELDEV2

SS1↑ = (PDCLK).BSY/.(S.SS1)

SS1↓ = (PDCLK).PPT2

       +(#) CLEAR

SS2↑ = (PDCLK).BSY/.(S.SS2)

SS2↓ = (PDCLK).PPT2

       +(#) CLEAR

TAOV↑ = (PDCLK).EWCZ/.SWCZ.TA200

TAOV↓ = (PDCLK).KLRSTAT

        +(#) CLEAR

TSL = DDS.OPIPR

VALDAT = PNBSY/ = BSY/+11.PPT1+MQ/.MACG/.PPT1.(SS1+SS2)

WIn = GCWI.Ci+GPXWI.PXn            (i=18-23,n=1-6)

WMEM = RMEM/.(MACG+MQ)

WP = WR.SGSH/.I/

WR↑ = (PDCLK).(S.WR).BSY/.IOP/

WR↓ = (PDCLK).BSY/

      +(#) CLEAR

WS = DDS.OPIPR.WR.WRINH/
```

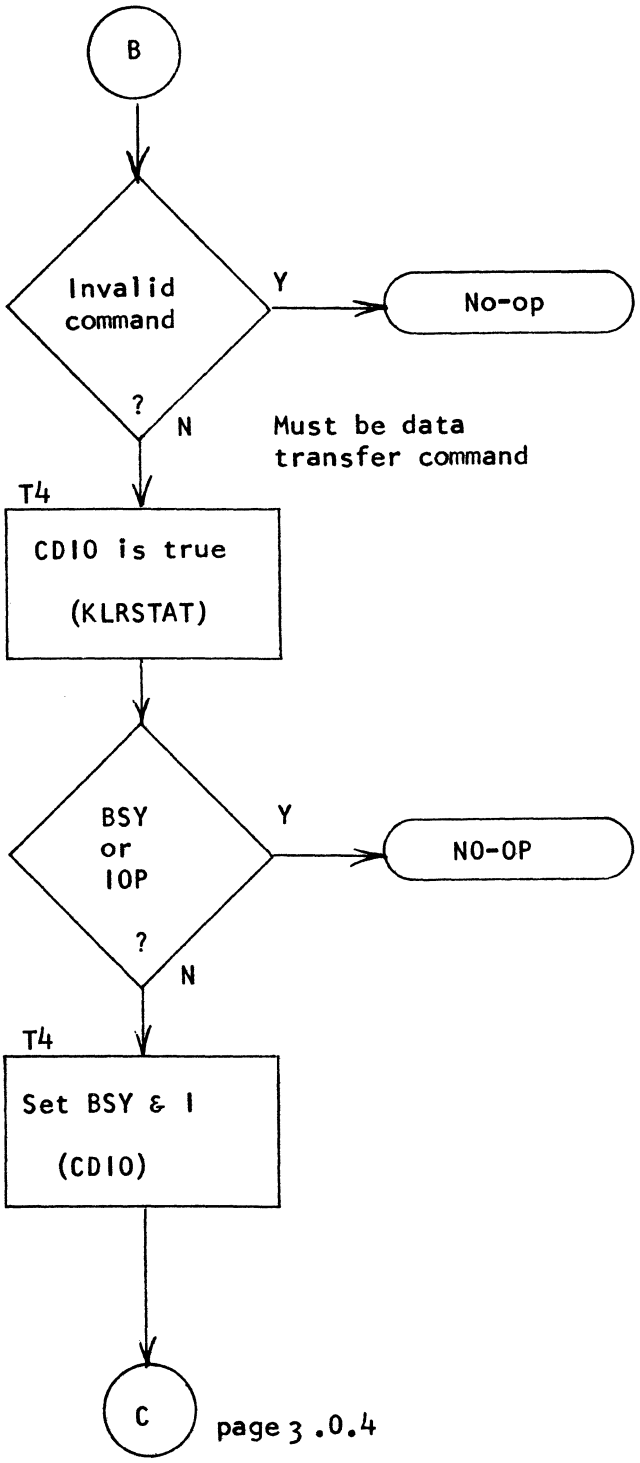
APPENDIX 3.0

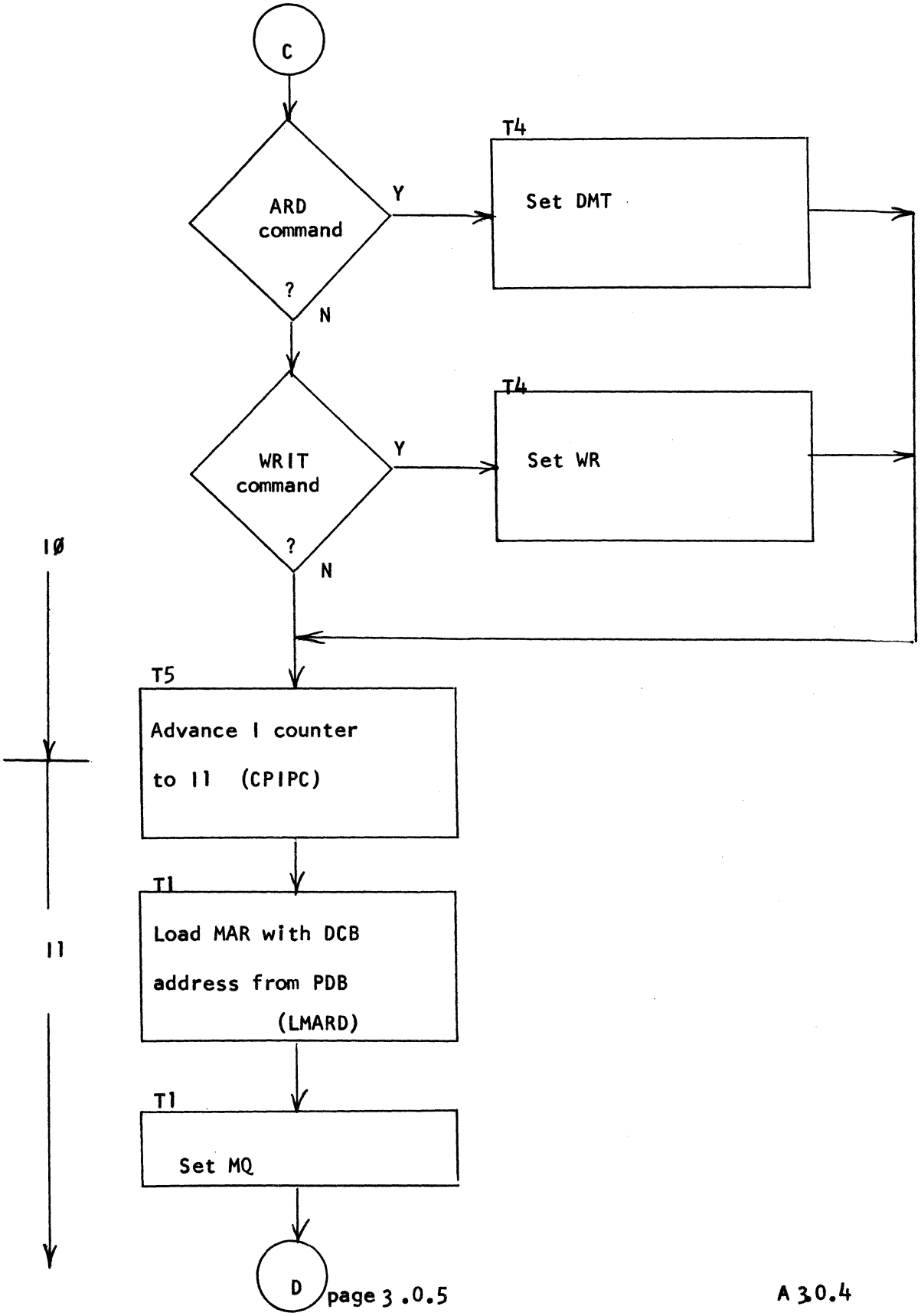
DISC CONTROL UNIT

LOGIC FLOW CHART

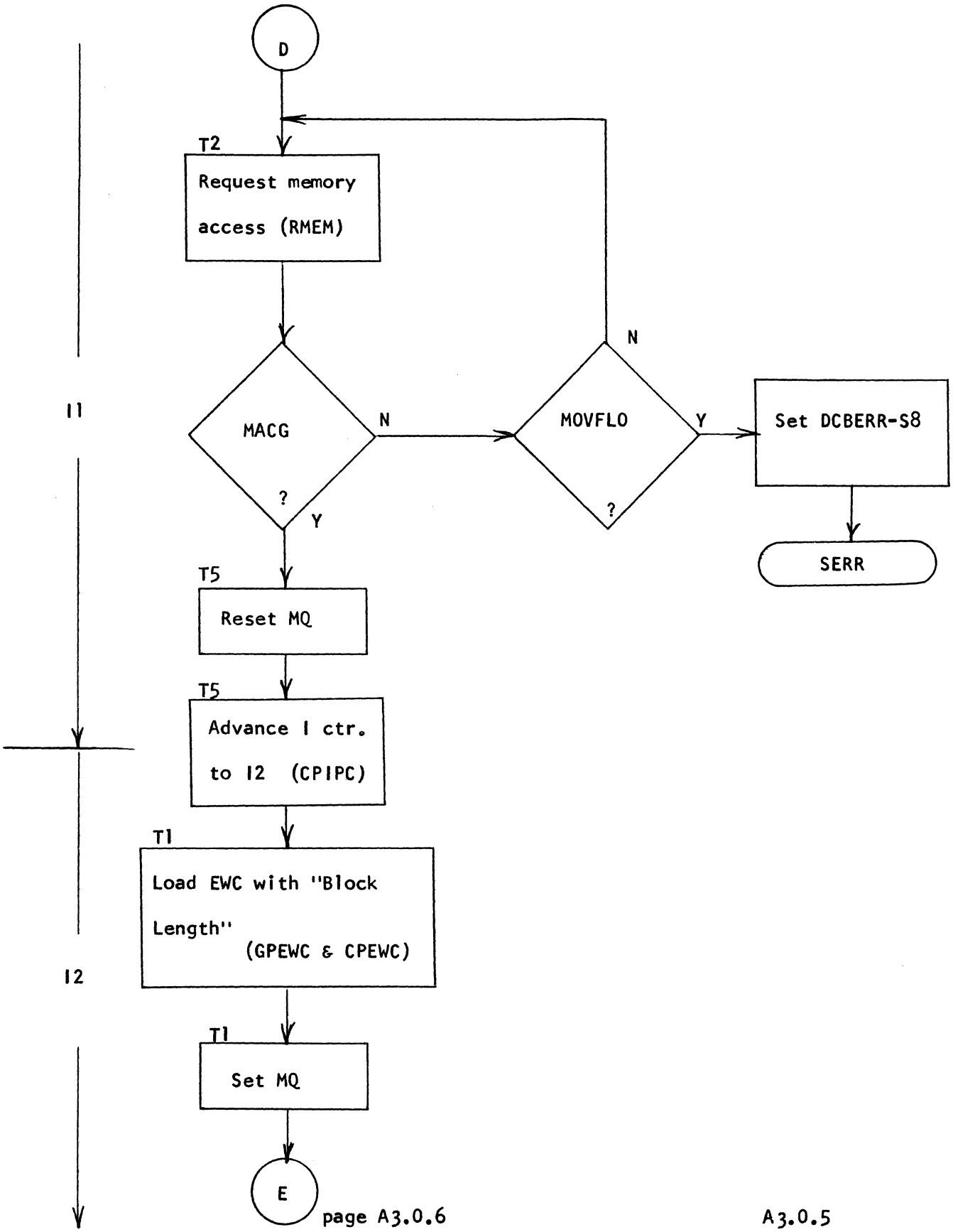



A
RDS command ?
Y
BSY ?
N
Set SS1
Reset SS1
T4
T2
Y
No-op
N
T1
Gate Status Reg. to PDB (RDST)
T2
Clear Status Reg. (KLRSTAT)
End
ARDS command ?
Y
BSY ?
N
Set SS2
Reset SS2
T4
T2
Y
No-op
N
T1
Gate TASA to PDB (GTASAP)
End
B

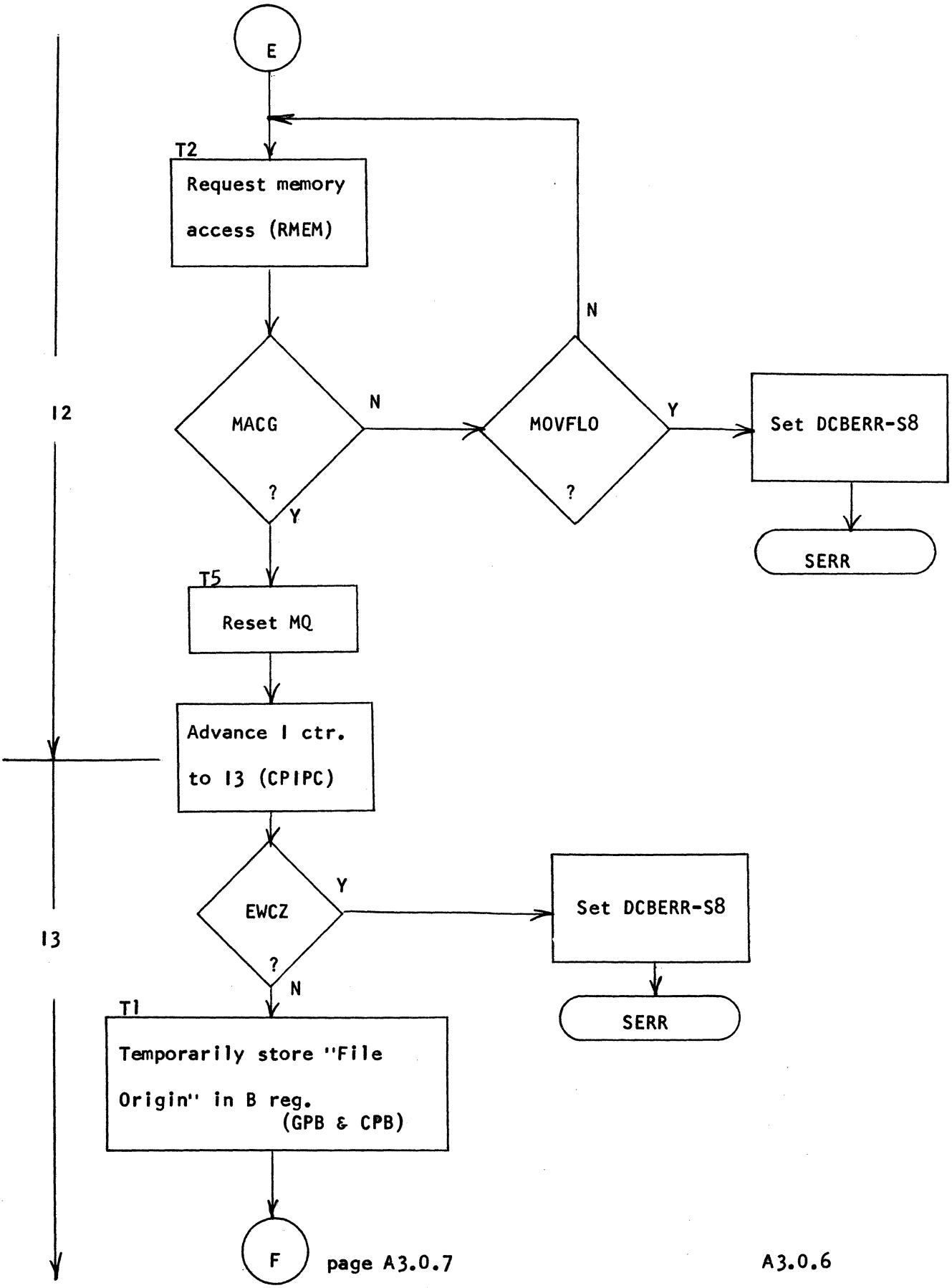

B
Invalid command
Y
No-op
?
N
Must be data transfer command
T4
CDIO is true
(KLRSTAT)
BSY or IOP
Y
NO-OP
?
N
T4
Set BSY & I
(CDIO)
C
page 3 .0.4

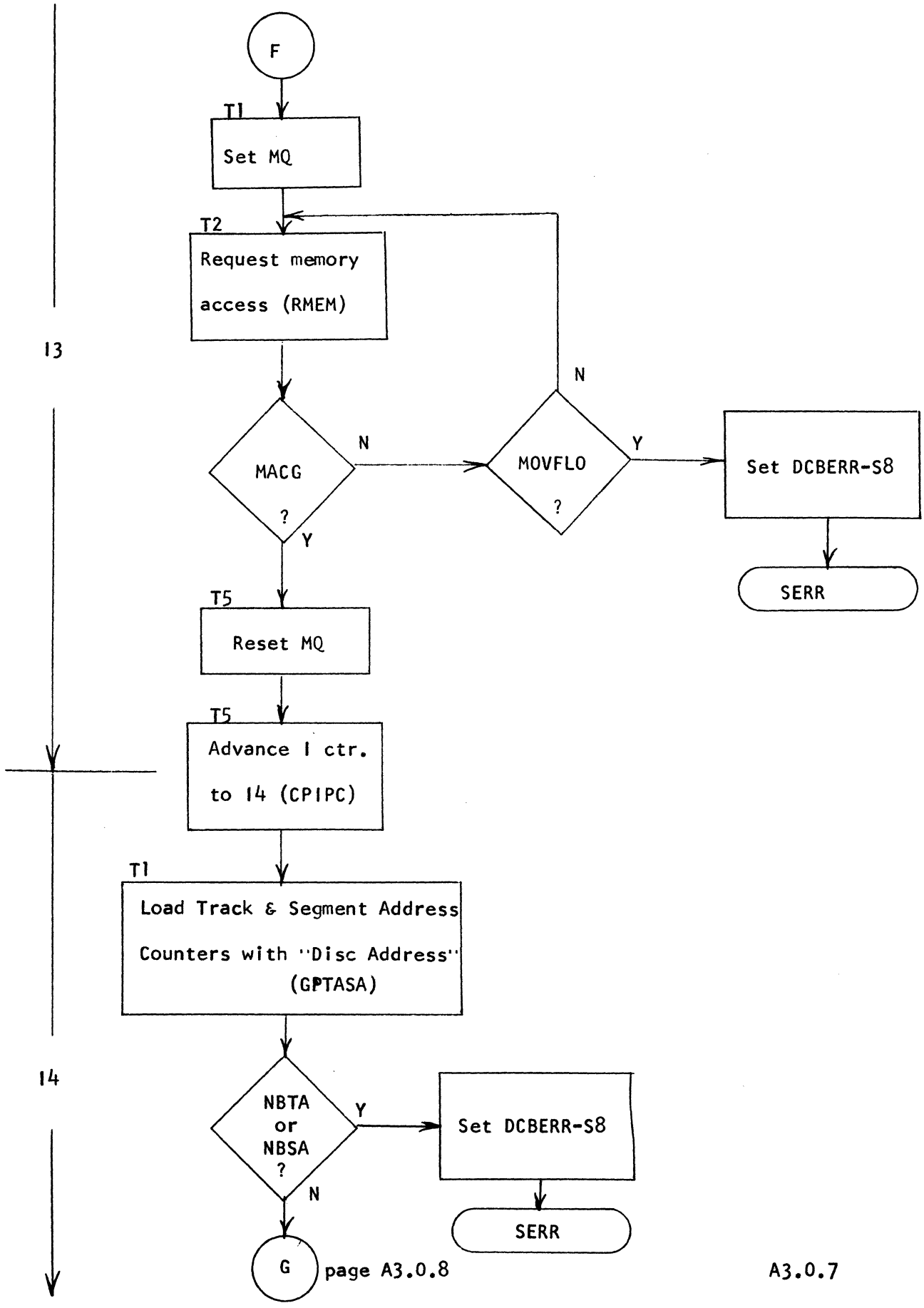

C
ARD command ?
Y
T4
Set DMT
N
WRIT command ?
Y
T4
Set WR
N
10
T5
Advance I counter to 11 (CPIPC)
T1
Load MAR with DCB address from PDB (LMARD)
11
T1
Set MQ
D

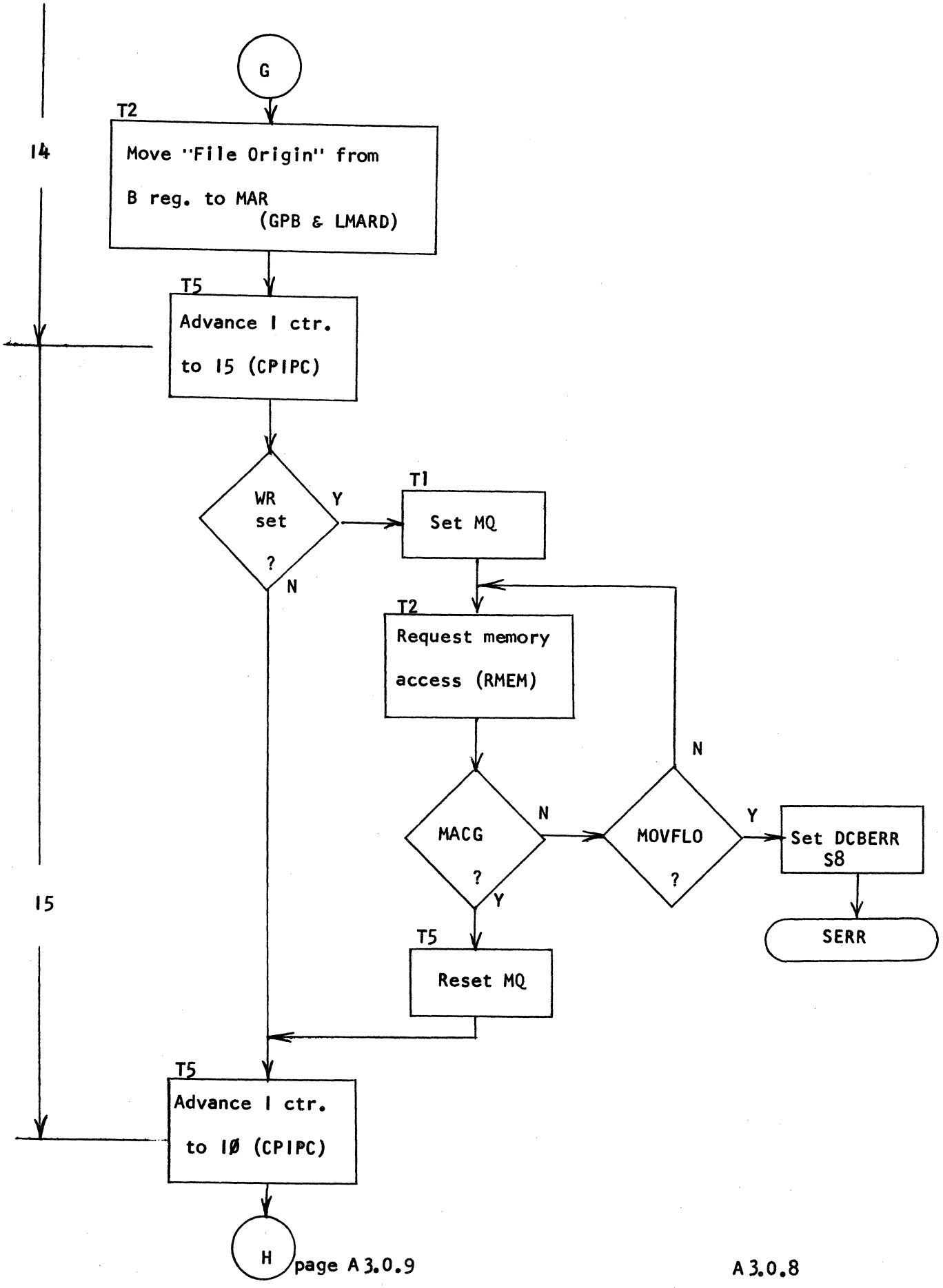
A 30.4

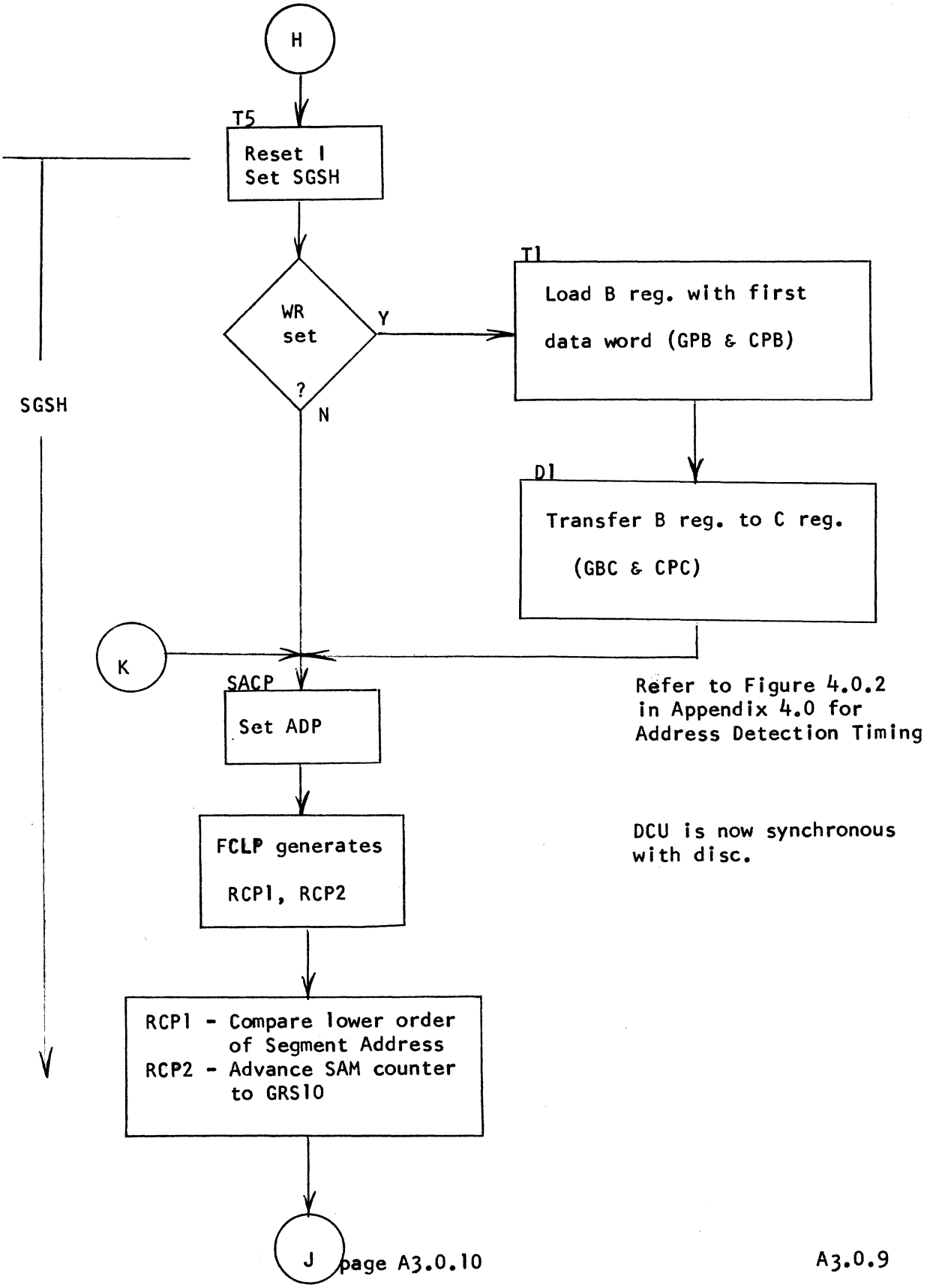

D
T2
Request memory access (RMEM)
MACG
?
N
Y
MOVFLO
?
N
Y
Set DCBERR-S8
SERR
I1
T5
Reset MQ
T5
Advance I ctr. to I2 (CPIPC)
T1
Load EWC with "Block Length" (GPEWC & CPEWC)
I2
T1
Set MQ
E

page A3.0.6


E
T2
Request memory access (RMEM)
MACG
?
N
Y
MOVFLO
?
N
Y
Set DCBERR-S8
SERR
T5
Reset MQ
Advance I ctr. to 13 (CPIPC)
EWCZ
?
Y
N
Set DCBERR-S8
SERR
T1
Temporarily store "File Origin" in B reg. (GPB & CPB)
F
12
13


F
T1
Set MQ
T2
Request memory access (RMEM)
13
MACG ?
N
MOVFLO ?
N
Y
Set DCBERR-S8
SERR
Y
T5
Reset MQ
T5
Advance I ctr. to 14 (CPIPC)
T1
Load Track & Segment Address Counters with "Disc Address" (GPTASA)
14
NBTA or NBSA ?
Y
Set DCBERR-S8
SERR
N
G
page A3.0.8

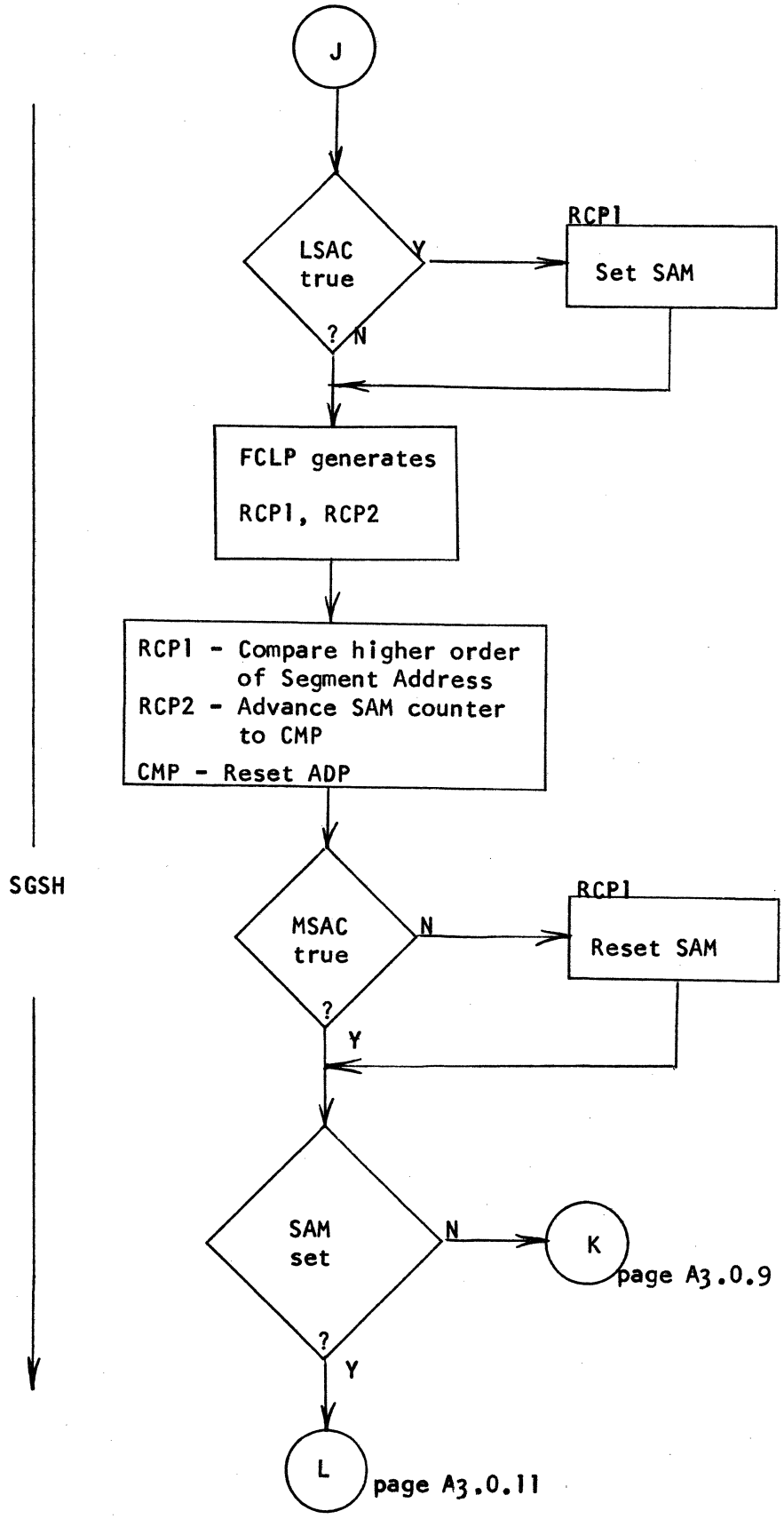

G
T2
Move "File Origin" from
B reg. to MAR
(GPB & LMARD)
14
T5
Advance I ctr.
to 15 (CPIPC)
WR
set
?
Y
N
T1
Set MQ
T2
Request memory
access (RMEM)
MACG
?
N
Y
MOVFLO
?
Y
N
Set DCBERR
S8
SERR
15
T5
Reset MQ
T5
Advance I ctr.
to 1Ø (CPIPC)
H

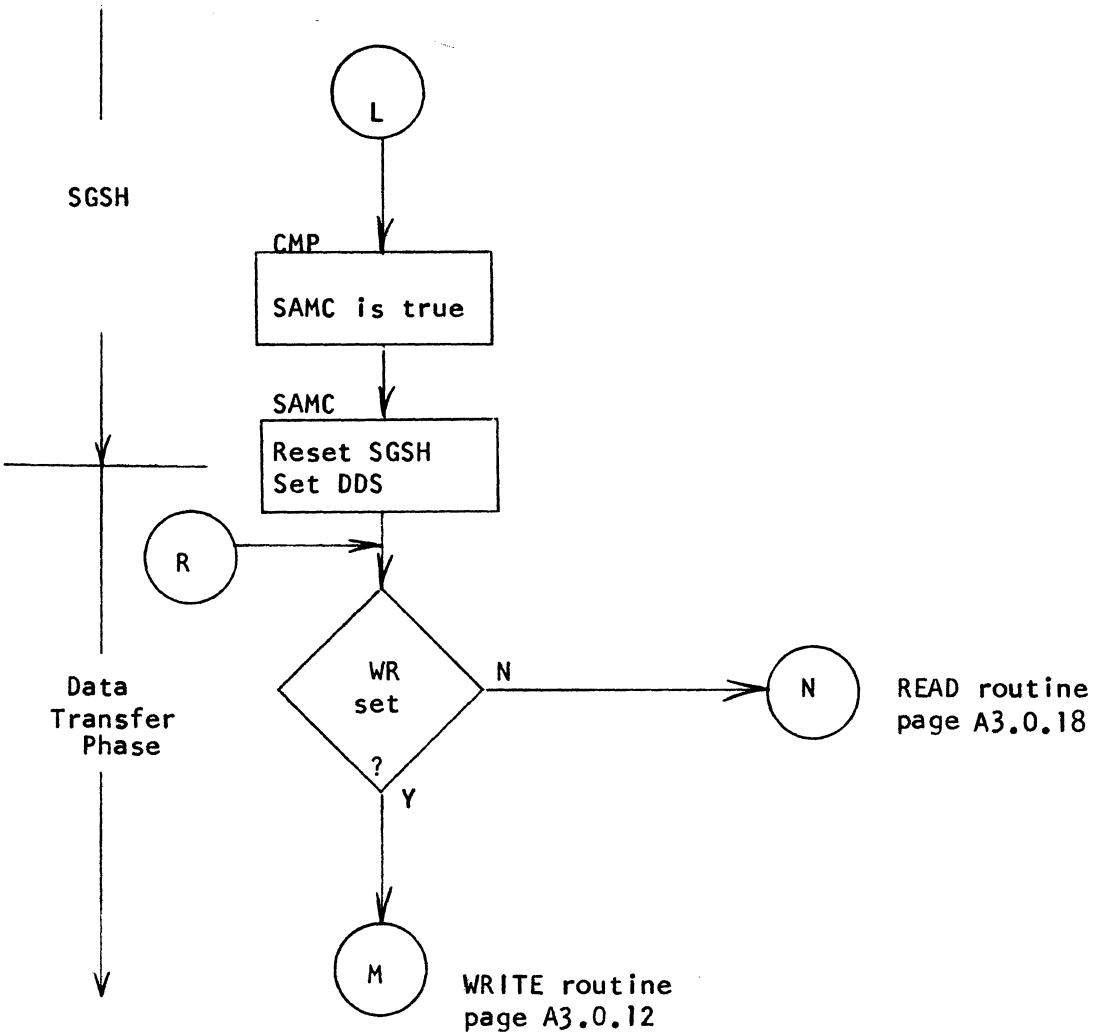


Refer to Figure 4.0.2 in Appendix 4.0 for Address Detection Timing

DCU is now synchronous with disc.

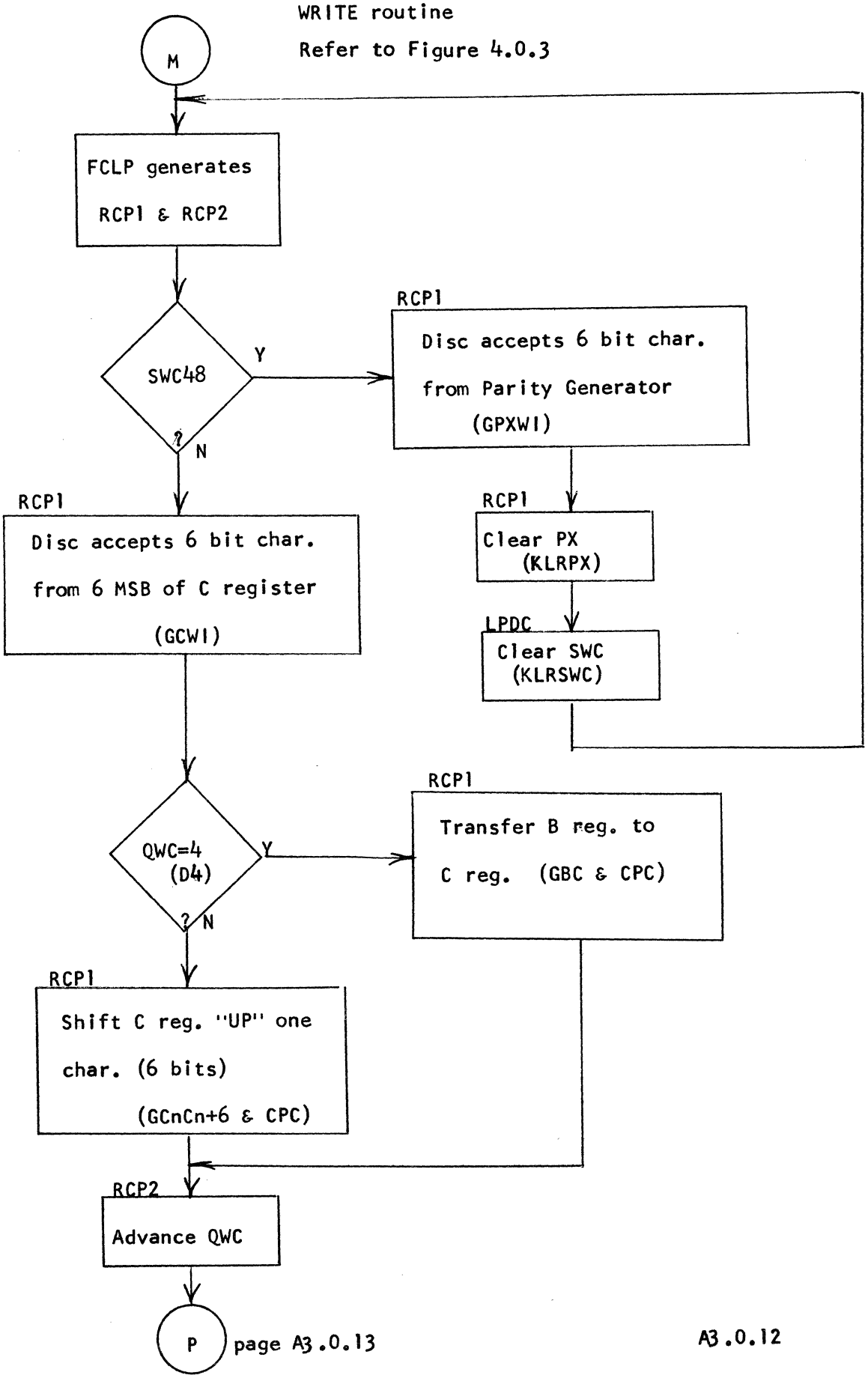
page A3.0.10

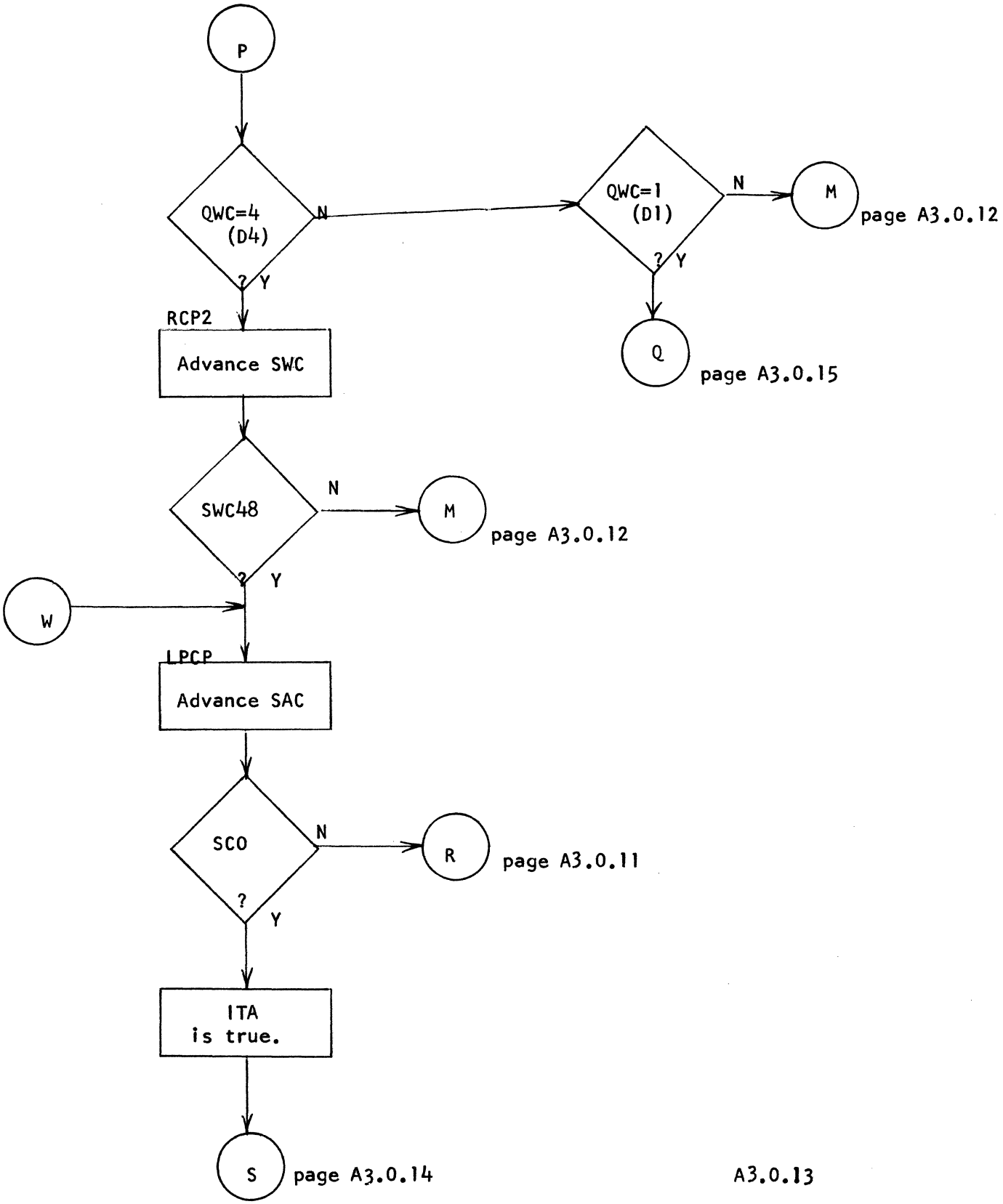

J
LSAC true
Y
?
N
RCP1
Set SAM
FCLP generates
RCP1, RCP2
RCP1 - Compare higher order of Segment Address
RCP2 - Advance SAM counter to CMP
CMP - Reset ADP
SGSH
MSAC true
N
?
RCP1
Reset SAM
Y
SAM set
N
?
K
page A3.0.9
Y
L
page A3.0.11

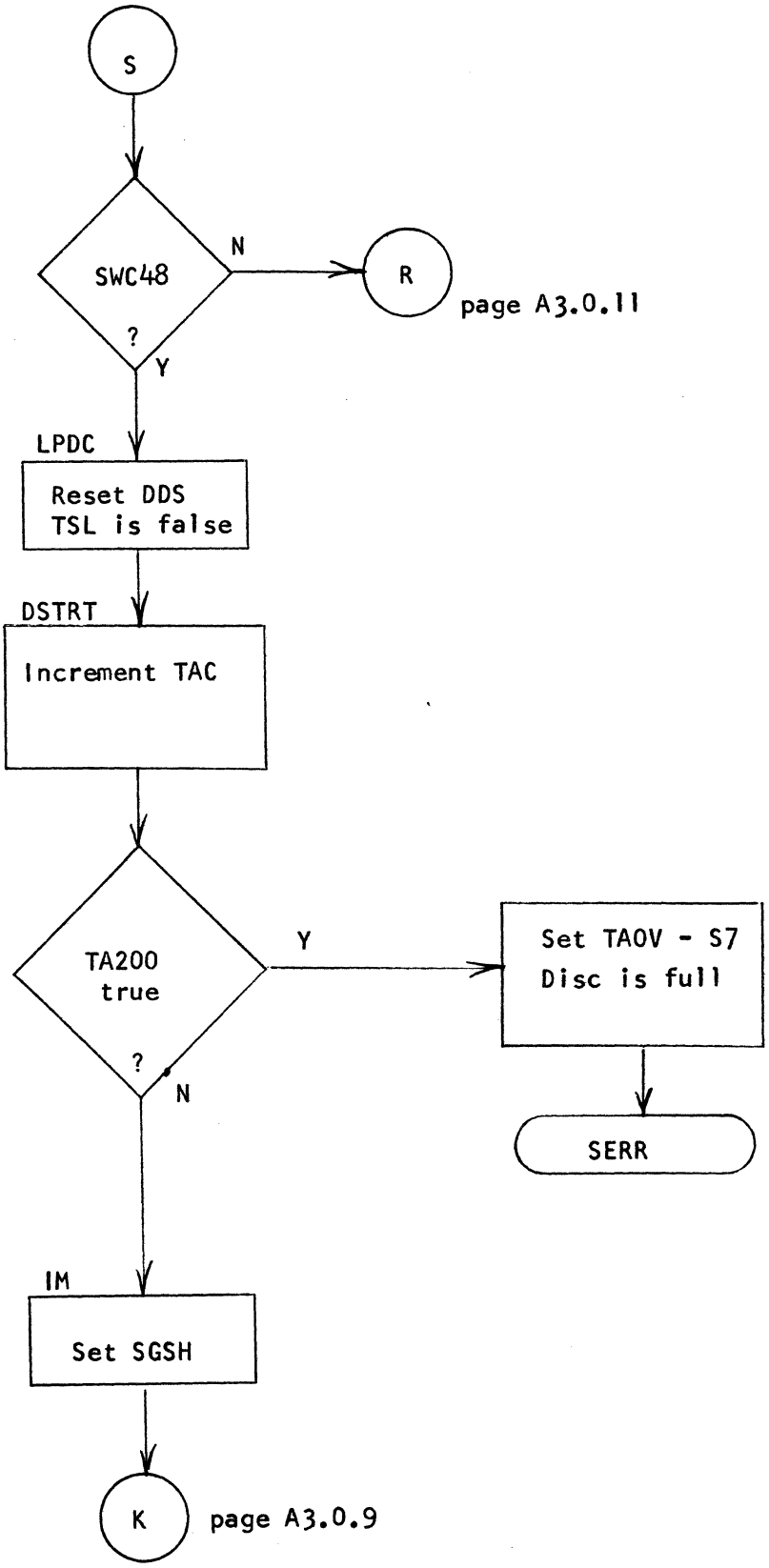

L
SGSH
CMP
SAMC is true
SAMC
Reset SGSH
Set DDS
R
WR
set
?
N
N
READ routine
page A3.0.18
Data
Transfer
Phase
Y
M
WRITE routine
page A3.0.12

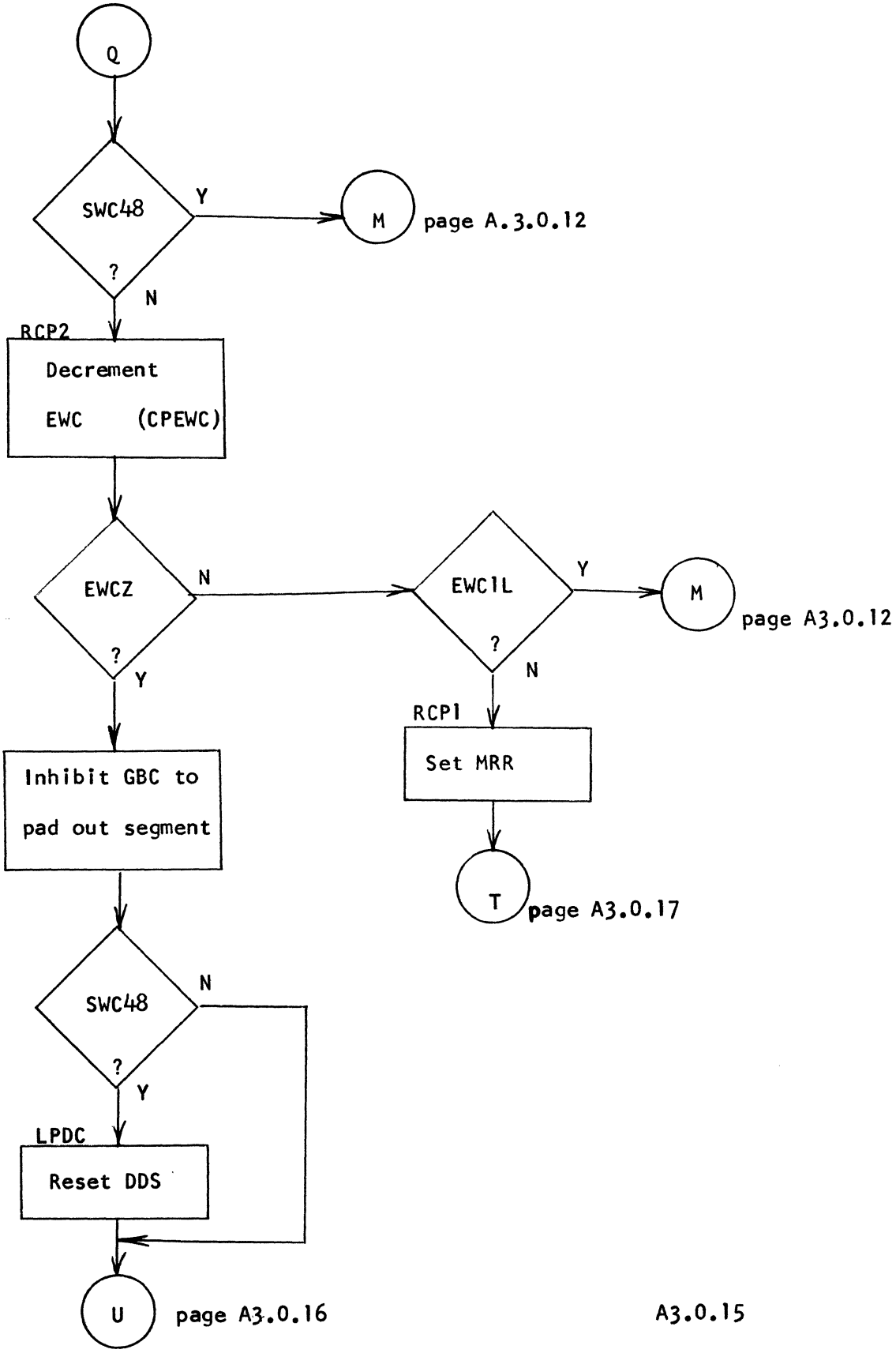
WRITE routine

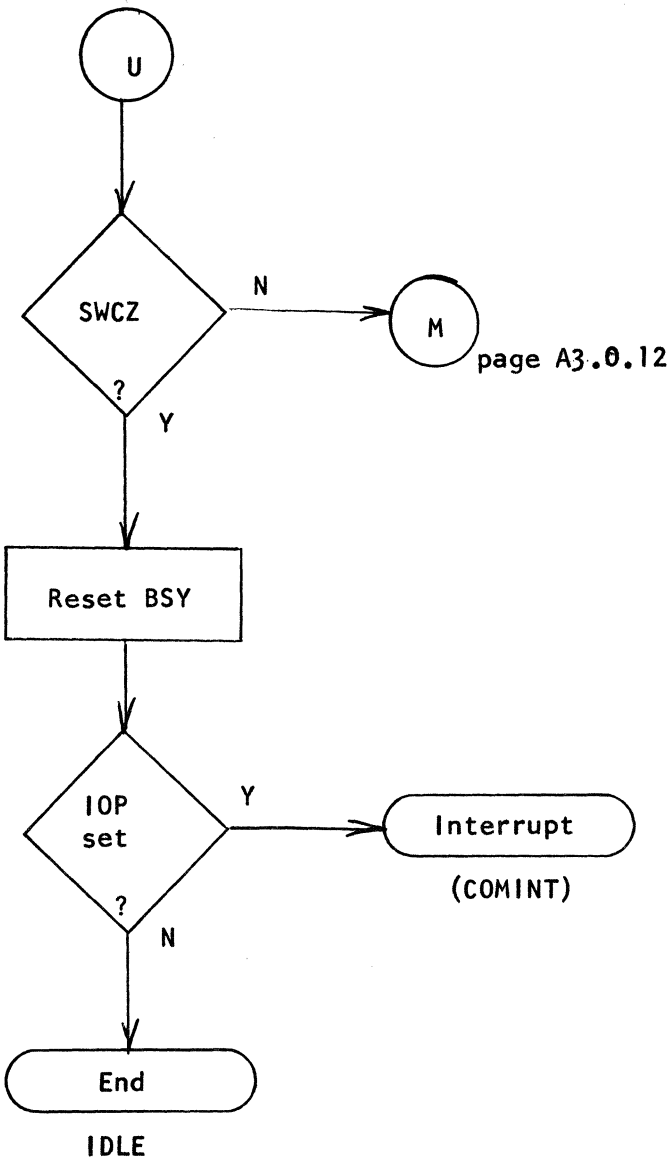
Refer to Figure 4.0.3

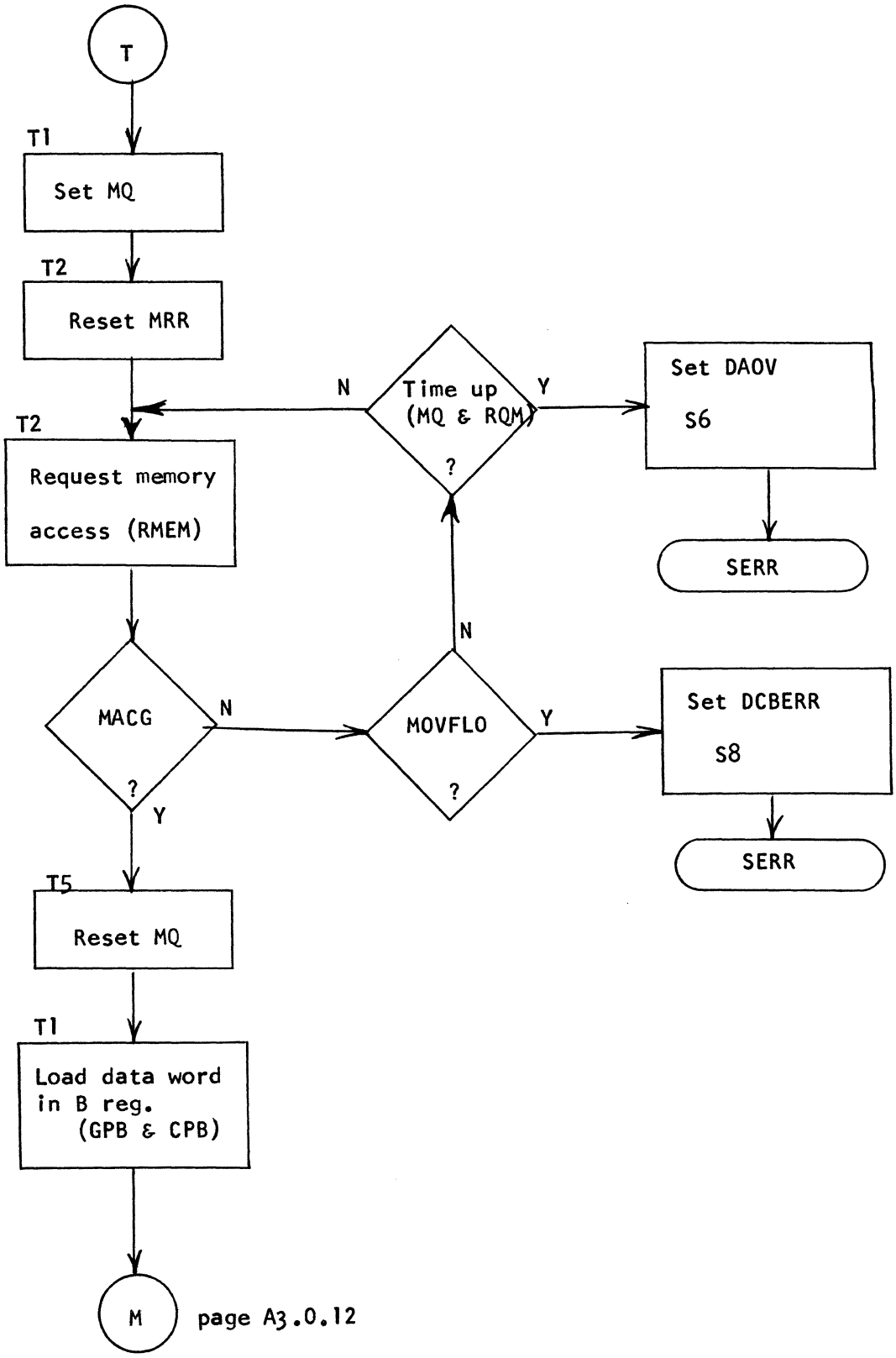



P
QWC=4
(D4)
N
?
Y
QWC=1
(D1)
N
M
page A3.0.12
?
Y
Q
page A3.0.15
RCP2
Advance SWC
SWC48
N
M
page A3.0.12
?
Y
W
LPCP
Advance SAC
SCO
N
R
page A3.0.11
?
Y
ITA
is true.
S
page A3.0.14


S
SWC48
?
N
R
page A3.0.11
Y
LPDC
Reset DDS
TSL is false
DSTRT
Increment TAC
TA200
true
?
Y
N
Set TAOV - S7
Disc is full
SERR
IM
Set SGSH
K
page A3.0.9

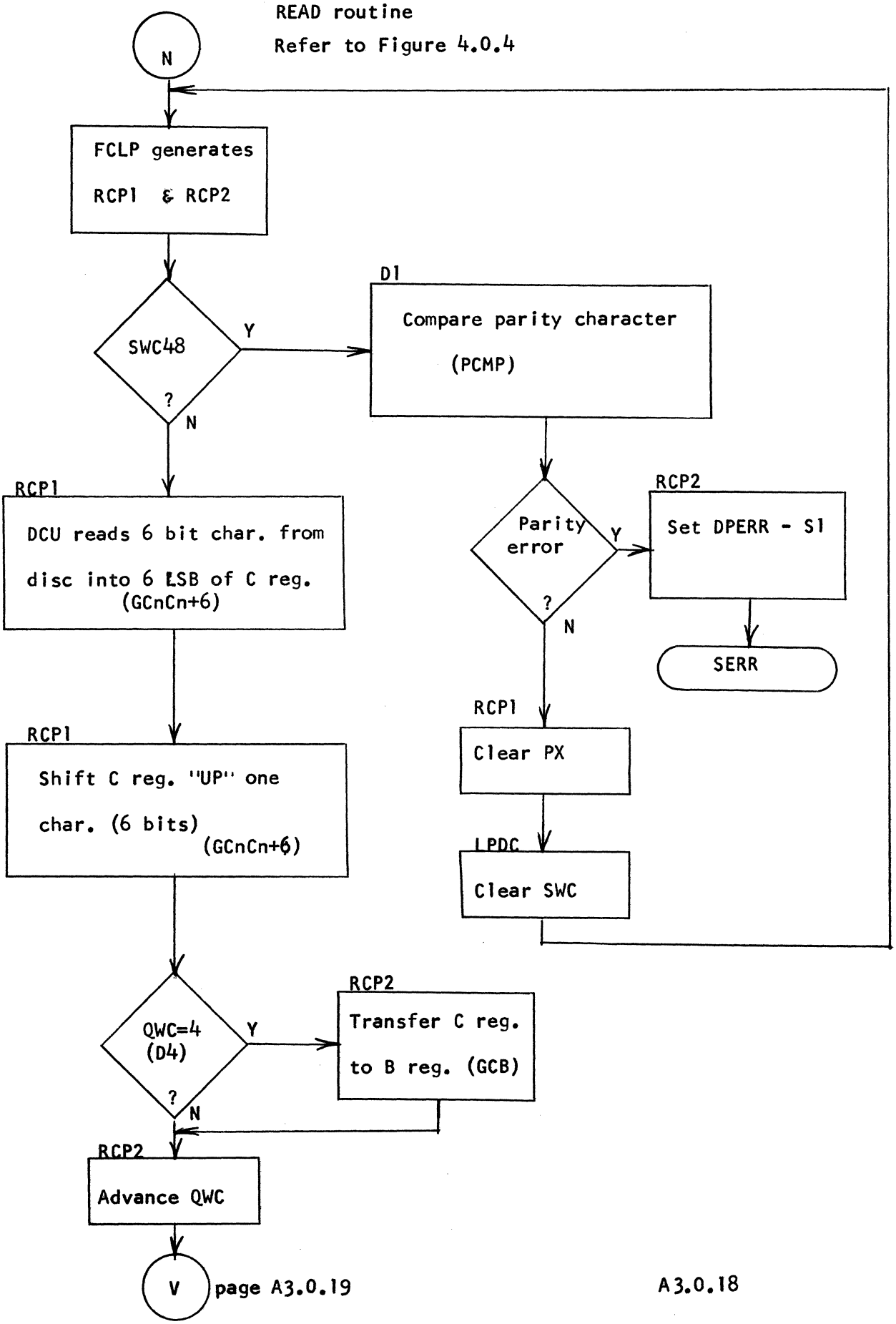

Q
SWC48
Y
?
N
M
page A.3.0.12
RCP2
Decrement
EWC (CPEWC)
EWCZ
N
?
Y
EWC1L
Y
?
N
M
page A3.0.12
RCP1
Set MRR
T
page A3.0.17
Inhibit GBC to
pad out segment
SWC48
N
?
Y
LPDC
Reset DDS
U
page A3.0.16


U
SWCZ
?
N
M
page A3.0.12
Y
Reset BSY
IOP
set
?
Y
Interrupt
(COMINT)
N
End
IDLE

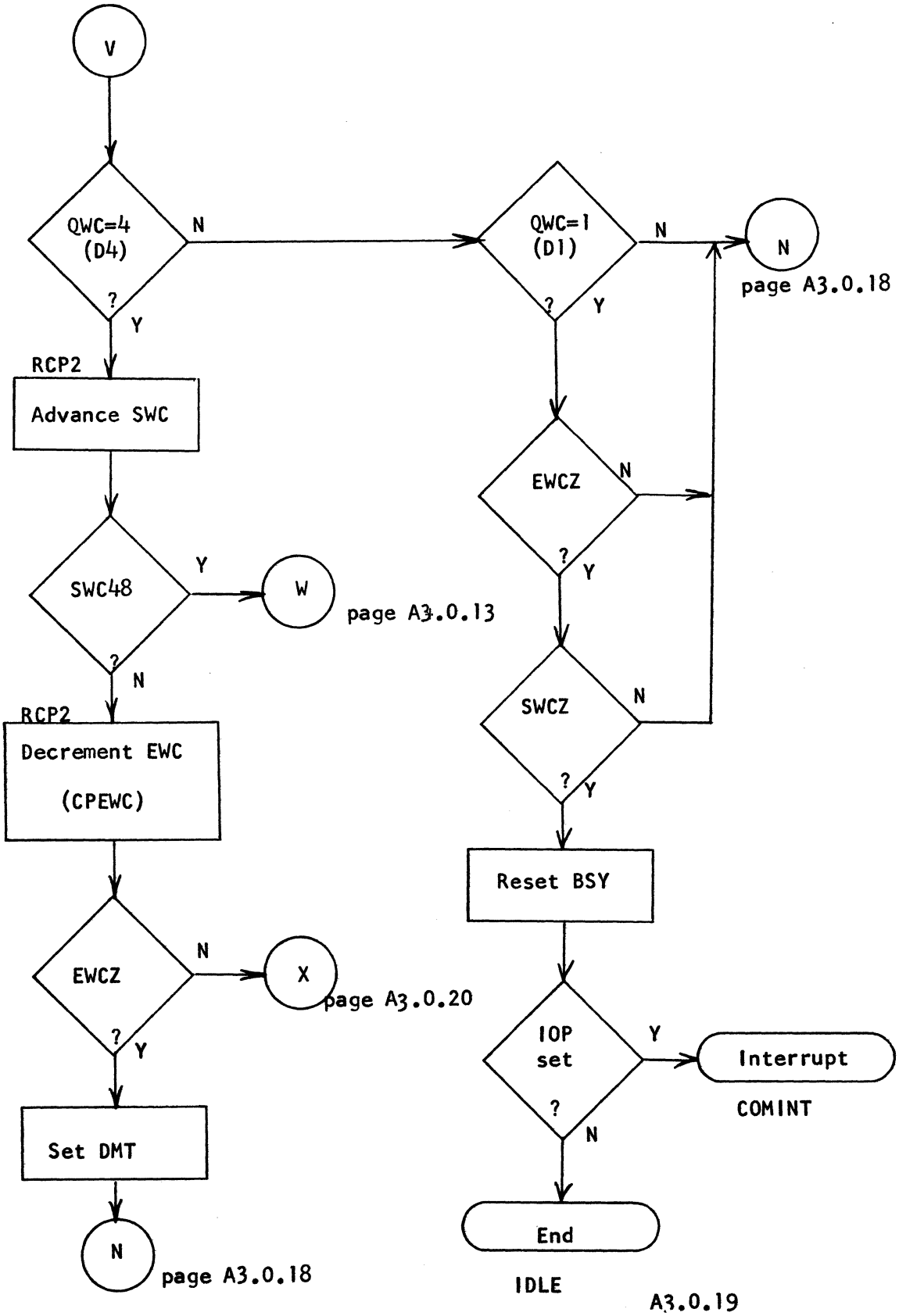

T
T1
Set MQ
T2
Reset MRR
T2
Request memory
access (RMEM)
N
Time up
(MQ & RQM)
?
Y
Set DAOV
S6
SERR
MACG
?
N
Y
MOVFLO
?
N
Y
Set DCBERR
S8
SERR
T5
Reset MQ
T1
Load data word
in B reg.
(GPB & CPB)
M
page A3.0.12

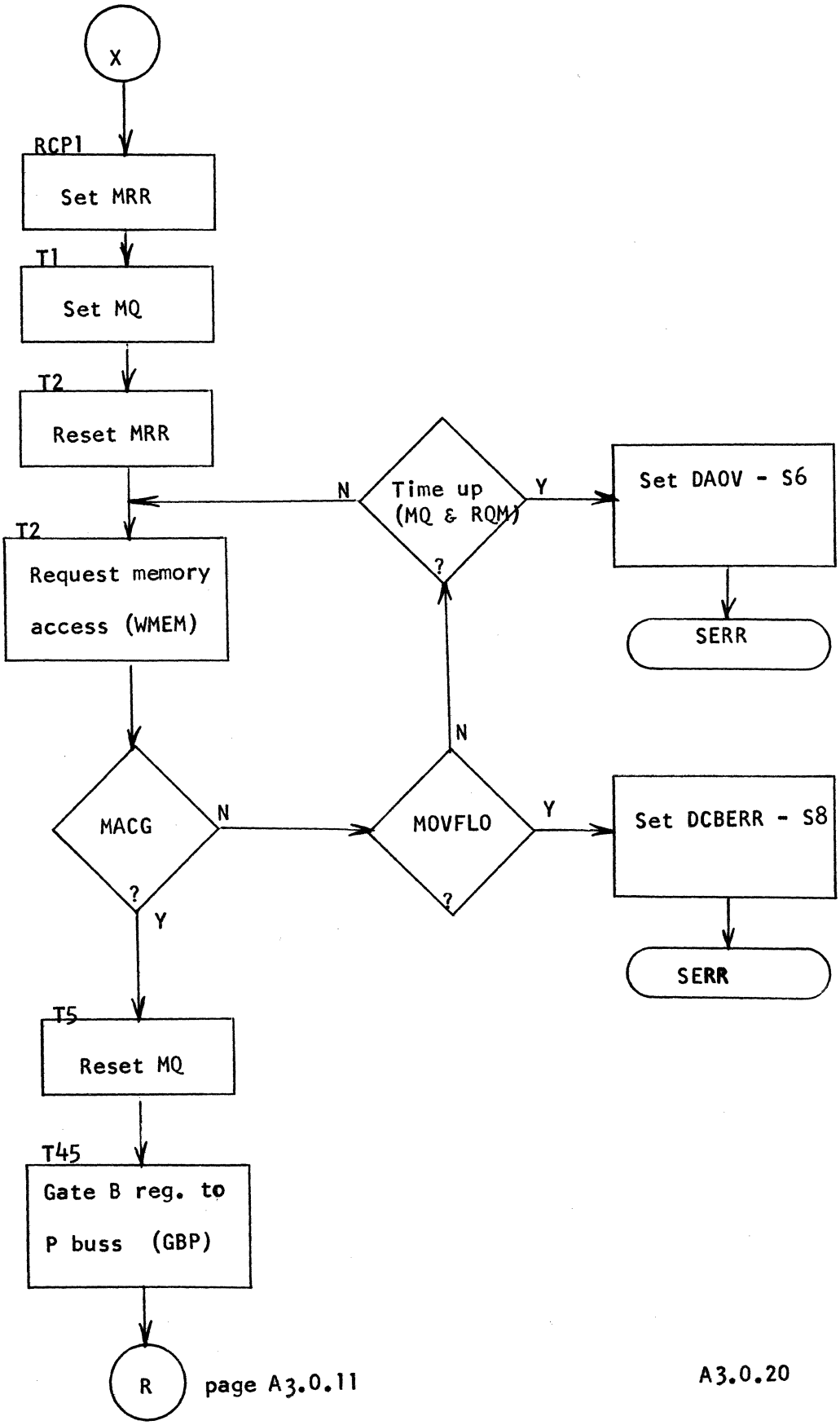
READ routine

Refer to Figure 4.0.4

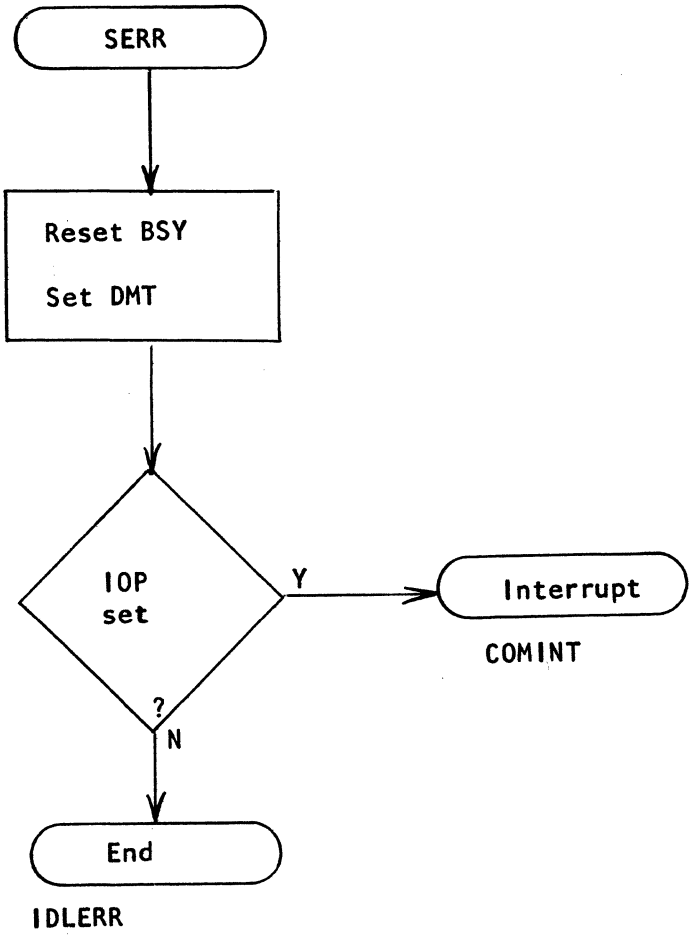


page A3.0.19


V
QWC=4
(D4)
N
?
Y
RCP2
Advance SWC
SWC48
Y
W
page A3.0.13
?
N
RCP2
Decrement EWC
(CPEWC)
EWCZ
N
X
page A3.0.20
?
Y
Set DMT
N
page A3.0.18
QWC=1
(D1)
N
N
page A3.0.18
?
Y
EWCZ
N
?
Y
SWCZ
N
?
Y
Reset BSY
IOP
set
Y
Interrupt
COMINT
?
N
End
IDLE

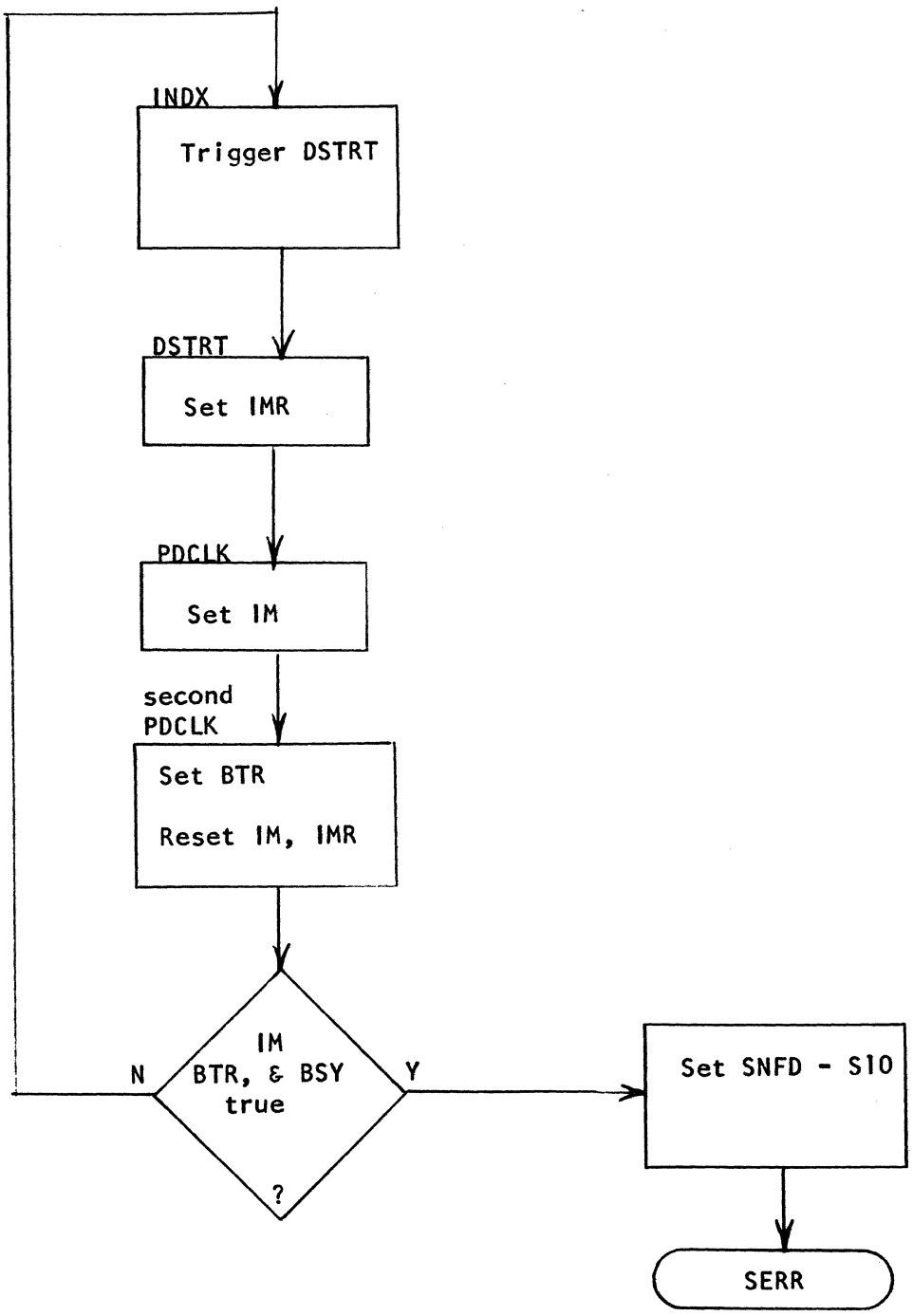

X
RCP1
Set MRR
T1
Set MQ
T2
Reset MRR
T2
Request memory access (WMEM)
Time up (MQ & RQM)
?
N
Y
Set DAOV - S6
SERR
MACG
?
N
Y
MOVFLO
?
N
Y
Set DCBERR - S8
SERR
T5
Reset MQ
T45
Gate B reg. to P buss (GBP)
R

page A3.0.11


SERR
Reset BSY
Set DMT
IOP
set
Y
Interrupt
COMINT
?
N
End
IDLERR

Index Mark Synchronization

Refer to Figure 4.0.6



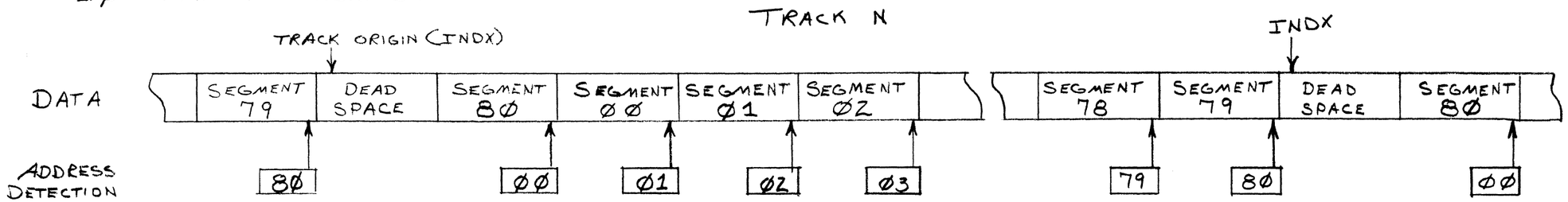
APPENDIX 4.0

DISC CONTROL UNIT

D.C.U. TIMING

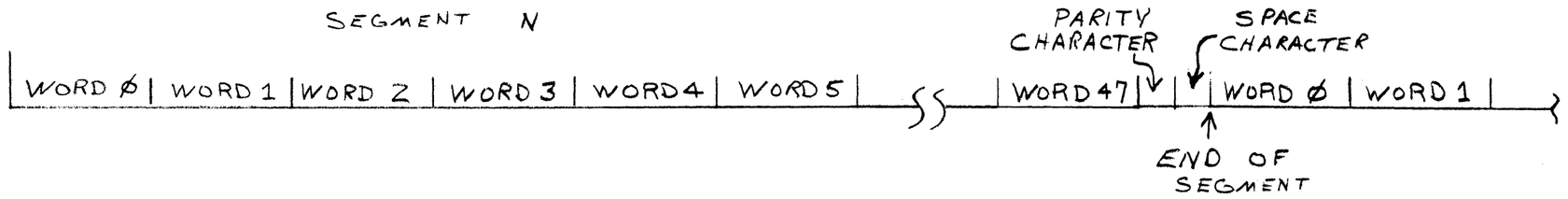
List of Figures

1.0 TRACK ORGANIZATION

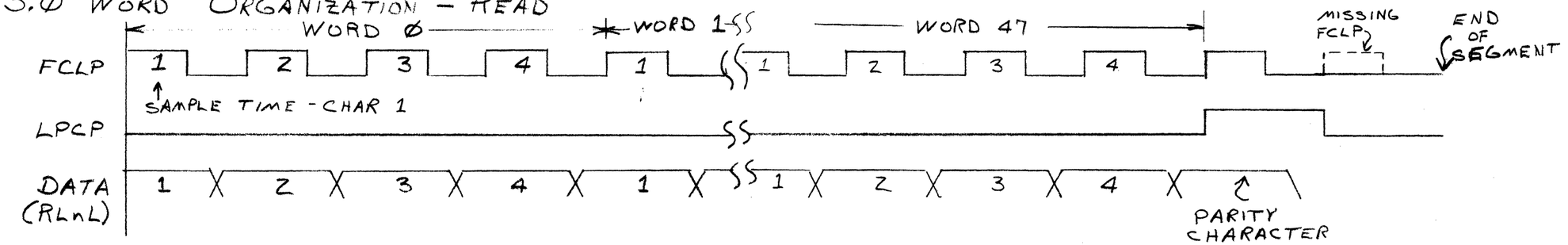


80 SEGMENTS/TRACK
48 WORDS/SEGMENT
4 CHARACTERS/WORD
6 BITS/CHARACTER

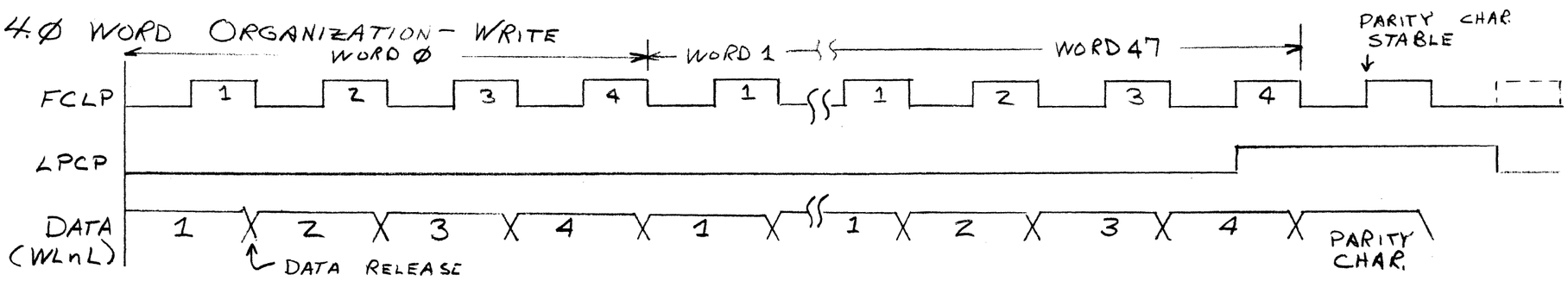
2.0 SEGMENT ORGANIZATION



3.0 WORD ORGANIZATION – READ

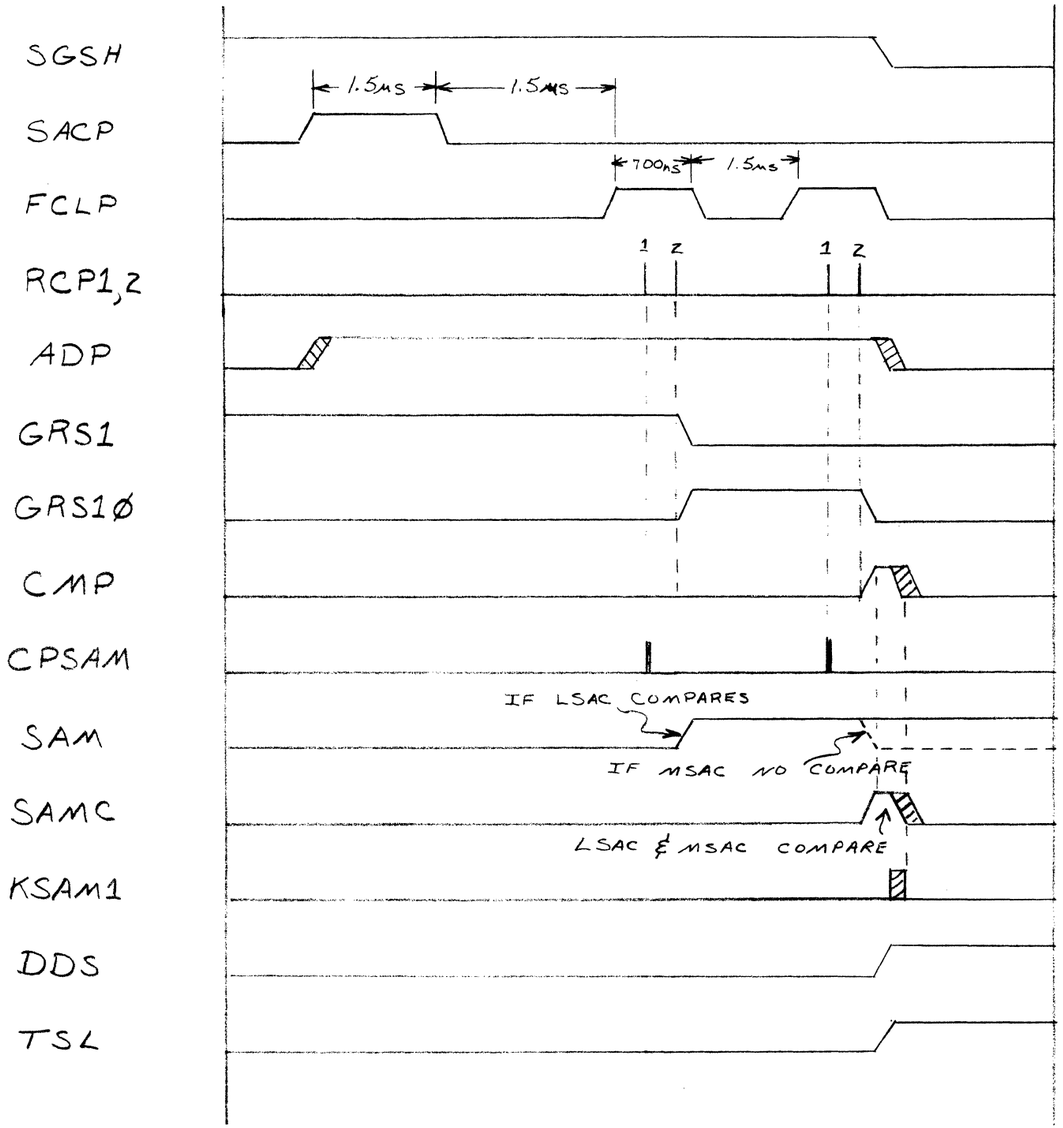


4.0 WORD ORGANIZATION – WRITE



Disc Data Organization

FIGURE 4.0.1



SGSH ↓ = PDCLK • SERR + (#) (CLEAR + BSY/ + SAMC)

FROM DISC

FROM DISC

DERIVED FROM FCLP

ADP↑ = PDCLK • SAI/ • SACP • SGSH ; ADP↓ = PDCLK • (SGSH/ + CMP)

COUNTER - ADVANCED ON RCP2

COUNTER - ADVANCED ON RCP2

COUNTER - ADVANCED ON RCP2, CLEARED BY KSAM1

CPSAM = ADP • RCP1

SAM ↑ = CPSAM • LSAC • GRS1 ; SAM↓ = CPSAM • MSAC/ • GRS1Ø + (#) KSAM

SAMC = SAM • CMP

KSAM1 = ADP/ • PECLK

DDS ↑ = (#) SAMC

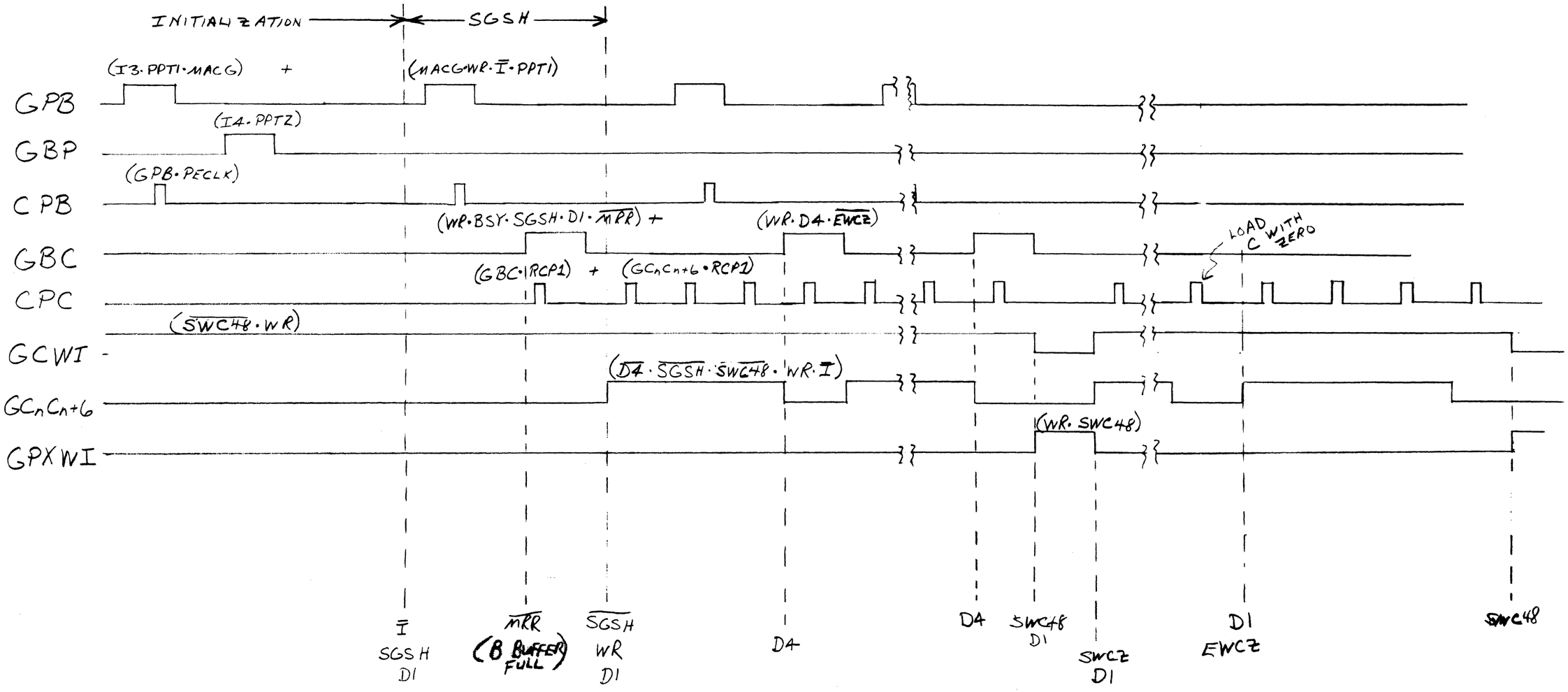
TSL = DDS • OPIPR

NOTES:

1. ▨ - ACTUAL RELATIVE TIMING MAY VARY BECAUSE OF ASYNCHRONOUS OPERATION OF DISC CLOCKS AND FZ4 CLOCKS
2. TO CHECK ADDRESS DETECTION
   LOOP ON READING SEGMENT ØØ, ANY TRACK
   SYNC ON INDX
   DELAYED TRIGGER - SACP

ADDRESS DETECTION

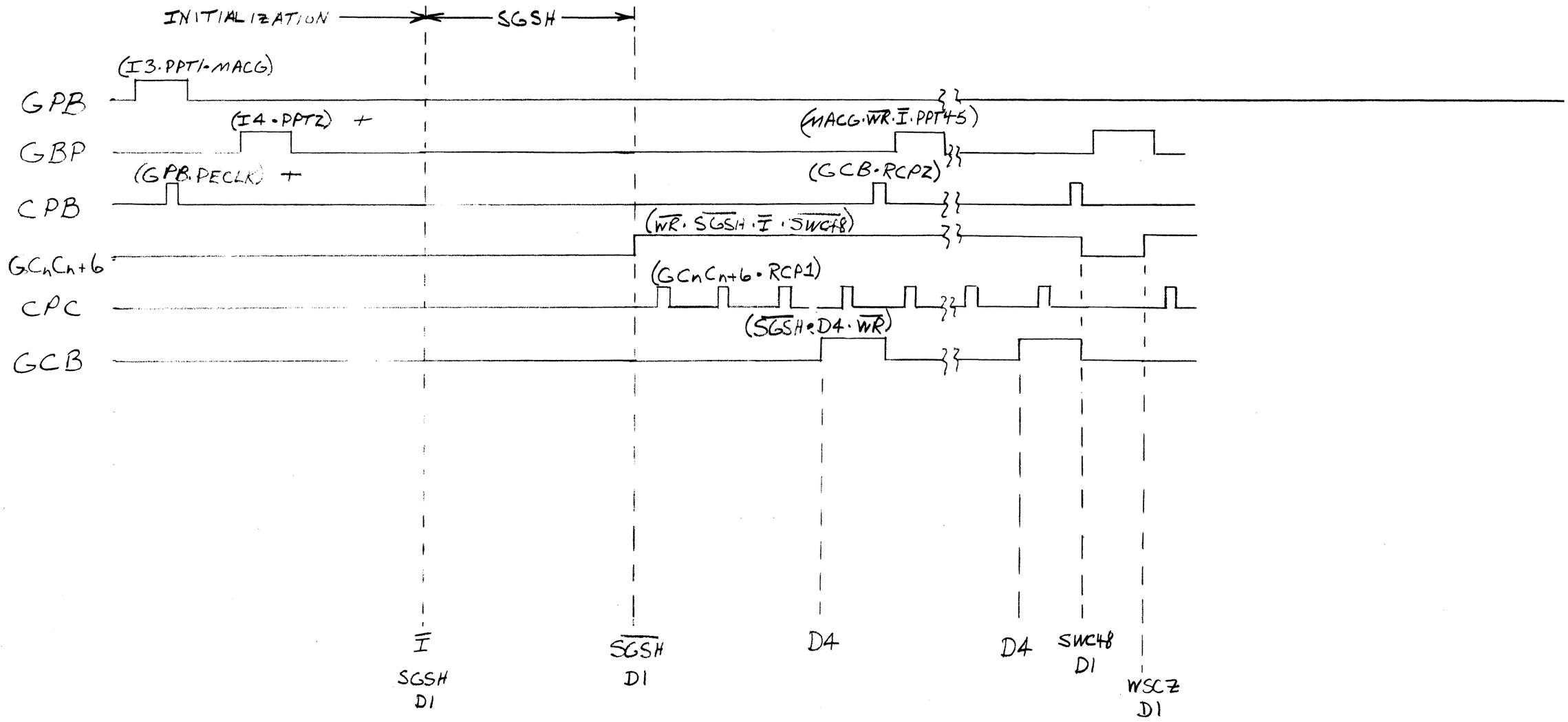
FIGURE 4.0.2



CHARACTER BUFFER TIMING

WRITE TO DISC

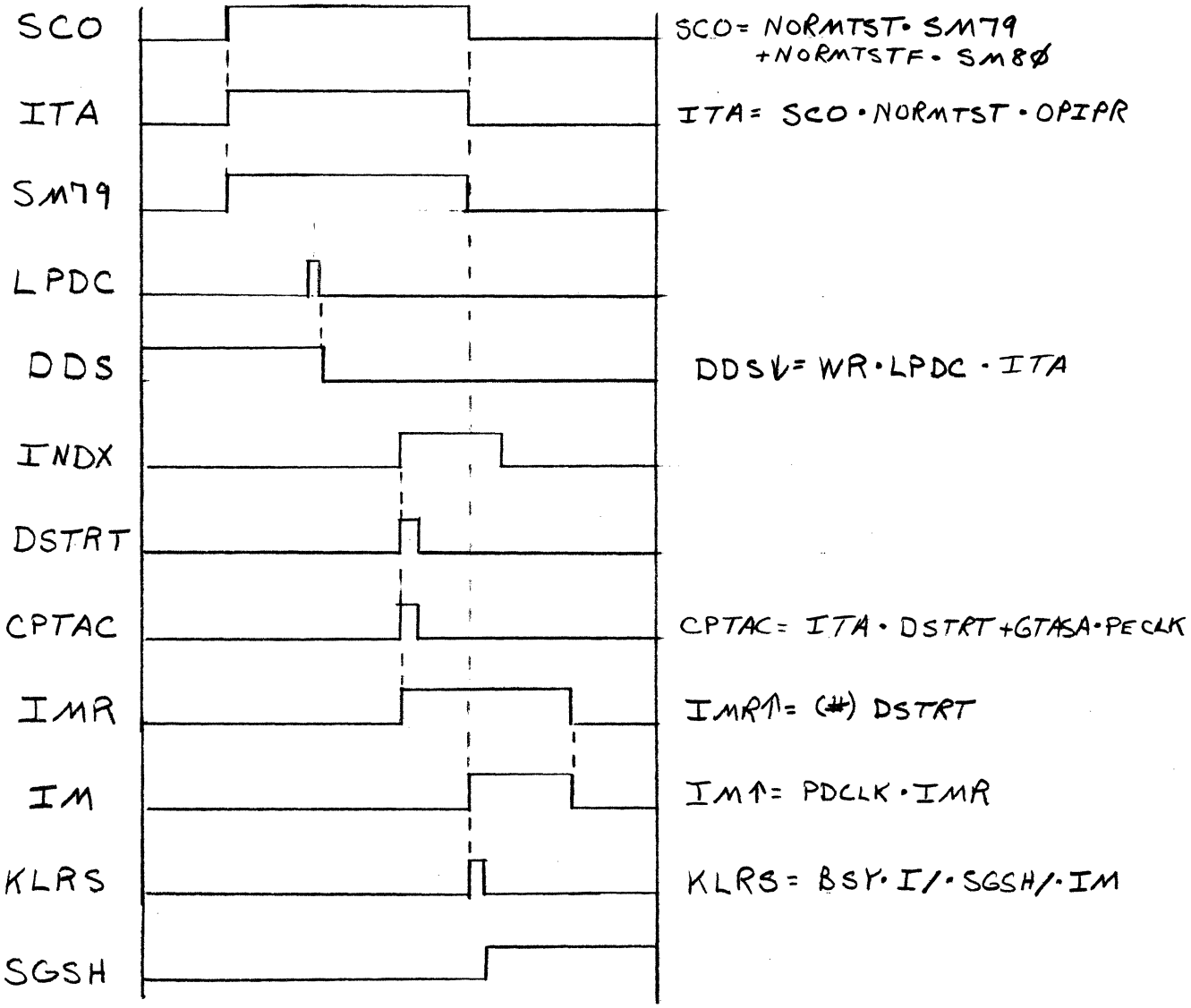
FIGURE 4.0.3



CHARACTER BUFFER TIMING

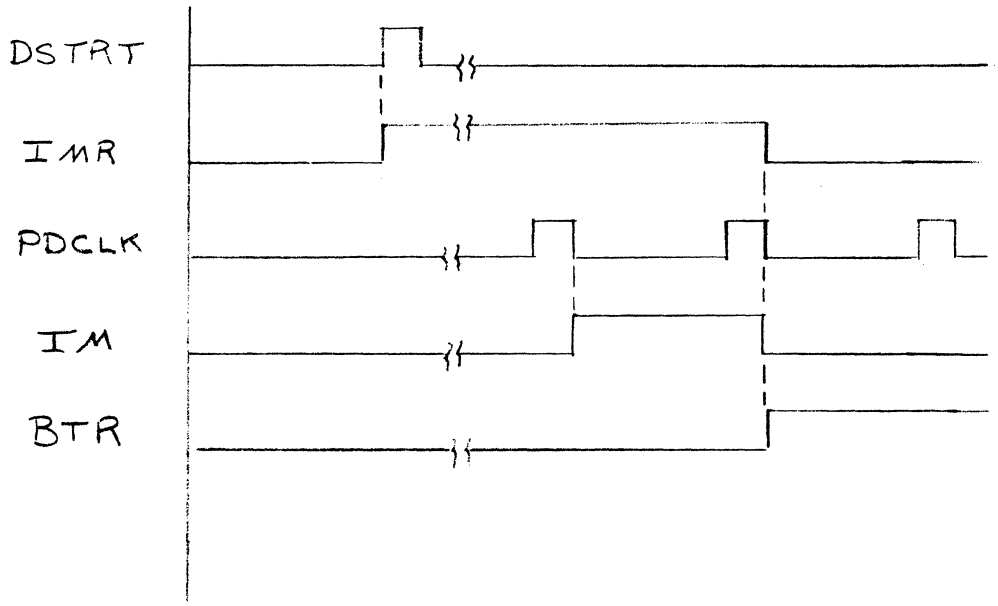
READ FROM DISC

FIGURE 4.0.4



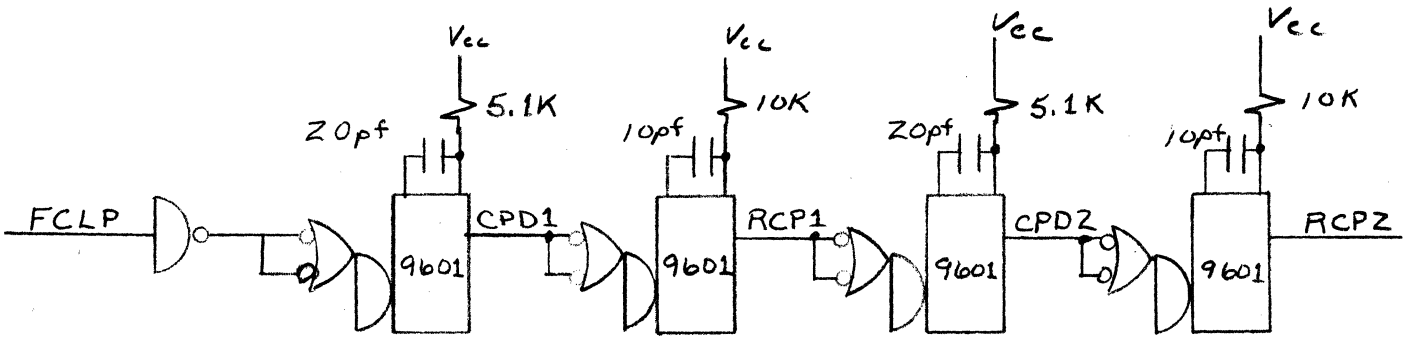
INCREMENT TRACK ADDRESS

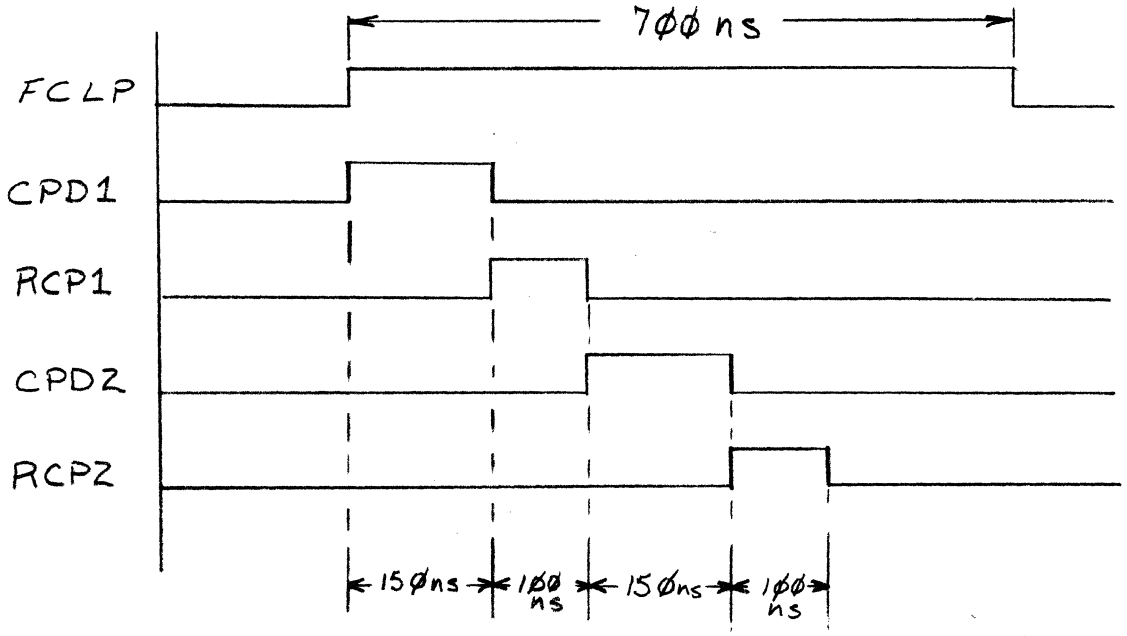
FIGURE 4.0.5



INDEX MARK RESYNC TIMING

FIGURE 4.0.6

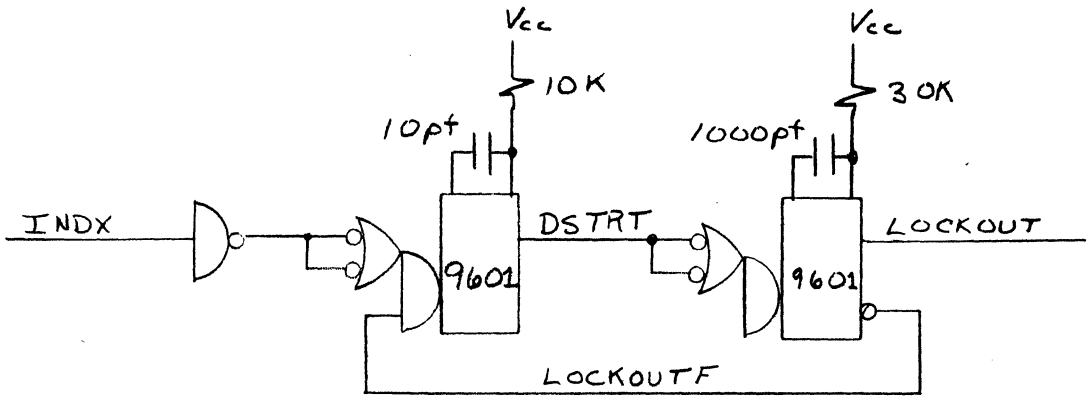


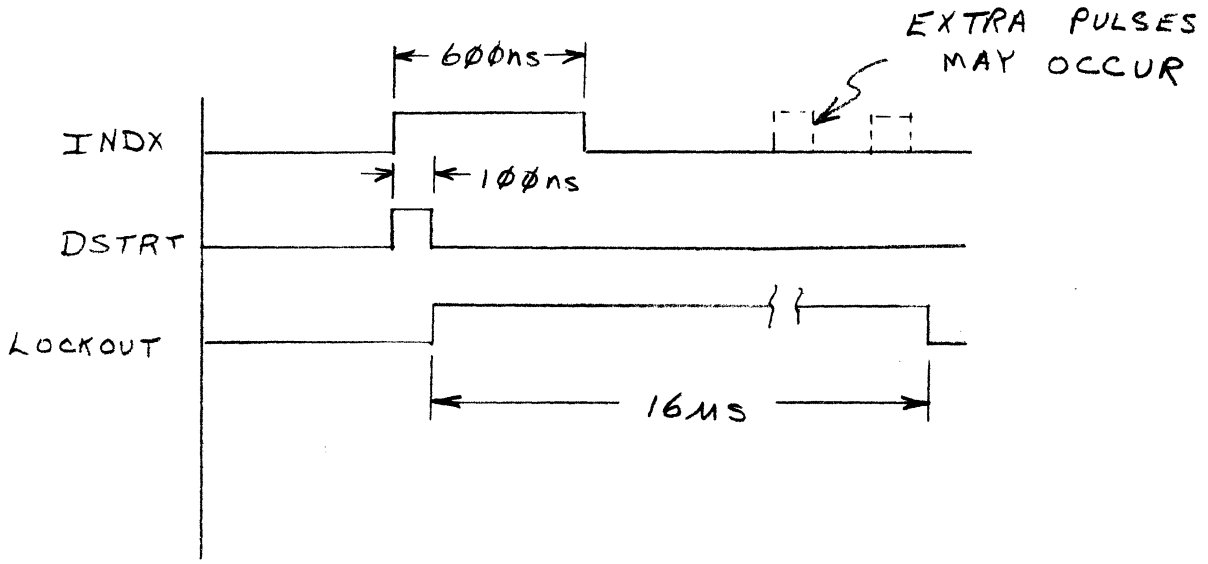


ONE-SHOT TIMING

CHARACTER CLOCK GENERATION

FIGURE 4.0.7





LOCKOUT INHIBITS NOISE PULSES

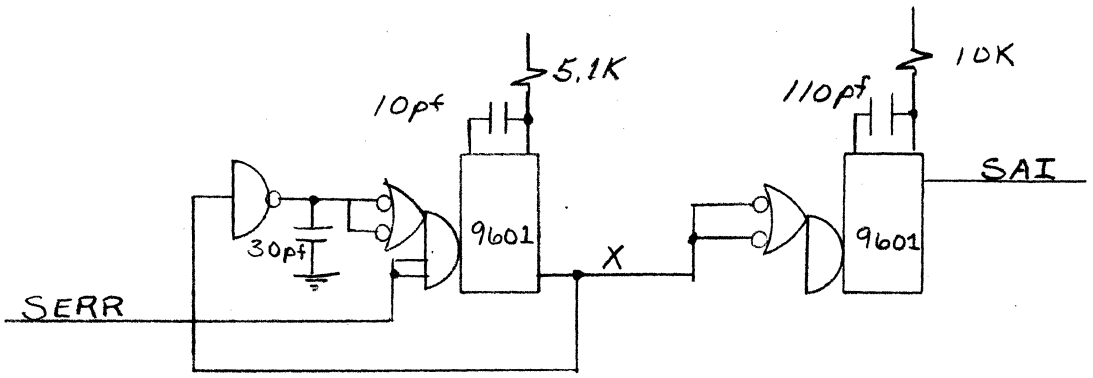
IN THE DISC "DEAD SPACE" FROM RETRIGGERING

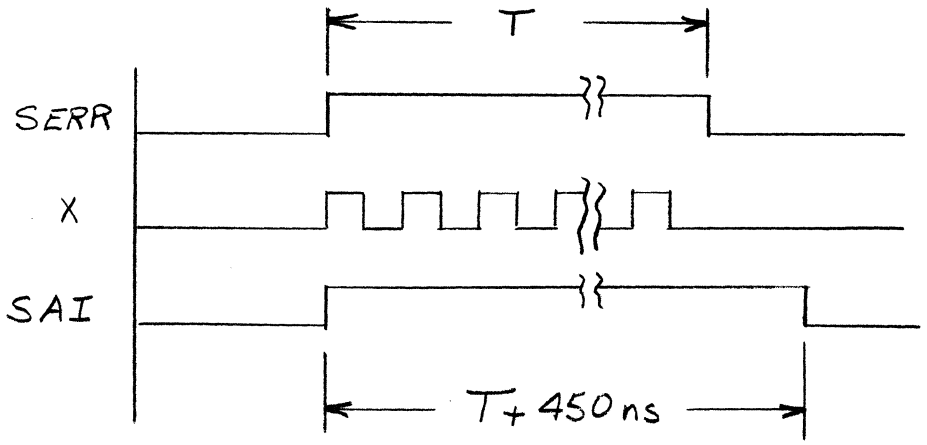
DSTRT

ONE SHOT TIMING

INDEX PULSE

FIGURE 4.0.8



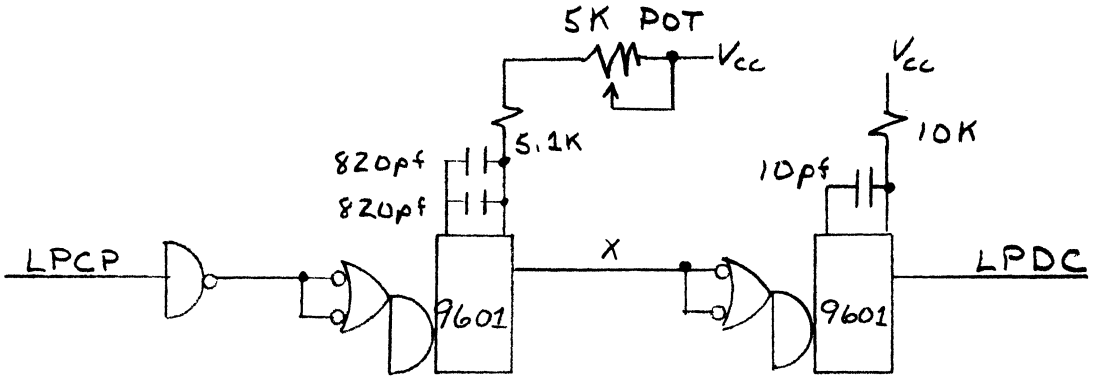


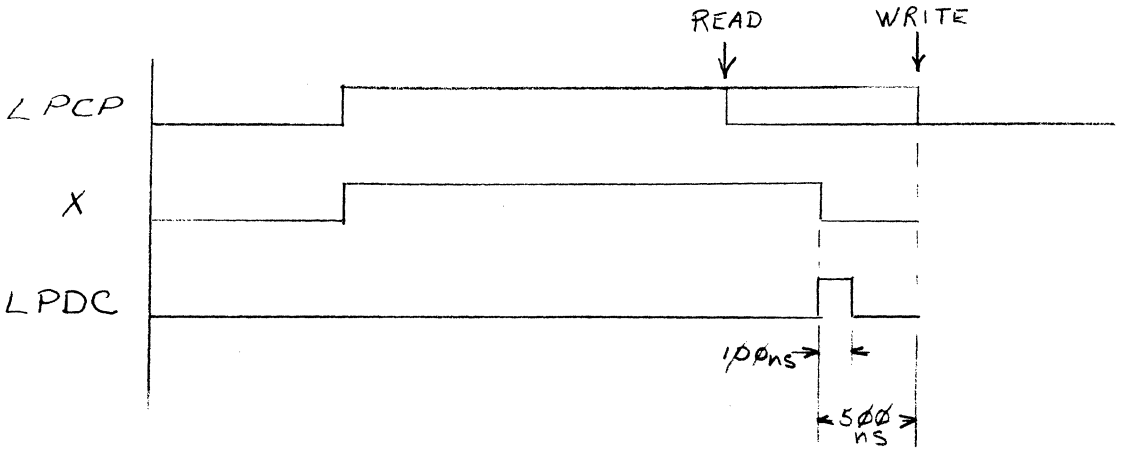
INHIBITS ADDRESS DETECTION FOR AT LEAST ONE PHASE TIME AFTER ERROR IS CLEARED.

ONE-SHOT TIMING

SEGMENT ADDRESS INHIBIT

FIGURE 4.0.9





BENCH ADJUSTMENT: SET LPDC↑ @ LPCP↑ + 3.8 msec

ON-LINE ADJUSTMENT: IN WRITE MODE,
SET LPDC↑ @ LPCP↓ − 500 nsec

ONE SHOT TIMING
PARITY STROBE
FIGURE 4.0.10

APPENDIX 5.0

DISC CONTROL UNIT

DCB AND DATA FORMATS

1. DCB Address Word (DCBP)

23 14	13 0
IGNORED	DCB ADDRESS

The DCB Address Word should be stored in the A register prior to issuing a SPU data transfer instruction (RD, ARD, WRIT). Octal format is required.

2. Block Length

The Block Length is stored at "DCB Address".

23 14	13 0
IGNORED	BLOCK LENGTH

The Block Length specifies the number of words in the file to be processed. This number may be from 1 to maximum residual core.

3. File Origin

The File Origin is stored at "DCB Address + 1".

23 14	13 0
IGNORED	FILE ORIGIN

The File Origin is the location in core memory where data transfers will begin.

4. Disc Address

The Disc Address is stored at "DCB Address + 2".

23 17	16 8	7 0
IGNORED	TA	SA

The Disc Address is the starting address on the disc for data transfers. Bits 0-7 are the BCD Segment Address (SA) which ranges from 00 to 79 BCD. A maintenance segment (80) can be addressed in "test" mode. Bits 8-16 are the BCD Track Address (TA) which ranges from 000 to 199 BCD.

5. Data

All 24 bits in each word written to the disc are written and retrieved in pure binary form.

APPENDIX 6.0

DISC CONTROL UNIT

COMMAND SET

The DCU Command Set consists of ten commands:

TYPE	COMMAND	ASSEMBLER FORMAT	OCTAL CODE
1.0 Test			
1.1	Status Test	STST 70B	06000070
1.2	Error Test	ETST 70B	06010070
2.0 Logic Initialization			
2.1	Priority On	PON 70B	06013070
2.2	Priority Off	POFF 70B	06011070
2.3	Priority Complete	PCOMP 70B	06001070
3.0 Data Transfer			
3.1	Read Status	RDS 70B	06611470
3.2	Alternate Read Status	ARDS 70B	06613470
3.3	Read Disc	RD 70B	06401470
3.4	Parity Check	ARD 70B	06403470
3.5	Write Disc	WRIT 70B	06421470

COMMAND ACTION

1.1 Status Test

This instruction returns the general status from the DCU into the control panel indicators GT, EQ, LT, and BE.

Refer to App. 8.0 for status interpretation.

1.2 Error Test

This instruction returns the error status into the control panel indicators.

Refer to App. 9.0 for error interpretation.

2.1 Priority On

This instruction enables the interrupt control of the DCU by setting the INA flip-flop in the CPI.

General status is returned.

2.2 Priority Off

This instruction resets the DCU interrupt control (INA) preventing an interrupt to the FST-1.

General status is returned.

2.3 Priority Complete

This instruction resets the Interrupt in Process (INP) control flip-flop in the DCU/CPI.

Whenever the interrupt system is used , this instruction must be executed at the end of an interrupt service routine.

General status is returned.

3.1 Read Status

This instruction reads the Status Register of the DCU into the accumulator.

Refer to App. 7.0 for status bit definition.

General status is returned.

3.2 Alternate Read Status

This instruction reads the Track and Segment Address counters into the accumulator with the same format as the Disc Address of the DCB.

The value of the TASA is equal to the address of the next segment, after the processed file, in BCD format.

General atatus is returned.

3.3 Read Disc

This instruction is preceded by a LDA with the DCB pointer.

The DCU fetches the 3 word DCB and performs word transfers to memory without further intervention.

The DCU checks parity on all segments which have been read.

General status is returned.

3.4 Parity Check

This instruction performs as the Read Disc instruction except that data transfers to memory are inhibited.

Parity checking occurs as with a read.

General status is returned.

3.5 Write Disc

This instruction is preceeded by a LDA with the DCB pointer.

The DCU fetches the 3 word DCB and performs word transfers to the disc without further intervention.

Parity is generated for each segment and general status is returned.

APPENDIX 7.0

DISC CONTROL UNIT

STATUS REGISTER

Bit Position	Logic Name	Meaning when set
0	DNR	Disc is not "READY"
1	DPERR	DCU Parity Error
2	INA	DCU interrupts are enabled
3	INTINH/	Interrupt inhibit switch is normal
4	MPRO/	MEMORY PROTECT switch is normal
5	NORMTST	NORMAL-TEST switch is normal
6	DOV	Data overflow - memory not available when required
7	TAOV	Track Address Overflow
8	DCBERR	Data Control Block error - TASA or memory address out of bounds
9	IOP	Interrupt operation active
10	SNFD	Segment not found
11	WRINH/	WRITE INHIBIT switch is normal
12	DWINH	Disc WRITE INHIBIT switch is in INHIBIT
23	SERR	Some error exists in the DCU

APPENDIX 8.0

DISC CONTROL UNIT

GENERAL STATUS

General Status is returned by the DCU for all SPU commands except Error Test (ETST). This information is returned on the BN buss bits 20-23 to the FST-1 control panel indicators BE, LT, EQ, and GT respectively.

Status response, as interpreted by testing indicators with BOI instructions, is as follows:

Indicator	Meaning when set
BE	Disc not ready-operator intervention required
LT	Busy
EQ	Idle with error - Subsystem is ready and idle but an error occurred during last operation.
GT	Idle - Subsystem is ready for new job

APPENDIX 9.0

DISC CONTROL UNIT

ERROR STATUS

Error status is returned by the DCU for the SPU command Error Test (ETST).

Status response, as interpreted by testing the control panel indicators, is as follows:

Indicator	Meaning when set
BE	DCB error - memory or disc address out of range
LT	Data overflow - DCU could not get access to memory in time.
EQ	DCU parity error
GT	Track address overflow - disc is full.