APPLICATION NOTES/TECHNICAL BULLETINS

SENTRY AND XINCOM TEST SYSTEMS

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SENTRY APP. NOTE	TITLE AND ABSTRACT	DATE
13	**Testing One-Chip Calculators on the Sentry 100/200/400** This application note describes the techniques of using a Sentry 100, 200, or 400 tester to completely test a typical one chip calculator. The application note discusses special wiring, finding sync, simulating keyboard inputs, and reading segment drivers.	
14	**Sentry Series – Testing Input Breakdown Voltage on MOS/LSI Devices** This application note shows two example programs for measuring large input breakdown voltages.	12-72
15	**Sentry Series Parameter Testing For Static MOS LSI Arrays** This application note discusses MOS/LSI parameter testing efficiency. It presents program formats to keep parameter test time to a minimum.	8-72
16	**Sentry Series – Testing Random Access Memories on a Sentry 600** This application note discusses briefly the problems of testing RAMs and how to avoid large functional patterns with alternate drivers to compliment data patterns; it also has some program excerpts.	11-72
17, Rev. 2	**Using Magnetic Tape for Data Collection, Analysis and Reduction on the Sentry Series** The purpose of this application note is to discuss the reasons for data-logging on magnetic tape and show that the data obtained can be manipulated by the Sentry's computer, giving a complete statistical study of any device that can be tested on a Sentry 200, 400 and 600.	8-73
18	**1103 1024-Bit Random Access Memory Factor Program Description Using RAMPAT** This application note is a description of a Sentry 600 test program for a 1024-bit dynamic random access memory of the 1103 type. The test program consists of nine basic tests. The first two tests exercise the ping-pong pattern (GALPAT equivalent) with different timing and voltage conditions. The next two tests use the Read-Write Modify pattern with row address A4 as the least significant address bit with two different timing and voltage conditions. Tests 5 and 6 are refresh tests using a Checkerboard pattern with the row address bits re-defined to make A0 the least significant bit. Here the test rate is slow to check refresh capability. The last three tests are d.c. parametric tests for voltage breakdown, leakage and power supply current.	2-73
19	**Device Program Pinning Alteration Using Series 5000C Testers** This application note describes an easy way to change the pinning of a program without interfering with any normal testing operations.	12-72

APP. NOTE	TITLE AND ABSTRACT	DATE
20	**Automatic Timing Calibration and Pin De-skewing — Sentry 600** This application note shows programming techniques that may be used on the Sentry 600 test system to reduce timing errors related to system inaccuracies. Through these techniques, measurement and stimulus accuracy can approach the programming resolution of the timing generators. Total errors in timing between stimulus pins and sensing comparators can accumulate to several nanoseconds. Only through differential measurement techniques can the 160 pico-second timing resolution of the Sentry 600 realize its full potential for accurate propagation delays, rise times and other timing measurements on complex functional devices.	2-73
21	**Testing Access Time on Read Only Memories** This application note discusses the reason to test access time on ROMs, the use of ROMPONG (an assembly language program that exercises a ping-pong type test on a functional pattern), pin assignments, and setting up the tester for testing.	5-73
22	**Sentry 600 Test Plan Description for the RCA COS/MOS CD4034AD 8-Stage Static Bidirectional Parallel/Serial, Input/Output Bus Register Integrated Circuit** As the title says this is a test plan description including 17 volt function tests, contact tests, leakage tests, 2.8V function tests and noise immunity tests, channel resistance tests, a 1K-3K resistor test, dynamic test parameters, time measurement procedures, rise and fall time tests, test plan flow chart, and program listing.	3-73
24	**Calculating Logarithms and Antilogarithms on Sentry II, 200, 600, and 610 Test Systems** This application note describes the FACTOR coding to be used for the calculation of logarithms and antilogarithms on Sentry test systems.	6-76
25	**9300 4-Bit Shift Register Functional and Parameter Test Program — Sentry 400** This application note presents a procedure for testing a 9300 4-Bit Shift Register for functional operation and DC parametric quality using the Sentry 400 array test system; it covers wiring the load board, initial set-up instructions, program listing, and setting up the input clock.	8-71
26	**Batch System vs Foreground/Background System** The comparative merits of batch systems and foreground/background systems are the heart of this application note.	7-73
27	**Universal Load Boards for the Sentry 500 and 600** This application note takes a hollow center performance board and a fuzz button ring and discusses how to use them as universal load boards with only the DUT board changing with device types.	7-73
28	**Testing At Frequencies Greater Than 5 MHz On a 5 MHz Sentry 600/500 System** This application note describes testing at frequencies greater than 5 MHz on 5 MHz systems by ORing two timing generators together to produce two pulses, sampling an output pin twice during one period, and making the least significant address pin an RZ type to allow two different addresses in one period.	3-73

APP. NOTE	TITLE AND ABSTRACT	DATE
29	**Testing 7490 Decade Counter on Sentry 600** This application note describes three variations of a 7480 Decade Counter test program and includes source listings and sample outputs.	3-74
30	**PSCAN** This application note discusses the use, output, and loading of PSCAN, an assembly language overlay that scans all programmed tester pins to establish the complete pin-by-pin programmed status of the test system.	5-74
31	**Miscellaneous Numerical Manipulation in Factor** This application note discusses rounding off fractional numbers to integers and bit manipulation of FACTOR variables.	5-74
32	**Generating RANDOM Integers with RANNUM** This application note is a brief, one-page description of RANNUM, outlining initialization, random or non-repeating numbers, and restrictions.	5-74
33, Rev. 1	**Extending the Number of Global Variables with GLOBS on the Sentry 200/600/610 and Sentry II** GLOBS is an assembly language overlay that can extend the number of system global variables to 120. This application note discusses placing assembly language overlays on the disk, the GLOBS calling sequences, initializing the system, DOPSY commands, plus examples of GLOBS usage.	3-76
34	**Minimizing Access Time for Assembly Language Overlays** This application note describes a technique for minimizing the access time required to load an Assembly Language overlay. The access time is made up of the time required to search the disk directory ($DIRCT) for the file name and the time required to transfer the file to core. This technique minimizes the time spent searching the directory.	6-74
35, Rev. 2	**XGRAPH: A General Purpose X-Y Plotter for the Sentry 200/600/610 and Sentry II** XGRAPH is an assembly language utility program which is executed by an EXEC statement call from within the user's FACTOR test program. Each individual call to XGRAPH performs a specific function such as output a single line of the graph including the ordinate value on the output device. It can clear and/or open the disk file required for the composite Shmoo plot, composite one set of test results upon the previous set, or produce a top of form on the line printer. XGRAPH functions are illustrated in this application note in terms of sample plots and excerpts of the FACTOR programs which produce them. Included in this application note are the various specific calling sequences for these graphic functions, conditions, and usage requirements as well as the sample programs and plots.	3-76

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36	**Testing Random Access Memories (RAMs) with the Sentry Hardware Pattern Generator (HPG)** This application note discusses setting up Local Memory to control the pattern generator; defining the read/write pins, RAM size, the address pins, data pins, etc.; loading the pattern generator with the pattern algorithm; executing the test; set up and algorithms for a read-modify-write-cycle and for column and row bar patterns; and testing refresh time.	4-75
37	**Testing CMOS Devices On a Sentry 600/610** This application note discusses CMOS testing from designing a performance board through measuring VOL, isolating inputs from the pin electronics, measuring input leakage, programming input current tests, and measuring VOH. This note includes a sample program for CMOS testing.	4-75
38	**Using the Power of the Sentry 600/610 Disc-Based System to Develop Test Programs** This application note illustrates how the power of a Sentry disc based system can be used to simplify program writing. This document consists of two sections. In the first a method of generating fast and flexible TTL Sentry 600 test programs is described. On the disc, the programmer stores small program segments that are inserted into each device test program. With this method, any TTL gate can be programmed within a half hour or a typical MSI device can be programmed and debugged in less than six hours. In the second section the programming of a ROM is illustrated. The programmer uses ROMPAT and string files to extract a test pattern and generate a Sentry 600 program. Typical development time for each functional pattern is about three minutes.	4-75
39	**A General Algorithm for Testing One-Chip Calculators on the Sentry 100** This note describes a generally applicable method of testing one-chip display calculators with multiplexed display drives, on-chip free-running clock circuit, and keyboard strobing interlaced or coincident with display strobing and sharing common lines. The discussion assumes the use of the Fairchild Sentry 100 tester with the Model 8438 Submultiplex Unit. The general method can be applied to all units in the Sentry Series, however.	6-75
40	**Algorithmic Pattern Generation Techniques** This paper describes a method of generating algorithmicly a truth table that can be easily checked and debugged for pin activity on LSI devices.	
41	**Sentry 600, 610, and Sentry II Pin Electronics Switching Time Characterization Program** PINCH collects and displays data on the dynamic switching properties of the Sentry 600, 610, and Sentry II.	9-75

APP. NOTE	TITLE AND ABSTRACT	DATE
42	**LMLOAD: A Program For Transferring Functional Test Data Between Local Memory and Disk Files** LMLOAD is an Assembly Language Utility program for transferring functional test data from Local Memory to disk and back again. Large bodies of SET F data, previously loaded in Local Memory, compiled, and stored on disc, may be executed from within a given test program without being present in its program source file. LMLOAD, thus, significantly reduces compile time.	9-75
43	**LMSAVE: A Utility Program Aid for Microprocessor Test Generation** LMSAVE is an Assembly Language Utility program for use with microprocessor test generation programs. LMSAVE currently supports six separate functions: • Transfers functional test data between Local Memory and files on disk. Data is transferred at run time thus obviating need for large quantities of SET F's in the FACTOR source file. This function is identical to that of utility program LMLOAD (Application Note 42). • Transfers single data items between FACTOR program and "virtual RAM memory" file on disk. Data is read or written in true random access fashion. • Allows input of user-generated microprocessor diagnostic program from cards or mag tape into the "virtual RAM memory." • Converts floating point numbers to Octal or Hexidecimal and returns them to the calling FACTOR program in TASCII format for printing on an output device. • Converts microprocessor opcodes to their corresponding mnemonics and returns them to the calling FACTOR program in TASCII format for printing on an output device. • Accepts data from an input device in either Octal or Hexidecimal and returns it to the calling FACTOR program.	9-75
44	**Measuring Frequency of Clock Generators Using External Sync on 10MHz Sentry Systems** This application note is to introduce external sync and to illustrate how the frequency of an on-chip oscillator can be measured. This technique also demonstrates how to measure the propagation delay of a pulse that is less than the delay of the sync pulse to T_0.	9-75
45	**Testing Universal Asynchronous Receiver/Transmitter Devices on the Sentry II** This application note discusses the basics of UART design, the problems and requirements of UART testing, and the strategy used in testing UARTs along with a program sample.	9-75
46	**Sentry II Pattern Processor: An Answer to Testing Large Dynamic Memories** This application note discusses lightly the hardware organization of the PPM and then goes on to illustrate and explain PPM programming, Address and Data Generator microword block formats, and the flowcharting of microword programs.	9-75

APP. NOTE	TITLE AND ABSTRACT	DATE
47	**TDX User's Guide** This TDX Users Guide describes the usage of the improved version of TDX, standard equipment on Rev. 10.2C. TDX (Tape Disc Transfer) is a file management tool for transferring groups of files between Disc and Tape. It is a DOPSY Utility which functions by generating an appropriate set of DOPSY commands (CREATE, FDUMP, JOB, NOTE, SET, VERIFY, UTILITY 'BMT', etc.) on disc in a Disc Input File (DIF). When all the commands have been generated, the Primary Input Device (PID) is pointed at this DIF. This causes the group of files to be transferred using these standard DOPSY commands.	10-75
48	**FST-1 Magnetic Tape Formats** This application note provides the necessary information to write a magnetic tape that can be processed on an FST-1 using available FST-1 Software. The information will also be useful to the FST-1 Assembly language programmer wishing to write or process tapes in these formats.	12-75
49	**LEAD: A Microprocessor Testing Tool** This application note discusses the LEAD (*L*earn, *E*xecute, *A*nd *D*iagnose) strategy of microprocessor testing; it includes the basic LEAD philosophy, a sample program cross-referenced by a program map to the generated functional test sequence, a sample functional test result printout, a sample parametric test result, a sample yield analysis, and a sample shmoo plot. LEAD allows microprocessor diagnostic programs to be written in the microprocessor's own language. A reference microprocessor is used while the tester learns the microprocessor's responses to a given set of stimuli. Once this truth table of responses and stimuli is learned, it can be used with any device test program.	12-75
50	**Testing Peripheral Interface Devices** This application note discusses the complexity of peripheral interface devices and the resultant testing problem, the limitations of earlier testing systems in facing this problem, and the Sentry II solution to the problem. Included within this discussion is a portion of a Sentry II peripheral interface device test program, shmoo plots showing parameter relationships, a yield analysis printout, and a datalog analysis of specific failures.	12-75
51	**SPLOT — Sensitivity Plot** This application note covers SPLOT, an overlay program that can be called from a TOPSY or a manual analysis command. The note includes sample uses of SPLOT, a program description, usage instructions, a description of resulting displays, and instructions for creating SPLOT from an object file.	3-76
52	**Extending the Test Rate Above 10MHz on the Sentry II** This application note is a sister piece to Application Note 28 and presents a simple way to extend the pulse rate seen by the DUT to frequencies higher than 20MHz while not exceeding the pin electronics power/duty cycle specifications.	3-76

APP. NOTE	TITLE AND ABSTRACT	DATE
53	**Sentry 600 Tester – Recovery of Files from TDX Tape with Unreadable Directory** This application note, written by a customer of FST, faces reading or writing problems on magnetic tape and delineates the recovery technique if just the directory is scrambled or if the files themselves are in trouble.	3-76
54	**Sentry Series Recommended Spare Parts Kits**	3-76
55	**PPLOG-A Fail Matrix Datalogger for the Pattern Processor Module (PPM)** This application note describes a PPLOG, a specialized datalogger which produces a 'fail matrix' map of a Random Access Memory test pattern being executed by the Pattern Processor Module of a Fairchild Systems Technology Sentry II test system.	6-76
56	**Test Head Calibration Techniques for Time Measurements on the Sentry II** This application note discusses the use of a Sentry II to obtain propagation delay measurements. A discussion of the basic accuracies to be expected using standard hardware and software techniques and a method to obtain time delay measurements approaching the basic time base resolution of ±160 ps are presented.	10-76
57	**Testing a TV Character Generator with the Sentry II Sequence Processor** A test program for a MOS integrated circuit intended for displaying a TV channel number on the screen of a TV receiver was recently completed. This program uses a number of sequence processor features and hopefully, this note will be easy to relate to the capabilities of Sentry II.	8-76
58	**How to Generate Complex Function Patterns – The Easy Way with a Sentry II** Sentry II computing power, coupled with efficient programming, can greatly reduce programmer workload and increase system efficiency. In the Sentry II, the Sequence Processor is a useful and versatile tool for achieving these operating advantages. With the right approach, it is easy to get the SPO to work.	12-76
59	**How to Use the Pattern Generator as a Clock-burst Counter on the Sentry 600 or 610** The pattern-generator feature of the Sentry 600 and 610 test systems is normally used to Test RAM's with various patterns. This note describes a different application: the repetitive use of a single test pattern in local memory, called a clock burst.	10-76
60	**How to Use the Sentry II Sequence Processor to Test an 8K x 25-Bit Ram PCB** Use of the Sequence Processor Module (SPM) in the SENTRY II semiconductor test system permits efficient testing of memory boards. A typical RAM-board testing procedure is described.	11-76

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61	**Load Board Decoupling Techniques for the Sentry Series Tester** Proper decoupling eliminates measurement accuracy degrading errors. This paper concerns itself with decoupling techniques applicable to the Sentry series testers.	12-76
62	**A Description of the 8080 Microprocessor Test Program Package Using the Sequence Processor** This application note describes the software program package designed to test and evaluate the 8080 8-bit, N-channel microprocessor. Features of the Sentry II or Sentry VII Sequence Processor Module are brought into play to increase the efficacy of the test situation.	2-77
63	**SPLOT — Sensitivity Plot (Including Revisions 1, 2, and 3)** This application note is a thorough update to application note #51.	2-77
64	**Local Memory Address Mode of the Pattern Processor Option** This application note describes the use of the Pattern Processor Module (PPM) in testing Programmable Read Only Memories (PROM). The basic principles of the Pattern Processor, operating in a local memory Address Mode (PPAM), are described.	4-77
65	**PXLOG — Pattern Execution Log for Sentry PPM Program (Preliminary)** PXLOG (Pattern EXecution LOG) is an assembly-language program providing observation of sequential events execution from the Pattern Processor Module (PPM) program execution. This application note describes how pattern execution may be verified and how programs under development may be debugged.	5-77
66	**Testing 100K ECL Devices on the Sentry Test System** This application note discusses five problems that are associated with testing 100K ECL devices and solutions proposed — using a specific device within the 100K family.	10-77
67	**Description of the Intel 8085 Microprocessor Test Programs for the Sentry II/VII with Sequence Processor Module** This application note describes the software program package of test and support programs for incoming inspection or engineering evaluation of the 8085 microprocessor. The diagnostic program is a software compatible extension of the 8080, described in application note #62.	11-77
68	**Testing on the Sentry High-speed Test Station** This application note gives several examples of techniques for using the Sentry high-speed test station to its fullest advantage.	12-77

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