AUTOMATED TESTING

OF

INTEGRATED CIRCUITS

An Instructional Course

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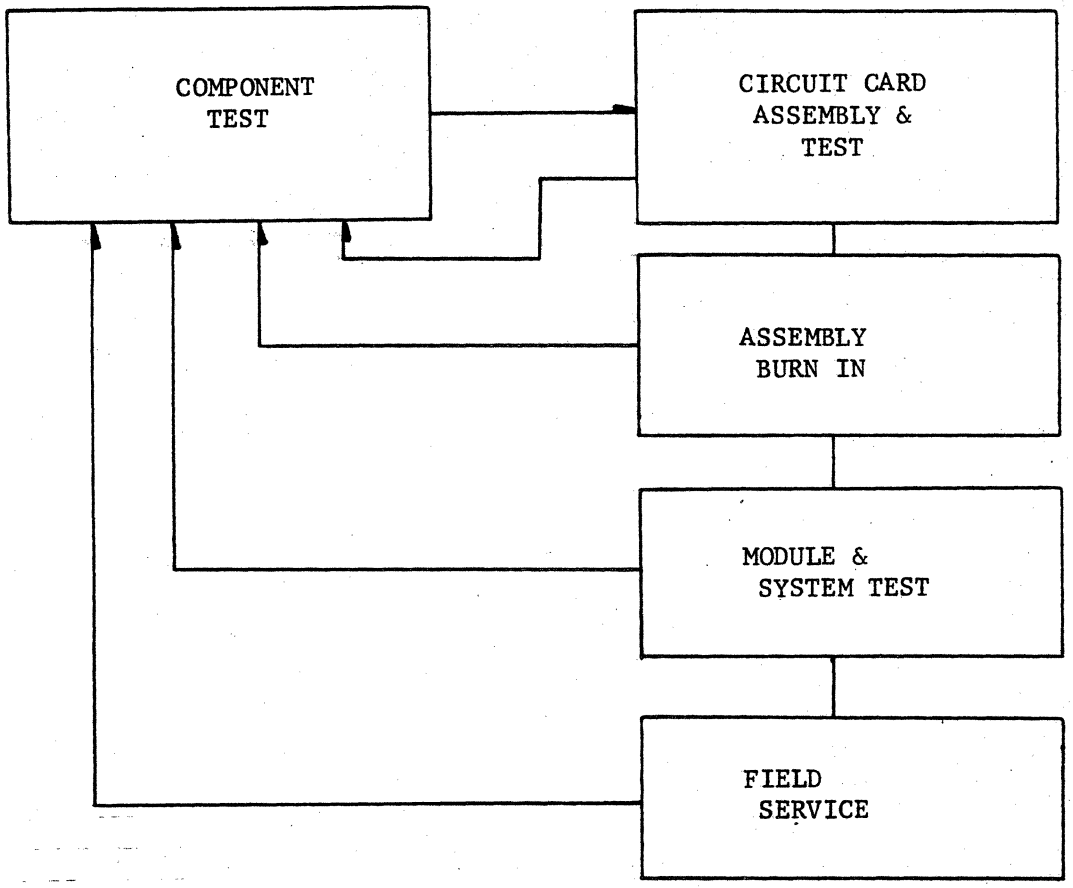

CORPORATE TEST PLANNING

FIG. I.1

1.0 LARGE SCALE INTEGRATION TESTING - GENERAL TECHNIQUES

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1.1 Introduction

The development of an LSI final test plan has as its overall objective the delivery of a component with a guaranteed performance margin. Together with an effective reliability effort, this test plan will produce components that work from the beginning to the end of product life.

The plan is not developed spontaneously. A great amount of engineering effort and feedback from everyone involved is needed to generate an effective plan. For this reason, we can distinguish several stages in the development of a final test plan: 1) General Testing Stage in which types of test, impact of time, money and management are the background for the other stages; 2) Device Familiarization Stage in which the component is learned and massaged in order to uncover marginal parameters and vector sequences; 3) Device Characterization Stage in which the most marginal parameters are studied over many differently processed devices in order to establish usability; 4) Final test plan stage in which the parts are tested effectively and their test performance monitored along with their factory and field behavior.

1.2 General Testing Stage

Throughout the development of the test plan, many factors of a general nature shape the specific test strategies chosen. These factors are first enumerated so that their effect on the test plan may be weighed and considered.

The test plan and its development will differ depending upon whether one is a manufacturer of the device, a user, or both. Each group uses the same techniques through the familiarization and characterization stages, but from different viewpoints, namely, pre and post final data sheet. The manufacturer is more cost conscious; whereas, the user is more reliability oriented.

The test plan must be a coordinated effort of the Evaluation Department, the Test Department, the Assembly Test Department and Field Service. Only with such an integrated effort can cost effective testing be done so that testing is not underdeveloped (which results in increased manufacturing costs) or overdeveloped (which results in increased test costs).

Testing is a corporate responsibility. (See fig. I.1) The advantage gained at any point in the manufacturing of a finished product can be easily decimated by not returning accurate and complete data back to the test organization. If the field and/or factory rejection rate is high and no feedback is provided to the test area, no cost savings or improvement can be realized. Proper records show up low reliability parts and deficient manufacturers. If failures are logged on a percentage used basis, the biggest and most serious problems can be attacked first.

It must be recognized that the component test engineer is a specialist and possesses unique skills. The nature of the job requires him to have an engineering background, knowledge of device physics, circuit design experience, high level and possibly machine level programming knowledge, and a basic statistical background. These tools are required for the science of testing. The art of testing further requires a knack of discerning relationships, an eye towards simplification and the ability to diagnose and trouble shoot. The addition of reliability engineering, including knowledge of different technology's failure mechanisms, is another valuable asset. Experience is an absolute necessity. Relegation of testing and test engineering to secondary roles is an invitation to added cost.

No amount of testing can give a part quality or make a part reliable. The test can only comment on the quality already present in the device. The question of reliability is a separate issue, in which testing plays an ancillary role.

The final test plan costs money. Yet, testing is cost added in order to avoid cost later. Equipment, manpower and time are all part of this added cost. The familarization and characterization stages that follow will prove to be cost avoidance programs because they increase the effectiveness while shortening the test time of the final test plan. These considerations are general in nature and work themselves into every phase of testing.

The formula for a good final test plan is planning. Each step must be planned and documented. Planning for failure must also be included. A few examples illustrate why: (subset of Murphy's Laws)

a) The test that will fail is the one that has been omitted.

b) The test system will always fail in such a way as to pass bad parts.

c) The most important parameter will never be characterized.

d) The test manager has no testing experience.

e) Automatic handlers are not automatic.

f) Problems always disappear when probing with a scope.

g) The application never matches the test requirement.

h) The manufacturer with the best part goes out of business.

1.3 Familiarization - Finding the Weaknesses

The familiarization stage in LSI test plan generation is for the most part a "sleeves rolled up", hands-on process. It is the stage in which the test engineer uses every tool at his disposal to learn the device. If the engineer's own experience is limited, if his arsenal of hardware and/or software tools, or his time, or his information is limited, then the results of this

Final Test Plan

The final test plan will depend greatly upon managerial impact. This impact at the corporate level implies a commitment in dollars to do a reliable and quality manufacturing job. Management at the department level must mirror this and base judgements on data and studies provided by engineering staff. The role of the test engineer is central. When engineers begin to think they can manage, and managers begin to engineer, mistakes are made. The engineer's job is to supply correct and complete data for his management staff with which to make decisions. Where decisions must be made based on little or no data, mistakes are made. The amount of time and money needed by engineering must be tempered with the overview provided by management.

The final test plan must be based on knowledge. This knowledge is not only of a first-hand nature. It is important to know people, people associated with the manufacturer of the device, test equipment, other users and vendors. These people provide a ready library of information regarding all types of components and their tests.

The final test plan must not necessarily be a totally do-it-yourself project. Doing it yourself is not always the most cost effective way, whether this pertains to the building of test equipment or writing the test program. The merits of buying, rather than making, must be strongly considered especially regarding the test systems.

The final test plan can be complex or simple. It should not be as simple as plugging the component into the system. System testing as a substitute for component testing is lacking in its ability to ascertain margin in the component under test.

The final test plan can be made up of many types of tests. Technically, the test engineer must be aware of the advantages of the different types of tests and choose those required. DC Tests such as leakage and breakdown are specified for process quality or fan in/fan out. Stress tests are required for reliability considerations. Forward diode tests are useful for continuity and process information. Power current measurements are necessary for reliability and board design margin. Resistance tests are necessary on active or passive pull up devices. Proper output drive levels are necessary for system design margin.

AC tests differ more in terms of semantics than in actuality. For clarity, an AC functional test is one performed with a set of input/output voltage settings, a set of input/output timing settings, and a particular truth table. An AC parametric test is one in which some number, such as access time, rise time, fall time or propagation delay is measured directly. Other examples of AC tests are the frequency of a VCO or the distortion of a UART output signal. The test engineer must decide if his requirements call for AC parametric tests and which AC functional tests are required to ensure margin.

The final test plan requires the time spent in characterizing a part to be quickly used. Hence, the marriage of engineering and production test equipment is a prime consideration. Cross compilers and universal test languages have been partially developed, but not to the extent that a few days turnaround is possible at this time.

TRUTH TABLE PREPARATION

1. SEGMENT DEVICE INTO FUNCTIONAL BLOCKS.
2. PREPARE FLOW CHARTS TO TEST LEGAL COMBINATIONS.
3. PREPARE FLOW CHARTS TO TEST ILLEGAL COMBINATIONS.
4. FILL IN VARIATIONS FOR 2.
5. BUILD AUTOMATIC VECTOR GENERATORS BASED ON 2.
6. USE SIMULATION TO CHECK COMPLETENESS OF 5.

FIG. II.1

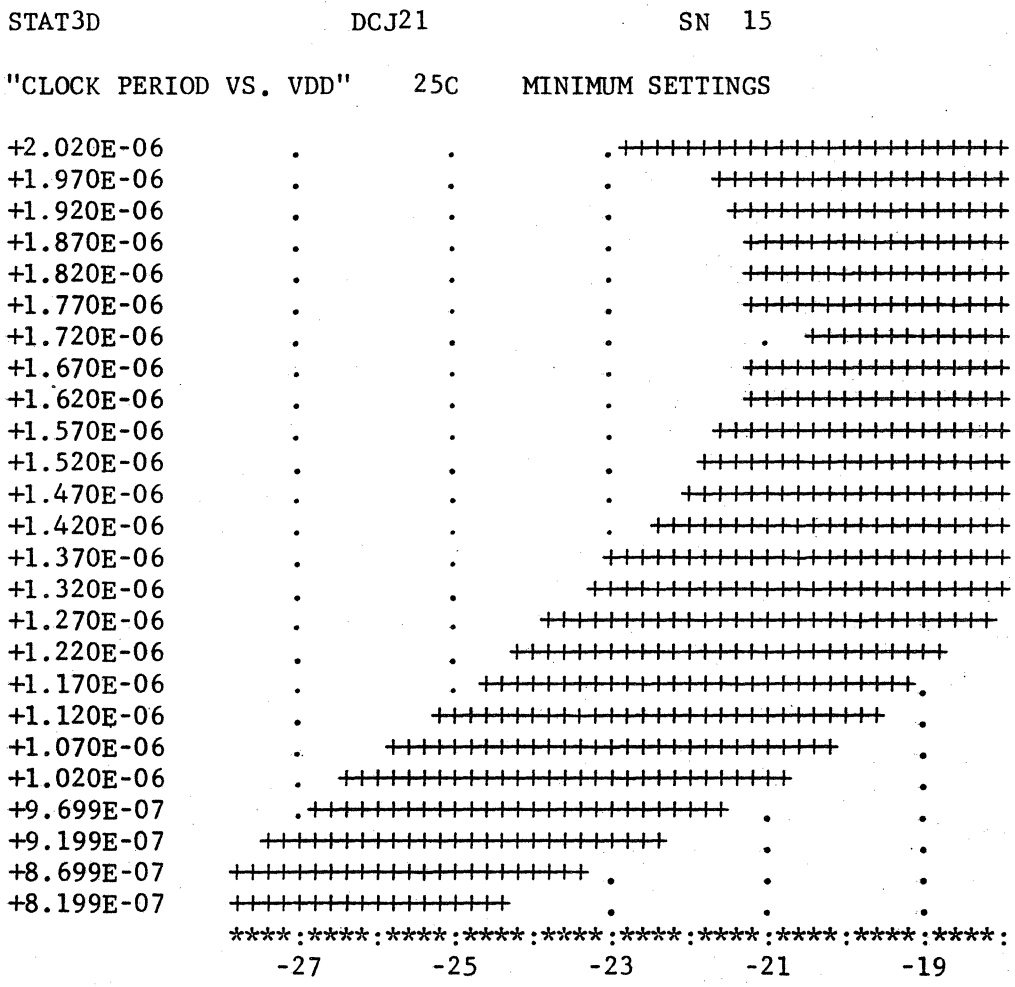


FIG. II.2

familiarization will be limited and the final test plan will be less than optimum. Familiarization is an easily understood but subtly applied art. The importance of failures is the keynote of LSI familiarization. The type of failure uncovered at each point should be carefully noted and understood.

In familiarization, experience is the major factor. An experienced test engineer with inferior equipment will uncover more information than an inexperienced man with sophisticated tools. Experience causes one to take note of a small item that would otherwise go uncovered, and experience provides quick and right decision when difficulties arise.

While the engineer needs the hardware to manipulate input voltage and timing parameters, he must first of all address himself to the functional complexity of LSI and the problem of selecting input vectors and sensing output response. (See fig. II.1)

This combination and sequence of logical inputs and outputs has been variously referred to as a set of vectors, a truth table, a test pattern, a functional test and a test algorithm. We will use the words "truth table" to describe the operational states of the device.

In the case of LSI, truth tables sometimes run in the millions of cycles without being all exhaustive. Each truth table must first of all exercise all combinations that are functionally legal and elicit definite known responses. For the sake of completeness, it must also exercise illegal combinations to ensure that the device ignores these. How many of each kind is what familiarization is all about. A minimal or chip-alive truth table will exercise each function or operation at least once.

It is, therefore, the first task of familiarization to establish the minimum set of vectors which assures that the device is functionally operating. If a register can be tested with four simple combinations, there is no reason to test it with all the binary combinations possible.

Experience has taught that simple combinations such as all ones, all zeroes, alternate ones and zeroes, and the complement for any operations involving buses, registers, and serial devices are sufficient. The combination of bits needed for exhaustive testing is 2^N, not counting transitional states. These vectors have not generally shown failure modes other than those discovered by the more simple patterns.

There are systems that automatically check or even generate test vectors using "stuck" and "open" techniques. While these may suffice for test purposes, experience has indicated that when the device tests good but fails at the system level, the test must be able to simulate the system's operation to uncover and understand the failure.

With very few exceptions, the truth table is someone's definition of all inclusive and worst case. The truth table normally comes from: a) A device design engineer who knows or suspects potential trouble areas; b) A system engineer who is contemplating the use of the part and has ideas of how he wants it to work and; c) A test engineer who, because of experience and equipment adds, subtracts, or even generates the testing truth table. This truth table will later be amended by characterization results and experience in both testing and product usage.

testing will soon appear. A table of percentage to failure from worst case or nominal should be constructed so that later in the indepth characterization stage the most sensitive (having least margin) parameters can be investigated for many parts and the insensitive parameters can be dismissed. This list should definitely include any parameters that were omitted on the data sheet. The reasons for their omission quickly become clear.

As examples of sensitivity plotting, figure II.2 illustrates simple pass/fail ranging for two parameters. Figures II.3-4 are samples of AC parametric measurement.

It is important that each plot include complete vertical and horizontal data, background data and other pertinent descriptive information such as program identification, test temperature, and any special conditions surrounding the test.

All of the examples have been composed of two parameter plots. One can study the behavior of single parameters, but the insight gained is minimal. Three dimensional shmooing is also possible on a graphics terminal or with a pseudo third dimension as figure II.4 shows.

In investigating a device for sensitivity, several choices become available. The solutions are a matter of philosophy.

The engineer must distinguish between logical failures and level failures. A level failure indicates that the part is operational but does not meet prescribed output timing or voltage conditions. A logical failure indicates that the part is functionally incorrect. Level failures, while falling outside of data sheet operation, indicate that the part is still operational. Tighter processing or simple cell change may cause data sheet operation. The logical failure means that internal logic is not able to respond under the present set of conditions. Whether one ranges to specified output limits, or to looser output limits is entirely the engineer's choice. However, should one choose to range to specified limits, he must understand that the failure modes that are uncovered are blurred by the performance of the output driver stage. The preferred method is to range loosely so that the true internal failure modes may be noted and attacked. The failure mode of the output stage is then treated as a separate matter. Both sets of data are important, and a decision must be made relative to indepth characterization.

During LSI familiarization, while it is important to visualize where the sensitives of the device are and where the device will or will not work, by far the most important and the more difficult, more time consuming task is the tabulation of the failure modes at points where the device no longer works. It is by careful analysis of the failures at these points that the sensitive functional modules emerge. One automatic method is to superimpose a failure key over the usual pass/fail indicators of a normal shmoo plot. (See Fig. II-5.)

This type of plot becomes difficult to composite unless one restricts the number of failure modes being studied. An alternative is to use separate shmoos for separate functions. This method is used with Rams, where single patterns are used for each plot.

Trivial functions such as disable/enable inputs and inputs that monitor switches should never be omitted from the truth table, or merely tested statically.

The truth table should be organized hierarchically. Logically independent modules should be exercised before dependent modules so that fundamental failures will appear first. This is very important in cases where the test being used will abort as soon as any failure is noted. Most automatic test systems work this way.

Armed with a truth table; means for controlling input parameters (hardware and/or software control); and means for output monitoring (CPU, scope, logic analyzer) the test engineer can now address himself to the device and get the device's "feeling". About fifty parts from the same supplier are sufficient to indicate general weaknesses in a part, provided these parts are not hand selected.

The familiarization plan at this point is not haphazard. A theoretical understanding of the device gleaned from a logic schematic, circuit layout and cell placement might indicate potential marginal or race circuits. These should have been studied if possible. Experience with similar parts often leads to similar sensitive areas. Talks with others using the same circuit, are beneficial in getting a jump up the learning curve.

After the engineer has carefully studied data sheets (whether intended, preliminary, or final) and has a clear idea theoretically of the limits that the device will be required to perform to, he should plan his approach and keep documented results. This documentation plays an important part in later problem analysis. Depending on how complete it is, much time may be saved. Too often work has to be repeated because results were not kept on the first pass.

A nominal valued program must first be organized so that we are assured the device is being massaged correctly. Secure in the knowledge that the parts are at least working somewhere, one begins to study the iteration of each parameter against the other. This is known as "shmooing", "sensitivity plotting", "ranging", "characterizing". If the results of all services for one set of ranged parameters are similar, it suffices to store a sample with notations of the failure mode in each of the non-operating areas.

A form of timing variation that has proved beneficial, is the use of "scaled" timing. All timing relationships are defined in dependent terms related to a single variable. By ranging the single variable against operating voltage a gross overview of device operational range is provided.

One normally begins with a set of "worst case" rather than nominal conditions because this leads to failure sooner with much tighter limits on the parameters in question. The choice is up to the test engineer.

Parts should be ranged beyond the minimum and maximum data sheet parameters to the point of failure. This data then indicates where the devices operate, how much margin they have, and what kind of screening the supplier is doing. If the parts are working just beyond the minimum or maximum point, a lack of correlation between the incoming inspection group and the supplier's final

THREE AXIS SHMOO PLOT

DEVICE TYPE:	4K RAM	BATCH :	LOG DATE: 09/16/76
PART NUMBER:	4096-5	WAFER :	LOG TIME: 15:47:51
TEST PRGM :	XNBOB	DEVICE:	PRT DATE: 09/16/76
LOAD BOARD :	392366	STAGE :	PRT TIME: 15:47:54

V :VDD3 TRAC (NS)

12.00	251	251	251	251	251	251	252	252	252	252	253	253	254	255	256	257	259
11.75	252	253	253	253	253	253	254	254	254	254	255	256	256	257	258	260	260
11.50	255	255	255	255	255	255	255	255	256	256	257	257	258	259	260	262	263
11.25	258	258	258	258	257	258	258	258	258	259	259	260	260	261	262	264	265
11.00	261	261	260	260	260	260	260	260	260	260	261	261	262	263	265	266	268
10.75	265	264	264	264	263	263	263	263	263	263	263	264	265	266	267	268	270
10.50	269	269	268	268	267	267	267	267	267	267	267	267	268	269	270	271	273
10.25	274	273	273	272	271	271	271	270	270	270	270	271	271	272	273	274	276
10.00	280	279	278	277	276	276	275	275	275	275	275	275	275	276	277	278	280
9.75	287	286	284	283	282	281	281	280	280	280	279	280	280	280	281	282	284
9.50	295	293	291	290	289	288	287	287	286	285	285	285	285	285	286	287	289
9.25	307	304	301	300	298	296	295	293	293	292	291	291	291	291	292	293	295
9.00	325	320	316	313	310	307	305	303	301	300	300	299	299	298	299	300	-
8.75	359	348	339	333	327	322	319	316	313	311	309	308	307	307	307	308	-
8.50	-	-	-	-	359	348	340	335	330	326	323	320	319	318	317	-	-
8.25	-	-	-	-	-	-	-	-	359	349	343	338	334	332	330	-	-
8.00	-	-	-	-	-	-	-	-	-	-	-	-	361	355	-	-	-
7.75	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7.50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7.25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7.00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

-5.00 -4.75 -4.50 -4.25 -4.00 -3.75 -3.50 -3.25 -3.00 -2.75 -2.50 -2.25 -2.00 -1.75 -1.50 -1.25 -1.00

V :VBB3

FIG. II.4

STAT3D TEST PLAN 4008B SN 3

"OUTPUT ACCESS WITH MINIMUM VOLTAGES"

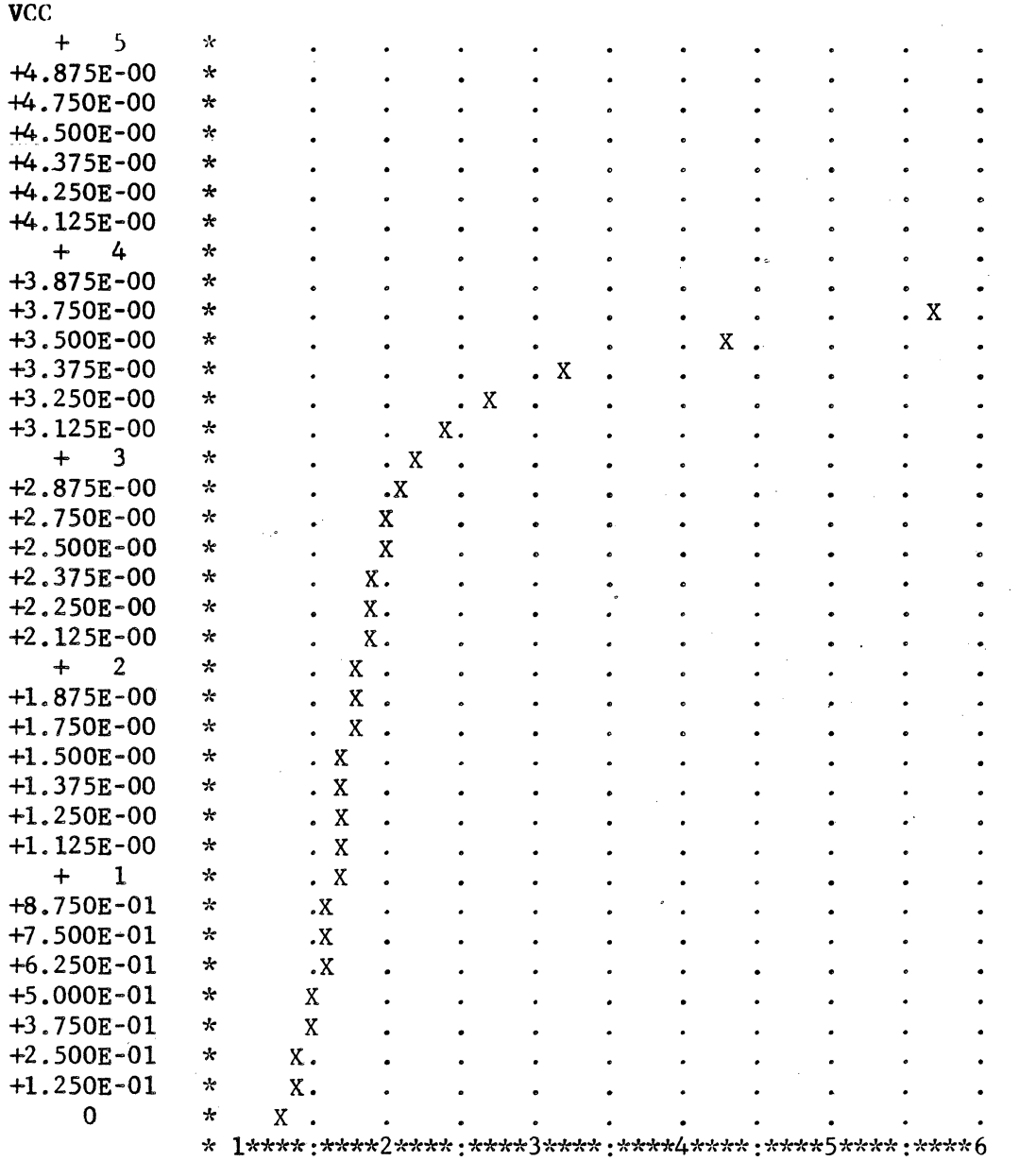


FIG. II.3

The investigation of all functional failure modes at the same time by using a fail buffer or displaying them line by line is a difficult task. Because of the mass of data already present to be analyzed, this task is better left to the monitoring stage of the final test plan. If plenty of margin exists for two different parameters, then the failure mode becomes less important.

Failure mode analysis is important for later final test correlation. The test engineer must be certain that, as final testing proceeds, no new failure modes begin to appear that were not present in initial familiarization work.

To be complete, familiarization must also be done at maximum operational and junction temperatures. While the operational areas will shift, no new functional failure modes should appear. Temperature effects on frequency and propagation delay are a few examples of shifted operational areas.

The effects of burn-in should be studied. This acceleration should cause little or no change from the start of burn-in to the end of burn-in in operating areas of a device. This is not always true and varies from manufacturer to manufacturer. No new failure modes should be seen for a stable design and process.

In LSI familiarization, test equipment also plays an essential role. From the above discussion, familiarization of LSI requires a general purpose computer controlled test system. Since eventually, a rigid production test will emerge from all the work, the relationship between this familiarization/characterization system and the dedicated production test system must not be minimized.

We are not yet at a stage of universal test language or a simple program conversion from system to system. Hence, the merits of available systems must be carefully considered for your requirements.

The usefulness of the system to the test engineer must be thoroughly considered. Programming must be flexible yet simple. Program entry and change must be minimally time consuming. Allowance of program change (hardware function) on the fly and display of program status on the fly are a must. Interpretation of results, repeatability and drift are also important considerations.

The systems must have the hardware capability required by your application. Voltage/timing ranges, accuracies, resolutions and drifts must be analyzed. Pin formatting modes such as RZ, NRZ, RI, XOR, double pulse must be considered. The flexibility of the truth table generator should include on the fly subroutining and reformatting. All hardware functions must be programmable, modifiable on the fly, and displayable.

The hardware and test plan should be able to handle certain properties which, while not exclusively characteristic of LSI, naturally lend themselves to LSI circuitry. Few test plans translate into a one for one hardware pin assignment.

Examples of these properties are:

STAT3D TEST PLAN DCC38 SN 15

NOMINAL BACKGROUND
BASIC VECTOR TABLE - LOOPBACK,REPEAT,ALARMS MISSING

PERIOD VS. VG1

```
                ****:****:****:****:****:****:****:****:****:
+1.792E-05                                                  CBA
+1.742E-05                                                  CBA
+1.692E-05                                                  CBA
+1.642E-05                                                  CBA
+1.592E-05                                                  CBA
+1.542E-05                                                  CBA
+1.492E-05                                                  CBA
+1.442E-05                                                  CBA
+1.392E-05                                                  CBA
+1.342E-05                                                  CBA
+1.292E-05                                                  CBA
+1.242E-05                                                  CBA
+1.192E-05                                                  CBA
+1.142E-05                                                 CCBA
+1.092E-05                                                 CCBA
+1.042E-05                                                 CCBA
+9.918E-06                                                CCBAA
+9.418E-06                                                CCBAA
+8.917E-06                                                CCBAA
+8.417E-06                                                CCBAA
+7.917E-06                                                CCBAA
+7.417E-06                                               CCBAAA
+6.917E-06                                               CCBAAA
+6.417E-06                                              DCCBAAA
+5.917E-06                                             DCCCBAAA
                ****:****:****:****:****:****:****:****:****:
              -18       -16       -14       -12       -10
```

	LOC	STEP	PIN
A	3	10	FC MATCH
B	3444	28	16,20,24,27,31
C	3147	15947	1,60
D	37	2065	48

FIG. II.5

1.4 Characterization - Quantizing the Weaknesses

In depth characterization has for its primary purpose the collection, reduction and distribution of parametric data over many lots in order to establish a data base for production testing and monitoring.

Familiarization has indicated where the device is sensitive, and what shmoo plots are necessary in order to see how the sensitivity varies from sample lot to sample lot. A program containing these shmoo directives is now organized. This program is quite rigid. The sample must be chosen so that it is representative of the total population and statistically significant. It is better to choose small samples from many lots rather than large samples from a small number of lots. Data should be presented in both single lot and combined lot form. Combined lot data shows total capability. Single lot data shows drifting trends.

There is a choice in the use of characterization. The performance of "x" times "y" tests is desirable for the sake of completeness, but many times results in hours of test time per device because of the length of a single truth table pass, or because of the nature of the shmoo as demonstrated by a test associated with refreshing or low frequency behavior. In these cases, it is necessary to change from incremental stepping to a binary search method. (See Fig. III-1).

Instead of testing at each point between a minimum and a maximum limit, a test is performed first at the upper extreme, then halfway between the upper and lower limits, and then either halfway again higher or lower depending on pass/fail results and the search for either an upper or lower limit. This is the fastest way of arriving at the limits of an operational parameter. However, the method can lead to false results in at least two cases: 1) The large differential voltage swings may capacitively charge internal nodes momentarily altering internal operations; and 2) The technique may bypass operational "holes" where the device has two operating points. Both pitfalls can be avoided if their presence was observed in familiarization. Presentation of binary search information is easily handled by assuming that the part operates from the upper to the lower extreme and by merely filling in the incremental array for plotting.

A decision must also be made regarding characterizing from pass to fail or vice versa. Because of intertwined junction temperature effects, the choice of ranging from high to low voltages may have better results than ranging from low to high. Hysteresis effects can be both harmful or helpful. In cases where the device is marginal, these small points may become cause for a legal battle.

Inherent in the characterization process is the decision to store raw data, reduced data or both. Final reports need contain only reduced data. If the raw data has been carefully scanned and gross departures explained, then its storage value is minimal. Careful numbering of components and printouts will save a good amount of retracing in the data analysis.

Presentation of characterized information closely resembles the familiarization plots discussed earlier. It adds the dimension of quantity to

A. High speed parallel/low speed serial devices - truth tables may have to be artificially segmented in order to fulfill timing resolution requirements.

B. Asynchronous events - all testers are by nature synchronous. The testing of asynchronous events must be handled artificially.

C. Time multiplexed inputs - timing must be specified by more than two edges for a single pin.

D. Transducer inputs - inputs that must monitor switches, capacitors, or other sensors and must functionally switch these sensors and still be available for DC testing.

E. Free running and free starting devices - the tester must be able to be slaved to the device for free running devices and able to synchronize itself by pattern and sequence recognition techniques for devices that are not presettable.

At every failure point, the engineer must know and be convinced that the failures are real, and not the product of a tester quirk or programming gaffe. A single example suffices. Any memory or register should not merely be written and read, but rather written with a complement pattern, and then written and read. This insures that each cell at each parameter setting in fact changed, and not merely "remembered" the old data.

Vicarious experience with the part can be obtained from both the manufacturer and other end users. The test engineer may require this information because he doesn't have enough time to devote to the familiarization stage or because he wants to supplement his own knowledge of the part. While he may know where a device does not operate and what the worst case pattern is, he may not have the expertise to understand why. The manufacturer certainly knows much about the part, but his knowledge is limited to what he has tried. An end user will usually refine this knowledge. For this reason, attendance at good seminars and symposia is a must. They provide an excellent interchange of information and ideas.

The engineer may elect or be forced to skip the whole familiarization process and go directly to characterization based on no or secondhand information or have someone else do the characterization. In either case, knowledge is relegated to the third party, who is not responsible for the final test plan and thereby is not liable. The apparent savings in time will last until problems appear that were not present initially. It must also be stated, however, that there exist independent test laboratories which have advanced the science and art of testing and provide a most useful function because of their vast experience on a variety of parts. If your requirements, however, are not clearly understood or foreseen, then you may easily misuse their services.

The techniques of familiarization will uncover the part's weaknesses and relationship to the data sheet and indicate what areas must be characterized in depth on a large sample of parts.

replace simple pass/fail information, or averages to three dimensional data. (See Fig. III.2-3).

The presentation of DC characterization information is most successfully presented as both a distribution and a cumulative percentage or "s" plot. (See Fig. III.4).

The use of the mechanical concept of "centroid of the area" is an interesting method of presenting a figure of merit or a single number for an entire shmoo plot. Trending then becomes a simple matter of plotting the centroid, whether for two dimensions or three.

High and low temperature characterization and pre- and post-burn-in characterization are considerations that familiarization should have indicated as necessary or unnecessary. Modified forms of characterization for these conditions can be done for the sake of completeness.

The characterization phase involves much analysis. Automatic handlers and good programming should present a wealth of raw and composite data for the engineer to study, tabulate and summarize.

If characterization has been properly done, then it leads to the formulation or corroboration of a realizable data sheet. It predicts what percentage of parts will fail at incoming inspection and how they will fail.

Characterization will lead to the optimum minimum program that we can run in order to expect a quality part. Minimum, because it contains only necessary truth table statements and combinations of voltage and timing and optimum because it is the least amount of testing necessary to ensure an acceptable failure rate.

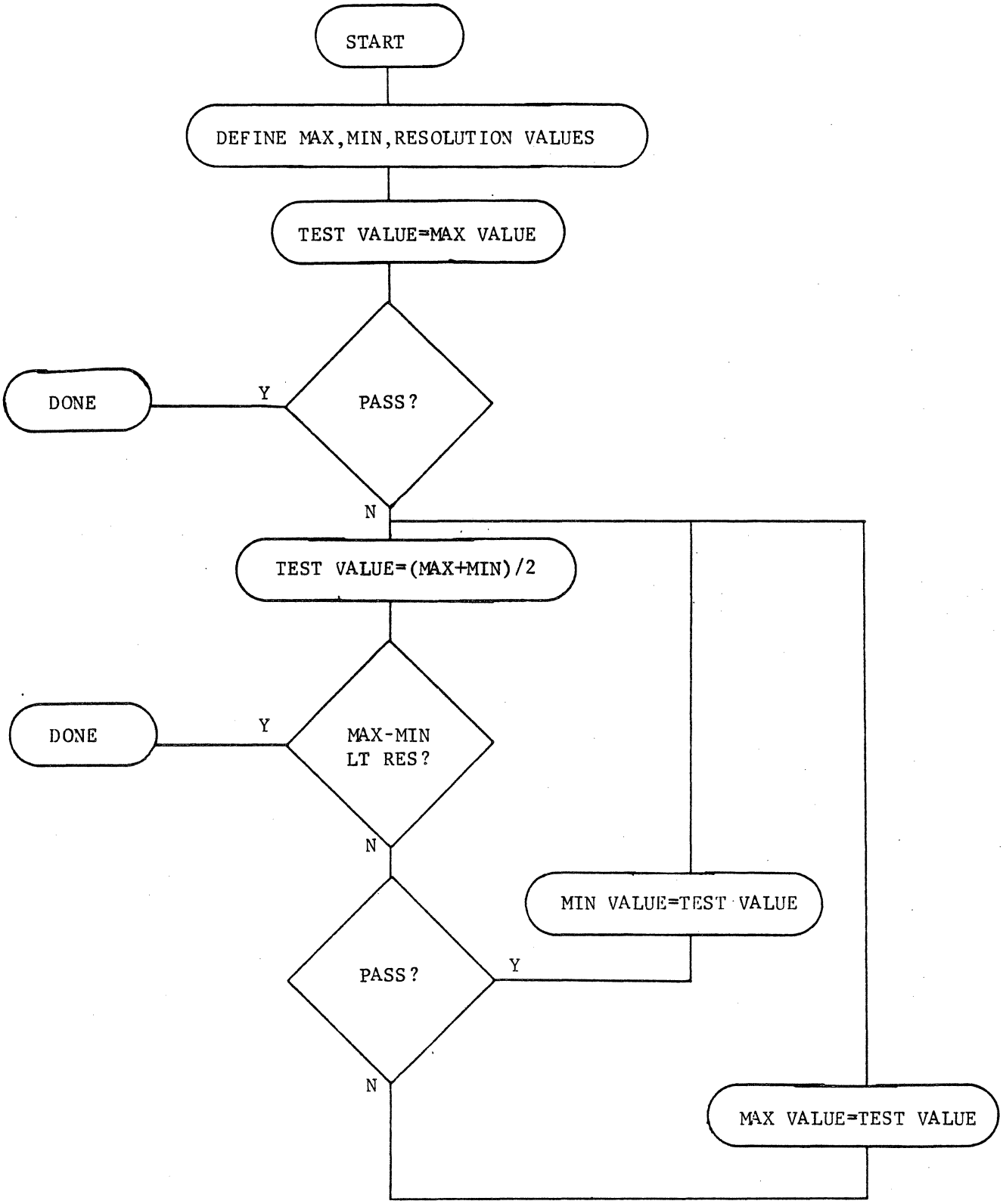
The engineer may elect or be forced to omit indepth characterization and go directly to a final test plan. In so doing, he runs the risk of not understanding the failure he experiences at both the test and set level, and of not knowing how good or bad is the part he is using.

1.5 Final Test Plan - Monitoring the Weaknesses

The results of familiarization and characterization have led to the development of a minimal functional and dc test program that guarantees the accepted part has adequate margin for its use.

Physically the test program consists of: A) Documented headers showing pin usage, revision levels, program options, binning options; B) Continuity tests that eliminate rejection due to faulty insertion or tools; C) Functional tests with the truth table and voltage/timing conditions that were shown to be necessary in characterization; D) DC tests that are required for reliability or interface considerations; E) Failure bins that automatically generate failure rate and modes; F) Stress tests that weed out potentially weak devices; G) Copious explanatory information and flow charts.

The truth table used in the final test is a composite of the characterization truth table. Whereas the characterization truth table exercised functions



BINARY SEARCH FOR AN UPPER OPERATING LIMIT

FIG. III.1

```
STAT3D              TEST PLAN    VCO2            SN    74


           TCI  --  VCO PERIOD  --  COLD

VDD=-008     VGG=-012     VGGH=-016     VC2=-024

   VC1
             *.****.****.****.****.****.****.****.****.****.****.
-2.250E+01   *
   - 22      *
-2.150E+01   *$0
   - 21      *9100
-2.050E+01   *601100
   - 20      *51 111100
-1.950E+01   *2111012200
   - 19      *  013201210
-1.850E+01   *    11220220
   - 18      *      1220220
-1.750E+01   *       0231120
   - 17      *         123130
-1.650E+01   *          122130
   - 16      *          013230
-1.550E+01   *            013230
   - 15      *              13230
-1.450E+01   *              013230
   - 14      *               013230
-1.350E+01   *                014320
   - 13      *                  1422
-1.250E+01   *                   1431
   - 12      *                    1441
-1.150E+01   *                    01441
   - 11      *                     01431
-1.050E+01   *                      01431
   - 10      *                       01440
-9.500E-00   *                        01440
   -  9      *                         00540
-8.500E-00   *                          00540
   -  8      *                           0441
-7.500E-00   *                            0441
   -  7      *                             01530
-6.500E-00   *                              01440
   -  6      *                                1242
-5.500E-00   *                                  1341
   -  5      *                                    12420
             *.****.****.****.****.****.****.****.****.****.****.
                                  PERIOD
        +1.140E-05     +1.590E-05     +3.490E-05     +1.150E-04
             +1.226E-05     +1.954E-05     +5.022E-05
                  +1.365E-05     +2.541E-05     +7.498E-05
NUMBER OF DEVICES TESTED ARE     73
```

FIG. III.3

```
STAT3D              TEST PLAN DC021          SN     137

LOT  T3512      "PERIOD VS. VCH"      90C      8/8/75

SECONDS       ****:****:****:****:****:****:****:****:****:****:

+1.792E-05  *                 23678999$$$$$$$$$$$$$$$$$$$$7
+1.742E-05  *                 13678999$$$$$$$$$$$$$$$$$$$$7
+1.692E-05  *                 13578999999$$$$$$$$$$$$$$$$$$7
+1.642E-05  *                 124688999$$$$$$$$$$$$$$$$$$$8
+1.592E-05  *                  24688999$$$$$$$$$$$$$$$$$$$9
+1.542E-05  *                  13678999$$$$$$$$$$$$$$$$$$$9
+1.492E-05  *                  03578999$$$$$$$$$$$$$$$$$$$9
+1.442E-05  *                   3478999$$$$$$$$$$$$$$$$$$$9
+1.392E-05  *                   2367899$$$$$$$$$$$$$$$$$$$9
+1.342E-05  *                   2367899$$$$$$$$$$$$$$$$$$$8
+1.292E-05  *                   1356899$$$$$$$$$$$$$$$$$$$8
+1.242E-05  *                    2468999$$$$$$$$$$$$$$$$$$9
+1.192E-05  *                    1367899$$$$$$$$$$$$$$$$$$9
+1.142E-05  *                     347899$$$$$$$$$$$$$$$$$$$
+1.092E-05  *                     236889$$$$$$$$$$$$$$$$$$$
+1.042E-05  *                     136789$$$$$$$$$$$$$$$$$$$
+9.918E-05  *                      247899$$$$$$$$$$$$$$$$$8
+9.417E-05  *                      136789$$$$$$$$$$$$$$$$$9
+8.917E-05  *                       256889$$$$$$$$$$$$$$$$8
+8.417E-05  *                       135789$$$$$$$$$$$$$$$$9
+7.917E-05  *                        23678$$$$$$$$$$$$$$$$80
+7.417E-05  *                        25689$$$$$$$$$$$$$$$$8
+6.917E-05  *                         3478999999$$$$$$$$$92
+6.417E-05  *                         025789999999999999991
+5.917E-05  *                           2578999999999999992

                ****:****:****:****:****:****:****:****:****:****:
           -4         -3         -2         -1          0         +1
                                    VOLTS

SAMPLE SIZE - 136
```

FIG. III.2

linearly, the production truth table should perform as many tests simultaneously as possible. The linear truth table can be kept by engineering for failure analysis. The truth table should be mapped to the local memory for ease of interpretation.

The test program is organized so that the most likely failure points occur first (after continuity and stress tests). This maximizes throughput and minimizes time spent on bad parts.

Only those necessary functional tests should be used. If the engineer has elected to or been forced to skip characterization then he must include many combinations lest he run the risk of passing bad parts.

Proper set up procedures prior to testing and at selected intervals during testing are most important. System diagnostic programs should have verified that the system is performing per its specification. A sizable number of benchmark devices should have been run to ensure that all tooling is in good order and to double check system operation. If the device taxes the limits of system operation, then self-calibrating procedures must be used before testing or, if necessary, before each device is tested.

An LSI test plan should also contain the ability to summarize fail data, or to pass failure information to a mass storage device for later on/off line reduction. Data collection can be done both on and off line. The choice is determined by throughput impact, resources available, tester capability, program capability, level of operator intervention. An LSI test plan should also provide for the characterization of every Nth device so that a running record of device performance may be monitored. The plan should include alarm controls so that when failures approach a predetermined limit, first set-up and then engineer support is called immediately and automatically.

The test program must keep track of numbers. How many were tested? How many passed? How many failed? How many failed each dc test? How many failed each functional test? These numbers are easily tabulated automatically, and can even be generated manually. Numbers are necessary for testing as inventory and throughput indicators, as well as efficiency and operator scorecards. In the case of LSI, the numbers are important because they are the entry point for any problem analysis.

The final test plan should be used first of all on the parts that were characterized so that an initial correlation may be established. The more or less steady state nature of characterization may lead to different results than the one shot nature of a final test. All differences must be resolved.

The test plan should include good engineering practices in building all load boards. Supplies should be adequately decoupled. Input pulse aberrations should be kept to a minimum. Output loads should reflect the system environment.

Concurrent with the inception of the test program, four tasks should immediately go into effect: A) Cost reduction; B) Yield improvement; C) System correlation and D) Supplier correlation.

```
STAT3D                TEST PLAN   DCA21              SN      34

PTRG RANGE 4 PROGRAM - PIN      8       BREAKDOWN @ 1 MICROAMP

VOLTAGE LT  ****1****2****3****4****5****6****7****8****9****10    CUM%

-026        +   .         .         .         .         .              3
-029        +   .         .         .         .         .              6
-030        ++  .         .         .         .         .             12
-031        +++++         .         .         .         .             24
-032        ++++++++      .         .         .         .             41
-033        ++++++++++    .         .         .         .             65
-034        ++  .         .         .         .         .             71
-035        ++++.         .         .         .         .             79
-036        +++++         .         .         .         .             91
-037        ++++.         .         .         .         .            100

            ****1****2****3****4****5****6****7****8****9****10

THE MEAN IS -3.248E+01
STANDEV  IS +2.451E-00


INPUT
************ COMPOSITE  PRINTOUT ************

VOLTAGE LT  ****1****2****3****4****5****6****7****8****9****10    CUM%
-030            .         .         .         .         .              0
-031            .         .         .         .         .              1
-032        +   .         .         .         .         .              3
-033        +   .         .         .         .         .              5
-034            .         .         .         .         .              6
-035        ++  .         .         .         .         .             10
-036            .         .         .         .         .             11
-037        ++  .         .         .         .         .             15
-038        +++ .         .         .         .         .             19
-039        ++  .         .         .         .         .             22
-040        ++++++        .         .         .         .             28
-041        +++++         .         .         .         .             34
-042        +   .         .         .         .         .             36
-043        ++++++        .         .         .         .             43
-044        ++++++        .         .         .         .             50
-045        ++++++        .         .         .         .             57
-046        +++++++       .         .         .         .             66
-047        +   .         .         .         .         .             68
-048        +++ .         .         .         .         .             72
-049        +++++         .         .         .         .             77
-050        ++++++++++++++++++++  .         .         .            100
            ****1****2****3****4****5****6****7****8****9****10
NUMBER OF SAMPLE DEVICES - 34
THE MEAN IS -4.375E+01
STANDEV  IS +4.051E-00
```

FIG. III.4

References:

1. R.F. Widmar, "Backdoor Characterization - an essential element of LSI testing", Semiconductor Test Symposium 1974.

2. E.R. Hnatek, "User's Tests, not data sheets, assure IC performance, Electronics, November 27, 1975.

3. Mr. Marshall, "Logic in Testingland", EDN Reprint.

4. R.E. Huston, "The Art of LSI Testing," Fairchild Technical Bulletin 8, June, 1976.

5. Datatron, "Preconditioning and Testing Semiconductors," Handbook.

The engineer should look for tests which return no or few failures, for sections of the truth table which never fail, for improving the order of testing. Elimination of these will reduce the cost of testing.

Initial test plan usage must include samples of system tested parts to doubly ensure that no system defective devices are being passed in testing. The exchange is inherently self-balancing. System failures will cause additions to the test program, and the elimination of critical tests will cause system malfunction.

By stacking failure modes and concentrating on the most common failure, yield improvements can be made. This is the method of backdoor characterization as outlined in the 1974 Cherry Hill Test Symposium paper by this author. Backdoor characterization is also necessary to guarantee that the nature of the part as characterized did not change.

In cases where familiarization and characterization have been bypassed, backdoor characterization will indicate device sensitivities that should be characterized.

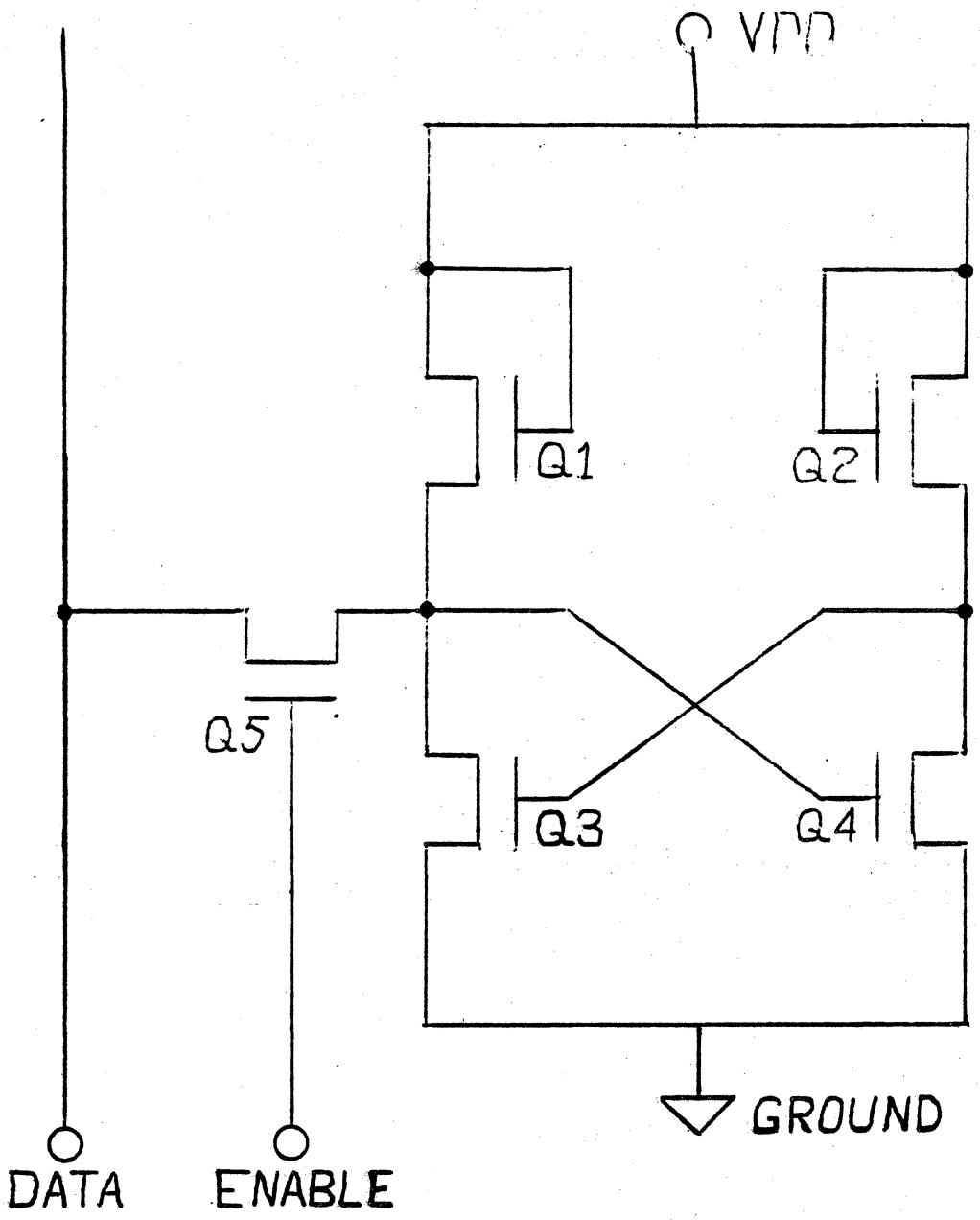
Early in the life of a device test program, an effort should be made to correlate results with each supplier. Through an exchange of documented rejects and analysis reports the potential for a better part exists. If the rejects are solely due to faulty test methods and the supplier points this out, then at least testing knowledge has been increased.

Using the techniques of reporting by exception, the cost of accumulating data on parts that experience low reject rates, low factory failure rates, and low field failure rates will remain minimal while providing information where it is needed.

Again, test equipment plays a major role. Whether or not this test equipment was used for familiarization, it must still be capable of massaging LSI with a natural environment. This requires sophisticated hardware. The system must also be capable of datalogging and providing some degree of parameter alteration. The basic qualities required are reliability, repeatability, diagnostic capability, and throughput speed. Results should be easily correlatable with engineering equipment.

At the present time, no good dedicated low cost LSI production test system exists. It is assumed by the above discussion that the final test program does not stand alone but exists in an environment of continuous monitoring that has been established on a corporate basis.

To summarize, an optimum final test plan is that plan which, in the shortest time possible, guarantees operating margin by the proper selection of test conditions. The techniques of familiarization and characterization have been shown to lead to the selection of these test conditions by establishing a firm data base. The monitoring process has been proven necessary to guarantee that these same conditions continue to be proper.



STATIC MEMORY CELL

FIGURE 1

2.0 SEMICONDUCTOR MEMORY TESTING

Robert Hickling
Fairchild Systems Technology
San Jose, California

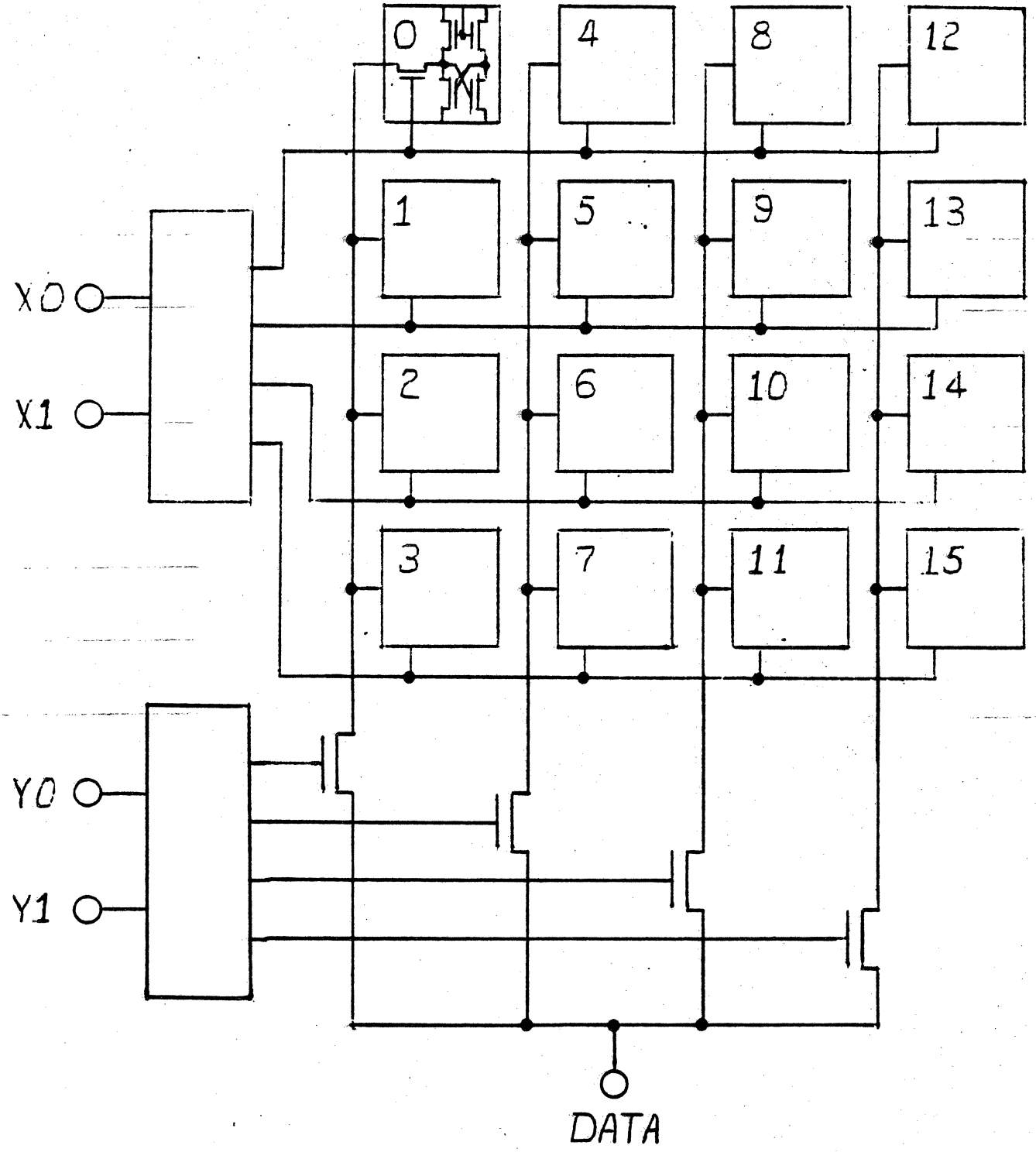
2.1 Random Access Memories

2.11 Device Organization

[redacted], let's cover the [redacted] of the random access memory, which is the [redacted] Flip-flops in integrated form have been around in one form or another for over ten years, but what is making them such a big thing recently is the collection of so many of them onto a single chip. To get some terminology straight, let's spend a little time on the flip-flop. Earlier memories were made exclusively of this sort of circuit; even now, all memories known as static memories use some variant of it. In Figure 1, notice that the flip-flop is basically a four transistor circuit. It is shown here with an extra transistor (Q5) on the left side which will allow selective access to it when it is buried in the middle of an array of such circuits. To trace the activity of the flip-flop as it performs its basic function of remembering a 1 and a 0, it must first be forced into a known state. The rules are that the only access to it are the data bus and the enable bus. If the enable line which turns on Q5 is raised, we can then force the data bus to the 1 state. It must be assumed that it is possible to drive the data bus hard enough to override Q3 if it should be turned on. In doing this, Q4 will be turned on; this in turn will pull the gate of Q3 low forcing it to be off; the flip-flop is now stable in what will be the 1 state. If Q5 is turned off, anything can be done on the data bus without affecting the state of the flip-flop. At any time the enable line can be raised to allow the flip-flop to drive the data bus. Thus, it can be determined if it was last driven to the 0 or the 1 state. Later, the enable line can be raised again and the data bus can be driven to the 0 state. This will turn Q4 off; Q4's pull up [redacted] will pull the gate of Q3 high leaving Q3 on. Now the flip-flop is stable in the 0 state and can be reaccessed at any later time observing that it was last driven to the 0 state.

That is the basic function of a flip-flop as it would be used in a random access memory. Selective access to it must be allowed and you must be able to either receive data from it or drive data into it. This is the basic element of a static memory device. A detailed discussion of the variety of storage mechanisms for dynamic memories will follow later. In dynamic devices, the storage and retrieval mechanism is similar, but there are fewer components required for each storage element.

To form a memory device, arrange a large number of these flip-flops in an array. Today devices with 4096 bits are common - with 16,384 bit devices coming and 65,536 bit devices on the drawing boards. The sheer size is part of what makes these devices difficult to test. The other part of the problem results from the lengths that circuit designers went to in cramming



MEMORY ARRAY STRUCTURE

FIGURE 2

so much into such a small space. This has resulted in a myriad of complex timing and waveform control required to use and test these devices.

For ease of explanation a fairly simple sixteen bit memory will serve as an example. The usual practice would be to arrange the flip-flops in a square array, so for these purposes the sixteen bits will be arranged in a 4x4 array, as in Figure 2. In addition, there is associated with each row a horizontal enable line attached to the gate of what corresponds to Q5 of the original flip-flop diagram. Also, the data bus nodes for each of the flip-flops of each column are tied together. In this arrangement, whenever an enable line is raised high, that row will drive the data bus so that the contents of that row is available at the bottom of the diagram. These enable lines are driven by a simple 1-of-4 decoder. Its nature is such that, with only two X address lines going onto the chip, the decoder will select one and only one of the four possible combinations of the two address lines and raise the appropriate enable line high. At the bottom is the Y address decoder. It is similar in nature to the X decoder, but its function is to select which of the four data buses is to be allowed at the final data output.

With this organization, consider the two X address lines and the two Y address lines to be a single four bit address. Counting in binary from zero to fifteen on this address bus will sequentially access each of the sixteen flip-flops in the order in which they are numbered in Figure 2.

This configuration allows unique access to each bit, but it would not be acceptable to allow the data bus to go directly to the outside world. The flip-flops themselves have very little drive capability, and the levels and drive capabilities required to write into them would not read very much like a TTL specification. In Figure 3 is a slightly expanded version of this memory with enough added peripheral circuitry to make it a usable device. In fact, this is very nearly the architecture of older static RAMs such as the 1101. The added features are a buffer for the data to be driven off the chip capable of driving at least one TTL load; a data input buffer to ensure that the device threshold is about 1.5 volts; a write enable input and a chip select. The function of the write enable input is to allow an external timing signal, usually called a write pulse, to determine when data input is to be driven onto the internal data bus. The function of the chip select is usually to allow several devices to have their outputs tied together to make a longer memory. If there were no chip select function, the two outputs could not be wire OR'd without causing them to fight each other.

In this example, data into the chip and data out from the chip are given separate pins. This is the usual case, but there are devices in which data in and out share the same pin. In this case, the data pin is said to be an input/output pin, or an I/O pin. The usual arrangement for this case is as shown in Figure 3. Whenever write enable is on, the output buffer is disabled. This is usually the case whether data is I/O or separate, because frequently in system applications the two will be tied together. The reason for keeping them separate is that in applications where they would not be tied together, use would be quite clumsy and extra circuitry would have to be added to separate the two functions. In addition, the job of testing is considerably easier when they are separate.

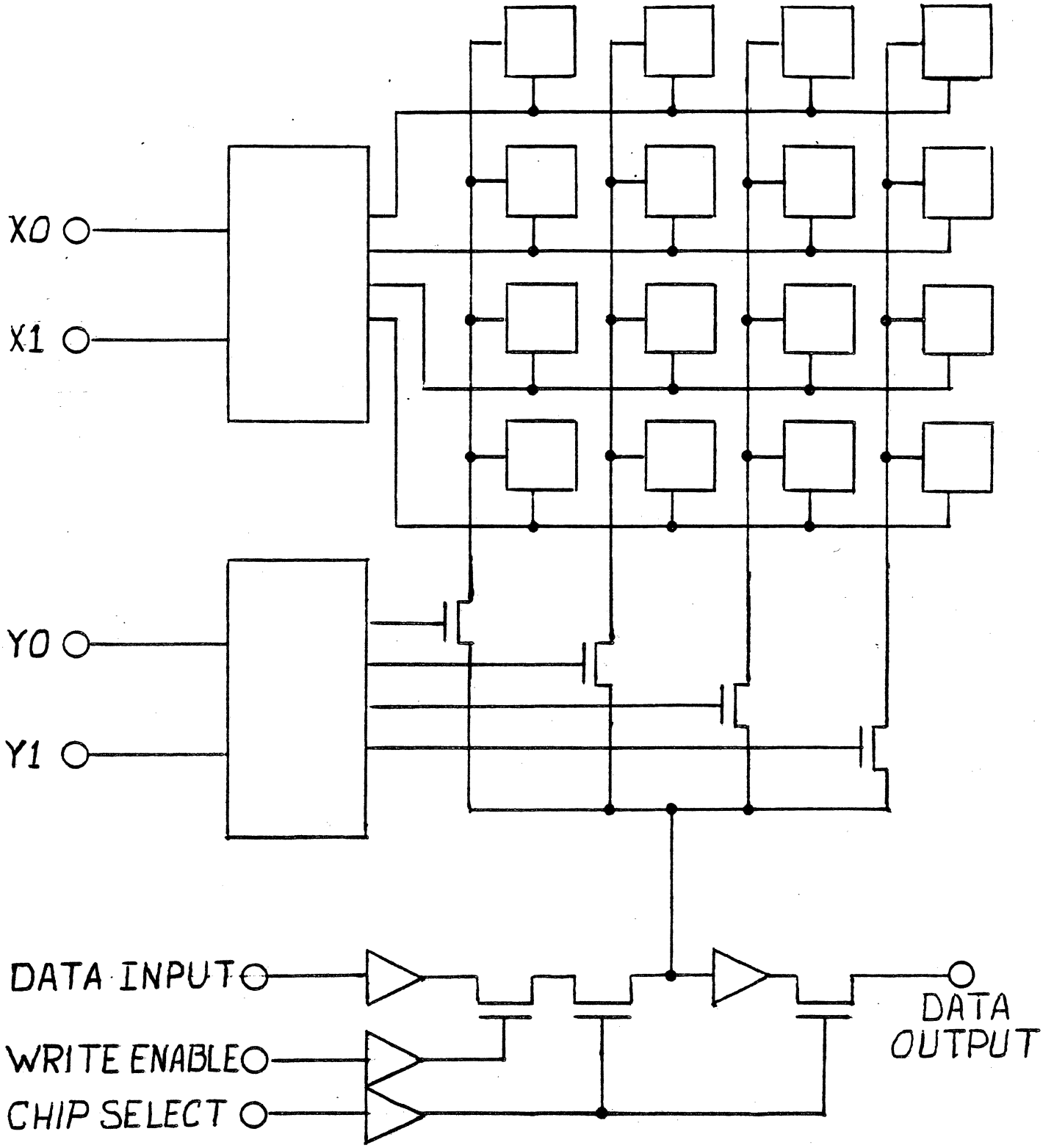
2.12 Testing Requirements

To determine what must be done to the memory before calling it tested, it would be helpful to start with a list of the elements of the circuit. The list would read as follows:

1. The flip-flop array
2. The X decoder
3. The Y decoder
4. The output buffer
5. The output buffer disabling circuit (chip select)
6. The input buffer
7. The input buffer disabling circuit (write enable)

The question is: What must be done to verify the integrity of each of these elements? Starting at the top of the list, a good first stab at verifying the sixteen bits of the memory might be to write 0's into all of them; read them out; write 1's and read them out. An obvious objection might be that all the components must work for this exercise to be performed successfully. That is largely true. At least the input buffer and its enable must work. The output buffer and its enable function must work too. But on closer inspection, it will be seen that it is entirely possible for the X and Y decoders to be stuck in one condition. Assume that they are both stuck at the 0 address. What was done was the writing of a 0 into bit 0 sixteen times and then that same 0 was read back sixteen times. The same holds for the 1, obviously. However, assuming that the decoders are working, what has been determined? It is known that the data input buffer works, the data output buffer works and none of the bits are stuck in the 0 or the 1 state. It has also been verified that there is an absence of what I call horizontal shorts. There are four basic ways that a short in the array of bits will cause a malfunction. There may be a short to ground or VDD causing an apparently stuck bit, or there may be a short from one bit to its adjacent neighbor. If the short is from the right side of bit 0 to the left side of bit 4, that would be a short from the data barred side of bit 0 to the data side of bit 4. Depending on which is stronger, one of the bits will take on the opposite state of the other. In similar fashion, the opposite sort of short would be a vertical short from the right side of bit 0 to the right side of bit 1. Now, depending on which of the two is stronger, one will take on the same state as the other. So, under the assumption that the decoders are functional, the solid 0's and solid 1's pattern has verified the input buffer, the output buffer and the absence of three of the four types of shorts in the array.

The next logical thing to do is to eliminate the possibility of vertical shorts. The description of this malfunction is that adjacent bits will not maintain opposite states, so we must devise a pattern in which all



BASIC RAM

FIGURE 3

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

SOLID 0'S

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

SOLID 1'S

0	1	0	1
1	0	1	0
0	1	0	1
1	0	1	0

CHECKERBOARD

1	0	1	0
0	1	0	1
1	0	1	0
0	1	0	1

INVERTED CHECKERBOARD

1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

DIAGONAL STRIPE

N TYPE PATTERNS

FIGURE 4

adjacent bits have opposite data. In Figure 4, notice the checkerboard pattern accomplishes just that. If the checkerboard is written into the memory and read out and the inverted checkerboard is written in and then read out, all the various forms of hard shorts which may be lurking in the flip-flop array have been weeded out. One additional fact has been established by the checkerboard: for it to work successfully, the X and Y decoders must both be capable of switching between at least two locations. However, that is all that is verified. Since each group of four bits is identical to all other groups of four bits, a memory of any size can pass the checkerboard pattern if the X and Y decoders will switch between at least two locations.

The next obvious thing to do is attack the decoders. A pattern is needed which will verify that there are, in fact, four unique X positions and four unique Y positions. At the bottom of Figure 4, notice a pattern called the diagonal stripe which is intended for just this purpose. Observe that if the Y decoder is set at column 0, then counting from 0 to 3 on the X decoder will produce a single 1 from X position 0 and a 0 from all other X positions. This ensures that when attempting to access bit 0 you do access bit 0, and with anything but 0 on the X decoder inputs you do not access bit 0. If the Y address is then changed to the second column, you verify the same facts about X position 1. Continuing this process for the remaining columns, it has been verified that there are the correct number of rows in the memory and, hence, the X decoder works. Now all that must be done is to repeat this exercise for the Y decoder, right? Wrong. It is already done. Nothing more will be learned by reading this pattern out again, holding the X decoder fixed while counting on the Y decoder. It might make the explanation of Y decoder integrity easier, but it would not find any additional faults.

The only item left on the list of components to be tested is the chip select. It has two functions and, therefore, will require two different exercises. First, let's attack the function of not writing into the memory when the chip is de-selected. No new patterns are required for this, simply some reuse of what we already have. The solid pattern is quite adequate. Write the memory full of 0's, attempt to write the memory full of 1's with the chip de-selected and read back the fact that the memory is full of 0's. For peace of mind, this may be repeated with inverted data. The other chip select function of disabling the output buffer is usually not a matter of pattern. It is most often tested with some sort of precision measurement unit capable of forcing a voltage and measuring the resulting current. The procedure is usually to attempt to read out a 0, de-select the chip, force a 1 voltage value and measure the leakage of the turned off output transistor. Then, repeat the procedure, reading out a 1 and forcing a 0 voltage.

At this point, all the components of the memory have seemingly been tested and you might be tempted to quit. But this has been too simple and memory testing is supposed to be hard. Product and test engineers seem to be adept at coming up with test sequences which can take a whole minute to run on large RAMs like the 4096 bit variety. That equates to about 120 million cycles at a typical cycle time of 500 nanoseconds. Those test times result from the famous N^2 patterns (or infamous, if you are of a production bent). Before leaving the simple patterns, I wish to spend a minute tooting their respective horns. The complex patterns are good for their intended purposes,

pattern making $2N^2$. What do these numbers mean in terms of total test time? For our sixteen bit device, $2N^2=512$. For a memory with a 500 nanosecond cycle time, this translates to 250 microseconds. That is hardly worth talking about, but when $2N^2$ is applied to a 4096 bit device the number of cycles is 33,554,432 which translates to 16.6 seconds. If the pattern is repeated with inverted data, and then all that is repeated at maximum and minimum voltage, the test time has easily exceeded one minute without doing any other testing. Therein lies the hideous truth about N^2 patterns. Each time the size of the memory is doubled, the test time is multiplied by four. Unfortunately, memory sizes don't double -- they quadruple. Each new generation of larger and larger memories takes sixteen times as long to test as its predecessor. If PingPong should be required on a 16K memory with a 500 nanosecond cycle, it will take about 270 seconds. A 65K memory will take about 4300 seconds, or 71 minutes.

Did someone say there must be a better way? Yes, there are alternatives. They involve compromise, but the skeptic keeps forgetting his questions before the tester can give him the answers if he doesn't compromise. This is the predicament which has led us to a search for shorter patterns which will accomplish nearly the same results as the N^2 patterns. The primary category of interest at this point is called the $N^{3/2}$ family of patterns. One of the most straight-forward examples of this type is called the Walking Row Bar. The name describes it well. Instead of putting a single odd bit into the memory, we place a single odd row into the memory. In other words, begin by filling the memory full of 0's; write all of X row 0 with 1's; then perform either a modified PingPong or straight sequential read out of the entire contents of the memory. Repeat this process consecutively, moving the odd row down one position at a time until it has occupied each of the row positions. A thorough checkout of the X axis decoder has now been completed. If this pattern is coupled with its logical counterpart, called the Walking Column Bar, you can have nearly as much confidence in the integrity of the memory as with the N^2 patterns. The total number of cycles required is remarkably improved. In the sixteen bit example, this would take four readings of the sixteen bits. Four, in this case, is not one-fourth of sixteen, but rather the square root of sixteen. Thus, you have N times the square root of N as the number of cycles required, which equals $N^{3/2}$: hence, the name of this category of patterns.

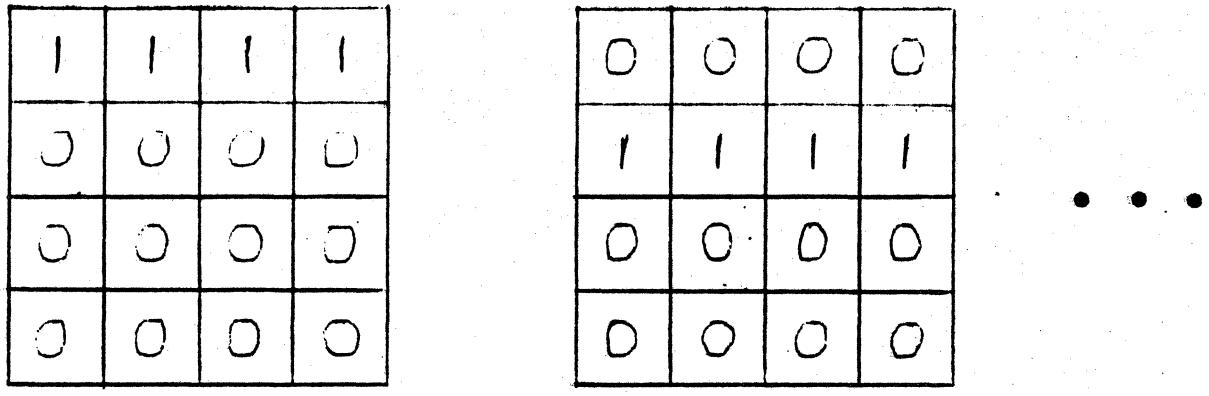
Another follow-on to this scheme of things would be the sliding diagonal, which is a variation of the diagonal stripe data pattern described earlier. Beginning with a diagonal stripe as the data pattern, proceed to slide the diagonal one position at a time. It doesn't matter whether you slide it to the left, right, up or down as long as it is moved one position at a time. Looking back at Figure 4, start with the original diagonal stripe in the memory and read it out and then slide the diagonal down one position. It is obvious that the bottom row will fall off the end of the memory, but you must assume that the memory is circular in that dimension so that the row which fell off the bottom reappears at the top. Continue the sliding process until the diagonal has occupied all of the possible positions.

Another pattern which is a little more elegant is called the Butterfly and it works in a very similar fashion to the Galloping pattern. In the Butterfly, a single odd bit will occupy every location, but instead of reading

but it is important to learn all that can be learned from the simple patterns. Their simplicity and their speed are their primary virtues. On completion of the exercises described thus far, there is a very high probability that there is nothing wrong with the device. If a failure occurs in a simple pattern, the nature of the failure is difficult to misinterpret. The name usually ascribed to this family is "the simple N type patterns". The origin of this name stems from the fact that the performance of the pattern on a memory of N bits requires 2N cycles. As in the aforementioned example, where N is sixteen, any of the N type patterns would require sixteen cycles to write the pattern in and sixteen cycles to read it back out.

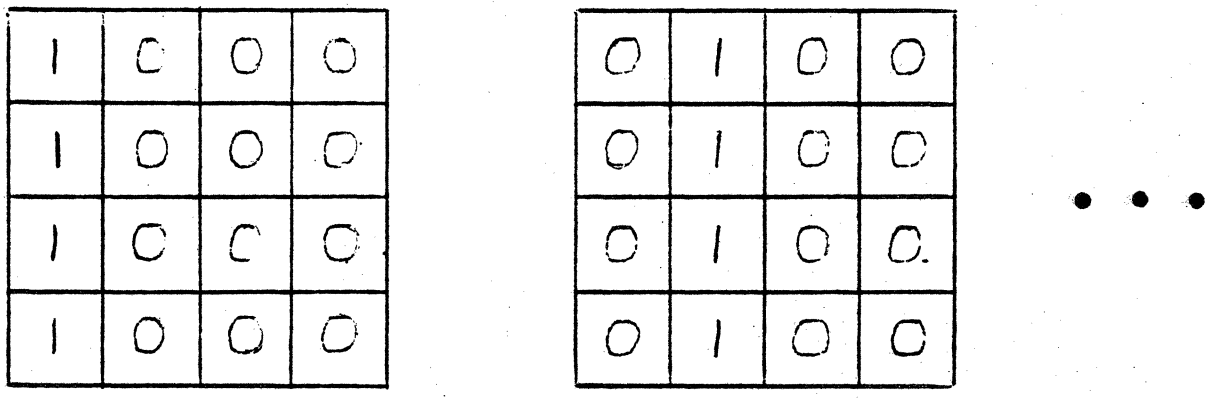
So what types of defects or weaknesses can be found with these N^2 patterns, and how is such an exercise constructed. After a few bad experiences with customer returns and the inherent skepticism of high reliability people, one might be persuaded to verify with more certainty that each of the bits is present and does not interact with nearby bits. Since the [redacted] stripe seemed to be geared toward uniqueness of addresses, let's pick up on the logic of that pattern. Recall that after reading out column 0 it seemed evident that in column 0 bit 0 was completely unique. The only other place any 1's could have come from would be some other column. So, instead of writing a diagonal stripe into the memory, let's stop with a single 1 in the bit 0 position and fill the rest of the memory with 0's. Now if the entire memory is read out and no other 1's are found, the absolute uniqueness of bit 0 can no longer be questioned. Now move the odd bit to address 1 and read out the entire memory. The occurrence of a single 1 at address 1, and 0's at all other locations, verifies the absolute uniqueness of bit 1. This process may be continued until the odd bit has occupied all N bits, at which time it is certain that this is an N bit memory. It is also clear that all N bits have been read N times and, therefore, the basic N^2 pattern has been created. This is quite reasonably called the walking 1 pattern, where a single 1 has essentially been walked through a field of 0's.

What else might the skeptic choose to find incomplete in the set of exercises performed? So far, it has been sufficient to count sequentially through the addresses of the memory, and that is not very typical of real device usage. Besides, these are called random access memories and you should be able to skip from any address to any other address. It is a well-known fact that some address transitions are slower than others and if the access time is to be guaranteed, you must test all address transitions. With a little clever thought about what was described for the walking 1 pattern, a method can be seen for doing just that. While the odd bit is at location 0, rather than simply reading back the entire memory contents, alternately read bit 0 and then the next bit from the remainder of the memory. An address transition from every address to address 0 will then have been performed. What's more, you have observed a transition of data from 0 to 1 in going from everywhere to address 0. If any bit other than the odd bit contains a 1, a transition from bit 0 to that bit and back would leave the output in the 1 state and it would be unknown if that was a slow address transition or not. Therefore, the walking data pattern combined with this particular addressing sequence is about the only way of verifying the worst case access time for all possible address transitions. This addressing sequence with the walking data sequence is known as the Galloping 1 or the PingPong pattern. In counting cycles, this pattern is exactly twice the length of the Walking 1



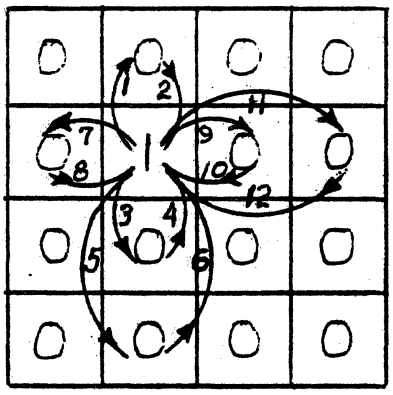
1ST PASS 2ND PASS

WALKING ROW BAR



1ST PASS 2ND PASS

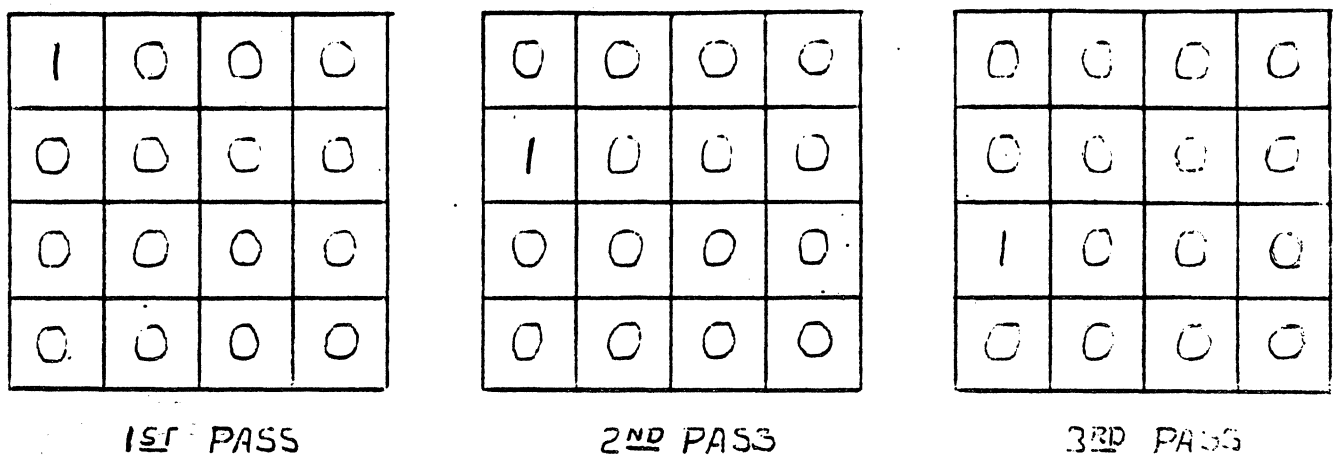
WALKING COLUMN BAR



6TH PASS OF BUTTERFLY

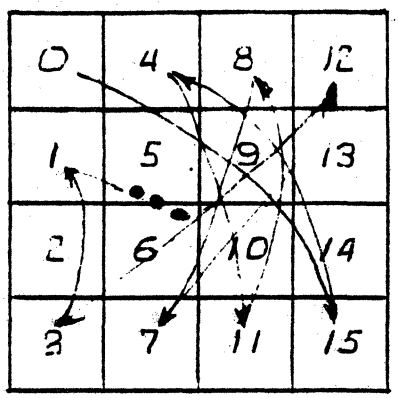
$N^{3/2}$ PATTERNS

FIGURE 6

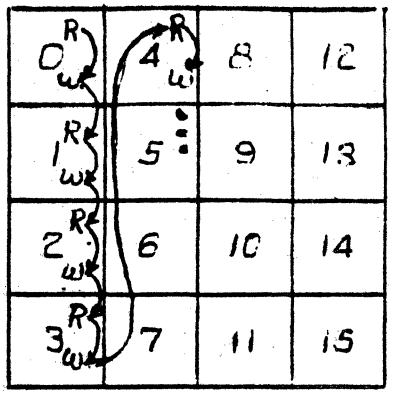


WALKING 1 SEQUENCE

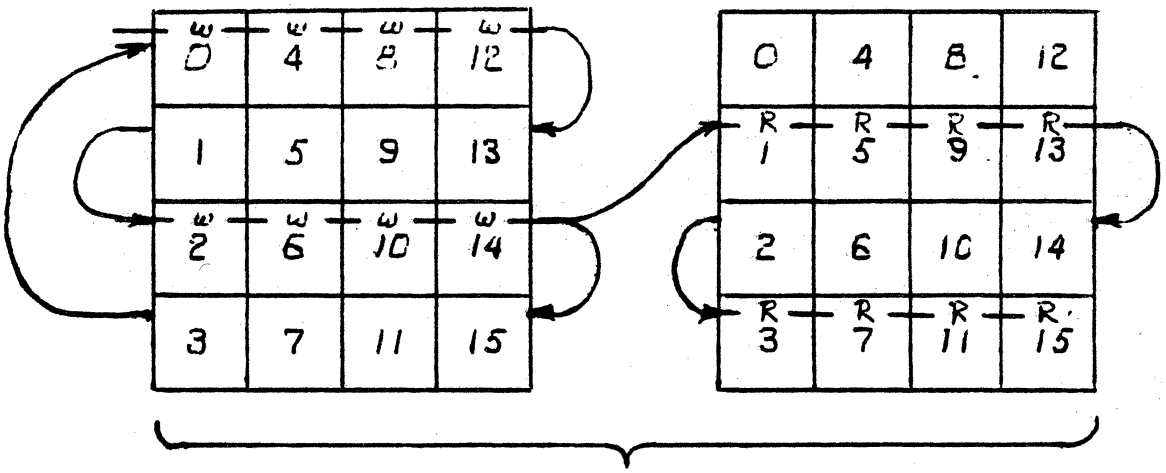
FIGURE 5



ADDRESS COMPLEMENT



READ-MODIFY-WRITE



ROW DISTURB

FIGURE 7

the entire memory for each position of the odd bit, only the row and column of the odd bit will be read. Beginning with the odd bit in the bit 0 position, the addressing sequence would be 0, 1, 0, 2, 0, 3. That completes the X axis; then read 0, 4, 0, 8, 0, 12. Move the odd bit to position 1, and continue with the sequence 1, 0, 1, 2, 1, 3, 1, 5, 1, 9, 1, 13. If this sequence is continued to the end, you will have performed something which looks a great deal like PingPong in only $2N^{3/2}$ cycles. In Figure 6 the sequence of reading is shown pictorially for bit position 5. It is this perspective which gives the pattern its name.

There are some variations on N type patterns which emulate various parts of N^2 patterns. One of the common things which is seen from time to time is the address complement sequence. In order to keep a maximum of activity on the address decoders, you can alternately go from the top to the bottom working your way toward the center rather than going from 0 to N in a sequential fashion. In the sixteen bit case, the sequence would be 0, 15, 1, 14, 2, 13, etc., finally ending in 6, 9, 7, 8. The result is a complete inversion of the address field almost every step of the way. This is an attempt to reproduce the worst cycles from the PingPong pattern. The assumption is that the slowest address transitions are those with lots of address lines changing at the same time. This is a simple technique and, in fact, experimental results show that this almost always gives a slower value for access time that a straight sequential addressing scheme.

Another variation which is quite interesting is one which makes the solid 1's and 0's pattern a much more powerful tool. It is called the read-modify-write sequence. Most data sheets specify a completely different set of timing for the situation where a bit can be read out and written back into memory in the same cycle. It is possible to take advantage of an added diagnostic capability of this sequence by simple alternate interleaving of read and write cycles. For this sequence, instead of writing the entire memory and then reading it back, a read cycle is followed by a write cycle on each cell. With the memory full of 0's, read the 0 from bit 0; write it to a 1; move to bit 1; read a 0; write a 1; move to bit 2; read a 0; write a 1; etc. If the writing of a 1 into any bit were to disturb any of the bits which are to be tested after it, the error would be detected when that bit was reached in the ascending address pass. For example, if when a 1 is written into bit 3 it upsets bit 7 and changes it to a 1, the read 0 test will fail on bit 7. It is also possible for a "backward disturbance" to occur. Suppose that writing a 1 into bit 3 causes a disturbance, such that the 1 just written into bit 2 is destroyed. Since a single pass of read-modify-write does not return to bit 2, this error would go undetected. For that reason, the original read-modify-write sequence is not effective unless immediately followed by a read-modify-write 1's to 0's and then all of that must be repeated with descending addresses. On completion of all that, you will have caught all combinations of forward and backward disturbances which are sensitive to read-modify-write.

So far, everything I have talked about is applicable to almost any random access memory, I would like to discuss dynamic memories and some test patterns that are uniquely associated with them. First, what makes up a dynamic memory as opposed to a static memory? Notice the first appendix, which is a copy of an application note on the family of 4096 bit

on the capacitor of Figure D, Q1 is turned on. When this bit is read out it will be 0. The reading sequence will be to precharge the data bus to a 1; enable Q2; Q1 will discharge the data bus; disable Q2; the 0 state of the data bus must be latched, inverted and driven back down the data bus; enable Q3 and reinforce the original 1 on the capacitor.

That may be logical and breathtaking, but somebody thought it was a waste of time to have to recharge the data bus for the reinforcement phase of that sequence, so the idea came about to allow the data to be inverted. Instead of inverting the 0 that was sensed, reinforce the 0 that is already on the data bus. Remember that this is happening to all 64 bits of the selected row, even though only one is seen as data out. The problem is: How do you know if what is in a row is true or inverted data? For that problem, a 65th column, called the status column, is added to each row whose only purpose in life is to remember if the row has been inverted an even or odd number of times. Data onto or out from the chip gets exclusive OR'd with its row "status bit" so that this inversion process is transparent to the user. That was nice for the user, but woe be unto the test engineer. Most designs of this type include no provisions for initialization of the status bit. I have gone to all this trouble to define distinctive data patterns which tell something, and now it is unknown whether the 1 just written was stored as a 1 or a 0. All that is known is that it will be a 1 again by the time it comes back out. Well, it's not really all that bad. If each pattern and its complement are performed, coupled with a few variations, the desired effect can be accomplished. Remember that inversion will always occur on a whole row at a time. If you are particularly concerned about a checkerboard, the worst possible case would be that all even rows are inverted and odd rows are not. That would turn the checkerboard into vertical stripes. An easy solution would be to write a pattern of vertical stripes which would appear in the array as a checkerboard. Since it is impossible to determine which, if any, of the rows are inverted, the test plan for this device should include both checkerboards and vertical stripes. This is an example of how important it is to become familiar with the internal working of a memory before establishing the final sequence of patterns to be used in an efficient high-quality test plan. It also points out the need from time to time to develop special patterns geared to a special problem which may only occur in a particular memory.

Finally and fortunately, notice Figure E which is the one transistor cell. It is popular primarily because it is small and non-inverting. It is only a capacitor and an enable transistor. With that kind of simplicity, chip size goes down and yield goes up. How can anything be that good?

One disadvantage is that this cell has no transistor to buffer the capacitor. The capacitor itself has to move the data bus and that tends to make it more sensitive in the areas of noise and refresh time. Refresh time is the length of time that the storage capacitor will hold its charge before the level degrades to an unusable level. In the description above, notice that the reading of any bit in a row will refresh the entire row. It is easy to imagine a situation in the real world where one section of the memory gets used repeatedly and the remainder is unexercised for a

memories. On page 4 is a variety of the kinds of dynamic cells. It should be reasonably apparent from this, why they are called dynamic memories. The basic difference is that they do not have a static flip-flop as originally described. Notice in the upper left-hand cornor, a drawing similar to that which was discussed initially. The only difference here being that they have shown both a data and a data bar line and an extra transistor to enable access to both sides of the flip-flop. The reason for having both data and data bar is for speed. Start with the flip-flop in the 0 state. Q2 is on and Q3 is off, so that Q1 would enable a 0 onto the data bus and Q4 would enable a 1 onto the data bar bus. To invert the data in that cell with only the data line to do that job, Q2 must be overridden. To supply enough current to overwhelm Q2 and drive all the capacitance of the data bus would make a slow cell. If, at the same time, it is possible to pull down on the data bar line, you only have to overpower the pull-up resistor on the right side and that would then turn off Q2 and allow the raising of the data line to happen more quickly.

Looking at Figure B on the same page, notice the four transistor dynamic cell which is extremely similar in nature to the original static flip-flop -- with the exception that the pull-up resistors are gone. The whole basis behind dynamic cells is that they do not have any form of pull-up resistors. They rely on stray capacitance on the gates of the storage transistors to hold a charge. Here you see them noted as C1 and C2, such that when we write data into this circuit, C1 will hold the gate of Q2 in one state, and C2 will hold the gate of Q3 in the opposite state. That will work for a period of time, but there are elements in the circuit which will eventually bleed the charge from these capacitors.

They are very small capacitors, typically of the order of a few hundred femtofarads. Typically these capacitors are guaranteed to maintain their charge for only about two milliseconds. This circuit looks very similar to our original static arrangement, but the three transistor cell in Figure C on that page shows a different concept. In essence, the entirety of the memory function is performed by Q2. Writing into the bit is accomplished by turning on Q1 and driving the data into capacitor C1. Data is read out from the memory by precharging the read data bus to the 1 state and turning on Q3. Depending on the state of the gate, the bus either will or will not be discharged by Q2. This structure has the disadvantage of requiring four buses, which significantly complicates the layout of the memory. Notice that in the original static cell a data and data barred bus were required to run vertically across the chip, with a single row select running horizontally. The same busing arrangement was required for the four transistor dynamic cell. This form requires four buses because of separate read data and write data lines. In the three transistor cell of Figure D, there is essentially the same configuration except that the read and write data buses have been combined. The advantage of the four bus configuration of Figure C is speed, because the data lines have less capacitance. Notice that each data bus touches only one transistor in each cell. In Figure D, the single data line is connected to both select transistors Q2 and Q3 making heavier capacitive loading and, therefore, a cell which is not quite so fast. There is an interesting aspect of the three transistor cells which makes them different from all the others, and that is that they are inverting cells. Observe that if a 1 is stored

for those days, you decide to build a black (or usually gray) box. In Figure 8 is the diagram for such a box. First, it has a pair of free-running one shots to provide a master clock. They, in turn, drive a four bit counter which will allow you to count through the RAMs addresses. The overflow from that counter drives another counter which will be the sequence control. Obviously, alternate passes through the memory will be write, read, write, read, etc.; so, the first bit of the sequence controller will handle the inversion of the data by feeding one side of an exclusive or gate through which data must pass enroute to the MUT (memory under test). Finally, you must sequence through the three patterns so that the last two bits will perform the job of pattern selection. You also need a few more one shots to make a write pulse and a data output strobe. Now for the hard part; how are the data patterns to be generated? Solid 0's is easy with a short to ground. Solid 1's happen automatically because that is only inverted solid 0's. How about checkerboard? A little close inspection will show that the exclusive or of X0 and Y0 produce a checkerboard. The diagonal stripe is more difficult. It could be described as producing a 1 whenever the X address is equal to the Y address. If you exclusive or X0 with Y0 (likewise with X1 and Y1), and require that these both be false at once with an or gate, you have what is needed. There is a fourth possibility for the pattern selector, but for now just ground it and call it room for expansion.

To provide some means of informing the operator whether the MUT passed or failed, exclusive or what comes out of the MUT with what went in. It is possible to capture the occurrence of an error in a D-type flip-flop which get clocked after a delay, allowing for the MUT's access time, which then turns on a LED marked "fail". With a little more control logic for the start button, you have a basic operational memory tester. Believe it or not, a lot of memories in this world have been shipped with no more functional testing than that. And wasn't it clever of you to leave an available port for an additional pattern if anybody should require one? If only you had known. If the original circuit was not placed in an expandable nineteen inch rack, it would soon be scrapped because addition of the "Gee, but if"'s soon turned the original clean little circuit into a hopeless patchwork of modifications.

Within two or three years, the first of the programmable memory pattern generators appeared. For all practical purposes these can only be called special purpose computers. Macrodata was the first major test equipment vendor to produce such a module. Since then, virtually everyone has some sort of memory pattern generator available. All of these generators have a number of qualities in common. They have a main memory in which a program may be stored. Each word of the program contains instructions for the various major sections which would be segmented, as shown in Figure 9. The first major block controls generation of the address sequence; second, is control of data; third, is control of special functions of the MUT -- such as read, write and chip select; last, is control of which program instruction to perform next.

Address control sections can usually perform such activities as:

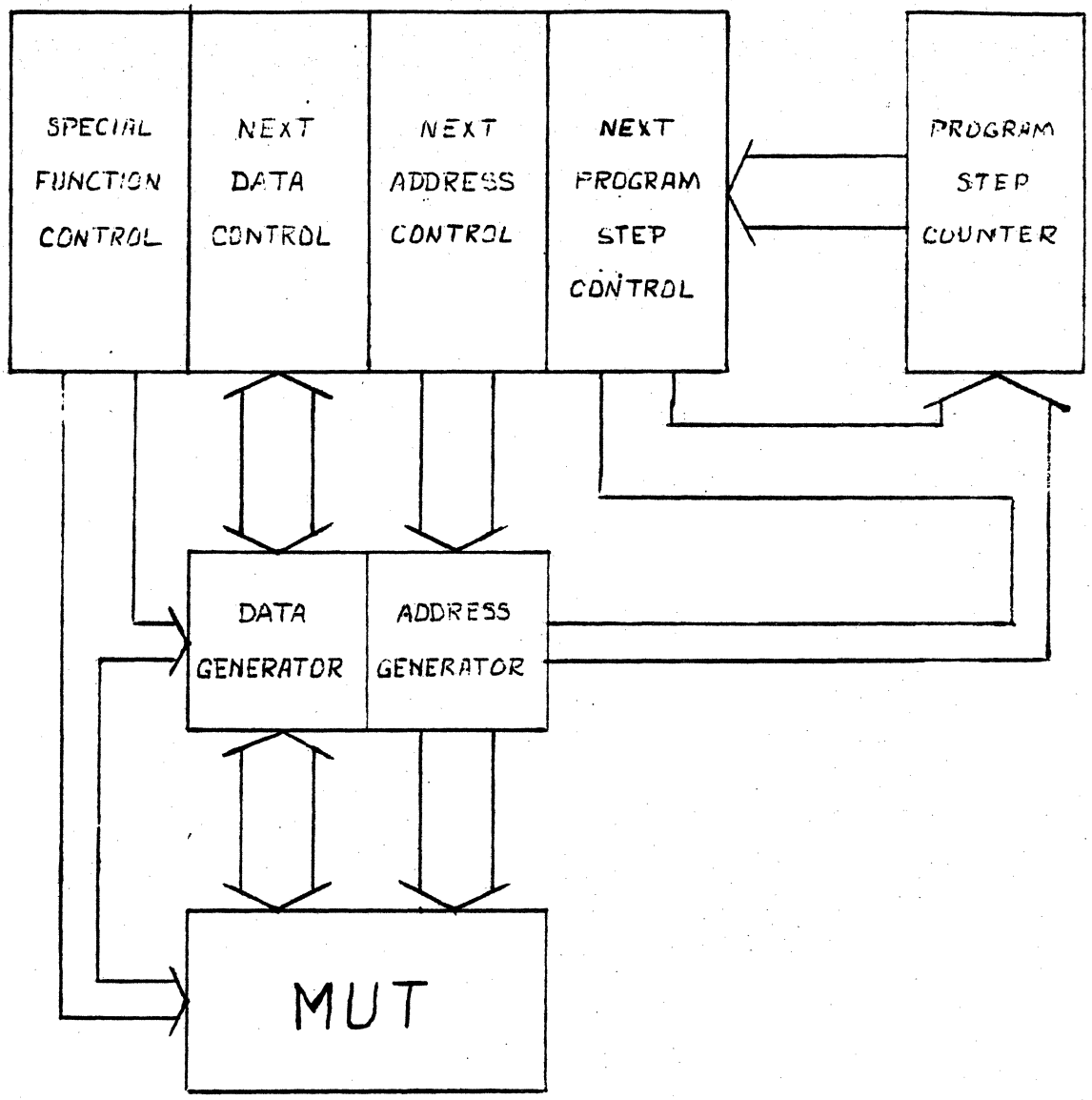
long period of time. The question is, how long can this go on? The answer on most data sheets is two milliseconds. That value is the guaranteed time for the whole temperature range, which is usually 0°C to 75°C. In fact, the refresh problem is most severe at the 75° end of the range. A general rule of thumb is that the refresh time will be cut in half for every 12.5°C that the temperature rises. That is because a diode to the device substrate is the discharge mechanism and the rule of thumb describes the temperature dependence of reverse biased diode leakage. Extending these numbers a little says that if a part is marginal at 75°C with a 2 mS refresh time, the room temperature value will be about 32mS and the 0°C value will be about 128mS.

What is the test for refresh time? There are two basic ways. The first is what I call passive refresh. For a passive refresh test, simply fill the device with a data pattern, wait for the refresh interval and then read the pattern back to verify that all is well. In general, discharge of the storage capacitors will only go from 1 to 0, so it may be sufficient to store solid 1's for this activity. If it is not certain whether a 1 at the outside world ends up as a high or low on the capacitor, the process must be repeated with solid 0's. The other form of refresh is what I call active refresh. The skeptic may well argue that activity in a row adjacent to an inactive row will create noise which will aid in the discharge of the inactive row. In active refresh, write the memory full of 1's and then alternately write 1's and 0's into the even-numbered rows. When the refresh interval has expired, return to the odd-numbered rows and see if any bits were dropped. This is then repeated, hammering on the odd rows and leaving the even rows undisturbed. An unfortunate circumstance in 4096 bit RAMs is that with a 500 nanosecond cycle, a writing of all bits takes two milliseconds. This leaves no time for even- or odd-row hammering at 75°C. Therefore, the memory must be exercised in segments of perhaps eight or sixteen rows at a time. For the worst case, one could write row 1; hammer rows 0 and 3 for two milliseconds; read row 1; hammer rows 1 and 3 for two milliseconds; read row 2; etc. This would check the refresh time of each row one at a time with a maximum of adjacent disturbance. Another name for this activity is row disturb.

2.13 Tester Requirements

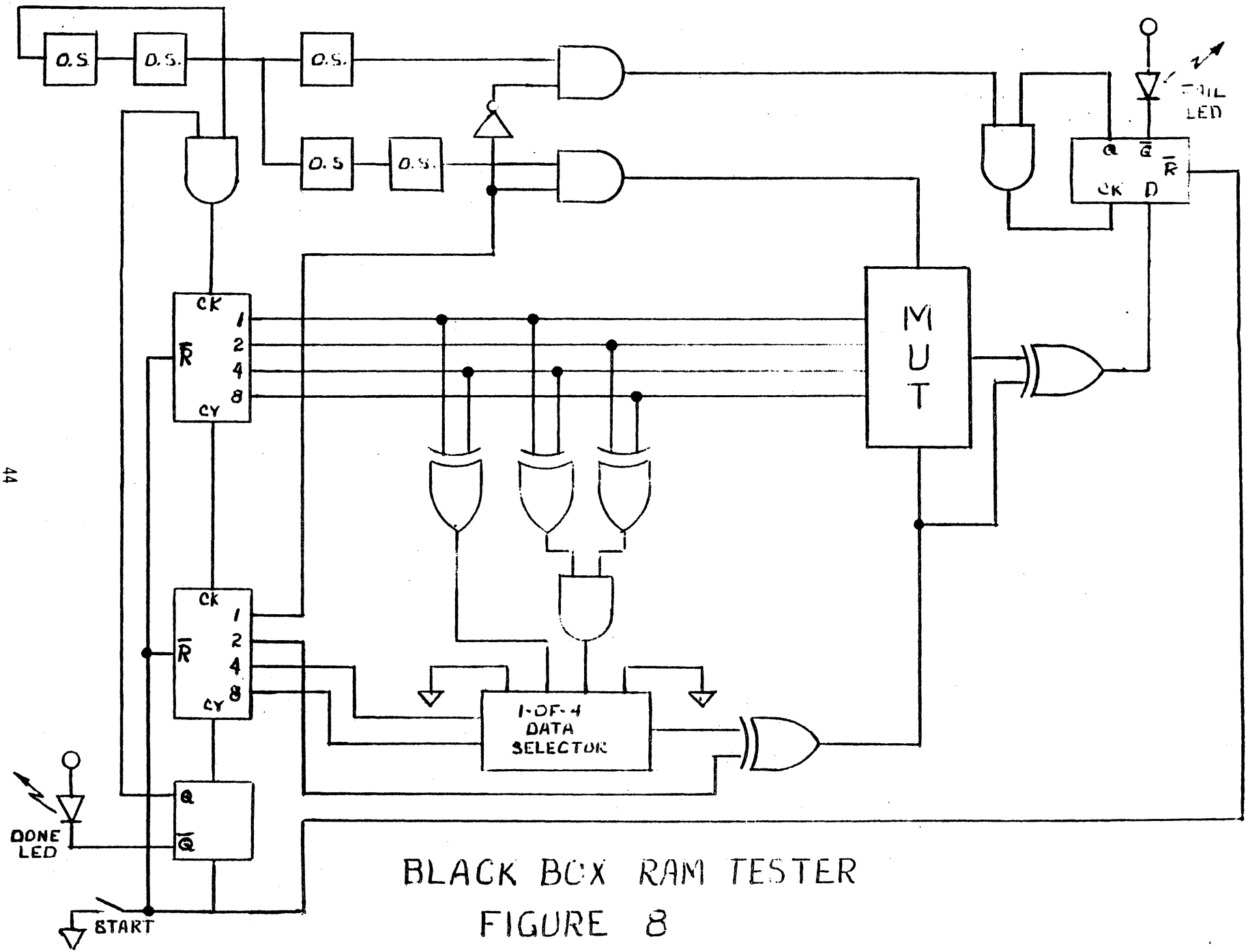
At this time, it would be valuable to spend some time discussing the hardware required to perform all these patterns. Assuming that all aspects including timing and analog levels are important, the machinery is not simple. A lot of time could be spend discussing programmable timing generators, drivers and comparators, but suffice it to say that they are important if a thorough job is to be done. For now, I will confine the discussion to the hardware required to generate the data and address sequences previously discussed.

It may be helpful to approach pattern generators from an historical point of view. Suppose that it is 1967 and there is a brand new device which is a sixteen bit RAM. Your job is to test it. The product engineers have explained that they want to perform solid 0's, solid 1's, checkerboard, inverted checkerboard, diagonal and inverted diagonal. In true fashion



MEMORY TESTER BLOCK DIAGRAM

FIGURE 9



BLACK BOX RAM TESTER

FIGURE 8

Almost all pattern generators alive today can do all the patterns described earlier. The differences are usually traceable to what the vogue pattern was at the time it was designed. Some were designed to be very easy to use and are, therefore, very inflexible. The patterns we discussed here may be the end of their capability. Others were designed with the intent of maximum flexibility and are much more difficult to use. The simplicity-flexibility product is a universal phenomenon like the speed-power product. A measure of the sophistication of a pattern generator must take both qualities into account. Ease of programming and ability to generate patterns not yet thought of are not as easy to measure as watts and seconds, but both should be considered. The complexity of the job and the fast cycle times of bipolar RAMs have dictated that pattern generators be constructed of ECL logic. Most are capable of running in the ten to twenty MHz range.

2.2 Read Only Memories

2.21 Device Organization

Read only memories are very similar in basic layout to RAMs. The basic difference being that data cannot be written into them in normal usage. The flip-flop array is replaced by an array of shorts to an enable line via diodes. The earliest variety was the mask programmable ROM. In this type, the writing of data is accomplished by sending the truth table to the vendor. The vendor will have a special mask made so that the appropriate shorts are made during the wafer fabrication process. This is a very expensive initial investment of approximately $10,000. However, subsequent copies have the cheapest cost per bit to be found in semiconductor memories. The rules are to be sure the truth table is right the first time, and be sure the pattern will be used in high volume. In Figure 10 is a diagram showing the basic structure of a ROM. Evident there, is the same form as in the RAM, with horizontal row selects associated with an X address decoder and vertical data lines which feed into a Y address data selector. The main difference is that the writing circuitry is absent and the flip-flop array has degenerated to a set of present or not present diodes. These are sometimes known as half transistor cells. Here, if an enable line is high, its associated diodes are reverse biased and it has no effect on the data buses. The X decoder's job is to pull one, and only one, enable line low. Observe that if enable line 0 is pulled low, there is a diode from it to all eight data buses and they will, therefore, all be pulled to ground. If enable line 1 is pulled low, there are no diodes between it and the data lines; so the pull-up resistors at the top of the diagram will pull all the data lines high. Another difference indicated here is that the Y decoder is not a 1-of-8 data selector; it is four 1-of-2 data selectors. This ROM has sixty-four bits organized as 8 x 8 in its array, but there are only four address lines, allowing only sixteen addresses. For any given address, the results from four of the sixty-four bits will be seen at the four data output pins. Its organization would be described as 16 x 4. Having more than one output is typical of ROMs; most have between four and ten outputs. RAMs usually have either one or four.

1. Increment the address

2. Decrement the address

3. Add a constant to the address

4. Select one or more alternate addresses

5. Invert the address

Data generators vary from one vendor to another, considerably more so than address generators. Some treat data exactly the same as addresses, such that the data is a result of a sequential computation. Others derive the data from some logical relation of various bits of the current address. Following are some typical address to data relationships:

1. Data = 1 if $X0 \oplus Y0 = 1$

2. Data = 1 if X = Y

3. Data = 1 if address = alternate address

4. Data = Y0

5. Data = X0

6. Data = any of the above, inverted

Special function control performs such activities as enabling read pulses, write pulses, one or more chip selects and control of whether or not a go-no go decision is to be made.

Program sequence control sections can usually perform a wide variety of functions which are typical of computer branch instructions. The following are common activites:

1. Branch if address = 0

2. Branch if address = maximum

3. Branch if address = alternate address

4. Call a subroutine

5. Return from a subroutine

6. Branch if refresh timer has expired

7. Branch unconditional

Programmable ROMs are of two basic varieties. The earlier types were of the bipolar technology. They are made with all the diodes intact and connected to their enable lines by a fusable link, usually a nickel chromium alloy. The scheme was to have a special set of circuitry capable of handling heavy currents (100-200 mA) which circumvented the normal output buffers. By selecting a bit and driving sufficient current into the output pin, the link can be melted to create an open circuit. This also implies a healthier-than-normal X decoder, because it will have to handle this excessive programming current.

One big advantage of the programmable ROM is, that for the price of only a single unit, a truth table can be programmed and tried. Another attractive quality is that if twenty copies of ten different patterns are required, it is not necessary to pay $100,000 in tooling charges.

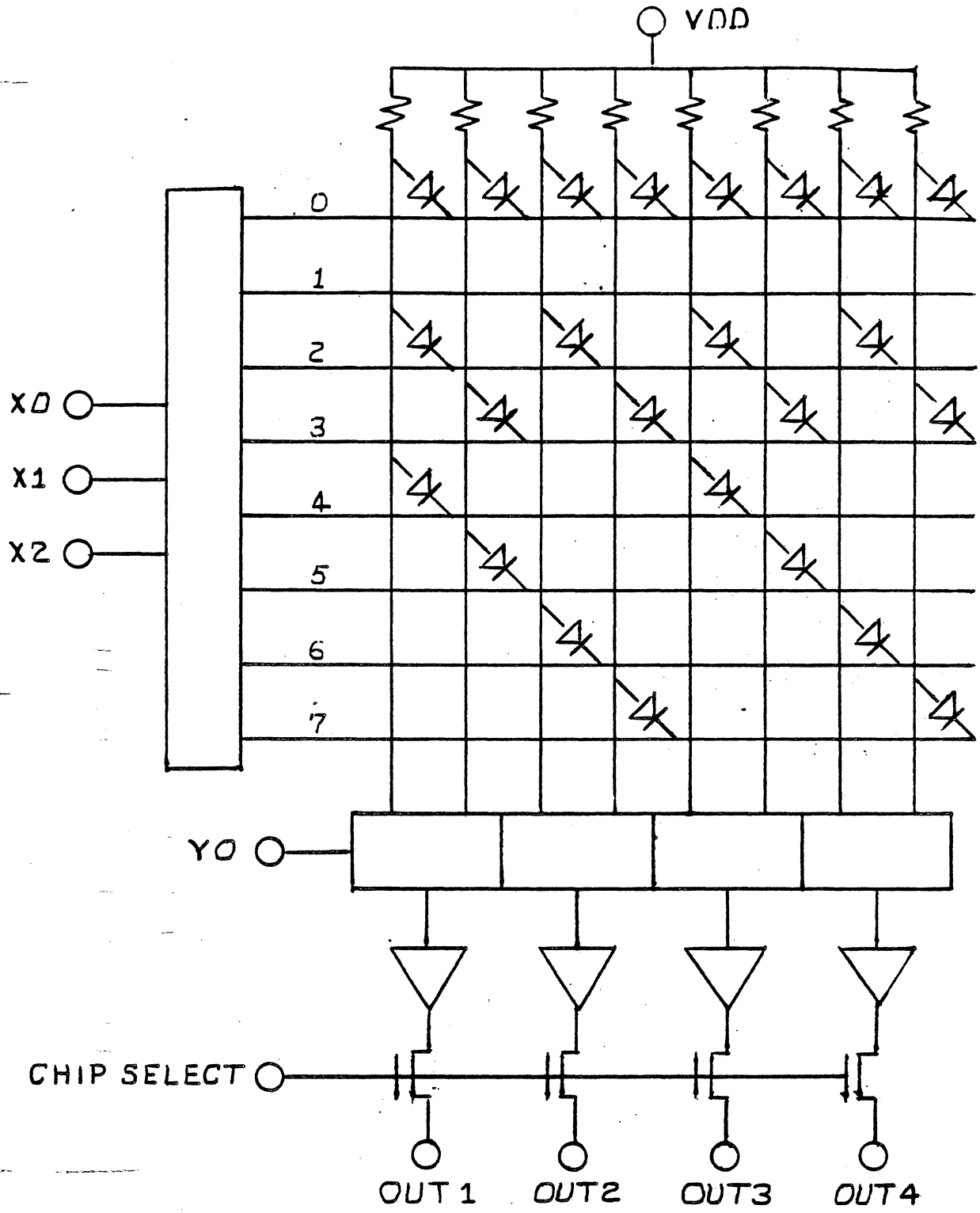
The other variety is called the EPROM or erasable programmable ROM. This sounds like a conflict in terms. It shouldn't be possible to erase and rewrite a read only memory. Their nature in the writing process is quite cumbersome requiring a long period of time and many high voltage pulses. To fill a large EPROM can take 30 to 100 seconds. The erasing operation requires exposure to ultra-violet light. Since this process is so time consuming, the family is not considered to be read/write memory. The other fact which qualifies it as a ROM is that it doesn't forget when power is removed.

2.22 Testing Requirements

What must be done to test this variety of memory? The three different kinds must each be described separately. The end-user may well find a family of pin-for-pin compatible parts, such that his design will work with EPROM, PROM or masked ROM. But the testing done by the vendor and at incoming inspection is quite different.

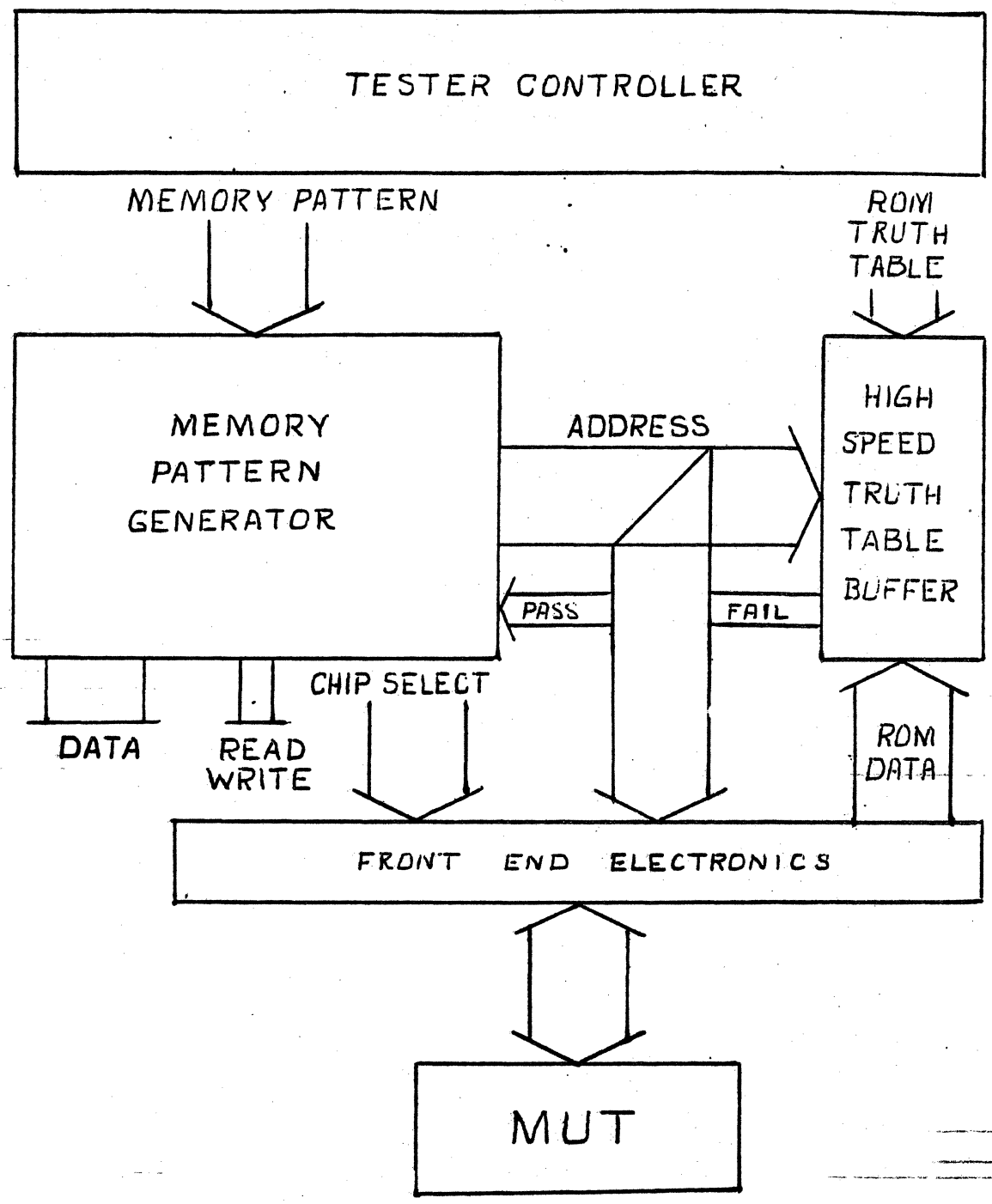
2.23 Masked ROMs

The masked ROM is the most straight-forward because there is a minimum that can be done to it. The data contained in the memory array cannot be changed, so all the sections of the RAM pattern discussion related to the data patterns must be thrown out. Likewise, all the sections of the discussion of tester hardware related to algorithmic data generation must be discarded. ROM data is totally random. Masked ROM testing, then, is simply a special form of random logic testing wherein the data input is some sort of binary counting scheme with random expected output data. Since the ROM is a purely combinatorial device, the lines of its truth table may be shuffled into any sequence and can be expected to pass. As a matter of fact, the user may well expect the vendor to have tested it with the truth table shuffled into all possible sequences, or at least he may expect that no guaranteed parameter will be exceeded if it is done. Hence, all of the sections of the RAM pattern discussion related to addressing sequences do apply. Here again, the N^2 patters rear their ugly heads as the only sure bet that the worst case access time has been discovered. Here, ROMs have an edge over RAMs because multiple bits are accessed simultaneously. The value of N is the number of addresses,



BASIC ROM ORGANIZATION

FIGURE 10



ROM TESTER BLOCK DIAGRAM

FIGURE 11

rather than the number of bits. A 4096 bit ROM, organized as 512 x 8, would pass through the $2N^2$ calculation as 524,288 cycles, rather than the 33.5 million required for the 4K RAM.

Since the truth table for a ROM is a hybrid between random logic testing and algorithmic RAM testing, the test equipment required would optimally be a hybrid between a random logic tester and a memory pattern generator. In Figure 11, is a block diagram of such an organization. The memory pattern generator has all the features described earlier for RAMs, plus a high speed buffer made of RAMs. The address lines go to the MUT and simultaneously to the high speed memory. The buffer memory outputs are available to the tester's comparators as expected data from the MUT, rather than the pattern generator's expected data. If the buffer has been thoughtfully loaded with a copy of the ROM truth table, it is possible to perform any conceivable addressing sequence that the pattern generator can create, without further concern for the random nature of the MUT.

2.3 PROMs

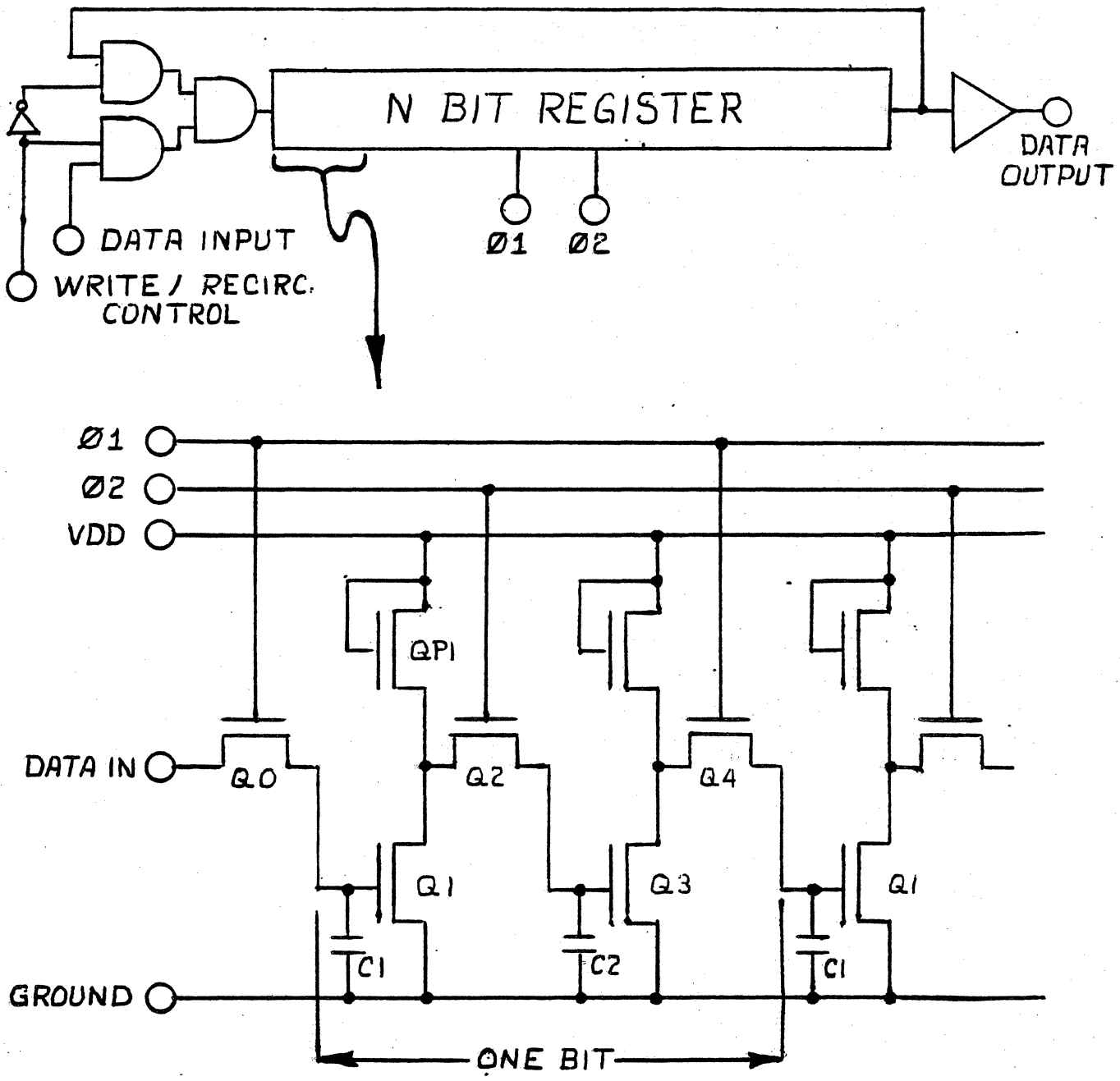
The fusable link programmable ROMs are a quite different problem. They are originally built completely full of either 1's or 0's. If the vendor were to blow any of the links in an attempt to verify programmability, he would have rendered it useless. Thus, the vendor and incoming inspector are faced with the fuse maker's chore of determining that if overloaded, the link will blow. There are two approaches to the problem. You can trust statistics and try to blow a sample or you can enable the programming circuitry and almost blow each link, observing a number of electrical characteristics which indicate that they are about to go. Both tactics are employed by various vendors.

The statistical approach is not one of blowing every link in one out of ten devices for lot qualification. A more common practice is to imbed an extra row and column of bits which can only be accessed in a special test mode. A rather clever scheme I saw was one which blew every other bit of the extra row and column at the wafer probe stage. After assembling the units, this "checkerboard" pattern could be used as a pattern to get a rough handle on access time, and then most of the remaining test bits could be blown. It can be argued that the checkerboard does not guarantee address uniqueness, but recall the qualities of read-modify-write. If you blow one bit; read out the fact that only one is blown; blow another bit; verify that only two are blown; etc., you can be quite certain that the decoder line is capable of handling the programming current.

The programming path inspection method is an interesting exercise in "Howmanyvoltagemeasurementscanyoumakepersecond". The idea is to force varying amounts of current (up to one-half the blow value) down the programming path, observing various pertinent voltages and impedance variations. A surprising amount can be learned about address uniqueness and bit blowability with this technique.

2.31 EPROMs

The testing of the various floating gate ultra-violet erasable ROMs is,



SHIFT REGISTER ORGANIZATION

FIGURE 12

at best, tedious. Test times are long because of the time involved in writing into them. Many repetitions of high voltage pulses typify the writing process. Usually, this adds up to the ten millisecond timeframe for the writing of a single bit. Multiplying this times thousands of bits results in tens of seconds. With the ultra-violet erasable types, the process of erasing one pattern and writing a new one, does not lend itself to a clean single insertion test. It is also difficult to verify that these devices maintain a pattern for six months, in a few seconds of test time. In short, testing these re-programmable ROMs is difficult and expensive. This contributes significantly to their cost. For that reason, they will probably never be as cheap as the other forms of semiconductor memory. On the other hand, they have proven to be invaluable in system debugging situations and are unlikely to fall from popularity.

2.4 Shift Registers

2.41 Device Organization

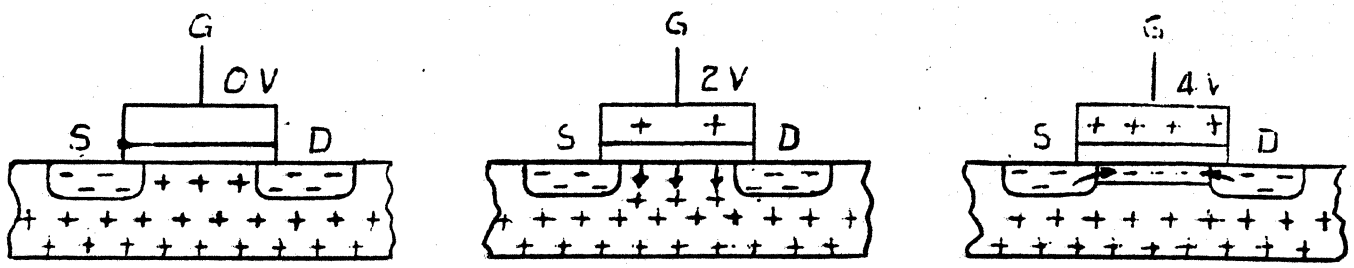
Shift registers have been around a long time. They are cheap, fast, and dense. They have always seemed to keep pace with, or possibly a little ahead of, random access memories for number of bits per chip. For several years they seemed to fall out of favor because RAMs were getting larger and faster, but recently they have reappeared in the form of charge coupled devices. Working models with 65K bits per chip have appeared.

Shift registers comprise the category known as serial memory; they function just as the name implies. If a bit is written into a shift register, it will be passed along from one bit position to the next, until it reaches the end. At that time, you may either do something with it or simply recirculate it back to the input for future reference. Most shift registers are two phase dynamic circuits. In Figure 12 is a block diagram of a shift register and a detail of a typical bit structure.

The scheme is much like a master slave flip-flop arrangement. Begin with both clock phases off and present a 0 at the input node. There will be no effect in Q1 because Q0 is off. Now momentarily turn on Q0 with a pulse on clock Ø1; capacitor C1 will be discharged to a 0 and remain there after Q0 is turned off; the 0 on C1 will turn Q1 off, allowing QP1 to pull its drain high. Now a pulse on clock Ø2 will momentarily turn on Q2 allowing capacitor C2 to be charged to the 1 state; the 1 on C2 will turn on Q3, causing its drain to be pulled low. A 0 has now propagated from the input of the shift register to the output of the first bit. The next pulse on clock Ø1 will bring new data into the first bit via Q0 and place our original 0 on C1 of the next bit via Q4. This continues until the 0 has propagated to the end of all N bits at which time it may be taken from the data output pin and recirculated back to the input, or we may replace it with another 0 or a 1.

2.42 Testing Requirements

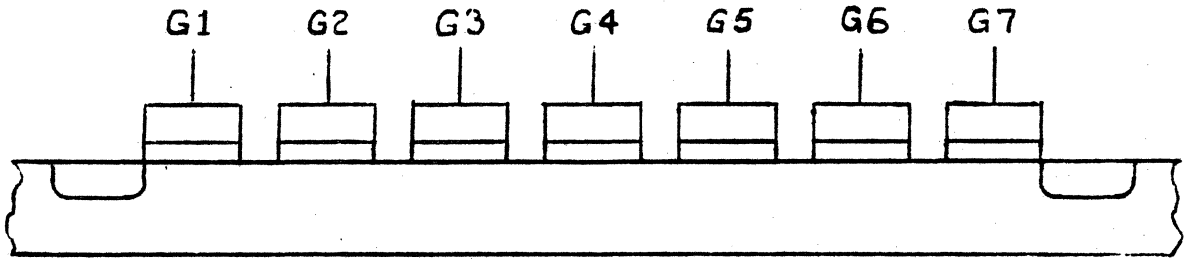
The shift register is relatively simple, with a minimum of peripheral circuitry. The array of bits in a RAM may only occupy 50% to 70% of the chip area, where in a shift register the string of bits may occupy



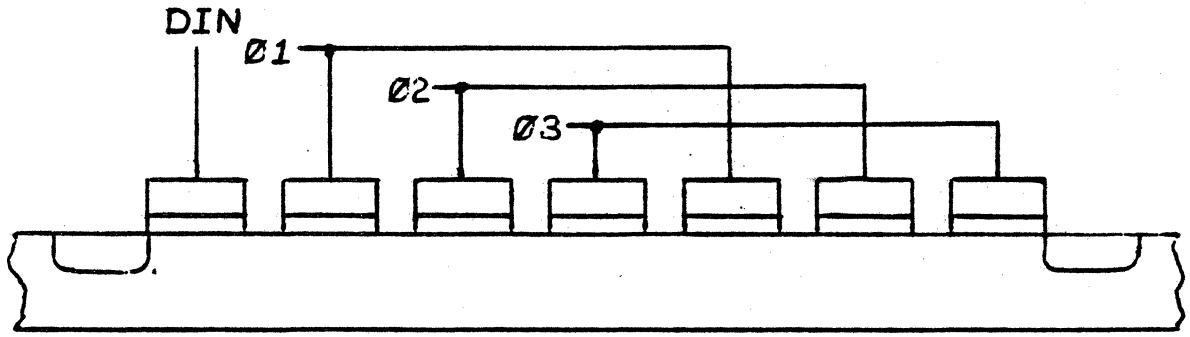
A) GATE OFF

B) GATE AT THRESHOLD

C) GATE ON



D) SERIES OF ADJACENT GATES



E) 3 PHASE CCD SHIFT REGISTER

CHARGE COUPLED DEVICE MECHANISM

FIGURE 13

80% to 90%. As a result of this, testing is considerably simplified. A most helpful feature is that any given bit of data or sequence of data bits written into the register will occupy all bit positions as it is shifted from the input to the output. Quite clearly, this eliminates the elaborate proliferation of patterns for verification of bit uniqueness. If the register can pass a large number of 0's with a single 1 in the middle and a large number of 1's with an imbedded 0, there should be little doubt about the integrity of the bits. If a search is made to discern possible bit to bit disturbances, the layout of the register should interact only with the bits immediately before and after itself. However, in doing a shift register the layout artist is hardly likely to design a chip which is two mils wide and four inches long. Quite obviously, the string of bits will be zigzagged into 32 rows of 32 bits in an attempt to create a nearly square chip. The most elaborate scheme I have yet encountered for discerning interaction as the data snakes back and forth, is the following data pattern:

10110011100011110000....

Several repetitions of this data pattern should eventually create any conceivable adjacent disturbance pattern which might be envisioned.

Generally, shift register patterns can be produced by a pattern generator designed for a RAM. All that needs to be different is that the address lines remain unused and the patterns must be written assuming a straight sequential access to the device.

2.5 CCD Memories

2.51 Device Organization

Charge coupled devices are in a different category from all the devices discussed so far. They are not a straight-forward redesign of standard capacitors and transistors. The basic mechanism bears a resemblance to the action of an MOS transistor. In Figure 13, a sequence of diagrams traces an evolution of concepts which leads to the CCD mechanism. In diagram a) is a basic N-channel MOS transistor. It is built on a P-type wafer and has two zones of N material diffused into the top surface to serve as a source and drain. The gap between the source and drain is covered by a thin layer of glass (SiO_2) which will serve as a nearly perfect insulator. On top of the glass is a layer of conductive material, usually either aluminum or polysilicon. This conductive layer is the gate electrode. Observing the path between source and drain within the silicon, there is a diode in one direction as the transition is made from the N-type drain to the P-type substrate, and another diode in the other direction in going from the substrate to the N-type source. It is obvious then, that if the source is tied to ground, the drain can be moved either above or below ground and no current will flow to the source because one or the other of the diodes will be reverse biased. If the gate electrode is raised to a voltage more positive than the substrate, the laws of electrical attraction and repulsion dictate that the positive charge normally distributed throughout the P-type substrate will be repelled away from the surface just under the gate. As the gate voltage continues to rise,

the more electrons there will be in each packet. If an image had been photographically focused on to the surface of a large array of such a structure, the packets under gates receiving much light would be larger than the packets under gates receiving little light. If the packets are now shifted off the chip, it is easy to visualize that the image has been captured electrically and could be used to modulate a video signal for television or any of a number of visual applications.

A detrimental facet of CCD devices results from the fact that heat also generates electron-hole pairs. If a gate is raised high and held for a few milli-seconds, an appreciable number of electrons will gather under it. This is a continuous process which tries to add charge to a packet for as long as it remains on the surface being pushed from gate to gate. Thus, the CCD structure is dynamic in nature. In general, a packet will remain intact and well-defined for only a few hundred transitions, after which it must be detected and reinjected if it has not reached the final output.

There are three basic organizations used in CCD memories. In Figure 14 is a block diagram of each of the three. First is the straight serpentine organization. The refresh amplifiers are usually spaced either 128 or 256 bits apart. The line addressable RAM organization is similar to the serpentine arrangement, except that each refresh point is made available to the outside world by a 1-of-N selector. Finally, is the serial-parallel-serial structure at the bottom of Figure 14. Here the data is shifted serially into a fast N bit input register, then the entire register is shifted in parallel into N slow registers. The N bits are shifted slowly to the bottom until they reach the fast output register, where they are presented on the data out pin at full speed.

2.52 Testing Requirements

Most of what was said about shift register testing is also true of CCD testing. The most difficult exercise that can be done is to pass a single empty bucket through a register filled with full buckets. "Slop" from the full buckets will eventually accumulate in the lone empty bucket along with thermally generated charge. The internal structure of the device must be known in order to select an appropriate data stream which will cause a single empty bucket to travel down each path. This is usually a straight-forward determination. A primary difficulty in CCD testing results from the fact that the CCD structure is entirely a gate structure. This simplicity gives designers the confidence to use large chip areas and expect reasonable yield. With chips of 65K bits and a gate capacitance of 200femtofarads, the result is approximately 1200 picofarads per clock. The CCD itself burns no power, but the driving of magahertz-range clock pulses into 1200 pf loads amounts to very healthy clock drivers. If the clock-lines are buffered on the chip, heavy surge currents will cause noise which the CCD mechanism is sensitive to. This also produces heat to which CCD's are also sensitive. An additional complication is that in the act of maximizing density, the various clocks overlap each other as much as they lie over the substrate. Clock-to-clock capacitances equal to the clock-to-ground capacitances are not uncommon. Therefore,

a particular value will be reached at which all positive charge will be totally absent in a very thin layer just beneath the gate. This zone is now void of free charges and consists of intrinsic silicon which is neither P-type nor N-type. This zone is called the depletion region because it is depleted of carriers. The gate voltage which produces this condition is called the threshold voltage. If the gate is raised to any value of voltage above threshold, the depletion region becomes so attractive to negative charge that free electrons in the N-type source and drain rush in forming an N-type channel. The transistor is now said to be turned on and any difference in voltage between the source and drain will cause current to flow. The more positive the gate voltage, the deeper the channel becomes and the channel is, therefore, less resistive such that for a given source to drain voltage, the current flow will be greater.

The basic element of the charge coupled device looks and works very much like a transistor except that it has no source or drain. In Figure 13-d is a structure which resembles a transistor with six gates between a single source drain pair. If one of the middle gates is raised well above threshold, the surface beneath it will be heavily depleted, causing that area to be hungry for negative charge. If none of the other gates are turned on, nothing more will happen because there is no source of electrons. If gates 1 and 2 are raised simultaneously, the N-type source provides an ample source of electrons and the area under them will be flooded. Now if gate 1 is turned off, the packet of electrons attracted to gate 2 will be isolated and unable to move. If gate 3 is raised now, it becomes an attractive place for electrons to be, so the packet of charge will be evenly distributed under gates 2 and 3. If gate 2 is now turned off, the only escape is to gate 3. This process may be continued until the packet of charge reaches the drain, at which time a sensing circuit can detect its presence. If we had tied the gates together in pairs as in Figure 13-e, then as the packet of charge was moved from gate 4 to gate 5, gate 2 would have been raised momentarily. Depending on whether gate 1 is raised at that time, a new packet of charge may or may not enter the stream and be trapped under gate 2. Thus the presence or absence of charge can be interpreted as a 1 or 0 and can be propagated from one end to the other. This is a basic three phase CCD shift register, sometimes known as a bucket brigade. Other more thorough descriptions of this activity speak in terms of surface potential or surface voltage. Activity on the gates cause potential wells and barriers, causing buckets of charge to be dumped into wells or to be blocked by barriers -- but the resulting activity is the same as described here.

An interesting aspect of the CCD structure is that it is not necessarily digital in nature. The number of electrons can be varied in each packet of charge, such that an analog detection circuit at the output could produce a different voltage as each packet comes out, rather than a logic 1 or 0. The question is: how would such a phenomenon be useful? Suppose the shift register just described had no input and the chip was accessible to light. It is a well known fact that light generates electron-hole pairs when it strikes silicon. If, while gates 2 and 5 are raised, the chip is exposed to light, the generated electrons will gather under the positively charged gates and the holes will be absorbed into the substrate. The brighter the light or the longer the exposure,

if clocks are not buffered on the chip, it is very difficult to prevent undesirable cross-talk between the clock lines.

It is not impossible to overcome these difficulties. I only wish to caution you that in setting about CCD testing, you would be well-advised to check out your clock driving capability and take special care in grounding and power supply bypassing.

3.0 MICROPROCESSOR AND PERIPHERAL LSI TESTING

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3.1 Introduction

In the discussion and reference material provided in this session, it is impossible for me to avoid any references to the particular test system I am most familiar with. The purpose of this material is to convey the message of what problems are likely to be encountered when developing microprocessor test programs and to show solutions to these problems.

Most general purpose LSI test systems have the basic ingredients necessary -- such as a large disc memory system, high speed data buffer memories and programmable pin electronics with level, timing and I/O control. I will be referencing some particular features in terms of the Fairchild Sentry II hardware and software nomenclature which will be defined below. The reader should be able to associate these features with equivalents for other systems. When possible in the lecture period, students familiar with other hardware/software systems are encouraged to share their knowledge.

3.2 Basic Considerations to Test Strategy

The microprocessor/LSI testing problem can be divided into several categories which are defined as follows:

1) The Function Test - This is the functional pattern of ones and zeroes which are applied to a device under test (DUT) for which the DUT responses are "measured". The measurement of a response is usually a go-no-go comparison to an "expected" response pattern.

2) Parametric Tests for Specified AC and DC Parameters - This consists of the measurement of a DUT voltage, current or timing parameter and comparison with a specified limit.

3) Characterization Tests - These tests are designed to measure the interaction of device parameters or the interaction of device functional states in order to fully understand all of the "unspecified" characteristics of a small chip of silicon. The results of the knowledge gained from these tests are used for product evaluation and process control.

The three categories just defined have interactions -- such as the necessity of a functional exercise to precondition a device for a parametric measurement. Or, -- characterization programs involve the procedures used for parametric measurements and functional pattern implementation.

The separation of these three subjects is to point out that a particular user may, or may not, elect to perform characterization or parametric tests. Also, the details of implementing these three steps are unique.

3.3 Function Test

The tasks necessary in the design and implementation of the function test can be divided into sub-categories such as:

1) Functional pattern definition from the device point of view. That is, what functional patterns are necessary to use in order to be assured that the microprocessor under test meets all of its functional specifications? At this point, a judgement decision is necessary -- there is no way that a 100% complete functional exercise which does all possible microprocessor unit (MPU) instructions with all possible data arguments under all possible external conditions will ever be implemented. If it were, test time per device would be several hundred years. A reasonable set of functional tests must be defined at the beginning, with plans for growth when certain anamolies are discovered in your applications or via the grapevine in the MPU user community.

2) The mechanism of pattern expression and implementation must be considered. What are the off line resources available, such as CAD for device simulation? What hardware mechanisms does the tester have? What information about an MPU do you have at your disposal -- data sheets, user manual, block diagram, state transition diagram, instruction set, end use application programs, circuit diagram, photo micrographs of silicon real estate, etc?

In the case of the architecturally simple device, although it may have many active elements such as a RAM or shift register, it was found that effective testing could be achieved with algorithmically defined pattern sequences. However, occasionally for these devices, layout perturbations to regular arrays occurred to achieve optimum chip area or geometry and, hence, this resulted in complications to the test pattern. For example, topological scrambling of address lines to achieve true physical patterns in memories, or strange disturbance patterns to expose subtle coupling effects can be required.

The microprocessor test problem can be thought of as testing a RAM, ROM, shift register, decoder, counter, sequence controller, multivibrator, tri-state I/O ports, and arithmetic logic unit all rolled into one. The diagnostic design could be based on considering each of these MPU building blocks such as testing the program counter by making it increment, or testing an internal array of registers with classical RAM patterns like a diagonal, etc.

The microprocessor diagnostic could also be considered in light of the overall aspects of the device. That is, applying a group of instructions

and data to the device which represent a "problem" for the MPU to solve or compute. Then, observing the fact that the problem solution is correct one can assume the proper internal operation of a number of device functions. If the solution was incorrect, some malfunction must have occurred. A critical decision must be made -- should the MPU response be "tested" or evaluated on each instruction cycle, or is the evaluation of a problem solution sufficient? The pitfall with the latter choice is the possibility of multiple errors cancelling each other, producing the same end result as a properly functioning device.

Other engineering considerations affecting the functional testing strategy may be based on the microprocessor application, systems analysis, design confirmation, interface verification and enhancement features. Device manufacturing or user incoming inspection operations impact test strategy, based on requirements to maximize throughput, accumulate process data and characterize product performance.

3.4 Function Test Definition

The source of a test engineer's data for function text preparation is usually one of the following:

1) Truth table already defined (like for a RAM or many MSI devices)

2) A logic diagram description (gate level) which can be input to a CAD test generation system with a truth table output (many custom LSI manufacturer's have this).

3) A written functional description of a device's operation (which many times is very nebulous to the engineer who has to test it). RAMs, game chips are usually in this category.

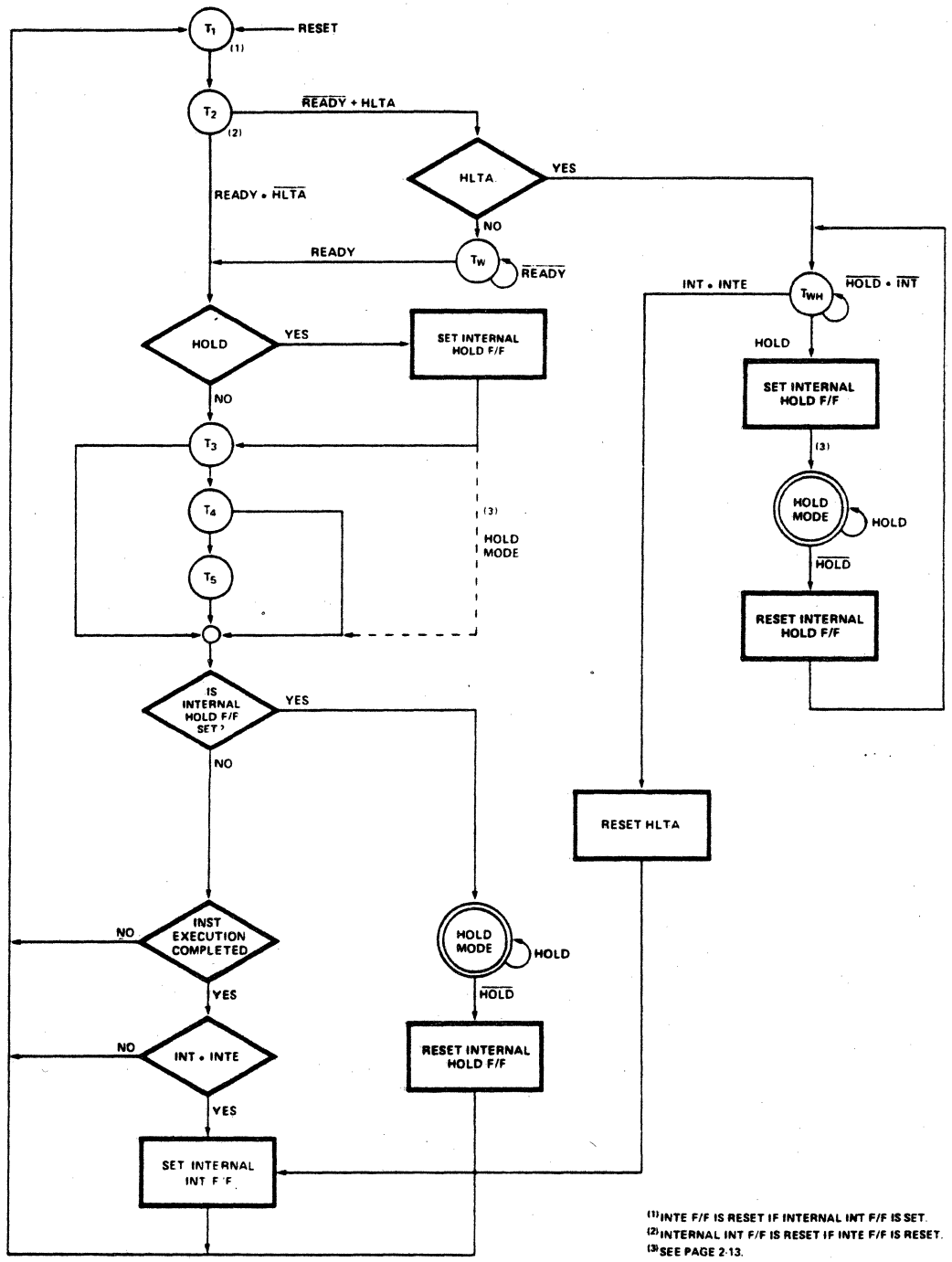
4) Machine state diagrams and instruction code definitions for microprocessors.

The fourth case is where the next part of this discussion begins. In Figure 1 is a reproduction from the manufacturer's user manual of a state transition diagram for the 8080 microprocessor. Figure 2 & 3 show input and output instruction cycle logic activity on the MPU pins.

The information on these three figures partially describe the interface to an 8080 MPU from the outside world. The functional pattern from the tester must obey these interface rules. Each type of microprocessor has its own interface rules -- some simple, others very complex. Before test pattern implementation can proceed, the test engineer must understand the particular MPU's interface rules.

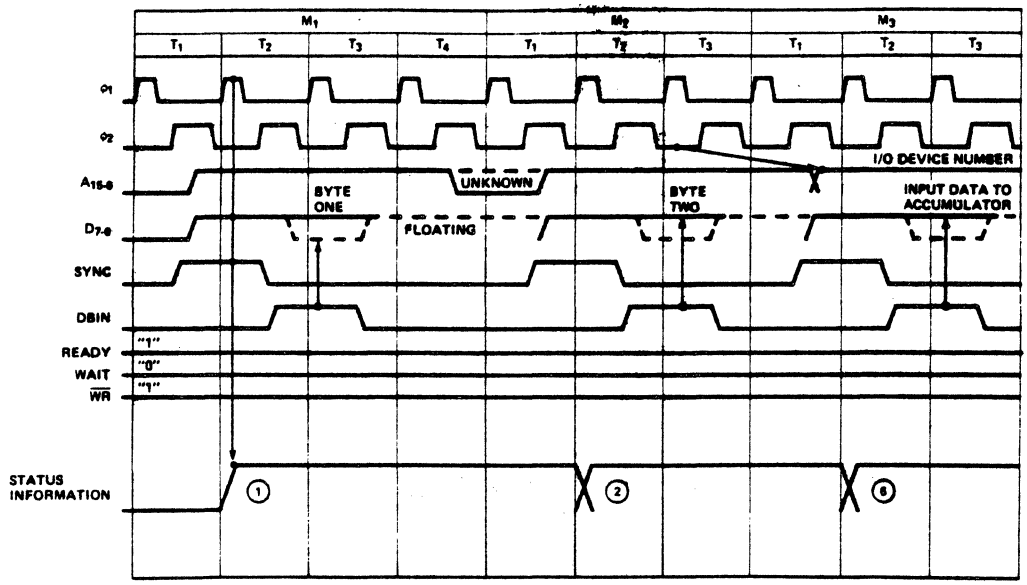
3.5 Getting Started

A simple function test is a good step to try when getting familiar with a new device. Programming the steps to apply power, setup timing and functional levels and performing a simple MPU test such as loading the



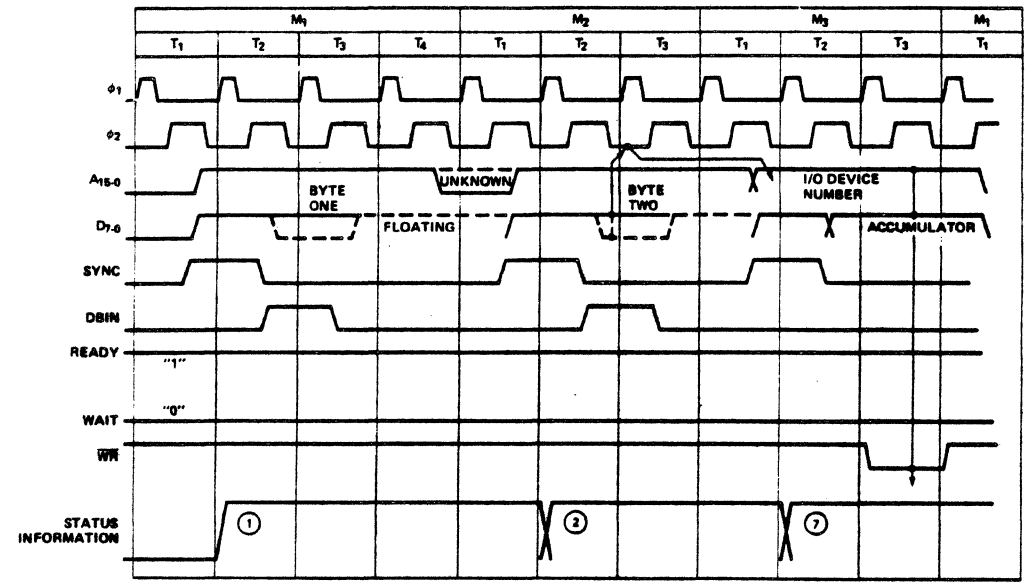
CPU State Transition Diagram

FIGURE 1



NOTE: (N) Refer to Status Word Chart

Figure **Input Instruction Cycle**



NOTE: (N) Refer to Status Word Chart

Figure **Output Instruction Cycle**

FIGURES 2 & 3

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the 8080 data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
											Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

Table 8080 Status Bit Definitions

FIGURE 4

accumulator and reading it back is the first task. Of course, a test fixture consisting of a socket, load board and pin assignments must be defined, too. In the work I have done with microprocessors and the test system I use, a one-to-one pin assignment between the MPU socket and tester pins is normal. With other systems, it may be necessary or convenient to group pins by their function, such as address, data, clocks, etc.

During your initial learning phase, don't try to start off with min/max voltages or timing. Write a simple program, using nominal levels, expressed as variables which can easily be altered. Try to get the tester/MPU interface to work first by keeping it simple.

3.6 Timing

Timing relations for some microprocessors can be quite complex. The scope of this discussion assumes you are using automatic test equipment with computational capability. The definition of tester timing generator delays and widths, or start/stop times should be made by writing equations in terms of the manufacturer's timing parameters. The manufacturer has defined timing in certain ways for a good reason -- because those parameters relate to the internal device design.

Figure 5 shows the timing relationships for an 8080. There may be some redundant parameters defined by the manufacturer, and some min/max constraints on one parameter which affect another. That is, you may not be able to use all minimum values concurrently. In the case of an 8080, TCYC, the cycle time is actually a function of TØ1, TD1, TØ2 and rise/fall times of the clocks. But cycle time is the common buzz word used to indicate a device grade level, hence, TCYC may be one of the independent variables. Assuming the rise and fall times are of equal value, TR, for a tester with timing expressed in terms of pulse delay and width, the following equations apply.

TD2 = TCYC-4TR-TØ2-TD1-TØ1

TD2DLY = TØ2-TOFF (clock phase 2)

TG2WDT = 3TR+TD2+TØ1+TD1

TG1DLY = TR+TD2+TG2DLY (clock phase 1)

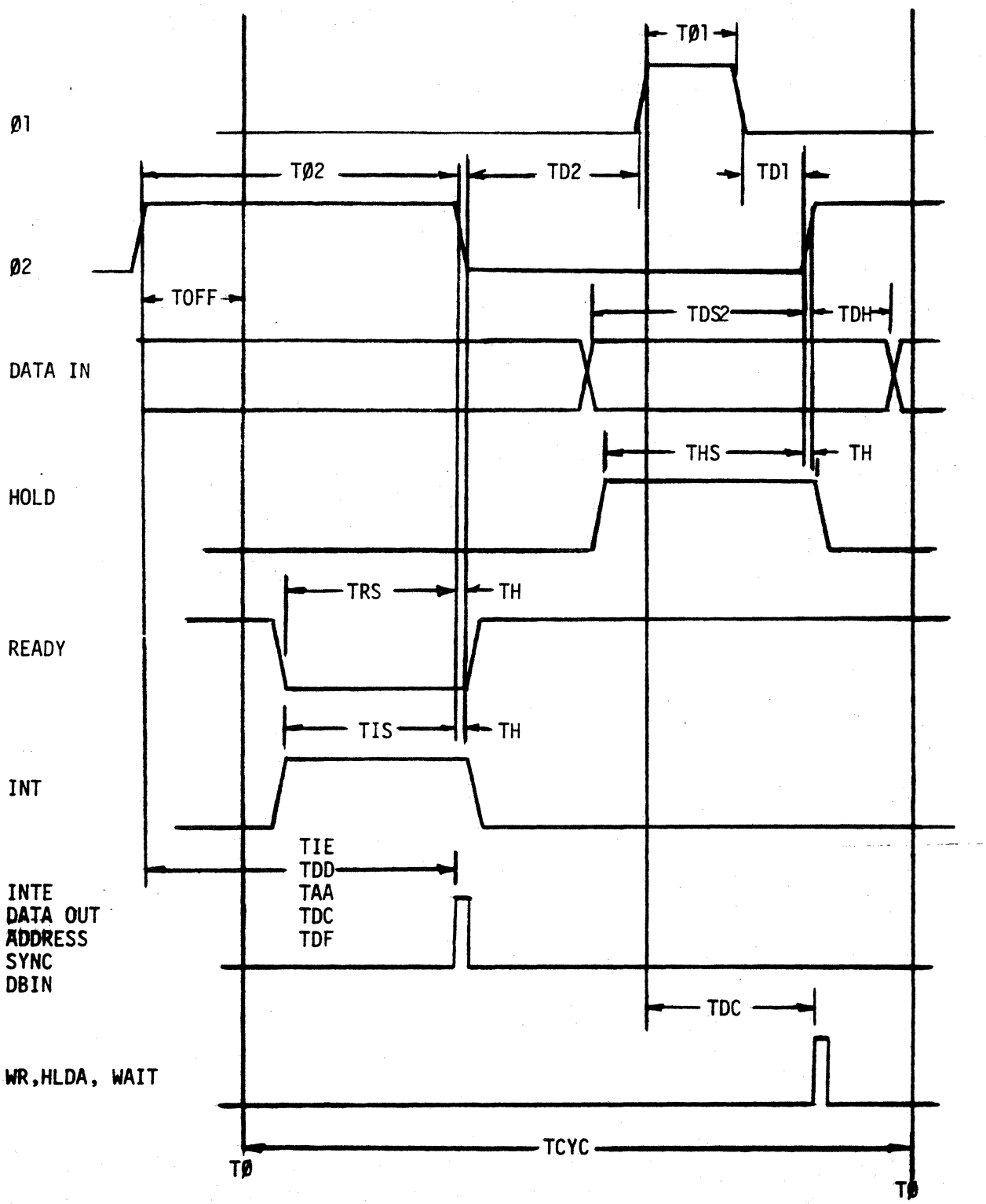
TG1WDT = TR+TØ1

TG3DLY = TCYC-TDS2-TOFF-2TR (data input)

TG3WDT = 2TR+TDS2+TDH

TG4DLY = TCYC-THS-TOFF-2TR (hold input)

TG4WDT = 2TR+THS+TH



8080T TIMING DIAGRAM

TG5DLY = TG2DLY-TRS-TR (ready input)

TG5WDT = 2TR+TRS+TH

TG6DLY = TG2DLY-TIS-TR (interrupt input)

TG6WDT = 2TR+TIS+TH

TG2DLY = TDD-TOFF (outputs relative to Ø2)

TG8DLY = TG1DLY+TR+TDC (outputs relative to Ø1)

The TOFF parameter for the above timing set defines the placement of the waveforms relative to the tester's cycle period. The mode in which the tester is being used in examples presented here is that input/output changes on the data bus pins will occur at time TOFF relative to phase 2 rising edge.

3.7 Initialization

Some form of initialization, or reset pattern, must precede the first MPU operation to be tested. This is defined in the manufacturer's specifications and usually requires holding a reset pin in an active state for some number of clock cycles. Just for good measure when getting started, throw in some extra reset cycles (just in case that data sheet is in error).

For a single chip microprocessor, the first activity after the reset is an instruction fetch. The first address out of the MPU has some defined value, such as ØØØØ for the 8080, or $FFFC_{16}$ for a 6502 or 6800. You might actually write a small truth table, with the reset cycles and a few instruction cycles, and use the tester's function fail datalogger to record the MPU outputs.

After writing a few test vectors by hand, you will conclude that a) specifying input data is tedious, with all those ones and zeroes all over your coding form, but b) keeping track of all the expected responses is really tough, and c) you could really use a computer to wade through this functional test preparation problem. There are already two computers at your disposal while you're sitting at your tester console -- the one driving the tester and that little one plugged into your test socket. You may also be lucky enough to have a big CAD/Test Generation system at your disposal, but for an MPU with its logic described on 34 pages of size D drawings -- good luck!

3.8 Diagnostic Language

One advantage you have, with an MPU, is some form of defined language -- its instruction set. The single chip microprocessors all have assembly language mnemonics (unfortunately all different) and for some of the bit slice processors you can make up your own. There are several advantages for being able to implement your diagnostic exercise in the native language of the microprocessor to be tested:

1) MPU operations are specified in terms of instructions.

2) You can communicate clearly with others about your diagnostic (especially important in resolving user-vendor problems).

3) Your diagnostic, or part of it, can incorporate some critical end use application for which your MPU will be used.

How can a string of MPU instructions be converted into tester hardware instructions to be executed? The two approaches to consider are 1) a complete MPU emulator with conversion into tester hardware statements, or 2) use that MPU in the test socket and a software program which emulates the external environment to the microprocessor.

The latter method is recommended by this author because it can be the most expedient in really understanding the true nature of that complex device to be tested. What I mean by emulation of the external environment is to make the tester look like the peripheral components in a microprocessor system -- such as external memory, I/O controller, etc. This is depicted in Figures 6 & 7.

3.9 Virtual Memory

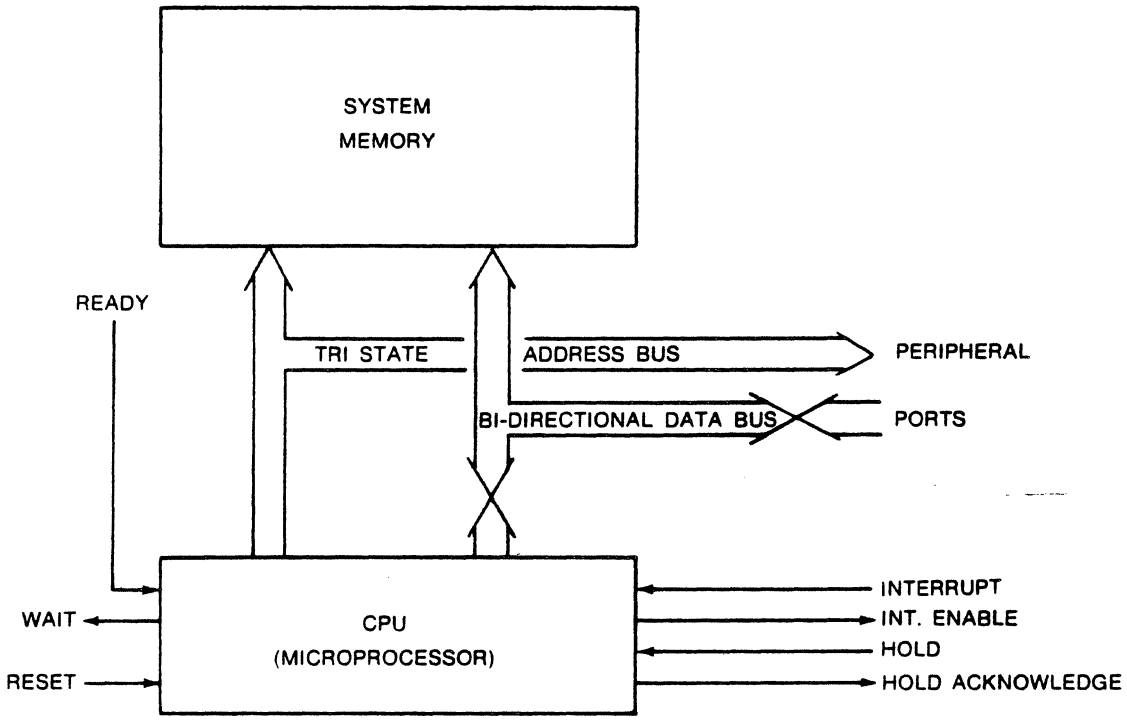
Typical microprocessors have up to 16 address pins and are capable of addressing 65536 memory locations. In order to allow a diagnostic to be expressed exactly as an end use program, we'll need a large random access memory in the tester to contain the diagnostic. Having this memory will allow your diagnostic to contain recursive loops. An area of the test system's mass memory can be used for this purpose. Monitoring the MPU's address will define where to fetch a byte of data from or where to store output data.

The access time to this virtual memory will be relatively slow, but it is used only in the pattern generation stage -- e.g. the conversion of the diagnostic expressed in the MPU language into the tester hardware format. Once the diagnostic is executed, using an MPU in the test socket, the virtual memory on the disc, and a tester software program to make the tester look like the MPU's external environment, you will have a functional pattern with all inputs and outputs described in a form for production testing.

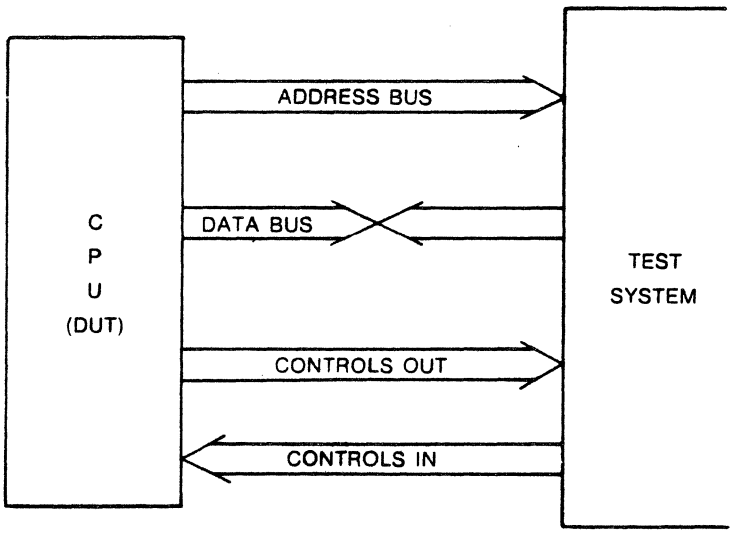
3.10 Learning

This process is called "learning" or signature response processing. It's more than just a pattern learning process common to generating ROM patterns. Here, the input stimulus to the MPU is a function of previous learned outputs. If the MPU has just executed a jump instruction, the next address will define where the next byte will be fetched from in memory.

The validation of learned responses from the MPU can be done several ways. After completing the diagnostic execution with one MPU, the recorded pattern can be "played back" to that MPU and other samples for confirmation. Also, the diagnostic execution from virtual memory is likely to



CPU-Basic System Block Diagram



Test System Supplying All Stimulus and Sense to CPU

FIGURES 6 & 7

go awry if the MPU in the test socket fails. Self checks can be made in the diagnostic to flag errors, such as conditional jumps to an error routine if data or ALU flags are improper. A "map" recording on the line printer can ge generated during diagnostic execution which gives a record of what's going on.

3.11 The Map

A printed record of events occurring during diagnostic execution is a valuable tool in failure diagnosis. The important constituents of information to be recorded are shown in Figure 8. This example, for an 8080, shows the number of clock cycles into the pattern of each bus transaction, the pattern memory address, microprocessor address, data read or written, the instruction mnemonic for instruction fetch cycles, and the content of important internal registers.

When diagnosing functional failures, this map is a valuable tool in comparing datalogged fail results with the correct data. The mechanism of getting the data for internal registers during pattern generation can be either by computation (modeling the MPU being tested), or by executing PUSH instructions to extract the data from internal registers of the MPU in the test socket. Both methods could be used if desired and results compared to give the ultimate in validating the learned pattern.

Another important aspect of this approach to pattern generation is the ability to document the reaction of the MPU to invalid instructions. For example most microprocessors do not use all of the possible opcodes, and the manufacturer rarely documents what these illegal opcodes would do. If you're using a MPU in a sensitive application and wish to perform a systems failure analysis, you should be able to predict the system's reaction to the failure of a component external to the MPU.

Also, the semiconductor manufacturer can take advantage of this technique for new MPU designs. Design errors in the initial masks can be easily detected and documented. And, even though the new chip may have some faults, a functional pattern which does work with the new device can be realized and used for process characterization which can greatly improve the chance of success on the next iteration in the design phase.

3.12 Pattern Generator Implementation

So far we have discussed the desirability of implementing the functional diagnostic in the microprocessor's own language and executing this diagnostic using a real device and mass memory in the tester. The record of the pattern accumulated in the tester's high-speed parallel pattern memory (buffer memory or local memory) is then saved for inclusion in the final test program in order to bypass the software overhead encountered in the generation phase.

The first step in implementing this process is to build what I call a background pattern in the high-speed tester memory (local memory will be used for this term). This background consists of the test vectors required

STAT1A TEST PLAN MAP SN 2

8080 TRUTH TABLE GENERATION FOR SPM REV 1 PAGE 1 AMD

LOCAL MEMORY PAGE 1

COUNT	L.M. ADDR	MPU ADDR	DATA R	DATA W	OPCODE	STAT	STACK ADDR	A/F	B/C	D/E	H/L
00000006	0007	0000	C3		JMP	A2	FFF2	0046	0000	0000	0000
READ WAIT TEST											
00000029	0015	0001	45			82					
00000032	0016	0002	00			82					
00000035	0017	0045	3E		MVI A	A2	FFE1	0046	0000	0000	0000
00000039	0020	0046	00			82					
00000042	0021	0047	32		STA	A2	FFD0	0046	0000	0000	0000
00000046	0022	0048	00			82					
00000049	0023	0049	00			82					
WRITE WAIT TEST											
00000052	0024	0000		00		00					
00000065	0031	004A	3E		MVI A	A2	FFF0	0046	0000	0000	0000
00000069	0032	004B	FF			82					
00000072	0033	004C	32		STA	A2	FFDF	FF46	0000	0000	0000
00000076	0034	004D	FF			82					
00000079	0035	004E	FF			82					
WRITE WAIT TEST											
00000082	0036	FFFF		FF		00					
00000095	0043	004F	F3		DI	A2	FFF1	FF46	0000	0000	0000
READ HOLD TEST											
00000110	0057	0050	21		LXI H	A2	FFE0	FF46	0000	0000	0000
00000114	0060	0051	00			82					
00000117	0061	0052	00			82					
00000120	0062	0053	36		MVI M	A2	FFCF	FF46	0000	0000	0000
00000124	0063	0054	00			82					
WRITE WAIT TEST											
00000127	0064	0000		00		00					
00000140	0071	0055	2C		INR L	A2	FFBD	FF46	0000	0000	0000
00000145	0072	0056	36		MVI M	A2	FFAC	FF02	0000	0000	0001
00000149	0073	0057	FB			82					
00000152	0074	0001		FB		00					
00000155	0075	0058	2C		INR L	A2	FF9B	FF02	0000	0000	0001
00000160	0076	0059	36		MVI M	A2	FF8A	FF02	0000	0000	0002
00000164	0077	005A	C9			82					
00000167	0100	0002		C9		00					
00000170	0101	005B	31		LXI SP	A2	FF79	FF02	0000	0000	0002
00000174	0102	005C	F6			82					
00000177	0103	005D	FF			82					
00000180	0104	005E	E1		POP H	A2	FFF6	FF02	0000	0000	0002
00000184	0105	FFF6	08			86					
00000187	0106	FFF7	07			86					
00000190	0107	005F	D1		POP D	A2	FFF8	FF02	0000	0000	0708
00000194	0110	FFF8	06			86					
00000197	0111	FFF9	05			86					
00000200	0112	0060	C1		POP B	A2	FFFA	FF02	0000	0506	0708
00000204	0113	FFFA	04			86					
00000207	0114	FFFB	03			86					
00000210	0115	0061	F1		POP PSW	A2	FFFC	FF02	0304	0506	0708
00000214	0116	FFFC	02			86					
00000217	0117	FFFD	01			86					
00000220	0120	0062	FB		EI	A2	FFFE	0102	0304	0506	0708
00000224	0121	0063	00		NOP	A2	FFFE	0102	0304	0506	0708
READ WAIT TEST											
00000247	0127	0064	00		NOP	A2	FFFE	0102	0304	0506	0708
INTERRUPT REQUESTED											
00000251	0130	0065	C7		RST 0	23	FFFE	0102	0304	0506	0708
00000256	0131	FFFD		00		04					
00000259	0132	FFFC		65		04					
00000262	0133	0000	00		NOP	A2	FFFC	0102	0304	0506	0708
READ WAIT TEST											
00000285	0141	0001	FB		EI	A2	FFFC	0102	0304	0506	0708
00000289	0142	0002	C9		RET	A2	FFFC	0102	0304	0506	0708
00000293	0143	FFFC	65			86					
00000296	0144	FFFD	00			86					
00000299	0145	0065	00		NOP	A2	FFFE	0102	0304	0506	0708
INTERRUPT REQUESTED											
00000303	0146	0066	CF		RST 1	23	FFFE	0102	0304	0506	0708
00000308	0147	FFFD		00		04					
00000311	0150	FFFC		66		04					

FIGURE 8

to reset or initialize the MPU (as discussed earlier in the familiarization process you should go through). Following the reset vectors should be nothing but data which has only the clocks running, no interrupts or other special controls active, and all zeroes or null data for the address and data bus pins. Also, the data bus pins should be in the output state (drivers only) and comparators enabled on all outputs.

When this pattern is applied to the MPU, a functional failure should occur after the reset. Because the output expect data was all zeroes, a failure will occur for those pins responding with a 1. The following simplified flow diagram in Figure 9 shows the basic steps to process each byte of the diagnostic. In this example, there are two control pins -- VMA indicating a valid memory address is on the address bus, and R/W indicating a Read or Write operation to external memory.

3.13 Special Backgrounds

Now, what do we do with those special interface pins, such as interrupt request pins, or memory not ready pins, or hold or DMA pins to allow other devices to have direct memory access? Since the diagnostic is being executed from the MPU instruction set, how can we invoke activity on these special pins in order to test the MPU's reaction to their requested operation?

My solution to this is to allow flag codes to be appended to the diagnostic data in virtual memory. When an instruction or data byte is fetched or written into a memory address containing a flag code, or background flag, the generator is designed to interpret this flag and modify some data in the initial background of data in local memory. Recall that the initial background data in local memory was a null value or inactive state for these special control pins. Background flags can be defined to manipulate each one of these pins or combinations of them. For the 8080 generator described below, background codes are:

1 for not ready

2 for hold

3 for interrupt request

4 for release interrupt request

The data in your diagnostic, which is normally two hexadecimal digits for an 8 bit MPU, would have an extra digit appended to it to activate a desired external event. For example, an ADD A instruction has an opcode of 87. To cause a wait operation on this instruction, the data would be 187.

One other mechanism should be mentioned. How is pattern generation terminated? Again a special background code can be used for the last instruction to tell the generator to terminate. The termination process should consist of a branch to the end of the pattern memory, and calling a utility program to save the pattern data on the disc. Also, it is

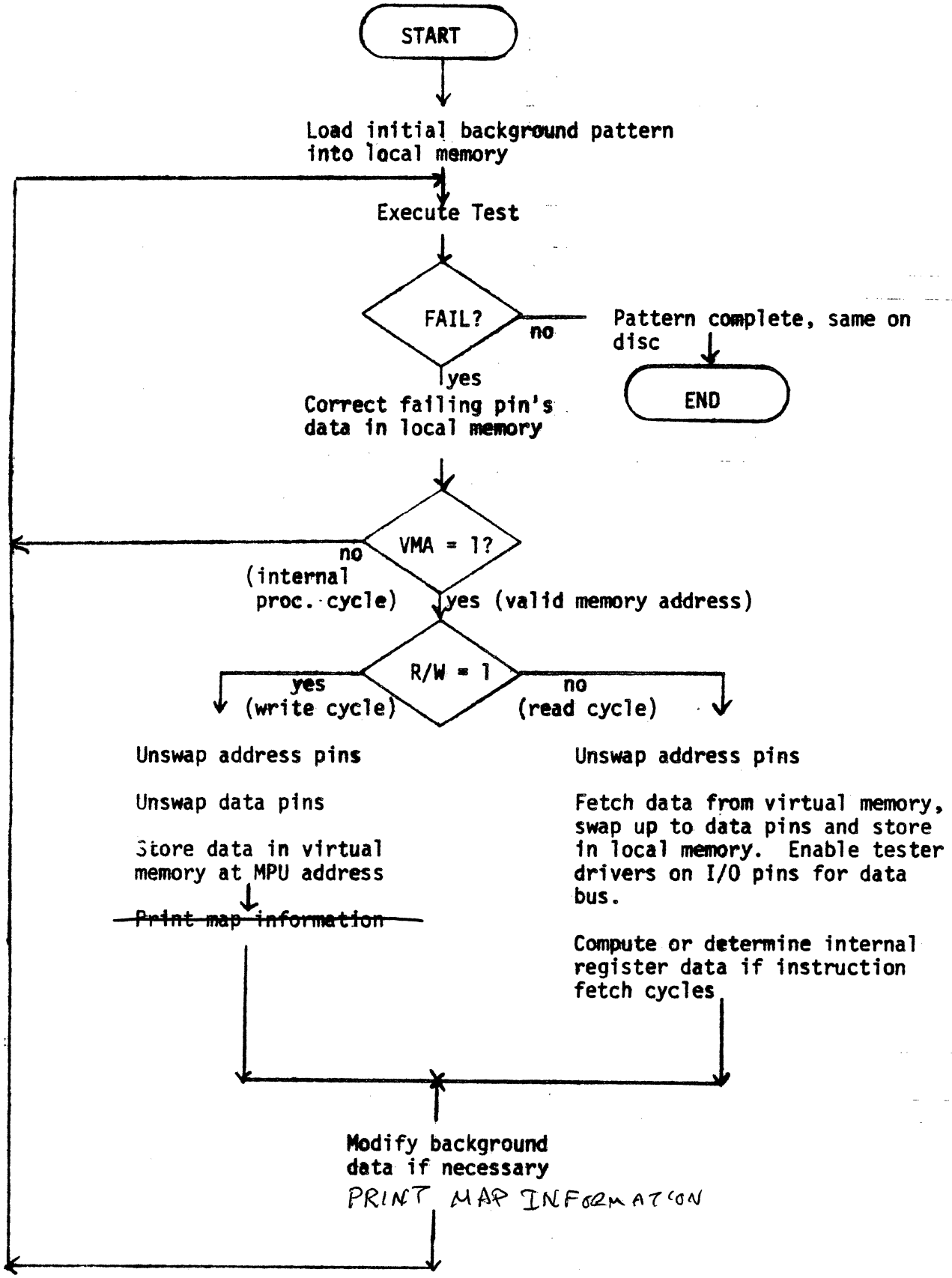


FIGURE 9 - Simplified MPU

Pattern Generation Flow Chart

useful to keep a record during generation of what instructions were executed and how many, and display or print this information when finished.

The next section contains exerpts from documentation for the 8080 program package I recently developed for a Sentry II/VII with a sequence processor subsystem. The sequence processor module (SPM) enhances the high-speed local memory by allowing nexted subroutines and I/O, mask and waveform format changes to be described within the functional pattern. This results in a sizeable pattern compression (3.5:1 minimum) and greater throughput.

3.14 8080SPM Program Package

The programs contained in the 8080SPM package are designed for evaluation and testing the 8080 8 bit N Channel microprocessor. This software makes use of many features in the Sentry II or Sentry VII Sequence Processor Module in order to more effectively test the 8080 at higher throughput and less cost.

The major programs in this package, used under job '80SP' are:

SPG80 - A sequence processor pattern generator which allows the 8080 diagnostic to be implemented in 8080 codes and execute the same as a final 8080 application.

8080T - An evaluation test program with all functional, ac and dc tests including characterization Shmoo plots.

8080D - A diagnostic in 8080 instruction codes designed to validate all specified functions of the 8080.

LBCHK - A diagnostic to check the 8080 load board. (LB1135)

LMSAVE - An overlay for MPU pattern generation used by SPG80 and 8080T.

MNEMON - A list of 8080 assembly language mnemonics called by LMSAVE.

LMLOAD - An overlay used to transfer data between disc and local memory.

SPLOT - A utility program for executing Shmoo plots.

80T - A truncated version of 8080D (first phase)

MAP - A program for listing 8080 pattern maps from a DIF data file originally created by SPG80.

.ASGN - A DIF file which assigns disc files for SPG80 use.

.DELETE - A DIF file for deleting SPG80 files after completion of a generation.

.INSTL - A DIF file for creating the coreimage files LMSAVE, LMLOAD and SPLOT after loading this software package.

CMPOS - A program for displaying composite shmoo plots from disc data created by 8080T.

INTØØ1 - A pattern file for Intel 8080A.

AMDØØ1 - A pattern file for AMD 9080.

NECØØ1 - A pattern file for NEC 8080A.

3.15 8080 Sequence Processor Pattern Generator (SPG80)

3.151 Introduction

SPG80 is a function test generation program for the 8080 microprocessor and makes use of the sequence processor system (SPM) in the Sentry II or VII to achieve a significant reduction in test time. This software allows the user to represent the 8080 diagnostic in 8080 instruction codes and applies the LEAD (learn, execute, and diagnose)philosophy to build SPM data codes. Use of this software and the SPM allows the compaction of thousands of test vectors into a minimum local memory space with no sacrifice in the ability to test all properties of the 8080's reaction to each instruction such as status, address, data, floating pins, wait, interrupt, hold and others.

The use of subroutines allows each byte to be represented by only one local memory vector. MPU status, address and data are expressed simultaneously with two sets of 8 tester comparators used to differentiate between status and data response on the MPU data bus. The invert register function is used to pass MPU data and address to the called subroutines. Various subroutines are used depending on the number of cycles required to complete each byte. Clock bursts of various counts are used to simulate long wait or hold periods.

The generator creates a virtual memory to represent MPU address space in which the user's diagnostic is loaded. The diagnostic program may have special "background" flags appended to the normal 8 bit MPU bytes to invoke special sequences such as interrupt request, long wait (not ready) conditions or hold periods. Once an interrupt request is invoked, it remains on until the MPU acknowledges, or until another background defects it. Waits and holds can also be executed on MPU write cycles if the background flag exists at the MPU memory address being written into.

Special information is logged for each execution byte to document the user's 8080 diagnostic. This document is a valuable tool for failure analysis for it gives a record of the cycle count of each byte, MPU address, data read or written into virtual memory, instruction mnemonics, MPU status, and the content of all 8080 internal registers (stack, A,F,B, C,D,E,H, and L). Special flags are logged when backgrounds are invoked for waits, holds and interrupt requests. At the completion of diagnostic

execution, a record of what instructions were tested and how many times is listed. Also a list of unused op-codes is tabulated.

3.152 SPG80 Operating Instructions

1. The diagnostic program is entered into the MPU virtual memory from cards (SWITCH = 3) or magnetic tape (SWITCH = 6). The format of the source diagnostic is described in the LMSAVE documentation and is repeated here. Beginning in column 1 are:

```
Address Byte1 Byte2 Byte3    Comment
```

where address beings in column 1 and is in hexadecimal from Ø to 1ØØFF. Address space ØØØØ to FFFF is for normal memory addressing and 1ØØØØ to 1ØØFF is for in/out instruction data. One blank space separates each address and data byte. Data bytes are also in hexadecimal notation. Up to three data bytes may be on each card (record). Cards or records may leave the address field blank, in which case data bytes are loaded in the next consecutive location from the previous byte. All data fields need not be used. A card with no address and data specified will leave the address unchanged. Comments, such as assembly language mnemonics begin after column 19. A card or record with a // card or end of file record will terminate the loading process.

The diagnostic may be resident on the Sentry disc and transferred to the MPU memory by using a scratch mag tape as follows:

```
// MTAP REW
// FDUMP '8080D' MTW
// MTAP REW
// TOPSY
/. LOAD 'SPG80'
/. SWITCH 6
START TESTER
```

When debugging a new diagnostic, SPG80 switch option 4 may be used for listing and modifying the MPU virtual memory.

2. Preparation of file space on disc is necessary before executing SPG80. The data files begin with the letters SPG followed by 3 digits. SPGØØØ is the MPU virtual memory file and must be assigned 66528 words to accommodate the 65536 main memory addresses plus extra space for I/O data. Also, LMSAVE requires disc areas to be an integer multiple of its 1Ø56 word core memory buffer, hence, 66528 words is used. Files for local memory data must also be assigned. The program uses four ranks plus the SPM microcode rank. Hence, the size should be five times the local memory depth, e.g. 2Ø48Ø words for a 4Ø96 word local memory. The actual number of words generated will be approximately half of the worst case maximum because ranks with no data changes need not be saved. The files begin with the letters SPG and use three numbers to represent the local memory page. Page 139 must always be assigned for it is used to store the initial local memory image. A copy of the generation map can be saved on disc for making extra copies. A disc data file must be defined for storage of the map. The size of this file is over 4ØØØØ words for the diagnostic '8080D'

Example file assignments for a 4Ø96 word local memory are:

```
// ASSIGN 'SPG000' 66528 WORDS DATA
// ASSIGN 'SPG001' 2Ø48Ø WORDS DATA
// ASSIGN 'SPG139' 2Ø48Ø WORDS DATA
// ASSIGN '.MAP' 5ØØØØ WORDS DATA
```

A utility DIF file called '.ASGN' has been made to perform the above assignments. To use this, in DOPSY

```
// SET DIF '.ASGN'
```

3. After file assignment and loading the diagnostic into SPGØØØ function test generation may begin. Switch should be set to zero. The program is set for logging 6Ø lines per line inch, 8Ø lines per page can be enabled by altering statement 4 to 8Ø.

With an 8080 in the test socket, depress start to begin generation. The program will ask you to input starting page number before proceeding (be sure it agrees with one assigned on disc, otherwise a terminal error 1ØØ will be issued).

Also, because there are some variations in the makeup of instructions cycles for various versions of the 8080, this program will ask you to identify the manufacturer of the 8080 before proceeding.

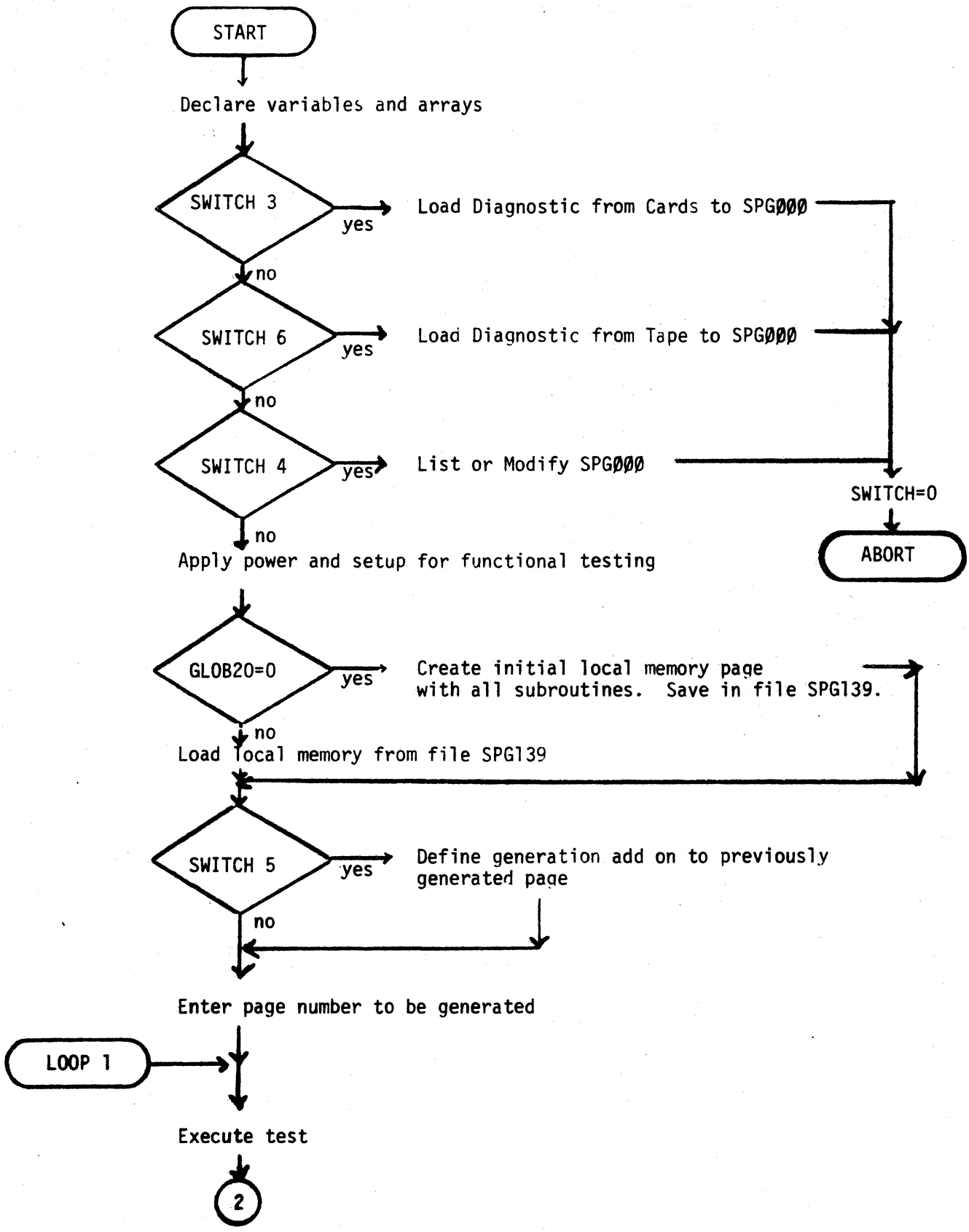
If during diagnostic development, it is desired to execute generation faster, the internal register capture may be omitted by altering statement 3 to zero. This will eliminate the execution of four push instructions per diagnostic instruction.

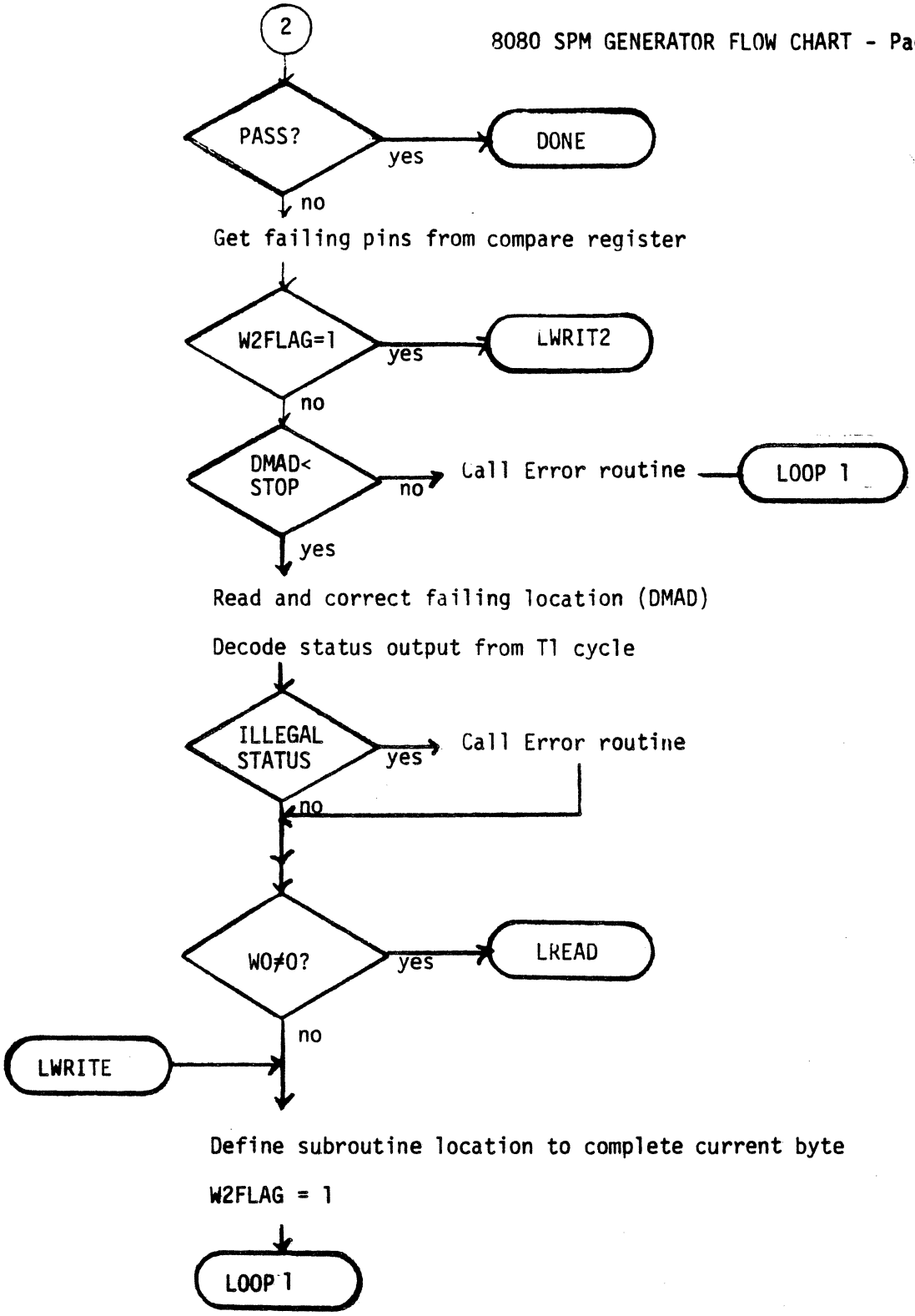
Normal diagnostic generation terminates when a special flag is fetched from MPU memory. This flag word is FFFF hexadecimal. When this occurs, the generated data in local memory is saved on disc, and a summary of instructions tested and not tested is logged. Also the execution of the HALT (HLT) instruction with interrupt disabled will also cause generation completion.

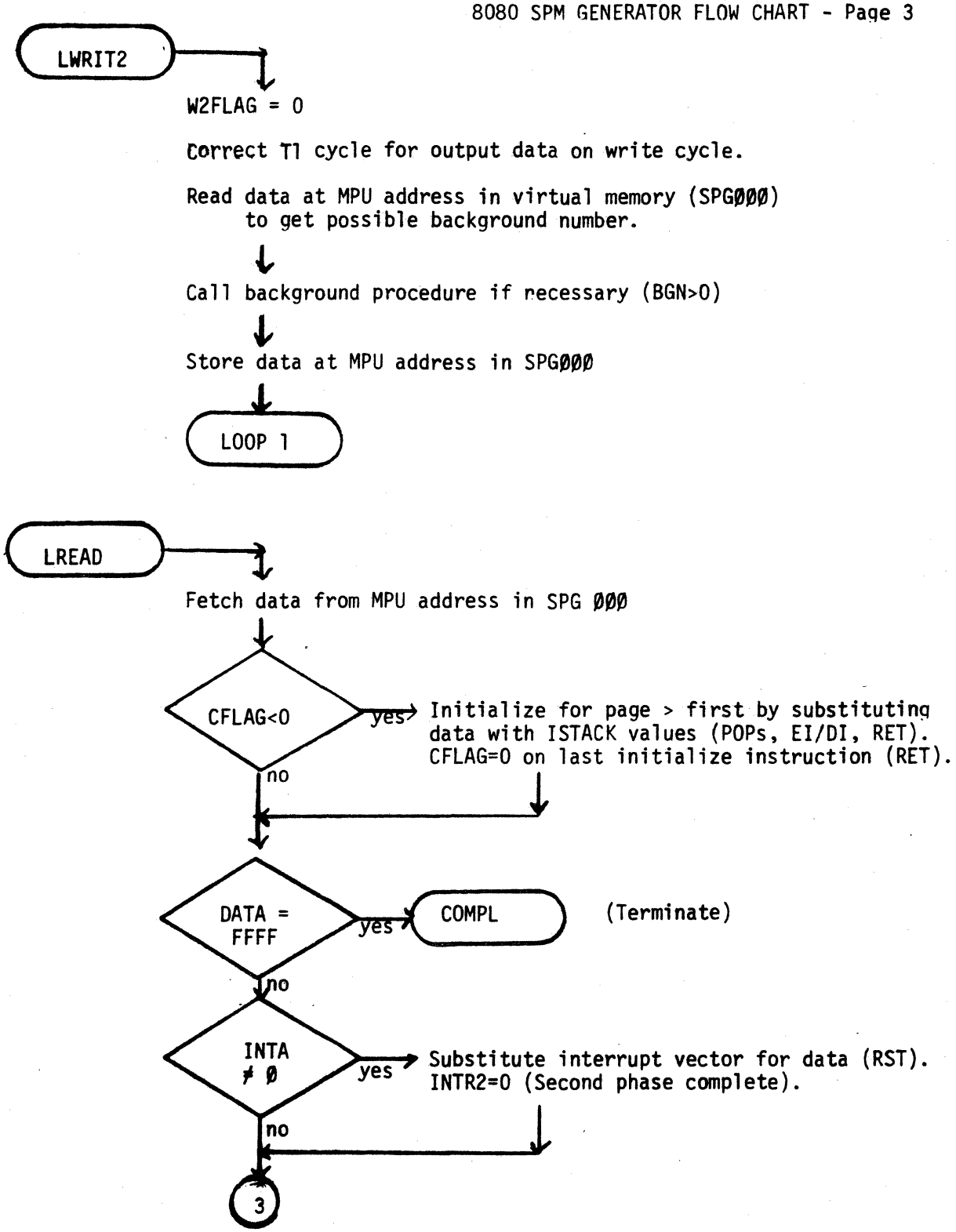
Premature termination with the proper termination and saving of local memory data can be invoked by depressing the lamp test button. On the next instruction fetch cycle, the completion procedure is performed.

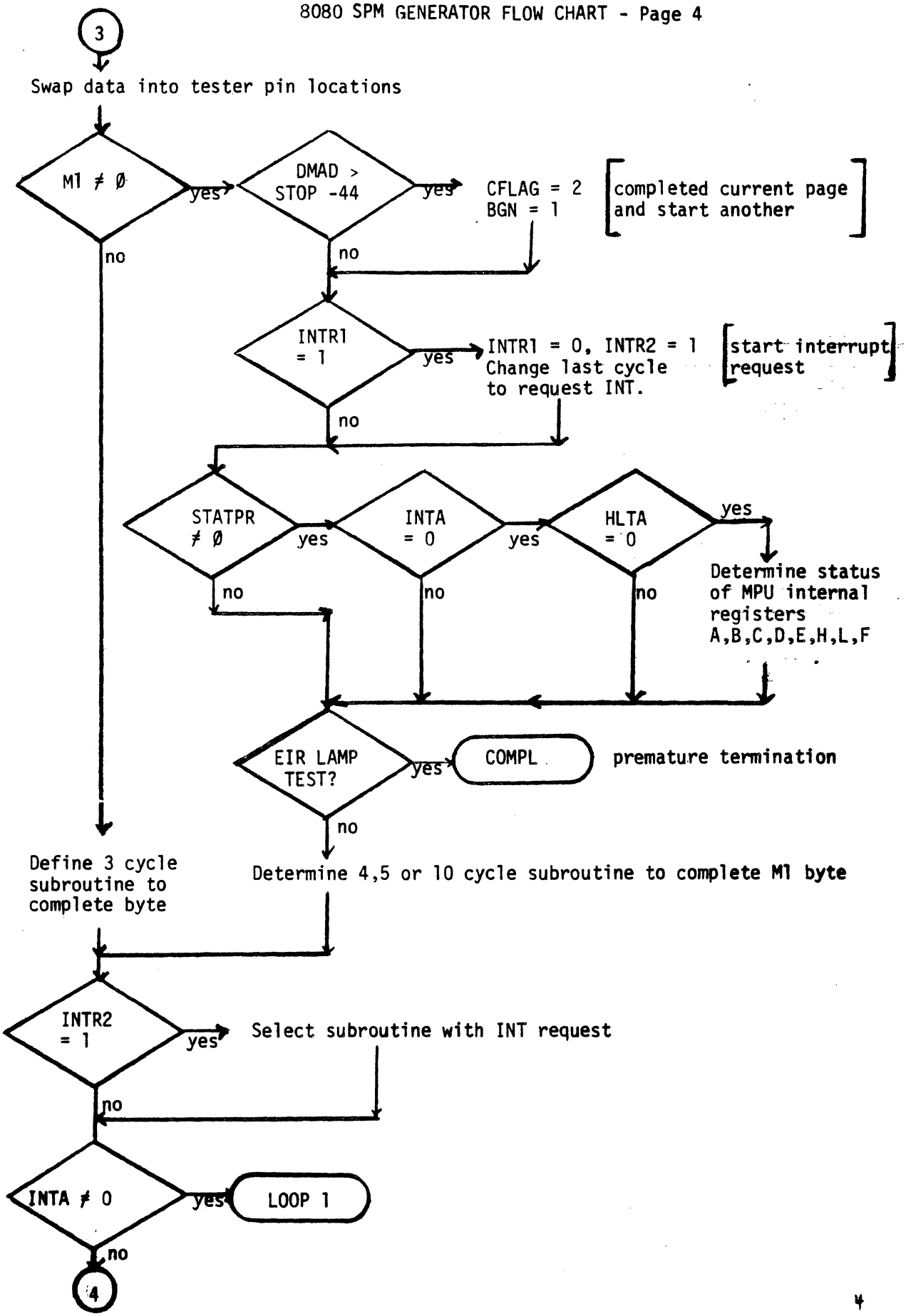
If the generator detects improper responses from the 8080 under test, a diagnostic message is displayed and a program pause executed. At this point, you may look at pin activity with an oscilloscope by initiating a continuous loop in analysis mode with the etc command. An error is detected if a failure occurs in a subroutine (local memory address greater than stop) or if the status is all ones.

4. After completing the generation procedure for your diagnostic, the local memory data may be used by the 8080 test program, 8080T. However, to protect files, 8080T uses files named with the manufacturer's abbreviation as the first three characters. Therefore, GOTO to DOPSY and do the following:

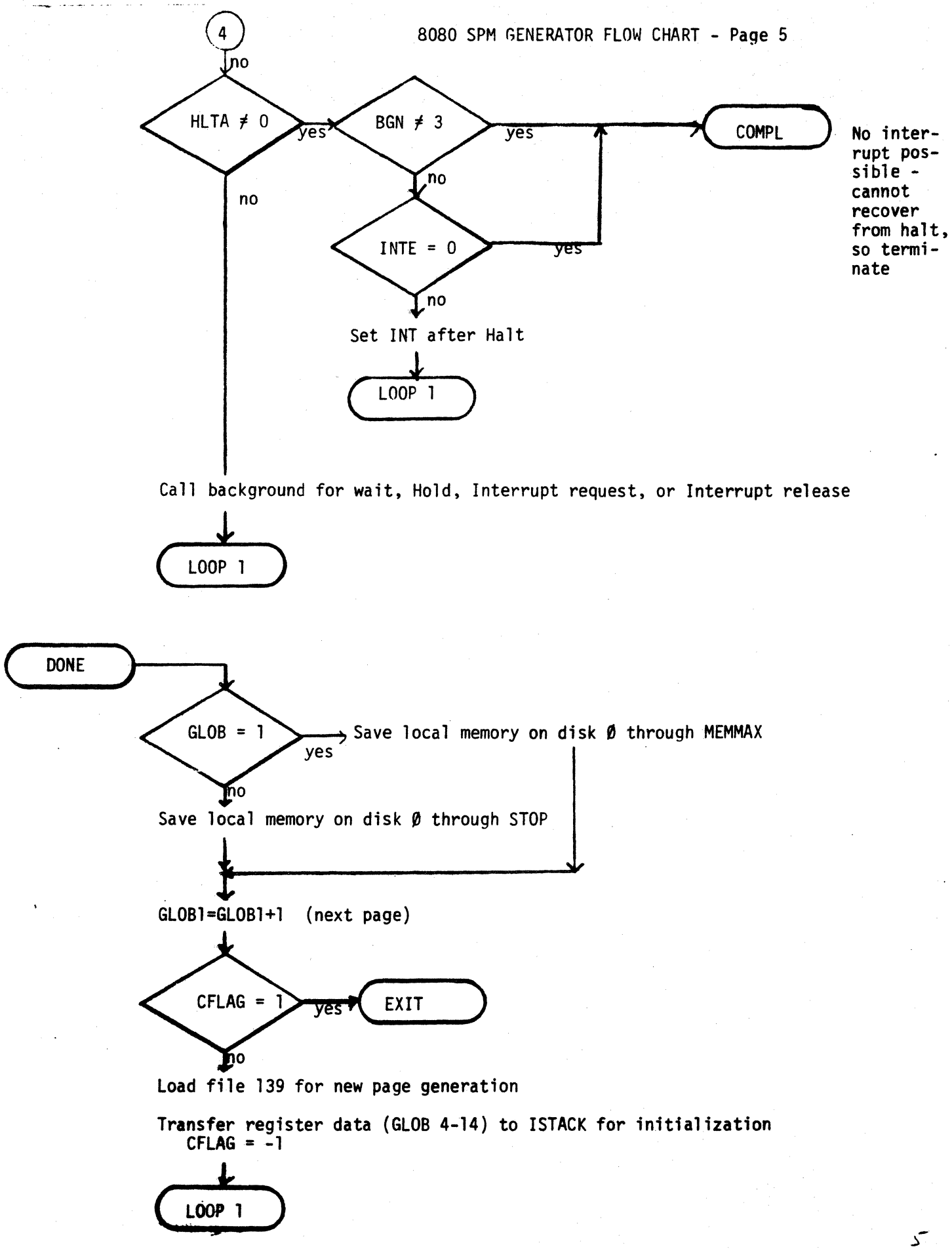

START
Declare variables and arrays
SWITCH 3
yes
Load Diagnostic from Cards to SPGØØØ
no
SWITCH 6
yes
Load Diagnostic from Tape to SPGØØØ
no
SWITCH 4
yes
List or Modify SPGØØØ
no
SWITCH=0
ABORT
Apply power and setup for functional testing
GLOB20=0
yes
Create initial local memory page
with all subroutines. Save in file SPG139.
no
Load local memory from file SPG139
SWITCH 5
yes
Define generation add on to previously
generated page
no
Enter page number to be generated
LOOP 1
Execute test
2

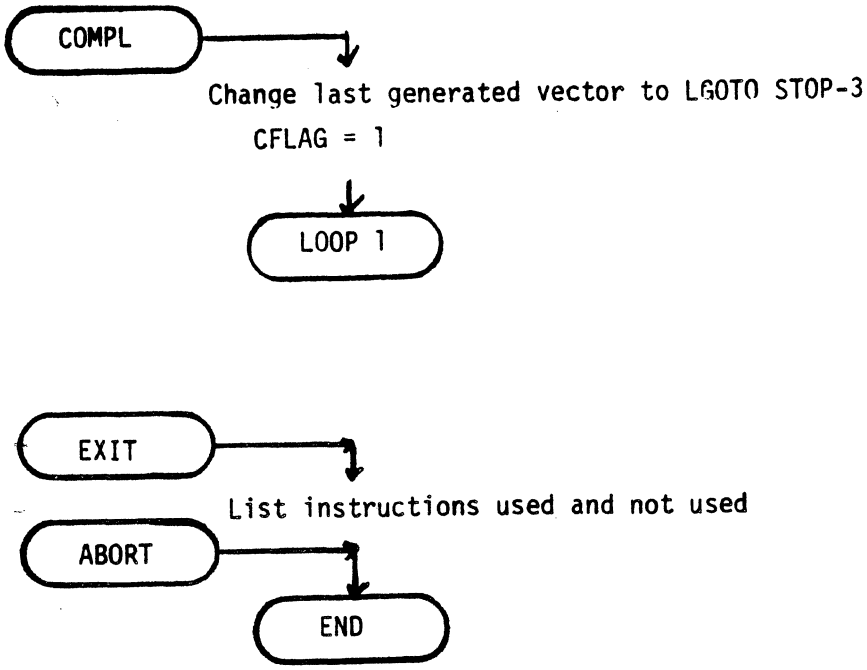

2
PASS?
yes
DONE
no
Get failing pins from compare register
W2FLAG=1
yes
LWRIT2
no
DMAD<
STOP
no
Call Error routine
LOOP 1
yes
Read and correct failing location (DMAD)
Decode status output from T1 cycle
ILLEGAL
STATUS
yes
Call Error routine
no
WO≠0?
yes
LREAD
no
LWRITE
Define subroutine location to complete current byte
W2FLAG = 1
LOOP 1


LWRIT2
W2FLAG = 0
Correct T1 cycle for output data on write cycle.
Read data at MPU address in virtual memory (SPGØØØ)
to get possible background number.
Call background procedure if necessary (BGN>0)
Store data at MPU address in SPGØØØ
LOOP 1
LREAD
Fetch data from MPU address in SPG ØØØ
CFLAG<0
yes
Initialize for page > first by substituting
data with ISTACK values (POPs, EI/DI, RET).
CFLAG=0 on last initialize instruction (RET).
no
DATA =
FFFF
yes
COMPL
(Terminate)
no
INTA
≠ Ø
yes
Substitute interrupt vector for data (RST).
INTR2=0 (Second phase complete).
no
3


3
Swap data into tester pin locations
M1 ≠ Ø
yes
DMAD > STOP -44
yes
CFLAG = 2
BGN = 1
completed current page and start another
no
no
INTR1 = 1
yes
INTR1 = 0, INTR2 = 1
Change last cycle to request INT.
start interrupt request
no
STATPR ≠ Ø
yes
INTA = 0
yes
HLTA = 0
yes
Determine status of MPU internal registers A,B,C,D,E,H,L,F
no
no
no
EIR LAMP TEST?
yes
COMPL
premature termination
no
Define 3 cycle subroutine to complete byte
Determine 4,5 or 10 cycle subroutine to complete M1 byte
INTR2 = 1
yes
Select subroutine with INT request
no
INTA ≠ 0
yes
LOOP 1
no
4

4


4
no
HLTA ≠ 0
yes
BGN ≠ 3
yes
COMPL
No interrupt possible - cannot recover from halt, so terminate
no
no
INTE = 0
yes
no
Set INT after Halt
LOOP 1
Call background for wait, Hold, Interrupt request, or Interrupt release
LOOP 1
DONE
GLOB = 1
yes
Save local memory on disk Ø through MEMMAX
no
Save local memory on disk Ø through STOP
GLOB1=GLOB1+1 (next page)
CFLAG = 1
yes
EXIT
no
Load file 139 for new page generation
Transfer register data (GLOB 4-14) to ISTACK for initialization
CFLAG = -1
LOOP 1


COMPL
Change last generated vector to LGOTO STOP-3
CFLAG = 1
LOOP 1
EXIT
List instructions used and not used
ABORT
END

```
/. DOPSY
// FDUMP 'SPGØØ1'
// DELETE 'INTØØ1'
// CREATE 'INTØØ1' DATA
```

This method will not only rename the file, but compact the number of words assigned on the disc to the amount used.

The abbreviations are INT for Intel, AMD, NEC, TXI for Texas Instruments and NAT for National Semiconductor.

After verifying correct generation with 8080T and other 8080 devices, the SPG files may be deleted from disc if desired. The DIF file '.DELETE' may be used for this.

5. Continuation of a previously aborted generation run or to expand a previously completed run is possible by setting SWITCH to 5. The old pattern file name should begin with SPG and the other SPG files created by '.ASGN' are also needed. After loading SPGØØØ, depress start and SPG80 will ask you to identify the number of the old or original file. It is recommended that the old file number be different from the new file in case the re-generation is not successful and a rerun is necessary. One caution here: The virtual memory is being changed as the MPU writes data. If a restart is made at a point prior to a write operation, you may want to restore SPGØØØ first using SWITCH = 4.

3.16 Description of 8080 Local Memory - Sequence Processor Action

The use of local memory subroutines allows each byte of an 8080 operation to be represented by one local memory vector - the LSET IX with LCALL subroutine. The MPU status (T1 cycle), address and data are expressed simultaneously with the LSET IX word. Two sets of eight tester comparators are used to differentiate between status and data responses out of the MPU under test. The 40 device pins are connected to the first 40 tester pins on a one to one basis. In addition, tester pins 41-48 are also connected to MPU pins 3-10 respectively. Pins 41-48 will monitor MPU status outputs at T1 time, while tester pins 3-10 will perform data I/O during T2 cycles.

The two mask registers will be used to select the two groups of comparators on the data bus. Mask B will always be used at T1 time, which is the LSET IX - LCALL vector with DB and MB enabled. Mask B remains constant throughout the full pattern test with all address, control and status (41-48) pins enabled.

When a subroutine is entered the T2 cycle is next (since T1 was the calling vector). However, before executing the T2 cycle, Mask A is defined first to enable all address, control and data (3-10) pins. The LSET MA word at the beginning of the subroutine does not add any test time for it is fetched during the 480 nanosecond interval between clock cycles. (In fact, the test period would have to be less than 200 ns for the LSET MA word to require period extension.)

If the byte operation was for an MPU write cycle, the first SET F in the subroutine would enable DB and MA. The DB register defines tester pin 3-10 to not be inputs. Since MA is enabled, the expected MPU response is a function of F and I data for pins 3-10. F is kept at Ø so the Invert register express the expected response. The Invert register was defined at T1 time by the calling LSET IX vector, but not used until T2 in the subroutine when MA was enabled. A normal write cycle for the 8080 takes 3 clock periods and the local memory vectors would be as follows:

```
     LSET MB  1000000000 0000011110 1001111011 1111111111 11111111;
     ENABLE DB,MB
(T1) LSET IX  0000110101 0000100010 0010010011 1111111111 00000100-
                                                          LCALL 023W;

     LSUBR 023W 1;
     LSET MA  1011111111 0000011110 1001111011 1111111111 00000000;
     ENABLE DB,MA:
(T2) SET F    0000000000 0000000010 0110000000 0000000000 00000000;
(T3) SET F    0000000000 0000000110 0110000000 0000000000 00000000-
                                                             LEND;
```

Note, the LSET MB is shown above for illustration purposes. Since MB never changes, it is defined only at the beginning of the test pattern.

For an MPU read cycle, the first cycle (T1) is just like that for a write, with the LSET IX - LCALL vector defining address, data, status and control pins. The subroutine differs in two respects. First, DA is enabled for the T2-T3 cycles to enable tester drivers on data bus pins 3-10. The read subroutine must also account for the T4 and possible T5 cycles. In these cycles, the address and data are in an undefined transitory state, hence, an LSET MA is used to mask these pins. An example of an M1 (instruction fetch) byte operation is as follows:

```
     ENABLE DB,MB;
(T1) LSET IX  0000011111 0000100010 0010101001 1100000000 01000011-
                                                          LCALL 02345R;

     LSUBR 02345R 1;
     LSET MA  1011111111 0000011110 1001111011 1111111111 00000000;
     ENABLE DA,MA;
(T2) SET F    0000000000 0000001110 0110000000 0000000000 00000000;
(T3) SET F    0000000000 0000000110 0110000000 0000000000 00000000;
     LSET MA  0000000000 0000011110 1001000000 0000000000 00000000;
     ENABLE DB;
(T4) SET F    0000000000 0000000110 0110000000 0000000000 00000000;
(T5) SET F    0000000000 0000000110 0110000000 0000000000 00000000-
                                                             LEND;
```

One subtlety with the approach described above is in handling the sync pin 19. If F_{19} is Ø then at T1 time, the LSET IX must have I_{19} = 1 (sync high). Then in the subroutine, F_{19} must be a 1 to cancel I_{19}. That is,

the actual data on pin 19 is $F_{19} \oplus I_{19}$ (exclusive OR). F_{19} must be 1 for all cycles in this subroutine. When the subroutine is exited, the next cycle will be T1 and pin 19 will be high again. Since F_{19} was 1 when leaving the subroutine, then the LSET IX must make $I_{19} = 0$ ($F_{19} \oplus I_{19} = 1 \oplus \emptyset = 1$). Now, the subroutine called by this second LSET IX is entered with $I_{19} = 0$. Therefore, F_{19} must be $\emptyset$ to get a $\emptyset$ on pin 19. Therefore, this second subroutine cannot be the same as the first. Two versions of each subroutine type have been created. They are labled with the first character being O or E. For LSET IX with past $F_{19} = 0$ and $I_{19} = 1$, a subroutine type O is called where $F_{19} = 1$ in this type. For LSET IX with past $F_{19} = 1$ and $I_{19} = 0$, a subroutine type E is called when $F_{19} = 0$ in this type.

There are six basic subroutine types used for 8080 patterns - four for read operations and two for write. The four for read are for 3,4,5 and 10 cycle operations. The 3 cycle type is for second, third bytes of an instruction. The 4 and 5 cycle types are for first byte instruction fetch cycles. The 10 cycle type is for the double add instructions (DAD).

The two write subroutine types are for 3 cycle and 5 cycle operation. Only the XTHL instruction requires the 5 cycle operation.

Each of the six subroutines are duplicated for handling the sync pin, making 12. The interrupt testing also requires special subroutines which have the INT request pin high only on the last cycle of a byte. This, therefore, requires doubling the above 12 subroutines, making a total of 24. These are all short routines and occupy less than 120 words of local memory space.

Wait and hold operations require special treatment. In order not to introduce any "dead" cycles in the pattern, wait and hold tests are put in the main stream of the pattern, e.g. not in subroutines. A read wait test would appear as follows:

```
      ENABLE DB, MB
      LSET IX    ...                    - LCALL
      LSET IX    ...                    - LCALL
      LSET I     0010101100 0000100000 0010010011 1011000100 01000011;
      LSET MA    1000000000 0000011110 0110000100 1111111111 00000000;
 (T1) SET F      0000000000 0000000110 0100000000 0000000000 00000000;
      ENABLE DB,MA
(T2W) SET FC 2   0000000000 0000001100 0101000000 0000000000 00000000;
      ENABLE DB,MB
(T2W) SET FC 9   0000000000 0000001100 0101000000 0000000000 10111100;
(T2W) SET F      0000000000 0000001100 0101000000 0000000000 10111100-
                                                              LCALL E23R
```

In the above example, LSET I, not IX, was used to define address, data, etc. The LSET MA prepares mask A for later use in the first two cycles of the T2W state. The first SET F gives the T1 cycle with MB enabled to monitor the MPU status output. Also this SET F has pin 23 = $\emptyset$ which pulls the ready line low (not ready). The SET FC 2 with MA enabled gives the first two wait cycles. However, MA has masked strobing the data bus response because the MPU data bus is off (DBIN=1) and the

external pullup load times capacitance requires two cycles to get the output pulled up above the S1 sense level. The SET FC 9 enables MB which allows strobing of the data bus (via pins 41-48). Note that the combination of I and E on pins 41-48 gives an effective expected response of all ones. The last SET F calls the appropriate read subroutine which will have Ready high and complete the T2-T3-... steps.

The wait procedure for a write operation is different because the MPU data bus remains active. Here we need only to make the T2 vector use SET FC count with ready low at T1 and T2W.

```
      LSET I    1011101000 0000110000 0010000100 0011000000 00000000;
      LSET MA   1011111111 0000011110 1001111011 1111111111 00000000;
      ENABLE DB,MB;
 (T1) SET F     0000000000 0000000110 0100000000 0000000000 00000000;
      ENABLE MA;
(T2W) SET FC 9  0000000000 0000000000 0101000000 0000000000 00000000;
(T2W) SET F     0000000000 0000000000 0101000000 0000000000 00000000=
                                                        LCALL E23W;
```

The hold routine has to execute the T2,T3 steps of a byte before entering the hold state. Therefore, all steps of a hold test will be in the main line section and no subroutines used.

```
      ENABLE DB,MB;
      LSET I    0011111011 0000100000 0010010000 1100000000 01010010;
 (T1) SET F     0000000000 0010000110 0110000000 0000000000 00000000;
      LSET MA   1011111111 0000011110 1001111011 1111111111 00000000;
      ENABLE DA,MA
 (T2) SET F     0000000000 0010001100 1110000000 0000000000 00000000;
      LSET MA   0000000000 0000001110 1001000000 0000000000 00000000;
 (T3) SET F     0000000000 0010000100 1110000000 0000000000 00000000;
      LSET I    1011111111 0000100000 0010111011 1111111111 00000000;
      ENABLE DB
 (T4) SET F     0000000000 0010000100 1110000000 0000000000 00000000;
      LSET MA   1011111111 0000001110 1001111011 1111111111 00000000;
 (TH) SET FC 9  0000000000 0010000100 1110000000 0000000000 00000000;
 (TH) SET F     0000000000 0000000100 1110000000 0000000000 00000000;
 (TH) SET F     0000000000 0000000100 0110000000 0000000000 00000000;
      LSET IX   ... next byte
```

Hence, the LSET I between T3, T4 sets expected data on all address and data pins to a 1 which are checked during TH cycles.

For a hold after write, the pattern is:

```
     ENABLE DB,MB
     LSET I    1000000100 0000110000 0010000000 1100000010 00000100;
(T1) SET F     0000000000 0010000110 0110000000 0000000000 00000000;
     LSET MA   1011111111 0000011110 1001111011 1111111111 00000000;
     ENABLE MA:
(T2) SET F     0000000000 0010000000 0110000000 0000000000 00000000;
(T3) SET F     0000000000 0010000000 1110000000 0000000000 00000000;
     LSET I    1011111111 0000100000 0010111011 1111111111 00000000;
     LSET MA   0000000000 0000001110 1001000000 0000000000 00000000;
(TH) SET F     0000000000 0010000100 1110000000 0000000000 00000000;
     LSET MA   1011111111 0000001110 1001111011 1111111111 00000000;
(TH) SET FC 9  0000000000 0010000100 1110000000 0000000000 00000000;
(TH) SET F     0000000000 0000000100 1110000000 0000000000 00000000;
(TH) SET F     0000000000 0000000100 0110000000 0000000000 00000000;
     LSET IX   ... next byte
```

In the above procedures, the IMASK mode is being used. IMASK automatically masks comparator outputs on pins which are inputs during that cycle. Therefore, it was not necessary to set MA to zero on MPU read cycles. IMASK has another benefit that this program applies. Since MA and MB are set up to care about output on nearly every clock cycle a problem arises when a timing test is to be made on a particular output which has a time specification other outputs may not meet. This means that other outputs may need to be masked so as not to produce a failure when a certain output pin's response time is being measured. For those pins which are outputs always (not I/O) we have set DA and DB to zero via the long register data bus (SET DA,DB - not LSET). This will leave the K3 relay on the pin electronics card open. Now, if the LSET DA and LSET DB instructions in the first two local memory locations are set to 1 for certain output pins, the IMASK feature will inhibit strobing those pins. They really don't become inputs because of the open K3 relay. This gives an effective "master mask" register for output only pins which eliminates the need to alter all of the LSET MA/MB vectors in local memory.

With the SPM techniques discussed above, a very thorough 8080 diagnostic can be contained within a single local memory load. This single local memory load, using about 80% of a 4096 word memory allows testing of all instructions in a meaningful and thorough sequence with all outputs tested for a.c. response specifications and the necessary set ups for d.c. tests.

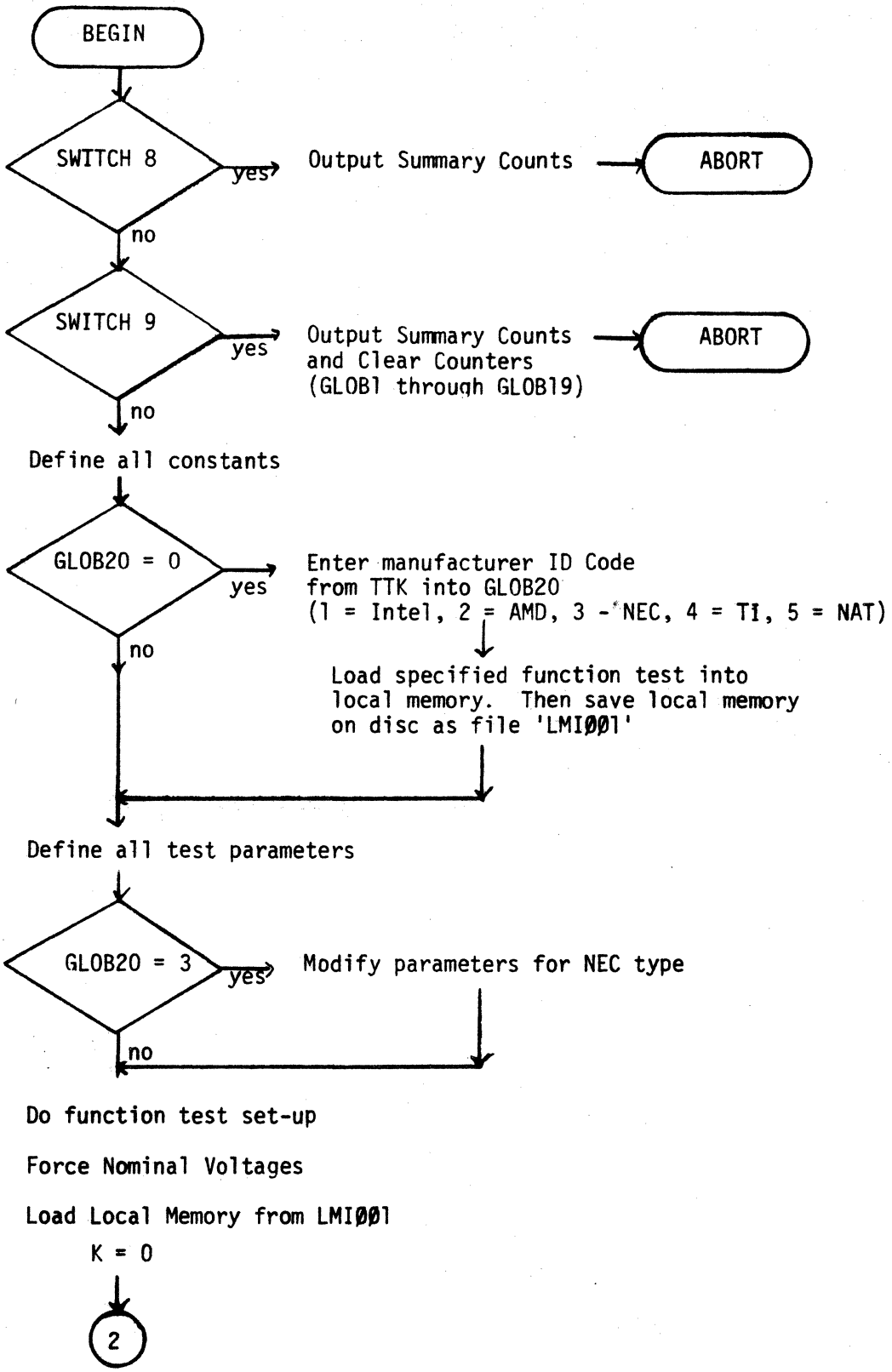
When applying the local memory patterns for d.c. tests, many measurements must be made while the MPU is being cycled in hold or wait loops. This is accomplished in the FACTOR program by substituting SET FC 9 microcode in the sequence processor with a SET FC CONTINUOUS instruction. For example, to do a VOH test on address and data, a STA at address FFFF with A=FF is executed and a wait condition on the write cycle is imposed. The d.c. test program will then modify the SET FC to a continuous type and start the local memory so that the PMU can measure each pin's VOH value. After completing these measurements, the continuous mode is terminated and original SET FC microcode restored in the altered local memory location.

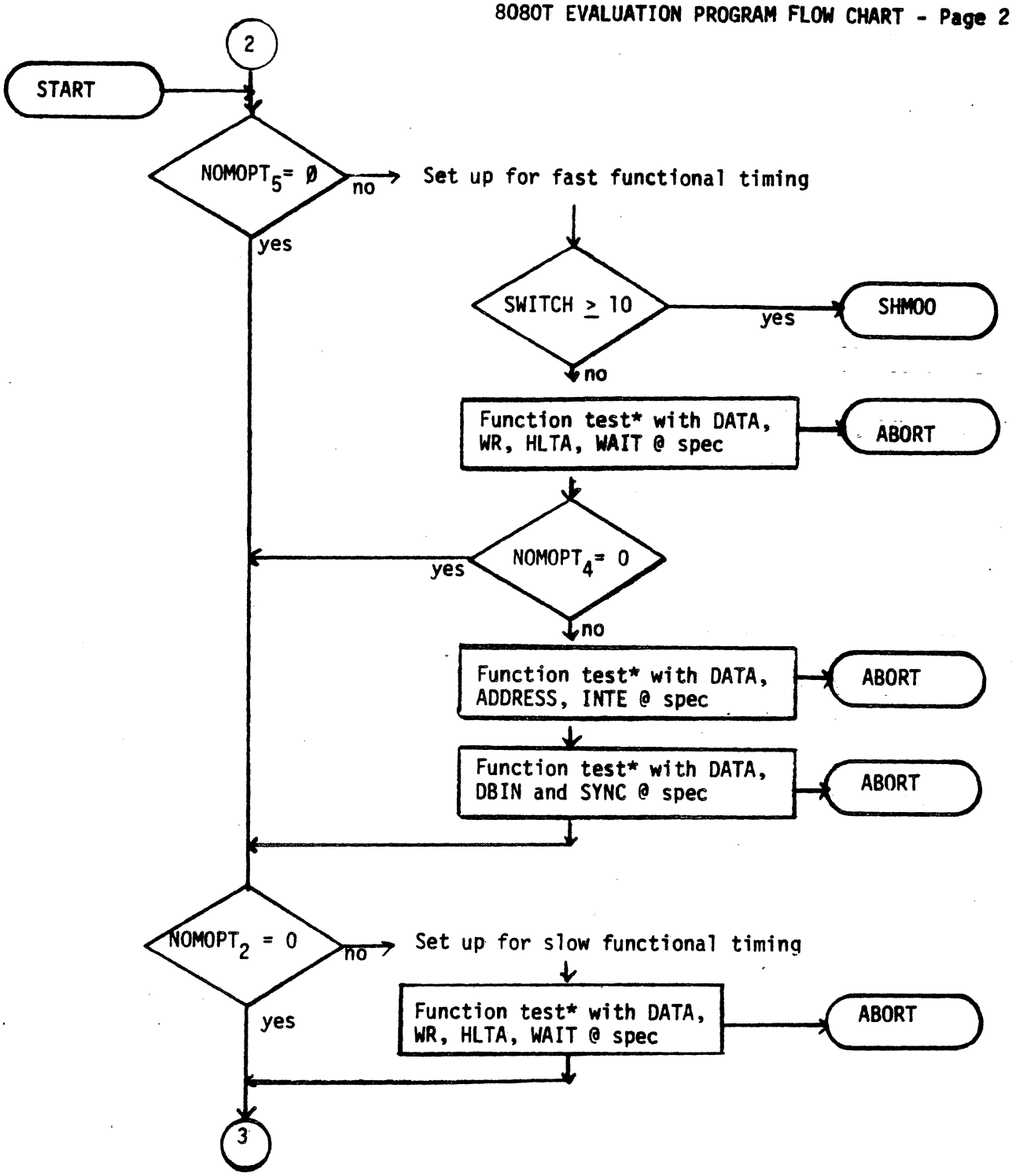
3.161

8080SPM LOCAL MEMORY ALLOCATIONS

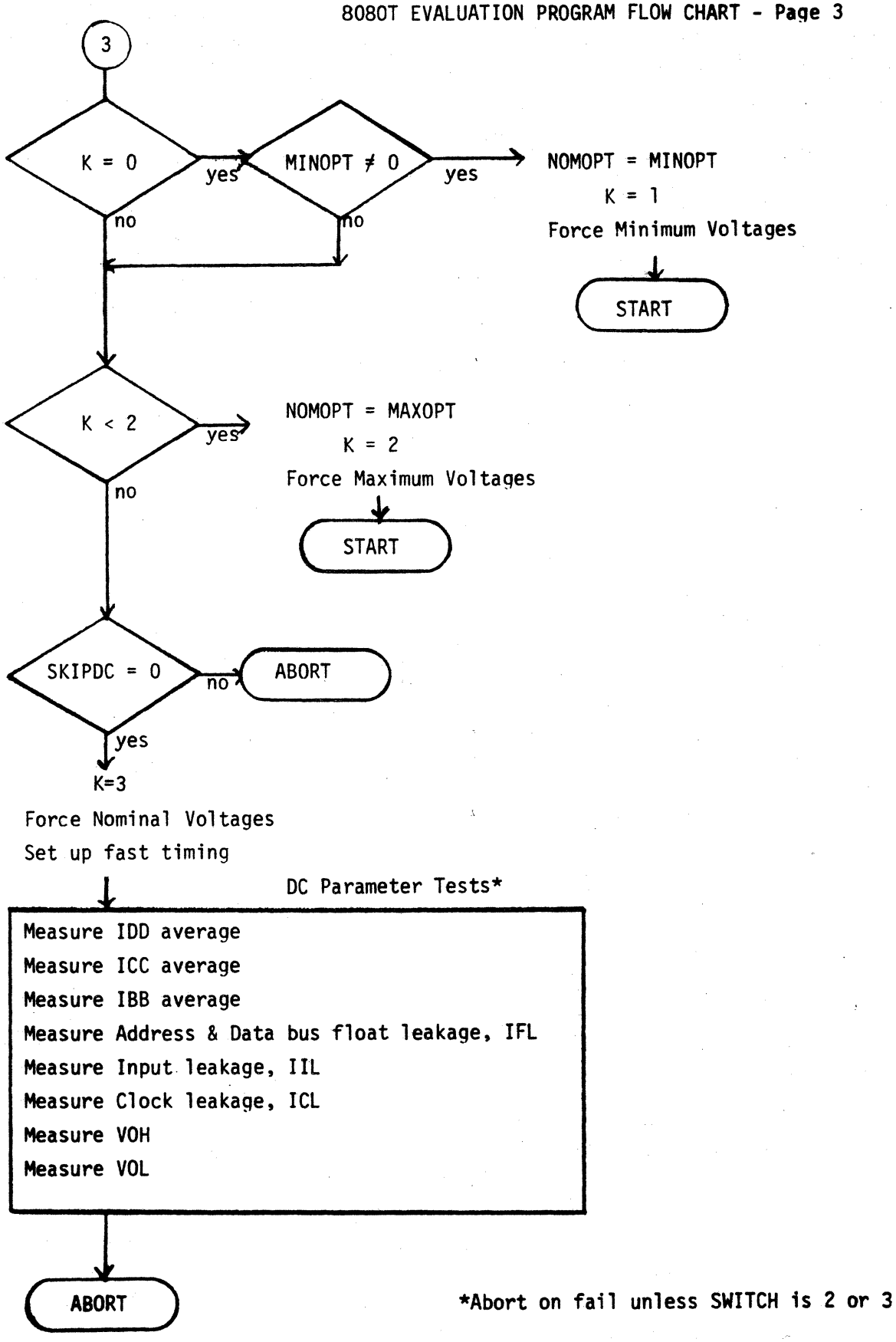
	Location	Function
First Local Memory Page	0	Define DA
	1	Define DB
	2	Clear Mask A
	3	Enable Mask B for address, status, control pins
	4	Set Invert on phase 2 and ready pins
	5	Reset for 3 cycles (MA for don't care)
	6	Two cycles (MA)
	7	LSET-IX for address, status, data, control pins - Call subroutine for remaining cycles of byte.
	8	
	:	:
	n	If last instruction, goto STOP-3 to terminate. If another local memory page is needed, start wait operation and goto MTLOOP for continuous wait.
	n+1	Unused LSET IX data
	:	
	STOP-3	Clear MA
	STOP-2	Clear MB
	STOP-1	Clear I except phase 2 and ready pins
(MEMMAX-120)	STOP	Clear F except WO and phase 1 pins. Major loop ends here.
	02345R	5 cycle read subroutine for SYNC=1 in I register
	:	:
	E2345R	5 cycle read subroutine for SYNC=Ø in I register
	:	:
		Other subroutines for different byte cycles for read and write
	:	:
	I2345R	Like 02345R but with INT request on last cycle
	:	:
	A2345R	Like E2345R but with INT request on last cycle
	:	:
	WTLOOP	Continuous loop with not ready (T2W state)
(4095 MAX)	MEMMAX	Not ready SET F with goto location 37_8.

Second Local Memory Page	0	
	:	Reset like first page
	6	
	7	LXI SP, POP H, POP D, POP B, POP PSW
	:	EI/DI and RET to initialize MPU to last condition
	:	of previous page. This area used for generation or
	31	debug loops.
	32	Same instruction as last on previous page with not
	:	ready invoked.
	37	Last not ready (T2W) cycle. Entry point from previous
	:	page.
	:	Remainder same as first page.


BEGIN
SWITCH 8
yes
Output Summary Counts
ABORT
no
SWITCH 9
yes
Output Summary Counts
and Clear Counters
(GLOB1 through GLOB19)
ABORT
no
Define all constants
GLOB20 = 0
yes
Enter manufacturer ID Code
from TTK into GLOB20
(1 = Intel, 2 = AMD, 3 = NEC, 4 = TI, 5 = NAT)
no
Load specified function test into
local memory. Then save local memory
on disc as file 'LMIØØ1'
Define all test parameters
GLOB20 = 3
yes
Modify parameters for NEC type
no
Do function test set-up
Force Nominal Voltages
Load Local Memory from LMIØØ1
K = 0
2

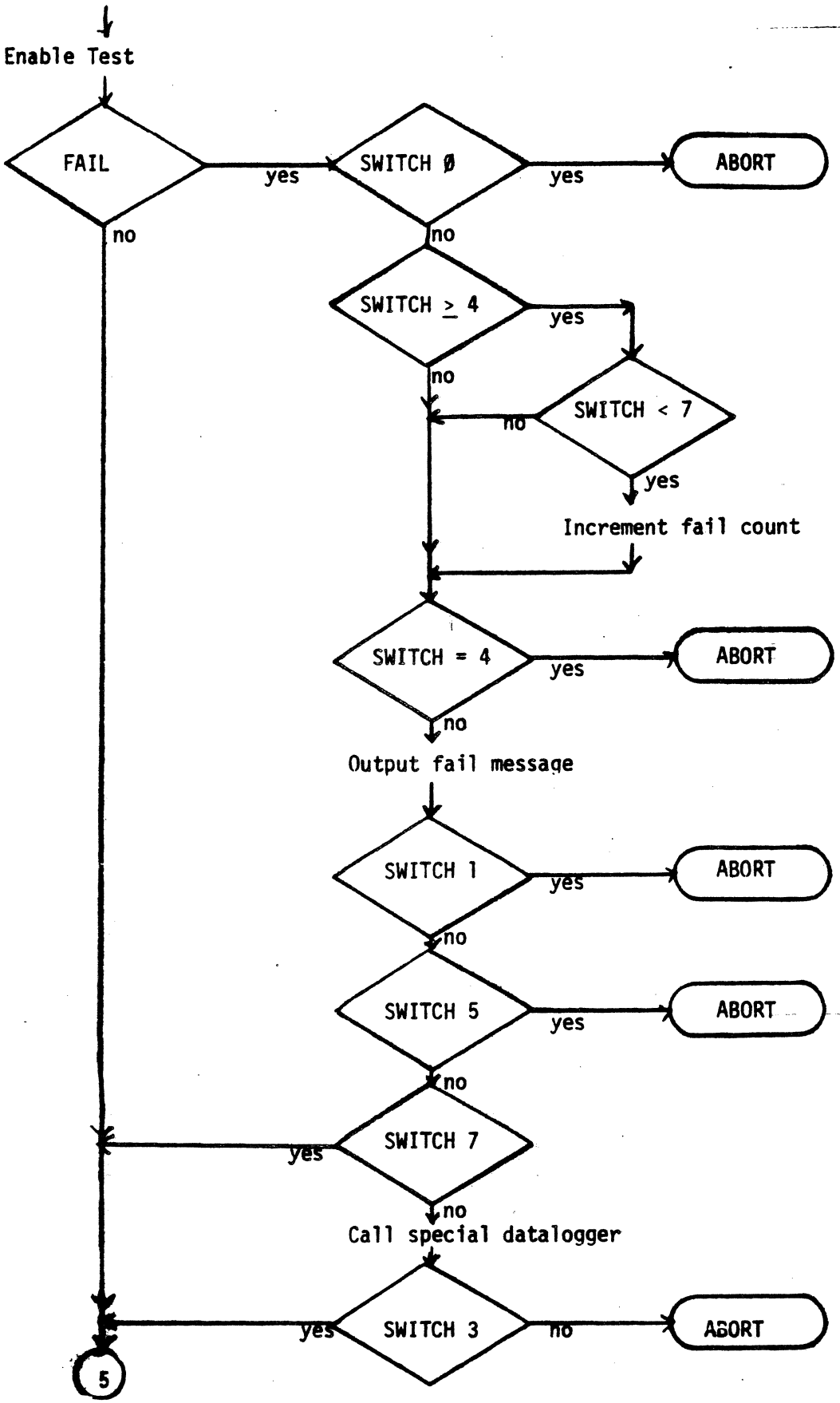


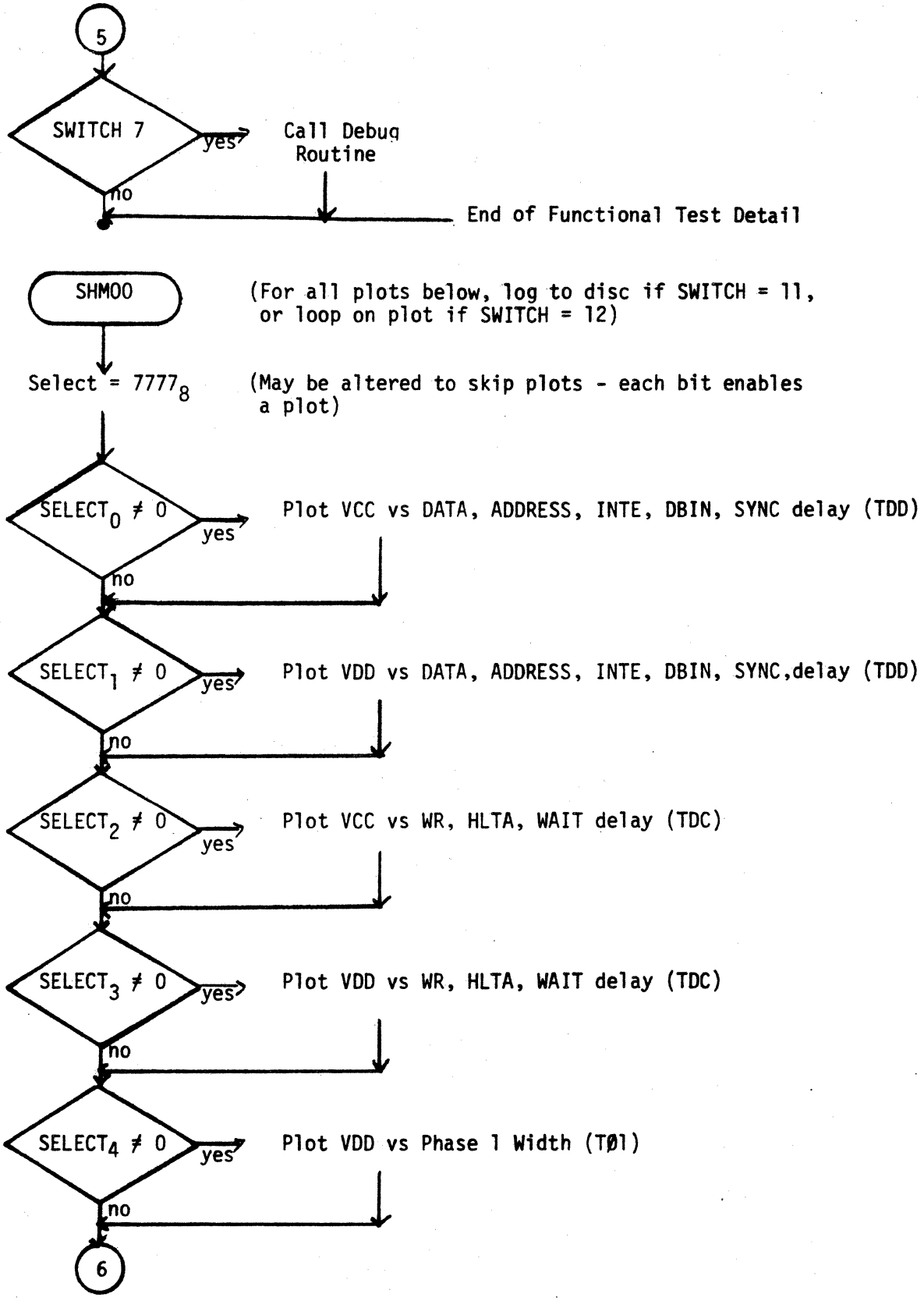
*See function test flow detail on page 4 of this program flow chart.

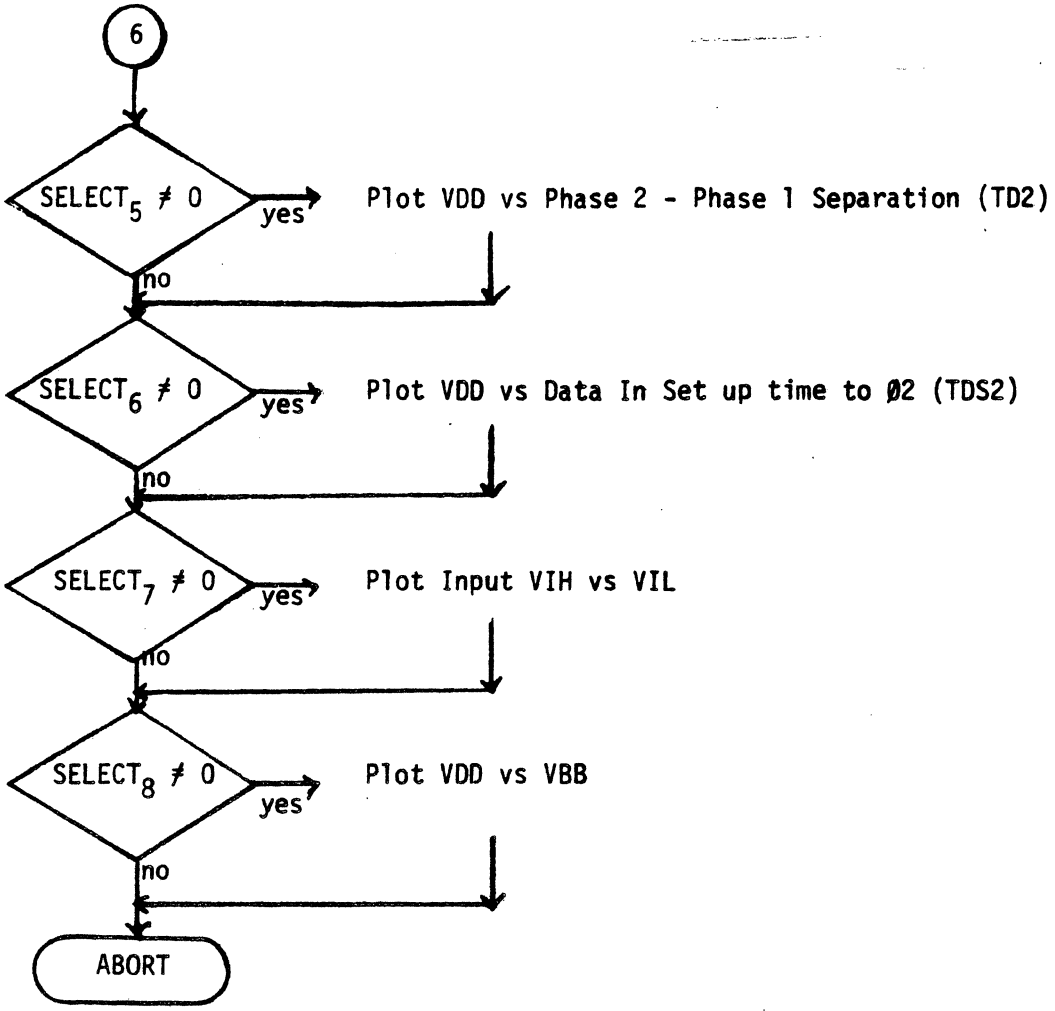


*Abort on fail unless SWITCH is 2 or 3

Function Test Detail




5
SWITCH 7
yes
Call Debug Routine
no
End of Functional Test Detail
SHM00
(For all plots below, log to disc if SWITCH = 11, or loop on plot if SWITCH = 12)
Select = 7777₈
(May be altered to skip plots - each bit enables a plot)
SELECT₀ ≠ 0
yes
Plot VCC vs DATA, ADDRESS, INTE, DBIN, SYNC delay (TDD)
no
SELECT₁ ≠ 0
yes
Plot VDD vs DATA, ADDRESS, INTE, DBIN, SYNC,delay (TDD)
no
SELECT₂ ≠ 0
yes
Plot VCC vs WR, HLTA, WAIT delay (TDC)
no
SELECT₃ ≠ 0
yes
Plot VDD vs WR, HLTA, WAIT delay (TDC)
no
SELECT₄ ≠ 0
yes
Plot VDD vs Phase 1 Width (TØ1)
no
6


6
SELECT5 ≠ 0
yes
Plot VDD vs Phase 2 - Phase 1 Separation (TD2)
no
SELECT6 ≠ 0
yes
Plot VDD vs Data In Set up time to Ø2 (TDS2)
no
SELECT7 ≠ 0
yes
Plot Input VIH vs VIL
no
SELECT8 ≠ 0
yes
Plot VDD vs VBB
no
ABORT

3.18 Timing Description for 8080T Test Program

'8080T' performs function tests under two basic timing conditions - fast and slow. The fast test uses a cycle time of TCYC = 480 nanoseconds for the 8080A, and the slow test is at TCYC = 2 microseconds. For both these conditions, all other timing relationships are held constant, e.g. only TD2, the phase 2 to phase 1 non overlap interval changing. A nominal rise time (TR) parameter of 10 nanoseconds is used.

The subroutine SETTIME is called after defining TCYC and all tester timing generator delay and width values computed. Note the variable TOFF. This describes the offset of the phase 2 rising edge relative to the tester TØ time. TØ is the beginning of a tester period and is the time that I/O pins may change from in to out or out to in. TOFF is approximately the TDF time where the 8080 outputs turn off and tester drivers turn on to avoid conflict.

The first function test with fast timing uses strobe timing generator seven to sample the DATA, ADDRESS, DBIN, INTE and SYNC pins. The timing parameter, TDD, is used because it is the greater of the values TDD, TAA, TDF, TIE or TDC. In effect, only the DATA bus is being checked for its minimum access time here and the other pins are monitored in the interest of science. Timing generator eight monitors the three outputs (WR, HLDA, WAIT) whose delay time is relative to phase 1 and are specified to be valid at TDC after phase 1 rising edge.

Another fast function test is made with TG8 looking at ADDRESS and INTE, testing for a response within TDA of phase 2 rise (TIE = TDA for 8080A). (See local memory action description).

A third fast function test is used to verify the DBIN and SYNC timing, TDC relative to phase 2.

The slow function test is performed once with the same conditions as the first fast test, e.g. DATA, ADDRESS, DBIN, INTE and SYNC strobed by TG7 TDD after Ø2 and WR, HLDA and WAIT strobed by TG8 TDC after Ø1.

Several SHMOO plot exercises are included in 8080T to display critical timing parameters versus operating voltage levels. The ones currently included are:

VCC vs TDD
VDD vs TDD
VCC vs TDC
VDD vs TDC
VDD vs TØ1
VDD vs TD2
VDD vs TDS2
VIH vs VIL
VDD vs VBB

3.19 8080 Functional Diagnostic Description

The diagnostic, 8080D, is designed to exercise all 243 valid instructions with a reasonable degree of intelligence to validate each instruction's operation. 1,377 instruction tests are performed by 8080D, resulting in about 11,000 test cycles. Some op-codes are used only once, but these are types with internal register arguments. Each type of arithmetic operation is performed many times in order to check effects on flag bits (carry, zero, parity, etc.) and each test of a particular arithmetic operation many reference a different internal register so as to combine the verification of an op-code and ALU.

The initial phase of the diagnostic is designed to test the state controller. Instructions requiring all combinations of 3-4-5 or 10 cycle byte operations are used with various tests on external control lines - reset, ready, hold and interrupt. This section is also used for setting up the MPU for d.c. parametric tests.

Beginning at REGT (2FØØ) is a test for the internal memory file. This test is like a spiral pattern for a RAM. A 1 is loaded into the A register. Then the subroutine DIAG shifts the bit left and deposits it into register B. Then another shift and move to register C and so on until each register is loaded with a unique word (diagonal). The registers are then examined in the subroutine LOOK. This process is repeated, moving the diagonal to the left each time so bits in each register are tested for uniqueness. The complement of the spiral (shifting diagonal) is then performed.

Next, beginning at MOVA (3Ø1F), all register to register move operations are tested. Note that each register has unique values to validate each move.

The accumulator group instructions are tested next, beginning with ADD at 31Ø2. As mentioned above, the various arguments to be added to check this function thoroughly can be put into internal registers so that all register references with ADD are tested. Flags are tested by performing conditional jump tests. A failure in a flag will cause a halt, thus causing a failure. The order of these tests are ADD, ADC, SUB, SBB, AND, CMP, XOR and OR.

The I/O instructions are tested at 334Ø. A typical sequence is to load A with FF and then IN all zeroes and test A for all zeroes.

Rotation instruction testing begins at 338Ø with RLC operations. Starting with 80 in A, the first RLC is performed and carry tested. Now with 1 in A, the RLC and test for carry = Ø is made eight times until carry goes high. For each step, A is examined for correct content. Then RRC, RAL, RAR are performed in similar fashion.

At 33CØ the increment, decrement register checks are made, where each register has a unique value.

Jumps, calls and returns are then exercised beginning at BRANCH (34ØØ). Starting with A = 0 and carry cleared, all conditional jumps, calls

```
                        ********************************************
                        ********************************************
                        **                                        **
                        **                                        **
                        **  COPYRIGHT (C) FAIRCHILD CAMERA AND    **
                        **  INSTRUMENT CORPORATION 1977.  ALL     **
                        **  RIGHTS RESERVED.  NO PART OF THIS     **
                        **  PROGRAM MAY BE PHOTOCOPIED, REPRO-    **
                        **  DUCED OR TRANSLATED TO ANOTHER        **
                        **  PROGRAM LANGUAGE WITHOUT THE PRIOR    **
                        **  WRITTEN CONSENT OF FAIRCHILD CAMERA   **
                        **  AND INSTRUMENT CORPORATION.           **
                        **                                        **
                        **                                        **
                        **                                        **
                        ********************************************
                        ********************************************
                         *8080 MICROPROCESSOR DIAGNOSTIC PROGRAM
                         *TRI-STATE AND DC SETUP TESTS
0000 1C3 45 00          INT0    JMP LAB0
0008 00                 INT1    NOP             INTERRUPT SUBROUTINES
     FB                         EI
     3C9                        RET             3RD INTERRUPT REQ.
0010 300                INT2    NOP         CHECK INT.  DISABLE 4TH REQ.
     00                         NOP
     FB                         EI
     00                         NOP
     C9                         RET
0018 00                 INT3    NOP
     FB                         EI
     3C9                        RET             5TH REQUEST
0020 00                 INT4    NOP
     FB                         EI
     3C9                        RET             6TH REQUEST
0028 00                 INT5    NOP
     FB                         EI
     3C9                        RET             7TH REQUEST
0030 00                 INT6    NOP
     FB                         EI
     C9                         RET
0038 00                 INT7    NOP
     FB                         EI
     C9                         RET
0045 3E 00              LAB0    MVI A,0         0 INTO A
     32 00 00                   STA  0000       OUTPUT ALL ZERO
     3E FF                      MVI A,FF
     32 FF FF                   STA  FFFF       OUTPUT ALL HIGH
     2F3                        DI              WITH HOLD
0050 21 00 00                   LXI H 0,0       RESTORE LOCATION 0
     36 00                      MVI M,0         NOP
     2C                         INR L
     36 FB                      MVI M,FB        EI
     2C                         INR L
     36 C9                      MVI M,C9        RET
     31 F6 FF                   LXI SP FFF6     INITIALIZE
     E1                         POP H
     D1                         POP D
0060 C1                         POP B
     F1                         POP PSW
     FB                         EI
     100                        NOP               READ WAIT TEST
     300                        NOP             INTERRUPT REQUEST
     300                        NOP             2ND INTERRUPT REQUEST
     178                        MOV A,B         (5) READ WAIT TEST
     77                         MOV  M,A        (7)
     36 78                      MVI  M,78       (10)
     187                        ADD  A          (4) READ WAIT TEST
     CD 100 01                  CALL LAB1       (17) READ WAIT TEST
     C3 00 102                  JMP  LAB2       (10) READ WAIT TEST
0100 AF                 LAB1    XRA  A          (4)
     DC 04 01                   CC   *+1        (11)
     D8                         RC              (5)
     C9                         RET             (10)
0200 D4 00 03           LAB2    CNC  LAB3       (17)
     D3 00                      OUT  00         (10)
```

```
      DB 00                     IN   00      (10)
      31 66 44                  LXI  SP,4466
      F5                        PUSH PSW          TEST HOLD ON WRITE
      E5                        PUSH H            TEST HOLD ON WRITE
      C5                        PUSH B            TEST HOLD ON WRITE
      31 FF 7F                  LXI  SP,7FFF  (10)
      D5                        PUSH D       (11)
      32 2AA 255                STA          (13) HOLD
      22 55 AA                  SHLD         (16)
      E3                        XTHL         (18)
      FB                        EI
     376                        HLT           WITH INTR.  8TH REQUEST
      00                        NOP
      F3                        DI
      3C3 00 2F                  JMP REGT      9TH INT.  REQUEST.
0300  D0                LAB3    RNC          (11)
0708  100                                     WRITE WAIT TEST
4465  200                                     WRITE HOLD TEST
4461  200                                     WRITE HOLD TEST
4460  200                                     WRITE HOLD TEST
FFF6  08                                     INITIAL L REG
      07                                              H
      06                                              E
      05                                              D
      04                                              C
      03                                              B
      02                                              PSW
      01                                              A
      66                                              PCL
FFFF  100                                             PCH
                        *INTERNAL REGISTER TEST
2F00  3E 01             REGT    MVI A,1       SPIRAL PATTERN TEST
      32 21 2F                  STA TEMP
      CD 22 2F                  CALL DIAG     WRITE DIAGONAL
      CD B0 33                  CALL LOOK     READ IT BACK
      07                        RLC           SHIFT DIAGONAL
      D2 02 2F                  JNC REGT+1    NEXT PASS
      EE FF                     XRI FF        COMPLEMENT PATTERN
2F11  32 21 2F          REGT1   STA TEMP
      CD 22 2F                  CALL DIAG     WRITE COMPLEMENT DIAG
      CD B0 33                  CALL LOOK     READ IT BACK
      07                        RLC           SHIFT DIAGONAL
      DA 11 2F                  JC  REGT1     NEXT PASS
      C3 1F 30                  JMP MOVA
2F21  00                TEMP    NOP
2F22  07                DIAG    RLC
      47                        MOV B,A
      07                        RLC
      4F                        MOV C,A
      07                        RLC
      57                        MOV D,A
      07                        RLC
      5F                        MOV E,A
      07                        RLC
      67                        MOV H,A
      07                        RLC
      6F                        MOV L,A
      3A 21 2F                  LDA TEMP
      C9                        RET
                        *TEST ALL MOVE INSTRUCTIONS
3000  3E 01             LOAD1   MVI  A,1
      06 02                     MVI  B,2
      0E 04                     MVI  C,4
      16 08                     MVI  D,8
      1E 10                     MVI  E,10
      26 20                     MVI  H,20
      2E 40                     MVI  L,40
      36 80                     MVI  M,80
3010  C9                        RET
                        *MOVES TO A REGISTER
301F  CD 00 30          MOVA    CALL LOAD1
      78                        MOV  A,B
      7F                        MOV  A,A
      77                        MOV  M,A
      79                        MOV  A,C
      77                        MOV  M,A
      7A                        MOV  A,D
      77                        MOV  M,A
      7B                        MOV  A,E
      77                        MOV  M,A
      7C                        MOV  A,H
      77                        MOV  M,A
      7D                        MOV  A,L
      77                        MOV  M,A
```

```
      AF                        XRA   A
      7E                        MOV   A,M
      77                        MOV   M,A
      3E 01                     MVI   A,1
                        *MOVES TO B REGISTER
3034  47                        MOV   B,A
      70                        MOV   M,B
      40                        MOV   B,B
      41                        MOV   B,C
      70                        MOV   M,B
      42                        MOV   B,D
      70                        MOV   M,B
      43                        MOV   B,E
      70                        MOV   M,B
      44                        MOV   B,H
      70                        MOV   M,B
      45                        MOV   B,L
      70                        MOV   M,B
      06 00                     MVI   B,0
      46                        MOV   B,M
      70                        MOV   M,B
      06 02                     MVI   B,2
                        *MOVES TO C REGISTER
3047  4F                        MOV   C,A
      71                        MOV   M,C
      48                        MOV   C,B
      71                        MOV   M,C
      49                        MOV   C,C
      4A                        MOV   C,D
      71                        MOV   M,C
      4B                        MOV   C,E
      71                        MOV   M,C
      4C                        MOV   C,H
      71                        MOV   M,C
      4D                        MOV   C,L
      71                        MOV   M,C
      0E 00                     MVI   C,0
      4E                        MOV   C,M
      71                        MOV   M,C
      0E 04                     MVI   C,4
                        *MOVES TO D REGISTER
305A  57                        MOV   D,A
      72                        MOV   M,D
      50                        MOV   D,B
      72                        MOV   M,D
      51                        MOV   D,C
      72                        MOV   M,D
      52                        MOV   D,D
      53                        MOV   D,E
      72                        MOV   M,D
      54                        MOV   D,H
      72                        MOV   M,D
      55                        MOV   D,L
      72                        MOV   M,D
      16 00                     MVI   D,0
      56                        MOV   D,M
      72                        MOV   M,D
      16 08                     MVI   D,8
                        *MOVES TO E REGISTER
306D  5F                        MOV   E,A
      73                        MOV   M,E
      58                        MOV   E,B
      73                        MOV   M,E
      59                        MOV   E,C
      73                        MOV   M,E
      5A                        MOV   E,D
      73                        MOV   M,E
      5B                        MOV   E,E
      5C                        MOV   E,H
      73                        MOV   M,E
      5D                        MOV   E,L
      73                        MOV   M,E
      1E 00                     MVI   E,0
      5E                        MOV   E,M
      73                        MOV   M,E
      1E 10                     MVI   E,10
                        *MOVES TO H REGISTER
3080  67                        MOV   H,A
      74                        MOV   M,H
      60                        MOV   H,B
      74                        MOV   M,H
      61                        MOV   H,C
      74                        MOV   M,H
      62                        MOV   H,D
```

```
      74                    MOV   M,H
      63                    MOV   H,E
      74                    MOV   M,H
      64                    MOV   H,H
      65                    MOV   H,L
      74                    MOV   M,H
      26 00                 MVI   H,0
      66                    MOV   H,M
      74                    MOV   M,H
      26 20                 MVI   H,20
                     *MOVES TO L REGISTER
3093  6F                    MOV   L,A
      75                    MOV   M,L
      68                    MOV   L,B
      75                    MOV   M,L
      69                    MOV   L,C
      75                    MOV   M,L
      6A                    MOV   L,D
      75                    MOV   M,L
      6B                    MOV   L,E
      75                    MOV   M,L
      6C                    MOV   L,H
      75                    MOV   M,L
      6D                    MOV   L,L
      2E 00                 MVI   L,0
      6E                    MOV   L,M
      75                    MOV   M,L
      2E 40                 MOV   L,40
      C3 00 31              JMP   AGI
                     *CHECK ACCUMULATOR GROUP INSTRUCTIONS
3100  36 80       AGI       MVI   M,80
                     *ADD
3102  87                    ADD   A       1+1=2
      77                    MOV   M,A
      C6 FF                 ADI   FF      2+FF=1+CARRY
      77                    MOV   M,A
      DA 0B 31              JC    *+2     CARRY SET?
      76                    HLT           NO-ERROR
310B  B8                    CMP   B       1 LT 2, SET CARRY
      80                    ADD   B       1+2=3
      77                    MOV   M,A
      D2 12 31              JNC   *+2     CARRY CLEAR?
      76                    HLT           NO-ERROR
3112  B9                    CMP   C       3 LT 4, SET CARRY
      81                    ADD   C       3+4=7
      77                    MOV   M,A
      D2 19 31              JNC   *+2     CARRY CLEAR?
      76                    HLT
3119  BA                    CMP   D       7 LT 8, SET CARRY
      82                    ADD   D       7+8=F
      77                    MOV   M,A
      D2 20 31              JNC   *+2
      76                    HLT
3120  BB                    CMP   E       F LT 10, SET CARRY
      83                    ADD   E       F+10=1F
      77                    MOV   M,A
      D2 27 31              JNC   *+2
      76                    HLT
3127  BC                    CMP   H       1F LT 20, SET CARRY
      84                    ADD   H       1F+20=3F
      77                    MOV   M,A
      D2 2E 31              JNC   *+2
      76                    HLT
312E  BD                    CMP   L       3F LT 40, SET CARRY
      85                    ADD   L       3F+40=7F
      77                    MOV   M,A
      D2 35 31              JNC   *+2
      76                    HLT
3135  36 80                 MVI   M,80
      BE                    CMP   M       7F LT 80, SET CARRY
      86                    ADD   M       7F+80=FF
      77                    MOV   M,A
      D2 3E 31              JNC   *+2
      76                    HLT
                     *ADC
313E  3E 01                 MVI   A,1
      B8                    CMP   B       1 LT 2, SET CARRY
      8F                    ADC   A       1+1+1=3
      77                    MOV   M,A
      D2 47 31              JNC   *+2
      76                    HLT
3147  B9                    CMP   C       3 LT 4, SET CARRY
      88                    ADC   B       1+3+2=6
      77                    MOV   M,A
```

```
        D2 4E 31                JNC   *+2
        76                      HLT
314E    BA                      CMP   D       6 LT 8, SET CARRY
        89                      ADC   C       1+6+4=B
        77                      MOV   M,A
        D2 55 31                JNC   *+2
        76                      HLT
3155    BB                      CMP   E       B LT 10, SET CARRY
        8A                      ADC   D       1+B+8=14
        77                      MOV   M,A
        D2 5C 31                JNC   *+2
        76                      HLT
315C    BC                      CMP   H       14 LT 20, SET CARRY
        8B                      ADC   E       1+14+10=25
        77                      MOV   M,A
        D2 63 31                JNC   *+2
        76                      HLT
3163    BD                      CMP   L       25 LT 40, SET CARRY
        8C                      ADC   H       1+25+20=46
        77                      MOV   M,A
        D2 6A 31                JNC   *+2
        76                      HLT
316A    36 80                   MVI   M,80
        BE                      CMP   M       46 LT 80, SET CARRY
        8D                      ADC   L       1+46+40=87
        77                      MOV   M,A
        D2 73 31                JNC   *+2
        76                      HLT
3173    36 80                   MVI   M,80
        8E                      ADC   M       87+80=7+CARRY
        77                      MOV   M,A
        CE F8                   ACI   F8      1+7+F8=0
        77                      MOV   M,A
        C3 80 31                JMP   SUB

                        *SUB
3180    3E 01           SUB     MVI   A,1
        B8                      CMP   B       1 LT 2, SET CARRY
        97                      SUB   A       1-1=0
        77                      MOV   M,A
        CA 89 31                JZ    *+2
        76                      HLT
3189    D2 8D 31                JNC   *+2
        76                      HLT
318D    B8                      CMP   B       0 LT 2, SET CARRY
        90                      SUB   B       0-2=FE
        77                      MOV   M,A
        DA 94 31                JC    *+2
        76                      HLT
3194    FA 98 31                JM    *+2
        76                      HLT
3198    91                      SUB   C       FE-4=FA
        77                      MOV   M,A
        D2 9E 31                JNC   *+2
        76                      HLT
319E    FE FF                   CPI   FF      FA LT FF, SET CARRY
        92                      SUB   D       FA-8=F2
        77                      MOV   M,A
        D2 A6 31                JNC   *+2
        76                      HLT
31A6    FE FF                   CPI   FF      F2 LT FF, SET CARRY
        93                      SUB   E       F2-10=E2
        77                      MOV   M,A
        D2 AE 31                JNC   *+2
        76                      HLT
31AE    FE FF                   CPI   FF      E2 LT FF, SET CARRY
        94                      SUB   H       E2-20=C2
        77                      MOV   M,A
        D2 B6 31                JNC   *+2
        76                      HLT
31B6    FE FF                   CPI   FF      C2 LT FF, SET CARRY
        95                      SUB   L       C2-40=82
        77                      MOV   M,A
        D2 BE 31                JNC   *+2
        76                      HLT
31BE    36 80                   MVI   M,80
        FE FF                   CPI   FF      82 LT FF, SET CARRY
        96                      SUB   M       82-80=2
        77                      MOV   M,A
        D2 C8 31                JNC   *+2
        76                      HLT
31C8    F2 CC 31                JP    *+2
        76                      HLT
31CC    D6 FF                   SUI   FF      2-FF=3
        77                      MOV   M,A
```

```
                DA D4 31                JC    *+2
                76                      HLT
31D4 C3 DF 31                           JMP   SBB
                                *SBB
31DF AF                         XRA   A
31E0 3E 01      SBB             MVI   A, 1
                9F                      SBB   A          1-1=0
                CC E7 31                CZ    *+2
                76                      HLT
31E7 DE 01                              SBI   1          0-1=FF+BORROW
                DC ED 31                CC    *+2
                76                      HLT
31ED 98                                 SBB   B          FF-2-1=FC
                77                      MOV   M, A
                D4 F3 31                CNC   *+2
                76                      HLT
31F3 FE FF                              CPI   FF         FC LT FF, SET CARRY
                99                      SBB   C          FC-4-1=F7
                77                      MOV   M, A
                D4 FB 31                CNC   *+2
                76                      HLT
31FB FE FF                              CPI   FF         SET CARRY
                9A                      SBB   D          F7-8-1=EE
                77                      MOV   M, A
                D4 03 32                CNC   *+2
                76                      HLT
3203 FE FF                              CPI   FF         SET CARRY
                9B                      SBB   E          EE-10-1=DD
                77                      MOV   M, A
                D4 0B 32                CNC   *+2
                76                      HLT
320B FE FF                              CPI   FF         SET CARRY
                9C                      SBB   H          DD-20-1=BC
                77                      MOV   M, A
                D4 13 32                CNC   *+2
                76                      HLT
3213 FE FF                              CPI   FF         SET CARRY
                9D                      SBB   L          BC-40-1=7B
                77                      MOV   M, A
                D4 1B 32                CNC   *+2
                76                      HLT
321B 36 80                              MVI   M, 80
                FE FF                   CPI   FF         SET CARRY
                9E                      SBB   M          7B-1-80=FA+BORROW
                77                      MOV   M, A
                DC 50 32                CC    AND
                76                      HLT
                                *AND
3230 3E FF      LOAD2           MVI   A, FF
                06 FE                   MVI   B, FE
                0E FD                   MVI   C, FD
                16 FB                   MVI   D, FB
                1E F7                   MVI   E, F7
                26 EF                   MVI   H, EF
                2E DF                   MVI   L, DF
                36 BF                   MVI   M, BF
3240 C9                                 RET
3242 CA 46 32   CHECK1          JZ    *+2
                76                      HLT
3246 3E FF                              MVI   A, FF
3248 C9                                 RET
3250 CD 30 32   AND             CALL  LOAD2
                A7                      ANA   A
                BF                      CMP   A
                CD 42 32                CALL  CHECK1
                A0                      ANA   B
                B8                      CMP   B
                CD 42 32                CALL  CHECK1
                A1                      ANA   C
                B9                      CMP   C
                CD 42 32                CALL  CHECK1
                A2                      AND   D
                BA                      CMP   D
                CD 42 32                CALL  CHECK1
                A3                      ANA   E
                BB                      CMP   E
                CD 42 32                CALL  CHECK1
                A4                      ANA   H
                BC                      CMP   H
                CD 42 32                CALL  CHECK1
                A5                      ANA   L
                BD                      CMP   L
                CD 42 32                CALL  CHECK1
                A6                      ANA   M
```

```
                BE                      CMP   M
                CD 42 32                CALL   CHECK1
                E6 00                   ANI   0
                CA A0 32                JZ     XOR
                76                      HLT
3290            AF              CLEAR   XRA   A
                47                      MOV   B,A
                48                      MOV   C,B
                51                      MOV   D,C
                5A                      MOV   E,D
                63                      MOV   H,E
                6C                      MOV   L,H
                77                      MOV   M,A
                70                      MOV   M,B
                71                      MOV   M,C
                72                      MOV   M,D
                73                      MOV   M,E
                74                      MOV   M,H
                75                      MOV   M,L
329E            C9                      RET
                              *XOR
32A0            CD 90 32        XOR     CALL  CLEAR
                3E FF                   MVI   A,FF
                06 55                   MVI   B,55
                0E AA                   MVI   C,AA
                A8                      XRA   B
                77                      MOV   M,A
                A9                      XRA   C
                77                      MOV   M,A
                47                      MOV   B,A
                3E FF                   MVI   A,FF
32B0            0E 55                   MVI   C,55
                16 AA                   MVI   D,AA
                A9                      XRA   C
                77                      MOV   M,A
                AA                      XRA   D
                77                      MOV   M,A
                4F                      MOV   C,A
                3E FF                   MVI   A,FF
                16 55                   MVI   D,55
                1E AA                   MVI   E,55
                AA                      XRA   D
32C0            77                      MOV   M,A
                AB                      XRA   E
                77                      MOV   M,A
                57                      MOV   D,A
                3E FF                   MVI   A,FF
                1E 55                   MVI   E,55
                26 AA                   MVI   H,AA
                AB                      XRA   E
                77                      MOV   M,A
                AC                      XRA   H
                77                      MOV   M,A
                5F                      MOV   E,A
                3E FF                   MVI   A,FF
32D1            26 55                   MVI   H,55
                2E AA                   MVI   L,AA
                AC                      XRA   H
                77                      MOV   M,A
                AD                      XRA   L
                77                      MOV   M,A
                26 20                   MVI   H,20
                3E FF                   MVI   A,FF
                2E 55                   MVI   L,55
                36 AA                   MVI   M,AA
32E1            AD                      XRA   L
                BE                      CMP   M
                CA E7 32                JZ    *+2
                76                      HLT
32E7            AE                      XRA   M
                CA EC 32                JZ    *+2
                76                      HLT
32EC            3E FF                   MVI   A,FF
                EE 55                   XRI   55
                77                      MOV   M,A
                EE AA                   XRI   AA
                CA 00 33                JZ    OR
                              *OR
3300            CD 00 30        OR      CALL  LOAD1
                B7                      ORA   A
                77                      MOV   M,A
                B0                      ORA   B
                77                      MOV   M,A
                B1                      ORA   C
```

```
                77                      MOV   M,A
                B2                      ORA   D
                77                      MOV   M,A
                B3                      ORA   E
                77                      MOV   M,A
                B4                      ORA   H
                77                      MOV   M,A
                B5                      ORA   L
3310            77                      MOV   M,A
                36 80                   MVI   M,80
                B6                      ORA   M
                77                      MOV   M,A
                36 80                   MVI   M,80
                AE                      XRA   M
                77                      MOV   M,A
                AD                      XRA   L
                77                      MOV   M,A
                AC                      XRA   H
                77                      MOV   M,A
                AB                      XRA   E
                77                      MOV   M,A
                AA                      XRA   D
3320            77                      MOV   M,A
                A9                      XRA   C
                77                      MOV   M,A
                A8                      XRA   B
                77                      MOV   M,A
                AF                      XRA   A
                77                      MOV   M,A
                F6 55                   ORI   55
                77                      MOV   M,A
                F6 AA                   ORI   AA
                77                      MOV   M,A
                C3 40 33                JMP   IO
                              *CHECK I/O
3340            AF            IO        XRA   A
                D3 00                   OUT   0
                D3 FF                   OUT   FF
                3E FF                   MVI   A,FF
                DB 00                   IN    0
                77                      MOV   M,A
                3E FF                   MVI   A,FF
                DB FF                   IN    FF
                77                      MOV   M,A
                3E FF                   MVI   A,FF
                D3 00                   OUT   0
                D3 FF                   OUT   FF
                AF                      XRA   A
                DB 00                   IN    0
                77                      MOV   M,A
                AF                      XRA   A
                DB FF                   IN    FF
                77                      MOV   M,A
                C3 80 33                JMP   ROT
                              *ROTATION INSTRUCTIONS
3380            3E 80         ROT       MVI   A,80
                07                      RLC
                DA 87 33                JC    *+2
                76                      HLT
3387            77                      MOV   M,A     1,2,4,8,10,20,40,80
                07                      RLC
                D2 87 33                JNC   *-2
                77                      MOV   M,A
                0F                      RRC
                DA 92 33                JC    *+2
                76                      HLT
3392            77                      MOV   M,A     80,40,20,10,8,4,2,1
                0F                      RRC
                D2 92 33                JNC   *-2
                77                      MOV   M,A     80  CARRY IS SET
                3E 00                   MVI   A,0   CARRY SET
339A            77                      MOV   M,A     0,1,2,4,8,10,20,40,80
                17                      RAL
                D2 9A 33                JNC   *-2
339F            77                      MOV   M,A     0,80,40,20,10,8,4,2,1
                1F                      RAR
                D2 9F 33                JNC   *-2
33A4            77                      MOV   M,A
                C3 C0 33                JMP   INC
                              *INCREMENT CHECK
33B0            70            LOOK      MOV   M,B
                71                      MOV   M,C
                72                      MOV   M,D
                73                      MOV   M,E
```

```
        74                      MOV   M,H
        75                      MOV   M,L
        77                      MOV   M,A
        C9                      RET
33C0    CD 00 30        INC     CALL  LOAD1
        B8                      CMP   B         SET CARRY
        35                      DCR   M
        3D                      DCR   A
        05                      DCR   B
        0D                      DCR   C
        15                      DCR   D
        1D                      DCR   E
        25                      DCR   H
        2D                      DCR   L
        CD B0 33                CALL  LOOK
        DA D3 33                JC    *+2
        76                      HLT
33D3    04                      INR   B
        0C                      INR   C
        14                      INR   D
        1C                      INR   E
        24                      INR   H
        2C                      INR   L
        3C                      INR   A
        34                      INR   M
        CD B0 33                CALL  LOOK
        AF                      XRA   A
        47                      MOV   B,A
        05                      DCR   B
        D2 E5 33                JNC   *+2
        76                      HLT
33E5    70                      MOV   M,B
        C3 00 34                JMP   BRANCH
                        *CHECK JMPS, CALLS AND RETURNS
3400    AF              BRANCH  XRA   A         CLEAR A AND CARRY
        DA 41 34                JC    FAIL1
        DC 41 34                CC    FAIL1
        C2 41 34                JNZ   FAIL1
        C4 41 34                CNZ   FAIL1
        E2 41 34                JPO   FAIL1
3410    E4 41 34                CPO   FAIL1
        FA 41 34                JM    FAIL1
        FC 41 34                CM    FAIL1
        D8                      RC
        C0                      RNZ
        E0                      RPO
        F8                      RM
        D2 21 34                JNC   *+2
        76                      HLT
3421    F2 25 34                JP    *+2
        76                      HLT
3425    CA 29 34                JZ    *+2
        76                      HLT
3429    EA 2D 34                JPE   *+2
        76                      HLT
342D    D4 33 34                CNC   SUBNC
        C3 42 34                JMP   JMP1
3433    F4 37 34        SUBNC   CP    SUBP
        D0                      RNC
3437    CC 3B 34        SUBP    CZ    SUBZ
        F0                      RP
343B    EC 3F 34        SUBZ    CPE   SUBPE
        C8                      RZ
343F    00              SUBPE   NOP
        E8                      RPE
3441    76              FAIL1   HLT
3442    3E FF           JMP1    MVI   A,FF
        87                      ADD   A         FF+FF=FE+C
        D2 91 34                JNC   FAIL2
        D4 91 34                CNC   FAIL2
        CA 91 34                JZ    FAIL2
        CC 91 34                CZ    FAIL2
3451    EA 91 34                JPE   FAIL2
        EC 91 34                CPE   FAIL2
        F2 91 34                JP    FAIL2
        F4 91 34                CP    FAIL2
        DA 61 34                JC    *+2
        76                      HLT
3461    FA 65 34                JM    *+2
        76                      HLT
3465    C2 69 34                JNZ   *+2
        76                      HLT
3469    E2 6D 34                JPO   *+2
        76                      HLT
```

```
346D E4 73 34                  CC    SUBC
    C3 92 34                   JMP   JMP2
3473 FC 77 34        SUBC      CM    SUBM
    D8                         RC
3477 C4 7B 34        SUBM      CNZ   SUBNZ
    F8                         RM
347B E4 7F 34        SUBNZ     CPO   SUBPO
    C0                         RNZ
347F CD 83 34        SUBPO     CALL  NEST5
    E0                         RPO
3483 CD 87 34        NEST5     CALL  NEST6
    C9                         RET
3487 CD 8B 34        NEST6     CALL  NEST7
    C9                         RET
348B 00              NEST7     NOP
    C9                         RET
3491 76              FAIL2     HLT
3492 00              JMP2      NOP
    C3 00 40                   JMP   LXI
                     *THE FOLLOWING INSTRUCTIONS ARE FOR 8080 ONLY
                     *CHECK INDEX REGISTER LOADING (LXI)
4000 CD 90 32        LXI       CALL  CLEAR
    01 DC FE                   LXI   B,FEDC
    11 98 BA                   LXI   D,BA98
    21 54 76                   LXI   H,7654
    31 23 01                   LXI   SP,0123
    C5                         PUSH  B
4010 D5                        PUSH  D
    E5                         PUSH  H
    F5                         PUSH  PSW
    CD 90 32                   CALL  CLEAR
    F1                         POP   PSW
    E1                         POP   H
    D1                         POP   D
    C1                         POP   B
    CD B0 33                   CALL  LOOK
                     *CHECK LOAD AND STORE A FROM MEMORY
401D 3E AA                     MVI   A,AA
    32 23 01                   STA   0123
4022 AF                        XRA   A
    3A 23 01                   LDA   0123
    77                         MOV   M,A
                     *CHECK INDEX REGISTER EXCHANGES
4027 EB                        XCHG
    E3                         XTHL
    CD B0 33                   CALL  LOOK
    F9                         SPHL
402D C1                        POP   B
    21 40 40                   LXI   H,4040
4031 E9                        PCHL
    76                         HLT
                     *CHECK DOUBLE ADDS
4040 01 AA AA                  LXI   B,AAAA
    21 55 55                   LXI   H,5555
    AF                         XRA   A
    09                         DAD   B        AAAA+5555=FFFF
    E5                         PUSH  H        CHECK DAD
    F5                         PUSH  PSW      CHECK STATUS
    23                         INX   H        FFFF+1=0
    E5                         PUSH  H
    F5                         PUSH  PSW
    2B                         DCX   H        0-1=FFFF
    E5                         PUSH  H
    F5                         PUSH  PSW
4050 AF                        XRA   A        CLEAR A
    11 44 44                   LXI   D,4444
    21 BB BB                   LXI   H,BBBB
    19                         DAD   D        BBBB+4444=FFFF
    E5                         PUSH  H
    21 55 55                   LXI   H,5555
    29                         DAD   H        (DOUBLE SHIFT LEFT)
    E5                         PUSH  H
    31 AA AA                   LXI   SP,AAAA
4061 21 55 55                  LXI   H,5555
    39                         DAD   SP
4065 E5                        PUSH  H
    C3 70 40                   JMP   STAX
                     *CHECK INDIRECT STORE AND LOADS
4070 01 87 A9        STAX      LXI   B,A987
    11 43 65                   LXI   D,6543
    3E BC                      MVI   A,BC
    02                         STAX  B
    3E DE                      MVI   A,DE
    12                         STAX  D
```

```
      AF                        XRA   A
      0A                        LDAX  B
      77                        MOV   M,A
      1A                        LDAX  D
      77                        MOV   M,A
4081  C3  90  40                JMP   INX
                        *CHECK INDEX INCREMENT,DECREMENT
4090  01  FF  00          INX   LXI   B,00FF
      11  FF  01                LXI   D,01FF
      21  FF  02                LXI   H,02FF
      31  FF  03                LXI   SP,03FF
      03                        INX   B
      13                        INX   D
      23                        INX   H
      33                        INX   SP
40A0  CD  B0  33                CALL  LOOK
      0B                        DCX   B
      1B                        DCX   D
      2B                        DCX   H
      3B                        DCX   SP
      CD  B0  33                CALL  LOOK
40AA  C3  B0  40                JMP   CMA
                        *CHECK CMA,STC,CMC AND DAA
40B0  AF                CMA     XRA   A       CLEAR A, RESET CARRY
      F5                        PUSH  PSW
      2F                        CMA           A=FF
      F5                        PUSH  PSW
      37                        STC           CARRY SET
      F5                        PUSH  PSW
      3F                        CMC           CARRY CLEAR
      F5                        PUSH  PSW
      3F                        CMC           CARRY SET
      F5                        PUSH  PSW
      3E  AA                    MVI   A,AA
      2F                        CMA           A=55
      77                        MOV   M,A
      27                        DAA
      77                        MOV   M,A
      C3  D0  40                JMP   SHLD
                        *CHECK SHLD, LHLD
40D0  21  55  55        SHLD    LXI   H,5555
      22  01  01                SHLD  0101
      21  00  00                LXI   H,0000
      2A  01  01                LHLD  0101
      E5                        PUSH  H
      FFFF                      TERMINATE DIAGNOSTIC GENERATION
```

Example 8080SPM Pattern Generation

Output Map

STAT1A TEST PLAN MAP SN 1

8080 TRUTH TABLE GENERATION FOR SPM REV 1 PAGE 1 AMD

LOCAL MEMORY PAGE 1

COUNT	L.M. ADDR	MPU ADDR	DATA R	DATA W	OPCODE	STAT	STACK ADDR	A/F	B/C	D/E	H/L
00000006	0007	0000	C3		JMP	A2	FFF2	0046	0000	0000	0000
READ WAIT TEST											
00000029	0015	0001	45			82					
00000032	0016	0002	00			82					
00000035	0017	0045	3E		MVI A	A2	FFE1	0046	0000	0000	0000
00000039	0020	0046	00			82					
00000042	0021	0047	32		STA	A2	FFD0	0046	0000	0000	0000
00000046	0022	0048	00			82					
00000049	0023	0049	00			82					
WRITE WAIT TEST											
00000052	0024	0000		00		00					
00000065	0031	004A	3E		MVI A	A2	FFF0	0046	0000	0000	0000
00000069	0032	004B	FF			82					
00000072	0033	004C	32		STA	A2	FFDF	FF46	0000	0000	0000
00000076	0034	004D	FF			82					
00000079	0035	004E	FF			82					
WRITE WAIT TEST											
00000082	0036	FFFF		FF		00					
00000095	0043	004F	F3		DI	A2	FFF1	FF46	0000	0000	0000
READ HOLD TEST											
00000110	0057	0050	21		LXI H	A2	FFE0	FF46	0000	0000	0000
00000114	0060	0051	00			82					
00000117	0061	0052	00			82					
00000120	0062	0053	36		MVI M	A2	FFCF	FF46	0000	0000	0000
00000124	0063	0054	00			82					
WRITE WAIT TEST											
00000127	0064	0000		00		00					
00000140	0071	0055	2C		INR L	A2	FFBD	FF46	0000	0000	0000
00000145	0072	0056	36		MVI M	A2	FFAC	FF02	0000	0000	0001
00000149	0073	0057	FB			82					
00000152	0074	0001		FB		00					
00000155	0075	0058	2C		INR L	A2	FF9B	FF02	0000	0000	0001
00000160	0076	0059	36		MVI M	A2	FF8A	FF02	0000	0000	0002
00000164	0077	005A	C9			82					
00000167	0100	0002		C9		00					
00000170	0101	005B	31		LXI SP	A2	FF79	FF02	0000	0000	0002
00000174	0102	005C	F6			82					
00000177	0103	005D	FF			82					
00000180	0104	005E	E1		POP H	A2	FFF6	FF02	0000	0000	0002
00000184	0105	FFF6	08			86					
00000187	0106	FFF7	07			86					
00000190	0107	005F	D1		POP D	A2	FFF8	FF02	0000	0000	0708
00000194	0110	FFF8	06			86					
00000197	0111	FFF9	05			86					
00000200	0112	0060	C1		POP B	A2	FFFA	FF02	0000	0506	0708
00000204	0113	FFFA	04			86					
00000207	0114	FFFB	03			86					
00000210	0115	0061	F1		POP PSW	A2	FFFC	FF02	0304	0506	0708
00000214	0116	FFFC	02			86					
00000217	0117	FFFD	01			86					
00000220	0120	0062	FB		EI	A2	FFFE	0102	0304	0506	0708
00000224	0121	0063	00		NOP	A2	FFFE	0102	0304	0506	0708
READ WAIT TEST											
00000247	0127	0064	00		NOP	A2	FFFE	0102	0304	0506	0708
INTERRUPT REQUESTED											
00000251	0130	0065	C7		RST 0	23	FFFE	0102	0304	0506	0708
00000256	0131	FFFD		00		04					
00000259	0132	FFFC		65		04					
00000262	0133	0000	00		NOP	A2	FFFC	0102	0304	0506	0708
READ WAIT TEST											
00000285	0141	0001	FB		EI	A2	FFFC	0102	0304	0506	0708
00000289	0142	0002	C9		RET	A2	FFFC	0102	0304	0506	0708
00000293	0143	FFFC	65			86					
00000296	0144	FFFD	00			86					
00000299	0145	0065	00		NOP	A2	FFFE	0102	0304	0506	0708
INTERRUPT REQUESTED											
00000303	0146	0066	CF		RST 1	23	FFFE	0102	0304	0506	0708
00000308	0147	FFFD		00		04					
00000311	0150	FFFC		66		04					

LOCAL MEMORY PAGE 1

COUNT	L.M. ADDR	MPU ADDR	DATA R	DATA W	OPCODE	STAT	STACK ADDR	A/F	B/C	D/E	H/L
00000314	0151	0008	00		NOP	A2	FFFC	0102	0304	0506	0708
00000318	0152	0009	FB		EI	A2	FFFC	0102	0304	0506	0708
00000322	0153	000A	C9		RET	A2	FFFC	0102	0304	0506	0708
00000326	0154	FFFC	66			86					
00000329	0155	FFFD	00			86					
INTERRUPT REQUESTED											
00000332	0156	0066	D7		RST 2	23	FFFC	0102	0304	0506	0708
00000337	0157	FFFD		00		04					
00000340	0160	FFFC		66		04					
00000343	0161	0010	00		NOP	A2	FFFC	0102	0304	0506	0708
INTERRUPT REQUESTED											
00000347	0162	0011	00		NOP	A2	FFFC	0102	0304	0506	0708
00000351	0163	0012	FB		EI	A2	FFFC	0102	0304	0506	0708
00000355	0164	0013	00		NOP	A2	FFFC	0102	0304	0506	0708
00000359	0165	0014	DF		RST 3	23	FFFC	0102	0304	0506	0708
00000364	0166	FFFB		00		04					
00000367	0167	FFFA		14		04					
00000370	0170	0018	00		NOP	A2	FFFA	0102	0304	0506	0708
00000374	0171	0019	FB		EI	A2	FFFA	0102	0304	0506	0708
00000378	0172	001A	C9		RET	A2	FFFA	0102	0304	0506	0708
00000382	0173	FFFA	14			86					
00000385	0174	FFFB	00			86					
INTERRUPT REQUESTED											
00000388	0175	0014	E7		RST 4	23	FFFA	0102	0304	0506	0708
00000393	0176	FFFB		00		04					
00000396	0177	FFFA		14		04					
00000399	0200	0020	00		NOP	A2	FFFA	0102	0304	0506	0708
00000403	0201	0021	FB		EI	A2	FFFA	0102	0304	0506	0708
00000407	0202	0022	C9		RET	A2	FFFA	0102	0304	0506	0708
00000411	0203	FFFA	14			86					
00000414	0204	FFFB	00			86					
INTERRUPT REQUESTED											
00000417	0205	0014	EF		RST 5	23	FFFA	0102	0304	0506	0708
00000422	0206	FFFB		00		04					
00000425	0207	FFFA		14		04					
00000428	0210	0028	00		NOP	A2	FFFA	0102	0304	0506	0708
00000432	0211	0029	FB		EI	A2	FFFA	0102	0304	0506	0708
00000436	0212	002A	C9		RET	A2	FFFA	0102	0304	0506	0708
00000440	0213	FFFA	14			86					
00000443	0214	FFFB	00			86					
INTERRUPT REQUESTED											
00000446	0215	0014	F7		RST 6	23	FFFA	0102	0304	0506	0708
00000451	0216	FFFB		00		04					
00000454	0217	FFFA		14		04					
00000457	0220	0030	00		NOP	A2	FFFA	0102	0304	0506	0708
00000461	0221	0031	FB		EI	A2	FFFA	0102	0304	0506	0708
00000465	0222	0032	C9		RET	A2	FFFA	0102	0304	0506	0708
00000469	0223	FFFA	14			86					
00000472	0224	FFFB	00			86					
00000475	0225	0014	C9		RET	A2	FFFC	0102	0304	0506	0708
00000479	0226	FFFC	66			86					
00000482	0227	FFFD	00			86					
00000485	0230	0066	78		MOV A,B	A2	FFFE	0102	0304	0506	0708
READ WAIT TEST											
00000509	0236	0067	77		MOV M,A	A2	FFFE	0302	0304	0506	0708
WRITE WAIT TEST											
00000513	0237	0708		03		00					
00000526	0244	0068	36		MVI M	A2	FFFE	0302	0304	0506	0708
00000530	0245	0069	78			82					
WRITE WAIT TEST											
00000533	0246	0708		78		00					
00000546	0253	006A	87		ADD A	A2	FFFE	0302	0304	0506	0708
READ WAIT TEST											
00000569	0261	006B	CD		CALL	A2	FFFE	0606	0304	0506	0708
00000574	0262	006C	00			82					
READ WAIT TEST											
00000596	0270	006D	01			82					
00000599	0271	FFFD		00		04					
00000602	0272	FFFC		6E		04					
00000605	0273	0100	AF		XRA A	A2	FFFC	0606	0304	0506	0708
00000609	0274	0101	DC		CC	A2	FFFC	0046	0304	0506	0708
00000614	0275	0102	04			82					
00000617	0276	0103	01			82					
00000620	0277	0104	D8		RC	A2	FFFC	0046	0304	0506	0708
00000625	0300	0105	C9		RET	A2	FFFC	0046	0304	0506	0708

LOCAL MEMORY PAGE 1

COUNT	L.M. ADDR	MPU ADDR	DATA R	DATA W	OPCODE	STAT	STACK ADDR	A/F	B/C	D/E	H/L
00000629	0301	FFFC	6E			86					
00000632	0302	FFFD	00			86					
00000635	0303	006E	C3		JMP	A2	FFFE	0046	0304	0506	0708
00000639	0304	006F	00			82					
00000642	0305	0070	02			82					
READ WAIT TEST											
00000664	0313	0200	D4		CNC	A2	FFFE	0046	0304	0506	0708
00000669	0314	0201	00			82					
00000672	0315	0202	03			82					
00000675	0316	FFFD		02		04					
00000678	0317	FFFC		03		04					
00000681	0320	0300	D0		RNC	A2	FFFC	0046	0304	0506	0708
00000686	0321	FFFC	03			86					
00000689	0322	FFFD	02			86					
00000692	0323	0203	D3		OUT	A2	FFFE	0046	0304	0506	0708
00000696	0324	0204	00			82					
00000699	0325	0000		00		10					
00000702	0326	0205	DB		IN	A2	FFFE	0046	0304	0506	0708
00000706	0327	0206	00			82					
00000709	0330	0000	00			42					
00000712	0331	0207	31		LXI SP	A2	FFFE	0046	0304	0506	0708
00000716	0332	0208	66			82					
00000719	0333	0209	44			82					
00000722	0334	020A	F5		PUSH PSW	A2	4466	0046	0304	0506	0708
WRITE HOLD TEST											
00000727	0335	4465		00		04					
00000742	0351	4464		46		04					
00000745	0352	020B	E5		PUSH H	A2	4464	0046	0304	0506	0708
00000750	0353	4463		07		04					
00000753	0354	4462		08		04					
00000756	0355	020C	C5		PUSH B	A2	4462	0046	0304	0506	0708
WRITE HOLD TEST											
00000761	0356	4461		03		04					
WRITE HOLD TEST											
00000776	0372	4460		04		04					
00000791	0406	020D	31		LXI SP	A2	4460	0046	0304	0506	0708
00000795	0407	020E	FF			82					
00000798	0410	020F	7F			82					
00000801	0411	0210	D5		PUSH D	A2	7FFF	0046	0304	0506	0708
00000806	0412	7FFE		05		04					
00000809	0413	7FFD		06		04					
00000812	0414	0211	32		STA	A2	7FFD	0046	0304	0506	0708
00000816	0415	0212	AA			82					
READ HOLD TEST											
00000831	0431	0213	55			82					
READ HOLD TEST											
00000846	0445	55AA		00		00					
00000849	0446	0214	22		SHLD	A2	7FFD	0046	0304	0506	0708
00000853	0447	0215	55			82					
00000856	0450	0216	AA			82					
00000859	0451	AA55		08		00					
00000862	0452	AA56		07		00					
00000865	0453	0217	E3		XTHL	A2	7FFD	0046	0304	0506	0708
00000869	0454	7FFD	06			86					
00000872	0455	7FFE	05			86					
00000875	0456	7FFE		07		04					
00000878	0457	7FFD		08		04					
00000883	0460	0218	FB		EI	A2	7FFD	0046	0304	0506	0506
00000887	0461	0219	76		HLT	A2	7FFD	0046	0304	0506	0506
00000891	0462	0219	76			8A					
HALT ACKNOWLEDGED											
INTERRUPT REQUESTED											
00000905	0475	021A	FF		RST 7	2B	7FFD	0046	0304	0506	0506
00000910	0476	7FFC		02		04					
00000913	0477	7FFB		1A		04					
00000916	0500	0038	00		NOP	A2	7FFB	0046	0304	0506	0506
00000920	0501	0039	FB		EI	A2	7FFB	0046	0304	0506	0506
00000924	0502	003A	C9		RET	A2	7FFB	0046	0304	0506	0506
00000928	0503	7FFB	1A			86					
00000931	0504	7FFC	02			86					
00000934	0505	021A	00		NOP	A2	7FFD	0046	0304	0506	0506
00000938	0506	021B	F3		DI	A2	7FFD	0046	0304	0506	0506
00000942	0507	021C	C3		JMP	A2	7FFD	0046	0304	0506	0506
00000946	0510	021D	00			82					
00000949	0511	021E	2F			82					

LOCAL MEMORY PAGE 1

COUNT	L.M. ADDR	MPU ADDR	DATA R	DATA W	OPCODE	STAT	STACK ADDR	A/F	B/C	D/E	H/L
00010869	6051	0101		55		00					
00010872	6052	0102		55		00					
00010875	6053	40D6	21		LXI H	A2	03F5	B583	00FF	01FF	5555
00010879	6054	40D7	00			82					
00010882	6055	40D8	00			82					
00010885	6056	40D9	2A		LHLD	A2	03F5	B583	00FF	01FF	0000
00010889	6057	40DA	01			82					
00010892	6060	40DB	01			82					
00010895	6061	0101	55			82					
00010898	6062	0102	55			82					
00010901	6063	40DC	E5		PUSH H	A2	03F5	B583	00FF	01FF	5555
00010906	6064	03F4		55		04					
00010909	6065	03F3		55		04					

SUMMARY OF INSTRUCTIONS TESTED

INSTRUCTION	# USED
NOP	17
STAX B	2
INR B	1
MVI B	7
DAD B	1
DCX B	1
DCR C	1
RRC	9
STAX D	1
INR D	1
MVI D	8
DAD D	1
DCX D	1
DCR E	1
RAR	9
SHLD	2
INR H	1
MVI H	9
DAD H	1
DCX H	2
DCR L	1
CMA	2
STA	20
INR M	1
MVI M	17
DAD SP	1
DCX SP	1
DCR A	1
CMC	2
MOV B,C	1
MOV B,E	1
MOV B,L	1
MOV B,A	22
MOV C,C	1
MOV C,E	1
MOV C,L	1
MOV C,A	18
MOV D,C	4
MOV D,E	1
MOV D,L	1
MOV D,A	18
MOV E,C	1
MOV E,E	1
MOV E,L	1
MOV E,A	18
MOV H,C	1
MOV H,E	4
MOV H,L	1
MOV H,A	17
MOV L,C	1
MOV L,E	1
MOV L,L	1
MOV L,A	17
MOV M,C	32
MOV M,E	32
MOV M,L	32
MOV M,A	141
MOV A,C	1
MOV A,E	1
MOV A,L	1
MOV A,A	1
ADD C	1
ADD E	1
ADD L	1
ADD A	3
ADC C	1
ADC E	1
ADC L	1
ADC A	1
SUB C	1
SUB E	1
SUB L	1
SUB A	1
SBB C	1
SBB E	1
SBB L	1
SBB A	1
ANA C	1
ANA E	1
ANA L	1

1377 INSTRUCTIONS EXECUTED

INSTRUCTION	# USED
LXI B	3
INX B	1
DCR B	2
RLC	121
LDAX B	1
INR C	1
MVI C	8
LXI D	4
INX D	1
DCR D	1
RAL	9
LDAX D	1
INR E	1
MVI E	8
LXI H	10
INX H	2
DCR H	1
DAA	1
LHLD	1
INR L	3
MVI L	8
LXI SP	6
INX SP	1
DCR M	1
STC	1
LDA	17
INR A	1
MVI A	36
MOV B,B	2
MOV B,D	1
MOV B,H	1
MOV B,M	1
MOV C,B	4
MOV C,D	1
MOV C,H	1
MOV C,M	1
MOV D,B	1
MOV D,D	1
MOV D,H	1
MOV D,M	1
MOV E,B	1
MOV E,D	4
MOV E,H	1
MOV E,M	1
MOV H,B	1
MOV H,D	1
MOV H,H	1
MOV H,M	1
MOV L,B	1
MOV L,D	1
MOV L,H	4
MOV L,M	1
MOV M,B	33
MOV M,D	32
MOV M,H	32
HLT	1
MOV A,B	2
MOV A,D	1
MOV A,H	1
MOV A,M	1
ADD B	1
ADD D	1
ADD H	1
ADD M	1
ADC B	1
ADC D	1
ADC H	1
ADC M	1
SUB B	1
SUB D	1
SUB H	1
SUB M	1
SBB B	1
SBB D	1
SBB H	1
SBB M	1
ANA B	1
ANA D	1
ANA H	1
ANA M	1

ANA	A	1	XRA	B	2
XRA	C	3	XRA	D	3
XRA	E	3	XRA	H	3
XRA	L	3	XRA	M	2
XRA	A	17	ORA	B	1
ORA	C	1	ORA	D	1
ORA	E	1	ORA	H	1
ORA	L	1	ORA	M	1
ORA	A	1	CMP	B	6
CMP	C	3	CMP	D	3
CMP	E	3	CMP	H	3
CMP	L	3	CMP	M	4
CMP	A	1	RNZ		2
POP	B	3	JNZ		2
JMP		18	CNZ		2
PUSH	B	2	ADI		1
RST	0	1	RZ		1
RET		65	JZ		15
CZ		3	CALL		57
ACI		1	RST	1	1
RNC		2	POP	D	2
JNC		66	OUT		3
CNC		9	PUSH	D	2
SUI		1	RST	2	1
RC		3	JC		16
IN		3	CC		4
SBI		1	RST	3	1
RPO		2	POP	H	2
JPO		2	XTHL		2
CPO		3	PUSH	H	9
ANI		1	RST	4	1
RPE		1	PCHL		1
JPE		2	XCHG		1
CPE		2	XRI		3
RST	5	1	RP		1
POP	PSW	2	JP		3
DI		2	CP		2
PUSH	PSW	10	ORI		2
RST	6	1	RM		2
SPHL		1	JM		3
EI		10	CM		2
CPI		11	RST	7	1

SUMMARY OF INSTRUCTIONS NOT EXERCISED

INSTRUCTION	OPCODE	INSTRUCTION	OPCODE
INVALID	0008	INVALID	0010
INVALID	0018	INVALID	0020
INVALID	0028	INVALID	0030
INVALID	0038	INVALID	00CB
INVALID	00D9	INVALID	00DD
INVALID	00ED	INVALID	00FD
INVALID	00ED		

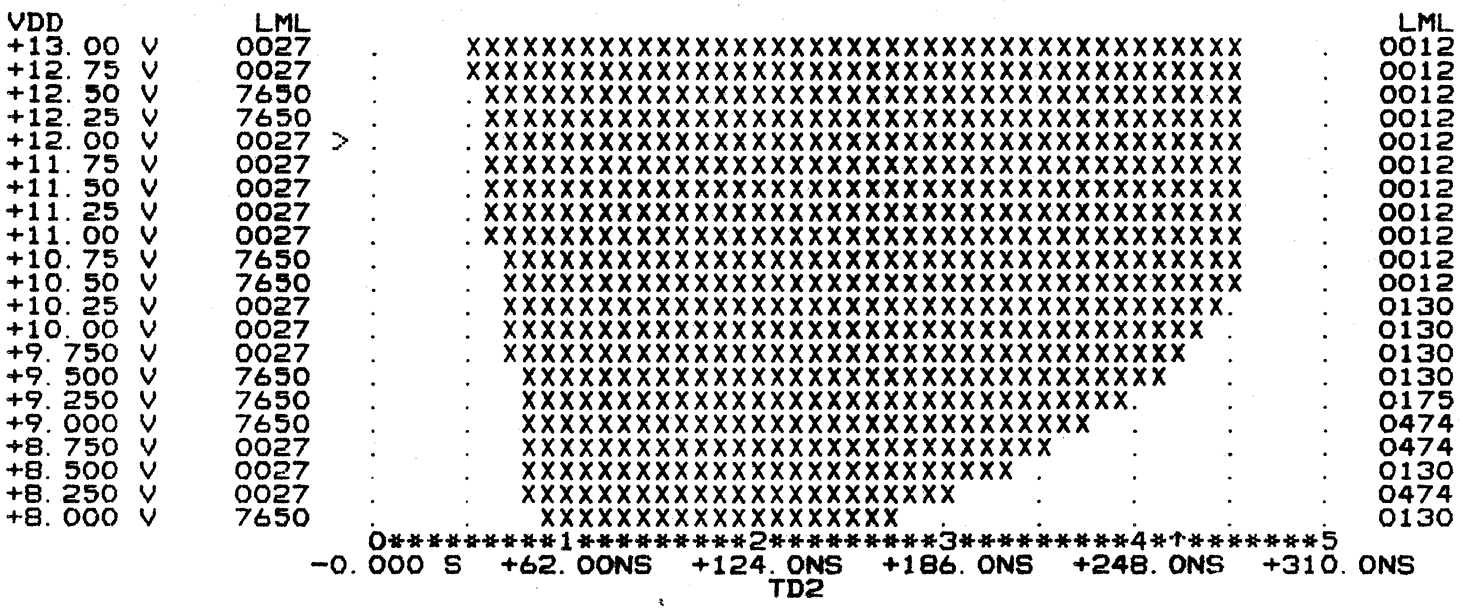
SUMMARY OF BACKGROUNDS USED

BACKGROUND	# USED
1	40
2	6
3	9

Example of Shmoo Plot

```
SHMOO PLOT AT STATEMENT NUMBER  1565                    SPLOT REVISION 3.2

VDD  YSTART=+13.00 V          YSTOP=+8.000 V          YDELTA=+250.0MV
DPS2 YSTART=+13.00 V          YSTOP=+8.000 V          YDELTA=+250.0MV
TD2  XSTART=+310.0NS          XSTOP=-0.000 S          XDELTA=+6.200NS
 PD2 XSTART=+99.99NS          XSTOP=+410.0NS          XDELTA=-6.200NS
 PW2 XSTART=+420.0NS          XSTOP=+110.0NS          XDELTA=+6.200NS
 PD5 XSTART=-30.01NS          XSTOP=+280.0NS          XDELTA=-6.200NS
```




```
SHMOO PLOT OF PHASE 1 DELAY FROM PHASE 2 (TD2)
LOCAL MEMORY PAGE =   1                                    INT
```

Example Composite Shmoo Plot

```
STAT1A        TEST PLAN  COMPOS       SN        1

COMPOSITE SHMOO PLOT AT STATEMENT NUMBER      946
COMPOSITE NUMBER   9

VDD  YMAX =    13       V       YMIN =     8       V      YDELTA =+2.500E-01V
VBB  XMAX = -001        V       XMIN = -006        V      XDELTA =+1.000E-01V


VDD
    +   13      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7
+1.275E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$77
+1.250E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$777
+1.225E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$777
    +   12      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.175E+01      *>$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.150E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.125E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$77777
    +   11      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.075E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.050E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
+1.025E+01      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$7777
    +   10      * $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$777
+9.750E-00      * 77777$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$777
+9.500E-00      * 37777777777777777777777$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$777
+9.250E-00      * 33333337777777777777777777777777777$$$$$$$$$$$$$$$$$$$$$$$777
    +    9      * 33333333333337777777777777777777777777777777777$$$$$$$$$$$777
+8.750E-00      * 33333333333333333337777777777777777777777777777733333
+8.500E-00      * 33333333333333333333333377777777777777777777773333
+8.250E-00      * 33333333333333333333333333333337777777777777733333
    +    8      * 33333333333333333333333333333333333337777777773333
                  0*********1*********2*********3*********4*********5
      0           *         ↑         .         .         .         .
                  .         .         .         .         .         .

        0  = -006       V         1  = -005       V         2  = -004       V
        3  = -003       V         4  = -002       V         5  = -001       V
```

and returns which do not meet the conditions are tried. If a branch occurs, it is a failure. Then jumps, calls and returns which do meet the conditions are tested.

The above conditions are all reversed by loading A with FF and adding FF to FF getting FE + carry which is non zero, negative and odd parity. All jumps, calls and returns are again tested.

Double register operation tests and stack pointer tests are the last phase of 8080D beginning at 4ØØØ. LXI, PUSH, POP, XCHG, XTHL, SPHL, PCHL, DAD, LDAX, STAX, INX, DCX and SHLD are in this category. Also, the decimal adjust function DAA is exercised.

3.20 Testing Peripheral Interface Devices

3.201 Introduction

The peripheral interface is typical of the devices being introduced to support microprocessor systems. Many microprocessor systems will have more than one peripheral interface per microprocessor; thus, the usage of peripheral interfaces will increase the usage of microprocessors.

A peripheral interface is a complex I/O (Input/Output) device used to transfer data between a microprocessor and one or more peripherals. The peripheral interface also can communicate control signals for hand-shaking and interrupt control.

To test the peripheral interface's many I/O configurations requires a tester capable of changing I/O connections, timing, and pulse shapes.

3.202 Peripheral Interface Description

A peripheral interface is an I/O device used to interface one or more peripherals to a microprocessor. In the case of the Intel 8255 Programmable Peripheral Interface (Figure 1), 24 I/O pins can be individually programmed to communicate with the eight-pin bidirectional data bus in three major modes of operation.

Mode 0 permits two eight-bit ports (Ports A and B) and both halves of the third port (Port C) to be individually programmed as inputs or outputs; thus, there are 16 possible input and output combinations in Mode 0 (Table 1).

Mode 1 permits Ports A and B to have hand-shaking and interrupt control signals. Port C gives up three pins to each of the two ports that are operating in Mode 1. Ports A and B do not have to be in Mode 1 at the same time.

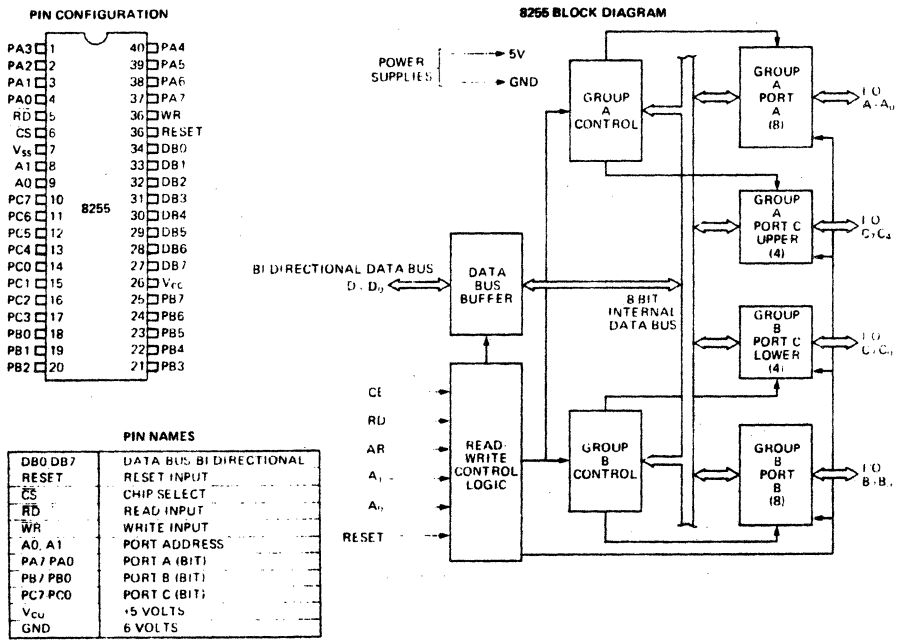


Figure 1. 8255 Block Diagram (Intel 8080 Microcomputer System's User's Manual, September 1975.)

PORT A	PORT B	FIRST PORT C	SECOND PORT C
1	1	1	1
0	1	1	1
1	0	1	1
0	0	1	1
1	1	0	1
0	1	0	1
1	0	0	1
0	0	0	1
1	1	1	0
0	1	1	0
1	0	1	0
0	0	1	0
1	1	0	0
0	1	0	0
1	0	0	0
0	0	0	0

Table 1. 16 Input/Output Combinations for Mode 0.

Port A can operate in a bidirectional mode, Mode 2, using five of the Port C pins for interrupt and hand-shaking control. Mode 2 operation permits Port A to go from an input to an output or vice versa without a mode definition cycle.

3.203 Testing Requirements of Peripheral Interfaces

In order to test peripheral devices such as Intel's 8255, the tester must be able to provide all the input and output conditions required by the device. The 8255 complicates testing with 32 I/O pins and 62 possible input and output combinations, and, along with the 62 possible input/output combinations, there are 62 possible care and don't care conditions of pin data.

To guarantee the timing specifications of the peripheral device, data from the tester should be in an Exclusive OR (XOR) mode as shown in Figure 2. Data into the device must be stable for a period of time (set up time) before a control signal (read, write, strobe, acknowledge, etc) transmits or receives this data. The data must also be stable for a time (hold time) after the control signal. Any instability or noise during valid data time may cause the wrong data to be received or transmitted.

The control signals of the 8255 must be in a return-to-one mode (RO); i.e., a pulse for zero data only and no pulse for one data. Moreover, three of the device pins may have input data in one mode requiring XOR data and control signals in another mode requiring RO data. Also, the timing requirements of these inputs change with the mode of operation. Thus, input signals can become very complex.

The address and chip select timing specifications are different in a read and write operation; thus, programmed timing must be redefined in a functional test without a break or discontinuity of the functional test.

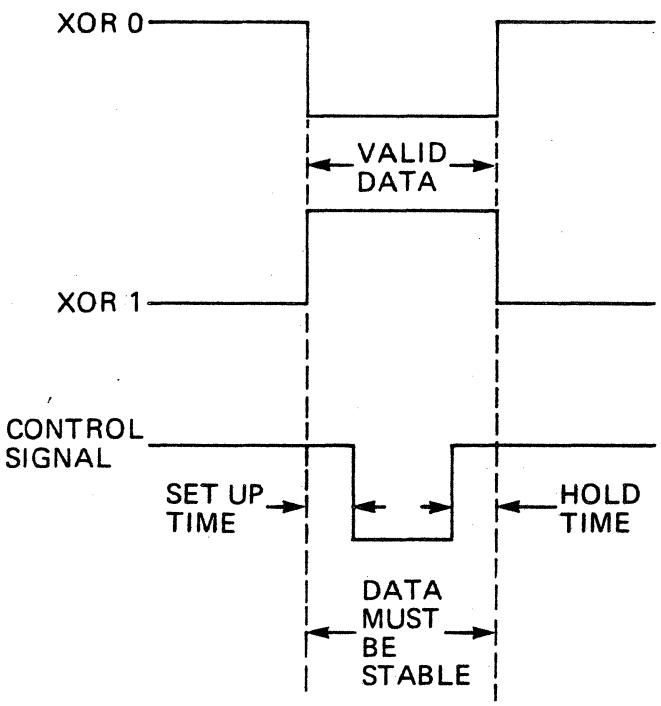

XOR 0
VALID DATA
XOR 1
CONTROL SIGNAL
SET UP TIME
HOLD TIME
DATA MUST BE STABLE

Figure 2

Testing the hand-shaking and interrupt capabilities of the peripheral device requires the ability to strobe the output data in different time slots on the same outputs, and the ability to redefine strobe timing is desirable.

3.21 Suggested Reference Material

1975 Semiconductor Test Synposium Digest of Papers
IEEE 75CH1041-3C

1976 Semiconductor Test Synposium Digest of Papers
IEEE 76CH1179-1C

International Microelectronics Conference Proceedings
1975 Industrial and Scientific Conference Management, Inc.,
Chicago, Illinois

4.0 DISCUSSION OF TESTING PHILOSOPHY

By Technology, Circuit Function & Application

Eugene Hnatek
Monolithic Memories, Inc.
Sunnyvale, California

William Woodard
and DCA Reliability Laboratory
Mountain View, California

4.1 Introduction

The myriad of available technologies and integrated electronic functions presents a major and often perplexing problem to the user who must test these circuits to ensure himself of their integrity. In order to be able to effectively test the various available technologies of ICs, one must understand these technologies and the functional designs involved. The inherent different test strategies required to properly test all device types would require many device specialists. Such a staff of specialists is obviously very difficult, if not impossible, to justify in all but the very largest companies.

By virtue of the theme of this seminar - Automated Testing of Integrated Circuits - and your presence here, the decision to use automated test equipment has already been made and justified. Thus, the ensuing discussions will be slanted toward this aspect.

It is the purpose of this session to put the testing philosophy of integrated circuits as a function of technology and the intended application into proper perspective. Relying on the authors own extensive experience, electrical test guidelines are presented for TTL, Linear, ECL, CMOS, CCD, NMOS and PMOS (RAM, ROM/PROM, and Microprocessor) ICs - based on inherent IC technology and design idiosyncracies.

These testing guidelines should be used as a starting point in developing your own electrical test strategies for the types of ICs your company uses in volume.

Then the all important application environment, that of reliability testing to weed out infant mortalities in a simulated actual system environment is discussed. Such germane topics as hermeticity tests, temperature cycling and burn-in are discussed in the context of being able to locate and remove certain accelerated failure modes that are peculiar to a given technology or IC functional design.

Of necessity, because of the sophistication of present day integrated circuits and end user equipment, both the electrical testing and application aspects must be properly combined to minimize failures. As such, screening attrition rates are presented for both commercial and high reliability integrated circuits to show the effectiveness of such a philosophy.

In effect, this session puts the topic of automated testing in proper perspective using the cohesive and permeating factor of device technology and reliability.

IC testing involves a mixture of technology and economics. The end to be achieved by the testing is always the same - proper, reliable operation of

the final product or system containing the ICs. And towards this end there is universal agreement that ICs must be tested.

But where?...when?...How?...and with what? The right answers to these questions result in good products at reasonable cost. The wrong answers spell trouble, either in faulty products, unreasonably high product costs, or both.

A distinction should be made here between the IC supplier and the IC user. The supplier must test. It is his product, and he is obliged to see that it meets his stated specifications. The user, though, is under no such obligations. He can use his purchased ICs with no testing of his own whatsoever, or he can go so far as to duplicate, or even exceed, the suppliers testing. This is the user's basic problem. As is usually the case, the best solution generally lies somewhere between the two extremes, but exactly where depends on a variety of factors.

4.11 Why Test?

Why do integrated circuits have to be tested? The answer to the question is straightforward. An integrated circuit is a product, fabricated by sophisticated mechanical and chemical processes, that is intended to perform a complex electrical function. As a product, it is subject to statistical variations.

Even simple products, such as screw fasteners produced by automatic screw machines, are subject to statistical variations. In the case of integrated circuits, processing complexity increases the chance of such variations a thousandfold.

Like all semiconductor suppliers, the integrated circuit supplier speaks in terms of yield to a specification. The yield on early manufacturing runs can vary anywhere from zero to 90 percent, depending on the nature of the specification and the sophistication of testing at the "chip" stage. Yield is defined as the ratio of units shipped to the number of good chips committed to assembly.

Once the manufacturing process has been established, yields should run between 40 to 90%, again depending on the nature of the product. Because of the large numbers of rejects (10 to 60%), it is obviously imperative that each integrated circuit be tested at least once prior to shipment. The amount and type of testing depends on many factors.

These statistical variations of the IC process, plus the increased usage of integrated circuits in electronic systems has been accompanied by an increased concern over IC failures. As a result, more and more users, particularly in the industrial area, have become interested in performing some type of screening operation at incoming inspection. Some of the most common causes of these failures are as follows:

- Do not meet electrical specifications
- Damage in transit from supplier's plant
- Latent defects

- Damaged in user's assembly process
- User misapplication
- Poorly or incorrectly written specifications
- Incorrect diagnosis

The industrial component user simply cannot tolerate the warranty costs, repair costs, loss of customer goodwill and eventual loss of sales that accompanies field failures. Often there is a direct relationship between field failures and component failures and for this reason, industrial component reliability must be equal to or the same as that required in aerospace applications. Theoretically, when an IC supplier does 100% testing of his parts, every part shipped should be good

Although IC suppliers normally do a reasonably good job of testing, there are still many ways that errors can be passed on to the user. For example, testing may be invalid if the test instrument has not been properly calibrated or has been incorrectly programmed. Then an operator may place devices in a wrong bin or when removing reject sticks or bins he mixes them with good devices. Other problems after testing consist of jamming ICs into sticks by air or motor drives or improper marking of the product. Latent defects, such as increasing leakage or cold bonds, will frequently be accepted by the 100% testing. Seldom can these types of errors and defects be completely eliminated. Consequently, most suppliers are unwilling to guarantee their shipments better than some specified AQL.

Many IC suppliers "guarantee" tested parts to a 1% AQL. What does this mean? Is it good enough? Let's see what this, as well as a 2% and 0.1% level, can do to the PC board rejection rate. It is somewhat frightening to realize that at a 1% defective component level, no boards will pass final test that have 100 ICs on them, and at 2%, none will pass final test with 50 ICs (Figure 1). It is obvious that the number of ICs per board must remain low unless the percent defective "guarantee" approaches the 0.1% level. If not, the PC board testing and rework costs will be quite high. However, this has not happened. Present day PC boards contain in excess of 250 ICs and the supplier still provides product guaranteed to an AQL of only 1%.

This untenable situation has prompted users to perform component incoming inspection tests to reduce product costs.

The results of these tests reveal user's reject rates up to 30% depending on technology and device complexity, but more commonly 0.1% to 10% at component-receiving inspection.

The economics are largely up to the individual situation, however, and should be looked at in terms of "false economy" related to "cheap ICs". Are they really cheap? Look at the total cost out the door. How many make it? If you reject 10% in your factory, that represents a 10% increased device cost, not to mention the cost in finding the rejects. Be sure to analyze the "total cost".

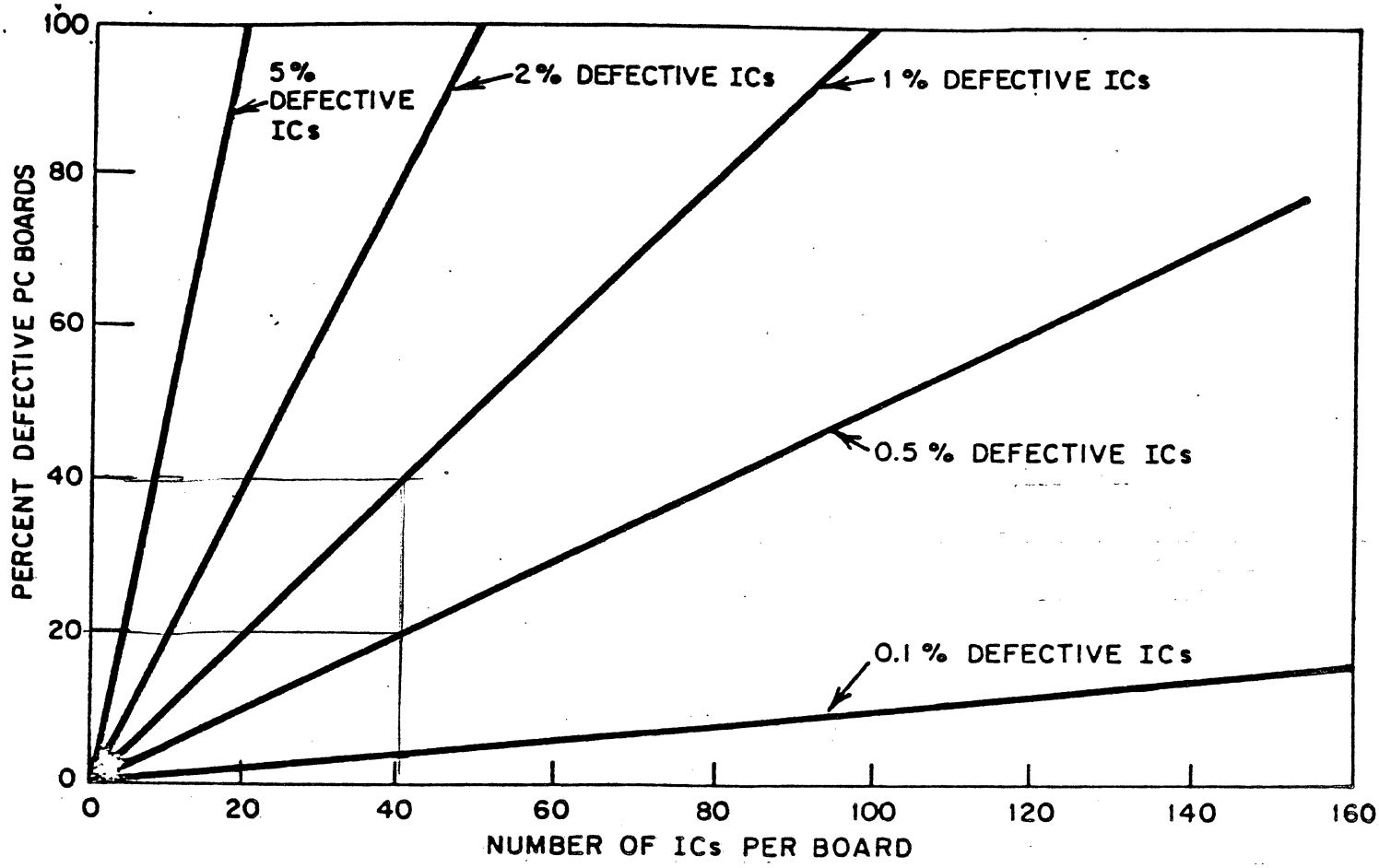
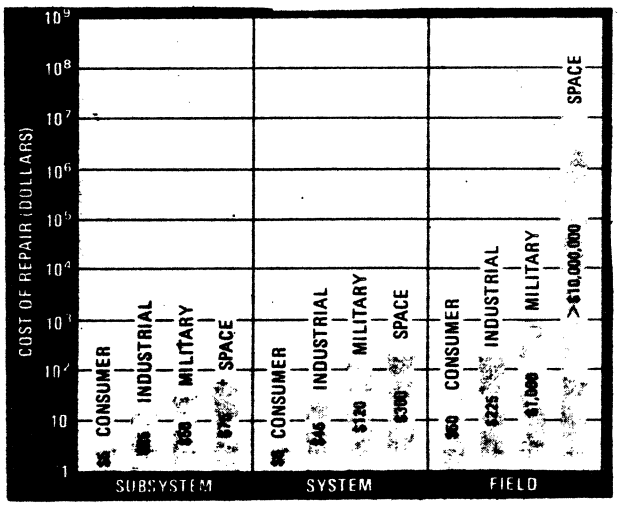


Figure 1: The number of defective PC boards rises rapidly as the number of ICs on a board goes up and as the percentage of defective ICs rises.

Table 1

Accumulative Cost of Repair As A Function Of End Usage



The integrated circuit user involved in the construction of military or aerospace equipment has a somewhat different need than the industrial user. The fundamental criterion overriding even cost, against which all other factors are measured in a military electronic system, is frequently reliability; and it is understating the case to say that measuring up to this criterion is expensive for supplier and user alike.

4.12 Objective of Testing

The objective of testing any device is to prove that it meets its rated specifications. Likewise, in engineering or product development, testing may take the form of analysis to compare actual performance to design goals. To satisfy these objectives, it is necessary to decide what tests have to be made and then to execute these tests as efficiently and economically as possible.

In any test definition, it is necessary to have a detailed knowledge of the physical structure of the device, and of its potential failure mechanisms. Proper development of test procedures should not only prove that the device is functional, but that it will continue to operate satisfactorily over a period of time.

4.13 How Much Testing is Required?

In most situations, the unique requirements of the user dictate the amount of testing required on incoming ICs. Specifically, the requirements relate to:

- Number of ICs used
- Market for end product (military, aerospace, industrial, etc.)
- IC operating considerations
- User design safety margin
- Application environment

In determining how much testing you should do, bear in mind the cost of not testing. Whether this cost is expressed in dollars and cents or product integrity, it serves as the focal point around which testing decisions are made. Users decide on a testing program they can afford based on the cost of finding and replacing a bad device and on the value they place on their reputation. The expense of repair escalates (table 1) as value is added to the component through the assembly stages. This is why many users chose to screen at the component level rather than or in addition to the system or subsystem level.

4.14 Data Sheet Specifications

The justification for automated testing is high volume, short duration testing of repeatable parameters, i.e., throughput at low cost per package. This necessitates understanding the device you are testing, and understanding the

device specifications; knowing which parameters and functions are 100% tested by the supplier; which are sample tested; and which are not tested at all, but guaranteed by virtue of the circuit design, so that meaningful test plans can be created. Certain electrical parameters such as temperature coefficient, input resistance, capacitance, gainbandwidth product, and the like, are not readily adaptable to automated testing and thus not tested, but guaranteed by circuit design.

Thus, the supplier's electrical specifications and his method of testing these parameters is of major importance. The specifications should reflect the devices being purchased and should differentiate between those parameters that are 100% tested and those guaranteed by design. Test specifications must be clear and well understood; there is no room for misinterpretation.

By functionality, TTL SSI tests are of necessity high speed, cost effective tests. Only dc tests are performed to guarantee device conformance to data sheet limits. AC testing and temperature testing are guaranteed by correlation and/or design. MSI TTL is taking over in volume from SSI. MSI testing requires full functional testing. The dc testing at 25° C guarantees the ac and temperature testing. Proper LSI TTL testing requires a knowledge of the chip layout. High speed dc, ac and functional tests must be performed at temperature extremes. For TTL circuits, input leakage current, and temperature drift are the parameters which cause most rejects.

Data sheet limits represent the supplier's best efforts to characterize the IC. However, those efforts are often made on prototype devices and on samples taken from the first few lots. Subsequent process changes based on field reports of performance limitations may necessitate product redesign and/or modify the spec limits, but several runs of devices may be shipped before the new design and test program is generated.

Volume testing to the IC supplier means performing go-no-go tests that try to select "good" devices 99% of which fall somewhere between the minimum and maximum published limits for a given spec. The "typical" specification limit quoted by the supplier and widely taken as gospel by designers mean typical for the suppliers engineering characterization samples, not necessarily for the user.

In any shipment one may very well receive ICs from one lot clustered at the minimum specs as well as another lot clustered at the maximum (Figure 2). Most designers would like to believe the "typical" spec published by the supplier since they often cannot afford the performance loss of designing against top-and-bottom worst case specs. Therefore, he may find totally unacceptable deviant lots that the supplier correctly labels totally acceptable.

Then there are fabrication problems. For two supposedly "Chinese copy" devices from two suppliers, even though the specifications can be the same and the devices are pin compatible, there is no assurance that the devices are identical parametrically. This is very important even if several suppliers use the same mask sets. For example, the requirement for a second source is so important that the primary supplier often provides

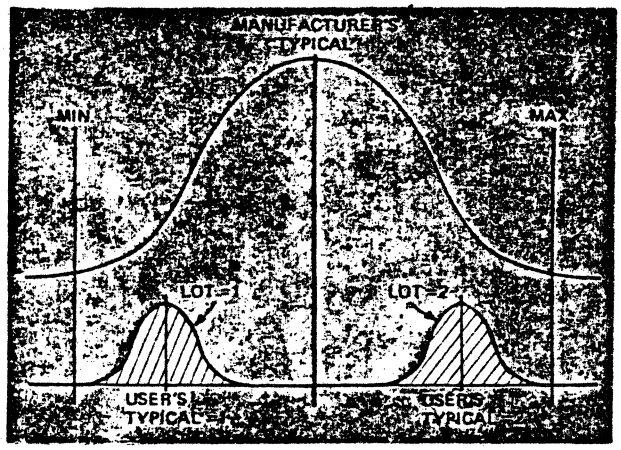


Figure 2: A "typical" data sheet value is an illusion. The supplier usually generates his typical specifications by averaging data over sample lots. On the other hand, a user's shipment may contain units from two different production lots with greatly differing specs.

the mask sets to an approved second source via a licensing agreement. Even with these masks, there is no certainty that the products will be identical - different line widths and mask registrations are normally encountered by one supplier when using another supplier's masks. Then there is the problem of making the processes match. All of which combined tend to yield a product with different characteristics than the primary source. This was not the case with simple logic functions. Thus, the following questions must be answered when evaluating a supplier's data sheet and attempting to generate a test plan from it:

- Which parameters on the supplier's data sheet are 100% tested?
- Are these parameters tested only at 25° C with correlated limits at the temperature extremes?
- Are all combinations of inputs and outputs tested?
- Are the test conditions and parametric limits specified on the data sheet those to which tests are performed?
- Do other suppliers of this device have the same test conditions and parameter limits as does the primary source?

The best solution is to procure a random sample of from 50 to 200 devices from each supplier under consideration and subject these devices to a comprehensive qualification/characterization test program. The results of this program will enable you to generate your specification to which all suppliers will provide parts and to which the device will be tested, both by the supplier and by you during your incoming inspection testing sequence.

Next, correlation should be made between the supplier's and user's test systems, the specification parameters, test conditions and limits, and device functions tested.

Standards of measurement should be established against which both supplier and user must correlate.

4.15 Categories of Electrical Test

The integrated circuit contains many internal circuit nodes which cannot be tested. All testing must be performed using only the terminals which are present on the outside of the package. The parameters which are measured must guarantee that the device will operate with other digital integrated circuits from the same family as long as the fan out and fan in rules are observed. Currents and voltages are measured at each terminal while the device is in each of its possible states. The integrated circuit is also subjected to fast pulses and its response time is measured to ensure that it will operate at the specified frequency. Flip flops or circuits with memory may also be tested for setup and release time, clock skew, ability to trigger with a minimum width and minimum amplitude trigger pulse,

and toggle rate. The testing of TTL being a mature technology, is straightforward and mechanistic in nature. Basically, no new surprises are foreseen; however, several key points are presented relating to testing circuits.

The types of tests that can be conducted on ICs can be divided into several categories. These are dc (static) test, ac (dynamic) tests and functional tests.

Functional Testing

The intent of functional testing is to provide verification that the device under test performs the intended logic function. This type of testing implies logical stimuli on all input nodes simultaneously with respect to the time at which logical signals on output nodes are measured and compared with expected values.

Even though the device under test might be static dc logic, careful consideration should be given to the dynamic characteristics of the test drive and detector circuits. For example, a slow rise/fall time of the drive circuits in conjunction with a capacitive load on an output node, e.g., due to an excessively long cable to a high input impedance detector circuit, can lead to multiple clocks which are intolerable for synchronous networks. Increasing the driver rise time and/or reducing the magnitude of the capacitive discharge current would correct this difficulty.

The volume of data required for functional testing is dependent on the logic complexity and the available means for test generation.

For example, a combinatorial logic network with 10 inputs and 10 outputs might be tested exhaustively requiring approximately (2^{10}) (20) bits of data, whereas a 30 input synchronous network with 10 internal memory states would require such a large volume of test data that practical exhausive testing becomes extremely questionable.

There are a number of ways to perform functional acceptance testing on ICs. The testing can employ statistical sampling techniques with defined risks, or it can be done on a 100% basis. The testing is go-no-go, for the lot or for individual circuits in the lot. Presuming the circuit is well characterized, an approach to functional testing can be developed using some combination of methods that provides the user with reasonable guarantees while minimizing the testing problems.

One approach to functional acceptance testing involves a 100% test of basic dc or small signal parameters at room ambient conditions to establish that all of the circuits in a lot are operational and sample tests of all other parameters under worst case operating conditions. Both dc and ac tests can be performed at high and low temperature limits. The 100% testing is done on a go-no-go basis with only the number passed and the number failed recorded.

There will normally be a PDA (percent defective allowable) associated with the 100% test, to signal the occurrence of an abnormally low yield and allow for its investigation. The user's risk is established for the sample tested

by relating the sample size to an LTPD (lot tolerance percent defective) number. This LTPD number corresponds to the maximum percent of out-of spec parts to a 90% confidence level. (The probability is 0.9 that the maximum percent out-of-spec parts is less than the LTPD number.)

Sample test results should be recorded so that they are identifiable to the lot in question. These data can serve as a running check on worst case parameter distributions and the legitimacy of the worst case limits.

User testing of ICs at temperature extremes poses many problems. The alternative, though, is extrapolation of room temperature measurements. Extrapolation is often even more of a problem and in cases of LSI circuits, not valid for drawing inferences from room temperature measurements to parameter behavior at temperature extremes. For example, testing at the high ambient temperature is required on dynamic MOS RAMs and certain linear ICs.

Static Tests

Static or dc tests are those in which steady-state voltages and currents are applied to certain terminals of the device, and the corresponding voltages and currents at the same or other terminals are measured. In a digital integrated circuit these tests define the fan-out, static noise immunity, power dissipation, etc., of the device. In a linear device, the static parameters are those that define such parameters as bias current, input offset voltage and current, common-mode rejection ratio and power dissipation.

Test rates for measuring dc parameters are influenced by the implementation technique, the required accuracy, settling time of measurement signals, and analog-to-digital conversion time. Test rates can be enhanced by functional testing prior to testing dc parameters, thereby shortening the total test time required to run through the entire test program on those devices that are catastrophic failures.

Measurement signals from the tester circuits must provide continuity between tests in order to avoid generating transient changes in the applied logic levels. For example, typical measuring circuits employ ranging techniques which switch values of sense and feedback resistances. If a range change in a measuring circuit were to cause the voltage V_{IH} to pass through the V_{OH} threshold prior to stablizing, the internal states of the circuit under test could be altered and hence effect the validity of the intended measurement. Worse yet, the circuit under test can be switched into an unknown state which could adversely influence the results of subsequent tests.

There are various implementation methods for performing a dc measurement; however, it should be noted that in general it is necessary to preset the internal states prior to measuring a dc parameter.

DC testing does not duplicate the actual end performance of the device. Consequently it is usually used in conjunction with dynamic (ac) testing and functional testing or when dynamic testing is impractical.

DC testing by itself is relatively inexpensive.

Dynamic Tests

Dynamic tests are those in which voltage pulses or sinusoidal voltages are applied to the inputs of the device, and measurements in terms of time or instantaneous voltage are made at the output. This yields measurements under actual operating conditions, thus allowing device performance to be determined much more realistically.

The dynamic parameters of a digital integrated circuit are propagation delay, output transition time, dynamic noise immunity, etc. The dynamic parameters of a linear device define its high frequency performance.

A typical, dual four-input gate requires some 40 to 50 static tests and eight to 20 dynamic tests to define its performance completely. More complex devices require correspondingly more tests. Usually, as the complexity of a device increases, the number of static parameter tests increases only slightly, whereas the number of dynamic parameter tests increases rapidly.

Dynamic testing is considerably more expensive than dc testing alone. The cost can sometimes exceed one-third of the price of the unit tested. To get around this, some users test most device parameters on a dc basis, and employ ac testing for those parameters, such as noise immunity, which cannot be adequately checked or correlated by dc techniques.

4.16 Technology Considerations

The myriad of different technologies available, (TTL family, ECL, linear, CMOS, CCD, PMOS and NMOS) strongly influence the circuit behavior. As such, it is important to understand the salient features of each technology in conjunction with the circuit design because they affect the devices electrical parameters and thus testability. Each of the following sections presents both technological process and circuit design considerations so that you can appreciate how they affect device performance and how they relate to the specification limits.

With mature technologies and processes, specifically TTL, SSI and MSI functions, detailed discussions are not presented on testability since it is well understood. Only those significant points which could possibly cause one problems are noted. However, details of the more complex and less understood devices (Linear ICs and Bipolar and MOS Memories) are presented in depth.

4.2 Bipolar ICs

4.21 TTL Circuits

As digital integrated circuits have emerged, they have fallen neatly into families such as diode transistor logic (DTL), current mode logic, and the popular transistor-transistor (TTL) logic.

TTL is a saturated logic in which transistors are switched from saturation to cutoff. Isolation is achieved by reverse biased P-N junctions causing high capacitance.

The basic technology for fabricating TTL circuitry is a mature gold doped process as shown in Figure 3. This is used in standard TTL, HTTL and LPTTL circuits. The gold acts as a recombination center reducing the lifetime of minority carriers and thus providing faster devices. However, the gold diffusion has some disadvantages: it reduces transistor gain which if too low prevents the transistors from saturating or having excessive turn-on delay. A narrower base can be used to increase h_{FE}, but this can lead to excessive junction leakage. The Schottky process sidesteps this problem. Without the need for gold doping, low storage time and high h_{FE} can be simultaneously achieved. The Schottky transistor has a higher offset voltage than does the conventional gold doped NPN transistor.

The Schottky process (Figure 4) used in STTL and LSTTL devices is based on the Schottky diode which is basically nothing more than a metal semiconductor junction. A problem with the Schottky diode clamp is that edge effects around the metal semiconductor periphery cause higher field strengths which, in turn, cause "soft" reverse breakdowns of the Schottky barrier diodes.

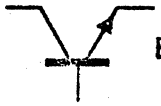
Extension of aluminum over the thermal oxide around the contact cut provide "field plate" protection which tends to minimize the field effects from the edge of the metal semiconductor junctions. With some devices, such as Proms, which see much higher reverse biases during high voltage programming, field plate geometries are not sufficient to protect against losing programming current through soft, leaky Schottky reverse-bias junctions. A p-type guard ring (Figure 5) around the edge of the metal semiconductor junction is used so that the reverse breakdown takes on the characteristic of the higher base collector junction, BV_{cbo} and provides an adequate solution to any soft breakdowns encountered during high voltage programming.

The Schottky process thus provides faster ac performance and lower input current designs than the gold doped process. However, STTL and LSTTL circuits are susceptible to transient currents which can cause a glitch and forward bias the base-collector transistor junction. Also from a processing viewpoint, two transistor bases cannot be placed in the same isolated region (as they can with STD TTL, HTTL and LTTL) since a parasitic PNPN (SCR) will be formed. Schottky and low power Schottky TTL circuits possess low noise immunity on rise time than standard TTL circuits and will often oscillate due to very fast on/off times.

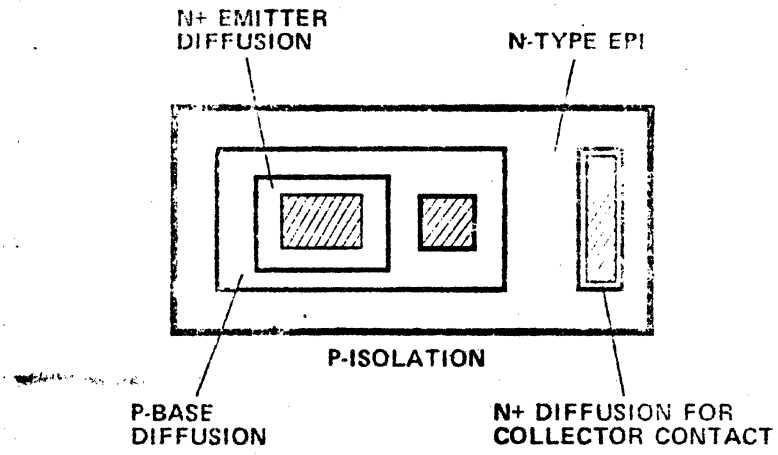
The basic differences between standard power (54/74), low power (54/74L), high power (54/74H), Schottky (54/74S) and low power Schottky (54/74S) TTL circuits is one of resistor values and transistor geometries, plus the Schottky barrier diode, where applicable, to achieve desired performance (speed or power) characteristics.

The 54/74, 54L/74L and 54H/74H are mature technologies and are well understood from a testing viewpoint. Whereas 54S/74S and 54LS/74LS are approaching their adolescence and as such, some problems need to be ironed out.

The TTL circuit's speed and power are closely related. The faster the device, the higher its power consumption and the slower the device, the lower the power consumption. Consequently, TTL devices are rated by a term called the speed-power product. This is an effective means of comparison of logic types since speed and power are closely related.



BIPOLAR NPN TRANSISTOR



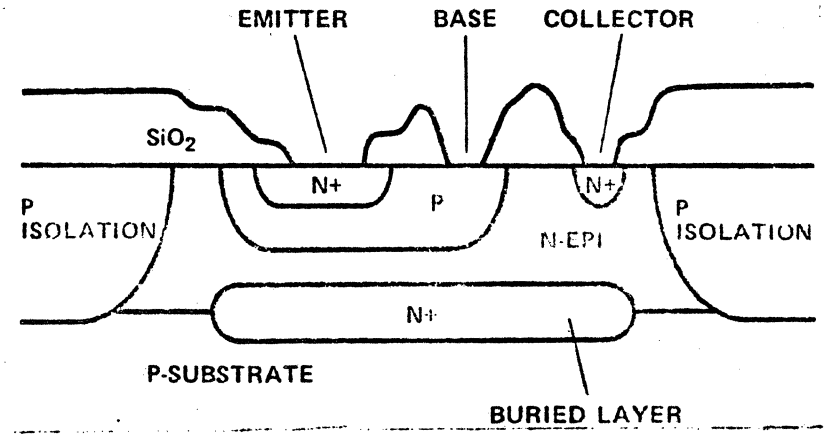
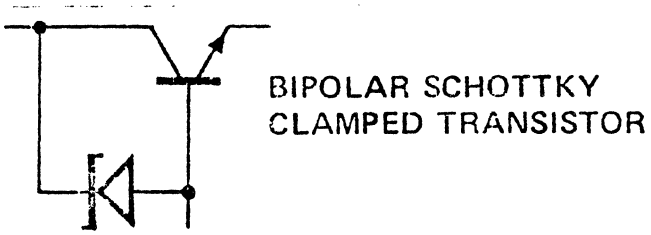
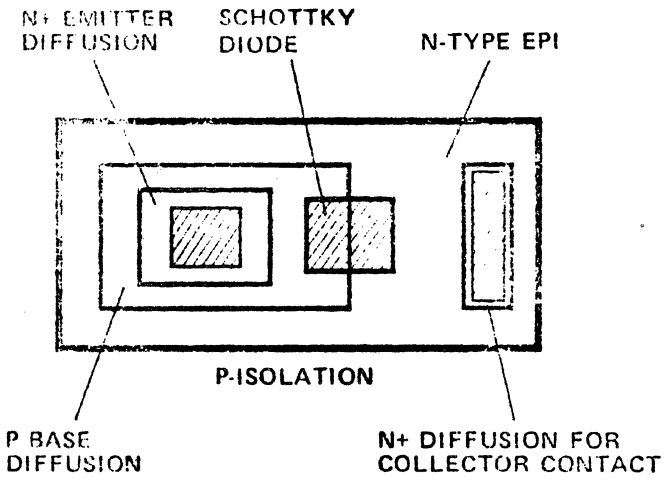


Figure 3


BIPOLAR SCHOTTKY
CLAMPED TRANSISTOR


N+ EMITTER DIFFUSION
SCHOTTKY DIODE
N-TYPE EPI
P-ISOLATION
P BASE DIFFUSION
N+ DIFFUSION FOR COLLECTOR CONTACT

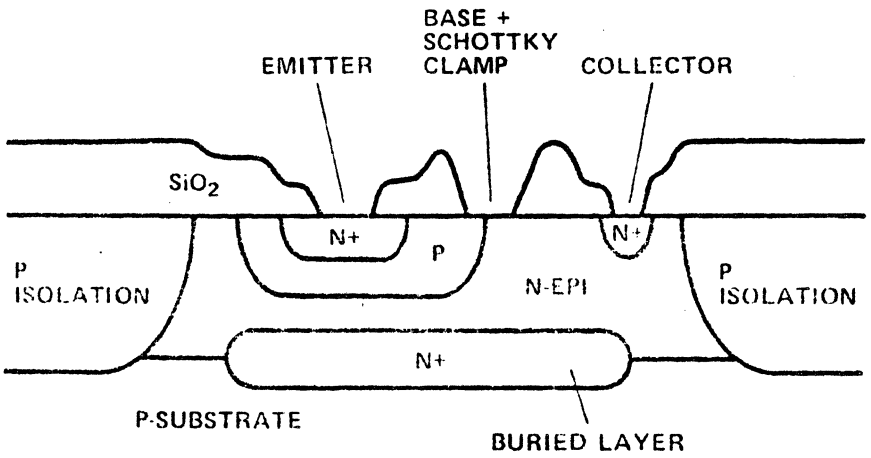

BASE + SCHOTTKY CLAMP
EMITTER
COLLECTOR
SiO2
N+
P
N+
P ISOLATION
N-EPI
P ISOLATION
N+
P-SUBSTRATE
BURIED LAYER

Figure 4

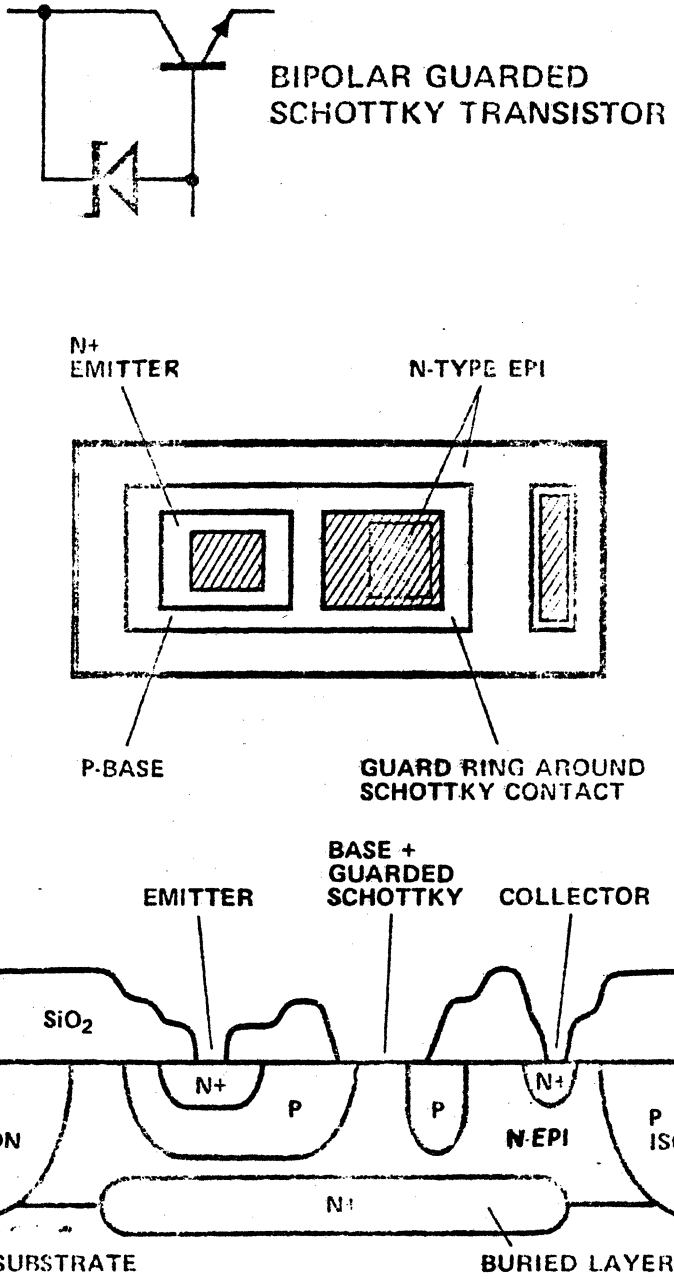

BIPOLAR GUARDED
SCHOTTKY TRANSISTOR
N+
EMITTER
N-TYPE EPI
P-BASE
GUARD RING AROUND
SCHOTTKY CONTACT
BASE +
GUARDED
SCHOTTKY
EMITTER
COLLECTOR
SiO2
N+
P
P
N+
P
ISOLATION
N-EPI
P
ISOLATION
N+
P-SUBSTRATE
BURIED LAYER

Figure 5

Figure 6 shows a plot of the speed-power products for the various TTL families as well as those for CMOS and ECL 10K logic families. Low power TTL has the lowest average gate power dissipation and also the slowest speed. Then comes LPSTTL, STD TTL, HTTL and, finally the fastest TTL family - STTL.

Figures 7 and 8 depict the various types of TTL input and output structures, respectively, which are in common usage, and their performance advantages and disadvantages.

By functionality, TTL SSI tests are of necessity high speed, cost effective tests. Only dc tests are performed to guarantee device conformance to data sheet limits. Ac testing and temperature testing are guaranteed by correlation and/or design. MSI TTL is taking over in volume from SSI. MSI testing requires full functional testing. The dc testing at 25° C guarantees the ac and temperature testing. Power LSI TTL testing requires a knowledge of the chip layout. High speed dc, ac and functional tests must be performed at temperature extremes. Input leakage current and temperature drift are the parameters which cause most rejects.

Generally, the digital integrated circuit supplier employs a correlation technique that uses an extended V_{CC} voltage range for dc and functional tests at room temperature (25°C), instead of the normal V_{CC} specified limits at both temperature extremes. The correlated V_{CC} values run well below and above normal minimum and maximum values respectively and depend on such design factors as the number of V_{BE} and V_{CE} drops, etc., in the circuit. A typical device might use 4.3V V_{CC} at 25°C to correlate with normal functionality at 4.75V and 0°C (Figure 9).

This technique is very effective for commercial temperature range SSI and MSI circuits. However, the military temperature range presents a problem. SSI circuits correlate fairly well using the extended V_{CC} technique, but this approach starts to fail with some of the MSI and many LSI circuits. The reasons involve the inability of increased V_{CC} voltage performance to correlate with increases in internal circuitry leakage experienced at high temperatures. Surface leakage increases exponentially with temperature and cannot be predicted at high temperatures that device specifications require, 70°C and +125°C ambient. At the low end, 0°C and -55°C, beta and resistor value combinations prove to be too complex in large circuits to correlate with a V_{CC} voltage drop.

In terms of ac testing, SSI and MSI circuits don't change access times significantly with temperature variations. And what change does occur, is predictable. However, this is not the case with LSI devices. LSI circuits vary with temperature - the parts run hotter due to chip currents and shear chip physical size than do SSI and MSI circuits. For LSI circuits it is important that at a minimum ac tests be performed at 25°C, and preferably at temperature extremes.

Thus, it becomes clear that to guarantee actual high and low temperature range circuits (RAMS, PROMs/ROMs, ALUs and the like), these devices must be temperature tested dc, ac and functionally either by sampling (AQL and LTPD) or on a 100% basis.

FIGURE 6

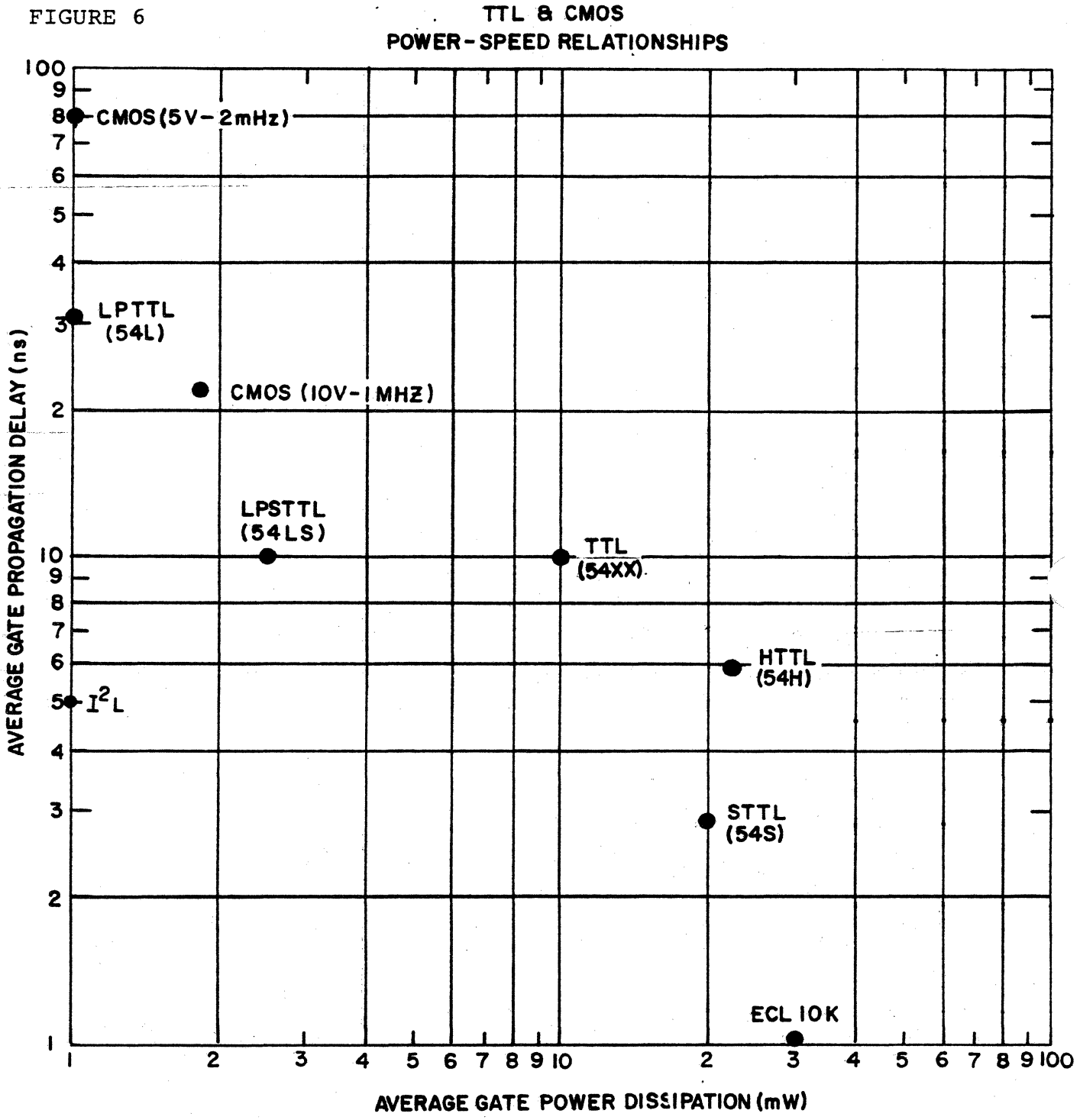
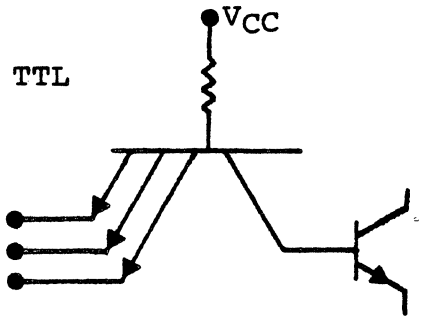


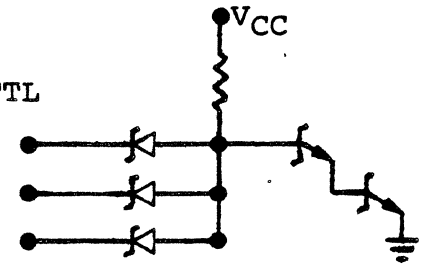
Figure 6

STD TTL



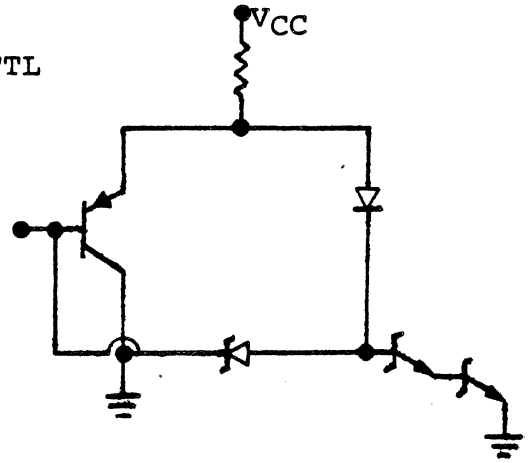
- All have same speed
- Simple Structure
- Low inverse β on Input MET

LSTTL



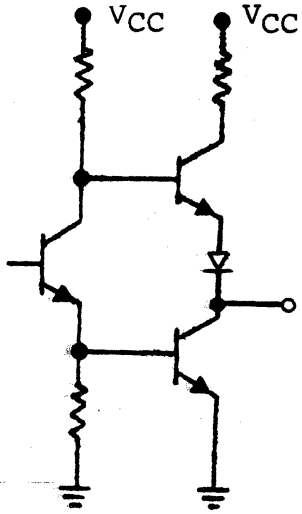
- Has some threshold problems
- Works well with high input resistor values

STTL



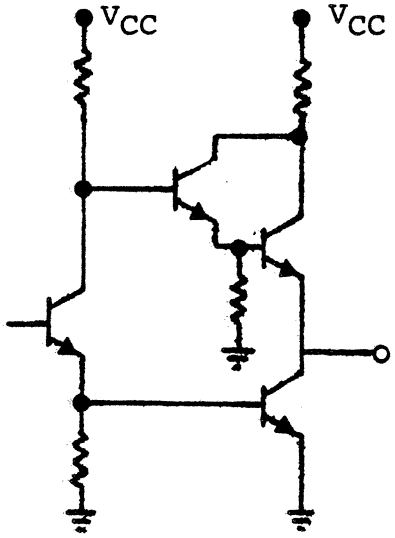
- Low I_N
- Highest Fan-In (can parallel more inputs)
- Most complex Structure
- Requires pnp transistor on same chip (vertical)

Figure 7: Types of TTL Inputs



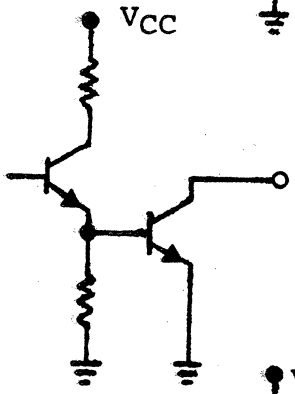
BASIC TOTEMPOLE OUTPUT

- Simple structure
- High speed circuit



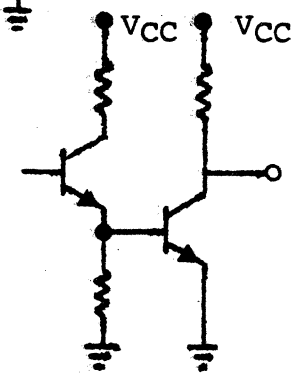
DARLINGTON OUTPUT

- Fastest rise & fall times
- More power than basic totempole structure



OPEN COLLECTOR OUTPUT

- Allows collector "OR"ing
- Slower than basic totempole
- Needs pull-up resistor



PASSIVE OUTPUT

- Allows collector "OR"ing
- Slower than basic totempole
- Eliminates need for pull-up resistor

Figure 8: TTL Output Structures

As mentioned previously, since TTL is a mature technology, no new testing surprises are foreseen. However, several key points are now presented relating to testing TTL circuits.

First, high frequency bipolar transistors can be damaged by static discharge just as are MOS devices; so similar handling precautions are required. Next, when TTL logic changes level - a high to low transistion - a current spike occurs at the threshold changeover as shown in Figure 10. This current spike results in instantaneous high power dissipation which heats the chip.

The power supply oscillation can be seen on a dc basis - the voltage keeps changing. Thus, you are observing an ac phenomena with a dc measurement. If one sets the voltage from 0 to 0.3V, no problems may be encountered. But, if voltage is set at threshold levels (0.3 to 1.5V) problems are observed and drivers cannot stabilize out. It appears as if inputs are changing - thus, confusing the circuit.

Threshold testing could also cause one a problem. The thresholds are very stable as determined by V_{BE}. However, gain coupled through the DUT (Device Under Test) can cause noise to be generated such that it masks out the threshold level and one can get an erroneous reading. The low input impedance of a TTL device is what is responsible for this potential threshold problem.

In logic circuits almost all of the faults which occur manifest themselves as the classical stuck-at-1 or stuck-at-0 conditions. In a few situations failures can assume an intermediate value, somewhere between a "1" and "0".

It is important to be able to preset the logic to a known condition before beginning actual testing. This is frequently a problem with sequential circuits as they are often wired so that they assume an unpredictable state when power is first applied to the circuit. From a testing viewpoint, a desirable implementation is to provide automatic clearing of a line to the test system, such as CLEAR or PRESET (Figure 10).

Faults which can occur in the initialization logic of a circuit are difficult to detect. As such, provision to transmit the state of these latched circuits directly to the tester is important. In the case of shift registers, the states of all the internal flip flops can be read out in sequence to verify the initialization. With N-stage counters, this can become tediously long because as many as 2^n clocked inputs are required to traverse all the states.

4.22 Emitter-Coupled Logic

Emitter-coupled logic (ECL) provides the shortest access time of all semiconductor technologies. Since it is a time-consuming process to bring a transistor out of saturation, performance at this speed is achieved by preventing the transistors from entering into the saturation region. Thus, ECL is a form of circuitry in which transistors are switched between two well-defined levels in such a manner that they never saturate; instead, the transistors remain in the active or current mode of operation. Switching is accomplished by means of a signal appearing across a common emitter

	COMMERCIAL	MILITARY
STANDARD Temperature and V_{CC} Ranges	0 - 70°C 4.75 - 5.25V	-55 to +125°C 4.5 - 5.5V
CORRELATED	@ 25°C 4.3 - 6.0V	@ 25°C 3.8 - 7.2V
CORRELATION ACCURACY SSI MSI LSI	 99%+ 98-99%+ 97-98%	 97-99% 90-97% 85-95%

Figure 9: Functional Temperature Test Correlation

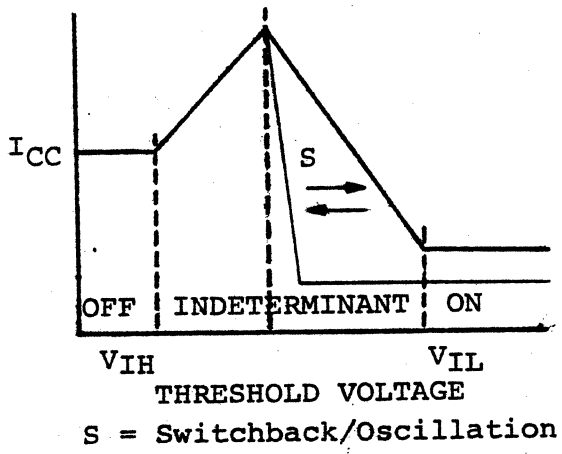


Figure 10: TTL Threshold Voltage

This also appears as a threshold oscillation problem. The Test System Driver sees the negative resistance region and depending on the severity and width of the peak, the threshold level may or may not oscillate. In oscillation, the power supplies become unstable as they go through the threshold region. This condition is process dependent and varies from lot to lot.

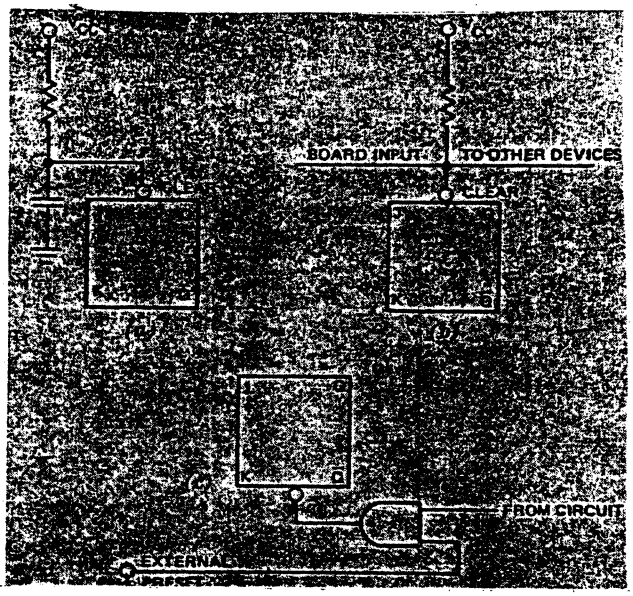


Figure 11: Initialization. A desirable implementation is to provide automatic clearing of a line to the test system, such as Clear or Preset. a) Power-on initialization scheme; b) Tester or external control of initialization; d) An external line can be used even when the Clear or Preset is used in the circuit.

resistor; hence the name. One of the major design factors to prevent transistor saturation in the ON state is achieved by using very low value load resistors R_L. This type of storage cell thus draws constant current, except during switching transients, and relatively high power consumption typical of unsaturated circuit operation is experienced.

The basic technology employed for ECL storage circuitry is similar to that of TTL: epitaxial material and p-diffusion isolation. However, the emphasis for ECL is speed, dictating low stray capacitance, close component spacing and careful control of base-emitter input characteristics. Also, the cut off frequency (f_t) of the transistors in ECL circuits must be higher than for TTL, necessitating extremely shallow and narrow base regions in ECL circuit transistors. All of these considerations cause added process complexity for ECL. Double-level metallization is required, but metal migration is a more severe problem in ECL circuits than in TTL circuits because of the higher current values experienced with ECL.

In the basic ECL circuit of Figure 12, the three input signals, A,B,C, can be either at -0.8 or at -1.7V. Only when all three are at -1.7V can the reference transistor Q_4 conduct - at which time its collector voltage drops to about -3.3V, from near ground. The emitter-follower stage Q_6 returns these levels to those of the inputs, permitting the circuit to drive another like it.

At the same time, the collectors of the input transistors, electrically common, are complementary to the reference transistor's collector. Another emitter follower provides normal signal levels from this point. Thus, the circuit has two outputs that are always complementary except at the moment of transition. At no time is any conducting transistor saturated, which accounts for ECL's speed capability.

With the convention that -0.8V represents a logic "0" and -1.7V a logic "1", this circuit performs the AND/NAND function - AND from the output at Q_6 and NAND or NOT-AND from Q_5 (Figure 12). The OR function is obtained by connecting the emitter-follower inputs to similar points in another circuit.

No inverters are needed when ECL circuits are used because the logic block that produces any given function also produces its complement. And both emitter-follower outputs can be designed to drive as many similar circuits as desired, reducing the need for special power and line drivers that are often called for by other logic families.

The high speed aspect of ECL tends to create significant voltage and current transients. To overcome them, the designer must lay out his printed circuit boards to include microstrip transmission lines, and he must make sure the circuits are properly grounded, although sometimes he may try to live with the transients or try to control them with simple diode clamps.

The testing of ECL logic circuits involves millivolt, high accuracy, low noise testing. In testing ECL devices there are several points to remember. First, the speed or access time of ECL devices cannot be readily measured on automatic test systems since test system inaccuracy or error band (±5nS) is generally greater than the ac parameters being measured,

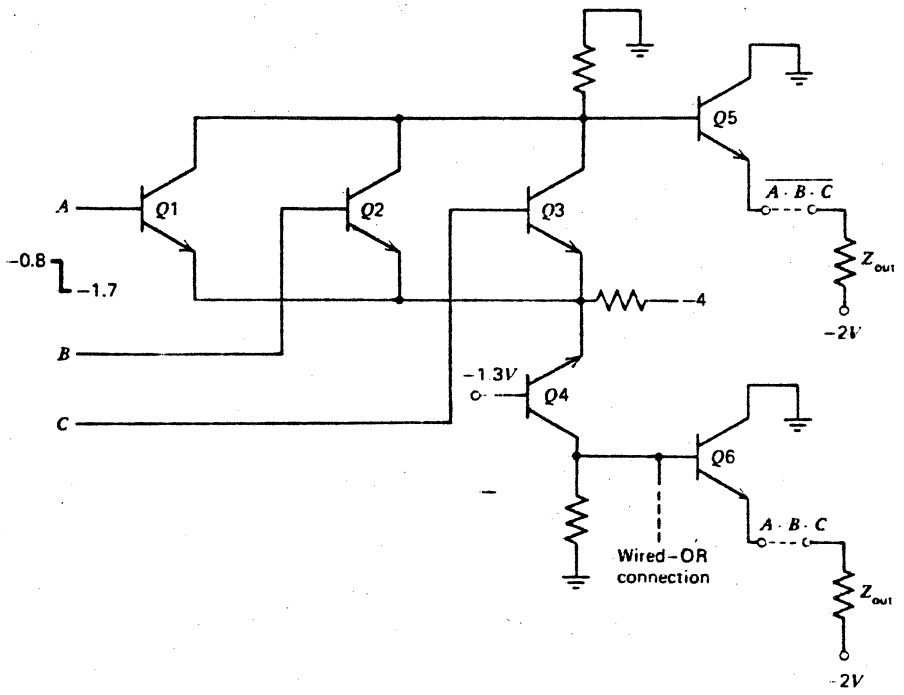


Figure 12: Basic ECL circuit

1-2nS or less. Secondly, threshold cannot be tested. Measuring leakage current is not a problem. A basic incompatibility exists between parts from two different suppliers. Since ECL is a very high speed logic, power dissipation (power supply current) and chip heating can be a problem. Different supplier's parts have different temperature coefficients. Thus, you must make sure which supplier's parts you are testing and to what specifications you are testing them to. Then each supplier's part differs in speed as well. If your design mixes parts from both suppliers (each supplier has different timing conditions), system timing will be critical.

4.23 Bipolar Memories

TTL SSI and MSI circuit functions are mature and well understood. Consequently the testing of these is straightforward with no significant problems being presented by the technology or function. The overall incoming inspection, electrical test reject rate has stabilized at a respectable 0-3% for all functions. However, LSI functions both bipolar and MOS present new and exciting test problems and, thus, deserve greater attention. The predominant area of LSI growth and circuit innovation has been in circuits with MOS technology. However, advances in bipolar technology namely the Schottky process, oxide isolation, walled emitters, ion implantation and integrated injection logic has brought forth a rejuvenation and proliferation of high performance bipolar products.

4.231 Bipolar RAMs

4.2311 Bipolar Memory Cells

Bipolar memories for use in high speed applications, essentially use high density, monolithic versions of the familiar bipolar transistor cross-coupled flip-flop. Although faster than MOS, they are somewhat more expensive to manufacture and consume more power. They also tend toward lower packing densities (although bipolar memories with high packing densities - rivaling those of MOS - are being produced), resulting in more costly system construction. One problem in increasing this density is isolating individual transistors from one another. Conventionally, this is achieved using reverse-biased p-n junctions, but these require more space and have higher capacitance than alternative insolation means.

Recent improvements in packing density have made bipolar memories competitive with MOS types, particularly in applications requiring higher speeds. Further advantages of bipolar devices include simplicity of the system peripheral circuitry required and compatibility with bipolar logic. They are well-suited to high speed scratchpad or cache memory applications in large computers.

Bipolar memories are manufactured by processes similar to those used in logic circuit production - notably transistor-transistor logic (TTL), emitter-coupled logic (ECL), and integrated injection logic (I^2L). Gold doping to reduce transistor recovery time, and Schottky diode clamping to prevent transistor saturation are used with TTL configurations to increase speed. On the other hand, ECL, though somewhat more difficult to manufacture and more costly, does not saturate and is, therefore, inherently

faster. ECL memories are suitable where cost is secondary to very high speed. Complex process variations to achieve the fastest possible performance have been introduced.

To produce significantly faster memories than those built with standard TTL or ECL, complex bipolar techniques are required. This involves an extra diffusion and two layers of aluminum (to reduce interconnection resistance). These approaches produce extremely fast, high cost memories. For many applications that need highest speed performance, no other technology can do the job, so complex bipolar will remain a significant RAM technology. When speed is the prime requirement, the ECL circuit form is used and can easily be made TTL compatible.

The basic storage cell for both bipolar and static MOS memories is the bistable flip-flop (Figure 13). Simple, fast and generally insensitive to process variations, it offers high-yield, low-cost components.

To write into and read out of a memory cell, gating is required. Some gating techniques commonly used for bipolar cells are shown in Figure 14. Each flip-flop in a large interconnected array has a unique location that may be addressed by word and bit line signals.

In Figure 14a, the basic flip-flop has two dual-emitter transistors. One emitter from each transistor is tied to separate bit lines; the other is tied to a common word line. To read, word line voltage is raised. The current which normally flows through the flip-flop is transferred to one of the bit lines. A current sensing amplifier detects the bit line with the signal current. To write, the word line voltage is also raised, and the desired state is forced by unbalancing the bit line voltages.

The small, simple circuit in Figure 14a has been used in many of the larger bipolar memories. Access speed depends largely on current available from the cell for sensing. To maintain consistently fast switching speed, the collector load resistors R_C must not vary widely.

In Figure 14b, the circuit is particularly suitable for the Schottky process because the two gating Schottky diodes are made within the collector region of the flip-flop transistor, minimizing the cell size increase. To read a cell, word-line voltage is lowered. Signals are detected on the bit line through the Schottky diode. To write, word-line voltage is lowered. Signals are detected on the bit line through the Schottky diode. To write, word-line voltage is lowered and a large current is fed into one bit line through the Schottky diode, which simultaneously turns on the off transistor and increases the other's collector load current, forcing it to turn off quickly. Since the size of R_C does not significantly affect access speed, R_C may be large to reduce power dissipation.

A collector bulk resistor which provides a high resistance for a given area, can be used as R_C as shown in Figure 14b. The circuit in Figure 14c, popularly used in emitter coupled logic (ECL) circuits, uses two layers of metal interconnections through a single layer 128-bit ECL memory circuit.

A bit is selected by raising its word-line voltage. Writing or reading is accomplished in similar fashion to the multi-emitter in a, except that

the voltage across the selected cell is higher than across the unselected one, thus large sense current is available from the selected flip-flop. The voltage across unselected flip-flops is quite low, maintaining low standby power dissipation.

A novel variation applicable to all these bipolar processes is oxide isolation, a common form of which is called isoplanar. Using silicon oxide to isolate the various on-chip components results in higher packing densities and slightly higher speeds. Other bipolar processes achieve electrical isolation of the circuit elements with reverse-biased p-n junctions, but they occupy more space and have higher capacitance than junctions built with oxide isolation. New N-channel MOS circuits are almost as fast as oxide isolation circuits, yet considerably less expensive.

However, the combination of a walled-emitter (subnanosecond ECL) technique and oxide isolation process should provide higher density and faster (20 ns access time) random access memories. (This combination should also produce 4k bipolar RAMs with essentially the same chip size as NMOS Dynamic 4K RAMs.)

4.2312 Memory Organization

Basically a RAM requires that any location within it be reachable or accessible without regard to any other location in any order. At the selected location, data may be written (stored) in the memory or read (retrieved) from it. Between the time data are written and read, they must be reliably stored.

Semiconductor RAMs are always read/write - you can enter or remove data in any cycle. Semiconductor read-only memories or ROMs, on the other hand, generally are not read/write devices.

Both should be distinguished from serial memories, like shift registers, first-in first-outs, and so on, where bits can be accessed and recycled only serially.

Semiconductor RAMs are fabricated using either bipolar or MOS technology. Bipolar memories are typically 1.5 to 3 times faster than n-channel MOS devices and an order of magnitude faster than p-channel MOS devices.

The typical RAM is composed of a matrix of storage cells arranged in an X-Y coordinate system (Figure 15). Address bits A_0, A_1, A_2 and A_3 define the row in which a particular memory cell is located while A_4 through A_8 define the column. Associated with each column are the driving and sensing means for carrying out write and read functions. In the write operation, data are transferred from the input to the addressed cell, erasing those previously written. Similarly, the state of the addressed cell is sensed during a read operation. If data are destroyed during a read cycle, they are automatically replaced on completion of that cycle.

Decoders for addressing X and Y lines in the storage matrix can be seen together with an I/O block which houses read/write circuitry for interfacing the memory with external circuits.

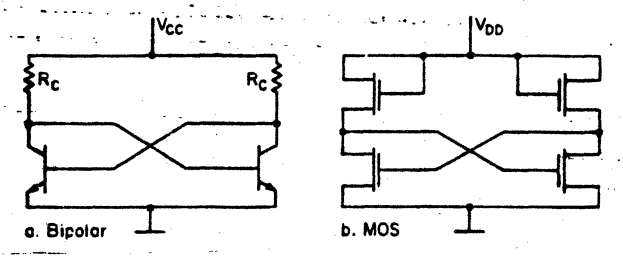


Figure 13: Bistable Flip-Flop. The bipolar inverter is made of a transistor and a collector load resistor, R_C. In MOS R_C is another MOS transistor, which provides a small area non-linear resistor when its gate is tied to its drain.

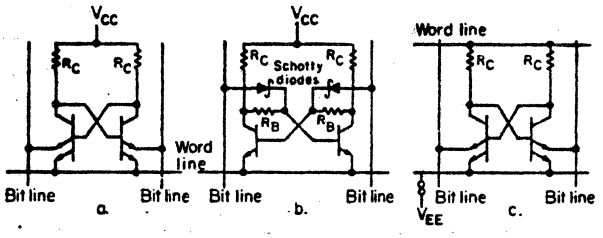


Figure 14: Gating techniques for Bipolar Cells

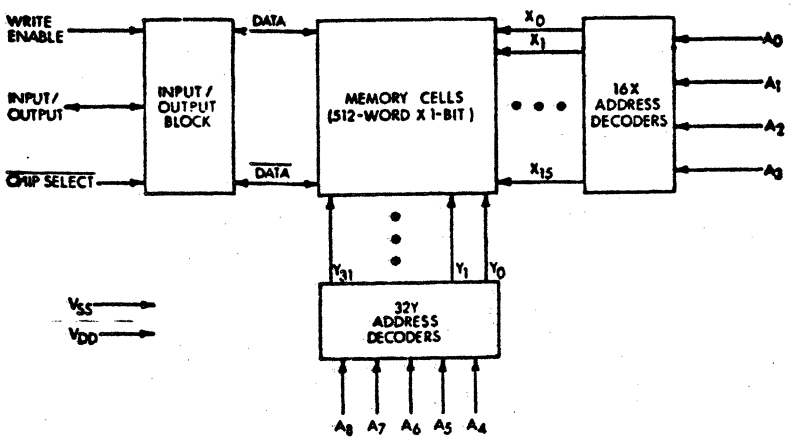


Figure 15: Block Diagram of a Static RAM

Bipolar RAMs are extremely simple to use. The devices have only four types of inputs and one type of output:

INPUTS	OUTPUTS
Addresses	Data Out
Read/Write	
Chip Selects	
Data In	

Inputs

The addresses select which bit location is to be read from or written into. For example, a 1024x1 RAM has 10-binary address lines or 2^{10} which is 1024 different binary address locations. A 256x1 RAM has 8-address lines, i.e., 2^8 or 256 locations, etc.

The read/write signal is a single pin, and controls whether one writes into or reads out of the device. Most bipolar TTL RAMs have a logic "1" or high on this line for reading and logic "0" or low for writing. Timing is simple - the write condition is the only time when one must be careful not to destroy information in the memory. All other inputs should be stable or at their desired conditions before the read/write signal is put into the write condition. The other inputs should also be held for a short time after the read/write signal returns to the read condition. The above care will guarantee that one will not inadvertently write into a previous address or a subsequent address.

The chip selects or select lines are like addresses. They control which of the 1024x1, 256x1 or other RAM devices in an array are operated upon. Chip selects are usually logic "0" or low to select the memory device and logic "1" to de-select. If a memory is de-selected, it will not permit writing or reading.

The data-in is as named. It is the condition or logic of this line that will be written into the addressed cell when the write pulse is applied.

Outputs

The data output is a standard TTL or ECL output available in open collector or Tri-state (TTL), or open emitter (ECL) and merely handles data out of the addressed cell when reading with the chip selected. For a Tri-state device, data out goes to the high impedance state when the memory is de-selected.

4.2313 Test Problems Related to Circuit Design

4.23131 Cell Matrix

The cell matrix, shielded by peripheral and support circuits, is the most difficult problem area to test or analyze. Cell matrices, no matter which technology is used, all have the common problem of dropping bits. Starting with the simplest matrix, the cross-coupled bipolar cell; let us examine

some failure modes and ways to uncover them. Bipolar RAM circuits are fast, but dissipate high power. Efforts to reduce matrix power result in a common design trap today - design instability. It is common, at least in the early stages of design, to see devices display cell instabilities. Cell currents have become so small that minute variations in word line/bit line currents can disturb the cell. Trade-offs have to be made between total power versus word-line and bit-line currents.

Processing variations affect device betas, gain resistor values and leakage currents, and all these must be considered. When this problem has been identified, a mask change is required to increase bias currents to obtain matrix stability. In the MOS area, cell information can also be lost due to improper bias.

Dynamic MOS circuits have their own unique problems. Here, information is stored on a gate capacitance and a periodic refresh is required for data retention. In these designs, extra support hardware is required to perform the refresh function. Special recirculation loops or an additional column to keep track of the true or complement row state further complicates the matrix. The test problem becomes that of a black box within a black box. Device matrices can grow to be a massive piece of hardware with inherent crosstalk, parasitics, and leakage.

Shorted or open memory cells are easy to detect. If any cell shorts internally, it cannot function and is detectable by writing and reading an all zeros and an all ones pattern.

Adjacent cell shorts are also easily detectable. Depending on what is shorted, the shorted cells must contain either the same or complementary data. An all ones or all zeros test will detect complementary data. Identical data will be detected with a checkerboard, since shorts between cells touching at a corner are extremely unlikely. If this possibility exists, the shorts can be detected with horizontal bar and vertical bar patterns.

Because of its sophisticated nature, testing of the matrix is a tedious job. It is buried behind a variety of support hardware making evaluation difficult. Temperature, voltage and timing variations and complex patterns are useful in locating matrix problems. It has been found that temperature and voltage are good tests unless the device includes well designed temperature and voltage compensation. When this condition exists, extensive timing and pattern testing is required. It is difficult at times to determine the exact location of a failure because it may appear to be in the matrix when it is really in the I/O control. It is one thing to have a fully functional matrix, but another to correctly get information in or out.

4.23132 Sense Amplifier and Write Circuitry

Sense/Write circuitry and bit-line(s) form a two-way street since information must pass through bi-directionally. In the case of a bipolar device, information may be lost during transfer from the cell to the outside because of sensing problems. Device power considerations may be such that insufficient current is left to reliably sense the state of the cell. A marginal design will not always display a catastrophic failure and can be hard to detect.

Information storage presents its own peculiarities. In order to read the correct data, information must first be properly written. Bit line switch current must be sufficient to reliably change the state of the cell. Proper write timing must also be maintained. To reliably write a location, current transitions on the bit line must be properly timed. Cells may be left in the wrong state in circuits with poor write control circuitry or those having slow rise/fall times.

Dynamic MOS devices further complicate testing problems. Timing and charging currents greatly influence the success of reliably reading or writing the matrix. As an illustration, during a read of the 1103, bit lines must be charged, data transferred around the refresh loop and then out the data buffer. Information may be lost at several spots along the way. Writing is accomplished by impressing data on the bit line and overriding the data previously on the bit line. In either case, timing and charging currents provide additional chances of failure. Other problems may be attributed to voltage, temperature variations and pattern sensitivity.

From the outside, it becomes extremely hard to pinpoint the exact location of functional failures. Temperature, timing and voltage variations are effective methods of screening out faulty devices. Each of these parameters interacts, causing some ambiguity in determining which is the cause of failure, and their application requires extensive and time-consuming testing. Of particular interest are the timing relationships between the write enable, data in and the matrix X-Y decoder. Timing becomes an even more sensitive parameter when the Y-dimension decoding is an intricate part of the read/write circuitry. In this case, special consideration must be given to the Y-dimension circuitry.

4.23133 Decoding Circuitry

The decoding circuitry controls the matrix, allowing information to be stored and retrieved in an orderly fashion. Semiconductor memories are organized into arrays so that a group of cells are shared on a common line or pair of lines for sensing and writing in one direction and on a common selection line in the other direction. This would be a linear organization. The sense lines are then usually multiplexed via another group of selection lines. There are variations to this scheme, but the linear array usually results in the smallest cell area. This array organization is shown in Figure 16. Rather than having the multiplex switch common to a column of cells, it could be included in each cell giving an internal X-Y organization as shown in Figure 17.

Most semiconductor memory cells exhibit all or some of the following properties. If two or more cells are selected at the same time and a write occurs, it is likely that both cells will assume the correct state. If two or more cells are selected and read at the same time with identical data in each cell, it is likely that the output will assume the correct state.

From this information, it is apparent that a test such as write all ones, followed by read all ones, then write all zeroes followed by read all zeroes, is essentially useless. For example, an array could conceivably have totally nonfunctional decoders with one memory cell selected and connected to the

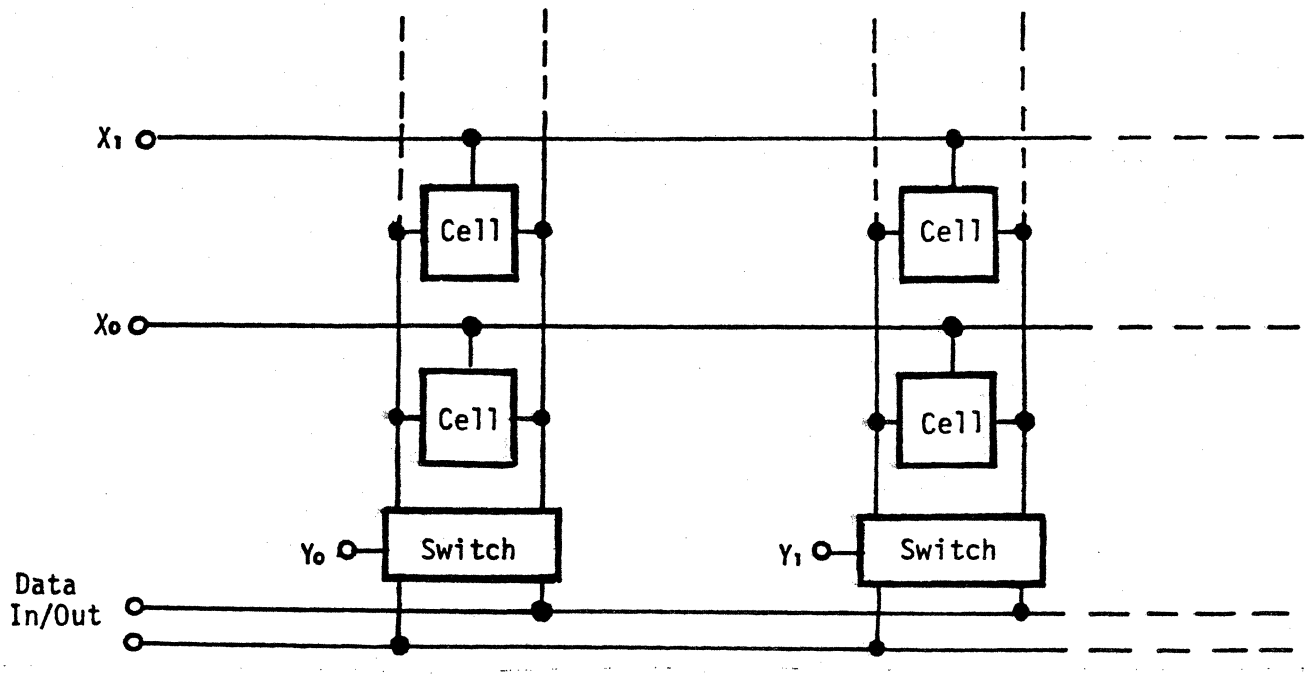


Figure 16: Linear Organization with Multiplex

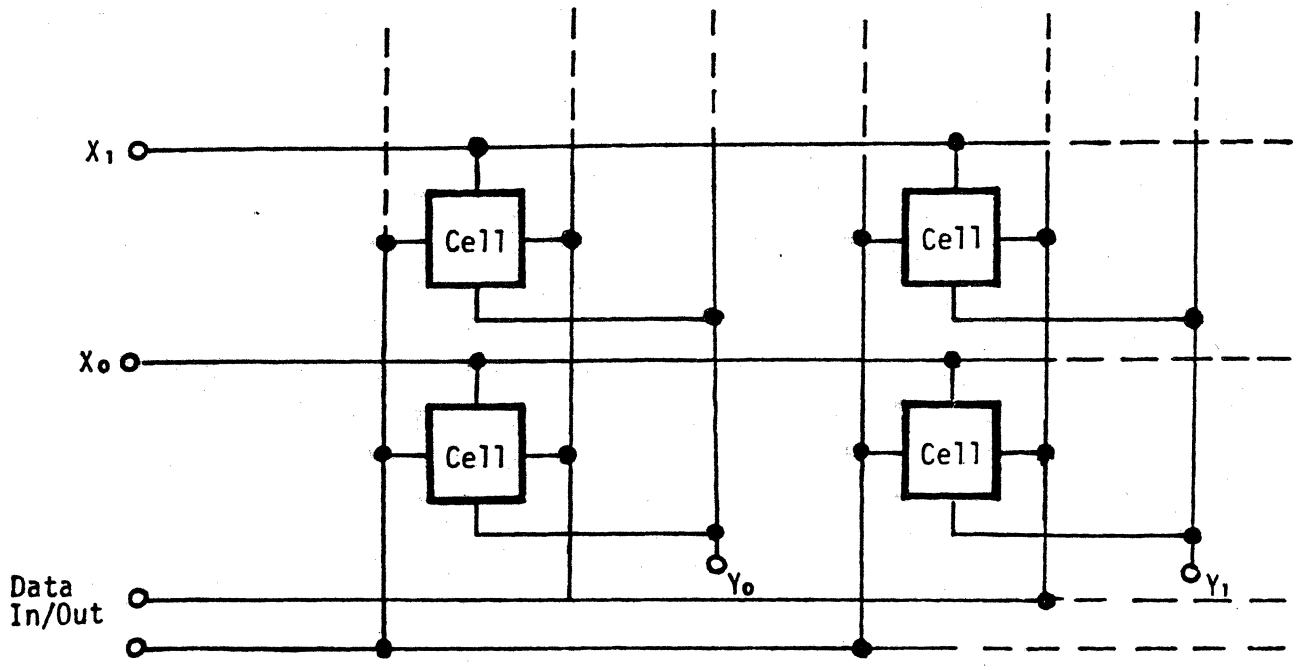


Figure 17: X-Y Organization

input-output lines and still test good with this test.

Most memory cells, if multiply selected, will lose correct data. This is true because writing and reading is usually performed on the same line or pair of lines. Selecting two or more cells at the same time shorts them together via the sense-write line(s). They will then assume the same state. There are many methods to keep this from happening with correct design, but processing problems or defects can cause them to occur. Tests for this condition can and should be provided.

Simple decoders used in bipolar arrays are fairly immune to temperature variations. Timing skews constitute the foremost problem in decoders. The size of the array will greatly influence decoder skew since the larger the array the greater the number of logic levels that are required to perform the decode function. Skew in the decoders can cause multiple or partial selection within a matrix during both a read and a write operation. When this occurs the results are either a slow address to data access time, disturbance of a previously stored bit, or both. RAMs have been seen which successfully passed required tests, but were later found to have faulty decoders which restricted operation to half the matrix.

In some designs, this multiple selection is eliminated by clocking the decoder outputs so that they always unselect before selection. In others it is taken care of by careful design of decoder gates and address inversion circuitry, such that outputs unselect before they select. Some designs allow for some multiple selection, either two cells in a linear select or four cells in an X-Y organization. Unfortunately, changes in temperature and power supply variations can drastically affect the results, as well as the operating frequency. In addition, multiple selection must occur with one of the multiple selected cells in the state opposite the others to cause dropping off a bit. Finding these problem areas usually requires lengthy N^2 test patterns.

MOS devices can have decoder skew problems, although several available designs use on-chip register and clocking to eliminate skew. Skew is reduced, but often at the expense of special timing clocks. Input level shifting or special clock buffers can influence device operation and in each case will require special attention.

Some devices will fail due to internal races between buffers, decoders and clock circuits. Decoder problems can be uncovered by using address patterns which are unrelated to powers of two, timing variations and temperature. Under no circumstances should a random access memory be exercised only with a sequential addressing scheme. An absolute minimum requires a complementing pattern which will give the maximum number of logic transitions. Special attention should also be given to critical timing and input levels.

Address decoder failures can result in inaccessible cells, cells with more than one address, or more than one cell with the same address.

Notice the distinction made between the RAM cell, the physical piece of silicon in which the word is stored, and its address, the code word used to open that cell. The test strategy is to create a pattern which identifies each location, and establishes that each address opens one and only location.

4.23134 Access Time Measurements

The problem with access time measurements is that they are pattern sensitive: access times depend on the sequence in which the memory cells are addressed.

The reason is that addressing a given memory cell is not a completely independent act. It consists of changing a previous address to the present one. When a given cell is addressed, two independent events must each be completed within their own specified time:

- The previous memory cell must be closed (disconnected from the I/O bus).
- The present memory cell must be opened (connected to the I/O bus).

4.23135 Example of Pattern Dependency in a Bipolar Memory Array

Most bipolar memory arrays use some version of a multimitter flip-flop with a sense-write pair shared between a group of cells. The number of cells that may be shared on a line is a function of the signal current of a selected cell versus the error or leakage current from the unselected cells. Sensing is performed differentially. The error current is dependent on the state of the cell. The direction of the error current varies for different designs. A typical situation is illustrated for a bipolar cell in Figure 18.

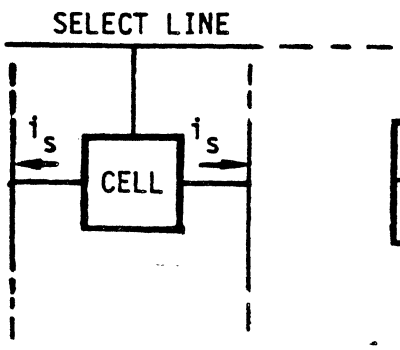
If 16 of these cells were shared on a sense line pair, the sense differential would be minimum when all ones were stored or all zeroes were stored. The error currents from the remaining cells would subtract resulting in a differential of 0.25mA. The sense difference would be maximum when one cell was opposite from the rest (15 zeroes and 1 one, or 15 ones and 1 zero). The sense difference would be 1.75mA. This, of course, is an ideal case. In actual fabrication, minor defects in cells might cause larger variations. The worst case transient change while reading will be maximum one to minimum zero or maximum zero to minimum one. This would occur when address changes occur between the location with a zero and the background locations with ones or vice versa.

These variations in current will cause a variation in access time dependent on stored pattern and address sequence. Figure 19 shows why access time varies with differential sensing. The same situation holds true for single ended sensing.

Memories that exhibit no pattern dependency on the sense currents will still exhibit similar differences in access time variations. These variations can be caused by individual cell defects, differences in drive levels for different parts of the array or system, layout variations and processing variations.

4.23136 Write Recovery Time

A write operation in one cycle can affect the read access time in the next cycle. This is due to the fact that in most semiconductor memories, the



	ZERO STORED		ONE STORED	
	SENSE 0	SENSE 1	SENSE 1	SENSE 0
UNSELECTED CELL	- .05	.0001	.0001	-0.05
SELECTED CELL	+ 1.00	.0001	.0001	+ 1.00

Figure 18

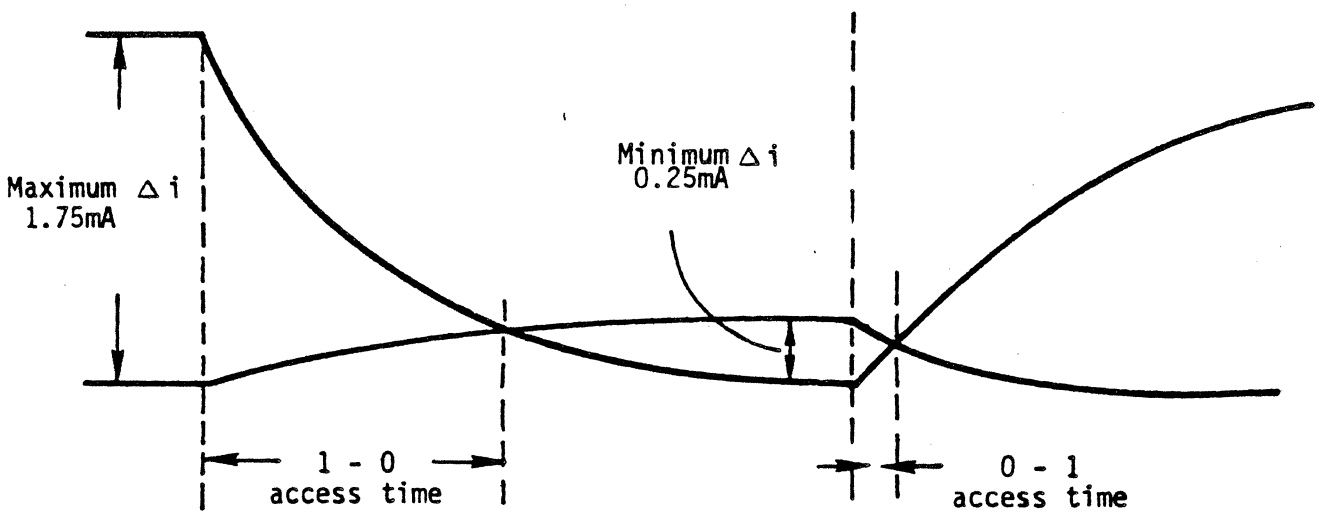


Figure 19: Access Time Variation due to Unequal "1" and "0" Level Sense Differentials

same lines are used for reading and writing. Usually, the voltage swing for writing is much larger than that used for reading. These sense lines must recover to their read level status before proper read operation can occur. In some memories, this recovery is influenced in the same manner as in the read operation.

4.2314 Memory Test Patterns

Memories require the three basic tests discussed earlier - dc, ac and functional - be performed at temperature extremes. It is generally preferable to perform the functional or pattern testing and the ac testing simultaneously.

To prove that a read/write random access memory is completely functional, the following aspects must be checked:

- Every cell of the memory must be capable of storing a "0" and a "1".
- The cell addressing circuits, or decoders, must correctly address every cell.
- The sense amplifiers must operate correctly.
- There must be no interaction between cells.
- For dynamic MOS memories, the cells must be capable of storing data for a specified time without being refreshed.

Selecting the proper test sequence and optimizing ac testing patterns, although a difficult task, is a must to achieve efficient and thorough testing.

There are many different types of test patterns that are useful for testing memories. Each has its place or use along with certain tradeoffs as to the sufficiency of the test, complexity of the test, and the test time. Certain patterns are specifically aimed at a problem area. Some of the popular test patterns are:

- Ping-Pong or Galpat
- Walk
- March
- Diagonals
- Checkerboard

In general, these patterns fall into two basic categories: They are either N type patterns or N^2 type patterns. Patterns such as checkerboard and single diagonal are N patterns. Walking and Ping-Pong (Galpat) are N^2 patterns or some multiple of N^2. The N^2 patterns can take well over 10 seconds of test time for 4k and 16k dynamic RAMs, depending upon how many

power supply levels they are run at. Using them in production drastically affects throughput rates and consequently testing costs. In order to minimize or optimize the pattern testing time, one must carefully consider the philosophy of the design of the memory being tested and take into account its topological relationships, circuit design details and interconnect techniques in the overall testing strategies.

It has been found that taking a $4N^2$ pattern was a waste of valuable test time when after studying a particular device, a 4N pattern was found that would achieve the same results; for example. Using a developed test pattern without forethought can be called a shotgun approach to memory testing.

The 1k RAM, as an example, is basically a row-column matrix of cells (i.e., cells are related to one another electrically by row and by column). The devices usually have topographically and electrically separate X decoders and Y decoders. Any test bit within the memory is most closely related to other bits in its row and column since they are connected electrically as well as bits in its four corners which are related topographically. The conditions of other bits not in these positions have very little relationship to the bit being tested, either topographically or electrically. Based on this relationship, and this model a special group of tests were designed to compare against more lengthy N^2 patterns to test their effectiveness. Using the row-column model, one arrives at a third type of pattern which can be considered for testing memories and which may be more production oriented. This type of testing would involve, for example, the moving of a diagonal row followed by the reading of the field or the moving of a bit from one position to another followed by the reading of the horizontal row and the vertical column in which the bit being tested is located. This type of testing does not represent either N or N^2, but rather $N^{3/2}$ power type testing.

Based on measurements of address access time, the ping-pong pattern has been found to be very effective in finding slow bits. This pattern, however, is a multiple N^2 pattern and extremely time consuming to run in production. The power of this pattern lies in its activity generation level, both internal on the decoders and in the data out lines. Using the row/column model as the field and the intercept as the test bit, the same level of activity is generated using only $N^{3/2}$ patterns. In other words, doing a ping-pong read, but only in row and column of the test bit before walking or moving the test bit to the next location, etc. A similar amount of decoder activity is also present in the X and Y decoders; however, they are separately activated. Since the decoders are topographically and electrically isolated from one another, it is expected that this $N^{3/2}$ pattern approach will be equally as effective as the full ping-pong pattern and will run 16 times faster (for the 1024-bit example).

A number of different patterns were designed to compare their capability of finding slow bits while function/ac testing. These are:

Checkerboard

Stripe

March

Fixed diagonal (with row/column read)

Sliding diagonal (with row/column read)

Walk (with row/column read)

Full ping-pong

The results of these tests showed that the bipolar isoplanar 1k RAMs (93415/93425) tested exhibited extremely low sensitivity of access time to the various patterns used. In all cases observed, $N^{3/2}$ patterns with row/column ping-pong reads were as effective as the full ping-pong ECL, as well as TTL RAMs. The decoder paths exercised in the fixed diagonal, although not repeated as many times, were the same as those exercised in the $N^{3/2}$ patterns.

The checkerboard, stripe, and march patterns which had only binary advancing or complementing addressing combined with mixed "1" and "0" patterns in their rows and columns were somewhat less efficient in finding slow bits.

Based on this data, a test bit opposite to all other bits in its row and column appears to represent a worst case pattern condition within the array. In addition, a row column ping-pong read of these bits combines a worst case decoder delay situation.

The overall results indicate that efficient $N^{3/2}$ tests can be devised for testing memories of this type. The exact nature of the read cycles may not be the same in all memories, but the technique appears to be useful.

4.2315 Test Results

Most bipolar RAMs display one or more of the following distinct problems: slow access time, excessive leakage current, instabilities, and temperature sensitivity. The major contributor to these problems is temperature, since it affects stability and timing in a device. Temperature generally has an adverse affect on device access time. It has been the rule, rather than the exception, that many different device types are fully functional when exercised in a 25°C environment. One such device successfully passed exhaustive testing at room temperature. It was later loaded with an all "1" pattern and left in a dc state as the temperature was elevated. With a rise in temperature, the location which was dc selected dropped to a "0". Attempts to write that location failed; the cell had assumed a permanent "0" state. A device such as this one would have been quite easy to detect, had elevated temperature been used. A circuit running close to its maximum access time at 25°C will often fail this specification at elevated temperature. Today, allowances are made for access and timing margin increases with temperature by guard banding, but how can one guard band for a functional failure? Satisfactory guard banding is virtually impossible when minimum/maximum timing, voltage margins and pattern sensitivities, coupled with minimal test time are considered. The first test which should be performed is a temperature test, and if the device basses that, then more subtle tests can be employed.

Bipolar devices are very susceptible to multiple selection, since unequal path delays are possible and nongated decoders are used. Certain bipolar RAMs, when addressed at a location containing a zero, show a positive glitch at the access time due to a slow decoder path and partial selections of locations where "1"s are stored. If the worse case address condition can be found to maximize decoder skew, then a floating "1" or "0" data pattern is a good test. A little foresight may well save valuable test time.

Electrical incoming inspection tests of a sample of 7992 bipolar RAMs in accordance with the supplier's test conditions and limits showed a reject rate of 6.9% (See section on reliability).

4.232 Bipolar ROMs/PROMs

4.2321 Technologies

Most bipolar PROMs/ROMs use Schottky processing; however, one of the drawbacks with the Schottky diode clamp is that edge effects around the metal semiconductor periphery cause higher field strengths which cause soft reverse breakdowns of the Schottky barrier diodes as discussed earlier. Extension of aluminum over the thermal oxide around the contact cut provides field plate protection which tends to minimize the field effects from the edge of the metal semiconductor junction. When designing PROMs, however, much higher reverse biases are experienced in the course of high voltage programming. Field plate geometries are not sufficient to protect against losing valuable programming current through soft, leaky Schottky reverse bias junctions. A p-type guard ring around the edge of the metal semiconductor junction is used so that the reverse breakdown now takes on the characteristics of the higher base-collector junction, BV_{cbo}. This guarded Schottky clamped transistor structure provides an adequate solution to any soft breakdowns encountered during high voltage PROM programming.

Numerous design factors effect parasitics and in PROMs they may significantly limit programming current. "Epi" resistors are frequently employed in the design of devices using a thin epitaxial Schottky bipolar process. They provide a convenient source of small geometry, high value resistors taking advantage of the higher sheet resistivity of the lightly doped epitaxial layer and the lack of isolation requirements. Minimum geometry epi resistors are narrow and normally used at TTL biases. However, they may tend to pinch off to an extremely high resistance at the high voltages used during programming causing the original circuit design to become nonfunctional.

This is due to the width of the charge depletion region increasing with higher reverse biases across the isolation epi p-n junction. PROM design must consider this pinch off effect specifically throughout the programming path. Isolation diffusions are a source of parasitics. The diffusion widths must be large enough to prevent parasitic npn action where large programming currents result in large substrate currents.

There are three technologies commonly used for making bipolar PROMs that relate to fuses: avalanche breakdown, metallic (usually nichrome) and polysilicon fuses.

4.23211 Nichrome Fuse PROMs

The earliest PROMs were made with a nichrome fuse technology. In fact, because of the known history and improved reliability of nichrome fuse PROMs, they are very popular today with Monolithic Memories, Motorola, Signetics, Fairchild and Harris Semiconductor emphasizing this approach.

A narrow strip of nichrome (Figure 20), an alloy of nickel and chromium, is deposited as a very thin film link to the column lines of the PROM. There is a diode in series with the nichrome strip, and the strip is covered with glass.

To program the cell, the conductive nichrome strip is destroyed. Several programming methods are used to take advantage of various postulated mechanisms for destroying the strip. Slow, relatively low-current pulses appear to oxidize the nichrome with oxygen from the surrounding glass, changing it from a low-resistance conductor to a high-resistance conductor. Fast, high current pulses appear to fracture the strip, and some further separation may occur from electromigration.

A platinum silicide Schottky process is being considered to minimize temperature and V_{CC} power supply variations found in aluminum silicon Schottky process.

National Semiconductor and Texas Instruments replace the nichrome link with a tungsten titanium fuse, which is a low voltage fuse technology. Titanium tungsten is compatible with platinum silicide and is easier to work with than polysilicon fuse technology.

4.23212 Polysilicon Fuse PROMs

The polysilicon PROM is very similar to a nichrome PROM, except for the fuse material. The fuses are formed from N-doped polycrystalline silicon deposited on the wafer. Figure 21 is a cross-section of the fuse in which a layer of thermal oxide is visible underneath the polysilicon. This oxide under the fuse is left after the etch process which defines the fuse and removes some surrounding field oxide.

Programming of the polysilicon fuses occurs by a melting and "pull back" mechanism similar to that observed in standard wire element fuses. One novel aspect of the cell construction is that the surface passivation layer is removed from the active region of the fuse. Because of the dimensional change in the fuse when it opens, the fuse must not be constrained by a glass scratch protection layer. Completely covered fuses do not separate well. The polysilicon PROMs have a "window" etched through the glassivation over each fuse to allow freedom for the molten fuse to roll apart and thicken. All junctions are, of course, covered by field oxide and all of the die is covered by glassivation, except the pads and the centers of the fuses.

Intel and AMD produce PROMs utilizing polysilicon fuses.

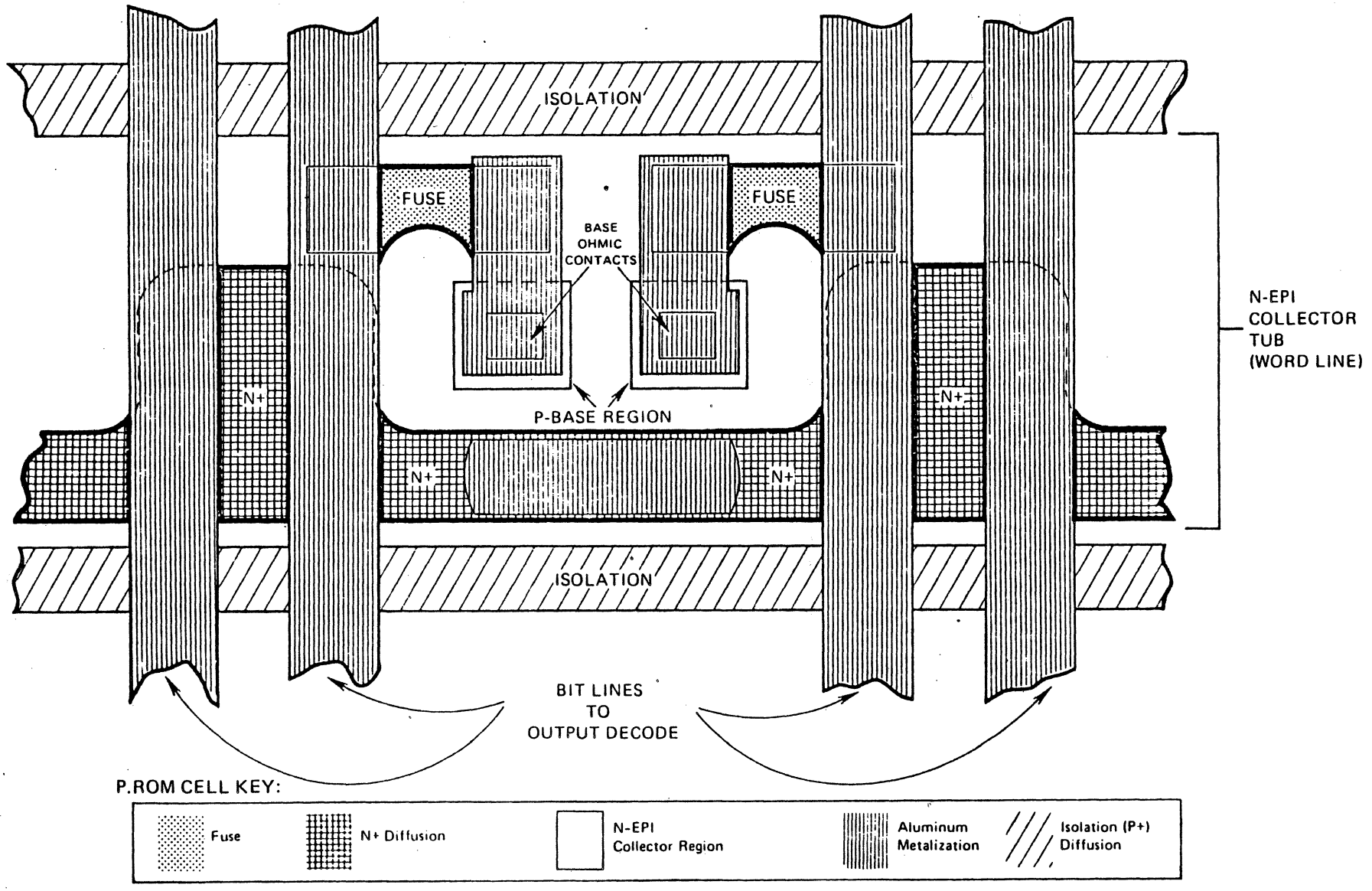


Figure 20: Typical PROM Cell

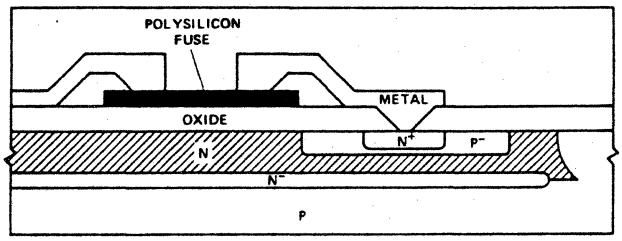


Figure 21: Cross-Section of Polysiclicon PROM Cell

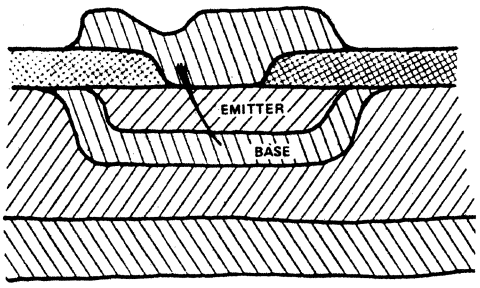


Figure 22: Avalanche Breakdown

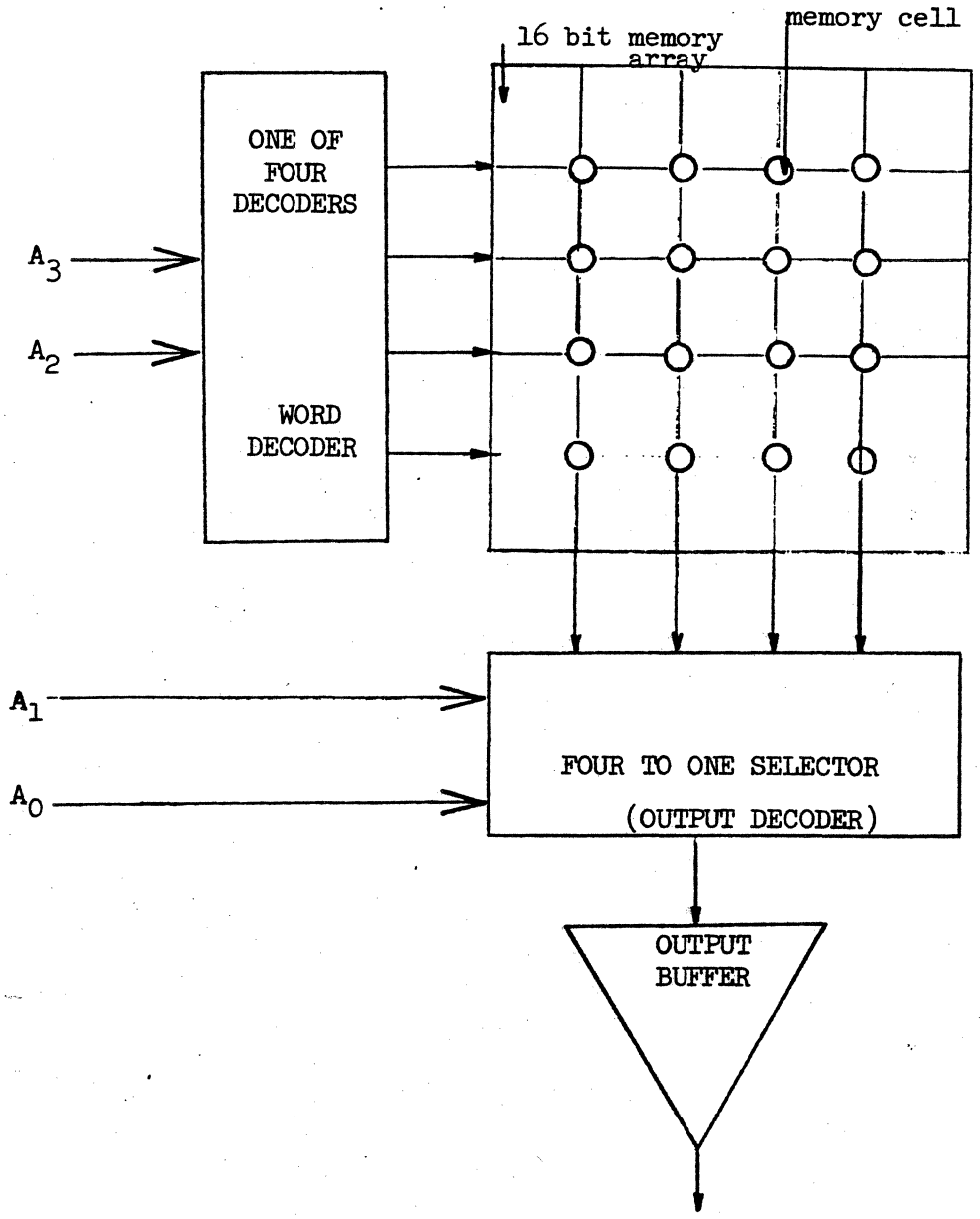


Figure 23: Functional description of ROM and PROM. PROM is sold by the supplier with all cells in the same state (high).

4.23213 Avalanche Breakdown PROMs

The avalanche breakdown (Figure 22) technique uses a transistor at each storage cell. The emitter-base diode is reverse biased when the cell is accessed and appears to be an open circuit. This is the unprogrammed state of the cell - that is, the AIM fuse is simply a shorting diode which gaped open during programming.

Programming is accomplished by applying high voltage pulses to the emitter, breaking down the emitter-base junction in the avalanche mode. When sufficient programming pulses are applied, the aluminum metal contact to the emitter starts migrating through the N material. Eventually it reaches the P base material shorting out the p-n junction and closing the circuit at the cell. Essentially, the process takes advantage of what is normally a high stress failure mode in ICs to selectively program the cells.

With this process there exists the problem of going all the way through to the substrate and getting resulting substrate leakage. Intersil was the AIM technology to manufacture their PROMs.

4.2322 ROM Testing

4.23221 ROM Device Structure

The ROM/PROM, both bipolar and MOS, is a much simpler device (being read only) than a ROM (Figure 23). ROMs have neither data inputs nor write enable, consequently, the only three timing parameters that need testing are the address access time, enable access time, and enable recovery time (See Figure 24).

A truth table of the output data at each address of the ROM is called "bit pattern" (for 1024-bits, there are 10^{300} different bit patterns). Today it is not uncommon for a supplier of ROMs to have hundreds or thousands of bit patterns for each configuration, e.g., 32x8, 256x4, 1kx10, etc. For these three configurations in RAMs, three test programs will suffice; however, the same three ROM configurations may need as many as three thousand test programs!

For ROMs, V_{OL} and V_{OH} tests are not as straightforward as in the simpler case of gates and similar devices. This point can be illustrated by the following example:

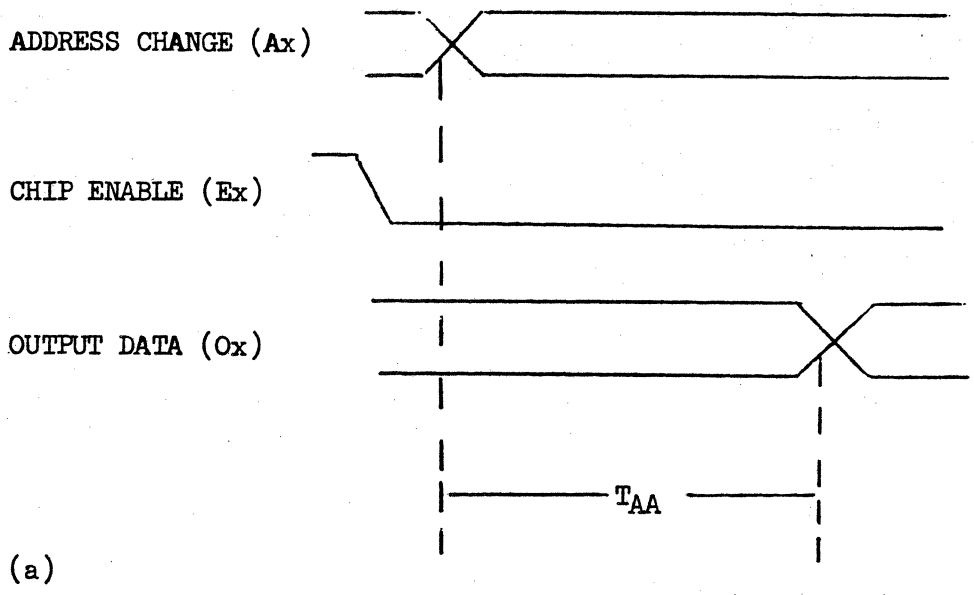
Suppose we want to test the following DC-TTL parameters

$$V_{OL} = 0.4V \quad @ \quad 16mA$$

$$V_{OH} = 2.4V \quad @ \quad -0.4mA$$

For the NAND gate (Figure 25), which is a special case ROM, it is fairly easy to generate the dc parametric test, since the input patterns necessary for V_{OL} and V_{OH} tests are known and constant.

For ROMs, the output dc parametric tests are more difficult to generate, since different input patterns are required to perform the same test.



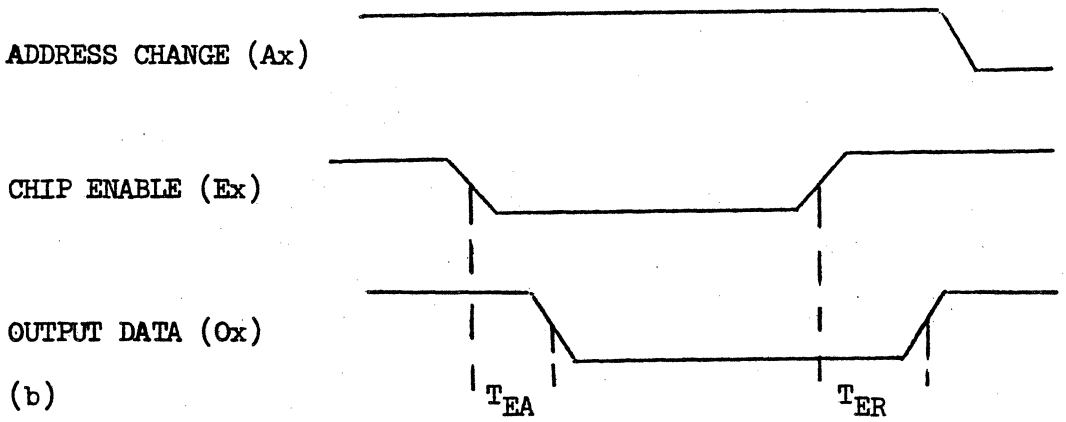


Figure 24: Illustration of dynamic testing of ROM.
(a) Address to output delay or address access time (T_{AA})
(b) Enable to output delay (T_{EA}), and Enable Recovery Time (T_{ER})

1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

TEST FOR	INPUT DRIVERS		OUTPUT PARAMETRIC	
	1	2	FORCE	MEASURE
V_{OL}	2.0V	2.0V	16 MA	0.4 V
V_{OH}	0.8V	0.8V	2.4 V	-0.4 MA

Figure 25: Generating an output parametric test for a constant truth table is an easy task.

Figure 26 illustrates this last point with the two (simplified) ROMs and the two different input patterns required to perform the same V_{OL} test.

Table 1A shows that the maximum ROM array is larger than the maximum RAM array. This is due mostly to the number of ROM outputs. Typically, ROMs are either four or eight or ten outputs wide; by contrast, a typical RAM width is only one output and occasionally four outputs.

4.23222 ROM Test Requirements

While dynamic testing of ROMs is a necessity, it is simpler than in RAMs since it requires only one programmable clock and one programmable strobe positioning. However, adequate dynamic testing requires checking all possible address transitions, rather than simply scanning them. This test is similar to Galpat and it takes $2N^2$ cycles, where N is the number of words in the ROM under test.

One ROM configuration can have thousands of bit patterns associated with it, and all ROMs from the same family have exactly the same electrical test conditions; it does not make sense to regenerate the same test program thousands of times. Instead, the test program has to be written in such a way that the unique bit pattern can be overlayed on "dummy" bit patterns without affecting the rest of the electrical specifications.

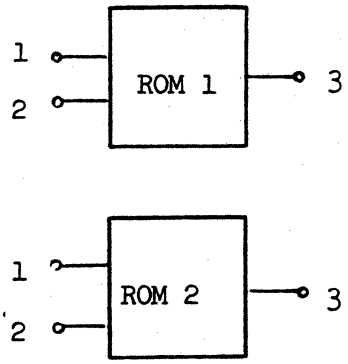
This method calls for only one master program. The software procedure of editing the new bit pattern into the dummy pattern space is called "overlay" since only an edit is required for each bit pattern rather than generating many large programs with the same dc testing repeated (Figure 27).

Each ROM will have a different address at which the output will be at logic LOW. However, to properly test the output for V_{OL}, it is necessary to test each address at which the output is LOW. In the same way the address at which the output is HIGH has to be provided by proper dc testing of V_{OH}. In both cases, it is necessary to specify the output if the ROM has more than one output. Modification of the stimuli for the output parametric test should be part of the overlay process rather than an additional lengthy patching procedure.

4.2323 PROM Testing

The bipolar unprogrammed PROM is sold by the semiconductor supplier as a blank array with all bits in generally the HIGH state. This imposes unique testing requirements.

The need to test decoding exists only for PROMs and not for ROMs. Figure 23 shows the decoding circuitry associated with any ROM or PROM. This decoding circuitry is tested indirectly in the case of ROM, while testing the expected bit patterns. If any of the decoding circuitry is not decoded, it will appear as wrong information on the ROM output. On the other hand, a blank PROM contains the same information at all addresses, so that if certain lines are never decoded, the output information will still appear valid. Thus it is necessary to find a different way of testing the decoding circuitry.



INPUTS		OUTPUTS (3)	
1	2	ROM 1	ROM 2
0	0	0	1
0	1	1	0
1	0	0	0
1	1	1	1

DEVICE NUMBER	INPUT PATTERN		OUTPUT LOW TEST (V_{OL})	
	1	2	FORCE	MEASURE
ROM 1	0.8V	0.8V	16 MA	0.4V
ROM 2	0.8V	2.0V	16 MA	0.4V

Figure 26: Generating an output parametric test for inter-family ROMs with different bit patterns requires modification of the input pattern until the output is in the desired state.

Table 1A

Comparison of array dimensions for ROM and RAM (in both cases bipolar technology was used)

LARGEST AVAILABLE SIZE BY	RAM	ROM
Number of bits	1K	10K
Number of words	1K	2K
Number of outputs	4	10
Number of enables	3	4

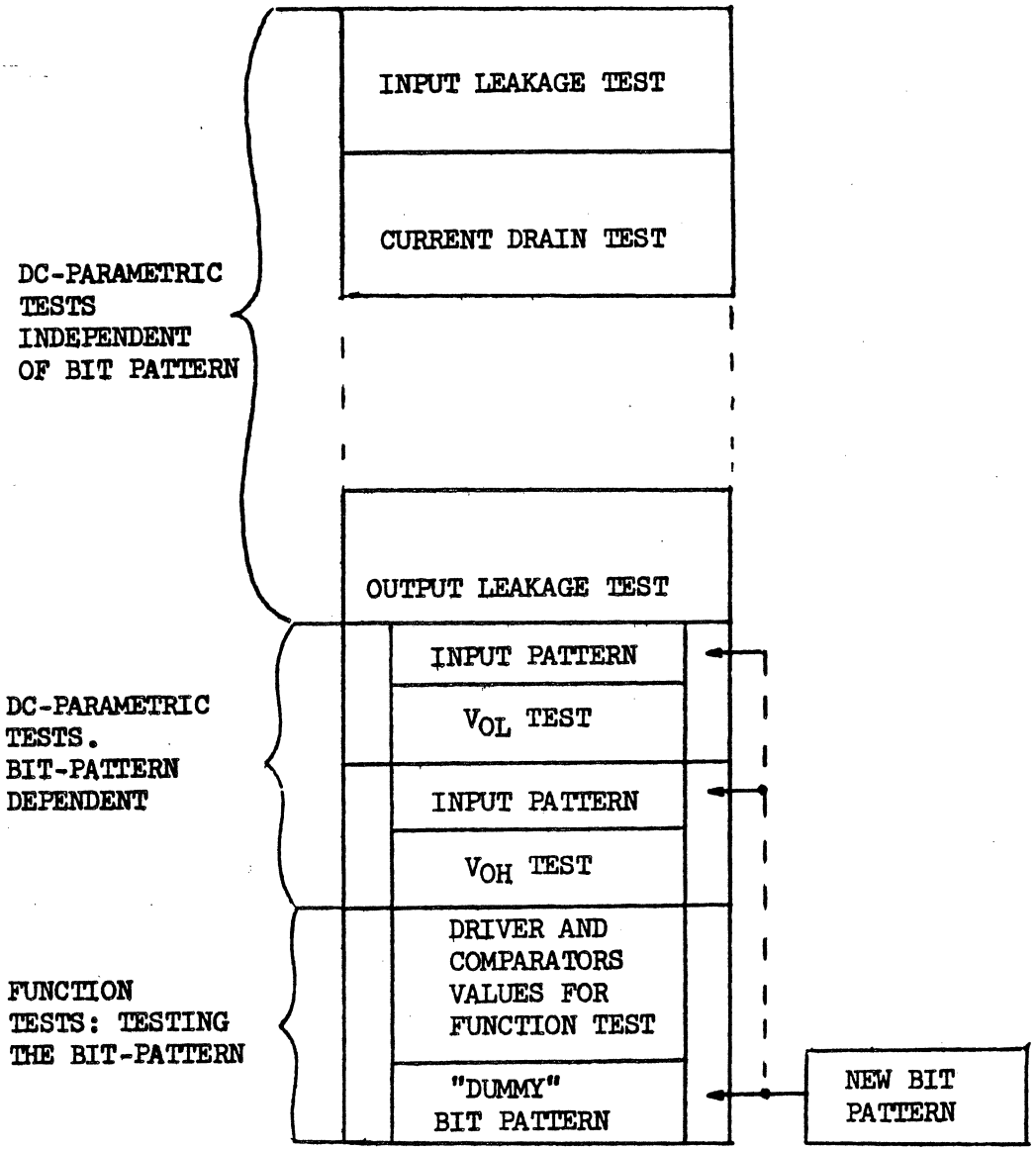


Figure 27: Example of modular program structure with an overlay of the bit pattern. The dotted arrows indicate the necessary patches for proper V_{OL} and V_{OH} tests.

Testing of the decoding circuitry requires high voltage (10-15V) on certain addresses, while scanning the rest of the address lines and examining the output data. The address line which accepts the high voltage is also used as a regular address line during the array testing. This calls for separate control of the various address lines in such a way that by a simple command, an address line can be connected either to an input driver (whose reference is common to all input drivers), or to a programmable bias supply.

Figure 28 shows a PROM with an additional row and column. The additional row contains alternate "1"s and "0"s so it is used to test the output selector circuitry. The additional column also contains alternate information and it is used to test the word decoder by selecting X_4 and scanning A_2, A_3 in all possible permutations. (In this case, the simplified PROM has only four combinations.)

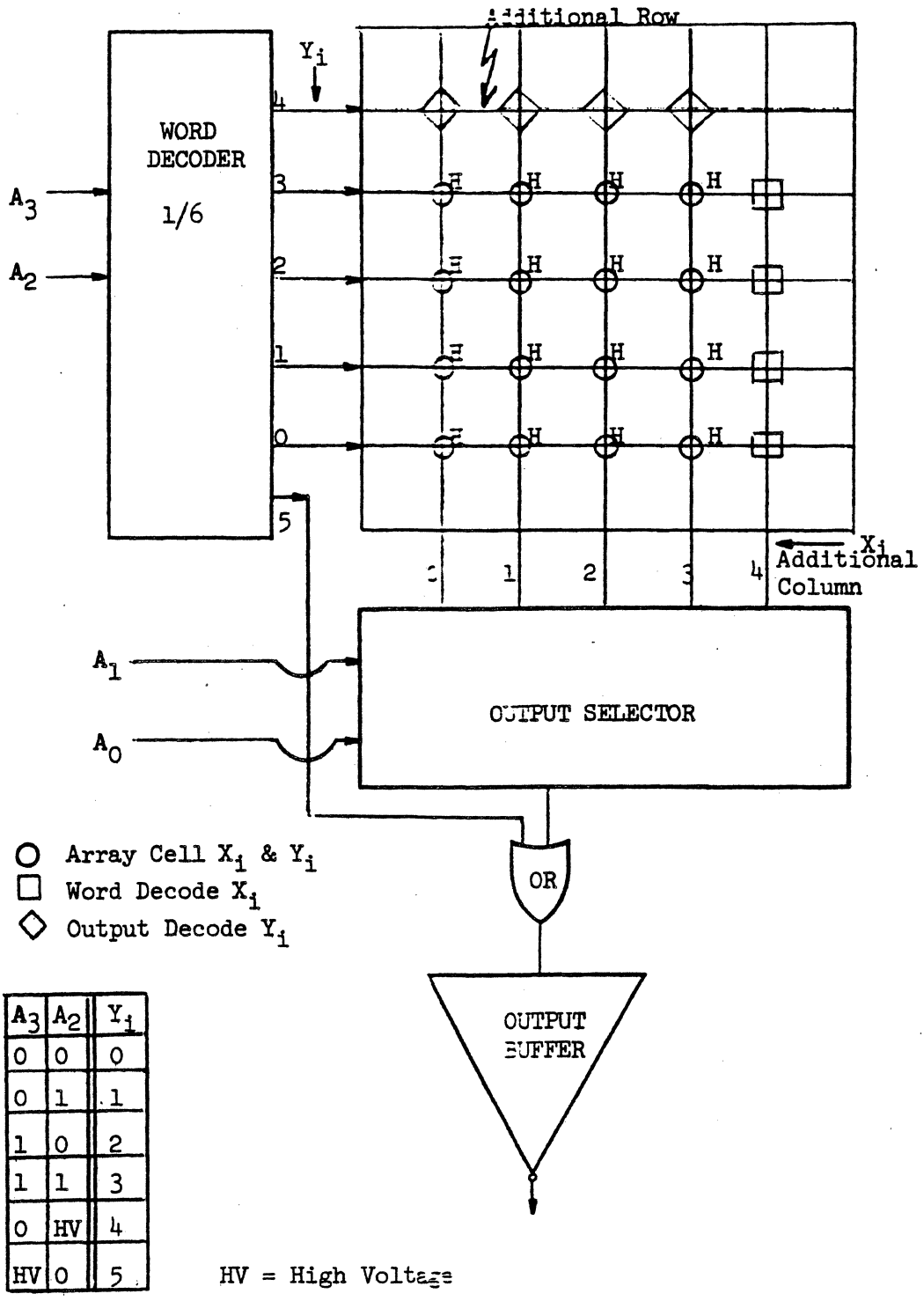
The unprogrammed PROM which is sold with all HIGHs needs to be tested for the LOW state (V_{OL}). This problem does not exist on ROMs where the random information will contain some LOWs, somewhere in the array.

Figure 28 shows symbolically the "OR" connection to the output buffer. One input to the OR gate is the same as in the ROM: simply the selected cell contents. The other input to the OR gate is unique to PROM, and it is derived from the word decoder utilizing the three state input concept. In the simplified illustration of Figure 28 when A_3 is at HIGH voltage, e.g., above 9V, the line Y_5 is selected and turns on the output transistor, enabling the tester to perform the V_{OL} test.

The key point to remember in PROM design is that the device must not only work at the normal voltage supply levels (4.5 to 5.5V for TTL), but also function at the higher programming voltage levels (typically 20-30V). Only the programming path need be tolerant of high voltages and currents; however, since most design approaches involve a fully decoded memory array matrix to minimize external pins to the outside world, one finds that much of the circuitry must consider the potential reverse bias leakages and breakdowns at the higher voltages experienced during programming. However, blowing a test fuse changes circuit dc characteristics (V_{OL}, etc.) because programming is a stressful environment.

In addition to testing, the user of PROMs is faced with the task of programming these devices. Many investigators have researched the effects of pulse width, rise time, and number of programming pulses on programmed fuse reliability. It is now well known that fuses requiring long program pulses and blowing on the dwell or flat of the pulse, have an increasing probability of failure via growback. This longer time corresponds to lower programming current requirements (Figure 29), and reflects a non-adiabatic fusing mechanism. Fast, adiabatic fusing results when programming times are held below 1.0ms. Blowing the fuse on a fast risetime guarantees high programming currents, i.e., high dEp/dt conditions, where Ep represents the programming energy.

This has been shown to favor wide separations of conductive material, nichrome, in the gap of a blown fuse. The wider the gap, the higher the dielectric breakdown of the gap. Experimental data suggests that growback



A_3	A_2	Y_i
0	0	0
0	1	1
1	0	2
1	1	3
0	HV	4
HV	0	5

HV = High Voltage

Figure 28: Functional description of PROM showing the additional column for word decoding and output decoding, respectively. The sixth line of the word decoder (Y_5) is used to turn on the output transistor to test for V_{OL}.

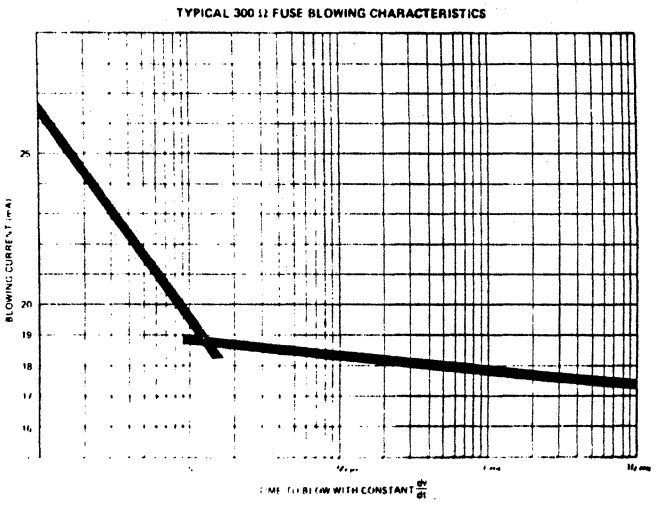


Figure 29

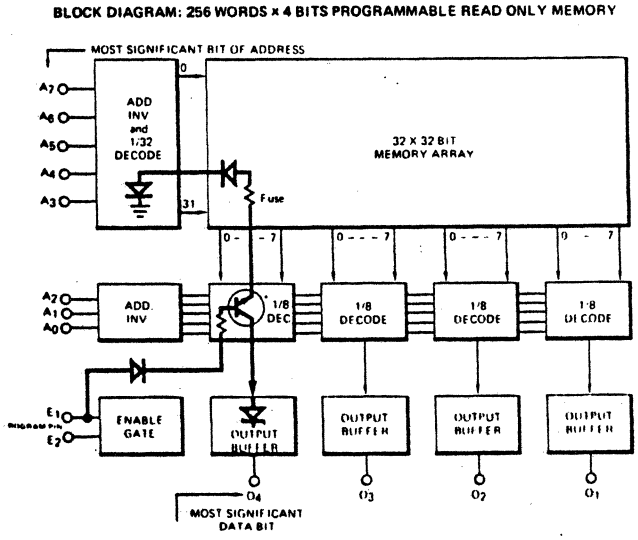


Figure 30

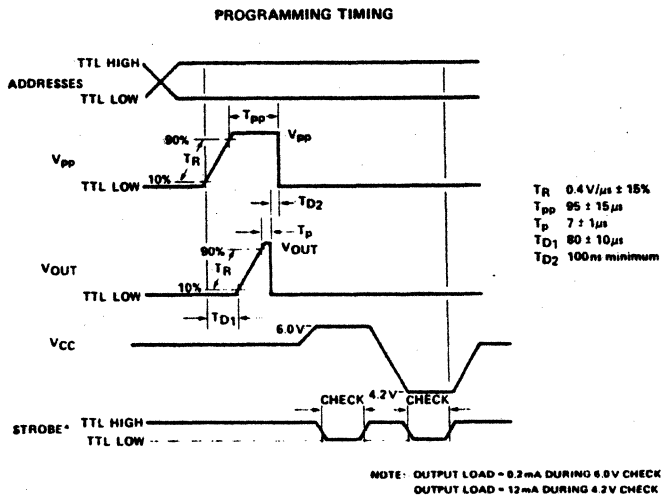


Figure 31

is nothing more than the dielectric breakdown of the nickel and chrome oxide matrix found in the gap under the influence of very high potential fields originating from the close separations of the two conductive sides of the blown fuse under biased conditions, i.e., circuit operation. Such field strengths may approach 10^7V/cm for separations of $\leq$100Å during normal circuit operation where a worst case potential of 3.0V exists across a blown fuse.

To eliminate the possibility of slow programming, a redefinition of program pulse timing is necessary. The PROM circuits discussed here use a program pin (enable) pulse (Figure 30) and an output pin pulse. The program pin pulse supplies the necessary base drive for the output decode (Bit line) multiplex transistor through which the actual programming current is directed from the output pin. It is important that the program pin pulse dwell overlap the rise and fall of the output pulse (Figure 31).

The output pulse is very short, <80µs, and almost sawtooth in shape, emphasizing programming on the rise time. The dwell, in fact, is only long enough to make oscilloscope presentations easy to read, calibrate and verify that there are no voltage spikes exceeding V_{OUT}.

Verification is performed after each pulse at correlated V_{CC} thresholds. Both extremes should be checked to guarantee the specified spectrum or window of device functional operation between the V_{CC} and temperature limits. Although the correlated V_{CC} levels shown in Figure 31 are for the commercial PROM, they have proven to be adequate for military temperature/V_{CC} range devices, so long as the parts have seen prior 100% temperature testing prior to test fusing.

The number of tests that can be performed on unprogrammed PROMs are limited, and additional testing after programming is required. Test fuses have been incorporated in PROM designs to allow the unprogrammed device to be tested functionally, checking internal threshold and decoding circuits. However, there is no valid means of performing ac testing on unprogrammed devices. One must wait until programming before testing the PROMs' ac characteristics.

Then there is the problem of temperature test correlation. This was discussed in the section on TTL circuits and applies here as well. The end result being that PROMs must be 100% temperature tested, dc, ac and functionally.

If one looks at an LSI circuit under dc test, it is immediately apparent that as little as 5% of the actual circuitry is being exercised, typically only the input and output devices. One must also test the array and all the logic circuitry involved in decoding that array, thereby guaranteeing internal thresholds, as well as those visible at inputs and outputs.

On an unprogrammed PROM, the supplier must perform 100% temperature screening before test fusing such that the test bit line and word line are used along with its pre-programmed pattern. This checks both the output (bit) decode and the address (word) decode circuitry. After test fusing this becomes impossible to perform, since no pattern remains to be interrogated.

Testing the actual array at both temperature extremes is accomplished by performing the I_{CEX} or V_{OH} leakage tests at every address location with the circuit enabled. Since all bits should be in the HIGH state in an unprogrammed device, the output should be off (high). If the circuit was designed in the reverse manner so that the output is LOW for an unprogrammed bit, V_{OL} should be tested at every address location. In the latter case, although low V_{CC} and low temperature should be worst case conditions for V_{OL}, it is important to check both sets of extremes as the enable circuit may be sensitive at the high temperature and V_{CC} extremes, causing a malfunction in which the outputs are disabled and reflect a HIGH, off logic state.

It is recommended that 100% dc and functional testing at temperature extremes be performed after programming. The majority of incoming test failures with bipolar ROMs/PROMs are V_{OL}, V_{OH}, I_{CC}, t_{AA}, and output lakage current rejects in addition to unprogrammed bits (for PROM). It is mandatory that electrical tests be performed after programming at temperature extremes.

Tests conducted on several 32x8 PROMs showed that the MMI 5331 is less susceptible to glitch problems than the Signetics 82S123, Texas Instruments 54S288, Intersil Im6510 and Harris 7603 PROMs.

4.3 Linear ICs

The testing of Linear Integrated Circuits (LICs) has presented a perplexing problem to many users, primarily because they don't understand how the devices are constructed; they don't understand how the devices operate; they don't understand the terms used to identify device performance; and the supplier's data sheet is not consistent with a given application.

Up until recently, LICs used a form of bipolar technology to achieve the desired performance characteristics; however, now bipolar technology is combined with MOS or CMOS technology and the technique of ion implantation to obtain high performance LICs.

The three largest categories of LICs, based on usage or for which users perform receiving/incoming inspection tests, are operational amplifiers, voltage comparators and voltage regulators. Each of these will be treated in this section.

4.31 Operational Amplifiers

4.311 Technology

Early op amps made use of lateral pnp transistors (Figure 32) to solve dc level shifting problems in design. These monolithic transistors have relatively poor f_T resulting in limited overall frequency response in the op amp. In addition, bipolar transistors (when biased for good frequency response) make the input current relatively large. Thus the op amp input circuit shown in Figure 32 limited the op amp speed and presented a high bias current.

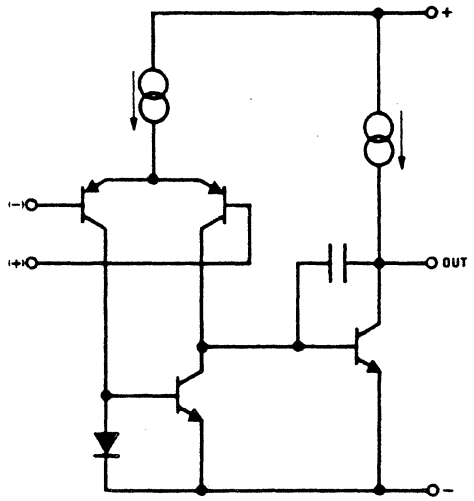


Figure 32: Lateral pnp input circuit

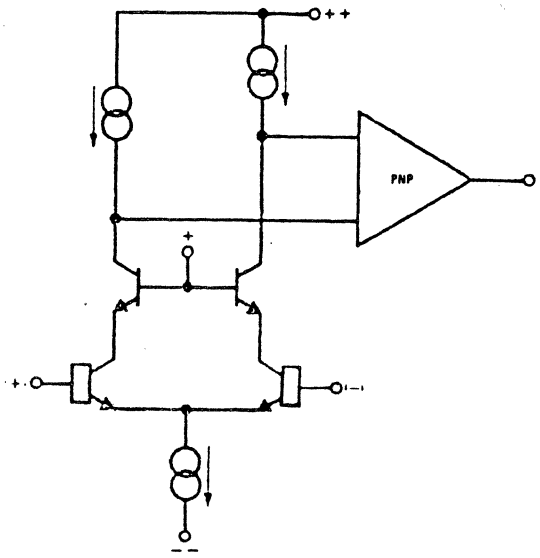


Figure 33: Super Beta Input Stage

Most first generation IC operational amplifiers were unsuited for applications involving high impedance signal sources. The high input currents of these early devices were just not adaptable as active filters, voltage followers, integrators, summing amplifiers, sample and holds, high impedance transducer amplifiers, and a few other general purpose applications.

Three circuit solutions have been advanced to solve the input impedance and offset problem. They are bipolar super-gain punch-through transistors; bipolar Darlington pairs and triplets; and the field effect transistors.

The super beta npn transistors first announced in National's LM108 op amp (Figure 33) reduced the input current. This was a major step forward in op amp technology. Unfortunately, lateral pnp transistors were still needed and, therefore, the speed of the op amp was essentially unchanged.

Super gain transistors are standard bipolar transistors which have emitters that have been diffused for extremely high current gains. Typically, current gains of 5,000 can be obtained at 1uA collector currents which are competitive with FETs. It is also possible to operate these transistors at zero collector-base voltage, eliminating the leakage currents that plague the FET. Therefore, they can provide lower error currents at elevated temperatures.

Standard bipolar transistors in a Darlington connective have been tried in a number of IC designs to get very low input currents. First order calculations indicate that a Darlington should be competitive with super gain transistors on input current specifications. But differential amplifiers, using Darlington-connected transistors have problems that may not be immediately obvious.

The offset voltage depends not only on the inherent emitter base voltage match of the transistors, but also on the percentage match of current gains. A 10% mismatch in current gains gives a 2.5mV offset. Within a given process, bias currents drop faster than offset currents as the transistor current gains are raised. Therefore, the better the transistors, the worse the offset voltage.

In addition to being a major contributor to offset voltage, this dependence on current-gain matching causes other problems. In a simple differential amplifier, the offset voltage drift can be correlated with offset voltage because of the predictable nature of emitter-base voltage. This is not so with Darlingtons, as bias current matching is not predictable over temperature. At high temperatures, this effect is aggravated further by leakage currents, so it is impossible to predict performance over a wide temperature range based on room temperature tests.

Reducing the collector current of double diffused silicon transistors to very low currents (below 1uA), as is done in a Darlington, does not improve input currents as much as might be expected. Lowering the collector current by a factor of 10 reduces the bias current by about a factor of 7 and the offset current by a factor of 3. These numbers are typical; the results obtained near the edges of a production distribution are significantly worse. In addition, the variation of input currents with temperature

varies as the square of the current gain. Since the gain of integrated circuit transistors falls off by a factor of 2 to 5 going from 25° down to -55°C, the input currents obtained at the minimum operating temperatures are considerably higher than at room temperature.

Other limitations of Darlingtons are that they have higher noise, lower common mode rejection and reduced common mode slew rate. Further, they have one-half the transconductance of a simple differential stage; this doubles the effect of dc offset terms in the output circuitry.

To summarize, Darlingtons can give typical input currents competitive with super gain transistors; however, if the full range of production variables is taken into account, along with -55° to 125°C operation, the performance is degraded considerably (or the yields reduced) both with respect to offset voltage and input current. Modified Darlingtons where the operating current of the input transistors is made large by comparison to the base current of the output transistors, do not suffer from problems caused by current gain matching.

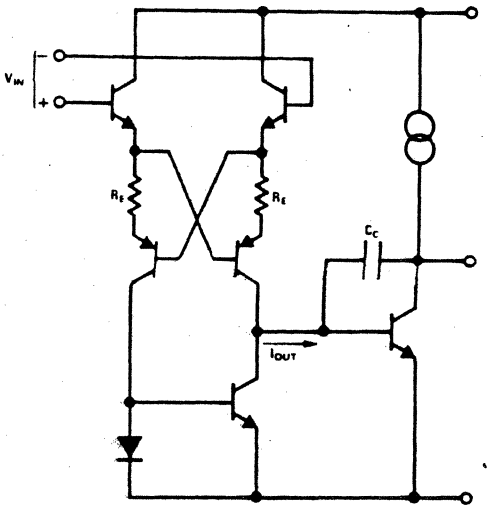
Slew rate enhancement techniques (Figure 34) have been developed but these tend to degrade both V_{OS} and V_{OS} drift due to the increased circuitry added at the input stage. More important are the problems which arise due to the undesired gain enhancement during slew which can cause transient instabilities. Finally, a large differential input overdriver is required for enhancement.

A useful technique for increasing the bandwidth is to feed the signal around the slow responding stage (Figure 35). This "feedforward" technique was introduced in a monolithic amplifier by National (LM118). Although the bandwidth is significantly improved, the settling time and input current are relatively unaffected.

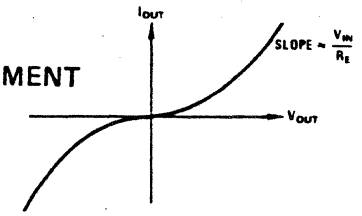
The limitations of the standard linear IC process allow only an improvement in a single specification at a time. To overcome these limitations better active devices to design with are required. Field effect transistors are electric field sensitive. An electric field is established in a capacitor proportional to charge; therefore, the FET is a charge operated device. This is not enough, because the Ebers Moll theory also establishes the bipolar transistor as a charge operated device. The FET has no bias current, yet it can have an appreciable initial source drain current. That is the big difference between bipolars and FETs.

FET input stages have long been considered the best way to get low input currents in an op amp. JFET inputs are characterized by high, not too well controlled, offset current and low picoamp input currents at room temperature. However, this current, which is the leakage current of the gate junction, doubles every 10°C, so performance is severely degraded at high temperatures. Another disadvantage, up until now, has been the difficulty of matching FETs.

FET op amps have high input capacitance and high stray capacitance from output to input which can cause instability problems in a given application.



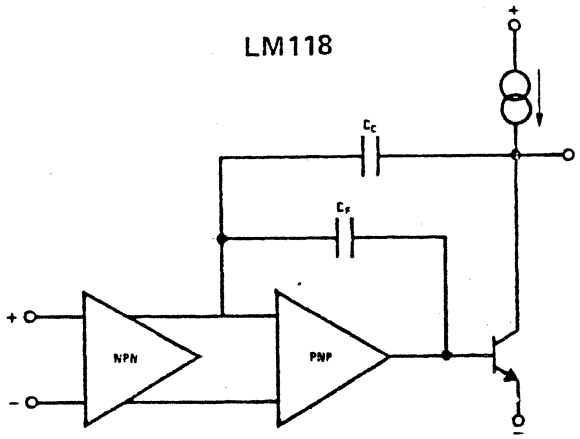
LARGE I_{OUT} DRIVES C_C FOR HI SLEW . . .
BUT *NOT* HI BW



SLEW ENHANCEMENT

Figure 34

LM118



FEEDFORWARD

GIVES LARGE BW & SLEW
BUT *NOT* SETTLING OR I_{BIAS}

Figure 35

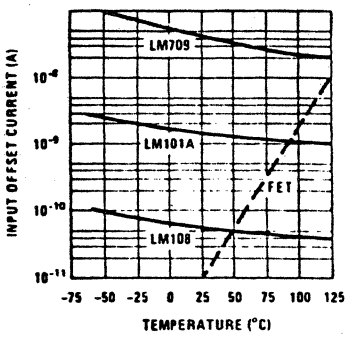


Figure 36: Op Amp Performance Comparison

Figure 36 compares the performance of several IC op amps. FET input amplifiers are clearly better than the 709's. The LM108 equals typical FET amplifier performance at about 50°C. At 125°C the LM108 is about two orders of magnitude better than FET amplifiers.

The BI-FET process (Figure 37) provides an improved active device - an ion implanted p-channel JFET which can be built on the same chip with standard bipolar transistors. The good control of the implant results in well-matched JFETs. They are also wider band devices than lateral pnp transistors with roughly the same breakdown voltages. Their input current, however, is orders of magnitude less.

Notice that the matching of these FETs (Table 2) gives essentially the same V_{OS} and V_{OS} drift as that of the bipolar transistors. The input current (Ig) is down several orders of magnitude, the noise performance is improved, especially for large source resistances and the bandwidth limitations of lateral pnp transistors has been overcome.

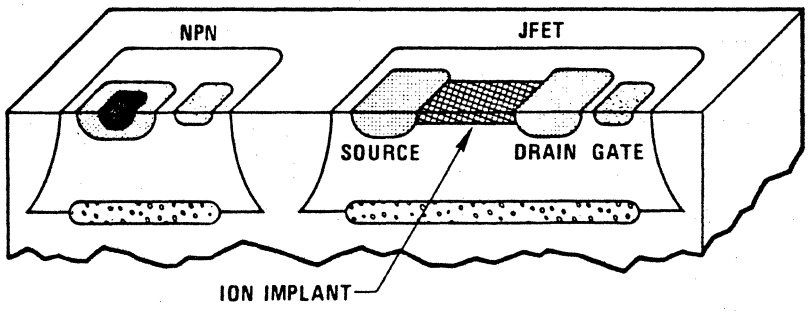
The LF156 is a commercially available JFET input op amp developed by National Semiconductor utilizing the BI-FET process. The basic design of the LF156 (Figure 38) is a differential JFET input stage followed by a differential bipolar second stage (for symmetrical second stage bias current loading). FET current source loads are used for the first stage to minimize V_{OS} and V_{OS} drift. As a result, a common mode feedback loop is required.

Common-mode feedback loops are interesting. At dc, the compensation capacitor (10pF) is an open circuit and the feedback to the sources of the input FETs is common-mode. For ac inputs, the compensation capacitor will absorb the output current of the first stage. Note that the other differential output current is constrained to be essentially zero (there is no place for current to be absorbed). Therefore, the entire differential input voltage is impressed across the gate source of the noninverting input FET. This provides a gain doubling differential to single-ended conversion.

The performance of the output stage of an op amp has also been limited by the poor frequency response of the monolithic lateral or vertical pnps. A significant improvement in the open loop output impedance (at both high output currents and high frequencies) has been made in the LF156 by use of a FET.

The ability of an op amp to absorb high frequency load transients or to drive large capacitive loads (and maintain stability) is determined by the high frequency open-loop output impedance. In order to keep this small, a high frequency FET-npn composite is used for the lower side and the upper npn output transistor remains biased ON even during output current sinking to bypass the composite at high frequencies.

The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. During normal operation the junction temperature rises above the ambient as a result of internal power dissipation P_d. The use of a heat sink is recommended if input bias current is to be kept to a minimum.



LOW V_{OS}, LOW I_{BIAS}
WIDE BW & SLEW RATE ? ...

Figure 37: Matched JFETs and Bipolar Transistors

Table 2

Comparison of JFET and Bipolar Transistors

	P-CHANNEL JFET'S		PNP BIPOLAR DEVICES
I_G	30 pA	I_B	3000 pA
V_{OS}	2 mV		ABOUT THE SAME
$\Delta V_{OS}/\Delta T$	3.5μV/°C		ABOUT THE SAME
BW	10 MHz		1 MHz
BV_{GSS}	50V		
NOISE VOLTAGE	8 nV$\sqrt{Hz}$		
NOISE CURRENT	"FORGET IT"		

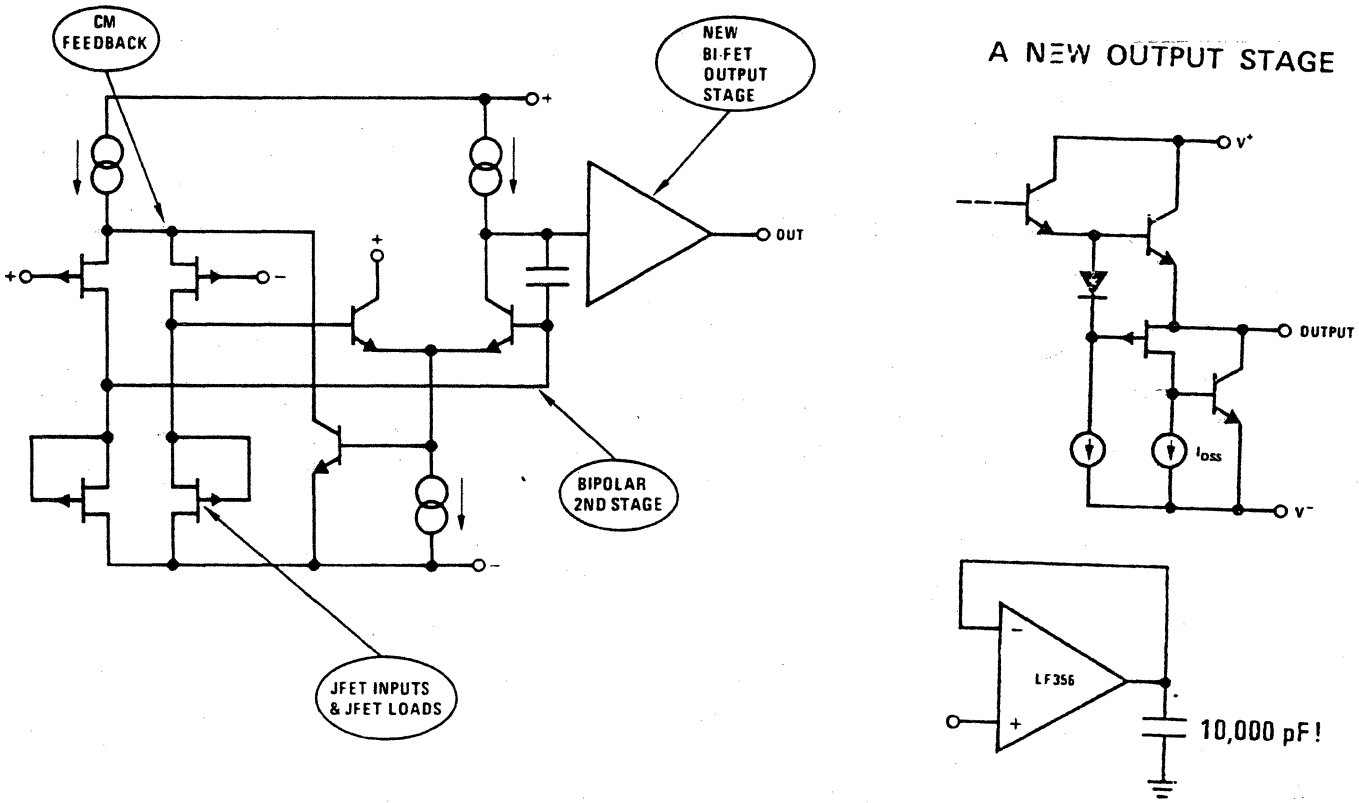


Figure 38: LF156 Op Amp Basic Circuit

The noise benefits of an FET input op amp are most significant for large source resistance (Figure 39). This is a result of the very small magnitude of the input current. The noise current for a FET is so small, it is hard to measure, but it can be calculated from the standard shot noise equation:

$$\frac{i_n}{\sqrt{Hz}} = \sqrt{2qIg}$$

The benefits of the New V_{OS} adjust circuitry which is used in the LF156 are shown in Figure 40. A change in V_{OS} drift of only 0.5uV/°C per mV of adjust is typically achieved.

Notice that the long term V_{OS} drift of the LF156 approaches that of the better bipolar op amps (Figure 41).

Op amps built with MOS FET inputs are characterized by low gain, high input offset voltage and low, but noisy, input leakage. While transient differential voltages on the MOS gates will not affect amplifier performance, steady state operation under these conditions at elevated temperatures may result in offset voltage degradation.

The RCA CA3140 features a PMOS input stage and bipolar output stage. The CA3140 provides the advantage of a MOS FET input with the speed of bipolar and high supply voltage operator capability: 4 to 44V, dual or single supply. That means very high input impedance; 1.5T typ. Very low input current; 10pA typ. at ±15V. Low input offset voltage; as low as 2mV max. Wide common-mode input voltage range - can be swung 0.5V below negative rail. In addition, output swing complements input common mode range permitting full utilization of low supply voltages (down to 4V). And PMOS input devices are protected to 1000V by rugged bipolar diodes between the FET to gate and substrate.

The CA3140 needs no external compensating circuitry. It is characterized for low cost TTL systems requiring operation at 5V and maintains operation down to 4V. Its wide bandwidth - 4.5MHz unity gain - makes possible low cost video and audio circuits. For low cost sample and hold and other data acquisition systems, it offers fast settling time: 1.4 us typ. to 10mV. When it's driving power transistors, the output swings to within 0.2V of the negative supply, eliminating the need for level shifting circuitry.

The CA3140, which is pin compatible with the industry's standard, uA741 general purpose op amp, has a higher slew rate and very low input current 10pA vs. 80,000pA for the uA741. Table 3 compares the CA3140 with the uA741.

A gross distinction can be made between JFET and MOS FET op amps: the JFET front end generally gives slightly better performance in some respects - like lower noise and lower offset voltage drift. But don't overlook the fact that the MOSFET front end should be the choice if you're really interested in broad common mode voltage operating range - in fact, it can go from rail to rail of the supply voltage. This means that you can even

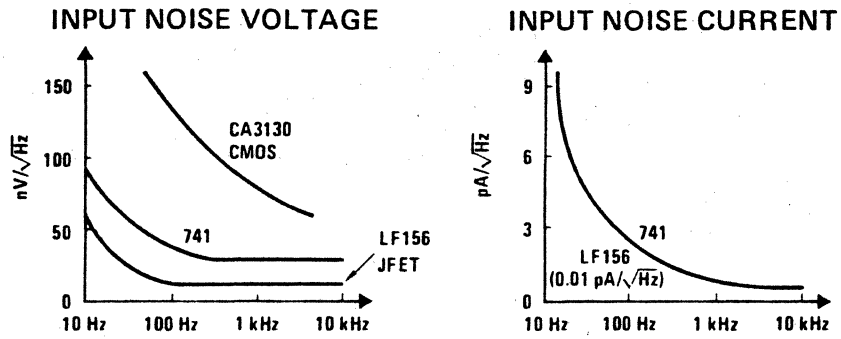
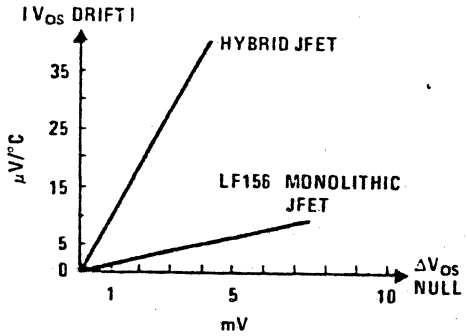


Figure 39

THE LF156 HAS LESS DRIFT PER MILLIVOLT OF OFFSET ADJUST THAN ANY OTHER FET OP AMP



CHANGE IN OFFSET DRIFT WITH V_{OS} NULL

Figure 40

LONG TERM DRIFT OF OFFSET VOLTAGE
(T_j = 125°C)

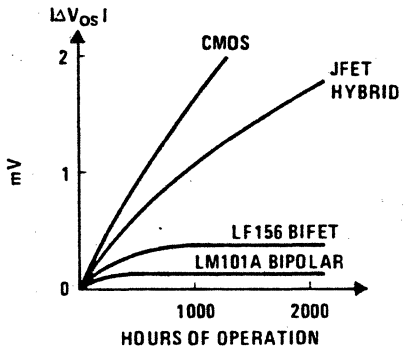
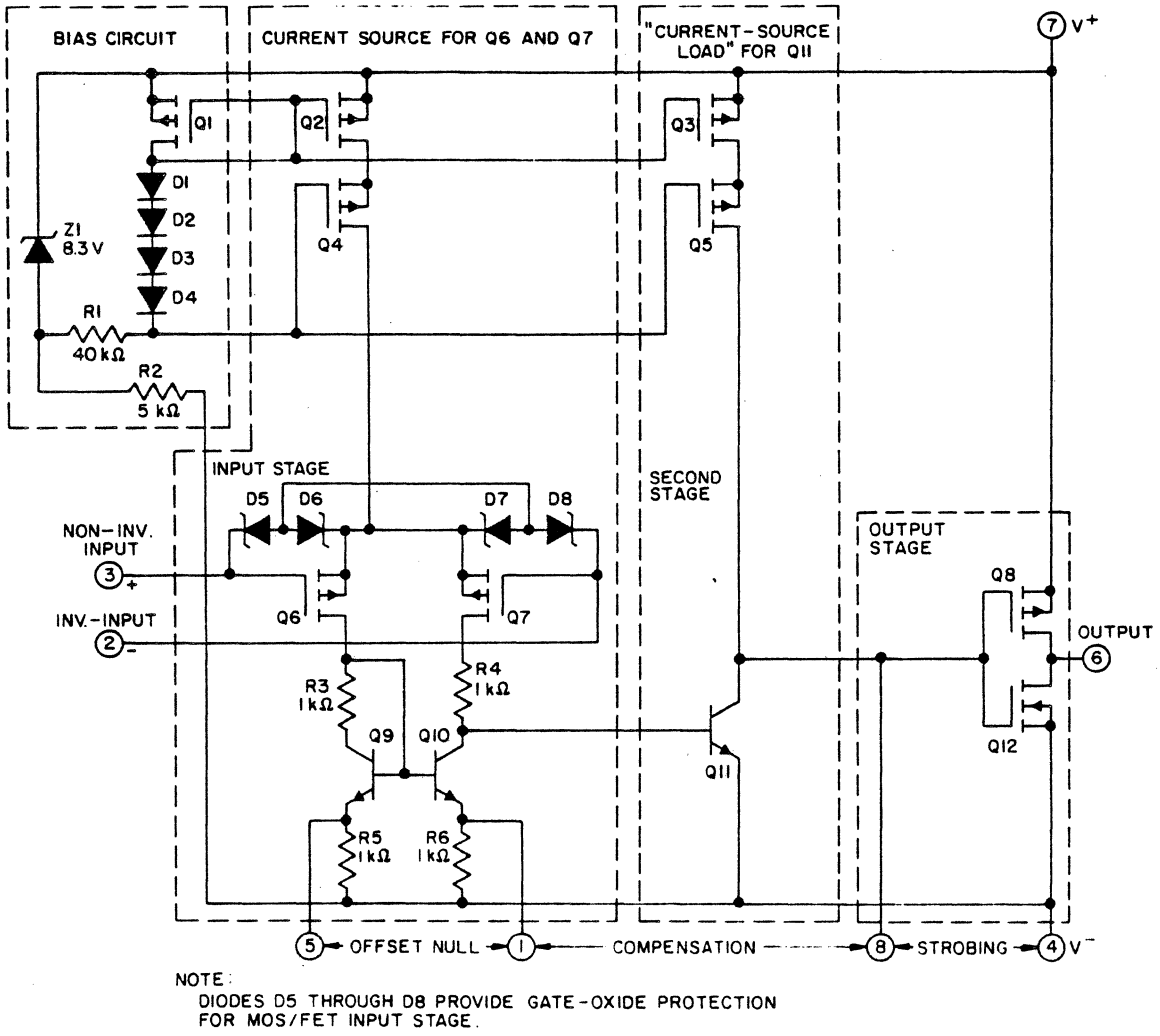


Figure 41

Table 3

CA3140 versus 741

Characteristics at Supply Volts: V+ 15, V− 15 @ 25°C	Limits						Units
	CA 314OT, S			CA741CT,S			
	MIN	TYP	MAX	MIN	TYP	MAX	
Input Resistance, R_I	300,000	1,500,000	—	0.3	2	—	MΩ
Input Current, I_I	—	10	50	—	80,000	500,000	pA
Input Offset Current, I_{IO}	—	0.5	30	—	20,000	200,000	pA
Input Offset Voltage V_{IO}	—	5	15	—	2	6	mV
Slew Rate, SR (Closed Loop)	—	9	—	—	0.5	—	V/μs
Gain-Bandwidth Product f_T	—	4.5	—	—	1.0	—	MHz
Common-Mode Input Range, V_{ICR}	−15	−15.5 to +12.5	+11	−12	±13	+12	V
Output Swing $R_L = 2K\Omega$	−14	−14.4 to +13.0	+12	−10	±13	+10	V
Large Signal Voltage Gain A_{OL} $R_L = 2K\Omega$	—	20,000	—	—	20,000	—	



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

Figure 42: Schematic diagram of the CA3130 CMOS Op Amp

operate the op amp from a single polarity supply without jacking up your input signal.

The CA3130 CMOS op amp has even lower input characteristics than the CA3140. The schematic diagram of the CA3130 (Figure 42) portrays the simplicity of its three-stage circuit design; each stage is of unique design and provides characteristics of advantage to the user.

Input Stage

The differential input stage uses PMOS field effect transistors (Q_6 and Q_7) that work into a mirror pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6. The mirror pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second stage bipolar transistor (Q_{11}). When desired, offset nulling can be effected by connecting a 100 kilohm potentiometer across terminals 1 and 5 and the potentiometer slider arm to terminal 4. Cascode connected PMOS transistors Q_2, Q_4 are the constant-current source for the input stage, and are biased by the bias-circuit shown. Small diodes (D_5 through D_8) provide gate oxide protection for Q_6 and Q_7 against high voltage transients, including static electricity during handling.

The use of PMOS transistors (Q_6, Q_7) results in ultra-high input resistance (approximately 1.5 teraohms, i.e., 1.5×10^{12} ohms) and ultra-low input current (5pA, typical). Additionally, the use of the PMOS transistors permits common mode random operation down to approximately 0.5V below the negative supply-rail potential. While operating in this region, there is no "phase reversal" of the output signal.

Second Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage consisting of bipolar transistor Q_{11} and its cascode-connected load resistance provided by PMOS transistors Q_3 and Q_5. These transistors are biased from the same potentials used to bias PMOS transistors Q_2 and Q_4, respectively. This circuit design permits Miller-effect compensation (roll-off) by the use of a single low value external capacitor. For example, a 47pF capacitor provides sufficient compensation for stable unity gain operation in most applications.

Output Stage

The output stage consists of a drain loaded inverting amplifier using CMOS transistors (PMOS Q_8 and NMOS Q_{12}) operating in the linear Class A mode. Consequently, the small signal "cross-over" distortion of the output signal frequently encountered in op amps is eliminated. The nonlinearity in the output stage of the CA3130 with large signal excursions requires the use of feedback for good waveform reproduction. As a voltage follower, the amplifier can achieve 0.01% accuracy levels including the negative supply rail.

The use of CMOS transistors in the output stage of the CA3130 permits the output signal to be swung within millivolts of either supply rail when the

Table 4

Summary of Characteristics of CA3130B CMOS Op Amp

Parameter	Test Conditions (25°C)	Min.	CA3130B Typ.	Max.
Input offset voltage (mV)	$V^{\pm}$ = ±7.5 V	–	0.8	2
Input offset current (pA)	$V^{\pm}$ = ±7.5 V	–	0.5	10
Input current (pA)	$V^{\pm}$ = ±7.5 V	–	5	20
Large signal voltage gain (dB)	V_o = 10 V_{pp}, R = 2 k, V^+ = 15 V, V^- = 0 V	100	110	–
Common-mode rejection ratio (dB)	V^+ = 15 V, V^- = 0 V	86	100	–
Common-mode input-voltage range (V)	V^+ = 15 V	0	−0.5 to 12	10
Power supply rejection ratio (μV/V)	$V^{\pm}$ = ±7.5 V	–	32	100
Output voltage (V)				
Max.	*R_L = 2 k	12	133	–
Min.	*R_L = 2 k	–	0	0.01
Max. output current (mA) *				
Source	V_o = 0	12	22	45
Sink	V_o = 15 V	12	20	45
Supply current (mA) * (R_L = ∞)	V_o = 7.5 V	–	10	15
	V_o = 0 or V_o = 15 V	–	2	3
Input resistance (Teraohms)	#	–	1.5	–
$\Delta V_{IO}/\Delta T$ (μV/°C) *	$V^{\pm}$ = ±7.5 V, V_o = 10 V_{pp}, R_L = 2 k, T_A = −55 to +125°C	–	5	15
Unity-gain crossover frequency # (f_t = MHz)	C_c = 0	–	15	–
	C_c = 47 pF	–	4	–
Slew rate (V/μs) #	Open loop, C_c = 0	–	30	–
	Closed loop, C_c = 56 pF	–	10	–

*V^+ = 15 V; V^- = 0 V.

#$V^{\pm}$ = ±7.5 V.

IC is operating into very high resistance loads. In Figure 42, terminals 4 and 8 are designated for use when it is desired to strobe the output stage into quiescence. Strobing is accomplished by external switching circuitry which pulls terminal 8 down to the potential of terminal 4, thereby shutting off current flow in the output stage and forcing terminal 6 up to approximately the potential of terminal 7 (assuming very high output load resistance at terminal 6).

The CMOS transistor output stage offers yet another advantage in that the transistors provide short circuit protection; their channel resistances increase with increasing temperature so that they can protect against excessive current flow under short circuit conditions.

Although the CMOS output stage in the CA3130 can typically sink and source current of about 20mA, greater current handling capability is easily provided by paralleling auxiliary CMOS transistor-pairs at terminals 4, 5, 7 and 8.

One can certainly see that testing this myriad of device configurations can present a perplexing problem to say the least.

4.312 Op Amp Specifications

The problems associated with the high speed testing of operational amplifiers stem from three main sources: the magnitude of the voltages and currents to be measured; the necessity of maintaining the amplifier in its linear operating range during measurements; and the presence of an amplifier imperfection - input offset voltage. These three problems affect some parameter measurements, but not others. The particular measurements affected are input offset voltage, input bias current, input offset current, and voltage gain. Parameters relatively free from measurement problems are: positive and negative output current, positive and negative output voltage swing, and total supply current.

Due to the complexity of the linear IC, the specified parameters are usually functions of a number of variables - some of which are of first order importance and some of lower order, while many are nonlinear. Let's discuss op amp specifications and what they mean.

Input Offset Voltage, V_{OS}

The ideal differential amplifier for most applications is one that produces zero volts out for zero volts between the input terminals. Practical amplifiers have an offset voltage as shown in Figure 43a. If you connect the two inputs together, the output voltage will not be zero, but will be equal to the input offset amplified by the open loop gain. This can be reduced to zero by introducing an additional input voltage just sufficient to cancel this offset. The value of this voltage will be equal to $-V_{OS}$ and the output will go to zero when this is applied as shown in Figure 43b.

V_{OS} is usually specified in millivolts and is defined as that voltage which must be applied between the input terminals of the amplifier to make the output go to zero. It should be noted that if V_{OS} is not adjusted to

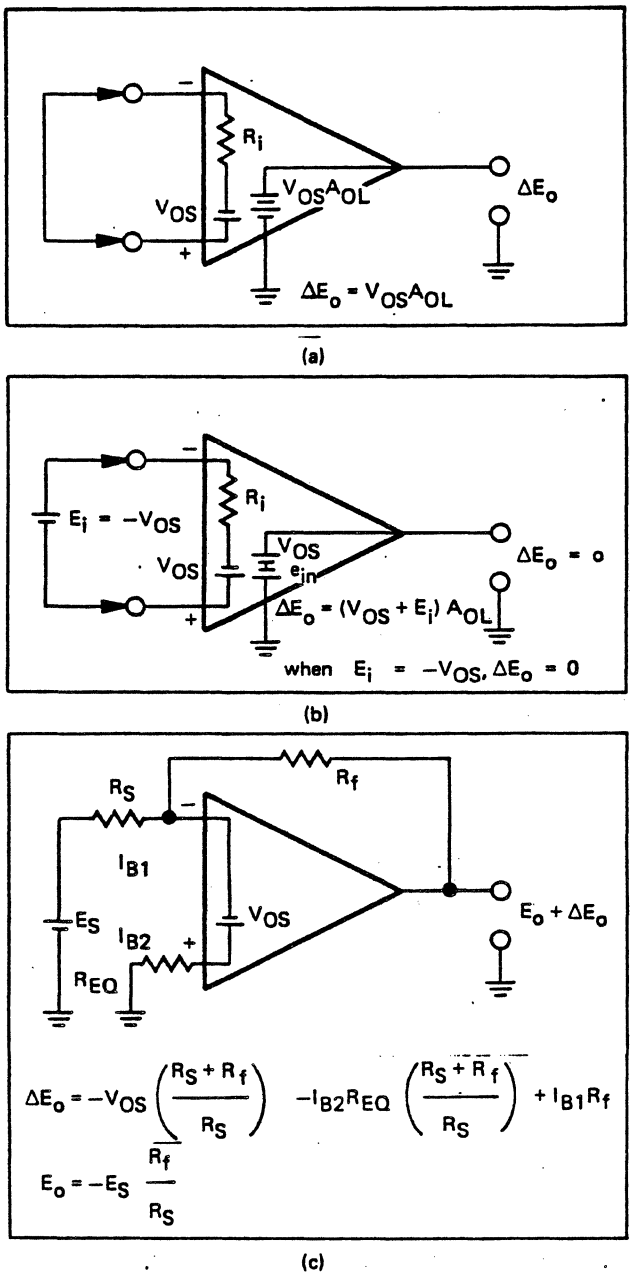


Figure 43: Effect of Input Offset Voltage and Current

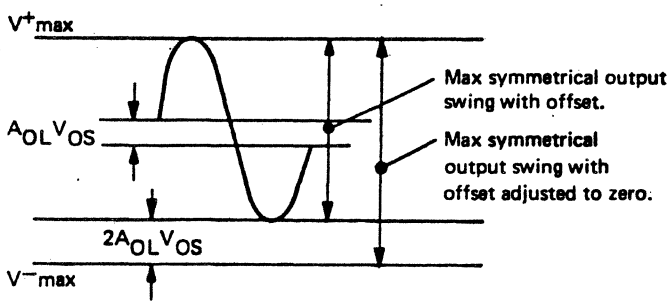


Figure 44: V_{OS} adjustment

zero in some way, the output voltage offset from zero will reduce the maximum symmetrical output swing as shown in Figure 44.

Terminals for V_{OS} adjustment are often not supplied on IC amplifiers. The close matching of input transistor V_{BE}'s possible in IC amplifiers results in very low V_{OS} values. One method of adjusting V_{OS} to zero is to adjust the current level in one side of the input stage so that the V_{BE}'s do match. Even if terminals are available for this purpose, it should be remembered that this adjustment has various second order effects on dc stability and frequency response which are generally unspecified by the supplier and are best evaluated by the user for his particular application. If no provision is made for offset adjustments, this may be included in the external circuitry, but its effect on drift must be considered.

V_{OS} is also measured with the circuit in Figure 45. In many applications, the maximum value of V_{OS} at other than V_{CM} = OV is important, since the operational amplifier is used in the noninverting mode. Applications also exist where it is advantageous to operate with supplies other than ±15V and R_S = 0 ohms. Another word of warning - be sure you understand the conditions under which V_{OS} is tested and guaranteed by the manufacturer. For example, the 101A/107/108 operational amplifiers specify a guaranteed V_{OS} over V_S = ±5V to ±20V; R_S = 50 ohms to 50 kohms; and V_{CM} of +5, -2 to ±15V.

On the other extreme, V_{OS} for the 741, 747, 748 is specified for operation at ±15V supplies and V_{CM} = OV. To the supplier, in order to properly guarantee 101A/107/108 devices, V_{OS} must be measured under 18 different sets of operating conditions. The 741 V_{OS} specification can be guaranteed with four measurements. Obviously, the user is receiving a far less tested device in one case than the other. He should be knowledgeable of his application's requirements so that he does not get into trouble when using the less comprehensive specification.

Input Bias Current I_B and Input Offset Current I_{OS}

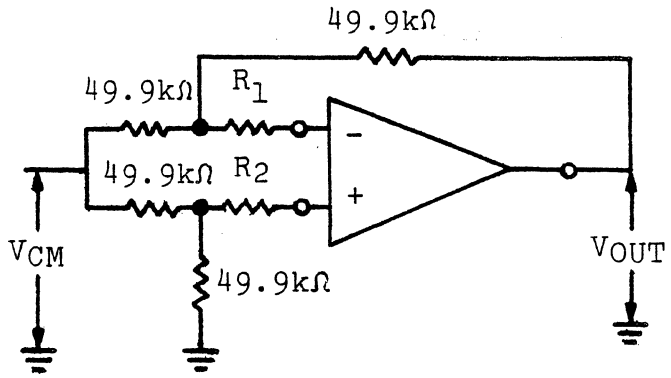
The input stage of any practical amplifier requires some bias current. For an IC amplifier, the bias currents at each input are inherently closely matched. Figure 46 shows the nature of the input bias currents I_{B1} and I_{B2} and the resulting offset voltage. For an IC differential amplifier the Input Bias Current specification is the average of the two input currents:

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For IC amplifiers Input Offset Current is defined as the difference in the currents at the two input terminals when the output is at zero or,

$$I_{OS} = [I_{B1} - I_{B2}]$$

If the source resistances R_S are equal for each input, then the effective offset voltage at the amplifier input will be equal to $I_{OS}R_S$. The sum of I_B average and I_{OS} maximum defines the maximum value of I_B that would be



For R_S = 50Ω $R_1 = R_2 = 0$

For R_S = 50kΩ $R_1 = R_2$ = 49.9k

NOTE: The ratios of the resistors in this circuit must be matched to better than 0.025% to eliminate common mode error.

Figure 45: Circuit for measuring V_{OS}

108 101A 725

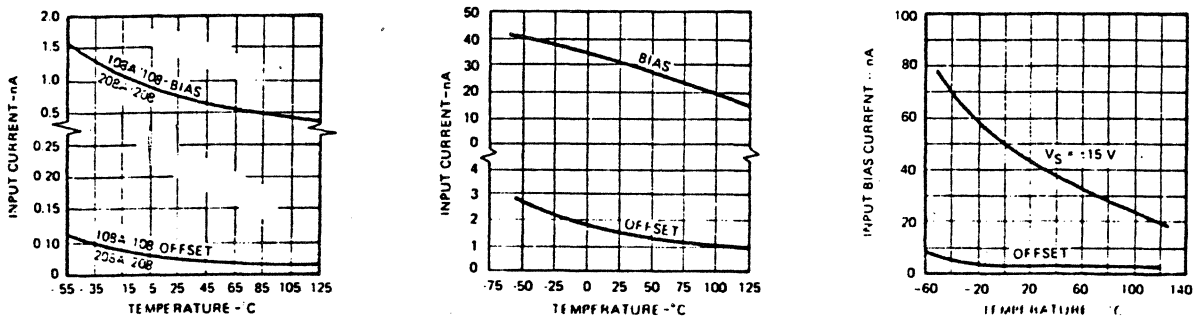


Figure 46: Input Bias and Offset Currents as a function of temperature for these popular OP Amps.

observed for a particular operational amplifier. The 301A operational amplifier is measured under nine different combinations of V_S, CMR AND R_S in order to properly describe its performance.

Average Temperature Coefficient of Input Offset Current $\Delta I_{OS}/\Delta T$

The average temperature coefficient of input offset current is the ratio of the change in input offset current over the operating temperature range to the temperature range.

This parameter is deceptive and sometimes misinterpreted. The units of $\Delta I_{OS}/\Delta T$ imply a linear relationship between I_{OS} and change in temperature.

The curves for three of the more popular operational amplifiers indicate differently as shown in Figure 46.

I_{OS} changes with temperature proportionately to I_B as the above curves indicate. Input Bias Current changes as a function of h_{Fe} which changes from 1.5 to 3.0 times over a 25°C to -55°C temperature range. As indicated, this change is not linear as the expression nA/°C implies. In practice, the curve is closer fit with an exponential. Important to understand is:

1. Each linear integrated circuit h_{Fe} (I_B) falloff will vary with temperature.

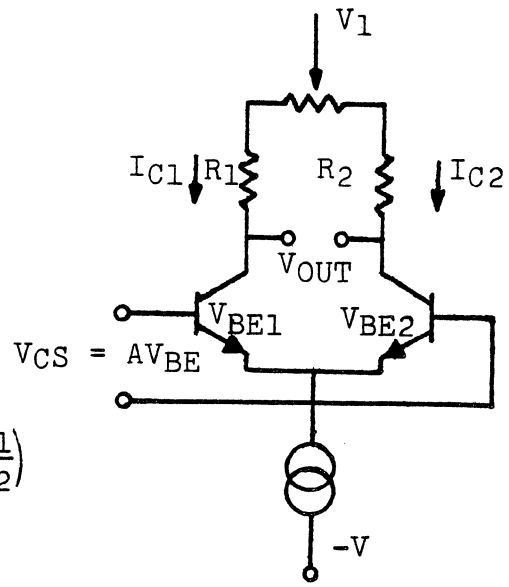
2. Suppliers guaranteeing the $\Delta I_{OS}/\Delta T$ parameter measure I_{OS} at -55°C, 25°C and 125°C and calculate the specified $\Delta I_{OS}/\Delta T$.

When depending upon this parameter for circuit performance, consider that the information given defines three points on the curve of I_{OS} vs. temperature - not the slope of the entire curve. Verification of $\Delta I_{OS}/\Delta T$ for devices such as the 108, where I_{OS} currents less than 100pA must be measured at -55°C and 125°C, are possibly the most technically difficult production tests that are performed today.

Average Temperature Coefficient of Input Offset Voltage $\Delta V_{OS}/\Delta T$

The average temperature coefficient of input offset voltage is the ratio of the change in input offset voltage over the operating temperature range to the temperature range.

Again, as with $\Delta I_{OS}/\Delta T$, the units of the specification imply linearity. The parameter is guaranteed via a three-point measurement (-55°C, 25°C and 125°C) to approximate a straight line. This is an accurate approximation typical of operational amplifiers exhibiting single differential pair input stages. This straight line temperature relationship is expressed by the following equation:



$$VOS = \Delta V_{BE} = \frac{KT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) + \frac{KT}{q}\left(\frac{I_{S1}}{I_{S2}}\right)$$

$$\frac{V_{OS}}{T} = \frac{K}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) + \frac{K}{q} \ln\left(\frac{I_{S1}}{I_{S2}}\right)$$

I_{S1} and I_{S2} are functions of the transistor geometry, spacing, etc., and are constant with temperature. I_{C1} and I_{C2} are collector currents that are not directly a function of temperature, but are affected through R_1 and R_2 which change approximately 0.2%/°C. If transistors are not identical, and collector currents are not equal, then temperature effects ΔV_{BE} in the following manner:

$$\frac{\Delta V_{BE}}{\Delta T} = \frac{K}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) + \frac{K}{Q}\left(\frac{I_{S1}}{I_{S2}}\right)$$

Note that if I_{C1} and I_{C2} are changed such that $\frac{K}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$ and $\frac{K}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\right)$ are equal and opposite, then theoretically $\frac{\Delta V_{BE}}{\Delta T} = 0$. This is the theoretical basis for V_{OS} nulling via mismatching of collector currents. As mentioned earlier, in practice, collector resistors R_1 and R_2 are not identical and, hence, do not track perfectly over temperature. Also, if the term $\frac{K}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$ is a second order function of temperature, then the previous differentiation with respect to temperature, considering it a constant, would not be balid. This explains the practical departure from theory in obtaining zero V_{OS} temperature coefficient performance of monolithic operational amplifiers.

Input Resistance R_{IN}

The input resistance is the resistance looking into either input terminal with the other grounded and is related to the input bias current by the relationship:

$$R_{IN} = \frac{mkT}{qIB}$$

Where m is a constant set by the chip configuration and the diffusion schedule,

k = Boltsmann's constant

T = Temperature, °K

q = Electron charge

As such, R_{IN} is guaranteed by measurement of I_B. The constant m varies between 1 and 2 for the particular operational amplifier.

Input Voltage Range Specifications

Common Mode Input Voltage Range, V_{CM}, is the maximum voltage that may be applied from either input of the amplifier to ground. Differential input voltage is the maximum voltage that may be applied directly between the input terminals.

Exceeding these specifications may permanently degrade the amplifier or cause catastrophic failure. The designer should examine the application carefully to see what signal overload conditions may apply and provide input clamps to protect the amplifier inputs from excessive voltage excursions. These excursions may be found in integrators; during turn on the feedback capacitor may try to charge through the input during an output transient. Another case where problems may arise is when the input signal slews faster than the output. Input spiking of this sort is often responsible for amplifier failures that occur after a period of months due to slow deterioration of the input circuits.

Common Mode Rejection Ratio CMRR

The common mode rejection ratio is the ratio of the input voltage range to the peak-to-peak change in the input offset voltage over this range.

Common mode rejection ratio is found from the difference between V_{OUT} at the negative common mode limit and V_{OUT} at the positive common mode limit referred to the input.

$$CMRR = 20 \log \left[\frac{(V_{CM+} - V_{CM-}) \times 10^3}{V_{OUT}(V_{CM-}) - V_{OUT}(V_{CM+})} \right]$$

Input voltage range (V_{CM}) specifications are also guaranteed by the CMRR tests. This test provides an accurate measure of operational amplifier symmetry at dc and low frequencies. Figures 47 and 48 indicate approximately a 20dB/decade roll-off of CMR with frequency.

Most applications are concerned with the ability of the amplifier to reject a common ac signal such as 60 Hz. Linear integrated circuit specifications do not provide this ac specifications due to production testing complexity and costs. CMRR does roll-off with frequency, but usually not below 100 Hz.

725A

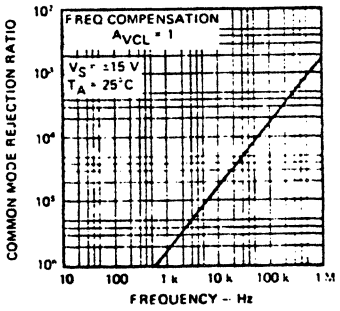


Figure 47:
CMRR plot for uA725A

101A

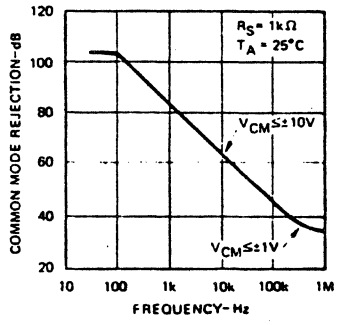


Figure 48:
CMRR plot for LM101A

725

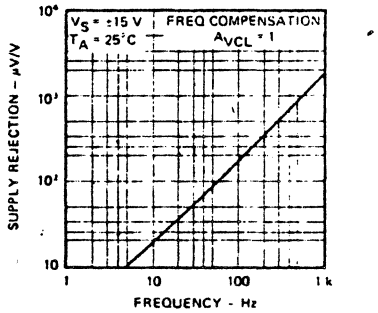


Figure 49:
PSRR plot for uA725

101A

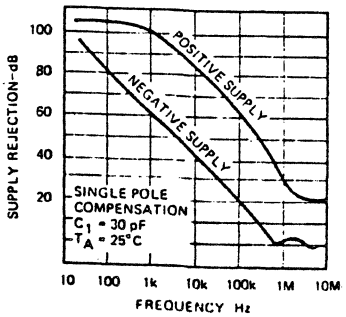


Figure 50:
PSRR plot for LM101A

Data sheet typical curves usually provide accurate trend information to allow for user extrapolation.

Power Supply Voltage Rejection Radio, PSRR

Power supply voltage rejection ratio is the ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

Power supply rejection radio is found from the difference in V_{OUT} at the highest supply voltage and V_{OUT} at the lowest supply voltage referred to the input:

$$PSRR = 20 \log \left[\frac{(V_{SMAX} - V_{SMIN}) \times 2 \times 10^3}{V_{OUT}(V_{SMAX}) - V_{OUT}(V_{SMIN})} \right]$$

NOTE: V_{CMIO} for these tests.

Figures 49 and 50 describe the roll-off of PSRR with frequency for the 725 and 101A.

Figure 50 suggests that the PSRR of an amplifier to both positive and negative supplies is not identical. Testing of PSRR is performed by changing both supplies simultaneously from their lowest specified value (V_S = ±5V) to the highest value (V_S = ±20V). The measurement is made after transients have settled to a dc condition. The PSRR specification should not be considered to be a measure of single supply rejection without consulting the linear integrated circuit supplier regarding the specific device. The parameter should not be applied to ac line rejection without adequate derating based upon trend extrapolation or additional supplier information.

Large Signal Voltage Gain, A_{OL}

Large signal voltage gain is the ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage. Large signal voltage gain is found from the difference in V_{OS} at V_1 = 0 and V_{OS} at $V_1 = \pm V_{OUT}$ for each combination of supply voltages and source resistance and is given by:

$$A_V = \left[\frac{V_{OUT}}{V_{OS}(V_1 = -V_{OUT}) - V_{OS}(V_1 = 0)} \right]$$

Since the changes in V_{OS} are very small (typically 20 to 100uV), it is recommended that an additional amplifier with a gain of at least 1000 be used to amplify the signal before measurement. Also, to reduce the effects of thermal feedback, V_1 should be a pulse having a width of about 100ms and a low duty cycle. Gain is measured over the specified range at supply voltages. A rule of thumb for most operational amplifiers is that A_{OL} will fall off at 6dB/oct with supply voltage. Gain is also inversely proportional to temperature from the following relationship:

$$A_V = R_L G_m \approx \frac{T_1}{T_1 T} \approx \left[\frac{1}{\text{Temperature}}\right]/\text{Stage}$$

This relation is representative of gain stages utilizing passive load resistors. For stages using active loads driving low input impedance stages, the effective R_L varies with temperature as a function of h_{FE}. This increases the effect of temperature on A_{OL} for amplifiers, such as the 741, 101A and 108.

A common problem to many monolithic operational amplifiers is a lack of channel symmetry with respect to gain. This is due to the inability to obtain monolithic pnp transistor gain/bandwidth comparable to monolithic npn performance required for symmetric output swing. Figure 31 shows the result of this effect.

Because of this design limitation, it is important that each amplifier be measured for A_{OL} at both positive and negative full output swing (±10V). Historical ac (10 to 150Hz) gain measurement techniques have proven to be inaccurate and not reproducible due to low frequency operational amplifier noise and the low frequency break point (<5 Hz) of most compensated monolithic operational amplifiers. The superficial advantage of ac gain measurement was thought to be the reduction of self-heating during measurement. Self-heating is a problem, but if the device is pulse tested, gain measurements can be reproduced. Operational amplifier gain measurement is probably the last accurate and reproducible measurement for both supplier and user.

Output Voltage Swing, V_{OUT}

The output voltage swing is the peak-to-peak amplifier output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage. For single-ended outputs, the peak output swing is that referred to zero, which can be obtained without clipping.

V_{OUT} is measured under all specified supply voltage and load conditions for both positive and negative swing. This parameter is used to replace the output resistance specification which is an ac amplifier term, since it is very difficult and costly for a linear IC supplier to perform the ac testing required to guarantee R_{OUT}. The combination of V_{OUT} and Slew Rate accurately determine the large signal bandwidth of an operational amplifier.

Power Supply Current

Power supply current is the current required from the power supplies to operate the device with no load. This parameter is usually measured in the voltage follower circuit as shown in Figure 52. The positive current also flows to the negative supply since the output is unloaded.

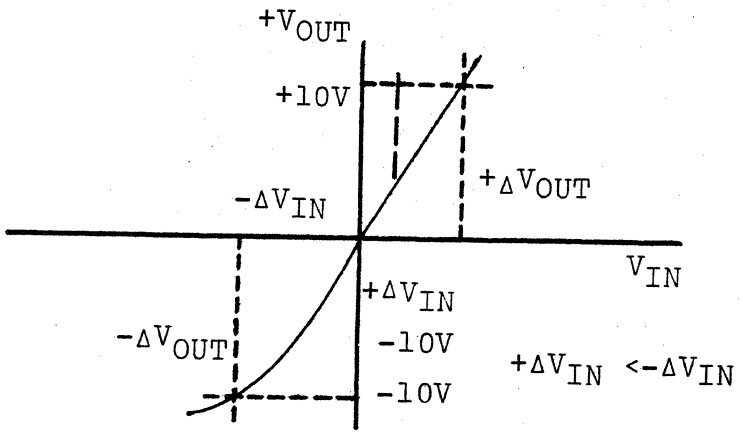


Figure 51

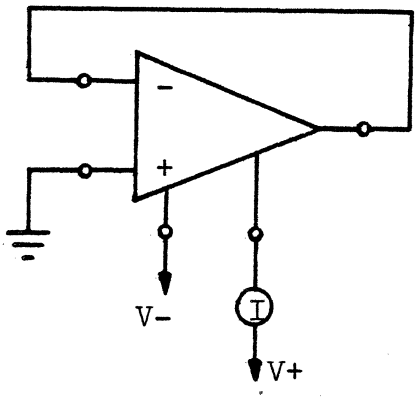


Figure 52: Power Supply Current Test Circuit

101A

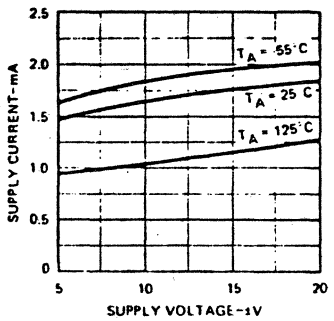


Figure 53:
Power Supply Current

101A

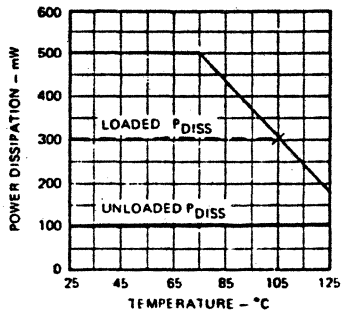


Figure 54:
Power Dissipation

Sometimes neglected in the calculation of worst case circuit power consumption are:

- Circuit power consumption is specified unloaded.
- Worst case device power dissipation does not occur at the maximum operating temperature extreme.

A loaded operational amplifier will cause additional power to be dissipated. As an example, if 10V rms is delivered to a 2Kohm load, 5mA is supplied through the operational amplifier. If the no load current is 2.5mA (10IA limit) the loaded current requirement is the I_{TOTAL} = 2.5mA + 5mA = 7.5mA. This increases the actual internal power consumption by:

$$(7.5mA \times 40V) - (2.5mA \times 40V) = 200mW$$

Figure 53 shows the variation of power supply current with supply voltage as a function of ambient temperature, and Figure 54 can be used to see the effect of increased internal power dissipation due to loading.

The dashed line indicates the circuit cannot be safety operated at +125°C without heat sinking a reduction in supply voltage (±20V) or reducing the load. As shown, the unloaded device can be safely operated and loaded to increase internal dissipation to 175mW without heat sinking. Be sure your worst case power dissipation has been examined. Don't count on one spec limit (V_{OUT}, I_{OUT}) to protect you from exceeding another P_{DISS}.

Because monolithic resistors increase approximately 0.2%/°C, the linear integrated circuit draws less current at high temperature.

Output Shortcircuit Current, I_{SC}

Output shortcircuit current is the maximum output current available from the amplifier with the output shorted to ground or to either supply. Most linear integrated circuits are output short circuit protected. Unfortunately, not all suppliers perform adequate 100% tests to ensure indefinite short circuit protection. To guarantee this parameter, it is necessary to measure the available output current of each device under shorted conditions to ensure that each device is capable of supplying sufficient current in excess of the safe operating internal power rating. These minimum current limits should be a part of every user's specification. It is the parameter most often left unspecified.

Slew Rate (Large Signal Bandwidth) and Bandwidth

The two dynamic parameters specified for op amps are slew rate and rise time (or bandwidth).

Bandwidth is the frequency at which the differential gain is 3dB below its low frequency value. Slew rate is the internally limited rate of change in output voltage with a large amplitude step function applied to the input.

The slew rate may not be constant as the output voltage changes. The more pronounced the break points in the slope of the response curve are, the more variation will occur in the slope, as the output signal slews. It should also be noted that the slew rate in the positive direction may be different than the negative going rate.

Both bandwidth and slew rate measure the ac performance of an operational amplifier. Bandwidth is a small signal term which is specified and tested for in terms of rise time and overshoot. Rise time is defined as the time required for a small signal output voltage step to change from 10% to 90% of its final value as shown in Figure 55. The output voltage change, specified, must be small to ensure that all stages in the amplifier are operating under small signal conditions. Typical output response for a uA709 is shown in Figure 55 and approaches that predicted by G BW considerations as shown.

The equation for estimating transient response of a linear first order system is as shown in Figure 55.

Overshoot is the amplitude in percent above the final value of the amplifier reached when responding to a step input. Both parameters have theoretical and practical significance.

(1) $\text{Bandwidth} = \frac{0.41}{tr}$

for overshoot = 0%

(2) $\text{Bandwidth} = \frac{0.45}{tr}$

for overshoot = 5%

(3) $\text{Bandwidth} = \frac{0.51}{tr}$

for overshoot = 9%

Although these equations idealize the practical situation in terms of either Gaussian or constant amplitude response, they do provide a useful measure of amplifier bandwidth using pulsed step response techniques.

As examples using the values from Figures 57 and 58 for the 715 and 741 operational amplifiers:

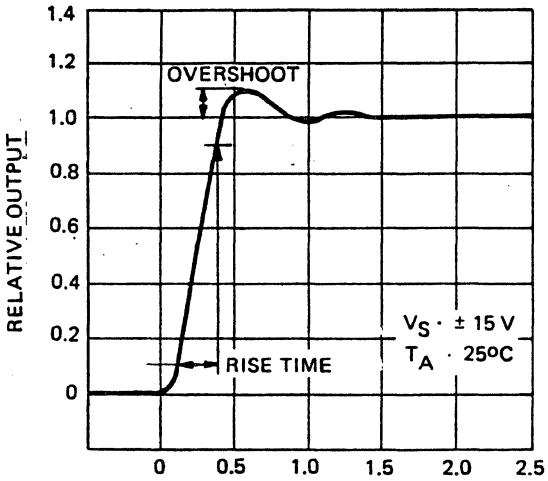
$tr = 75ns$

$\text{overshoot} = \frac{30mV}{400mV} = 7.5\%$

715 Operational Amplifier

Selecting Equation (3):

$$\text{Bandwidth} = \frac{0.51}{tr} = \frac{0.51}{0.075 \times 10^{-6}} = 68MHz$$



μA709 Transient Response

GBW for μA709 connected for A_{CL} = OdB = 1 MHz

$$t_r = \frac{0.35}{f}$$

$$t_r = \frac{0.35}{1} = 0.35\,\mu S$$

Figure 55: Rise Time

715

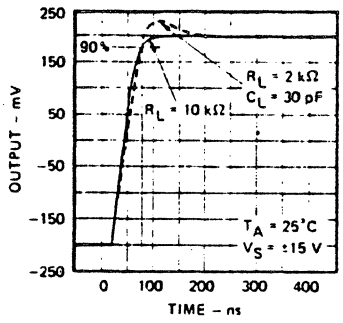


Figure 56

741

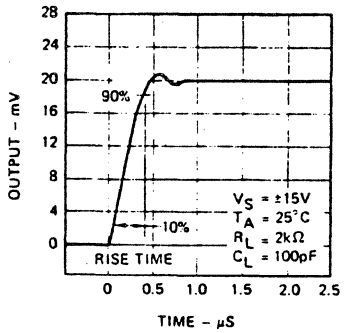


Figure 57

741

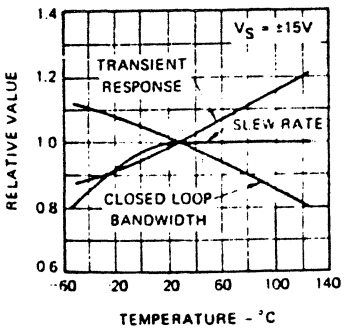


Figure 58

741

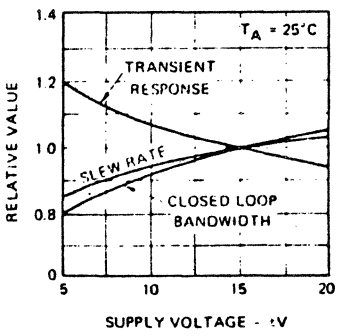


Figure 59

tr = 0.4us

overshoot = $\frac{1mV}{20mV}$ = 5%

741 Operational Amplifier

Selected Equation (2):

$$\text{Bandwidth} = \frac{0.45}{tr} = \frac{0.45}{0.4 \times 10^{-6}} = 1.1MHz$$

As temperature increases, the transient response (bandwidth) of the amplifier is reduced even though transistor $f\lambda$ (carrier mobility) is improved. This is the result of increasing diffused load resistors with temperature. Reduced supply voltages (Figure 59) reduces bandwidth (increases tr) due to effectively wider transistor basewidth.

Linear integrated circuit suppliers do not measure operational amplifier bandwidth or guarantee it. Rise time and overshoot are specified, however. These parameters do vary from manufacturing lot to lot as much as 20 to 30% in some monolithic operational amplifiers.

The practical application of operational amplifiers is more concerned with the large signal bandwidth or slew rate of the amplifier. Most applications require the amplifier input and output to swing ±10V and drive large amounts of current (5mA). This is not considered a small signal operating mode and cannot be analyzed as such. It is a nonlinear problem and must be analyzed as such. The term slew rate describes the amplifier under these nonlinear conditions.

Figures 60 and 61 show large signal bandwidth and slew rate. They are related by the expression:

$$\text{Slew Rate} = (V_{peak})\ (2\pi x \text{ large signal bandwidth})$$

Using the values from Figure 60 for the 101A compensated for unity gain bandwidth, the large signal bandwidth is approximately 4KHz.

$$\text{Slew Rate} = V_{peak}\ (2\pi \text{ large signal bandwidth})$$

$$= (14V)\ (2\pi x\ 4 \times 10^3\ Hz)$$

$$\text{Slew Rate} = 0.35V/us$$

The large signal pulse response given for the 741 in Figure 61 indicates that the amplifier output will swing from -5V to +5V in 15us on the leading edge and in 20us on the trailing edge.

$$SR_{\text{Leading Edge}} = \frac{10V}{15us} = 0.67V/us$$

$$SR_{\text{Leading Edge}} = \frac{10V}{20us} = 0.5V/us$$

Notice that the negative going slew rate differs from the positive and is degraded. Figures 62 and 63 for the high slew rate (SR = 15V/us) 715 also indicate this effect.

The amplifier can follow an input signal until the input stage can no longer supply a proportional current to the second stage. The second stage is effectively an integrator and because the input differential pair dynamic range is limited to 2I (total current available from the current source), the output of the integrator will begin to distort upon input stage limiting.

If 2I varies from unit to unit or over temperature, then it is clear that variations in slew rate will result. Operational amplifiers such as the 101A, 107, and 108 are designed for constant I_B over temperature so that low $\Delta I_{OS}/\Delta T$ is obtained. In order to do this, a complex current source biasing network is required that depends upon critically interrelated pinch resistor, EPI resistor, and V_{BE} tracking. This network is not designed to insure constant source current from run to run, but source current that tracks h_{FE} with temperature. The result is 30% to 40% run-to-run variation in slew rate and large signal bandwidth. Other amplifiers of different current source design do not exhibit such variation, but also do not provide a low $\Delta I_{OS}/\Delta T$.

Figures 62 and 63 show degraded slew rate performance when the operational amplifier output swings to -10V. This lack of output symmetry is due to the h_{FE} and $f\lambda$ limitations of pnp transistors and level shifting techniques that result in current drive limitations at frequency.

Noise

In ac coupled circuits, it is not the drift but the random noise signals which are generated in the amplifier which limit the lowest recognizable input signal. One noise figure of extreme importance is popcorn noise.

Popcorn noise is of such amplitude, that if present at the frequency of interest low level noise current and voltage measurements are meaningless. Unfortunately, when most suppliers present typical noise curves, they discard "popcorn" noise devices from the "typical" sample. Popcorn noise is primarily noise current and is related to surface cleanliness. It increases with temperature. It is discussed as the percentage of units exhibiting popcorn noise rather than by amplitude definitions. The lower operating current the amplifier, the fewer number of "popcorn" noise devices and the lower the amplitude. The 108/208/308 amplifier is the best performer to date with respect to this parameter. The 741 is one of the worst.

Input Noise Voltage is defined as the square root of the mean square narrowband noise voltage at the output divided by the measurement system gain with low source resistance and is given by the following formula:

$$\text{INPUT NOISE CURRENT} = \sqrt{I_N^2} = \sqrt{\frac{\overline{e_{meas}}^2 - 4kTR_S - \overline{e_N}^2}{R_S^2}} \quad \text{for } \Delta f = 1\text{Hz}$$

101A

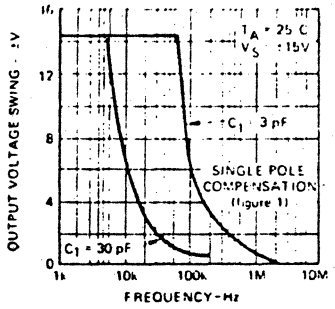


Figure 60

741

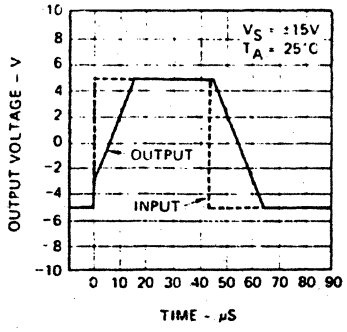


Figure 61

715

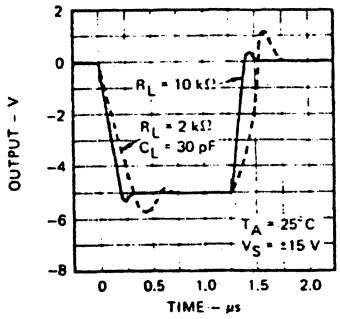


Figure 62

715

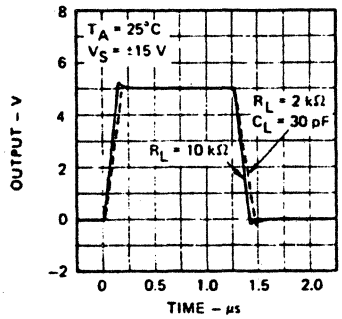


Figure 63

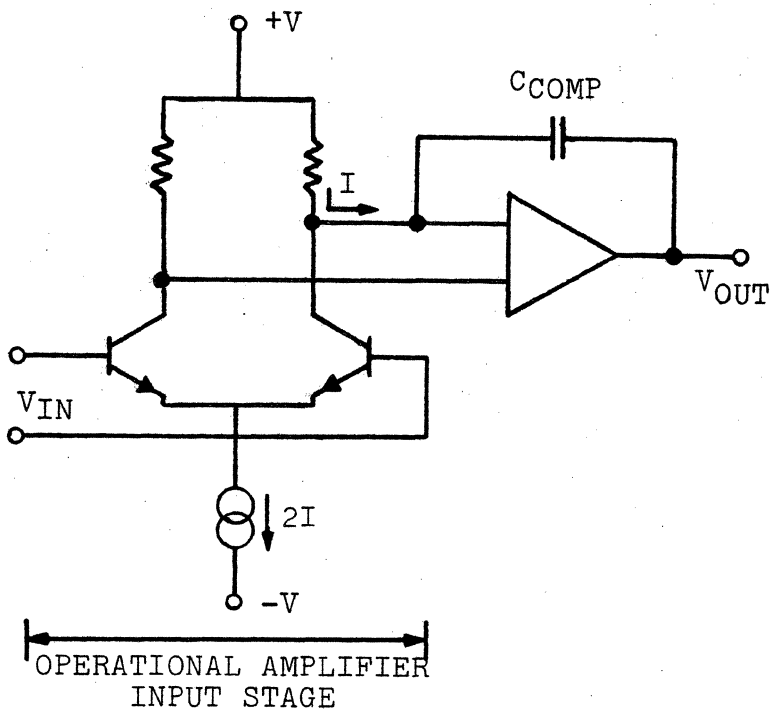


Figure 64

Broadband Noise is the total RMS noise at the output of the amplifier, over the specified bandwidth and source resistance, divided by the gain of the amplifier. Noise measurements are only performed upon request and are not part of the supplier's test sequence.

4.313 Op Amp Test Methods

Meaningful testing of op amps has become a controversial issue: test methods and usefulness have been questioned. Test circuits shown in MIL-STD-883 were originally developed for hand testing the first generation of amps, such as the 709. These circuits are not suited for automatic test equipment due to the large number of circuit changes required in a test sequence and because they are mostly for ac testers. Satisfactory testing of present day op amps, such as the 108, 108A and 725 for dc characteristics is not possible with MIL-STD-883 test circuits.

This section discusses the common pitfalls encountered when testing op amps and presents several general purpose test circuits for measuring the performance of today's op amps that work both for bench testing as well as for automatic test equipment.

Complete dc testing requires a test circuit such as that shown in Figure 65. Table 5 provides a detailed step-by-step "cook book" approach, using a 741 op amp as an example, to be used in measuring and calculating the data sheet electrical parameters using the circuit of Figure 65.

The dc parameters listed in Table 5 are by no means the only ones by which to judge an op amp's performance. Slew rate and noise are two important op amp characteristics that can be tested by Figure 66 and Figure 67 respectively. Figure 66a depicts a circuit suitable for measuring slew rate, small signal reset time and overshoot. To minimize phase shifts that alter amplifier rise time and overshoot, a small capacitor is added across the feedback resistor. This capacitor compensates for the simulated inductance across the input. For example, the commonly used circuit shown in Figure 66b has a faster rise time and more overshoot than the one in Figure 66a. A 100pF capacitor is added across the 10k feedback resistor in Figure 66b for a more accurate measure of slew rate, rise time and overshoot.

To produce low cost op amps, IC supplier keep device handling at a minimum through the use of automatic test equipment. Ac parameters, such as gain and phase margins and input and output impedances, can be bench tested in specially fabricated test fixtures. However, the added handling time and the special test fixtures required here escalate the device cost.

In some applications the input impedance is important. For dc applications, however, the input bias current I_{IB} is the limiting factor and is easily measured. As a result, it makes more sense and costs less to measure an op amp's input bias current, input offset voltage (V_{IO}) and input offset current (I_{IO}) at common mode extremes than to measure dc input impedance.

Input impedance becomes important for frequencies above 1kHz. Here it is more desirable to add a voltage follower, such as the LM110, to the amplifier's input than to test its ac input impedance.

TABLE 5 MEASURING DATA SHEET PARAMETERS

1. Input offset voltage at zero common-mode voltage[1]

a. *Measure:* $V_{test\,1}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 and S2 closed; $V_{test\,2}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 and S2 open

b. *Calculate:* V_{IO} $(R_S = 100\Omega) = \frac{V_{test\,1}}{1000}$ V_{IO}, $(R_S = 10k\Omega) = \frac{V_{test\,2}}{1000}$

2. Input offset current at zero common-mode voltage[1]

a. *Measure:* $V_{test\,1}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 and S2 closed; $V_{test\,2}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 and S2 open

b. *Calculate:* $I_{IO} = \frac{V_{test\,1} - V_{test\,2}}{(1000)\ (10k\Omega)}$

3. Input bias current at zero common-mode voltage[1]

a. *Measure:* $V_{test\,1}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 closed, S2 open; $V_{test\,2}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1 open, S2 closed

b. *Calculate:* $I_{IB} = \frac{V_{test\,2} - V_{test\,1}}{(2000)\ (10k\Omega)}$

4. Common-mode rejection ratio

a. *Measure:* $V_{test\,1}$ with $+V_S = +3V$, $-V_S = -27V$, $V_O = +12V$, S1 and S2 open; $V_{test\,2}$ with $+V_S = +27V$, $-V_S = -3V$, $V_O = -12V$, S1 and S2 open

b. *Calculate:* CMRR (dB) $= 20 \log_{10} \frac{V_{test\,2} - V_{test\,1}}{(24V)\ (1000)}$

5. Supply-voltage rejection ratio

a. *Measure:* $V_{test\,1}$ with $+V_S = +5V$, $-V_S = -5V$, $V_O = OV$ (GND), S1 and S2 open; $V_{test\,2}$ with $+V_S = +20V$, $-V_S = -20V$, $V_O = OV$ (GND), S1 and S2 open

b. *Calculate:* PSRR (dB) $= 20 \log_{10} \frac{V_{test\,2} - V_{test\,1}}{(30V)\ (1000)}$

6. Positive-gain and positive-output swing

a. *Measure:* $V_{test\,1}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1, S2 and S3 closed and S4 open for $R_L = 2k\Omega$ (S3 open and S4 closed for $R_L = 10k\Omega$); $V_{test\,2}$ with $+V_S = +15V$, $-V_S = -15V$, S1 and S2 closed, $V_O = -10V$, S3 closed and S4 open for $R_L = 2k\Omega$
or $V_O = +12V$, S3 open and S4 closed for $R_L = 10k\Omega$

b. *Calculate:* positive gain $= \frac{(+12V)\ (1000)}{V_{test\,2} - V_{test\,1}}$ for $R_L = 10k\Omega$;

or positive gain $= \frac{(+10V)\ (1000)}{V_{test\,2} - V_{test\,1}}$ for $R_L = 2k\Omega$

7. Negative-gain and negative-output swing

a. *Measure:* $V_{test\,1}$ with $+V_S = +15V$, $-V_S = -15V$, $V_O = OV$ (GND), S1, S2 and S3 closed and S4 open for $R_L = 2k\Omega$ (S3 open and S4 closed for $R_L = 10k\Omega$); $V_{test\,2}$ with $+V_S = +15V$, $-V_S = -15V$, S1 and S2 closed, $V_O = +10V$, S3 closed and S4 open for $R_L = 2k\Omega$
or $V_O = -12V$, S3 open and S4 closed for $R_L = 10k\Omega$

b. *Calculate:* negative gain $= \frac{(-12V)\ (1000)}{V_{test\,1} - V_{test\,2}}$ for $R_L = 10k\Omega$;

or: negative gain $= \frac{(-10V)\ (1000)}{V_{test\,1} - V_{test\,2}}$ for $R_L = 2k\Omega$

Note 1: To measure V_{IO}, I_{IO} or I_{IB} at common-mode voltage (Fig. 5) the power supplies are manipulated as follows:

for +12 V common-mode voltage, $+V_S = +3V$, $-V_S = -27V$, $V_O = +12V$

for −12 V common-mode voltage, $+V_S = +27V$, $-V_S = -3V$, $V_O = -12V$

Calculate: V_{IO}, I_{IO} or I_{IB} as illustrated above in the examples given for zero common-mode voltage

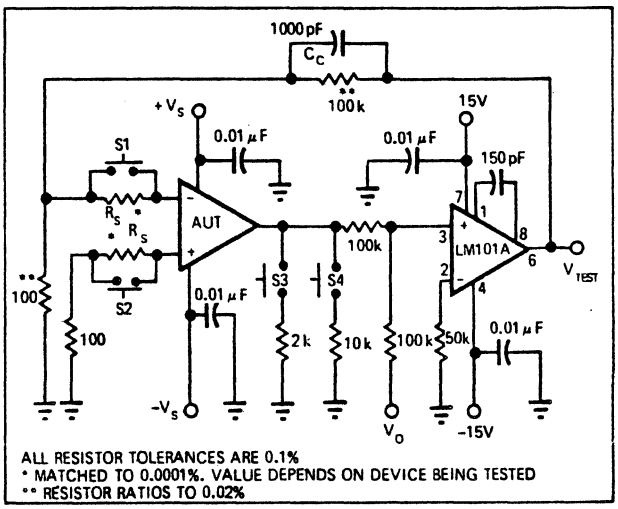


Figure 65: Complete op amp testing for dc characteristics can be achieved with this test circuit. Table 5 should be used in conjunction with this circuit.

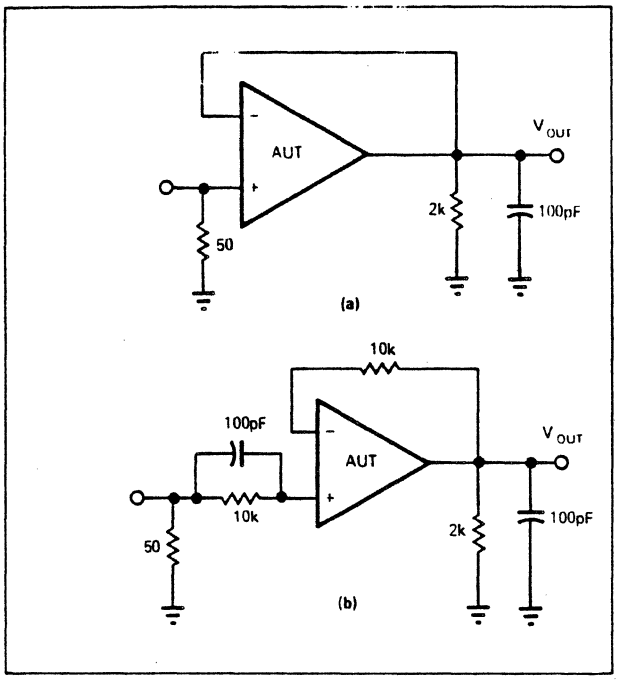


Figure 66: Slew rate, rise time and overshoot can be measured with either of these circuits. Stray capacitance will have little influence on (a), resulting in better correlation between test fixtures than (b) for small-signal risetime and overshoot tests. To measure op amp slew rate accurately, use (b). It has faster risetime and more overshoot due to amplifier phase shift.

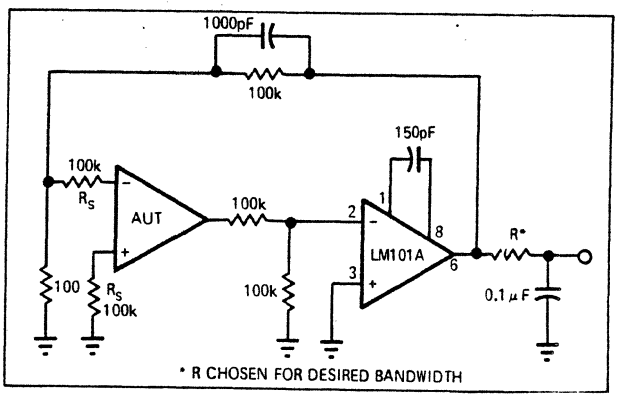


Figure 67: Measurement of op amp noise currents and "popcorn" noise is easily achieved with small variations of Figure 65.

Output impedance depends on closed-loop gain. For most modern op amps, the low frequency unity-gain closed-loop output impedance is less than 0.01 ohms. For applications where the closed-loop gain is less than 40dB, the output impedance can be neglected. Remember that most op amps incorporate output short circuit protection where the output decreases as the load current increases. For integrator applications, the maximum output current is normally limited by the short circuit current limit rather than by the output impedance. Settling time measurements can be made using the circuit of Figure 68. This circuit, which is a bench setup and not adaptable to automatic test systems, allows determination of the time constant and the closeness of fit to an exponential.

Referring to the schematic, the basic settling-time measurement circuit includes R1, R2, CR1 and CR2. The unknown signal is applied to R1 and a dc reference is applied to R2. The result is that as the unknown approaches the dc reference (which is set to a voltage that is the negative of the unknown final value), the output approaches OV as the input approaches the final value. CR1 and CR2 reduce the scope's overload.

If the dc reference is replaced with a switched reference, a null can be produced for every instant of time that the signal and the reference are the same. Thus, if the reference is a first order exponential, the output will reflect any deviation of the unknown from an exponential and when the "γ adjust" is set for minimum output, the 10 kohm potentiometer will be proportional to the time constant. Of course, the exact γ is (R3 + R4) C1 = γ. The R3 potentiometer can be calibrated directly in time constant.

4.314 Common Test-Circuit Problems

All too often, op amps that show up as bad devices at a user's receiving inspection station or in actual use are in reality good devices because of test circuits employed and the manner in which they were tested.

To prevent these test circuit problems, use the test circuit of Figure 65 and follow the precautions listed below:

1. Check for oscillation of the test loop. Incorrect compensation of the buffer amplifier will cause oscillations which show up as excessive offsets, low gain, high supply current, or as oscillations. A capacitor C_c in Figure 65 will normally stabilize the loop.

2. When checking input voltage, take care not to cause the inputs of the op amp to break down as this will degrade input characteristics. This is particularly important when testing devices like the 709 and the 725 which have low input breakdown voltages of 6V.

   There are two ways of measuring maximum input voltage. The first method makes use of a current which is forced through the inputs. The subsequent breakdown voltage is measured. This method, however, is not recommended since it causes reverse base - emitter breakdown of the input transistors and degrades input performance.

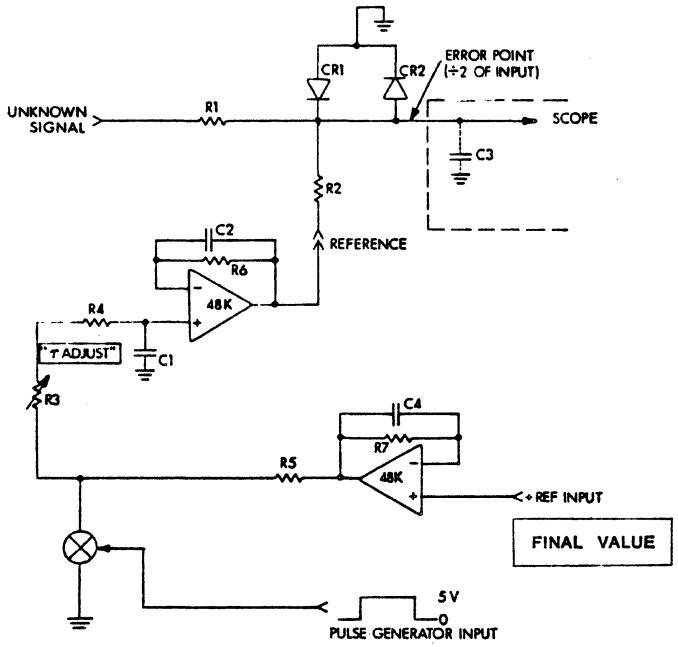


Figure 68: An unknown input is compared with an exponential, and the difference is displayed on an oscilloscope. The exponential waveform's time constant and final value may be adjusted to yield zero deflection of the oscilloscope for every point in time when the unknown is identical to the exponential.

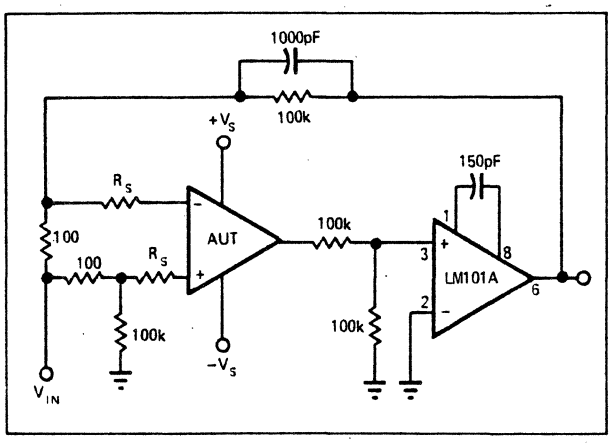


Figure 69: Resistor tolerances can produce significant errors in the measurement of an op amp common-mode rejection ratio (CMRR). The value of the source resistors R_S depends upon the type of amplifier under test.

With the second method, a voltage is applied to the inputs and the resultant current is measured. This method is a much safer one in that it does not degrade the op amp.

3. Check the tolerances of the circuit components. Incorrect tolerances of the circuit resistors can produce a significant measurement error. For example, if the common-mode rejection ratio (CMRR) is being tested by varying the input voltage as shown in Figure 69, resistor matching must be such that the error (twice the resistor match) is small compared to the measured value. If CMRR is to be measured to 80dB, the resistor match should be at least 100dB or 1 part in 10^5 - a 0.001% match.

   When using source resistors R_S, they must also be matched to minimize the error due to bias current change with input voltage. This is also necessary when using the circuit in Figure 65. During the era of the 709 op amp, a resistor match of 0.02% was sufficient. For modern op amps, such a match of 2 parts in 10^4 is twice the magnitude of the error that you're trying to measure. This will either add or subtract from the CMR error of the op amp.

4. Minimize thermal effects when performing dc tests. Thermal effects are particularly noticeable when making gain measurements - especially where negative or infinite gains are often measured. Thermal effects can be minimized by pulse testing with a very short duty cycle of less than 5%. In this way the instantaneous and time dependent effects can be observed. With these tests, and even with tests where the junction temperature of the device varies a small amount, the difference between the instantaneous and the final values is dependent on the loop response time. For relatively slow devices such as the 725, the loop response combined with thermal response may be greater than 30 seconds for certain tests.

5. Input and output voltages must not exceed either of the supply voltages during usage or testing. Transients that occur when the power supply is turned ON and OFF often result in a higher input voltage than supply voltage. This condition can cause a catastrophic op amp failure. The negative supply voltage or ground should always be applied first or simultaneously with the positive supply to avoid "latch up" or device destruction. Some op amps can be destroyed when an input voltage is applied to the op amp and both supplies are turned OFF. This turns ON the collector base diode of the input transistors and grounds the positive power supply while it is OFF.

   Device inputs can be degraded if a dc voltage is placed on the output of an integrator or on the input of a sample and hold circuit and the positive supply is again OFF. If a large capacitor is used, the inputs may be destroyed.

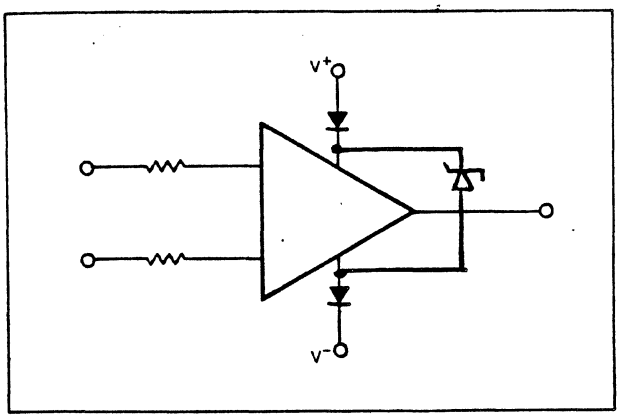


Figure 70: To protect an op amp from power supply transients and high input voltages, a pair of diodes and two resistors are used.

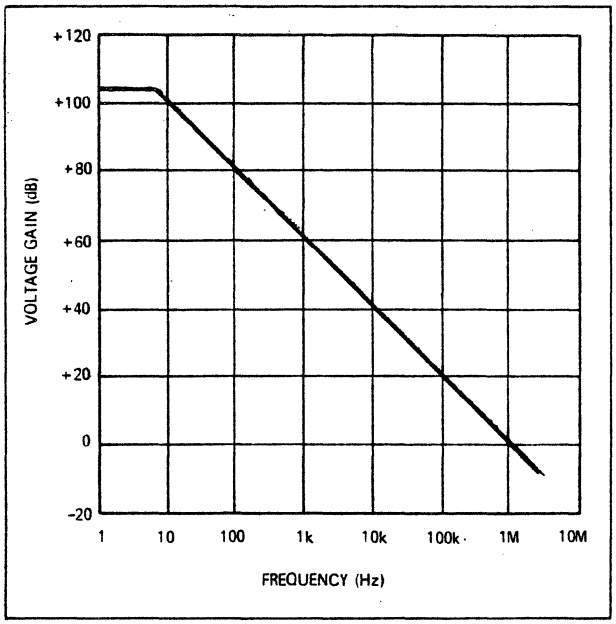


Figure 71: Op amp open-loop gain should be measured at dc to 5Hz, since the gain of most amplifiers begins to roll off beyond 5Hz. Frequency response shown is typical for an amplifier with single pole compensation.

A high voltage diode inserted in each power supply lead will prevent failures caused by transients and power supply reversals. Additionally, a resistor inserted in each input will limit the input current caused by high transient voltages (the zener diode protects against overvoltage). Both of these configurations are shown in Figure 70.

4.315 Op Amp Testers

Op amp testers are capable of testing almost all linear circuit parameters - open loop voltage gain, input offset voltage and current, power supply sensitivity and overshoot, etc.

However, measurements of voltage drift with temperature of dc amplifiers is still extremely slow, difficult and expensive. Also the measurement of input impedance at high temperatures tends to be relatively inaccurate. In fact, all extreme temperature measurements in linear circuits get to be questionable unless every last item of variation in wiring harnesses, external components and allowable noise levels is tied down.

An op amp tester should be capable of checking an op amp's performance over the entire guaranteed operating range. Common mode rejection ratio (CMRR) must be checked over the entire input voltage range. CMRR degrades at the common mode extremes. Testing CMRR over a 30V input range provides a large range of measurement accuracy particularly when testing op amps with greater than 100dB of common mode rejection.

For devices such as the LM101A and LM107 whose parameters are specified over the entire common mode range, input offset voltage, input offset current and input bias current must be tested at the input voltage extremes. The testing of input offset current at the common mode extremes is particularly important because it can detect channels in the input transistors as well as high temperature failures.

At least one parameter should be tested at the minimum specified supply voltages - power supply rejection ratio (PSRR). It should be measured by varying both power supplies simultaneously from minimum to maximum values. As with CMRR a larger voltage excursion permits greater test accuracy.

Gain should be measured either at dc or at low frequency ac (5Hz or less) since the gain of most op amps begins to roll off at about 5Hz (Figure 71).

4.316 Op Amp Test Circuits

Op amps are segregated into several families of devices - previously determined by input/output characteristics. These categories are:

- General Purpose
- FET Input
- High Slew Rate
- High Current

4.317 General Test Information

Op amps are subject to static discharge phenomena as are MOS devices, which causes the inputs to degrade, increasing input current. MOS and CMOS input op amps are subject to the same handling procedures as are CMOS and MOS logic circuits. Input bias current is the critical parameter for device stability. Input impedance is not tested; it is guaranteed by I_{bias}.

For general purpose op amps (741, 101A, etc.) one could obtain good correlation between dc characteristics and temperature drift. Now with specialized circuits, such as the BiFET LF156 op amp, 100% temperature drift testing at low temperature is a must. High temperature drift is predictably 15uV/°C and repeatable, but 5uV/°C is not predictable.

Suppliers do not test parameters that require elaborate bench setups - those that are not easily automatible: input impedance, rise time, overshoot, phase margin, gain margin, settling time, noise, and the like.

Suppliers can test gain bandwidth (GB) product at fixed frequency, but not at different frequencies. GB product is not the same as unity gain crossover. If gain rolls off at 6dB/octave and another pole is not seen, a unity gain point is never reached. GB product is dependent on whether the input signal is put on the inverting or noninverting input. Have the supplier define what input is tested.

FET Input Op Amp

Gate current doubles every 10°C rise in temperature. If I_{OS} = 25pA at 25°C and the chip has a 10°C rise to 35°C due to junction heating, the I_{OS} limit becomes 40pA. One must look at quiescent dissipation and loading conditions.

There is a problem with low inputs with the standard configuration of Pin 4 = V-, Pin 3 positive input, and compensation on Pin 1. There is large voltage potential between the input and the adjoining pins. If the resistance between the pins is 10^9 ohms, due to circuit board wiring, and a 1V differential exists, a leakage current of 1nA would exist. This is not insignificant with a pA input device. 15V differential between Pins 4 and 3 would produce 5nA of leakage current - again, a significant amount. Thus, computer interface board and pc board layout is extremely important.

If an op amp is as good as the specifications say it is, can you really use it? Do you care about 15 to 20pA input current? If so, don't put the device on a pc board. One LIC vendor floats the inputs on teflon standoffs when making his electrical measurements.

There is good correlation between 25°C and high temperature extremes; currents increase at predictable rates. Under cold conditions, there is poor correlation due to leakage effects caused by condensation. Circuit mounting may not allow you to use asset of part. FET input op amps must be 100% tested for temperature drift.

High Slew Rate Op Amp

Several points regarding the testability of high slew rate op amps are as follows:

- The higher the input stage current, the faster the device.
- How much current is required to charge the compensation capacitor?
- Slew rate is sample tested on a regular basis or 100% tested depending on supplier's device.
- Slew rate is process dependent.

Power Op Amp

Pulse testing which is used on automated systems, is undefined testing because the chip temperature is not stabilized. Duration of pulse, quiescent power dissipation, and integrity of die all affect the test results. One must pay attention to thermal layout to minimize errors due to thermal gradients across the chip.

4.32 Voltage Comparators

A differential voltage comparator is a high gain, differential input, single ended output amplifier. A comparator is simplistically an op amp with a zener diode as a clamp. However, the use of an op amp as a comparator provides limited response time for most applications. The function of a comparator is to compare a signal voltage on one input with a reference voltage on the other and producing a logic "1" or "0" at the output where one input is higher than the other.

Being similar to an op amp, the comparator is characterized by some of the same parameters - input offset voltage and current, output bias current, voltage gain, input voltage range, response time, and supply current. In addition, several new parameters are specified: saturation voltage, output leakage current, and strobe on current. Thus in testing the comparator, some of the guidelines presented previously for op amps also apply. In addition, the following list summarizes potential difficulties in testing voltage comparators.

- Specification problems.
- Open or closed loop operation. The voltage comparator is not designed to be operated stable in a closed loop condition; however, suppliers specify closed loop parameters A_V, I_{OS} and I_{PIDS}. Thus, a conflict exists.

- Testing a comparator closed loop doesn't reflect usage.

- Example of specification problem: LM111 comparator strobe current. LM111 is strobed with a current source. This is a test condition, not a test limit. Military specifications say to measure this strobe current, but it can't be done. Thus the test is meaningless.

- Some comparators can't be measured closed loop. All you can do is put a voltage on the input and see if the output switches (NE521/522, 527/529). These are really digital circuits.

- PSRR, CMRR and Gain can't be measured if there is no closed loop operation.

Comparators tend to oscillate in many instances in the active region of operation. This active region is very narrow. The parameters of input offset voltage and current and gain are performed using error band testing. Thus a degree of uncertainty exists. Also as with op amps, the inputs are sensitive to static discharge, and input currents tend to increase as the device degrades.

4.33 IC Voltage Regulators

An IC voltage regulator consists of an error amplifier (op amp), a zener voltage reference and a pass transistor circuit all on one chip. The pass circuit usually includes the short circuit current limit transistor.

To a large extent, each of these constituents of the IC regulator is tested separately. When a load is applied to the operational amplifier, the output voltage will decrease slightly due to the output resistance to the amplifier.

With an integrated circuit regulator, another factor must be considered when computing the total change in output expected under a given set of loading conditions. This is the heating of the chip caused by increase in load current. Since the voltage reference is not perfect, its output will change with temperature, whether the temperature change is in the ambient air or is caused by loading the regulator. As an example, consider the 723 under the standard test conditions of V_{IN} = 12V, V_{OUT} = 5V, and I_L = 1mA to 50mA:

- Typical load regulation = -0.03%
  Change in power dissipation due to loading = 49mA x 7V = 343mW
  Increase in chip temperature = $343\text{mW} \times \frac{1}{6.8\text{mW}/^\circ\text{C}} = 50.5^\circ\text{C}$

- Typical temperature coefficient of output voltage = ±0.002%/°C; therefore, the change in the output voltage due to temperature is +0.002%/°C x 50.5°C = ±0.101%.

- Thus, the change in output will be -0.131% or +0.071%, depending upon the direction of the drift of the reference voltage.

It is obvious that the temperature drift effects are the dominant factor under these particular conditions.

Suppliers of integrated circuit voltage regulators specify load and line regulations under conditions of CONSTANT CHIP TEMPERATURE so that the performance of the regulating section of the circuit can be measured separately from the temperature drift of the reference. This makes it possible for the user to calculate the overall performance of the regulator under any conditions of input voltage, output voltage and loading.

Constant chip temperature is achieved by making the measurements under pulsed conditions with the load applied for only a short time and with a low duty cycle. Since the regulator is tested at essentially constant junction temperature, it is necessary to use a low duty cycle when bench testing in order to correlate the results. This eliminates the temperature drift in the reference caused by the large change in power dissipation when the regulator is loaded.

Line regulation (and its ac counterpart - ripple rejection) is the measure of reference stability with changes in input voltage. Supply voltage rejection of the error amplifier is also a factor, but it is usually an order of magnitude better than the regulation of the reference. Temperature drift measures the reference stability with respect to temperature variations. Again, temperature drift of the error amplifier is much less than that of the reference.

Load regulation is governed by the amplifier gain as is the regulator input impedance. The pass transistor also affects both the load regulation and the effective output impedance of the regulator. As the load current increases, the drop across the current limit sense resistor increases and the current limit transistor begins to conduct. This causes the output voltage of the regulator to change before current limiting occurs affecting load regulation and regulator output impedance. For this reason, some regulators are specified with the current limit sense resistor shorted.

Maximum regulator output current and short circuit current are functions of the pass circuitry, except that maximum output current is also limited by the maximum allowable package power dissipation. In this respect, maximum output current is also limited by the quiescent current.

4.331 Prime IC Regulator Performance Specifications

Line Regulation

One major problem with all voltage regulator parameters is that no all suppliers specify them in the same way. Line regulation is defined as the percentage change in regulated output voltage for a change in input voltage.

Ripple Rejection

Ripple rejection is ac line regulation. Whereas line regulation is measured at dc, ripple rejection is defined as the line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal. Like line regulation, ripple rejection is sensitive to input/output differential voltage.

Load Regulation

Load regulation is defined as the percentage change in regulated output voltage for a change in load from minimum load current to the maximum load current specified (for example, from 0 to 50mA load current for a 723 regulator). One problem encountered in measuring and specifying both line and load regulation is the chip temperature variation due to input voltage and load variations. Suppliers normally specify temperature drift separately.

Standby (Quiescent) Current Drain

Standby current drain is that current which flows into the regulator and through to ground. It does not include any current drawn by the load or by external resistor networks. Standby current drain reduces the maximum output current capability because of quiescent power dissipation as shown in the following example:

Conditions E_{IN} = 40Vdc, T_A = 50°C

Find: Power limited full load current.

REGULATOR X	REGULATOR Y
T_j max = 150°C, P_{diss} max = 800 mW	T_j max = 150°C, P_{diss} max = 800 mW
Θ_{ja} (TO5) = 150°C/W	$\Theta_{ja} = \frac{1}{6.8\ mW/°C} = 50°C$
ΔT = 100°C with T_a = 50°C	ΔT = 100°C with T_a = 50°C
$(\frac{100°C}{150°C})$ (1W) = 667 mW available	$(\frac{100°C}{150°C})$ (1W) = 667 mW available
Worst case quiescent of Regulator X current = 2mA	Worst case quiescent of Regulator Y current = 4mA
Internal P_{diss} = (2mA) (40V) = 80mW	Internal P_{diss} = (4mA) (40) - 160mW required
Therefore, the device can dissipate only another 667 mW = 80 mW = 587 mW	Therefore, the device can dissipate only another 667 mW = 160 mW = 507 mW

Conclusion: Regulator X can deliver more output current than can Regulator Y. This is primarily due to the much lower standby current of Regulator X.

Temperature Drift

Temperature drift is the percentage change in output voltage (or reference voltage) for a temperature variation from room temperature to either temperature extreme. Approximately 85% to 90% of this drift occurs in the regulator's internal reference circuitry. The remaining 10 to 15% is due to error amplifier or bias current drift. Temperature drift is the major cause of output voltage change in an IC regulator.

Example of Nonconstant Junction Temperature

Load regulation under actual usage conditions will be worse than the regulator spec limits due to temperature drift.

Conditions	Regulator Spec Limits
E_{IN} = 12V	Load Regulation 0.1%
E_{OUT} = 5V	Temperature drift 0.01%/°C
I_L = 1mA to 50mA	θ_{JA} = 160°C/W

- Change in power dissipation = (12V - 5V) (50mA - 1mA) =

  7V x 49mA = 343mW

- For a θ_{JA} of 160°C/W, the temperature rise will be

  (160°C/W) (0.343) = 55°C

- With a specification temperature drift of 0.01%/°C, the output voltage change is

  (5V) (0.01%) (55°C) = 27.5mV

- However, the output voltage change due to load regulation is

  (0.1%) (5V) = 5mV

- Thus, the output voltage effects due to temperature drift swamp out the effects due to load regulation.

The same analysis applies to line regulation. However, it should be noted that large line variations of long duration that raise the chip temperature more than a few degrees are seldom a problem.

What does this example mean? If one desires, the best regulation possible when the load current changes, one should minimize chip temperature changes

by using an external pass transistor. In addition to reducing chip temperature variations, operating a regulator at lower than rated load currents results in improved load regulation as illustrated in Figure 71A. Because a voltage regulator is specified over a wide range of conditions, it is not a simple matter to test it.

How then should one go about testing these parameters? The answer to this question is generally dependent on who does the testing: the supplier or the user. A supplier must use automatic test equipment to be cost effective and thus competitive in the commercial marketplace. Automatic equipment can test a regulator in much less than one second. This means that there is little heating of the device during the test sequence. For this reason, most parameters are specified at constant junction temperature (T_j) with temperature drift specified separately.

The user, however, must be careful since in actual applications, and unlike op amp applications, the regulator is rarely operated at a constant junction temperature. How this effects line and load regulation is illustrated by the example just presented.

4.332 Voltage Regulator Test Circuits

Since an IC voltage regulator looks much like an op amp, it can be tested in a similar circuit. Figure 72 shows the circuit diagram for a universal IC regulator test setup.

The user can plug in almost any existing IC regulator - a Fairchild 723, a national LM105, a Motorola 1566, etc. - into this general purpose circuit and by cycling the setup switches S1 to S4 through the seven modes shown in Table 6, check the specifications that are important to a user. However, this circuit cannot be used for regulators where the feedback loop is kept inside. For example, the fixed output LM109 which has just three terminals, input, output and ground, could not be connected into this tester.

The universal test circuit of Figure 72 has an op amp buffer in the regulator's feedback loop. This buffer permits the output of the regulator under test to be adjusted independently of the regulator's V_{REF} eliminating the need for different dividers for different output voltages. The adjustment is through an external signal $V_{OUT(SET)}$.

Take the case of a 723 regulator being tested in mode 4 of Table 6. For this mode the raw dc input, V_{IN}, to the regulator is 40V and the V_{OUT} should be +37V. The +37V is commanded by making $V_{OUT(SET)}$ -37V. Figure 73 shows how the voltages adjust around the loop. This can be understood by considering that the differential inputs of the two amplifiers in the loop - the error amplifier and the buffer amplifier - must respectively be within millivoltages of each other. Then the inputs to the error amplifier must be at the 7.15V level of the regulator reference and the inputs to the buffer amplifier must be at the ground level of the inverting input. The loop takes care of the rest.

The voltage measurements V_M for the tests are made at the output of the buffer amplifier. This voltage is essentially the same voltage as at the

TABLE 6

VOLTAGE REGULATOR TEST SEQUENCE

Test		APPLY (IN VOLTS)		SWITCH POSITIONS					MEASURE	MEASURED PARAMETER	
Mode	Parameter	V_{IN}	V_{out}	S_1	S_2	S_3	S_4	I_L	Value	Equation	Units
1.	Load Regulation (mid range)	12 12	−7.15 −7.15	open open	closed closed	open open	open open	MIN MAX	V_{M1} V_{M2}	Ld.R. = $\frac{V_{M2} - V_{M1}}{V_{M1}} \times 100$	%
2.	Line Regulation	40	−7.15	open	closed	open	open	MIN	V_{M3}	Ln.R. = $\frac{V_{M3} - V_{M1}}{V_{M1}} \times 100$	$\%/V_{IN}$
3.	Load Regulation (low end)	12 12	−2.0 −2.0	closed closed	closed closed	open open	open open	MIN MAX	V_{M4} V_{M5}	Ld.R. = $\frac{V_{M4} - V_{M5}}{V_{M4}} \times 100$	%
4.	Load Regulation (high end)	40 40	−37 −37	open open	closed closed	open open	open open	MIN MAX	V_{M6} V_{M7}	Ld.R. = $\frac{V_{M6} - V_{M7}}{V_{M6}} \times 100$	%
5.	Quiescent Current	30	−7.15	open	closed	open	open	MIN	I_Q	Direct	mA
6.	Ripple Rejection	12Vdc + ±1V @ 10KHz	−7.15	open	closed	open	open	MIN	V_{M8} (ac.)	Rp.R. = 20 log V_{M8}	dB
7.	I_{SC} (short ckt.)	12	−7.15	open	open	closed	closed	–	V_{SC} (V_{out})	$I_{SC} = \frac{V_{SC(mV)}}{R_{SC}}$	mA

inverting input of the error amplifier since the currents flowing into the error amplifier will be small. The output of the buffer amplifier makes a convenient, low impedance point to make these measurements.

The measurement V_M then reflects the change in the error amplifier voltage (relative to V_{REF} which will not change much) with the various V_{IN} and I_L changes imposed by the tests. It might be thought of as showing how "hard" the internal gain stages of the regulator have to work to counteract the imposed disturbances. The less the change in V_M, the higher the internal gain and the better the regulation ability.

To explain how the universal test circuit of Figure 72 is used, we will run down the seven modes of Table 6 one by one. We will be talking in terms of testing the 723 and the values in Table 6 pertain to this device. Different values would be used for other devices.

1. Load Regulation (mid-range)

   This is the basic test of the DUTs regulating ability for a mid-range input of 12V. The switches set up the conditions. Switch S2 is closed to short out the regulator's short circuit sensing resistor R_{SC} as the 723 specifications call for this. Obviously, this helps the 723 look better, especially at higher load currents because the short circuit cutout transistor is not robbing the DUTs pass transistor of base drive. But this may not be the most realistic test so far as the user is concerned for the application may call for operation with the short circuit protection. If so, it is a simple matter to also test with S2 open.

   As has been explained, the $V_{OUT(SET)}$ commands the regulator output voltage V_{OUT} to be its complement. For this basic mid-range test, the 723 is to be putting out its zener reference voltage or 7.15V. Therefore, $V_{OUT(SET)}$ is -7.15V. This means that even if the DUT's zener happens to stray from the 7.15V, as it can within the leeway allowed by the 723 specifications, the test circuit will still hold all DUTs at 7.15V, which makes for more uniform results.

   The constant current sink loading then "commands" the two specified output currents which set the range over which the Ld.R (Load Regulation) equation in the table will be computed. The 723 specifications call for an I_{MIN} of 1mA and an I_{MAX} of 50mA. Actually, because the test circuit holds V_{OUT} at a known level, fixed value resistors could be used for the loading rather than the current sink shown.

2. Line Regulation

   Because the "V_{M1}" measurement from the first mode can be retained and used for this computation, only one measurement has to be made in this mode. The V_{IN} is raised to 40V, its high end for the 723, and the change in V_M read. The computation for Ln.R

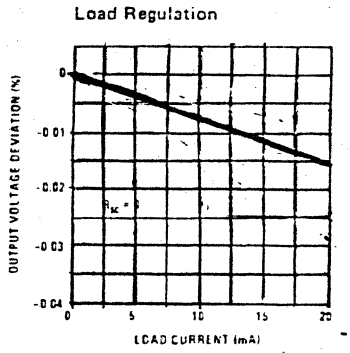


Figure 71A

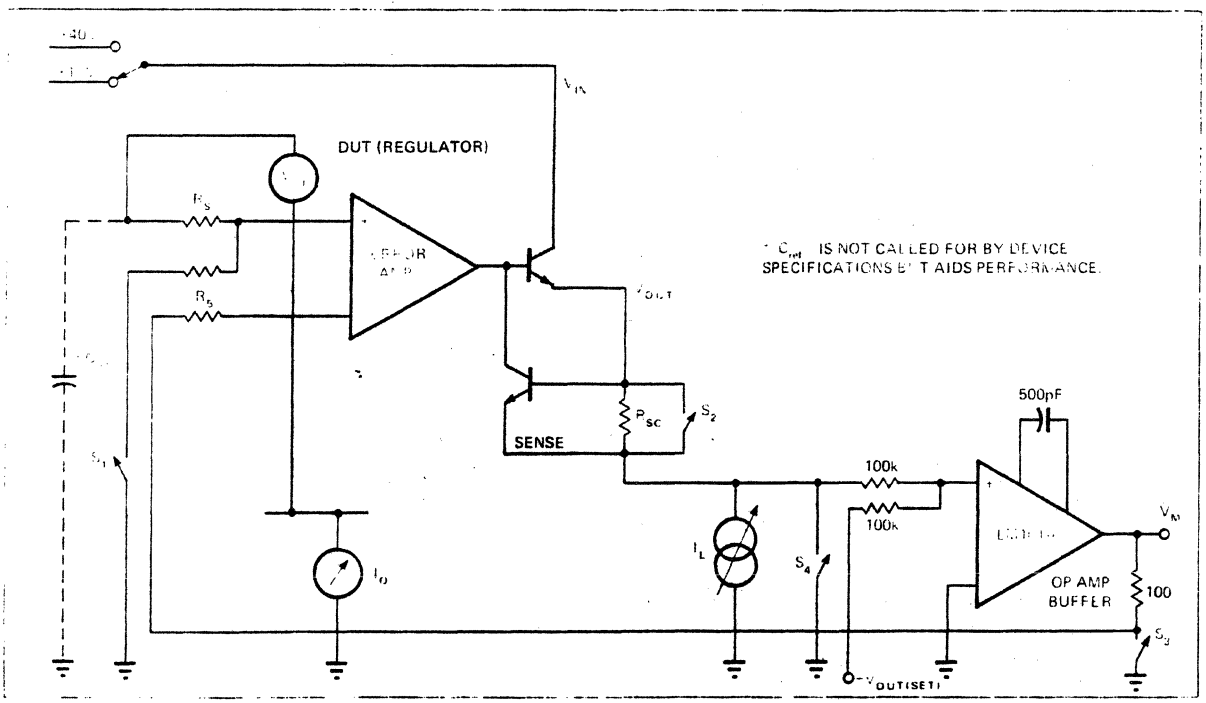


Figure 72: Basic general purpose IC voltage regulator test circuit is shown with manual switches for setting up the test modes. Table 6 lists how these switches should be operated for the seven basic tests. The values for the tests relate to the popular 723 IC regulator, but obviously, they could be adjusted to suite other low power linear regulators. The purpose of the buffer amplifier (LM101A) is explained in the text.

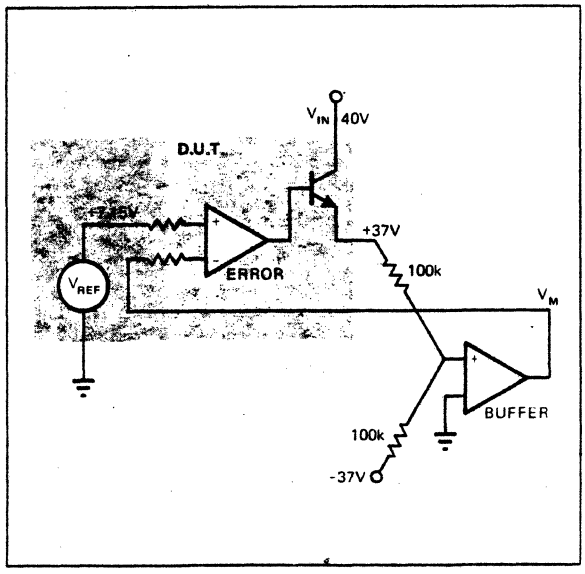


Figure 73: Independent adjustment of regulator-under-test's output is accomplished by applying an external signal to the buffer amplifier. The closed loop test setup forces the regulator-under-test's output to be the complement of this signal.

(Line Regulation) then represents how much the DUTs error amplifier input had to change to hold the V_{OUT} called for by $V_{OUT(SET)}$. This is an indication of the DUT's gain which in turn reflects on the DUT's ability to regulate. Specifications for this test call for load current of I_{MIN}.

3. Load Regulation (Low End)

The $V_{OUT(SET)}$ is put at -2V to set V_{OUT} at +2V and the change in V_M is read for the I_{MIN} and I_{MAX} load currents. Note that S1 is closed in this mode to properly simulate the fact that the positive or noninverting side of the DUT's error amplifier would be seeing a divided down or degraded portion of the DUT's V_{REF}. The purpose of closing S1 is not to command the lower output voltage because that is done independently by $V_{OUT(SET)}$.

4. Load Regulation (High End)

The $V_{OUT(SET)}$ is lowered to -37V to raise V_{OUT} to +37V and again the change in V_M is read for the I_{MIN} and I_{MAX} load currents. Again, the less V_M has to change, the better the DUT's regulating ability.

5. Quiescent Current

This test checks the current that the DUT itself is drawing. For the 723, the specified conditions for this test are that the input voltage V_{IN} be raised to 30V and the output voltage V_{OUT} be held at its nominal 7.15V mid-range value. The quiescent current is sensed in the ground leg as shown in Figure 72.

6. Ripple Rejection

The degree to which the DUT will regulate against ac variations in the input line is measured by superimposing a 10kHz ±1V signal on the midrange 12V V_{IN} and measuring the resulting ac signal on V_M. Again, the better the regulating capability of the DUT, the smaller the correction signal fed back to the inverting input of the DUT's error amplifier or the smaller V_M. Incidentally, the user may want to add a capacitor across the DUT's zener as shown by C_{REF} in Figure 72. The 723 test specifications don't allow this, but users often put it in as it significantly improves performance.

7. Short Circuit

In this final mode, the two switches that haven't been closed up till now - S3 and S4 - are closed and the one switch that has been closed up till this point - S2 - is opened. Switch S4 applies the short circuit at the DUT's output. Switch S3 is closed to simulate the fact that under this short circuit condition, the feedback to the DUT's error amplifier would be at ground. The 100 ohm resistor before S3 protects the output of the buffer amplifier.

Switch S2 is opened to activate the DUT's short circuit (overcurrent) protection circuit. The value of the short circuit current (the remaining current after the DUT overcurrent protection has shut the DUT down) is measured by looking at V_{OUT} which is now the voltage across the short circuit sensing resistor R_{SC}. This is the one instance where the voltage measurement isn't made at the output of the buffer amplifier.

A Semi-Automatic Version

Figure 74 shows how the circuit of Figure 72 can also be upgraded for more complete line and load regulation testing and also more closely approximate the high speed automatic test systems used by IC suppliers. This should interest the engineer whose company uses a fair number of IC regulators, but not enough to warrant the investment in fully automatic checkout equipment and who wants line and load regulation at other than standard conditions. Here some of the switches are transistorized for higher speed bounceless operation from electronic commands. Transistor Q_4 shorts the output to ground for the load regulation test. Switch S2 of Figure 72 which divided the reference voltage has been omitted for simplicity.

With this arrangement, the first four modes of Table 6 can be compressed into less than a minute. A triangular wave is fed into V_{IN}. This carries V_{IN} from the minimum voltage to the peak voltage and back to minimum in less than 5ms. Transistor Q_5 switches the full load current in for the rising portion of the ramp, and then out for the falling portion. Thus, this cycle subjects the DUT for the full range combination of V_{IN} and I_L for a given V_{OUT} during one 50ms cycle.

The results are displayed V_M vs. V_{IN} on an XY scope readout as shown in Figure 74. The slope of the curve indicates how much V_M varies with V_{IN}. The change in I_L halfway through the triangular wave will cause the return trace to be higher than the rising V_{IN} trace. This vertical difference indicates the degree of change in V_M with the change in loading at any input voltage. Therefore, the display gives an at-a-glance visual indication of the DUT's regulating ability.

This cycle can be repeated for all prescribed V_{OUT} levels, the $V_{OUT(SET)}$ input being used to set the V_{OUT} levels as in Figure 72. As far as the equipment is concerned, one cycle per each $V_{OUT(SET)}$ is all that is needed. However, a human observer will need enough cycles so that he can read the scope. Therefore, it might take a minute to step through the three V_{OUT} levels indicated for the 723 in Table 6. By using marks on the CRT screen to indicate acceptable performance, this test could be given to a technician to perform on a production basis.

The quiescent current can be measured at the peak V_{IN} point when V_{OUT} is at its mid-range value. The short circuit current can be measured by putting the three-pole, double-throw switch S6 at its No. 2 position and measuring V_{SC} across the current limiting resistor.

The user will have to add his own ripple test signal and measurement to this circuit. Typically ac measurements are not part of high speed auto-

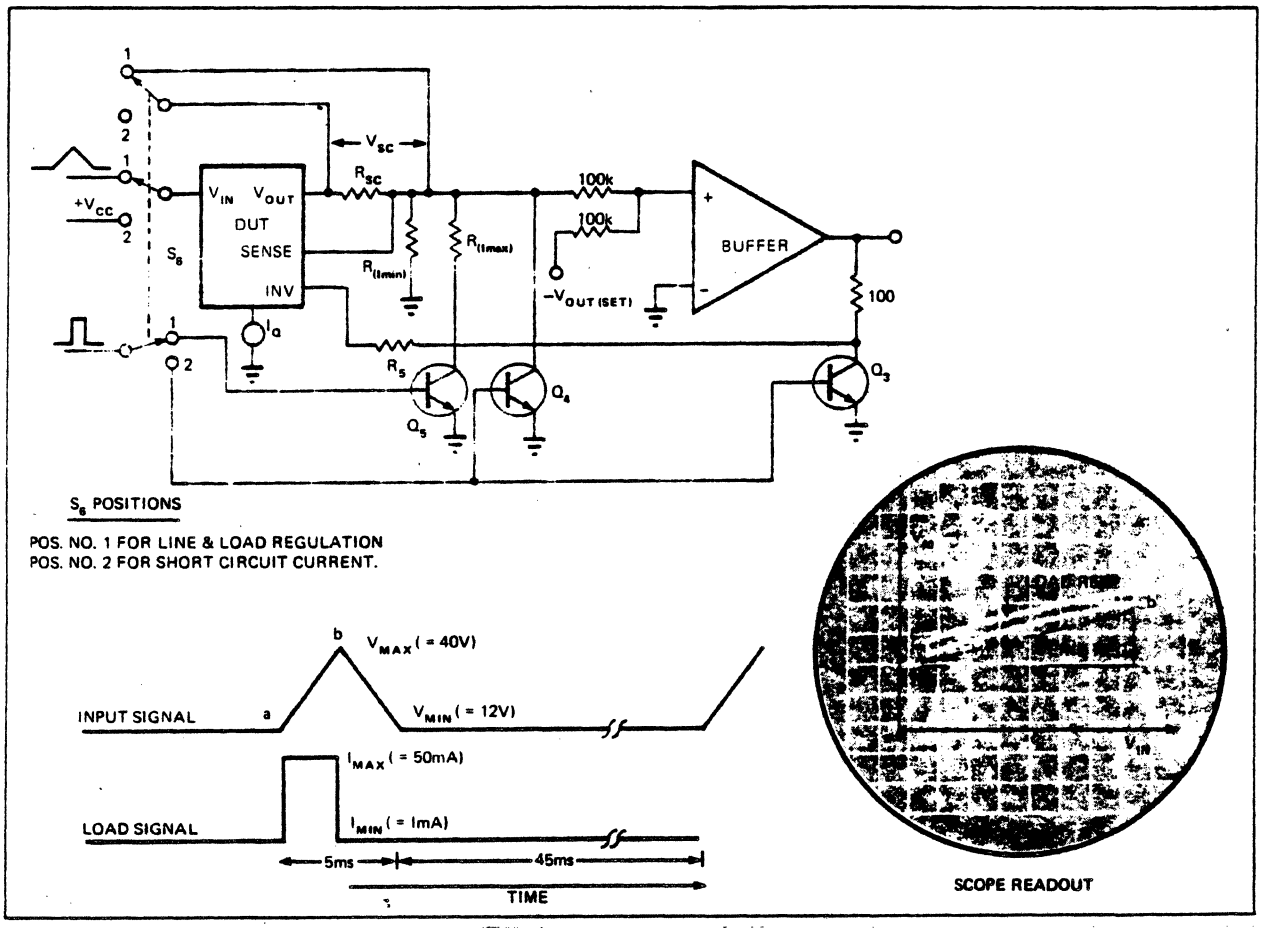


Figure 74: Automated bench tester version of Figure 72 simulates the type of testing done at high speed by automatic test equipment at the IC supplier's factory. The triangular ramp on the input voltage sweeps the DUT (device under test) across its line-regulation specifications while the load is switched, to check the load regulation specifications. This displays the V_{OUT} vs. V_{IN} transfer function on a scope. The input excitations are then switched to Position 2 to check the DUT's short circuit behavior.

matic tests, because the speed of the line regulation test is such that its dynamics are fast enough to correlate to the ripple rejection test. If the DUT hasn't the bandwidth to keep up with the 200Hz test cycling rate, this deficiency will show up in the test results.

One testing problem that the circuit of Figure 74 will help the user appreciate is the way the supplier's high speed tests must necessarily slight the DUT's temperature rise characteristics. Though the test sweeps the DUT over a full range of loadings, the actual time under load is so brief that the tests are performed at essentially constant chip temperature.

The I_Q measurement does indicate how much the regulator will heat itself in operation, above and beyond what it dissipates in dropping voltage through its pass transistor. But there is no indication of how the performance parameters will vary with heating. The user must put these circuits in temperature chambers to find this out.

4.333 Voltage Regulator Test Hints

As mentioned several times already, power regulators are tested under pulse conditions. The chip is not allowed to heat to its normal junction temperature at rated current. Thus with a 2mV/°C change in reference, and 0 to 90°C temperature rise depending on loading, the IC voltage regulator is more dramatically affected than op amps with temperature variation. In actual practice, the voltage regulator is operational under steady state current conditions and the chip heats up. Thus the voltage regulator specifications listed at 25°C do not apply at actual operating temperature and load conditions.

4.34 Linear IC Summary

In summation, linear ICs are subject to static discharge damage due to use of high frequency bipolar transistors or MOS input transistors. The primary failure modes of linear ICs are degraded inputs, open outputs and zero power drain.

Furthermore, all tests should be performed at temperature extremes and IC voltage regulator pulse tests must be somehow correlated to the actual applications usage - load current and chip temperature.

4.4 MOS ICs

MOS (metal-oxide semiconductor) technology gets its name from the basic MOS structure of a metal electrode over an oxide dielectric over a semiconductor substrate. The transistors of an MOS IC are field-effect transistors (FETs), which are also used as resistors because the MOSFET is a high impedance device. Most MOS monolithic ICs are digital circuits built entirely of MOSFETs.

One of the most exciting features of the MOS transistor is its simplicity. An electric field, applied through the oxide insulated gate electrode, is used to control the conductance of a channel layer in semiconductor material under the gate. The channel is a lightly doped region between two

highly doped areas called the source and the drain. Compared with monolithic bipolar ICs, MOS ICs hay be characterized by slower operation and lower output power. As with many different technologies, there are application areas in which the MOS structure clearly excels and others in which it does not compare favorably.

The MOS transistor is an almost ideal switch since when the gate and source potentials are equal, no current flows between the source and the drain. However, when the gate voltage with respect to the source is raised to a critical level (called threshold voltage), the transistor turns ON and current can flow from source to drain. The threshold voltage is negative on the gate of this type of MOS transistor to establish an electrostatic field that inverts the n material under the gate to a p-channel between the source and drain.

Figure 75 depicts a typical PMOS structure. The MOS transistor is a self-isolating device, because all junctions are reverse biased during normal operation. This is extremely desirable when making ICs. Since isolation diffusions are not needed, the packing density of the transistors on a chip is extremely high.

With many MOS transistors on a chip, however, a parasitic problem can arise. The key to avoiding the problem is in the manufacturing process. A parasitic transistor is formed between two adjacent p+ regions when a high voltage metal line crosses them. Unless the "field" oxide under this line is thick enough, the high voltage inverts the surface of the n-type substrate and turns ON the transistor that is formed. This parasitic transistor is exactly like a conventional transistor except it has thicker gate oxide and, therefore, a higher threshold voltage.

The manufacturing process must provide a field oxide thick enough to place the thresholds of the parasitic transistors above the maximum voltages in the circuit. Since these voltages are often greater than -30V, the field oxide must be at least 1.5μ thick. This oxide can be thermally grown, but it takes a long time. More often, the thick oxide is deposited. Methods of deposition include electron-beam evaporation, r-f sputtering, and the thermal oxidation of silane. The last method is the most common because it is the cleanest and most reproducible.

A problem incurred with MOS structures is the limitation in gate voltage due to the relatively thick oxide utilized in these devices. Since the charge necessary for destruction is only 10^{9}C, it is necessary to protect each external lead with a breakdown device such as a zener diode. This breakdown device must be included in the mask design for MOS structures.

MOS technology consists of three basic processes: p-channel, n-channel, and CMOS. All are made predominantly with silicon or aluminum gate methods, but they can also be built with ion implantation or silicon-on-sapphire techniques.

With PMOS, the source and drain are doped p-type regions on the silicon substrate, and the channel created between these regions consists of holes rather than electrons; with NMOS, the opposite occurs and the channel is

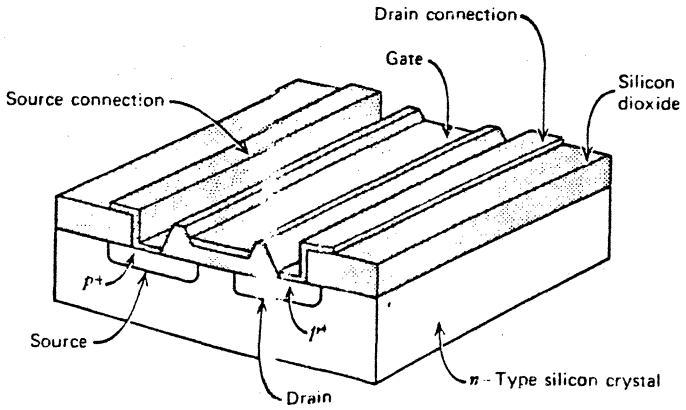


Figure 75: The PMOS structure. This device shows the conventional metal-oxide semiconductor gate sandwich that gives the technology its name. Also apparent are the overlaps between gate and source, and between gate and drain. This overlap increases parasitic capacitance and limits the speed of devices with this structure.

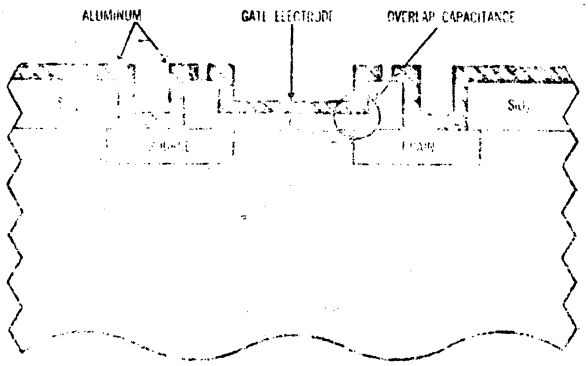


Figure 76: Gate electrode overlap in the source and drain regions of this typical MOS transistor produces parasitic capacitance that slows the device. In the silicon gate process overlap is greatly reduced.

made of electrons. Since electrons move more easily through silicon crystals than holes, n-channel transistors are faster than p-channel transistors. This can also be expressed as n-channel transistors having greater gain than p-channel devices of similar size. MOS transistor gain is boosted by broadening channel width, so for equivalent gains or speed, n-channel transistors are smaller than p-channel, permitting greater packing density.

With n-channel, higher substrate doping levels are practical allowing transistors to be placed closer together, further increasing the packing density. But the n-channel manufacturing process very lightly dopes silicon surfaces, resulting in increased leakage currents. Unless processing is carefully controlled, a wide variation in leakage occurs, both initially and with time. Dynamic circuits are much more sensitive to leakage current than are static circuits since periodic refreshing without memory loss depends on a tight distribution of leakage rates.

The CMOS approach combines both n- and p-channel transistors on the same chip by diffusing or implanting isolated doped substrate regions for the n-channel transistors. Since most CMOS diffused interconnections are similar to conventional p-channel circuits, SMOS has less exposure to leakage-current variation than straight n-channel.

For CMOS circuits an extra diffusion is required for the n-channel substrates, as well as additional source and drain diffusions CMOS is more expensive to manufacture than either n- or p- channel. Furthermore this special substrate region takes up considerable space, giving CMOS a lower packing density than either n- or p- channel.

The primary advantage CMOS offers is a very low quiescent power requirement. Speed and transient power (the major element of power when dynamic circuits are operated at full repetition rate) are similar for CMOS and n-channel circuits operating from their normal supply voltages.

CMOS is finding increased potential in small and medium (256, 512 and 1024 bit) 100% logic compatible memory components presently served by TTL, as evidenced by the increased product offering in this area. At low power supply voltages, CMOS is faster than NMOS and cheaper than bipolar TTL.

All the MOS variations mentioned so far can be produced either with metal gates (aluminum) or silicon gates. In the metal gate process, the gate electrode is positioned after the source and drain regions have been formed. To work effectively, the gate electrode must overlap the source and drain regions (Figure 76). This overlap produces parasitic capacitance that slows circuit speed.

In the silicon gate process, source and drain regions are formed after the gate electrode has been positioned; the gate electrode defines the edge of the source and drain regions, reducing overlap. Silicon is used because aluminum cannot withstand the processing temperatures needed to produce the source and the drain. Silicon gate MOS has three distinct advantages: It produces high yields because the gate oxide is protected immediately after it is grown; it can operate at higher speeds due to smaller gate size and no overlap; and compatibility with other technologies.

Table 7

Major Characteristics of Basic MOS Process and Bipolar Logic Families

MOS Process	Threshold Voltage (V)	Supply Voltage $V_{DD}(V_{GG})$ (V)	Propagation Delay (nsec/gate)	Frequency (MHz)	Power Dissipation/ Gate (mW)[a]	Noise Margin	
						Logic "1"	Logic "0"
p-channel MOS							
High threshold { medium power	−3.5 to −5	−17 to −27	75	2	1.7	3	1.5
High threshold { low power			300	0.5	0.45		
Low threshold { (100)	−1.5 to −2.5	−12 to −17	70	2	1.0	2	0.7
Low threshold { silicon gate			60	5	1.0		
Ion implant, depletion loads	−1.5 to −5	−12 to −27	35	5	1.5	1.5	1
n-Channel MOS							
Metal gate	1–2	5–20		10	1.0	1	1
Silicon gate							
Complementary (CMOS)							
Metal gate	+1.5 to +2.5	3–18	40	20	50 nW	$V_{DD}/2.2$	
Silicon gate	±0.5 to ±2.5	1.2–15	25	25	50 nW		
Bipolar lines							
TTL		$5.0^{+20\%}_{-10\%}$	10	60	15[b]	1.2	1.2
ECL		$5.2^{+20\%}_{-10\%}$	1	400	25–35	0.4	0.4
DTL		5.0 ± 10%	30		8		
RTL		3.0 ± 10%	24		12		

[a] In milliwatts except as noted.

[b] The 54L/74L series has approximate power dissipation of ~1 mW/gate.

Silicon gates still use aluminum for low resistance interconnections. In more complicated memory cells, silicon and aluminum layers are used together to produce interconnections with high packing density. This combination makes the silicon gate more expensive to manufacture than a standard aluminum gate.

Table 7 compares some of the primary characteristics of MOS and bipolar logic families.

4.41 PMOS Devices

The most common device, the p-type enhancement mode, is built on a substrate of n-type silicon into which are diffused two p-regions: the source and the drain (Figure 77). The discussion to follow pertains to the p-type enhancement mode MOS IC. These are normally formed by diffusing two wells of p-type impurity (phosphorus) into the substrate, which in operation are connected by an induced p-region which is the channel.

The gate or control element covers the region between the source and the drain and is insulated from the semiconductor material by a layer of silicon oxide. The input resistance of the gate is extremely high - on the order of 10^{18} ohms - and the input impedance at high frequencies is almost purely capacitive. The gate is a layer of metal, usually aluminum, as are the contacts to the source and the drain. Normally, the oxide layer under the gate is made much thinner than the protective oxide on the rest of the chip in order to enhance the effect of the gate field on the conductance of the channel region.

If the gate, the source, and the substrate are grounded and a negative voltage is applied to the drain (Figure 77b), no current will flow between the source and drain because they are isolated from each other by the reverse biased drain-to-body p-n junction.

If a negative voltage is applied to the gate (Figure 77c), the surface of the n-type silicon inverts, becoming essentially p-type. The negative gate voltage attracts holes from the n-type substrate to the surface. Initially, the channel area very near the surface has an excess of electrons, because the material is n-type, but the holes drawn into the area by the gate field neutralize these electrons. At some gate voltage, the attracted holes just compensate for these electrons and the channel behaves like the intrinsic semiconductor. At higher gate voltages, the holes predominate and the channel area, less than 1μ deep, is referred to as "inverted"; it now behaves like a p-type semiconductor, providing a current path from source to drain.

However, the surface region under the gate does not invert, and no conduction can occur until the gate voltage is more negative than the threshold voltage V_T which is about -5V for most p-channel enhancement mode devices. This effect results, in part, from the presence of impurity charge in the silicon, which must be neutralized before the channel region can invert. In general, the thinner the gate oxide, the lower the threshold voltage. Figure 78 depicts the turn-on characteristics of a typical MOSFET.

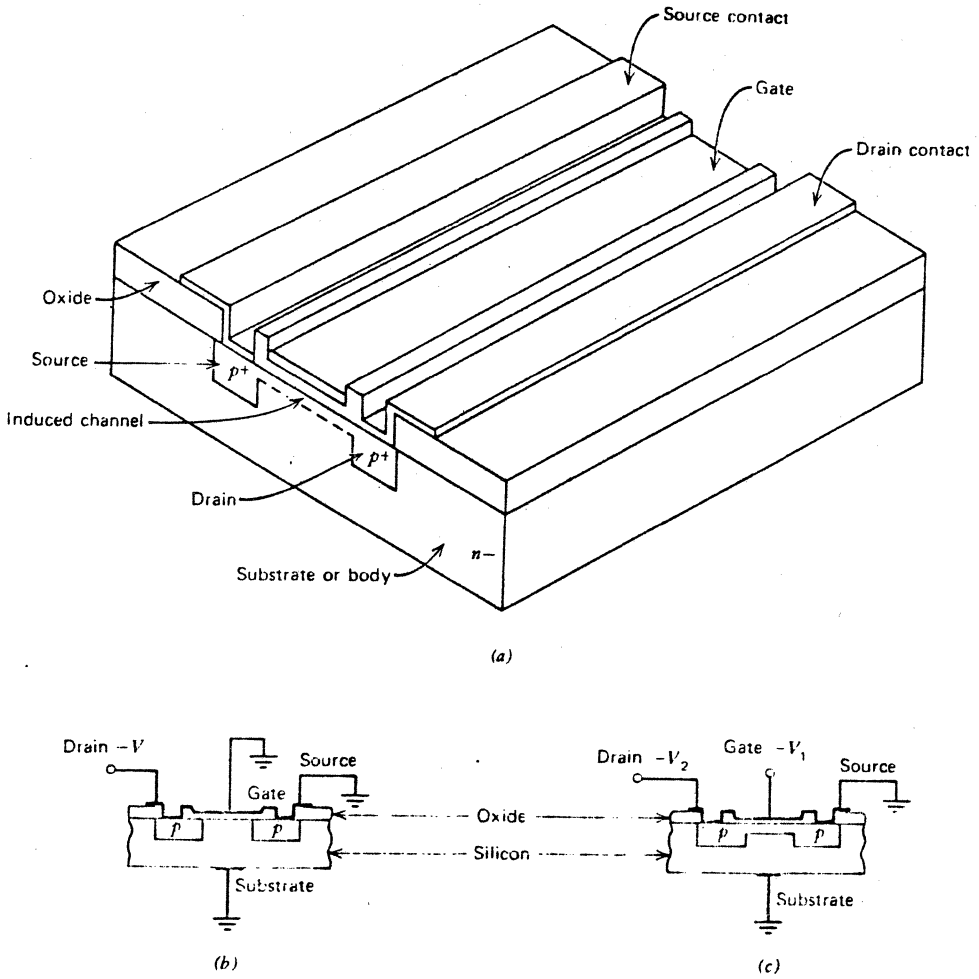


Figure 77: The PMOS device: (a) basic structure, (b) nonconducting state, (c) conducting state.

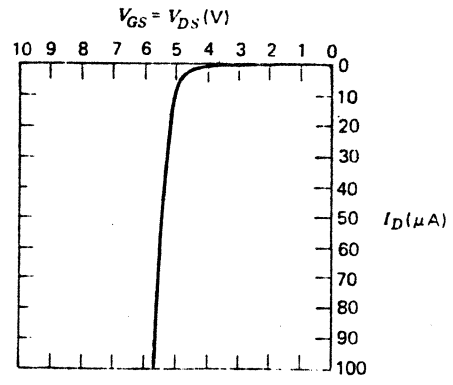


Figure 78: Turn-on characteristics of a typical MOSFET

As the gate voltage V_{GS} becomes more negative than the threshold V_T, the conducting channel is formed and its depth increases with increasingly negative gate voltage. For low drain current, the channel is an ohmic resistance and the current I_D is directly proportional to the drain-to-source voltage V_{DS}. As V_{DS} becomes more negative, however, the channel saturates and the current levels off (Figure 79).

The saturation phenomenon is easily understood. Assume that the device is operated with the source grounded and the gate at -12V. If the drain voltage is 0V, no current flows, even though a channel exists. As the drain voltage is made negative, current flows from the source to the drain through the resistance channel (Figure 80). The voltage difference between the gate and the body of the device is -12V at the left and decreases long the length of the channel (because of the resistive voltage drop) to a minimum of $-12-(V_{DS})$V at the drain. This voltage difference determines the extent to which a channel is formed in the substrate material.

If the negative voltage $-V_{DS}$ increases enough, the gate-to-body voltage at the drain $-12-(-V_{DS})$ approaches the threshold voltage V_T and the voltage near the drain is just sufficient to form a channel at that point. If V_{DS} is made still more negative, the inversion channel terminates short of the drain; the drain current is limited and becomes independent of further changes in V_{DS}. If a voltage is applied to the drain when the device is OFF (i.e., when $[V_{GS}] < [V_T]$), ideally no current flows. There will, however, be the small drain-to-body current, which varies with junction area as well as with the bulk resistivity of the material. For junctions of the size normally encountered in discrete MOSFETs, this current is in the nanoampere range; for the smaller junctions normally used in MOS ICs, it may be as low as a few picoamperes.

4.42 The NMOS Structure

A typical NMOS structure is shown in Figure 81. ICs made with n-channel transistors offer advantages over the p-channel devices. The most obvious advantage stems from the higher mobility of the charge carriers in an n-channel device.

P-channel transistors use holes for conduction. At normal field intensities, hole mobility is about $200cm^2$/V-sec. On the other hand, n-channel transistors use electrons to accomplish the charge conduction. Since electron mobility is $400cm^2$/v-sec, twice that of hole mobility, an n-channel device will have one-half the ON resistance or impedance of an equivalent p-channel device with the same geometry and under the same operating conditions. Thus, n-channel transistors need be only half the size of p-channel devices to achieve the same impedance. Therefore, n-channel ICs can be smaller for the same complexity or, even more important, they can be more complex with no increase in silicon area.

Along with greater packing density, n-channel circuits offer a speed advantage over p-channel circuits. This is a direct result of smaller junction areas, since the operating speed of an MOS IC is largely limited

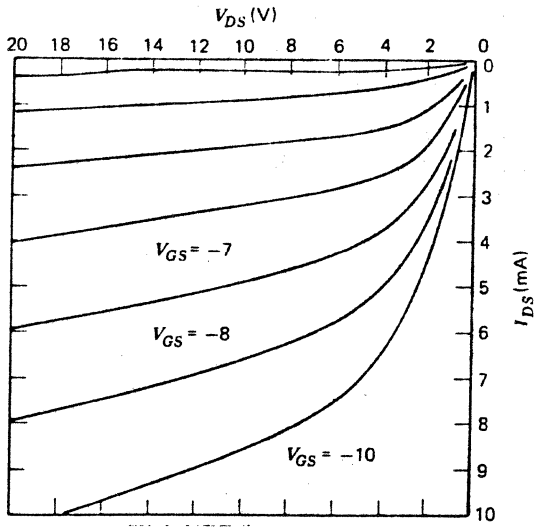


Figure 79: Drain characteristics of a typical MOSFET

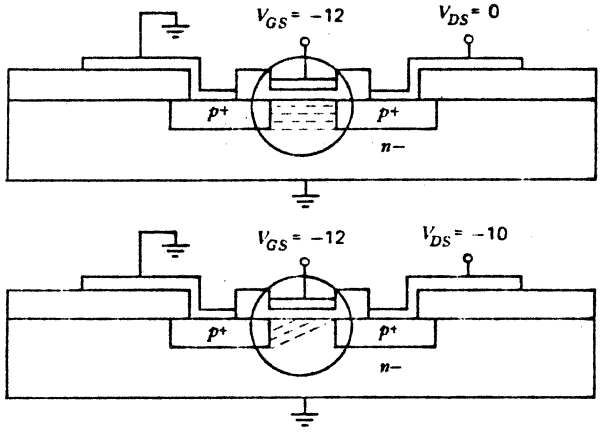


Figure 80: The saturation phenomenon: drain-to-source voltage effects are limited by channel pinchoff.

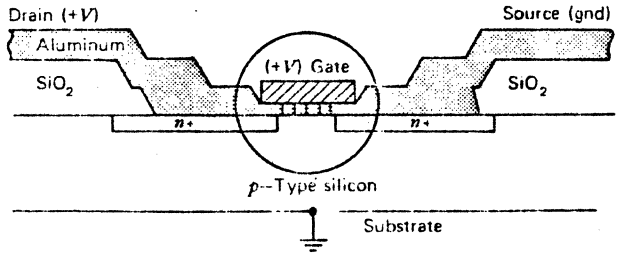


Figure 81: A typical NMOS structure.

by internal RC time constants. A diode's capacitance is directly proportional to its size and n-channel junctions can be smaller than p-channel junctions.

However, most of the mobile contaminants (the dread of MOS processing people) are positively charged. Since n-channel transistors operate with the gate positively biased with respect to the substrate, these ions collect along the oxide-silicon interface. The charge (Q_{po}) from this layer of ions causes a shift in threshold voltage which tends to make the transistor normally ON (current flows from source to drain with no voltage on the gate).

Beside the mobile positive ions, a fixed positive charge also exists at the oxide-silicon interface. This charge called Q_{SS} results from various steps in the manufacturing process and also tends to make the device normally ON. These two charges (Q_{po} and Q_{ss}) exist in p-channel devices, too, but the positive ions are pulled to the aluminum-oxide interface by the negative gate bias. There, they cannot affect the device threshold. In addition, the fixed charge in a p-channel device gives higher thresholds. Although this is undersirable, it is not as severe a condition as having the device permanently biased ON.

For an n-channel device, the oxidation of the silicon takes place at the silicon-silicon dioxide interface. No real abrupt change occurs between silicon and silicon dioxide; rather, there is a transition zone. This transition zone contains positively charged silicon atoms which increase the absolute magnitude of the threshold voltage for a p-channel device and decrease the absolute magnitude of the threshold voltage for an n-channel device. The result is that it is difficult to make an n-channel device that is OFF at zero gate voltage. This is why it is more difficult to make an n-channel device than a p-channel device.

Most n-channel devices have moderate doping levels and are, in fact, normally ON devices. When used, the circuit designer provides a negative bias to the source to turn the device OFF. The PMOS ICs are not TTL compatible; the NMOS ICs are TTL compatible. All in all, this presents a fairly complicated picture. In the past it was difficult to design circuits using n-channel (an extra bias supply is needed for one thing), and it was difficult to control the process required to manufacture them. Today, however, n-channel devices overtaken p-channel as the standard MOS technology devices.

4.43 Threshold Voltage

The threshold voltage of an MOS transistor is the most important process and temperature dependent device parameter. For example, increasing the applied substrate-to-source voltage, decreases the rate of charge of threshold voltage with temperature. It is desirable in most cases to have a process that produces low threshold voltages. An IC with low threshold transistors will operate at lower power supply voltages than a high threshold circuit (-5 and -15V for the low voltage circuits vs. -13 and -27V for the high voltage circuits). This means lower cost power supplies and lower systems cost.

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An even more desirable feature is that the low voltage circuit is directly compatible with bipolar ICs; that is, it requires and produces the same input and output signal swings. This compatibility gives a system designer more flexibility. He can design using both MOS and bipolar circuits without worrying about signal level shifting or interfacing.

In addition, low signal voltages also imply higher operating frequencies. If a voltage only has to swing between 0 and -5V, it can change state faster than a voltage swinging between 0 and -10V.

The advantages of low voltage MOS are apparent; unfortunately, the best method of making it is not. There are several ways of modifying processes and device structures to achieve lowered threshold voltages.

Low threshold MOS circuits have three major advantages over the high threshold circuits. First, they simplify the task of establishing an interface between the MOS circuit and a bipolar circuit. Second, they substantially improve the MOS circuit's speed-power product. Finally, they facilitate generating bias and clock levels. To appreciate the actual importance of these three advantages, the high threshold circuit's shortcomings must be fully understood.

Because the low state transistor turns ON with only 2V on its gate (in some designs the voltage is even less) a simple interface between a driving bipolar circuit and a driven MOS circuit is possible. (The interface between a driving MOS circuit and a driven bipolar circuit, does not involve the MOS threshold and is equally simple with both kinds of MOS circuits.) This simplicity is attributable to the capacity of the MOS chip's input signal to have positive and negative levels quite close together - as close as 0 and 4V - and still have enough overdrive to nearly saturate the input MOS transistor. Normally, the substrate of either bipolar or MOS circuits is connected to system ground; the main supply voltage for DTL and TTL circuits is +5V; and the signal swing for the most common variety of p-channel MOS is between ground and a negative voltage; therefore, by biasing the MOS substrate to +5V, which is the bipolar supply voltage, the MOS input signal swing goes from 0 to -5V and from +5 to +1V. This transition makes the MOS input easy to generate with bipolar circuits.

With the low threshold circuits, the supply voltage can be as low as 5V for slow circuits that switch in a few microseconds and 10V for more typical speeds of 1μs or less. The lower voltages result in lower power dissipation and a speed power product lower than that obtainable with high threshold circuits. (In speed-power products, little numbers are better than big numbers, because speed in this context actually is the switching time in seconds rather than frequency in reciprocal seconds - the usual dimension of speed.)

In addition to the interface and speed-power advantage, the low threshold circuits require smaller bias (half the power supply requirements of high threshold process) and clock levels. Low threshold MOS circuits, however, have some disadvantages, including a lower field inversion threshold, slow speeds, and low noise immunity.

In general, silicon bipolar transistors are capable of operating at much higher frequencies when compared to conventional silicon MOSFETs. One of the major reasons for the relatively slow speed of the MOSFET is the presence of an appreciable gate-to-drain capacitance. For an enhancement type device, since there is no initial channel present with zero gate-to-source voltage, the gate electrode must be required to extend completely over the gap region between the drain and source so that a conducting channel can be formed between the two regions when the appropriate polarity gate voltage is applied. The gate electrode is usually designed to overlap both the drain and source electrodes so that any slight misalignment in the positioning of the gate electrode during the fabrication process will not result in a device failure. Thus, because of the overlap of the gate and drain and the gate and source electrodes and because of the thin insulating layer that separates them, appreciable values of parasitic gate-to-drain and gate-to-source capacitances will be observed in conventional MOSFET structures.

In particular, since the output of a MOS amplifier (or inverter) stage is taken from the drain electrode while the input is applied to the gate electrode, the gate-to-drain capacitance can be considered as a feedback capacitor from the output back to the input. Since the output is 180° out of phase with respect to the input signal because of the inversion in the amplifier, the feedback signal through the gate-to-drain capacitance is negative feedback. As the frequency of operation is increased, the effect of the negative feedback capacitance also increases and the observed gain begins to decrease rapidly.

Another very important consideration in any comparison of the relative speeds of bipolar and MOS devices is the difference in typical values of transconductance per unit area between the two types of structures. Because the transconductance per unit area of a silicon MOSFET fabricated through the use of conventional processing techniques is typically less than that of a silicon bipolar transistor operating at a comparable current level, the time required by the MOSFET to either charge or discharge a given capacitive load will be greater than the time required by the bipolar transistor.

The gate input impedance of a MOSFET is, for all practical purposes, purely capacitive, and this capacitance must be charged or discharged to change the state of the device. Therefore, in integrated circuit applications where the gate input capacitance associated with a particular stage must be charged and discharged by the previous stage, the longer times required by MOS devices for charging and discharging will result in slower circuit speeds.

The ratio of the transconductance to the gate input capacitance of a MOSFET can be used as a figure of merit for the speed of the device or for the relative speed of integrated circuits employing interconnected combinations of similar devices. The g_m/C_{IN} ratio can be increased by the following:

- Driving the MOSFET harder by applying higher values of gate-to-source voltage.
- Increasing the mobility of the carriers in the inversion layer.
- Decreasing the drain-to-source spacing.
- Decreasing the gate input capacitance by decreasing the parasitic capacitances associated with the amount of overlap of the gate electrode over the drain and source regions.

The transconductance of a MOSFET can be increased by increasing the channel width of the device. However, the gate input capacitance will also increase proportionally and the g_m/C_{IN} ratio will remain unchanged. Similarly, the use of a material with a higher dielectric constant for the gate insulator or decreasing the thickness of the gate insulator will have no effect on this ratio since both the transconductance and the gate input capacitance will increase by the same factor. (When the effect of a constant value of stray capacitance is considered, however, a second-order increase in speed can result when these quantities are increased.)

4.44 MOS Handling Procedures

Insulated gate metal oxide semiconductor field effect transistors (MOS FETs), like bipolar high frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOS FET if a type with an unprotected gate is picked up and the static charge built in the handler's body capacitance is discharged through the device. Any static charge is not dissipated due to high input impedance. Charge builds up until the gate junction is destroyed.

With proper handling and applications procedures, however, MOS circuits are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOSFETs which do not include gate-protection diodes, can be handled safely if the following basic precautions are taken:

1. Devices should be inserted in conductive containers such as metal rails or conductive foam.

2. Persons handling devices should be grounded by metallic wristbands.

3. Tips of soldering irons should be grounded.

4. Devices should never be inserted into or removed from circuits with power on.

With MOS devices, the input voltage cannot be higher than the supply voltage. If allowed to happen, carriers are injected into the substrate, building up current flow and destroying the device.

4.45 MOS Logic Functions

Digital logic functions can be implemented by two general types of MOS circuits: (1) conventional dc or static logic that uses techniques similar to those employed in bipolar ICs, and (2) dynamic or ac logic that uses temporary memory and clocked load resistors.

The big difference between conventional static logic and dynamic logic is that the latter is a sampling type logic. That is, a dynamic circuit samples the state of the signal at its input periodically by means of a clock pulse and provides a corresponding output in the form of a stored charge on a capacitor, rather than as a continuous dc output voltage. The dynamic circuit, therefore, needs to draw drain current only during the sampling period, and that is how the very significant savings in power is achieved.

Dynamic logic is feasible with MOS because the input to an MOS transistor is almost purely capacitive. Thus, a logic circuit working into an MOS load needs only to provide a path for quickly charging or discharging the input capacitance of the load to establish a specific logic level.

4.451 dc or Static Logic

In static logic a relatively high impedance MOS device that needs very little area is substituted for a diffused load resistor (Figure 82), which requires much more area. This MOS load (or pull up) device is held in conduction at all times. There are two methods of accomplishing this result: one uses a single power supply applied to both the gate and the drain of the load device; the other uses two supplies with the more negative one tied to the gate. By using a second supply that is at least one gate threshold drop more negative than the drain supply V_{DD}, the drop across the load device becomes essentially zero when the inverter is OFF.

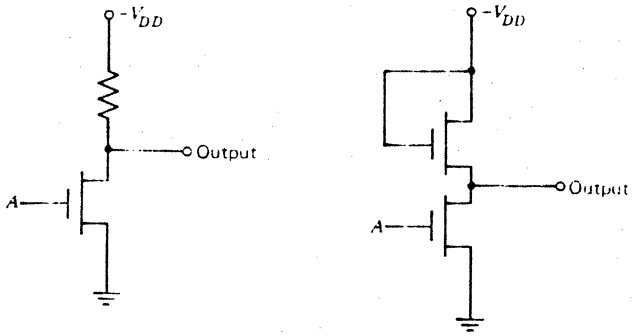


Figure 82: An example of static logic: the load resistor is replaced with another MOS device so that the circuit can be made entirely of MOS devices.

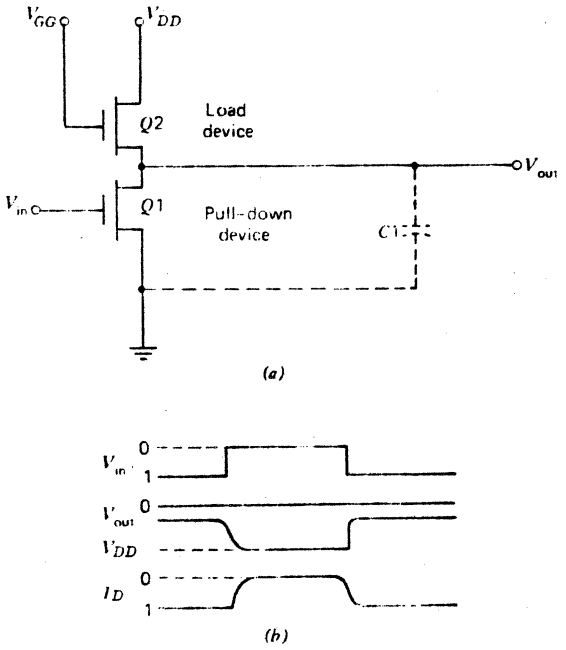


Figure 83: (a) Typical static MOS inverter circuit, (b) waveforms. The following conditions apply: (1) transistors are p-channel, (2) V_{GG} and V_{DD} are negative.

Figure 83 shows the conventional static MOS inverter. In this circuit, transistor Q_2 is biased ON and serves as a fixed resistance. Its value is many times that of the ON resistance of switched transistor Q_1 so that the output voltage can approach zero when Q_1 is turned on by V_{IN}. Because the inverter requires a high ratio between Q_2 and Q_1, it is called a ratio inverter.

When V_{IN} is at a logic "1", Q_1 is turned ON, causing current to flow from V_{DD} to ground. Due to the high resistance value of Q_2 compared with Q_1 in the ON condition, the voltage drop across Q_1 is very small, causing V_{OUT} to be virtually at ground. When V_{IN} goes to "0" Q_1 is cut off causing C_1 to charge to V_{DD}. Because R_{Q2} is high, the charge time for C_1 is relatively slow. When V_{IN} returns to a logic "1", C_1 discharges rather quickly through the low resistance of Q_1. The high resistance of Q_2 reduces current amplitude, but the substantial ON-time results in considerable power dissipation. Moreover, the long charge time for C_1 reduces circuit speed.

The load and pull down devices in an MOS inverter differ in size. The load device is designed to have an ON impedance about 20 times that of the pull down device. This ratio has been selected to assure that the output node goes to near ground when the inverter is conducting.

For all MOS devices, if some capacitance is required, the residual or parasitic capacitance that exists between the gates and the substrate or between the p-diffusions and the substrate is all that is needed.

4.452 ac or Dynamic Logic

Dynamic logic uses clocked load devices in conjunction with the inherent gate capacitance of the MOS device to give one simpler circuits and greatly reduced power consumption. Since power is consumed only when the clocks are ON, dynamic logic lets the designer trade off power consumption for speed of logic operations.

Dynamic logic has a characteristic that is similar to storing a charge on a capacitor; therefore, it has to run at a certain minimum frequency because the charge leaks off owing to the junction leakage. Therefore, the dynamic logic concept can be used only for circuits that operate above a minimum frequency of about 10kHz.

The MOS device is uniquely suited for this application because its gate looks like a perfect capacitor with virtually no leakage. This intrinsic gate capacitance serves as temporary storage in conjunction with two phase clocking to establish a built in delay in any gating structure. Unlike dc logic, in most cases there is no need to add extra devices to the intrinsic gate structure in order to provide delay. The function of the two phase clocking is to direct the flow of information from one gate to the next. One bit of delay (one clock period) occurs in the case where two adjacent logic gates are clocked with the same phase.

Figure 84 shows the dynamic inverter. Note that an additional transistor Q_3 is employed. This is a coupling transistor which gives the impression that dynamic logic is more expensive than static logic simply because it requires more components. This, however, is not the case, since the component count between static and dynamic logic quickly equalizes as circuit complexity increases beyond that of the basic gate.

With the dynamic inverter shown, performance does not necessarily depend on a high resistance ratio between Q_2 and Q_1. From the timing diagrams it is seen that signal transfer from the input to the output is accomplished only during the time that the phase 2 clock turns ON transistor Q_3. During phase 2, transistors Q_1 and Q_2 cannot be turned ON simultaneously, so that the resistance ratio between the two does not affect the output in any way. The operation of the dynamic inverter of Figure 84 is as follows: at t_0, V_{IN} goes to zero turning OFF Q_1. At the same time $\emptyset_1$ goes low, turning on Q_2 and causing C_1 to charge to V_{DD}. At t_1, $\emptyset_2$ turns ON Q_3 causing the charge on C_1 to be transferred to C_2. Because C_1 is made much larger than C_2, this charge transfer can occur without reducing the output voltage. At t_2, V_{IN} turns ON Q_1 and $\emptyset_1$ turns ON Q_2. This causes C_1 to discharge partially, but this discharge cannot be transmitted to C_2 because Q_3 is turned OFF. When $\emptyset_1$ turns OFF Q_2 at t_3, a partial charge still remains on C_1. This charge is discharged through Q_1 which is still turned ON by V_{IN}. Thus at t_4 when $\emptyset_2$ turns ON Q_3, C_2 also is permitted to discharge through Q_1 to ground.

During this cycle, drain current flows only at t_1 to charge up C_1 and from t_2 to t_3 the short amount of time during which both Q_1 and Q_2 are turned ON simultaneously.

The ac inverter structure combined with ac NOR and NAND gates (Figure 85), provides the basic guilding blocks required for logic design. A point to note is that a NOR gate clocked at Phase 1 time in series with an inverter clocked at Phase 2 time constitutes an OR gate with some delay. On the other hand, a NAND gate followed by an inverter and clocked the same way, gives a logic AND gate including the small delay. Essentially the input is clocked by Phase 1 through the first series-coupling device to the gate capacitance of the second inverter pull down device, where it is stored between clock pulses. Next, Phase 2 clocks the data through this inverter and stores them on the next gate until the subsequent Phase 1 time.

If no delay is desired, all the clocks can be returned to a common phase. In this case, all series devices between gates of a common phase can be omitted, since their main function is to isolate data until the alternate clock time. Thus, a gating structure with no delay would need no series devices.

To ensure the proper flow of data, the two clocks $\emptyset_1$ and $\emptyset_2$ should never be a logic "1" (V_{DD}) simultaneously. Also, the capacitive memory time constant must be greater than the time period between the trailing edges of $\emptyset_1$ and $\emptyset_2$, or vice versa, whichever is greatest, so that a logic "1" stored on the gate capacitor is not degraded by leakage to a voltage below the gate threshold level. High speed operation is limited by the ability to fully charge the gate capacitor to a logic "1" level during the clock ON time. This ratioless dynamic circuit draws a very small amount

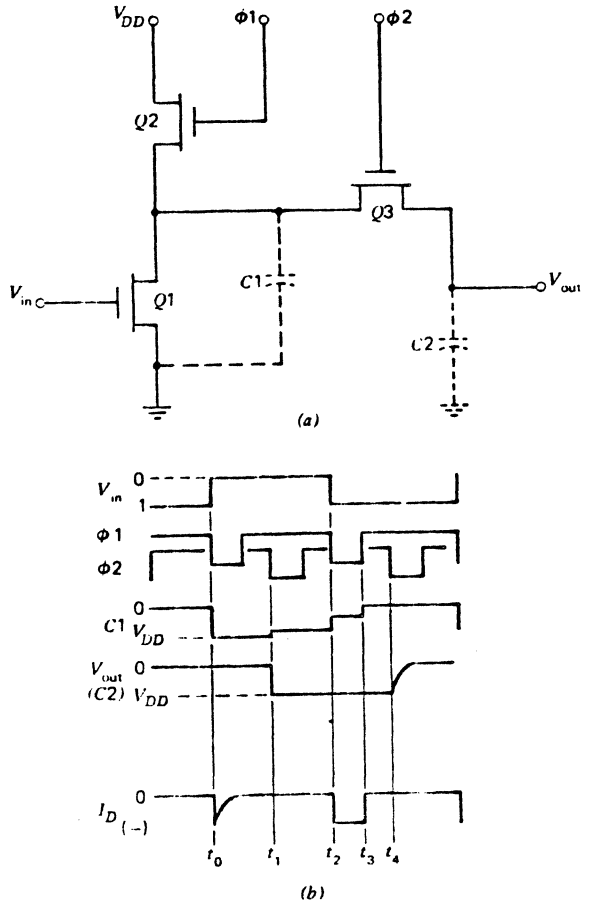


Figure 84: (a) Circuit for dynamic, two phase ratioless inverter, (b) waveforms.

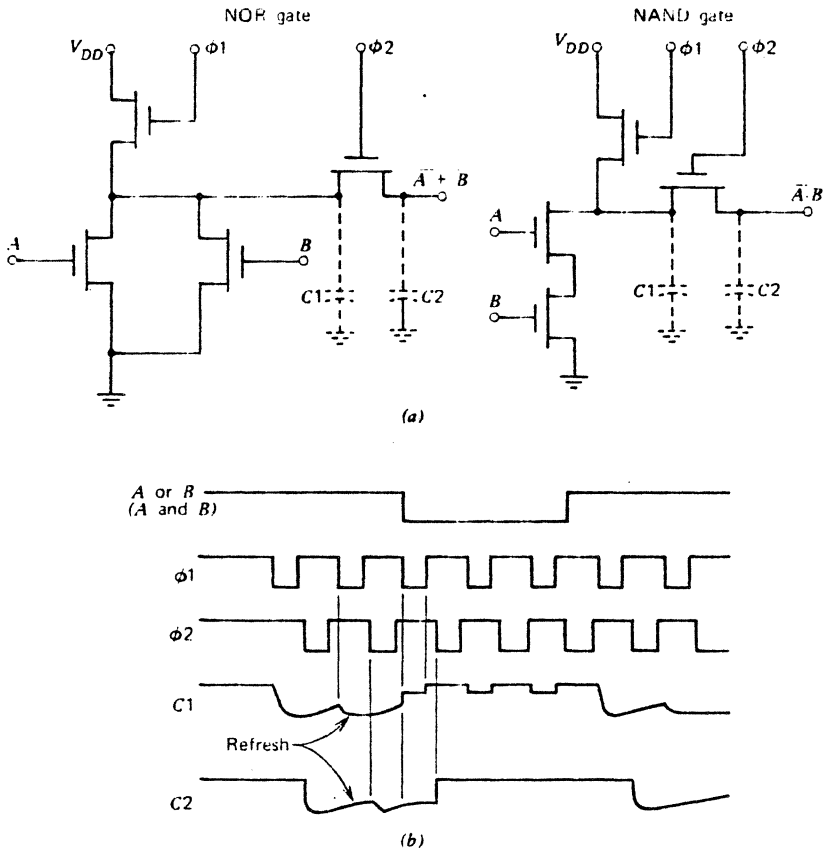


Figure 85: (a) Dynamic ratioless two phase gate circuits; (b) waveforms

of power compared with a static circuit. Nevertheless, during every second Phase 1 clock pulse, both the transistors cascaded across the power supply line are turned ON at the same time. This consumes dc power for the duration of the Phase 1 pulse.

The power saving attributes of dynamic logic are quite obvious. As a trade off, however, it demands at least two clock phases, which adds a considerable amount of complexity to circuit design. The clock pulses not only cause a sampling of the input signal, they also provide for "refreshing" the charge on the capacitors in the event that specific voltage levels must be maintained for more than a few milliseconds. Because of this, the clocks must run continuously to maintain proper operation, and the frequency and spacing of the pulses are critical. In addition to an upper frequency limit set by the high frequency capabilities of MOS circuitry, dynamic circuits have a minimum clock frequency limit in order to prevent loss of data due to excessive discharge of the capacitors as a result of leakage between clock pulses.

4.46 Shift Registers

Common to all data processing equipment is the ability to transfer digital data. The transfer of such data generally involves temporary storage combined with the ability to move the data by a prescribed number of bit positions.

A shift register holds N bits of data that can be entered, stored and sampled on command. In addition, the register can shift the data from one storage position to an adjacent position. For an N-bit shift register, N clock pulses are necessary for the data appearing at the input to be transferred to the output.

Shift registers can be static or dynamic. Either static or dynamic registers produce output logic levels within the standard MOS range. So the output can be tied to the input to recirculate data or shifted directly into another register or another logic circuit. The registers are readily interfaced with bipolar logic circuits, such as TTL. There are, however, several important differences between static and dynamic registers.

A static register is implemented with flip flops which are bistable devices. Therefore, when a bit is clocked into the register, it remains there until a second clock pulse shifts it into a succeeding flip flop, or out of the register. Once a static register is loaded, the clock can be stopped and the information will remain in the register, available for repeated retrieval until it is deliberately obliterated. The price paid for the nondestructive storage feature of static registers is more transistors per storage cell. Static cells are about 1.5 times as large as dynamic cells. Cost per bit and power dissipation are higher.

In a dynamic circuit, this is not the case. Since the bit information is stored in a capacitor, the circuit must be continually clocked in order to restore any charge that might leak off between inputs. This continuous succession of clock pulses causes each bit to ripple through the register and finally to disappear when it has reached the last stage of the register chain.

Nevertheless, the dynamic register can be used for data storage simply by feeding the output back to the input. When testing shift registers, they must be initialized or reset prior to beginning testing to obtain valid data on the output for effective measurement of a shift register performance.

4.47 CMOS Devices

Conventional MOS circuits are constructed with single polarity MOS devices, in most cases, p channel enhancement mode transistors. As discussed previously, these devices consist of a single crystal of n-type silicon which has p-type drain and source regions diffused into it. Complementary MOS (CMOS) on the other hand, combines devices of both polarities on the same chip. In this case, the basic building block is not one, but two MOS transistors - one n-channel (Figure 86) enhancement mode transistor and one p-channel enhancement mode transistor.

CMOS ICs are normally fabricated on an n-type substrate which serves as the substrate material for all p-channel MOS devices as well as p+ tunnels, diodes, and resistors. A p-type substrate is provided for the complementary n-channel MOS devices, n+ tunnels, diodes and resistors by diffusing a lightly doped p-well region into the original n-type substrate. The n-channel units exhibit the higher carrier mobility associated with electrons and they have approximately twice the transconductance of p-channel units with identical geometry. Therefore, the matching of a p-channel with an n-channel unit requires that a p-channel unit with a given channel length L have approximately twice the channel width W of the n-channel unit with which it is to be matched.

Protective guardbands surround separate MOS devices, tunnels, wells, and diodes or combinations of MOS devices that are interconnected through common diffused regions for the purpose of preventing leakage between the entities named. All p-channel devices, tunnels, and diodes must be surrounded by a continuous n+ guardband which also serves as a tunnel to help conduct current from the external supply voltage V_{DD} across the n-type substrate to every p-channel device tied to the external supply. Similar heavily doped p+ guardbands surround all n-channel devices, tunnels and diodes to help conduct current from the external ground supply V_{SS} across the p-well to every n-channel device tied to ground. Contact to the n-type substrate may be made through the n+ guardband and returned to the V_{DD} pad; contact to the p-well substrate may be made through the p+ guardband and returned to the ground pad.

Complementary MOS offers some unique advantages over single polarity devices. Probably the most notable of these is in the area of power dissipation. Because they have two transistors in series, complementary circuits consume very little quiescent power. In either logic state, one transistor or the other is OFF. This means that there is no dc path to ground in the circuit and the only power dissipated is due to the leakage through the OFF transistor. This feature makes CMOS particularly well suited for aerospace applications and in battery operated equipment. Additional advantages include low standby power, high noise immunity, TTL compatibility, a single power supply, wide operating voltage ranges,

insensitivity to temperature variation, moderate operating speed and ease of use. The advantage of CMOS come with a price tag attached. In this case, the penalties are larger chip size and thus lower packing density and higher cost.

The problem of packing density is fairly obvious. CMOS uses two transistors to do the job that one does in many p-channel circuits. For a relatively complex function, a CMOS chip is on the order of 25 to 30% larger than an equivalent p-channel chip. This reduced packing density also contributes to increased cost, since the price of any IC is directly related to the chip size. As chips get bigger, yields go down and costs go up.

The other factor that contributes to higher costs is processing complexity. A CMOS circuit goes through more steps because of the additional diffusion steps required. Each step in the manufacturing process adds its own increment to the total cost.

The most basic CMOS circuit, the inverter consists of one p-channel and one n-channel enhancement type MOS transistor, as schematized in Figure 87. In this figure the operation of a simple PMOS inverter is compared with an equivalent CMOS circuit. In the circuit of Figure 87a, transistor Q1 is switched while Q2 serves as a fixed load resistor. When the input signal turns Q1 ON, current flow from the power supply is instituted. The output voltage is determined by the ON resistance value of Q1 compared with the fixed resistance value of Q1 and can never go to zero.

In the complementary circuit (Figure 87b) when the input signal is low (ground), the n-channel transistor Q1 is OFF and the p-channel device is ON. The output, therefore is "shorted" to the positive supply voltage. If the load resistance is an MOS gate, which has a very high input resistance, virtually no current is drawn from the supply and the output voltage approaches $+V_{DD}$. When the input signal goes high, Q1 is turned ON and Q2 is turned OFF. Again, no dc current can flow from the supply, but the output is drawn to ground through the low ON resistance of Q1. The output voltage varies from almost $+V_{DD}$ to zero.

Here it is evident that the single channel circuit draws current from the power supply during the entire ON portion of the input signal. The CMOS circuit, on the other hand, draws no dc current at all. The only power dissipation occurs during the transitions of the input signal. In either logic state, one MOS transistor is ON while the other is OFF. Because one transistor is always turned OFF, the quiescent power consumption of the CMOS device is extremely low; more precisely, it is equal to the product of the supply voltage and the leakage current.

Because of the complementary nature of the interconnections of the series p- and n-type devices in the basic inverter, the transfer characteristic of a CMOS logic gate is as shown in Figure 88. The high input impedance of the gate causes the input and output signal to swing completely from zero volts (logic "0") to V_{DD} (logic "1") when sufficient settling time is allowed. The switching point is shown to be typically 45 to 50% of the magnitude of the power supply voltage, and it varies directly with

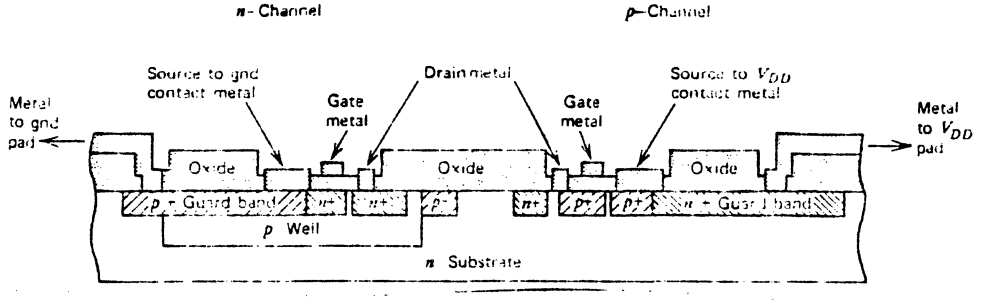


Figure 86: Cross-Sectional view of a complementary pair.

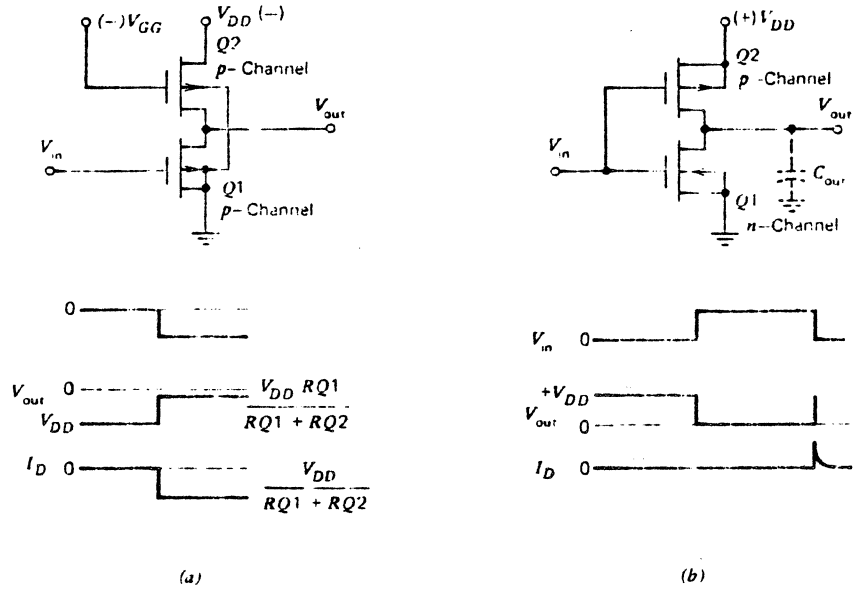


Figure 87: Comparison of inverter operations of (a) Single Channel MOS; and (b) CMOS

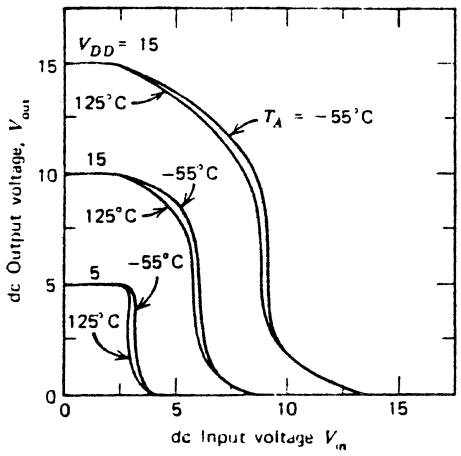


Figure 88: Transfer characteristic of a CMOS logic gate.

that voltage over the entire range from 6 to 15V for high threshold devices and 3 to 15V for low threshold devices. The CMOS transfer characteristic of Figure 88 illustrates the high noise immunity of MOS devices (i.e., typically 45% of the supply voltage). Figure 88 also reveals the negligible change in operating point as temperature varies from -55 to +125°C. Because of the ideal nature of these switching characteristics, CMOS devices operate reliably over a much wider range of voltage than other forms of logic circuits.

The exceptionally high ac and dc noise immunity of CMOS ICs is attributable to the relatively low output impedances (ca. 600 ohms), moderate speed operation, steep transfer characteristics, and output voltages within 10mV of V_{DD} when driving other CMOS circuits. The high values of noise immunity are achieved with power consumptions in the microwatt range as compared with much higher (milliwatt) consumptions and lower noise immunities (ca. 1V) for saturated bipolar logic. Because of their high cross-talk noise immunity, CMOS circuits are useful in applications requiring long lines or in circuits with closely coupled wiring. Moreover, CMOS circuits are not susceptible to ground line noise or to noise produced by improper ground returns; therefore, it is not necessary to use large ground planes. Similarly the high power supply noise immunity eliminates the need for complex filtering circuits.

An analysis of noise immunity involves consideration of immunity to both ac and dc noise. Whereas ac noise is usually considered to be made up of those noise spikes with pulse widths shorter than the propagation delay of a logic gate, dc noise spikes are considered to have pulse widths longer than the propagation delay of one gate. Since ac noise immunity, which varies in direct proportion to dc noise immunity, is largely a function of the propagation delays and output transition times of logic gates, it is a function of the input and output capacitances.

Because CMOS logic gates typically change state near 50% of the supply voltage, and because of the steep transfer characteristics exhibited during transitions, exceptionally high input voltages are required to significantly change or falsely switch the output logic state. Typically, then, the input to a CMOS logic gate operating at a dc supply voltage of 10V may change by 4.5V before the output begins to change state. In addition ac noise immunity is extremely high because of the high static or dc noise immunity and the moderate speed operation of standard CMOS circuits. The high ac noise immunity also implies high immunity to cross-talk noise.

Figures 89 and 90 illustrate CMOS logic gate noise immunity. These definitions assure that the logic level at the output of the driving device is recognized as the same logic level at the input to the load device. The dc noise level at the junction is equal to or less than the difference in maximum magnitudes of the output and input logic levels.

4.471 CMOS handling/Usage Precautions

Handling Precautions. Most CMOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have

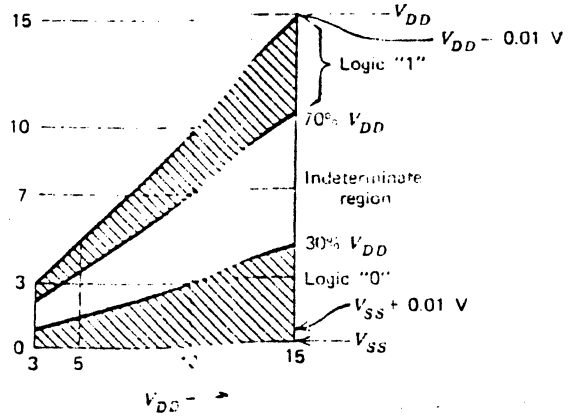


Figure 89: Guaranteed noise immunity values

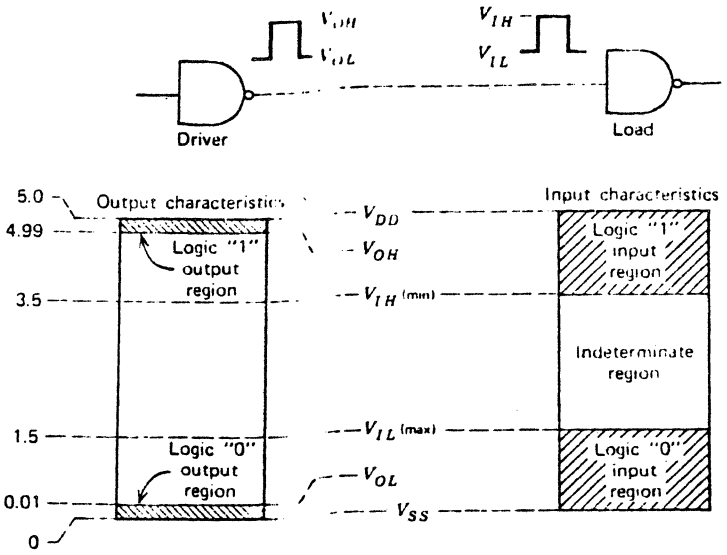


Figure 90: Output-to-input logic level characteristics

diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces fully protect CMOS devices from gate oxide failure (70 to 100V limit) for static discharge or signal voltage up to 1 to 2kV under most transient or low current conditions.

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

- Soldering-iron tips and test equipment should be grounded.
- Devices should be inserted in conductive containers such as metal rails.
- Persons handling devices should be grounded by metallic wristbands.

When automatic handling equipment is used, static electricity may not always be eliminated through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The device insulated part of the automatic handling mechanism (anvil transport) can generate very high levels of static electricity which are developed by the continuous flow of devices sliding over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical and inexpensive. Ionized air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

When the possibilities exist for appreciable static energy discharge, and proper handling techniques are not used, electrical damage can result as follows:

- shorted input protection diodes
- shorted or open gates
- opening in metal paths from the device input

Testing Precautions. In common with many electronic components, CMOS circuits should be operated and tested in circuits which have reasonable values of current limiting resistance or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure. A reasonable value of current limiting is 0.5 to 1.0A.

Usage Precautions. All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high current type, such as the 4009A, 4010A, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200mW to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed circuit boards that may temporarily become unterminated, should have a pull up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 0.2 to 1 megohm.

Signals shall not be applied to the inputs while the device power supply is OFF unless the input current is limited to a steady state value of less than 10mA.

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher output current CMOS types, such as the 4007A, 4009A and 4010A. In general, these types can all be safely shorted for supplies up to 5V, but will be damaged (depending on type) at higher power supply voltages. For cases in which a short circuit load, such as the base of a pnp or an npn bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 200mW.

4.472 CMOS Test Problems

The majority of CMOS devices available to date have been basically SSI and MSI functions with a few LSI functions. Some of the problems encountered with testing the 4000 series CMOS logic family are summarized by generic part number as shown in Table 8. One significant point should also be noted: certain suppliers of the 4000 family do not test all combinations of inputs and outputs or all on-chip functions that have external package connections. In addition for the 4043 quad 3-state R/S latch that same supplier specifies V_{OL} and V_{OH} tests limits for 4 different supply voltages (3, 5, 10 and 15V), but tests for only two (3 and 15V) at 25°C, one at high temperature and one at low temperature. He specifies quiescent device current for 5V and 10V, but tests only at 10V; and output drive current is not tested at temperature extremes. Only is the "diode test" tested for all inputs and outputs for this device, the other parameters are tested for one input gate and one output gate. Consequently, you during your incoming inspection testing may reject parts which were supposedly completely tested by the supplier. But in reality they were not. Thus as with any logic family and any supplier, it is important for you to find out just how the supplier is testing his product, the test conditions and limits he is using and the extent of his testing.

This is not to say that CMOS is not a good technology, Early in the product life of TTL, many problems existed, but now that the process is mature, TTL provides no unusual usage or testing problems. However, CMOS is just in its adolescence and as such, processes some growing pains. We are not trying to chastise CMOS but to present the picture as it is so that you can test the devices you are using properly and understand some of the reasons for your rejects.

TABLE 8

CMOS DEVICE TEST PROBLEMS

CD4030	Low V_{OH} and I_{DP} due to inability of product to amplify input levels enough to generate true output digital "1".
CD4025	High I_{DN} failure rate at Pin 10 due to marginal ground distribution at Pin-10 Not tested by supplier; note being added to data sheet to reflect this condition.
CD4044	High I_L (leakage current) failure rate. Mask defect Mask being redesigned
CD4000	Dual 3-input NOR gate plus inverter Supplier tests NOR gates, but no functional test on inverter Inverter portion does not meet data sheet electrical limits; note being added to supplier data sheet to reflect this condition.
CD4036	30% to 50% functional incoming test reject rate.
CD4061	Timing problems. Field temperature failure (device drops a bit)
CD4016	50% to 60% catastrophic failures at Incoming Inspection testing due to bad gate oxide.

4.48 MOS Memories

The user of random access memory devices, integrating them into a memory system demands a much greater degree of confidence that the part is good. Once that device becomes part of a system, it becomes very difficult or impossible to detect some failure mechanisms. Some systems contain faults that may go undetected for months before, by chance, a certain sequence of addressing or data causes a failure. Some users that could tolerate a 1% failure rate on MSI or SSI devices, now demand one to two orders of magnitude fewer failures of elements in a memory system. These users may turn to very thorough and time consuming test procedures to achieve high confidence levels. It is essential that the supplier provide the user with adequate test information to allow him to develop a thorough testing plan in incoming QC and evaluation functions.

The advantage of MOS technology lies in its usage in the fabrication of dense, low cost LSI devices - primarily memories. The primary areas of concern in the fabrication of memories are bit density, operating speed, power consumption, and reliability. The earliest memories, such as the 1103 1K RAM, were fabricated using PMOS technology; however, the use of NMOS technology provides several distinct advantages over p-channel MOS RAMs.

First the higher mobility provides an increased transconductance, g_m, and thus, faster speed performance. Second, lower voltage operation is possible, resulting in higher density packing. Third, the lower voltage operation provides the interface compatibility with low level logic that makes n-channel storage elements easier to use because of the simplified peripheral circuitry. Two significant additional advantages result from the n-channel developments: simplified refreshing and simplified timing.

Most of the speed limitations of present MOS memories can be eliminated by a combination of process and circuit improvements. One of the limitations of the circuits in use today is the time delay of cell address information propagating down an RC transmission line in which resistance results from interconnection tunnels. This limitation can be removed by the use of double-level metallization.

A second practical limitation of some cells is the need to read from the same data lines used to write, since the transient from a write cycle makes high speed reading difficult. This problem is eliminated by cell redesign in which the read line is separate from the write lines. With these two improvements, MOS memory cells are capable of very high speed performance, having a cycle time of less than 50ns.

Double-level metallization will not only improve performance, but also will permit the service lines to run on top of the storage cells rather than beside them, almost doubling the cell density. Combining this feature with smaller basic cells and with ever improving photolithographic capabilities, chips having 4096 and 16,384 bits are replacing the lower complexities in use today, reducing assembly and testing costs.

4.481 MOS RAMs

MOS random access memories may be either static or dynamic. Static RAM cells are flip flop type circuits which store data in either of two stable states. Most static MOS RAM cells use six transistors for each bit location (Figure 91). Dynamic RAMs use the absence or presence of charge on a capacitor to store information - typically with either one or three transistors per cell (Figure 92). However, since the capacitor that stores the charge has leakage, the stored information must be refreshed periodically (about every 2ms at 70°C).

Static logic cells are physically larger than dynamic cells. Although the static cell load and data bus transistors can be small, the two driving transistors must be big to accommodate large currents due to the principles of operation. In the typical configuration, the load transistors are constantly conducting current. When an input is applied to the driving transistors, an existing direct path to ground causes high power dissipation. Other configurations try to reduce power dissipation by clocking the load transistors or using node capacitances (marked 1 and 2 on Figure 91) to store charge.

Usually, dynamic RAMs require externally generated clock signals. Consequently, the components must provide additional pins for the clock inputs. Dynamic RAMs dissipate less power during access or refresh operations only.

RAM operation consists of a write data and read data cycle. The write operation sets an addressed memory cell to a "0" or "1" condition until another write operation occurs in that specific cell. Retrieving information from a memory consists of a cycle that accesses a specific address and reads its content via a buffered circuit to the data out pin of the RAM (Figure 93).

As mentioned in the section on bipolar RAMs, semiconductor IC RAMs are fabricated from a planar array of cells, each of which is uniquely accessed by the decoding of an address field consisting of x-column and Y-row components. Most 4k dynamic MOS RAMs decode the X and Y fields simultaneously. To provide a chip package with fewer pins, some suppliers have designed RAMs that use sequential multiplexing to share the address pins.

RAM operation requires signals for control as well as addressing. It needs an enable signal to precondition internal nodes of the memory array. It also uses that signal as an internal clock for the read/write pin to define whether the device should function in the read, write or read-modify-write mode at the specified address.

4.4811 Design Influences on Testability[1]

This section concerns itself with the test results that are obtained as a function of how various stages of the memory are designed.

Address Buffers. Problems of typical address buffers are those arising from the need to meet TTL compatibility specifications. Consider, however,

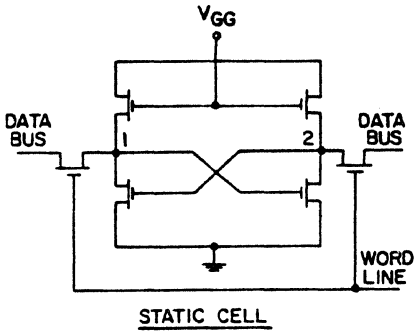


Figure 91: Static MOS memory cell contains 6 transistors that flip-flop. The number used depends on the bus requirements. This technique inherently reduces possible cell coupling.

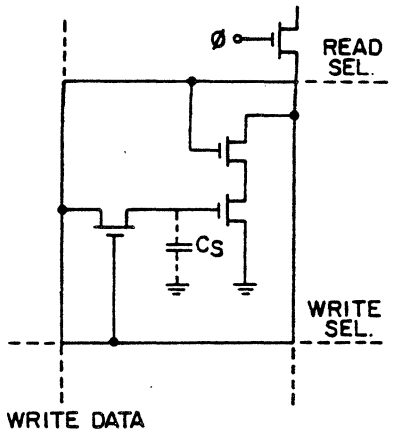


Figure 92: Dynamic MOS memory cell recharges parasitic circuit capacitances periodically. The cells are refreshed by rows and a refresh amplifier on each column recharges the columns.

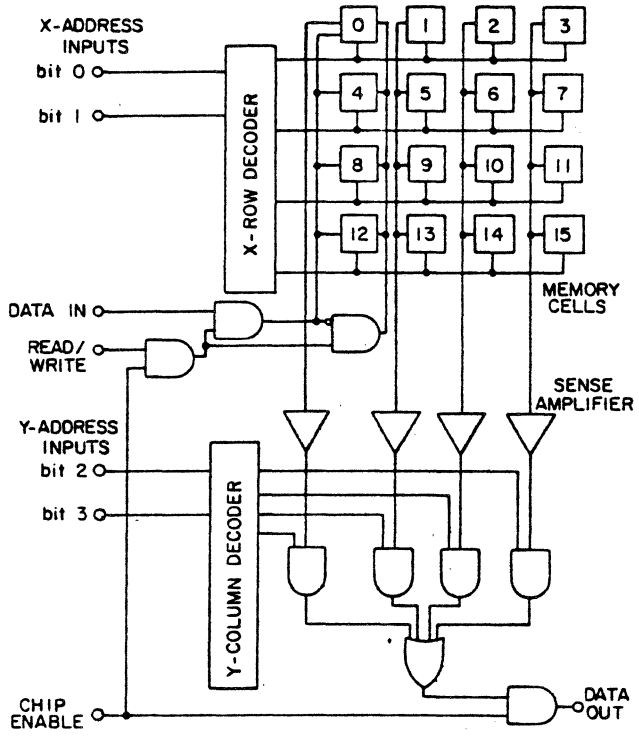


Figure 93: This simplified diagram shows the logic for a 16-bit RAM whose data output goes through a buffer circuit internally driven by a selected sense amplifier.

the logical and timing problems that can arise in the circuit of Figure 94 if the address buffers are less than ideal. A usual design approach is to sample the state of one buffer using an OR-gate to derive a clock Ø for strobing the decoder some set time after one or other address buffer output rises. The correct operation of the decoder will, therefore, suffer if variations in input level, address set-up time, or CE clock rise time can give a spurious glitch output on the low going output of a buffer, or worse still, variations in time delay through the buffer as a function of any of these variables. Such skew timing from buffer to buffer then shows up only as decoder pattern sensitivity.

It is quite common for a second clock signal to be fed to a group of address buffers to ensure a "don't care" state after the address hold time by shutting off power or steering the input. If such a common clock has an assymetrical load, it can have its level or timing dependent on all the address buffer states, and so address buffers in the group can interact: one memory design has its necessary V_{IL} determined in part by the level of V_{IH} and the number of buffers with a V_{IH} input due to such interaction. These interactions are especially troublesome because an automatic tester when plotting a V_{IH}/V_{IL} shmoo gives no indication of whether the problem is a cycle-to-cycle interaction in one buffer, or coupling from one buffer to another in the same cycle. It is therefore desirable to restrict all possible interactions through common clocks or levels by having as few as possible.

In one popular family of memories, the timing hazard of deriving the decoder-enabling clock from only one address buffer (whose time delay is grossly V_{IH} and V_{IL} sensitive) is alleviated by the logical arrangement shown in Figure 95. This is, however, only patching up the problem, since the testing strategy must now either assume the circuit is functioning as intended or else undertake the complex and tedious task of checking out the part for decoder pattern sensitivity with varying levels applied to different address inputs. There is no other way of ensuring that a "stuck zero" does not exist on the output of one or more NOR gates except by observing the address buffer outputs.

There is a clear trend towards using a dynamic sense flip-flop as an address buffer, strobed by a single clock. Such circuits fail in a "digital" way, giving in the limit the "wrong" output as input conditions or transistor parameters degrade. This is infinitely preferable, from the testability viewpoint, to earlier designs with address buffers whose output timing or levels suffered first.

Decoders

MOS dynamic RAM designs invariably use a dynamic NOR gate form of decoder in which only one (usually out of 64) precharged nodes is left undischarged to gate the decoder strobing clock through to the selected line. This basic circuit (Figure 96) leaves the unselected lines low, but only floating low. In a conventional memory design, extra circuitry is added to hold down unselected X lines. Without such provision, partial multiple selection can

[1]MOS Dynamic RAM - Design for Testability
R.C. Ross and R. Harland . 1976 IEEE Memory LSI Test Symposium

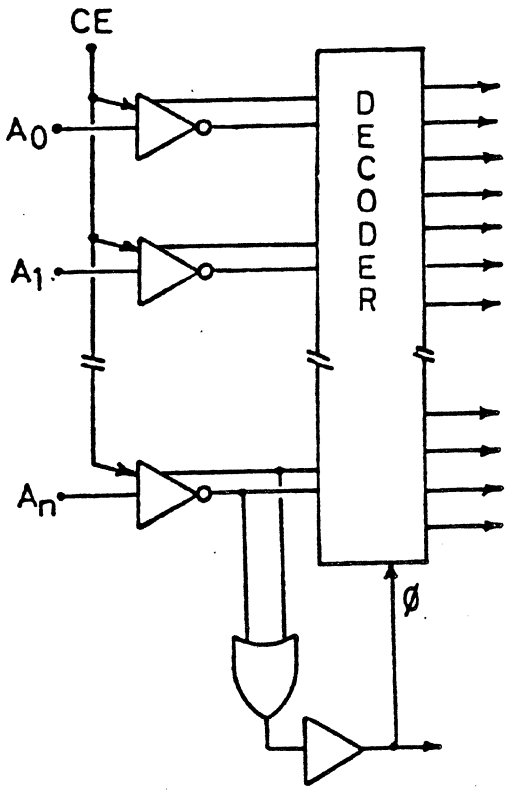


Figure 94: Decoder Clock Ø Derived from A_n or $\overline{A}_n = 1$

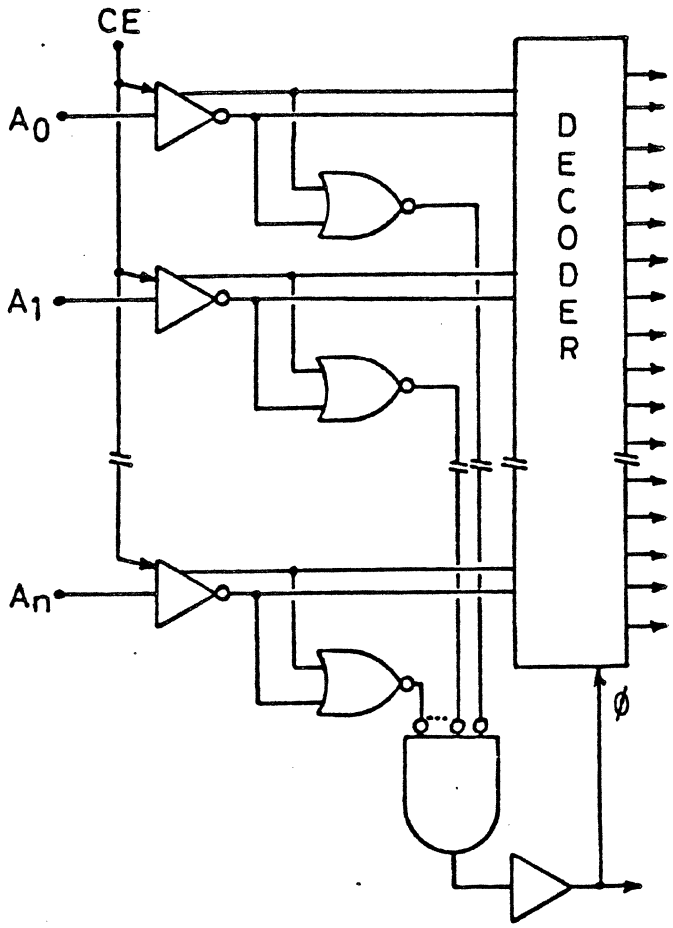


Figure 95: Decoder Clock Ø derived from $\Sigma_{A_i}^{n}$ or $A_i = 1$

occur as rising bit lines couple back into such floating X lines.

Less universal is any arrangement clamping bit lines to a fixed potential while the memory is quiescent. If no bit line clamps are provided, then a leaky bit line may simply fall to a level that forward biases all access transistors on that line, or less catastrophic, (but harder to test) for to a level that impairs sense amplifier sensitivity.

As already noted, almost every memory on the market uses an active hold-off for the X decoder. Virtually none takes the same precaution on the Y axis, despite the risk of multiple partial Y selection that can result from a self-bootstrapping action in the Y access transistor (Figure 97).

It is a common design oversight to neglect the back end of the cycle when considering timing race hazards. In most designs, the access to the cell is removed first by shutting off the selected X line. If this is achieved before any other function, then there will be no risk of damaging the cell contents as bit lines are precharged, etc. The most likely variable capable of causing a timing race in this respect, is clock fall time.

In normal operation the most likely race hazards at the beginning of a cycle are those which arise from the distributed RC time constants of lines other than metal runs. In particular, unless compensation circuits are used, polysilicon X lines can cause a race hazard between the selection of a cell and the initiation of sensing which worsens as distance from the X decoder increases. This is particularly unfortunate. A process control parameter, polysilicon sheet rho, turns up only as a pattern sensitivity problem.

Sensing

The effect that varying bit line levels may have on sense amplifier sensitivity has been noted. There are, however, many other designs for testability hazards in this area. Sense amplifier balance may be achieved using structures matching one sort of capacitance with another, e.g., gate capacitance/diffusion capacitance, may be dependent on a repeat pattern as staggered circuit layouts are used to solve a layout problem. Balance may be alignment sensitive. A common source of difficulty is in the provision of an effective mid-point reference to discriminate between stored "1" and stored "0" states. This reference, if derived in a simple circuit, may be very V_{DD} noise level sensitive. In more complex arrangements, the effective reference level may depend on other factors, such as CE clock rise time or even the data pattern on the last active cycle - a particularly unpleasant problem for testing.

Some recent designs of memory use the charge on a dummy cell as the reference and this charge is scaled geometrically rather than by setting the voltage to a mid-level. When used in conjunction with a bit line precharged to a high level, the power cycle time limitation of simple balanced sense amplifiers is avoided. As shown in Figure 98, there are then two possible conditions to consider in arriving at the new "1" level written back into the cell during a refresh operation. In Case 1, the bit line potential exceeds $V_{DD} - V_T$ at the end of the longest active cycle. In this condition,

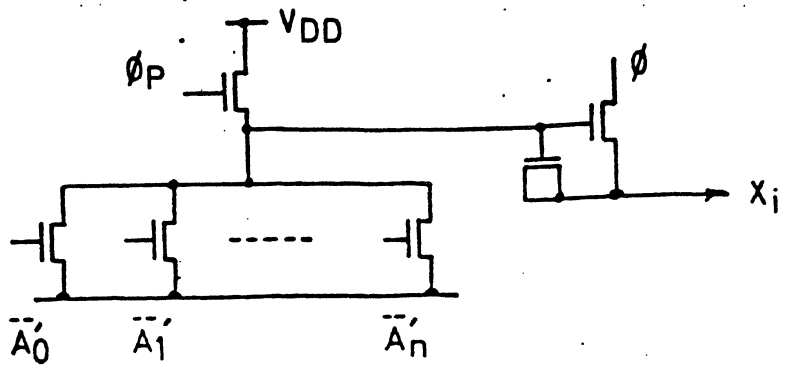


Figure 96: Basic Dynamic Noil Decoder

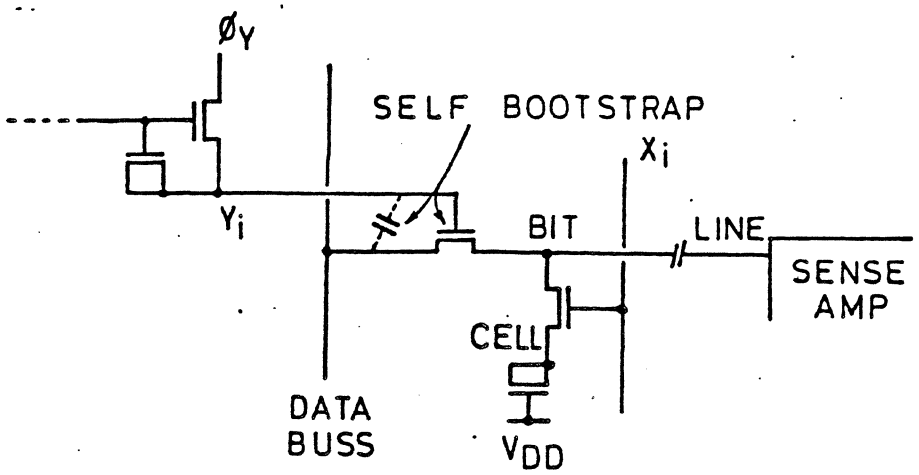


Figure 97: Risk of partial multiple Y access as data buss rises

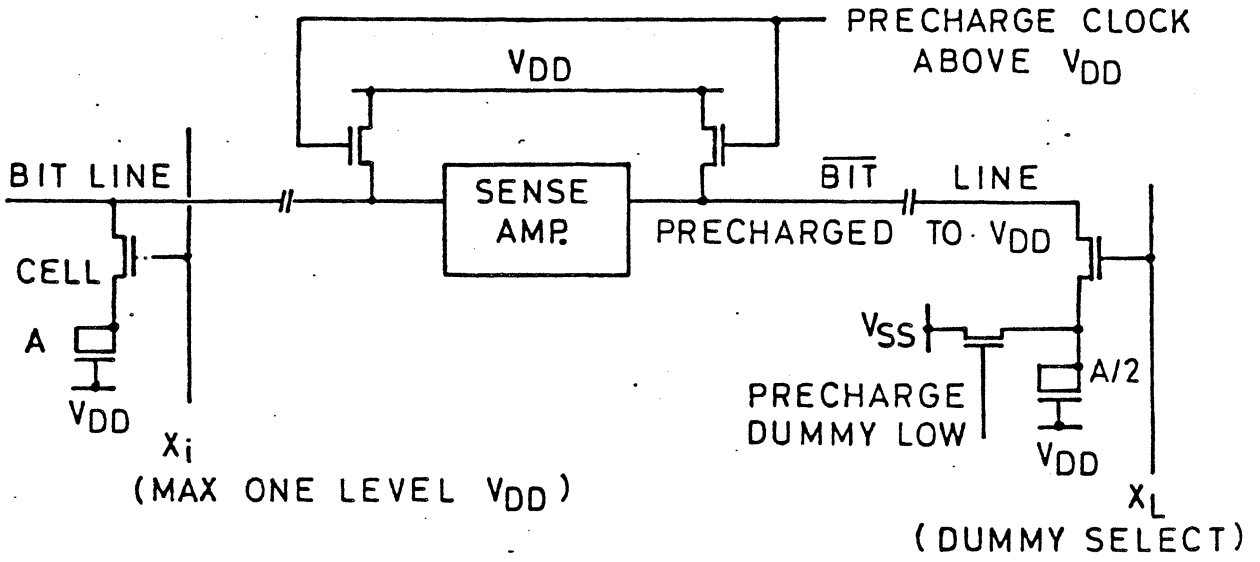


Figure 98: Precharged high bit line for non-destructive read-out of "ones"

the cell "1" level is limited by the X line potential to a maximum of $V_{DD} - V_T$. In Case 2, however, with the bit line lower than $V_{DD} - V_T$, one component of the new "1" level will be a fraction of the old "1" level, as determined by charge-sharing with the bit line. This is potentially risky because a poor "1" level can then "walk its way down" until failure occurs. Testing to prove this does not happen is costly since it involves repeated checking of patterns for "losing ones" with both maximum active cycle time (to allow maximum decay of the bit line level) and maximum refresh storage time (to allow maximum decay of the cell level).

Other Circuits

Fewer generalizations are possible with the remaining circuits. To ease test problems, it is desirable for every peripheral node to be reset to some standard level in between active cycles. This reduces the risk of performance in one cycle being dependent on the state written in or read out of the address pattern of the previous one. It is also desirable to ensure the Y access circuits are totally disabled by an invalid chip-select condition so as to ensure that refresh action is truly Y address independent.

In addition, the discussion in the section on bipolar memories entitled, "Test problems related to circuit design" apply to both MOS and Bipolar Memories alike.

4.4812 Test Considerations

"Dynamic RAMs" due to design optimization (speed and power), also utilize on chip "dynamic support" circuits. The combination of these circuits can provide unique problems since the "support circuits" inject noise and the "dynamic cells" are susceptible to noise. Due to the narrow margin separating the "stored charge" from the "injected noise" generated by the support circuits, testing for data retention (refresh) can be very critical. Furthermore, the level of "noise injection" is dependent mostly on clock input waveforms, making it the most critical problem in test equipment. Testing of both static and dynamic memories can be divided into three major categories:

1. Testing for speed of operation.
2. Testing for data retention.
3. DC Testing.

Performance Testing

AC testing is performed to guarantee all areas of operation specified on the data sheet. General timing is more critical in dynamic MOS RAMs. Each timing parameter requires extensive testing in order to verify correct circuit operation.

Access time and cycle time are the two major performance characteristics of the semiconductor RAM. Access time is defined as the time delay at specified thresholds, from the presentation of an enable or address input

pulse until the arrival of the memory data output. Cycle time, the time it takes to complete an operation, is the time required to access data (read), enter data (write), read and write, and update or modify the state of a memory location. The cycle times of dynamic MOS RAMs are longer than access times because of refresh requirements; static MOS and bipolar RAMs cycle times are about the same as their access time. Static RAMs are slower than Dynamic RAMs, although new process/design breakthroughs are providing approximately equal access time for both 4K Dynamic and Static MOS RAMs.

Testing for maximum performance of dynamic memories is conducted at the worst case point of the specification which is:

Min. Operating Voltage (V_{DD})

Max. Substrate Bias (V_{SX})

Min. Clock Amplitude

Min. Access and Cycle Time

Max. Rise and Fall Times

Min. Load Impedance

The above listed conditions are general for any circuit testing. Memories require a special test pattern which aggravates testing of minimum access time following a Write operation which usually results in a long recovery time, especially when the data to be read is opposite from the data written on the previous cycle. Address sequencing is only critical in marginal cases. Of course, the test pattern must be constructed such that all bits are tested for both "0" and "1" conditions as well as testing the operation of the decoder circuits.

Many of the classical patterns developed for the 1103 1K MOS RAM are applicable to other RAMs as well, March, Checkerboard, Rowpatt, column patt, Galpatt, Diagonal, and the like and will not be discussed here. The test pattern applicable to a particular device must be considered separately. To develop a viable test pattern one must understand the physical structure of the device and its potential failure mechanism. Then combining this with the historical test patterns as a basis, you must modify them as necessary or generate a new test pattern, to not only prove that the device is functional but that it meets its operating characteristics over a period of time.

It is neither practical nor necessary to use N^2 patterns for incoming inspection tests of large volumes of RAMs. Simpler sequential patterns must be found that demonstrate the particular marginality unique to that RAM/supplier specification.

By analysis of circuit configuration and circuit evaluation (characterization), a shorter pattern (such as $n^{3/2}$) is obtained that exercises the memory in the same way as the longer, general purpose N^2 pattern.

Testing for Data Retention

Contrary to common belief, data storage in "dynamic memory cells" is limited by "noise considerations" instead of "leakage current." Presently manufactured memory devices are only capable of holding data in the millisecond range (at room temperature) under half-selected (noise disturb) conditions; however, a single cell can maintain its state for seconds in the non-selected condition. Since noise injection can be limited with substrate bias, refresh time vs. substrate bias curves can be utilized for general studies. However, such curves only indicate the "worst case" problem on a device and are not useful to pinpoint problem areas. Noise sensitivity investigation can be divided into two groups: a) study of support circuit effects, b) analyses of cell-to-cell interference.

The first group can be separated easily by the location of the malfunction which is always nearby the support circuits. Special clock waveform control is required to aggravate the noise injection. The following clock waveform parameters are the most effective to show up these problems:

(a) Fast rise and fall times.

(b) Overshoots.

(c) DC levels between V_{SS} and V_{SX}.

(d) Long clocks.

Circuit studies indicate that voltage doubler capacitors are the major cause of injections, with forward biased junctions as second, and partially turned on isolation, third. The last item is always associated with process problems, field turn-on voltage and/or punchthrough. Testing for this effect makes the clock driver requirements in testers very stringent.

Testing cell-to-cell interference is more difficult due to the large number of variables involved. The most effective way to generate noise in the matrix is usually a Write operation. It is extremely important to generate a pattern with a particular design in mind. The following factors should be considered:

(a) Possible signal paths.

(b) Effect of half-selected condition.

(c) Power supply noise, especially on V_{SS} line.

(d) Storage cell circuit and layout.

(e) Possible leakage paths due to half-selected or nearby selected conditions.

(f) Completeness of refresh operation.

(g) Partial Write condition.

(h) Effect of Read cycle without refresh.

It is very important that the test equipment used will be capable of generating the required test sequence without pauses or interruption. It is desirable to combine the functional tests and dynamic tests where the device is clocked with its specified timing relationships and the output sampled by high speed comparators. This is called real time function testing. This type of testing is most important for dynamic MOS memories. Also, by executing function tests at real time speeds, it takes less time to write and read the required patterns.

MOS circuits will often drop bits when operated at elevated temperature. Here, the question of whether the storage location is at fault is shared with other potential problems like refresh, timing and leakage. Leakage can rise to the point where the refresh rate is no longer adequate. It is thus imperative that MOS Dynamic RAMs be tested at high temperature extremes to guarantee performance.

DC Testing

Prior to the sophisticated AC tests for dynamic memories, a series of simple DC tests are performed to verify successful completion of the assembly process. These consist of standard shorts, opens, and protection diode tests. DC testing of dynamic memories is not unique. However, several points are worth emphasizing:

(a) Testing of power supply currents during operation may be required.

(b) Due to a large number of inputs (addresses), simultaneous testing of inputs is very economical.

4.4813 Data Sheet Conditions

Additionally, it should be noted that each memory data sheet must be consulted for that product's peculiar usage conditions such as power sequencing, timing conditions, valid data and the like. The following few examples are presented for illustrative purposes.

1) 2107B 4K RAM

- During CE ON V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only
- V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}

2) MK4096 4K RAM

- Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed

- Output voltage swings from V_{SS} to V_{CC} independent of differential voltage between the two

- t_{DS} and t_{DH} are referenced to $\overline{CAS}$ leading edge in random write cycle operation and the write leading edge is read-write or read-modify-write cycle

3) MCM6605A 4K RAM

- Output data is inverted from input data and is valid t_{ACC} after CE goes high

- CS should be high within t_{CSU} for a refresh cycle or before R/W goes low for a read refresh cycle

- Addresses are high when CE is latched

4) MM5070 4K RAM

- V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}

- To perform write, TSP must be pulsed low after minimum hold time and the appropriate data placed on I/O

4.4814 RAM test Results

The problems encountered with electrical testing the 1103 1K MOS Dynamic RAM have been discussed in the literature numerous times. However, problems peculiar to various other MOS RAMs have surfaced after extensive evaluation of these devices was performed in conjunction with incoming electrical tests. The next section presents a sample of some of these problems by generic part number to serve as an illustrative example of the aforementioned points in this section on MOS memories. In addition the following statements can be made regarding MOS RAMs.

- MOS memories are more susceptible to charge less than bipolar memories due to basic cell design - i.e. charge storage on MOS capacitor.

- Dynamic MOS memories are susceptible to noise which is dependent on clock input waveforms.

- Dynamic MOS devices are much more pattern sensitive than are static or bipolar devices.

- Refresh tests must be performed at 70°C.

- Data retention tests are necessary in critical applications for static MOS RAMs.

- MOS memories are subject to static discharge problems.

- Static MOS RAMs use dynamic decoders (via chip select) to obtain reduced power consumption. Thus, these must be tested as they are for dynamic RAMs.

- Static NMOS RAMs are faster at -55°C than at +125°C

4.4815 MOS RAM Device Problem Summary

The following summarizes problems encountered in testing and characterizing various MOS RAMs.

4096 16 Pin 4K RAM

Manufacturer A

- TCRL timing problems (relationship between $\overline{CAS}$ and $\overline{RAS}$)
  - Parts work at two extremes but fail in between
  - Failures are due to noise generated on chip due to external source - moving the strobe moves the noise
  - Prime Source - no problem

2107B 22 Pin 4K RAM

- Decoder/chip overheating problem
- Sense amplifier data problem
- High power dissipation
- Whenever an address was accessed, a number of times in succession, the address drivers went to a 10V reference level resulting in a slow decode
- Short address hold time (insufficient address time)
- Address loading problem. Bring address line inside cycle, address line pulls down source device causing jitter. One can never set address line to Zero. This creates a noise problem - lose address decode.
- VOL varies with V_{DD}. VOL level problem

MCM6605 22 Pin 4K RAM

- At internal visual inspection, the device had exposed oxide over 25% of the die surface (no vapox)
- Refresh problem as a function of temperature
- Access time vs temperature problem

- Low breakdown voltage
- Bad process from contamination viewpoint. Several devices were "zapped" during 15v cell stress test(3 pin holes)

TMS4060 22 Pin 4K RAM

- Require long write pulse width
- Small CE
- Long CS low
- CE causes latchup on DO in some instances
- Data hold time at 25°C is an exact requirement (necessary)
- TMS4060-2 had disturb problem. Using a refresh checkerboard with V_{DD} high and V_{BB} low at 25°C, the device lost data (sagged) at 20 msec. Make sure device is disturbed during testing
- Sensitive to V_{BB}
- It has had bonding problems
- An oxide problem exists that is brought out by burn-in (forming lead)

MM5280

- Early parts should pattern sensitivity using an n 3/2 pattern across rows and down columns at high V_{DD} and low V_{BB} a hole appeared in the operating region shmoo plot. National supposedly redesigned the devices reference

µpD411

- Over a long time (16-17 hours) a hole appears in the shmoo plot
- µpD411 uses an anodized aluminum process which is difficult to control

MK4027

- No problems discovered to date

S2222 512 Bit CMOS RAM

- Large shift in leakage current
- Fails to meet specification limits at rated V_{CC}, must derate V_{CC}

- Shift in DC/AC characteristics after burn-in
- Low voltage parts, 5V not 10V as stated

CD4061 256 Bit CMOS RAM

- Timing problems at all temperatures
- Galpatt sensitivity
- Construction problem - slug/die bonding; caves under metal

AMS 6003/NSC 5262

- Very conservative specification limits (Ref. A 2048 Bit RAM Characterization by E.R. Hnatek, R. Schmitt 1975 IEEE Memory LSI Test Symposium)

4200 Static 4K RAM (Ref. How Static is the Static 4K RAM? by E.R. Hnatek et al 1976 IEEE Memory LSI Test Symposium)

- Data Retention problem due to open pullup resistor in memory cell
- No pattern sensitivity
- Conservative specification limits

Electrical inspection test summary of a sample of 55,000 16 pin 4K MOS RAMs at 70°C resulted in a reject rate of 2.7%; indicating the viability and stability of the product.

Some of the MOS memories are becoming mature products and experience reject rates at the incoming inspection level comparable to SSI and MSI TTL devices.

4.49 MOS PROMS

FAMOS PROM

MOS technology does not lend itself readily to fusing or avalanching. There are some very interesting developments that permit programming the MOS ROM, however. These programming techniques utilize the fact that charge can be stored within the gate dielectric or within varied gate structures. This charge storage can be a semipermanent mechanism and provides for long-term programming of the MOS PROM. Figure 99 shows the cross section for a programmable MOS ROM structure, the floating Gate Avalanche-Injection MOS (FAMOS) charge storage device.

The memory cell is programmed by the transport of hot electrons from the vicinity of the drain junction to the floating gate, with the application of a high junction voltage - in excess of 30V. Once the electrons have

been collected on the floating gate, the memory cell transistor assumes an "on" condition. The on or off (programmed or unprogrammed) condition can be detected through the use of a select transistor with row and column decode. This basic cell has been implemented in the 1702A 2048 bit PMOS PROM array.

A variation of the same basic FAMOS cell uses a two layer polysilicon process where the first layer forms the floating gate, and the second layer forms the select gate. Again cell operation depends on the transport of electrons to the floating gate where they are collected and used to offset the threshold voltage as measured with the top polysilicon gate. This basic single transistor memory cell has been implemented in the 2708 8192 bit N-Channel FAMOS PROM and is shown in Figure 100.

Both memory cells program the floating gate to a potential of about -12 volts. At normal operating temperatures this programmed voltage remains indefinitely. The electrons are removed by illuminating the memory cell with ultraviolet light for five to ten minutes. The ultraviolet light produces a photocurrent from the floating gate back to the substrate thereby discharging the gate back to its original condition.

The FAMOS charge-storage device described above can be used as the basic storage element in a large memory array. A circuit schematic of the memory cell and its associated decoding circuitry is shown in Figure 101. The decode and sense circuits shown are common to both the PROGRAM and READ modes. To select a bit to be programmed, the address decode inputs as well as the V_{DD} and V_{GG} lines are energized to -50V. Programming of a memory bit is accomplished by coincidence selection of the X and Y select lines. The applied programming pulse is transferred to the selected FAMOS device that turns normally ON due to the electron charge transferred to its floating gate. All other memory bits are not programmed due to either the lack of a pulse on the Y select line or the absence of a transfer pulse on the X select line. The programming signal V_P is a -50V, 5.0msec pulse. The amount of charge stored in a memory cell in response to a programming pulse is typically 3.0×10^{-7} C/cm^2 which is equivalent to 10V on the gate of a conventional MOS transistor. The load current required to program a memory bit is approximately 5.0mA.

Memory cell operation in the READ mode is similar to that of other ROMs. A memory bit is selected by a coincidence of signals on the X and Y select lines. However, compared to the programming mode the READ mode voltages are substantially lower. Since the programming threshold is -30.0V, the maximum READ voltage of -15V guarantees a wide margin to avoid disturbing the information during the READ mode. Information in the selected memory cell is sampled by the output sense circuit. If a "0" is stored in the cell (charge on the floating gate) the FAMOS device is ON and the level at the input of the sense circuit is close to V_{CC}. A "1" corresponding to no charge stored in the cell is reflected by a more negative level (close to V_{DD}) at the input of the sense circuit. Information can be decoded and sensed in either the static (no clocks) or dynamic mode (2 clocks). The static mode of operation eliminates the need for clocks at the expense of increased power dissipation and reduced speed, while the dynamic mode offers advantages in both performance categories. The option

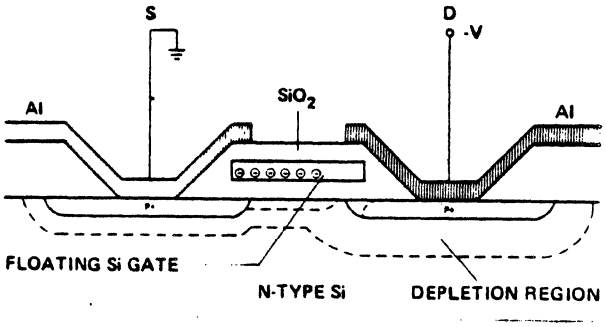


Figure 99.

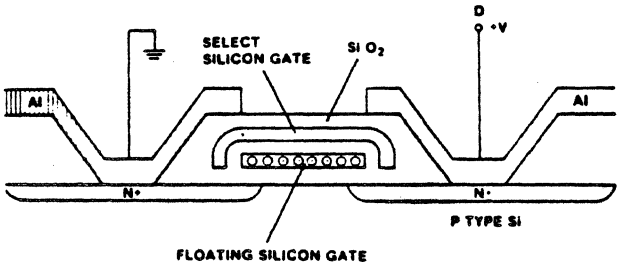


Figure 100

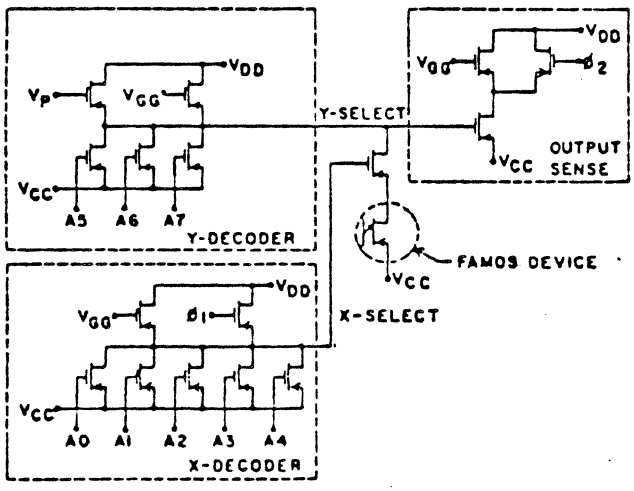


Figure 101: Memory cell with its associated decode and sense circuits.

of the two modes of operation is achieved by parallel load transistors in the decode and sense circuitry, one connected to the clock lines and the other to V_{GG} as shown in Figure 101. The load device connected to the V_p terminal is connected to Ø1 in the dynamic READ mode. Mode selection is accomplished by activating the clocks with V_{GG} connected to V_{CC} in the dynamic mode. V_{GG} is activated in the static mode with the clocks connected to V_{CC}.

A typical electrically programmable ROM consists of a monolithic array of 2048 FAMOS devices organized as 256 words of 8-bits. A block diagram of this memory organization is shown in Figure 102. All circuit blocks are common to both the PROGRAM and READ modes with the exception of the PROGRAM data input buffers. In the PROGRAM mode the eight output terminals are used as data inputs to determine the information pattern in the eight-bits of each word, while word address selection is performed by the X and Y decoders through the input drivers. The PROGRAM data input circuitry for one of eight outputs is shown in Figure 103. To inhibit the programming of a bit, a negative voltage is applied to the data input terminal. This voltage level is transferred to the inhibit transistor (chip select is enabled), which turns ON and overrides the Y select signal. To allow programming of a selected bit, the data input terminal is kept at ground.

Initially, all 2048-bits are in the "1" state corresponding to normally OFF FAMOS devices (no charge on the floating gate). Information is introduced by selectively programming "0" in the proper bit locations through charging the FAMOS devices from the PROGRAM terminal. The supply (V_{DD}, V_{GG}, V_p), address (A_0 - A_8) and data input (D_{1N1} - D_{1N8}) voltages in the PROGRAM MODE are detailed in Figure 104. A timing diagram for the applied voltage sequence in the PROGRAM mode is shown in Figure 105.

In the READ mode the PROGRAM data input buffers are inhibited by the chip select signal to cut OFF the feedback path from the output to the memory array established in the PROGRAM mode. Memory operation in the READ mode is the same as in conventional mask programmable ROMs. The input and output buffers provide for full TTL compatibility and addressing is accomplished by the X and Y decoders operating at the voltage levels detailed in Figure 104.

A selected memory cell with a charged FAMOS device will be reflected by a low "0" TTL level at the output, while a memory bit that is not charged will result in a high "1" TTL level. Both the static and dynamic modes of decoding and sensing are available in a single package through use of parallel load transistors. Mode selection is done by activation of either the clock lines (Φ_1, Φ_2) or the V_{GG} terminal in the dynamic and static modes, respectively. Typical access times are 400nsec in the dynamic mode and 700 nsec in the static mode.

As can be seen from the above description, electrical programming of the memory is conceptually the same as operation in the READ mode with the exception of the voltage levels. (Figure 104). Hence, the memory can be easily programmed from punched paper tape or other data input devices through an electrical programming terminal. Once programmed, the information pattern in the memory can be erased (restored to the all "1" state)

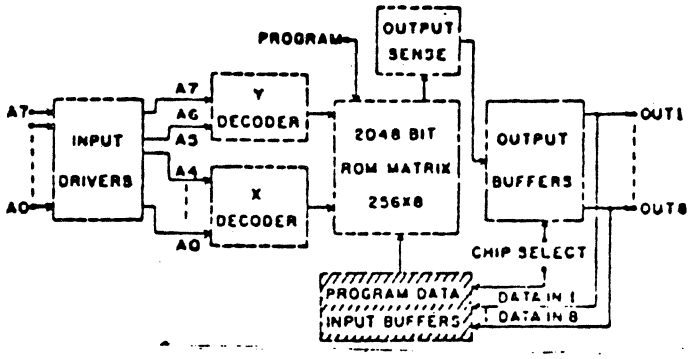


Figure 102: Block diagram of typical memory organization

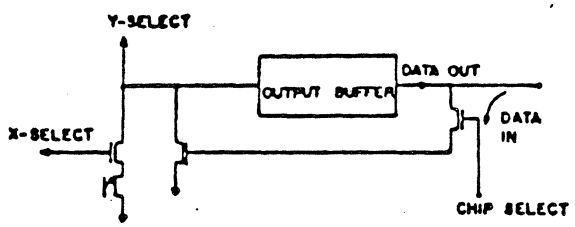


Figure 103: Circuit description of PROGRAM data input buffers.

APPLIED VOLTAGE (VOLTS) / MODE	V_{DD}	V_{GG}	V_P	ϕ_1	ϕ_2	V_{CC}	ADDRESSES / DATA IN
PROGRAM	-50.0	-50.0	-50.0	V_{CC}	V_{CC}	0.0	-40.0
STATIC READ	-9.0	-9.0	V_{CC}	V_{CC}	V_{CC}	+5.0	TTL
DYNAMIC READ	-9.0	V_{CC}	-9.0	-9.0	-9.0	+5.0	TTL

Figure 104: Applied voltage level to the memory in the PROGRAM and READ modes of operation.

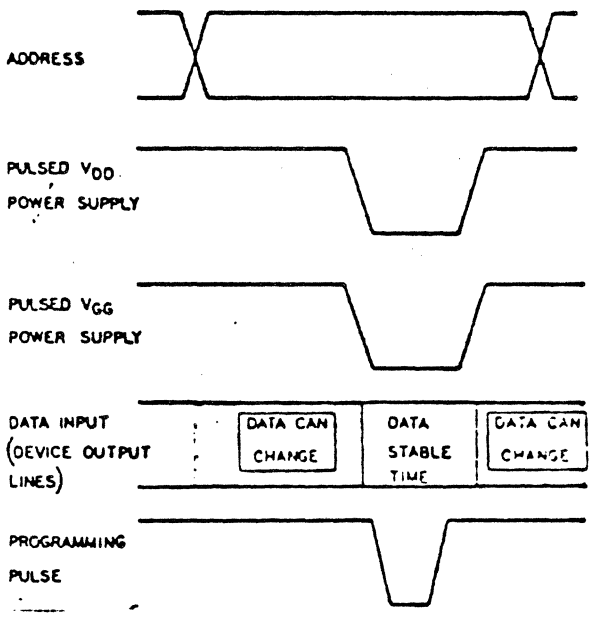


Figure 105: Timing diagram for the PROGRAM mode.

by ultraviolet light before packaging or by exposure to X-ray radiation. Reliability information regarding the stability of the FAMOS PROM cell programmed is available from Intel Corporation.

4.492 MAOS PROM

Another programmable-ROM uses the gate dielectric itself for charge storage. A class of dielectrics including alumina and silicon nitride may be used as gate dielectrics for the MOS transistor and can also provide a re-programming feature. The cross section for a memory cell using alumina dielectric is shown in Figure 106. This element is termed a MAOS memory element.

The MAOS element is programmed by the application of a positive or negative gate voltage pulse above a critical polarization level. For p-channel devices, a positive gate voltage is used to write into the cell. A write voltage of 50 V amplitude requires 10 to 20 μs for programming prototype structures. The access times for readout are approximately the same as for standard MOS ROM arrays. Erasing requires an opposing polarity on the gate. This type of memory cell may be reprogrammed at a fast rate. This type of device can be called a read mostly memory (RMM) since it begins to take on the aspects of a random access memory structure in terms of reprogramming speed.

4.493 Testing MOS ROM/PROM

The testing considerations discussed for Bipolar ROMs/PROM apply as well for MOS ROMs/PROMs. In addition, there are several failure modes to be watchful of in testing the devices. First, MOS PROMs are subject to a charge loss characteristic by virtue of inherent device construction. Nearly all retention testing at high temperature tends to accelerate charge loss failures. MOS PROMs require programming voltages well in excess of normal operating voltages and these voltages are carried through each row and column during the programming operation. Being a stressful process, devices or cells with weak gate dielectrics will be uncovered. The majority of rejects of MOS PROMs during incoming electrical inspection is for excessive output leakage current and charge loss.

One thing is evident, more work needs to be done in the area of MOS PROM/PROM testing.

4.5 Charge Coupled Devices (CCDS)

The charge-coupled devices operates by storing and transferring charge, representing information, between potential wells at or near the surface of silicon. The potential wells are formed by closely spaced MOS capacitors that are being pulsed into a deep-depletion mode by a multiphase clock voltage. This charge is then transferred along the semiconductor surface in shift register fashion, by simple manipulation of the voltages that constrain it.

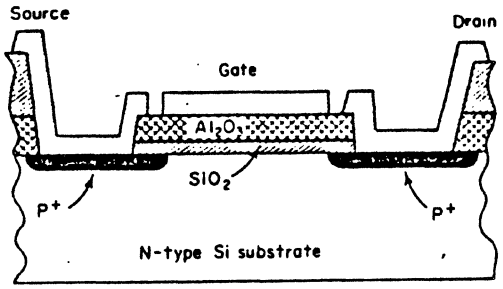


Figure 106: Cross section of an alumina-dielectric device.

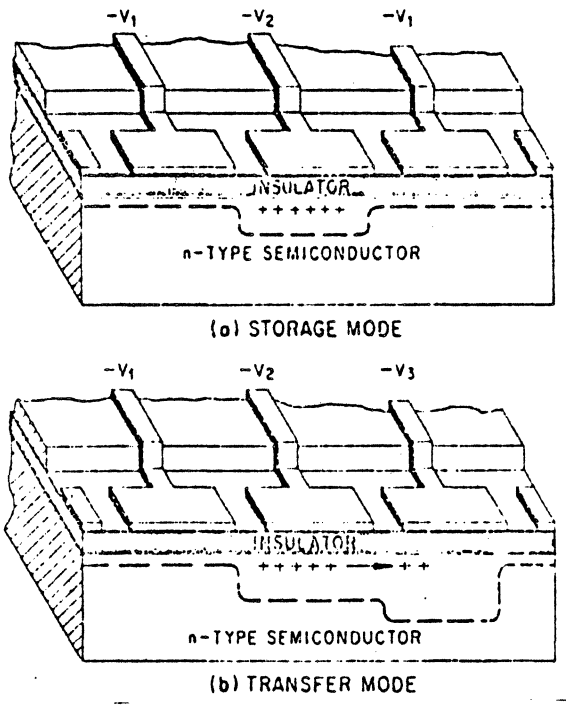


Figure 107: CCD Operation

Structurally, a CCD consists of an n-type or p-type silicon substrate, an MOS-type silicon dioxide insulation layer, and a metallized electrode over that (Figure 107). Notice that no p-n junctions are required to shift data from one point to another, whereas conventional MOS shift registers need a minimum of three transistors per data point and about six to eight diffusions per transistor. Diffused p-n junctions are required in a CCD only to input and output data and, in memory devices, also to regenerate a signal after it has made a number of shifts.

In operation, a CCD with, say, an n-type silicon substrate first has a threshold voltage of about -1 to -2 volts ($-V1$) applied to the substrate so that a uniform depletion layer forms beneath all electrodes. Next, to enter the storage mode, a more negative voltage of around -10V ($-V2$) is applied to an individual electrode -- the middle one in the storage element of Figure 107 (a) for example -- creating a deeper depletion region beneath it that spatially defines the potential well. The device can now receive and store charges (minority carriers). In a memory device these would be injected into the substrate by an input p-n junction, and in a camera device they would take the form of hole-electron pairs created by light impinging on the silicon substrate. In either case, since the minority carriers in n-type silicon are holes, and since the electrode is negative with respect to the substrate, the holes are attracted toward the electrode and held in the potential well beneath it. Charge stored in and transferred between potential wells forms the basis of all charge-coupled technology. Shown here is a three-phase system. In storage mode (a), voltage $-V2$ is greater than bias voltage $-V1$, and forms a potential well that captures the charge. In the transfer mode (b), charge moves along to the next electrode as soon as a still larger voltage $-V3$ has been applied to that electrode and created a larger potential well beneath it.

In the transfer mode, the stored charge is shifted along by the application of $-V3$, a still more negative voltage of about -20V, to the third electrode of the element, as shown in Figure 107 (b). This establishes a well of even greater potential under that electrode, which attracts to it the holes stored under the middle electrode. The voltages are now returned to the condition of Figure 107 (a), except that they have moved on by one electrode.

If a long chain of these electrodes is fabricated and voltage applied so as to continuously create deeper potential wells to the right of full wells, then charge will be caused to "flow" from left to right along the chain.

Basically, charged-coupled devices are dynamic shift registers. They can be used wherever a serially accessed memory is used -- a CCD memory consists of a number of parallel shift registers that transport charge. The digital input signal is converted to charge and is clocked through the register. During each transfer step, a small amount is lost (each transfer is about 99.99% efficient). "Dark currents" that arise from thermal effects, from substrate leakage, and from the clock voltages also cause changes in the amount of charge. Therefore, at the end of the register,

the charge is identified as either a "0" or a "1", and a refreshed signal is recirculated through the register. This process is repeated until a new data signal replaces the old.

4.51 Charge Coupled Memory Device Organization

Charge coupled memories have a myriad of different device organizations that reflect on the system operation and performance. Though, they are simple shift registers, their diversity and aggregate behavior impose peculiar constraints on the design of memory testers and test programs.

The different types of charge coupled memory devices appearing in the commercial market can be grouped into two categories:

(1) Charge Coupled Memory with common clock lines.

(2) Charge Coupled Memory with individually controlled clock lines.

The first category includes memory devices that have common clocks for groups of shift registers so that data moves simultaneously in all the shift register channels. This category can be further divided into two different device types: Short Loop Common Clock (SLCC) CCD Organization (example: Intel 16K), and Serial-Parallel-Serial CCD Organization (example: Bell Northern Research 16K). The SLCC CCD memory is organized with 32 to 256 shift registers each of 64 to 256 bits each and a decoder selects access to one of the shift registers. Such a device is shown in Figure 108. It may also employ internal multiplexing to increase the data rate.

Figure 109 shows a Serial-Parallel-Serial Memory Organization. The data rate through the input and output serial registers is high (1 to 10MHz), whereas, the data shifts slowly in all the parallel shift registers. Consequently, the overall chip dissipation is low and high packing density is achieved. Another important feature of the SPS structure is that for an NxM CCD chip, each charge packet has to make only 2(N+M) charge transfers, therefore, a large block of date can be refreshed by one signal regenerator.

Figure 110 depicts a charge coupled memory having individually controlled clock lines for all the registers. However, it has common input/output circuitry. Data is moving only in one of the registers at a time. Hence, the chip dissipation is low. But each register must move completely once during the refresh interval and the refresh must be done individually.

Charge coupled memories can be operated in horizontal or vertical modes either with continuous clock or burst clock. The testing should be performed in all the different modes of operation so as to evaluate the capabilities of the device completely and decide on the optimum mode of operation. The test modes may also be different for devices having common clock lines (BNR 8K, Intel 16K), or individual clock lines (Fairchild LARAM and other variations).

In the horizontal mode clock phases are applied so that data moves in the registers in the horizontal direction. For devices with common clock lines,

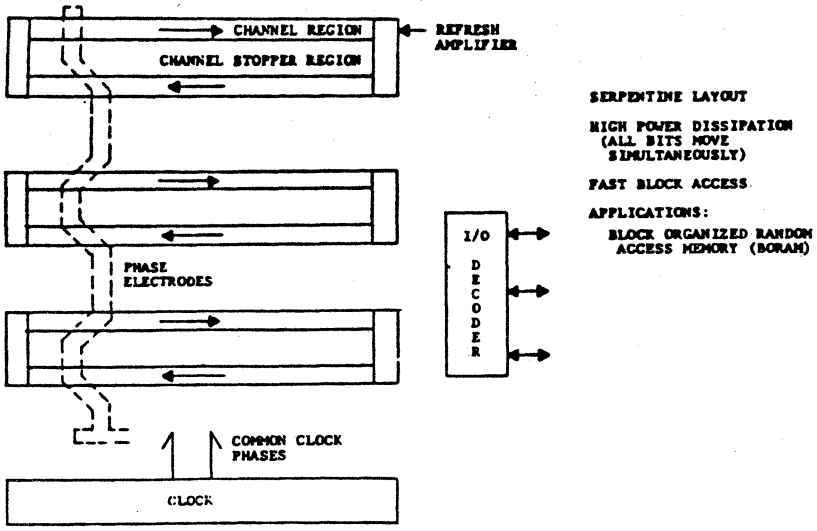


Figure 108: Short Loop Common Clock (SLCC) CCD Organization

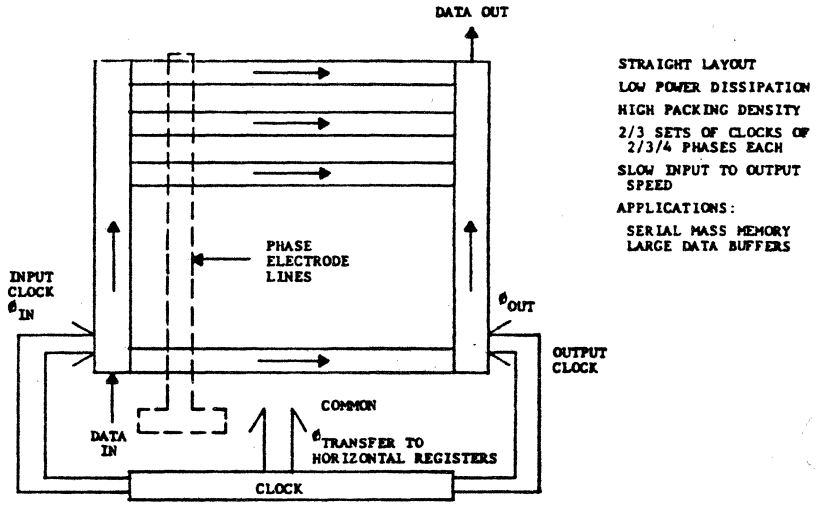


Figure 109: Serial-Parallel-Serial CCD Memory Organization

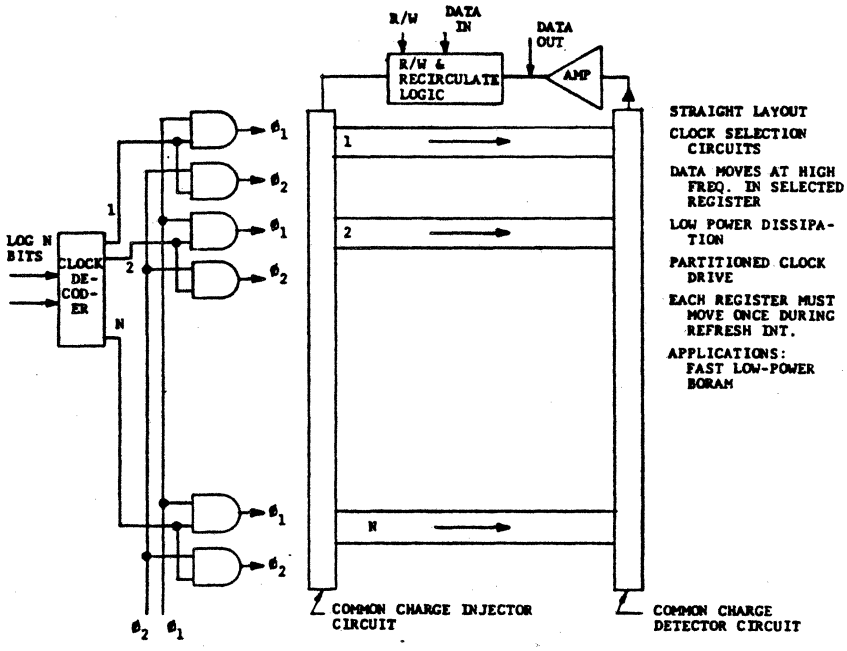


Figure 110: Charge Coupled Memory with Individually Controlled Clock Lines

data in all the registers moves simultaneously but we access a particular register as selected by the decoder. If successive registers are to be accessed one continues applying the clock and selects the access to successive registers. Depending upon the device design and fabrication, the device can be run at frequencies from 10KHz to 10MHz.

Intel's 2416 device, when run at a 1MHz data rate, takes 256 μs to access the entire 256 bit shift register while the BNR 16K device, when run at a 10MHz data rate takes 409.6 μs to access the entire 4096 bit register. The high frequency operation is limited by the charge transfer mechanism and speed of peripheral sense, regeneration, and decode circuitry. For devices with individual clock lines, the horizontal mode of operation is the preferred one. One register at a time is selected and moved around completely to align it with the rest of the registers.

In the vertical mode of operation, one accesses the data from the output end of all the registers by sequencing through all the register addresses. For devices with common clock lines, one moves the data horizontally in all the registers by one position and then sequentially reads out the data while keeping the registers stationary. The shift clock applied to the register is a low frequency (10KHz to 100KHz), so that enough time is provided to access a group of shift registers. If the minimum low frequency clock, consistent with the maximum storage time, does not allow enough time to access each of the registers, one repeats the test on groups of registers. The maximum data rate in the vertical mode is limited by the speed of the input/output circuitry, particularly the address decoder. Devices having individually clocked registers may be operated in the vertical mode. In that case, data in successive registers is moved by one bit at a time and a vertical segment of the data is taken from the output end of the registers. If operated in this mode, the average bit access time is much longer (1ms) and, therefore, this mode of operation is not recommended, unless high frequency shifting is employed to access the beginning of the data block.

Operation and testing of the CCD can be performed by applying a continuous clock or a periodic burst clock. Devices with common clock lines lend themselves easily to either continuous or the periodic clock modes. The application of the periodic burst mode of operation has several system advantages, namely, the access to a block of information stored in a register can be immediately available without any wait time. If a request for access is made during the refreshing burst clock, one has to wait until the beginning of the block moves to the output end. If the device is operated in this mode, the dark current is, however, not averaged and local defects can introduce fixed pattern noise. If the devices have internally generated reference voltages that are stabilized by the clock, the burst mode of operation is not recommended. Devices with individually controlled clock lines are normally operated with a burst clock which is successively applied to all the registers. Thus, access is made in the horizontal mode. They can be, however, operated in the vertical mode with the application of a continuous low frequency clock to the device while sequencing through the address lines every cycle. This way, the dark current is averaged and errors due to dark current spikes are eliminated, but the average access time to any word becomes very long (~10ms).

4.52 CCD Performance

In addition to the usual parameters that characterize MOS devices, such as gate threshold, oxide charge and interface states, the two most important performance characteristics of CCD's are (1) dark current and (2) transfer efficiency or inefficiency.

Charge coupled devices operate in the thermal non-equilibrium state, and hence, the dark current generated tends to fill up the charge wells and revert the device to the thermal equilibrium.

Transfer inefficiency in charge transfer occurs due to the finite mobility of the carriers and charge trapping in the localized surface states. Generally, the upper frequency limit of the charge transfer is determined by the transfer inefficiency.

In addition to these two parameters, the general performance limitations of the peripheral circuits determine the overall performance of the charge coupled memory.

Dark Current

The dark current or thermally generated background charge can be measured (1) either directly as the (average) drain current during the continuous operation of a CCD, (2) or the CCD clock can be periodically stopped for a fixed integration time while the thermally-generated charge is collected. The clocks are then cycled and the dark current profile is read-out and detected. The second approach has the advantage of providing a complete profile of the dark current distribution including the magnitude of the localized dark current spikes that are very sensitive to the applied gate voltage.

Dark current background levels as low as 5 to 10 nA/cm^2 have been reported. However, the control of dark current and dark current spikes is still one of the more critical aspects of CCD manufacturing.

Charge-Transfer Efficiency

The fraction of charge transferred from one well to the next is referred to as the charge transfer efficiency, η. The fraction left behind per transfer is the transfer loss, or transfer inefficiency, denoted by ε, so that $\eta + \varepsilon = 1$. Because η determines how many transfers can be made before the signal is seriously distorted and delayed, it is a very important figure of merit for a CCD. If a single charge pulse with an initial amplitude P_o is transferred down a CCD register, after n transfers the amplitude P_n will be:

$$P_n = P_o \eta^n \simeq P_o (1-n\varepsilon) \quad \text{(for small } \varepsilon) \quad (1)$$

Clearly, ε must be very small if a large number of transfers are required. If we allow an $n\varepsilon$ product of 0.1, an overall loss of 10 percent, then a three-phase, 330 stage shift register requires $\varepsilon < 10^{-4}$, or a transfer efficiency of 99.99 per cent.

The maximum achievable value for η is limited by how fast the free charge can transfer between adjacent gates and how much of the charge gets trapped at each gate location by stationary trapping states. In surface-channel devices the charge trapping is normally attributed to the fast states at the $Si-SiO_2$ interface. The trapping of charge by the interface states can be avoided by means of bulk (buried) channel construction. In bulk-channel CCD's small trapping type transfer losses have also been observed and are being attributed to charge trapping by stationary bulk states.

High transfer efficiency (>99.99% per transfer) is necessary for high-frequency applications requiring long chains. One approach for improving high-speed transfer efficiency is to construct a potential slope inside each well so that charge is propagated by the built-in field rather than thermal diffusion. This reduces charge transit time across the well to a few picoseconds. Resistive gate layers and very closely-spaced small gates on thick insulator layers assist in providing built-in fields.

Transfer efficiency is also improved by reducing the number of traps (interface states) in the CCD channel. One promising method buries the transfer channel below the surface of the semiconductor where the material is more uniform. Minority carriers will follow a buried channel if the region is doped preferentially with ions of opposite charge (n-type silicon may be doped with boron). Satisfactory doping profiles can be attained with ion-implantation techniques.

Excellent transfer efficiencies up to frequencies of many megahertz have been achieved using ion-implantated channels. One limitation of this technique, however, is that only small quantities of charge can be handled. For high signal levels, other methods must be employed.

Refreshing CCD Shift Registers

Quantities of charge can be inserted into a CCD chain by building a p-n junction into the semiconductor at the beginning of the line of cells. Another p-n junction will be required to extract the information at the output end. The resulting device can be operated as an analog delay line or digital shift register.

It should be noted that not all of the charge supplied by the input device will be delivered to the output diode. A certain fraction is "waylaid" in traps at the semiconductor surface and may be re-emitted later as noise. Also, it takes time to transport all of the carriers, so transfer efficiency requirements impose limitations on operating frequency for any given device configuration.

Transfer efficiency may be improved by injecting a uniform small portion of charge in each well of the input so that no well is ever completely empty. This charge in the channel fills slow traps along the channel and thus improves charge transfer. A certain low signal level is then associated with binary zero detection. (This is termed "fat-zero" operation.)

When transfer efficiency falls below acceptable limits, the data may be extracted, restored, and reinserted into the CCD chain. At the end of the first CCD chain, an output p-n junction detects degraded "bits" and supplies signals to the gate of a FET amplifier operated in the saturation mode. A set of "clean" "1's" is supplied to the next chain, and the output of the FET amplifier modulates the input circuit of that chain. In practice the refresh circuit is fabricated on the same chip as the memory.

Power dissipation in the CCD shift register is approximately linear with clock frequency, and is highest when large quantities of charge are being transferred. Typical values for practical devices with small dimensions are in the 1 to 5 μW/bit range.

Operational Region

The operational region defines the margin of the external parameters within which the memory device can function properly. It should be realized that the operational region is multi-dimensional. The principal dimensions involved are V_{DD}, V_{BB}, V_{SS}, access time, temperature, clock frequency, clock transistion time, relative clock timings, clock levels, etc. The two-dimensional shmoo plot only shows a cross-section of the operational surface in a multi-dimensional space. Generally, shmoo plots with V_{DD} vs. V_{BB}, and V_{DD} vs. access time are generated at different temperatures and at low and high frequency limits, with the other timing set at extreme conditions.

For CCD's, particularly the ones with common clocklines, the clock capacitance is very high, usually, several hundred picofarads. A large portion of this capacitance is due to inter-electrode capacitance and is more so in the overlapping gate structure and serpentine structures having crisscross clocklines. This leads to large power dissipation on the clock drivers and imposes the lower limits on the clock transition times. The upper limit of the transistion time is due to the fact that, signals may go through the partially on/off transistors.

The upper limit of the clock frequency is limited either by the charge transfer process or the inherent speed-sensitivity of the sense amplifier. For surface channel CCD's with "fat zero" operation, the frequency limit is about 10MHz. For bulk channel CCDs, the charge transfer is determined by the bulk mobility and the speed is limited by the peripheral circuits to about 20MHz.

The low frequency limit is determined either by the storage time in the active channels or by the leakage at the storage nodes of the peripheral circuits when dynamic circuitry is employed.

Storage Time

Storage time is defined as the time within which the data must be refreshed in a CCD memory. There are two different types of storage time - the storage time in the continuous (or distributed) mode and the storage time in the halt mode with a burst refresh.

The storage time in the continuous mode T_c is

$$T_c = NT_{max} = \frac{Q_{Inf}}{2I_{av}}$$

where

N = the number of storage sites before the refresh amplifier

Q_{Inf} = size of the information packet

$I_{av} = \sum_{j=1}^{N} I_{j/N}$ where I_j = thermal current generated at storage site j.

If the device is operated in the halt mode with a burst of refresh, the storage time will be determined by the dark current generation at the worst storage site, i.e. the site with the largest I_j.

Thus,

$$T_H = \frac{Q_{Inf}}{2\ I_j\ (max)}$$

Therefore, the halt time is controlled by the largest I_j in the shift register.

One can measure T_c by decreasing the shift clock frequency until information is lost. On the other hand, one can measure the storage time while reading the information in a burst at a particular high frequency and repeating this until an error occurs. Here, there is a distinction between the SLCC type and the LARAM type organizations. For the SLCC type, with the clock applied, all the bits in the shift registers are refreshed. Therefore, we have to read out one shift register and wait for a certain time (the halt time) before another readout on another track. For the LARAM, however, the refresh is done one shift register at a time. Therefore, after the halt period, the readout can be done sequentially.

For the above analysis, it can easily be seen that,

$$TC > T_H$$

Therefore, the storage time is usually shorter in the burst mode of operation, if this mode is allowed on the device.

4.53 Testing CCDS[1]

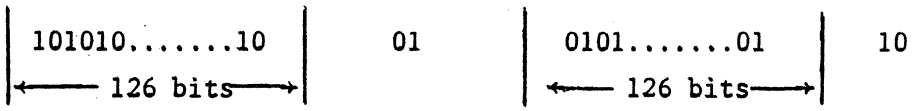
For testing CCDs, there are two kinds of patterns we are concerned with,

[1]Charge Coupled Memory Test Philosophy by G. Panigrahi et al 1975 IEEE Memory/LSI Test Symposium Proceedings.

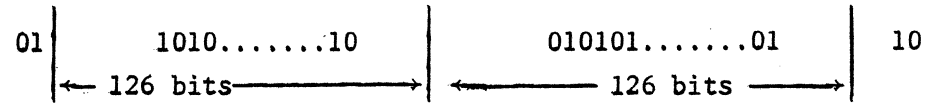
i.e., one is the test data pattern (or background signal pattern), and the other is the test program pattern. These patterns are used to test the sensitivity of the CCD chip that includes both the charge coupled section and the peripheral circuitry. The worst-case patterns should be picked out for a particular CCD organization. Operational margins can be established by shmooing along various dimensions using different test patterns. The results help the system designers to decide what external parameters should be used in order to achieve the maximum operational margins. The test patterns and the test program patterns are detailed in this section.

The worst-case data pattern (or background signal pattern) for charge transfer in the CCD channel is a full packet in an otherwise empty channel and an empty packet in an otherwise full channel. If a full packet corresponds to an "1" and an empty packet to a "0", we would have the maximum deterioration of "1" due to transfer inefficiency in the channel, whereas the latter, maximum deterioration of "0" would occur due to transfer inefficiency and consequent pick-up of the residue charge. These patterns should be exercised such that the "1" should be behind a string of "0's", and the "0" should be behind a string of "1's". It is desirable to have complement patterns in the adjacent channels so that shorts or leakage through the channel stops can be detected.

There are several points to be remembered when the data patterns are loaded into the device: (a) the number of bits per refresh amplifier, (b) the topological layout of the shift registers, (c) input/output data multiplexing and whether the multiplexed data is refreshed by the same refresh amplifier, (d) the organization of the CCD - whether the data flow is serpentine, uni-directional or serial-parallel-serial (SPS). Take the Intel 2416 16K bit CCD as an example. There are 64 storage bits prior to refresh, and four channels per shift register loop. The data-flows in channels (1), (2), and in channels (3), (4), are in opposite directions, and the data are multiplexed between channels (1) and (2), and between channels (3) and (4). The data entered into channel (2) will be shifted to channel (3), similarly, for channels (1) and (4). The worst-case data patterns entering into the channel are as follows:



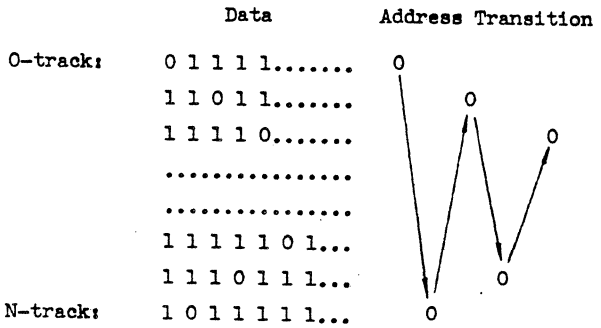
Another advantage of using the above pattern is that the refresh amplifier is being exercised simultaneously by high frequency toggling. If the data-flow was uni-directional, the data pattern is as follows:



It is desirable, however, to keep the refresh amplifier at a constant level for some time before toggling because it has been found that, in some cases, the refresh amplifier becomes saturated and sluggish in responding. The SPS has a peculiar structure as the data flows are perpendicular to each other. Because the serial shift registers are clocking at a higher frequency than the parallel shift registers, they should limit the high frequency performance of the device. Shorts or leakage among the parallel channels should also be checked. A diagonal of "1's" in a background of "0's" and the complement of this pattern can be used. It is advantageous to have the diagonal tilted away from the input/output ports.

The test patterns are used to check (1) read and write operations at the correct locations, (2) storage of "1" and "0" at each storage element, (3) correct operation of the sense amplifier, and (4) device behavior for different possible transitions. These include READ/READ and READ/WRITE transitions. The MARCH pattern can be used. MARCH is very fast, and is the least extensive test. The advantages and disadvantages of WALKING, GALPAT, GALPAT with Write recovery, and PING PONG, are well known and will not be repeated here. We shall merely point out some characteristics of the test patterns for CCDs.

For SLCC structures, two modes of operations are possible, namely, horizontal mode and vertical mode. In the horizontal mode, the content of the whole shift register is read out or written in. In this case, the data rate is limited by the clock frequency. In the vertical mode, the data is stationary and is read out sequentially through all shift registers. The data rate in this case is limited by the speed of the address decoder and/or the output circuit. A severe test for the address decoder is by the use of a Gray code and its complement, so that for an N bit address at least (N-1) address lines are making transitions in the test pattern. However, in some testers the Gray code cannot be generated easily. If this is the case, the following pattern is useful to test the worst-case response time of the decoder.



The address transition of Ping Pong in this situation would be starting from the upper half of the shift registers:

$A \longrightarrow \overline{A} \longrightarrow \overline{\overline{A}} + 1$ ....., and, with the above pattern turned upside down and from the lower half of the shift registers:

$A \longrightarrow \overline{A} \longrightarrow \overline{\overline{A}} - 1$ ..... In this case, any access to the wrong address will be detected as a "1" at the output, assuming no data inversion.

A pattern which is useful in checking faulty addressing in the vertical mode is:

	Data
Track 0	0 1 1 1 1 1 1.....
Track 1	1 0 1 1 1 1 1.....
	1 1 0 1 1 1 1.....
	1 1 1 0 1 1 1.....
	.....
	.....
	.....
	.....

The bits are accessed vertically in the sequential fashing. For structures with individual clock lines, the vertical mode is not recommended because of the time involved in shifting the bits in each line during access. The testing is done by reading and writing the entire shift register.

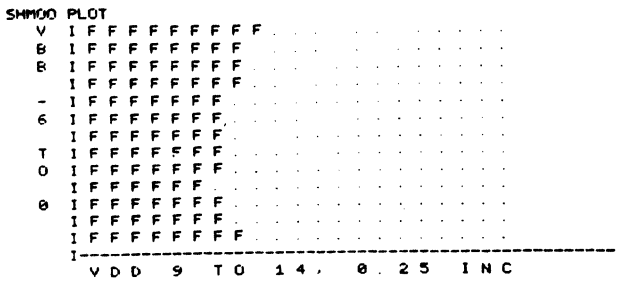
The testing of charge coupled memories with no address decoder, like BNR 16K and Fairchild 9K CCD's, involves simply verifying whether each location can be set to "1" and "0" levels.

In the test patterns, the $\overline{CS}$ (and $\overline{CE}$) should also be inserted to check its proper functioning.

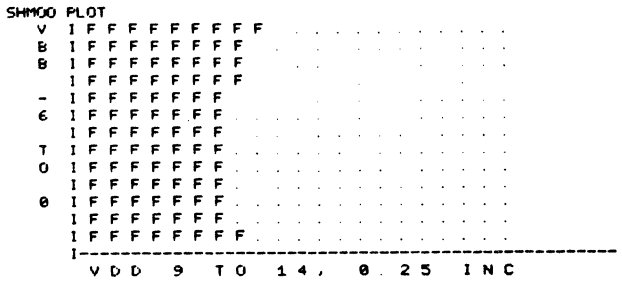
As an example shmoo plots were performed using different patterns. It was found that the operational regions are roughly the same for a particular device no matter which test pattern is used, indicating the address decoder is not limiting the performance (Fig. 111). However, the operational region using READ mode is slightly wider than those using RMW (Fig. 112).

4.54 Test System Considerations

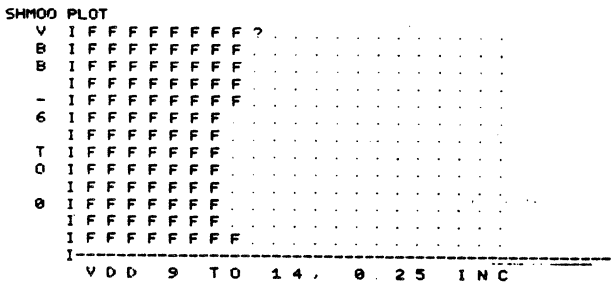
Most of the automatic memory testers currently available on the market are geared towards testing of random access memories. Due to the specific characteristics of charge coupled memories as pointed out earlier in this section, the tester manufacturers need to take into account the special requirements in order to allow the users to accomplish effective testing of charge coupled memories. The following suggestions are made from the user's point of view.



INTEL 16K CCD VBB VS VDD
SHMOO PLOT FOR PING-PONG @ 25°C

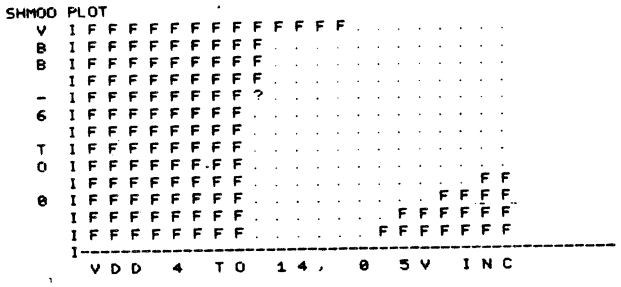


INTEL 16K CCD VBB VS VDD
SHMOO PLOT FOR MARCHING @ 25°C



INTEL 16K CCD VBB VS VDD
SHMOO PLOT FOR GALPAT @ 25°C

FIGURE 111: Shmoo Plots of V_{BB} vs V_{DD} using various test patterns; (A) Ping-Pong (B) Marching (C) Galpat Read write separate mode was used.



WALKING @ 25°C RMW
SHIFT PERIOD 1026N

FIGURE 112: Shmoo Plot of V_{BB} vs V_{DD} in the RMW mode, using the walking pattern.

(1) There should be a large number of independent programmable clock phases, up to ten or more. (e.g. 4 for clock phases, 1 for address RZ, 1 for data RZ, and 1 each for strobe, CS, CE, & RE.

(2) Each individual clock phase should have the provision to have its trailing edge programmed to occur in some later cycle other than the cycle containing the leading edge. The number of cycles between the leading and trailing edges of each clock should be programmable under software control.

(3) As pointed out earlier, the CCD memory may be sensitive to clock transition times. All clock phases, therefore, should have independently programmable transition times, independently programmed, because the memory may have different requirements for different clock phases.

(4) All the clock phases should have individually programmable clock high and clock low levels.

(5) The voltage level for address high, address low, data high and data low should be individually programmable.

(6) Provision to test devices have common Input/Output lines.

(7) Provision to test multiple input/output devices up to 9 inputs and 9 outputs. Each output of the device should have high and low threshold sensing.

(8) A maximum of twelve address lines is sufficient as this already allows accessing up to 4096 shift registers each of which could be anywhere from 32 bits to 16K bits.

(9) Test programs for CCD memory testing consist of both data patterns and test patterns, in contrast with RAM testing where only test patterns are used. Therefore, the test programs for CCD memories take more storage space than the corresponding test programs for RAM testing. Consequently, space allocations for test programs should be expanded.

(10) There should be at least six "nestable" loops available to allow flexible programming.

(11) The testers should be capable of performing three dimensional shmoo plots, e.g., plotting V_{BB} vs. V_{DD} with T_{ACC} as the third parameter, etc.

4.6 Microprocessors

The advent of the monolithic microprocessor has presented an exciting new dimension to designing data processing and communication systems. But they have presented both the user and supplier with a serious problem: That of testing. From a users viewpoint microprocessor testing, on an incoming basis, is difficult because every generic microprocessor is

different. Variations occur in device architecture, chip layout, data routing, the random logic nature of the μp, the instructional languages, the I/O capabilities, pin counts, bit sizes, bus organizations, fabrication processes, on chip interrelationship between functional blocks and relationships between software and hardware.

From a suppliers viewpoint there exist a myriad of possible applications, whether the system be controller or computer, over which the operation of the μp must be guaranteed and tested in a cost effective manner to maintain a competitive position in the marketplace.

At best μp testing is an evolutionary trial and error situation.

How does one adequately test a microprocessor chip (μp) to ensure that it has no shortcomings for all possible applications? A very difficult but crucial question in many suppliers and users minds. However, at present there is no answer or panacea that will solve the problem. What exists are several generalized guidelines to aid one in developing a viable test program for a μp. The purpose of this section is to briefly touch upon these guidelines in order to provide an awareness of what's involved in testing a μp and to "stimulate more thought on the subject".

4.61 Component or System

The first observation is that the μp cannot be tested using a philosophy similar to that for testing TTL, SSI and MSI component functions. Nor can the μp be viewed and tested as a combination of individual components. The μp is a monolithic system of untested parts and must be treated as such. Normally a system consists of pretested parts, but the constituent parts of a microprocessor cannot be tested. Thus a complete reorganization of the test engineers thought process is required in order to devise a meaningful test plan for these devices.

4.62 When is Testing Necessary?

The supplier must always test his product. However, as will be shown later, what types of testing he performs will be determined by feedback from his customers (i.e., from their field usage applications problems.)

For users there exists several sets of conditions depending on the quantity of parts procured as well as the maturity of the product. During the infancy of a given product or system (in its product life cycle curve) the quantity of units sold is small and the selling price is high. A significant percentage of the selling price is related to testing the product, i.e., it is given a lot of attention to assure complying with its performance limits. This condition holds true until the product has gained wide acceptance, yields are improved, competition becomes keen, and prices drop. Thus, user testing is not critical or necessary unless the application requires a product selection.

During the products growth and maturity cycles, the volume produced and shipped is high and the selling price is low. The care and testing the product received during its infancy is no longer possible. Consequently

shorter and "more effective tests have to be devised by the supplier to remain competitive. However, in this mode a greater possibility exists of product not being adequately tested and thus incoming inspection tests by the user is most definitely required.

Based on µp consumption, can a small user justify the cost of performing incoming inspection tests if all he ships are, say ten systems per month? For very small users of µps it just doesn't make economic sense to perform incoming inspection tests. His board tests are used in lieu of up incoming inspection tests to satisfy himself of the products performance.

For large users of µps, it is mandatory that incoming inspection testing be performed to ensure the validity of the product. As the prices of the µp drop and the quantities shipped increase, more testing will be required.

4.63 Test Requirements

Continuing with the concept developed in the previous section, the types of testing performed by the supplier and user vary radically because of their different requirements. The supplier would like to test every possible condition the µp will encounter. But such exhaustive testing is not practical. The supplier has to guarantee his product for all possible application conditions that exist. In order to do this he must use the best available worst case instruction sequence based on a combination of field application feedback and characterization test data. Thus, the supplier tests the µp "enough" to provide a statistical assurance that it will function properly for most applications. But is this enough for the user? Also, the supplier does not convey directly the usage problems encountered in the field by specific users to all users of the product.

Most suppliers are reluctant to give any information relating to how they test the product and what problems have been encountered. There is a lack of two way communication.

Large multi-application users of µps have the same problem as the supplier: Ensure that the product is tested for and can withstand all possible applications conditions. However, these users don't have the feedback from all µp users of their problems, nor do they have access to any characterization data. Thus they are forced to use their own limited field data and/or perform characterization testing themselves.

However, a large user or potential user of µps does have a lever - that being volume. Consequently the suppliers are more receptive to his demands and may provide the required information but only on a proprietary basis. If the volume of µps used is sufficiently large this category of user will do his own incoming inspection tests or have the supplier institute tests that utilize field usage information as well as results of the suppliers own characterization tests. This benefits all users of µps because, the supplier uses a single set of test conditions for his product. Thus, the tests generated by the supplier as a result of the feedback of the large users of the µp are instituted across

the board to all users. In this way the small user receives the feedback of field related problems, but in an indirect way.

Many small to medium users have a specific application for the µp. This requires an application oriented test program. They don't have the volume required for the vendor to do the testing in the manner which they require at a minimal cost nor can they get information from him relative to the best way to test the part. This category of users must have the assurance that the µp works properly in their particular applications. However, in order to meet their requirements, they may have to perform characterization testing as well as incoming inspection tests or have a qualified independent test laboratory do it for them.

The very small users of the µp need the same assurance of the products integrity as do the large users but because of their volume usage cannot justify testing the product. They rely on their board tests to verify the integrity of the µp.

4.64 Characterization and Incoming Inspection Testing

Characterization testing is the key to successful screening and inspection testing. With LSI devices, characterization plays the dominant role in the development of the incoming inspection test specifications and provides the information required by the user to determine how the LSI device matches his system requirements.

Electrical characterization testing can be defined as the thorough and exhaustive testing of a sample of a given device type through all practical combinations of supply voltages, temperature, timing conditions, parametric variations, instruction sequences, interrupts, and the like, to find its response under these conditions and to find the limits within which the device remains functional, i.e., defines the operating limits. From the user's viewpoint, the characterization testing is based on his need to define specific margins of design safety. From an IC suppliers viewpoint, the data gathered helps to establish obtainable and realistic specification limits and meaningful and economically viable shortened final test programs.

Characterization testing includes stringent functional testing using patterns or truth tables; instruction sequences, timing and parametric variations under temperature extremes. Worst case patterns and instruction sequences with supply and timing variations are applied to the device to expose it to as many failure modes as is practical and determine its performance under the most severe conditions.

A unique form of electrical characterization is the use of the OEM's System Constraints (supply voltages, instruction, timing conditions, operating temperatures, etc.) The test program/pattern parameters are held constant except one which is varied (or iterated) until that parameter results in a device failure (non-functionality). The last valid operating point is then noted and testing of another variable is begun. This process is repeated until all parameters are tested to failure for the entire sample population. This voluminous data must then be put into a form that is easy to interpret so that meaningful conclusions can be

reached. To this end various graphic displays, histograms, shmoo plots, and probability distributions are generated to make it easy to grasp the precise effects of temperature, supply voltage, or timing conditions on any of the part's key parameters.

Characterization testing is performed by the supplier, the user, or the independent test laboratory (ITL). Electrical characterization is performed prior to the release of a new product to establish data sheet limits, and outgoing supplier final test programs once the device is in the field or after field failures occur (backdoor characterization).

Supplier characterization is often oriented toward multiple user applications and can provide a corrective loop closure path in the process.

The differences between electrical characterization testing and incoming receiving inspection testing can be summarized as follows:

Characterization	Incoming Inspection
Sample of parts tested	Large volume of parts tested
Exhaustive & complex test sequence	Simple testing
Long test duration	Short test time; throughput is the key
High engineering content	Low or no engineering content
Requires ancillary data storage equipment: Line printers, hardcopy printouts, special routines, mass storage media, etc.	Requires automatic handlers
Collect vast amounts of data	No data required - Go-No-Go
Sophisticated flexible test system	Dedicated system
Normally done one time or as problems occur	Continuously performed

There are several distinct reasons why electrical characterization testing is important. First, the supplier himself, cannot thoroughly test the part for all possible failure modes and generally has not characterized it from an individual user's system viewpoint. Secondly, a user needs to know how a given part type will work in his system with many variables present and what design safety margin exists, if any. Thirdly, the user/supplier needs to know the actual operating limits of the part types. All data sheet specifications, unfortunately, are not arrived at by a complete study of the device or thorough analysis of the test data. Also, electrical characterization enables one to establish meaningful and viable test programs and it helps the user detect process changes which may affect his design safety margins.

Microprocessor testing is an evolutionary trial and error procedure relying heavily on user feedback. The supplier cannot completely characterize a product for all possible software and hardware conditions, (this would take 20 to 50 years to do so), and still have a product in the field. What he can do is devise his characterization tests based on chip layout design sensitivities (architectural), instruction sequence, relationship of software to hardware, data paths, applications feedback from customer field problems and the like. The results of these characterization tests are then used to generate final tests that consider only the sensitive parameters or instructions until modified by another worst case condition. Many suppliers, such as Intel and others, have ongoing continuous characterization programs in existence to detect worst case instruction sequences and test conditions, that continually update their final test programs. What is worst case one day is not worst case the next. For example, a µp that is used in a different way in the field than it has been used before, with a different ordering or execution of the instruction set, can lead to a failure or a device malfunction. This provides another worst case situation that brings to light new instruction or pattern sensitivities. When fedback to the supplier, he incorporates this test into his ongoing characterization as well as in his final test program.

A simple analogy is presented using the 1103 1K RAM. When the 1103 was first introduced, the supplier could not cost effectively final test the RAM for all possible worst case situations and pattern sensitivities when he introduced the product. What he did was put the product out in the field and the users (see the IEEE 1973 and 1974 Memory/LSI Testing Symposium records), themselves found the problems. These were the Bodeo effect, the Fourth Pattern, ^{T}WC problem and column disturb refresh. Then the supplier assimilated the users inputs to redesign the product and change the specification limits. Again, in order to be competitive in the marketplace the supplier could not incorporate all these worst case situations into his outgoing tests. Also the product was not specified properly initially because of the competitive nature of the marketplace in getting the product out first. However, the user definitely was interested in worst case situations. In fact, the large users of the 1103 are those who found its shortcomings, and since they bought large volumes of the product they had the suppliers attention. They had a lever and it resulted in the part being redesigned and different parameters being redefined via several iterations such that today you have good 1103 RAMs that are in widespread use. The feedback and learning that took place between the large users of the 1103 and the prime supplier now benefit all users of the 1103 in that the resultant changes were incorporated into the "standard" product that large and small users alike now procure. The same evolutionary trial and error procedure is happening with microprocessors. In effect, viable microprocessor test programs are yet to be developed.

The supplier, to be competitive in the marketplace, cannot test for all possible usage conditions. Consequently certain applications or usage conditions arise that may not be tested for. However, the user needs to know if the part can meet his particular requirements. The supplier has designed his final test program to combine as economically as possible

his characterization test program results with field applications problem feedback. Things such as pattern sensitivity, instruction sensitivity, interrupts, variation of the supply voltages and timing conditions should be tested extensively during the characterization of the product and then only the sensitive parameters/instructions tested during the suppliers outgoing final tests and the users incoming inspection tests.

4.64 Microprocessor Test Philosophy

In order to devise a meaningful test philosophy the test engineer must view the µp as a system (rather than a combination of MSI components) and orient his thinking appropriately. He must be familiar with software as well as hardware. In fact the software development is the critical phase in µp test program generation.

Up to the present we have used the word testing in general terms. The physical testing of a µp is the easy part of the task. The overall test philosophy or test program development and instruction sequence generation are the critical tasks of "testing a microprocessor". There are four basic elements to developing a µp test program.

These are:

1. Develop a test plan
2. Generate an instruction sequence
3. Generate a bit pattern corresponding to the instruction sequence
4. Test the part

Items 1 and 2 are the difficult elements. They are the crux of testing a µp. Once these are defined and generated, then 3 and 4 follow automatically and almost mechanically.

Of prime importance in µp test program generation is the test plan development phase. How will the device be tested? What is the underlying goal which I hope to accomplish by this test? What are my constraints (economical and otherwise)? Is the testing to be oriented toward a particular application or must it be general (and thus harder to develop) to cover all applications? These are questions to be answered during this phase of the program generation.

Generating an instruction sequence is the crux of the entire matter of µp testing. On the surface it is easy to generate an instruction sequence at will. However, the rationale of why a particular instruction sequence was chosen and the resultant effectivity and validity of that instruction sequence and not another in testing a device is why this phase of µp test program generation is so important.

4.66 Basic Microprocessor Test Methods

Five methods have been developed for generating the instruction sequence and subsequently testing the μp.

These are:

1. The self Diagnostic Method
2. The Comparison Method
3. The Algorithmic Pattern Generation Method
4. The Stored Response Method
    A. Emulation
    B. Simulation
5. Modular Sensorialization

The advantages and disadvantages of each of these methods are summarized in Table 7. However, it should be noted that in essence each of these methods is a variation of the stored response method. For example, the comparison method stores the instruction set in the "known good μp". The algorithmic pattern generation technique generates a sophisticated instruction sequence via the pattern generator (through software).

Modular Sensorialization, a phrase coined by Macrodata is used in conjunction with an algorithmic pattern generator to test μps. Here the functional test pattern is partitioned into simple short instruction sequences which are repeated and modified under control of an algorithmic pattern generator.

The present date topological designs show that a μp can be partitioned into several modules, overlapped or non-overlapped, from both its physical layout and logic structure -- such as the program counter, arithmetic logic unit (ALU), accumulator, stack pointer, etc. Each module is able to communicate with the outside world through a minimal interaction between modules. As a result the μp can be treated, in principle, as building blocks of logic modules in an orderly constructed manner.

These modules, at least internally are relatively isolated from one another thus, any physical problems which occur causing failures and sensitivities will more likely be contained within the module.

After partitioning, μp testing can proceed from one module to another. In normal practice one can initialize the μp to a known condition and then execute the test commencing with the first module. This should cover the execution of certain instructions in the microprocessor language. Then, the same procedure applies to the second module and another set of μp instructions are executed. The exact procedure is then applied to each module in turn which exercises the μp instructions

until all modules, in conjunction with all μp instructions, are fully tested. This is modular sensorialization.

The fallacies are: The layout of functional modules in a μp sometimes does not follow the block diagram, algorithmic pattern generation is a difficult technique with limited exposure.

The affects of interconnection of modules via on chip buses to each other and the interrelationship of all instructions each to another is not considered with this approach. How are worst case patterns for each module determined?

Table 7

Basic Microprocessor Test Methods

Test Method	Description	Summary of Characteristics
1. Self-Diagnostic	Load "worst case" instruction set into μp memory. Then place μp in intended operating environment.	Tests •Limited Diagnostic (Functional Only) 1) Error Negation 2) Timing Varies •Easy to Implement •Low Cost •Applications Oriented •Small User Oriented
2. Comparison	Compares DUT with known good device. Input data are sent to both μps simultaneously but with separate drivers. Output data are monitored from both devices and considered valid when data coincidence occurs.	•Limitations 1) Functional Tests only 2) No Parametric Measurements 3) Dependence on Known "Good" Device 4) Identical Faults Between Known & Unknown Device Undetected. 5) Inflexibility to Change Input Test Pattern 6) Synchronization Between Good μp and DUT •Utilize Real Time Cycle Response Testing •Production Oriented •Easy to Implement •Low Cost
3. Algorithmic Pattern Generation	All instructions stored in high speed local buffer memory. Depending on expected output some instructions go into local buffer while rest are generated by high	•Limitations: 1) Partial functional testing 2) Personality Board 3) Requires that test engineer understand μp architecture and application.

	Test Method	Description	Summary of Characteristics
3.	Algorithmic Pattern Generation (continued)	speed pattern generator. All instructions when addressed in local buffer and sent to µp are verified in proper sequence.	4) Lack of parametric or µp dynamic tests. 5) Engineer has full control over test program •Low Cost •Flexible Programming •Allows Multiple Fault Diagnosis •Engineer has full control over test program •Harder to implement than 1 or 2 •Has sophisticated test system
4.	Stored Response	An emulation or simulation program is kept in bulk memory and then applied to DUT to generate output data response. •Emulation: 1) Diagnostic program loaded into test system and translated into 1's and 0's and applied to reference device. 2) Reference device tested with comprehensive set of diagnostic instructions 3) Outputs of reference devices recorded in memory 4) Truth table developed in user/machine language 5) Test sequence applied to DUT •Simulation: 1) Use RAM or PROM to simulate sequence of operation of µp by storing predefined instruction sequence 2) Simulated outputs sampled and correlated to input patterns 3) Stored in buffer or on disc 4) Transfer pattern to buffer to DUT	Tests: •Functional, Parametric, and Dynamic •Extensive Engineering and Evaluation Modes •Multiplexed Operation •Uses 2 Steps: Pattern Identification and Test Execution •Emulation: 1) Easy to implement 2) Uses Reference Device 3) Tests µp with its Operating Instructions •Simulation: 1) Harder to Implement 2) Ease of Programming 3) Flexibility to Change Program 4) High Hardware Cost for Super Buffer & Added PROMs & Pattern Generator 5) Depends on Known Good Device 6) Does Not Duplicate Microprocessor Environment 7) Simulation is Built by Means of Software 8) Requires Detailed Understanding of µp 9) Requires High Level Language •Highest Cost •Hardest to Implement •Sophisticated Test System Required

Test Method	Description	Summary of Characteristics
5. Modular Sensorialization	Divide µp into recognizable functional modules and test each separately	Advantages: •Low Cost •Requires Pattern Generator •No Gold or Known Good Device •Input/Output Responses are Generated by Pattern Generator Disadvantages: •Requires Knowledge of µp Structure and Pattern Generator •Doesn't Test Interaction Between Modules and Instructions

4.67 Microprocessor Test Results

µps exhibit the following types of test problems:

- Pattern sensitivity
- Interrupt problems
  - Trigger on wrong priorities for multilevel interrupt
  - Lose Data
- Failure to execute instruction and/or interrupt
- Loss of carry and bits during recirculation of data
- Mnemonic sensitivity
- Instruction and instruction sequence sensitivity
- Loss of data
- High leakage current
- Slow access time

Tests on several different microprocessors have revealed the following:

1) Microprocessors must be initialized and synchronized prior to the onset of testing because not all microprocessors power up to a known state, or within a specified number of clock cycles (most microprocessors require varying numbers of micro-cycles for different instructions, requiring synchronization of the µp).

2) Some pattern sensitivity has been located with on chip RAM.

3) µps are voltage sensitive.

4) Instruction and instruction sequence sensitivity exists in most µps. Certain groupings of instructions, when repetitively cycled through the µp and each successive loop resulted in more failures recorded on a shmoo plot. Thus, there is a definite relationship between software and hardware.

5) Most failures have been attributed to mask defects.

6) µp testing requires finding worst case instruction sequences and combining these with min./max. power supply and timing conditions to obtain viable test plan.

One thing is for certain, there is no best way or standard way of testing a µp. This is yet to be developed. For you as users, the best means of testing the µp is by simulating the system -- i.e., using the instructions, supply voltage and timing conditions as they are used in your system.

4.7 Applications Aspects

4.71 IC Reliability

IC Reliability is a composite of design, wafer process, assembly/package, screening and testing factors.

There are more than half a dozen reasons why ICs fail. Figure 113 illustrates to what extent each major failure mode contributes to IC mortalities. Since the distribution is normalized, it does not take into account the small percentage of failures caused by anomalous defects.

What factors must be considered in assessing component reliability? The answer to this question depends on the user's needs and may be as simple as "calculate the failure rate on the basis of life test data" or as complex as "access the reliability based on all factors from design to complex reliability testing and analysis."

In order to assure oneself that the soft and catastrophic electrical failures, as well as mechanical (package related) defects are removed from a population of parts prior to installation in pc boards, many people have turned to reliability improvement programs which are based on the military/aerospace screening specifications. Reliability improvement programs ensure that the parts used in a system are stable and contain no inherent defects or sensitivities by combining the proper electrical and environmental tests for a given application.

Testing or stressing a component does not make it more reliable. On the contrary reliability must be an inherent quality -- it is a function of the process being used to fabricate the device. As a result, the more mature components' technologies tend to produce the more reliable devices.

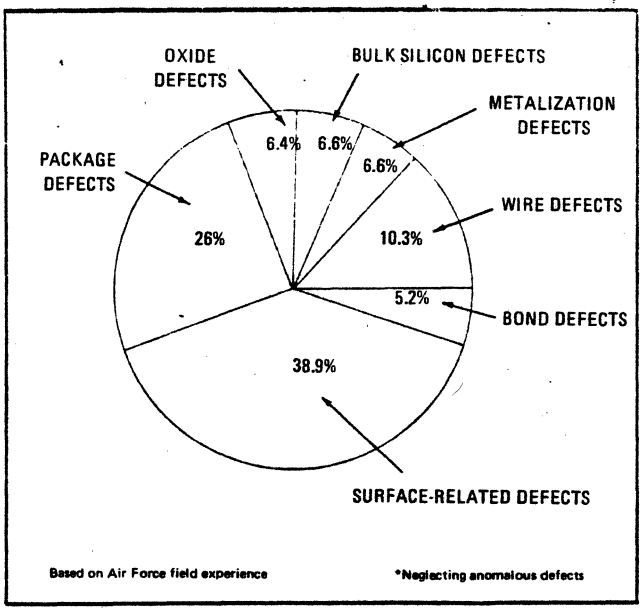


Figure 113: Normalized Failure Mode Distribution for ICs

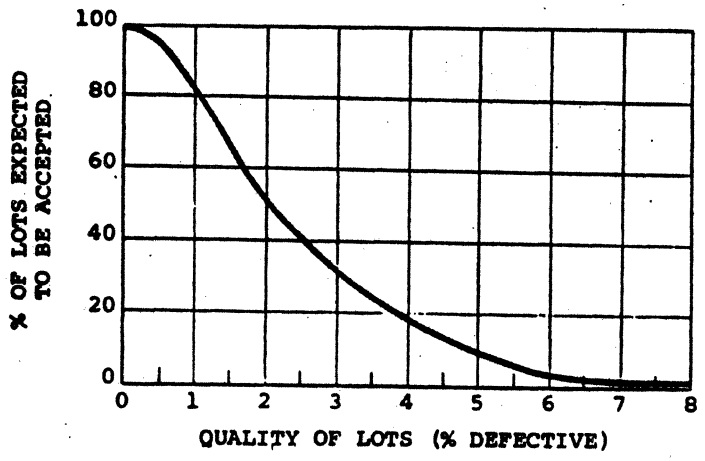


Figure 114: How many duds? Sample testing to a 0.65 percent Acceptable Quality Level generally means that 95 percent of lots with 0.65 percent defective devices will be accepted. Each defective device that slips past incoming inspection leads to expensive troubleshooting and rework.

The yields of a mature process are also inclined to be higher, but high yields do not necessarily mean high reliability.

The extent to which devices are screened and the severity of the screens depend on the type of component, as well as the end application. As a rule, passive components tend to have lower failure rates than active ones, and simple ICs generally fare better than complex ones. Needless to say, components being used in an aerospace program are subjected to far tighter screening than those going into a television set. However, standard military test procedures are commonly employed to screen commercial, as well as industrial devices.

Reliability and Quality

The words "reliability" and "quality" are often used interchangeably as though they were identical facets of a product's merit, but, they are different. Definitions for quality and reliability are often the subject of controversy, however the definitions given here will fulfill the needs of this discussion.

Quality pertains to the population of faulty devices among the good ones as they arrive at the user's plant. Or, in another view, quality is related to the number of faulty devices that escape detection at the supplier's plant. The supplier's procedure of testing outgoing parts on a sample basis monitors the success of reducing the number of faulty ICs that escape detection by 100 percent testing.

With LSI devices such as microprocessors there is not a clean cut distinction between reliability and quality because of the complexity of these devices. Reliability is a measure of a parts performance after it has been operating in a given socket for a period of time. It measures how long the part will last. Quality, however, is considered to be how well a given lot of units is prepared for a customer from the standpoint of meeting his parametric and functional requirements. This is especially true with microprocessors since the supplier cannot adequately test the devices for all possible usage conditions. As such quality escapes occur at the outgoing test point which manifest themselves as system failures. This is a quality and not reliability problem.

The term AQL is used in quality control to specify the percentage of parts in a lot that can be defective and still have a 95 percent probability of lot acceptance. As the AQL figure decreases, the sampling plan makes it more difficult for bad parts to escape detection, thus upgrading the average quality level of the shipments.

For practical purposes of discussion, 0.65 percent AQL means that a lot containing 0.65 percent defective parts will have a 95 percent chance of being accepted; however, as shown in Figure 114, it also could mean a lot with 2.09 percent defectives will be accepted 50 percent of the time and lots with 4.8 percent defectives will be accepted 10 percent of the time.

Defective devices that slip through will be costly to find and replace later on. A customer who buys ICs at a 1 percent AQL could receive lots with varying percentages of defective parts. For ease in relating an example, assume that the customer receives a lot that just happens to be 1 percent defective. If he places 10 on a board, then on the average, one out of 10 boards will be unacceptable, or if he chooses to put 50 on a board only one out of two will be good. Putting 100 devices on a board virtually assures that none will be satisfactory. Clearly, large board populations lead to expensive troubleshooting and rework costs: the earlier the defectives are culled out the better.

Anyone using the AQL procedure must accept the premise that defectives may exist in an accepted lot. The only way to separate and eliminate defectives effectively while still accepting good units, is 100 percent sorting.

In most instances, the number of rejects accepted at 0.65 percent AQL is sufficient to justify 100 percent inspection for purchasers of IC components. In fact, if we study shipments made by suppliers who use AQL and other sampling procedures, we find that the number of rejects shipped is far from insignificant.

Consider the company that uses 10,000 devices a month, at 15 cents each or $1,500 per month. Typically, a company tries to "catch" defective components in normal board and system checkout operations. With luck, only 3 percent of the mounted and soldered devices will fail at an approximate cost of $10 to locate and $3 to replace each failed device. That's $3,900 (300 failed) and an additional 2 percent probably will fail in the field. This is not only expensive but damaging to the company's reputation. Locating and repairing of approximately 200 field failures, at an average of $50 a call, amounts to another $10,000. By the time all the rejects are caught, it has cost the company about $14,000 -- almost ten times the original monthly lot purchase price. Stated another way, the 15 cent devices have cost about $1.65 each, or probably $4 to $5 if used in military equipment.

Despite reasonable quality control at the semiconductor suppliers plant, a bonding problem might go through outgoing tests undetected. Failures showing up at the board or system test level cause test and rework expenses to soar, but the real problem is the stoppage of the production line. The only real answer is 100 percent testing at the incoming inspection station.

Characteristic Reliability of Unscreened Devices

The type of materials and method of assembly used are most important to the reliability of a part. Reliability cannot be tested into a part, however, reliability can be tested into populations. There are tests which will subject the IC to stresses beyond those in actual use. Such tests can eliminate most short-life parts.

Stress tests will accelerate the time to failure of weak parts, allowing the population of parts shipped to demonstrate a higher reliability in use. Considerable data exists to show what stress levels a properly manufactured circuit, utilizing a certain technology, should be capable of withstanding. The data cover vibration, mechanical shock, thermal shock, constant acceleration, moisture resistance, etc. In addition, it has been established that a properly manufactured circuit should be capable of storage or operation within rated conditions for thousands of hours without significant degradation.

All semiconductor devices exhibit a bathtub failure curve as shown in Figure 115. Initially, the device failure rate will be relatively high as "mavericks" (infant mortalities), not representative of the main population, fail. These failures are usually associated with one or more manufacturing defects. The failure rate then declines to a farily constant value which is representative of the main population where it remains for a period of hundreds of thousands to millions of hours depending upon temperature, applied voltage, circuit complexity and other factors. Farther out on the time scale, the failure rate can be expected to increase as devices fail of "old age" (as devices wear out both physically and electrically.) The curve for particular semiconductor types will be similar in shape with values that are specific for the device.

Operating time is usually expressed in hours, and failure rate in percent per thousand hours. Typical semiconductor failure rates as a function of operating time for various temperatures are shown (Figure 115). At higher temperatures, the "infant mortality" slope is greater and a stable population is achieved in a shorter time.

The temperatures cited (Figure 115) are some of those commonly employed for semiconductor burn-in. These curves show high temperature burn-in as an effective means of weeding out infant mortalities.

"Dead on arrivals" are parts not operating to specification when received from the supplier, whereas infant mortalities are operational upon receipt but fail over a short period of time.

Associated with each area of the curve are specific failure mechanisms. Table 8 lists some of the more common mechanisms along with the associated thermal activation energy (defined later). These failure mechanisms are now discussed.

4.72 Discussion of LSI Failure Modes

Failure mechanisms for SSI/MSI TTL, and linear ICs have been discussed and investigated at great length. Table 8 summarizes the failure modes associated with these devices. As such a reiteration of these will not be presented here. Instead we will concern ourselves with the failure modes peculiar to LSI devices and to MOS and bipolar technologies.

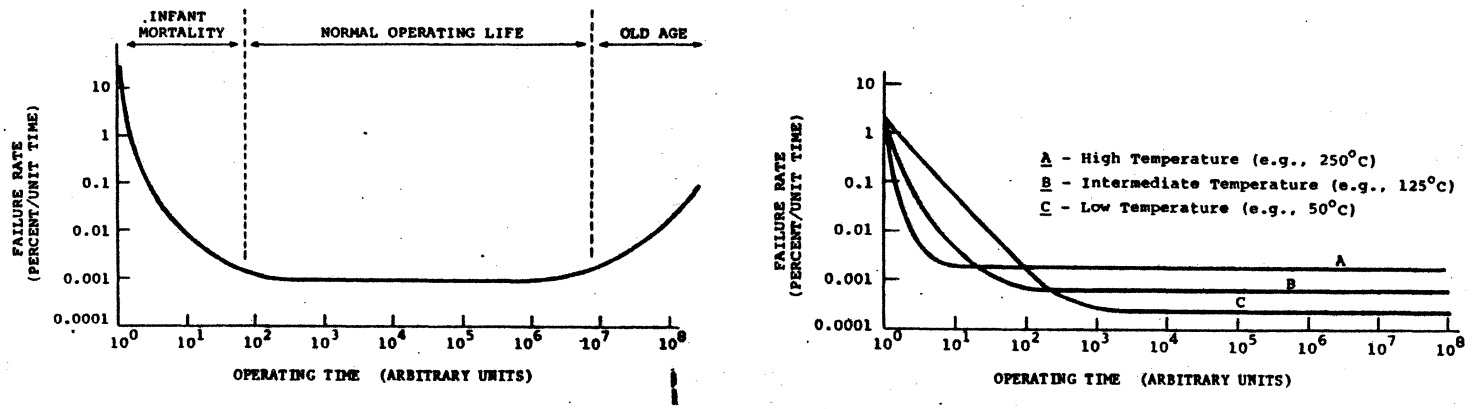


Figure 115: Bathtub Curve

TIME-DEPENDENT FAILURE MECHANISMS IN SILICON SEMICONDUCTOR DEVICES

DEVICE ASSOCIATION	PROCESS	RELEVANT FACTORS	ACCELERATING FACTORS	ACCELERATION (E_A APPARENT ACTIVATION ENERGY)
SILICON OXIDE AND SILICON SILICON OXIDE INTERFACE	SURFACE CHARGE ACCUMULATION	MOBILE IONS, V, T	T	BIPOLAR E_A 1.0 - 1.05 eV MOS E_A 1.2 - 1.35 eV
	DIELECTRIC BREAKDOWN	E, T	E	
	CHARGE INJECTION	E, T, Q_{SS}	E, T	E_A 1.3 eV (SLOW TRAPPING)
METALLIZATION	ELECTROMIGRATION	T, J, A, GRADIENTS OF T AND J, GRAIN SIZE	T, J	E_A 0.5 - 1.2 eV J^n (n 1 to 4)
	CORROSION CHEMICAL GALVANIC ELECTROLYTIC	CONTAMINATION HUMIDITY (H) V, T	H, V, T	STRONG H EFFECT E_A=0.3 - 0.6 eV (FOR ELECTROLYSIS) V MAY HAVE THRESHOLDS
	CONTACT DEGRADATION	T, METALS IMPURITIES	VARIED	
BONDS AND OTHER MECHANICAL INTERFACES	INTERMETALLIC GROWTH	T, IMPURITIES, BOND STRENGTH	T	Al-Au E_A 1.0 - 1.05 eV
	FATIGUE	TEMPERATURE CYCLING, BOND STRENGTH	T EXTREMES IN CYCLING	
HERMETICITY	SEAL LEAKS	PRESSURE DIFFERENTIAL ATMOSPHERE	PRESSURE	

Table 8

V VOLTAGE E ELECTRIC FIELD A AREA
T TEMPERATURE J CURRENT DENSITY H HUMIDITY

LSI devices have all the reliability problems associated with discrete semiconductors, plus others. The smaller geometries associated with LSI circuits are reported to result in increased susceptibility to a number of degradation mechanisms. Larger area chips are required, making the devices more prone to defects inherent in the semiconductor materials and increasing the probability and number of process defects, such as pin holes and metallization faults. Larger packages are required (up to 64 external leads) to assemble the LSI devices, thereby introducing more bonds and increasing the probability of bond failure. The larger packages are more difficult to hermetically seal, increasing the susceptibility to leaks.

Unlike the transistor, the LSI device must be tested as a system, making the testing approach more complex and less thorough than with discrete components. Interaction between adjacent active elements of the LSI circuit can give rise to an unwanted parasitic transistor action. Coupled capacitance effects can, under various combinations of logic patterns, cause an LSI device to lose stored information -- a phenomenon called pattern sensitivity.

The complexity of LSI devices makes reliability testing and assessment more difficult. Burn-in screening for example, one of the most effective screen tests for integrated circuits, becomes itself a complex problem when designing the driving circuitry needed to stress each element of the LSI device. Because of the small geometries and, hence, the large numbers of elements and functional parameters of LSI circuits, failure analysis is much more complex than with discrete devices; however, experience has shown that systems using LSI devices are more reliable than systems using discrete components. One contributing factor is the general improvement in semiconductors in recent years.

Most failure modes observed on lower complexity ICs are also observed in LSI circuits. It has been shown that for bipolar ICs, equal numbers of assembly or package related failures and die or chip related failures exist; however, a different package die failure mode ratio for LSI circuits has been reported. These findings show that approximately 45% of MOS LSI failures are due to chip-related failures and only 28% were due to package and assembly related failures; 20% of the remaining failures were attributed to handling and 12% were due to a variety of causes. Of the 45% chip related failures, 20% were attributed to oxide faults compared with 6-7% for other ICs.

Unlike bipolar ICs, the oxide in an MOS circuit performs a dual function: It protects the semiconductor material and determines the operating parameters of the MOS circuit. It is this difference that gives a different character to the physics of failure and failure distribution of MOS LSI circuits.

MOS/Bipolar Chip Related Failure Modes

There are a number of fundamental differences between MOS and bipolar silicon devices which impact integrated circuit reliability. The principal ways in which digital MOS ICs differ from digital bipolar ICs relative

to reliability is in the higher substrate resistivity, the use of higher applied voltages, and in the importance of the properties of the gate oxide of MOS devices.

MOS fabrication technology differs from bipolar technology in having greater process simplicity. Accordingly, it is easier to attain higher chip complexity with MOS, and thus higher gate-to-pin ratios can be attained. Since wire bond failures are a significant factor in limiting the reliability of small-scale integrated circuits, MOS thus offers the possibility of significant improvements in equipment reliability by reducing the number of wire bonds and external interconnections. Moreover, MOS offers the possibility of lower power dissipation per function, which in turn improves device reliability by producing lower chip temperatures during operation. In typical bipolar ICs (TTL), device dissipation is significant. By contrast, dissipation in MOS devices such as CMOS and SOS CMOS is quite low.

MOS also has an advantage relative to bipolar devices in that the high impedance of MOS devices does not result in high current densities in the metal interconnections, and thus electromigration (current-induced mass transport) is not a common problem in MOS devices. Also, high current density problems at metal-silicon contacts are less frequent. The high impedance of MOS devices also makes multilevel interconnections feasible in complex arrays without significantly compromising circuit properties. Diffused crossunders in the single-crystal silicon are effective, and if another level of interconnections in addition to that provided by the metallization layer is required. Polycrystalline silicon, deposited as part of the silicon-gate process, is quite effective as an interconnection level. By contrast, an additional level of interconnections in bipolar arrays means use of metal-over-metal crossovers, which requires additional technology and introduces possible new failure mechanisms.

Since localized defects in silicon are a factor in integrated circuit reliability, one advantage of MOS compared to bipolar circuits is that no epitaxial layer is required for conventional monolithic MOS devices. MOS devices are thus fabricated in silicon of better crystallographic perfection, with no possibility of stacking faults, or of epitaxial spikes which cause device problems and damage the masks used for photolithography. Finally, since MOS processing is simpler than bipolar processing, and requires less steps, the possibility of manufacturing errors which adversely affect reliability is thus lower. However, bipolar technology is very mature and a relatively debugged process.

MOS ICs use many of the same materials and processes as bipolar ICs and small-signal transistors. Accordingly, improvements in silicon materials, oxidation, photolithgraphy, diffusion, metallization, passivation and plastic encapsulation, and also in device physics, process control, and electrical characterization have resulted in substantial improvements in the reliability of both types of integrated circuits.

Many types of MOS devices are being produced at present. These differ in types of active devices, in gate dielectric and gate metallization used, and in processes, designs, circuits and packaging.

Initially introduced commercial MOS ICs were based on high-voltage p-channel enhancement-mode transistors. Lower voltage types and complementary MOS devices were subsequently introduced. In this report the reliability of the most commonly used types of MOS integrated circuits is discussed, and specific examples of the effects of device construction features and operating conditions on device reliability are given. Construction features of importance are:

Active Devices

P-Channel (High V_T)
P-Channel (Low V_T)
Complementary
N-Channel
Depletion-Mode
Charge-Coupled Devices

Dielectric

SiO_2
SiO_2-PSG
SiO_2 (Cl)
SiO_2-Si_3N_4
SiO_2-Al_2O_3
Si on Sapphire

Gates

Al
Polycrystalline Si
Floating

Circuit

Input Protection
Static
Dynamic

Other factors of importance in MOS ICs include device and design features (dielectric thickness and quality, design rules, device complexity, in-process controls), specifications (maximum and minimum operating voltages, operating temperature range), electrical testing (tests performed on the wafer and on packaged devices), screening (amount of burn-in or other screens applied), and packaging (hermetic-sealed conventional package, frit-sealed package, plastic encapsulated device). Operating conditions of importance include chip temperature, applied voltage, voltage transients, moisture content of the ambient, and exact circuit usage.

MOS Failure Modes

Since many processing steps, materials, and construction features are common to both MOS and bipolar ICs, many of the possible failure mechanisms which have been reported apply to both types of devices. For example, passivation, chip-to-substrate bonding, wire bonding, and package sealing or molding procedures are similar for MOS and for bipolar ICs.

MOS failure modes can be classified into the categories of shorts, opens and degradations. Shorts are most commonly due to dielectric failure of the gate (thin) oxide. Dendrite formation in gold-metallized devices can also result in resistive shorts. Electrical opens may be due to microcracks in the metallization at topographic steps, to photolithography problems, to corrosion of metallization, to fusion of metal due to overstress, or to open wire bonds. Degradation-type effects are attributable to the motion of ions (such as Na+) in the SiO_2, or to surface charge spreading effects and consequent inversion.

4.721 Chip Related Failure Causes

Chip related failure causes for LSI devices are summarized in Table 9 for both bipolar and MOS devices and their frequency of occurrence. These failure causes may yield any failure mode depending on when and where on the chip they occur -- loss of data, etc.

Table 9

Chip Related Failure Causes and
Related Frequency of Occurrence

Cause	PMOS	NMOS	Bipolar
Photolithographic defects	6	6	10
Oxide defects	6	10	4
Oxide/junction contaminants	6	10	2
Metallization faults	6	4	8
Diffusion defects	8	10	6
Mechanical defects in the chip	6	6	10
Design defects	8	10	6

10 = high frequency of occurence

Photolithographic defects are caused by poor quality working plates (causing tears, pin holes and metal defects), poor mask registration and misalignment and the like. These types of defects can be rectified by use of better quality plates, redundant masking techniques, and self aligning masking techniques. Implementing these on SSI and MSI devices increases the cost but doesn't reduce the number of defects significantly. But it does for microprocessors and other LSI devices.

Since MOS is a surface oriented process, the principal MOS failure mechanisms are due to motion of charge in or on oxides, and shorts through gate oxides. These oxide faults include:

1. Excessively thin oxide. The oxide layer is too thin to withstand normal operating voltages and will cause breakdown across the oxide, destroying the MOS transistor due to either localized breakdown at defects or intrinsic breakdown at input circuits. Less severe cases of excessively thin oxide may contribute to device leakage.

   Breakdown at inputs is principally attributable to overstress, due to static electricity discharges of sufficiently high energy. While virtually all MOS ICs contain an input protection circuit, such circuits vary considerably in design, principle of operation, and effectiveness. Susceptibility of silicon devices to static electricity effects is not unique to MOS circuits, and has also been reported to occur with bipolar integrated circuits.

2. Slow trapping represents charge accumulation at the $Si-SIO_2$ (see Figure 116) interface. In P-Channel devices, the crystal orientation of the substrate material (silicon) is usually < 111 > and positive charges accumulate at the interface during the application of negative bias on the polysilicon gate. This can cause a threshold voltage (V_{TH}) shift at the interface of approximately 1.0V after exposure to 250°C for a period of 30 minutes. The original threshold voltage for this material is in the 3 to 4 volt range). The crystal orientation of N-channel devices, such as the 2107 4K RAM is < 100 > which is much less prone to this drift. Under the same conditions, V_{TH} will drift only about 0.01 volt. This failure mechanism is defined as a wearout failure and with an activation energy of leV is readily detected by High Temperature Bias Testing.

3. Polarization causes threshold voltage drift by the presence of polarizable molecules in the gate oxide region. The most common cause is the presence of phosphorous in the gate oxide material.

4. Contamination. The presence of foreign materials in the oxide layer may cause leakage or localized charge concentration in the oxide layer.

   Several forms of alkali ion migration are possible, including the commonly reported transverse Na+ ion movement in an electric field at an elevated temperature, and lateral Na+ ion movement followed by transverse movement. The net result of alkali ion migration is to increase the threshold voltage of p-channel transistors, decrease the threshold of n-channel transistors, or to decrease the field inversion voltage of n-type regions. Contamination can be detected by High Temperature Bias Testing. The silicon gate process, however, allows the device to be

subjected to high temperature gettering which "cleans" the oxide and prevents further contamination during subsequent processing.

5. The effect of surface charge phenomena can be observed with suitable test patterns. Charge can spread across the surface of a device and create parasitic transistors or leakage paths. The problem is aggravated by mobile ions on the die surface. Generally, ultra-clean processing combined with raising the field threshold (by process techniques) will prevent this problem. The phenomenon can be detected by high temperature bias testing although the temperature dependence can vary.

6. Pin holes or cracks cause the same effects as excessively thin oxide. Oxide rupture has been observed in MOS devices in thin (gate) oxide areas. 1000A° thick silicon dioxide (SiO_2) has a normal oxide breakdown voltage of approximately 95 volts. However, localized partial pin holes result in lower breakdown voltage. These weak spots also show significant degradations under temperature bias conditions which eventually result in a short circuit. There are two types of pin holes: from "top-down" as a result of partial etching, and "bottom-up" which is always at the field oxidegate oxide interface. Process improvements have been revised to significantly improve these problems. "Top-down" pin holes are mostly eliminated by double masking (two layers of photoresist) the contact hold etching. "Bottom-up" weak oxides are greatly reduced by lower substrate defects (mostly dislocations) and HCl oxide (self-cleaning) growing process.

   The above process improvements mostly eliminated the oxide rupture occurence on internal circuitry; however, circuits in direct contact (I/Os) with the module pins are still susceptible to ruptures due to static charges (protective devices are not 100% effective). Functional problems caused by oxide rupture are dependent on the ruptured location. Experimental data shows the highest occurrence is in large (W/L ratio) devices, usually in input buffer or decoder circuits. This can be explained with the coincidence of longer thin-to-thick oxide interface and higher power stress. Most of the "whole" or "half-chip" failures are results of oxide ruptures.

The above failure mechanisms may be eliminated in a number of ways. The most effective method is to ensure contamination-free processing of the wafers. This precludes the accidental introduction of foreign materials, i.e., materials not belonging to a given process step. Polarization is prevented by eliminating the use of phosphorous in the gate oxide growth step. Tight process controls will eliminate excessively thin oxide, pin holes or cracks. In addition, a high voltage cell stress test performed during manufacture on all devices will eliminate oxide breakdown failures in shipped parts.

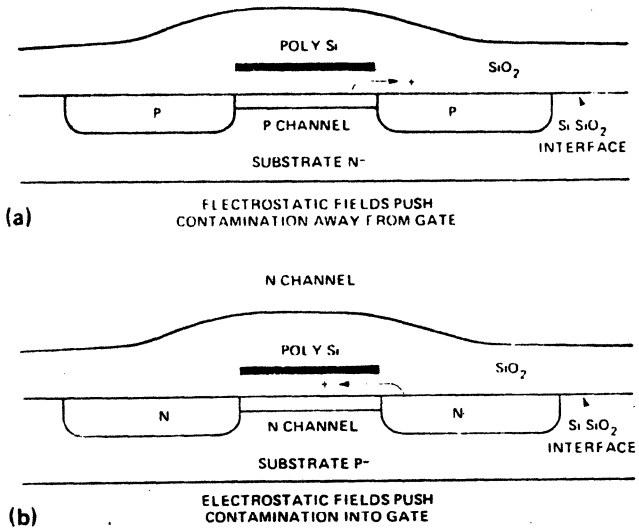


Figure 116: Effect of Contamination

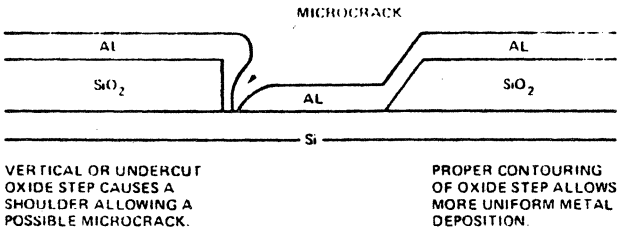
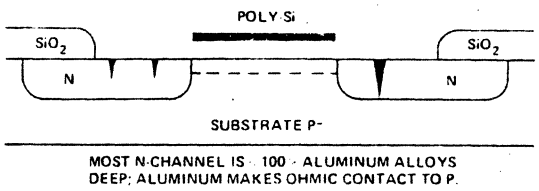
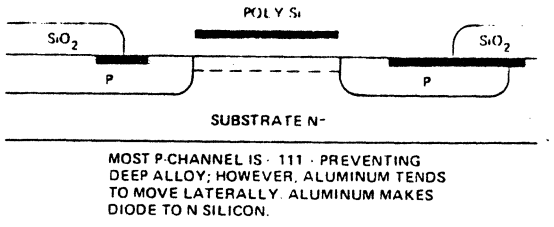


Figure 117: Microcrack Formation



(a)



(b)

Figure 118: Effect of Over Alloying

Metallization Faults

Metallization faults (defects relating to metal conductor paths on the semiconductor die) are another cause of semiconductor failure and fall into four categories:

1. Contamination. Contamination under metal can be caused by improper cleaning of die prior to metallization, contaminated metal, improper vacuum in the deposition chamber, humidity or other contaminants introduced prior to package seal.

2. Electromigration. Electromigration is activated by excess current density in conductors ($>2x10^5$ A/cm^2 for aluminum). This causes the conductor material to migrate, especially in the thinner part of the conductor and eventually causes the conductor to separate.

   Al migration normally considered in bipolar circuit reliability is not critical due to low currents and low junction temperature unless weak points exist in the power busses. Process improvements are "sloped-etching" in Al gate process, "re-flowed Vapox" in Si-gate to improve edge coverage. Either "hot" aluminum deposition (large grain) or "co-deposited aluminum" (Si, Cu, etc.) can be used to improve migration characteristics.

3. Microcracks. Microcracks are caused by sharp edges at the oxide steps (see Figure 117) which, due to either insufficient edge coverage or adhesive problems), in turn cause a shadowing effect at the bottom of the oxide step resulting in a crack in the metallization as shown. In order to prevent problems the basic process must be such that all steps are contoured and appropriate metal deposition techniques are employed. This random failure mechanism is readily detected by thermal cycling or operating life.

   Aluminum metal corrosion in ICs has been the subject of considerable investigation. It has been shown that low-temperature-deposited glass-like inorganic passivation materials can be very effective in reducing the possibility of Al corrosion. Opens in Al have been shown to principally occur at cracks or pin holes in passivation glass layers and specific techniques for detecting and for minimizing occurrence of such localized defects in the integrity of passivated glass layers have been developed.

4. Contact failures can be of several types. Poor cleaning prior to metallization can cause marginal adhesion to silicon and results in opens during life test. Overalloying results in the migration of metal through the semiconductor junction causing short circuits in the devices, and is more serious in N-channel devices and is illustrated in Figure 118a. Suitable processing precautions can prevent this failure mechanism. High temperature operating life is the most applicable life test although high temperature bake is also effective.

Contamination and overalloying are prevented by tight process control and rigid quality control inspections as well as extensive testing. Electromigration is eliminated by keeping the current density well below $5x10^5$ A/cm^2 (for passivated circuits) of cross-sectional conductor area and microcrack formation is prevented by contouring the oxide steps.

Surface Defects and Foreign Materials

Surface defects and foreign materials are caused by improper quality control during manufacture and are commonly due to improper handling of materials during assembly. Visual inspections are the best preventative for these problems.

Faulty Diffusions

Faulty diffusions and crystal imperfections are very rare in most MOS devices since the failure mechanisms will almost always be detected during classification tests as a catastrophic or degradation failure. Since MOS devices are normally much more functionally complex than bipolar circuits, more extensive testing is performed, thus these failure modes are seldom experienced by MOS device users.

Memory/Microprocessor Failure Modes

Failure modes of LSI devices (memories, microprocessors and the like) are divided into two major categories:

Catastrophic failures
Soft failures

The catastrophic failures can be attributed to the following (as discussed previously):

Oxide rupture

Interruption of Al lines

Wire bond failures

Corrosion due to contamination (such as trapped moisture in CERDIP due to devitrification of glass material).

Soft failures being hard to detect, can be simply out of specification conditions at a certain operating condition: In some instances soft failures can't be reproduced. For example, test system noise can cause soft failure and being truly random in nature, this noise can't be reproduced. This is why characterization testing is important. Most soft failures of memories are single bit failures. They occur for one of the following reasons: slow access, lo-s of data in cells, or multiple addressing.

These causes can create system failures due to a combination of the following conditions:

- Voltages
- Temperature
- Static Noise
- Timing Changes
- Data or Address Pattern
- Noise Pulses on Power Supply or Clock Lines

The advent of the microprocessor in addition to the above soft failures, has added those related to software and the interrelationship between software and hardware:

- Pattern and pattern sequence sensitivity
- Interrupt
  - Trigger on wrong priorities for multilevel interrupt
  - Lose data
- Failure to execute instruction and/or interrupt
- Loss of carry and bits during recirculation of data
- Mnemonic sensitivity
- Instruction and instruction sequence sensitivity

It should be noted that soft errors found early in system operations can be the result of insufficient testing for data pattern, temperature, voltage margins, or a combination of these.

MOS PROMS

MOS PROMS are primarily susceptible to charge loss (memory cell retention) failures.

Cell charge loss characteristics were studied for the FAMOS PROM[1]. The single transistor structure used is the N-channel two layer polysilicon cell. By measuring the two terminal threshold voltages before and after programming, the offset voltage (V_{TP}-V_T) on the floating gate can be determined. Figure 119 shows the two terminal V_T bias configuration and the resulting IV characteristics. These parts were then baked at 200, 250 and 300°C to accelerate the charge loss. The Degradation rate of programmed

[1]FAMOS PROM Reliability Studies, by G. Gear, 1976 IEEE Reliability Physics Symposium

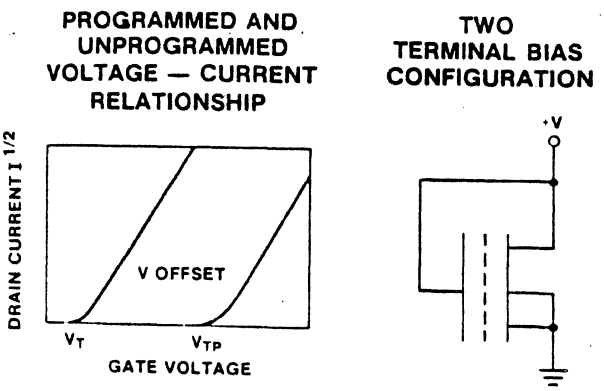


Figure 119

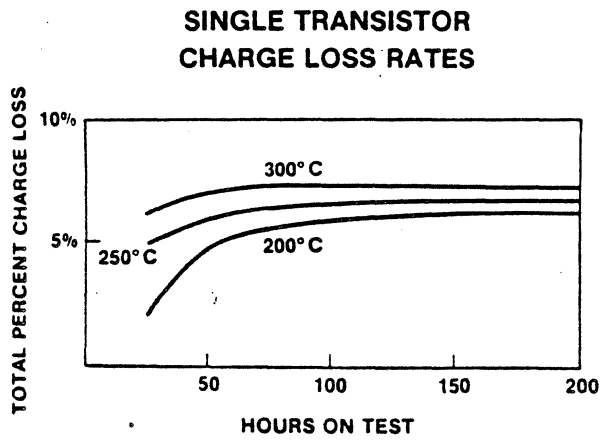


Figure 120

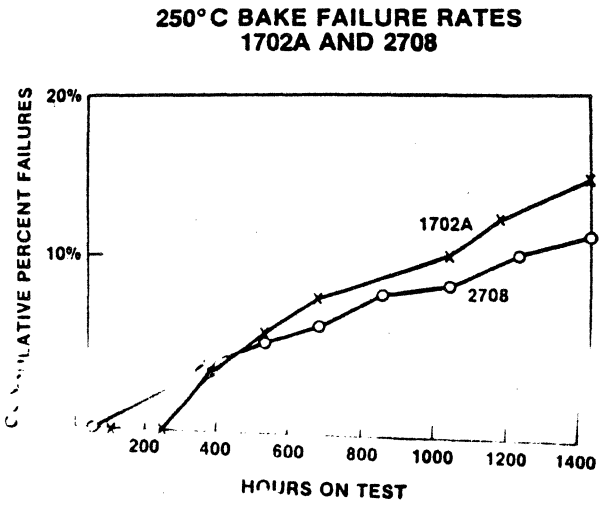


Figure 121

threshold voltage at the various temperatures is shown in Figure 120. Each data point represents the normalized average of ten individual transistors.

Cell retention in both the 2048 bit PMOS and the 8192 bit NMOS arrays were evaluated using high temperature bakes. A bit pattern was selected that programmed about 90% of the PROM cells but contained some unprogrammed bits in each row and column so a complete functional test could be performed. These parts were then baked at high temperatures and the cumulative percent failures plotted with time. Figure 121 shows the 250°C retention characteristics of the PROM and NMOS PROM arrays.

Bipolar Failure Modes

Bipolar TTL failure modes can be grouped into the following categories: Pipes (collector-to emitter shorts in which crystal imperfection allows emitter diffusion to go through collector), emitter base junction shorts or leakage, low impedance devices - threshold failure, and overstressed component.

Bipolar PROMs

Bipolar PROMs present unique failure modes due to the construction of the fuse, especially so in the nichrome devices.

Since nichrome is a thin film, surface effects play a large part in defining the fuse structure. Reactions that are not important, or that do not occur in bulk nichrome, become significant in the thin film structure due to the higher free energy associated with surface chemical and physical phenomena. Both ESCA, Electron Spectroscopy for Chemical Analysis, using x-ray photo-electrons, and Auger Electron Spectroscopy have shown that subsequent process steps play a significant role in determining nichrome structure and its contact to the aluminum interconnect metallization. Other studies have shown that moisture levels in the lifting reagent can attach thin nichrome films. The metal etch used in removing unwanted aluminum metallization over the fuse may also attack the nichrome. Usually an oxidizing agent, such as nitric acid, is added to the metal etch reagent to passivate the nichrome against attack. However, the very process of passivation involves oxidation of the surface of the nichrome and, considering its thin nature, any shift in fuse characteristics as a result of the altered surface structure must be monitored.

There are certain failure modes that are indiginous to bipolary PROM circuits. These are "growback" and opening of non-programmed fuse, and nonfuse related failures. Also weighing heavily in reliability assessment, is the fact that the PROM is not a finished product until after programming and verification. If these steps, however, are performed properly, the device should have failure rates similar to those of mask-programmed ROMs. Each of the PROM's peculiar failure modes are now discussed.

"Growback" Phenomenon

The growback phenomena is historically the most widely discussed failure

mode of PROMs. Basically, growback is a field induced mechanism where metal dendrite formation occurs in the gap region of the blown fuse. Growback is a failure mode where too much residual nichrome is left after blowing the fuse. This might cause dielectric breakdown in which the metal actually forms a filament, bridging the blown gap and creating a high resistance short.

Growback may appear for several reasons: First, the blown link may grow back together, either because of electromigration or a crystal regrowth phenomenon; and secondly, a fused link might also appear to have reconnected if in fact the link were not completely blown to begin with, but instead were only partially opened to form a high impedance short.

To prevent growback, programming the PROM (blowing fuses) must be accomplished using fast high voltage pulses with the programming to occur on the rise time -- this guarantees high programming current. Fuses requiring long program pulses and blowing on the dwell or flat of the pulse have an increasing probability of growback.

Several conclusions relating to "growback" can be made:

- The phenomena appears as an early mortality failure mechanism and does not impact long term life (MTBF) of the device. Field experience of billions of device hours support this contention.

- Potential early failures can be removed effectively by use of a dynamic burn-in at maximum temperature and V_{CC}, followed by a special functional test.

The results of the growback phenomena have applied to metal link fuses; however, the polysilicon fuse has been reported to growback (by a Navy study) because the passivation coat must be left off of the fuse. And with this coating removed, fuse material can splatter and a small gap is possible.

The overall problem of fuse growback is well understood and is not considered to pose a reliability program at present.

Opening of a Nonprogrammed Fuse

Programming during read occurs when fuses are too narrow and therefore may be opened by the relatively low read current. Polysilicon fuses, for example, typically require at least 16mA of current to open. During programming, fuses receive 20-80mA of current (depending on fuse resistance and nonfuse circuit impedances). Up to 12mA may flow through nonselected fuses at this time, due to breakdowns and parasitic resistance paths. Occasionally, 12mA is sufficient to open a fuse, inadvertently programming a nonselected bit. This event would be detected at program verification as fusing error and does not represent a reliability hazard.

The impedance of a nonselected fuse may rise due to partial blowing of the link, but more commonly, the impedance will be reduced because the

center of the fuse thickens. On intact fuses whose impedance has risen, the highest observed impedance is 2.5K ohms, well below the 12K ohms required to sense an open.

Nonfuse Related Failures

Nonfuse related failures are those not directly attributable to the fuse element. Included are specific failures in decoder and sense amps or gross failures, such as metal defects, oxide faults, oxide-junction contamination, diffusion defects, mechanical defects in the chip, design defects in the classical assembly, and package related failures -- open bond wires, lifted bonds, lifted chips, and hermeticity rejects.

4.722 Assembly and Package Related Failure Modes

The classical assembly and package related failure modes for ICs include:

- Open bond wires
- Lifted bonds
- Lifted chips
- Hermeticity

Assembly, package faults and mechanical faults in the chip, such as cracks in the silicon and metallization, can generally be screened out by various mechanical and environmental stresses. These include:

- Stabilization Bake
- Centrifuge
- Fine and Gross Leak Tests
- Thermal Intermittence Testing (with plastic packages and gold wires)

With large LSI devices, die attach is extremely important. When attaching a large chip, say >10,000 mil^2, to a metallized ceramic substrate, there is seldom enough gold to form an adequate volume of gold-silicon eutectic material to result in the desired void free chip attach. Therefore one must supply additional eutectic material in the form of a small gold-silicon preform. This will help in reaching the optimum thermal dissipation capability that a particular package and chip size allows. The θJA (Junction to ambient temperature coefficient) or θJC (Junction to case temperature coefficient) of the device is critical in reliability calculations determining the acceleration of failure rates due to the dependence on Junction temperature.

Potential package related failures are important for LSI devices such as microprocessors for the following reasons: Large die size could affect proper bonding of the die to the package; the large number of wire bonding

pads and number of external package pins required increase the probability of a bad wire bond occurring; the large package size could present sealing problems which are brought to light by hermeticity and temperature cycling tests. The integrity of the die and wire bonds could be ascertained by centrifuge tests, but extreme care must be taken so as not to crack the package by improperly performing this test. The total package must be rigidly supported over its entire surface area during this test so that bending movements do not occur during the centrifuge cycle. Severe flexing can result in damage to the LSI package in the form of hairline cracks.

The reliability of thin nichrome films (in bipolar PROMs) vs. dry hermetic packaging has received wide attention via the use of nichrome resistor structures. Hermetic packages, using devitrified (crystalized) high lead content glasses, were found to have residual moisture levels high enough to condense out at low temperatures inside the cavity forming a thin film over the chip. If the device was then biased (functioning) under this low temperature condition, electrolytic attack might occur; specifically anodic dissolution would take place when two areas on the circuit (bonding pad and a fuse in the case of a PROMO were connected by the water film and a potential difference of at least 2.5 volts existed. Although the $si0_2$ glassivation was thought to prevent moisture from reaching the nichrome fuse which it covers, there is always the chance that a small invisible crack or pin hole may permit the condensed water vapor to contact the nichrome film below. Devitrified glasses, commonly used in sealing CER DIP packages, are particularly sensitive to this phenomena of high residual moisture content in the package cavity. The source of the moisture comes from water strongly bonded in the glass which was formed when an organic binder was burned off during the manufacture of the raw assembly piece parts. This binder is used to hold the glass particles together until subsequent firing in a furnace can fuse the glass together. Later during IC package sealing, this glass first melts to form a hermetic seal and then undergoes a phase transformation called devitrification where the glass assumes a more ordered crystalline structure. It is during this latter process that most of the latent moisture is evolved and trapped in the cavity.

One approach to avoid the residual moisture is to use a vitreous seal which does not crystallize after sealing and therefore does not precipitate out as large amount of moisture as in the devitrifying seals. These vitreous glasses are often sealed in air to prevent reduction of lead oxide to metallic lead and can therefore contain appreciable moisture if the air is not carefully dried.

CER DIP packages used for commercial temperature ranges, 0° - 70°C, are not affected by this phenomena since the moisture never condenses out in a biased mode especially considering that chip temperatures are some 20° - 30°C in excess of the ambient temperature outside the device. Vitreous seals could be used on military temperature ranges if residual moisture levels could be proven low enough or as an alternate approach, the chip can be made moisture proof by using a redundant silicon oxide barrier to reduce the possibility of a glassivation flaw exposing a nichrome thin film. The "freeze-out" test specified in the MIL-M-38510/201 detail specification on the 512 bit PROM, provides one method to determine whether or not residual moisture is attacking nichrome. The water drop

test, in the same document, determines the integrity of the glassivation. It is important to note, however, that most single layer glassivation techniques using deposited SiO_2 are not much more than scratch protection barriers. Visual inspection for small glassivation flaws is virtually impossible; so a better solution for military temperature range PROM's is to avoid residual moisture in the first place. This is accomplished by using the well known gold-tin, 80:20, Au/Sn, solder seals. These are of proven reliability in side-brazed dual-in-line configuration as well as in the ceramic-filled glass flatpacks. The sealing environment can use every dry nitrogen or forming gas (N_2/H_2 mixtures) with furnace profiles that result in very dry hermetic packages.

4.73 Types of Reliability Tests

Improved lot reliability is accomplished by compressing time in accelerated testing by using time, power and temperature relationships.

The various screens employed in reliability testing are designed to prematurely activate these time-related failure mechanisms. As shown in Table 10, different screens are needed to detect different failure modes because no single screening test is sufficient to find all of them, or even most of them. This is why a sequence of screens frequently is used to detect the mix of failure modes most appropriate for the end application.

Stabilization Bake

Stabilization bake is designed to stabilize electrical drift characteristics and accelerate chemical degradation such as surface contamination, bulk defects, etc. This test is performed at the maximum rated storage temperature (generally 150°C) on non-operating devices for 24 hours or more. The IC storage temperature is normally much higher than its operating temperature, and stabilization bake will expose temperature dependent effects that may not be uncovered in burn-in. Stabilization bake is generally effective for metal-oxide-silicon (MOS) devices since 24 hours are insufficient to screen out potential ionic contamination problems. A better test to eliminate this failure mechanism would be a high temperature, reverse bias burn-in for logic elements and a high temperature, functional burn-in for large-scale-integration (LSI) devices.

Temperature Cycling

Temperature cycling mechanically stresses the IC by alternate heating and cooling (10-cycles from -55°C to +125°C,) exposing poor bonds and package seal problems. This test is effective for small devices, however, it can be potentially destructive to LSI units by inducing latent defects such as microcracks in ceramic packages.

Burn-In

Burn-in is widely accepted as a means of assuring reliability because it simulates actual operation of the device accelerated through a time, power, temperature relationship. Burn-in is most effective for detecting die related failure mechanisms such as, drifts due to inversion or channeling

Table 10

Failure Mechanism Detectable by Screening Tests

Screening Test \ Failure Mechanism	Substrate mounting defects	Bulk silicon defects	Substrate surface defects	Bonding and wire defects	Particle contamination and extraneous material	Seal defects	Package defects	External lead defects	Thermal mismatch	Electrical stability
Internal visual exam	●		●	●	●		●			
External visual exam						●	●	●		
Stabilization bake		●	●	●						●
Thermal cycling	●		●	●		●	●		●	
Thermal shock	●		●	●		●	●		●	
Centrifuge	●			●	●		●			
Shock	●			●	●		●			
Vibration	●			●	●		●			
X-ray	●			●	●	●	●			
Burn-in	●	●	●	●						●
Leakage tests						●				

and oxide pin holes, as well as bonding and wire defects and electrical stability which may cause early system failures.

Power burn-in consists of operating under maximum electrical and thermal conditions, usually for 96, 168 or 240 hours at 70°C or 125°C. The time, voltage stress levels and temperature relationship along with the choice of driving or loading circuitry (for LSI devices), to accelerate the removal of infant mortalities, determine the effectiveness of burn-in (that percentage of the ultimate total number of failures that are located by the burn-in).

Three basic types of burn-in are employed to weed out infant mortalities:

- Static or HTRB Burn-in
- Dynamic Burn-in
- High Voltage Cell Stress

The burn-in conditions developed for a particular device must be based on an understanding of that device's construction, operation, and topography. One must partition the device type and determine how many junctions/gates are reverse biased and how many are actually stressed under forward or reverse bias conditions to determine which type of burn-in is most effective.

Some suppliers (such as Intel and TI) and users are finding that the use of high voltage cell stress tests are more effective in uncovering oxide defects in MOS memories/LSI devices than is dynamic burn-in. A typical high voltage cell stress test involves cycling through all addresses for two seconds both high and low with 20V V_{DD} being applied (for a 12V rated part for example) at an ambient temperature of 125°C.

For example, during the initial reliability evaluation of 4K RAMs such as the 2107B, an Infant Mortality failure rate of approximately 1% was determined. The primary failure mode was oxide breakdown. The failure rate versus time and temperature is shown in Figure 122. Since the failure rate of infant mortality failures was too high, all devices were subjected to a 48 hour 160°C Dynamic Burn-In. This test involves exercising the memory at the elevated temperature. While it can be seen from Figure 122 that this burn-in did accelerate the failure rate to some extent, its effect in accelerating oxide breakdown failures was not as high as desired. This is because oxide breakdown failures have a thermal activation energy of 0.3eV so that the temperature dependence is relatively small. As a result, a high voltage cell stress test was implemented along with process improvements which succeeded in screening most of the potentially defective devices. Figure 123 and Table 11 show the results of the High Voltage Cell Stress test versus Dynamic Burn-In. Note that when high voltage cell stressed devices are returned to normal operating voltage, the random failure rate decreases. This data shows that cell stress eliminates more oxide defects than Dynamic Burn-In.

Static or HTRB (dc) burn-in will screen out devices with thermally activated surface related defects showing up as excessive leakage currents, speed

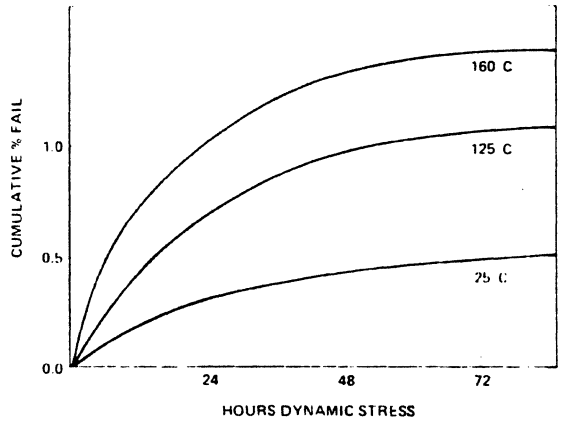


Figure 122: Temperature Dependence of Oxide Breakdown Failures

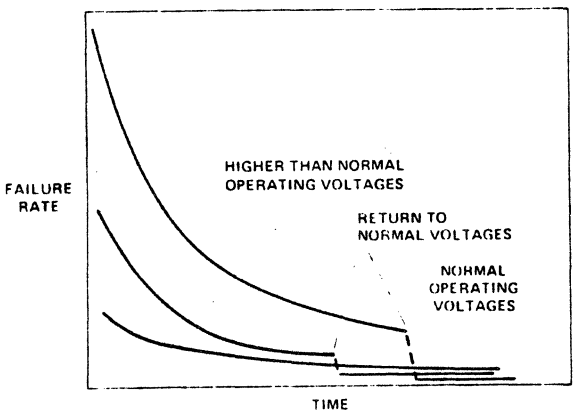


Figure 123: Effect of High Voltage Cell Stress on Infant Mortality Failures

Table 11

Comparison of Observed Failure Modes After Burn-In vs. the High Voltage Cell Stress Test

% of Total Cell Stress Failures	Ratio of Cell Stress to Dynamic Burn-In Failures	Failure Mode
11.8%	4.5:1	Total Array
35.3%	3:1	Single Bit
11.8%	1.8:1	Row
17.6%	1:1	Column
23.5%	1:1	Miscellaneous

degradation or threshold voltage shifts after electrical tests. In fact, static (HTRB) burn-in is appropriate for locating defects in certain MOS devices because MOS devices have higher field and lower doping levels, the failures of which are readily identified by HTRB burn-in. Whereas dynamic burn-in in which all clock and address lines are continually sequenced, will show up defects on MOS transistor memory cells resulting from weak oxides and locates pipes (collector to emitter shorts in which crystal imperfections allows the emitter diffusion to go through to the collector) and emitter-base shorts for bipolar memories in which current must be flowing to isolate the defects. Both burn-in screens will detect some of the same defects in a device, but each will detect additional unrelated defects. The best screen would be to perform several burn-in methods, but this is not always economical.

However it has been shown that the reliability of bipolar LSI devices is most realistically evaluated using Dynamic Burn-In (MIL-STD-883 Condition D). A static or HTRB burn-in activates only 5-10% of the entire LSI chip -- normally only those circuits (sense amplifier and decoder) on the periphery of the circuit near the bonding pads (external pin connection) -- as shown by voltage contrast plots.

Accelerated Burn-In

A school of though emanating from Bell Telephone Labs advocates the use of accelerated (high temperature) burn-in rather than the conventional 168 hour/ 125°C burn-in. It is felt that the conventional burn-in only removes a small part of the failures from typical microcircuit populations. According to Bell Labs, burn-in times on the order of 16 hours at 300°C have usually been needed to effectively remove freak devices; whereas over 100,000 hours of burn-in at 125°C would be required to achieve the same results.

Establishing the optimum burn-in time for high temperature (>125°C) requires correlation data from devices burned-in under various time and temperature conditions. Data are available on high temperature bias stressing of individual MOS test transistors. Very little correlation data are available on high temperature burn-in of complete MOS LSI circuits.

Accelerated burn-in testing as specified to date is applicable to SSI TTL and CMOS devices and certain linear ICs, but is not appropriate for MSI/LSI devices for the following reasons: Only between 5-15% of all circuitry is being biased, the majority of the chips circuitry isn't stressed, there is no correlation between accelerated testing and dynamic burn-in, a dedicated test cell using the same design rules and processes as the entire circuit with the components broken out for ease of measurement is required.

The major purpose of accelerated testing is to compress the normal life span of devices. High temperature testing, however, can cause problems. For example, ICs encapsulated in tin plated packages exposed to a temperature above 150°C can become unsoldered.

Accelerated life testing tends to provide heated debates when discussed in terms of predicting results at normal stress levels. Acceleration factors cannot be obtained by calculating failure rates at different temperatures and plotting by some scale against temperature.

At high temperatures, many devices undergo unpredictable changes in their characteristics. A few representative devices should be exposed to the intended conditions and electrically characterized to verify that they will operate there.

Some judgement should then be applied to determine whether the operating conditions are reasonable. If the devices appear to be in reasonable current and voltage ranges for all terminals, are not oscillating in a different manner than intended and are at reasonable temperatures, the test may formally begin.

Often, the same generic device types (ICs), of various suppliers being compared or tested, require different forcing functions. Thus, one cannot use exactly the same conditions of test for all suppliers' devices.

LIFE TESTS

One of the most effective ways of gathering failure rate data on a semiconductor device is life testing.

During the initial phases of a new product, the failure mechanisms must be determined in each portion of the reliability life curve. Since infant mortality failures occur very early in a device's life, no acceleration is necessary. However, when information on wearout failure mechanisms is required, the device must have its life "accelerated". This is accomplished by either subjecting the device to a high temperature, a high voltage or both. If high temperature testing is used and the thermal activation energy of the failure mechanism is well defined (so that the failure can be "accelerated"), a plot as shown in Figure 124 can be made. This is an arrhenius plot in which time is plotted against the reciprocal of temperature and the slope of the curve is the thermal activation energy in electron volts. Using this plot, failure rate data taken at one temperature may be translated to another temperature with reasonable accuracy. In this form the plot follows the relation:

$$\tau = \tau_0 \exp \frac{E}{KT} \qquad (1)$$

where τ = MTBF (Mean Time Between Failures) at the desired temperature

τ_0 = MTBF at the test temperature

E = The thermal activation energy (eV)

K = Boltzmanns constant (8.63×10^{-5} eV/°K)

T = Test temperature in °K.

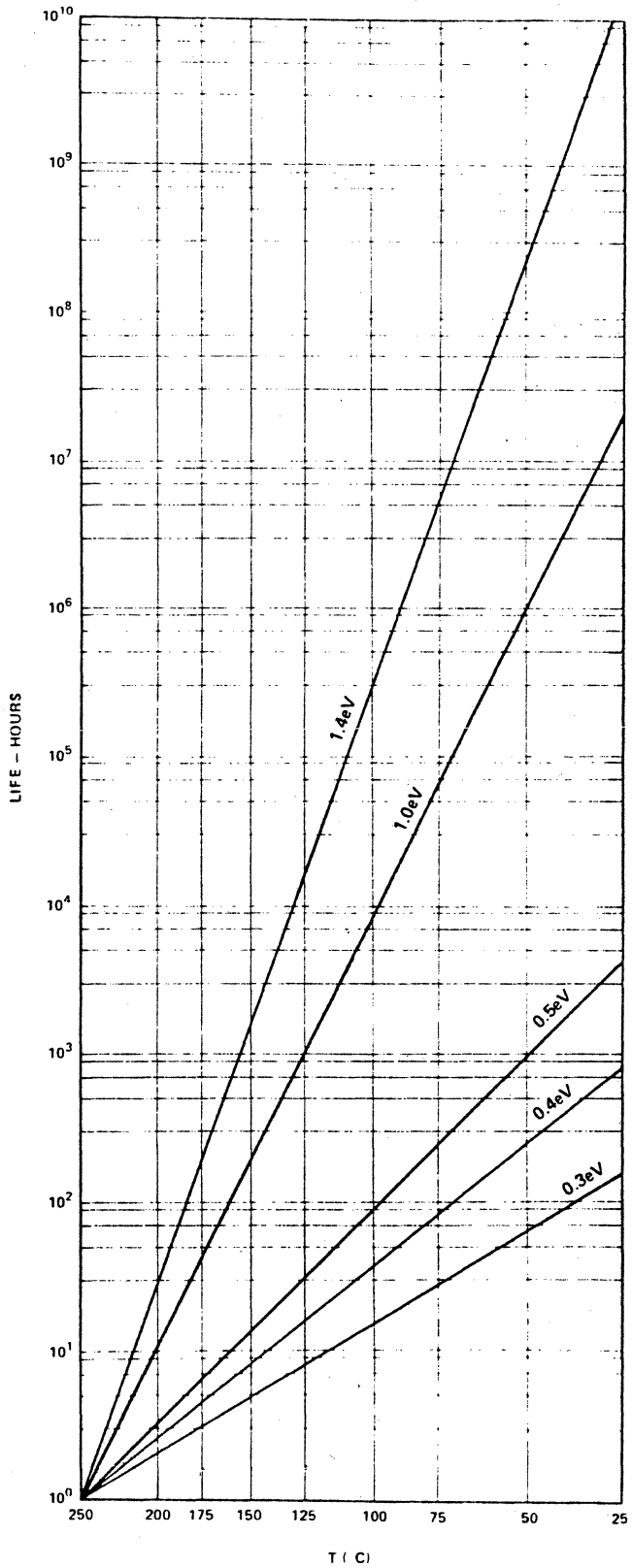


Figure 124: Arrhenius Plot

The acceleration factor may be calculated by:

The acceleration factor may be calculated by:

$$F = \exp E/K\,(1/T_1 - 1/T_2) \qquad (2)$$

where T_1 is the test temperature (°K) and
T_2 is the desired temperature (°K).

Figure 124 shows an Arrhenius plot with several thermal activation energies for common failure mechanisms (see Table 12).

Thermal activation energy describes the temperature dependence of a failure mechanism and is the slope of the plot of failure rate or its reciprocal, life, versus the reciprocal of temperature (see equations 1 and 2). Equation 1 can be solved for E giving:

$$E = KT \exp^{-1} \frac{\tau}{\tau_o}$$

Electrical Testing

Electrical testing is normally the final operation in reliability screening. Electrical testing does not contribute to the reliability of the good material! It identifies devices which do not conform to electrical specification.

Soft errors found early in system operations can be the result of insufficient testing for data pattern, temperature, voltage margins, or a combination of these; thus, the need for electrical testing using comprehensive patterns at power and temperature supply extremes. As such, electrical incoming inspection alone can only reduce some of the user's assembly and field service costs.

Figure 125 presents a graphical presentation of how a combination of the previously discussed tests affect component failure rates. The screening tests of curve 4 (Figure 125) most effectively weed out the incipient failures.

4.74 Failure Rate Calculations

The model in MIL-HDBK-217 for LSI devices is inadequate for failure analysis calculations. There exists some confusion as to device complexity and replacement complexities. For example, the 6701 4 bit slice replaces 1028 gates but contains 288 on chip gates. If that model was used one would never obtain operational devices. In actual practice failure rates are

Table 12

Failure Mechanisms in MOS

Failure Mode	Type	Activation Energy (E_{act})	Detection	Preventive Measure
Slow Trapping	Wearout	1.0 eV	High Temp Bias	Ultra-Clean Processing
Contamination	Wearout/Infant	1.4 eV	High Temp Bias	Ultra-Clean Processing
Surface Charge	Wearout	.5-1.0 eV	High Temp Bias	Ultra-Clean Processing
Polarization	Wearout	1.0 eV	High Temp Bias	Eliminate Phosphorus in Gate Oxide
Electromigration	Wearout	1.0 eV	High Temp Operating Life	$J < 10^5$ A/cm^2
Microcracks	Random	– –	Temp Cycling	Contoured Oxide Steps
Contacts	Wearout/Infant	– –	High Temp Operating Life	Ultra Clean Processing
Oxide Defects	Infant/Random	.3 eV	High Voltage Operating Life and Cell Stress	Ultra Clean Processing

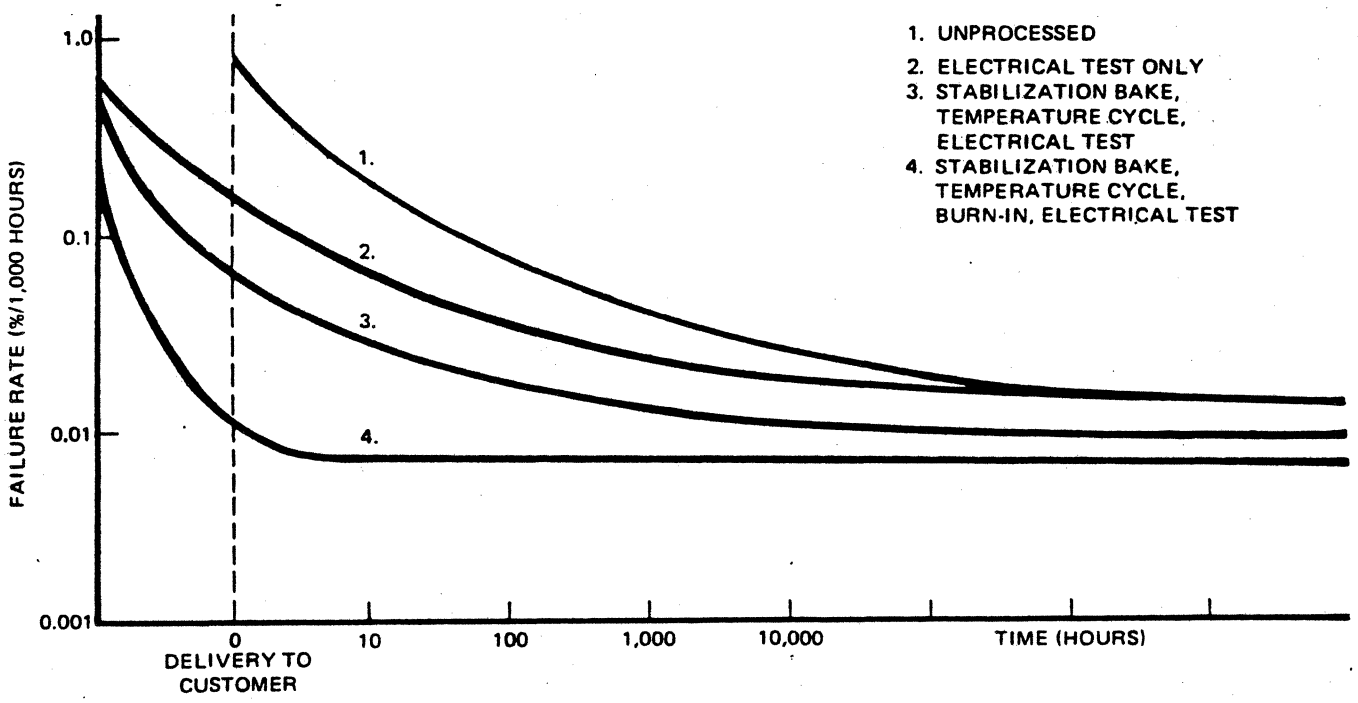


Figure 125: Selection of Screening Tests Influence Component Failure Rates

TABLE 13

MANUFACTURER	TOTAL TESTED	PERCENT FAILED	REASON FAILED
		7400 SERIES	
Signetics	1M	5%	ac parameter (T_{pd})
Fairchild	500k	5%	ac parameter (T_{pd})
		7%	mechanical (bent leads, marking)
National	550k	3%	ac parameter (T_{pd})
		10%	mechanical (bent leads, marking)
TI	750k	2%	ac parameter (T_{pd})
		4%	mechanical (solderability, bent leads)
		SHUL	
TI	1.5M	2%	ac parametric
	2.1M	0.9%	ac parametric
		4%	mechanical (plating)

Of the devices that passed this screening, only 0.05% failed after assembly.

TABLE 14

TYPE PART	TOTAL TESTED	FAILED DC	FAILED RT FUNCTIONAL	FAILED AC PARAMETRIC	TOTAL FAILED
TTL/SSI	8328	5.9%	0.7%	4.5%	10.9%
TTL/MSI	905	8.0%	0.8%	21.6%	27.4%

Source Logic in Testingland - A Tale of Measurement Techniques by Martin Marshall, EDN January 20, 1976

several orders of magnitude better than those predicted by MIL-HDBK-217 even with proper adjustments for device complexity.

4.75 Reliability Screening Test Results

This section summarizes tests performed by DCA Reliability Laboratory over the past two years. The data used was chosen at random from DCA's data base.

4.751 Bipolar TTL ICs

The 54XX/74XX series is a relatively mature product family. Consequently, its attrition rate after subsequent screening tests, is very respectable at 1 to 5% for plastic encapsulated products, but from 1-13% for military temperature grade product from a population of 1-million devices representing many generic part types and several suppliers as well as differing date codes. The introduction of MSI and LSI devices in the series is tending to provide higher attrition rates while the gates and flip flops have very low attrition rates. The primary electrical failure mode is degradation of input parameters, such as an increase in input leakage current due to a soft-knee condition of the input diodes.

Table 13 shows the test results provided by one large user of 7400 series TTL devices. These results reveal quality variations between similar products from several major semiconductor suppliers. These ICs are intended for computer-related applications, or approximately reliability class C (commercial) of MIL-STD-883. The company uses a combined dc, real-time functional and ac parametric test system. The results shown are for illustration only, because quality levels can shift over periods of time.

Table 14 shows the results of tests of 5400 series TTL SSI and MSI circuits performed in accordance with MIL-STD-883 Method 5004 Class B. The total failed is less than the sum of the parts because some ICs failed more than one kind of test.

Table 15 summarizes reliability screening test results performed on digital (5400 series TTL) ICs intended for usage on several aerospace programs.

Overall all rejects for these digital integrated circuits show that the order of lowest to highest reject rate is military temperature range product (MTR) at 6.2% followed by MIL-M-38510 Class B at 7%, Level A precap/SEM product at 12.1% and finally MIL-STD-883 Class B screened product at 18.8%. Again the population size (813) of MIL-M-38510 Class B products from Table 1 is too small from which to draw any meaningful inferences.

Hermeticity rejects are very high for MIL-STD-883 Class B product which supposedly was already subjected to this test at the suppliers' facility. Pre burn-in electrical test rejects are relatively low and consistent for all reliability categories, but post burn-in electrical rejects are higher

TABLE 15

Digital ICs Tested Per Method 5004 MIL-STD-883 Class B

Procured Reliability Level	Qty. Tested	No. Rej.	% Rej.	H	Pre BI	Post BI	X	Other
MIL-Temp Range Product 54XX	38,349	2,364	6.2	442	397	814	558	153
MIL-STD-883 Class B	1,729	325	18.8	163	23	50	71	18
MIL-STD-883 Class A precap with SEM	629	76	12.1	5	2	7	60	2
MIL-M-38510 Class B	813	57	7.0	0	1	49	0	1

H = Hermeticity rejects

Pre Bi = Pre burn-in electrical test rejects

Post BI = Post burn-in electrical test rejects (including delta criteria)

X = X-ray rejects

Other = Other rejects such as cosmetic defects

for screened product (MIL-M-38510 Class B and MIL-STD-883 Class B) than for unscreened product. MIL-STD-883 Class B screened product had a lower reject rate than MIL-M-38510 Class B screened product. But remember that the MIL-M-38510 product electrical limits are established by the appropriate MIL-M-38510 "slash sheet" whereas the MIL-STD-883 Class B electrical limits are established by the suppliers data sheet limits so this might be a reason for the disparity.

Level A precap/SEM devices which had the most stringent precap visual requirements had the highest x-ray reject rate. This was followed in order by MIL-STD-883 Class B and MTR product respectively.

Table 16 summarizes the attrition rate of bipolar MSI/LSI circuits after exposure to stabilization bake (48 hours @ 150°C), temperature cycling, hermeticity tests, and 168 hours @ 125°C burn-in and electrical measurements.

4.752 4000Series CMOS ICs Test Results

A test sequence was devised based on MIL-STD-883 Class B for both commercial (plastic encapsulated) and military (hermetically sealed) temperature range devices. All electrical tests were performed in accordance with the suppliers' data sheet.

The device types chosen for the evaluation represented a broad spectrum of widely used types in the 4000 series family to see if there were any logic functions particularly sensitive to one screen or another by virtue of device design and construction. The population of military temperature range devices was 13,043. The population for the commercial temperature range devices consisted of a sample with a size of 73,929 devices. With these sample sizes, it was felt that a viable and meaningful representative cross section and distribution of suppliers' production flows could be evaluated.

The results of these tests as summarized in Figure 126 and Table 17 for commercial devices with a screening sequence of stabilization bake, temperature cycling, burn-in and electrical measurements; and Figure 127 and Table 18 for military temperature range devices screened in accordance with MIL-STD-883 Class B Method 5004 demonstrated the effectiveness of environmental and electrical tests as screens for weeding out incipient failures. In total, over 13,000 hermetic devices ranging from simple Quad 2 Input NAND gates to a 256-bit static RAM were 100% tested in accordance with Method 5004 Class B of MIL-STD-883. The failure rate for these devices was 12.7% of the devices that failed, 7.8% failed hermeticity tests, 53.5% failed pre burn-in electrical tests (indicating that temperature cycling and stabilization bake were effective in culling some rejects), 28.5% failed post burn-in electrical tests (emphasizing the value of this screen), and 10.2% failed x-ray tests indicating poor in-line QA (precap visual) procedures. The pre and post burn-in electrical failures were not skewed toward the more complex devices. Both simple (SSI) and complex (MSI and LSI) devices exhibited similar failure rates. For nonhermetic devices, an overall 6.0% reject rate was exhibited.

Table 16

Bipolar MSI/LSI Attrition Summary

BIPOLAR MSI/LSI ATTRITION SUMMARY

PRODUCT TYPE	QTY TESTED	QTY REJECTED	% REJECTED
Shift Registers	36,335	896	2.5
Read-Only Memories	2,949	127	4.0
Random-Access Memories	6,185	698	11.5

(ROMs/RAMs had a density to 1024-bits)

COMMERCIAL (PLASTIC ENCAPSULATED) TEMPERATURE RANGE DEVICES

Total Tested = 73,929

% Failures per Device Type at Electrical Test after Burn-In

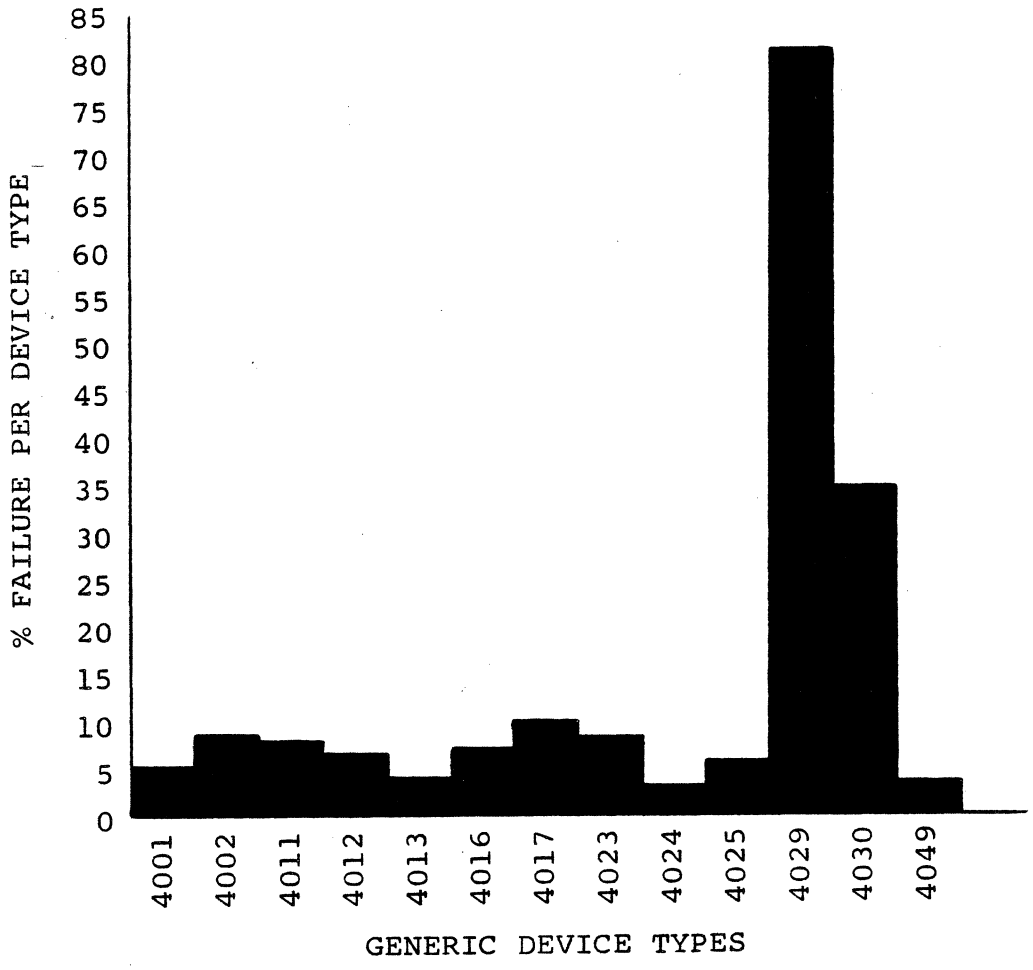


Figure 126

Table 17

Attrition Summary
Commercial Temperature Range Devices with Burn-In

TOTAL NO. TESTED	NO. FAILURES	% FAILURES
73,929	4,493	6.08

FIGURE 127 MILITARY (HERMETIC) TEMPERATURE RANGE DEVICES

Total Tested = 13,043

Cumulative % Failures per Device Type at Electrical Test after Burn-In

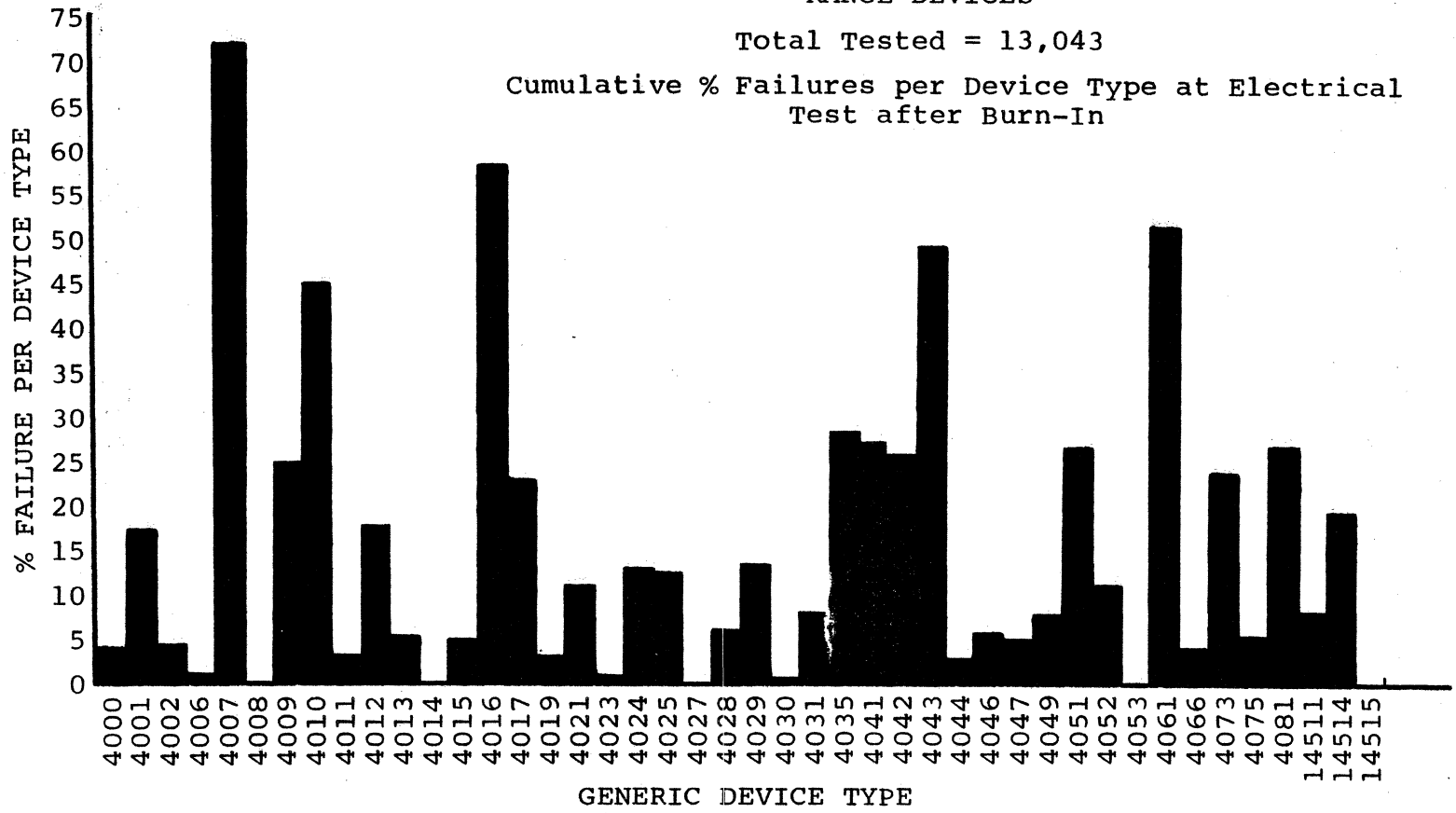


Table 18

Attrition Summary
Military Temperature Range Devices

TOTAL NO. DEVICES TESTED	NO. OF FAILURES	% FAILURES	FAILURES AT				
			HERMETICITY	EM1	EM2	XRAY	OTHER
13,043	1,661	12.7	135	822	470	205	29

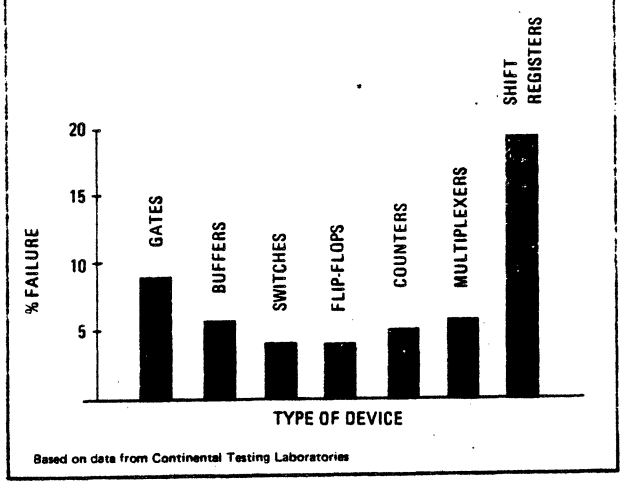
Table 19

CMOS IC's

SCREENING SUMMARY*

Type of Device	Number Tested	% Failure
Gates	29,843	8.4
Buffers	19,487	5.4
Switches	18,134	3.5
Flip-Flops	19,117	3.4
Counters	9,129	5.1
Multiplexers	2,533	5.9
Shift Registers	8,552	18.8

*Per MIL-STD-883, class B



Based on data from Continental Testing Laboratories

Table 20

CMOS ICs Tested Per MIL-STD-883 Method 5004 Class B

Procured Reliability Level	Qty	No. Rej.	% Rej.	H	Pre BI Elect.	Post BI Elect.	X	Other
MIL-Temp Range	13,179	1,931	14.7	307	850	531	226	17
MIL-STD-883 Class B	119	26	21.8	0	3	23	0	0
MIL-STD-883 Class A with SEM	7,066	755	10.7	15	107	139	288	206
MIL-M-38510 Class B	100	10	10.0	0	1	9	0	0

Table 19 presents further CMOS test data. In Table 19 the failure percentages of seven categories of CMOS devices are examined, including small-, medium-, and large-scale circuits. As expected, the high-complexity devices, like shift registers and multiplexers, are the most prone to failure. However, lower-order devices, such as gates and buffers, also have a high incidence of failure. Since CMOS has been in wide use for only a relatively short time, its reliability profile is only beginning to take shape. The data given here is based on devices shipped by a mix of suppliers during 1975.

Table 20 presents a summary of CMOS rejects from testing performed for several major aerospace programs which follows the expected trend - the highest reliability level of procured product has the lowest reject rate when subjected to subsequent screening. MIL-STD-883 Level A screened product with SEM and MIL-M-38510 Class B product had the lowest overall reject rates (10.7% and 10%, respectively). However, the MIL-M-38510 Class B product had a very small (100 pieces) population and comes from one supplier. Thus, this data is interesting but not meaningful for drawing valid conclusions from. Military temperature range (MTR) product had an overall reject rate of 14.7% followed by MIL-STD-883 Class B screened product with the worst reject rate (21.8%) in subsequent screening.

Hermeticity rejects were nonexistent for screened product but as expected occurred for MTR unscreened product.

Pre burn-in electrical test rejects were consistent and low for MIL-STD-883 Class A screened product with SEM, MIL-M-38510 Class B product and MIL-STD-883 Class B product. MTR product had twice the reject rate of the screened product.

However, for post burn-in electrical test rejects MIL-STD-883 Class B product had the highest reject rate!! with MIL-STD-883 Class A product having the lowest reject rate (as expected) followed by MTR. This high reject rate of MIL-STD-883 Class B product is alarming since the product has already had a 168 hour burn-in and post burn-in electrical measurements at the suppliers facility and it should be stable. Perhaps the burn-in used by the supplier is different and less effective than that performed by DCA or the CMOS process used is very unstable and a third burn-in possibly would produce still more rejects.

The highest reliability product (MIL-STD-883 Class A with SEM) had the highest x-ray and visual reject rate.

Table 21 shows further data for MIL-Temperature range devices - a screening summary of three popular logic families - standard TTL, CMOS, and ECL.

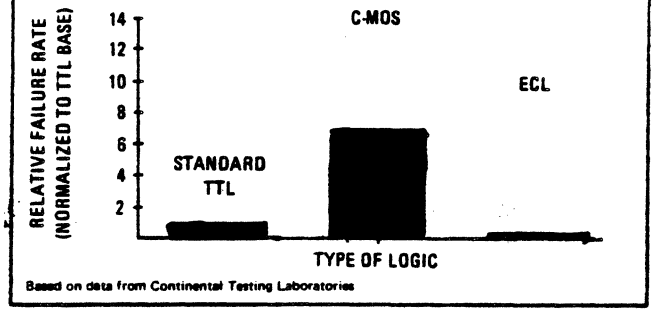
These tests indicate that both CMOS and ECL are far more prone to failure than standard TTL. The percent failures given here can be "normalized" to 0.05% per 10,000 devices for TTL, 0.62% per 10,000 devices for CMOS, and 0.37% per 10,000 devices for ECL. The conclusion may be drawn, therefore, that a CMOS device can fail almost twelve times as often as a TTL unit, while an ECL device is less likely to fail as often. Please note

Table 21

Screening Summary

SCREENING SUMMARY*		
Type of Logic	Number Tested	% Failure
Standard TTL	282,238	1.4
C-MOS	107,005	6.6
ECL	10,859	0.4

*Per MIL-STD-883, class B



Based on data from Continental Testing Laboratories

Table 22

Linear IC Test Summary

DEVICE CATEGORY	QUANTITY TESTED	QUANTITY FAILED	% FAILED
Op Amps	27,347	2,764	10.10
Comparators	125,551	8,142	6.48
Voltage Regulators	6,066	704	11.60
Miscellaneous Circuits (Timers, PLLs, Function Generators, etc.	970	82	8.50
TOTAL	159,934	11,692	7.31

however, that the pouplations for TTL and CMOS are reasonably large and represent a substantial mix of suppliers and part types whereas the ECL population is comparatively small and made up of only about a dozen different device types. From this data alone it is unwise to assume ECL is always less likely to fail than TTL.

4.753 Linear IC Test Results

The generic device types represented by the following data reflect the most popular devices throughout the industry.

In most instances, the lot size was 300 or greater and contained several date codes of products. In some instances, less than 300 devices of a given specialized generic device type were tested. This testing was normally of a single date code and, thus, not representative of the overall quality and reliability of a supplier's production line. Consequently, the results of these "small-single-date-code-specialized function" lot tests are separated from the more valid data and are contained in a miscellaneous category for information purposes only. No conclusions are based on that data.

Table 22 summarizes the test results of these three categories of linear ICs, as well as a miscellaneous circuit category that contains timers, phase locked loops, function generator circuits, and the like. As can be seen, the overall failure rate for all 159,934 units tested is 7.31%. The basic failure mode is the degradation of the input characteristics at both pre and post burn-in electrical measurement points.

Figure 128 depicts the results of the operational amplifiers by generic part type. As can be seen, the mature products exhibit a very respectable 1.5 to 8% failure rate. Both the newer and/or more specialized circuits have substantially higher failure rates -- as high as 26%. The miscellaneous category consisted of small quantities (single date code) of specialized (not widely used) op amps. The failure rate of some was rather high, but as mentioned previously, due to the small lot size, valid conclusions and predictions could not be made.

Figure 129 shows the test results of comparator tests for several generic part types. Overall, the comparators had a very respectable failure rate. The uA711 heavily skewed the total data with 98,000 parts tested. The 529 had a high failure rate, but did not have as high a population size. The miscellaneous category contains small quantities of some of the newer high speed comparators and quad comparators.

The following is a more severe example of linear IC attrition rates. For the Space Shuttle Program, linear ICs were procured with SEM (Scanning Electron Microscope examination), Level A Precap, stabilization bake, temperature cycle, centrifuge and hermeticity tests per MIL-STD-883 Method 5004. The units were then subjected to a MIL-STD-883 Class A screening sequence at DCA which included pre and post burn-in measurements and delta computations at three temperatures. The results were as follows:

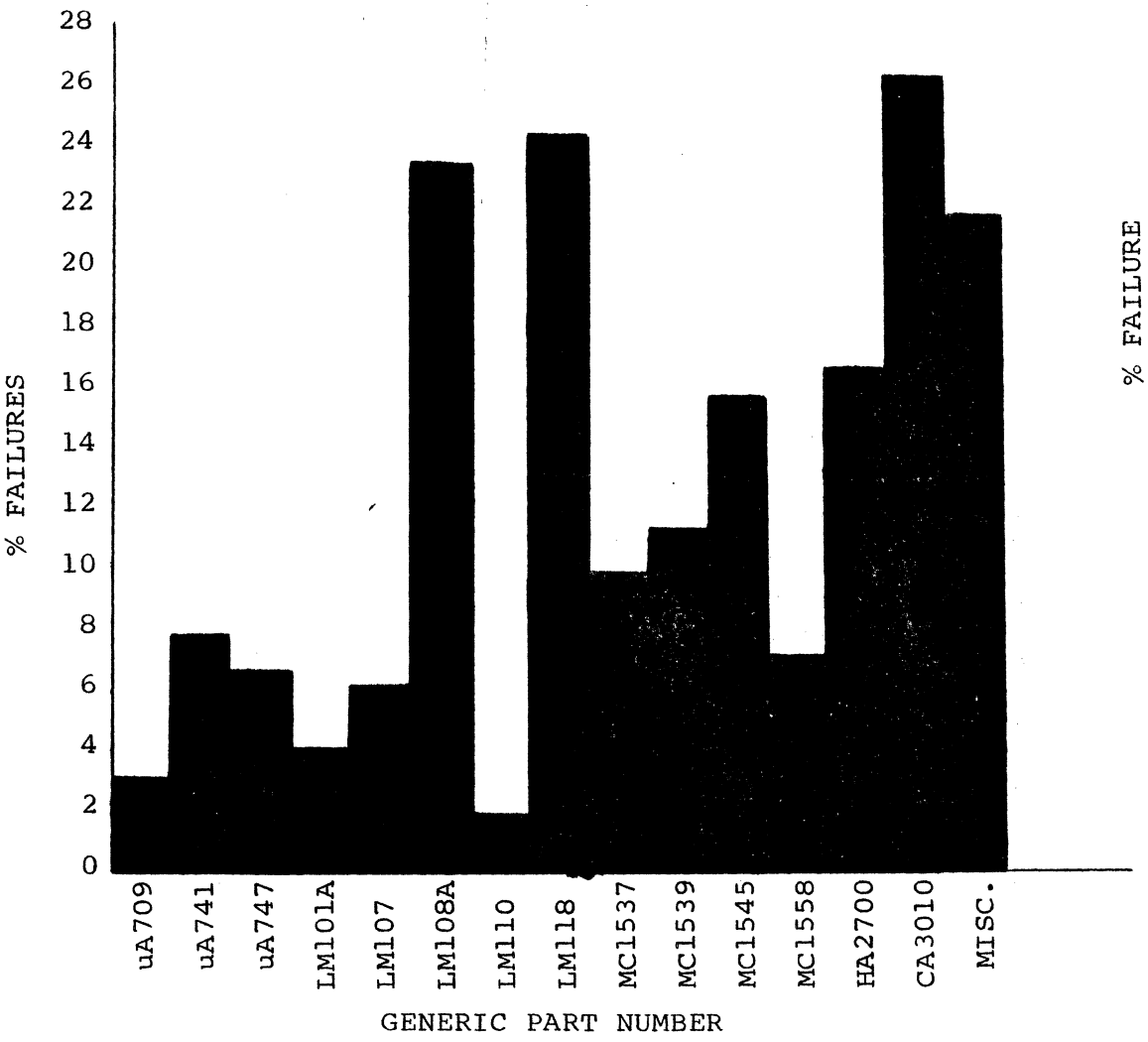


Figure 128

Operational Amplifiers. Note; Miscellaneous category consists of small lot size (in some instances single date code) of popular and specialized op amps.

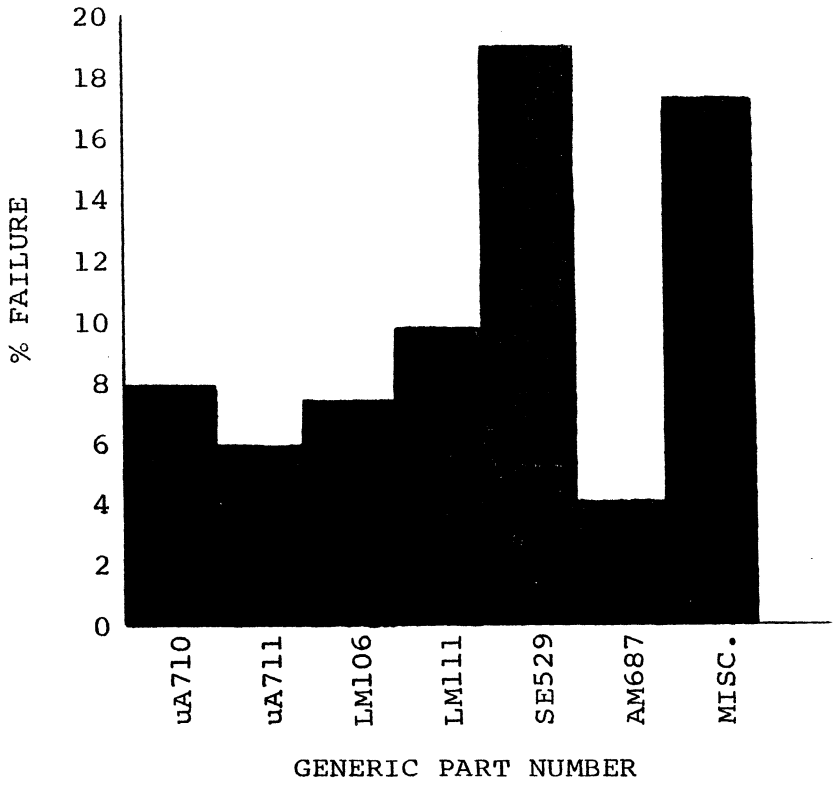


Figure 129

Comparators. Note: Miscellaneous category includes very small lot sizes of specialized comparators and the failure rate is not reflective of comparators as a whole.

PART TYPE	QTY	TOTAL FAILURES	FAILURE RATE %	FAILURES AT F/L & G/L	PRE BI ELECT	POST BI ELECT	X-RAY
LM108F	1891	477	25.2	88	7	253	129
LM108AF	616	235	38.2	34	42	91	68
LM111F	1065	388	36.4	35	7	234	112
LM118	286	62	21.7	8	3	19	19

These results show that even with environmental testing and SEM inspection performed by the supplier, a very high reject rate was incurred. This leads one to the general conclusion that deviations are being taken to the screening procedures at the suppliers plant or that complete test sequences are not being performed.

These results as well as those of Figure 128 and 129 demonstrate the need for an additional screening sequence upon receipt of the parts from the supplier and underscore the validity of burn-in.

Table 23 summarizes the reliability screening test results performed on linear ICs intended for usage on several aerospace programs.

Table 23 shows that military temperature range (MTR) and MIL-STD-883 Class B screened linear ICs had the lowest reject rate followed by MIL-M-38510 Class B product and MIL-STD-883 Level A precap with SEM unscreened product, respectively. The latter two reliability levels having 3 to 4 times the reject rates of MTR and MIL-STD-883 Class B screened products. It can be seen from Table 23 however, that the population size of MIL-M-38510 product is too small and comes from a single supplier to draw proper inferences from and is included only as a matter of interest.

Screened and MTR product have a minimum of 2 times lower reject rate as a percentage of total rejects, than does Level A precap/SEM unscreened product.

As mentioned before the small population of linear MIL-M-38510 Class B product and the high pre and post burn-in electrical reject rate cannot be used to draw valid conclusions regarding the reliability of this product category. Level A precap/SEM (2.1%) and MIL-STD-883 Class B (4.22%) product have the lowest pre burn-in reject rates followed closely by unscreened (MTR) product with a 5.36% reject rate as a percentage of total rejects. However, "Level A" precap/SEM product has 2-3 times the reject rate of MIL-STD-883 Class B product and MTR product respectively during post burn-in electrical tests and x-ray examination. This is ironic for several reasons. First, it is expected that unscreened unburned-in product such as Level A precap/SEM product should have a higher reject rate than the burned-in MIL-STD-883 Class B product. However, the same reasoning holds true for MTR product. But the data doesn't bear that out. MTR product had lower post burn-in electrical reject rate than MIL-STD-883 Class B screened product (4.44% and 6.77%, respectively). "Level A" precap/SEM product has the highest x-ray examination reject rate.

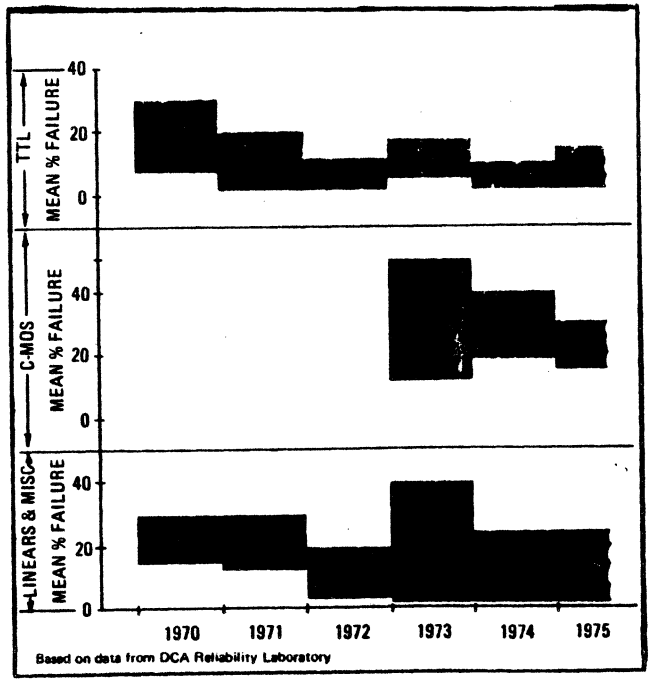
Table 23

Linear ICs Tested Per Method 5004 MIL-STD-883 Class B

Procured Reliability Level	Qty	No. Rej.	% Rej.	H	Pre BI	Post BI	X	Other
MIL-Temp Range	23,310	2,989	12.8	316	1,255	1,036	216	166
MIL-STD-883 Class B	5,129	910	17.7	93	211	337	253	16
MIL-STD-883 Class A precap with SEM only	4,058	1,224	30.3	193	85	602	331	0
MIL-M-38510 Class B	57	29	50.9	0	12	16	1	0

Table 24

Five Year Failure Analysis for ICs



The reject data of Tables 14, 20 and 23 reflect integrated circuits which were screened for eight major aerospace programs and were procured with the following initial reliability levels: MIL-STD-883 Method 5004 Class A pre-cap visual inspection with SEM (scanning electron microscope) examination but no environmental screening, MIL-M-38510B screened product; MIL-STD-883B screened product; and military temperature range (MTR) unscreened product and then all were tested in accordance with Method 5004 MIL-STD-883 Class B.

The data presented so far shows some alarming reject rates. This leads one to ask the question, "are components failing more?" which is answered by Table 24. The time plot given in Table 24 shows the lowest and highest mean (average) failure percentages that occurred most often in each year for a 5 year interval (1970 through 1975) for TTL, CMOS and linear integrated circuits.

In every case, failures seem to be increasing over what they were in 1970. For each group, as a matter of fact, the upper means for 1974 are higher than those for 1970 by 10% or more. The negative conclusion would be that reliability is getting poorer. However, users are more concerned today about reliability than they were five years ago, so that more devices are being screened. This could account for the apparently increasing number of weak devices.

In Table 24 the ICs group is broken down into its component parts. TTL devices, both standard and low-power types, account for about 85% of the ICs population through 1972. From 1973 on, the TTL contribution drops to about 70%, with CMOS and linear devices picking up the difference. Also, in the last two to three years, some high-noise-immunity, Schottky, and low-power-Schottky circuits are reflected in the TTL mix. Prior to 1973, CMOS was not being used in sufficient quantities for any meaningful test data to be available.

For every class of IC, the mean failure percentages seem to be declining, with TTL exhibiting the best reliability performance. However, the relatively high incidence of failures for both CMOS and linears is causing the means of the ICs group (Table 24) to balloon from 1973 on. The wide range of mean-failure rates in both CMOS and linears can possibly be attributed to increased use and more intensive screening, as well as to the introduction of higher-complexity devices.

But at least one other factor may have influenced the sudden increase in failures in 1973 for all three IC groups. That year shortages were at their worst and lead times were longest. Semiconductor suppliers may well have been shipping with below-par reliability standards because the demand for parts was excessive.

4.754 Memory/LSI Test Results

This section presents reliability test results for both bipolar and MOS memories and microprocessors.

Table 25 compiles 1000 hour life test data by device technology. The rejects are listed as a total and then subdivided as die related failures.

Table 25

Life Test
Data Summary by Technology

TECHNOLOGY	NO. TESTED	DEVICE HOURS	NO. REJECTS	DIE RELATED REJECTS	FAILURE RATE %/1000 HOURS
BIPOLAR	37,534	628.42×10^6	147	129	.02
PMOS	229,439	6839.7×10^6	725		.01
NMOS	26,617	3172.3×10^6	96	173	.01
MNOS	78	21.5×10^6	17		.01
CMOS	1,553	722.5×10^6	27	10	.01

Table 26

Die Related Malfunction Summary for LSI Device Technologies

FAILURE CLASSIFICATION	BIPOLAR		MOS		CMOS	
	NUMBER DEVICES	%	NUMBER DEVICES	%	NUMBER DEVICES	%
SURFACE	30	22.22	79	33.33	2	18.18
OXIDE DEFECTS	18	13.33	56	23.63	4	36.36
DIFFUSION DEFECTS	22	16.30	33	13.92		
METALLIZATION DEFECTS	23	17.04	25	10.55		
BOND DEFECTS	5	3.70	18	7.59	2	18.18
INTERCONNECTION DEFECTS	32	23.70	8	3.37		
DIE (MECHANICAL)	2	1.48	3	1.26	2	18.18
DEGRADED INPUT CKTRY	3	2.22	15	6.32	1	9.09

Table 26 then subdivides these die related failures into eight classification categories. As can be seen all categories of devices (bipolar, MOS and CMOS) exhibit less than .02% failures per thousand hours indicating a stable product. Tables 27 and 28 present detailed 1000 hour life test summaries for a sample of the total population of Table 25 for read only memories and random access memories, respectively by generic part number.

Table 29 provides greater detail on the p- and n- channel microprocessor data summarized in Table 25.

Microprocessors as can be seen, don't have the accumulated equivalent device operating hours as do other LSI (e.g., memories) technology categories. However, due to the complexity of large random access memories, these LSI circuits are used by IC suppliers from which to draw inferences regarding microprocessors, as we shall see later (Table 33). Tables 25 and 29 point to the need for more extensive testing regarding the microprocessor and the bit slice.

Tables 30 and 31 present greater detailed microprocessor life test data for 125°C and 70°C operating conditions, respectively. This data provides a larger base from which to draw conclusions than the selected data of Table 29 but is still inadequate. To add further depth to this presentation: Life test data provided by Intel and Fairchild Semiconductor is included in Tables 32 and 33, respectively. Table 32 presents extensive field test data gathered by Intel for 100,000 parts of the 8080 microprocessor and shows an amazingly low failure rate of 8-units out of 130 million device operating hours. Table 33, which was referred to earlier, presents life test data for the 2102 static 1K n-channel random access memory which Fairchild uses to draw inferences from for predicting the reliability of their F8 microprocessor because of the similar features of on-chip transistors, processing and die size.

100% environmental and mechanical reject summaries by technology are presented in Table 34. The screening tests which make up the environmental and mechanical test categories are delineated in Table 35. This data shows that SiGate MOS exhibit the lowest environmental reject rate followed by bipolar, MNOS, metal gate MOS and CMOS respectively. However, the population size of CMOS and MNOS memories is too small from which to draw conclusions. Mechanical screening attrition, in order of ascending reject rates are as follows: silicon gate MOS, metal gate MOS, bipolar, MNOS and CMOS. Data presented in Table 42 substantiates the high reject rates of CMOS memories. Table 36 presents the data of Table 35 in a different manner -- by package type -- and shows that memories encased in hermetic packages do indeed have a lower reject rate in both environmental and mechanical screening tests than do non-hermetic types.

Table 37 compares reject rates of metal gate and Silicon gate MOS memories and microprocessors. As can be seen Silicon gate devices exhibit a lower reject rate and thus higher level of reliability than do metal gate structures as first pointed out in Table 34. The rejects of Table 37 are categorized as die related rejects and performance related rejects, Tables 38 and 39 respectively. Silicon gate structures have lower die related and electrical rejects than do metal gate structures.

TABLE 27
READ ONLY MEMORY OPERATING
LIFE TEST SUMMARY BY GENERIC P/N (125°C)

BIPOLAR ROMS/PROMS (P)				
PART NUMBER	QTY	HOURS	NO.REJECTS	REASON FOR REJECT
MM5300 (P)	180	500	1	Wire-to-die short
MM5300 (P)	440	1000	1	--
MM5300 (P)	105	2000	0	--
MM5300 (P)	181	5000	1	Excessive leakage
82S129 (P)	1013	1000	19	Fuse growback
74S287 (P)	817	1000	2	Fuse growback
8256 (P)	554	1000	0	--
IM5600 (P)	164	1000	1	Initial failure
8223 (P)	43	1000	0	--
HA-0512 (P)	891	1000	4	Mechanical assembly (2)
HA-0512 (P)	50	1500	0	--
IM5603A (P)	26	500	0	--
IM5603A (P)	403	1000	0	--
IM5603A (P)	81	2000	0	--
IM5603A (P)	65	3000	0	--
MM5301 (P)	194	1000	2	Unknown
MM5301 (P)	76	5000	0	--
MM5604 (P)	201	1000	2	Metal short
MM5604 (P)	5	2000	0	--
MM5305 (P)	10	1000	0	--
MM5305 (P)	210	2000	0	--
MM5305 (P)	150	5000	0	--
MM5306 (P)	153	1000	0	--
MM5200	76	1000	0	--
MM5231	196	1000	1	Unknown
93434	102	1000	0	--
3301	154	1000	0	--
3301	67	2000	0	--
93406	81	1000	0	--
8205	99	1000	1	Oxide defect
8228	45	1000	0	--
MOS ROMS/PROMS				
3250	47	1000	0	--
3501	358	1000	0	--
1302	77	1000	0	--
4001	45	1000	0	--
1702A	620	1000	4	Charge loss
2708	440	2000	10	Charge loss

TABLE 28
RANDOM ACCESS MEMORY OPERATING LIFE
TEST SUMMARY BY GENERIC P/N (125°C)

PART NUMBER	QTY	HOURS	NO. REJECTS	REASON FOR REJECT
BIPOLAR				
82S06	45	1000	0	--
82S06	63	2000	2	Wire-to-die short
82S08	51	1000	1	Output latched at "0"
82S09	44	1000	0	--
93400	425	1000	0	--
93410	121	1000	0	--
93410	119	2000	1	Oxide pin hole
93410	45	4000	0	--
93415	60	500	0	--
93415	114	1000	2	Oxide(1),Dielectric Breakdown(1)
93415	91	2000	0	--
93415	38	3000	0	--
MM5531	120	1000	5	Unknown
MM5560	182	1000	1	Unknown
MOS				
1103	1303	1000	4	DC reject(3) Functional(1)
1103	204	2000	2	DC rejects
1103	290	3000	1	Excessive leakage current
1103	408	4000	8	DC rejects(6)Functional(2)
1103	72	5000	0	--
MK4096	205	1000	0	--
MK4096	40	2000	1	Lifted wire bond
MK4096	2394	4000	44	Metal short, oxide defect, lifted bond, open metal
IM6523(c)	423	1000	8	Oxide pin hole(1) Die attach defect(2)
IM6523(c)	32	3000	1	Oxide pin hole
IM6523(c)	73	5000	0	--
IM6508(c)	118	1000	1	Unknown
IM6508(c)	26	3000	1	Surface comtamination
IM6508	39	5000	1	Degraded
2107B	2699	168	2	Oxide defect(1)functional(1)
2107B	2443	1000	3	Oxide defect(1)fab defect(2)
2107B	1039	2000	0	--
2107B	640	5000	0	--
2105	210	1000	0	--
2101/A	350	1000	0	--
2111/A	300	1000	1	Catastrophic row/column failure
2112/A	350	1000	1	Catastrophic row/column failure
2102/A	1952	1000	2	Catastrophic
2102/A	105	5000	0	--
2102/A	230	9000	0	--
5101(C)	490	500	0	Address Input Failure
5101(C)	968	1000	2	Address Input Failure

C = CMOS

Table 29

Selected Microprocessor Life Data Summary

BASIC TECHNOLOGY	OP TYPE	COMPLEXITY (BITS)	TEST TYPE	STRESS LEVEL	NUMBER TESTED	PART HOURS	NUMBER FAILED
MOS (S. Gate)	p-Dyn	4	Rev Bias	125C	45	4.50E4	0
			Op Dyn	70C	1020	9.75E5	1
				125C	105	1.05E5	0
		8	Op Dyn	70C	1020	9.75E5	1
				85C	45	4.50E4	0
	n-Dyn	8	Op Dyn	85C	45	2.25E4	0
				125C	1286	5.71E5	4
				137C	-	5.62E3	0

Table 30

Microprocessor Operating Life Test Summary (125°C)

PART NUMBER	QTY	HOURS	NO. REJECTS	REASON FOR REJECT
4004	150	1,000	0	--
8080	50	500	0	--
8080	632	1,000	2	FUNCTIONAL
8080	80	2,000	0	--
8080	144	3,000	0	--
6800 (9 wafer lots)	358	10,000	9	7 FUNCTIONAL, 2 DC
6800	114	25,000	10	9 FUNCTIONAL, 2 DC
6800 (3 wafer lots)	101	30,000	2	FUNCTIONAL
2901 (4 date codes	80	2,000	0	--

TABLE 31

Microprocessor Operating Life Test Summary ($70^{o}C$)

PART NUMBER	QTY	HOURS	NUMBER OF REJECTS	REASON FOR REJECT
4004	30	500	0	-
	1,110	1,000	1	Open Interconnect
	30	2,000	0	-
8008	30	500	0	-
	960	1,000	1	Open Interconnect
	30	2,000	0	-
2650	45	500	0	-

TABLE 32

8080 Microprocessor Field Test Data

(Courtesy of Intel Corporation)

NUMBER OF DEVICES	OPERATING TIME/DEVICE	NUMBER OF FAILURES
100,000	1,280 hours	8

TOTAL DEVICE HOURS = 130,000,000

FAILURES:

4 failures due to V_{DD} high current damage.

1 failure due to 5000V spike on supply line.

2 functional failures.

1 package short

TABLE 33

Fairchild F8 Life Test Program

(Courtesy Fairchild Semiconductor Corporation)

- F8 process, die size and number of transistors is very similar to 2102.
  - 2102 8500 Transistors
  - F8 6000 Transistors
- Use Dynamic Operating Life Tests on 2102 as test vehicle in lieu of F8.
- No reliability screening prior to operating Life Test.

2102 LIFE TEST DATA (125°C)

	QTY TESTED	NUMBER HOURS	NUMBER REJECTS	REASON FOR FAILURE
CerDIP PACKAGE	40	1040	0	-
	51	1235	1	Transistor gate short @ 85 hours
	68	1235	1	Transistor gate short @ 85 hours
SIDE BRAZED PACKAGE	76	1045	1	Intermittent @ 85 hours
	41	1370	0	-
TOTAL DEVICE HOURS: 324,155				

TABLE 34

ENVIRONMENTAL/SCREENING
SUMMARY BY TECHNOLOGY

BASIC TECHNOLOGY	TEST	NUMBER TESTED	NUMBER FAILED	% DEF.
BIPOLAR	ENV	8,262	479	5.80
	MECH	2,681	45	1.68
MOS	ENV	6,737	914	13.60
	MECH	6,969	10	.14
SiGate MOS	ENV	21,213	726	3.42
	MECH	408	0	0.00
CMOS	ENV	158	54	34.20
	MECH	97	6	6.19
MNOS	ENV	290	30	10.30
	MECH	29,604	1,009	3.41

TABLE 35

SCREEN TEST CATEGORIZATION

ENVIRONMENTAL TESTS	MECHANICAL TESTS
Accelerated Life	Bond Strength
Autoclave	Constant Acceleration
Barometric Pressure	Lead Integrity
Dew Point	Mechanical Shock
Immersion	Power Cycling
Moisture Resistance	Solderability
Salt Atmosphere	Solder Heat
Seal (Hermeticity)	Visual Inspection
Temperature Cycling	Vibration Fatigue
Thermal Shock	Vibration Var. Freq.
	X-Ray

TABLE 36

ENVIRONMENTAL/SCREENING PACKAGE SUMMARY

PACKAGE TYPE	TEST	NUMBER TESTED	NUMBER FAILED	% DEF.
NONHERMETIC	ENV	2056	147	7.15
	MECH	332	4	1.20
HERMETIC	ENV	5475	224	4.09
	MECH	8913	31	.35

Table 37

Metal Gate Versus Silicon
Gate MOS Memory Attrition Comparison

GATE MATERIAL	TECHNOLOGY	QTY TESTED	QTY REJECTED	% REJECTED
METAL	PMOS	3,466	53	1.53
	NMOS	382	5	1.31
	TOTAL	3,848	58	1.51
SI GATE	PMOS MEMORY	10,942	48	.44
	PMOS µp	2,235	2	.09
	NMOS MEMORY	13,165	25	.19
	NMOS µp	1,331	4	.30
	TOTAL	27,673	79	.29%

Table 38

Die Related Reject Summary for
Silicon Versus Metal Gate Memory Devices

FAILURE CLASSIFICATION	METAL GATE		SILICON GATE	
	NUMBER DEVICES	%	NUMBER DEVICES	%
SURFACE DEFECTS	50	41.66	19	40.41
OXIDE DEFECTS	37	30.85	8	17.02
DIFFUSION DEFECTS	15	12.50	2	4.25
METALLIZATION DEFECTS	--	--	3	6.39
BOND DEFECTS	4	3.33	1	2.13
INTERCONNECTION DEFECTS	2	1.66	8	17.02
DIE (MECHANICAL)	--	--	3	6.39
DEGRADED INPUT CKTRY	12	10.00	3	6.39

Table 39

Electrical Reject Summary for
Silicon Versus Metal Gate Memory Devices

FAILURE CLASSIFICATION	METAL GATE		SILICON GATE	
	NUMBER DEVICES	%	NUMBER DEVICES	%
FUNCTIONAL REJECT	23	39.98	13	34.21
D.C. REJECT	6	10.17	12	31.58
PATTERN SENSITIVE	5	7.48	3	7.89
DATA LOSS	24	41.38	10	26.32

Table 40

Electrical Test
(Incoming Inspection) Summary

MEMORIES			
CATEGORY	QTY TESTED	QTY REJECTED	% REJECTED
Bipolar S/R	21,503	552	2.6
MOS S/R	8,424	621	7.4
Bipolar ROMs	3,655	397	10.9
Bipolar LSI	1,720	28	1.6
Bipolar RAMs	7,992	555	6.9
MOS RAMs	35,364	785	2.2
SSI TTL	198,264	2,228	1.1
MSI TTL	32,813	941	2.87

TABLE 41

ELECTRICAL TEST

BI ELECTRICAL TEST SUMMARY

MEMORIES						
CATEGORY	QTY TESTED	QTY REJECTED	% REJECT	EM-1	EM-2	OTHER
SSI	3,679	245	6.7	11	194	40
MSI	1,728	85	4.9	7	70	8
Bipolar S/R	486	14	2.9	5	9	0
MOS S/R	29,558	1,452	4.9	1,452	0	0
Bipolar ROMs	1,727	57	3.3	17	40	0
Bipolar RAMs	92	1	1.0	0	1	0
MOS RAMs	1,997	346	17.3	327	19	0

TABLE 42

RELIABILITY SCREENING

TEST SUMMARY

MEMORIES								
CATEGORY	QTY TESTED	QTY REJ.	% REJ.	H	EM-1	EM-2	X	O
SSI TTL	28100	1578	5.6%	249	207	671	333	118
MSI TTL	13847	1545	11.2%	361	221	461	378	75
Bipolar S/R	38794	967	2.5%	107	224	587	20	29
MOS S/R	9924	1208	12.2%	0	182	928	98	0
Bipolar LSI	86	40	46.5%	13	20	7	NT	0
Bipolar ROM	3367	171	5.1%	92	57	17	2	3
Bipolar RAM	5697	692	12.2%	6	320	307	38	21
CMOS RAM	2047	575	28.1%	197	140	129	106	3

NT = Not Tested

100% Screening Attrition Summaries for receiving inspection tests (electrical test only), electrical tests -- burn-in (168 hours @125°C) -- electrical test, and 100% reliability screening tests (Method 5004 of MIL-STD-883 Class B) are presented in Tables 40, 41 and 42 respectively for bipolar and MOS RAMs. For comparative purposes the attrition for SSI and MSI TTL functions are included in each table.

Incoming Inspection test results (Table 40) show that bipolar LSI (ALUs), MOS RAMs and bipolar shift registers have low reject rates and these are comparable with SSI and MSI TTL functions. Bipolar ROMs and RAMs and MOS shift registers have 2-4 times higher reject rates.

The combination of burn-in and electrical tests provides an effective means for weeding out potentially weak components. The data of Table 41 does not show an increase in reject rates from that of Table 40; as would usually be expected except for MOS RAMs -- the failure rate of which increases dramatically. Some possible reasons for this are different constituent generic device types, and smaller population size than that of Table 40. An interesting feature is gleaned from comparing the SSI/MSI TTL data with the memory data in Table 41. The SSI and MSI TTL reject rate is higher for this screening sequence than it is for memories, with the exception of MOS RAMs. Note the effectivity of pre burn-in electrical measurements in weeding out supposedly good product prior to burn-in for MOS shift registers and RAMs.

Parts subjected to MIL-STD-883 Class B 100% screening (Table 42) exhibit attrition rates from 2.5% for bipolar shift registers to 46.5% for a small population of ALUs. Bipolar ROMs have reject rates comparable with TTL SSI devices and bipolar RAMs and MOS shift registers have reject rates similar to TTL MSI devices. CMOS RAMs have a high reject rate as was shown earlier in Table 34. The data shows that burn-in is an effective screen as shown by pre and post burn-in electrical measurement reject rates in combination with hermeticity and x-ray testing. The measurement points listed (hermeticity, pre- and post-burn-in electrical, x-ray and others) are the places in the screening sequence at which rejects can be identified. The pre-burn-in electrical measurements pick up stabilization bake, temperature cycling and centrifuge rejects.

Conclusion

The results of the test data presented herein demonstrate that 100% component screening is definitely required to maximize component reliability and minimize resultant field repair costs.

Memories exhibit similar reject rates when subjected to 100% screening tests as do SSI and MSI TTL circuits. However, various technologies have higher reject rates than others. Silicon gate MOS structures have lower reject rates than do metal gate structures; hermetic encased products have lower reject rates than do non-hermetic parts; bipolar memories generally have lower reject rates than do MOS memories; and CMOS memories exhibit the highest reject rates. Life tests conducted at 125°C for 1000 hours demonstrate the stability of both bipolar and MOS memories and microprocessors.

Reliability test data taken to date, indicates that the inherent reliability of microprocessors is no worse than that for memories and other LSI devices. In fact, the limited amount of data taken so far indicates microprocessor reliability is better than for other LSI devices. However, from an electrical testing viewpoint the industry doesn't as yet have a viable and effective means of properly testing a microprocessor. As such, much more test data needs to be generated on microprocessors and communication of both laboratory and field reliability data is imperative in understanding the inherent reliability and failure modes of microprocessors.

Test data depicted herein demonstrates the need for some form of reliability improvement program. The particular screening tests to be performed are determined by an evaluation of the intended application and the end product's desired warranty conditions.