MAINTENANCE MANUAL VOLUME I
TR-48 ANALOG COMPUTER
MODEL 45.034

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LONG BRANCH NEW JERSEY


$$
\begin{aligned}
& \text { Does not apply see page } 66 \\
& \text { Fig. 4.4-1 }
\end{aligned}
$$

NOTICE

Figure 4.4-1 PATCH PANEL READOUT MODULE WIRING:

External Scope

Plotter/ Recorder Repetitive Operation Display


Figure 4.4-1

## NOTICE

```
~ Page v (List of Contents), Section IV, Paragraph 4
Change title as follows:
PATCH PANEL READOUT MODULE 12.763-1
```

| Page 6, Paragraph 5c. | Change first sentence as follows: |
| :--- | :--- |
|  | This connector provides terminations for slaving |
|  | two or more computers together for common mode- |
|  | control (except for Pot-Set PS mode) fron one |
|  | computer. |

Page 10, Paragraph 5d., SL (Slave) Section
Change description as follows:
... on the slaved computer. The slaved computer then responds to the selected modes (except PotSet which can not be slaved) of the master computer.

Page 10, Paragraph 5e., PS (Pot-Set) Section
Change description as follows:
(The summing junctions of the integrator networks are connected to $\pm$ ground by means of relay contacts.)

Page 64, Section IV, Paragraph 4 - Change paragraph title to:
PATCH PANEL READOUT MODULE 12.763-1
Add following information to last sentence of second paragraph:
... connected to J65, two Repetitive Operation Display unit inputs $\left(Y_{3}\right.$ and $\left.Y_{4}\right)$ and ten trunk ...

Page 12, Paragraph 7b。 Change first sentence as follows: ...TR-48 is a Model 51. 114 Service Shelf.

NOTE

SLAVING TR-48 COMPUTERS

## 1. SLAVING TWO TR-48 COMPUTERS

When slaving two TR-48 computers connect the 19.261 cable between the J61 plug connectors on the rear of each computer (Figure 1.5-1). Determine the computer to be slaved and depress the SL Mode Control button. On the slaved computer reference units (behind Attenuator Panel) remove the patch cord from the INT REF termination and place it in the EXT REF termination (patch cord now between EXT REF and REF IN terminations); this slaves the two computer reference supplies in addition to the computer modes.
2. SLAVE THREE OR MORE TR-48 COMPUTERS

The procedure is similar to the above except the slave cables from J61 of each computer terminate in the 47.040 Junction Box. (See Page 6) As described above, the slaved computer SL Mode Control buttons are depressed and the EXT REF to REF IN connection is made in each of the slaved computers. Note, that the master computer 19.261 slave cable must be terminated in the connector labeled MASTER (Position 1 ) on the 47.040 Junction Box. The slaved computers' 19.261 cables may be connected to any of the remaining connectors.

Page AI-26 Add Item 21 R9 Resistor, Fixed, Composition: 100 ohms $+10 \%$, IW; Allen-Bradley GB (EAI $627 \overline{101}$ 1) A Category

## NOTICE

1. Prior to setting up any D.F.G. (including the V.D.F.G.), the computer plus and minus reference supplies must be carefully balanced.
2. The D.C. Error Test Setup waveform for the Quarter-Square multiplier shown in Figure 2.3-5b shows the optimum error curve after DFG adjustment. Note, however, that a maximum allowable error deviation from +80 MV to -80 MV still maintains the unit within the allowable accuracy limits.
3. When following the typical VDFG Setup Procedure described on Page 46, the $X$ inputs of $+1,+2,+3$, etc. should be obtained from the output of an amplifier rather than directly from the wiper of a potentiometer. The amplifier permits the setting of the potentiometer under load in the computer Pot Set mode and provides a constant wiper load (the impedance of the VDFG changes with input magnitude).

Page 14 Paragraph la Technical Data，after sub－title Noise and Ripple： add＂（peak－to－peak）＂and after sub－title Offset Voltage change parenthetical notation to read＂（amplifier balanced，$\left.R_{f}=10 \mathrm{~K}\right)$＂
Page 17 Equation 2．1－2 should be $e_{o}=-\frac{Z_{f}}{Z_{\text {in }}} e_{\text {in }}$
last equation on page should be $e_{o}=-\frac{10 K}{100 K} e_{i n}=-0.1 e_{i n}$

Page 33 The second sentence of Paragraph（1）（d）should read＂This wave－ form should not exceed 160 millivolts peak－to－peak．＂

Figure 2．4－4 Potentiometer $⿰ ⿰ 三 丨 ⿰ 丨 三 1$（ $X^{2}$ DFG Test Setup）should be set for 0.050 not 0.500 as indicated．

Page 41 Delete the second，third，and fourth paragraphs under the Para－ graph heading＂a．Operation Considerations＂and replace with the following paragraphs．＂Note that the maximum output of the 16．276 Log $X$ Unit occurs when the absolute value of $X$ is 10 volts． The output is therefore $5 \log _{10} 1010=10$ volts，plus or minus depending on the generator used．The $1 / 2$ Log $X$ Unit，with an output equal to $1 / 2$ of the $\log X$ generator has a maximum absolute value output of 5 volts．

In Figure 2．5－2，the upper portion illustrates the patching for a plus $X$ input Log DFG and the lower portion shows the patching for a minus $X$ input DFG．＂

Figure 2．6－2 Title should read Figure 2．6－2 VDFG＂MODEL＂16．274 Components．
Figure 3．2－1－8 volt 1.5 Amp fuse on panel face should be＂2 AMP＂
Page 49 Paragraph 7b First Paragraph，Third sentence should read＇When the computer is switched to the Pot－Set mode relay voltage is applied to P1－R；if K2 is energized，K1 energizes and connects the four grounded to the +10 volt reference bus．${ }^{14}$

Page 52 Paragraph（́），Last sentence should read＂Typical switching time for a normal comparator is 3.5 milliseconds．＂

Paragraph（e），Last sentence should read＂Typical value of 0.5 millivolts．＂

## ERRATA cont'd

[^0]
## NOT ICE

In later models of the TR-48 Computer, the Variable DFG's, Models 16.154 and 16.156 , have been moved from the left-hand to the righthand side of the TR-48 rack. To accommodate this change, the DFG's have been inverted to allow access to the variable-resistor screwdriver adjustments. The 16.154-2 and $16.156-2$ variations incorporate this change and are identical with the $16.154-1$ and 16.156-1 variations respectively, except for the use of a new card to permit wiring to the rear connector and the use of a different cover and connector block. Note that Figure 2.6-1 shows the VDFG's mounted on the left-hand side of the TR-48 rack. The relative position and the numerical sequence of the VDFG's in relation to the prepatch panel is shown in Figure 1.

| + | - | + | - | + | - | + | - | + | - |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |
| V | V | V | V | V | V | V | V | V | V |  |
| Panel |  |  |  |  |  |  |  |  |  |  |
| Side | D | D | D | D | D | D | D | D | D | D |
| F | F | F | F | F | F | F | F | F | F |  |
| G | G | G | G | G | G | G | G | G | G |  |
| $(2)$ | $(3)$ | $(4)$ | $(5)$ | $(6)$ | $(7)$ | $(8)$ | $(9)$ | $(10)$ |  |  |

Figure 1. VDFG Location

1. NON-REPETITIVE OPERATION


Time Scale: Normal
Feedback Capacitor $=10 \mathrm{MFD}$


Time Scale: $0.1 \beta$
Feedback Capacitor $=1 \mathrm{MFD}$
2. REPETITIVE OPERATION


Rep Op Time Scale: Normal Feedback Capacitor $=0.02$ MFD


Rep Op Time Scale: $0.1 \beta$ Feedback Capacitor $=0.002$ MFD

## 3. SPECIAL OPERATION

a. Patching for an integrator that stays in the operate mode while other integrators are in Repetitive Operation:


Time Scale: $0.1 \beta$
Feedback Capacitor $=1$ MFD

Patch the reset relay termination to the RS termination on the Readout Panel 12.763. The integrator is in the operate mode as long as the computer is in repetitive operation. The integrator is placed in the reset mode by placing the computer in the reset mode.

b. Patching for an integrator that is in the reset mode when the computer is in the operate mode and when the computer is in reset, the integrator is in operate:


1. Cross patch the OPR-RESET terminations.
2. All other patching is as shown under NONREPETITIVE and REPETITIVE OPERATION.

The Dual Integrator Network 12.764 patching block configuration has been modified to further simplify the TR-48 Integrator patching. The old time scale area (TS) of the patching block ( see below ) has been sub-divided into two areas designated NORM and SPEC. For normal repetitive operation a two connector bottle plug is placed in the SPEC area; the word NORM remains exposed thus indicating normal operation. Placing a two connector bottle plug in the NORM area, exposing SPEC (indicating special), the integrator is placed in the operate mode when the Rep-Op button is depressed and remains in that mode until the computer mode is changed.


## NOTICE

| Page 30 | Restriction (2) for division should read: "The divisor must be positive." |
| :---: | :---: |
| Page 34 | The second sentence of the first footnote (*) should read: "As an example---card 1 conducts; if both are negative only card 3 conducts." |
| Figure 2.3-7 d and e. The connections from the output of the amplifier ( connected to the TDVM) to termination B should go from the output of the amplifier to termination $+\mathbb{U}$. |  |
| Figure 3.2-1 | Regulated Power Supply 10. 203. <br> Change the $-8 V$ Fuse rating shown on the front panel to read 3 AMPS. |
| Page 56, Paragraph 2. a. Change the Max Load Current for the -8 V dc supply to read 3.0 AMPS . |  |
| Page AI-15 | Add following description: <br> Resistor, Fixed, Wirewound: 1 ohm $\pm 10 \%, 2 W$; International <br> Resistance Co. Type BW-2 (EAI 636127 0). |
| Page AI-22 | Item 3, delete Ref. Desig. R5 and R42. <br> Add new description for R5 and R42 as follows: <br> Resistor, Variable, Wirewound: IK ohms $\pm 20 \%$; CTC Type 115 <br> (EAI A642 569 O). |
| Page AI-23 | Item 17, change description of R19, R22 as follows: <br> Resistor, Variable, Wirewound: 100 ohms $\pm 20 \%$, CTC Type 115 <br> (EAI A642 577 O). |
| Page AI-24 | Item 24, Item 3, delete Ref. Desig. R5 and R42. Add new description for R5 and R42 as follows: Resistor, Variable, Wirewound: 2 K ohms $\pm \mathbf{2 0 \%}$; CTC Type 115 (EAI A642 580 O). |
| Page AI-25 | Item 17, change description of R19, R22 as follows: <br> Resistor, Variable, Wirewound: 500 ohms $\pm 20 \%$; CTC Type 115 <br> (EAI 642579 0). |
| Page AI-29 | Item 5, change description of DS1 as follows: <br> Lamp, Incandescent: Hudson Lamp Co. 2307 (EAI A578 047 1). |
| Page AI-32 | Change descriptions of Items 6 and 7 as follows: <br> Item 6 R1. Resistor, Fixed, Wirewound, Precision: 82,000 <br> ohms $\pm 1 \%$; Resistance Products Co. PB Type (EAI A638 541 O). |
|  | Item 7 R2. Resistor, Fixed, Wirewound, Precision: 100,000 ohms $\pm 1 \%$; Resistance Products Co. PB Type (EAI A638 483 3). |

Page
INTRODUCT ION
SECTION I - TR-48 ANALOG COMPUTER

1. GENERAL DESCRIPIION ..... 2
2. TECHNICAL AND PHYSICAL DATA ..... 2
3. EQUIPNENI COMPIEMENI ..... 3
4. INSTALLATION AND PRELIMINARY CHECKS ..... 5
5. EXTERNAL CONNECTIONS ..... 6
a. General ..... 6
b. A.C. Connectors (AC1, AC2, AC3) ..... 6
c. Slave and Trunk Connector (J61) ..... 6
d. Trunk-Function Switch Connectors (J62, J63, and J64) .. ..... 6
e. Recorder/Plotter Connector (J65) ..... 7
f. Oscilloscope Connector (J66) ..... 7
6. OPFRATION ..... 7
a. POWER Switch ..... 8
b. Multi-range Voltmeter Controls ..... 8
c. Signal Selectors ..... 8
d. Mode Control Pushbuttons ..... 9
e. Repetitive-Operation Timing Selector ..... 10
f. Overload Indicators ..... 11
g. Patch Panel Engage/Disengage Switch ..... 11
Page
7. TR-48 MAINTENANCE ..... 11
g. General Information ..... 11
b. Maintenance Accessories and Equipment ..... 12
c. Applicable Drawings ..... 13
SECTION II - COMPUIING COMPONENTS AND ACCESSORIES
8. DUAL D.C. AMPLIFIER 6.514 ..... 14
a. Technical Data ..... 14
b. Operating Considerations ..... 14
\&. Theory of Operation ..... 16
d. Maintenance and Test Procedures ..... 20
9. DUAL INIEGRATOR NETWORK 12.764 ..... 23
․ Operating Considerations ..... 24
b. Theory of Operation ..... 25
c. Maintenance ..... 27
d. Trouble Analysis ..... 28
10. QUARTER-SQUARE MUITIPLIER 7.099 ..... 29
a. Operating Considerations ..... 30
b. Theory of Operation ..... 30
c. Maintenance and Test Procedures ..... 33
11. $\mathrm{X}^{2}$ DIODE FUNCTION GENERATOR 16.275 ..... 37
a. Operating Considerations ..... 37
b. Theory of Operation ..... 38

## CONTENIS (Cont)

Page
4. $X^{2}$ DIODE FUNCTION GENERATOR 16.275 (Continued)
c. Maintenance and Test Procedures ..... 38
5. LOG $X(16.276)$ AND $1 / 2$ LOG $X(16.281)$ DIODE FUNCTION GENERATORS ..... 40
a. Operating Considerations ..... 41
b. Theory of Operation ..... 41
c. Maintenance and Test Procedures ..... 42
6. VARIABLE DIODE FUNCTION GENERATOR 16.274 ..... 45
a. Operating Considerations ..... 45
b. Theory of Operation ..... 47
c. Maintenance and Test Procedures ..... 47
7. COEFFICIENI SETTING ATTENUATOR GROUP 2.440 ..... 49
g. General ..... 49
b. Circuit Description ..... 49
c. Maintenance ..... 49
8. SIGNAL COMPARATOR 40.404 ..... 50
a. General ..... 50
b. Comparator Patching ..... 50
c. Circuit Description ..... 51
d. Maintenance and Test Procedures ..... 51
9. FUNCIION SWITCH GROUP 2.462 ..... 52
SECTION III - POWER AND REFERENCE CIRCUITS

1. REGULATED POWER SUPPLY 10.200 ..... 54

## CONTENIS (Cont)

Page
a. General ..... 54
b. Circuit Description ..... 54
c. Routine Maintenance and Adjustments ..... 55
2. TDVM POWER SUPPLY 10.203 ..... 55
g. General ..... 55
b. Circuit Description ..... 56
3. REFERENCE REGULATOR 43.104 ..... 56
a. General ..... 56
b. Reference Patching ..... 57
c. Circuit Description ..... 57
d. Routine Maintenance and Adjustment ..... 57
4. DUAL D.C. AMPLIFIER 6.282 ..... 58
a. General ..... 58
SECIION IV - CONIROL AND MONITORING CIRCUITS

1. CONTROL PANEL 20.790 ..... 59
a. General ..... 59
b. Monitoring Circuitry ..... 59
c. Computer Mode Control ..... 60
2. DIGITAL VOITMETER 26.183 ..... 62
3. REPETITIVE OPERATION ..... 62
a. General ..... 62

## CONTENIS (Cont)

## Page

## 3. REPEIITIVE OPERATION (Continued)

b. Repetitive Operation Mode ..................................... 62
c. Timing Unit and Rep Op Control Module .................. 62
d. Repetitive Operation Timing Adjustments ................ 63
4. PATCH PANEL READOUT MODULE 12.762 ..6.4......…............ 36

APPENDIX I - REPLACEABLE PARTS LIST ......................................... AI-1

| Figure Number | Title |
| :---: | :---: |
| 1.1-1 | Typical TR-48, Front View |
| 1.3-1 | TR-48 Computer (Panels and Covers Removed to Show Component Locations) |
| 1.4-1 | TR-48 Rear View, Cover Plates Removed |
| 1.5-1 | Plug Plate, Rear TR-48 |
| 1.5-2 | Readout Address for 12.762 Trunk Module |
| 1.6-1 | TR-48 Control Panel |
| 1.7-1 | Test Shelf in Use |
| 2.1-1 | Dual D.C. Amplifier, Model 6.514 |
| 2.1-2 | Amplifier Patching, Typical Configurations |
| 2.1-3 | Operational Amplifier, Block Diagram |
| 2.1-4 | High-Gain D.C. Amplifier, Simplified Block Diagram |
| 2.1-5 | High-Gain Amplifier, Simplified Schematic |
| 2.1-6 | Amplifier 6.514, Simplified Schematic |
| 2.1-7 | Output Current Test Circuit |
| 2.1-8 | Amplifier Dynamic Error Test Setup |
| 2.1-9 | Amplifier Stabilizer Test Setup |
| 2.1-10 | Properly Functioning Overload Stabilizer Waveshapes |
| 2.2-1 | Dual Integrator Network, Model 12.764 |
| 2.2-2 | Integrator, Simplified Schematic |
| 2.2-3 | Integrator Operational Test Setup |
| 2.2-4 | IC Resistor-Ratio Check Circuit |

ILLUSTRATIONS (Cont)

| Figure Number | Titie |
| :---: | :---: |
| 2.2-5 | Integrator Drift Rate Test Setup |
| 2.3-1 | Quarter-Square Multiplier, Model 7.099 |
| 2.3-2 | Multipiscation Patching |
| 2.3-3 | Simplified Partial-Schematic of One Squaring Circuit |
| 2.3-4 | Multiplication Patching and Simplified Schematic |
| 2.3-5 | Multiplier DC Error Mest Setup and Typical Waveform |
| 2.3-6 | 1 KC Waverorm |
| $2.3-7$ | Multiplier Adjustment Location and Test Setup Patching |
| 2.4-1 | $\mathrm{X}^{2}$ DFG, Model 16.275 |
| 2.4-2 | $+x^{2} / 10$ and $-x^{2} / 10$ Patching Configurations |
| 2.4-3 | Negative Input $\mathrm{X}^{2}$ DF'G, Simplified Schematic |
| 2.4-4 | $\mathrm{X}^{2}$ DFG Test Setup |
| 2.4--5 | $X^{2}$ DFG Adjuctment Location and Patching |
| 2.5-1 | $\log X$ DFG, Model $16.276(1 / 2 \mathrm{Log} X$ DFG, 16.281 Similar $)$ |
| 2.5-2 | Log X DFG Patching Diagram (1/2 Log X DFG Similar) |
| 2.5-3 | Positive Input Log X DFG Circuit, Simplified Schematic |
| 2.5-4 | Graphical Inputosomutht Compsrison of Positive Input Log X DFG |
| 2.5-5 | Log X DPG Dynamin Error Test Circuit |
| 2.5-6 | Log X Adjustment Location and Test Setup Patching |
| 2.6-1 | $\pm$ VDFG Unit Location and Chassis in Setup Position |
| 2.6-2 | VDFG, Model 16.274 Components |
| 2.6-3 | VDFG Patching Block and Simplified Schematic |

## ILLUSTRATIONS (Cont)

Figure
Number
2.6-4
2.6-5
2.6-6
2.6-7
2.6-8
2.7-1
2.8-1
2.8-2
3.1-1
3.2-1
3.3-1
3.3-2
4.1-1
4.3-1
4.3-2
4.4-1

## Title

+VDFG and -VDFG Patching and +VDFG, Simplified Schematic
$\pm$ VDFG Patching
Sample +VDFG Output Curve
-VDFG Operational Test Setup
+VDFG Operational Test Setup
Coefficient Setting Attenuator, Model 42.283
Signal Comparator, Model 40.404
Signal Comparator Test Setup
Regulated Power Supply 10.200
Regulated Power Supply 10.203
Reference Regulator 43.104
TR-48 Reference Circuits, Simplified Schematic
TR-48 Monitoring Circuits, Block Diagram
Rep-Op Timing Unit, Model 36.082
Repetitive Operation Timing Adjustments
Patch Panel Readout Module Wiring

## INTRODUCTION

## TR-48 Manuals

Operation, programming instructions, and maintenance data for the TR-48 Analog Computer, designed and manufactured by EAI, are contained in two separate publications provided with each computer. This handbook is intended to serve as a maintenance manual for the instrument, and is arranged in accordance with that use. The manual includes technical and physical descriptions of the computer and its plugin components, circuit theory and analysis of all components, and recommended test and adjustment procedures. In addition, this handbook contains parts lists and schematic and wiring diagrams for the $T R-48$. Sufficient operational data and patching instructions are given to permit the maintenance technician to set up and operate the instrument in accordance with the recommended test and adjustment procedures. Complete operating, patching, and programming instructions, in addition to fundamental analog applications, are contained in a separate Operator's Manual. (The Operator's Manual is also useful as an introduction to analog computation and simulation.)

The maintenance handbook is divided into four SECTIONS as follows:

SECTION I

SECTION II

SECTIONS III and IV

Contains the technical and physical description of the computer and plug-in components, describes installation and preliminary check procedures, lists and describes all operational controls and indicators, and outlines (in general terms) maintenance data, required test equipment, and a maintenance program for the TR-48.

Covers all computing components and accessories. For each component this section describes operational specifications, patching and setup instructions, circuit analysis, and a test and adjustment procedure designed to quickly verify component performance.

Provide generally the same data as above for POWER AND REFERENCE circuits, and the CONTROL AND MONITORING circuits, respectively.

The TR-48 replaceable parts lists are contained in Appendix I bound in the rear of this handbook. Electrical drawings are contained in Volume II.

## SECTION I

TR-48 ANALOG COMPUTER

1. GENERAL DESCRIPTION

The PACE ${ }^{(3)}$ TR-48 (Figure 1.1-1) is a solid-state, general-purpose, analog computer housed in a single cabinet suitable for installation on a laboratory cart or tabletop. The cabinet is composed of three sections, and houses all computing components, power supplies, and control and monitoring circuits necessary for relatively largescale problem solving capabilities.

The TR-48 contains space for 48 operational amplifiers ( 24 dual units), 60 manually operated, coefficient-setting attenuators, and non-linear components such as diode function generators and electronic multipliers. (See Paragraph 3 of this section for a complete component list.)

Computing components in the TR-48 are housed in the center section of the cabinet. (The component front panels form the computer patch bay.) Each TR-48 is factorywired to accept the full complement of computing components. Thus expansion to a larger system simply involves plugging in additional components into the center area.

The left-hand section of the computer contains the control and monitoring circuits of the TR-48. These include a 4 -place electronic digital voltmeter, a multi-range voltmeter, and push-button selection systems for readout and computer mode control.

The right-hand panel of the TR-48 contains the coefficient-setting attenuators, and function switches. Behind this panel are mounted the computer reference voltage components, and operational power supplies.

The component front panels are normally covered by the pre-patch panel, a $1350-$ hole board that permits pre-patching to be performed away from the computer. The patch bay and associated pre-patch board provide a central terminal point to permit connecting the TR-48 computing components into any desired configuration.

The rear panel of the computer contains connectors for remote control, recorder terminations, slaved operation, and AC power input.
2. TECHNICAL AND PHYSICAL DATA

Computer Type D-C Analog
Number of Components Cabinet contains 60 wired crades
(See SECTION I, Paragraph 3)
System Reference $\quad \pm 10$ volts (internally generated)
Primary Power Requirements
115 or 230 volts, 50 to 60 cycles. Fully expanded computer requires 150 watts.

Operational Voltage Levels (Internally Generated)

| Computing <br> Components | Digital Voltmeter | Relays |
| :--- | :---: | :---: |
| $\pm 15 \mathrm{~V} \mathrm{d-c}$ | $\pm 15 \mathrm{~V} \mathrm{d-c}$ | - |
| $+30 \mathrm{~V} \mathrm{d-c}$ | $+30 \mathrm{~V} \mathrm{d-c}$ | - |
| - | $+2 \mathrm{~V} \mathrm{d-c}$ | - |
| - | $-8 \mathrm{~V} \mathrm{d-c}$ | - |
| $6.3 \mathrm{~V} \mathrm{a-c}$ | $6.3 \mathrm{~V} \mathrm{a-c}$ | - |
| - | - | $20 \mathrm{~V} \mathrm{~d}-\mathrm{c}$ <br> (nominal value) |

Computer Physical Dimensions
Width..........................46-1/2 inches
Height.......................... 24 inches
Depth........................... 20 inches
Weight (Fully Expanded)..... 320 pounds
3. EQUIPMENT COMPLEMENT

As previously indicated, each TR-48 Computer is factory-wired for a full complement of computing components. With this arrangement, expansion to a larger system can be accomplished by plugging in additional components.

Figure 1.3-1 illustrates the computer component cradles and those components that each cradle is wired to accept. It should be noted that this illustration shows the standard arrangement for the TR-48. In accordance with individual system requirements, the cabinet may be wired for other component arrangements. In these cases, a supplemental layout wiring diagram is provided with the computer to indicate the particular cradle configuration.

For a complete list of TR-48 components, refer to Table 1.3-1 and Figure 1.3-1.


FIGURE I.I-I TYPICAL TR-48, FRONT VIEW


FIGURE 1.3-1
TR-48 COMPUTER (PANELS AND COVERS OPEN TO SHOW


| Component | Model No |
| :---: | :---: |
| TR-48 COMPUIING COMPONENTS |  |
| 1. Dual D-C Amplifier | 6.514 |
| 2. Dual Integrator Network | 12.764 |
| 3. Guarter-Square Multiplier (Standard) or Quarter-Square Nultiplier (High Accuracy) | $\begin{aligned} & 7.099 \\ & 7.096 \\ & \hline \end{aligned}$ |
| 4. $X^{2}$ Diode Function Cenerat or, <br> Log X Diode Function Generator, or $1 / 2 \log X$ Diode Function Generator | 16.275 16.276 16.281 |
| 5. Variable Diode Function Generator | 16.274 |
| 6. Readout Patching Module | 12.763 |
| 7. Trunk Patching Module (7A In Trunks) | 12.762 |
| 8. Function Switch Group | 12.766 |
| 9. Signal Comparat or | 40.404 |
| 10. Coefficient Setting Attenuat or Group | 42.283 |
| TR-48 POWER AND REFERENCE SUPPLIES |  |
| 11. TDVM Power Supply | 10.203 |
| 12. Regulated Power Supply | 10.200 |
| 13. Reference Regulator | 43.104 |
| 14. Dual D-C Amplifier | 6.282 |
| TR-48 CONEROL AND MONITORING COMPONENTS |  |
| 15. Repetitive Operation Group | 2.424 |
| 16. Digital Voltmeter (TDVM) | 26.183 |
| 17. Relay Panel | 11.148 |
| 18. Null Potentiometer* | 20.285 |
| TR-48 OPERATING AND MAINIENANCE ACCESSORIES |  |
| 19. Pre-Patch Panel | 5.183 |
| 20. Patching Kit (Bottle Plugs, and Patch Cords) | 5.171 |
| 21. Service Shelf | 51.114 |
| 22. AoC. Power Cable | 510.040 |

*Used only when computer has no Digital Voltmeter (TR-48-0)

## 4. INSTALLATION AND PRELIMINARY CHECKS

The TR-48 Computer is completely solid-state; thus, it requires very little primary power and no cooling other than that provided by normal working environments. The computer may be operated in any area that is not subjected to excessive dust or dirt or temperature extremes, and is relatively free from vibration.

After the computer is unpacked from its shipping container, a visual inspection should be made to ensure that no damage has occurred during shipment. Check all plug-in components for proper seating.

The computer is designed for operation from a 50 to 60 cyele a-c supply. The a-c circuits are factory-wired for 115 volt or 230 volt operation as specified in the purchase order for the computer. (Figure 1.4-1 and Drawing COO2 476 OA contain wiring requirements for operating from the 230 volt power source.) A 3-wire power cable is furnished with the TR-48 for connecting a-c power to AC1 (the lowest connector on the plug mounting-plate on the rear of the computer). The other end of the a-c power cable is terminated in a 3-prong plug for connection to a standard grounded and polarized receptacle. If the primary power line to which the computer is to be connected is not equipped with a three-terminal receptacle, a three-pole adapter must be used. In this case two precautions must be observed: (1) The power cable must be connected so that the neutral side of the a-c line is connected to the a-c common side of the primary power wiring in the computer; and (2) The ground wire on the adaptor must be connected to an earth ground. Failure to connect the a-c circuits in this manner will result in a safety hazard if the hot side of the computer primary power circuits should ever be inadvertently shorted to the computer cabinet. Also, the d-c amplifiers will have an excessively high noise level if the computer frame is not grounded.

After power is connected, the computer should be turned on, switched to the pot set mode (see SECTION I, Paragraph 6 for description of controls), and allowed to warm up for 15 minutes or so.

It should be noted that each TR-48 is completely checked and adjusted prior to shipment, and the computer should be ready for operation upon receipt. However, it is suggested that certain initial checks be performed when the computer is received; these checks should be performed periodically thereafter (once a week or so, depending on use) as a form of routine maintenance.

When the computer is first turned on and warmed up, all amplifiers should balance with the mode selector in PS (pot set). This balance condition is indicated by the fact that no overload lamps are lit. The power supply outputs should then be checked and levels adjusted if required. The computer voltmeter may be used for this purpose. Next the digital voltmeter should be zero-set (refer to the TDVM manual for adjustment procedures for this instrument). At this point the TR-48 is ready for normal operation as outlined in the following text. (SECTION I, Paragraph 6.)


FIGURE 1.4-I. TR-48 REAR VIEW, COVER PLATES REMOVED

## 5. EXTERNAL CONNECTIONS

## a. General

All external equipment terminations and wiring required for operation of the TR-48 is brought into the computer cabinet through a group of connectors mounted on a plate on the rear of the cabinet. Included here are connectors for primary abc power, external trunks, slaved operation (for common mode-control between two or more computers), and facilities for connecting external monitoring equipment such as oscilloscopes, plotters, and recorders to the TR-48.

Figure 1.5-1 shows the location and function of each connector, and the following sub-paragraphs describe the connector wiring and terminations within the computer.
b. A.C. Connectors (AC1, AC2, AC3)

AC1 is the primary power input connector for the TR-48. This is a 3-terminal connestor that mates with EAI Power Cable 510.040-1 to provide one hot lead, one netrail lead, and one ground lead. Refer to Paragraph 1-4 for details on connecting the computer to a primary power source.

AC2 and AC3 are convenience outlets for powering maintenance equipment such as an oscilloscope or VTVM. Both connectors are protected by F60 (1.5 amperes), the primary power fuse. AC2 is unswitched and is thus energized whenever the computer is connected to the power line. AC3 is controlled through the primary power switch on the computer control panel.
c. Slave and Trunk Connector (J61) Povizioi ex copt fr Preset hide. This connector provides terminations for slaving two or more computers together fum for common mode-control from one computer. Cable 19.261 is provided to connect ole the computers together for slaved operation. If two computers are to be slaved, the 19.261 cable should be installed between the J61 connectors on each TR -48. If more than two computers are to be slaved, a Model 47.040 Junction box is supplied and the 19.261 cable from each computer is connected to the junction box, which simply parallels the mode control lines of all computers.

When desiring to operate previously slaved computers separately, the slave cables) must be removed.

In addition to the slave circuits, the J61 connector carries the ten trunks that appear on the 12.763 Patch Panel Readout Module. Refer to Sheet 41 of the computer Wiring Diagram (B045 034 OW) for details on specific connections terminated at J61.
d. Trunk-Function Switch Connectors (J62, J63, and J64)

This group of connectors is wired to the three component cradles that accept a trunk or function switch module. (See Figure 1.3-1.) The wiring is arranged such that J62 is wired to module 5, slot 2 (cradle 22), J63 to module 8 , slot 2 (cradle 37), and J64 to module 11, slot 2 (cradle 52). EAI Cable 19.262 is designed for

$$
\text { petrie lack } 3 \text { page. }
$$

use with these connectors.
The function switches are located on the attenuator panel; the wiring from these switches terminates in a plag connector. By mating this plug with J62 or J63 the function switches are connected to the associated module slot (J62 connects the function switches to module 5, slot 2 and J63 to module 11, slot 2). The function Switch 12.766 Unit inserted in sither of the two slots provides the patching terminations at the Pre-Patch Panel.

Certain leads connected to $J 64$ are also routed to the control panel to permit readout via the selector system. Selector addresses A50 through A64 select these leads. Figure $1.5-2$ shows the trunk patching block and the corresponding address for each trunk in this area. The trunks in this area are normally used as in-trunks; this permits the operator to readout and check the incoming signal levels.

For complete details on the wiring to connectors J62, J63, and J64, see Sheets 41 and 42 of BO45 0340 W .

## e. Recorder/Plotter Connector (J65)

This connector is wired to the Readout Module 12.763 area (Module 2, slot 2) to make the input circuits of an external recorder or plotter accessible at the PrePatch Panel. Cable 19.323 is provided for connecting the EAI Series 1110 VARIPLOTTER to the TR-48 readout module. See 8 y .64 fo Pendout Danel.
In addition to the four signal terminations ( $\mathrm{X}_{1}, \mathrm{X}_{2}, \mathrm{Y}_{1}, \mathrm{Y}_{2}$ ), J 65 also includes three leads for control of the plotter penmlift circuit. This wiring is compatible with the control circuits of the 1110 Series of VARIPLOTTERS, and is arranged so that the pen circuits are energized only when the computer is in the operate mode. All connections to J65 are listed on Sheet 43 of BO45 034 OW; the pen control circuits are shown on Drawing D045 034 OS (Sheet 2).
f. Oscilloscope Connector (J66)

This connector provides inputs for an external oscilloscope to be terminated at the Patch Panel Readout Module. Cable 19.322 provides the signal leads between the oscilloscope and the computer. Sheet 43 of BO45 034 OW lists the connections to J66.
6. OPERATION

A detailed description of the operating procedures (including problem programming) for the $T R-48$ is given in the Operator's Handbook. This paragraph therefore, is limited to a brief description of the TR-48 operating controls.

All of the computer operating controis are located on the left-hand control panel of the insturment (Figure 1.6 m 1 ).


FIGURE 1.5-1 PLUG PLATE, REAR TR-48



## a. POWER Switch

This switch controls the application of primary power to the TR-48. It is a pushbutton switch that is depressed to turn the unit on and again depressed to turn the unit off. When power is applied to the TR-48 the switch face is illuminated.
b. Multi-range Voltmeter Controls

The following is a list of the voltmeter FUNCTION switch positions with a brief description of each.

## Position

BAL

PATCH

RELAY
$-15,-8,30$
15 , and 2

## Description

The stabilizer output of the amplifier addressed by the Selector System is applied to the voltmeter to facilitate checking and/or adjusting the amplifier balance. (The meter RANGE switch may by at any position except OFF when monitoring stabilizer outputs.)

Connects the meter, via the RANGE switch, to the VM Pre-Patch Panel termination (on 12.763 Readout Patch-Block).

Connects meter to the relay power supply (nominally -20 volts).

Connects meter to output of corresponding power supply; the proper scaling resistor is automatically selected.

The RANGE switch permits the operator to select full-scale deflection range of the voltmeter when the FUNCTION switch is in the PATCH position. This switch in general has no effect on the meter when the FUNCTION switch is in any position other than PATCH. Note, however, the RANGE switch must not be in the OFF position when monitoring amplifier stabilizers (BAL).

The OFF position of the RANGE swirtch is used to connect the attenuator wipers to the null pot (via the meter) for TR-48 computers that are not equipped with a DVM (TR-48-0).

## c. Signal Selectors

The signal SELECTOR permits the readout of various circuits of the TR- 48 Computer. A detailed explanation of these circuits is given in Section IV of this manual. The following is a list of signals available for readout with a standard selector system.

## Address

AOO through A47

A48 and A49

A50 through A64

A65 through A99
P00 through P59

P60 through P99

## Signal Source

Addresses the outputs of the $48 \mathrm{~d}-\mathrm{c}$ operational amplifiers. The address corresponds to the PrePatch Panel designation. Also addresses the stabilizers of these amplifiers for readout via the multi-range voltmeter when the FUNCTION switch is in the BAL position.

Addresses the positive and negative reference amplifier outputs for readout (A48 positive and A49 negative reference amplifier).

Addresses the 15 IN - TRUNKS, located in Module 8, slot 2 (cradle 37) of the Pre-Patch Panel, for monitoring. (See Figure 1.5-2.) These trunks terminate at $J 63$ on the rear of the TR-48. (See Figure 1.5-1.)

Unassigned.
Addresses the wipers (under load) of the attenuators for monitoring and adjustment. The attenuators are designated and labeled POO through P59 on the attenuator panel at the right-hand side of the computer.

Unassigned。

To have the addressed signals displayed by the DVM or multi-range voltmeter (VM) a patch connection must be made between the SEL and DVM and/or VM terminations on the Pre-Patch Panel 12.763 Readout Patching Block. The VM FUNCTION switch must be placed in the PATCH position to connect this instrument to the VM patching termination. Note, however, that the multi-range voltmeter should not be used to monitor attenuators because of the relatively low input impedance of the meter circuit. To prevent this situation a relay disconnects the VM from the selector system when the computer is placed in the PS mode.

## d. Mode Control Pushbuttons

These controls determine the operating mode of the computer. Following is a list of the pushbuttons and a brief description of their functions.

## Mode Pushbutton

OP (Operate)

## Description

When this button is depressed, all integrators are simultaneously released (operate bus energized) to respond to input signal voltages.

| Mode Pushbutton | Description |
| :---: | :---: |
|  | The integrator outputs change in potential as dictated by the inputs; a time varying behavior is produced. This generates the voltage solution of the programmed problem. |
| HD (Hold) | Depressing the HD pushbutton permits the problem solution to be stopped and all the voltages held at the potential attained up to the instant of depressing the button. After making the desired observations (or adjustments), the problem may be continued from this point by depressing the OP button or re-set to the starting point by depressing the RS button. |
| RS (Reset) | In the Reset mode, RS, all circuits except the integrators function normally. The integrator outputs are held at their respective initial conditions (IC) as dictated by the IC input voltage. (The integrator output is zero if no IC voltage is applied.) |
| PS (Pot Set) <br> Perviscon <br> Sirmmeris fumetovi <br> commocted titged. <br> lig nolay contacts. | In the Pot Set Mode, PS, relay contacts close, connecting the output of all the high-gain amplifiers to their inputs. This essentially provides the amplifiars with a zero feedback impedance (preventing them from overloading) and also holds the amplifier summing junction at virtual ground. This permits setting the attenuators under load conditions. (The summing junctions of the integrator networks are physically connected to $\pm$ ground.) |
| SL (Slave) | When a TR-48 Computer is to be slaved to another TR-48, this button is depressed on the slaved computer. The slaved computer then responds to the, selected modes of the master computer. <br>  |
| RO (Rep-Op) | The RO button places the computer in the repetitive operation mode. The computer automatically switches between the operate, and reset modes at a pre-determined rate. (See Paragraph 7 of this section.) |

e. Repetitive-Operation Timing Selector

This control, actually a dual control, determines the operate duration of the computer integrators when the TR-48 is in the Rep-Op mode. The control consists of
a four position outer switch and an inner vernier control that will expand each of the four ranges by two and one-half times.

## f. Overload Indicators

The overload indicators provide a visual alarm when an overload occurs in any of the operational amplifiers, i.e., when the summing junction error exceeds artolerable limit. An operational overload may be due to improper scaling or improper patching; in some cases a temporary overload (lamp flashes on and then goes out) may not cause appreciable error and the operator, after consideration, may choose to neglect the indication.

When the computer is initially turned on all the indicator lamps light; however, in a few seconds, as the amplifiers settle, all the lamps should go out. Should a lamp remain lit it generally indicates a patching error (such as the failure to provide un-used amplifiers with feedback). Prolonged overloads will not damage an amplifier.

## g. Patch Panel Engage/Disengage Switch

This switch controlsthe operation of the Pre-Patch Panel drive motor. For a description of the operation see the Pre-Patch Panel insertion and removal instructions in the Operators Handbook.

## 7. TR-48 MAINTENANCE

## a. General Information

The TR-48 is constructed of the best commercial grade components and hardware and is designed for long periods of trouble-free operation. Before shipment from the factory, each instrument is subjected to extensive quality control checks and adjustments.

In order to maintain the computer in peak operating condition, a definite plan for regular maintenance checks is recommended. It is not desirable to allow the computer to operate continuously until some malfunction occurs. If this course is followed there is no assurance of accuracy and optimum performance at any given time.

A maintenance program for equipment such as the $T R-48$ should be accomplished in three phases. First to be considered is the operational maintenance which occurs during periodic checks of such things as amplifier balance, power supply and reference levels, and diode function generator settings. Due to the frequency of these checks most malfunctions are discovered during this operational maintenance phase.

The second phase of a maintenance program would involve troubleshocting defective units discovered during the operational checks. This is most conveniently accomplished on the computer by operating the defective component on a test shelf as
shown in Figure 1.7-1. This permits the defective unit to operate in its normal environment, and at the same time exposes all components and wiring to facilitate troubleshooting.

The third phase of the maintenance program should consist of periodic testing of all components in a system. This is generally referred to as preventive maintenance. Tests should be designed to detect units that, while presently useful, may fail in the near future, or units whose performance may have gradually deteriorated. This type of maintenance is predicated on the availability of unit spares. Having unit spares on hand is highly recommended to permit using the computer while components are being periodically checked. Also, a malfunctioning component can be replaced immediately if a working spare is on hand.

To assist TR-48 maintenance personnel, this handbook includes in SECTION II, a complete circuit description for each unit in the computer, and a recommended test and adjustment procedure for that unit. Also included in this manual are replaceable parts lists (APPENDIX I) and Schematic and Wiring Diagrams for the computer and all plug-in components (VOLUME II).
b. Maintenance Accessories and Equipment


Included with the accessories provided with each TR -48 is a Model 51.116 Service Shelf. This unit fits into the component cradles of the computer and mates with the cradle connectors. The other end is terminated with a mating connector for the component under test.

As shown in Figure 1.7-1, by removing the component patching block at the same time the faulty component is removed from the computer, the service shelf may be inserted through the Patch Panel opening into the vacated module slot. To facilitate patching into the component on the service shelf the spring contacts on the front of the unit must be removed. These contacts may be readily removed by simply pulling them out with a pair of long -nose pliers; reasonable care should be exercised to prevent damaging the contacts.

When replacing the spring contacts they should be seated with the insertion tool provided. Only those component-block holes with small dots to their immediate left require contacts. To assure the contacts are at the proper angle when replaced, cover this dot with the contact projection that rests flush against the component front block.

It should be noted that the TR -48 itself contains many of the facilities required for component maintenance. The digital voltmeter (if it is not affected by the particular malfunction) permits reading doc voltages to four-place accuracy. The control panel voltmeter is also available for monitoring operational and computing voltages. The lowest voltmeter range permits reading potentials as low as 10 millivolts with reasonable accuracy. The sensitivity of the voltmeter may be increased by using a doc amplifier as a meter preamplifier. For this purpose a special feedback network consisting of a 10 megohm ( $\pm 1 \%$ ) resistor shunted by a .047 mfd capacitor should be made up with standard banana plugs. By connecting this network across an amplifier and using a gain of -10 input, voltages to be observed may be multiplied by a factor of 1000 before application to the meter circuit. Thus, by using the 0.1 -volt scale, potentials as low as 10 microvolt can be read with sufficient accuracy for maintenance purposes.


In addition to the facilities offered by the TR-48, maintenance personnel should have two other items of test equipment available for performing the test and adjustment procedures outlined in this manual: a d-c oscilloscope (Dumont, Model 403 or equivalent), and a vacuum tube voltmeter, or a high-impedance multimeter (Triplett, Model 630-A or equivalent).
c. Applicable Drawings

The following diagrams are contained in Volume II of this handbook.

| Drawing Number | Type | Description |
| :---: | :---: | :---: |
| B019 261 OA | Assembly | Trunk Cable |
| B019 262 OA | Assembly | Slave Cable |
| B019 322 OA | Assembly | Scope Cable |
| B019 323 OA | Assembly | 1110 VARIPLOTTER Cable |
| B019 330 OA | Assembly | 1100E VARIPLOTTER Cable |
| C045 034 OA (Sheet 3) | Assembly | 11.148 Relay Panel Layout |
| $\begin{aligned} & \text { D045 } 034 \text { OS } \\ & \text { (Sheets } 1 \text { through 3) } \end{aligned}$ | Schematic | Schematic diagrams of selector system, relay, panel, meter circuit, Patch Panel motor and Mode Control switches. |
| $\begin{aligned} & \text { B045 } 034 \text { OW } \\ & \quad \text { (Sheets } 2 \text { through 56) } \end{aligned}$ | Wiring | Wiring run sheets (plus key sheet) of computer rack wiring. |
| A047 040 aw | Wiring | Slave cable junction box (for slaving three or more computers). |



1. DUAL D.C. AMPLIFIER 6.514

The TR-48 Dual D.C.Amplifier 6.514 consists of two independent high-gain d-c amplifiers and two independent resistor networks (Figure 2.1-1). The amplifiers are transistorized and designed for optimum stability and frequency response. Chopper stabilization virtually eliminates amplifier drift. In addition the amplifiers feature high open-loop gain, low noise and offset, and a short-circuit-protected output stage. Conservatively rated components ensure long-term reliability.

Patched as an operational amplifier these units become the basic computing unit in an analog computer. Used with appropriate input and feedback networks each amplifier can perform such linear functions as inversion, summation, integration, and multiplication by a constant. Accessory components enable the amplifier to multiply two variables, divide variables, simulate transfer functions, limit, simulate deadtime, and generate analytic or arbitrary functions.
a. Technical Data

Output Voltage Range:
0 to $\pm 10$ volts minimum
Output Current Range:
at $\pm 10$ volts $\ddagger-c . . . . . . . . . .20$ milliamperes minimum
Noise and Ripple: 400 microvolts maximum ( 200 microvolts typical)

Offset Voltage (amplifier balanced) 20 microvolts maximum ( 5 microvolts typical)

## b. Operating Considerations

The data in this sub-paragraph is general operating information with which maintenance personnel should be familiar in order to rapidly isolate amplifier troubles and eliminate causes of apparent faults which may be due to improper amplifier usage。
(1) Amplifier Balancing. The amplifiers should be periodically balanced to assure computer accuracy. The amplifier balance should be checked as a matter of routine maintenance, although, under normal operating conditions, balancing is only required after a period of several months. An amplifier requiring frequent balancing is indicative of eventual failure.

## NOTE

> Initially, due to component aging, more frequent balancing of amplifiers may be required. Movement of the computer to different areas with extreme changes in ambient conditions (or extreme changes at the same location) may also necessitate amplifier balancing.
(2) Amplifier patching. The input and output terminations of the dual highgain amplifiers and the dual resistor networks are terminated at the Pre-Patch Panel and arranged for patching ease. The non-linear components are also located in close proximity to the amplifiers for ease of patching and short patch cord runs.

Patching, when using an amplifier (s) in conjunction with an integrator network or one of the non-linear. components, is covered in the paragraphs covering these units. This section is therefore limited to the description of an amplifier used in conjunction with a resistor network.

Figure 2.1-2a illustrates two of the more common amplifier patching arrangements. The upper amplifier makes use of the standard 4 -connector bottle plug, shown by the shaded area, and provides a summing circuit as shown schematically in Figure 2.1-2b. This configuration has two gain-of-one and two gain-ofoten inputs for summing, inversion, or multiplication.

The lower amplifier of Figure 2.1-2a provides one gain-ofoone and three gain-of-one tenth inputs by using two, 2 -connector bottle plugs shown by the shaded area. The simplified schematic of the configuration is shown in Figure 2.1-2c.

As previously indicated, these are only two of many possible amplifier configurations. An important point to note is that all amplifiers whether used (assigned) or unused (unassigned) for a particular problem solution, must be provided with feedback. Failure to provide a feedback circuit for an amplifier will cause that amplifier to overload as soon as the computer is switched to any mode other than pot-set.

The d-c operational amplifiers are rated for normal operational outputs of $\pm 10$ volts maximum. Thus the amplifier patching arrangements, regardless of the application, should be such that the output level does not exceed either plus or minus 10 volts. (The amplifiers are capable of slightly higher outputs to allow minor scaling discrepancies.)
(3) Amplifier Overload. The overload system provides a visual indication to the operator when an amplifier summing junction error exceeds a tolerable limit. The overloading of an assigned amplifier indicates that an error is induced in the problem solution at the instant of overlodd. An overload may be due to improper scaling or patching; in some cases a momentary overload may not induce appreciable error and the operator may choose to neglect the indication. Prolonged overloads will not damage the amplifier unless caused by excessively high voltages other than those normally obtainable from the computer itself.


THESE PINS
JUMPERED
b. PATCHING BLOCK

a. PRE-PATCH PANEL CONFIGURATIONS

b. SIMPLIFIED SCHEMATIC (GAINS OF I AND IO)

c. SIMPLIFIED SCHEMATIC (GAINS OF O.I ANDI)

FIGURE 2.1-2 AMPLIFIER PATCHING, TYPICAL CONFIGURATIONS

Overload of an unassigned amplifier will neither damage the amplifier or affect the problem solution. The fact that one or more unassigned amplifier overloadlamps are lit, however, may cause the operator to overlook an overload of an assigned amplifier. This will cause an erroneous problem solution, thus defeating the purpose of the overload alarm system.

When power is initially applied to the computer, all of the overload lamps light; after a few seconds all of the lamps should extinguish. The lamps may also momentarily flicker when switching from pot-set to some other computer mode.

## c. Theory of Operation

When a high-gain d-c amplifier is used in conjunction with input and feedback networks to perform mathematical operations, the resulting system is generally referred to as an operational amplifier. The operational amplifier is the basic and most versatile unit in the analog computer. It can be used for inversion, summation, multiplication by a constant, integration, and used in conjunction with special networks for squaring, extracting square root, generating logarithmic functions, etc.

To understand the basic concept of the operational amplifier, consider the simplified block diagram of Figure 2.1-3 where a high-gain amplifier (gain of $-A$ ) has a feedback impedance $Z_{f}$ and an input impedance $Z_{i n}$. The amplifier is designed so that it has three basic and essential characteristics.

1. The amplifier output ( $e_{o}$ ) is related to the summing junction voltage ( $e_{b}$ ) by the gain of the amplifier:

$$
\mathrm{e}_{\mathrm{o}}=-\mathrm{Ae} \mathrm{e}_{\mathrm{b}}
$$

2. The input stage of the amplifier draws negligible current: $\quad i_{b}=0$
3. The open loop gain of the amplifier is extremely high: A>>1 (on the order of $3 \times 10^{7}$ at d-c).

Using Kirchhoff's laws, the nodal current equation at the summing junction ( Sj ) is:

$$
i_{i n}=i_{f}+i_{b}
$$

or

$$
\frac{e_{i n}-e_{b}}{Z_{i n}}=\frac{e_{b}-e_{o}}{z_{f}}+i_{b}
$$

Since $e_{b}=\frac{-e_{0}}{A}$ and since $i_{b}=0$ from characteristics (1) and (2), respectively
then

$$
\frac{e_{\text {in }}}{Z_{\text {in }}}+\frac{e_{o}}{A Z_{f}}=-\frac{e_{o}}{A Z_{f}}-\frac{e_{o}}{Z_{f}}
$$

Solving for $e_{0}$ :

$$
\begin{equation*}
e_{o}=\frac{-\frac{z_{f}}{z_{i n}} e_{i n}}{1+\frac{1}{A}\left(\frac{z_{f}}{Z_{i n}}+1\right)} \tag{EQ2.1-1}
\end{equation*}
$$

In most applications the ratio of $Z_{f}$ to $Z_{\text {in }}$ is less than 30 and since $\frac{1}{A}$ approaches
zero, equation $2 \cdot 1-1$ becomes:

$$
e_{o}=\frac{z_{f}}{z_{i n}} e_{i n}
$$

(EQ 2.1-2)

Equation 2.1-2 illustrates one of the most important considerations of the operational amplifier: the input-output relationship of the operational amplifier is solely dependent on the ratio of the feedback to the input impedance.

Using equation 2.1-2 as the basis of discussion, the following sub-paragraphs describe the various uses of the operational amplifier.
(1) Inversion. When the same value resistor is used for both the feedback and the input impedance, the amplifier output voltage has the same amplitude as the input voltage but is opposite in polarity.

$$
e_{o}=-\frac{R_{f}}{R_{i n}} e_{i n}
$$

In the $T R-48$ the value of $R_{f}$ and $R_{i n}$ used for the inverter is normally 100,000 ohms, (100K) ; therefore

$$
e_{0}=-\frac{100 \mathrm{~K}}{100 \mathrm{~K}} e_{\mathrm{in}}=-e_{\text {in }}
$$

Thus a +10 volt input results in a -10 volt output, and the amplifier is said to have a gain of minus one. The accuracy of the output to input 1:1 ratio depends only on the comparative equality of $R_{\text {in }}$ to $R_{f}$.
(2) Multiplication by a Constant. A change in the ratio of the resistors results in multiplication by a constant. With $R_{f}$ equal to 100 K and $R_{i n}$ equal to 10 K , for example, the amplifier output is:

$$
e_{0}=-\frac{100 \mathrm{~K}}{10 \mathrm{~K}} e_{i n}=-10 e_{i n}
$$

An input of plus one volt results in an output of minus ten volts. This operational amplifier has a gain of ten. The multiplying constant can be made smaller than one by using a 10 K feedback resistor with a 100 K input resistor.

$$
e_{0}=\frac{10 \mathrm{~K}}{100 \mathrm{~K}} \quad e_{i n}=-0.1 e_{\text {in }}
$$

An input of minus ten volts produces an output of plus one volt.
(3) Summation. When multiple input resistors are used with a feedback resistor $\mathrm{R}_{\mathrm{f}}$, the basic relationship is extended to:

$$
e_{o}=-\left(\frac{R_{f}}{R_{1}} e_{1}+\frac{R_{f}}{R_{2}} e_{2}+\ldots+\frac{R_{f}}{R_{n}} e_{n}\right)
$$

The circuit can be used to algebraically sum an indefinite number of inputs; furthermore, each input may be multiplied by an arbritrary constant.
(4) Integration With Respect to Time. When the feedback element $Z_{f}$ is a capacitor rather than a resistor, the summing junction current equation is:

$$
\frac{e_{1}}{R_{1}}+\frac{e_{2}}{R_{2}}+\cdots+\frac{e_{n}}{R_{n}}=-c \frac{d_{e o}}{d t}
$$

Integrating this equation and assuming an initial charge on the feedback capacitor of $V_{0}$ :

$$
e_{0}=-\frac{1}{c} \int_{0}^{t}\left(\frac{e_{1}}{R_{1}}+\frac{e_{2}}{R_{2}}+\ldots+\frac{e_{n}}{R_{n}}\right) d t+V_{0}
$$

Alternately, if $Z_{f}$ is a capacitor having an operational impedance $1 / \mathrm{pc}$ and $\mathrm{Z}_{\mathrm{In}}$ is a resistor, the basic operational amplifier relationship (equation 2.5-2) becomes:

$$
e_{0}=-\frac{e_{i n}}{p R C}=-\frac{1}{R C} \int_{0}^{t} e_{i n} d t
$$

With this arrangement, the operational amplifier will integrate (with respect to time) any input voltage. In addition to integrating, the amplifier also inverts the input voltage. An indefinite number of inputs may be applied to produce the time-integral of the sum of the input voltages.
(5) Other Mathematical Operations. As previously indicated the operational amplifier has uses other than those indicated in sub-paragraph a through d. Complicated transfer functions can be simulated by using series and parallel RC networks for the feedback and input impedance. The circuit performance is still governed by the basic relationship of equation 2.5-2. For the general case where three-terminal networks are used, the short-circuit transfer impedance of $Z_{f}$ and $Z_{i n}$ must be used. (The short circuit transfer impedance of a network is the ratio of input voltage to short-circuit output current.) The input and feedback elements need not be linear; therefore, almost any non-linear characteristics can be approximated. The amplifier can also be used in conjunction with diodes and resistors to simulate the non-linear operations of limiting, dead-zone generation, absolute value derivation, $X^{2}$, Log $X$, etc.

A problem encountered in a d-e amplifier that is not prevalent in an a-c amplifier is drift or offset. That is, the output does not remain constant with a constant input and in particular does not remain at zerc with a zero input. This is an undesirable feature, especially when using a d-c amplifier for integration since drift can lead to serious computational errors. To compensate for possible drift and to stabilize the d-c amplifier, the TR-48 units contains an a-c amplifier or stabilization circuit.

Figure 2.1-4 is a simplified block diagram of the TR-48 high-gain amplifier. A d-c signal is changed to a-c by a electromechanical chopper and amplified by the stabilizer amplifier. The stabilizer output is rectified by the same electro-mechanical chopper and further amplified by the d--c amplifier circuit. Any a-c component on the d-c input by-passes the stabilizer (via the capacitor). Thus a-c components are amplified by the d-c section only, while d-c components are amplified by the cascaded stabilizer d-c amplifier combination.

To visualize the stabilizer circuit operation, assume the operational amplifier of Figure 2.1-4 is provided with a feedback element from the output of the d-c section to the input of the stabilizer section (Figure 2.1-3). Assume also that an input is applied via an input resistor and the amplifier output attains a level, as dictated by the feedback-input ratio, so that the summing junction (d-c input of Figure 2.1-4) is at virtual ground. If the amplifier now begins to drift, the drift voltage (or offset) at the output causes an unbalance between the feedback and input currents, or an offset at the amplifier summing junction. The stabilizer "sees" this offset as an input, amplifies it, and applies it in opposite polarity to the d-c amplifier where it cancels the original drift voltage. The cancellation is not complete but the effect is to reauce the drift by a factor equal to the gain of the stabilizer circuit. This permits the amplifier to be used for several months before there is a need to balance the amplifier manually to assure that the output is zero with a zero input.

Each 6.514 Amplifier Unit contains two identical but independent operational amplifiers. Figure 2.1-5 is the schematic diagram of one of the two amplifiers. (Compared to DOO6 282 OS, Figure 2.1-5 is the schematic of the amplifier on the upper half of the drawing; it is, however, typical of both amplifier circuits.)

Transistors Q6, Q7, and Q8, with associated circuitry, comprise the stabilization amplifier. Contacts 2 and 3 of electro-mechanical chopper $D 1$ change the d-c input to a-c for amplification by the stabilizer, and contacts 1 and 2 restore the stabilizer output to $d-c$ for application to the $d-0$ amplifier section.

Transistors Q17, Q1, Q2, Q3, Q4, and Q5 comprise the d-c amplifier portion of the unit. The output stage of the $d-c$ amplifier consists of Q4 and Q5, a complementary symmetry (or totem pole) circuit which provides the advantages of push-pull operation with single-ended input and output. The circuit is similar to a balanced bridge. With a zero input, equal current flows through Q4, I1, I2, and Q5 from the -15 volt to +15 volt supply; thus, the output is zero. An input signal causes one stage to conduct more heavily than the other, i.e., the bridge becomes unbalanced and current flows to the external circuit.


FIGURE 2.1-3. OPERATIONAL AMPLIFIER, BLOCK DIAGRAM


FIGURE 2.1-4. HIGH GAIN D-C AMPLIFIER, SIMPLIFIED BLOCK DIAGRAM


FIGURE 2.1-5. HIGH GAIN AMPLIFIER, SIMPLIFIED SCHEMATIC

Incandescent lamps (I1 and I2) are connected in series with the emitter of each output transistor to stabilize and protect these components. As current through a stage increases, the lamp impedance also increases, thus acting as a current limiting device. The diode current limiting network (CR1 and CR2) in the input circuit permits quick overload recovery.

Transistor Q17 uses the base-to-emitter voltage of Q1 as its operating potential and the base-to-emitter impedance of Q1 as its load; with this configuration, the amplifier input impedance becomes relatively high.

Figure 2.1-6 is a simplified schematic of one of the dual amplifiers and one of the dual resistor networks interconnected with a four-connector bottle plug. As shown in the figure, the 12.730 Network not only contains the input and feedback resistor of the amplifier, but also the balance potentiometer and the pot set relay. The pot set relay is energized when the computer is placed in the pot set mode; the relay contacts short the amplifier output to the input. Since the amplifier summing junction is tied to the output, the amplifier gain is zero; thusi, any current flow at the output of the amplifier is due to drift in the d-c section. The balance pot may then be adjusted for a potential equal in magnitude and opposite in polarity to that of the drift. The pot set relay also prevents the amplifiers from overloading when the Pre-Patch Panel is removed (thus disconnecting any patched feedback circuits) to expose the balance controls. When switching from pot-set to any other computer mode, the pot-set relay de-energizes, and the amplifier re-gains its patched feedback circuit (the 100K resistor of Figure 2.1-6, for example). During the switching time of the relay an amplifier may momentarily go into overload before settling.

## d. Maintenance and Test Procedures

As previously indicated the amplifier balance adjustment should be checked at periodic intervals to assure computer accuracy. The balance procedure [outlined in SubParagraph $b(1)]$ is also indicative of subsequent amplifier failure if frequent balance is required. Inability to balance an amplifier is a positive indication of component malfunction. Two tests are given in this sub-paragraph for checking a suspected amplifier and for checking repaired units to assure that a malfunction has been adequately rectified. Prior to attempting any maintenance procedure the amplifier must be balanced.
(1) Amplifier Output Current Check. Set up the test circuit shown in Figure 2.1-7 and select the amplifier under test for readout on the DVM. Apply positive and then negative reference to the amplifier input, observing the output voltage level in each case. A DVM reading of less than 10 volts magnitude in either case loud indicates the amplifier is not capable of supplying 20 milliamperes of current (the minimum allowable for reliable amplifier operation).
(2) Amplifier Dynamic Error Check. Set up the test circuit shown in Figure 2.1-8a. Note that the amplifier under test is used as an inverter while the second amplifier is used as a summer (gain-of-ten for both inputs). In patching the amplifier under test it is suggested that two 2-connector bottle plugs are used instead of the normal 4 -connector plug, since the input and feedback resistors may
have to be interchanged.
$2 \mathrm{r} / \mathrm{cm}$.
Set the scope horizontal (X) gain for approximately full scale deflection with the 6.3 V a-e input. Calibrate the vertical gain for 10 millivolts/centimeter. Set R2 for minimum resistance.

Potentiometer R1 is used to trim input resistor $R 5$ to the exact value of $R 6$, thus assuring the amplifier under test has an exact gain-of-one. Therefore, any error indication will be that of the amplifier tested and not of the input and feedback resistor ratio. This trimming is accomplished by adjusting R1 so that connections at $C$ and $D$ may be interchanged (io., $C$ connected to $D$ and $C^{\prime}$ to $D^{p}$; Figure 2.1-8b) without affecting the scope diagonal pattern. It may be necessary to interchange R5 with R6 (thus R6 will be in series with R1) should the impedance of R5 be greater than that of R6; this may easily be accomplished if two 2-connector bottle plugs are used to patch the amplifier under test.

Potentiometer $R 2$ is used to trim $R 4$ to the exact value of $R 3$, thus assuring amplifier 2 has an equal factor for both inputs. This trimming is accomplished by adjusting R2 so that connections at $A$ and $B$ may be interchanged (ice., A connected to B and $A^{8}$ to $B^{0}$, Figure 2.1-8c) without affecting the scope pattern.

With both R1 and R2 adjusted, the scope pattern indicates the amplifier dynamic error multiplied by a factor of 10 , $i_{.} e_{0}$, the extent that the line (peak-to-peak) deviates from the horizontal is 10 times the amplifier dynamic error at 10 millivolts/centimeter of deflection peak-to-peak. A typical amplifier will cause approximately 2.5 centimeters, or 25 millivolts of vertical deflection; this is actually 2.5 millivolts error. The maximum permissible scope deflection is 6 centimeters ( 60 millivolts).
(3) Trouble Analysis. The amplifier is used with different types of networks depending on the operation it is to perform; thus unsatisfactory performance may actually be due to a malfunction in the network rather than the amplifier. The mailfunction can usually be isolated to a particular chassis by interconnecting suspected components with those known to be good. Unlike most types of electronic equipmont, a faulty amplifier usually identifies itself immediately; if a component within the amplifier fails, the output voltage of the amplifier characteristically flops to its plus or minus limit (up to $\pm 13$ volts, depending on the load).

The most common indication of unsatisfactory amplifier operation is failure to balance properly. If an amplifier cannot be balanced, the malfunction can be localized to either the $d-c$ or stabilizer section by the following procedure.
(1) Place the amplifier on service shelf and patch a feedback resistor around the amplifier; remove all inputs.
(2) Disable the stabilizer by grounding the stabilizer output line. (This line is terminated at Pin $P$ of the rear connector or pin 1 of the chopper for the upper amplifier, and pin L of the rear connector or pin 9 of the chopper for the lower amplifier; see Drawing D006 282 OS.)


SYMBOL KEY:
(1) INDICATES PRE-PATCH PANEL PATCHING TERMINATION

INDICATES PATCH CORD ORbottle plug connection

NOTES:
I. SWITCHED RELAY VOLTS (NOM. -2OV) IS ONLY PRESENT WHEN THE COMPUTER IS IN THE POT SET MODE.
2. THE AMPLIFIER OUTPUT IS ALSO WIRED TO THE SELECTOR SYSTEM FOR READOUT.
3. RELAY KI SHOWN DE-ENERGIZED

FIGURE 2.I-6 AMPLIFIER 6.514, SIMPLIFIED SCHEMATIC


FIGURE 2.1-7 OUTPUT CURRENT TEST CIRCUIT

a. INITIAL TEST SET UP

b. C AND D LEAD INTERCHANGE

c. A AND B LEAD INTERCHANGE

FIGURE 2.1-8 AMPLIFIER DYNAMIC ERROR TEST SETUP
(3) Monitor the output voltage of the amplifier with an oscilloscope or voltmeter and slowly rotate the balance potentiometer.
(4) The amplifier output should flop between its plus and minus limits (about $\pm 13$ volts) as the balance control is turned from one end to the other. A slight delay in response is normal. If the amplifier fails to do this, the malfunction is probably in the $d-c$ section of the amplifier.
(5) Remove the ground from the BAL terminal. Connect an oscilloscope to the BAL terminal and observe the stabilizer output as the balance potentiometer is slowly rotated.
(6) The square wave output should change polarity, from negative-going to pos-itive-going, as the balance control is turned from one end to the other. Failure to do so indicates that the malfunction is probably in the stabilizer section.

The $d-c$ section of the amplifier may be checked by again disabling the stabilizer section and proceeding as outlined in the following procedure.
(1) Remove the feedback resistor and all inputs to the amplifier.
(2) Observe the output swing of each stage in turn as the balance control is rotated between its limits.

Troubles in the stabilizer section can frequently be isolated to a particular stage by the following procedure.
(1) Patch the amplifier as shown in Figure 2.1-9. The gain-of-ten input should cause the amplifier to overload.
(2) Circuit wave forms for a properly functioning stabilizer are shown in Figure 2.1-10. With an oscilloscope, compare these waveforms with the suspected stabilizer.

The following table lists some of the more common amplifier trouble symptoms and some suggested remedies. Note that the components listed in the remedy column are not always the source of the indicated symptoms. The components listed are for the upper amplifier only, see Diagram D006 282 OS for the corresponding items in the lower amplifier.

| Symptom | Suggested Remedy |
| :--- | :--- |
| Excessive High-Frequency Noise | Replace Q1 or Q17 or both |
| Excessive Low-Frequency Noise | Replace Q6 |
| Poor Frequency Response | Replace Q1; Check interstage <br> coupling networks |
| Amplifier oscillates with nega- <br> tive output, positive output <br> satisfactory | Replace Q4 |


| Symptom | Suggested Remedy |
| :--- | :--- |
| Amplifier oscillates with positive <br> output, <br> factory | Replace Q3 or Q5 or both |
| Excessive Offset | Replace C1 or C7 or both |
| Extremely High Offset | Replace Q1 |
| Negative Outpat Only | Replace I1 |
| Positive Output Only | Replace I2 |

(4) Applicable Drawings. The following drawings are contained in Volume II of this handbook:

Drawing Number C006 514 OS

D006 282 OS

B045 034 OW

Type
Schematic

Schematic

Wiring

## Description

Schematically shows all components of the 12.730 network and inter-connection to 6.282 amplifier. Also shows connections to rear connector (P1) of the 6.514 module.

Schematic diagram of d-c amplifier card only.

Contains run sheets listing wiring from 6.514 rear mating connector to other points in computer cabinet.
(5) Parts Lists. Appendix I contains the replaceable parts lists for the 6.514 amplifier. See Index of Appendix I.
2. DUAL INTEGRATOR NETWORK 12.764

The 12.764 Dual Integrator Network permits the conversion of either or both of the high gain amplifiers into integrating amplifiers merely by the insertion of T-shaped bottle plugs (Figure 2.2-1). The integrator networks are designed to provide maximum flexibility, and permit the computer to be used for real time, interative, or high speed repetitive operation (Rep-Op) problem solutions.

The design of the networks, and the access to circuits provided at the patching area permit the operator to determine the operating mode and time scale of each integrator individually.


FIGURE 2.1-9. AMPLIFIER STABILIZER TEST SETUP

POSITIVE INPUT

NEGATIVE INPUT

a. BASE OF Q6 (OR Q14)

b. COLLECTOR OF Q8 (OR Q16)

c. JUNCTION OF RII-RI5
(OR R34-R39)

FIGURE 2.1-10 PROPERLY FUNCTIONING OVERLOADED STABLIZER WAVESHAPES

c. T-PATCHING CONNECTOR

## a. Operating Considerations

The flexibility of the integrating amplifiers of the TR-48 is indicated by the PrePatch Panel terminations available to the operator. There are essentially six separate areas within the integrator network patching block; four of these areas (two each) function with respect to the individual integrator sections while the remaining two function with respect to both sections. This sub-paragraph describes some of the more common patching configurations.

There are two all-white areas on the integrator patching block of the Pre-Patch Panel. Each area is associated with one of the dual networks; they are conveniently located for patching to the dual d-c amplifiers, normally located to the immediate left, with the T-shaped bottie plugs. The bottle plug completes the following jumper connections: $B$ of the amplifier to $B$ of the integrator, SJ of the amplifier to SJ of the integrator, and 0 of the amplifier to 0 of the integrator (Figure 2.2-2). These three jumper connections must be made in order for the integrator to function.

The IC termination in the white area is for the insertion of the initial condition voltage ( $V_{0}$ ). The IC input should be equal in magnitude but opposite in polarity, to the desired IC, i.e., if an IC of -10 volts is desired (the output of the integrator to equal -10 volts at the instant integration starts) then a +10 volt potential must be applied to the IC termination.

The SJ termination is connected to the integrator summing junction when the unit is in the reset mode. If desired, the amplifier may be used to multiply the actual input IC voltage by a constant by connecting an input resistor to the SJ' termination of appropriate value.

Directly below each of the two all-white patching areas are a pair of terminations (in a cross hatched area) labeled 10ß. For normal time scale integrator operation, these two terminations must be jumpered together. The removal of the $10 \beta$ jumper changes the integrator time scale by a factor of 10 (faster integration rate).

The $10 \beta$ jumper also affects the integration rate when the computer is in repetitive operation. With the $10 \beta$ jumper in piace the Rep-0p rate is 500 times faster than real time; when the jumper is removed the Rep -0 p rate is increased by a factor of 10 , or 5000 times faster than the normal time rate. Since each integrator section of the dual unit has a $10 \beta$ jumper, the time scale of each integrator may be controlled independently.

Note that failure to insert the $10 \beta$ jumper when desiring to operate an integrator at normal time results in integrator gains of 10 and 100 instead of 1 and 10 respectively and will probably cause the amplifier to overload during problem solution.

For additional flexibility, the operate and reset buses as well as the operate and reset relay coils are also terminated at the Pre-Patch Panel. These circuits terminate in the cross-hatched area at the bottom of the integrator patching block. For normal integrator operation, a four-connector bottle plug is placed in this
area (the terminations are therefore jumpered horizontally). Terminating these circuits at the Pre-Patch Panel permits interchanging leads (such as connecting the operate relay to the reset bus and the reset relay to the operate bus); this facilitates the setup of a form of track (or sample) and hold.

The time scale bus (TS) for repetitive operation terminates in the cross hatched area just below the upper $10 \beta$ area. When desiring to operate in the normal repetitive operation mode, a two-connector jumper is placed between the lower two horizontal terminations of this cross hatched area.

By placing the two-connector jumper between the TS and OPR terminations in the upper half of the cross-hatched area (with jumper in lower half removed) the dual integrator may be made to operate in real time when the computer is placed in the Rep 0 p mode. This facilitates the usage of the integrators for iterative computation.

## b. Theory of Operation

The integrating network essentially provides the high-gain amplifiers with a capacitive feedback element in place of the resistive feedback component. In addition, relays are provided for time scaling, permitting the insertion of an IC voltage, and controlling the integrator operation (Figure 2.2-2).

Taking the algebraic sum of the input currents, if forced to pass through a feedback capacitor rather than a resistor, the current equation at the summing junction becomes:

$$
\begin{equation*}
c \frac{d e_{0}}{d t}=-\left[\frac{e_{1}}{-R_{1}}+\frac{e_{2}}{R_{2}}+\frac{e_{3}}{R_{3}}+\cdots\right] \tag{EQ.2.2-1}
\end{equation*}
$$

where $\quad c=$ capacitance in farads
$e_{0}=$ amplifier output voltage $e_{1}, e_{2}, e_{3}$, etc. = input voltages $R_{1}, R_{2}, R_{3}$, etc. = input resistor values in ohms

The relationships in equation $2.2-1$ depend on the fact that when current passes through a capacitor, the voltage across the capacitor changes at a rate proportional to the current. By integrating and assuming an initial condition (IC) voltage, ( $V_{0}$ ) across the capacitor, equation 2.2-1 becomes:

$$
\begin{equation*}
e_{0}=-\frac{1}{c} \int_{0}^{t}\left[\frac{e_{1}}{R_{1}}+\frac{e_{2}}{R_{2}}+\frac{e_{3}}{R_{3}}+\cdots\right] d t+V_{0} \tag{EQ.2.2-2}
\end{equation*}
$$

If $c$ has a value of 10 microfarads and all of the input resistors have a value of 100,000 ohms the RC time constant is one second. Equation 2.2-2 therefore reduces to:

$$
\begin{equation*}
e_{0}=-\int_{0}^{t}\left[e_{1}+e_{2}+e_{3}+\cdots \cdot\right] d t+V_{0} \tag{EQ.2.2-3}
\end{equation*}
$$

where $t$ is in seconds.


FIGURE 2.2-2. INTEGRATOR, SIMPLIFIED SCHEMATIC


FIGURE 2.2-3 INTEGRATOR OPERATIONAL TEST SETUP


FIGURE 2.2-4 IC RESISTOR-RATIO CHECK CIRCUIT


If one of the input resistors is changed to some value other than 100 K ( X ohms), then the corresponding input voltage must be multiplied by a factor of $100 \mathrm{~K} / \mathrm{X}$ before the summation and integration indicated by equation $2.2-3$. As an example, assume the input resistor for $e_{3}$ is 10 K ohms; equation $2.2-3$ becomes:

$$
\begin{equation*}
e_{0}=-\int_{0}^{t}\left[e_{1}+e_{2}+10 e_{3}+\ldots \cdot d d t+V_{0}\right. \tag{EQ.2.2-4}
\end{equation*}
$$

Similarily, should the capacitance of $c$ change to a value of $Y$ microfarads, then all of the inputs must be multipiled by a factor of $10 / Y$ (where $Y$ is in microfarads) before summation and integration. As an example, when the TR-48 is placed in repetitive operation (with the $10 \beta$ plug in place) the feedback capacitor beomes 0.02 microfarads. Each input must therefore be multiplied by a factor of $10 / 0.02$ or 500 . Should c be changed to 0.02 microfarads and the input resistor changed from 100 K to 10 K , that particular input is multiplied by $10 / 0.02$ times $100 \mathrm{~K} / 10 \mathrm{~K}$ or 5000 .

It can be seen, therefore, that the integrator rate-of-integration may be changed for individual inputs by changing the value of the input resistor, or the rate may by changed for all of the inputs by changing the value of the feedback capacitor.

A normal-time rate integrator of the TR- 48 produces an output voltage rate of change of 1 volt-per-second per-volt input via a 100 K resistors, and a output change of 10 volts-per-second perwolt input when the input is applied via a 10 K resistor (gain-of-one and gain-of-ten inputs of the dual d-c amplifier, respectively). With the $10 \beta$ plug removed, the gain-of-one and ten inputs provide a 10 volt-per-second pervolt and a 100 volt-per-second per-volt rate-of-change respectively.

The integrator, unlike most computational components, produces a varying output with a fixed input; therefore, if the integrators are controlled by the computer mode switches the overall operation of the computer is actually being controlled. The relays, K1, K2, and K3, of Figure 2.2-2 control the integrator operation in response to the computer mode switches. The following sub-paragraphs describe the relay positions for each of the computer modes and the integrator operation in each of these modes.
(1) Pot-Set Mode. In the pot-set mode all three of the relays are de-energized and attain the positions shown in Figure 2.2-2. Relay K2 grounds the resistor summing junction thus permitting the adjustment of any potentiometers connected to the integrator input under actual load.
(2) Reset Mode. Relay K3 is energized via the reset bus (contacts 2 and 3 make) and the capacitors are charged to the potential applied to the IC termination. Relays K1 and K2 remain de-energized.
(3) Operate Mode. Relay K3 is energized via the operate bus (contacts 1 and 2 make). Relay K2 is also energized by the operate bus via diode CR1. The inputs applied to the resistor network are applied to the amplifier and integrated.
(4) Hold Mode. This mode de-energizes all the relays; thus, integration is stopped and the unit is essentially in the pot-set condition. The main difference is that the pot set relay of the dual d-c amplifier is not energized; thus the amplifier output remains at the level determined by the charge on the feedback capacitor.
(5) Rep-Op Mode. This mode energizes the TS bus which in turn pulls in K1 and K2 (via CR2) and maintains them in the energized state as long as the computer is in repetitive operation. Relay $K 3$ remains free to respond to the reset and operate bus voltages.

## c. Maintenance

Since the high-gain amplifier and integrator-networks are contained in separate modules it is relatively simple to localize malfunctioning units. Integrator malfunctions are not normally due to the integrator network because the network contains so few components and these components are conservatively rated. Most integrators with unacceptable characteristics probably are caused by a high-gain amplifier that has high offset; consequently all tests should be performed with an amplifier of known satisfactory characteristics.
(1) Test Procedures
(a) Operational Check. The following simple operational check indicates the qualitive performance of the integrator.
(1) Patch the test circuit shown in Figure 2.2-3. Place the computer in the reset mode.
(2) Close S 1 ; the TDVM should read zero.
(3) Close S 2 ; the TDVM should read +10 volts.
(4) Place the computer in hold. The TDVM reading should remain at +10 volts.
(5) Place the computer in operate. The integrator output should change linearly from +10 volts at a rate of minus one volt per second. (A stop watch will normally be of sufficient accuracy for maintenance purposes for this test. If accurate measurement is required a more elaborate time-measuring procedure is required.)
(6) After exactly 20 seconds of operation place the computer in hold; the TDVM should read -10 volts.
(7) Place the computer in reset; the TDVM should read +90 volts.
(2) Initial Condition Resistor Ratia Check
(a) Set up the test circuit shown in Figure 2.2-4. Place the computer in the reset mode.
(b) Place both function switches in the left (L) position; record the TDVM reading.
(c) Place both function switches in the right ( R ) position; record the TDVM reading.
(d) The algebraic average of the readings in (b) and (ㄷ) , divided by 10 , should be less than 20 millivolts. (The algebraic average is the algebraic sum divided by two.)
(e) If the results of this test are unsatisfactory, the initial condition resistors are probably out of tolerance.
(3) Integrator Drift Rate
(a) Set up the test circuit shown in Figure 2.2-5. Place the computer in the reset mode.
(b) Place the computer in operate; after 100 seconds record the TDVM reading.
(c) The meter reading should be less than 0.05 volts; 0.05 volts corresponds to a drift rate of 50 microvolts per second.

## d. Trouble Analysis

A point-to-point resistance check is the quickest way to troubleshoot a malfunctioning integrator network. Comparison of readings with a properly functioning unit will frequently aid in isolating faulty components. The following table lists symptoms and probable causes for some malfunctions; this table assumes the high-gain amplifier is functioning properly. The table is not complete for all possible symptoms and causes; however, it should serve as a guide in troubleshooting.

| Mode | Symptom of Malfunction | Probable Cause |
| :---: | :---: | :---: |
| Reset | Amplifier output is zero for all ini- <br> tial condition inputs. | 1. Open IC input re- <br> sistor. <br> 2.Reset relay not <br> operating. <br> 3. Shorted feedback <br> capacitor. |
|  | Amplifier goes into overload if inputs <br> are connected. | Operate Relay is en- <br> ergized. |


| Mode | Symptom of Malfunction | Probable Cause |
| :---: | :---: | :---: |
| Reset (cont.) | Amplifier goes into overload when IC input is applied. The amplifier holds the voltage reached while in operation with no IC input | Open IC feedback resistor. |
|  | The amplifier output is not equal in magnitude to the initial condition input. | Ratio of IC Resistors is not unity. |
| Hold | Amplifier will not hold voltage reached during operation but resets to the IC input. | Reset relay energized. |
|  | Amplifier will not hold voltage reached during operation nor will it hold the IC input level. | Leaky or open feedback capacitor. |
| Operate | Integrator does not have the proper integration rate. | Check circuit time constants. Wrong value of input resistor or feedback capacitor used (check $10 \beta$ plugs). |

(1) Applicable Drawings. The following drawings are contained in Volume II of this handbook.

Drawing Number
C012 764 OS

B045 034 OW

## Type

Schematic

Wiring

## Description

Schematic Diagram of Dual D.C. Integrator Model 12.764.

Contains sheets listing wiring from the 12.764 rear mating connector to other points within the computer.
(2) Parts Lists. Appendix I contains the replaceable parts lists for the 12.764 Integrating Network. See Index of Appendix I.

## 3. QUARTER-SQUARE MULTIPLIER 7.099

The Model 7.099 Quarter-Square Multiplier as the input impedance of an external high-gain amplifier permits the multiplication of two variables (Figure 2.3-1). This unit utilizes the quarter-square multiplication technique to produce the product of two variables ( $X$ and $Y$ ) as illustrated by equation 2.3-1.

$$
\begin{equation*}
X Y=\frac{1}{4}\left[(X+Y)^{2}-(X-Y)^{2}\right] \tag{EQ.2.3-1}
\end{equation*}
$$



The TR-48 quarter-square mutiplier is basically a biased-diode circuit application of this technique. The design and Pre-Patch Panel termination configuration is such that the multipliers are also capable of division, squaring*, and obtaining the square root of an input variable.

## a. Operating Considerations

As previously indicated, the quarter-square multiplier is capable of performing four primary functions. The patching procedures for the multiplier divides these four functions into two separate groups: the multiplication-division group and the square-square root group. The two upper cross hatched areas of the patching block are marked with a capital $M D$ and a small square and square root sign respectively. A four-connector bottle plug connected in one or the other of these areas determines which functions the multiplier can perform.

Placing the four-connector plug in the square-square root area, leaving the MD exposed, prepares the multiplier for multiplication or division. Placing the four connector plug in the $M D$ area, leaving the small square and square root sign exposed, prepares the multiplier for squaring and/or obtaining the square root of an input variable. Note in each case that the function to be performed is exposed, while the bottle plug covers the other cross hatched area. This feature permits the operator to glance at a multiplier and tell whether its being used for multip-lication-division or square-square root operation.

Figure $2.3-2$ is a simplified patching diagram of the quarter-square multiplier. During multiplication both the positive and negative $X$ and $Y$ inputs are required even if neither of these inputs change sign during the problem solution. (The $X$ and $Y$ inputs are applied as shown in the figure regardless of the actual polarity of these variables.)

The multiplier is used as the input impedance for the operational amplifier when multiplying two variables. For division the multiplier is used as a feedback element for the operational amplifier. See the Operator's Handbook for the patching procedure for division, squaring, or square root operation.

When using the multiplier for division the following restrictions must be observed:
(1) The absolute value of the divisor must always be greater than or equal to the absolute value of the dividend.
(2) The divisor must not change sign. The divisor may be either positive or negative but it must not change in sign during a problem run.
(3) The divisor must never equal zero.
b. Theory of Operation

As previously stated the 7.099 multiplier utilizes the quarter-square multiplication technique illustrated by equation 2.3-1.

[^1]The TR-48 quarter-square multipliers employ diode function generators which in one case sums the two input variables and squares this sum. The output current of this DFG is in proportion to the quantity $1 / 4(X+Y)^{2}$. A second DFG takes the difference of the two inputs and squares this difference; the output in this case is negative and in proportion to $-1 / 4(X-Y)^{2}$. If these two currents are summed by an operational amplifier with an appropriate value feedback resistor, equation 2.3-1 is satisfied as follows:

$$
\begin{equation*}
1 / 4(X+Y)^{2}+\left[-1 / 4(X-Y)^{2}\right]=1 / 4\left[(X+Y)^{2}-(X-Y)^{2}\right]=X Y \tag{EQ.2.3-2}
\end{equation*}
$$

The two DFG outputs are scaled by a factor of one tenth; thus, the summing amplifier output is actually $1 / 10$ of the product XY. This permits both inputs, $X$ and $Y$, to reach a magnitude of 10 volts and not overload the amplifier. In addition, the amplifier inverts the input polarity; therefore, the amplifier output is actually -XY/10.

Figure 2.3-3 is a simplified schematic of the $(X+Y)^{2}$ DFG portion of the quartersquare multiplier. Each diode is back-biased at a different negative potential; thus, as the sum of $X$ and $Y$ increases, more diodes conduct (or reach their break points). As each diode conducts, the ratio of the feedback to input impedance of the amplifier changes in a pre-determined manner such that the amplifier output approximates the $(X+Y)^{2}$ curve. The input resistor and bias potential are selected so that the current through the diodes is equivalent to one tenth the square of $X$ plus $Y$. By providing a second DFG to produce an output current equivalent to minus one-tenth the square of the difference between $X$ and $Y$ and connecting it to the input of the amplifier for summation with the $(X+Y)^{2}$ current, equation 2.3-2 is satisfied.

To permit the multipliers to accept positive and negative values of either or both $X$ and $Y$ inputs and to allow both to vary in magnitude such that either may be larger, a combination of DFG units is required.

Figure $2.3-4$ is a simplified schematic of a quarter-square multiplier patched for multiplication. In the multiplier there are actually four DFG units similar to the one shown in Figure 2.3-3. In Figure 2.3-4, however, each DFG unit is simplified and shown as a composite with one diode, bias resistor, etc. At any one time only two of the four cards will conduct and produce the product of $X$ and $Y$ at the amplifier output.

Considering that either or both $X$ and $Y$ can be negative and that either may be the larger, there are eight combinations of polarity and magnitude relationships of $X$ and $Y$ that may be applied to the multiplier. All eight of these combinations are listed in Table 2.3-1; the DFG card designation (1, 2, 3, or 4) corresponds to the notations of Figure 2.3-4.

Note that on Figure 2.3-4 as well as on the actual Pre-Patch Panel of the TR-48 the $X$ and $Y$ input terminations are designated as $+X,+Y,-X$, and $-Y$. The sign designations of these terminations do not necessarily indicate the actual polarity



of either $X$ or $Y$ ．The $X$ and $Y$ variables as they are multiplied for the problem solution are applied to $+X$ and $+\mathbb{Y}$ respectively，regardless of their actual polarity． The inversion of these signals are applied to $-X$ and $-Y$ ．Thus，even if the problem variable $X$ is always negative，it is still patched to $+X$ and the inverted problem variable $X$ is patched to $-X$ ．

The first column of Table 2.301 gives the eight possible input combinations of $X$ and $Y$ ．The second column indicates the DFG unit considered in the remaining columns． The third column indicates the actual polarity of $X$ and $Y$ applied to the cards with respect to the conditions of column $\mathrm{I}_{\text {。 }}$ The foumth column indicates the polarity of the resultant summation of $X$ and $Y$ and the fifth column indicates the bias potential applied to the card diodes．For a card to conduct and provide an output，columns four and five must be of opposite polarity，otherwise the $X$ and $Y$ summation adds to the back bias of the diodes．

The last column（card output）indicates whether or not a card is conducting and if the current is proportional to the sum of $X$ and $Y$ or the difference（indicated as $(X+Y)^{2}$ and $(X-Y)^{2}$ respectively）。 These designations do not indicate the polarity of the signals and are not intended to indicate that a voltage may be read out at the mplifier summing junction（the amplifier summing junction is normally at viro tual ground potential）．

As an example of the quarter－square multiplier operation consider the first input combination of table 2.300 。 $X$ is positive，$Y$ is positive and $X$ is always larger than $Y$ ．DFG cards 2 and 3 do not conduct because in each case the summation of $X$ and $Y$ is additive to the reverse bias of the card diodes（as long as the three con－ ditions as stated above hold true）．

Card I will conduct because the summation of $X$ and $Y$ is positive and will overcome the negative severse bias of the card．The number of diodes that conduct is depend－ ent on the magnitude of this summation．Card 1 will produce a current output that is proportional to onementh of $1 / 4(X+Y)^{2}$ thus satisfying half of equation $2.3-1$ ．

Card 4 will also conduct because the summation of $X$ and $Y$ is negative in polarity and the diodes are reverse biased by a positive potential．（The inverted polarity of the variable $X$ is applied to this card and because $X$ is larger than $Y$ the rem sultant summation must be negative．）Since $X$ and $Y$ are opposite in polarity the resultant current output satisfies the $(X-Y)^{2}$ portion of the equation．In addi－ tion，because $X$ is larger and negative，this current is equivalent to minus one tenth of $1 / 4(X-Y)^{2}$ 。Thus，equation $2.3-1$ is satisfied as follows：

（EQ．2．3－3）

The XY product of the quarter © qqugre maltiplier is actually negative，however，due to the inversion by the amplifier．

Note that the cards supplying the $(X+Y)^{2}$ current and $(X-Y)^{2}$ current of the first two and last two input combinations of Table 2.3-1 are opposite to that of the middle four combinations, i.e., $(X+Y)^{2}$ is due to a positive $X$ and $Y$ summation in one case, and due to a negative $X$ and $Y$ summation in the other. This indicates the middle four combinations will produce a product opposite in polarity to the other four combinations; this should be the case since the middle four combinations consist of $X$ and $Y$ inputs of opposite sign.
c. Maintenance and Test Procedures

The Quarter-Square Multiplier is factory calibrated prior to shipment; re-calibration should not be attempted unless definitely indicated after throughly checking the unit. The multiplier requires the use of external high-gain amplifiers; ascertain that these components are functioning properly before attempting to troubleshoot the multiplier.
(1) D.C. Error Check
(a) Set up the test circuit shown in Figure 2.3-5. The input/feedback resistors of the amplifiers should be matched to $\pm 0.02 \%$ or better.
(b) Set the oscillator for a frequency of 5 cycles/second at 20 volts peak-to-peak amplitude.
(c) Set the oscilloscope $Y$ sensitivity to 10 millivolts/centimeter D.C. with zero reference in the center. Set the $X$ sensitivity for 2 volts/ centimeter.
(d) With both function switches in the position shown, observe the scope trace; Figure 2.3-5b. This waveform should not exceed 100 millivolts peak-to-peak. (This set up checks the two squaring circuits on PC1.)
(e) Place both function switches in the R position; observe the scope trace. (This setup checks the two squaring circuits on PC2.)
(2) Phase Shift and Gain Error Check
(a) Retain the test setup of Figure 2.3-5. Increase the oscillator frequency to 1 KC at 20 volts peak-to-peak.
(b) With both function switches as shown on Figure 2.3-5, observe the scope trace and compare to Figure 2.3-6. The distance from A to B represents the phase shift error in millivolts ( 90 millivolts peak-to-peak maximum or 0.26 degrees). The distance from $C$ to $D$ represents the gain error in millivolts ( 160 millivolts peak-to-peak maximum). (This checks PC1.)
(c) Repeat step (b) with both function switches in the $R$ position to check PC2。

a. TEST SETUP

b. 5c.p.s. WAVEFORM

FIGURE 2.3-5 MULTIPLIER DC ERROR TEST SETUP AND TYPICAL WAVEFORM


FIGURE 2.3-6 I KC WAVEFORM

TABLE 2.3-1 Multiplier Input Combination and Card Conduction Sequence*

| X and Y Polarity \& Magnitude Relationship | DFG Card Designation | Actual Card Input Polarity | $\begin{array}{\|c} \hline \text { Polarity of } \\ X \& Y Y \\ \text { Summation } \end{array}$ | Card Bias Polarity | Card** <br> Output |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```X positive (+) Y positive (+) X>Y``` | 1 | X ( + ), Y ( + ) | (+) | (-) | $(X+Y)^{2}$ |
|  | 2 | $\mathrm{X}(+), \mathrm{Y}(-)$ | (+) | (+) | None |
|  | 3 | $\mathrm{X}(-), \mathrm{Y}(-)$ | (-) | $(-)$ | None |
|  | 4 | X ( - , , Y (+) | (-) | (+) | $(X-Y)^{2}$ |
| ```X positive (+) Y positive (+) X<Y``` | 1 | $\mathrm{X}(+), \mathrm{Y}(+)$ | (+) | (-) | $(X+Y)^{2}$ |
|  | 2 | $X(+), Y(-)$ | (-) | (+) | $(X-Y)^{2}$ |
|  | 3 | $X(-), Y(-)$ | (-) | (-) | None |
|  | 4 | $X(-), Y(+)$ | (+) | (+) | None |
| ```X positive (+) Y negative (-) X>Y``` | 1 | $\mathrm{X}(+), \mathrm{Y}(-)$ | (+) | (-) | $(X-Y)^{2}$ |
|  | 2 | $\mathrm{X}(+), \mathrm{Y}(+)$ | (+) | (+) | None |
|  | 3 | $\mathrm{X}(-), \mathrm{Y}(+)$ | $(-)$ | $(-)$ | None |
|  | 4 | $\mathrm{X}(-), \mathrm{Y}(-)$ | (-) | (+) | $(\mathrm{X}+\mathrm{Y})^{2}$ |
| $\begin{gathered} \mathrm{X} \text { positive }(+) \\ \text { Y negative (-) } \\ \mathrm{X}<\mathrm{Y} \end{gathered}$ | 1 | $X(+), Y(-)$ | (-) | (-) | None |
|  | 2 | $X(+), Y(+)$ | (+) | (+) | None |
|  | 3 | $X(-), Y(+)$ | ( + ) | (-) | $(X-Y)^{2}$ |
|  | 4 | $X(-), Y(-)$ | $(-)$ | (+) | $(X+Y)^{2}$ |
| ```X negative (-) Y positive (+) X>Y``` | 1 | $\mathrm{X}(-), \mathrm{Y}(+)$ | (-) | (-) | None |
|  | 2 | $X(-), Y(-)$ | (-) | (+) | $(\mathrm{X}+\mathrm{Y})^{2}$ |
|  | 3 | $X(+), Y(-)$ | (+) | (-) | $(\mathrm{X}-\mathrm{Y})^{2}$ |
|  | 4 | $X(+), Y(+)$ | (+) | (+) | None |
| $\begin{gathered} X \text { negative }(-) \\ Y \text { positive }(+) \\ X<Y \\ \hline \hline \end{gathered}$ | 1 | $X(-), Y(+)$ | (+) | (-) | $(X-Y)^{2}$ |
|  | 2 | $X(-), Y(-)$ | (-) | (+) | $(X+Y)^{2}$ |
|  | 3 | $\mathrm{X}(+), \mathrm{Y}(-)$ | (-) | (-) | None |
|  | 4 | X (+), Y (+) | (+) | (+) | None |
| $\begin{gathered} X \text { negative }(-) \\ Y \text { negative }(-) \\ X>Y \\ \hline \end{gathered}$ | 1 | $X(-), Y(-)$ | (-) | $(-)$ | None |
|  | 2 | $X(-), Y(+)$ | (-) | (+) | $(X-Y)^{2}$ |
|  | 3 | $X(+), Y(+)$ | $(+)$ | (-) | $(X+Y)^{2}$ |
|  | 4 | $\mathrm{X}(+), \mathrm{Y}(-)$ | (+) | $(+)$ | None |
| ```X negative (-) Y negative (-) X<Y``` | 1 | $X(-), Y(-)$ | (-) | $(-)$ | None |
|  | 2 | $X(-), Y(+)$ | (+) | (+) | None |
|  | 3 | $X(+), Y(+)$ | (+) | (-) | $(\mathrm{X}+\mathrm{Y})^{2}$ |
|  | 4 | $X(+), Y(-)$ | (-) | (+) | $(X-Y)^{2}$ |

* When $X=Y$ in magnitude, either the $X+Y$ or $X-Y$ term equals zero; thus only one card will actually conduct. As an example, when $X=Y$ and both are positive in polarity only card 1 conducts; if both are negative only card 4 conducts.
** See Text
(3) Diode Break-Point Check and Adjustment. The following procedure permits checking of the multiplier diode break-point settings. Before attempting to change any of the break-point potentiometer adjustments, double check the test set-up; be certain that the associated amplifiers are functioning properly, and be sure the proper potentiometer is being adjusted.
(a) Patch the multipliers as shown in Figure 2.3-7b.
(b) Apply the positive inputs listed in Table 2.3-2 (in sequence starting at 2.5V) for Figure 2.3-7b. The TDVM should read out the potential listed in the output column in each case. (Note that the output may be $\pm 0.01$ volt.)
(c) If any output reading indicates adjustment is necessary, adjust the potentiometer listed in the potentiometer column.
(d) Repeat steps (b) and (c) as necessary;interaction of the DFG break-point settings necessitates this procedure for optimum accruacy.
(e) Patch the multiplier as shown in Figure 2.3-7c. (Note the patch connection in the lower portion of the $M D$ area; note also that the $+Y$ termination at the top of the patching block must be used.)

TABLE 2.3-2 Multiplier Adjustment Data; PC1

| Figure <br> Reference | Input Voltage | Potentiometer | Output |
| :---: | :---: | :---: | :---: |
| Figure <br> $2.3-7 \mathrm{~b}$ | +2.5 V | PC1-R1 | $-0.64 \mathrm{~V} \pm .01$ |
|  | +3.9 V | PC1-R2 | $-1.54 \mathrm{~V} \pm .01$ |
|  | +5.3 V | PC1-R3 | $-2.82 \mathrm{~V} \pm .01$ |
|  | +6.7 V | PC1-R4 | $-4.50 \mathrm{~V} \pm .01$ |
|  | +8.1 V | PC1-R5 | $-6.58 \mathrm{~V} \pm .01$ |
|  | +9.5 V | PC1-R6 | $-9.04 \mathrm{~V} \pm .01$ |
|  | -2.5 V | PC1-R7 | $+0.64 \mathrm{~V} \pm .01$ |
|  | -3.9 V | PC1-R8 | $+1.54 \mathrm{~V} \pm .01$ |
|  | -5.3 V | PC1-R9 | $+2.82 \mathrm{~V} \pm .01$ |
|  | -6.7 V | PC1-R10 | $+4.50 \mathrm{~V} \pm .01$ |
|  | -8.1 V | PC1-R11 | $+6.58 \mathrm{~V} \pm .01$ |
|  | -9.5 V | PC1-R12 | $+9.04 \mathrm{~V} \pm .01$ |



FIGURE 2.3-7 MULTIPLIER ADJUSTMENT LOCATION AND TEST SETUP PATCHING
(f) Repeat steps (b) through (d) but apply the inputs listed in table 2.3-2 for Figure 2.3-7c.
(g) Patch the multiplier as shown in Figure 2.3-7d.
(h) Repeat steps (b) through (d) but apply the inputs listed in table 2.3-3 for Figure 2.3-7d.
(i) Patch the multiplier as shown in Figure 2.3-7e. Note that the $+Y$ input toward the bottom of the patching block must be used.
(i) Repeat steps (b) through (d) but apply the inputs listed in table 2.3-3 for Figure 2.3-7e.

TABLE 2.3-3 Multiplier Adjustment Data; PC2

| Figure <br> Reference | Input Voltage | Potentiometer | Output |
| :---: | :---: | :---: | :---: |
| Figure$2.3-7 d$ | $+2.5 \mathrm{~V}$ | PC2-R1 | $-0.64 \mathrm{~V} \pm .01$ |
|  | +3.9V | PC2-R2 | $-1.54 \mathrm{~V} \pm .01$ |
|  | $+5.3 \mathrm{~V}$ | PC2-R3 | $-2.82 \mathrm{~V} \pm .01$ |
|  | +6.7V | PC2-R4 | $-4.50 \mathrm{~V} \pm .01$ |
|  | +8.1V | PC2-R5 | $-6.58 \mathrm{~V} \pm .01$ |
|  | $+9.5 \mathrm{~V}$ | PC2-R6 | $-9.04 \mathrm{~V} \pm .01$ |
| $\begin{aligned} & \text { Figure } \\ & 2.3-7 e \end{aligned}$ | $-2.5 \mathrm{~V}$ | PC2-R7 | $+0.64 \mathrm{~V} \pm .01$ |
|  | -3.9V | PC2-R8 | $+1.54 \mathrm{~V} \pm .01$ |
|  | -5.3V | PC2-R9 | $+2.82 \mathrm{~V} \pm .01$ |
|  | $-6.7 \mathrm{~N}$ | PC2-R10 | $+4.50 \mathrm{~V} \pm .01$ |
|  | -8.1V | PC2-R11 | $+6.58 \mathrm{~V} \pm .01$ |
|  | -9.5V | PC2-R12 | $+9.04 \mathrm{~V} \pm .01$ |

(4) Applicable Drawings. The following diagrams are contained in Appendix II of this handbook.

Drawing Number
C007 099 OA

Type
Assembly

## Description

Assembly diagram of 7.099 Multiplier.

Drawing Number
B007 099 OS

C007 044 OS

B045 034 OW
Wiring

## Description

Schematically shows connections between patching block and printed circuit card and between the cards and the rear module connector.

Schematic diagram of 7.096 multiplier printed circuit cards.

Contains run sheets listing wiring from the multiplier rear mating connectors to other points within the computer.
(5) Parts Lists. Appendix I contains the replaceable parts lists for the 7.099 quarter-square multiplier. See Index of Appendix I.
4. $X^{2}$ DIODE FUNCTION GENERATOR 16.275

The $X^{2}$ Diode Function Generator (Figure 2.4-1) is capable of producing $+X^{2}$ or $-X^{2}$ for limited or bi-polar inputs, as well as extracting the square-root of an input. These functions are generated by using the DFG as the input ( $X^{2}$ ) or feedback ( $\sqrt{X}$ ) elements of a high-gain d-c amplifier.

The output functions are approximated by a series of straight line-segments of various slopes. The slopes of the line segments are attained by a series of paralleled resistors each with a diode gate in series. The diode gates are reverse biased such that the input magnitude must attain certain levels to cause succeeding diodes to conduct. As a diode conducts (or the diode breakpoint is reached) the gain of the operational amplifier used in conjunction with the generator changes so the line segment slope approximates that of the function curve. The breakpoint of each diode gate is selected so that the amplifier output produces a very accurate approximation of the $X^{2}$ function.

## a. Operating Considerations

The $X^{2}$ DFG actually consists of two independent $X^{2}$ DFG's: one which produces an $X^{2}$ output for input of $X \leq 0$ and one which produces an $X^{2}$ output for inputs of $X \geq 0$. These two individual DFG units may be combined to produce $X^{2}$ for inputs of $-10 \leq$ $\mathrm{X} \leq+10$ 。

This paragraph only describes the patching procedures required to operate the DFG as separate units. This will enable the technician to check out each circuit individually. The patching procedures for operating the DFG in other configurations are given in the TR-48 Operator's Manual (Appendix IV).

Figure 2.4-2 shows the patching configuration for operating the two DFG's of the 16.275 unit individually; the diagram also gives the input signal limits.

b. PATCHING BLOCK

FIGURE 2.4-1 $\mathrm{x}^{2}$ DFG, MODEL 16.275


FIGURE 2.4-2. $-\frac{x^{2}}{10}$ AND $+\frac{x^{2}}{10}$ patching configuration

## b. Theory of Operation

As previously stated the $X^{2}$ DFG actually consists of two separate function generators; one accepts only positive inputs, and the other accepts only negative inputs. The two units are essentially identical with respect to theory of operation and differ mainly in diode orientation and polarity of bias voltage. This description will, therefore, cover only the circuit which accepts negative input values of X .

Drawing C016 275 OS is the schematic diagram of the entire $X^{2}$ unit; Figure 2.4-3 is a simplified schematic of the negative input portion (right-hand portion of C 016 275 OS). (The temperature compensation thermistors and certain bias resistors, as well as some of the gated resistor networks are eliminated for clarity.)

The diodes, CR8, CR9 ....CR13, and CR14 are back biased at different potentials so that as the input signal reaches various levels more and more of the diodes conduct. As each diode conducts, the slope of the amplifier output is changed and corrects the straight line approximation of the $\mathrm{X}^{2}$ curve.

The $X^{2}$ DFG can also be used to produce $\sqrt{X}$ by using the unit as a feedback element for the amplifier, i.e., the diode-resistor networks replace R3, and R3 becomes a fixed input resistor. The patching configuration for this function as well as others, are given in the Operator's Manual. If the DFG's function properly when patched as shown in Figure 2.4-2 the $X^{2}$ DFG may be assumed to be in proper working order. Should the DFG then indicate a fault when patched in another operational mode the error is generally external to the DFG (improper patching, faulty external component, etc.).

## c. Maintenance and Test Procedures

The $X^{2}$ DFG is designated with high-quality, conservatively rated components and will provide long-term trouble-free operation. The unit is factory calibrated prior to shipment; re-adjustment should only be attempted when definitely indicated by thorough checkout.

## (1) $X^{2}$ DFG Test Procedure

(a) Set up the test circuit shown in Figure 2.4-4.
(b) Set potentiometers 1, 2, and 3 for the values indicated on the diagram. Potentiometer 5 is to be set so the comparator switches when IN reaches -10 volts.
(c) Set function switch $F_{1}$ to +10 volts (L) and $F_{2}$ to the output of Integrator 1 (L).
(d) Place the computer in reset and than in operate. When the comparator switches (at -10 volts, thus placing both integrators essentially in the hold mode) adjust potentiometer 4 for a -10 volt output from amplifier (measure with TDVM).
(e) Place the computer in reset; address amplifier 5 for readout on the TDVM. Set the computer in operate and note TDVM variations. The maxreading should not exceed 0.4 volts ( $0.4 \%$ or 40 millivolts into a gain-of-ten amplifier). Typical error is $0.2 \%$ or 0.2 volts on TDVM.
(f) The above procedure checks the $X^{2}$ unit for a negative input. If desired to obtain an error plot, connect this circuit to the $X$ and $Y$ inputs of a VARIPLOTTER as shown by dotted lines on Figure 2.4-4.
(g) To check the generator for a positive input, place function switches $F_{1}$ and $F_{2}$ in the $R$ position and repeat step (e).
(2) $X^{2}$ DFG Break-Point Adjustment. The following adjustments should only be attempted when definitely indicated as necessary. The amplifiers used in conjunction with the $X^{2}$ DFG during this procedure must be functioning properly.
(a) Patch the $X^{2}$ DFG as shown in Figure 2.4-5b.
(b) Apply the positive inputs listed in Table 2.4-1 (in sequence starting at 2.5 V ). The TDVM should read out the potential listed in the output column in each case.
(c) If any readout indicates adjustment is necessary, adjust the potentiometer listed in the middle column.
(d) Repeat steps (b) and (c) as necessary; interaction of the DFG breakpoint settings necessitates this procedure for optimum accuracy.
(e) Patch the $X^{2}$ DFG as shown in Figure 2.4-5c.
(f) Repeat steps (b) through (d) but use the data listed in Table 2.4-2.

TABLE 2.4-1

| Input Voltage | Potentiometer | Output |
| :---: | :---: | :---: |
| +2.5 V | $R 1$ | $-0.64 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| +3.9 V | $R 2$ | $-1.54 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| +5.3 V | $R 3$ | $-2.82 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| +6.7 V | $R 4$ | $-4.50 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| +8.1 V | $R 5$ | $-6.58 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| +9.5 V | $R 6$ | $-9.04 \mathrm{~V} \pm .01 \mathrm{~V}$ |



FIGURE 2.4-3 NEGATIVE INPUT $x^{2}$ DFG, SIMPLIFIED SCHEMATIC


FIGURE 2.4-4 $x^{2}$ DFG TEST SETUP


FIGURE 2.4-5 $x^{2}$ DFG ADJUSTMENT LOCATION AND PATCHING

TABLE 2.4-2

| Input Voltage | Potentiometer | Output |
| :---: | :---: | :---: |
| -2.5 V | R 7 | $+0.64 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| -3.9 V | R 8 | $+1.54 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| -5.3 V | R 9 | $+2.82 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| -6.7 V | R 10 | $+4.50 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| -8.1 V | R 11 | $+6.58 \mathrm{~V} \pm .01 \mathrm{~V}$ |
| -9.5 V | R 12 | $+9.04 \mathrm{~V} \pm .01 \mathrm{~V}$ |

(3) Applicable Drawings. The following drawings are contained in Volume II of this handbook.

Drawing Number
C016 275 OA

C016 275 OS
BO45 034 OW

Type
Assembly

Schematic
Wiring

## Description

Shows components mounted on module block and wiring from block to printed circuit card.

Schematic diagram of $\mathrm{X}^{2}$ DFG unit.
Contains run sheets listing wiring from 16.275 rear mating connectors to other points in the computer console.
(4) Parts Lists. Appendix I contains the replaceable parts lists for the 16.275 amplifier. See Index of Appendix I.
5. LOOG X $(16.276)$ AND $1 / 2$ LOG $X(16.281)$ DIODE FUNCTION GENERATORS

The 16.276 Log X DFG and $16.281 \mathrm{1} / 2 \mathrm{Log} X$ Diode Function Generators (Figure 2.5-1) generate a logarithmic function of an input variable. These units are extremely versatile since they may be used to perform multiplication, division, squaring, obtaining the square-root in addition to the capability of raising an input to an unusual or variable power.

The $16.276 \log X$ and $16.2811 / 2$ Log $X$ DFG units are essentially identical in theory and operation; the main difference lies in the output function. The output function of the Log X DFG is scaled at five times the $\log$ to the base 10 of ten times the absolute value of $X$ (equation 2.5-1).

$$
\begin{equation*}
e_{0}=-5 \log _{10}(10|x|) \tag{EQ.2.5-1}
\end{equation*}
$$

The minus sign of equation $2.5-1$ indicates the polarity of the $D F G$ output ( $e_{0}$ ) is
opposite to that of the input variable $X, i_{0} e_{0}$ if $X$ is positive, $e_{0}$ is negative. The output function of the $16.2811 / 2$ Log X DFG is, as indicated, half of that of equation 2.5-1 or:

$$
\begin{equation*}
e_{0}=-2.5 \log _{10}(10|X|) \tag{EQ.2.5-2}
\end{equation*}
$$

Both the Log $X$ and $1 / 2 \log X D F G$ contain four separate $\log$ function generators: two cards which accept only positive inputs and two cards which accept only negative in puts.

## 2. Operating Considerations

Figure $2.5-2$ illustrates the patching procedure for obtaining the $\log$ of $+X$ and $-X$ with the 16.276 Log $X$ DFG. The patching for the $16.2811 / 2$ Log $X$ DFG is similar; as indicated previously the difference lies in the output function.

Note that the maximum value of the output of the 16.276 unit occurs when $X$ is either plus or minus 10. The output is, therefore, $\pm 5 \log _{10} 10 / 10 \mid= \pm 10$ volts. The $1 / 2$ $\log X$ unit, therefore, with an output equal to $1 / 2$ of the 16.276 unit has a maximum output voltage range of $\pm 5$ volts.

In Figure 2.5-2 the lower two DFG input cards are patched as separate $\log X$ DFG units with limited inputs. The top two cards are shown combined permitting an input where $-10 \leq X \leq+10$ volts.

During maintenance checkout procedures, by operating each DFG as a separate limited input unit, a fault may be rapidly isclated to a small portion of the overall cirm cuitry.

## b. Theory of Operation

Drawings C016 276 OS and C016 281 OS are the schematic diagrams of the Log $X$ and $1 / 2 \log X$ DFG printed circuit cards respectively. Comparing the two schematics reveals that the two are similar and actually only differ in resistor values. The resistor values of the 16.281 unit are approximately twice the magnitude of those of the 16.276 unit with the exception of $R 1$ through $R 4$ (the feedback resistors between the $R$ and $B$ terminations)。 It can be seen that the outputs of the $1 / 2 \mathrm{Log} X$ will ke onemalf the magnitude of the Log $X$ DFG。

Because of this similarity the Log X (16.276) DFG is used as the basis of this desm cription. Note on Schematic C016 276 OS that there axe two separate but similar circuits. The circuit on the left-hand side responds only to negative input signals; the circuit on the right-hand side responds only to positive input signals. These two circuits differ only in the orientation of the diodes with respect to the bias voltages and also the polarities of the bias voltages. Again, due to this similarity, only the rightohand circuit (sensitive to positive input signals) is described.


FIGURE 2.5-1 LOG $\times$ DFG, MODEL 16.276 ( $\frac{1}{2}$ LOG $\times$ DFG 16.281 SIVILAR)


FIGURE 2.5-2 LOG $\times$ DFG PATCHING DIAGRAM
( $\frac{1}{2}$ LOG $\times$ DFG SIMILAR)

Figure 2.5-3 is a simplified schematic of the positive input circuit of the 16.276 Log X DFG. This circuit functions in a maner similar to all of the DFG units of the TR-48; as the input signal reaches various levels the input-oto feedback impedance ratio is changed, thus changing the gain of the associated amplifiar. In the case of the Log $X$ DFG there are six changes in slope of the amplifier output, or six straight-line segments are used to approximate the log curve.

The main difference in the Log $X$ circuit operation as compared to most other TR-48 DFG units is that with a neax zero input all of the diodes are forward biased and conducting. Thus, when the input ( + IN) of Figure 2.5-3 is close to zero, resistors R25 through R31 are all in parallel and the amplifier has a gain greater than 10.

As the input level increases towerd +10 volts the diodes are reverse biased and their corresponding resistors are removed from the parallel group. This process continues until the gain of the amplifier is somewhat less than 0.25 ( 20.9 K input resistor, 5 K feedback resistor)。

Figure 2.5-4 compares graphically the input-to-output voltages of the Log X positive inpat circuit. Note that due to the inversion of the amplifier, the output signal is negative, or as previously indicated, $-5 \log 10$ 10\|Xl。 This curve illustrates the initial steep slope of the output curve (requiring a high amplifier gain) and the decrease in slope as $X$ approaches 10 volts (requixing. very small amplifier gain).
\&. Maintenance and Test Procedures
The Log $X$ and $1 / 2$ Log $X \quad D F G$ 's are factory calibrated prior to shipment. Adjustment should not be attempted unless definitely indicated as necessaxy by the dynamic error check described in the following sub-paragraph.
(1) Dynamic Error Test Procedure Log X Ded. This test can be used to indicate if adjustment of the Log DFG's is required and also to check the DFG output after completion of the adjustment procedure.
(a) Set up the test circuit shown in Figure 2.5-5a. (The setup shown is for the -Log $X$ cards only.) An oscilloscope or vol.tmeter may be substituted for the VARIPLOTIER. Set the plotter I input to 0.1 volt/inch sensitivity and the $X$ input to 1.0 volt/inch.
(b) Figure 2.5-5b shows a typical exror plot. Note that when checking a $-\log X$ card that the resultant plot starts at the right and runs to the left side of the plotter.
(c) If the error plot does not remain within the $\pm 0.1$ volt limits ( $0.1 \%$ error) refer to the static adjustment procedure.
(d) To check a $+\mathrm{Log} X$ card, substitute the plus for the minus card of Fi.gure 2.5-5 and change the IC input of the two integrators to +10 volts. Change the +10 inpirt to integrator- 2 to -10 volts.

The resultant error curve should be similar to Figure 2.5-5c. Note in this case the plot will run left to right.
(2) Dynamic Erroz Test Procedure 1/2 Log X DFG
(a) Set up a test circuit similar to that shown in Figure 2.5-5a with this single exception; the output of amplifier-3 should be applied to amplifier-4 through a gain-of-two input.
(b) The remainder of the test procedure and the results are the same as listed for steps (b) through (d) of the Log X cards.
(3) Static Adjustment Procedure: Log X DFG. The setup temperature should be approximately 750F.
(a) Set up the test circuit shown in Figure 2.5-6b.
(b) Apply the inputs as indicated in Table 2.6-1 in the sequence listed, to the +IN termination.
(c) If an adjustment is made, recheck the previous setting before proceeding to the next adjustment (due to interaction between adjustments).
(d) Repeat Steps (b) through (c) as necessary.
(e) Set up the test circuit for the second +Log X card. Repeat (b) through (d) but adjust the potentiometers on the PC2 unit.
(£) Set up the test circuit shown in Figure 2.5-6c. Apply the inputs listed in Table 2.6-2 to the -IN termination.
(g) Repeat Steps (c) through (e) but for the -Log cards. (See adjustment notations indicated in Table 2.6-2.)

Table 2.6-1. +Log X Adjustment Data

| +X Input | Number | justment. Potentiometer | TDVM Readout |
| :---: | :---: | :---: | :---: |
| +0.32V | 1 | PC1-R22 | $-2.15 \mathrm{~V}+0.05 \mathrm{~V}$ |
| +1.16V | 2 | PC1mR42 | $-5.23 \mathrm{~V}+0.05 \mathrm{~V}$ |
| +2.47V | 3 | PC1-R41 | $-6.92 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| +4.28V | 4 | PC1-RLO | $-8.13 \mathrm{~V}+0.05 \mathrm{~V}$ |
| +6.51V | 5 | PC1-R39 | $-9.05 \mathrm{~V}+0.05 \mathrm{~V}$ |
| +9.13V | 6 | PC1-R38 | $-9.79 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |



FIGURE 2.5-3 POSITIVE INPUT LOG X DFG CIRCUIT, SIMPLIFIED SCHEMATIC


FIGURE 2.5-4 GRAPHICAL INPUT-TO-OUTPUT COMPARISON OF POSITIVE INPUT LOG XDFG

a. TEST CIRCUIT

infut voltage (plotter $x$ input)
b. TYPICAL DYNAMIC ERROR PLOT; - LOG X DFG

$\begin{array}{cccccccccc} & \mid & \mid & \mid & \mid & \mid & \mid & \mid & \mid & \mid \\ -10 & -9 & -8 & -7 & -6 & -5 & -4 & -3 & -2 & -1\end{array}$
infut voltage (plotter x input)
c. TYPICAL DYNAMIC ERROR PLOT; + LOG X DFG

FIGURE 2.5-5 LOG $X$ DFG DYNAMIC ERROR TEST CIRCUIT


FIGURE 2.5-6 LOG $X$ ADJUSTMENT LOCATION AND TEST SETUP PATCHING

Table 2.6-2. -Log $X$ Adjustment Data

| -X Input | Adjustment |  | Number |
| :---: | :---: | :---: | :---: |
| Potentiometer | TDVM Readout |  |  |
| -0.32 V | 1 | PC1-R19 | $+2.15 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -1.16 V | 2 | PC1-R5 | $+5.23 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -2.47 V | 3 | PC1-R4 | $+6.92 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -4.28 V | 4 | PC1-R3 | $+8.13 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -6.51 V | 5 | PC1-R2 | $+9.05 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -9.13 V | 6 | PC1-R1 | $+9.79 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |

(4) Static Adjustment Procedures; $1 / 2 \log X$ DFG. The $1 / 2$ Log $X$ DFG is adjusted in a similar manner to the Log X DFG. Using the test setups as shown on Figure 2.5-6 proceed as indicated in Paragraph (3) but use the data of Tables 2.6-3 and 2.6-4.

Table 2.6-3. $+1 / 2$ Log $X$ Adjustment Data

| +X Input | Number $\begin{gathered}\text { Adjustment } \\ \text { Potentiometer }\end{gathered}$ |  | TDVM Readout |
| :---: | :---: | :---: | :---: |
| +0.32V | 1 | PC1-R22 | $-1.08 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| +1.16V | 2 | PC1-R42 | $-2.62 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| +2.47V | 3 | PC1-R4 1 | $-3.46 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| +4.28V | 4 | PC1-R40 | $-4.07 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| +6.51V | 5 | PC1-R39 | $-4.56 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| $+9.13 \mathrm{~V}$ | 6 | PC1-R38 | $-4.90 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |

Table 2.6-4. -1/2 Log $X$ Adjustment Data

| -X Input | NumberAdjustment <br> Potentiometer |  | TDVM Readout |
| :---: | :---: | :---: | :---: |
| -0.32 V | 1 | PC1-R19 | $+1.08 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -1.16 V | 2 | PC1-R5 | $+2.62 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -2.47 V | 3 | PC1-R4 | $+3.46 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -4.28 V | 4 | $\mathrm{PC} 1-\mathrm{R} 3$ | $+4.07 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -6.51 V | 5 | PC1-R2 | $+4.56 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |
| -9.13 V | 6 | PC1-R1 | $+4.90 \mathrm{~V} \pm 0.05 \mathrm{~V}$ |

(5) Applicable Drawings. The following drawings are contained in Volume II of this handbook.

Drawing Number
C016 276 OA

C016 276 OS

C016 281 OA

C016 281 OS

Title
Assembly

Schematic

Assembly

Schematic

## Description

Shows components mounted on module and wiring from block to printed circuit cards.

Schematic Diagram of 16.276 printed circuit cards.

Shows components mounted on module and wiring from block to printed circuit cards.

Schematic diagram of 16.281 printed circuit card.
(6) Parts Lists. Appendix I contains the repiaceable parts lists for both the 16.276 and 16.281 units. See Index of Appendix I.

## 6. VARIABLE DIODE FUNCTION GENERATOR 16.274

The Variable Diode Function Generator (VDFG) permits the operator to generate a function whose complexity makes it extremely difficult, if not impossible, to obtain by other complater components.

The TR-48 VDFG actually consists of two VDFG's: a negative VDFG that responds to inputs between -10 volts and zero, and a positive VDFG that repsonds to inputs between zero and +10 volts. These VDFG's may be used individually (split) or combined to form a $\pm$ VDFG that accepts inputs from -10 to +10 volts.

The VDFG units mount on slide-out shelves behind the control panel (Figure 2.6-1). Thus the units are readily accessible for curve setup. The various input and output leads are cabled from the rear of the VDFG components to specific positions behind the Pre-Patch Panel (Figures 2.6-1 and 1.3-1); by inserting a wired-through chassis in the proper module, the input and output terminations are brought to the Pre-Patch Panel patching block. Figure 2.6-2 shows the various components of the 16.274 VDFG in addition to the slide out chassis shown in Figure 2.6-1.

## a. Operating Considerations

Figure 2.6-3 shows the VDFG patching area and a simplified schematic of the overall unit; the plus and minus VDFG portions show only single diode-gated resistor circuits for clarity. Figure $2.6-4$ shows the patching for the plus and minus VDFG's separately; this figure also contains a simplified schematic of the plus VDFG. The minus VDFG is similar except that the diodes are oriented in the opposite sense and are biased by plus reference.

TR 48 \# 82


COMPONENTS REMOVED TO SHOW SLIDE OUT UNIT
a. VDFG UNIT LOCATION

b. VFDG LOCATIONS AND ASSOCIATED PRE-PATCH PANEL AREAS


FIGURE 2.6-2. VDFG MODULE 16.274 COMPONENTS


FIGURE 2.6-3 VDFG PATCHING BLOCK AND SIMPLIFIED SCHEMATIC


Figure 2.6-5 shows the VDFG patching to combine the plus and minus VDFG's for bipolar inputs. Note that a four-connector bottle plug covers the 10 SEG area of the patching block; one of the +IN terminations is jumpered to a -IN termination to combine the input leads.

Each VDFG unit has eleven adjustments; one is a parallax control and the other ten are slope potentiometers to adjust the output curve slope between unitary incremental inputs of $X$. When used in the $\pm$ VDFG combined mode the parallax pots of the $-V D F G$ and + VDFG are interdependent.

The parallax potentiometer permits the operator to set the value of $Y$ (at $X=0$ ) within the range of +10 to -10 volts. The +1 slope adjustment permits the operator to set the initial line segment slope between 0 and 1 volt so that with 1 volt into the DFG, the $Y$ output can be set to a voltage between $\pm 2$ volts above or below the $X=0$ point (i.e., a slope of 2 volts/volt). The remaining slope potentiometers ( 2 to 10) permit the operator the change the slope of each preceding segment by a voltage slope of one volt per volt.

Figure 2.6-6 is a sample output curve of a plus VDFG. This curve is used as the basis for the typical VDFG set-up procedure.

The following procedure is for the set-up of a +VDFG patched as shown on Figure 2.6-4. The set-up adjustments of the +VDFG must be started at $X=0$ and continued in sequence to $X=+10$. The procedure for the -VDFG is accomplished in a similar manner, again starting at $X=0$ and in sequence $X=-10$.

When setting up a VDFG for combined plus and minus inputs the operator again starts at $X=0$. Once the $X=0$ point is set (parallax potentiometer) the operator must proceed in sequence to either +10 or -10 on one VDFG, then starting again at zero, proceed in sequence to the limit of the remaining VDFG.

## Typical VDFG Set-Up Procedure

(1) Release the quarter-turn locking device and slide the desired +VDFG forward exposing the set-up controls.
(2) Select the $Y=f(X)$ amplifier output (designated 01 on Figure 2.6-4) for readout on the DVM (or multi-range voltmeter if the DVM is not available).
(3) Ground the +IN termination of the VDFG. Using a small-blade screw driver set the PARALLAX control for a DVM readout of -2 volts.
(4) Apply +1 volt to the + IN termination and adjust the +1 control for a DVM readout of -1 .
(5) Apply +2 volts to + IN. Adjust the +2 control for -1 .
(6) Continue the procedure applying $X=+3$, +4 , etc., and adjusting the corresponding control for the proper DVM readout as listed in the table.
(7) For optimum accuracy repeat the set-up procedure, starting with Step (3), and making any necessary touch up adjustments.
b. Theory of Operation

Figure 2.6-4 is a simplified schematic of the +VDFG (portions of the diode networks are eliminated for clarity). The VDFG approximates a desired curve with straight line segments in a manner similar to the fixed diode function generators. As the input level increases, the diodes conduct (or reach their breakpoint) one by one and change the input-to-feedback impedance ratio and thus the amplifier output slope, thus changing the VDFG function to a desired curve. Note, however, that the breakpoint of each diode is fixed and cannot be changed. Only the slope of a line segment (or gain of the amplifier) is variable.

The PARALLAX control (R26, Figure 2.6-4) permits the operator to offset the $X, Y$ point at $X=0$ to any point along the $Y$ axis between -10 and +10 volts. Potentiometer R6 determines the slope between $X=0$ and $X=+1$; this adjustment permits setting the slope to a maximum of 2 volts per volt input either in a positive or negative direction. Potentiometer $R 7$ determines the change in slope between $X=+1$ and $X=+2$ volts with respect to the slope between $X=0$ and $X=+1$ volt. Each potentiometer in turn determines the change in slope of its corresponding line segment over the previous line segment slope.

## c. Maintenance and Test Procedures

There are no calibration adjustments for the VDFG units since the slope potentiometers are set in accordance with the required function. The overall condition of the VDFG's can be determined by the following operational tests. These tests are set up for an oscilloscope display of the VDFG output; an XY plotter may be substituted if desired.
(1) Operational Test: -VDFG
(a) Set up the test circuit shown in Figure 2.6-7a. Set the scope $X$ and X range for 1 volt/centimeter.
(b) Place the computer in Rep-0p at the 20 millisecond rate and adm just the potentiometer input of the integrator for a 0 to -10 volt ramp output per Rep-0p cycle.
(c) With a zero input to the DFG check the PARALLAX control for a full +10 to -10 volt range; set the PARALLAX at $X=0$.
(d) Adjust the $1 V$ control for a slope of zero from $X=0$ to $X=-1$ volt.
(e) Set the $2 \mathrm{~V}, 4 \mathrm{~V}, 6 \mathrm{~V}, 8 \mathrm{~V}$ and 10 V controls fully clockwise.


FIGURE 2.6-5. $\pm$ VDFG PATCHING


FIGURE 2.6-6. SAMPLE +VDFG OUTPUT CURVE

a. OPERATIONAL TEST CIRCUIT

b. SCOPE TRACE, FIRST TEST

c. SCOPE TRACE, SECOND TEST

FIGURE 2.6-7. -VDFG OPERATIONAL TEST SETUP
(£) Set the $3 \mathrm{~V}, 5 \mathrm{~V}, 7 \mathrm{~V}$, and 9 V controls fully counter-clockwise.
(g) Using the test circuit of Figure 2.6-7a and placing the computer in the Rep-Op mode, check the scope for the trace as shown in Figure 2.6-7b.
(h) Apply a fixed -1 volt input to the DFG (PARALLAX control still at zero) and check range of the 1 V adjustment. The output should swing between -2 and +2 volts. Reset the -1 adjustment to zero.
(i) Set the $2 \mathrm{~V}, 4 \mathrm{~V}, 6 \mathrm{~V}, 8 \mathrm{~V}$ and 10 V controls fully counter-clockwise.
(i) Set the $3 \mathrm{~V}, 5 \mathrm{~V}, 7 \mathrm{~V}$ and 9 V controls fully clockwise.
(k) Using the test circuit of Figure $2.6-7 \mathrm{a}$ with the computer in Rep-0p, check the scope for the trace as shown in Figure 2.6-7c.
(2) Operational Test: +VDFG
(a) Set up the test circuit shown in Figure 2.6-8a. Set the scope $X$ and Y range for 1 volt/centimeter.
(b) Repeat steps (b) through (k) of the -VDFG procedure substituting positive potential inputs and observing traces $b$ and $c$ of Figure 2.6-8.
(3) Applicable Drawings. The following diagrams are contained in Volume II of this handbook.

## Drawing Number

CO16 274 OA

C016 156 OS

C016 154 OS

BO45 034 OW

## Type

Assembly

Schematic

Schematic

Wiring

## Description

Shows wiring of module behind Pre-Patch Panel area.

Schematic diagram of +VDFG unit mounted behind controi panel.

Schematic diagram of --VDFG unit mounted behind control panel.

Contains wire run sheets for computer wiring including interconnecting wiring between patchpanel area modules and VDFG connectors behind connectors behind control panel.
(4) Parts Lists. Appendix I contains the replaceable parts lists for the 16.274 VDFG units. See Index of Appendix I.

## 7. COEFFICIENT SETTING ATTENUATOR GROUP 2.440

## a. General

The coefficient setting attenuators in the TR- 48 are mounted on the right-hand panel of the computer cabinet. The panel can accept a total of 60 attenuators, in addition to 5 function switches.

Each 2.440 Attenuator Group consists of five potentiometers and an associated 42.283 Module that plugs into various cradles behind the patch panel. (See Figure 1.3-1.) In addition to providing patching terminations for the five pots, the 42.283 Module contains two relays to enable any pot to be selected for setting and readout.

The potentiometers are 10-turn, wire-wound units, equipped with calibrated, frontpanel dials. The resistance element of each pot is protected by $1 / 32$ ampere fuse in series with the wiper element. The fuse is mounted in a holder on the rear of the pot and can be reached by opening the attenuator panel door.

Four of the five pots in each group have two terminals (wiper and one end of the resistance winding) available at the patch panel. The fifth pot of the group is wired so that the wiper and both ends of the winding are terminated at the patch pansl. See Figure 2.7-1.

## b. Circuit Description

The circuit configuration of the 42.283 Module and the associated pots is shown on Drawing CO42 287 OS. The ungrounded end of each pot is connected to the patch panel through normally closed contacts on K 1 , the Coefficient relay. When the computer is switched to the pot-set mode, K1 is energized, and connects the four grounded pots to the +10 volt reference bus. (Reference must be patched to the ungrounded pot.) Thus, each pot may be set to the required coefficient.

A particular pot is selected for setting and readout by depressing appropriate pushbuttons on the control panel signal SELECTOR. The K2 relays of any consecutive pair of five-pot groups ( $0-9,10-11$, etc.) are energized by depressing first the $P$ button of the SELECTOR hundreds row, and then any one of the top six buttons (0-5) in the tens row. When K2 in each pair of groups is energized, the wipers of all ten pots are comnected to the ten switches (0-9) in the SELECTOR units row. From this point the wiper of one pot may be connected to the DVM (via the selector line) by depressing the appropriate units push-button (0-9).
c. Maintenance
(1) Applicable Drawings. The following diagrams are contained in Volume II of this handbook.

Drawing Number
CO42 283 OS

Type
Schematic

## Description

Schematic diagram of attenuator module.

a. OPERATIONAL TEST CIRCUIT

b. SCOPE TRACE,FIRST TEST

c. SCOPE TRACE, SECOND TEST

FIGURE 2.6-8. +VDFG OPERATIONAL TEST SETUP

b. PATCHING BLOCK

Drawing Number
BO45 034 OW

Type
Wiring

## Description

Contains wire run sheets for computer wiring from Pot Panel to Attenuator module connector plugs behind Pre-Patch Panel.
(2) Parts Lists. Appendix I contains the replaceable parts lists for the 42.283 Attenuator Units. See Index of Appendix I.
8. SIGNAL COMPARATOR 40.404
a. General

The 40.404 Comparator (Figure 2.8-1) consists of a sensitive switching amplifier that drives a double-pole, double-throw relay. This component is generally used to perform automatic switching functions when required in a problem setup. The amplifier compares two inputs and controls the associated relay in accordance with the relative signal level of each input.

The 40.404 Comparator is a dual unit, containing two amplifiers and two relays; the two sections are identical.

## b. Comparator Patching

The patching area for the dual comparator includes two sets of input terminations and four sets of relay contact terminations. Each set of $I N$ and $\mathbb{N N}_{2}$ terminations provides inputs for the potentials to be compared. Usually one of these inputs is a bias voltage against which a particular problem voltage is to be compared.

Each amplifier is arranged such that when the sum of the two input voltages is zero or less (negative), the associated relay is energized and the contacts transfer to the normally open side. If the input sum is positive the relay is de-energized.

To set up a comparator for an accurate switching level, use the following procedure. Connect reference of the appropriate polarity to a coefficient setting attenuator, and connect the attenuator wiper to the input of a gain-of-one amplifier. Patch the amplifier output to the $\mathrm{IN}_{1}$ termination, and set the pot for the desired switching level. Patch the output of the amplifier to the $\mathbb{I N}_{1}$ input. Connect reference voltage (same polarity as above) across anotner attenuator; connect the wiper to the $\mathbb{I N}_{2}$ termination, and then adjust the second attenuator until the really operates. Finally, remove the setup amplifier from the $\mathbb{N N}_{1}$ terminal, and connect this point to the control voltage source in the problem setup.

With the arrangement described, the normally-closed relay contacts will make when the inpat sum is positive, and the relay will transfer to the normally open side when the input sum is negative.

## c. Circuit Description

The comparator amplifier and relay circuitry is shown on Drawings B006 134 OS, and BO40 404 OS. Each input termination is connected through a summing resistor to the base of Q1. As long as the sum of the inputs is positive, Q1 is cat off; Q6 is also cut off and the relay is de-energized.

The conditions in the amplifier at this time are as follows: Q1 is cut off as mentioned above; Q3 is conducting because the base is returned to the -15 volt supply through R3, and the emitter is connected to the +15 volt supply through R9. (Q4 is not conducting, as explained below.) $Q 5$ is cut off by the bias developed across R8. No current flows in the emitter circuit through R10, and Q6 is reversebiased to cut off through R11.

Any drift due to temperature is reduced through the use of Q2 and Q4. Note that an increase in temperature will increase Ico in the input transistor Q1 and a similar increase will occur in Q2. These changes are applied to the base and emitter of Q3 respectively, thus causing the two increases to cancel.

When the sum of the inputs at the base of Q1 is zero or negative, the transistor conducts due to the slight forward bias applied to the emitter through R5. Collector current in R3 biases Q3 to cutoff and, as a result, Q5 is driven into conduction. Since $Q 5$ is connected as an emitter-follower, Q6 also conducts due to the forward bias developed across R11. Relay K1 in the collector circuit is energized and the relay transfers to the - contacts.

When Q1 conducts, the emitter current through R6 develops cut-off bias for the emitter of Q2. As Q2 is turned off, Q4 conducts, drawing current through R9 which applies reverse bias to the emitter of $Q 3$. Thus the emitter receives a negative signal at the same time the positive signal is applied to the base.

Diodes CR1 and CR2 protect the input transistor by limiting the amount of voltage which can be applied across the base-emitter junction. In the output circuit of Q6, diode CR3 protects the transistor against momentary application of a high-forward bias to the collector caused by the collasping field around the relay coil when the circuit is broken.

## d. Maintenance and Test Procedures

(1) Comparator Check. The most important chararteristics of the signal comparator are the switching sensitivity and the switching time. These may be checked readily by using an oscilloscope and the test circuit as shown in Figure 2.8-2. The comparator is driven alternately by positive and negative-going ramp voltages (generated by the integrator). With the arrangement shown, the scope will display a triangular waveform from which the switching time and switching sensitivity may be determined. To perform these checks, proceed as follows:
(a) Patch the circuit shown in Figure 2.8-2; set the scope controls for an internal sweep rate of 2 milliseconds/centimeter and for a sensitivity of 0.1 volts/centimeter.


NOTE
THE 6.134 AND 6.134-I ARE PHYSICALI.Y AND ELECTRICALLY IDENTICAL EXGEPT THE 6.134-I dOES NOT HAVE A PLUG CONNECTOR


FIGURE 2.8-2 SIGNAL COMPARATOR TEST SETUP
(b) Set the function switches as shown; switch the computer first to the reset and then to the operate mode. Adjust the attenuator for- a reading of zero volts on the voltmeter (meter sensitivity should be 0.1 volt.)
(c) The distance between the top and bottom peaks of the triangular wave form represents twice the switch time ( 1 centimeter equals two milliseconds). Typical switching time for a normal comparator is 7 milliseconds.
(d) Move function switch S 2 to ground the 100 ohm resistor. Set the scope sweep for 50 milliseconds/centimeter, and the sensitivity to 0.5 millivolts/centimeter.
(e) The peak-to-peak voltage of the displayed waveform represents the switching sensitivity. Typical values are 2 to 3 milivolts.
(£) The second set of contacts may be checked for switching time by setting S1 to the lower position.
(2) Applicable Drawings. The following drawings are contained in Volume II of this handbook.

| Drawing Number | Type | Description |
| :--- | :--- | :--- |
| C040 404 OA | Assembly | Shows printed circuit card lo- <br> cation on module and wiring to <br> patching block and rear connec- <br> tor of module. |
| B040 404 OS | Schematic | Schematic diagram of relay con- <br> tact connection for TR-48 com- <br> parator. |
| B006 134 OS | Schematic | Schematic diagram of 6.134 Ampli- <br> fier used in 40.404 Comparator <br> Module. |

(3) Parts Lists. Appendix I contains the replaceable parts lists for the 40.404 Comparator Module. See Index of Appendix I。
9. FUNCTION SWITCH GROUP 2.462

A typical TR-48 Computer includes five function switches that are generally used to perform manual switching operations in problem setups.

Each function switch is a double-pole, triple-throw (center off) unit. Associated contacts are jumpered together to increase the current-handing ability; the switch is thus wired as a single-pole, triple-throw unit.

The 2.462 Group consists of the group of five switches, and a 12.766 patch panel module for terminating the switch contacts at the pre-patch panel.

The 12.766 Module may be used in module 5, slot 2, or module 8 , slot 2. (See Figure 1.3-1。) Since these cradles are wired to rearmpanel connectors J62 and J63, respectively, the plug that terminates the function switch wiring must be connected to the rearmpanel connector that is wired to the cradle into which the 12.766 module is mounted. These cradles are all wired in the same fashion.

The replaceable parts for the 2.462 Function Switch Group is contained in Appendix I. See the Index of Appendix I. The following is a list of Applicable Drawings contained in Volume II of this handbook.

## Drawing Number

C012 766 OA

BO45 034 OW

## Type

Assembly

Wiring

## Description

Shows the wiring of the function switch patching module from the patching block to the module rear connector.

Contains wire lists giving the wiring from the function switches on the Pot Panel to the connector at the rear of the Patching Module.

SECTION III
POWER AND REFERENCE CIRCUITS

1. REGULATED POWER SUPPLY 10.200

## a. General

This unit supplies all operational voltages required for the TR-48 components. The power supply is constructed on a small U-shaped chassis (see Figure 3.1-1) that mounts in a cradle behind the attenuator panel in the right-hand bay of the TR-48 cabinet. The mating cabinet connector is designated PS1.

The power supply chassis contains all components except the regulator transistors. These are fastened on a heavy metal heat sink that is mounted behind the component cradles. (See Figure 1.1-2.)

The 10.200 Power Supply operates directly from commercial 50 to 60 cycle power sources; the transformer primary windings are wired for 115 or 230 volts a-c by jumpers on the PS1 connector in the cabinet. The outputs provided by this unit are listed in the following table.

| VOLTAGE | MAX LOAD <br> CURRENT |
| :---: | :---: |
| $+30 \mathrm{~V} \mathrm{d-c*}$ | 0.5 amp |
| $+15 \mathrm{~V} \mathrm{~d}-\mathrm{c}^{*}$ | 1.5 amps |
| $-15 \mathrm{~V} \mathrm{~d}-\mathrm{c}^{*}$ | 2.0 amps |
| $-20 \mathrm{~V} \mathrm{~d}-\mathrm{c}$ | 2.0 amps |
| $-6 \mathrm{~V} \mathrm{d-c}$ | 1.0 amp |
| $6.3 \mathrm{~V} \mathrm{a}-\mathrm{c}$ | 2.5 amps |

*Electronically regulated to $1.0 \%$ of the rated level.

## b. Circuit Description

The circuit configuration of the 10.200 is shown on Drawing C010 200 OS. As this drawing indicates, the unit actually consists of three regulated 15-volt supplies, a 20 -volt filtered supply, an unfiltered 6 -volt supply, and a 6.3 volt a-c source.

The three 15 -volt supplies are all similar in circuit configuration; each consists of a full-wave rectifier, a filter capacitor, a series regulator (externally mounted)
and a regulator amplifier in the form of a plag-in printed circuit card. Each twostage regulator controls the output level of its associated rectifier-filter by amplifiying any deviation from the rated 15 -volt level, and applying the amplified difo ference voitage to the base of the associated series regulator. Thus, by controlling the emitter-tomcollector impedance of the regulating transistor, the output is stabilized at the 15 -volt level as long as the current-handing capability of the regalating transistor is not exceeded.

The three 15 -volt supplies are connected to +15 volt, -15 volt, and +30 volt buses to facilitate distribution of this power to all components. The upper supply on the diagram (CR1-CR2) provides the -15 volt power since its negative terminal is connected to the -15 volt bus and its positive terminal ( $\mathrm{P} 1-3,4$ ) is grounded. The second 15 -volt supply (CR3, CR4) provides the +15 volt power since the negative terminal is grounded and the positive terminal is connected to the +15 volt bus. The +30 volt power is provided by the second and third 15 -volt supplies (CR3-4, and CR5-6, respectively). This is accomplished by connecting the negative side of the third supply ( $\mathrm{P} 1-9,10$ ) to the +15 volt bus and the positive side ( $\mathrm{P} 1-11,12$ ) to the +30 volt bus. This arrangement connects these two sources in series to provide the +30 -volt potential.

## c. Routine Maintenance and Adjustments

Level adjustments for each of the 15 -volt regulated sources are provided in the form of panel mounted screw driver set potentiometers. The voltage levels should be checked occasionally, using the front panel voltmeter. If the supplies require adjustment, the +15 volt level should be set before adjusting the 30 -volt outpat. This is necessary since the 30 -volt supply is comprised of two seriesmonnected 15 -volt supplies.

Preventive maintenance of the 10.200 should consist of an occasional check of the ability of each source to maintain regulation under maximum load conditions. This can be accomplished by connecting appropriate values of load resistances across each supply to determine that the supply maintains regulation up to the maximum load current indicated in the table in sub-paragraph a.

It should be noted that regulated supplies of this type are relatively insensitive to any gradual deterioration that may occur in component characteristics, and will often continue to operate satisfactorily if such deterioration occurs. Usually a power supply malfunction results in complete loss of regulation; this is evidenced by overload indications in all amplifiers. In nearly all cases of regulation failare, the trouble can be cured by transistor replacement.
2. TDVM POWER SUPPLY 10.203

## a. General

The 10.203 Power Supply (Figure 3.2-1) provides d-c operating potentials of -8 volts and +2 volts for the TR-48 Digital Voltmeter. This power supply plugs into a cradle behind the attenuator panel in the right-hand bay of the computer. The mating cabinet connector is designated PSZ。



FIGURE 3.2-1. REGULATED POWER SUPPLY 10.203

The 10.203 supply operates directly from commercial 50 to 60 cycle power sources; the transformer primary windings are wired for 115 or 230 volts a-c by jumpers on the PS2 connector in the cabinet. The outputs provided by this unit are listed in the following table.

*Electronically Regulated

## b. Circuit Description

The circuitry of the 10.203 Power Supply is shown on Drawing B010 203 OS. This simple unit consists of two full-wave rectifier and filter circuits supplying the 8-volt and +2 volt d-c potentials. Transistor Q1 functions as a series regulator to regulate the +2 volt output. Zener diode CR5 stabilizes the base of Q1.

The transformer includes an additional 6.3 volt winding to supply a-c power to the oven heater of the comparator in the digital voltmeter.
3. REFERENCE REGULATOR 43.104
a. General

The TR-48 uses a system reference level of $\pm 10$ volts for computational purposes. These potentials are generated by the 43.104 Reference Regulator, (Figure 3.3-1) and a 6.282 Dual D.C. Amplifier; both of these components are located in cradles behind the attenuator panel in the right-hand bay of the TR-48 cabinet. The mating cabinet connectors for the amplifier and regulator are designated P68 and P69 respectively.

The reference regulator includes a temperature-stabilized zener diode which functions as an internal reference standard. Under normal operating conditions, the regulator-amplifier combination generates $\pm 10$ volt potentials that are maintained to within $0.02 \%$ of 10 volts , and that are stable up to the maximum output of 250 milliamperes for each reference source.

Provision is made for using an external 10-volt reference source. The external reference line is terminated at Pin T of J69; by connecting the external reference source to this point and changing one patch cord (see sub-paragraph b), the computer reference circuits can be slaved to an external voltage standard.

## b. Reference Patching

To connect the TR-48 reference circuits for internal reference, a patch cord is required between the REF IN and INT REF terminations on the reference regulator front panel. If an external 10-volt standard is to be used, the REF IN termination should be patched to EXT REF. To connect the amplifier to the regulator, each of the $S$ terminations on the regulator must be patched to a corresponding $\underline{S}$ termination on the 6.282 Dual D.C. Amplifier.

## c. Circuit Description

The configuration of the TR-48 reference circuits is shown in Figure 3.3-2. (For detailed circuitry of the amplifier and regulator see Drawings D006 282 OS and C043 104 OS respectively.)

The $\pm 10$ volt reference potentials are generated by using a zener diode as a voltage standard, and applying the zener-stabilized potential to a pair of cascaded d-c amplifiers with sufficient gain to develop the required reference levels. As shown in Figure 3.3-2, CR1 (the zener diode) and R10 are connected across the -15 volt supply to provide a stable source of approximately -6 volts. Resistors R7, R8, and R9 form the amplifier input resistor; R5 is connected as a 10,000 ohm feedback resistor across the amplifier. The input resistance value is selected and set at the time of manufacture so that the amplifier output is exactly 10 volts. To permit the reference source to deliver more load current than the amplifier itself is capasble of delivering, an emitter-follower power stage (transistor Q4, mounted on the heat sink bracket), is driven by the amplifier. With this arrangement, the maximum load current capability of the source is increased to about 250 milliamperes.

The negative reference source consists of a similar arrangement. In this case the closed-loop gain of the amplifier is unity, thus multiplying the +10 volt level by a factor of -1 to develop the -10 volt potential. Potentiometer $R 1$ permits a small gain adjustment (BAL ADJ) so that the pius and minus 10 volt levels may be precisely balanced with respect to each other.

To protect the reference circuits from overload damage, a bank of incandescent lamps is connected into the emitter circuit of each power amplifier. These lamps permit the amplifiers to function normally when delivering load currents of up to about 250 milliamperes. If a reference source is loaded beyond this point, the circuit loses regulation, the output level drops accordingly, and no damage can occur to the reference supply components.
d. Routine Maintenance and Adjustment

Prior to shipment, each reference regulator is adjusted to yield +10 volts $\pm 0.02 \%$; the negative source is balanced against this standard. These reference levels may be checked and re-adjusted at any time, if sufficiently accurate equipment is available. If not, EAI recommends that the regulator be returned to the factory should component replacement or adjustment become necessary.


FIGURE 3.3-1. REFERENCE REGULATOR 43.104


NOTE
I. VALUE OF R7 DETERMINED AT TIME OF MANUFACTURE
2. Q4 AND Q5 ARE LOCATED ON HEAT SINK BEHIND COMPONENT CRADLES
3. * DENOTES AMPLIFIER CONNECTOR
4. DENOTES PATCH CORD OR BOTTLE FIGURE 3.3-2 TR-48 REFERENCE CIRCUITS, SIMPLIFIED SCHEMATIC

When required, the balance control (BAL $A D J$ ) on the reference regulator may be adjusted to within $0.01 \%$ by using measuring circuits provided by the TR-48 itself. To set this control, use two gain-of -10 summing amplifier inputs; patch plus reference to one input and minus reference to the other. Observe the amplifier output a with the control panel voltmeter on the 0.1 volt scale. Set the BAL ADJ control for a zero reading. Reverse the input polarities and again observe the amplifier output. If a voltage is indicated, set the BAL ADJ control for the mean of the difference. Continue this process until the same voltage (in both polarities) is obtained when switching the reference inputs.

Each amplifier in the 6.282 should be checked occasionally for balance. This is readily accomplished by setting the control panel VOLTMETER FUNCTION switch to the BAL position, and selecting the desired amplifier with the control panel SELECTOR. (The plus reference amplifier is No. 48, and the minus is No. 49.) The associated AMP BAL control should be set for a zero reading.
4. DUAL D.C. AMPLIFIER 6.282
a. Genera?

As previously indicated this unit contains the two operational amplifiers used with the 43.104 Reference Regulator to generate the plus and minus 10 volt reference potentials.

The 6.282 amplifier circuitry is identical with that of the 6.514 Dual D.C. Amplifier described in SECTION 2-1 of this manual. Refer to that section for all details regarding circuit description and maintenance techniques for the 6.282 Amplifier.

CONTROL AND MONITORING CIRCUITS

1. CONTROL PANEL 20.790 (See Figures 1.3-1 and 1.6-1.)

## a. General

The control and monitoring facilities for the TR-48 are consolidated at the 20.790 Control Panel, which forms the left side of the computer front panel. The monitorm ing circuits of the TR-48 include a multi-range voltmeter with associated RANGE and FUNCIION selector switches, an electronic digital voltmeter*, a push-button select readout system, and a set of amplifier overload lamps.

The control facilities on this panel include power on/off, pre-patch panel engage and disengage, and a push-button switch for controlling the computer mode of operation.

## b. Monitoring Circuitry

The TR-48 monitoring circuits are shown in block diagram form in Figure 4.1-1. The four main components of this system are the 3 -level pushmbutton signal SELECTOR system, the selector relays (mounted on the 11.148 Relay Unit), the digital voltmeter, and the multi-range voltmeter with associated RANGE and FUNCIION selectors.

In the standard TR-48, the readout system is wired to scan 175 points in the computer. (The maximum capacity of the system is 230 points; thus, some computers may be wired to read out additional points.) These 175 circuits inslude 50 amplifier output terminals, 50 amplifier stabilizer outputs (for balancing purposes), the wiper of each of the 60 coefficient setting attenuators, and fifteen of the leads connected to J64 (IN TRUNK connector on the rear of the TR-48 cabinet).

As the block diagram shows, the amplifier outputs, the stabilizer lines and the J64 leads are connected to contacts of the selector relays. (See Sheet 2 of Drawing D045 034 OS.) The coils of these relays are controlled by the kundreds (in position A) and tens push-buttons of the signal SELECTOR (shown in the center of Figure 4.1-1).

The switching action of the relays connects selected groups of the monitored points to contacts on the units push-buttons. By depressing one of these buttons, the
*Computers not equipped with a digital voltmeter have a 10-turn potentiometer and associated reference voltage selector switch for measuring computing voltage levels. These components are mounted on the 20.790 Control Panel in place of the digital voltmeter readout unit.
selected point is connected to the selector line, which is terminated at Pin 5 of switch S8c. (See Sheet 3 of D045 034 OS。)

The coefficient setting attenuators are selected for readout by a similar process. Operating the $\mathcal{P}$ pushobutton (hundreds row) and then one of the tens buttons will energize the output relay of each Attenuator Group in a pair of groups (see Sheet 1 of 0045034 OS and CO42 283 OS). This switching action connects the wipers of the ten selected attenuators to the contacts of the units level of the signal SELECTOR; thus, one of these ten attenuators may be selected by operating the appropriate pushobutton in the units level.

As previously indicated, the output of the signal SELECTOR is connected to pin 5 of switch S8c. This control is the PS (pot set) pushobutton of the computer MODE control. (See Paragraph 5 of SECIION I, and submparagraph \& below for details of computer operational modes.) With the computer switched to any mode other than pot set, the selector output line is connected to the SEL terminations of the patch panel readout module. Terminations for the inputs to the DVM and the multi-range voltmeter are adjacent to the SEL terminations, so that bottle plugs may be used to connect either or both of these instruments to the selector line. It should be noted, however, that the voltmeter circuit is a relatively heavy load and should never be used to monitor circuits that cannot tolerate loading; for this reas on the selector line is routed through the PS switch. Thus, when the computer is in the PS mode, the selector line is connected directly to the DVM input and will not be affected by voltmeter loading even if the SEL and VM terminations are patched together.

Amplifiers are selected for balance monitoring in the same fashion as for output monitoring. The only difference is that the stabilizer of the selected amplifier is connected to the balance monitoring line, rather than the selector line. The balance monitoring line is connected to the meter through the VOLTMETER RANGE and FUNCTION switches.

## £. Computer Mode Control

The operational modes of the $T R-48$ are controlled by a 6 -position push-button MODE switch on the 20.790 Control Panel. Operating these buttons performs various switching functions depending on the mode selected. The main function is to drive switching transistors which energize or de-energize certain control buses; actual component switching is accomplished by relays which are connected to these buses. (The switching transistors are Q1, Q2, and Q3, mounted on the heat sink bracket on the back of the computer.)

Detailed operational descriptions of mode control appear in the TR-48 Operator ${ }^{9}$ s Manual. This paragraph is intended only as an electrical description of the mode circuits to show how the control buses are energized.

The mode control circuits are shown on Sheet 2 of Drawing D045 034 OS. S8 is the MODE selector; this switch is constructed so that only one button can be down at any time. A lamp inside each button indicates the selected mode.

The switching functions performed in each mode are summarized in the following table.


FIGURE 4.I-I.
TR-48 MONITORING

|  | CIRCUIT |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | OPERATE BUS | RESET BUS | TIME SCALE BUS | $\begin{aligned} & \text { SW. REL BUS } \\ & \text { (AMPL. P.S. RE- } \\ & \text { LAYS) } \end{aligned}$ | DVM INPUI LINE | SIGNAL SELECTOR |
| HOLD (HD) | De-energized | De-energized | De-energized | De-energized | Connected to Patch Panel. (DVM Terminal on Readout Module.) | Connected to Patch Panel. (SEL Terminal on Readout Module.) |
| POTSET (PS) | De-energized | De-energized | De-energized | $\begin{aligned} & \text { Energized } \\ & (-20 \text { volts }) \end{aligned}$ | Connected directly to selector line. (Disconnected from Patch Panel.) | Connected to DVM Input. (Disconnected from Patch Panel.) |
| RESET (RS) | Demenergized | $\begin{aligned} & \text { Energized } \\ & (-20 \text { volts }) \end{aligned}$ | De-energized | De-energized | Same as HOLD | Same as HOLD |
| $\begin{gathered} \text { OPERATE } \\ (\mathrm{OP}) \end{gathered}$ | Energized (-20 volts) | De-energized | De-energized | De-energized | Same as HOLD | Same as HOLD |
| SLAVE (SL) | Disconnected trol. Contro ternal source through slave | rom Mode Conled from ex(master TR-48) table. | De-energized | De-energized | Same as HOLD | Same as HOLD |
| REPET IT IVE <br> OPER. (RO) | Connected to by Rep Op Tin | and controlled ng Unit | $\begin{aligned} & \text { Energized } \\ & (-20 \text { volts }) \end{aligned}$ | De-energized | Same as HOLD | Same as HOLD |

## 2. DIGITAL VOITMETER 26.183

The 26.183 DVM provides accurate and rapid measurements of $d-c$ voltages. When mounted in the TR-48, the DVM main chassis is housed in a cradle behind the control panel, and the four-place display unit is mounted on the front of the control panel. The main chassis connector designated $D V-P 1$ mates with $D V-J 1$ in the $D V M$ cradle; DV-J2, and $D V-J 3$ serve to connect the DVM display unit to the main chassis.

## 3. REPET IT IVE OPERAT ION

a. General

Repetitive operation of an analog computer consists of forcing the computer to speed up the time of probiem solution, and to continually repeat the problem solution. The rate at which this occurs is usually high enough to permit displaying computing voltages on a conventional oscilloscope.

In the $T R-48$ the repetitive operation feature is provided by a Model 36.082 Timing Unit (Figure 4.3-1) and a REP OP Control Module on the 20.790 Control Panel. (See Figure $1.6-1$.) These circuits permit the computer to be switched rapidly (at a selectable rate) between the operate and reset modes of operation.

The timing unit is mounted in a cradle behind the attenuator panel and mates with J67 in the cabinet. The control module connects to CPoJ11.
b. Repetitive Operation Mode

The computer is prepared for repetitive operation by depressing the RO button of the MODE control. This switching action connects operating potentials ( $\pm 15$ volts and -20 volts) to the timing unit circuits, connects the reset and operate buses to the reset and operate control lines in the timing unit, and also energizes the time scale bus. Under these conditions, the computer time scale is changed to permit high-speed runs (in faster than real time), and switching between the reset and operate modes is controlled automatically by the timing unit.

Refer to the $T R-48$ Operator ${ }^{1}$ s Manual for operation of the Rep Op system.

## c. Timing Unit and Rep Op Control Module

These components are shown schematically on Drawings C036 082 OS and BOO2 435 OS. The function of the timing unit is to provide control voltages to energize the reset and operate buses, and to supply sweep voltages for the display oscilloscope. The control module consists of a 4 -position COMPUTE TIME switch and a VERNJER potentiometer. These components permit selection of the repetitive operation rate by controlling the operation of the Q1-T1 blocking oscillator in the timing unit. (See Drawing C036 082 OS.) The blocking oscillator drives Q2, which supplies the oscilloscope sweep voltage. (Pin L of the timing unit connector is wired to the terminal adjacent to the pulse symbol on the Patch Panel Readout Module。)


FIGURE 4.3-1. REP-OP TIMING UNIT, MODEL 36.082

The blocking oscillator also triggers a monostable multivibrator (Q3, Q4) which controls the repetitive operation reset timing. The multivibrator output is taken from Q5 (an isolating stage) and drives the 4-stage switching amplifier consisting of Q8, Q9, Q10, and Q11. The circuitry is arranged such that the sharp negative-going pulse appearing at pin 4 of T1 triggers the multivibrator. The resultant switching action drives the reset bus (connected to pin Y) to -20 volts while the multivibrator is cycling. When the multivibrator switching cycle is completed, the reset bus potential drops back to zero and the operate bus is energized. ( -20 volts). This action continues at the rate selected by the COMPUIE TIME control. Adjustment of the multivibrator rate is provided by R9 in the base circuit of Q4.

The isolated output of the multivibrator is also brought ourt to the front panel of the timing unit to provide an oscilloscope sync signal for adjusting the repetitive operation timing circuits. Refer to sub-paragraph d below for complete details.

## d. Repetitive Operation Timing Adjustments

Five screwdriver adjust potentiometers are included in the timing circuits to permit calibration of repetitive operation timing. These controls consist of R1, R2, R3, and R4, mounted on the rear of the REP OP COMPUE TIME switch, and R9 on the timing unit card. The COMPUXE TIME pots control operate timing, and the timing unit pot permits adjustment of reset time. To check and adjust these controls proceed as follows:
(1) Prepare the computer for operation; remove the timing unit from its cradle and mount it on the test shelf.
(2) Patch a real time integrator and connect it to the repetitive operation display scope as shown in Figure 4.3-2.
(3) Set the COMPUE TIME switch to the 20 millisecond position; rotate the VERNIER control fully counter-clockwise.
(4) Set the oscilloscope controls for a 5 millisecond/centimeter sweep, and for external sync (adjust as necessary).
(5) Switch the computer to the repetitive operation mode. Set the integrator input voltage as high as possible without amplifier overioad, then adjust the vertical sensitivity of the scope for sufficient deflection to observe the waveform shown in Figure 4.3-2.
(6) If the displayed waveform is not as shown, adjust R9 on the timing unit until the reset time is $1 C$ nilliseconds ( $\pm 5 \%$ )。
(7) To set the operate time, adjust R1 on the COMPUTE TIME switch assembly (behind the attenuator panel) for an operate time of 20 milliseconds.
(8) Repeat step (7) for each of the remaining ranges; re-adjust the scope controls accordingly. In each case adjust the appropriate potentiometer for the operate time ( $\pm 5 \%$ ) as selected by the switch.
4. patch panel readour module fror 763 Pevieión /2 763

The 12.762 Module provides a consolidated patch panel area in which all TR-48 monitoring circuits (inciuding external equipment cabled to the computer) are terminated. The readout module is normally positioned in module 2, slot 2 (J7) of the computer cabinet, as shown in Figure 1.3-1.

Internal monitoring facilities terminated at the readout module include the signal selector output line and the digital voltmeter and multimange voltmeter input terminals. External circuits terminated at the readout module include $X$ and $Y$ inputs to an oscilloscope connected to J66 on the rear of the TR-48 cabinet, two sets (X and Y) of plotter/recorder inputs connected to J65, and ten trunk lines that enter the TR-48 at J61. (See Figure 1.3-1 and Paragraph 1-5 for details on the external connector moduie.)

Figure $404^{-1}$ is a schematic diagram showing the function and origin of all terminations brought out to the readout module.

A. TIMING ADJUSTMENT TEST SETUP

B. DESIRED WAVEFORM

(SEE FIG. 4.1-2)

FROM
SWEEP OUTPUT OF TIMING UNIT
 EXTERNAL PLOTTER/ RECORDER CONNECTOR Drignan. $B 019.323 .04$
 EXTERNAL TRUNK CONNECTOR

FIGURE 4.4-1. PATCH PANEL READOUT MODULE WIRING
For wiring Drawing. See B045 034 ow whet 14

## APPENDIX I

## REPLACEABLE PARTS LIST

This appendix lists all replaceable parts in the TR-48 Analog Computer, Model 45.034. In each case a brief description of the part and a manufacturer's number are listed. Where applicable, a reference symbol (schematic designation) is included. To enable a particular sheet to be readily located, an index precedes the individual spare parts lists.

The category column in the parts list indicates the availability of each listed part so that a replacement part can be obtained as quickly as possible. The components in category $A$ are standard electronic items that are usually available from any commercial electronic supplier. In order to expedite obtaining items of this nature, it is suggested that they be purchased from a local source whenever possible. If necessary, these parts may be ordered from EAI.

The components in category $B$ are items that can be obtained from EAI or any of the listed manufacturers. However, in most cases EAI is in a position to offer the most rapid service on items in this category.

The parts in category $C$ are custom-made components and proprietary items that are available only from EAI. When ordering items of this type, please specify the type number and serial number of the basic unit in which the part is located, as well as the part identification.

Where possible, sufficient information is given for category $C$ items to permit an electrically-similar replacement part to be obtained locally. Thus, if desired, a temporary repair may be made while the exact replacement is being obtained from EAI. Note, however, that EAI does not guarantee that the affected unit will operate within specifications when the specified category $C$ part is not used.

PLEASE NOTE THAT EAI RESERVES THE RIGHT TO MAKE PART SUBSTITUTIONS WHEN REQUIRED. IN ALL CASES, EAI GUARANTEES THAT THESE SUBSTIIUIIONS ARE ELECTRICALLY AND PHYSICALLY COMPATIBLE WITH THE ORIGINAL COMPONENTS.

## PARTS LIST INDEX

TR-48 ANALOG COMPUTER, MODEL 45.034


## PARTS LIST INDEX (Cont)

|  | Model Number | Component | Page |
| :---: | :---: | :---: | :---: |
| 2. | 2.424 | Repetitive Operation Module (Continued) |  |
|  | g. 20.534 | Repetitive Operation Switch Unit | AI-4 |
|  | b. 36.082 | Timing Unit | AI-5 |
| 3.4. | 6.282 | Dual DC Amplifier | AI-7 |
|  | 6.514 | Dual DC Amplifier |  |
|  | 2. 6.282 | Dual DC Amplifier Card | AI-7 |
|  | b. 12.730 | Resistor Network Card | AI-10 |
| 5. | 7.099 |  | AI-11 |
|  | 8. 7.044 |  | AI-11 |
|  | $\frac{\text { g. }}{\text { b. }} 7.044-1$ |  |  |
| 6. | 10.200 | Regulated Power Supply ............................. | AI-13 |
|  | 3. 43.107 | Power Supply Regulator Card ....................... | AI-14 |
| 7. | 10.203 | Power Supply ..........................................0. | AI-15 |
| 8. | 12.764 | Integrator Network | AI-16 |
| 9. | 16.274 | Variable Diode Function Generator <br> -Variable DFG Card ......................................... <br> +Variable DFG (Parts and symbols identical <br> with 16.159-1) ........... | AI-17 |
|  | … $16.154-1$ |  | AI-18 |
|  | b. 16.156-1 |  |  |
| 10. | 16.275 |  | AI-20 |
|  | a. 16.099 | $\mathrm{X}^{2}$ DFG Card | AI-20 |
| 11. | 16.276 | Log $X$ DFG $\qquad$ <br>  <br> Log $X$ DFG (Parts and symbols identical <br> with 16.127)........................... | AI-22 |
|  | … 16.127 |  | AI-22 |
|  | b. 16.127-1 |  |  |
| 12. | 16.281 | $\begin{array}{r} 1 / 2 \log X \text { DFG } \\ 1 / 2 \log X \text { DFG Card } \\ 1 / 2 \log X \quad \text { DFG (Parts and symbols identical } \\ \text { with } 16.134 \text { ) } \end{array}$ | AI-24 |
|  | 3. 16.134 |  | AI-24 |
|  | b. $16.134-1$ |  |  |
| 13. | 20.790 | Control Panel ............0.......................... | AI-26 |
|  | 층 20.753 | Overload Indicator | AI-28 |
|  | b. 20.791 | Overload Indicator | AI-29 |
| 14. | 20.825 | Null Control Panel | AI-30 |
| 15. | 26.183* | TR-48 TDVM |  |
| 16. | 26.195 | Display Unit | AI-31 |
| 17. | 40.404 | Comparator | AI-32 |
| 18. | 42.283 | Attenuator | AI-33 |
| 19. | 42.287 | Attenuators/Function Switch Panel | AI-34 |
| 20. | 43.104 | Reference Regulator | AI-35 |

[^2]

| ITEM | REF. DESIG. | DESCRIPTION | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | R1 | Resistor, Variable, Composition: 20 K ohms $\pm 20 \%$, . 2 W ; Bourns Laboratories 276-1-203 | 6424710 | B |
| 2 | R2 | Resistor, Variable, Composition: 50K ohms $\pm 20 \%$, .2 W ; Bourns Laboratories 276-1-503 | 6424720 | B |
| 3 | R3 | Resistor, Variable, Composition: 100K ohms $\pm 20 \%$, $.2 W$; Bourns Laboratories 276-1-104 | 6424820 | B |
| 4 | R4 | Resistor, Variable, Composition: 200 K ohms $\pm 20 \%$, .2 W ; Bourns Laboratories 276-1-204 | 6424900 | B |
| 5 | R5 | ```Resistor, Fixed, Wirewound, Precision: 2900 ohms \pm1%, .005% Stability; National Resis- tor Corp. EU-2 Type``` | A638 4390 | C |
| 6 | R6 | Resistor, Variable, Composition: 7.5 K ohms $\pm 20 \%$, 1 W ; Reon Resistor Corp. RA75221R2X | A642 4860 | C |
| 7 | R7 | Resistor, Fixed, Composition: 4.7 K ohms $\pm 10 \%$ 1W; Allen-Bradley GB | 6274721 | A |
| 8 | S6 | Switch, Rotary: 2 Sections, 6 Positions; Centralab PA037-085 | B658 1800 | C |


| ITEM | REF. desig. | DESCRIPTION | eal no. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | C1 | ```Capacitor, Fixed, Plastic: 10 UF +C%-5%, 50V``` | B 5210770 | C |
| 2 | C2 | Capacitor, Fixed, Ceramic: 1,000 PF GMF; 600V; Cornell-Dublier BYA6D1 | 5150050 | C |
| 3 | C3 | Capacitor, Fixed, Paper: . $05 \mathrm{UF} \pm 20 \%$, 200V; Aerovox P8292ZN, | 5202100 | A |
| 4 | C4 | Capacitor, Fixed, Electrolytic: 50 UF $+100 \%-10 \%$, 25V; Callins Industries PSS Type | A516 1980 | C |
| 5 | C5 | Capacitor, Fixed, Electrolytic: 100 UT $+150 \%-10,0,25 \mathrm{~V}$; P.R. Nallory Pet-A Type | 1516 1910 | C |
| 6 | CR1-6 | Diode, Germanium: Clevite CTP 462 Type | 6140430 | B |
| 7 | CR7, E | Rectifier, Silicon: Pacific Semiconductors PSCC5 Type | 6140350 | B |
| $\varepsilon$ | Q1-7 | Transistor, Germanium: PNF; Industro | B686 0320 | C |
| 9 | QE, 10 | ```Transistor, Germanium: PNP; General Electric 2N321 Type``` | 6860040 | A |
| 10 | Q9,11 | Transistor, Germanium: PNF; Tung-Sol 2 N 242 Type | 6860180 | A |
| 11 | R1,2 | Kesistor, Fixed, Composition: 47K Ohms $\pm 10 \%, 1 / 2 N ;$ Allen-Bradley EB | 6264731 | A |
| 12 | R3 | Resistor, Fixed, Composition: 18K Ohms $\pm 10 \%, 1 / 2 \mathrm{~W}$; Allen-Bradley EB | 6261831 | a |
| 13 | R4 | Resistor, Fixed, Composition: 2.2 K Ohms $\pm 10 \%, 1 / 2 N$; Allen-Bracley EB | 6262221 | A |
| 14 | R5,13,16 | Resistor, Fixed, Composition: 10K Ohms $\pm 10 \%, 1 / 2 N$; Allen-Bradley EB | 6261031 | A |
| 15 | R6,14 | Resistor, Fixed, Composition: 15K Ohms $\pm 10 \%, 1 / 2 N$; Allen-Eradley EB | 6261531 | 1 |
| 16 | ${ }_{20}^{\mathrm{R} 7,1 \varepsilon, 10},$ | Resistor, Fixed, Composition: 1K Ohms $\pm 10 \%, 1 / 2 N$; Allen-Bradley EB | 6261021 | A |
| 17 | R8 | Resistor, Fixed, Composition: 220 K Ohms $\pm 10 \%, 1 / 2 N ;$ Allen-Bradley ED | 6262241 | A |
|  |  |  | UNIT titletriang unit |  |
|  |  |  | MODEL NO. 36.082 | of 2 |







| ITEM | Ref. desig. | description | eal no. | *Cat. |
| :---: | :---: | :---: | :---: | :---: |
| 2 | $\begin{aligned} & \mathrm{CR} 1,2 \\ & \mathrm{R} 1-4 \end{aligned}$ | Diode, Silicon: Hughes Semiconductors $1 \mathbb{N} 45$ Resistor, Fixed, Wirewound, Precision: 3550 Ohins $\pm .05 \%$, $005 \%$ Stability | B614 0070 $B 6387640$ | c |
| 1 | CR1-14 | 2.044 (1/4) ${ }^{2}$ MUTITRLIER <br> Diode, Silicon: General Instrument DR837 <br> Resistor, Variable, Composition: 15K Ohms $\pm 30 \%$, Chicago Telephone Supply UPE-70 Type | $\begin{aligned} & A 6140420 \\ & A 6424570 \end{aligned}$ | B |
| 3 | R2,3,8,9 | Resistor, Variable, Composition: 2.5K Uhms $\pm 30 \%$; Chicago Telephone Supply UPE-70 Type | A642 4450 | c |
| 4 | $\begin{aligned} & \mathrm{R} 4,5,6,10, \\ & 11,12 \end{aligned}$ | Resistor, Variable, Composition: 1K Ohms $\pm 30 \%$; Chicago Telephone Supply UPE-70 Type | A642 4440 | c |
| 5 | R13,39 | Resistor, Fixed, Composition: 300 Uhms $\pm 5 \%, 1 / 2 \mathrm{w}$; Allen-Bradley EB | 6263010 | A |
| 6 | R14,40 | Thermistor: 88 Ohms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$; Keystone Carbon Co. L3006-88-77-S11 | A646 0040 | B |
| 7 | R15,41 | Resistor, Fixed, Composition: 12K Ohms $1 / 2 \mathrm{~W}$; Allen-Bradley EB | 6261231 | A |
| 8 | R16,42 | Thermistor: 550 Ohms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$; Keystone Carbon Co. L2006-550-92-S10 | A646 0030 | B |
| 9 | R17,43 | Resistor, Fixed, Composition: 820K Ohms $\pm 10 \%, 1 / 2 w ;$ Allen-Bradley EB | 6268241 | A |
| 10 | H18,44 | Resistor, Fixed, Wirewound, Precision: 14,800 Uhms $\pm 1 \%$, .01\% Stability; Resistance Products Co PB Type | A638 2820 | c |
| 11 | R19,45 | Kesistor, Fixed, Wirewound, Precision: 18,000 Ohns $\pm 1 \%, .01 \%$ Stability; Resistance Products Co PB Type | A638 2830 | C |
| 12 | R20,46 | Resistor, Fixed, Wirewound, Precision: 22,400 Uhms $\pm 1 \%$, .01\% Stability; Resistance Products Co PB Type | 186382840 | c |
|  |  |  | UNIT TITLE $(1 / 4)^{2}$ MULT IPLIER |  |
|  |  |  | Sh 1 of 2 |  |


| ITEM | REF．DESIG． | DESCRIPTION | EAI NO． | ＊CAT． |
| :---: | :---: | :---: | :---: | :---: |
| 13 | K21，47 | Resistor，Fixed，Wirewound，Precision： 29，600．Uhms $\pm 1 \%$ ，． $01 \%$ Stability； Resistance Products Co PB Type | A638 2850 | C |
| 14 | R22，48 | Kesistor，Fixed，Wirewound，Precision： 43，300 Ohms $\pm 1 \%, .01 \%$ Stability； Resistance Products Co PB Type | A638 5250 | C |
| 15 | R23，49 | Hesistor，Fixed，Wirewound，Precision： 82,000 Uhms $\pm 1 \%$ ，．01\％Stabi」ity； Resistance Products Co PB Type | 46385410 | C |
| 16 | R24，50 | Thermistor： 300 K Ohms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$ ； Keystone Carbon Co．L1215－300K－152－\＄12 | A646 0020 | B |
| 17 | $\begin{aligned} & k 25-36, \\ & 51-62 \end{aligned}$ | Resistor，Fixed，Wirewound，Precision： 25，000 Uhms $\pm 1 \%$ ，．01\％Stabi」ity； Resistance Products Co PB Type | A638 3050 | C |
| 18 | $\begin{aligned} & R 37,38,63, \\ & 64 \end{aligned}$ | Resistor，Fixed，Wirewound，Precision： 27,000 Uhms $\pm 1 \%, .01 \%$ Stabi」ity； Resistance Products Co PB Iype | 46383060 | C |


| ITEM | REF. DESIG. | DESCRIPTION | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | C1, 2, 4 | Capacitor, Fixed, Electrolytic: 2500 UF, 25V; P.K. Mallory 20-20979 | 5160520 | $B$ |
| 2 | C3 | Capacitor, Fixed, Electrolytic: 4500 UF, 25V; P.R. Mallory SPU-20-6312 | 5162450 | C |
| 3 | CR1-4 | Rectifier, Silicon: General Eıectric 1N1342A | 6141240 | B |
| 4 | CK5-12 | Rectifier, Silicon: Solitron Devices, Inc. CER-680 | 6141100 | B |
| 5 | F1,4 | Fuse, Cartridge, Fast Acting, Visual Indicating Type: 2 Amps, 125V; Bussman GMw2 | 5701380 | A |
| 6 | F2 | Fuse, Cartridge, Fast Acting, Visual Indicatin Type: 1-1/2 Amps, 125V; Bussman GMw 1-1/2 | 5701370 | A |
| 7 | F 3 | Fuse, Cartridge, Fast Acting, Visual Indicating Type: $1 / 2 \mathrm{Amp}, 125 \mathrm{~V}$; Bussman Graw $1 / 2$ | 5701350 | A |
| 8 | 71 | Transformer, Power: 2ea 105/115/125V 50/60 CPS Primaries, lea 33VCT 3ea 32 VCT and lea 6.3V Secondaries; James Electronics A7271 | 06841730 | C |




| ITEM | REF. DESIG. | DESCRIPTION | Eal No. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | C1 | Capacitor, Fixed, Pıastic: 1 UF $\pm .05 \%$, 25V | 521.137 | C |
| 2 | C2 | Capacitor, Fixed (Adjustable), Plastic: . 002 UF $\pm .1 \%$ Adjustable Range | 524.011 | C |
| 3 | C3 | Capacitor, Fixed, Plastic: 9 UF $\pm .05 \%$, 25V | 521.138 | C |
| 4 | C4 | Capacitor, Fixed (Adjustable), Plastic: . 018 UF $\pm .1 \%$ Adjustable Range | 524.012 | C |
| 5 | CR1,2,3 | Diode, Germanium: Clevite CTP462 | 6140430 | B |
| 6 | K1 | Relay: 18V DC Coil, 4 Form C Contacts; Aliied Controls T-154-4C-520 | 6181710 | B |
| 7 | K2 | Relay: 12.6V DC Coil, 2 Form C Contacts; <br> C.P. Clare RP7641-G40 | 6180970 | B |
| 8 | K3 | Relay: 940 Uhms CT Coil, 2 Form A Contacts; James Electronic Corp C2213 | 06181490 | C |
| 9 | R1,2 | Resistor, Fixed, Wirewound, Precision: 10,000 Ohms $\pm .1 \%$; Resistance Products Co PB Type | A638 2450 | c |



| ITEM | REF．DESIG． | DESCRIPTION |  | EAI NO． | ＊CAT． |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | CR1－9 | Rectifier，Silicon\＆eneral Instrument DR587 Resistor，Variable，Composition：25K Ohms $\pm 30 \%$ ，． 2 W ；Chicago Telephone Supply Co． UPE－＇70 Type |  | A6140420 | C |
| 2 | $\begin{aligned} & \mathrm{R} 1-4,6-11, \\ & 26 \end{aligned}$ |  |  | A642 4520 | C |
| 3 | $\begin{aligned} & \mathrm{R} 14,16, \\ & 18,20,22, \\ & 24,27,29, \\ & 31 \end{aligned}$ | Resistor，Fixed，Wirewound，Precision：9，000 Uhms $\pm .5 \%$ ，． $01 \%$ Stability；Resistance Products Co PB Type |  | A638 5650 | C |
| 4 | R15 | Resistor，Fixed，Wirewound，Precision：11，000 Uhms $\pm .5 \%, .01 \%$ Stability；Resistance Products Co PB Type |  | A638 5560 | C |
| 5 | R17 | Kesistor，Fixed，Wirewound，Precision：12，547 Ohms $\pm .5 \%$ ，． $01 \%$ Stabi＿ity；Resistance Products Co PB Type |  | A638 5610 | C |
| 6 | R19 | Resistor，Fixed，Wirewound，Precision：14，347 Ohms $\pm .5 \%$ ，． $01 \%$ Stability；Resistance Products Co PB Type |  | 8.6385570 | C |
| 7 | R21 | Resistor，Fixed，wirewound，Precision：16，945 Ohms $\pm .5 \%$ ，． $01 \%$ Stabi」ity；Resistance Products Co PB Type |  | A638 5620 | C |
| 8 | $R 23$ | Resistor，Fixed，Wirewound，Precision：20，670 Ohms $\pm .5 \%, .01 \%$ Stabi」ity；Kesistance Products Co PB Type |  | A638 5580 | C |
| 9 | R25 | Resistor，Fixed，Wirewound，Precision：26，493 Uhms $\pm .5 \%$ ，． $01 \%$ Stabi」ity；Resistance Products Co PB Type |  | A638 5630 | C |
| 10 | R28 | Resistor，Fixed，Wirewound，Precision：36，882 Ohms $\pm .5 \%, .01 \%$ Stability；Resistance Products Co PB Type |  | A638 5590 | C |
| 11 | $R 30$ | Resistor，Fixed，Wirewound，Precision：60，677 Ohms $\pm .5 \%, .01 \%$ Stabi」ity；Resistance Products Co PB Type |  | $A 638 \quad 5640$ | C |
| 12 | R32 | Resistor，Fixed，Wirewound，Precision：171，000 Ohms $\pm .5 \%, .01 \%$ Stabiцity；Resistance Products Co PB Type |  | A638 5600 | C |
|  |  |  | UNIT TITLE <br> －VARIABLE DFG |  |  |
|  |  |  | 16．154－1 | 54－1 |  |



| ITEM | REF. DESIG. | description | EAINO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 2 | $\begin{aligned} & \mathrm{CR} 1,2 \\ & \mathrm{R} 1-4 \end{aligned}$ | Diode, Silicon: Hughes Semiconductors 1N459 <br> Resistor, Fixed, Wirewound, Precision: 3550 Ohms $\pm .05 \%$, . $005 \%$ Stability | $\begin{aligned} & B 6140070 \\ & 36387640 \end{aligned}$ | B C |
| 1 2 | CR1-14 R1,7 | $16.092 \mathrm{X}^{2} \mathrm{DFG}$ <br> Diode, Silicon: General Instrument DR837 <br> Resistor, Variable, Compsition: 5K Ohms $\pm 30 \%$, Chicago Telephone Supply UPE-70 Type | $\begin{aligned} & A 6140420 \\ & B 6424460 \end{aligned}$ | B |
| 3 | R2,3,8,9 | Kesistor, Variable, Composition: 2.5K Ohms $\pm 30 \%$; Chicago Telephone Supply UPE-70 Type | A642 4450 | C |
| 4 | $\begin{aligned} & \mathrm{K} 4,5,6,10, \\ & 11,12 \end{aligned}$ | Resistor, Variable, Composition: 1 K Uhms $\pm 30 \%$; Chicago Telephone Supply UPE-70 Type | A642 4440 | C |
| 5 | R13,32 | Kesistor, Fixed, Composition: 300 Ohms $\pm 5 \%, 1 / 2 \mathrm{~W}$; Allen-Bradley EB | 6263010 | A |
| 6 | R14,33 | Thermister, 88 uhms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$; Keystone Carbon Co. L3006-88-77-S11 | A646 0040 | B |
| 7 | R15,34 | Resistor, Fixed, Composition: 12 K Ohms $\pm 10 \%$, $1 / 2 W$; Allen-Bradley EB | 6261231 | A |
| 8 | R16,35 | Thermistor: 550 Ohms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$; <br> Keystone Carbon Co. L2006-550-92-S10 | A646 0030 | B |
| 9 | R17,36 | Resistor, Fixed, Composition: 820K Ohms $\pm 10 \%, 1 / 2 \mathrm{~W}$; Allen-Bradley EB | 6268241 | A |
| 10 | R18,37 | Resistor, Fixed, Wirewound, Precision: 14,800 Ohms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type | 16382820 | c |
| $11$ | R19,38. | Resistor, Fixed, Wirewound, Precision: 18,000 Ohms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type | A638 2830 | C |
| 12 | R20,39 | Resistor, Fixed, Wirewound, Precision: 22,400 Ohms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type | 16382840 | C |
| - note: the category column is designed to indicate availability of parts. <br> a - indicates parts that should be purchased locally. <br> a- Indicates parts that can be purchased locally or from eal. <br> - INDICATES PARTS THAT SHOULD BE PURCHASED FROM EAI. <br> the proper eal part should beinstalled for category citems. a compLETE description ts given to provide for temporary repalrs; however,EAI WILL NOT BE RESPONSIBLEIF UNIT IS NOT WITHIN SPECIIICATIONS UNDER <br> THESE CONDITIONS. these conditions. |  |  | UNIT TITLE   <br>  $X^{2}$ DFG  <br> MODEL NO.   <br> 16.275 Sh 1 of 2  |  |
|  |  |  |  |  |


| ITEM | REF. DESIG. | DESCRIPTION |  | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 13 | R21,40 | Resistor, Fixed, Wirewound, Precision: 29,600 Uhms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type |  | A638 2850 | C |
| 14 | R22,41 | Resistor, Fixed, Wirewound, Precision: <br> 43,300 Uhms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type |  | A638 5250 | C |
| 15 | R23,42 | Resistor, Fixed, Wirewound, Precision: <br> 85,500 Ohms $\pm 1 \%, .2 \mathrm{~W}$; Resistance Products Co PG Type |  | 46382870 | C |
| 16 | R24,43 | Thermistor: 300 K unms $\pm 5 \%$ at $37.8^{\circ} \mathrm{C}$; <br> Keystone Carbon Co. L1215-300K-152-S12 |  | A646 0020 | 8 |
| 17 | $\begin{aligned} & \mathrm{K} 25-30, \\ & 44-49 \end{aligned}$ | Resistor, Fixed, hirewound, Precision: <br> 12,500 Ohms $\pm 1 \%$, . 2 W ; Resistance Products Co PB Type |  | A638 2800 | C |
| 18 | R31,50 | Resistor, Fixed, kirewound, Precision: <br> 13,500 Ohms $\pm 1 \%$, . 2 h ; Resistance Products Co PB Type |  | A638 2810 | C |


| item | REF. DESIG. | description |  | EAINO. |  |  |  | T. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | R1-4 | Resistor, Fixed, Wirewound, Precision: 5000 ohms $\pm .05 \%$, . $005 \%$ stability; Julie Research Labs R45 |  | B638 | 765 |  |  | C |
|  |  | 16.127 Log X DFG |  |  |  |  |  |  |
| 1. | CR1-12 | Diode, Silicon: General Instrument DR837 <br> Resistor, Variable, Composition: 2 K ohms $\pm 30 \%$; . 3 W ; Chicago Telephone Supply UPE-70 Mode1 (Modified) |  | A614 | 042 |  |  | B |
| 2 | R1,2,38,39 |  |  | A642 | 448 |  |  | C |
| 3 | $\begin{aligned} & \mathrm{R} 3,4,5,40, \\ & 41,42 v \\ & \text { see } n \end{aligned}$ | Resistor, Variable, Composition: 1 K ohms $\pm 30 \%$; . 3 W ; Chicago Telephone Supply UPE-70 Model (Modified) |  | B642 | 444 |  |  | C |
| 4 | R6,32 | Resistor, Fixed, Wirewound, Precision: 9,800 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 609 | 0 |  | C |
| 5 | R7,33 | Resistor, Fixed, Wirewound, Precision: 19,600 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 611 | 0 |  | C |
| 6 | R8,34 | Resistor, Fixed, Wirewound, Precision: 21,200 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 470 |  |  | C |
| 7 | R9, 35 | Resistor, Fixed, Wirewound, Precision: 15,500 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 610 |  |  | C |
| 8 | R10,36 | Resistor, Fixed, Wirewound, Precision: 5,000 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 608 |  |  | C |
| 9 | R11,37 | Resistor, Fixed, Wirewound, Precision: 4,280 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 440 |  |  | C |
| 10 | R12,25 | Resistor, Fixed, Wirewound, Precision: 20,900 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 447 |  |  | C |
| 11 | R13,26 | Resistor, Fixed, Wirewound, Precision: 49,200 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 | 450 |  |  | C |
| - Note: the category column is designed to indicate avallability of parts. <br> a - indicates parts that should be purchased locally. <br> B-INDICATES PARTS THAT CANBE PURCHASED LOCALLY OR <br> THE PROPEREAI PART SHOULD BE INSTALLED FOR CATEGORY C ITEMS. A COMplete description ts given to provide for temporary repalrs; however. eai will not be responsible if unit is not within specifications under these conditions. |  |  | Unit title LOG X DFG |  |  |  |  |  |
|  |  |  | MODEL NO. |  |  |  |  |  |


| ITEM | REF. DESIG. | DESCRIPTION |  | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 12 | R14,27 | Resistor, Fixed, Wirewound, Precision: <br> 27,700 ohms $\pm 1 \% ; .005 \%$ stability; National <br> Resistance Corp., EU-2 Type |  | A638 4490 | C |
| 13 | R15,28 | Resistor, Fixed, Wirewound, Precision: 13,000 ohms $\pm 1 \% ; .005 \%$ stability; National Resistance Corp., Eu-2 Type |  | A638 4440 | C |
| 14 | R16,29 | Resistor, Fixed, Wirewound, Precision: 4,440 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 4410 | C |
| 15 | R17,30 | Resistor, Fixed, Wirewound, Precision: 694 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type |  | A638 4380 | C |
| 16 | R18,31 | Resistor, Fixed, Wirewound, Precision: 317 ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp EU-2 Type |  | A638 4370 | C |
| 17 | R19,22 | Resistor, Variable, Composition: 300 ohms <br> $\pm 20 \%$; 3 W ; Chicago Telephone Supply UPE-70 <br> Model (Modified) |  | $\begin{aligned} & 16424490 \\ & \text { g? motic } \end{aligned}$ | C |
| 18 | R20, 23 | ```Resistor, Fixed, Wirewound, Precision: 2,900 ohms 土. 1%; .005% stability; National Resisf tance Corp., EU-2 Type``` |  | A638 4390 | C |


| ITEM | REF. DESIG. | DESCRIPTION |  | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | RI-4 | Resistor, Fixed, Wirewound, Precision: ohms $\pm .05 \% ; .005 \%$ stability; Julie Res Labs R45 | 5000 search | B638 7650 | C |
|  |  | $16.1341 / 2$ Log X DFG |  |  |  |
| 1 | CR1-12 | Diode, Silicon: General Instrument DR837 |  | A614 0420 | B |
| 2 | R1, 2, 38, 39 | Resistor, Variable, Composition: 4 K ohms $\pm 30 \%$; . 3 W ; Chicago Telephone Supply UP Model (Modified) | PE-70 | A642 4870 | C |
| 3 | $\begin{aligned} & R 3,4,5,40, \\ & 41,42 \end{aligned}$ | Resistor, Variable, Composition: 2 K ohms $\pm 20 \%$; . 3W; Chicago Telephone Supply UP Model (Modified) | PE-70 | B642 4480 | C |
| 4 | R6,32 | Resistor, Fixed, Wirewound, Precision: <br> 19,900 ohms $\pm 1 \% ; .005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 6130 | C |
| 5 | R7,33 | Resistor, Fixed, Wirewound, Precision: <br> 39,600 ohms $\pm 1 \%$; . $005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 6150 | C |
| 6 | R8,34 | Resistor, Fixed, Wirewound, Precision: <br> 41,100 ohms $\pm 1 \% ; .005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 4340 | C |
| 7 | R9, 35 | Resistor, Fixed, Wirewound, Precision: <br> 30,700 ohms $\pm 1 \% ; .005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 6140 | C |
| 8 | R10,36 | Resistor, Fixed, Wirewound, Precision: <br> 11,000 ohms $\pm 1 \% ; .005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 6120 | C |
| 9 | R11,37 | Resistor, Fixed, Wirewound, Precision: <br> 8,450 ohms $+1 \%$; . $005 \%$ stability; Natio <br> Resistance Corp., EU- 2 Type | onal | A638 4270 | C |
| 10 | R12,25 | Resistor, Fixed, Wirewound, Precision: <br> 41,800 ohms $\pm 1 \%$; . $005 \%$ stability; Nati <br> Resistance Corp., EU-2 Type | ional | A638 4330 | C |
| 11 | R13,26 | Resistor, Fixed, Wirewound, Precision: 101,600 ohms $\pm 1 \%$; .005\% stability; Nat Resistance Corp., EU-2 Type | ional | A638 4360 | C |
| - Note: the category column is designed to indicate avallability of parts. <br> a - Indicates parts that should be purchased locally. <br> b - Indicates parts that can be purchased locally or from eal. <br> C. INDICATES PARTS THAT SHOULD BE PURCHASED FROM EAI. <br> The proper eal part should beinstalled for category citems. a comPLETE DESCRIPTION IS GIVEN TO PROVIDE FOR TEMPORARY REPAIRS; HOWEVER, EAI WILL Not be responsible if Unit is not within specifications under THESE CONDITIONS. |  |  | $\begin{aligned} & \text { UNIT TITLE } \\ & 1 / 2 \text { LOG } X \text { DFG } \end{aligned}$ |  |  |
|  |  |  | $\begin{array}{\|r} \hline \text { MODEL NO. } \\ 16.281 \\ \hline \end{array}$ | Sh. 1 |  |


| ITEM | REF. DESIG. | DESCRIPTION | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 12 | R14, 27 | ```Resistor, Fixed, Wirewound, Precision: 55,400 ohms }\pm1%;.005% stability; Nationa Resistance Corp., EU-2 Type``` | A638 4350 | C |
| 13 | R15,28 | ```Resistor, Fixed, Wirewound, Precision: 26,000 ohms }\pm1%;.005% stability; Nationa Resistance Corp., EU-2 Type``` | A638 4300 | C |
| 14 | R16,29 | ```Resistor, Fixed, Wirewound, Precision: 8,870 ohms }\pm1%;.005% stability; National Resis- tance Corp., EU-2 Type``` | A638 4280 | C |
| 15 | R17,30 | ```Resistor, Fixed, Wirewound, Precision: 1,480 ohms }\pm1%; .005% stability; National Resis- tance Corp., EU-2 Type``` | A638 424.0 | C |
| 16 | R18,31 | Resistor, Fixed, Wirewound, Precision: 605 <br> ohms $\pm 1 \%$; . $005 \%$ stability; National Resistance Corp., EU-2 Type | A638 4230 | C |
| 17 | $\left\lvert\, \begin{array}{ll} \text { R19, } 22 \\ \text { See } \end{array}\right.$ | Resistor, Variable, Composition: 500 ohms <br> $+30 \%$; 3 W ; Chicago Telephone Supply UPE-70 <br> Model (Modified) | A642 4500 | C |
| 18 | R20, 23 | Resistor, Fixed, Wirewound, Precision: 5,800 ohms $\pm .1 \% ; .005 \%$ stability; National Resistance Corp., EU-2 Type | A638 4250 | C |


| ITEM | REF. DESIG. | DESCRIPTION | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | CR1, 2 | Diode, Germanium: Clevite CTP462 | 6140430 | B |
| 2 | DS 1-8 | Lamp, Incandescent: General Electric 328 | 5780100 | A |
| 3 | M1 | Meter, DC Microammeter: 50-0-50 Microamp <br> Movement with Scale per EAI Dwg A214 027 0; Assembly Products, Inc. 561 Model | 5900320 | C |
| 4 | R1 | Resistor, Fixed, Composition: 8.2 K ohms $\pm 10 \%$ 1/2W; Allen-Bradley EB | 6268221 | A |
| 5 | R2 | Resistor, Fixed, Film: 4000 ohms $\pm 1 \%, 1 / 2 \mathrm{~W}$; Weston 9852B | 6340960 | B |
| 6 | R3 | Resistor, Fixed, Film: 18,000 ohms $\pm 1 \%, 1 / 2 \mathrm{~W}$; Weston 9852B | 6340970 | B |
| 7 | R4 | Resistor, Fixed, Film: 58,000 ohms $\pm 1 \%, 1 / 2 \mathrm{~W}$; Weston 9852B | 6340980 | B |
| 8 | R5 | Resistor, Fixed, Film: 198,000 ohms $\pm 1 \%, 1 / 2 \mathrm{~W}$ Weston 9852B | 6340640 | B |
| 9 | R6 | Resistor, Fixed, Film: 598,000 ohms $\pm 1 \%, 1 / 2 \mathrm{~W}$ Weston 9852B | 6340990 | B |
| 10 | R7 | Resistor, Variable, Wirewound: 500 ohms $\pm 10 \%$ .25W; Bourns Laboratories 273-1-501 | B642 2890 | B |
| 11 | R8 | Resistor, Fixed, Film: 700 ohms $\pm 1 \%, 1 / 2 W$; Weston 9852B | 6343390 | B |
| 12 | S 1 | Switch, Rotary: 3 Sections, 1 Pole Per Section, 2-12 Postions; Centralab PA-2009 | 6580110 | A |
| 13 | S 2 | Switch, Rotary: 1 Section, 2 Poles, 2-12 Positions; Centralab PA-2000 Series | B658 1970 | C |
| 14 | S3 | Switch, Push: 2 ea 2 Form A Contacts; Capitol Machine Co. SP-202 Model | B656 0770 | C |
| 15 | S4 | Switch, Push: 10 ea 2 Form A Contacts; Capitol Machine Co. SP-210 Model | C656 0780 | C |
| 16 | S5 | Switch, Push: 10 ea 2 Form A Contacts; Capitol Machine Co. SP-210 Model | C656 0781 | C |
| 17 | S6 | Switch, Push, Rocker: DPDT; Cutler-Hammer 8!38K1-BK-09 | 6560800 | B |
| - Note: the category column is designed to indicate availability of parts. <br> a - indicates parts that should be purchased locally. <br> b- indicates parts that can be purchased locally or from eaio <br> C. INDICATES PARTS that should be purchased from eat. <br> the proper eal part should be installed for category citems. a com- <br> PLETE DESCRIPTION TS GIVEN TO PROVIDE FOR TEMPORARY REPAIRS; HOWEVER. <br> EAI WILL NOT BE RESPONSIBLE IF UNIT IS NOT WITHIN SPECIFICATIONS UNDER <br> these conditions. <br> date 5 / 22/ |  |  | UNIT TITLE <br> ve hare $20^{\text {CONTROL PANEL }}$ |  |
|  |  |  | MODEL NO. <br> 20.790 |  |







| ITEM | REF. DESIG. | DESCRIPTION |  | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | CR1,2 | Kectifier, Silicon: Hughes Semi-Conducto HR10212 |  | 6140340 | $B$ |
| 2 | CR 3 | Diode, Germaniun: Clevite CTP462 Type |  | 6140430 | $B$ |
| 3 | K 1 | Kelay: 430 Ohins D.C. Coil, 2 Form C Cont General E^ectric 352791G210-R-29 | acts | 6181260 | B |
| 4 | 6 1-5 | Transistor, Germanium: PNP; Industro |  | B686 0320 | C |
| 5 | 46 | Transistor, Germaniua: PNP; General Elec 2N321 Type | tric | 6860040 | $A$ |
| 6 | K1 <br> seenotice | Resistor, Fixed, Wirewound, Precision: $820 \frac{70,000}{6}$ Ohms $\pm 1 \%$, .2W; Resistance Prod Co PB Type | ucts | \$638 2880 | C |
| 7 | $\mathrm{R} 2 \sim$ <br> foe notice | Kesistor, Fixed, Wirewound, Precision: <br> 12,00 Ohins $\pm 1 \%, .2 \mathrm{~W}$; Resistance Produ Co PB Type / 00 000 | ucts | A638 2890 | C |
| 8 | K3,4 | Kesistor, Fixed, Composition: 27 K Ohms $\pm$ $1 / 2 W$; Allen-Bradey EB | $=10 \%,$ | $626 \quad 2731$ | A |
| 9 | K5 | Resistor, Fixed, Composition: 12K Onns $\pm$ $1 / 2 W$; Allen-Bradey EB | $10 \%,$ | 6261231 | A |
| 10 | K6 | Resistor, Fixed, Composition: 330 Uhms $\pm$ 1/2W; Allen-Bradley EB | $10 \%,$ | 6263311 | A |
| 11 | K7 | Resistor, Fixed, Composition: 4.7K Uhms 1/2W; Allen-Bradley EB | $\pm 10 \%,$ | 6264721 | L |
| 12 | K8,11 | Resistor, Fixed, Composition: 15K Ohms $\pm$ $1 / 2 \mathrm{~W}$; Allen-Bradley EB | $10 \% \text {, }$ | 6261531 | 6 |
| 13 | 89 | Resistor, Fixed, Compsition: 8.2K Uhms $\pm$ $1 / 2 W$; Allen-Bradley $E B$ | $10 \% \text {, }$ | 6268221 | A |
| 14 | R10 | Resistor, Fixed, Composition: 2.2K Uhms $=$ $1 / 2 h$; Allen-Bradley EB | $\pm 10 \%,$ | 6262221 | A |
| 15 | H12 | Resistor, Fixed, Composition: 100 Ohms $\pm 1$ 1/2W; Allen-Bradley EB | $10 \% \text {, }$ | 6261011 | A |
|  |  |  | UNIT TITLE |  |  |
|  |  |  | COMPARATOR |  |  |
|  |  |  | $\begin{array}{\|r} \hline \text { MODEL NO. } \\ 40.404 \\ \hline \end{array}$ |  |  |




| ITEM | REF. DESIG. | description | EAI NO. | *CAT. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | C1 | Capacitor, Fixed, Electrolytic: 50 UF, 25V; International Electronic Industries | A516 1220 | c |
| 2 | Ch1 | Diode, Silicon: Zener; Pacific Semi-Conductor 1N752 | 6140780 | B |
| 3 | DS 1-14 | Lamp, Incandescent: General Electric 1705 | 5780370 | A |
| 4 | R1 | Resistor, Variable, wirewound: 50 Uhms $\pm 10 \%$, . 25w; Bourns Laboratories 200L-1-500 | 6420740 | B |
| 5 | K2,3 | Kesistor, Fixed, Wirewound, Precision: 20,000 Uhms $\pm .1 \%, .005 \%$ Stability; Resistance Products Co PB Type | A638 7020 | C |
| 6 | R4,6 | Kesistor, Fixed, Composition: 10K Ohms $\pm 10 \%$, $1 / 2 W$; Allen-Bradley EB | 6261031 | A |
| 7 | k5,12 | Kesistor, Fixed, Wirewound, Precision: 10,000 Uhms $\pm .1 \%, .005 \%$ Stability; Resistance Products Co PB Type | A638 7430 | C |
| 8 | R7 | Resistor, Fixed, Wirewound, Precision: Value determined at time of manufacture. | - | - |
| 9 | K8 | Resistor, Fixed, Wirewound, Precision: 5,000 Uhms $\pm 1 \%, .01 \%$ Stability; Resistance Products Co PB type | A638 3150 | C |
| 10 | R9 | Resistor, Variable, wirewound: 250 Ohms $\pm 10 \%$, .25w; Bourns Laboratories 271-1-251 | 6424910 | B |
| 11 | K10 | Resistor, Fixed, Composition: 1 K Ohns $\pm 10 \%$, $1 / 2 \mathrm{w}$; Allen-Bradley EB | 6261021 | A |
| 12 | R11 | Resistor, Variable, Wirewound: 20 Ohms $\pm 10 \%$, .25w; Bourns Laboratories 200L-1-200 | 6420730 | B |
| 13 | R13,14 | Resistor, Variable, Composition: 50K Ohms $\pm 30 \%$, . 2 W ; Chicago Telephone Supply HH1860 | 6423510 | B |
|  |  |  | UN |  |
|  |  |  | REFERENCE REGULATOR |  |
|  |  |  | $\begin{array}{r\|} \hline \text { MODEL NO. } \\ 43.104 \\ \hline \end{array}$ |  |


[^0]:    Page 56 and
    Figure 3.3-2 Paragraph 3a Change the desigmation of the cabinet connectors for Reference Amplifier and Reference Regulator to J67 and J68 respectively. Also, on Figure 3.3-2, Pin T of J68 (J69 on drawing) is wired to J61-1 for reference slaving.

    Page 62 Paragraph 3a Change designation of cabinet connector for Rep Op Timing Unit to J69.

[^1]:    *The unit actually produces the product of $X$ times the absolute value of $X$; thus, the " $X^{2 / 1}$ output will change sign with a sign change of $X$.

[^2]:    *The components marked with an asterisk (*) are listed for reference only. The parts lists for these components appear in a separate manual for the respective components.

