

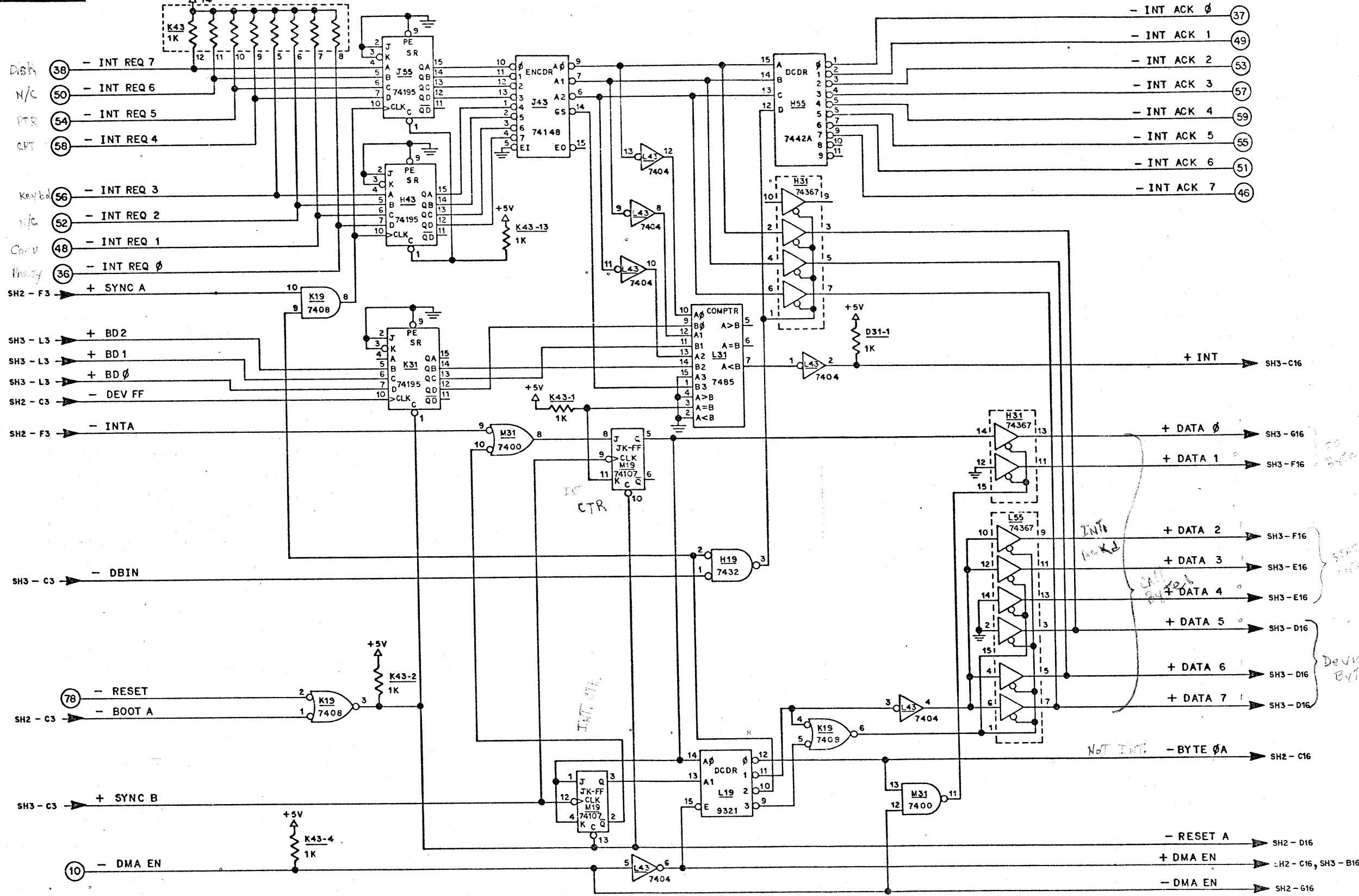


**Diablo Systems Incorporated**

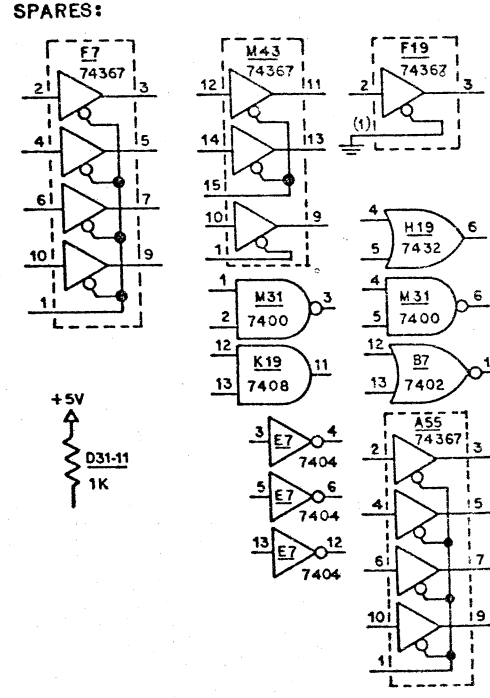
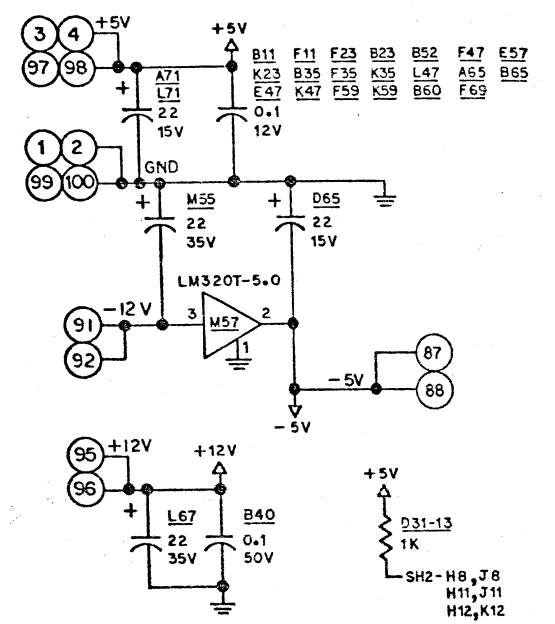
## **Schematic Diagrams**

Model \_\_\_\_\_ Serial No. \_\_\_\_\_



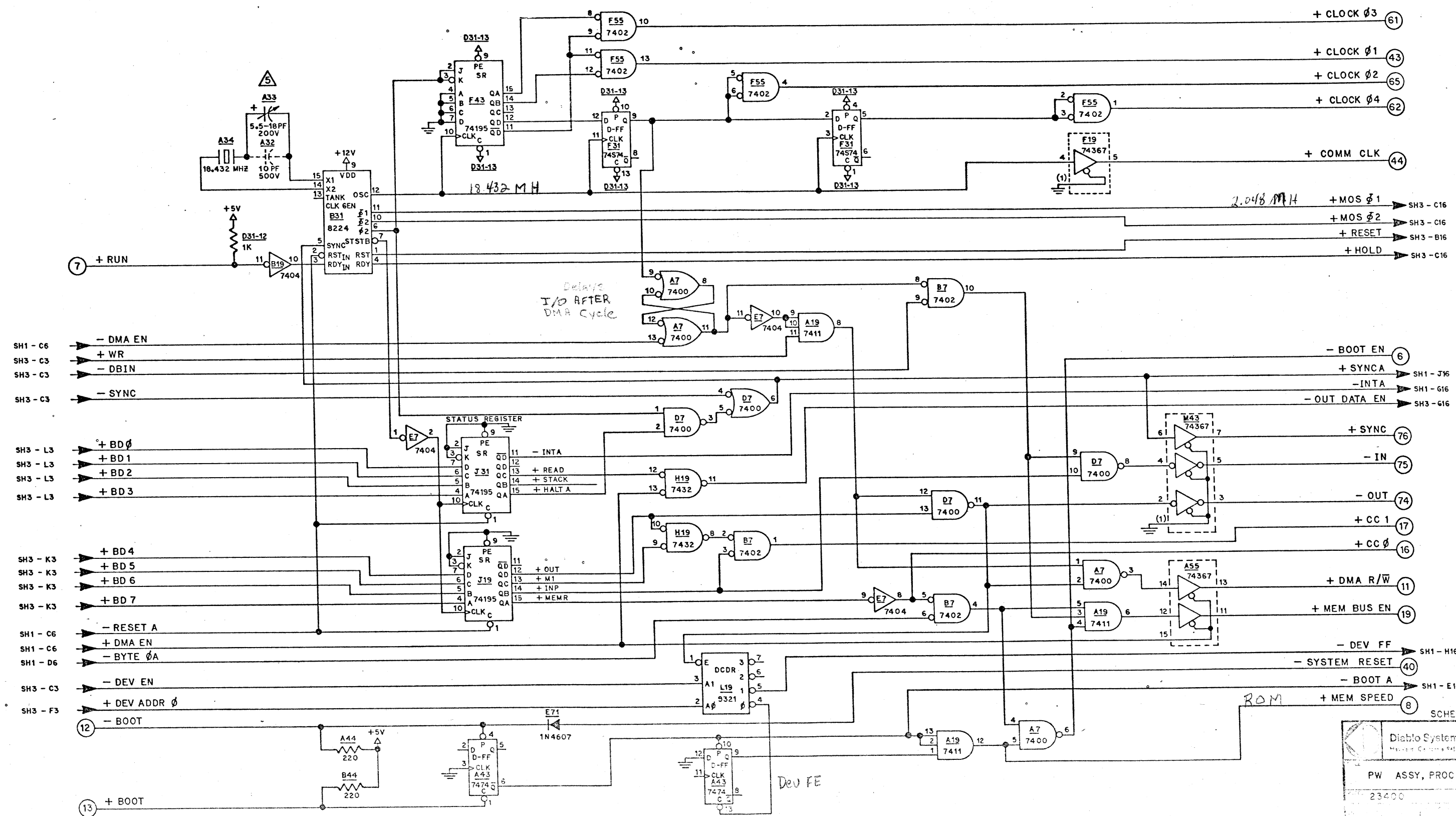


- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.  
 4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;  
 +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.  
 ON 23404-01, TRIMMER CAPACITOR A33 IS DELETED AND CAPACITOR A32 IS ADDED. (23404-02 SHOWN).



SCHMATIC DIAGRAM

Diablo Systems Incorporated  
 Hayward, California 94545  
 TITLE PW ASSY, PROC 2  
 MODEL 23400



SCHEMATIC DIAGRAM

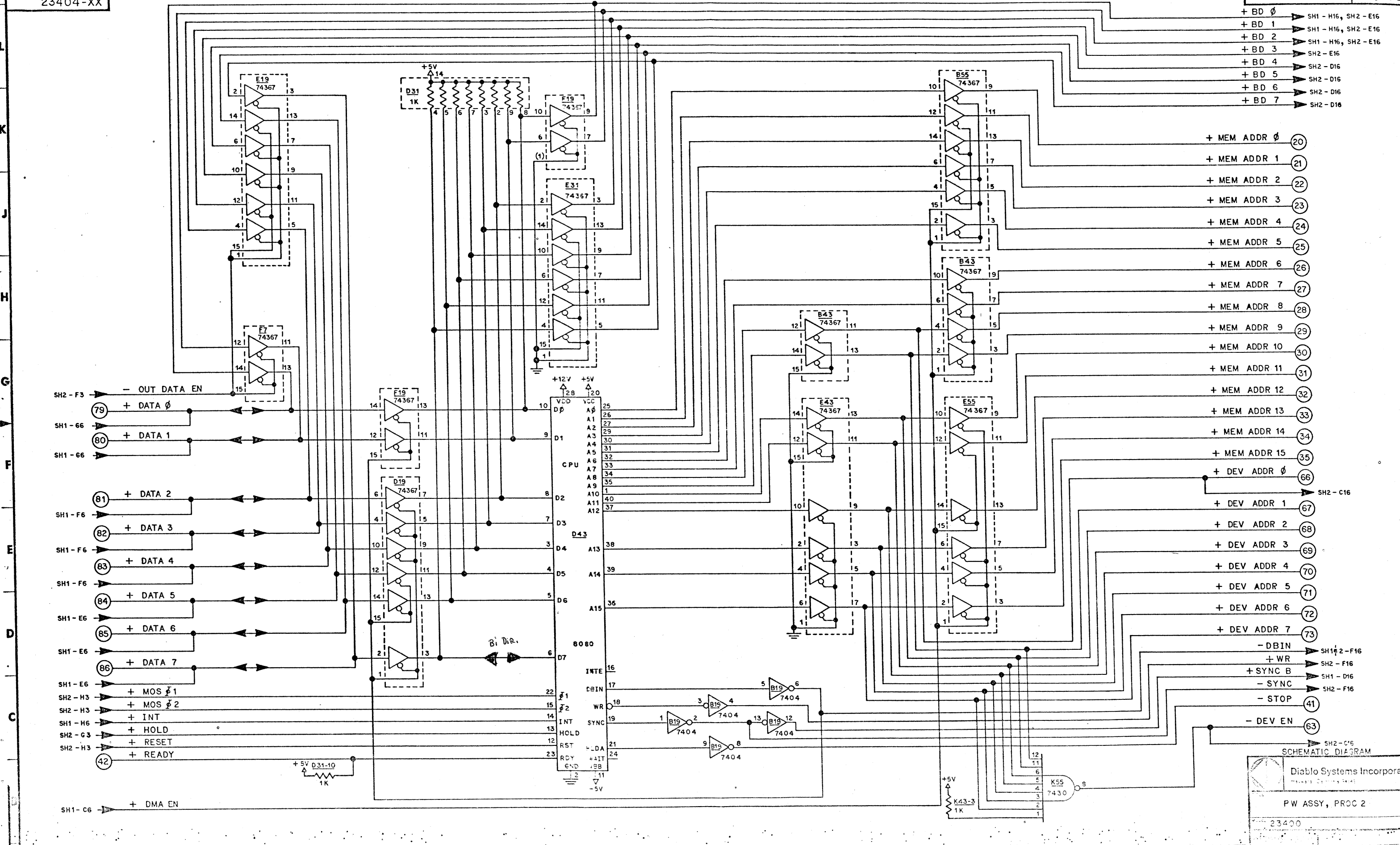
Diablo Systems Incorporated  
 Hayward, California 94545

PW ASSY, PROC 2

23400

PRODUCT NO. 23404-XX

PRODUCT NO. 23404-XX



SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, PROC 2

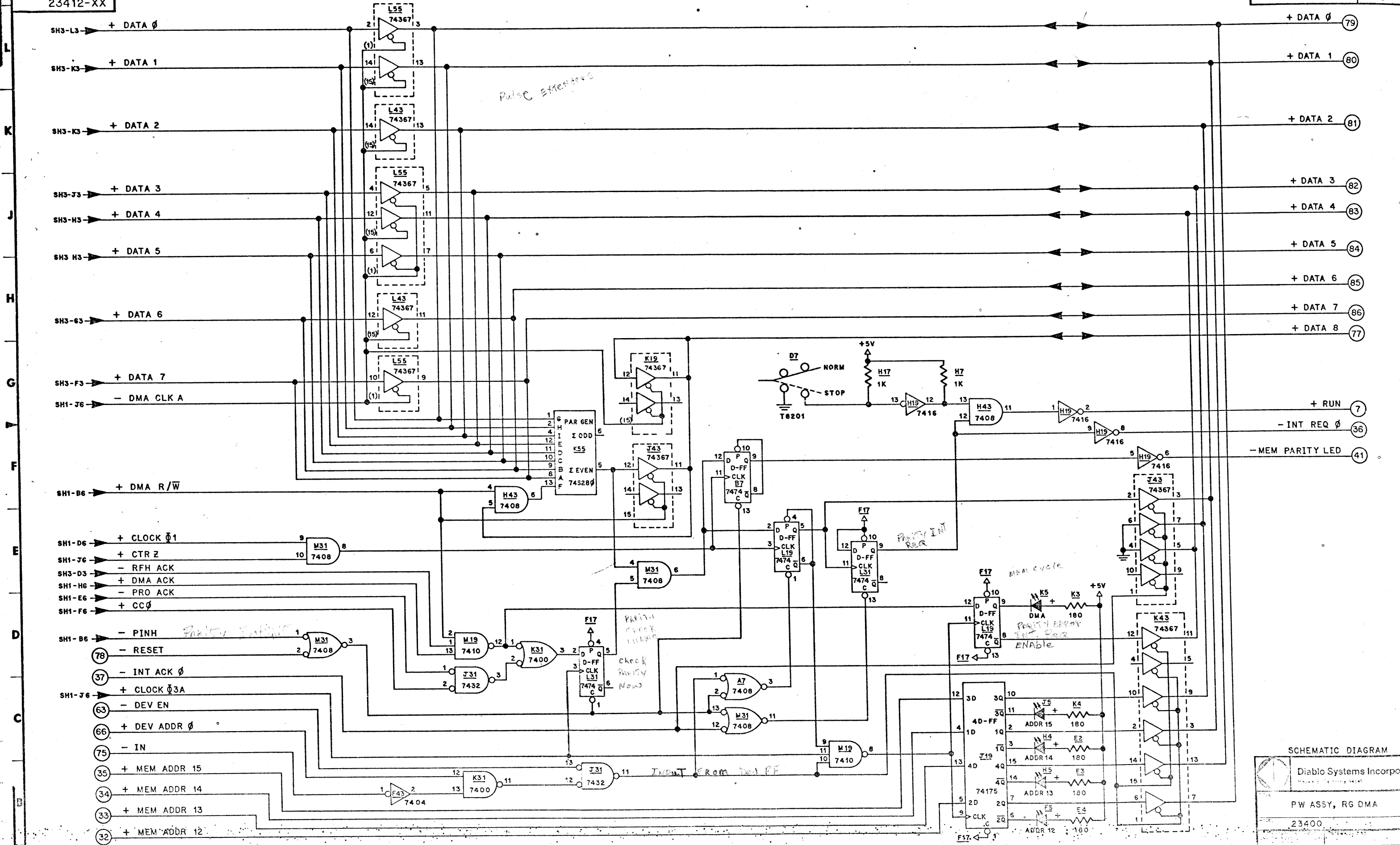
23400





23412-XX

23412-XX

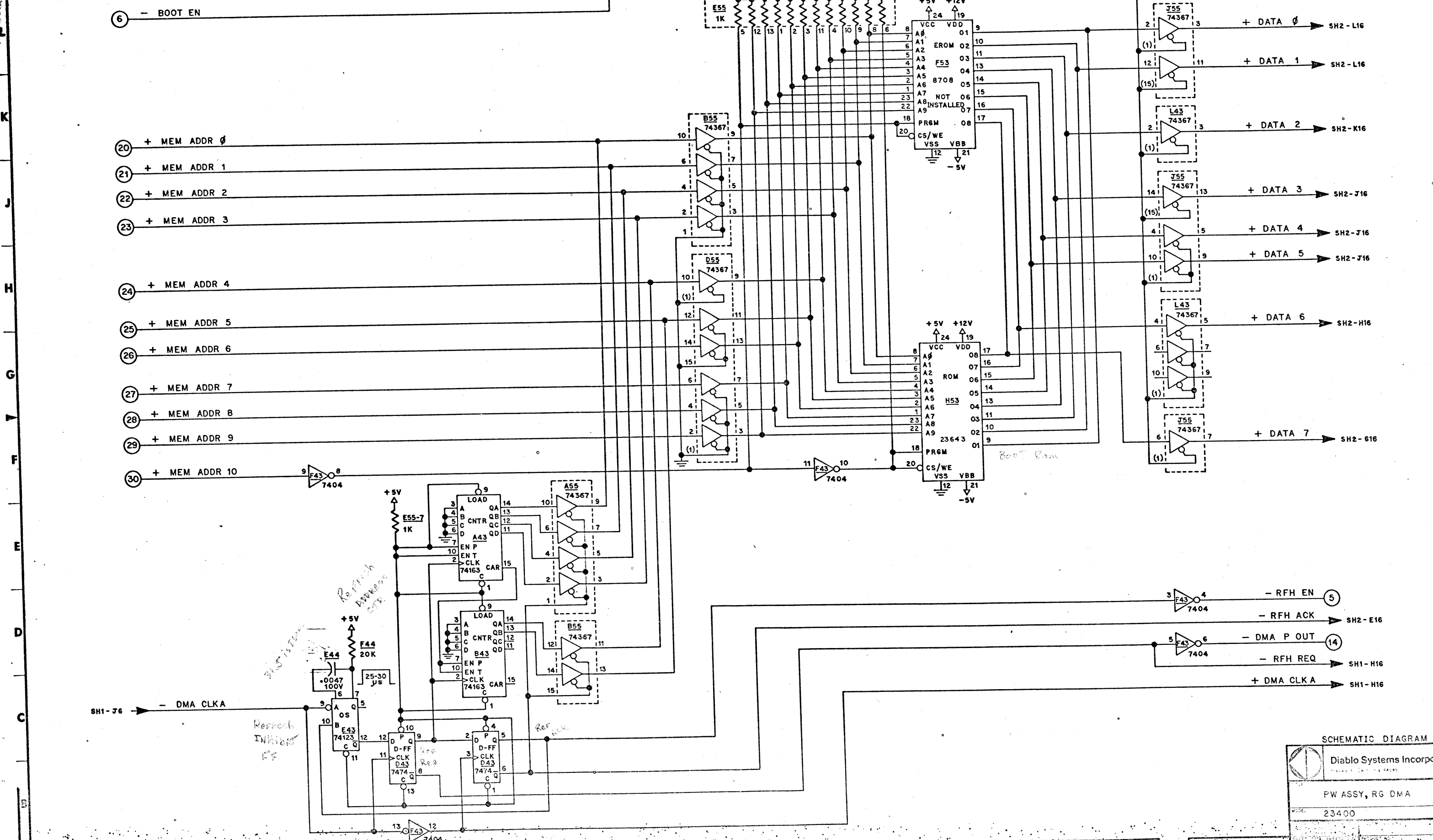


SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 PW ASSY, RG DMA  
 23400



PRODUCT NO 23412-XX

23412-XX D3



K  
J  
H  
G  
V  
F  
E  
D  
C

SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 PW ASSY, RG DMA  
 MODEL 23400  
 23412-XX











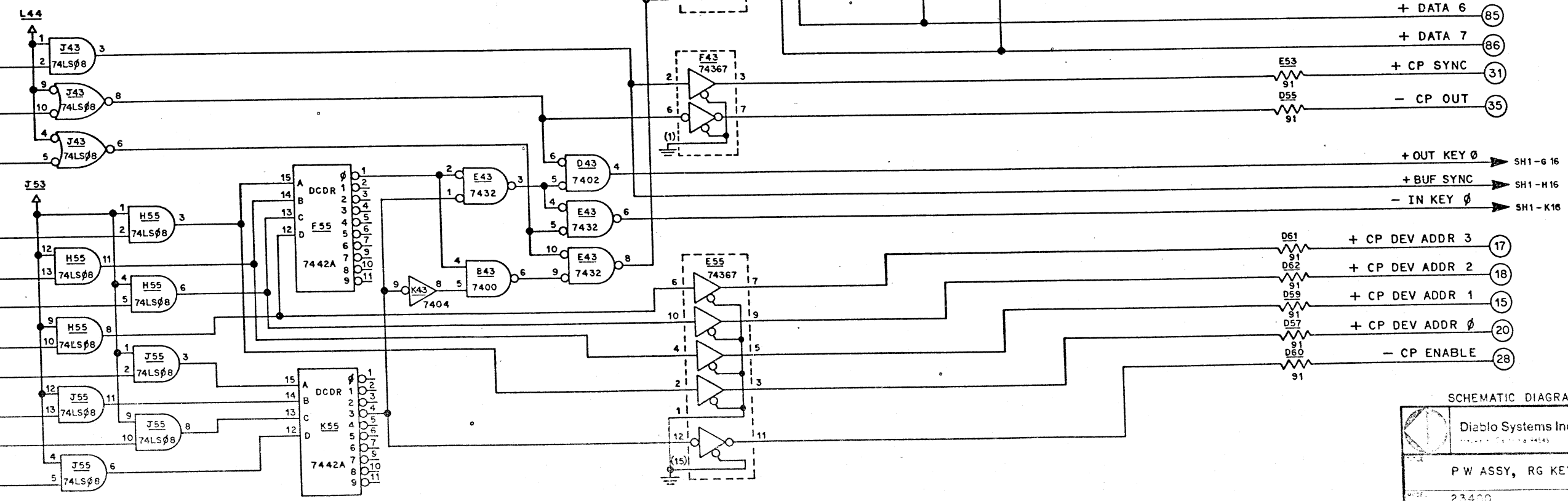
SH1 - L5 → + DATA 0  
 SH1 - K5 → + DATA 1  
 SH1 - K5 → + DATA 2  
 SH1 - K5 → + DATA 3  
 SH1 - K5 → + DATA 4  
 SH1 - J5 → + DATA 5

(25) + CP DATA 0  
 (14) + CP DATA 1  
 (23) + CP DATA 2  
 (12) + CP DATA 3  
 (21) + CP DATA 4  
 (10) + CP DATA 5  
 (19) + CP DATA 6  
 (16) + CP DATA 7

(76) + SYNC  
 (74) - OUT  
 (75) - IN

(66) + DEV ADDR 0  
 (67) + DEV ADDR 1  
 (68) + DEV ADDR 2  
 (69) + DEV ADDR 3  
 (70) + DEV ADDR 4  
 (71) + DEV ADDR 5  
 (72) + DEV ADDR 6  
 (73) + DEV ADDR 7

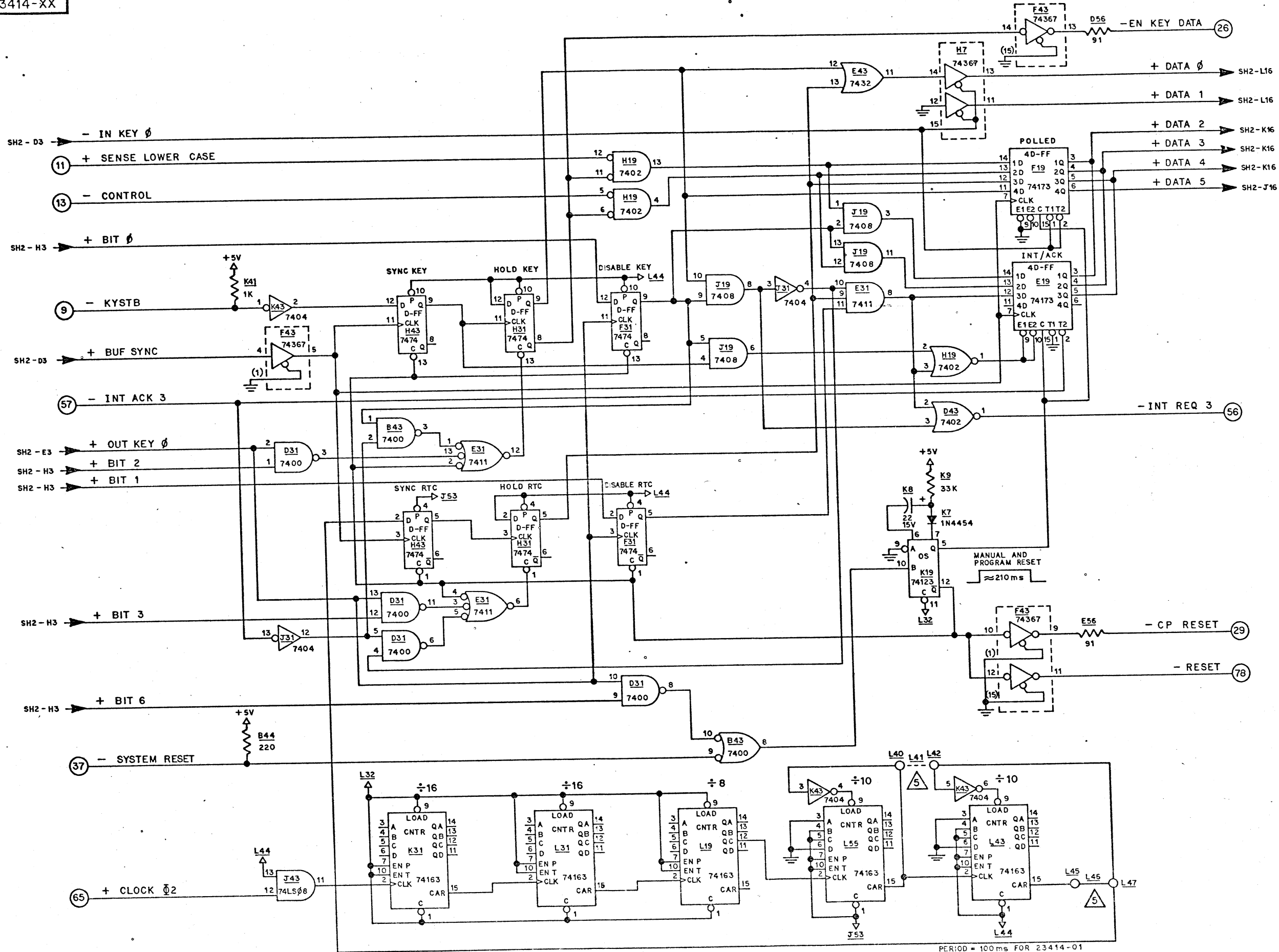
+ CP BUF DATA 0 (40)  
 + CP BUF DATA 1 (22)  
 + CP BUF DATA 2 (38)  
 + CP BUF DATA 3 (24)  
 + CP BUF DATA 4 (36)  
 + CP BUF DATA 5 (34)  
 + CP BUF DATA 6 (32)  
 + CP BUF DATA 7 (30)  
 + BIT 0 → SH1-J16  
 + BIT 1 → SH1-G16  
 + BIT 2 → SH1-E16  
 + BIT 3 → SH1-E16  
 + BIT 6 → SH1-D16  
 + DATA 0 (79)  
 + DATA 1 (80)  
 + DATA 2 (81)  
 + DATA 3 (82)  
 + DATA 4 (83)  
 + DATA 5 (84)  
 + DATA 6 (85)  
 + DATA 7 (86)  
 + CP SYNC (31)  
 - CP OUT (35)  
 + OUT KEY 0 → SH1-G 16  
 + BUF SYNC → SH1-H 16  
 - IN KEY 0 → SH1-K 16  
 + CP DEV ADDR 3 (17)  
 + CP DEV ADDR 2 (18)  
 + CP DEV ADDR 1 (15)  
 + CP DEV ADDR 0 (20)  
 - CP ENABLE (28)



SCHEMATIC DIAGRAM  
 Diablo Systems Incorporated  
 P.W. ASSY, RG KEY  
 23400  
 1 2 2 8 23414-XX

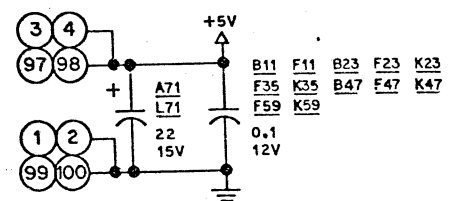
PRODUCT NO 23414-XX

23414-XX D2

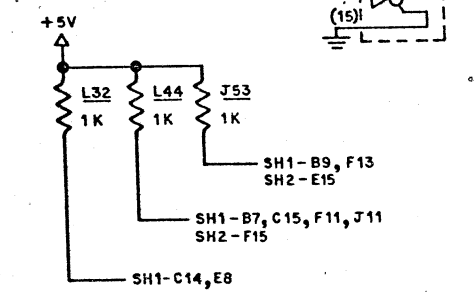
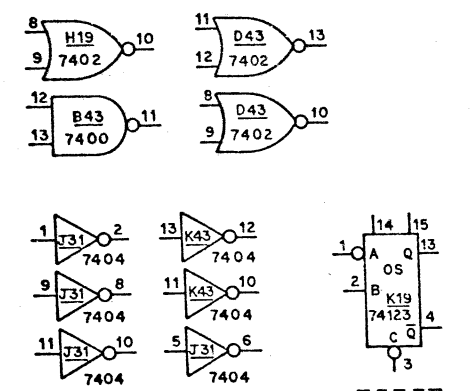


- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL CAPACITANCE SPECIFIED IN MICROFARADS  
 4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;  
 +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

△ 23414-01 SHOWN.  
 ON 23414-02 ASSEMBLY, JUMPER L41 IS INSTALLED AND THE CONDUCTOR L46 IS CUT.



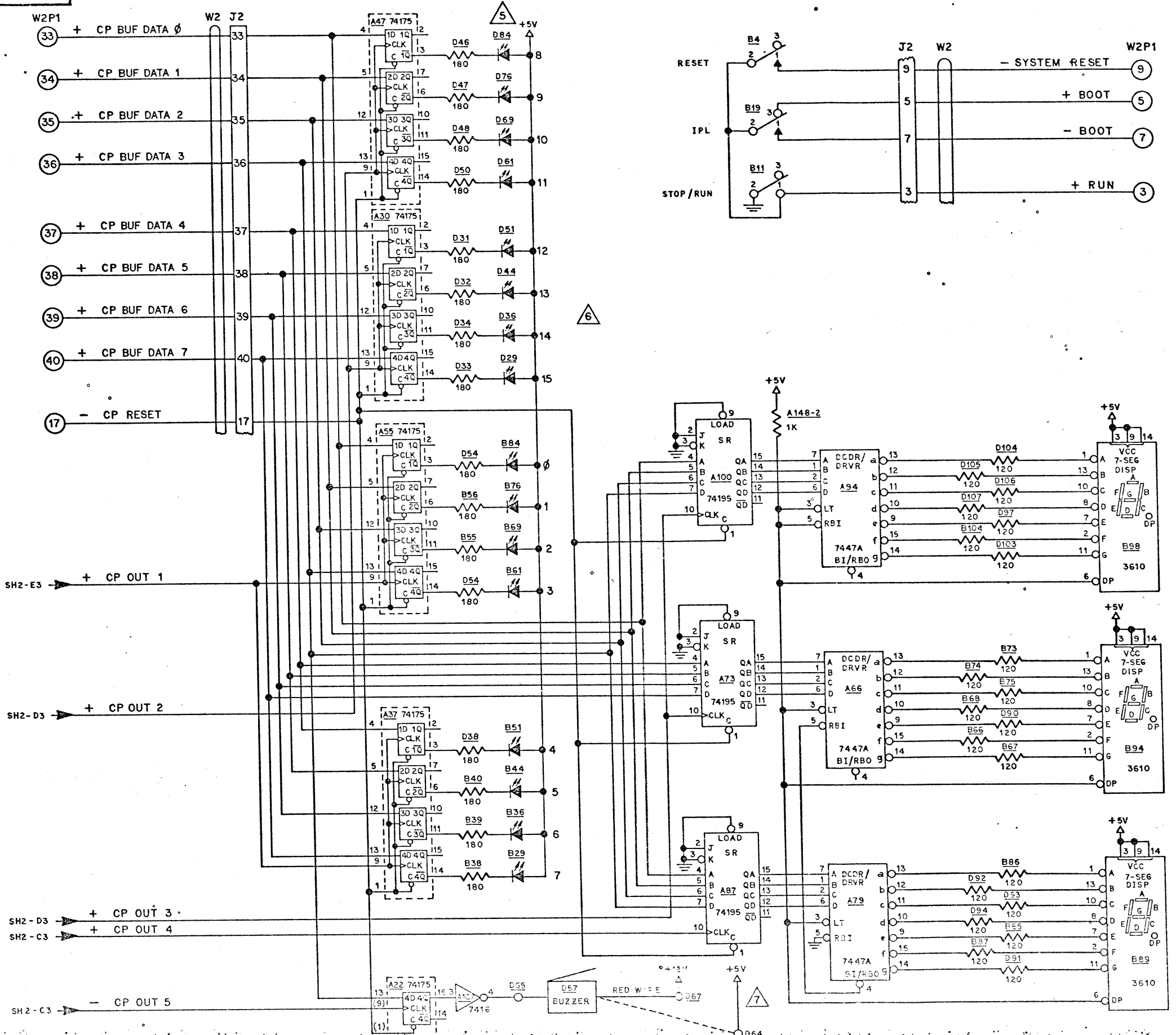
SPARES:



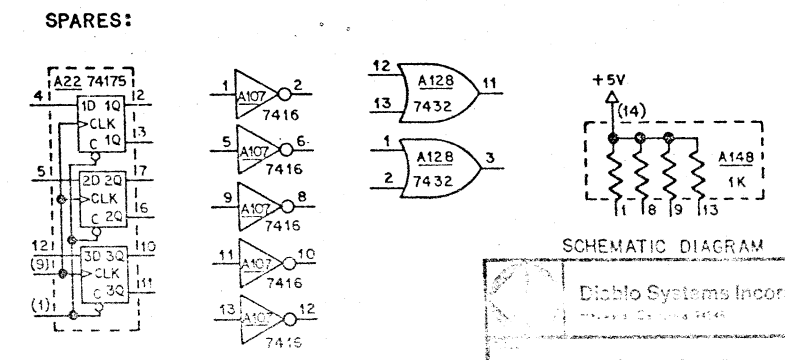
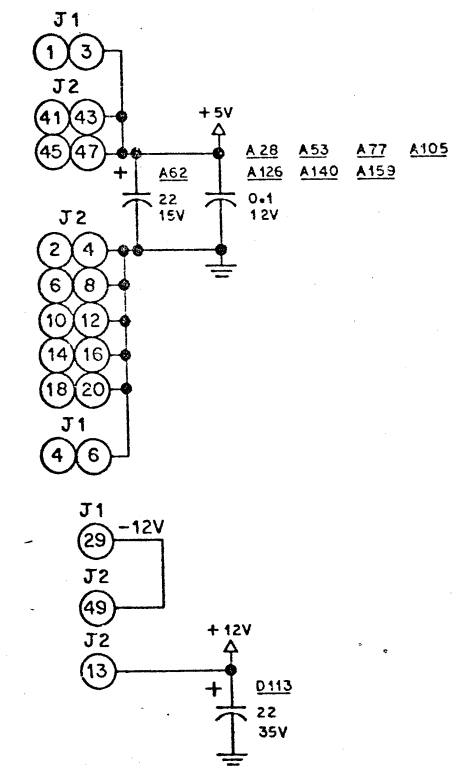
PERIOD = 100ms FOR 23414-01  
 PERIOD = 10ms FOR 23414-02

SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 PW ASSY, RG KEY  
 23400





- NOTES: UNLESS OTHERWISE SPECIFIED
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  2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
  3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
  4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
- △ 5 ALL LIGHT EMITTING DIODES ARE MV 5753.
- △ 6 23632-02 SHOWN ON 23632-01 AND 23632-03, IC'S A30 A47 A155 AND ASSOCIATED RESISTORS, LED'S AND SWITCHES ARE OMITTED.
- △ 7 ON 23632-01 AND 23632-02 THE BUZZER IS CONNECTED TO + 12V; ON 23632-03 AND 23632-04 THE BUZZER IS CONNECTED TO + 5V.

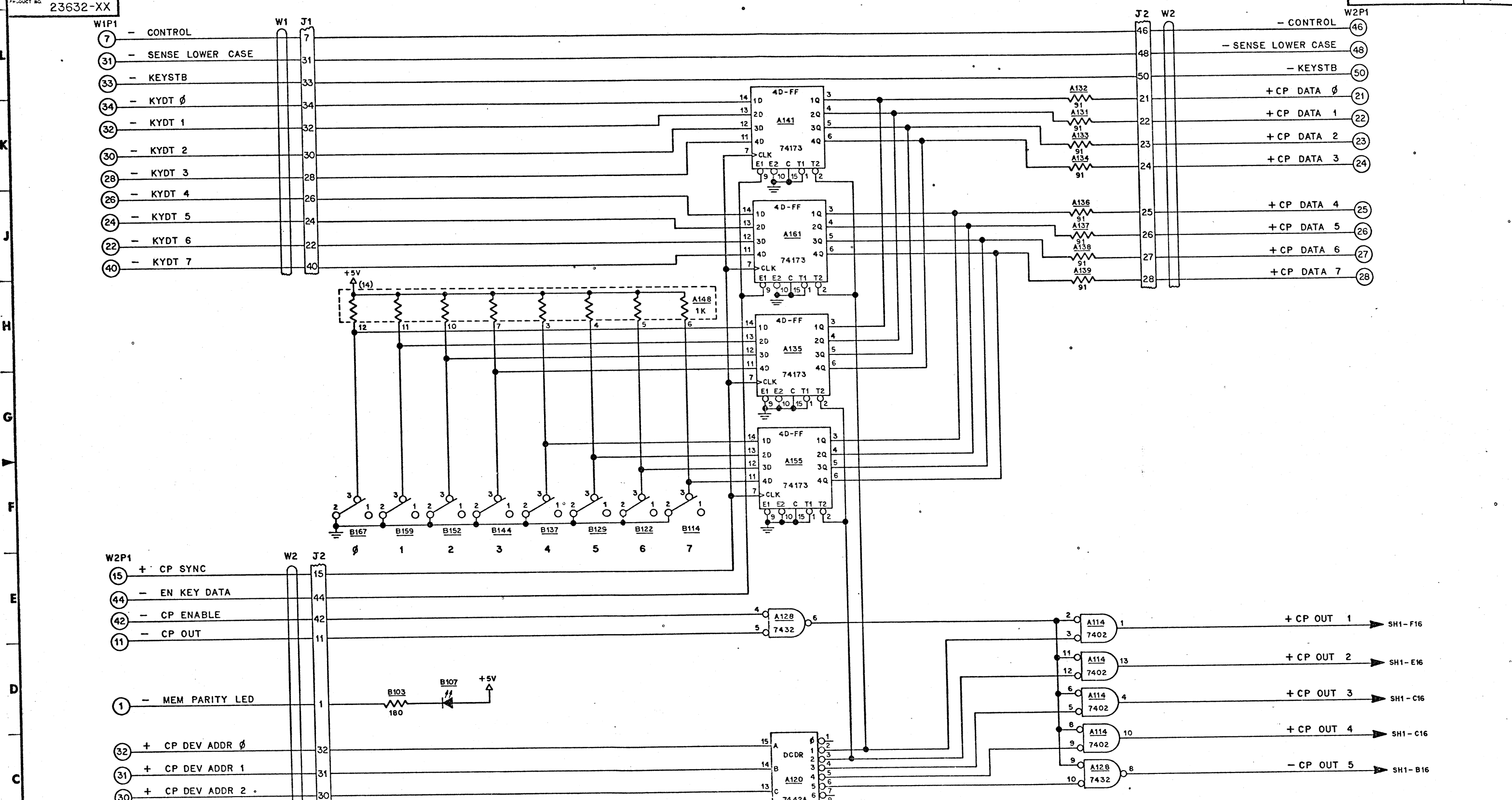


SCHEMATIC DIAGRAM

Diblo Systems Incorporated

PW ASSY, RGCPN

23400



SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
Hayward, California 94545

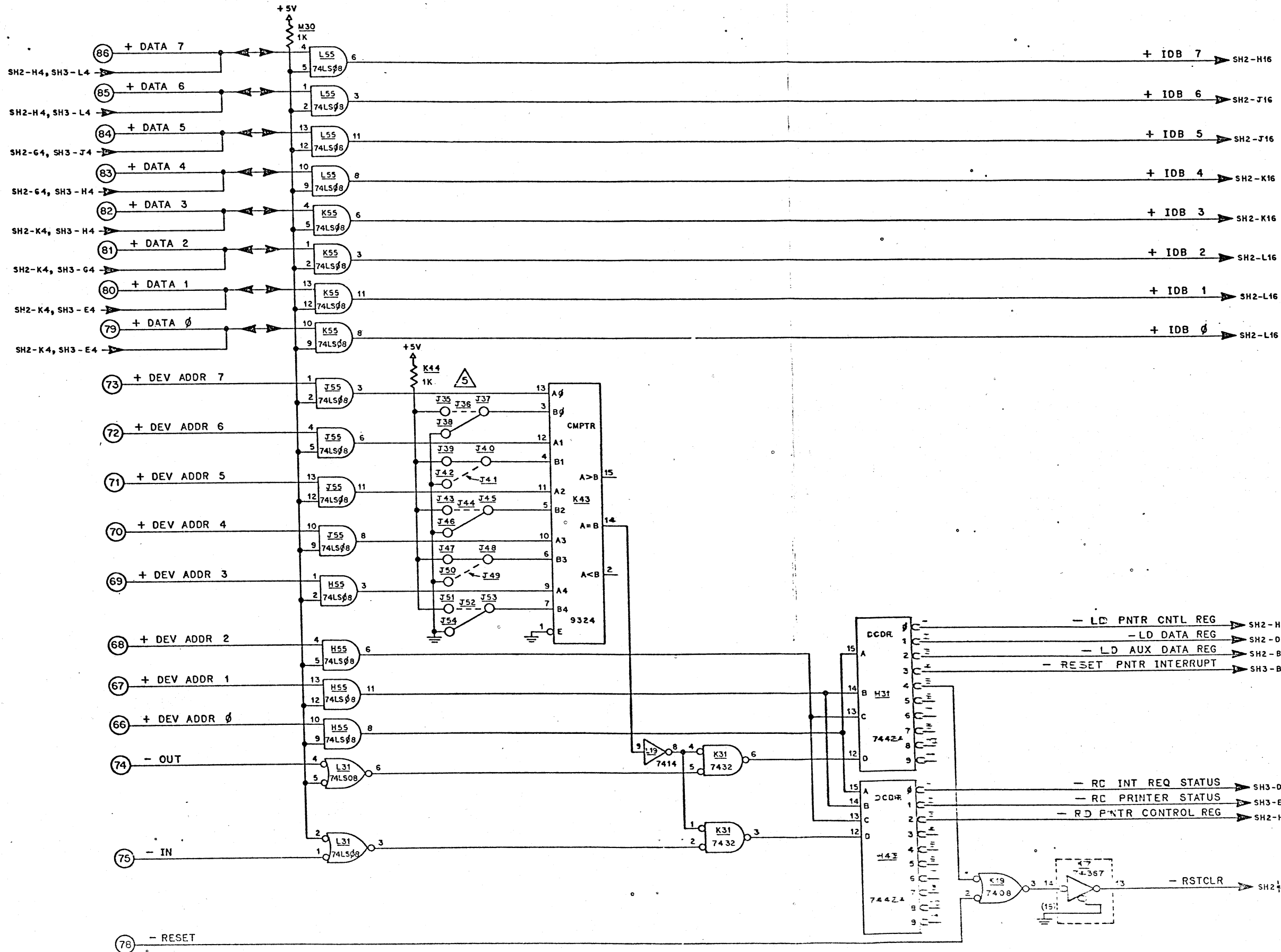
TITLE PW ASSY RGCPN

MODEL 23400

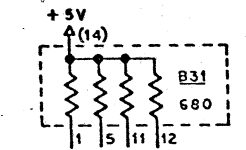
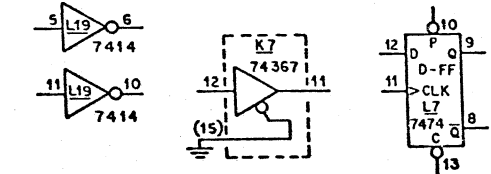
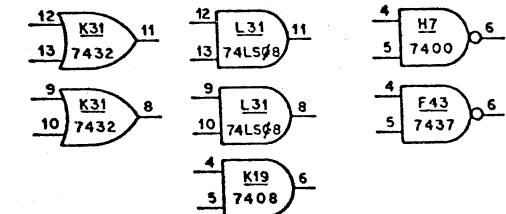
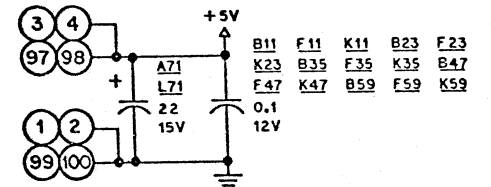
DATE 3-17-76

REV 1 2 2 11

23632-XX

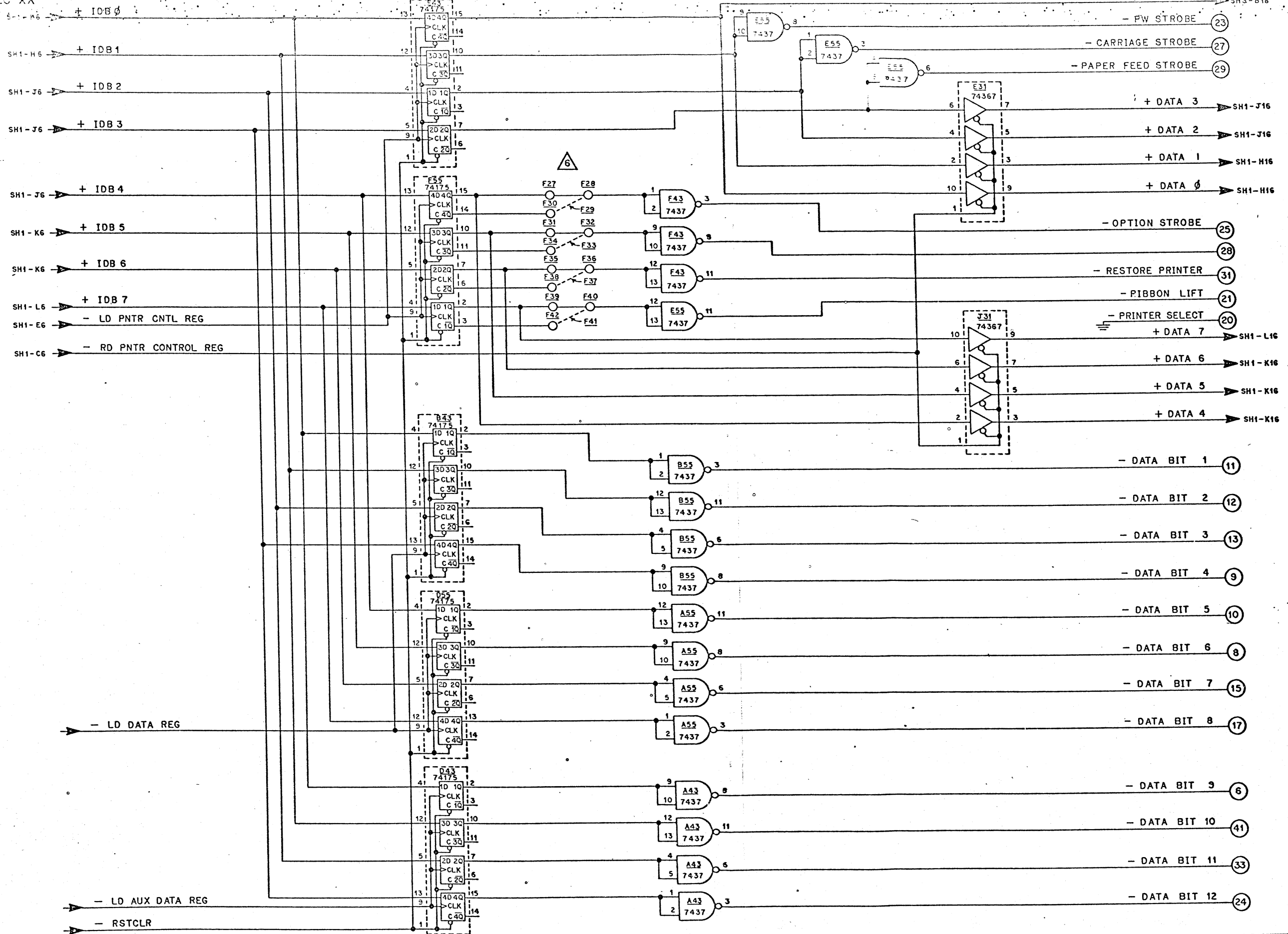


- NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
  2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
  3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
  4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
- △ 5 STRAPS DEFINE DEVICE ADDRESS 5.
- △ 6 23420-01 SHOWN. THE POLARITY OF THE STATUS AND CONTROL LINES IS STRAPABLE DEPENDING ON THE INTERFACE REQUIREMENTS. STATUS AND CONTROL SIGNALS ARE FOR THE H<sub>y</sub> TYPE II PRINTER.
- △ 7 ACKNOWLEDGE AND REQUEST SIGNALS ARE STRAPABLE TO OTHER INTERRUPT LEVELS.



SCHEMATIC DIAGRAM  
Diablo Systems Incorporp  
PW ASSY, RG PNT  
23400  
23420-XX





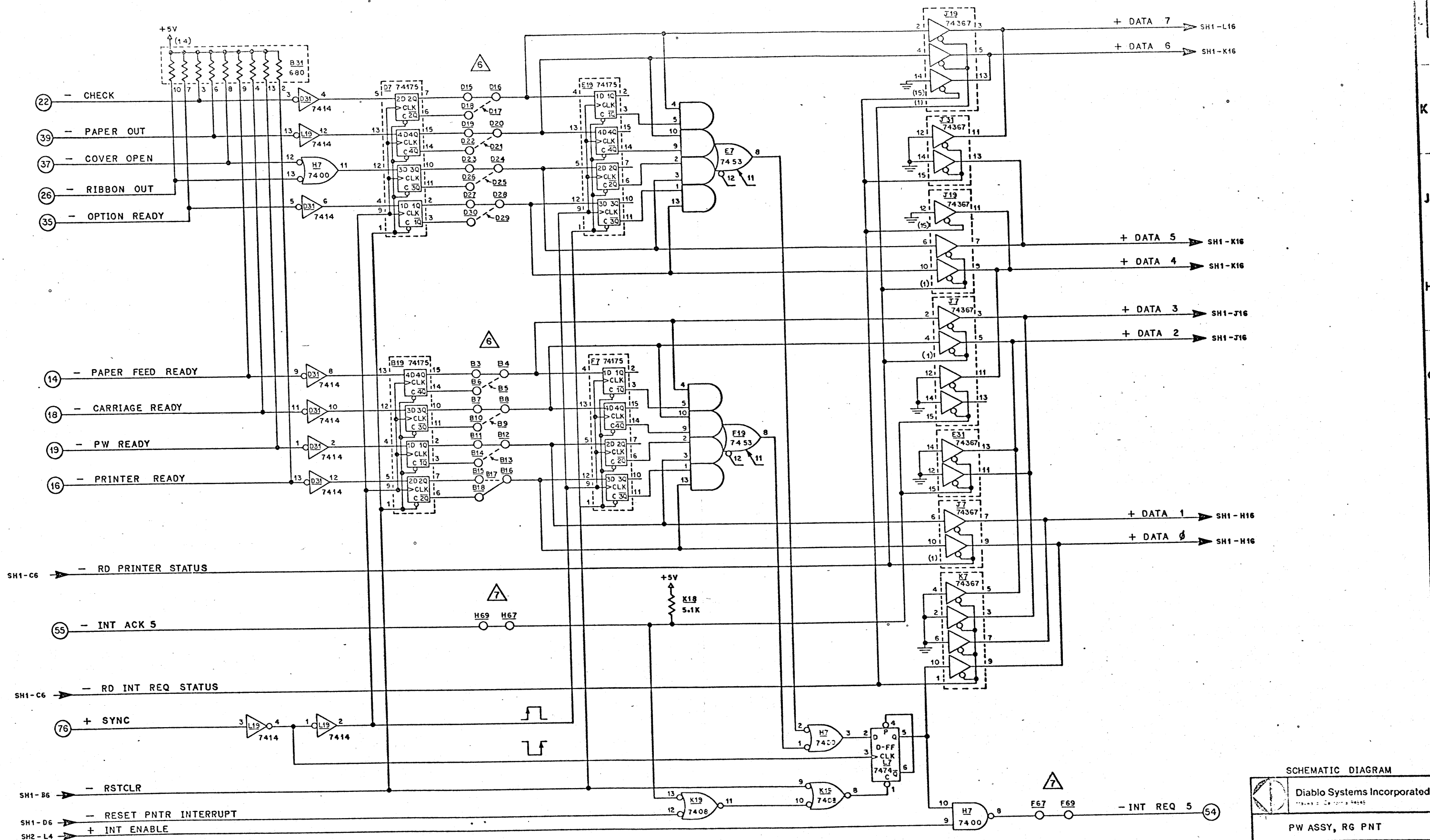
SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
 17000 California 94545

PW ASSY, RG PNT

MODEL 23400

SHEET TOTAL SHEETS 28 PRODUCT NO 23420-XX A1



SCHMATIC DIAGRAM

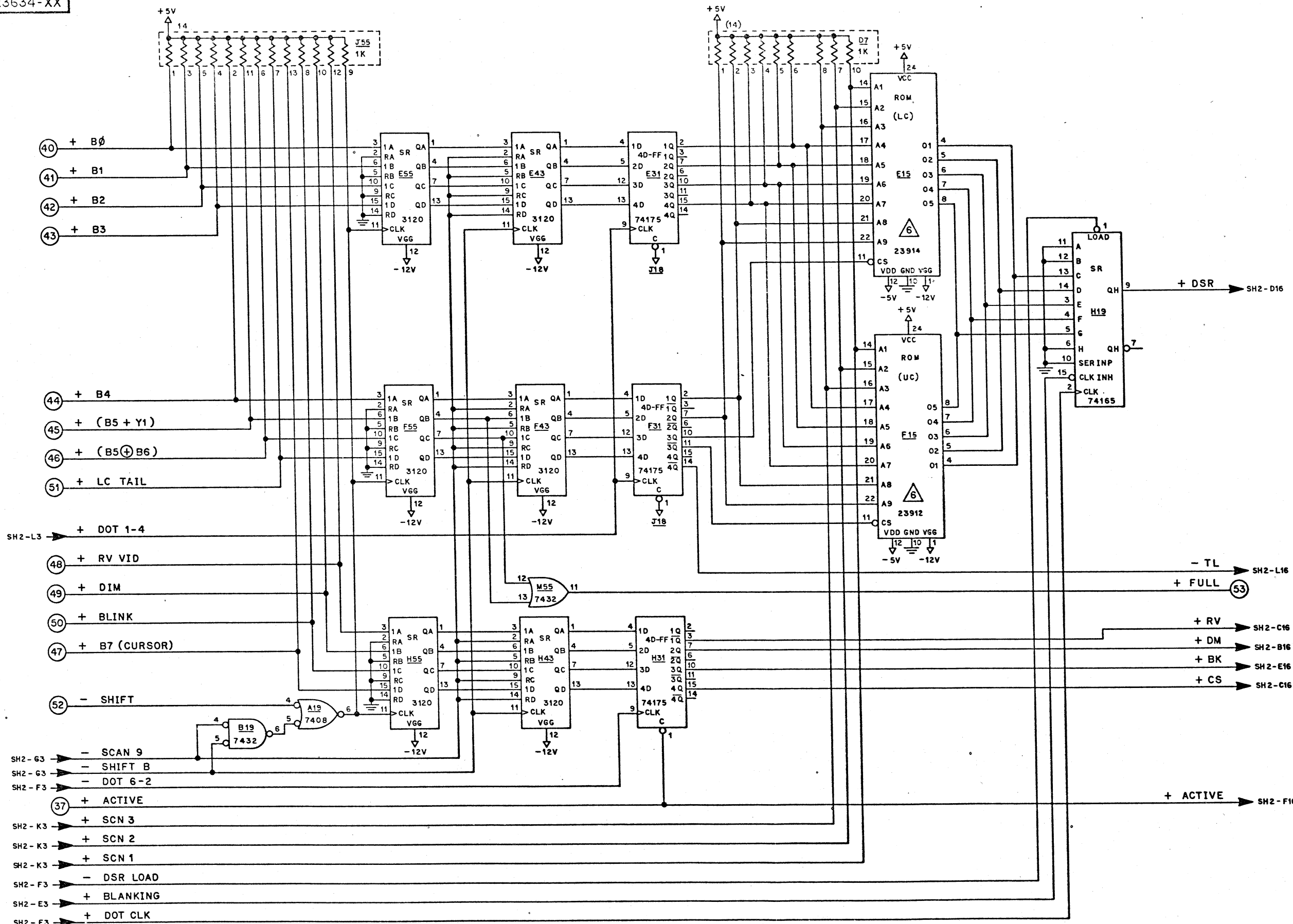
Diablo Systems Incorporated  
 10000 S. De Anza Blvd., Cupertino, CA 95014

PW ASSY, RG PNT

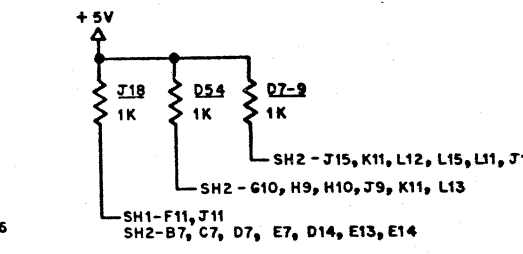
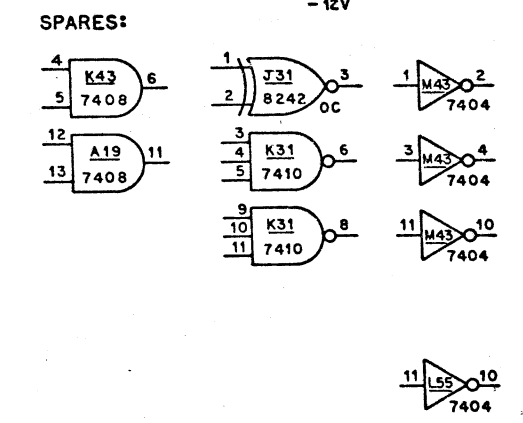
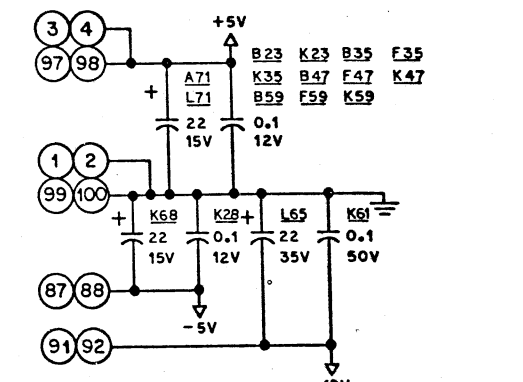
WORK: 23400

DATE: 7-14-76

23420-XX A1



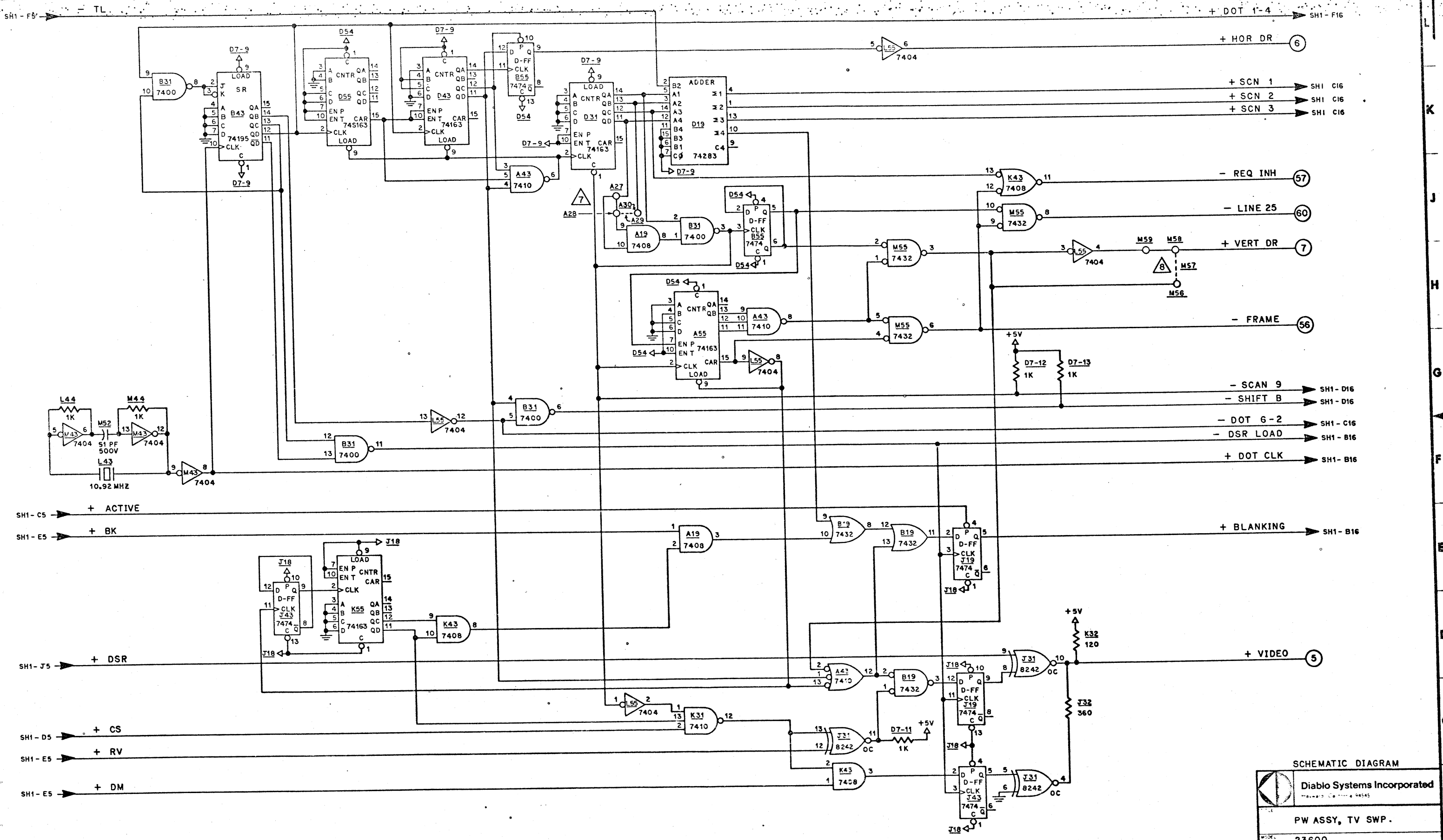
- NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
  2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
  3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
  4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
  5. 23636-01 SHOWN.
- ⚠ 6 MASKED ROM CHARACTER-GENERATOR: UPPER CASE 23912, LOWER CASE 23914.
- ⚠ 7 ON 23636-02 (FOR 50HZ OPERATION), JUMPER A29 IS INSTALLED AND THE TRACE BETWEEN A27 AND A28 IS CUT.
- ⚠ 8 FOR NEGATIVE VERTICAL DRIVE, CUT CONDUCTOR BETWEEN M58 & M59 AND INSTALL JUMPER IN LOCATION M57.



SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
 PW ASSY, TV SWP  
 MODEL: 23600





**SCHEMATIC DIAGRAM**

**Diablo Systems Incorporated**  
TRADEMARK © 1974 94545

**PW ASSY, TV SWP.**

MODEL: 23600

DATE: 6-30-76

SHEET: 8 D

PRODUCT NO: 23634-XX

23636-XX

23636-XX D2

SH4-J5 → + D7  
 SH4-J5 → + D6  
 SH4-J5 → + D5  
 SH4-J5 → + D4

SH4-K5 → + D3  
 SH4-K5 → + D2  
 SH4-L5 → + D1  
 SH4-L5 → + D0

SH4-E5 → - TAR LOAD

56 - FRAME

SH4-C5 → + TV ACK

SH3-D3 → + CR CODE

SH2-L3 → + X CLK

SH4-B5 → - CLOCK 03

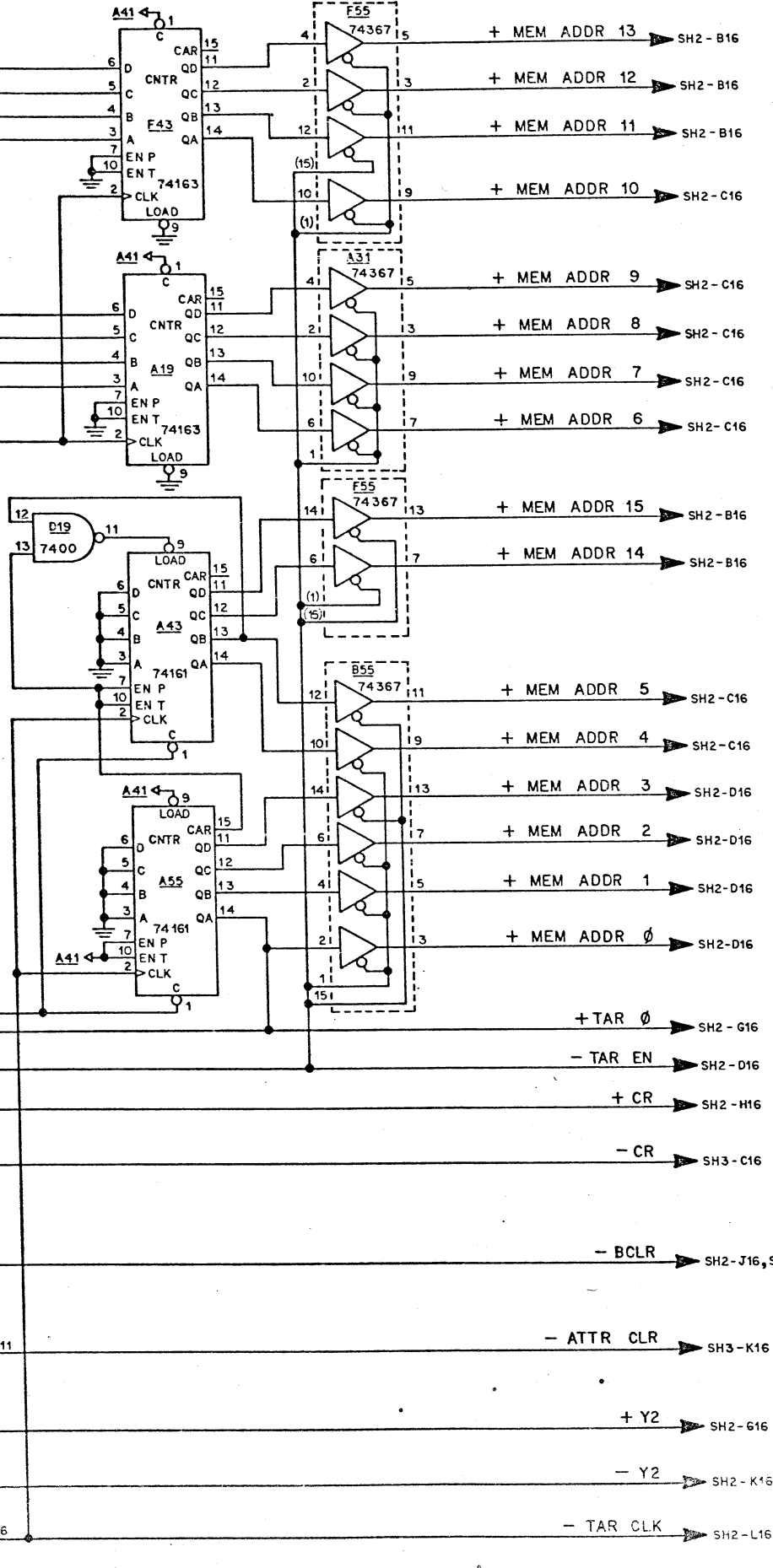
53 + FULL

SH4-B5 → - DMA RD CLK

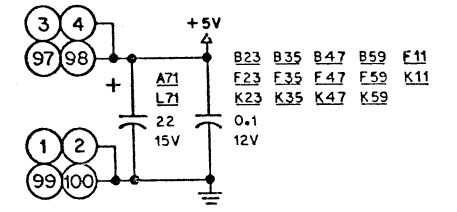
SH2-L3 → - X SHIFT

SH4-C5 → + RD CLK

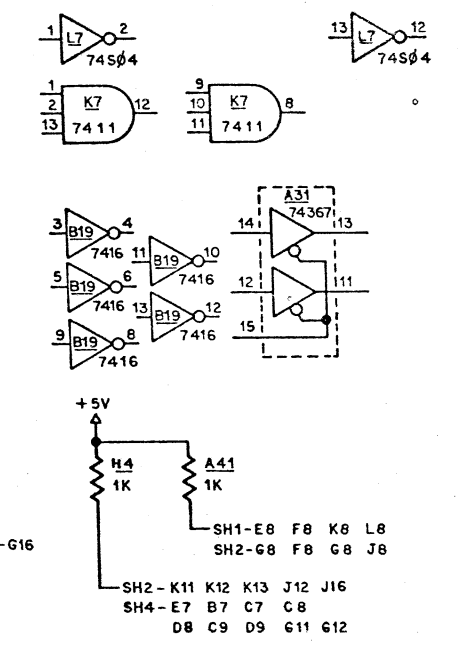
TABLE ADDRESS LOGIC



- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.  
 4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;  
 +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.  
 5. 23636-01 SHOWN.



SPARES:

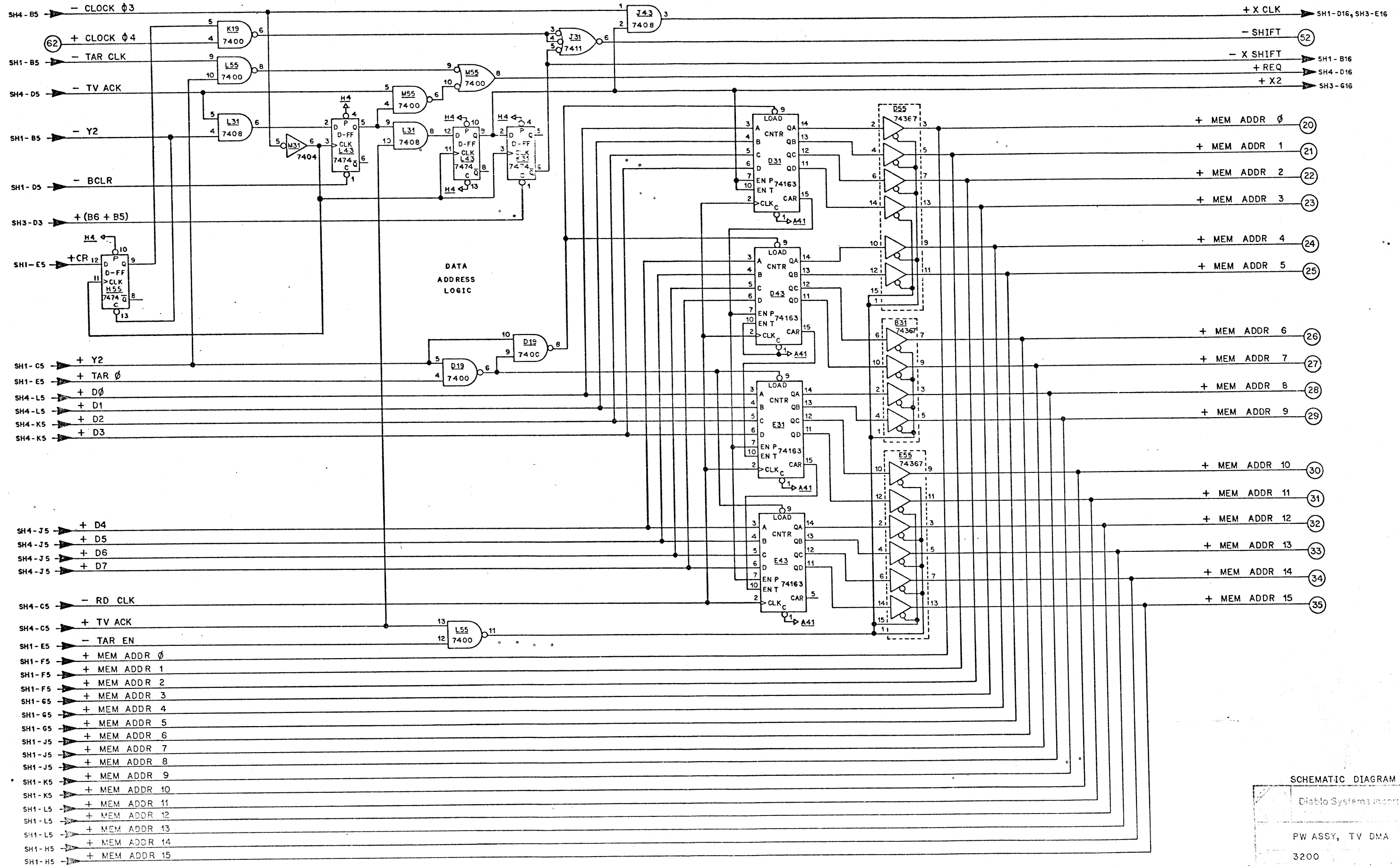


23636-XX

23636-XX

SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 PW ASSY, TV DMA  
 3200

8-11-76



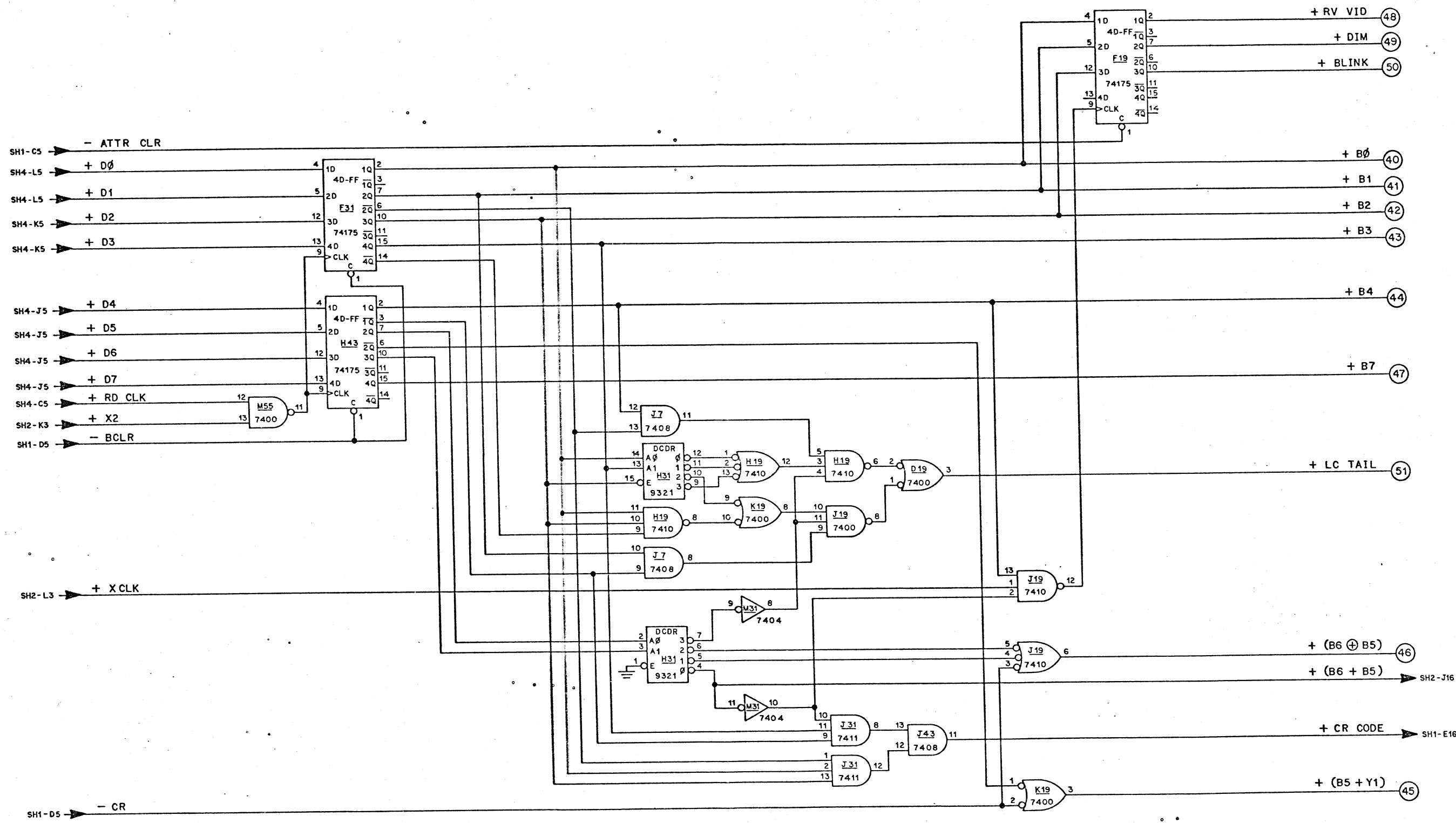
SCHMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, TV DMA

3200





SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
 PW ASSY, TV DMA  
 3200

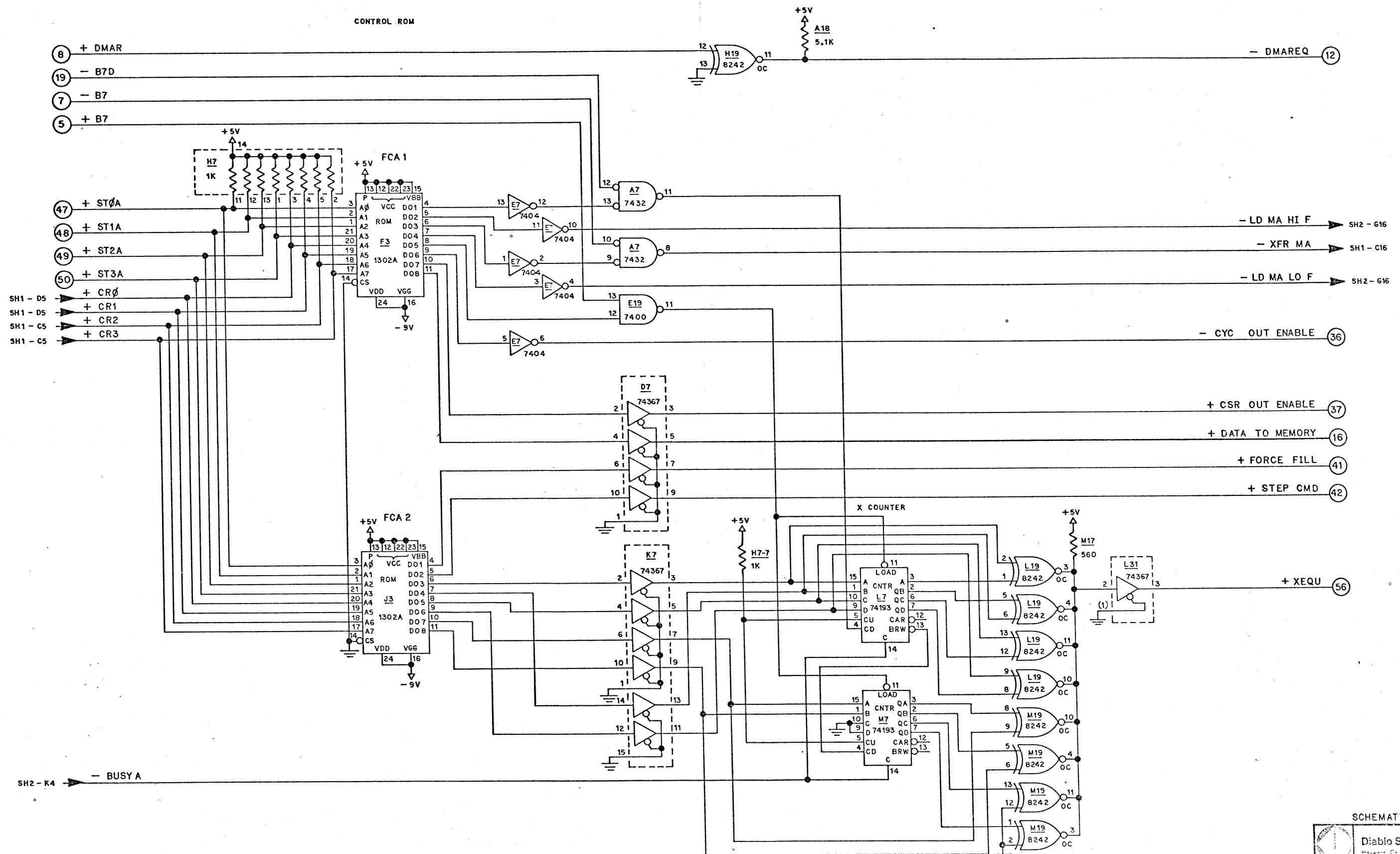








CONTROL ROM



**SCHEMATIC DIAGRAM**

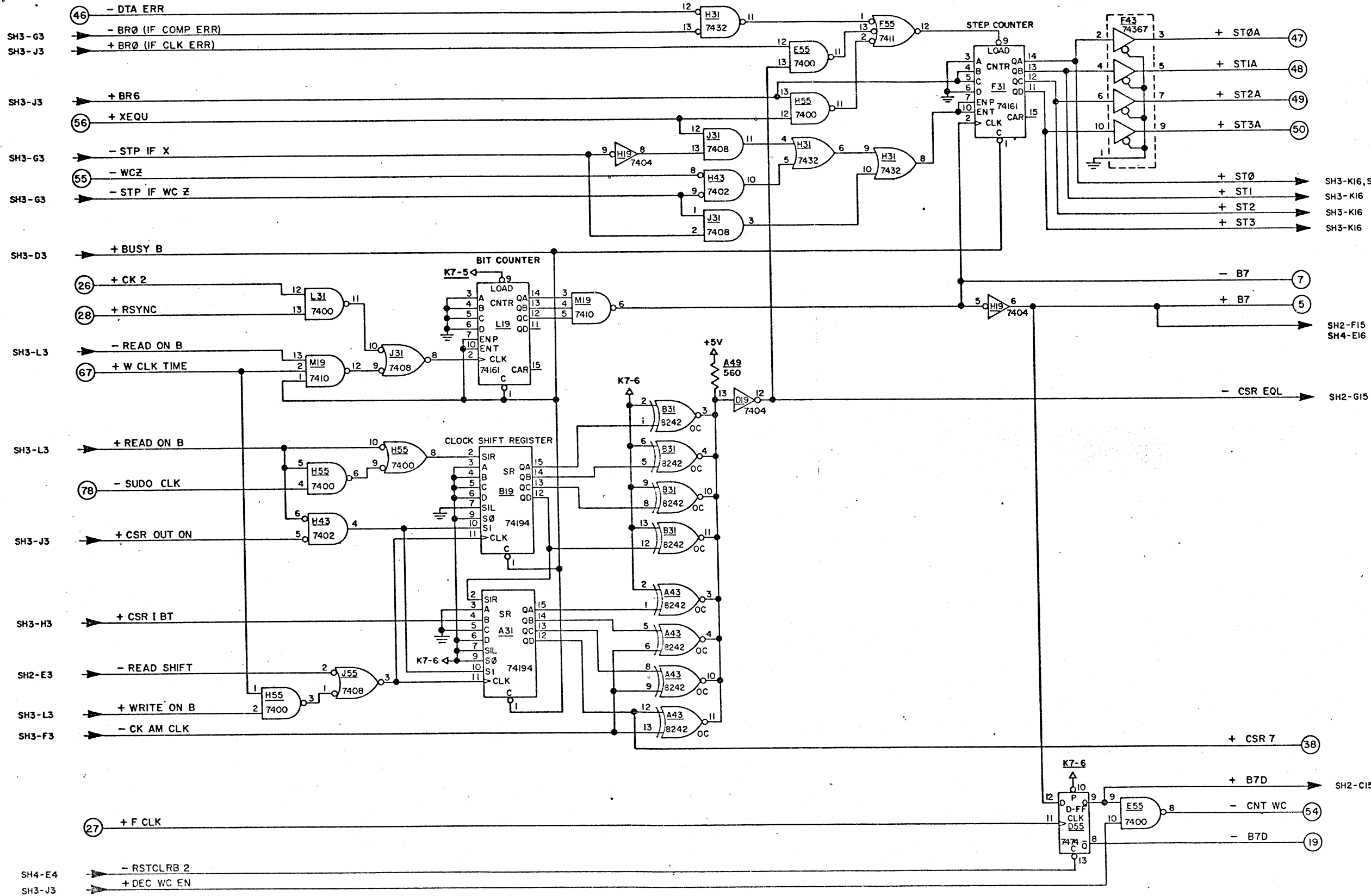
Diablo Systems Incorporated  
Hayward, California 94545

**PW ASSY, RG FCA**

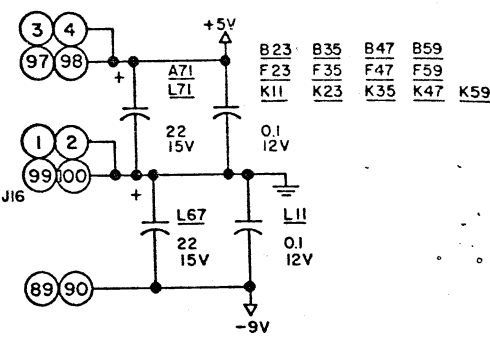
MODEL 23400

DATE 7-3-75

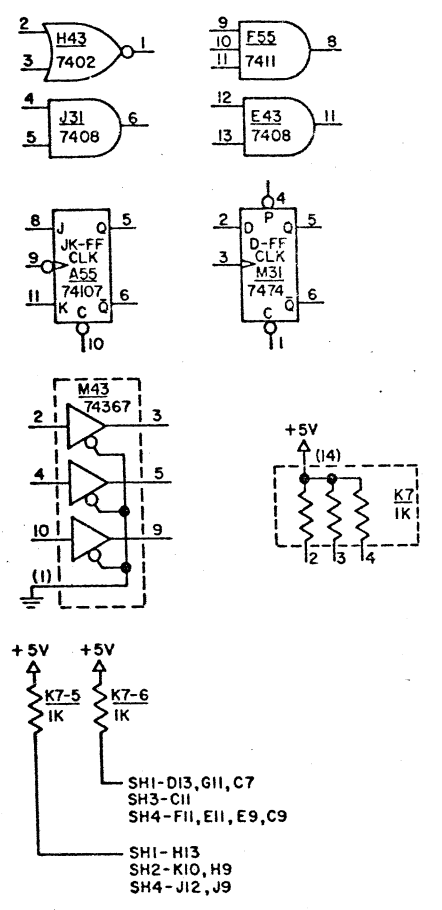
PRODUCT NO 23406-XX



- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.  
 4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;  
 +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.  
 5. 23408-01 SHOWN.

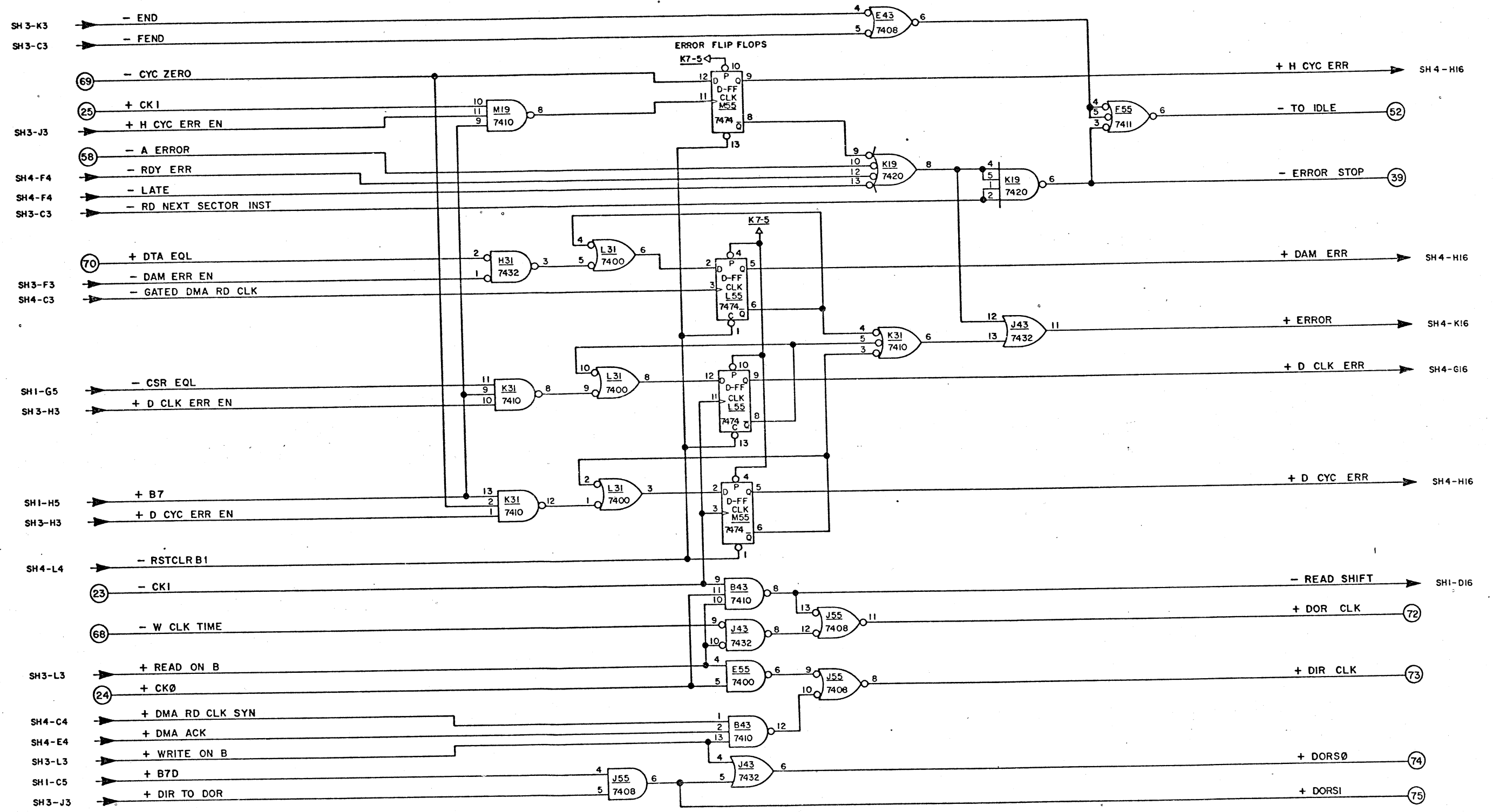


SPARES:



SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
 PW ASSY, RGFCB  
 MODEL 23400  
 23408-XX



SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 P W ASSY, RGFCB  
 23400

PRODUCT NO 23408-XX

PRODUCT NO 23408-XX

K

J

H

G

F

E

D

C

28

SHI-J5  
SHI-J5  
SHI-J5  
SHI-J5

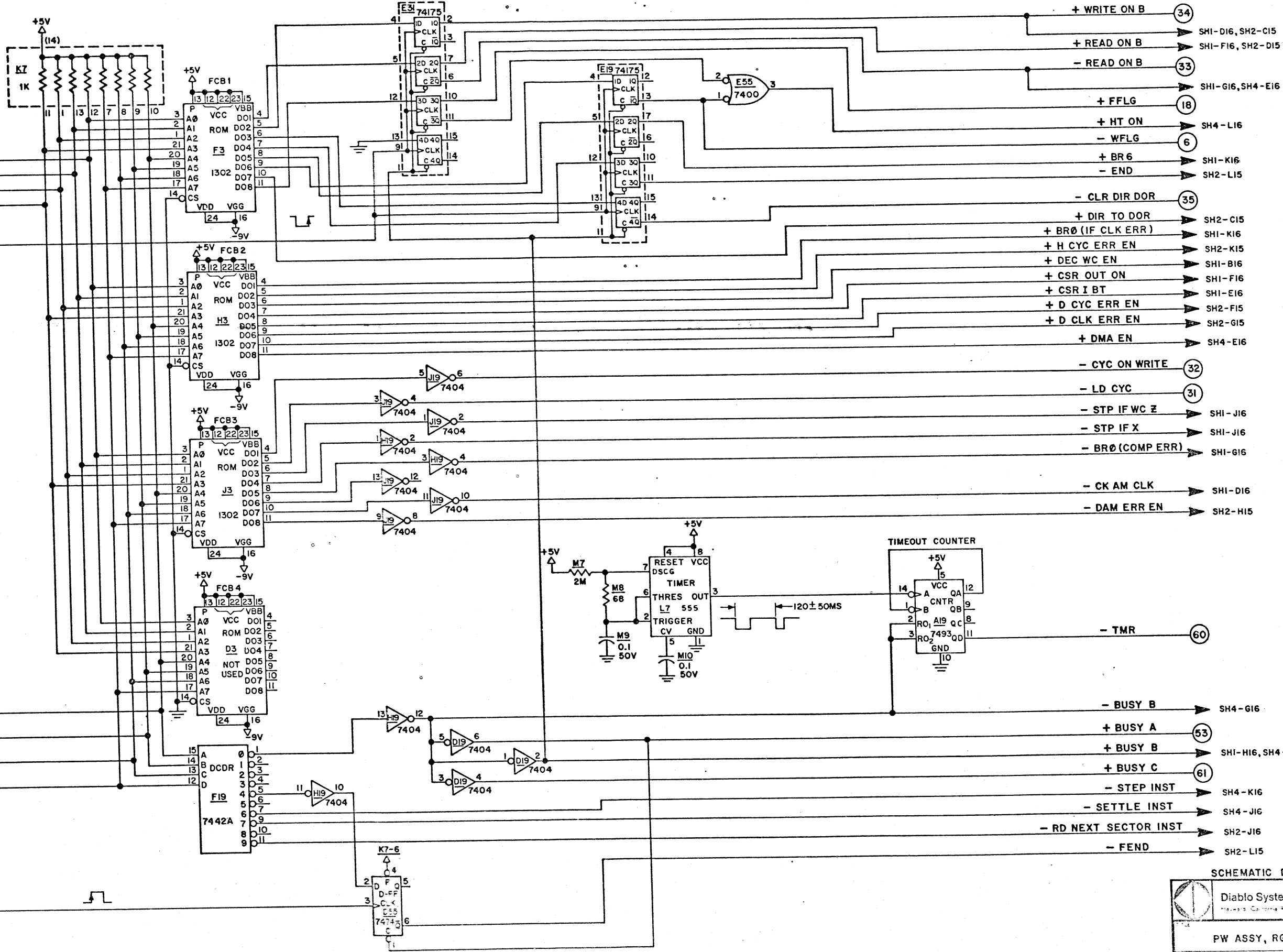
+ ST0  
+ ST1  
+ ST2  
+ ST3

(71) - WRITE DATA PHASE

(43) + CR0  
(44) + CR1  
(45) + CR2  
(51) + CR3

(57) + SELECTED INDEX

+ WRITE ON B (34)  
+ READ ON B (32)  
- READ ON B (33)  
+ FFLG (18)  
+ HT ON (6)  
- WFLG (6)  
+ BR6 (6)  
- END (6)  
- CLR DIR DOR (35)  
+ DIR TO DOR (35)  
+ BR0 (IF CLK ERR) (35)  
+ H CYC ERR EN (35)  
+ DEC WC EN (35)  
+ CSR OUT ON (35)  
+ CSR I BT (35)  
+ D CYC ERR EN (35)  
+ D CLK ERR EN (35)  
+ DMA EN (35)  
- CYC ON WRITE (32)  
- LD CYC (31)  
- STP IF WC Z (31)  
- STP IF X (31)  
- BR0 (COMP ERR) (31)  
- CK AM CLK (31)  
- DAM ERR EN (31)  
- TMR (60)  
- BUSY B (53)  
+ BUSY A (53)  
+ BUSY B (61)  
+ BUSY C (61)  
- STEP INST (61)  
- SETTLE INST (61)  
- RD NEXT SECTOR INST (61)  
- FEND (61)

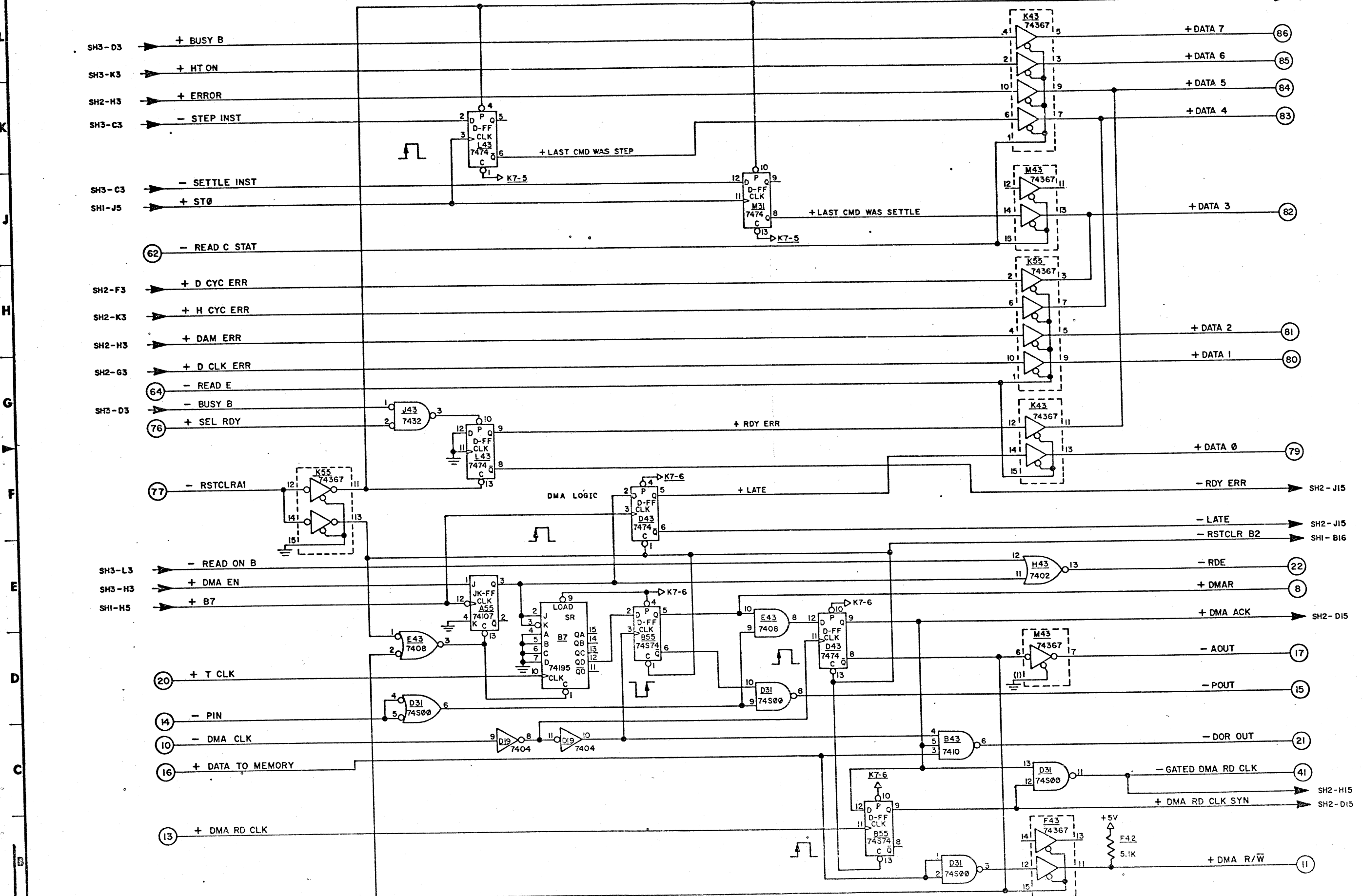


SCHEMATIC DIAGRAM

Diablo Systems Incorporated  
 PW ASSY, RGFCB  
 23400  
 23408-XX



23408-XX



**SCHEMATIC DIAGRAM**

Diablo Systems Incorporated  
Hawes - Corona 94545

PW ASSY, RGFCB

MODEL 23400

REV. 12-10-75

PRODUCT NO 23408-XX

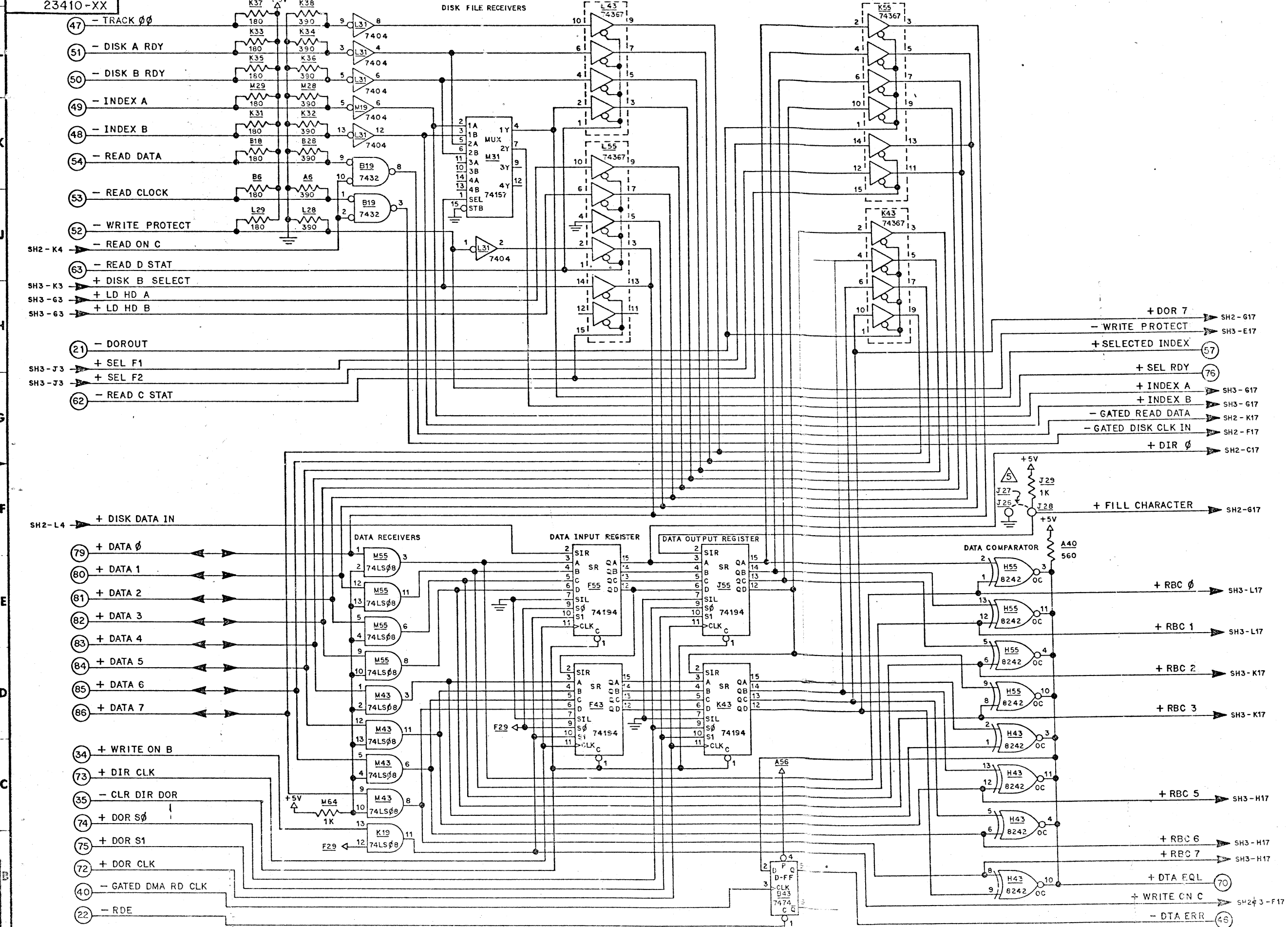
DATE 12-10-75

BY 4

4 12

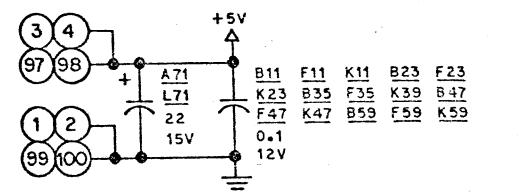
29

23408-XX

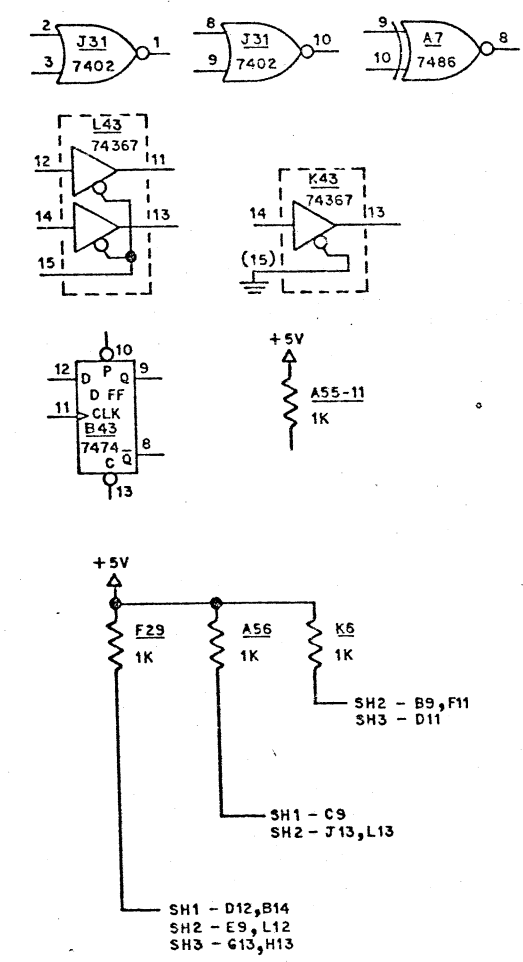


- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.  
 4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;  
 +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;  
 +5V TO PIN 8 OF 8-PIN IC, GND TO PIN 4.

ON 23410-01 FILL CHARACTER IS "FF" WITHOUT JUMPER.  
 ON 23410-02 FILL CHARACTER IS "0" WITH JUMPER.



SPARES:



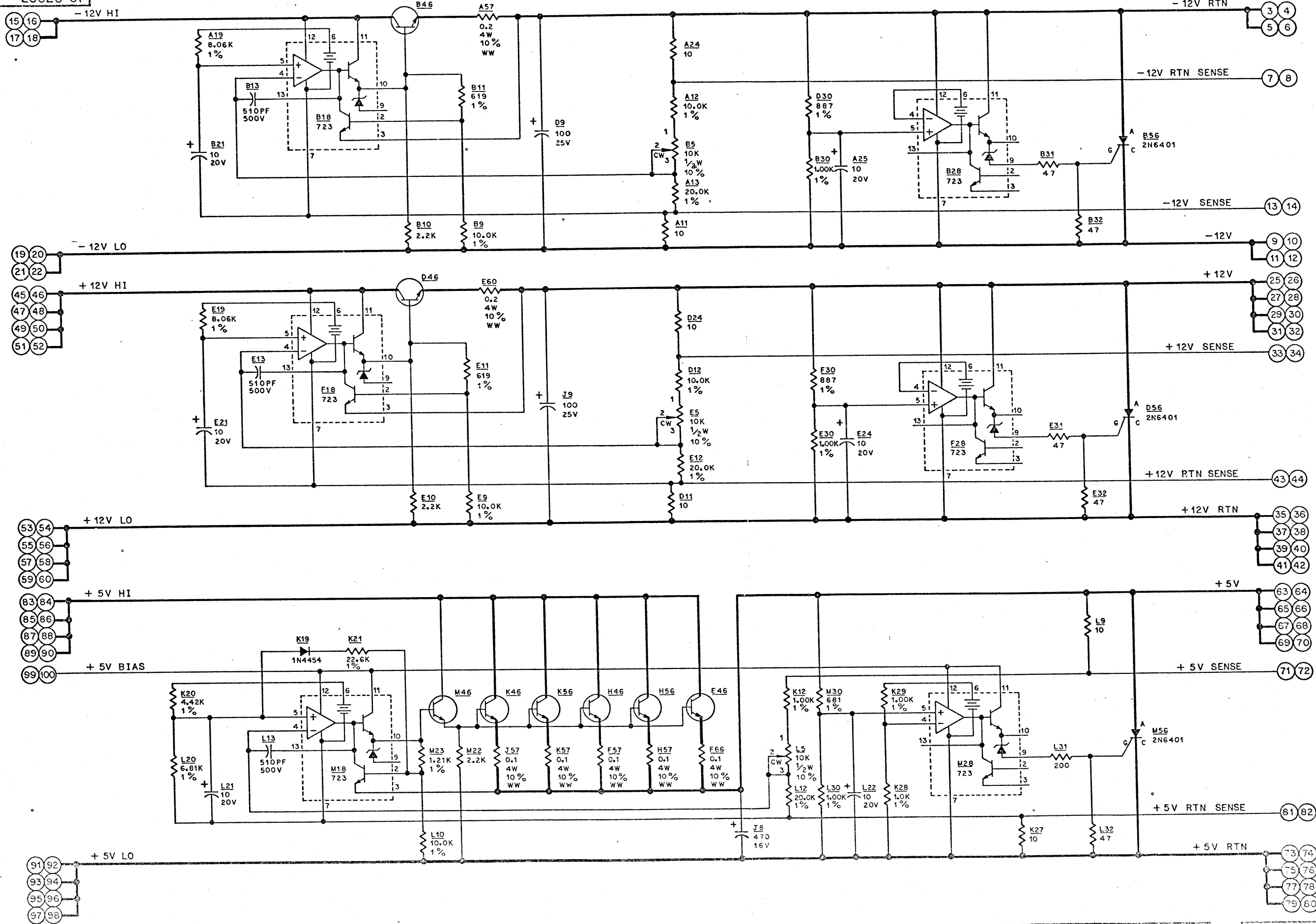






23628-01

23628-01



- NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS
  2. ALL RESISTORS ARE 1/4 WATT, ± 5%
  3. ALL 1% RESISTORS ARE 1/8 WATT.
  4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
  5. ALL TRANSISTORS ARE TIP3055 OR MJE 3055K.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG 12/5

3200

23628-01

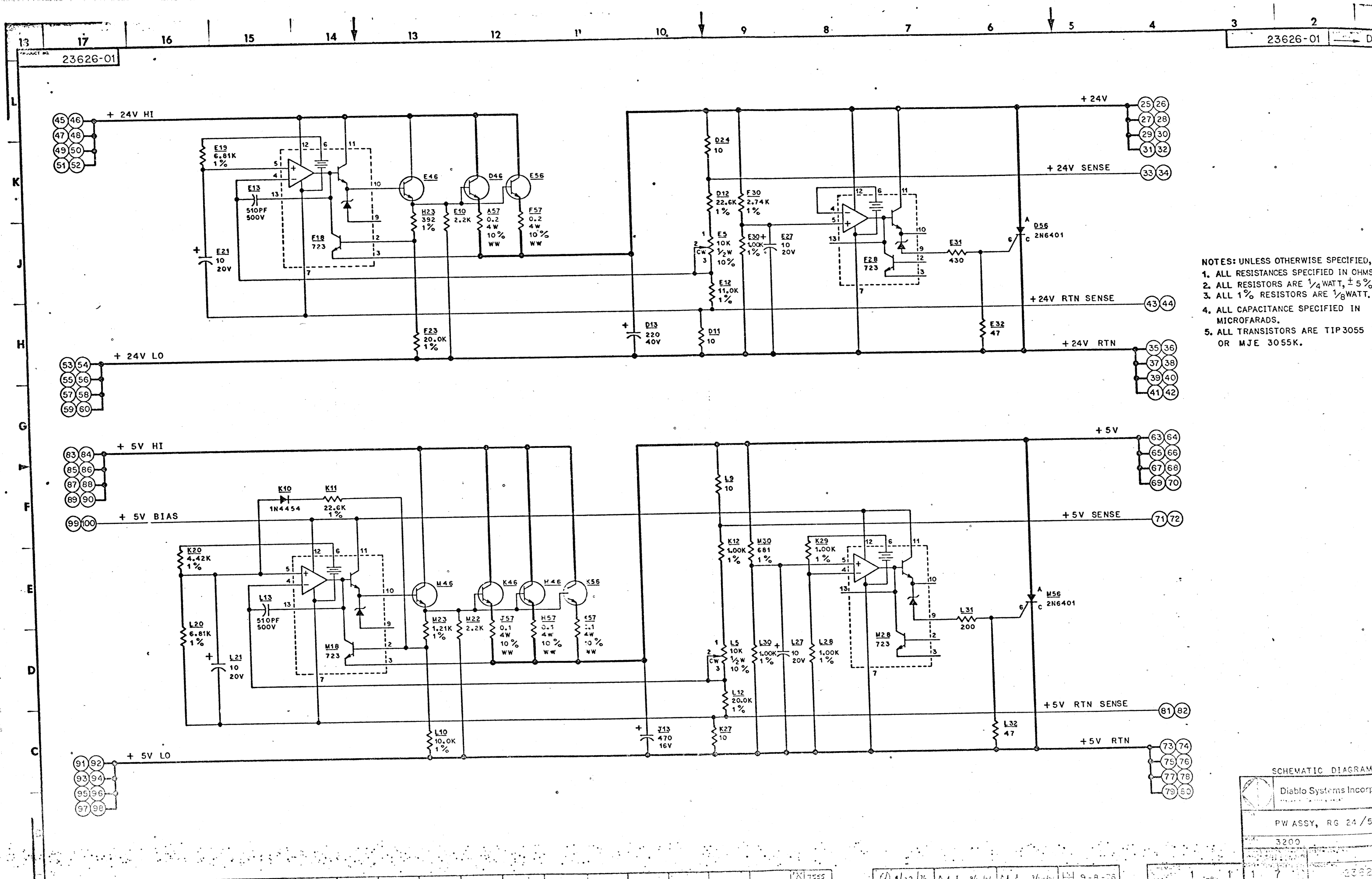
33

23628-01

A 7555 9/18/74

8-26-76

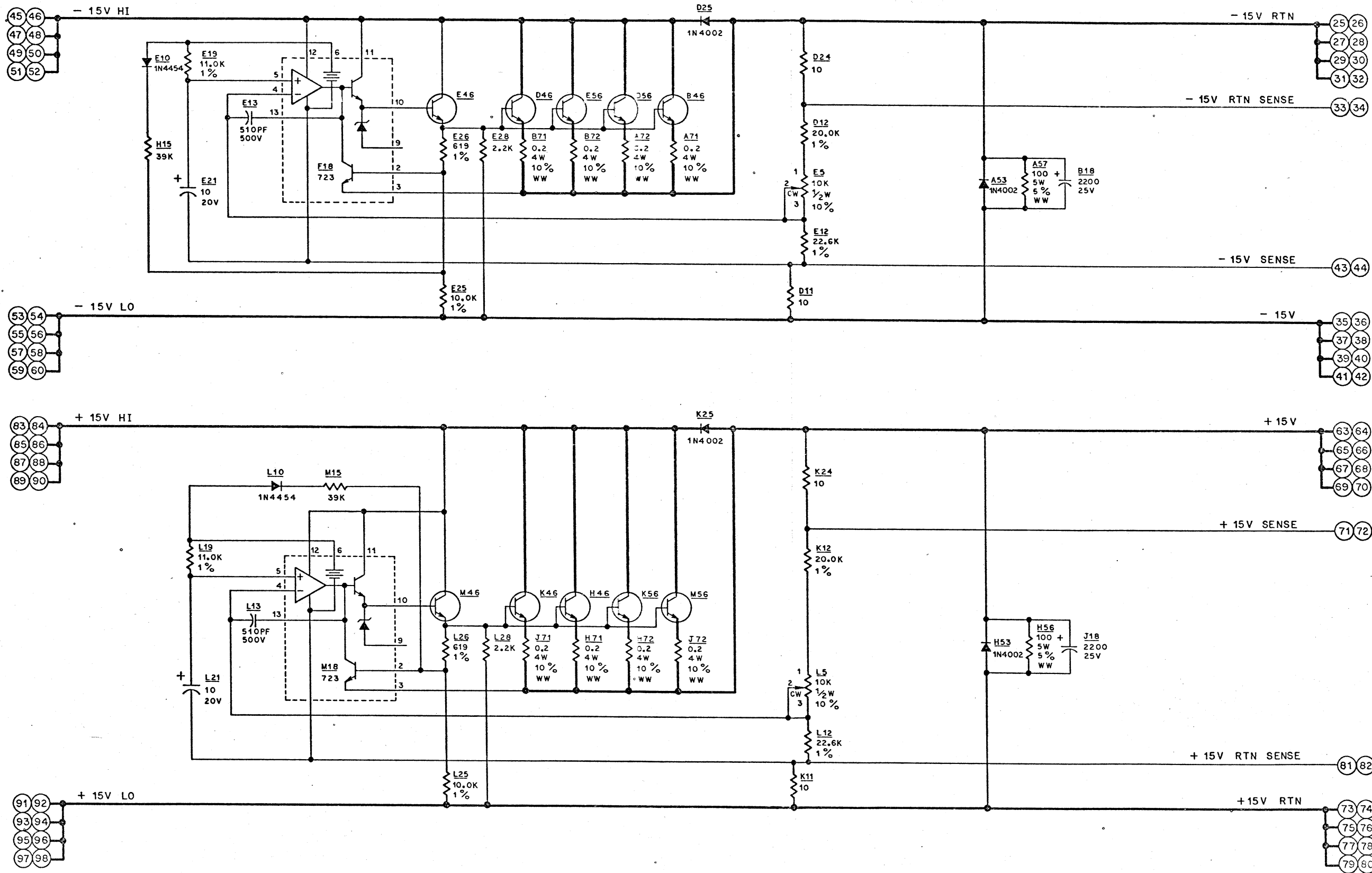
1 1 1 7



- NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
  2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
  3. ALL 1% RESISTORS ARE 1/8 WATT.
  4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
  5. ALL TRANSISTORS ARE TIP3055 OR MJE 3055K.

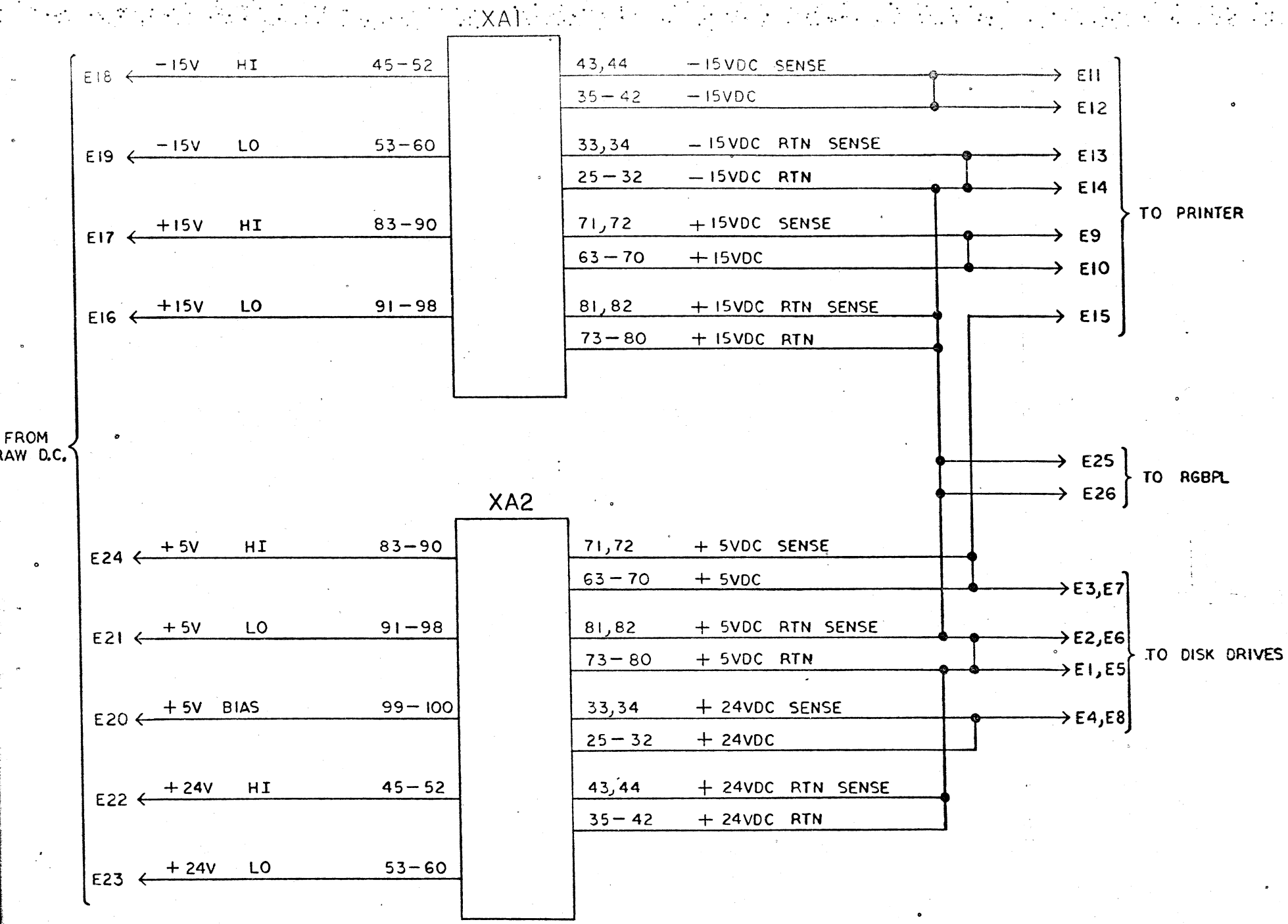
SCHMATIC DIAGRAM  
 Diablo Systems Incorporated  
 PW ASSY, RG 24/5  
 3200  
 23626-01

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- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTANCES SPECIFIED IN OHMS.  
 2. ALL RESISTORS ARE 1/4 WATT, ± 5%.  
 3. ALL 1% RESISTORS ARE 1/8 WATT.  
 4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.  
 5. ALL TRANSISTORS ARE TIP 3055 OR MJE 3055K.

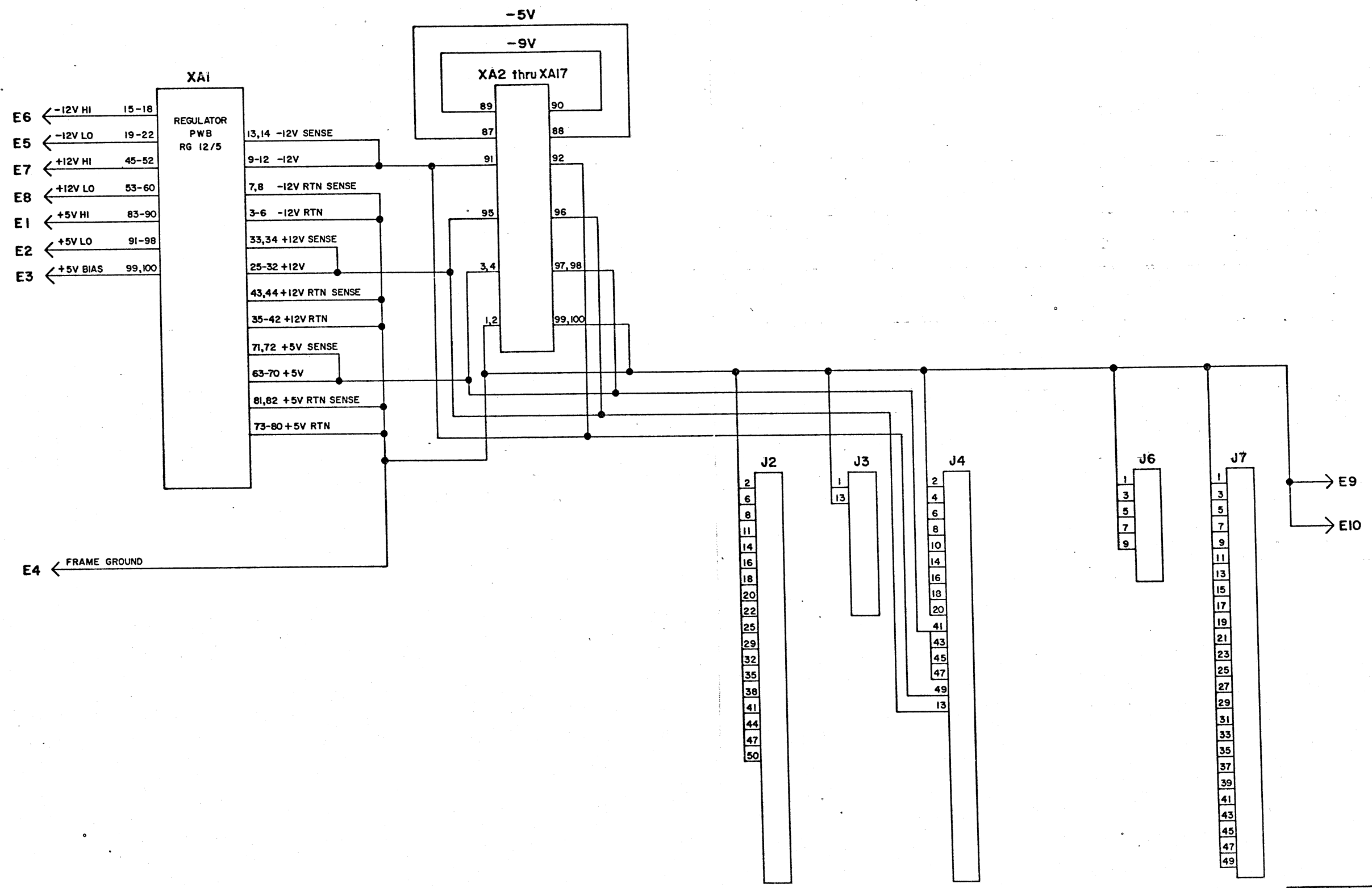
SCHEMATIC DIAGRAM					
Diablo Systems Incorporated					
PW ASSY, RG 15V					
3200					
1	1	1	6	23624-01	



23630

J	K	DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE	DRAWN	DATE	Diablo Systems Incorporated Hayward, California 94545	
G	H		R. MATSUMOTO	3-12-76		
E	F		CHECKED	D. Leach		9/15/76
C	D		MATERIAL	R. Man		9-15-76
A	B		HEAT TREAT	S. FEATER		9/14/76
REVISIONS			FINISH	SCALE		SHEET 1
NEXT ASSY, 23400		FINISH	PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED		SIZE C 23630	





**SCHEMATIC DIAGRAM**

DRAWN ED A.	DATE 4-5-76	Diablo Systems Incorporated Hayward, California 94545
CHECKED A	DATE 9/14/76	
ENGR S. Franke	DATE 11/21/76	
MFG	DATE 10/24/76	
FIRST USED IN EXT ASSY 23400		
SCHEMATIC: RGBPL POWER DISTRIBUTION		
SHEET 1	TOT SHT 14	SIZE D
		DWG NO 23622-XX

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TITLE

SIGNAL LIST, RGBPL

MODEL

3200

DWG NO.

23622-XX

REV

A

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DATE

8/31/76

\* SIGNAL ORIGIN

SIGNAL LIST SHEET

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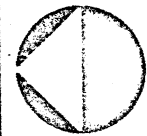
SHEET

4

OF

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SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- A ERROR - A OUT + ACTIVE - AUTO HD UNLD OFF											*55	37	*38	*58 17	58 *17			55	
+ BLINK - BOARD EN/-SEL 0-16K - BOARD EN/-SEL 16-32K - BOARD EN/-SEL 32-48K - BOARD EN/-SEL 48/64K												50	*50						
- BOOT + BOOT - BOOT EN + BUSY A + BUSY C									12 13 *6	6				53	*53 *61	59			*J4-7 *J4-5
+ B0 + B1 + B2 + B3 + B4												40 41 42 43 44	*40 *41 *42 *43 *44						
+ (B5 + Y1) + (B6 @ B5) + B7 + B7 (CURSOR) - B7												45 46 47	*45 *46 *47	5 7	*5 *7	5 6			
- B7D														19	*19				



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TITLE  
SIGNAL LIST, RGBPL

MODEL  
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8/31/76

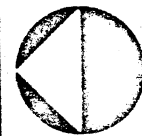
\* SIGNAL ORIGIN

SIGNAL LIST SHEET  
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14

SIGNAL NAME	SPARE XA2	RGPN XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- CARRIAGE READY - CARRIAGE STROBE + CC0 + CC1 - CHECK		18 *27  22							*16 *17	16 17	16 17								*J2-26 J2-17  *J2-12
+ CHIP EN + CK0 + CK1 - CK1 + CK2					53	53	53	53		*53					24 25 23 26	*24 *25 *23 *26			
+ CLOCK 01 + CLOCK 02 + CLOCK 03 + CLOCK 04 + CLR TO SEND	65	65	65	65	65	65	65	65	*43 *65 *61 *62	43 65 61 62	65 61 62	61 62	61 62						*J3-9
- CLR DIR DOR - CNT WC + COMM CLOCK - CONTROL - COVER OPEN		44  37	44						*44					54	*35 *54	35			*J4-46 *J2-5
+ CP BUF DATA 0 + CP BUF DATA 1 + CP BUF DATA 2 + CP BUF DATA 3 + CP BUF DATA 4				*40 *22 *38 *24 *36															J4-33 J4-34 J4-35 J4-36 J4-37
+ CP BUF DATA 5 + CP BUF DATA 6 + CP BUF DATA 7 + CP DATA 0 + CP DATA 1				*34 *32 *30 25 14															J4-38 J4-39 J4-40 *J4-21 *J4-22
+ CP DATA 2 + CP DATA 3 + CP DATA 4 + CP DATA 5 + CP DATA 6				23 12 21 10 19															*J4-23 *J4-24 *J4-25 *J4-26 *J4-27
+ CP DATA 7 + CP DEV ADDR 0 + CP DEV ADDR 1 + CP DEV ADDR 2 + CP DEV ADDR 3				16 *20 *15 *18 *17															*J4-28 J4-32 J4-31 J4-30 J4-29



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SIGNAL LIST SHEET

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\* SIGNAL ORIGIN

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SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
- CP ENABLE - CP OUT - CP RESET + CP SYNC + CR 0				*28 *35 *29 31										*43	43		J4-42 J4-11 J4-17 J4-15
+ CR 1 + CR 2 + CR 3 + CSR OUT ENABLE + CSR 7														*44 *45 *51 *37	44 45 51 37	37 38	
- CYC ON WRITE - CYC OUT ENABLE - CYC ZERO														*36	*32 36 69	32 36 *69	
+ DATA 0 + DATA 1 + DATA 2 + DATA 3 + DATA 4	79 80 81 82 83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83	79 80 81 82 83	79 80 81 82 83	79 80 *81 *82 *83	*79 *80 *81 *82 *83	*79 *80 *81 *82 *83		
+ DATA 5 + DATA 6 + DATA 7 + DATA 8 - DATA BIT 1	84 85 86	*84 *85 *86	*84 *85 *86	*84 *85 *86	*84 *85 *86 *77	*84 *85 *86 *77	*84 *85 *86 *77	*84 *85 *86 *77	*84 *85 *86 77	*84 *85 *86 *77	84 85 86	84 85 86	*84 *85 *86	*84 *85 *86	*84 *85 *86		J2-37
- DATA BIT 2 - DATA BIT 3 - DATA BIT 4 - DATA BIT 5 - DATA BIT 6		*12 *13 *9 *10 *8															J2-36 J2-39 J2-33 J2-40 J2-41
- DATA BIT 7 - DATA BIT 8 - DATA BIT 9 - DATA BIT 10		*15 *17 *6 *41															J2-42 J2-43 J2-46 J2-47



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SIGNAL LIST SHEET

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SHEET

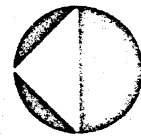
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OF

14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
- DATA BIT 11 - DATA BIT 12 + DATA SET READY + DATA TERM RDY + DATA TO MEMORY		*33 *24	15 *12											*16	16		J2-9 *J2-10 *J3-11 J3-14
+ DEV ADDR 0 + DEV ADDR 1 + DEV ADDR 2 + DEV ADDR 3 + DEV ADDR 4	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	*66 *67 *68 *69 *70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70	66 67 68 69 70				
+ DEV ADDR 5 + DEV ADDR 6 + DEV ADDR 7 - DEV EN + DIM	71 72 73	71 72 73	71 72 73	71 72 73	71 72 73	71 72 73	71 72 73	71 72 73	*71 *72 *73 *63	71 72 73 63	71 72 73	71 72 73	71 72 73	71 72 73			
+ DIR CLK - DISK A RDY - DISK B RDY - DISK 8 SELECT - DMA CLK										*9	9	9	9	10	10	*73 73 51 50 *9	*J2-26 *J2-28 J2-42
- DMA EN + DMAR + DMA RD CLK - DMA REQ - DMA P OUT (-PIN)									10	*10	10			8 13 12 *12	*8 13 12 14		
- DMA P IN (-TV P) + DMA R/W + DOR CLK - DOR OUT + DOR S0									*11	15 11	14/15 11	11	*14 *11	11	*11 *72 *21 *74	72 21 74	
+ DOR S1 + DTA EQL - DTA ERR														46	*75 70 46	75 *70 *46	





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SIGNAL LIST, RGBPL  
DRAWN R. MATSUMOTO DATE 8/31/76  
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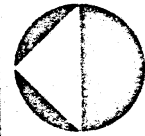
MODEL  
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23622-XX

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SHEET 8 OF 14

SIGNAL LIST SHEET  
5 OF 11

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
- EN KEY DATA - ERROR STOP				*26											*39	39	J4-44
+ F CLK - FDK P (-P OUT) + FFLG + FORCE FILL - FRAME													15 *56	18 *41	27 *15 *18	*27 41	
+ FULL												*53	53				
- GATED DMA RD CLK														40	*41	40	
+ HOR DR												*6					J6-2



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SIGNAL LIST, RGBPL

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\* SIGNAL ORIGIN

SIGNAL LIST SHEET  
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SIGNAL NAME	SPARE XA2	RGPN XA3	RGCOM XA4	RGKEY XA5	MEMØ4 XA6	MEMØ4 XA7	MEMØ4 XA8	MEMØ4 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
- IN - INDEX A - INDEX B - INT ACK Ø - INT ACK 1	75	75	75	75	75	75	75	75	*75 *37 *49	75 37	75	75	75			49 48	*J7-30 *J7-32
- INT ACK 2 - INT ACK 3 - INT ACK 4 - INT ACK 5 - INT ACK 6				57					*53 *57 *49 *55 *51			49	49				
- INT ACK 7 - INT P IN - INT P OUT - INT REQ Ø - INT REQ 1									*46 36 48	*36				46 15 *14			* GND
- INT REQ 2 - INT REQ 3 - INT REQ 4 - INT REQ 5 - INT REQ 6									52 56 58 54 50			58	58				
- INT REQ 7 + I/O EN									38 *45	38 45				*38			
- KY STB				9													*J4-50



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\* SIGNAL ORIGIN

SIGNAL LIST SHEET

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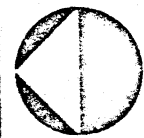
SHEET

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SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17		I/O
+ LC TAIL - LD CYC - LD HD A - LD HD B - LOAD DISK FILE CMD												51	*51		*31	31 *13 *12 61		J7-20 J7-22
- LO WRITE I - LINE 25												*60	60			*45		J7-46
+ MEM ADDR 0 + MEM ADDR 1 + MEM ADDR 2 + MEM ADDR 3 + MEM ADDR 4					20 21 22 23 24	20 21 22 23 24	20 21 22 23 24	20 21 22 23 24	*20 *21 *22 *23 *24	20 21 22 23 24	20 21 22 23 24	20 21 22 23 24	*20 *21 *22 *23 *24					
+ MEM ADDR 5 + MEM ADDR 6 + MEM ADDR 7 + MEM ADDR 8 + MEM ADDR 9					25 26 27 28 29	25 26 27 28 29	25 26 27 28 29	25 26 27 28 29	*25 *26 *27 *28 *29	25 26 27 28 29	25 26 27 28 29	25 26 27 28 29	*25 *26 *27 *28 *29					
+ MEM ADDR 10 + MEM ADDR 11 + MEM ADDR 12 + MEM ADDR 13 + MEM ADDR 14					30 31 32 33 34	30 31 32 33 34	30 31 32 33 34	30 31 32 33 34	*30 *31 *32 *33 *34	30 31 32 33 34	30 31 32 33 34	30 31 32 33 34	*30 *31 *32 *33 *34					
+ MEM ADDR 15 + MEM BUS EN - MEM PARITY LED + MEM SPEED - MEM SPEED					35 19 39	35 19 39	35 19 39	35 19 39	*35 *19 *8 *39	35 *19 8 *39	35	35	*35 *35					J4-1
- NDM RD DATA - NDM RD CLK - NDM XMIT CLK				21 16 18														#J3-5 #J3-3 #J3-4



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SIGNAL LIST, RGBPL

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3200

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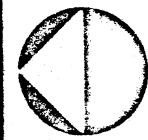
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R. MATSUMOTO

DATE  
8/31/76

SIGNAL LIST SHEET  
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14

SIGNAL NAME	SPARE XA2	RGPN XA3	RGC XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
- OPTION READY - OPTION STROBE - OUT	74	35 *25 74	74	74	74	74	74	74	*74	74	74	74	74	74			*J2-7 J2-19
- PAPER FEED READY - PAPER FEED STROBE - PAPER OUT - P OUT (-FDK P) - PIN (-DMA P OUT)		14 *29 39							*14				15		*15 14		*J2-34 J2-15 *J2-3
- PRINTER READY - PRINTER SELECT - PW READY - PW STROBE		16 *20 19 *23															*J2-28 J2-24 *J2-27 J2-21
+ READ SYNC - RD E - READ C STAT - READ D STAT - READ E														*62 *63 *64	28 *22 62 64	*28 22 62 63	
- READ CLOCK - READ DATA - READ ON B + READY + RECD SIGNAL DET									42	*42					*33	53 54 33	*J7-12 *J7-10  *J3-15
- REQ INH + REQ TO SEND - RESET - RESTORE PRINTER - RFH EN	78	78 *31	*19 78	*78	78	78	78	78	78	78	78	*57 78	57 78				J3-7 J2-13
- RIBBON LIFT - RIBBON OUT		*21 26															J2-23 *J2-4



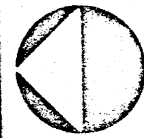
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TITLE SIGNAL LIST, RGBPL				MODEL 3200	DWG NO. 23622-XX	REV. A
DRAWN R. MATSUMOTO		DATE 8/31/76	* SIGNAL ORIGIN		SIGNAL LIST SHEET 9 OF 11	SHEET OF 12 14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
+ RING IND - RST CLR A1 + RUN + R/ $\bar{W}$ + RV VID			29		18	18	18	18	7 18	*7 *18		48	*48	*77	77	77	*J3-18 J4-3
- SEEK DIRECTION IN + SEL RDY - SELECT 1 - SELECT 2 - SELECT 3															76	*7 *76 *15 *16 *17	J7-48 J7-8 J7-6 J7-4
- SELECT 4 - SEL 0-16K/-BOARD EN - SEL 16-32K/-BOARD EN - SEL 32-48K/-BOARD EN - SEL 48-64K/-BOARD EN					52/48	51/48	50/48	49/48								*18	J7-2
+ SELECTED INDEX + SENSE LOWER CASE - SHIFT + SIGNAL QUALITY + SPECIAL FUNCTION 12				11								52	*52	57	57	*57	*J4-48 *J3-16 J3-23
+ SPECIAL FUNCTION 14 + SPECIAL FUNCTION 23 + SPECIAL FUNCTION 25 - STEP + STEP CMD			*20 *27 *11													*11 42	J3-2 J3-20 J3-21/24 J7-24
+ ST0A + ST1A + ST2A + ST3A - STOP														47 48 49 50	*47 *48 *49 *50		
- SYSTEM RESET + SYNC - SUDO CLK	76	76	76	37 76	76	76	76	76	*76	76	76	76	76	76	76		

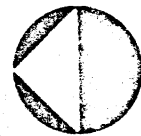




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TITLE SIGNAL LIST, RGBPL				MODEL 3200	DWG NO. 23622-XX	REV. A
DRAWN R. MATSUMOTO		DATE 8/31/76		SIGNAL LIST SHEET 10 OF 11		SHEET OF 13 14

SIGNAL NAME	SPARE XA2	RGPN XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
+ T CLK - THIS UNIT COMMAND - TMR - TO IDLE - TRACK 00														*65 60 52	20 *60 *52	*20 65 47	*J7-38
- TV P (-DMA P IN)										15	14/15		*14				
- VERT DR + VIDEO												*7 *5					J6-8 J6-10
+ W CLK TIME - W CLK TIME - WCZ - WRITE DATA AND CLK - WRITE DATA PHASE														*55	67 68 55 71	*67 *68 *8 71	J7-44
- WFLG - WRITE GATE + WRITE ON B - WRITE PROTECT														6	*6 *34	*14 34 52	J7-18 *J7-16



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TITLE

SIGNAL LIST, RGBPL

MODEL

3200

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SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17	I/O
+ XEQU - XMIT DATA - XMIT TIMING EXT			*23 *25											*56	56		J3-3 J3-22
SPARE 1 SPARE 2 SPARE 3 SPARE 4 SPARE 5												8 10 63		59	59	10	J6-4 J6-6 J7-40

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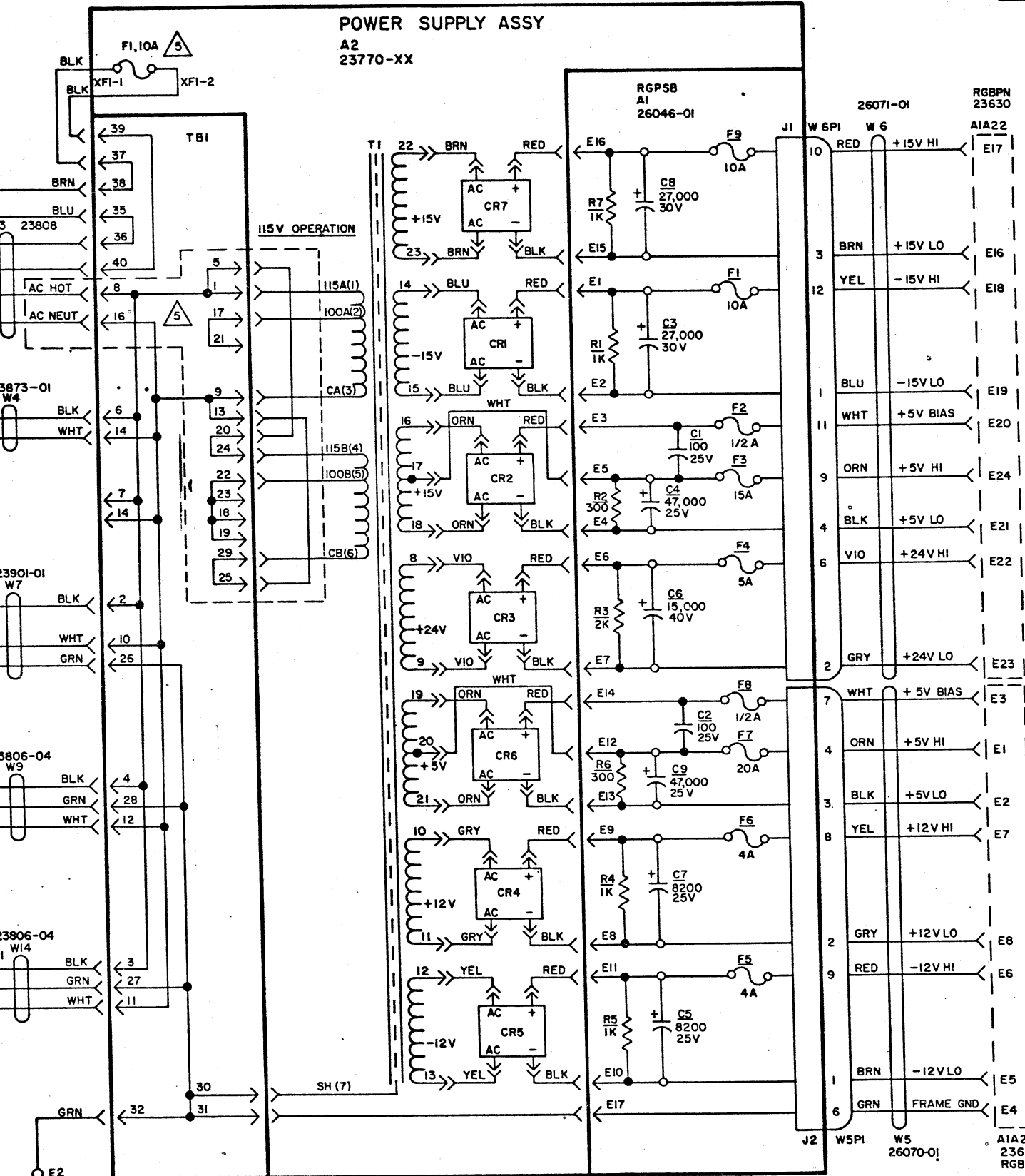
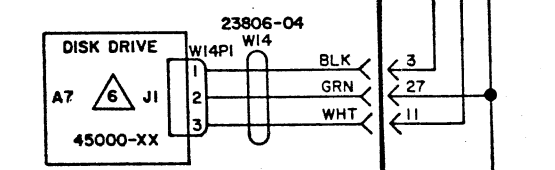
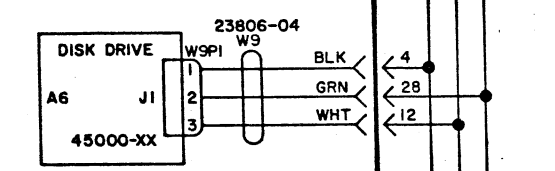
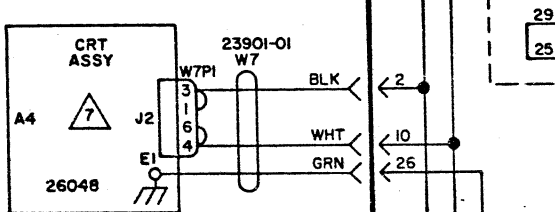
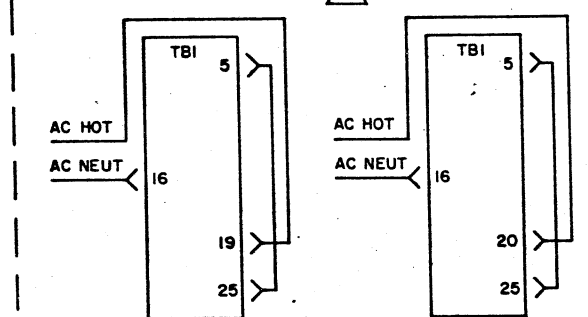
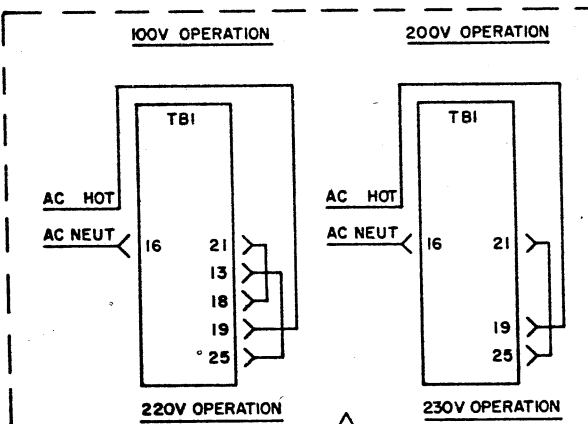
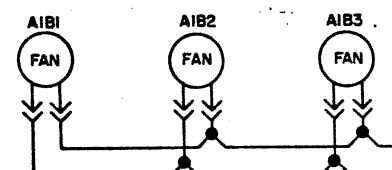
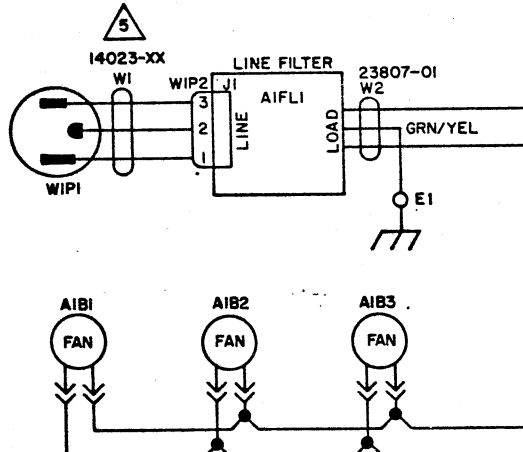
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B

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### POWER SUPPLY ASSY

A2  
23770-XX

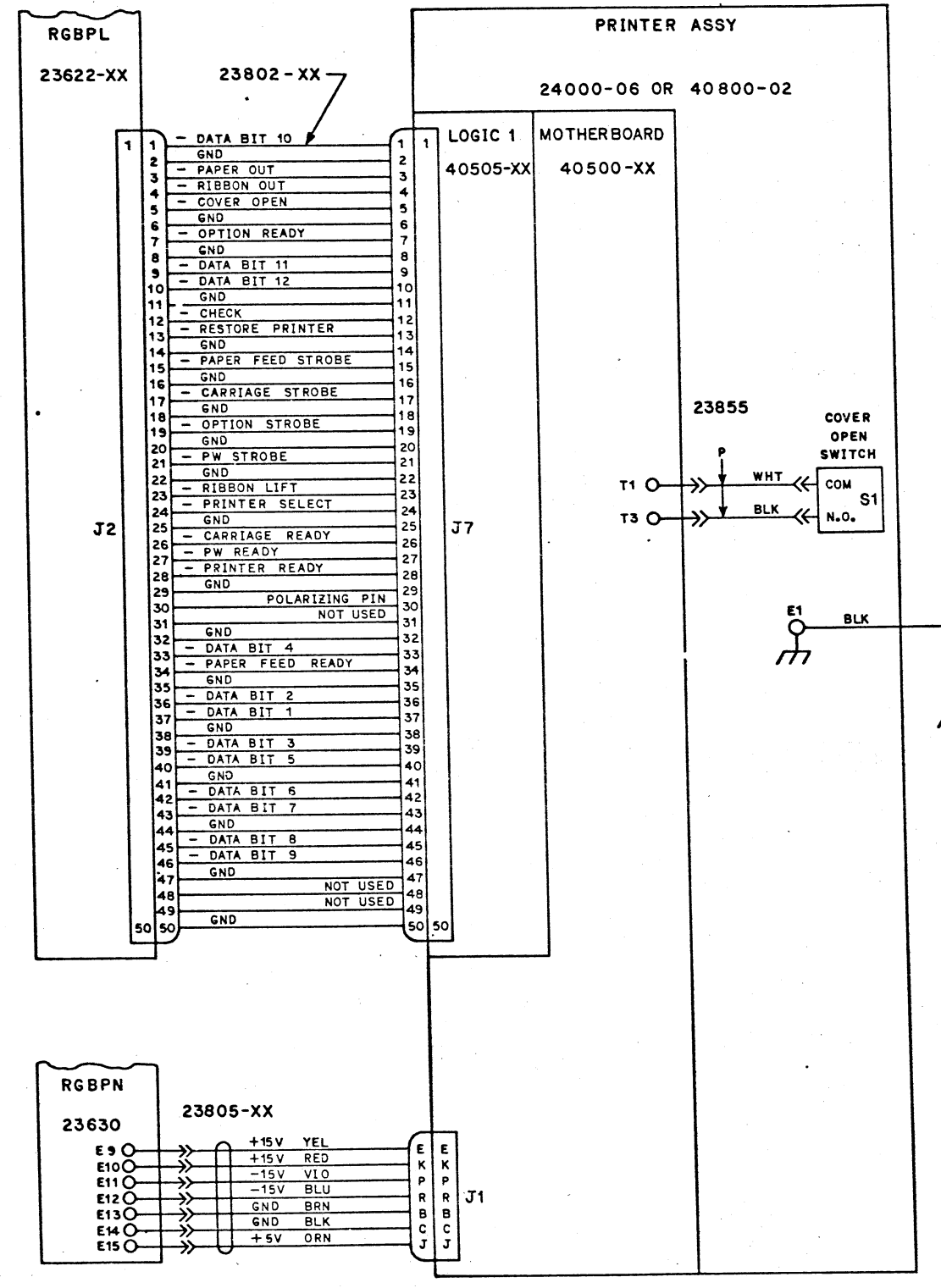
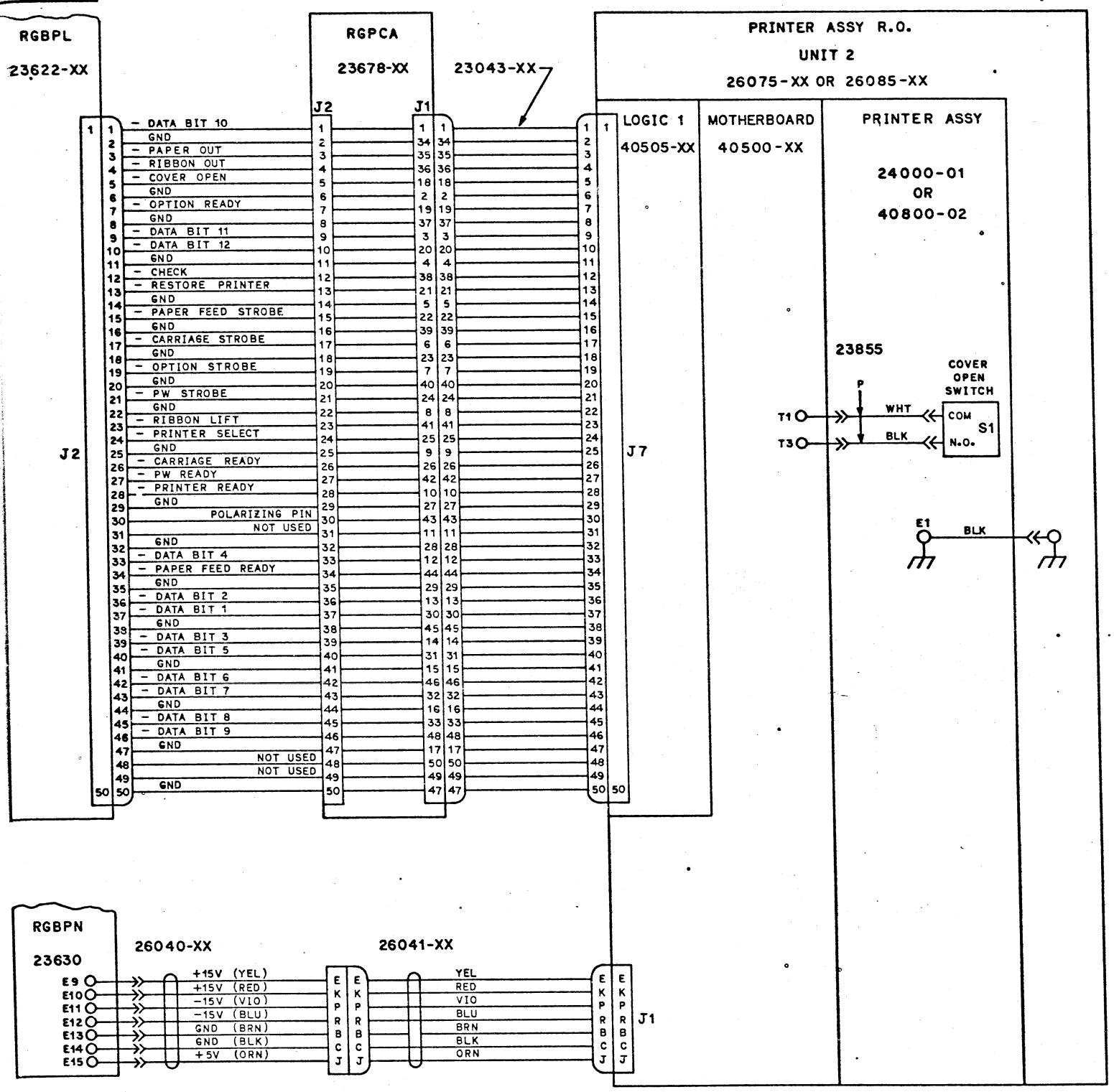


- NOTES: UNLESS OTHERWISE SPECIFIED
- CAPACITANCE IS SPECIFIED IN MICROFARADS.
  - RESISTANCE IS IN OHMS.
  - RESISTORS ARE 1 WATT.
  - ALL FUSES ARE SLOW BLOW TYPE.
- 5 FOR 200V - 230V OPERATION, POWER CORD WI IS NOT SUPPLIED AND FUSE F1 IS CHANGED TO 6.25A. FOR OPERATION AT OTHER THAN 115 V, MAKE CHANGES TO TBI AS SHOWN. NO CHANGES ARE REQUIRED IN PRIMARY LEADS OF TRANSFORMER (T1), OR IN LEADS OF 115V AUXILIARY DEVICES, OR FOR OPERATION FROM 47 TO 63HZ.
- 6 OPTIONAL DISK DRIVE.
- 7 INSTALLED ON 23932-XX ASSY ONLY.

# ADVANCE RELEASE

### SCHEMATIC DIAGRAM

DRAWN ED ADAMS	DATE 10-28-76	Diablo Systems Incorporated Hayward, California 94545
CHECKED	DATE	
ENGR	DATE	THESE DRAWINGS AND/OR SPECIFICATIONS AND THE DATA CONTAINED THEREIN ARE THE EXCLUSIVE PROPERTY OF DIABLO SYSTEMS, INC. ISSUED IN CONFIDENCE AND SHALL NOT, WITHOUT THE PRIOR WRITTEN PERMISSION OF DIABLO SYSTEMS, INC. BE SHOWN OR DISCLOSED IN ANY MANNER TO ANY PERSON, OR BE COPIED, REPRODUCED OR USED FOR ANY PURPOSE WHATSOEVER EXCEPT THE MANUFACTURE OF ARTICLES FOR DIABLO SYSTEMS, INC.
MFG	DATE	
FIRST USED NEXT ASSY: 23400-XX & 23932-XX		SCHEMATIC, POWER DISTRIBUTION
SHEET 1	TOT SHT 1	REV A
SHEET NO. 23676-01		REV. E.C.O. NO.



ADVANCE RELEASE

23679-01

23679-02

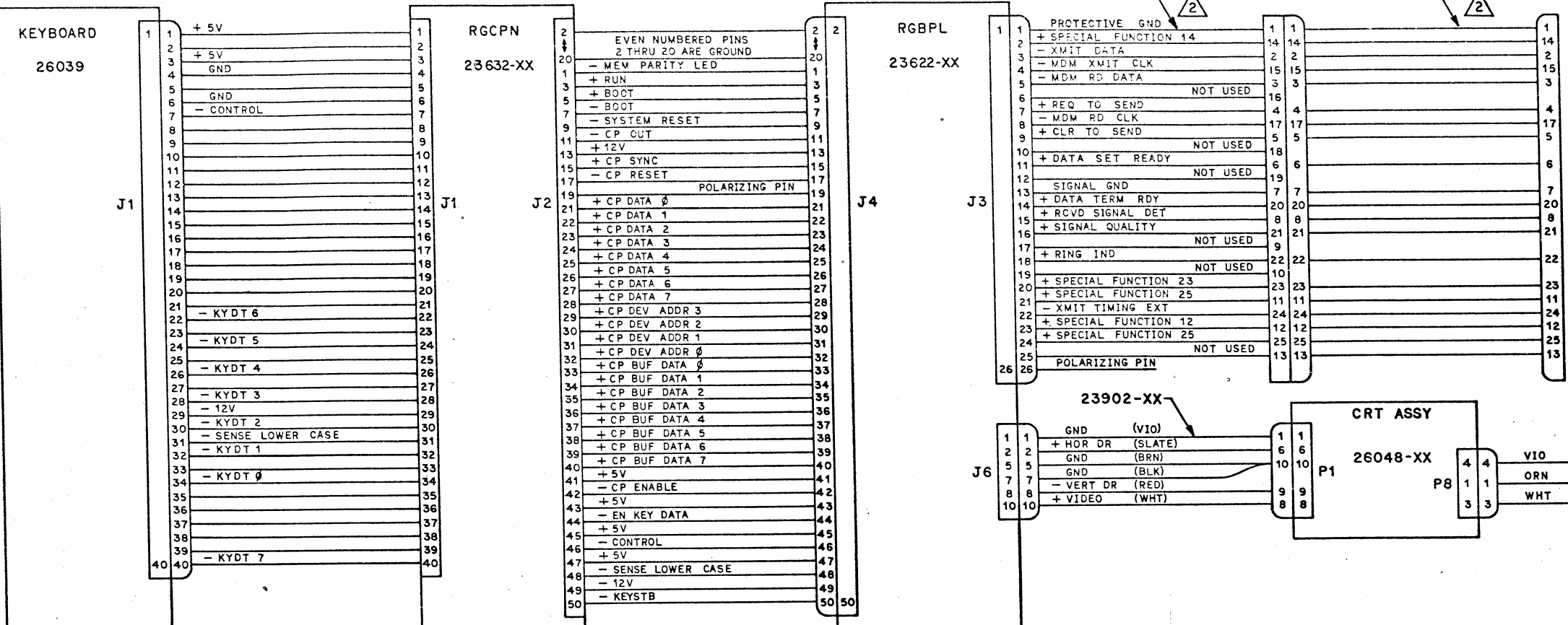
ON PROCESSOR ASSY WITH CRT (23932-XX), THIS R.O. PRINTER ASSY ( ) AND ASSOCIATED CABLES ARE AN OPTION.

ON PROCESSOR ASSY WITH PRINTER (23400-XX), THE CRT ASSY ( ) AND ASSOCIATED CABLES ARE REPLACED BY THIS PRINTER ASSY ( ) AND ASSOCIATED CABLES.

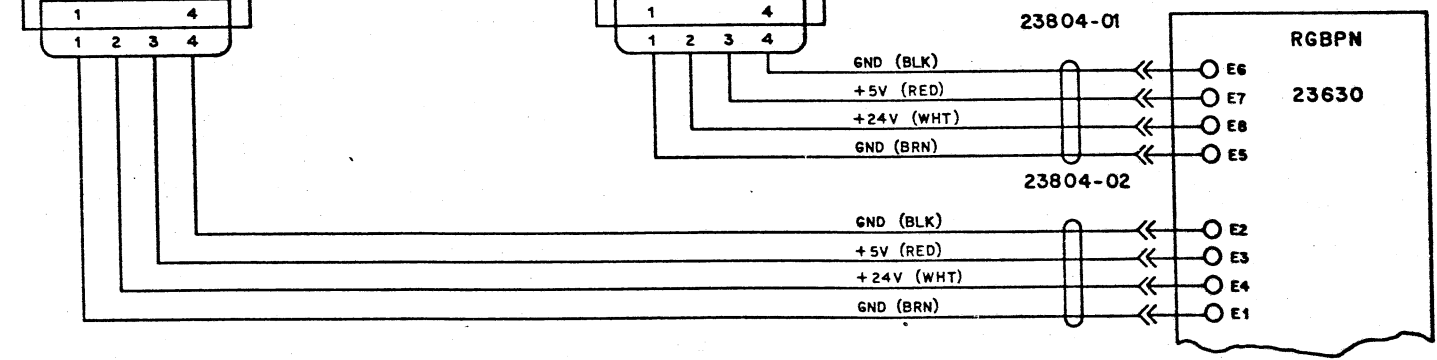
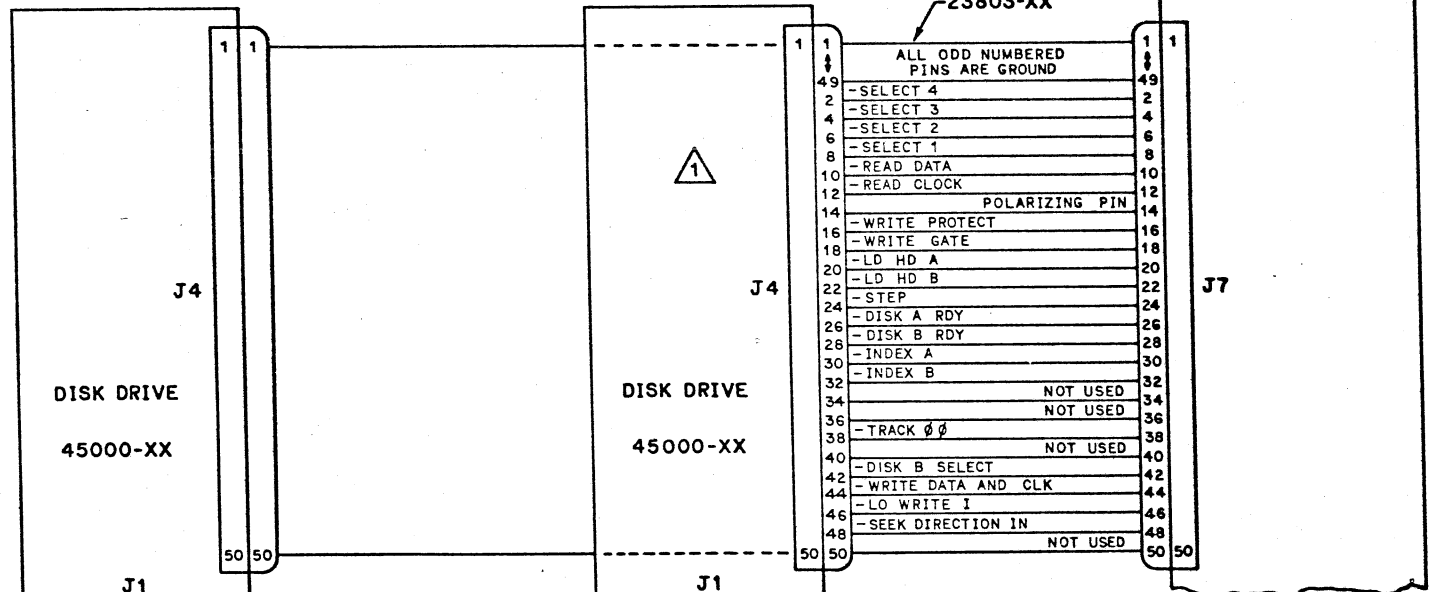
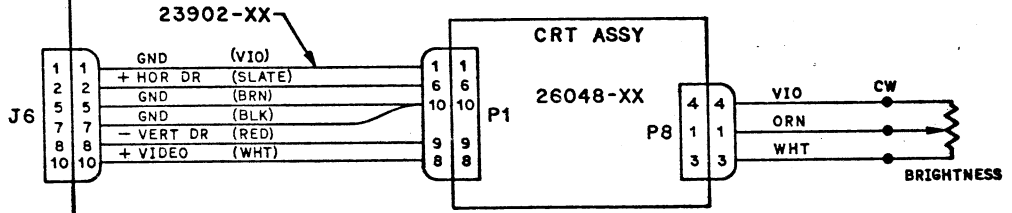
Diablo Systems Incorporated INTERCONNECTION DIAGRAM SIGNAL AND DC POWER CABLE

23679-XX

23679-XX D1



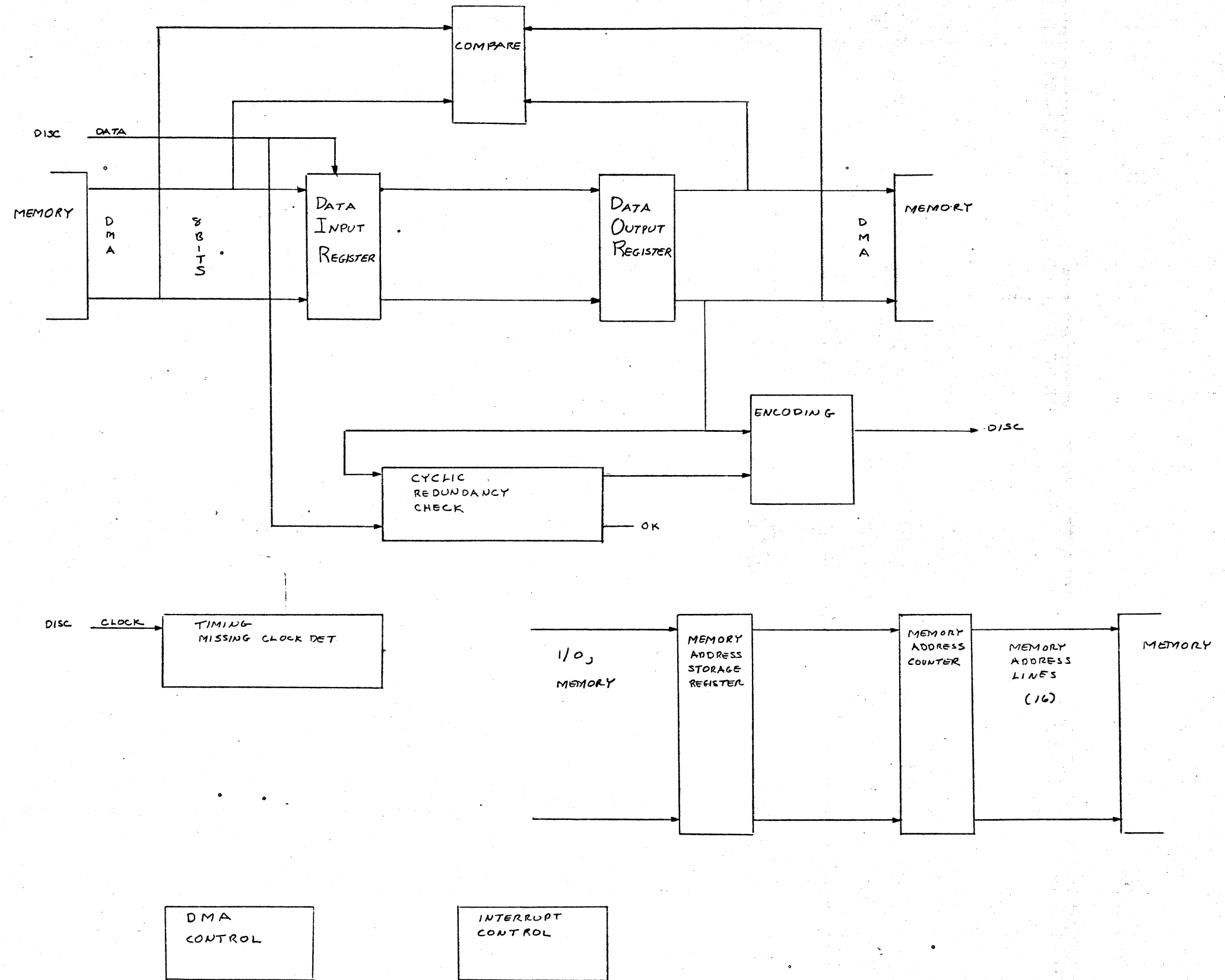
**NOTES:**  
 1 OPTIONAL DISK DRIVE.  
 2 CABLES 23801-XX AND 23906-XX ARE PART OF THE EIA OPTION (26084-XX).



**ADVANCE RELEASE**

**Diablo Systems Incorporated**  
 INTERCONNECTION DIAGRAM  
 SIGNAL AND DC POWER CABLES  
 MODEL: \_\_\_\_\_  
 SYSTEM LOG NO: \_\_\_\_\_  
 PRODUCT NO: 23679-XX

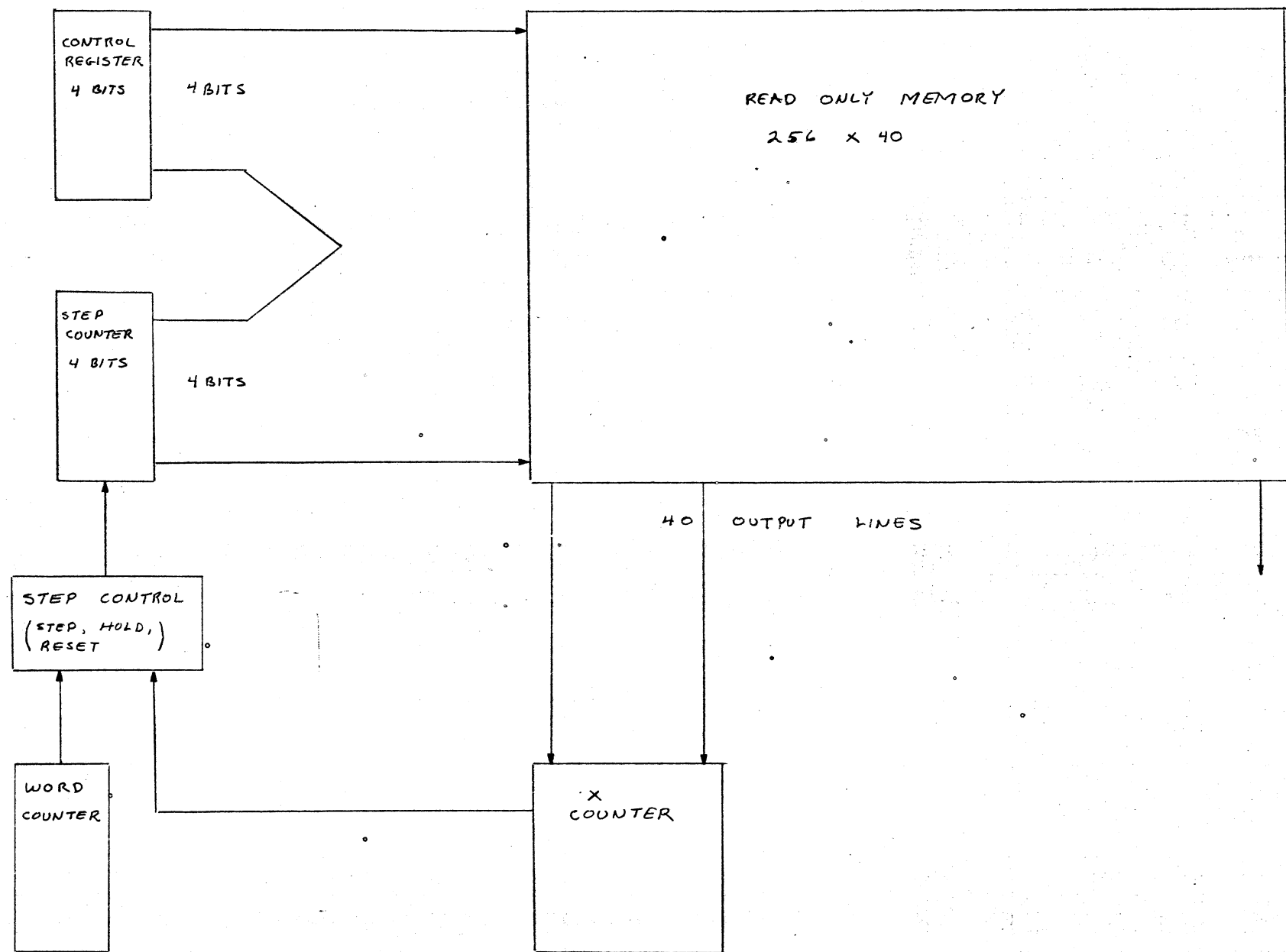




BLOCK DIAGRAM  
RANGER FLOPPY  
DISC CONTROLLER

R SWENSON NOV 16, 1975

MAIN CONTROL SEQUENCING



BLOCK DIAGRAM  
RANGER FLOPPY  
DISC CONTROLLER

R SWENSON NOV 1979

SHEET 2 OF 2

























