DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000312-03

PROGRAM

ERCC DIAGNOSTIC

TEXT TAPE

097-000312-03

ABSTRACT

THE ERCC DIAGNOSTIC IS DESIGNED TO VERIFY THE OPERATION OF THE ERCC OPTION AND TO DETECT AND LOCALIZE FAILURES IN THE ERCC LOGIC IN THE CPU AND IN ANY ERCC MEMORY IN THE SYSTEM. THE DIAGNOSTIC EXECUTES USING TEST LOCATIONS IN ALL ERCC MEMORY MODULES.

```
 0001 ERCC  MACRO REV 06.20              14:47:40 07/29/77
01
02
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: ERCC.TX                          PART NUMBER: 097-000312
10              ;
11              ;
12              ; DESCRIPTION: ERCC DIAGNOSTIC
13              ;
14              ;
15              ; REVISION HISTORY:
16              ;
17              ;       REV.            DATE
18              ;
19              ;       00              06/06/75
20              ;       01              08/06/76
21              ;       02              12/31/76
22              ;       03              08/05/77
23              ;
24              ;
25              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1975, 1976, 1977
26              ; ALL RIGHTS RESERVED.
27              ;*****************************************************************
```

```
!0002 ERCC
01              ;
                        .TITLE  ERCC
03              ;
04              ; ECLIPSE ERROR CORRECTION TEST
```

```
10003 ERCC
01                ;
02                ;ERCC DIAGNOSTIC
03                ;
04                ;THE DIAGNOSTIC IS DESIGNED TO RUN IN AN AUTO-LOAD
05                ;AUTO-RUN ENVIRONMENT.
06                ;
07                ;1.0 ABSTRACT
08                ;       1.1  ERCC DIAGNOSTIC
09                ;            THE ERCC DIAGNOSTIC IS DESIGNED TO VERIFY THE
10                ;            OPERATION OF THE ERCC OPTION AND TO DETECT AND
11                ;            LOCALIZE FAILURES IN THE ERCC LOGIC IN THE CPU
12                ;            AND IN ANY ERCC MEMORY IN THE SYSTEM. THE
13                ;            DIAGNOSTIC EXECUTES USING TEST LOCATIONS IN ALL
14                ;            ERCC MEMORY MODULES.
15                ;
16                ;
17                ;            THE PROGRAM WILL TEST
18                ;            NON-INTERLEAVED AND UP TO 8 WAY INTERLEAVED
19                ;            MEMORY CONFIGURATIONS.THE MEMORY MODULES
20                ;            MAY BE CORE OR SC .
21                ;
22                ;
23                ;
24                ;            IT IS ASSUMED THAT THE 21 BIT MEMORY
25                ;            TO BE TESTED,EXCLUDING THE ERCC OPTION,
26                ;            IS FAULT FREE.
27                ;
28                ;            THE FOLLOWING TYPES OF MEMORIES ARE SUPPORTED
29                ;            BY THIS PROGRAM.
30                ;
31                ;
32                ;               8K X 21 BIT CORE
33                ;               8K X 21 BIT S.C. (CACHE)
34                ;               32K X 21 BIT S.C.
35                ;
36                ;
37                ;
38                ;2.0 MACHINE REQUIREMENTS
39                ;       2.1  ECLIPSE PROCESSOR WITH ERCC OPTION
40                ;       2.2  8K READ/WRITE 21 BIT ERCC  MEMORY
41                ;       2.3  TTY
42                ;
43
```

```
10004 ERCC
01
02
03
04                ;
05                ;3.0 OPERATING PROCEDURE
06                ;       3.1  LOADING
07                ;            LOAD PROGRAM VIA THE BINARY LOADER.
08                ;       3.2  START ADDRESS
09                ;            SET SWITCHES TO 200 OCTAL .
10                ;       3.3  SWITCH SETTINGS
11                ;            SWITCH 0 (0) = USE CONTENTS OF "SWREG"
12                ;            SWITCH 0 (1) = USE DATA SWITCHES
13                ;            SWITCH 1 (1) = PROCEED FROM ERROR
14                ;            SWITCH 2 (1) = INHIBIT OUTPUT TO TTO
15                ;            SWITCH 3 (1) = PRINT FAILURE RATE
16                ;            SWITCH 4 (1) = INHIBIT PASS COUNT
17                ;            SWITCH 5 (1) = ENABLE OUTPUT TO LPT
18                ;            SWITCH 6 (1) = BYPASS EXIST TEST
19                ;            SWITCH 7 (1) = BYPASS MAPPED TESTING
20                ;            SWITCH 8 (1) = PRINT ERCC EXIST MAP
21                ;
22                ;*
23                ;*EXCEPTION
24                ;*           SWITCH 8 (1) = INHIBIT MAP DUMP EXECUTION
25                ;*                          I.E. MANUAL DUMP SELECTED @220
26                ;
27                ;            THE OPTION TO USE THE DATA SWITCHES OR
28                ;            THE CONTENTS OF LOC "SWREG" MAY ONLY BE
29                ;            EXERCISED AT THE BEGINNING OF THE PROGRAM
30                ;            OR FOLLOWING AN ERROR HALT.
31                ;
32                ;       3.4  NORMAL OPERATION
33                ;            PROGRAM WILL EXECUTE ALL DIAGNOSTIC TESTS
34                ;            IN ALL ERCC MEMORIES. AT END OF EACH PASS,
35                ;            A PASS COUNTER WILL BE PRINTED IF
36                ;            SWITCH 4 IS RESET.
37                ;
```

```
01
02
03
04              ;4.0 ERROR DESCRIPTION
05              ;       4.1  DIAGNOSTIC
06              ;            UPON THE DETECTION OF AN ERROR,THE C/PC,
07              ;            AND THE AC'S WILL BE PRINTED.ALSO,THE
08              ;            CONTENTS OF THE ADDRESS REGISTER IN ERCC
09              ;            AND THE FAULT CODE REGISTER WILL BE PRINTED
10              ;            ALONG WITH THE LOGICAL TEST ADDRESS.
11              ;            IF THE PROGRAM IS RUNNING IN MAPPED MODE,
12              ;            THE CURRENT PHYSICAL TEST BLOCK WILL
13              ;            ALSO BE PRINTED ALONG WITH OTHER MAP DATA.
14              ;            THE PROGRAM WILL THEN LOOP ON THE FAILING TEST
15              ;
16              ;
17              ;       4.2  DIAGNOSTIC - ABNORMAL
18              ;            SEVERAL TYPES OF UNEXPECTED FAILURES
19              ;            WILL CAUSE A PROGRAM HALT. THEY ARE AS FOLLOWS:
20              ;            PROTECTION FAULT
21              ;            UNEXPECTED INTERRUPT
22              ;            STACK OVERFLOW OR UNDERFLOW
23              ;            THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
24              ;            CORRECTED BEFORE RESUMING ERCC TESTING.
25              ;       4.3  ERCC EXIST TEST
26              ;            SINCE THE PROGRAM USES VARYING TEST LOCATIONS,
27              ;            IT MUST DETERMINE ON THE FLY IF THE
28              ;            TEST LOCATION DOES RESIDE IN AN ERCC MEMORY.
29              ;            IN THE DIAGNOSTIC, IF ALL OF MEMORY IS SCANNED,
30              ;            AND NO ERCC MEMORIES ARE FOUND, A
31              ;            MESSAGE "NO ERCC MEMORY" WILL BE OUTPUT TO THE TTY.
32              ;            SWITCH 6 CAN BE USED TO ELIMINATE THIS
33              ;            DYNAMIC EXIST TEST, BUT THIS SHOULD ONLY BE DONE
34              ;            IF THE FIRST 8K IN THE SYSTEM IS AN ERCC MEMORY.
35              ;            THIS FEATURE SHOULD ONLY BE USED IF THE OPTION
36              ;            IS FAILING SO BADLY, THAT THE SOFTWARE CANNOT
37              ;            DETERMINE THAT IT EXISTS.
38              ;
```



```
01
02
03
04              ;
05              ;5.0 PROGRAM DESCRIPTION
06              ;       5.1  DIAGNOSTIC
07              ;            THE DIAGNOSTIC IS COMPOSED OF THREE MAIN
08              ;            AREAS OF TESTING. THEY ARE AS FOLLOWS:
09              ;            A. CONTROL LOGIC TESTS
10              ;            B. FAULT CODE GENERATION TESTS
11              ;            C. ADDRESS TESTS
12              ;            THE FAULT CODE GENERATION TESTS AND THE
13              ;            CONTROL LOGIC TESTS ARE EXECUTED USING
14              ;            TEST LOCATIONS BETWEEN  17500 THROUGH 17577 IN ALL
15              ;            ERCC MEMORIES.THE ACTUAL TEST LOCATIONS ARE
16              ;            0,11,22,33,44,55,66 AND 77. THE ADDRESS TESTS ARE
17              ;            EXECUTED USING TEST LOCATIONS 16000 THROUGH 17577.
18              ;
19              ;
20              ;6.0 MONITOR LOCATIONS
21              ;            THE FOLLOWING LOCATIONS IN PAGE 0 MAY
22              ;            BE MONITORED/EXAMINED TO PROVIDE
23              ;            ADDITIONAL INFORMATION.
24              ;
25              ;
26              ;            LOC    TAG          DESCRIPTION
27              ;
28              ;            200    DTOSB        USED BY DTOS
29              ;            201    LOOPR        ADDRESS +1 OF LAST TEST ENTERED
30              ;            202    IBEG         STARTING LOC. OF PROGRAM
31              ;            203    PCNTR        PROGRAM PASS COUNTER
32              ;            204    ITRCT        ITERATION COUNT
33              ;            205    ECS          ERCC EXISTS SWITCH
34              ;                                0=NO ERCC
35              ;            206    MPSWT        MAP EXISTS SWITCH
36              ;                                0=NO MAP
37              ;            207    BET          BYPASS ERCC EXIST TEST SWITCH
38              ;                                0=DO NOT BYPASS
39              ;            210    PMODE        BYPASS MAPPED TESTING SWITCH
40              ;                                0=DO NOT BYPASS
41              ;            211    PEMAP        PRINT ERCC EXIST MAP SWITCH
42              ;                                0=DO NOT PRINT
43              ;            212    CADR         CURRENT ADDRESS UNDER TEST
44              ;                                LOW 15 PHYSICAL BITS
45              ;
46              ;7.0 MEMORY MAPS
47              ;
48              ;            7.1 ERCC EXIST MAP
49              ;
50              ;            SWITCH 8 MAY BE USED TO PROVIDE AN ERCC
51              ;            EXIST MAP IDENTIFYING WHICH MEM MODULES
52              ;            IN THE SYSTEM ARE ACTUALLY ERCC TYPE.
53              ;            SINCE ALL OF MEMORY MUST BE TESTED BEFORE THE
54              ;            ERCC EXIST MAP IS FULLY FORMED,IT IS NOT AVAILABLE
55              ;            UNTIL ONE COMPLETE PASS HAS BEEN MADE THROUGH THE
56              ;            CONTROL LOGIC AND FAULT CODE TESTS.
57              ;
58              ;            IN A SYSTEM WHICH CONTAINS MORE THAN ONE ERCC
59              ;            MEMORY,THE ERCC EXIST MAP SHOULD BE USED TO
60              ;            VERIFY THAT ALL THE ERCC MEMORIES IN THE
```

```
                ;               SYSTEM ARE IN FACT OPERATING AS
                ;               ERCC MEMORIES.
                ;
                ;
                ;
                ;
                ;
                ;               TO PROPERLY INTERPRET THE ERCC EXIST MAP,ONE
                ;               MUST BE FAMILIAR WITH THE PROGRAM TESTING SEQUENCE.
                ;               EIGHT LOCATIONS IN THE LAST 1K OF EACH 8K ERCC
                ;               MEMORY ARE USED.THE INTERLEAVE FACTOR WILL
                ;               DETERMINE THE TESTING SEQUENCE AS FOLLOWS,WHERE
                ;               THE FIRST MEMORY MODULE IS A,THE SECOND IS B ETC.
                ;
                ;               8K X 21 BIT CORE,32K X 21 BIT S.C.
                ;
                ;               CORE 8-WAY          A B C D E F G H
                ;               CORE 4-WAY          A B C D A B C D
                ;               CORE 2-WAY          A B A B A B A B
                ;               CORE NONE           A A A A A A A A
                ;
                ;               8K X 21 BIT S.C. (CACHE)
                ;
                ;               SC   8-WAY          A C E G B D F H
                ;               SC   4-WAY          A C A C B D B D
                ;               SC   2-WAY          A A A A B B B B
                ;               SC   NONE           A A A A A A A A
                ;
                ;
                ;
                ;
                ;               THE ERCC MAP CONSISTS OF 8X16 BIT WORDS (MMPU)
                ;*              16X16 BIT WORDS (MMPU1) WITH EACH WORD REPRESENT-
                ;*              ING ONE TEST LOCATION IN A SPECIFIC MODULE.
                ;               EACH WORD REPRESENTS 2 8K  MEM MODULES.
                ;               EACH BIT REPRESENTS ONE TEST LOCATION IN
                ;               A SPECIFIC MODULE.A BIT=1 DENOTES THAT
                ;               ERCC EXISTS FOR THAT TEST LOCATION.BIT
                ;               0 OF WORD 0 DENOTES THE FIRST TEST LOC
                ;               IN THE FIRST 8K.BIT 8 OF WORD 0 DENOTES
                ;               THE FIRST TEST LOC OF THE SECOND 8K ETC.
                ;
                ;               7.2 ERCC EXIST MAP-CORE
                ;
                ;
                ;I.E.           A SYSTEM HAS 128K,WITH THE FIRST 32K AND
                ;               THE LAST 32K AS ERCC MEMORIES,THE ERCC
                ;               EXIST MAP WOULD APPEAR AS FOLLOWS:
                ;
                ;               177777
                ;               177777
                ;               000000
                ;               000000
                ;               000000
                ;               000000
                ;               177777
                ;               177777
                ;
                ;
                ;               7.3 ERCC EXIST MAP-SEMICONDUCTOR (CACHE)
```



```
                ;
                ;I.E.           A SYSTEM HAS 128K,WITH THE FIRST 64K EIGHT WAY
                ;               INTERLEAVED AND THE LAST 64K NON-INTERLEAVED.IN THE
                ;               FIRST 64K,ONLY THE FIRST AND SECOND MEMORY MODULES (A,B)
                ;               ARE ERCC TYPE.IN THE LAST 64K,ONLY THE LAST MEMORY
                ;               MODULE IS ERCC TYPE.THE ERCC EXIST MAP WOULD APPEAR
                ;               AS FOLLOWS:
                ;
                ;               104210
                ;               104210
                ;               104210
                ;               104210
                ;               000000
                ;               000000
                ;               000000
                ;               000377
                ;
                ;
                ;
                ;               7.4 ERCC EXIST MAP-32K X 21 BIT S.C.
                ;
                ;               SAME AS 8K X 21 BIT CORE.SEE 7.2.
                ;
                ;
                ;
                ;
                ;
                ;
                ;
```

```
!0009 ERCC
01                ;
02                ;
03                ;8.0 PROGRAMMING DESCRIPTION
04                ;
05                ;
06                ;        8.1      DOA INSTRUCTION
07                ;
08                ;
09                ;                 THE DOA INSTRUCTION IS USED TO ENABLE
10                ;                 THE ERCC OPTION ACCORDING TO THE SETTING
11                ;                 OF BITS 14-15 IN THE SPECIFIED AC.
12                ;
13                ;
14                ;                 BITS 14-15       MEANING
15                ;
16                ;
17                ;                 00               DISABLE CHECKING AND CORRECTION.
18                ;                                  WRITE VALID CHECK FIELD BITS.
19                ;                 01               DISABLE CHECKING AND CORRECTION.
20                ;                                  WRITE CHECK BIT FIELD OF 37
21                ;                                  IF CORE MEMORY. IF SEMICONDUCTOR
22                ;                                  MEMORY OLD CHECK BIT FIELD
23                ;                                  IS UNAFFECTED.
24                ;                 10               ENABLE CHECKING AND CORRECTION.
25                ;                                  DO NOT INTERRUPT ON
26                ;                                  MEMORY ERROR.
27                ;                 11               ENABLE CHECKING AND CORRECTION.
28                ;                                  INTERRUPT ON MEMORY ERROR.
29                ;
30                ;        8.2      DIA INSTRUCTION
31                ;
32                ;
33                ;                 THE LOW ORDER 16 BITS OF THE 18 BIT PHYSICAL
34                ;                 ADDRESS OF THE MEMORY LOCATION IN ERROR IS
35                ;                 PLACED IN BITS 0-15 OF THE SPECIFIED AC.
36                ;
37                ;
38                ;        8.3      DIB INSTRUCTION
39                ;
40                ;                 A FIVE BIT ERROR CODE IS PLACED IN BITS 0-4
41                ;                 OF THE SPECIFIED AC.  BITS 5-13 OF THE SPECIFIED
42                ;                 AC ARE SET TO 0.THE HIGH ORDER 2 BITS OF THE
43                ;                 18 BIT PHYSICAL ADDRESS OF THE FAILING LOCATION
44                ;                 ARE PLACED IN BITS 14-15.  THE ERROR CODE TELLS
45                ;                 WHICH BIT WAS IN ERROR AND HAS BEEN CORRECTED.
46                ;                 THE VARIOUS ERROR CODES AND THEIR MEANINGS
47                ;                 ARE DESCRIBED BELOW.
48                ;
49                ;
50                ;                 FAULT CODE       MEANING (BIT LOCATION OF ERROR)
51                ;
52                ;                 00000            NO ERROR
53                ;                 00001            CHECK BIT 4
54                ;                 00010            CHECK BIT 3
55                ;                 00011            DATA BIT 0
56                ;                 00100            CHECK BIT 2
57                ;                 00101            DATA BIT 1
58                ;                 00110            MULTIPLE BIT ERROR
59                ;                 00111            DATA BIT 3
60                ;                 01000            CHECK BIT 1
```

```
 0010 ERCC
01                ;                 01001            DATA BIT 4
02                ;                 01010            ALL 21 BITS ARE 1.
03                ;                 01011            DATA BIT 6
04                ;                 01100            DATA BIT 7
05                ;                 01101            DATA BIT 8
06                ;                 01110            DATA BIT 9
07                ;                 01111            MULTIPLE BIT ERROR
08                ;                 10000            CHECK BIT 0
09                ;                 10001            DATA BIT 11
10                ;                 10010            DATA BIT 12
11                ;                 10011            DATA BIT 13
12                ;                 10100            DATA BIT 14
13                ;                 10101            ALL 21 BITS ARE 0.
14                ;                 10110            DATA BIT 2
15                ;                 10111            MULTIPLE BIT ERROR
16                ;                 11000            DATA BIT 10
17                ;                 11001            MULTIPLE BIT ERROR
18                ;                 11010            DATA BIT 5
19                ;                 11011            MULTIPLE BIT ERROR
20                ;                 11100            DATA BIT 15
21                ;                 11101            MULTIPLE BIT ERROR
22                ;                 11110            MULTIPLE BIT ERROR
23                ;                 11111            MULTIPLE BIT ERROR
24                ;
25                ;9.0 PROGRAM RUN TIME
26                ;
27                ;                 THE PROGRAM RUN TIME IS A FUNCTION OF THE
28                ;                 AMOUNT OF  ERCC MEMORY  IN THE SYSTEM.
29                ;                 IT IS APPROXIMATELY 30 SECONDS PER 8K OF ERCC
30                ;                 MEMORY.
31                ;
32                ;
33                ;*10.0 MANUAL MAP DUMP UTILITY
34                ;*           A MAP DUMP UTILITY IS AVAILABLE TO THE USER WHICH
35                ;*       DUMPS THE CURRENT CONTENTS OF EITHER THE MMPU OR MMPU1.
36                ;*                          THE USER MUST START THE DUMP UTILITY
37                ;*       AT LOCATION 220 (OCTAL), CAUTION SWITCH (8) MUST BE 0
38                ;*       I.E. = 0 (RESET). THE PROGRAM WILL HALT FOLLOWING MAP
39                ;*       DUMP EXECUTION.
40                ;
41                ;
42                ;
```

10011 ERCC

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS