


```

MM      MM  PPPPPPP  LL      000000  AAAAAA  DDDDDDDD
MM      MM  PPPPPPP  LL      000000  AAAAAA  DDDDDDDD
MMMM    MMMM PP      PP  LL      00      00  AA      AA  DD      DD
MMMM    MMMM PP      PP  LL      00      00  AA      AA  DD      DD
MM      MM  PP      PP  LL      00      00  AA      AA  DD      DD
MM      MM  PP      PP  LL      00      00  AA      AA  DD      DD
MM      MM  PPPPPPP  LL      00      00  AA      AA  DD      DD
MM      MM  PPPPPPP  LL      00      00  AA      AA  DD      DD
MM      MM  PP      LL      00      00  AAAAAAAAAA DD      DD
MM      MM  PP      LL      00      00  AAAAAAAAAA DD      DD
MM      MM  PP      LL      00      00  AA      AA  DD      DD
MM      MM  PP      LL      00      00  AA      AA  DD      DD
MM      MM  PP      LL      00      00  AA      AA  DD      DD
MM      MM  PP      LLLLLLLLLL 000000  AA      AA  DDDDDDDD
MM      MM  PP      LLLLLLLLLL 000000  AA      AA  DDDDDDDD

```

```

LL      IIIIII  SSSSSSSS
LL      IIIIII  SSSSSSSS
LL      II      SS
LL      II      SS
LL      II      SS
LL      II      SS
LL      II      SSSSSS
LL      II      SSSSSS
LL      II      SS
LL      II      SS
LL      II      SS
LL      II      SS
LLLLLLLLLL IIIIII  SSSSSSSS
LLLLLLLLLL IIIIII  SSSSSSSS

```

MPLOAD
Table of contents

(1)	228	MPDCL - Multi-processing DCL command line handling
(1)	641	MP\$\$UNLOAD - STOP/CPU DCL command
(1)	719	MP\$\$UNHOOK - Unhook multi-processing code from system

```

0000 1  :
0000 2  : Version:      'V04-000'
0000 3  :
0000 4  :
0000 5  :      .MCALL MFPR
0000 6  :      .TITLE MPLOAD - LOAD AND CONNECT CODE FOR MULTIPROCESSING
0000 7  :      .IDENT 'V04-000'
0000 8  :
0000 9  : *****
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0000 28 : *
0000 29 : *****
0000 30 : ++
0000 31 : Facility: Executive , Hardware fault handling
0000 32 :
0000 33 : Abstract:
0000 34 :
0000 35 : MPLOAD is the main control module for the installation of
0000 36 : the code required for multiprocessing. It changes mode to kernel,
0000 37 : acquires sufficient pool space and moves the code into it.
0000 38 : With all interrupts disabled, the necessary hooks are inserted
0000 39 : into the exec to connect several replacement routines.
0000 40 :
0000 41 : Environment: MODE=Kernel
0000 42 :
0000 43 : Author: RICHARD I. HUSTVEDT, Creation date: 15-MAY-1979
0000 44 :
0000 45 : Modified by:
0000 46 :
0000 47 : V03-009 KDM0024 Kathleen D. Morse 10-Oct-1982
0000 48 : Alter CHMx vectors in secondary SCB if system service
0000 49 : inhibit was requested at boot time.
0000 50 :
0000 51 : V03-008 KDM0020 Kathleen D. Morse 04-Oct-1982
0000 52 : Create a subroutine that unhooks the multi-processing
0000 53 : code from the system, that can be invoked from the

```

```

0000 53 : primary's invalidate time-out logic.
0000 54 :
0000 55 : V03-007 KDM0003 Kathleen D. Morse 06-Aug-1982
0000 56 : Make STOP/CPU provide correct address to EXES$DEANONPAGED
0000 57 : when the pool block was < 32 bytes off a page boundary.
0000 58 :
0000 59 : 01 -
0000 60 : --
0000 61 :
0000 62 :
0000 63 : INCLUDE FILES:
0000 64 :
0000 65 :
0000 66 :
0000 67 : MACROS:
0000 68 :
0000 69 :
0000 70 : .MACRO HOOK,LOC,TARGET :
0000 71 : .LONG LOC :
0000 72 : JMP @#TARGET :
0000 73 : .BLKB 6 ; Normal VMS contents of hook location
0000 74 : .ENDM HOOK ;
0000 75 :
0000 76 : .MACRO HOOKJSB,LOC,TARGET :
0000 77 : .LONG LOC :
0000 78 : JSB @#TARGET :
0000 79 : .BLKB 6 ; Normal VMS contents of hook location
0000 80 : .ENDM HOOKJSB ;
0000 81 :
0000 82 :
0000 83 : EQUATED SYMBOLS:
0000 84 :
0000 85 :
0000 86 : $CLIMSGDEF ; Define CLI error messages
0000 87 : $DSCDEF ; Define string descriptor fields
0000 88 : $DYNDEF ; Define dynamic structure types
0000 89 : $IPLDEF ; Define interrupt priority levels
0000 90 : $IRPDEF ; Define structure header fields
0000 91 : $LCKDEF ; Lock bit definitions
0000 92 : $MPMDEF ; Define MA780 registers
0000 93 : $MPSDEF ; Define secondary processor states
0000 94 : $NDTDEF ; Define nexus type codes
0000 95 : $PCBDEF ; Process control block definitions
0000 96 : $PHDDEF ; Process header definitions
0000 97 : $PRDEF ; Define processor register numbers
0000 98 : $PTEDEF ; Define page table entry format
0000 99 : $RPBDEF ; Define restart param block offsets
0000 100 : $SSDEF ; Define system error messages
0000 101 : $STATEDEF ; State definitions
0000 102 : $VADEF ; Define virtual address fields
0000 103 :
0000 104 :
0000 105 :
0000 106 : OWN STORAGE:
0000 107 :
00000000 108 : .PSECT $$$$$$BEGIN,PAGE ; Base PSECT
0000 109 MP$$BEGIN:: ;

```

```

00000000 0000 110 MPSS$GL_POOLDSC::          ; Structure descriptor for MP code
000001F0' 0004 111          .LONG      0          ; Adr of non-paged pool alloc for MP
01F0' 0008 112          .LONG      <<<<MPSS$END-MPSS$BEGIN>+511>@-4>@4> ; Size of pool used
62 000A 113          .WORD      <<<<MPSS$END-MPSS$BEGIN>+511>@-4>@4> ; Structure size
03 000B 114          .BYTE      DYN$C_LOADCODE ; Structure type of loadable code
000000AC'00000014' 000C 115          .BYTE      DYN$C_LC_MP ; Structure sub-type of multi-processing
0014 116 MPSS$HOOKTBL::          ; Addresses to be locked in WS
0014 117          .LONG      HOOKBASE,HOOKEND ;
0014 118          :
0014 119          : The convention for the following logical names is:
0014 120          :
0014 121          : 1) All hooks in the exec are prefixed by MPHS
0014 122          : 2) If the entire routine is replaced, then the
0014 123          : rest of the hook name is the same as the normal
0014 124          : routine name
0014 125          : 3) If there are only a few lines of new MP code to
0014 126          : be inserted, the hook name ends with HK and the
0014 127          : continuation point (if any) hook name ends with CONT
0014 128          : 4) All MP routines are prefixed with MPSS$
0014 129          : 5) If the MP routine entirely replaces an exec routine,
0014 130          : then the rest of the MP routine name is the same as
0014 131          : the normal routine name
0014 132          : 6) If there are only a few lines of new MP code, then
0014 133          : the rest of the MP routine name is a new name
0014 134          :
0014 135 HOOKBASE:          ; Base of hook table
0014 136          HOOK      MPH$SCHED,MPSS$SCHED ;
0024 137          HOOK      MPH$RESCHED,MPSS$RESCHED ; Reschedule interrupt
0034 138          HOOK      MPH$QAST,MPSS$QAST ; Queue AST
0044 139          HOOK      MPH$INVALIDHK,MPSS$INVALID ; Invalidate TB
0054 140          HOOK JSB MPH$BUGCHKHK,MPSS$BUGCHECK ; Check for 2ndary during bugchk
0064 141          HOOK      MPH$ASTDELHK,MPSS$ASTSCHEDCHK ; Resched process to 2ndary chk
0074 142          HOOK      MPH$NEWLVLHK,MPSS$ASTNEWLVL ; Set new PR ASTLVL
00000000 0084 143          .LONG      0 ; End of JMP/JSB type hooks
0088 144 SCB_IPL14:          ; Hook for SCB IPL=14 vector
00000000 0088 145          .LONG      0 ; Adr of longword
00000000 008C 146          .LONG      0 ; Old contents of longword
0090 147 SCB_IPL16:          ; Hook for SCB IPL=16 vector
00000000 0090 148          .LONG      0 ; Adr of longword
00000000 0094 149          .LONG      0 ; Old contents of longword
0098 150 SCB_VEC94:          ; Hook for XDELTA (SOFTINT 5)
00000000 0098 151          .LONG      0 ; Adr of longword
00000000 009C 152          .LONG      0 ; Old contents of longword
00A0 153 SCB_VECBC:          ; Hook for SOFTINT F
00000000 00A0 154          .LONG      0 ; Adr of longword
00000000 00A4 155          .LONG      0 ; Old contents of longword
00000000 00A8 156          .LONG      0 ; Empty hook at ends table
00AC 157 HOOKEND:          ;
00000000 158          .PSECT   _END,PAGE ; End PSECT
0000 159 MPSS$END::          ;
0000 160          :
00000000 161          .PSECT   __MPLOAD, LONG ;
0000 162          :
0000 163 LOCKRANGE:          ; Addresses to be locked in WS
00000525'000004E1' 0000 164          .LONG      LOCKSTART,LOCKEND ;
0008 165          :
0008 166 STOPRANGE:          ; Addresses to be locked in WS

```

```
000005DC'00000555' 0008 167 .LONG STOPSTART,STOPEND ;
0010 168
0010 169 :
0010 170 : Output buffer for SHOW CPU displays.
0010 171 :
00000000 0010 172 OUTPUT_LENGTH: .LONG 0
0014 173
0000005A 0014 174 OUTPUT_BUFFER:
0014 175 .BLKB 70
005A 176
005A 177 OUTPUT_BUF_DSC:
00000046 005A 178 .LONG 70
00000014' 005E 179 .ADDRESS OUTPUT_BUFFER
0062 180
0062 181 DCL_LINE_DSC:
00000000 0062 182 .LONG 0
00000000 0066 183 .LONG 0
006A 184
006A 185 STATE_VALUE:
00000000 006A 186 .LONG 0
006E 187
006E 188
006E 189 :
006E 190 : Array of ascid descriptor addresses for secondary
006E 191 : processor states. Ordered from minimum to maximum
006E 192 : value of the state. Indexed via numeric state value - 1.
006E 193 :
006E 194 STATES:
000000CB' 006E 195 .ADDRESS IDLE_STATE_DSC
000000BF' 0072 196 .ADDRESS DROP_STATE_DSC
000000A4' 0076 197 .ADDRESS BUSY_STATE_DSC
000000B0' 007A 198 .ADDRESS EXEC_STATE_DSC
00000086' 007E 199 .ADDRESS INIT_STATE_DSC
00000098' 0082 200 .ADDRESS STOP_STATE_DSC
0086 201
0086 202 INIT_STATE_DSC:
41 49 54 49 4E 49 0000008E'010E0000' 0086 203 .ASCID /INITIALIZE/
45 5A 49 4C 0094
0098 204 STOP_STATE_DSC:
50 4F 54 53 000000A0'010E0000' 0098 205 .ASCID /STOP/
00A4 206 BUSY_STATE_DSC:
59 53 55 42 000000AC'010E0000' 00A4 207 .ASCID /BUSY/
00B0 208 EXEC_STATE_DSC:
54 55 43 45 58 45 000000B8'010E0000' 00B0 209 .ASCID /EXECUTE/
45 00BE
00BF 210 DROP_STATE_DSC:
50 4F 52 44 000000C7'010E0000' 00BF 211 .ASCID /DROP/
00CB 212 IDLE_STATE_DSC:
45 4C 44 49 000000D3'010E0000' 00CB 213 .ASCID /IDLE/
00D7 214 GET_VERB_DSC:
42 52 45 56 24 000000DF'010E0000' 00D7 215 .ASCID /$VERB/
00E4 216 GET_LINE_DSC:
45 4E 49 4C 24 000000EC'010E0000' 00E4 217 .ASCID /$LINE/
00F1 218
00F1 219 STATE_CTL_DSC:
74 41 5F 21 2F 21 000000F9'010E0000' 00F1 220 .ASCID \!/_Attached processor is in the !AS state.\
65 63 6F 72 70 20 64 65 68 63 61 74 00FF
```

MPLOAD
V04-000

F 7

- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

Page 5
(1)

MPL
VO4

```
74 20 6E 69 20 73 69 20 72 6F 73 73 010B
65 74 61 74 73 20 53 41 21 20 65 68 0117
      2E 0123
      0124 221
      0124 222 ILSTATE_CTL_DSC:
74 41 5F 21 2F 21 0000012C'010E0000' 0124 223
65 63 6F 72 70 20 64 65 68 63 61 74 0132
61 20 6E 69 20 73 69 20 72 6F 73 73 013E
74 73 20 6C 61 67 65 6C 6C 69 20 6E 014A
      4C 58 21 20 66 6F 20 65 74 61 0156
      0160 224
      0160 225
      0160 226
```

223 .ASCID \!/_Attached processor is in an illegal state of !XL\

.LIST MEB ; Show macro expansions


```

41 8F 62 91 019E 285      CMPB      (R2),#^A\A\      ; Check for START verb
                                BEQL      START_CPU      ; Br to execute START/CPU command
4F 8F 62 91 01A2 286      BEQL      START_CPU      ;
                                CMPB      (R2),#^A\O\      ; Check for STOP verb
                                BEQL      STOP_CPU       ; Br to execute STOP/CPU command
                                01AA 289 ERRORX3:
50 00038090 8F D0 01AA 290      MOVL      #CLIS_IVVERB,R0      ; Report unrecognized command
                                01B1 291 ERRORX4:
                                04 01B1 292      RET              ; Exit with error status
                                01B2 293 START_CPU:
                                0078 31 01B2 294      BRW      MPSSLOAD      ; START/CPU DCL command execution
                                01B5 295      ; Continue loading MP code
                                01B5 296 STOP_CPU:
                                037D 31 01B5 297      BRW      MPSSUNLOAD      ; STOP/CPU DCL command execution
                                01B8 298      ; STOP/CPU DCL command execution
                                01B8 299      ;
                                01B8 300      ; GETDATA - This routine goes into kernel mode and copies
                                01B8 301      ; needed data into a local buffer.
                                01B8 302      ;
                                01B8 303 GETDATA:
                                0000 01B8 304      .WORD      0              ; Entry mask
51 50 01 9A 01BA 305      MOVZBL   #SS$ NORMAL,R0      ; Assume success
00000000'GF D0 01BD 306      MOVL      G^EXE$GL_MP,R1      ; Get adr of loaded MP code
                                9A 13 01C4 307      BEQL      ERRORX2       ; Br if MP not loaded
FE9D CF 0000'C1 D0 01C6 308      MOVL      MPSS$GL_STATE(R1),STATE_VALUE ; Copy state variable
                                04 01CD 309      RET              ; Exit from kernel mode routine
                                01CE 310      ;
                                01CE 311      ; The command was SHOW CPU. Change into kernel mode to
                                01CE 312      ; access the state variable for the secondary processor.
                                01CE 313      ;
                                01CE 314 SHOW_CPU:
                                01CE 315      $CMKRNL_S GETDATA      ; Acquire secondary state
                                DD 01CE      _PUSHL      #0
                                E5 AF DF 01D0      _PUSHAL   GETDATA
00000000'GF D4 50 E9 01D3      CALLS    #2,G^SYSS$CMKRNL
                                01DA 316      BLBC      R0,ERRORX4      ; Exit with error status
                                01DD 317      ;
                                01DD 318      ; Now format and output data.
                                01DD 319      ;
                                01DD 320 10$:
52 FF43 CF 9E 01DD 321      MOVAB    ILSTATE_CTL_DSC,R2      ; Assume illegal state
50 FE84 CF D0 01E2 322      MOVL      STATE_VALUE,R0      ; Get state value
                                01 50 D1 01E7 323      CMPL     R0,#MPSS$K_IDLESTATE ; Is this at least minimum value?
                                06 12 19 01EA 324      BLSS    20$              ; Br if bad value
                                06 50 D1 01EC 325      CMPL     R0,#MPSS$K_STOPSTATE  ; Is this at least maximum value?
                                0D 14 01EF 326      BGTR    20$              ; Br if bad value
50 FE76 CF40 D0 01F1 327      DECL     R0              ; Convert value to an index
52 FEF4 CF 9E 01F3 328      MOVL      STATES[R0],R0      ; Get address of ascii state text
                                01F9 329      MOVAB    STATE_CTL_DSC,R2      ; Output ascii state name
                                01FE 330 20$:      $FAO_S      CTRSTR=(R2),-
                                01FE 331      OUTLEN=OUTPUT_LENGTH,-
                                01FE 332      OUTBUF=OUTPUT_BUF_DSC,-
                                01FE 333      P1=R0              ; Format output line
                                50 DD 01FE      _PUSHL     R0
                                FE56 CF 7F 0200      _PUSHAQ   OUTPUT_BUF_DSC
                                FE08 CF 3F 0204      _PUSHAW   OUTPUT_LENGTH
00000000'GF 62 7F 0208      _PUSHAQ   (R2)
                                04 FB 020A      CALLS    #$$T2,G^SYSS$FAO

```

MP
Syl
MP
MP
MP
MP
MP
MP
ND
OU
OU
PCI
PCI
PHI
PR
PR
PTI
PTI
RPI
RPI
RPI
RPI
RPI
RPI
RPI
SCI
SCI
SCI
SCI
SCI
SCI
SCI
SCI
SE
SHI
SS
SS
SS
ST
ST
ST
ST
ST
ST
ST
SY
SY
VA

	9D 50	E9	0211	334	BLBC	RO,ERRORX4	; Exit with error status
FE3F CF	FDF8 CF	D0	0214	335	MOVL	OUTPUT_LENGTH,OUTPUT_BUF,DSC	; Initialize output buffer dsc
	FE3B CF	7F	021B	336	PUSHAQ	OUTPUT_BUF,DSC	; Dsc adr for output buffer
00000000	'GF 01	FB	021F	337	CALLS	#1,G^LIB\$POT_OUTPUT	; Output secondary processor state
	88 50	E9	0226	338	BLBC	RO,ERRORX4	; Exit with error status
			0229	339			
			0229	340	EXIT:		
50	01	9A	0229	341	MOVZBL	#SS\$_NORMAL,RO	; Exit with success code
		04	022C	342	RET		; Exit
			022D	343	.DSABL	LSB	

```

022D 345      .SBTTL
022D 346      :++
022D 347      : Functional Description:
022D 348      :
022D 349      :     MPSS$LOAD is linked together with all of the code required for multi-
022D 350      :     processing. The necessary amount of non-paged pool is allocated
022D 351      :     and rounded up to page boundary. Code is then moved into this
022D 352      :     block of pool. All of this code must be PIC although a limited
022D 353      :     amount of relocation will be done on data cells and the SCB for
022D 354      :     the secondary processor.
022D 355      :
022D 356      : Calling Sequence:
022D 357      :
022D 358      :     BRW     MPSS$LOAD
022D 359      :
022D 360      : Input Parameters:
022D 361      :
022D 362      :     None
022D 363      :
022D 364      : Environment:
022D 365      :
022D 366      :     Executed by the primary processor.
022D 367      :
022D 368      :
022D 369      :--
022D 370
022D 371 MPSS$LOAD::
022D 372      $LKWSET_S      INADR=LOCKRANGE ; Load multi-processing code for START
                                ; Lock critical code into WS
00      DD 022D      PUSHL #0
00      DD 022F      PUSHL #0
FDCB   CF 7F 0231    PUSHAQ LOCKRANGE
00000000'GF 03 FB 0235    CALLS #3,G^SYSS$LKWSET
21 50  E9 023C 373    BLBC  RO,ERRORX1 ; Exit if unable to lock pages
                                ; Lock critical data into WS
00      DD 023F      $LKWSET_S      INADR=MPSS$HOOKTBL
00      DD 0241      PUSHL #0
00000000C'EF 00 DD 0243    PUSHL #0
00000000'GF 03 FB 0249    PUSHAQ MPSS$HOOKTBL
OD 50  E9 0250 375    BLBC  RO,ERRORX1 ; Br if error
                                ; Execute kernel routine
00      DD 0253      $CMKRNL_S W^MPSS$LOADK
0279'CF 02 FB 0259    PUSHL #0
00000000'GF 02 FB 0259    PUSHAL W^MPSS$LOADK
                                CALLS #2,G^SYSS$CMKRNL
0260 377 ERRORX1:
04 0260 378      RET ; Return
0261 379
0261 380
50 00000000'8F 00 0261 381 LOCAL_MEM_ERR:
04 0268 382      MOVL #ERR$_LCLMEMUSED,RO ; Local memory cannot be used for MP
0269 383      RET
0269 384
50 00000000'8F 00 0269 385 MA780_NOT_USED:
04 0269 386      MOVL #ERR$_MA780_REQ,RO ; MA780 memory required for MP
0270 387      RET
0271 388
50 00000000'8F 00 0271 389 MA780_CNCT_ERR:
0271 390      MOVL #ERR$_SHMDBLUSE,RO ; MA780 memory used for MP and MA780

```

```

04 0278 391 RET ; system interconnect at same time
0279 392
0279 393
0279 394
OFFC 0279 395 MPSS$LOADK:: .WORD ^M<R2,R3,R4,R5,R6,R7,R8,R9,R10,R11> ; Entry mask
0278 396 .ENABL LSB
00000000'GF D5 0278 397 TSTL G^EXE$GL_MP ; Is secondary already started?
A6 12 0281 398 BNEQ EXIT ; Br on yes, don't do anything
00000000'GF D5 0283 399 TSTL G^EXE$GL_SHBLIST ; Is MA780 in use as sys intercnc?
E6 12 0289 400 BNEQ MA780 CNCT ERR ; Br if MA780 already in use
50 00000000'GF D0 028B 401 MOVL G^EXE$GL_RPB,R0 ; Get address of RPB
CA 30 A0 OC E0 0292 402 BBS #RPB$V_USEMPM,RPB$L_BOOTR5(R0),LOCAL_MEM_ERR ; Br if booted with
CD 30 A0 OB E1 0297 403 BBC #RPB$V_MPM,RPB$L_BOOTR5(R0),MA780_NOT_USED ; wrong memory
51 0008'CF 3C 029C 404 MOVZWL W^MPSS$GL_POOLDSC+IRPSW_SIZE,R1 ; Size of loadable code
00000000'GF 16 02A1 405 JSB G^EXE$ALONONPAGED ; Allocate necessary block
02A7 406
02A7 407 .IF DF,MPDBGSWT
02A7 408 SETIPL #0 ;***** Drop IPL for debugging
02A7 409 .ENDC
02A7 410
B6 50 E9 02A7 411 BLBC R0,ERRORX1 ; Exit if none available
50 52 D0 02AA 412 MOVL R2,R0 ; Remember starting address of pool
0000'CF 52 D0 02AD 413 MOVL R2,W^MPSS$GL_POOLDSC ; Assume nothing to return to pool
52 01FF C2 9E 02B2 414 MOVAB 511(R2),R2 ; Round up to page boundary
52 00001FF 8F CA 02B7 415 BICL #^X1FF,R2 ; Set to page boundary
SA 52 D0 02BE 416 MOVL R2,R10 ; Save address of block
00000000'GF 52 D0 02C1 417 MOVL R2,G^EXE$GL_MP ; Set exec pointer to MP code
51 52 50 C3 02C8 418 SUBL3 R0,R2,R1 ; Compute size of unused piece of pool
4F 13 02CC 419 BEQL 10$ ; Br if piece of pool was page-aligned
0A A0 08 A0 51 B0 02CE 420 MOVW R1,IRPSW_SIZE(R0) ; Set size of unused piece
0A A0 0362 8F B0 02D2 421 MOVW #<DYN$C[_C_MP28+DYN$C_LOADCODE],IRPSB_TYPE(R0) ; Set type
20 51 D1 02D8 422 CML R1,#32 ; Is piece too small to bother returning
4C 15 02DB 423 BLEQ 10$ ; Br if too small
0000'CF 52 D0 02DD 424 MOVL R2,W^MPSS$GL_POOLDSC ; Set page-aligned pool adr
0004'CF 51 C2 02E2 425 SUBL2 R1,W^MPSS$GL_POOLDSC+4 ; Set page-aligned pool size
0008'CF 51 C2 02E7 426 SUBL2 R1,W^MPSS$GL_POOLDSC+IRPSW_SIZE ; Set page-aligned size
02FC 427 ASSUME IRPSW_SIZE [E 10
62 0000'CF D0 02EC 428 MOVL W^MPSS$GL_POOLDSC,(R2) ; Initialize enough of pool block
04 A2 0004'CF D0 02F1 429 MOVL W^MPSS$GL_POOLDSC+4,4(R2) ; to allow its deallocate if an
08 A2 0008'CF D0 02F7 430 MOVL W^MPSS$GL_POOLDSC+8,8(R2) ; error exit is required
00000000'GF 16 02FD 431 JSB G^EXE$DEANONPAGED ; Return unused piece of pool
17 50 E8 0303 432 BLBS R0,10$ ; Br if successful
0306 433 DEA_ERR_EXIT:
50 DD 0306 434 PUSHL R0 ; Save error exit status
50 0000'CF D0 0308 435 MOVL W^MPSS$GL_POOLDSC,R0 ; Get address of pool allocated
00000000'GF 16 030D 436 JSB G^EXE$DEANONPAGED ; Release block of pool
50 8ED0 0313 437 POPL R0 ; Restore exit status
00000000'GF D4 0316 438 CLRL G^EXE$GL_MP ; Indicate no MP code loaded
04 031C 439 RET ; Exit with error status
031D 440
031D 441 10$:
50 0000'CF 9E 031D 442 MOVAB W^MPSS$BEGIN,R0 ; Address of start of code segment
59 SA 50 C3 0322 443 SUBL3 R0,R10,R9 ; Relocation offset is difference
0326 444 ;
0326 445 ; The addresses in the SCB for the secondary processor are now relocated
0326 446 ; by adding the relocation value. Any SCB pointer already a system space
0326 447 ; address is correct and need not be relocated.

```

```

51 0200'CF 9E 0326 448 :
50 80 8F 9A 0326 449 : MOVAB W^SCB$AL_BASE+512,R1 ; Get base of SCB
032B 450 : MOVZBL #128,R0 ; Do all 128 vectors
032F 451 : .DSABL LSB
032F 452 SCB_LOOP:
71 032F 453 : TSTL -(R1) ; Is vector in system space?
03 19 0331 454 : BLSS 10$ ; Yes, skip it
61 59 C0 0333 455 : ADDL R9,(R1) ; Other wise relocate pointer to point
F6 50 F5 0336 456 10$: SOBGR R0,SCB_LOOP ; to code segment. Do all 128 vectors
0339 457 :
0339 458 : Locate all the multiport memory controllers and initialize the SCB
0339 459 : vectors for the inter-processor interrupts. The first MA780 is used for
0339 460 : the multi-processing scheduling interrupt while the other MA780s are
0339 461 : vectored to an unexpected interrupt logging routine. The error interrupt
0339 462 : vectors for the MA780s are initialized for the secondary also, while
0339 463 : those for the primary were initialized in the normal VMS boot procedures.
0339 464 :
0339 465 LOC_MPM: ; Initialize vectors for MA780 memories
50 D4 0339 466 : CLRL R0 ; Initialize index
52 0000'CF 9E 033B 467 : MOVAB W^MPSS$INT58,R2 ; Get adr of error interrupt logger
52 59 C0 0340 468 : ADDL R9,R2 ; Relocate for eventual location
52 01 C8 0343 469 : BISL #1,R2 ; Set interrupt stack bit in vector
53 00000000'GF D0 0346 470 : MOVL G^MMG$GL_SBICONF,R3 ; Get address of SBI config array
54 0000'CF 9E 034D 471 : MOVAB W^MPSS$AL_MPMBASE,R4 ; Get address of first MA780 base
55 00000000'GF D0 0352 472 : MOVL G^EXE$GL_SCB,R5 ; Base address for primary SCB
56 00000000'GF D0 0359 473 : MOVL G^EXE$GL_RPB,R6 ; Get base of RPB
57 0000'CF DE 0360 474 : MOVAL W^SCB$AL_BASE,R7 ; Base address for secondary SCB
0365 475 :
10 00000000'GF 00' E1 0365 476 : BBC S^#EXE$V SSINHIBIT,G^EXE$GL_FLAGS,5$ ; If sys srv are being
44 A7 00000000'GF DE 036D 477 : MOVAL G^EXE$CMODEXECX,^X44(R7) ; inhibited, then revector the
40 A7 00000000'GF DE 0375 478 : MOVAL G^MPSS$CMODKRNIX,^X40(R7) ; entry points for CHMK and CHME
037D 479 5$:
037D 480 :
51 0090 C640 03 8B 037D 481 10$: BICB3 #3,RPB$B CONFREG(R6)[R0],R1 ; Get a type byte
51 40 8F 91 0384 482 : CMPB #NDT$_MPM0,R1 ; Is it a multiport memory?
7D 12 0388 483 : BNEQ 15$ ; Br if not an MA780
038A 484 :
58 0100 C740 DE 038A 485 : MOVAL 256(R7)[R0],R8 ; Compute address of first vector
40 A8 52 D0 0390 486 : MOVL R2,64(R8) ; Set IPL=X15 vector (error interrupt)
00C0 C8 52 D0 0394 487 : MOVL R2,192(R8) ; Set IPL=X17 vector (error interrupt)
0399 488 :
0000'CF D5 0399 489 : TSTL W^MPSS$AL_MPMBASE ; Is this the first MA780?
51 12 039D 490 : BNEQ 12$ ; Br if not
039F 491 :
51 0000'CF 9E 039F 492 : MOVAB W^MPSS$SINTSR,R1 ; Get adr of secondary interrupt rtn
51 59 C0 03A4 493 : ADDL R9,R1 ; Relocate for eventual location
51 01 C8 03A7 494 : BISL #1,R1 ; Set interrupt stack bit in vector
68 51 D0 03AA 495 : MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)
0080 C8 51 D0 03AD 496 : MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)
03B2 497 :
51 0000'CF 9E 03B2 498 : MOVAB W^MPSS$PINTSR,R1 ; Get adr of primary interrupt routine
51 59 C0 03B7 499 : ADDL R9,R1 ; Relocate for eventual location.
51 01 C8 03BA 500 : BISL #1,R1 ; Set interrupt stack bit in vector
58 0100 C540 DE 03BD 501 : MOVAL 256(R5)[R0],R8 ; Compute address of first vector
00000088'EF 58 D0 03C3 502 : MOVL R8,SCB IPL14 ; Remember adr for unload logic
0000008C'EF 68 D0 03CA 503 : MOVL (R8),SCB_IPL14+4 ; Remember contents for unload
68 51 D0 03D1 504 : MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)

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00000090'EF 0080 C8 9E 03D4 505 MOVAB 128(R8),SCB_IPL16 ; Remember adr for unload logic
00000094'EF 0080 C8 DO 03DD 506 MOVL 128(R8),SCB_IPL16+4 ; Remember contents for unload
0080 C8 51 DC 03E6 507 MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)
16 11 03EB 508 BRB 14$ ; Continue with common code
FF8D 31 03ED 509 ;
03ED 510 11$: BRW 10$ ; Branch assist
03F0 511
51 0000'CF 9E 03F0 512 12$: MOVAB W*MPSS$UNEXPINT,R1 ; Get adr of unexpected interrupt rtn
51 59 CO 03F5 513 ADDL R9,R1 ; Relocate for eventual location
51 01 C8 03F8 514 BISL #1,R1 ; Set interrupt stack bit in vector
68 51 DO 03FB 515 MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)
0080 C8 51 DO 03FE 516 MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)
0403 517
84 6340 DO 0403 518 14$: MOVL (R3)[R0],(R4)+ ; Remember adr for this MA780s registers
0407 519
E2 50 10 F2 0407 520 15$: AOBLS #16,R0,11$ ; Try all 16
040B 521
50 0000'CF DO 040B 522 MOVL W*MPSS$AL_MPMBASE,R0 ; Get base of MA780 registers
08 12 0410 523 BNEQ FOUND_MPM ; Found at least one MA780
50 037C 3F 3C 0412 524 MOVZWL #SS$ SHMNOTCNCT,R0 ; Indicate failure to find an MA780
FECC 31 0417 525 BRW DEA_ERR_EXIT ; Error exit with pool deall
041A 526 FOUND_MPM:
51 0000'CF 9E 041A 527 MOVAB W*MPSS$RESCHEDIPL5,R1 ; Get address of primary fork rtn
51 01 C8 041F 528 BISL #1,R1 ; Set interrupt stack bit in vector
00000098'EF 0094 C5 9E 0422 529 MOVAB ^X94(R5),SCB_VEC94 ; Remember adr for unload logic
0000009C'EF 0094 C5 DO 042B 530 MOVL ^X94(R5),SCB_VEC94+4 ; Remember contents for unload
000000A0'EF 00BC C5 9E 0434 531 MOVAB ^XBC(R5),SCB_VECBC ; Remember adr for unload logic
000000A4'EF 00BC C5 DO 043D 532 MOVL ^XBC(R5),SCB_VECBC+4 ; Remember contents for unload
00BC C5 0094 C5 DO 0446 533 MOVL ^X94(R5),^XBC(R5) ; Make XDELTA respond to softint ^XF
0094 C5 51 59 C1 044D 534 ADDL3 R9,R1,^X94(R5) ; Relocate for eventual location & store
0000'CF 20 C1 0453 535 ADDL3 #MPMSL_IIR,W*MPSS$AL_MPMBASE,- ; Compute address of
0000'CF 0458 536 W*MPSS$GL_MPMIIR ; interrupt request register
52 60 DO 045B 537 ; Interrupt routines
52 00 EF 045E 538 MOVL MPMSL_CSR(R0),R2 ; Read configuration register
52 52 02 0460 539 EXTZV #MPMSV_CSR_PORT,- ; Get port number
0463 540 #MPMS$CSR_PORT,R2,R2 ;
0463 541
0000'CF 53 52 10 C1 0463 542 ADDL3 #MPMSV_IIR_CTL,R2,R3 ; Set to control field
00001111 8F 53 78 0467 543 ASHL R3,#^XT111,W*MPSS$GL_PRIMSKT ; Generate interrupt trigger mask
0000'CF 52 04 C4 0471 544 MULL #4,R2 ; Compute bit position for trigger
0000'CF 0F 52 78 0474 545 ASHL R2,#^XF,W*MPSS$GL_PRIMSKC ; Align and store mask for clear
047A 546 ;
047A 547 ; Compute the physical addresses for the secondary SCB and the Secondary
047A 548 ; initialization routine starting address.
047A 549 ;
047A 550 SET_PHYS:
55 00000000'GF DO 047A 551 MOVL G*MMG$GL_SPTBASE,R5 ; Get base of SPT
51 0000'CF 9E 0481 552 MOVAB W*SCB$AL_BASE,R1 ; VA of Secondary processor SCB
51 51 59 CO 0486 553 ADDL R9,R1 ; Relocate to eventual location
51 15 09 EF 0489 554 EXTZV #VASV_VPN,#VASS_VPN,R1,R1 ; Get virtual page number
50 50 50 6541 DO 048E 555 MOVL (R5)[R1],R0 ; fetch PTE for it
50 50 15 00 EF 0492 556 EXTZV #PTESV_PFN,#PTESS_PFN,R0,R0 ; Isolate page number
0000'CF 50 09 78 0497 557 ASHL #9,R0,W*MPSS$GL_SCBB ; Save physical SCB address
51 0000'CF 9E 049D 558 MOVAB W^EXE$MPSTART,R1 ; VA of initialization routine
51 51 59 CO 04A2 559 ADDL R9,R1 ; Relocate to eventual location
51 15 09 EF 04A5 560 EXTZV #VASV_VPN,#VASS_VPN,R1,R1 ; Get virtual page number
50 6541 DO 04AA 561 MOVL (R5)[R1],R0 ; fetch PTE for it

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50  50  15  00  EF  04AE  562      EXTZV  #PTESV PFN,#PTES PFN,R0,R0 ; Isolate page number
   10 A6  50  09  78  04B3  563      ASHL   #9,R0,RPBSL_HALTPC(R6) ; Save starting physical address
                                04B8  564      ;
                                04B8  565      ; Relocate some stray locations
                                04B8  566      ;
                                04B8  567      MISC_RELOC:
00000000'EF  59  CO  04B8  568      ADDL   R9,XDELIBRK           ; Address for initial breakpoint
00000000'EF  59  CO  04BF  569      ADDL   R9,MPSS$GL_STRTVA     ; Address for jump into S0 space
00000000'EF  59  CO  04C6  570      ADDL   R9,MPSS$GL_ISP       ; Interrupt stack for secondary
                                04CD  571      ;
                                04CD  572      ; Remember the time and date that this code was loaded. This field
                                04CD  573      ; is used by the MONITOR utility to determine if the multi-processing
                                04CD  574      ; code has been reloaded during its last sampling interval (and therefore,
                                04CD  575      ; the cpu time accumulation cells have been re-initialized).
                                04CD  576      ;
0000'CF  00000000'GF  7D  04CD  577      MOVQ   G^EXES$GQ_SYSTIME,W^MPSS$GQ_MPSTRTIM ; Get time in 64 bits
                                04D6  578      ;
                                04D6  579      ; Now move the code into the pool segment after all relocation is done.
                                04D6  580      ;
                                04D6  581      MOVE_CODE:
6A  5B  0000'8F  3C  04D6  582      MOVZWL #<MPSS$END-MPSS$BEGIN>,R11 ; Size of MP code in bytes
   0000'CF  5B  28  04DB  583      MOVCS  R11,W^MPSS$BEGIN,(R10) ; Move code to allocated pool space
                                04E1  584      ;
                                04E1  585      .IF   DF,MPDBG$SWT
                                04E1  586      NOP                               ;***** Instruction for debug breakpoint
                                04E1  587      .ENDC
                                04E1  588      ;
                                04E1  589      ;
                                04E1  590      ; Begin locked down code that will execute at IPL=31 to actually
                                04E1  591      ; install needed hooks into the running system.
                                04E1  592      ;
                                04E1  593      LOCKSTART:
                                04E1  594      SETIPL #31
                                04E1  595      MTPR  #31,S^#PRS_IPL
12  1F  DA  04E1  595      JSB   G^INIS$WRITABLE       ; Set writable for installing hooks
55  00000000'GF  16  04E4  596      MOVAB HOOKBASE,R5           ; Get base of hook table
51  55  59  C1  04F1  597      ADDL3 R9,R5,R1              ; Get address of loaded mp code
   50  85  D0  04F5  598 10$:  MOVL  (R5)+,R0              ; Fetch address to install hook
   17  13  04F8  599      BEQL  20$                   ; Done if address is zero
   OA  A1  60  B0  04FA  600      MOVW  (R0),10(R1)           ; Save normal VMS contents for STOP/CPU
   80  85  B0  04FE  601      MOVW  (R5)+,(R0)+          ; Move JMP opcode + operand specifier
   OC  A1  60  D0  0501  602      MOVL  (R0),12(R1)           ; Save normal VMS contents for STOP/CPU
80  85  59  C1  0505  603      ADDL3 R9,(R5)+,(R0)+       ; Set address
   55  06  C0  0509  604      ADDL2 #6,R5                 ; Point to next hook
   51  10  C0  050C  605      ADDL2 #16,R1                ; Point to next hook
   E4  11  050F  606      BRB   10$                   ; Continue installing hooks
   0003  31  0511  607 20$:  BRW   HOOKS_DONE           ; Branch assist for hooks completed
                                0514  608      ;
                                0514  609      ; This code is loaded into the RPB. It is used as a safe place for
                                0514  610      ; the secondary to wait while the primary does a bugcheck. The first
                                0514  611      ; longword is modified by the primary after it reboots.
                                0514  612      ;
                                0514  613      .ALIGN LONG
                                0514  614      RPB_BUGCHK=-4           ; Address of longword that is modified
                                0514  615      ; by primary and secondary
                                0514  616      MPSS$RPB_WAIT::
F9 BF  17  0514  617      JMP   @RPB_BUGCHK           ; RPB loop for secondary to execute

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00000003 0517 618
          0517 619 RPB_LOOPSIZ = .-MPSSRPB_WAIT          ; Number of bytes for code for RPB loop
          0517 620
          0517 621 :
          0517 622 : Now load loop code into the RPB for bugcheck. This must be loaded
          0517 623 : in two steps. First, the loop code is loaded and then the loop address.
          0517 624 :
          0517 625 HOOKS_DONE:
0100 C6   FFF8 CF   03   28 0517 626          MOVCL #RPB_LOOPSIZ,W^MPSSRPB_WAIT,RPBSB_WAIT(R6) ; Load JMP loop
          00FC C6   10 A6  D0 051F 627          MOVL  RPBSL_HALTPC(R6),RPBSL_BUGCHK(R6) ; Now start the secondary
          0525 628                                     ; executing at EXE$MPSTART (phys. adr)
          0525 629 :
          0525 630 LOCKEND:                               ; End of locked code
          0525 631 :
          0525 632 : Installation of the multi-processing code is now complete
          0525 633 :
          0525 634 INSTALL_DONE:
00000000'GF 16 0525 635          JSB   G^INISRONLY          ; Reset protection on system pages
          12 00   DA 0528 636          SETIPL #0          ; Drop IPL
          50 01   D0 052E 637          BSBW  MTPR #0,S^#PRS_IPL
          04 0534 638          MOVL  MPSS$MAINIT          ; Initialize MA780 for interrupts
          0531 639          RET          ; Set status to success
          0534 639          RET          ; and return

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0535 641 .SBTTL MPSS$UNLOAD - STOP/CPU DCL command
0535 642
0535 643 :++
0535 644 : Functional Description:
0535 645 :
0535 646 : MPSS$UNLOAD is linked together with all of the code required for
0535 647 : multi-processing. This routine causes the secondary processor
0535 648 : to halt and then unloads the multi-processing code (i.e., restores
0535 649 : all the executive hook locations to their original values and
0535 650 : restores the SCB to its single processor VMS values.
0535 651 :
0535 652 : Calling Sequence:
0535 653 :
0535 654 : BRW MPSS$UNLOAD
0535 655 :
0535 656 : Input Parameters:
0535 657 :
0535 658 : EXE$GL_MP - Points to multi-processing code loaded in pool
0535 659 : EXE$GL_RPB - Points to RPB
0535 660 :
0535 661 : Environment:
0535 662 :
0535 663 : Executed by the primary processor.
0535 664 :
0535 665 :
0535 666 :--
0535 667
0535 668 MPSS$UNLOAD::
0535 669 $LKWSET_S INADR=STOPRANGE ; Unload multi-processing code for STOP
                                ; Lock critical code into WS
                                PUSHL #0
                                PUSHL #0
                                PUSHAQ STOPRANGE
                                CALLS #3,G^SYSS$LKWSET
                                BLBC RO,EXIT2 ; Exit if unable to lock pages
                                $CMKRNL_S W^MPSS$UNLOADK ; Execute kernel routine
                                PUSHL #0
                                PUSHAL W^MPSS$UNLOADK
                                CALLS #2,G^SYSS$CMKRNL
0554 672 EXIT2:
0554 673 RET ; Return
0555 674
0555 675
0555 676 STOPSTART:
0555 677
OFFC 0555 678 MPSS$UNLOADK:: .WORD ^M<R2,R3,R4,R5,R6,R7,R8,R9,R10,R11> ; Entry mask
0557 679 SETIPL #IPL$ SYNCH ; Synchronize on primary
                                MTPR #IPL$ SYNCH,S^#PR$ IPL
                                #SS$ NORMAL,RO ; Assume success
                                G^EXE$GL_MP,R10 ; Is multi-proc code loaded?
                                BNEQ 5$ ; Br on yes, continue unloading
                                BRW 100$ ; Branch assist
                                4$: BBSSI #MPSS$V_STOPREQ,MPSS$GL_STOPFLAG(R10),4$ ; Set STOP request flg
                                5$: BBSSI #LCK$V_INTERLOCK,MPSS$GL_INTERLOCK(R10),15$ ; Flush cache
                                10$: CMPL MPSS$GL_STATE(R10),#MPSS$R_INITSTATE ; Is secondary active?
                                15$: BGEQ 50$ ; Br if not active, no process to return
                                JSB MPSS$INTSCND(R10) ; Interrupt secondary with STOP request
                                20$: BBCC! #MPSS$V_STOPACK1,MPSS$GL_STOPFLAG(R10),20$ ; Wait for secondary
0557 680 MOVZBL
055A 681 MOVL
055D 682 BNEQ
0564 683 4$: BRW
0566 684 5$: BBSSI
0569 685 10$: BBSSI
056F 686 15$: CMPL
0575 687 BGEQ
057A 688 JSB
057C 689 20$: BBCC!
0580

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00 0000'CA 00 E6 0586 690 BBSSI #LCK$V_INTERLOCK,MPSSGL_INTERLOCK(R10),30$ ; Flush cache
01 0000'CA 28 D1 058C 691 30$: Cmpl MPSSGL_STATE(R10),#MPSSR_IDLESTATE ; Is secondary active?
                                13 0591 692 BEQL 50$ ; Br if not active, no process to return
                                0593 693 ;
                                0593 694 ; Return process executing on the secondary to the scheduling queues.
                                0593 695 ;
51 0000'CA D0 0593 696 MOVL MPSSGL_CURPCB(R10),R1 ; Get PCB address for process
52 0B A1 9A 0598 697 MOVZBL PCB$B_PRI(R1),R2 ; Get current priority of process
00 00000000'GF 52 E2 059C 698 BBSS R2,G^SCH$GL_COMQS,40$ ; Indicate something in sched queue
2C A1 0C B0 05A4 699 40$: MOVW #SCH$C_COM,PCB$W_STATE(R1) ; Indicate process is computable
53 00000000'GF 42 7E 05A8 700 MOVAQ G^SCH$AQ_COM[ER2],R3 ; Get tail of queue
93 61 0E 05B0 701 INSQUE (R1)@(R3)+ ; Place process in scheduling queue
0000'CA 06 D0 05B3 702 MOVL #MPSSK_STOPSTATE,MPSSGL_STATE(R10) ; Set secondary stopped
14 03 DA 05B8 703 SOFTINT #IPL$_SCHED ; Request primary reschedule
                                05B8 704 MTPR #IPL$_SCHED,S^#PRS_SIRR
                                05BB 704 ;
                                05BB 705 ; Now unload the multi-processing code.
                                05BB 706 ;
0000'CA 06 D0 05BB 707 50$: MOVL #MPSSK_STOPSTATE,MPSSGL_STATE(R10) ; Change INIT state to STOP
0000'CA 16 05C0 708 JSB MPSSUNHOOK(R10) ; Call routine to unhook MP code
12 02 DA 05C4 709 SETIPL #IPL$_ASTDEL ; Lower IPL for deallocate of pool
50 0000'CA D0 05C7 710 MTPR #IPL$_ASTDEL,S^#PRS_IPL
00000000'GF 16 05CC 711 MOVL MPSSGL_POOLDSC(R10),R0 ; Set address of block to return
03 50 E9 05D2 712 JSB G^EXE$DEANONPAGED ; Return block of nonpaged pool
50 01 9A 05D5 713 BLBC R0,100$ ; Branch if error
12 00 DA 05D8 714 100$: MOVZBL #SS$_NORMAL,R0 ; Return success code
04 05D8 714 SETIPL #0 ; Restore IPL
05DB 715 MTPR #0,S^#PRS_IPL
05DC 716 RET ;
05DC 717 STOPEND:

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05DC 719 .SBTTL MPSS$UNHOOK - Unhook multi-processing code from system
05DC 720
05DC 721 :++
05DC 722 : Functional Description:
05DC 723 :
05DC 724 : MPSS$UNHOOK is a part of the loadable multi-processing code.
05DC 725 : It unhooks the multi-processing code from the VMS system and
05DC 726 : resets the system to be a single processor 11/780, executing
05DC 727 : a vanilla VMS system.
05DC 728 :
05DC 729 : This code is invoked for two reasons: 1) a STOP/CPU DCL command
05DC 730 : and 2) an invalidate request time-out. It must be loaded into
05DC 731 : pool due to the latter usage.
05DC 732 :
05DC 733 : Calling Sequence:
05DC 734 :
05DC 735 : JSB MPSS$UNHOOK
05DC 736 :
05DC 737 : Input Parameters:
05DC 738 :
05DC 739 : R10 - address of multi-processing code in non-paged pool
05DC 740 :
05DC 741 : Environment:
05DC 742 :
05DC 743 : Executed by the primary processor.
05DC 744 :
05DC 745 : Side-effects:
05DC 746 :
05DC 747 : R0,R1 destroyed. EXE$GL_MP is cleared.
05DC 748 :
05DC 749 :--
05DC 750
00000000 751 .PSECT $AEXNONPAGED, LONG
0000 752 MPSS$UNHOOK:
0000 753 DSBINT ; Prevent all system events
7E 12 DB 0000 MFPR S^#PRS IPL, -(SP)
12 1F DA 0003 MTPR #31, S^#PRS IPL
50 00000000'GF 9E 0006 754 MOVAB G^SCH$GL NULLPCB, R0 ; Get address of null process PCB
50 6C A0 D0 000D 755 MOVL PCB$ PHD(R0), R0 ; Get address of null process PHD
38 A0 0000'CA C2 0011 756 SUBL MPSS$G[ NULLCPU(R10), PHD$ CPU$PUTIM(R0) ; Del secondary null time
00000000'GF 16 0017 757 JSB G^INIS$WRITABLE ; Make executive writable
51 0014'CA 9E 001D 758 MOVAB HOOKBASE(R10), R1 ; Get address of exec hook table
50 61 D0 0022 759 60$: MOVL (R1), R0 ; Get address of a hook
50 OD 13 0025 760 BEQL 70$ ; 0 ends the JMP/JSB type hooks
80 0A A1 B0 0027 761 MOVW 10(R1), (R0)+ ; Replace the JMP/JSB opcode
80 0C A1 D0 002B 762 MOVL 12(R1), (R0)+ ; Replace the longword destination
51 10 C0 002F 763 ADDL2 #16, R1 ; Point to next hook in table
51 EE 11 0032 764 BRB 60$ ; Repeat for each hook
51 04 C0 0034 765 70$: ADDL #4, R1 ; Skip the end indicator
50 81 D0 0037 766 80$: MOVL (R1)+, R0 ; Get address of SCB vector changed
60 05 13 003A 767 BEQL 90$ ; 0 ends the SCB vector changes
60 81 D0 003C 768 MOVL (R1)+, (R0) ; Replace SCB vector
00000000'GF D4 0041 769 BRB 80$ ; Repeat for each SCB change
00000000'GF 16 0047 770 90$: CLRL G^EXE$GL_MP ; Reset pointer to multi-proc code
12 8E DA 004D 771 JSB G^INIS$RDONLY ; Restore protection on executive pages
004D 772 ENBINT ; Lower IPL for deallocate of pool
MTPR (SP)+, S^#PRS_IPL

```

MP
Sy

MP
MP
MP
MP
MP
MP
ON
PC
PC
PC
PH
PH
SC

PS
--
\$A
LO

Ph
--
In
Co
Pa
Sy
Pa
Sy
Ps
Cr
As

Th
14
Th
19
10

MPLOAD
V04-000

F 8

- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
MPSS\$UNHOOK - Unhook multi-processing cod 5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

Page 18
(1)

05 0050 773 RSB ; Return to caller
0051 774
0051 775
0051 776 .END MPSS\$DCL

MP
VA

Ma
--
-S
-S
-S
TO
33
Th
MA

MPLOAD
Symbol table

\$ST2	= 00000004			LOCKRANGE	00000000	R	04
BUSY_STATE_DSC	000000A4	R	04	LOCKSTART	000004E1	R	04
CLISGET_VACUE	*****	X	04	LOC_MPM	00000339	R	04
CLIS_IVVERB	= 00038090			MA780_CNCT_ERR	00000271	R	04
DCL_LINE_DSC	00000062	R	04	MA780_NOT_USED	00000269	R	04
DEA_ERR_EXIT	00000306	R	04	MISC_RELOC	000004B8	R	04
DROP_STATE_DSC	000000BF	R	04	MMG\$GL_SBCONF	*****	X	04
DSCSA_POINTER	= 00000004			MMG\$GL_SPTBASE	*****	X	04
DSCSB_CLASS	= 00000003			MOVE_CODE	000004D6	R	04
DSCSK_CLASS_D	= 00000002			MPH\$ASTDELHK	*****	X	02
DYN\$C_LC_MP	= 00000003			MPH\$BUGCHKHK	*****	X	02
DYN\$C_LOADCODE	= 00000062			MPH\$INVALIDHK	*****	X	02
ERRS_CLMEMUSED	*****	X	04	MPH\$NEWLVLHK	*****	X	02
ERRS_MA780_REQ	*****	X	04	MPH\$QAST	*****	X	02
ERRS_SHMDBCUSE	*****	X	04	MPH\$RESCHED	*****	X	02
ERRORX1	00000260	R	04	MPH\$SCHED	*****	X	02
ERRORX2	00000160	R	04	MPM\$L_CSR	= 00000000		
ERRORX3	000001AA	R	04	MPM\$L_IIR	= 00000020		
ERRORX4	000001B1	R	04	MPM\$S_CSR_PORT	= 00000002		
ERRORX5	00000164	R	04	MPM\$V_CSR_PORT	= 00000000		
EXESALONONPAGED	*****	X	04	MPM\$V_IIR_CTL	= 00000010		
EXESMODEEXECX	*****	X	04	MPSSAC_MPMBASE	*****	X	04
EXESDEANONPAGED	*****	X	04	MPSSASTNEWLVL	*****	X	02
EXESGB_CPUTYPE	*****	X	04	MPSSASTSCHEDCHK	*****	X	02
EXESGL_FLAGS	*****	X	04	MPSS\$BEGIN	00000000	RG	02
EXESGL_MP	*****	X	04	MPSS\$BUGCHECK	*****	X	02
EXESGL_RPB	*****	X	04	MPSS\$CMODKRNLY	*****	X	04
EXESGL_SCB	*****	X	04	MPSS\$DCL	00000165	RG	04
EXESGL_SHBLIST	*****	X	04	MPSS\$END	00000000	RG	03
EXESGQ_SYSTIME	*****	X	04	MPSS\$GL_CURPCB	*****	X	04
EXESMPSTART	*****	X	04	MPSS\$GL_INTERLOCK	*****	X	04
EXESV_S\$INHIBIT	*****	X	04	MPSS\$GL_ISP	*****	X	04
EXEC_STATE_DSC	000000B0	R	04	MPSS\$GL_MPMIIR	*****	X	04
EXIT	00000229	R	04	MPSS\$GL_NULLCPU	*****	X	05
EXIT2	00000554	R	04	MPSS\$GL_POOLDSC	00000000	RG	02
FOUND_MPM	0000041A	R	04	MPSS\$GL_PRIMSKC	*****	X	04
GETDATA	000001B8	R	04	MPSS\$GL_PRIMSKT	*****	X	04
GET_LINE_DSC	000000E4	R	04	MPSS\$GL_SCB	*****	X	04
GET_VERB_DSC	000000D7	R	04	MPSS\$GL_STATE	*****	X	04
HOOKBASE	00000014	R	02	MPSS\$GL_STOPFLAG	*****	X	04
HOOKEND	000000AC	R	02	MPSS\$GL_STRTVA	*****	X	04
HOOKS_DONE	00000517	R	04	MPSS\$GQ_MPSTRTIM	*****	X	04
IDLE_STATE_DSC	000000CB	R	04	MPSS\$HOOKTBL	0000000C	RG	02
ILSTATE_CTL_DSC	00000124	R	04	MPSS\$INT58	*****	X	04
INISRDOPLY	*****	X	04	MPSS\$INTSCND	*****	X	04
INISWRITABLE	*****	X	04	MPSS\$INVALID	*****	X	02
INIT_STATE_DSC	00000086	R	04	MPSS\$K_IDLESTATE	= 00000001		
INSTALL_DONE	00000525	R	04	MPSS\$K_INITSTATE	= 00000005		
IPLS_ASTDDEL	= 00000002			MPSS\$K_STOPSTATE	= 00000006		
IPLS_SCHED	= 00000003			MPSS\$LOAD	0000022D	RG	04
IPLS_SYNCH	= 00000008			MPSS\$LOADK	00000279	RG	04
IRPSB_TYPE	= 0000000A			MPSS\$MAINIT	*****	X	04
IRPSW_SIZE	= 00000008			MPSS\$PINTSR	*****	X	04
LCK\$V_INTERLOCK	= 00000000			MPSS\$QAST	*****	X	02
LIB\$POT_OUTPUT	*****	X	04	MPSS\$RESCHED	*****	X	02
LOCAL_MEM_ERR	00000261	R	04	MPSS\$RESCHEDIPL5	*****	X	04
LOCKEND	00000525	R	04	MPSS\$RFB_WAIT	00000514	RG	04

MPLOAD
Symbol table

H 8

- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

MPSS\$SCHED	*****	X	02
MPSS\$INTSR	*****	X	04
MPSS\$UNEXPINT	*****	X	04
MPSS\$UNHOOK	00000000	RG	05
MPSS\$UNLOAD	00000535	RG	04
MPSS\$UNLOADK	00000555	RG	04
MPSSV_STOPACK1	= 00000001		
MPSSV_STOPREQ	= 00000000		
NDT\$ MPMO	= 00000040		
OUTPUT_BUFFER	00000014	R	04
OUTPUT_BUF_DSC	0000005A	R	04
OUTPUT_LENGTH	00000010	R	04
PCBSB_PRI	= 0000000B		
PCBSL_PMD	= 0000006C		
PCBSW_STATE	= 0000002C		
PHDSL_CPUTIM	= 00000038		
PRS_IPL	= 00000012		
PRS_SIRR	= 00000014		
PTESS_PFN	= 00000015		
PTESV_PFN	= 00000000		
RPBSB_CONFREG	= 00000090		
RPBSB_WAIT	= 00000100		
RPBSL_BOOTRS	= 00000030		
RPBSL_BUGCHK	= 000000FC		
RPBSL_HALTPC	= 00000010		
RPBSV_MPM	= 0000000B		
RPBSV_USEMPM	= 0000000C		
RPB_BUGCHK	= 00000510	R	04
RPB_LOOPSIZ	= 00000003		
SCBSAL_BASE	*****	X	04
SCB_IPL14	00000088	R	02
SCB_IPL16	00000090	R	02
SCB_LOOP	0000032F	R	04
SCB_VEC94	00000098	R	02
SCB_VECBC	000000A0	R	02
SCH\$AQ_COMT	*****	X	04
SCH\$C_COM	= 0000000C		
SCH\$GL_COMQS	*****	X	04
SCH\$GL_NULLPCB	*****	X	05
SET_PHYS	0000047A	R	04
SHOW_CPU	000001CE	R	04
SS\$DEVOFFLINE	= 00000084		
SS\$NORMAL	= 00000001		
SS\$SHMNOTCNCT	= 0000037C		
START_CPU	000001B2	R	04
STATES	0000006E	R	04
STATE_CTL_DSC	000000F1	R	04
STATE_VALDE	0000006A	R	04
STOPEND	000005DC	R	04
STOPRANGE	00000008	R	04
STOPSTART	00000555	R	04
STOP_CPU	000001B5	R	04
STOP_STATE_DSC	00000098	R	04
SYSS\$MKNRL	*****	GX	04
SYSS\$FAO	*****	X	04
SYSS\$KWSET	*****	GX	04
VASS_VPN	= 00000015		

VASS_VPN = 00000009
XDELIBRK ***** X 04

+-----+
! Psect synopsis !
+-----+

PSECT name	Allocation	PSECT No.	Attributes
. ABS .	00000000 (0.)	00 (0.)	NOPIC USR CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE
\$AB\$\$	00000000 (0.)	01 (1.)	NOPIC USR CON ABS LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$\$\$\$BEGIN	000000AC (172.)	02 (2.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC PAGE
END	00000000 (0.)	03 (3.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC PAGE
- MPLOAD	000005DC (1500.)	04 (4.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC LONG
\$TEXNONPAGED	00000051 (81.)	05 (5.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC LONG

+-----+
! Performance indicators !
+-----+

Phase	Page faults	CPU Time	Elapsed Time
Initialization	35	00:00:00.08	00:00:00.80
Command processing	136	00:00:00.87	00:00:05.33
Pass 1	464	00:00:17.71	00:00:43.37
Symbol table sort	0	00:00:02.80	00:00:05.53
Pass 2	165	00:00:03.78	00:00:08.57
Symbol table output	22	00:00:00.22	00:00:00.84
Psect synopsis output	3	00:00:00.03	00:00:00.03
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	827	00:00:25.49	00:01:04.47

The working set limit was 1800 pages.
101303 bytes (198 pages) of virtual memory were used to buffer the intermediate code.
There were 100 pages of symbol table space allocated to hold 1786 non-local and 25 local symbols.
781 source lines were read in Pass 1, producing 26 object records in Pass 2.
37 pages of virtual memory were used to define 35 macros.

+-----+
! Macro library statistics !
+-----+

Macro library name	Macros defined
-\$255\$DUA28:[MP.OBJ]MP.MLB;1	4
-\$255\$DUA28:[SYS.OBJ]LIB.MLB;1	15
-\$255\$DUA28:[SYSLIB]STARLET.MLB;2	12
TOTALS (all libraries)	31

1914 GETS were required to define 31 macros.

There were no errors, warnings or information messages.

MACRO/LIS=LISS:MPLOAD/OBJ=OBJ\$:MPLOAD MSRC\$:MPPREFIX/UPDATE=(ENH\$:MPPREFIX)+MSRC\$:MPLOAD/UPDATE=(ENH\$:MPLOAD)+EXECMLS/LIB+LIB\$:MP.ML

0248 AH-BT13A-SE
VAX/VMS V4.0

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MLOAD LIS

MPINIT LIS