

DDDDDDDD DDDDDDDDD DD DD BB BB BB GG PP PP EEEEEE EEEEEE RRRRRRRR MM MM 000000 PPPPPP
DDDDDDDD DDDDDDDDD DD DD BB BB BB GG PP PP EEEEEE EEEEEE RRRRRRRR MM MM 000000 PPPPPP
DD DD BB BB BB GG PP PP EE RR RR MMMM MMMM 00 00 PP PP
DD DD BB BB BB GG PP PP EE RR RR MM MM 00 00 PP PP
DD DD BB BB BB GG PP PP EE RR RR MM MM 00 00 PP PP
DD DD BBBB BBBB BBBB GG PPPPPP EEEEEE RRRRRRRR MM MM 00 00 PPPPPP
DD DD BBBB BBBB BBBB GG PPPPPP EEEEEE RRRRRRRR MM MM 00 00 PPPPPP
DD DD BB BB BB GG GGGGGG PP EE RR RR MM MM 00 00 PP
DD DD BB BB BB GG GGGGGG PP EE RR RR MM MM 00 00 PP
DD DD BB BB BB GG PP EE RR RR MM MM 00 00 PP
DD DD BB BB BB GG PP EE RR RR MM MM 00 00 PP
DDDDDDDD BBBB BBBB BBBB GGGGGG PP EEEEEE RR RR MM MM 000000 PP
DDDDDDDD BBBB BBBB BBBB GGGGGG PP EEEEEE RR RR MM MM 000000 PP
.....
.....

LL IIIIII SSSSSSSS
LL IIIIII SSSSSSSS
LL II SS
LL II SS
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LL II SS
LL II SSSSSS
LL II SSSSSS
LL II SS
LL II SS
LL II SS
LLLLLLLL LLLL IIIIII SSSSSSSS SSSSSSSS

DBGPERMOP
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0000 58 : B. Becker Dec, 1983 Inserted calls to fixed binary arithmetic routines.
0000 59 : B. Becker Dec, 1983 Added routines DBG\$CVT_TUQUADWORD_TO_VALUE and DBG\$CVT_TUOCTAWORD_TO_VALUE to convert to Unsigned Quad & Octawords. To fix the bug DEP/QUAD I = 8000000000000000 for example.
0000 60 :
0000 61 :
0000 62 :
0000 63 :
0000 64 : B. Becker Jan, 1984 Made the MOD operation work correctly.
0000 65 : K. Glossop Jan, 1984 Fixed G-Float complex add.
0000 66 :
0000 67 : MODULE FUNCTION
0000 68 : This module contains DBG\$PERFORM_OPERATOR, the routine that
0000 69 : performs arithmetic operations.
0000 70 :
0000 71 : IMPORTANT NOTE
0000 72 : This module contains many definitions of constants and
0000 73 : offsets that are duplicates of those in DBGLIB.
0000 74 : This includes:
0000 75 : Case labels (e.g., ADD_L_L, ADD_B_B, etc.) - the order of these
0000 76 : MUST be the same as the ORT\$K_ADD_L_L etc. definitions
0000 77 : in DBGLIB, or else the CASE statement will not work.
0000 78 : Offsets to fields within Value Descriptors (e.g., DBGSA_VALUE_VMSDESC)
0000 79 : If the fields of a value descriptor change then these
0000 80 : offsets must change accordingly.
0000 81 : Literal constants - there are 4 of these: ORT\$K_MIN_ROUT,
0000 82 : ORT\$K_MAX_ROUT, DBG\$K_BASIC, DBG\$K_PLI_UBIT (defined
0000 83 : below). These values must correspond to the value
0000 84 : for the same constant in DBGLIB.
0000 85 : There are more than just these four needed. see below.
0000 86 :
0000 87 :

```
0000 89 : External routines
0000 90 : SBTTL declarations
0000 91 : EXTRN DBGSABS FIXED
0000 92 : EXTRN DBG$ADD-FIXED FIXED
0000 93 : EXTRN DBG$BLISS INDIRECT
0000 94 : EXTRN DBG$BLISS-BITSELECT
0000 95 : EXTRN DBGSC-ADDRESS OF
0000 96 : EXTRN DBGSC-INDIRECTION
0000 97 : EXTRN DBGSC-SIZEOF
0000 98 : EXTRN DBGSC-ADD-TPTR L
0000 99 : EXTRN DBGSC-SUB-TPTR L
0000 100 : EXTRN DBGSC-SUB-TPTR-TPTR
0000 101 : EXTRN DBG$DIV FIXED FIXED
0000 102 : EXTRN DBG$EQ-FIXED-FIXED
0000 103 : EXTRN DBG$EQL-FIXED-FIXED
0000 104 : EXTRN DBG$GB LANGUAGE
0000 105 : EXTRN DBG$GEQ-FIXED-FIXED
0000 106 : EXTRN DBG$GTR-FIXED-FIXED
0000 107 : EXTRN DBG$LEQ-FIXED-FIXED
0000 108 : EXTRN DBG$LSS-FIXED-FIXED
0000 109 : EXTRN DBG$MUL-FIXED-FIXED
0000 110 : EXTRN DBG$NEQ-FIXED-FIXED
0000 111 : EXTRN DBG$PRED ENUM
0000 112 : EXTRN DBG$SUB FIXED FIXED
0000 113 : EXTRN DBG$SUCC ENUM
0000 114 : EXTRN DBG$UNARY_MINUS FIXED
0000 115 : EXTRN DBG$UNARY_PLUS_FIXED
0000 116 : EXTRN PLI$ANDBIT
0000 117 : EXTRN PLI$CATBIT
0000 118 : EXTRN PLI$CMPBIT
0000 119 : EXTRN PLI$DIV PK-LONG
0000 120 : EXTRN PLI$NOTBIT
0000 121 : EXTRN PLI$ORBIT
0000 122
0000 123
0000 124 : Invoke data definitions
0000 125 :
0000 126 : SSHRDEF : Shared error messages
0000 127 : SSSDEF : System error codes
0000 128 : SDSCDEF : Data definitions
0000 129 : SSTSDEF : Status code fields
0000 130 : $DBGDEF : Debug definitions
0000 131 : $CHFDEF : Signal argument definitions
0000 132 : $MTHDEF : Math. Lib. definitions
0000 133 : $STRDEF : String definitions
0000 134
0000 135
0000 136 : Literal constants - these are the same as those in DBGLIB - see note above.
0000 137 : (These used to be obtained from DBGCOMLIB.MLB, which was built from
0000 138 : DBGLIB.REQ. However, I decided that the overhead of building DBGCOMLIB
0000 139 : just for these four constants was not worth it. Since we already have
0000 140 : several other things that must be kept consistent across DBGLIB.REQ and
0000 141 : this module, I just duplicated the definitions here.)
0000 142 :
0000 143 : As you have noted, it turned out there are more things needed from
0000 144 : DBGLIB, since you have taken it out, so someone else duplicated some
0000 145 : more constants.
```

declarations

```

0000 146 :
0000 147
00000004 0000 148      dbg$k_basic = 4
0000000C 0000 149      dbg$k_pli_ubit = 12
0000000E 0000 150      dbg$k_pli_abit = 14
00000001 0000 151      ort$k_min_rout = 1
0000001C 0000 152      ort$k_max_rout = 284
00000004 0000 153      token$k_integer = 4
00000005 0000 154      token$k_hex_integer = 5
0000000A 0000 155      token$k_bin_integer = 10
0000000B 0000 156      token$k_oct_integer = 11
0000 157
00000000 158      .PSECT DBG$PLIT,BYTE,PIC,SHR,NOWRT
159 errmsg: 160      .ASCIC /DBGPERMOP\DBG$PERFORM_OPERATOR unknown routine index/
44 5C 50 4F 4D 52 45 50 47 42 44 00' 0000
4F 5F 4D 52 4F 46 52 45 50 24 47 42 000C
6E 6B 6E 75 20 52 4F 54 41 52 45 50 0018
20 65 6E 69 74 75 6F 72 20 6E 77 6F 0024
                           78 65 64 6E 69 0030
                           34 0000
44 5C 50 4F 4D 52 45 50 47 42 44 00' 0035
5F 41 46 52 54 5F 54 56 43 24 47 42 0041
72 6F 66 20 45 55 4C 41 56 5F 4F 54 004D
6F 63 6E 65 6B 6F 74 20 6E 67 69 65 0059
                           65 64 0065
                           31 0035
44 5C 50 4F 4D 52 45 50 47 42 44 00' 0067
44 41 55 51 54 5F 54 56 43 24 47 42 0073
55 4C 41 56 5F 4F 54 5F 44 52 4F 57 007F
6F 74 20 6E 67 69 65 72 6F 66 20 45 008B
                           65 64 6F 63 6E 65 6B 0097
                           36 0067
44 5C 50 4F 4D 52 45 50 47 42 44 00' 009E
41 55 51 55 54 5F 54 56 43 24 47 42 00AA
4C 41 56 5F 4F 54 5F 44 52 4F 57 44 00B6
74 20 6E 67 69 65 72 6F 66 20 45 55 00C2
                           65 64 6F 63 6E 65 6B 6F 00CE
                           37 009E
44 5C 50 4F 4D 52 45 50 47 42 44 00' 00D6
41 54 43 4F 54 5F 54 56 43 24 47 42 00E2
55 4C 41 56 5F 4F 54 5F 44 52 4F 57 00EE
6F 74 20 6E 67 69 65 72 6F 66 20 45 00FA
                           65 64 6F 63 6E 65 6B 0106
                           36 00D6
44 5C 50 4F 4D 52 45 50 47 42 44 00' 010D
54 43 4F 55 54 5F 54 56 43 24 47 42 0119
4C 41 56 5F 4F 54 5F 44 52 4F 57 41 0125
74 20 6E 67 69 65 72 6F 66 20 45 55 0131
                           65 64 6F 63 6E 65 6B 6F 013D
                           37 010D
                           0145
                           0145 171
                           172 ; Own Storage

```

declarations

```
0145 173 :  
00000000 174 .PSECT DBG$OWN,NOEXE,LONG,PIC  
00000000 175 save_operator_entry:  
00000000 176 .LONG 0  
00000000 177 save_result:  
00000000 178 .LONG 0  
00000000 179 dope1: .LONG 0  
00000000 180 dope2: .LONG 0  
00000000 181 scratch1: .LONG 0  
00000020 182 scratch2: .BLKL 4  
00000030 183 scratch1: .BLKL 4  
00000000 184 arg1_desc: .LONG 0  
00000000 185 arg1_valdesc: .LONG 0  
00000000 186 arg2_desc: .LONG 0  
00000000 187 arg2_valdesc: .LONG 0  
00000000 188 result_desc: .LONG 0  
00000000 189 result_valdesc: .LONG 0  
00000000 190 operand: .LONG 0  
0000005C 191 work_octa: .BLKL 5  
0000006C 192 .BLKL 4  
00000000 193 .BLKL 4  
00000000 194 .BLKL 4  
00000000 195 .BLKL 4  
00000000 196 .BLKL 4  
00000000 197 .BLKL 4  
00000000 198 .BLKL 4  
00000000 199 .BLKL 4  
00000000 200 .BLKL 5  
00000000 201 .BLKL 4  
00000000 202 .BLKL 4  
00000000 203 .BLKL 4  
00000000 204 .PSECT DBG$CODE,NOWRT,BYTE,PIC,SHR
```

dbg\$perform_operator

```
0000 206 .SBTTL dbg$perform_operator
0000 207 :++
0000 208 :GLOBAL ROUTINE DBG$PERFORM_OPERATOR(OPERATOR_ENTRY, ROUT_INDEX,
0000 209 LEFT_ARG, RIGHT_ARG, RESULT_ADDR): NOVALUE =
0000 210
0000 211 FUNCTION
0000 212 Perform the operation indicated by ROUT_INDEX, and leave the result
0000 213 at RESULT_ADDR.
0000 214
0000 215 There are assumptions made in this routine:
0000 216 1. Always check overflow conditions, and give informational message
0000 217 2. The result will be the same type as the operand's type
0000 218 3. Comparison result will be always a longword value
0000 219 4. There is no mixed mode operation, ie., BU + B, or no B + L, etc.
0000 220 some sort of conversion will be done before the operation
0000 221 5. Language rules always have precedence. There will be a special
0000 222 routine to perform the operation for that language
0000 223
0000 224 INPUTS
0000 225 OPERATOR_ENTRY - A pointer to the Operator Lexical Token Entry for
0000 226 operator.
0000 227
0000 228 ROUT_INDEX - A case index indicating which operation is to be
0000 229 performed. The possible values for this index are
0000 230 defined in DBGLIB.
0000 231
0000 232 LEFT_ARG - The address of the left operand (or, in the case of
0000 233 unary operators, the only operand). This is a
0000 234 pointer to a value descriptor.
0000 235
0000 236 RIGHT_ARG - The address of the right operand (in the case of
0000 237 unary operators, this operand is not used and its
0000 238 value will be zero. This address is a pointer
0000 239 to a value descriptor.
0000 240
0000 241 RESULT_ADDR - A pointer to a longword which contains a pointer
0000 242 to a Value Descriptor which should be filled in
0000 243 with the result of the operation. The reason for
0000 244 the extra level of indirection is that in some
0000 245 cases we may build a new descriptor instead
0000 246 of using the one that is passed to us. In this
0000 247 case, we update RESULT_ADDR to point to the
0000 248 new descriptor.
0000 249
0000 250 OUTPUTS
0000 251 The result of the operation is left in the result value descriptor.
0000 252 No value is returned.
0000 253 :++
0000 254
0000 255
0000 256 : Parameter offsets
0000 257 :
00000002 0000 258 bitpos = 2
00000004 0000 259 operator_entry = 4
00000008 0000 260 rout_index = 8
0000000C 0000 261 left_arg = 12
00000010 0000 262 right_arg = 16
```

```

000000014 0000 263 result_addr      = 20
0000000C 0000 264 token_name       = 12
00000000 0000 265
00000000 0000 266
00000000 267 : Register usage
00000000 268 r2    VMS Address of the left operand in value descriptor
00000000 269 r3    VMS Address of the right operand in value descriptor
00000000 270 r4    VMS Address of the result in value descriptor
00000000 271 r5    Temporary result
00000000 272 r6    Temporary result
00000000 273 If the operands are packed, then r6 = arg1 vms desc.
00000000 274 r7 = arg2 vms desc.
00000000 275 r8 = result vms desc.
00000000 276
00000000 277 : PSL
00000000 278 FU     Floating Underflow Trap enable
00000000 279 IV     Integer Overflow trap disable
00000000 280 :
00000000 281
00000000 282
00000000 283 .ENTRY dbg$perform_operator,^M<DV,r2,r3,r4,r5,r6,r7,r8,r9,r10,r11>
00000000 284 MOVAL trap_msg_handler,(FP) ; Enable trap exception handler
00000000 285 BISPSW #^X40 ; Enable Floating Underflow Traps
00000000 286 MOVL operator_entry(AP),save_operator_entry
00000000 287 ; Save operator entry pointer in static area
00000000 288
00000000 289 :NOTE:
00000000 290 : The block of code below uses absolute offsets such as 16 to get at fields
00000000 291 : inside of a Value Descriptor. This is because of difficulties of getting
00000000 292 : the symbolic definitions from DBGLIB into this module.
00000000 293 :
00000000 294 : So, until this is fixed, the block of code below has to be changed whenever
00000000 295 : the definition of a Value Descriptor changes. This just affects the
00000000 296 : code between the asterisks.
00000000 297 :*****+
00000000 298 MOVL left_arg(AP),r2 ; Get the address of the left argument
00000000 299 MOVL r2,arg1_valdesc ; Save the value descriptor address
00000000 300 ADDL2 #20,r2 ; Get pointer to VMS descriptor
00000000 301 MOVL r2,arg1_desc ; Save the VMS descriptor address
00000000 302 MOVL 4(r2),r2 ; Get the pointer to value
00000000 303 MOVL right_arg(AP),r3 ; Get the address of the right argument
00000000 304 TSTL r3 ; Test to see if there is a right argument
00000000 305 BEQL get_result_addr$ ; Get the result address
00000000 306 MOVL r3,arg2_valdesc ; Save the value descriptor address
00000000 307 ADDL2 #20,r3 ; Get pointer to VMS descriptor
00000000 308 MOVL r3,arg2_desc ; Save the VMS descriptor address
00000000 309 MOVL 4(r3),r3 ; Get the pointer to value
00000000 310 get_result_addr$:
00000000 311 MOVL result_addr(AP),r4 ; Get the address of the result
00000000 312 MOVL (r4),r4 ; Extra level of indirection for result
00000000 313 MOVL r4,result_valdesc ; Save result value descriptor address
00000000 314 ADDL2 #20,r4 ; Get pointer to VMS descriptor
00000000 315 MOVL r4,result_desc ; Save the VMS descriptor address
00000000 316 MOVL 4(r4),r4 ; Get the pointer to value
00000000 317 MOVL r4,save_result ; Save the result pointer
00000000 318 :*****+
00000000 319

```

dbg\$perform_operator

011C	8F	01	08 AC	AF	006E	320	: Case on routine index to perform the actual operation
					006E	321	:
					029E	0075	322 CASEW rout_index(AP),#ort\$k_min_rout,#ort\$k_max_rout
					02A8	0077	323 bgn: .WORD ADD_B_B - bgn
					02B2	0079	324 .WORD ADD_BO_BU - bgn
					02BC	007B	325 .WORD ADD_W_W - bgn
					02C6	007D	326 .WORD ADD_WO_WU - bgn
					02D0	007F	327 .WORD ADD_L_L - bgn
					02DA	0081	328 .WORD ADD_LO LU - bgn
					02DF	0083	329 .WORD ADD_F_F - bgn
					02E4	0085	330 .WORD ADD_D_D - bgn
					02EA	0087	331 .WORD ADD_G_G - bgn
					02F0	0089	332 .WORD ADD_H_H - bgn
					02FC	008B	333 .WORD ADD_FC_FC - bgn
					0308	008D	334 .WORD ADD_DC_DC - bgn
					0316	008F	335 .WORD ADD_GC_GC - bgn
					0324	0091	336 .WORD ADD_HC_HC - bgn
					032E	0093	337 .WORD SUB_B_B - bgn
					0338	0095	338 .WORD SUB_BO_BU - bgn
					0342	0097	339 .WORD SUB_W_W - bgn
					034C	0099	340 .WORD SUB_WO_WU - bgn
					0356	009B	341 .WORD SUB_L_L - bgn
					0360	009D	342 .WORD SUB_LO LU - bgn
					0365	009F	343 .WORD SUB_F_F - bgn
					036A	00A1	344 .WORD SUB_D_D - bgn
					0370	00A3	345 .WORD SUB_G_G - bgn
					0376	00A5	346 .WORD SUB_H_H - bgn
					0382	00A7	347 .WORD SUB_FC_FC - bgn
					038E	00A9	348 .WORD SUB_DC_DC - bgn
					039C	00AB	349 .WORD SUB_GC_GC - bgn
					03AA	00AD	350 .WORD SUB_HC_HC - bgn
					03B4	00AF	351 .WORD DIV_B_B - bgn
					03C7	00B1	352 .WORD DIV_BO_BU - bgn
					03D1	00B3	353 .WORD DIV_W_W - bgn
					03E4	00B5	354 .WORD DIV_WO_WU - bgn
					03EE	00B7	355 .WORD DIV_L_L - bgn
					0416	00B9	356 .WORD DIV_LO LU - bgn
					041B	00BB	357 .WORD DIV_F_F - bgn
					0420	00BD	358 .WORD DIV_D_D - bgn
					0425	00BF	359 .WORD DIV_G_G - bgn
					042C	00C1	360 .WORD DIV_H_H - bgn
					0465	00C3	361 .WORD DIV_FC_FC - bgn
					04D6	00C5	362 .WORD DIV_DC_DC - bgn
					0555	00C7	363 .WORD DIV_GC_GC - bgn
					05D4	00C9	364 .WORD DIV_HC_HC - bgn
					05DE	00CB	365 .WORD MUL_B_B - bgn
					05F7	00CD	366 .WORD MUL_BO_BU - bgn
					0601	00CF	367 .WORD MUL_W_W - bgn
					061A	00D1	368 .WORD MUL_WO_WU - bgn
					0624	00D3	369 .WORD MUL_L_L - bgn
					0642	00D5	370 .WORD MUL_LO LU - bgn
					0647	00D7	371 .WORD MUL_F_F - bgn
					064C	00D9	372 .WORD MUL_D_D - bgn
					0652	00DB	373 .WORD MUL_G_G - bgn
					0658	00DD	374 .WORD MUL_H_H - bgn
					0676	00DF	375 .WORD MUL_FC_FC - bgn
							376 .WORD MUL_DC_DC - bgn

dbg\$perform_operator

06B4' 00E1	377	.WORD	MUL_GC_GC	- bgn
06F8' 00E3	378	.WORD	MUL_HC_HC	- bgn
073C' 00E5	379	.WORD	MOD_L_C	- bgn
0756' 00E7	380	.WORD	MOD_LO LU	- bgn
076E' 00E9	381	.WORD	REM_L_C	- bgn
0779' 00EB	382	.WORD	REM_LO LU	- bgn
0791' 00ED	383	.WORD	SHIFT_CLEFT_L_L	- bgn
0799' 00EF	384	.WORD	SHIFT_RT_L_L	- bgn
07A8' 00F1	385	.WORD	SHIFT_RT_LO LU	- bgn
07D0' 00F3	386	.WORD	POWER_W_Q	- bgn
07E1' 00F5	387	.WORD	POWER_L_L	- bgn
07F0' 00F7	388	.WORD	POWER_F_L	- bgn
0801' 00F9	389	.WORD	POWER_D_L	- bgn
0812' 00FB	390	.WORD	POWER_G_L	- bgn
0825' 00FD	391	.WORD	POWER_H_L	- bgn
0838' 00FF	392	.WORD	POWER_FC_L	- bgn
0851' 0101	393	.WORD	POWER_DC_L	- bgn
086A' 0103	394	.WORD	POWER_GC_L	- bgn
0887' 0105	395	.WORD	POWER_FF	- bgn
0898' 0107	396	.WORD	POWER_DD	- bgn
08A9' 0109	397	.WORD	POWER_GG	- bgn
08BA' 010B	398	.WORD	POWER_HH	- bgn
08CB' 010D	399	.WORD	POWER_FC_FC	- bgn
08DF' 010F	400	.WORD	POWER_DC_DC	- bgn
08F3' 0111	401	.WORD	POWER_GC_GC	- bgn
0929' 0113	402	.WORD	CONCAT_T_T	- bgn
095F' 0115	403	.WORD	EQL_VT_VT	- bgn
099C' 0117	404	.WORD	EQL_T_T	- bgn
09DC' 0119	405	.WORD	EQ_VT_VT	- bgn
09EE' 011B	406	.WORD	GTR_VT_VT	- bgn
0A0D' 011D	407	.WORD	GTR_T_T	- bgn
0A1F' 011F	408	.WORD	LEQ_VT_VT	- bgn
0A3E' 0121	409	.WORD	LEQ_T_T	- bgn
0A50' 0123	410	.WORD	LSS_VT_VT	- bgn
0A6F' 0125	411	.WORD	LSS_T_T	- bgn
0A81' 0127	412	.WORD	NEQ_VT_VT	- bgn
0AA0' 0129	413	.WORD	NEQ_T_T	- bgn
0AB2' 012B	414	.WORD	EQL_B_B	- bgn
0AD1' 012D	415	.WORD	EQL_W_W	- bgn
0AE3' 012F	416	.WORD	EQL_L_L	- bgn
0B02' 0131	417	.WORD	EQL_F_F	- bgn
0B0F' 0133	418	.WORD	EQL_D_D	- bgn
0B1C' 0135	419	.WORD	EQL_G_G	- bgn
0B29' 0137	420	.WORD	EQL_H_H	- bgn
0B36' 0139	421	.WORD	EQL_FC_FC	- bgn
0B43' 013B	422	.WORD	EQL_DC_DC	- bgn
0B51' 013D	423	.WORD	EQL_GC_GC	- bgn
0B5F' 013F	424	.WORD	EQL_HC_HC	- bgn
0B73' 0141	425	.WORD	NEQ_B_B	- bgn
0B87' 0143	426	.WORD	NEQ_W_W	- bgn
0B9D' 0145	427	.WORD	NEQ_L_L	- bgn
0BB3' 0147	428	.WORD	NEQ_F_F	- bgn
0BC0' 0149	429	.WORD	NEQ_D_D	- bgn
0BCD' 014B	430	.WORD	NEQ_G_G	- bgn
0BDA' 014D	431			
0BE7' 014F	432			
0BF4' 0151	433			

dbg\$perform_operator

OC02' 0153	434	.WORD	NEQ_H_H	- bgn
OC10' 0155	435	.WORD	NEQ_FC_FC	- bgn
OC24' 0157	436	.WORD	NEQ_DC_DC	- bgn
OC38' 0159	437	.WORD	NEQ_GC_GC	- bgn
OC4E' 015B	438	.WORD	NEQ_HC_HC	- bgn
OC64' 015D	439	.WORD	GEQ_B_B	- bgn
OC71' 015F	440	.WORD	GEQ_W_W	- bgn
OC7E' 0161	441	.WORD	GEQ_L_L	- bgn
OC8B' 0163	442	.WORD	GEQ_LU_LU	- bgn
OC98' 0165	443	.WORD	GEQ_F_F	- bgn
OCA5' 0167	444	.WORD	GEQ_D_D	- bgn
OCB2' 0169	445	.WORD	GEQ_G_G	- bgn
OCC0' 016B	446	.WORD	GEQ_H_H	- bgn
OCCE' 016D	447	.WORD	GTR_B_B	- bgn
OCDB' 016F	448	.WORD	GTR_W_W	- bgn
OCE8' 0171	449	.WORD	GTR_L_L	- bgn
OCF5' 0173	450	.WORD	GTR_LU_LU	- bgn
OD02' 0175	451	.WORD	GTR_F_F	- bgn
OD0F' 0177	452	.WORD	GTR_D_D	- bgn
OD1C' 0179	453	.WORD	GTR_G_G	- bgn
OD2A' 017B	454	.WORD	GTR_H_H	- bgn
OD38' 017D	455	.WORD	LEQ_B_B	- bgn
OD45' 017F	456	.WORD	LEQ_W_W	- bgn
OD52' 0181	457	.WORD	LEQ_L_L	- bgn
OD5F' 0183	458	.WORD	LEQ_LU_LU	- bgn
OD6C' 0185	459	.WORD	LEQ_F_F	- bgn
OD79' 0187	460	.WORD	LEQ_D_D	- bgn
OD86' 0189	461	.WORD	LEQ_G_G	- bgn
OD94' 018B	462	.WORD	LEQ_H_H	- bgn
ODA2' 018D	463	.WORD	LSS_B_B	- bgn
ODAF' 018F	464	.WORD	LSS_W_W	- bgn
ODBC' 0191	465	.WORD	LSS_L_L	- bgn
ODC9' 0193	466	.WORD	LSS_LU_LU	- bgn
ODD6' 0195	467	.WORD	LSS_F_F	- bgn
ODE3' 0197	468	.WORD	LSS_D_D	- bgn
ODFO' 0199	469	.WORD	LSS_G_G	- bgn
ODFE' 019B	470	.WORD	LSS_H_H	- bgn
OE0C' 019D	471	.WORD	BIT_AND_B_B	- bgn
OE14' 019F	472	.WORD	BIT_AND_W_W	- bgn
OE1C' 01A1	473	.WORD	BIT_AND_L_L	- bgn
OE24' 01A3	474	.WORD	BIT_EQV_B_B	- bgn
OE2C' 01A5	475	.WORD	BIT_EQV_W_W	- bgn
OE34' 01A7	476	.WORD	BIT_EQV_L_L	- bgn
OE3C' 01A9	477	.WORD	BIT_NOT_B	- bgn
OE40' 01AB	478	.WORD	BIT_NOT_W	- bgn
OE44' 01AD	479	.WORD	BIT_NOT_L	- bgn
OE48' 01AF	480	.WORD	BIT_OR_B_B	- bgn
OE4D' 01B1	481	.WORD	BIT_OR_W_W	- bgn
OE52' 01B3	482	.WORD	BIT_OR_L_L	- bgn
OE57' 01B5	483	.WORD	BIT_XOR_B_B	- bgn
OE5C' 01B7	484	.WORD	BIT_XOR_W_W	- bgn
OE61' 01B9	485	.WORD	BIT_XOR_L_L	- bgn
OE7E' 01BB	486	.WORD	AND_B_B	- bgn
OE8A' 01BD	487	.WORD	AND_W_W	- bgn
OE96' 01BF	488	.WORD	AND_L_L	- bgn
OEAA' 01C1	489	.WORD	AND_D_D	- bgn
OEBA' 01C3	490	.WORD	NOT_B	- bgn

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OEB8'	01C5	491	.WORD	NOT_W	- bgn
OEBF'	01C7	492	.WORD	NOT_L	- bgn
OEC6'	01C9	493	.WORD	NOT_D	- bgn
OED1'	01CB	494	.WORD	OR_B_B	- bgn
OEDC'	01CD	495	.WORD	OR_W_W	- bgn
OEE7'	01CF	496	.WORD	OR_L_L	- bgn
OEF2'	01D1	497	.WORD	OR_D_D	- bgn
OF01'	01D3	498	.WORD	XOR_C_L	- bgn
OF17'	01D5	499	.WORD	UNARY_MINUS_B	- bgn
OF20'	01D7	500	.WORD	UNARY_MINUS_W	- bgn
OF29'	01D9	501	.WORD	UNARY_MINUS_L	- bgn
OF32'	01DB	502	.WORD	UNARY_MINUS_LU	- bgn
OF3B'	01DD	503	.WORD	UNARY_MINUS_F	- bgn
OF3F'	01DF	504	.WORD	UNARY_MINUS_D	- bgn
OF43'	01E1	505	.WORD	UNARY_MINUS_G	- bgn
OF48'	01E3	506	.WORD	UNARY_MINUS_H	- bgn
OF4D'	01E5	507	.WORD	UNARY_MINUS_FC	- bgn
OF56'	01E7	508	.WORD	UNARY_MINUS_DC	- bgn
OF5F'	01E9	509	.WORD	UNARY_MINUS_GC	- bgn
OF6A'	01EB	510	.WORD	UNARY_MINUS_HC	- bgn
OF75'	01ED	511	.WORD	UNARY_PLUS_B	- bgn
OF79'	01EF	512	.WORD	UNARY_PLUS_W	- bgn
OF7D'	01F1	513	.WORD	UNARY_PLUS_L	- bgn
OF81'	01F3	514	.WORD	UNARY_PLUS_F	- bgn
OF85'	01F5	515	.WORD	UNARY_PLUS_D	- bgn
OF89'	01F7	516	.WORD	UNARY_PLUS_G	- bgn
OF8E'	01F9	517	.WORD	UNARY_PLUS_H	- bgn
OF93'	01FB	518	.WORD	UNARY_PLUS_FC	- bgn
OF9C'	01FD	519	.WORD	UNARY_PLUS_DC	- bgn
OFAD'	01FF	520	.WORD	UNARY_PLUS_GC	- bgn
OFB0'	0201	521	.WORD	UNARY_PLUS_HC	- bgn
OFBB'	0203	522	.WORD	ABS_B	- bgn
OFC7'	0205	523	.WORD	ABS_W	- bgn
OFD3'	0207	524	.WORD	ABS_L	- bgn
OFDF'	0209	525	.WORD	ABS_F	- bgn
OFEB'	020B	526	.WORD	ABS_D	- bgn
OFF7'	020D	527	.WORD	ABS_G	- bgn
1006'	020F	528	.WORD	ABS_H	- bgn
1015'	0211	529	.WORD	INDIRECT_LU	- bgn
1026'	0213	530	.WORD	INDIRECT_TPTR	- bgn
1038'	0215	531	.WORD	BITSELECT	- bgn
104F'	0217	532	.WORD	DIFFERENCE_SET_SET	- bgn
10A3'	0219	533	.WORD	EQL_SET_SET	- bgn
10EA'	021B	534	.WORD	GEQ_SET_SET	- bgn
1109'	021D	535	.WORD	IN_SET_SET	- bgn
1114'	021F	536	.WORD	INTERSECT_SET_SET	- bgn
1169'	0221	537	.WORD	LEQ_SET_SET	- bgn
11B7'	0223	538	.WORD	NEQ_SET_SET	- bgn
1212'	0225	539	.WORD	UNION_SET_SET	- bgn
1262'	0227	540	.WORD	ADDRESS_L	- bgn
1276'	0229	541	.WORD	SIZEOF [- bgn
1287'	022B	542	.WORD	ADD_TPTR_L	- bgn
12A1'	022D	543	.WORD	SUB_TPTR_L	- bgn
12B8'	022F	544	.WORD	SUB_TPTR_TPTR	- bgn
0E66'	0231	545	.WORD	BIT_IMP_B_B	- bgn
0E6E'	0233	546	.WORD	BIT_IMP_W_W	- bgn
0E76'	0235	547	.WORD	BIT_IMP_L_L	- bgn

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12D5' 0237	548	.WORD	PRE-INCR_L	- bgn
12D5' 0239	549	.WORD	PRE-INCR_LU	- bgn
12E8' 023B	550	.WORD	PRE-INCR_D	- bgn
12FC' 023D	551	.WORD	PRE-INCR_TPTR	- bgn
131A' 023F	552	.WORD	POST_INCR_L	- bgn
131A' 0241	553	.WORD	POST_INCR_LU	- bgn
132B' 0243	554	.WORD	POST_INCR_D	- bgn
131A' 0245	555	.WORD	POST_INCR_TPTR	- bgn
133C' 0247	556	.WORD	PRE_DECR_C	- bgn
133C' 0249	557	.WORD	PRE_DECR_LU	- bgn
134F' 024B	558	.WORD	PRE_DECR_D	- bgn
1363' 024D	559	.WORD	PRE_DECR_TPTR	- bgn
1381' 024F	560	.WORD	POST_DECR_L	- bgn
1381' 0251	561	.WORD	POST_DECR_LU	- bgn
1392' 0253	562	.WORD	POST_DECR_D	- bgn
1381' 0255	563	.WORD	POST_DECR_TPTR	- bgn
13C7' 0257	564	.WORD	ADD_P_P	- bgn
13A3' 0259	565	.WORD	SUB_P_P	- bgn
143F' 025B	566	.WORD	MUL_P_P	- bgn
14E8' 025D	567	.WORD	DIV_P_P	- bgn
1571' 025F	568	.WORD	UNARY_PLUS_P	- bgn
1554' 0261	569	.WORD	UNARY_MINUS_P	- bgn
1598' 0263	570	.WORD	EQL_P_P	- bgn
15D3' 0265	571	.WORD	NEQ_P_P	- bgn
160B' 0267	572	.WORD	GTR_P_P	- bgn
161F' 0269	573	.WORD	GEQ_P_P	- bgn
1633' 026B	574	.WORD	LSS_P_P	- bgn
1647' 026D	575	.WORD	LEQ_P_P	- bgn
170E' 026F	576	.WORD	CONCAT_TF_TF	- bgn
172C' 0271	577	.WORD	EQL_TF_TF	- bgn
1812' 0273	578	.WORD	NEQ_TF_TF	- bgn
1781' 0275	579	.WORD	GTR_TF_TF	- bgn
1752' 0277	580	.WORD	GEQ_TF_TF	- bgn
17E1' 0279	581	.WORD	LSS_TF_TF	- bgn
17B2' 027B	582	.WORD	LEQ_TF_TF	- bgn
1838' 027D	583	.WORD	BIT_NOT_TF_TF	- bgn
184E' 027F	584	.WORD	BIT_AND_TF_TF	- bgn
186C' 0281	585	.WORD	BIT_OR_TF_TF	- bgn
18F6' 0283	586	.WORD	EQL_RFA_RFA	- bgn
190A' 0285	587	.WORD	NEQ_RFA_RFA	- bgn
191E' 0287	588	.WORD	UNARY_PPLUS_Q	- bgn
1924' 0289	589	.WORD	UNARY_MINUS_Q	- bgn
1936' 028B	590	.WORD	UNARY_PLUS_0	- bgn
1941' 028D	591	.WORD	UNARY_MINUS_0	- bgn
1965' 028F	592	.WORD	SUCC_ENUM	- bgn
1979' 0291	593	.WORD	PRED_ENUM	- bgn
198D' 0293	594	.WORD	UNARY_PLUS_FIXED	- bgn
19A1' 0295	595	.WORD	UNARY_MINUS_FIXED	- bgn
1985' 0297	596	.WORD	ABS_FIXED	- bgn
19C9' 0299	597	.WORD	ADD_FIXED_FIXED	- bgn
19E3' 029B	598	.WORD	SUB_FIXED_FIXED	- bgn
19FD' 029D	599	.WORD	MUL_FIXED_FIXED	- bgn
1A17' 029F	600	.WORD	DIV_FIXED_FIXED	- bgn
1A31' 02A1	601	.WORD	EQL_FIXED_FIXED	- bgn
1A4B' 02A3	602	.WORD	NEQ_FIXED_FIXED	- bgn
1A65' 02A5	603	.WORD	LSS_FIXED_FIXED	- bgn
1A7F' 02A7	604	.WORD	GTR_FIXED_FIXED	- bgn

:BB001
:BB001

dbg\$perform_operator

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1A99' 02A9 605 .WORD LEQ_FIXED_FIXED - bgn
1AB3' 02AB 606 .WORD GEQ_FIXED_FIXED - bgn
1892 31 02AD 607 BRW unknown_rout_index
          02B0 608
          02B0 609 int_overflow:
      52 00000000'EF  D0 02B0 610 MOVL save_operator_entry,r2
      52 0C A2  DE 02B7 611 MOVAL token_name(r2T),r2
      52  DD 02BB 612 PUSHL r2
      01  DD 02BD 613 PUSHL #1
000286A3 8F  DD 02BF 614 PUSHL #dbg$, iintovf
00000000'GF 03  FB 02C5 615 CALLS #3,G^LIB$SIGNAL
          04 02CC 616 RET
          02CD 617
          02CD 618 div_by_zero:
      00028240 8F  DD 02CD 619 PUSHL #dbg$, divbyzero
00000000'GF 01  FB 02D3 620 CALLS #1,G^LIB$SIGNAL
          04 02DA 621 RET
          02DB 622
          02DB 623 shift_count_negative:
      00028EC0 8F  DD 02DB 624 PUSHL #dbg$, sfcntneg
00000000'GF 01  FB 02E1 625 CALLS #1,G^LIB$SIGNAL
          04 02E8 626 RET
          02E9 627
          02E9 628 string_truncate:
      52 00000000'EF  D0 02E9 629 MOVL save_operator_entry,r2
      52 0C A2  DE 02F0 630 MOVAL token_name(r2T),r2
      52  DD 02F4 631 PUSHL r2
      01  DD 02F6 632 PUSHL #1
000286AB 8F  DD 02F8 633 PUSHL #dbg$, istrtru
00000000'GF 03  FB 02FE 634 CALLS #3,G^LIB$SIGNAL
          0305 635
          0305 636 branch_ret:
      04 00000000'EF  91 0305 637 CMPB DBG$GB_LANGUAGE, #DBG$K_BASIC
          01 13 030C 638 BEQL basics$
          04 030E 639 RET
          030F 640 basics$:
      64 64  CE 030F 641 MNEGL (r4), (r4)
          04 0312 642 RET
          0313 643
          0313 644
          0313 645 ****
          0313 646 : A D D   and   S U B T R A C T
          0313 647 :
          0313 648 :
          0313 649 ****
          0313 650
          0313 651
          0313 652 ; Additive Operators - Addition
          0313 653 ;
          0313 654 add_b_b:
      64 63 62 81 0313 655 ADDB3 (r2),(r3),(r4)
          01 1D 0317 656 BVS add_bs
          04 0319 657 RET
          FF93 31 031A 658 add_bs:
          031A 659 BRW int_overflow
          031D 660
          031D 661 add_bu_bu:

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dbg\$perform_operator											
64	63	62	81	031D	662	ADDB3	(r2),(r3),(r4)				
		01	1F	0321	663	BCS	add_bus				
			04	0323	664	RET			; Branch on C bit set		
				0324	665	add_bus:					
		FF89	31	0324	666	BRW	int_overflow				
				0327	667						
				0327	668	add_w_w:					
		64	63	62	A1	0327	669	ADDW3	(r2),(r3),(r4)		
			01	1D	032B	670	BVS	add_w\$			
				04	032D	671	RET				
				032E	672	add_w\$:					
		FF7F	31	032E	673	BRW	int_overflow				
				0331	674						
				0331	675	add_wu_wu:					
		64	63	62	A1	0331	676	ADDW3	(r2),(r3),(r4)		
			01	1F	0335	677	BCS	add_wu\$			
				04	0337	678	RET				
				0338	679	add_wu\$:					
		FF75	31	0338	680	BRW	int_overflow				
				0338	681						
				0338	682	add_l_l:					
		64	63	62	C1	033B	683	ADDL3	(r2),(r3),(r4)		
			01	1D	033F	684	BVS	add_l\$			
				04	0341	685	RET				
				0342	686	add_l\$:					
		FF6B	31	0342	687	BRW	int_overflow				
				0345	688						
				0345	689	add_lu_lu:					
		64	63	62	C1	0345	690	ADDL3	(r2),(r3),(r4)		
			01	1F	0349	691	BCS	add_lu\$			
				04	034B	692	RET				
				034C	693	add_lu\$:					
		FF61	31	034C	694	BRW	int_overflow				
				034F	695						
				034F	696	add_f_f:					
		64	63	62	41	034F	697	ADDF3	(r2),(r3),(r4)		
				04	0353	698	RET				
				0354	699	add_d_d:					
		64	63	62	61	0354	700	ADDD3	(r2),(r3),(r4)		
				04	0358	701	RET				
				0359	702	add_g_g:					
		64	63	62	41FD	0359	703	ADDG3	(r2),(r3),(r4)		
				04	035E	704	RET				
				035F	705	add_h_h:					
		64	63	62	61FD	035F	706	ADDH3	(r2),(r3),(r4)		
				04	0364	707	RET				
				0365	708						
				0365	709	add_fc_fc:					
	04 A4	04 A3	63	04 A2	62	41	0365	710	ADDF3	(r2),(r3),(r4)	
				41	0369	711	ADDF3	4(r2),4(r3),4(r4)		: Add Real Part	
				04	0370	712	RET			: Add Imaginary Part	
				0371	713	add_dc_dc:					
	08 A4	08 A3	63	08 A2	62	61	0371	714	ADDD3	(r2),(r3),(r4)	
				61	0375	715	ADDD3	8(r2),8(r3),8(r4)			
				04	037C	716	RET				
				037D	717	add_gc_gc:					
		64	63	62	41FD	037D	718	ADDG3	(r2),(r3),(r4)		

08 A4	08 A3	08 A2	41FD	0382	719	ADDG3	8(r2),8(r3),8(r4)
			04	038A	720	RET	
				038B	721	add_hc_hc:	
10 A4	64 10 A3	63 10 A2	62 61FD	038B	722	ADDH3	(r2),(r3),(r4)
			04	0390	723	ADDH3	16(r2),16(r3),16(r4)
				0398	724	RET	
				0399	725		
				0399	726		
				0399	727	; Additive Operators - Subtraction	
				0399	728		
64 62	63 01	83 1D	0399	730	729	sub_b_b:	
			04	039D	731	SUBB3	(r3),(r2),(r4)
				039F	732	BVS	sub_b\$
				03A0	733	RET	
	FF0D	31	03A0	734	sub_b\$:	BRW	int_overflow
			03A3	735			
64 62	63 01	83 1F	03A3	736	sub_bu_bu:		
			04	03A7	737	SUBB3	(r3),(r2),(r4)
				03A9	738	BCS	sub_bu\$
				03AA	739	RET	
	FF03	31	03AA	740	sub_bu\$:	BRW	int_overflow
			03AD	741			
64 62	63 01	A3 1D	03AD	743	sub_w_w:		
			04	03B1	744	SUBW3	(r3),(r2),(r4)
				03B3	745	BVS	sub_w\$
				03B4	746	RET	
	FEF9	31	03B4	747	sub_w\$:	BRW	int_overflow
			03B7	748			
64 62	63 01	A3 1F	03B7	750	sub_wu_wu:		
			04	03BB	751	SUBW3	(r3),(r2),(r4)
				03BD	752	BCS	sub_wu\$
				03BE	753	RET	
	FEEF	31	03BE	754	sub_wu\$:	BRW	int_overflow
			03C1	755			
64 62	63 01	C3 1D	03C1	757	sub_l_l:		
			04	03C5	758	SUBL3	(r3),(r2),(r4)
				03C7	759	BVS	sub_l\$
				03C8	760	RET	
	FEE5	31	03C8	761	sub_l\$:	BRW	int_overflow
			03CB	762			
64 62	63 01	C3 1F	03CB	764	sub_lu_lu:		
			04	03CF	765	SUBL3	(r3),(r2),(r4)
				03D1	766	BCS	sub_lu\$
				03D2	767	RET	
	FEDB	31	03D2	768	sub_lu\$:	BRW	int_overflow
			03D5	769			
64 62	63 04	43 03D5	771	sub_f_f:			
			04	03D9	772	SUBF3	(r3),(r2),(r4)
				03DA	773	RET	
64 62	63 63	03DA	774	sub_d_d:	SUBD3	(r3),(r2),(r4)	
			775				

dbg\$perform_operator

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        04 03DE    776      RET
64   62   63 43FD 03DF    777  sub_g_g: SUBG3  (r3),(r2),(r4)
          04 03E4    778      RET
          04 03E5    779      RET
64   62   63 63FD 03E5    780  sub_h_h: SUBH3  (r3),(r2),(r4)
          04 03EA    781      RET
          04 03EB    782      RET
          04 03EB    783      RET
04 A4   64 62 63 43 03EB    784  sub_fc_fc: SUBF3  (r3),(r2),(r4)
          04 A2   04 A3 43 03EF    785      SUBF3  4(r3),4(r2),4(r4)
          04 03F6    786      RET
          04 03F7    787      RET
          04 03F7    788  sub_dc_dc: SUBD3  (r3),(r2),(r4)
08 A4   08 A2   62 63 63 03F7    789      SUBD3  8(r3),8(r2),8(r4)
          04 03FB    790      RET
          04 0402    791      RET
          04 0403    792  sub_gc_gc: SUBG3  (r3),(r2),(r4)
08 A4   08 A2   62 63 43FD 0403    793      SUBG3  8(r3),8(r2),8(r4)
          04 0408    794      RET
          04 0410    795      RET
          04 0411    796  sub_hc_hc: SUBH3  (r3),(r2),(r4)
10 A4   10 A2   62 10 A3 63FD 0411    797      SUBH3  16(r3),16(r2),16(r4)
          04 0416    798      RET
          04 041E    799      RET
          04 041F    800      RET
          04 041F    801      RET
          04 041F    802 : ****
          04 041F    803 :
          04 041F    804 : D I V I D E and M U L T I P L Y
          04 041F    805 :
          04 041F    806 : ****
          04 041F    807 :
          04 041F    808 :
          04 041F    809 : Multiplicative - Division
          04 041F    810 :
          04 041F    811  div_b_b: DIVB3  (r3),(r2),(r4)
64   62   63 87 041F    812      BVS      div_bs
          01 1D     0423    813      RET
          04 0425    814      RET
          FE87   31 0426    815  div_bs: BRW    int_overflow
          0429    816      RET
          0429    817      RET
          0429    818  div_bu_bu: MOVZBL (r2),r2
52   62   9A 0429    819      MOVZBL (r3),r3
53   63   9A 042C    820      BEQL    div_bs
          08 13 042F    821      DIVL3  r3,r2,r5
          52 53   C7 0431    822      MOVB    r5,(r4)
          64 55   90 0435    823      RET
          04 0438    824      RET
          FE91   31 0439    825  div_bu$: BRW    div_by_zero
          043C    826      RET
          043C    827      RET
          043C    828  div_w_w: DIVW3  (r3),(r2),(r4)
64   62   63 A7 043C    829      BVS      div_w$ 
          01 1D     0440    830      RET
          04 0442    831      RET
          0443    832  div_w$: RET

```

: Zero-extend Dividend
: Zero-extend Divisor
: Test divisor is not zero

dbg\$perform_operator						
		FE6A	31	0443	833	BRW int_overflow
				0446	834	
				0446	835	div_wu_wu:
	52	62	3C	0446	836	MOVZWL (r2),r2
	53	63	3C	0449	837	MOVZWL (r3),r3
		08	13	044C	838	BEQL div_wu\$
55	62	63	C7	044E	839	DIVL3 (r3),(r2),r5
	64	55	B0	0452	840	MOVW r5,(r4)
			04	0455	841	RET
				0456	842	div_wu\$:
		FE74	31	0456	843	BRW div_by_zero
				0459	844	
	64	62	63	C7	0459	845 div_l_l:
		01	1D	045D	846	DIVL3 (r3),(r2),(r4)
		04	045F	847	BVS div_l\$	
				0460	848	RET
		FE4D	31	0460	849	div_ls:
				0463	850	BRW int_overflow
				0463	851	
				0463	852	div_lu_lu:
		63	D5	0463	853	TSTL (r3) ; Check for divide by 0
		1A	13	0465	854	BEQL div_lu1\$; Branch on divide by 0
		0B	14	0467	855	BGTR ext_prec_div ; Branch on +Divisor
	62	63	D4	0469	856	CLRL r5 ; Assume zero result
		046B	857	CMPL (r3),(r2) ; Compare Divident and -Divisor		
		046E	858		-- (divided by large number)	
		17	1A	046E	859	BGTRU set_quotient ; Result is 0, set it
	55	62	D0	0470	860	INCL r5 ; Result is 1
		56	D4	0477	861	BRB set_quotient ; Set it
52	64	55	63	7B	0479	862 ext_prec_div: ; Divident is quarward
		04	047E	865	EDIV (r3),r5,(r4),r2 ; Perform the DIV	
		04	0480	866	BCS div_lu2\$	
				0480	867	RET
				0481	868	div_lu1\$: ;
		FE49	31	0481	869	BRW div_by_zero
				0484	870	div_lu2\$: ;
		FE29	31	0484	871	BRW int_overflow
				0487	872	
	64	55	D0	0487	873	set_quotient: ; Set result
		04	048A	874	MOVL r5,(r4)	
			048B	875	RET	
			048B	876		
	64	62	63	47	048B	877 div_f_f: ;
		04	048F	878	DIVF3 (r3),(r2),(r4)	
			0490	879	RET	
			0490	880		
	64	62	63	67	0490	881 div_d_d: ;
		04	0494	882	DIVD3 (r3),(r2),(r4)	
			0495	883	RET	
			0495	884		
	64	62	63	47FD	0495	885 div_g_g: ;
		04	049A	886	DIVG3 (r3),(r2),(r4)	
			049B	887	RET	
			049B	888		
			049B	889	div_h_h:	

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	64	62	63	67FD	04	049B	890	DIVH3	(r3),(r2),(r4)	
						04A0	891	RET		
						04A1	892			
						04A1	893	div_fc_fc:		
56	04	55 A3	63 04	63 A3	45	04A1	894	MULF3	(r3),(r3),r5	: X = B<1>*B<1> + B<2>*B<2>
	51	56	55	55	45	04A5	895	MULF3	4(r3),4(r3),r6	
					41	04AB	896	ADDF3	r5,r6,r1	
					51	53	04AF	TSTF	r1	
					24	13	04B1	BEQL	div_fc\$	
56	04	55 A2	62 04	63 A3	45	04B3	898	MULF3	(r3),(r2),r5	: Real Part Division
	56	56	55	40	45	04B7	899	MULF3	4(r3),4(r2),r6	; C<1> = (A<1>*B<1> + A<2>*B<2>) / X
	64	56	51	47	04C0	900	ADDF2	r5,r6		
	55	04 A2	62 04	63 A3	45	04C4	902	DIVF3	r1,r6,(r4)	
56	62	04	A3	45	04C9	903	MULF3	(r3),4(r2),r5	: Imaginary Part Division	
	55	55	56	42	04CE	904	MULF3	4(r3),(r2),r6	; C<2> = (A<2>*B<1> - A<1>*B<2>) / X	
04	A4	55	51	47	04D1	905	SUBF2	r6,r5		
				04	04D6	906	DIVF3	r1,r5,4(r4)		
						04D7	RET			
					FDF3	31	04D7	908	div_fc\$:	
						04DA	909	BRW	div_by_zero	
						04DA	910			
55	00000010'EF	63	63	65	04DA	911	div_dc_dc:			
	00000020'EF	08 A3	08 A3	65	04E2	912	MULD3	(r3),(r3),scratch1	: X = B<1>*B<1> + B<2>*B<2>	
	00000020'EF	00000010'EF		61	04EC	913	MULD3	8(r3),8(r3),scratch2		
				55	73	04F8	914	ADDD3	scratch1,scratch2,r5	
				4C	13	04FA	915	TSTD	r5	
	00000010'EF	62	63	65	04FC	916	BEQL	div_dc\$		
00000020'EF	08 A2	08 A3	65	0504	917	MULD3	(r3),(r2),scratch1	: Real Part Division		
00000020'EF	00000010'EF		60	050E	918	MULD3	8(r3),8(r2),scratch2	; C<1> = (A<1>*B<1> + A<2>*B<2>) / X		
	64	00000020'EF	55	67	0519	919	ADDD2	scratch1,scratch2		
	00000010'EF	08 A2	63	65	0521	920	DIVD3	r5,scratch2,(r4)		
	00000020'EF	62	08 A3	65	052A	921	MULD3	(r3),8(r2),scratch1	: Imaginary Part Division	
00000010'EF	00000020'EF		62	0533	922	MULD3	8(r3),(r2),scratch2	; C<2> = (A<2>*B<1> - A<1>*B<2>) / X		
08 A4	00000010'EF	55	67	053E	923	SUBD2	scratch2,scratch1			
			04	0547	924	DIVD3	r5,scratch1,8(r4)			
					925	RET				
				FD82	31	0548	926	div_dc\$:		
					0548	927	BRW	div_by_zero		
					054B	928				
55	00000010'EF	63	63	63	45FD	054B	929	div_gc_gc:		
	00000020'EF	08 A3	08 A3	45FD	0554	930	MULG3	(r3),(r3),scratch1	: X = B<1>*B<1> + B<2>*B<2>	
	00000020'EF	00000010'EF	41FD	055F	931	MULG3	8(r3),8(r3),scratch2			
		0000005C7'EF	53FD	056C	932	ADDG3	scratch1,scratch2,r5			
	00000010'EF	62	63	45FD	0573	933	TSTG	div_gc\$		
00000020'EF	08 A2	08 A3	45FD	057C	934	MULG3	(r3),(r2),scratch1	: Real Part Division		
00000020'EF	00000010'EF	40FD	0587	935	MULG3	8(r3),8(r2),scratch2	; C<1> = (A<1>*B<1> + A<2>*B<2>) / X			
	64	00000020'EF	55	47FD	0593	936	ADDG2	scratch1,scratch2		
	00000010'EF	08 A2	63	45FD	059C	937	DIVG3	r5,scratch2,(r4)		
	00000020'EF	62	08 A3	45FD	05A6	938	MULG3	(r3),8(r2),scratch1	: Imaginary Part Division	
00000010'EF	00000020'EF	42FD	05B0	939	MULG3	8(r3),(r2),scratch2	; C<2> = (A<2>*B<1> - A<1>*B<2>) / X			
08 A4	00000010'EF	55	47FD	05BC	940	SUBG2	scratch2,scratch1			
			04	05C6	941	DIVG3	r5,scratch1,8(r4)			
				FD03	31	05C7	942	RET		
					05C7	943	div_gc\$:			
					05CA	944	BRW	div_by_zero		
					05CA	945				
					05CA	946	div_hc_hc:			

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      00000010'EF  63  63 65FD  05CA  947    MULH3  (r3),(r3),scratch1 ; X = B<1>*B<1> + B<2>*B<2>
55 00000020'EF  10 A3 10 A3 65FD  05D3  948    MULH3  16(r3),16(r3),scratch2
      00000020'EF  00000010'EF 61FD  05DE  949    ADDH3  scratch1,scratch2,r5
      00000064'EF  73FD  05EB  950    TSTH   div_hcs
      00000010'EF  62  63 65FD  05F2  951    MULH3  (r3),(r2),scratch1 ; Real Part Division
00000020'EF  10 A2 10 A3 65FD  05FB  952    MULH3  16(r3),16(r2),scratch2 ; C<1> = (A<1>*B<1> + A<2>*B<2>) / X
      00000020'EF  00000010'EF 60FD  0606  953    ADDH2  scratch1,scratch2
      64  00000020'EF  55 67FD  0612  954    DIVH3  r5,scratch2,(r4)
      00000010'EF  10 A2 63 65FD  061B  955    MULH3  (r3),16(r2),scratch1 ; Imaginary Part Division
      00000020'EF  62  10 A3 65FD  0625  956    MULH3  16(r3),(r2),scratch2 ; C<2> = (A<2>*B<1> - A<1>*B<2>) / X
00000010'EF  00000020'EF 62FD  062F  957    SUBH2  scratch2,scratch1
10 A4  00000010'EF  55 67FD  063B  958    DIVH3  r5,scratch1,16(r4)
      04  0645  959    RET
      0646  960  div_hcs:
FC84  31  0646  961    BRW   div_by_zero
      0649  962
      0649  963
      0649  964  : Multiplicative Operators - Multiply
      0649  965  :
      0649  966  mul_b_b:
      64  62  63  85  0649  967    MULB3  (r3),(r2),(r4)
      01  1D  064D  968    BVS   mul_b$ 
      04  064F  969    RET
      FC5D  31  0650  970  mul_b$:
      0650  971    BRW   int_overflow
      0653  972
      0653  973  mul_bu_bu:
      55  62  9A  0653  974    MOVZBL (r2),r5
      56  63  9A  0656  975    MOVZBL (r3),r6
      55  56  C4  0659  976    MULL2  r6,r5
      000000FF  8F  55  D1  065C  977    CMPL   r5,#^XFF
      04  1A  0663  978    BGTRU  mul_bus
      64  55  90  0665  979    MOVB   r5,7r4)
      04  0668  980    RET
      FC44  31  0669  981  mul_bus$:
      0669  982    BRW   int_overflow
      066C  983
      066C  984  mul_w_w:
      64  62  63  A5  066C  985    MULW3  (r3),(r2),(r4)
      01  1D  0670  986    BVS   mul_w$ 
      04  0672  987    RET
      FC3A  31  0673  988  mul_w$:
      0673  989    BRW   int_overflow
      0676  990
      0676  991  mul_wu_wu:
      55  62  3C  0676  992    MOVZWL (r2),r5
      56  63  3C  0679  993    MOVZWL (r3),r6
      55  56  C4  067C  994    MULL2  r6,r5
      0000FFFF  8F  55  D1  067F  995    CMPL   r5,#^xFFFF
      04  1A  0686  996    BGTRU  mul_wus
      64  55  B0  0688  997    MOVW   r5,7r4)
      04  0688  998    RET
      FC21  31  068C  999  mul_wus$:
      068C  1000   BRW   int_overflow
      068F  1001
      068F  1002  mul_l_l:
      64  62  63  C5  068F  1003  MULL3  (r3),(r2),(r4)

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01 1D 0693 1004      BVS    mul_ls
04 0695 1005      RET
0696 1006 mul_ls:   BRW    int_overflow
0699 1007
0699 1008
0699 1009 ; (note: in C, the code generated for this operation is much simplified -
0699 1010 ; MULL$. The reason to do so in here is to detect overflow condition.
0699 1011
0699 1012 mul_lu_lu:
55 00 62 63 7A 0699 1013 EMUL   (r3),(r2),#0,r5      ; Perform extended-precision multiplication
63 D5 069E 1014 TSTL   (r3)          ; Test multiplier
56 62 03 18 06A0 1015 BGEQ   positive_mulr  ; Multiplier >= 0
62 63 C0 06A2 1016 ADDL2  (r2),r6      ; Fudge, so overflow can be detected
06A5 1017 positive_mulr:
62 D5 06A5 1018 TSTL   (r2)          ; Test multiplicand
03 18 06A7 1019 BGEQ   positive_muld ; Multiplicand >= 0
56 63 C0 06A9 1020 ADDL2  (r3),r6      ; Fudge, so overflow can be detected
06AC 1021 positive_muld:
56 D5 06AC 1022 TSTL   r6            ; Test Result[low]
04 12 06AE 1023 BNEQ   mul_ls       ; Result[low] not= zero, overflow
64 55 D0 06B0 1024 MOVL   r5,r4        ; Get Result[high] as the result
04 06B3 1025 RET
06B4 1026 mul_ls:
FBF9 31 06B4 1027 BRW    int_overflow
06B7 1028
06B7 1029 mul_ff:
64 62 63 45 06B7 1030 MULF3  (r3),(r2),(r4)
04 06BB 1031 RET
06BC 1032 mul_dd:
64 62 63 65 06BC 1033 MULD3  (r3),(r2),(r4)
04 06C0 1034 RET
06C1 1035 mul_gg:
64 62 63 45FD 06C1 1036 MULG3  (r3),(r2),(r4)
04 06C6 1037 RET
06C7 1038 mul_hh:
64 62 63 65FD 06C7 1039 MULH3  (r3),(r2),(r4)
04 06CC 1040 RET
06CD 1041
06CD 1042 mul_fc_fc:
56 55 62 63 45 06CD 1043 MULF3  (r3),(r2),r5      ; Real Part Multiply:
04 A2 04 A3 45 06D1 1044 MULF3  4(r3),4(r2),r6      ; C<1> = A<1>*B<1> - A<2>*B<2>
64 55 56 43 06D7 1045 SUBF3  r6,r5,(r4)          ; Real part result
55 62 04 A3 45 06DB 1046 MULF3  4(r3),(r2),r5      ; Imaginary Part Multiply:
56 04 A2 63 45 06E0 1047 MULF3  (r3),4(r2),r6      ; C<2> = A<1>*B<2> + A<2>*B<1>
04 A4 56 55 41 06E5 1048 ADDF3  r5,r6,4(r4)          ; Imaginary part result
04 06EA 1049 RET
06EB 1050 mul_dc_dc:
00000010'EF 62 63 65 06EB 1051 MULD3  (r3),(r2),scratch1 ; Real Part Multiply:
00000020'EF 08 A2 08 A3 65 06F3 1052 MULD3  8(r3),8(r2),scratch2 ; C<1> = A<1>*B<1> - A<2>*B<2>
00000010'EF 00000020'EF 63 06FD 1053 SUBD3  scratch2,scratch1,(r4) ; Real part result
00000010'EF 62 08 A3 65 0709 1054 MULD3  8(r3),(r2),scratch1 ; Imaginary Part Multiply:
00000020'EF 08 A2 63 65 0712 1055 MULD3  (r3),8(r2),scratch2 ; C<2> = A<1>*B<2> + A<2>*B<1>
00000020'EF 00000010'EF 61 071B 1056 ADDD3  scratch1,scratch2,8(r4) ; Imaginary part result
08 A4 0726
04 0728 1057 RET
0729 1058 mul_gc_gc:
00000010'EF 62 63 45FD 0729 1059 MULG3  (r3),(r2),scratch1 ; Real Part Multiply:

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64 00000020'EF 08 A2 08 A3 45FD 0732 1060      MULG3 8(r3),8(r2),scratch2 ; C<1> = A<1>*B<1> - A<2>*B<2>
64 00000010'EF 00000020'EF 43FD 073D 1061      SUBG3 scratch2,scratch1,(r4) ; Real part result
       00000010'EF 62 08 A3 45FD 074A 1062      MULG3 8(r3),(r2),scratch1 ; Imaginary Part Multiply:
       00000020'EF 08 A2 63 45FD 0754 1063      MULG3 (r3),8(r2),scratch2 ; C<2> = A<1>*B<2> + A<2>*B<1>
       00000020'EF 00000010'EF 41FD 075E 1064      ADDG3 scratch1,scratch2,8(r4) ; Imaginary part result
          08 A4 076A
          04 076C 1065      RET
          076D 1066 mul_hc_hc:
64 00000010'EF 62 63 65FD 076D 1067      MULH3 (r3),(r2),scratch1 ; Real Part Multiply:
64 00000020'EF 10 A2 10 A3 65FD 0776 1068      MULH3 16(r3),16(r2),scratch2 ; C<1> = A<1>*B<1> - A<2>*B<2>
       00000010'EF 00000020'EF 63FD 0781 1069      SUBH3 scratch2,scratch1,(r4) ; Real part result
       00000010'EF 62 10 A3 65FD 078E 1070      MULH3 16(r3),(r2),scratch1 ; Imaginary Part Multiply:
       00000020'EF 10 A2 63 65FD 0798 1071      MULH3 (r3),16(r2),scratch2 ; C<2> = A<1>*B<2> + A<2>*B<1>
       00000020'EF 00000010'EF 61FD 07A2 1072      ADDH3 scratch1,scratch2,16(r4); Imaginary part result
          10 A4
          04 0780 1073      RET
          0781 1074
          0781 1075
          0781 1076 :*****
          0781 1077 :***** M O D U L U S and R E M A I N D E R *****
          0781 1078 :
          0781 1079 :
          0781 1080 :*****
          0781 1081
          0781 1082
          0781 1083 : Multiplicative - MOD operation
          0781 1084
          0781 1085 mod_l_l:
64 62 00 00 7A 07B1 1086      EMUL #0,#0,(r2),(r4)
64 64 64 63 7B 07B6 1087      EDIV (r3),(r4),(r4),(r4)
64 64 D5 07BB 1088      TSTL (r4)
       0B 13 07BD 1089      BEQL mod_l_ret$
       55 62 63 CD 07BF 1090      XORL3 (r3),(r2),r5
       55 D5 07C3 1091      TSTL r5
       64 63 03 18 07C5 1092      BGEQ mod_l_ret$
       64 63 C0 07C7 1093      ADDL2 (r3),(r4)
          07CA 1094 mod_l_ret$:
          04 07CA 1095      RET
          07CB 1096
          07CB 1097 mod_lu_lu:
64 62 63 63 D5 07CB 1098      TSTL (r3)
       0B 18 07CD 1099      BGEQ mod_lu$
       64 62 63 C3 07CF 1100      SUBL3 (r3),(r2),(r4)
       0D 1E 07D3 1101      BGEQU mod_lu_ret$
       64 62 D0 07D5 1102      MOVL (r2),(r4)
       08 11 07D8 1103      BRB mod_lu_ret$
          07DA 1104 mod_lu$:
          64 62 D0 07DA 1105      MOVL (r2),(r4)
          64 64 63 7B 07DD 1106      EDIV (r3),(r4),(r4),(r4)
          04 07E2 1107 mod_lu_ret$:
          07E2 1108      RET
          07E3 1109
          07E3 1110
          07E3 1111 : Remainder Operators
          07E3 1112
          07E3 1113 rem_l_l:
55 62 00 00 7A 07E3 1114      EMUL #0,#0,(r2),r5

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64	55	55	63	7B	07E8	1115	EDIV	(r3),r5,r5,(r4)	
				04	07ED	1116	RET		
					07EE	1117			
					07EE	1118	rem_lu_lu:		
			63	D5	07EE	1119	TSTL	(r3)	
64	62	63	OB	18	07F0	1120	BGEQ	rem_lu\$	
			C3	07F2		1121	SUBL3	(r3),(r2),(r4)	
64	62	63	OD	1E	07F6	1122	BGEQU	rem_lu_rets	
			D0	07F8		1123	MOVL	(r2),(r4)	
			08	11	07FB	1124	BRB	rem_lu_rets	
					07FD	1125	rem_lu\$:		
64	64	64	64	D0	07FD	1126	MOVL	(r2),(r4)	
			63	7B	0800	1127	EDIV	(r3),(r4),(r4),(r4)	
					0805	1128	rem_lu_rets\$:		
				04	0805	1129	RET		
					0806	1130			
					0806	1131			
					0806	1132	*****	*****	
					0806	1133	:		
					0806	1134	S H I F T		
					0806	1135	:		
					0806	1136	*****	*****	
					0806	1137			
					0806	1138			
					0806	1139	: Shift Operators		
					0806	1140	:		
64	62	63	78	0806	1141	shift_left_ll:		; same as shift_left_lu_lu	
			04	080A	1142	ASHL	(r3),(r2),(r4)		
					1143	RET			
		FACD	31	080B	1144	shift_left_ls\$:			
					1145	BRW	shift_count_negative		
					080E	1146			
					080E	1147	shift_rt_ll:		
			63	D5	080E	1148	TSTL	(r3)	
			08	19	0810	1149	BLSS	shift_rt_ls\$	
64	62	53	CE	0812	1150	MNEGL	(r3),r3		
			53	63	78	0815	1151	ASHL	r3,(r2),(r4)
			04	0819	1152	RET			
		FABE	31	081A	1153	shift_rt_ls\$:			
					1154	BRW	shift_count_negative		
					081D	1155			
					081D	1156	shift_rt_lu_lu:		
			63	D5	081D	1157	TSTL	(r3)	
			21	19	081F	1158	BLSS	shift_rt_lu\$	
		53	63	CE	0821	1159	MNEGL	(r3),r3	
			53	D5	0824	1160	TSTL	r3	
			16	13	0826	1161	BEQL	set_shift_result	
		55	53	D0	0828	1162	MOVL	r3,r5	
			55	D6	082B	1163	INCL	r5	
			55	78	082D	1164	ASHL	r5,#80000000,r6	
56	04C4B400	8F	55	78	0835	1165	ASHL	r3,(r2),r5	
		55	62	53	0839	1166	BICL3	r6,r5,(r4)	
		64	55	56	04	083D	1167	RET	
					083E	1168	set_shift_result:		
		64	62	D0	083E	1169	MOVL	(r2),(r4)	
				04	0841	1170	RET		
					0842	1171	shift_rt_lu\$:		

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FA96 31 0842 1172      BRW      shift_count_negative
          0845 1173
          0845 1174
          0845 1175 :*****
          0845 1176 : P O W E R
          0845 1177
          0845 1178
          0845 1179 :*****
          0845 1180
          0845 1181
          0845 1182 : Power of Operators
          0845 1183 :
          0845 1184 power_w_w:
    00000000'GF 7E 63 3C 0845 1185 MOVZWL (r3),-(SP)
    00000000'GF 7E 62 3C 0848 1186 MOVZWL (r2),-(SP)
    64 50 B0 084B 1187 CALLS #2,G^OTSS$POWII
    64 50 B0 0852 1188 MOVW r0,(r4)
    64 50 B0 0855 1189 RET
    00000000'GF 63 DD 0856 1190
    62 DD 0856 1191 power_l_l:
    02 FB 0858 1192 PUSHL (r3)
    64 50 D0 085A 1193 PUSHL (r2)
    04 0861 1194 CALLS #2,G^OTSS$POWJJ
    64 50 D0 0864 1195 MOVL r0,(r4)
    64 50 D0 0865 1196 RET
    00000000'GF 7E 63 D0 0865 1197
    7E 62 50 0868 1198 power_f_l:
    02 FB 086B 1199 MOVL (r3),-(SP)
    64 50 50 0872 1200 MOVF (r2),-(SP)
    04 0875 1201 CALLS #2,G^OTSS$POWRJ
    64 50 50 0876 1202 MOVF r0,(r4)
    64 50 50 0876 1203 RET
    00000000'GF 7E 63 D0 0876 1204
    7E 62 70 0879 1205 power_d_l:
    02 FB 087C 1206 MOVL (r3),-(SP)
    64 50 70 0883 1207 MOVD (r2),-(SP)
    04 0886 1208 CALLS #3,G^OTSS$POWDJ
    64 50 70 0887 1209 MOVD r0,(r4)
    64 50 70 0887 1210 RET
    00000000'GF 7E 63 D0 0887 1211
    7E 62 50FD 088A 1212 power_g_l:
    02 FB 088E 1213 MOVL (r3),-(SP)
    64 50 50FD 0895 1214 MOVG (r2),-(SP)
    04 0899 1215 CALLS #3,G^OTSS$POWGJ
    64 50 50FD 089A 1216 MOVG r0,(r4)
    64 50 50FD 089A 1217 RET
    00000000'GF 7E 63 D0 089A 1218
    7E 62 70FD 089D 1219 power_h_l:
    02 FB 08A1 1220 MOVL (r3),-(SP)
    64 50 70FD 08A8 1221 MOVH (r2),-(SP)
    04 08AC 1222 CALLS #5,G^OTSS$POWHJ_R3
    64 50 70FD 08AD 1223 MOVH r0,(r4)
    64 50 70FD 08AD 1224 RET
    00000000'GF 63 08AD 1225
    00000000'GF 63 08AD 1226 : Note that any time a library routine is called, the imaginary portion :KG001
    00000000'GF 63 08AD 1227 : of the real number must be pushed on the stack before the real part. :KG001
    00000000'GF 63 08AD 1228

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000000000'GF	7E 04	63 A2	D0 08AD	1229 power_fc_l:	MOVL (r3),-(SP)		:KG001
	7E 62	50 FB	08B0 08B4	1230 1231 1232	MOVF 4(r2),-(SP) MOVF (r2),-(SP)		:KG001
	64 50	50 08BE	08C1	1233 1234 1235	CALLS #3,G^OTS\$POWCJ MOVF r0,(r4) MOVF r1,4(r4)		
	04 A4	51 08C5	04 08C6	1236 1237	RET		
	7E 08	63 A2	D0 08C6	1238 power_dc_l:	MOVL (r3),-(SP)		:KG001
	7E 62	70 FB	08C9 08CD	1239 1240 1241	MOVD 8(r2),-(SP) MOVD (r2),-(SP)		:KG001
	64 50	70 08D0	08D7	1242 1243	CALLS #5,G^OTS\$POWCDJ_R3 MOVD r0,(r4)		
	08 A4	52 70	08DA 08DE	1244 1245	MOVD r2,8(r4) RET		
			08DF	1246			
	7E 08	63 A2	D0 08DF	1247 power_gc_l:	MOVL (r3),-(SP)		:KG001
	7E 62	50FD	08E2	1248 1249	MOVG 8(r2),-(SP) MOVG (r2),-(SP)		:KG001
	64 50	50FD	08E7	1250	CALLS #5,G^OTS\$POWCGJ_R3		
	08 A4	52 50FD	08F2 08F6	1251 1252 1253	MOVG r0,(r4) MOVG r2,8(r4)		
			08FB	1254	RET		
			08FC	1255			
	7E	63	50 08FC	1256 power_f_f:	MOVF (r3),-(SP)		
	7E	62	50 08FF	1257 1258	MOVF (r2),-(SP)		
	64	50	FB 0902	1259	CALLS #2,G^OTS\$POWRR		
			0909	1260	MOVF r0,(r4)		
			090C	1261	RET		
			090D	1262			
	7E	63	50 090D	1263 power_d_f:	MOVF (r3),-(SP)		
	7E	62	70 0910	1264 1265	MOVD (r2),-(SP)		
	64	50	FB 0913	1266	CALLS #3,G^OTS\$POWDR		
			091A	1267	MOVD r0,(r4)		
			091D	1268	RET		
			091E	1269			
	7E	63	70 091E	1270 power_f_d:	MOVD (r3),-(SP)		
	7E	62	50 0921	1271 1272	MOVF (r2),-(SP)		
	64	50	FB 0924	1273	CALLS #3,G^OTS\$POWRD		
			092B	1274	MOVD r0,(r4)		
			092E	1275	RET		
			092F	1276			
	7E	63	70 092F	1277 power_d_d:	MOVD (r3),-(SP)		
	7E	62	70 0932	1278 1279	MOVD (r2),-(SP)		
	64	50	FB 0935	1280	CALLS #4,G^OTS\$POWDD		
			093C	1281	MOVD r0,(r4)		
			093F	1282	RET		
			0940	1283			
	7E	63	50FD 0940	1284 power_g_g:	MOVG (r3),-(SP)		

dbg\$perform_operator

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00000000'GF 7E 62 50FD 0944 1286 MOVG (r2),-(SP)
              04 FB 0948 1287 CALLS #4,G^OTSSPOWGG
00000000'GF 64 50 50FD 094F 1288 MOVG r0,(r4)
              04 0953 1289 RET
              0954 1290
              0954 1291 power_h_h:
00000000'GF 7E 63 70FD 0954 1292 MOVH (r3),-(SP)
              62 70FD 0958 1293 MOVH (r2),-(SP)
00000000'GF 64 50 FB 095C 1294 CALLS #8,G^OTSSPOWHH_R3
              50 70FD 0963 1295 MOVH r0,(r4)
              04 0967 1296 RET
              0968 1297
              0968 1298 power_fc_fc:
00000000'GF 7E 04 A3 50 0968 1299 MOVF 4(r3),-(SP)
              7E 63 50 096C 1300 MOVF (r3),-(SP)
00000000'GF 7E 04 A2 50 096F 1301 MOVF 4(r2),-(SP)
              12 13 0973 1302 BEQL 1$ ; Check if the first operand=0 ;KG001
00000000'GF 7E 62 50 0975 1303 MOVF (r2),-(SP)
              04 FB 0978 1304 2$: CALLS #4,G^OTSSPOWCC ;KG001
00000000'GF 64 50 097F 1305 MOVF r0,(r4)
00000000'GF 04 A4 51 50 0982 1306 MOVF r1,4(r4)
              04 0986 1307 RET
              0987 1308
00000000'GF 7E 62 50 0987 1309 1$: MOVF (r2),-(SP) ; Check the second
              EC 12 098A 1310 BNEQ 2$ ; Are both = 0? ;KG001
000028ED8 5E 08 AE DE 098C 1311 MOVAF 8(SP),SP ; Yes, get rid of args. ;KG001
00000000'GF 00028ED8 8F DD 0990 1312 PUSHL #dbg$_undexpn ; Signal Undefined Exp. ;KG001
00000000'GF 01 FB 0996 1313 CALLS #1,G^IB$SIGNAL ; Signal it ;KG001
              04 099D 1314 RET ; And exit ;KG001
              099E 1315
00000000'GF 7E 08 A3 70 099E 1316 power_dc_dc:
              63 70 09A2 1317 MOVD 8(r3),-(SP) ; Push imaginary part first ;KG001
00000000'GF 7E 08 A2 70 09A5 1318 MOVD (r3),-(SP) ; Push the real part last ;KG001
              12 13 09A9 1319 MOVD 8(r2),-(SP) ;KG001
00000000'GF 7E 62 70 09AB 1320 BEQL 1$ ; Check if first op=0 ;KG001
              08 FB 09AE 1322 2$: CALLS #8,G^OTSSPOWCDCD_R3 ;KG001
00000000'GF 64 50 70 09B5 1323 MOVD r0,(r4) ;KG001
00000000'GF 08 A4 52 70 09B8 1324 MOVD r2,8(r4) ;KG001
              04 09BC 1325 RET ;KG001
              09BD 1326
00000000'GF 7E 62 70 09BD 1327 1$: MOVD (r2),-(SP) ; Same as F, almost ;KG001
              EC 12 09C0 1328 BNEQ 2$ ;KG001
000028ED8 5E 08 AE 7E 09C2 1329 MOVAD 8(SP),SP ;KG001
00000000'GF 00028ED8 8F DD 09C6 1330 PUSHL #dbg$_undexpn ;KG001
00000000'GF 01 FB 09CC 1331 CALLS #1,G^IB$SIGNAL ;KG001
              04 09D3 1332 RET ;KG001
              09D4 1333
00000000'GF 7E 08 A3 50FD 09D4 1334 power_gc_gc:
              63 50FD 09D9 1335 MOVG 8(r3),-(SP) ; See comments for FC&DC ;KG001
00000000'GF 7E 08 A2 50FD 09DD 1336 MOVG (r3),-(SP) ;KG001
              15 13 09E2 1337 MOVG 8(r2),-(SP) ;KG001
00000000'GF 7E 62 50FD 09E4 1338 BEQL 1$ ;KG001
              08 FB 09E8 1340 2$: CALLS #8,G^OT SPOWCGCG_R3 ;KG001
00000000'GF 64 50 50FD 09EF 1341 MOVG r0,(r4) ;KG001
00000000'GF 08 A4 52 50FD 09F3 1342 MOVG r2,8(r4) ;KG001

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dbg\$perform_operator

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        04 09F8 1343      RET
        09F9 1344
7E   62 50FD 09F9 1345 1$:    MOVG   (r2),-(SP)
        E9 12 09FD 1346  BNEQ   2$
        5E 08 AE 09FF 1347  MOVAG   8(SP),SP
00028ED8 8F DD 0A03 1348  PUSHL   #dbg$,undexpn
00000000'GF 01 FB 0A09 1349  CALLS   #1,G^[IB$SIGNAL
        04 0A10 1350  RET
        0A11 1351
        0A11 1352
        0A11 1353 :*****
        0A11 1354 :      C H A R     A N D     B I T     S T R I N G
        0A11 1355 .
        0A11 1356 .
        0A11 1357 .
        0A11 1358 .
        0A11 1359 .
        0A11 1360 : Concatenation
        0A11 1361 :
        0A11 1362 concat_t t:
00000038'EF  DD 0A11 1363  PUSHL   arg2_desc
00000030'EF  DD 0A17 1364  PUSHL   arg1_desc
00000040'EF  DD 0A1D 1365  PUSHL   result_desc
00000000'GF  03 FB 0A23 1366  CALLS   #3,G^STR$CONCAT
        01 50 D1 0A2A 1367  CMPL   r0,#sss_normal
        01 12 0A2D 1368  BNEQ   concat_t$
        04 0A2F 1369  RET
        0A30 1370 concat_t$:
51  00000030'FF  3C 0A30 1371  MOVZWL  @arg1_desc,r1
52  00000038'FF  3C 0A37 1372  MOVZWL  @arg2_desc,r2
53  00000040'FF  3C 0A3E 1373  MOVZWL  @result_desc,r3
        52 51 C0 0A45 1374  ADDL2   r1,r2
        53 52 D1 0A48 1375  CMPL   r2,r3
        03 15 0A4B 1376  BLEQ   concat_ok$
        F899 31 0A4D 1377  BRW    string_truncate
        04 0A50 1378 concat_ok$:
        0A51 1379  RET
        0A51 1380
        0A51 1381 eql_vt_vt:
63  62 B1 0A51 1382  CMPW   (r2),(r3)
        0D 13 0A54 1383  BEQL   eql_t_t
0002866B 8F  DD 0A56 1384  PUSHL   #dbg$-strngpad
00000000'GF  01 FB 0A5C 1385  CALLS   #1,G^[IB$SIGNAL
        0A63 1386 eql_t_t:
        64 01 D0 0A63 1387  MOVL   #1,(r4)
        00000038'EF  DD 0A66 1388  PUSHL   arg2_desc
        00000030'EF  DD 0A6C 1389  PUSHL   arg1_desc
00000000'GF  02 FB 0A72 1390  CALLS   #2,G^STR$COMPARE
        50 D5 0A79 1391  TSTL   r0
        02 13 0A7B 1392  BEQL   eql_t$
        64 D4 0A7D 1393  CLRL   (r4)
        0A7F 1394 eql_t$:
        F883 31 0A7F 1395  BRW    branch_ret
        0A82 1396
        0A82 1397
        0A82 1398 geq_vt_vt:
63  62 B1 0A82 1399  CMPW   (r2),(r3)

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dbg\$perform_operator

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0002866B 0D 13 0A85 1400 BEQL geq_t_t
00000000'GF 01 DD 0A87 1401 PUSHL #dbgs$ strngpad
                                CALLS #1,G^[IB$SIGNAL

00000000'GF 01 FB 0A8D 1402
00000038'EF 01 DO 0A94 1403 geq_t_t:
00000030'EF 02 DD 0A97 1404 MOVL #1,(r4)
00000000'GF 02 FB 0A9D 1405 PUSHL arg2_desc
                                CALLS #2,G^STR$COMPARE
00000000'GF 02 FB 0AA3 1406 PUSHL arg1_desc
00000038'EF 02 D5 0AAA 1407 TSTL r0
00000030'EF 02 18 0AAC 1408 BGEQ geq_t$ 
00000000'GF 02 D4 0AAE 1410 CLRL (r4)

F852 31 0AB0 1411 geq_t$:
0002866B 0D 13 0AB3 1412 BRW branch_ret
00000000'GF 01 FB 0AB3 1413

00000000'GF 01 B1 0AB3 1414 gtr_vt_vt:
0002866B 0D 13 0AB6 1415 CMPW (r2),(r3)
00000000'GF 01 FB 0AB8 1416 BEQL gtr_t_t
                                PUSHL #dbgs$ strngpad
                                CALLS #1,G^[IB$SIGNAL

00000000'GF 02 FB 0ACE 1417
00000038'EF 02 D5 0ADB 1418
00000030'EF 02 14 0ADD 1419 gtr_t_t:
00000000'GF 02 FB 0AC5 1420 MOVL #1,(r4)
00000038'EF 02 D5 0AC8 1421 PUSHL arg2_desc
00000030'EF 02 DD 0ACE 1422 PUSHL arg1_desc
00000000'GF 02 FB 0AD4 1423 CALLS #2,G^STR$COMPARE
00000000'GF 02 D5 0ADB 1424 TSTL r0
00000038'EF 02 14 0ADD 1425 BGTR gtr_t$ 
00000030'EF 02 D4 0ADF 1426 CLRL (r4)

F821 31 0AE1 1427 gtr_t$:
0002866B 0D 13 0AE1 1428 BRW branch_ret
00000000'GF 01 FB 0AE4 1429
00000000'GF 01 FB 0AE4 1430

00000000'GF 01 B1 0AE4 1431 leq_vt_vt:
0002866B 0D 13 0AE7 1432 CMPW (r2),(r3)
00000000'GF 01 FB 0AE9 1433 BEQL leq_t_t
                                PUSHL #dbgs$ strngpad
                                CALLS #1,G^[IB$SIGNAL

00000000'GF 01 FB 0AEF 1435
00000038'EF 01 DO 0AF6 1436 leq_t_t:
00000030'EF 01 DD 0AF6 1437 MOVL #1,(r4)
00000000'GF 01 FB 0AF9 1438 PUSHL arg2_desc
00000038'EF 01 DD 0AFF 1439 PUSHL arg1_desc
00000000'GF 01 FB 0B05 1440 CALLS #2,G^STR$COMPARE
00000000'GF 01 D5 0B0C 1441 TSTL r0
00000038'EF 01 15 0B0E 1442 BLEQ leq_t$ 
00000030'EF 01 D4 0B10 1443 CLRL (r4)

F7F0 31 0B12 1444 leq_t$:
0002866B 0D 13 0B12 1445 BRW branch_ret
00000000'GF 01 FB 0B15 1446
00000000'GF 01 FB 0B15 1447

00000000'GF 01 B1 0B15 1448 lss_vt_vt:
0002866B 0D 13 0B18 1449 CMPW (r2),(r3)
00000000'GF 01 FB 0B1A 1450 BEQL lss_t_t
                                PUSHL #dbgs$ strngpad
                                CALLS #1,G^[IB$SIGNAL

00000000'GF 01 FB 0B20 1451
00000038'EF 01 DO 0B27 1452 lss_t_t:
00000030'EF 01 DD 0B27 1453 MOVL #1,(r4)
00000038'EF 01 DD 0B2A 1454 PUSHL arg2_desc
00000030'EF 01 DD 0B30 1455 PUSHL arg1_desc
00000000'GF 01 DD 0B30 1456

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00000000'GF 02 FB 0B36 1457      CALLS #2,G^STR$COMPARE
              50 D5 0B3D 1458      TSTL r0
              02 19 0B3F 1459      BLSS lss_t$
              64 D4 0B41 1460      CLRL (r4)
              F7BF 31 0B43 1461 lss_t$: BRW branch_ret
              0002866B 8F DD 0B4B 1462      0B46 1463      0B46 1464
              00000000'GF 01 FB 0B51 1465 neq_vt_vt: 0B46 1466      CMPW (r2),(r3)
              63 62 B1 0B46 1467      BEQL neq_t_t
              0D 13 0B49 1468      PUSHL #dbg$ strngpad
              00000038'EF DD 0B5A 1469      CALLS #1,G^IB$SIGNAL
              00000030'EF DD 0B60 1470 neq_t_t: 0B58 1471      CLRL (r4)
              00000000'GF 02 FB 0B66 1472      PUSHL arg2_desc
              50 D5 0B6D 1473      PUSHL arg1_desc
              03 13 0B6F 1474      CALLS #2,G^STR$COMPARE
              64 01 D0 0B71 1475      TSTL r0
              F78E 31 0B74 1476      BEQL neq_t$ 0B71 1477      MOVL #1,r4
              0B74 1478 neq_ts$: 0B74 1479      BRW branch_ret
              0B77 1480
              0B77 1481
              0B77 1482 *****
              0B77 1483 :
              0B77 1484 : E Q L and N E Q
              0B77 1485 :
              0B77 1486 *****
              0B77 1487
              0B77 1488
              0B77 1489 : Equality Operators
              0B77 1490 :
              0B77 1491 eql_b_b: 0B77 1492      CLRL (r4)
              63 64 D4 0B77 1493      CMPB (r2),(r3)
              63 62 91 0B79 1494      BNEQ eql_bs
              03 12 0B7C 1495      MOVL #1,r4
              64 01 D0 0B7E 1496 eql_bs: 0B81 1496      BRW branch_ret
              F781 31 0B81 1497
              0B84 1498
              0B84 1499 eql_w_w: 0B84 1500      CLRL (r4)
              63 64 D4 0B84 1501      CMPW (r2),(r3)
              63 62 B1 0B86 1502      BNEQ eql_ws
              03 12 0B89 1503      MOVL #1,r4
              64 01 D0 0B8B 1504 eql_ws: 0B8E 1505      BRW branch_ret
              F774 31 0B8E 1506
              0B91 1507 eql_l_l: 0B91 1508      CLRL (r4)
              63 64 D4 0B91 1509      CMPL (r2),(r3)
              63 62 D1 0B93 1510      BNEQ eql_ls
              03 12 0B96 1511      MOVL #1,r4
              64 01 D0 0B98 1512 eql_ls: 0B98 1513      BRW branch_ret

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dbg\$perform_operator						
		0B9E	1514			
		0B9E	1515	eql_f_f:		
63	64	D4	1516	CLRL	(r4)	
62	51	OBA0	1517	CMPF	(r2),(r3)	
03	12	OBA3	1518	BNEQ	eql_f\$	
64	01	D0	1519	MOVL	#1,r4)	
F75A	31	OBA8	1520	eql_f\$:		
		OBAB	1521	BRW	branch_ret	
		OBAB	1522			
		OBAB	1523	eql_d_d:		
63	64	D4	1524	CLRL	(r4)	
62	71	OBAD	1525	CMPD	(r2),(r3)	
03	12	OBBO	1526	BNEQ	eql_d\$	
64	01	D0	1527	MOVL	#1,r4)	
F74D	31	OBBS	1528	eql_d\$:		
		OBBS	1529	BRW	branch_ret	
		OBBS	1530			
		OBBS	1531	eql_g_g:		
63	64	D4	1532	CLRL	(r4)	
62	51FD	OBBA	1533	CMPG	(r2),(r3)	
03	12	OBBE	1534	BNEQ	eql_g\$	
64	01	D0	1535	MOVL	#1,r4)	
F73F	31	OBBC	1536	eql_g\$:		
		OBBC	1537	BRW	branch_ret	
		OBBC	1538			
		OBBC	1539	eql_h_h:		
63	64	D4	1540	CLRL	(r4)	
62	71FD	OBCC	1541	CMPH	(r2),(r3)	
03	12	OBCE	1542	BNEQ	eql_h\$	
64	01	D0	1543	MOVL	#1,r4)	
F731	31	OBDD	1544	eql_h\$:		
		OBDD	1545	BRW	branch_ret	
		OBDD	1546			
		OBDD	1547	eql_fc_fc:		
63	64	D4	1548	CLRL	(r4)	
62	51	OBDD	1549	CMPF	(r2),(r3)	
0A	12	OBDB	1550	BNEQ	eql_fc\$	
04 A3	04 A2	51	OBEO	1551	CMPF	4(r2),4(r3)
03	12	OBEO	1552	BNEQ	eql_fc\$	
64	01	D0	1553	MOVL	#1,r4)	
F71D	31	OBEE	1554	eql_fc\$:		
		OBEE	1555	BRW	branch_ret	
		OBEE	1556			
		OBEE	1557	eql_dc_dc:		
63	64	D4	1558	CLRL	(r4)	
62	71	OBEA	1559	CMPD	(r2),(r3)	
0A	12	OBED	1560	BNEQ	eql_dc\$	
08 A3	08 A2	71	OBEF	1561	CMPD	8(r2),8(r3)
03	12	OBF4	1562	BNEQ	eql_dc\$	
64	01	D0	1563	MOVL	#1,r4)	
F709	31	OBF9	1564	eql_dc\$:		
		OBFC	1565	BRW	branch_ret	
		OBFC	1566			
		OBFC	1567	eql_gc_gc:		
63	64	D4	1568	CLRL	(r4)	
62	51FD	OBFE	1569	CMPG	(r2),(r3)	
0B	12	OC02	1570	BNEQ	eql_gc\$	

dbg\$perform_operator						
08	A3	08	A2	51FD	0C04	1571
		03	12	0C0A	1572	CMPG
64	01	D0	0C0C	1573	BNEQ	8(r2),8(r3)
			0C0F	1574	MOVL	eql_gc\$
F6F3	31		0C0F	1575	BRW	#1,r4)
			OC12	1576		eql_gc\$: branch_ret
			OC12	1577		
64	62	D4	0C12	1578	CLRL	(r4)
63	62	71FD	0C14	1579	CMPH	(r2),(r3)
0B	12	0C18	1580	BNEQ	eql_hc\$	
10	A3	10	A2	71FD	0C1A	CMPH
		03	12	0C20	1581	16(r2),16(r3)
64	01	D0	0C22	1582	BNEQ	eql_hc\$
			0C25	1583	MOVL	#1,r4)
F6DD	31		0C25	1584	BRW	eql_hc\$: branch_ret
			0C28	1585		
			0C28	1586		
			0C28	1587		
			0C28	1588		
64	62	D4	0C28	1589	CLRL	neq_b_b:
63	62	91	0C2A	1590	CMPB	(r4)
03	13	0C2D	1591	BEQL	(r2),(r3)	
64	01	D0	0C2F	1592	MOVL	neq_b\$
			0C32	1593	BRW	#1,r4)
F6D0	31		0C32	1594		neq_bs\$: branch_ret
			0C35	1595		
			0C35	1596	CLRL	neq_w_w:
64	62	D4	0C35	1597	CMPW	(r4)
63	62	B1	0C37	1598	BEQL	(r2),(r3)
03	13	0C3A	1599	MOVL	neq_w\$	
64	01	D0	0C3C	1600	BRW	#1,r4)
			0C3F	1601	BRW	neq_ws\$: branch_ret
F6C3	31		0C3F	1602		
			0C42	1603		
			0C42	1604	CLRL	neq_l_l:
64	62	D4	0C42	1605	CMPL	(r4)
63	62	D1	0C44	1606	BEQL	(r2),(r3)
03	13	0C47	1607	MOVL	neq_l\$	
64	01	D0	0C49	1608	BRW	#1,r4)
			0C4C	1609	BRW	neq_ls\$: branch_ret
F6B6	31		0C4C	1610		
			0C4F	1611		
			0C4F	1612	CLRL	neq_f_f:
64	62	D4	0C4F	1613	CMPF	(r4)
63	62	51	0C51	1614	BEQL	(r2),(r3)
03	13	0C54	1615	MOVL	neq_f\$	
64	01	D0	0C56	1616	BRW	#1,r4)
			0C59	1617	BRW	neq_fs\$: branch_ret
F6A9	31		0C59	1618		
			0C5C	1619		
			0C5C	1620	CLRL	neq_d_d:
64	62	D4	0C5C	1621	CMPD	(r4)
63	62	71	0C5E	1622	BEQL	(r2),(r3)
03	13	0C61	1623	MOVL	neq_d\$	
64	01	D0	0C63	1624	BRW	#1,r4)
			0C66	1625	BRW	neq_ds\$: branch_ret
F69C	31		0C66	1626		
			0C69	1627		

dbg\$perform_operator

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      0C69 1628 neq_g_g:
  63 64 D4 0C69 1629 CLRL   (r4)
  62 51FD 0C6B 1630 CMPG   (r2),(r3)
  03 13 0C6F 1631 BEQL   neq_g$ 
  64 01 D0 0C71 1632 MOVL   #1,(r4)
  F68E 31 0C74 1633 neq_g$:
  0C77 1634 BRW    branch_ret
  0C77 1635
  0C77 1636 neq_h_h:
  63 64 D4 0C77 1637 CLRL   (r4)
  62 71FD 0C79 1638 CMPH   (r2),(r3)
  03 13 0C7D 1639 BEQL   neq_h$ 
  64 01 D0 0C7F 1640 MOVL   #1,(r4)
  F680 31 0C82 1641 neq_h$:
  0C82 1642 BRW    branch_ret
  0C85 1643
  0C85 1644 neq_fc_fc:
  63 62 51 0C85 1645 CMPF   (r2),(r3)
  02 12 0C88 1646 BNEQ   test_imaginaryf
  64 D4 0C8A 1647 CLRL   (r4)
  04 A3 04 A2 0C8C 1648 test_imaginaryf:
  51 0C8C 1649 CMPF   4(r2),4(r3)
  03 13 0C91 1650 BEQL   neq_fc$ 
  64 01 D0 0C93 1651 MOVL   #1,(r4)
  F66C 31 0C96 1652 neq_fc$:
  0C96 1653 BRW    branch_ret
  0C99 1654
  0C99 1655 neq_dc_dc:
  63 62 71 0C99 1656 CMPD   (r2),(r3)
  02 12 0C9C 1657 BNEQ   test_imaginaryd
  64 D4 0C9E 1658 CLRL   (r4)
  08 A3 08 A2 0CA0 1659 test_imaginaryd:
  71 0CA0 1660 CMPD   8(r2),8(r3)
  03 13 0CA5 1661 BEQL   neq_dc$ 
  64 01 D0 0CA7 1662 MOVL   #1,(r4)
  F658 31 0CAA 1663 neq_dc$:
  0CAA 1664 BRW    branch_ret
  0CAD 1665
  0CAD 1666 neq_gc_gc:
  63 62 51FD 0CAD 1667 CMPG   (r2),(r3)
  02 12 0CB1 1668 BNEQ   test_imaginaryg
  64 D4 0CB3 1669 CLRL   (r4)
  08 A3 08 A2 51FD 0CB5 1670 test_imaginaryg:
  71 0CB5 1671 CMPG   8(r2),8(r3)
  03 13 0CBB 1672 BEQL   neq_gc$ 
  64 01 D0 0CBD 1673 MOVL   #1,(r4)
  F642 31 0CC0 1674 neq_gc$:
  0CC0 1675 BRW    branch_ret
  0CC3 1676
  0CC3 1677 neq_hc_hc:
  63 62 71FD 0CC3 1678 CMPH   (r2),(r3)
  02 12 0CC7 1679 BNEQ   test_imaginaryh
  64 D4 0CC9 1680 CLRL   (r4)
  10 A3 10 A2 71FD 0CCB 1681 test_imaginaryh:
  71 0CCB 1682 CMPH   16(r2),16(r3)
  03 13 0CD1 1683 BEQL   neq_hc$ 
  64 01 D0 0CD3 1684 MOVL   #1,(r4)

```

dbg\$perform_operator

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F62C 31 0CD6 1685 neq_hc$: BRW branch_ret
      0CD6 1686
      0CD9 1687
      0CD9 1688
      0CD9 1689 ;***** G E Q and G T R and L E Q and L S S
      0CD9 1690
      0CD9 1691
      0CD9 1692
      0CD9 1693 ;*****
      0CD9 1694
      0CD9 1695
      0CD9 1696 ; Relational Operators
      0CD9 1697
      0CD9 1698 geq_b_b:
64 01 D0 0CD9 1699 MOVL #1,(r4)
63 62 91 0CDC 1700 CMPB (r2),(r3)
63 62 B1 0CEC 1701 BGEQ geq_b$
64 02 18 0CDF 1702 CLRL (r4)
F61F 31 0CE3 1703 geq_b$:
64 01 D0 0CE3 1704 BRW branch_ret
63 62 91 0CE6 1705
64 02 18 0CE9 1706 geq_w_w:
64 01 D0 0CE6 1707 MOVL #1,(r4)
63 62 B1 0CE9 1708 CMPW (r2),(r3)
63 62 D1 0CEC 1709 BGEQ geq_w$
64 02 18 0CEC 1710 CLRL (r4)
F612 31 0CF0 1711 geq_w$:
64 01 D0 0CF0 1712 BRW branch_ret
63 62 91 0CF3 1713
64 02 18 0CF3 1714 geq_l_l:
64 01 D0 0CF3 1715 MOVL #1,(r4)
63 62 D1 0CF6 1716 CMPL (r2),(r3)
63 62 91 0CF6 1717 BGEQ geq_l$
64 02 18 0CF9 1718 CLRL (r4)
F605 31 0CFD 1719 geq_l$:
64 01 D0 0CFD 1720 BRW branch_ret
63 62 91 0D00 1721
64 02 18 0D00 1722 geq_lu_lu:
64 01 D0 0D00 1723 MOVL #1,(r4)
63 62 D1 0D03 1724 CMPL (r2),(r3)
63 62 91 0D03 1725 BGEQU geq_lu$
64 02 1E 0D06 1726 CLRL (r4)
F5F8 31 0DOA 1727 geq_lu$:
64 01 D0 0DOA 1728 BRW branch_ret
63 62 91 0DOD 1729
64 02 1E 0DOD 1730 geq_f_f:
64 01 D0 0DOD 1731 MOVL #1,(r4)
63 62 51 0D10 1732 CMPF (r2),(r3)
63 62 91 0D10 1733 BGEQ geq_f$
64 02 18 0D13 1734 CLRL (r4)
F5EB 31 0D17 1735 geq_f$:
64 01 D0 0D17 1736 BRW branch_ret
63 62 91 0D1A 1737
64 02 18 0D1A 1738 geq_d_d:
64 01 D0 0D1A 1739 MOVL #1,(r4)
63 62 71 0D1D 1740 CMPD (r2),(r3)
63 62 91 0D1D 1741 BGEQ geq_d$
```

dbg\$perform_operator

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64 D4 0D22 1742      CLRL   (r4)
F5DE 31 0D24 1743 geq_d$: BRW    branch_ret
                  0D24 1744
                  0D27 1745
                  0D27 1746 geq_g_g:
64 01 D0 0D27 1747      MOVL   #1,(r4)
63 62 51FD 0D2A 1748      CMPG   (r2),(r3)
02 18 0D2E 1749      BGEQ   geq_g$ 
64 D4 0D30 1750      CLRL   (r4)
64 D4 0D32 1751 geq_g$:
F5D0 31 0D32 1752      BRW    branch_ret
                  0D35 1753
                  0D35 1754 geq_h_h:
64 01 D0 0D35 1755      MOVL   #1,(r4)
63 62 71FD 0D38 1756      CMPH   (r2),(r3)
02 18 0D3C 1757      BGEQ   geq_h$ 
64 D4 0D3E 1758      CLRL   (r4)
64 D4 0D40 1759 geq_h$:
F5C2 31 0D40 1760      BRW    branch_ret
                  0D43 1761
                  0D43 1762
                  0D43 1763 gtr_b_b:
64 01 D0 0D43 1764      MOVL   #1,(r4)
63 62 91 0D46 1765      CMPB   (r2),(r3)
02 14 0D49 1766      BGTR   gtr_b$ 
64 D4 0D4B 1767      CLRL   (r4)
64 D4 0D4D 1768 gtr_b$:
F5B5 31 0D4D 1769      BRW    branch_ret
                  0D50 1770
                  0D50 1771 gtr_w_w:
64 01 D0 0D50 1772      MOVL   #1,(r4)
63 62 B1 0D53 1773      CMPW   (r2),(r3)
02 14 0D56 1774      BGTR   gtr_w$ 
64 D4 0D58 1775      CLRL   (r4)
64 D4 0D5A 1776 gtr_w$:
F5A8 31 0D5A 1777      BRW    branch_ret
                  0D5D 1778
                  0D5D 1779 gtr_l_l:
64 01 D0 0D5D 1780      MOVL   #1,(r4)
63 62 D1 0D60 1781      CMPL   (r2),(r3)
02 14 0D63 1782      BGTR   gtr_l$ 
64 D4 0D65 1783      CLRL   (r4)
64 D4 0D67 1784 gtr_l$:
F59B 31 0D67 1785      BRW    branch_ret
                  0D6A 1786
                  0D6A 1787 gtr_lu_lu:
64 01 D0 0D6A 1788      MOVL   #1,(r4)
63 62 D1 0D6D 1789      CMPL   (r2),(r3)
02 1A 0D70 1790      BGTRU  gtr_lus
64 D4 0D72 1791      CLRL   (r4)
64 D4 0D74 1792 gtr_lus:
F58E 31 0D74 1793      BRW    branch_ret
                  0D77 1794
                  0D77 1795 gtr_f_f:
64 01 D0 0D77 1796      MOVL   #1,(r4)
63 62 51 0D7A 1797      CMPF   (r2),(r3)
02 14 0D7D 1798      BGTR   gtr_f$ 

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dbg\$perform_operator						
64	D4	0D7F	1799		CLRL	(r4)
F581	31	0D81	1800	gtr_f\$:	BRW	branch_ret
		0D81	1801			
		0D84	1802			
		0D84	1803	gtr_d_d:		
64	01	D0	0D84	1804	MOVL	#1,(r4)
63	62	71	0D87	1805	CMPD	(r2),(r3)
	02	14	0D8A	1806	BGTR	gtr_d\$
	64	D4	0D8C	1807	CLRL	(r4\$)
			0D8E	1808	gtr_d\$:	
F574	31	0D8E	1809		BRW	branch_ret
		0D91	1810			
		0D91	1811	gtr_g_g:		
64	01	D0	0D91	1812	MOVL	#1,(r4)
63	62	51FD	0D94	1813	CMPG	(r2),(r3)
	02	14	0D98	1814	BGTR	gtr_g\$
	64	D4	0D9A	1815	CLRL	(r4\$)
			0D9C	1816	gtr_g\$:	
F566	31	0D9C	1817		BRW	branch_ret
		0D9F	1818			
		0D9F	1819	gtr_h_h:		
64	01	D0	0D9F	1820	MOVL	#1,(r4)
63	62	71FD	0DA2	1821	CMPH	(r2),(r3)
	02	14	0DA6	1822	BGTR	gtr_h\$
	64	D4	0DA8	1823	CLRL	(r4\$)
			0DAA	1824	gtr_h\$:	
F558	31	0DAA	1825		BRW	branch_ret
		ODAD	1826			
		ODAD	1827			
		ODAD	1828	leq_b_b:		
64	01	D0	ODAD	1829	MOVL	#1,(r4)
63	62	91	0DB0	1830	CMPB	(r2),(r3)
	02	15	0DB3	1831	BLEQ	leq_b\$
	64	D4	0DB5	1832	CLRL	(r4\$)
			0DB7	1833	leq_b\$:	
F54B	31	0DB7	1834		BRW	branch_ret
		0DBA	1835			
		0DBA	1836	leq_w_w:		
64	01	D0	0DBA	1837	MOVL	#1,(r4)
63	62	B1	0DBD	1838	CMPW	(r2),(r3)
	02	15	0DC0	1839	BLEQ	leq_w\$
	64	D4	0DC2	1840	CLRL	(r4\$)
			0DC4	1841	leq_w\$:	
F53E	31	0DC4	1842		BRW	branch_ret
		0DC7	1843			
		0DC7	1844	leq_l_l:		
64	01	D0	0DC7	1845	MOVL	#1,(r4)
63	62	D1	0DCA	1846	CMLP	(r2),(r3)
	02	15	0DCD	1847	BLEQ	leq_l\$
	64	D4	0DCF	1848	CLRL	(r4\$)
			0DD1	1849	leq_l\$:	
F531	31	0DD1	1850		BRW	branch_ret
		0DD4	1851			
		0DD4	1852	leq_lu_lu:		
64	01	D0	0DD4	1853	MOVL	#1,(r4)
63	62	D1	0DD7	1854	CMLP	(r2),(r3)
	02	18	0DDA	1855	BLEQU	leq_lus

dbg\$perform_operator						
64	D4	ODDC	1856	CLRL	(r4)	
F524	31	ODDE	1857 leq_lu\$:	BRW	branch_ret	
		ODE1	1858			
		ODE1	1859			
64	01	D0	ODE1	1860 leq_f_f:		
63	62	51	ODE4	1861 MOVL	#1,(r4)	
	02	15	ODE7	1862 CMPF	(r2),(r3)	
64	D4	ODE9	1863 BLEQ	leq_f\$		
		ODEEB	1864 CLRL	(r4)		
F517	31	ODEEB	1865 leq_f\$:	BRW	branch_ret	
		ODEEE	1866			
		ODEEE	1867			
64	01	D0	ODEEE	1868 leq_d_d:		
63	62	71	ODF1	1869 MOVL	#1,(r4)	
	02	15	ODF4	1870 CMPD	(r2),(r3)	
64	D4	ODF6	1871 BLEQ	leq_d\$		
		ODF8	1872 CLRL	(r4)		
F50A	31	ODF8	1873 leq_d\$:	BRW	branch_ret	
		ODFB	1874			
		ODFB	1875			
64	01	D0	ODFB	1876 leq_g_g:		
63	62	51FD	ODFE	1877 MOVL	#1,(r4)	
	02	15	OE02	1878 CMPG	(r2),(r3)	
64	D4	OE04	1879 BLEQ	leq_g\$		
		OE06	1880 CLRL	(r4)		
F4FC	31	OE06	1881 leq_g\$:	BRW	branch_ret	
		OE09	1882			
		OE09	1883			
64	01	D0	OE09	1884 leq_h_h:		
63	62	71FD	OE0C	1885 MOVL	#1,(r4)	
	02	15	OE10	1886 CMPH	(r2),(r3)	
64	D4	OE12	1887 BLEQ	leq_h\$		
		OE14	1888 CLRL	(r4)		
F4EE	31	OE14	1889 leq_h\$:	BRW	branch_ret	
		OE17	1890			
		OE17	1891			
		OE17	1892			
64	01	D0	OE17	1893 lss_b_b:		
63	62	91	OE1A	1894 MOVL	#1,(r4)	
	02	19	OE1D	1895 CMPB	(r2),(r3)	
64	D4	OE1F	1896 BLSS	lss_b\$		
		OE21	1897 CLRL	(r4)		
F4E1	31	OE21	1898 lss_b\$:	BRW	branch_ret	
		OE24	1899			
		OE24	1900			
64	01	D0	OE24	1901 lss_w_w:		
63	62	B1	OE27	1902 MOVL	#1,(r4)	
	02	19	OE2A	1903 CMPW	(r2),(r3)	
64	D4	OE2C	1904 BLSS	lss_w\$		
		OE2E	1905 CLRL	(r4)		
F4D4	31	OE2E	1906 lss_w\$:	BRW	branch_ret	
		OE31	1907			
		OE31	1908			
64	01	D0	OE31	1909 lss_l_l:		
63	62	D1	OE34	1910 MOVL	#1,(r4)	
	02	19	OE37	1911 CMPL	(r2),(r3)	
		OE37	1912 BLSS	lss_l\$		

dbg\$perform_operator

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64 D4 0E39 1913 lss_l$: CLRL (r4)
F4C7 31 0E3B 1914 BRW branch_ret
64 01 0E3E 1915
63 62 D1 0E41 1916 lss_lu_lu:
02 1F 0E44 1917 MOVL #1,(r4)
64 D4 0E46 1918 CMPL (r2),(r3)
          1919 BLSS lss_lu$ (r4)
          1920 CLRL
          1921
64 01 0E48 1922 lss_lus$:
F4BA 31 0E48 1923 BRW branch_ret
          0E4B 1924
          0E4B 1925 lss_f_f:
64 01 0E4B 1926 MOVL #1,(r4)
63 62 51 0E4E 1927 CMPF (r2),(r3)
02 19 0E51 1928 BLSS lss_f$ (r4)
64 D4 0E53 1929 CLRL
          0E55 1930 lss_f$:
F4AD 31 0E55 1931 BRW branch_ret
          0E58 1932
          0E58 1933 lss_d_d:
64 01 0E58 1934 MOVL #1,(r4)
63 62 71 0E5B 1935 CMPD (r2),(r3)
02 19 0E5E 1936 BLSS lss_d$ (r4)
64 D4 0E60 1937 CLRL
          0E62 1938 lss_d$:
F4A0 31 0E62 1939 BRW branch_ret
          0E65 1940
          0E65 1941 lss_g_g:
64 01 0E65 1942 MOVL #1,(r4)
63 62 51FD 0E68 1943 CMPG (r2),(r3)
02 19 0E6C 1944 BLSS lss_g$ (r4)
64 D4 0E6E 1945 CLRL
          0E70 1946 lss_g$:
F492 31 0E70 1947 BRW branch_ret
          0E73 1948
          0E73 1949 lss_h_h:
64 01 0E73 1950 MOVL #1,(r4)
63 62 71FD 0E76 1951 CMPPH (r2),(r3)
02 19 0E7A 1952 BLSS lss_h$ (r4)
64 D4 0E7C 1953 CLRL
          0E7E 1954 lss_h$:
F4B4 31 0E7E 1955 BRW branch_ret
          0E81 1956
          0E81 1957
          0E81 1958
          0E81 1959 ****
          0E81 1960 ****
          0E81 1961 : B I T W I S E   A N D   and   E Q V   and   N O T
          0E81 1962 :   O R   and   X O R   and   I M P
          0E81 1963 :
          0E81 1964 ****
          0E81 1965 :
          0E81 1966 :
          0E81 1967 ; Bitwise Operators
          0E81 1968 :
          0E81 1969 bit_and_b_b:

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dbg\$perform_operator							
64	53	63	92	OE81	1970	MCOMB	(r3),r3
	62	53	8B	OE84	1971	BICB3	r3,(r2),(r4)
			04	OE88	1972	RET	
				OE89	1973	bit_and_w_w:	
64	53	63	B2	OE89	1974	MCOMW	(r3),r3
	62	53	8B	OE8C	1975	BICB3	r3,(r2),(r4)
			04	OE90	1976	RET	
				OE91	1977	bit_and_l_l:	
64	53	63	D2	OE91	1978	MCOML	(r3),r3
	62	53	CB	OE94	1979	BICL3	r3,(r2),(r4)
			04	OE98	1980	RET	
				OE99	1981		
				OE99	1982	bit_eqv_b_b:	
64	53	63	92	OE99	1983	MCOMB	(r3),r3
	62	53	8D	OE9C	1984	XORB3	r3,(r2),(r4)
			04	OEAO	1985	RET	
				OEAI	1986		
				OEAI	1987	bit_eqv_w_w:	
64	53	63	B2	OEAI	1988	MCOMW	(r3),r3
	62	53	AD	OEAI	1989	XORW3	r3,(r2),(r4)
			04	OEAB	1990	RET	
				OEAB	1991		
				OEAB	1992	bit_eqv_l_l:	
64	53	63	D2	OEAB	1993	MCOML	(r3),r3
	62	53	CD	OEAC	1994	XORL3	r3,(r2),(r4)
			04	OEBO	1995	RET	
				OEBO	1996		
				OEBO	1997	bit_not_b:	
64	62	92	OEBO	1998		MCOMB	(r2),(r4)
		04	OEBO	1999		RET	
				OEBS	2000	bit_not_w:	
64	62	B2	OEBS	2001		MCOMW	(r2),(r4)
		04	OEBS	2002		RET	
				OEBS	2003	bit_not_l:	
64	62	D2	OEBS	2004		MCOML	(r2),(r4)
		04	OEBC	2005		RET	
				OEBC	2006		
				OEBC	2007	bit_or_b_b:	
64	62	63	89	OEBC	2008	BISB3	(r3),(r2),(r4)
			04	OECD	2009	RET	
				OECD	2010	bit_or_w_w:	
64	62	63	A9	OECD	2011	BISW3	(r3),(r2),(r4)
			04	OECD	2012	RET	
				OECD	2013	bit_or_l_l:	
64	62	63	C9	OECD	2014	BISL3	(r3),(r2),(r4)
			04	OECD	2015	RET	
				OECD	2016		
				OECD	2017	bit_xor_b_b:	
64	62	63	8D	OECD	2018	XORB3	(r3),(r2),(r4)
			04	OECD	2019	RET	
				OECD	2020	bit_xor_w_w:	
64	62	63	AD	OECD	2021	XORW3	(r3),(r2),(r4)
			04	OECD	2022	RET	
				OECD	2023	bit_xor_l_l:	
64	62	63	CD	OECD	2024	XORL3	(r3),(r2),(r4)
			04	OECD	2025	RET	
				OECD	2026	bit_imp_b_b:	

dbg\$perform_operator

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64 52 62 92 0EDB 2027      MCOMB   (r2), r2
64 63 52 89 0EDE 2028      BISB3   r2, (r3), (r4)
64 52 62 04 0EE2 2029      RET
64 63 52 B2 0EE3 2030      bit_imp_w_w:
64 63 52 A9 0EE3 2031      MCOMW   (r2), r2
64 52 62 04 0EE6 2032      BISW3   r2, (r3), (r4)
64 63 52 C9 0EEE 2033      RET
64 52 62 D2 0EEB 2034      bit_imp_l_l:
64 63 52 04 0EEE 2035      MCOML   (r2), r2
64 63 52 04 0EF2 2036      BISL3   r2, (r3), (r4)
64 52 62 0EF3 2037      RET
64 63 52 0EF3 2038
64 63 52 0EF3 2039
64 63 52 0EF3 2040      ;*****
64 63 52 0EF3 2041      ; LOGICAL AND and NOT and OR
64 63 52 0EF3 2042      ;
64 63 52 0EF3 2043      ;
64 63 52 0EF3 2044      ;
64 63 52 0EF3 2045
64 63 52 0EF3 2046
64 63 52 0EF3 2047      : Logical Operators
64 63 52 0EF3 2048      ;
64 63 52 0EF3 2049      and_b_b:
64 62 95 0EF3 2050      TSTB    (r2)          ; AND
64 20 13 0EF5 2051      BEQL    set_and_result
64 63 95 0EF7 2052      TSTB    (r3)
64 28 13 0EF9 2053      BEQL    set_and_result
64 64 01 00 0EFB 2054      MOVL    #1,r4
64 64 01 04 0EFE 2055      RET
64 62 95 0EFF 2056      and_w_w:
64 62 85 0EFF 2057      TSTW    (r2)
64 20 13 0F01 2058      BEQL    set_and_result
64 63 85 0F03 2059      TSTW    (r3)
64 10 13 0F05 2060      BEQL    set_and_result
64 64 01 00 0F07 2061      MOVL    #1,r4
64 64 01 04 0F0A 2062      RET
64 62 85 0F0B 2063      and_l_l:
64 62 14 0F0B 2064      TSTL    (r2)
64 62 14 0F0D 2065      BEQL    set_and_result
64 63 85 0F0F 2066      TSTL    (r3)
64 10 13 0F11 2067      BEQL    set_and_result
64 64 01 00 0F13 2068      MOVL    #1,r4
64 64 01 04 0F16 2069      RET
64 62 73 0F17 2070      and_d_d:
64 62 08 0F17 2071      TSTD    (r2)
64 62 08 0F19 2072      BEQL    set_and_result
64 63 73 0F1B 2073      TSTD    (r3)
64 04 13 0F1D 2074      BEQL    set_and_result
64 64 01 00 0F1F 2075      MOVL    #1,r4
64 64 01 04 0F22 2076      RET
64 62 95 0F23 2077      set_and_result:
64 64 04 0F23 2078      CLRL    (r4)
64 64 04 0F25 2079      RET
64 62 95 0F26 2080
64 62 95 0F26 2081
64 62 95 0F26 2082      not_b:
64 62 95 0F26 2083      TSTB    (r2)

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dbg\$perform_operator

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18 13 0F28 2084      BEQL   set_not_result
64 D4 0F2A 2085      CLRL   (r4)
          04 0F2C 2086      RET
          0F2D 2087 not_w: TSTW   (r2)
62 B5 0F2D 2088      BEQL   set_not_result
11 13 0F2F 2089      CLRL   (r4)
64 D4 0F31 2090      RET
          04 0F33 2091      OF34 2092 not_l: TSTL   (r2)
62 D5 0F34 2093      BEQL   set_not_result
0A 13 0F36 2094      CLRL   (r4)
64 D4 0F38 2095      RET
          04 0F3A 2096      OF3B 2097 not_d: TSTD   (r2)
62 73 0F3B 2098      BEQL   set_not_result
03 13 0F3D 2099      CLRL   (r4)
64 D4 0F3F 2100      RET
          04 0F41 2101      OF42 2102 set_not_result: MOVL   #1,(r4)
64 01 D0 0F42 2103      04 0F45 2104      OF46 2105      OF46 2106 or_b_b: TSTB   (r2)
62 95 0F46 2107      BNEQ   set_or_result : OR
28 12 0F48 2108      TSTB   (r3)
63 95 0F4A 2109      BNEQ   set_or_result
24 12 0F4C 2110      CLRL   (r4)
64 D4 0F4E 2111      RET
          04 0F50 2112      OF51 2113 or_w_w: TSTW   (r2)
62 B5 0F51 2114      BNEQ   set_or_result
1D 12 0F53 2115      TSTW   (r3)
63 B5 0F55 2116      BNEQ   set_or_result
19 12 0F57 2117      CLRL   (r4)
64 D4 0F59 2118      RET
          04 0F5B 2119      OF5C 2120 or_l_l: TSTL   (r2)
62 D5 0F5C 2121      BNEQ   set_or_result
12 12 0F5E 2122      TSTL   (r3)
63 D5 0F60 2123      BNEQ   set_or_result
0E 12 0F62 2124      CLRL   (r4)
64 D4 0F64 2125      RET
          04 0F66 2126      OF67 2127      OF67 2128 or_d_d: TSTD   (r2)
62 73 0F67 2129      BNEQ   set_or_result
07 12 0F69 2130      TSTD   (r3)
63 73 0F6B 2131      BNEQ   set_or_result
03 12 0F6D 2132      CLRL   (r4)
64 D4 0F6F 2133      RET
          04 0F71 2134      OF72 2135      OF72 2136 set_or_result: MOVL   #1,(r4)
64 01 D0 0F72 2137      04 0F75 2138      OF76 2139      OF76 2140 xor_l_l: RET

```

dbg\$perform_operator

```

62 D5 0F76 2141      TSTL   (r2)
07 13 0F78 2142      BEQL   xor_l_l_1$
63 D5 0F7A 2143      TSTL   (r3)
0A 13 0F7C 2144      BEQL   set_xor_result
64 D4 0F7E 2145      CLRL   (r4)
04 0F80 2146      RET
64 01 0D 0F81 2147  xor_l_l_1$:
07 13 0F81 2148      TSTL   (R3)
03 12 0F83 2149      BNEQ   set_xor_result
64 D4 0F85 2150      CLRL   (r4)
04 0F87 2151      RET
64 01 D0 0F88 2152  set_xor_result:
04 0F8B 2153      MOVL   #1,(r4)
0F8C 2154      RET
0F8C 2155
0F8C 2156 ;*****
0F8C 2157 ;
0F8C 2158 ; U N A R Y   M I N U S   and   P L U S
0F8C 2159 ;
0F8C 2160 ;*****
0F8C 2161
0F8C 2162
0F8C 2163 ; Negating Arithmetic
0F8C 2164 ;
0F8C 2165 unary_minus_b:
64 62 8E 0F8C 2166  MNEG B (r2),(r4)
01 1D 0F8F 2167  BVS   umbs
04 0F91 2168  RET
F31B 31 0F92 2169  umbs:
0F95 2170      BRW   int_overflow
0F95 2171
64 62 AE 0F95 2172  unary_minus_w:
01 1D 0F98 2173  MNEG W (r2),(r4)
04 0F9A 2174  BVS   umws
0F9B 2175  RET
F312 31 0F9B 2176  umws:
0F9E 2177      BRW   int_overflow
0F9E 2178
64 62 CE 0F9E 2179  unary_minus_l:
01 1D 0FA1 2180  MNEG L (r2),(r4)
04 0FA3 2181  BVS   uml$
0FA4 2182  RET
F309 31 0FA4 2183  uml$:
0FA7 2184      BRW   int_overflow
0FA7 2185
64 0000FFFF 8F 62 C3 0FA7 2186  unary_minus_lu:
04 0FAF 2187  SUBC3 (r2),#^FFFF,(r4) : The negative of an unsigned quantity
0FB0 2188  RET : is computed by subtracting its value
0FB0 2189
0FB0 2190  unary_minus_f:
04 0FB3 2191  MNEG F (r2),(r4)
0FB4 2192  RET
64 62 72 0FB4 2193  unary_minus_d:
04 0FB7 2194  MNEG D (r2),(r4)
0FB8 2195  RET
64 62 52FD 0FB8 2196  unary_minus_g:
0FB8 2197  MNEG G (r2),(r4)

```

dbg\$perform_operator

		04	0FBC	2198	RET
		64	62	72FD	2199 unary_minus_h:
				04	0FBD 2200 MNEG H (r2),(r4)
				04	0FC1 2201 RET
				04	0FC2 2202 RET
				04	0FC2 2203 unary_minus_fc:
		04 A4	64 04	62 52	2204 MNEG F (r2),(r4)
				04 A2	52 OFC5 2205 MNEG F 4(r2),4(r4)
				04	0FCA 2206 RET
				04	0FCB 2207 unary_minus_dc:
		08 A4	64 08	62 72	2208 MNEG D (r2),(r4)
				08 A2	72 OFCE 2209 MNEG D 8(r2),8(r4)
				04	0FD3 2210 RET
				04	0FD4 2211 unary_minus_gc:
		08 A4	64 08	62 52FD	2212 MNEG G (r2),(r4)
				08 A2	52FD OFD4 2213 MNEG G 8(r2),8(r4)
				04	0FDE 2214 RET
				04	0FDF 2215 unary_minus_hc:
		10 A4	64 10	62 72FD	2216 MNEG H (r2),(r4)
				10 A2	72FD OFE3 2217 MNEG H 16(r2),16(r4)
				04	0FE9 2218 RET
				04	0FEA 2219 RET
				04	0FEA 2220 RET
				04	0FEA 2221 : Move a scalar quantity
				04	0FEA 2222 :
		64	62	90	0FEA 2223 unary_plus_b:
				04	0FED 2224 MOVB (r2),(r4)
				04	0FEE 2225 RET
		64	62	B0	0FEE 2226 unary_plus_w:
				04	OFF1 2227 MOVW (r2),(r4)
				04	OFF2 2228 RET
		64	62	D0	OFF2 2229 unary_plus_l:
				04	OFF2 2230 MOVL (r2),(r4)
				04	OFF5 2231 RET
				04	OFF6 2232 RET
		64	62	50	OFF6 2233 unary_plus_f:
				04	OFF6 2234 MOVF (r2),(r4)
				04	OFF9 2235 RET
		64	62	70	OFFA 2236 unary_plus_d:
				04	OFFA 2237 MOVD (r2),(r4)
				04	OFFD 2238 RET
		64	62	50FD	OFFE 2239 unary_plus_g:
				04	OFFE 2240 MOVG (r2),(r4)
				04	1002 2241 RET
		64	62	70FD	1003 2242 unary_plus_h:
				04	1003 2243 MOVH (r2),(r4)
				04	1007 2244 RET
				04	1008 2245 RET
		04 A4	64 04	62 50	1008 2246 unary_plus_fc:
				04 A2	50 1008 2247 MOVF (r2),(r4)
				04	1008 2248 MOVF 4(r2),4(r4)
				04	1010 2249 RET
				04	1011 2250 unary_plus_dc:
		08 A4	64 08	62 70	1011 2251 MOVD (r2),(r4)
				08 A2	70 1014 2252 MOVD 8(r2),8(r4)
				04	1019 2253 RET
				04	101A 2254 unary_plus_gc:

dbg\$perform_operator

```

08 A4 64 08 62 50FD 101A 2255    MOVG   (r2),(r4)
          08 A2 50FD 101E 2256    MOVG   8(r2),8(r4)
          04 1024 2257    RET
          1025 2258 unary_plus hc:
10 A4 64 10 62 70FD 1025 2259    MOVH   (r2),(r4)
          10 A2 70FD 1029 2260    MOVH   16(r2),16(r4)
          04 102F 2261    RET
          1030 2262
          1030 2263
          1030 2264 ;*****
          1030 2265 ;*****
          1030 2266 ;ABSOLUTE VALUE
          1030 2267 ;*****
          1030 2268 ;*****
          1030 2269
          1030 2270 abs_b:
          62  95 1030 2271    TSTB   (r2)
          04  19 1032 2272    BLSS   abs_b_negate
          64  62 90 1034 2273    MOVB   (r2),7r4
          04 1037 2274    RET
          64  62 8E 1038 2275 abs_b_negate:
          04 1038 2276    MNEG B (r2),(r4)
          103B 2277    RET
          103C 2278
          103C 2279 abs_w:
          62  B5 103C 2280    TSTW   (r2)
          04  19 103E 2281    BLSS   abs_w_negate
          64  62 80 1040 2282    MOVW   (r2),7r4
          04 1043 2283    RET
          64  62 AE 1044 2284 abs_w_negate:
          04 1044 2285    MNEG W (r2),(r4)
          1047 2286    RET
          1048 2287
          1048 2288 abs_l:
          62  D5 1048 2289    TSTL   (r2)
          04  19 104A 2290    BLSS   abs_l_negate
          64  62 D0 104C 2291    MOVL   (r2),7r4
          04 104F 2292    RET
          64  62 CE 1050 2293 abs_l_negate:
          04 1050 2294    MNEG L (r2),(r4)
          1053 2295    RET
          1054 2296
          1054 2297 abs_f:
          62  53 1054 2298    TSTF   (r2)
          04  19 1056 2299    BLSS   abs_f_negate
          64  62 50 1058 2300    MOVF   (r2),7r4
          04 105B 2301    RET
          64  62 52 105C 2302 abs_f_negate:
          04 105C 2303    MNEG F (r2),(r4)
          105F 2304    RET
          1060 2305
          1060 2306 abs_d:
          62  73 1060 2307    TSTD   (r2)
          04  19 1062 2308    BLSS   abs_d_negate
          64  62 70 1064 2309    MOVD   (r2),7r4
          04 1067 2310    RET
          1068 2311 abs_d_negate:

```

dbg\$perform_operator

```

64 62 72 1068 2312      MNEGD  (r2),(r4)
04 106B 2313      RET
106C 2314
106C 2315 abs_g:
62 53FD 106C 2316      TSTG   (r2)
05 19 106F 2317      BLSS   abs_g_negate
64 62 50FD 1071 2318      MOVG   (r2),(r4)
04 1075 2319      RET
64 62 52FD 1076 2320 abs_g_negate:
04 107A 2321      MNEGG  (r2),(r4)
107B 2322      RET
107B 2323
107B 2324 abs_h:
62 73FD 107B 2325      TSTH   (r2)
B8 19 107E 2326      BLSS   abs_b_negate
64 62 70FD 1080 2327      MOVH   (r2),(r4)
04 1084 2328      RET
64 62 72FD 1085 2329 abs_h_negate:
04 1089 2330      MNEGH  (r2),(r4)
108A 2331      RET
108A 2332
108A 2333
108A 2334
108A 2335
108A 2336 :*****
108A 2337 : D E R E F E R E N C I N G
108A 2338 :
108A 2339 :
108A 2340 :*****
108A 2341
108A 2342
108A 2343 : Dereferencing Pointers
108A 2344
108A 2345 indirect_lu:
00000030'EF DD 108A 2346      PUSHL  arg1_desc
00000000'EF 01 FB 1090 2347      CALLS  #1,d5g$bliss_indirection
64 50  D0 1097 2348      MOVL   r0,(r4)
04 109A 2349      RET
109B 2350
109B 2351 : Indirection of a pointer in language C.
109B 2352 : We pass in the entire value descriptor (because the indirection
109B 2353 needs to look at the typeid). The routine returns a new descriptor
109B 2354 that represents the result of the indirection. We put a pointer
109B 2355 to this new descriptor back into the RESULT_ADDR output parameter.
109B 2356 :
109B 2357 indirect_tptr:
00000034'EF DD 109B 2358      PUSHL  arg1_valdesc
00000000'EF 01 FB 10A1 2359      CALLS  #1,d5g$sc_indirection
14 BC 50  D0 10A8 2360      MOVL   r0,@result_addr(AP)
04 10AC 2361      RET
10AD 2362
10AD 2363
10AD 2364
10AD 2365
10AD 2366 :*****
10AD 2367 : B I T   S E L E C T I O N
10AD 2368 :*****

```

dbg\$perform_operator

```

10AD 2369
10AD 2370
10AD 2371 ; BLISS bit-select operator (X<p,s,e>)
10AD 2372 ;
10AD 2373 bitselect:
00000040'EF DD 10AD 2374      PUSHL   result_desc
00000030'EF DD 10B3 2375      PUSHL   arg1_desc
          04 AC DD 10B9 2376      PUSHL   operator_entry(AP)
00000000'EF  03 FB 10BC 2377      CALLS   #3,dbg$bliss_bitselect
          04 10C3 2378      RET
          10C4 2379
          10C4 2380
          10C4 2381 :*****
          10C4 2382 :
          10C4 2383 : S E T
          10C4 2384 :
          10C4 2385 :*****
          10C4 2386
          10C4 2387
          10C4 2388 : Difference of Two Sets
          10C4 2389
          10C4 2390 difference_set_set:
          55   D4 10C4 2391      CLRL    r5
          56   D4 10C6 2392      CLRL    r6
55   00000030'FF B0 10C8 2393      MOVW    @arg1_desc,r5
56   00000038'FF B0 10CF 2394      MOVW    @arg2_desc,r6
00000040'FF 00000030'FF B0 10D6 2395      MOVW    @arg1_desc,@result_desc
          50 54 D0 10E1 2396      MOVL    r4,r0
          10E4 2397 difference_set1$:
          80 82 83 88 10E4 2398      BICB3  (r3)+,(r2)+,(r0)+
          55 D7 10E8 2399      DECL    r5
          56 D7 10EA 2400      DECL    r6
          55 D5 10EC 2401      TSTL    r5
          06 12 10EE 2402      BNEQ   difference_set2$
          56 D5 10F0 2403      TSTL    r6
          10 12 10F2 2404      BNEQ   difference_set4$
          21 11 10F4 2405      BRB    difference_set_ret$
          10F6 2406 difference_set2$:
          56 D5 10F6 2407      TSTL    r6
          EA 12 10F8 2408      BNEQ   difference_set1$
          10FA 2409 difference_set3$:
          80 82 FF 8F 8B 10FA 2410      BICB3  #^XFF,(r2)+,(r0)+
          F8 55 F5 10FF 2411      SOBGTR r5,difference_set3$
          13 11 1102 2412      BRB    difference_set_ret$
          80 FF 8F 83 8B 1104 2413 difference_set4$:
          F8 56 F5 1109 2414      BICB3  (r3)+,#^XFF,(r0)+
          00000040'FF 00000038'FF B0 110C 2415      SOBGTR r6,difference_set4$
          04 1117 2416      MOVW    @arg2_desc,@result_desc
          1117 2417 difference_set_ret$:
          1118 2418      RET
          1118 2419
          1118 2420
          1118 2421      : Set Equal
          1118 2422      :
          1118 2423      eql_set_set:
          64  D4 1118 2424      CLRL    (r4)
          55  D4 111A 2425      CLRL    r5

```

dbg\$perform_operator

```

55 00000030'FF 56 D4 111C 2426 CLRL r6
56 00000038'FF B0 111E 2427 MOVW aarg1_desc,r5
B0 1125 2428 MOVW aarg2_desc,r6
112C 2429 eql_set1$:
82 83 91 112C 2430 CMPB (r3)+(r2)+  

2D 12 112F 2431 BNEQ egl_set_ret$  

55 D7 1131 2432 DECL r5  

56 D7 1133 2433 DECL r6  

55 D5 1135 2434 TSTL r5  

09 12 1137 2435 BNEQ egl_set2$  

56 D5 1139 2436 TSTL r6  

16 12 113B 2437 BNEQ egl_set4$  

64 01 D0 113D 2438 MOVL #1,(r4)  

1C 11 1140 2439 BRB eql_set_ret$  

1142 2440 eql_set2$:  

56 D5 1142 2441 TSTL r6  

E6 12 1144 2442 BNEQ egl_set1$  

1146 2443 eql_set3$:  

82 00 91 1146 2444 CMPB #^X00,(r2)+  

13 12 1149 2445 BNEQ egl_set_ret$  

F8 55 F5 114B 2446 SOBGTR r5,eql_set3$  

64 01 D0 114E 2447 MOVL #1,(r4)  

OB 11 1151 2448 BRB eql_set_ret$  

1153 2449 eql_set4$:  

00 83 91 1153 2450 CMPB (r3)+,#^X00  

06 12 1156 2451 BNEQ egl_set_ret$  

F8 56 F5 1158 2452 SOBGTR r6,eql_set4$  

64 01 D0 115B 2453 MOVL #1,(r4)  

115E 2454 eql_set_ret$:  

04 115E 2455 RET  

115F 2456  

115F 2457  

115F 2458 ; Set B is a subset of Set A  

115F 2459:  

115F 2460 geq_set_set:  

64 D4 115F 2461 CLRL (r4)  

55 D4 1161 2462 CLRL r5  

56 D4 1163 2463 CLRL r6  

56 00000030'FF B0 1165 2464 MOVW aarg1_desc,r6  

55 00000038'FF B0 116C 2465 MOVW aarg2_desc,r5  

50 52 D0 1173 2466 MOVL r2,r0  

52 53 D0 1176 2467 MOVL r3,r2  

53 50 D0 1179 2468 MOVL r0,r3  

74 11 117C 2469 BRB leq_set1$  

117E 2470  

117E 2471  

117E 2472 : IN, C is an element of Set B  

117E 2473:  

64 63 01 62 EF 117E 2474 in_set_set:  

03 03 13 1183 2475 EXTZV (r2),#1,(r3),(r4)  

64 01 D0 1185 2476 BEQL in_set$  

04 1188 2477 MOVL #1,(r4)  

1188 2478 in_set$:  

1188 2479 RET  

1189 2480  

1189 2481  

1189 2482 ; Intersection of Two Sets

```

dbg\$perform_operator

```

      1189  2483 ; intersect_set_set:
      1189  2484 ; intersect_set1$:
      55   D4    1189  2485 CRL r5
      56   D4    118B  2486 CLRL r6
      55   00000030'FF B0    118D  2487 MOVW @arg1_desc,r5
      56   00000038'FF B0    1194  2488 MOVW @arg2_desc,r6
      50   54    B0    119B  2489 MOVW @arg1_desc,@result_desc
      50   54    D0    11A6  2490 MOVL r4,r0

      80   82    51    83    92    11A9  2491 intersect_set2$:
      80   82    51    8B    11AC  2492 MCOMB (r3)+,r1
      80   82    51    8B    11AC  2493 BICB3 r1,(r2)+,(r0)+

      55   D7    11B0  2494 DECL r5
      56   D7    11B2  2495 DECL r6
      55   D5    11B4  2496 TSTL r5
      06   12    11B6  2497 BNEQ intersect_set3$
      56   D5    11B8  2498 TSTL r6
      0F   12    11BA  2499 BNEQ intersect_set4$
      1F   11    11BC  2500 BRB intersect_set_ret$

      56   D5    11BE  2501 intersect_set3$:
      56   D5    11BE  2502 TSTL r6
      E7   12    11C0  2503 BNEQ intersect_set1$

      80   82    F9    00    8B    11C2  2504 intersect_set4$:
      80   82    F9    55    F5    11C6  2505 BICB3 #^X00,(r2)+,(r0)+

      12    11    11C9  2506 SOBGTR r5,intersect_set3$
      12    11    11C9  2507 BRB intersect_set_ret$

      80   00    83    8B    11CB  2508 intersect_set1$:
      80   00    83    8B    11CB  2509 BICB3 (r3)+,#^X00,(r0)+

      00000040'FF 00000038'FF B0    11D2  2510 SOBGTR r6,intersect_set4$
      04    04    11DD  2511 MOVW @arg2_desc,@result_desc

      11DE  2512 intersect_set_ret$:
      11DE  2513 RET

      11DE  2514
      11DE  2515
      11DE  2516 : Set A is a subset of Set B
      11DE  2517
      11DE  2518 leq_set_set:
      64    D4    11DE  2519 CLRL (r4)
      55    D4    11E0  2520 CLRL r5
      56    D4    11E2  2521 CLRL r6
      55    00000030'FF B0    11E4  2522 MOVW @arg1_desc,r5
      56    00000038'FF B0    11EB  2523 MOVW @arg2_desc,r6

      50   82    83    8B    11F2  2524 leq_set1$:
      50   82    83    8B    11F2  2525 BICB3 (r3)+,(r2)+,r0
      50   95    11F6  2526 TSTB r0
      31   12    11F8  2527 BNEQ leq_set_ret$
      55   D7    11FA  2528 DECL r5
      56   D7    11FC  2529 DECL r6
      55   D5    11FE  2530 TSTL r5
      09   12    1200  2531 BNEQ leq_set2$
      56   D5    1202  2532 TSTL r6
      1A   12    1204  2533 BNEQ leq_set4$
      64   01    D0    1206  2534 MOVL #1,r4
      20   11    1209  2535 BRB leq_set_ret$

      56   D5    120B  2536 leq_set2$:
      56   D5    120B  2537 TSTL r6
      E3   12    120D  2538 BNEQ leq_set1$


      120F  2539 leq_set3$:

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dbg\$perform_operator

```

50  82  FF 8F   8B  120F  2540      BICB3  #^XFF,(r2)+,r0
      50  95 1214  2541      TSTB   r0
      13  12 1216  2542      BNEQ   leq_set_ret$
      F4  55  F5 1218  2543      SOBGTR r5,leq_set3$
      64  01  D0 121B  2544      MOVL   #1,(r4)
      0B  11 121E  2545      BRB    leq_set_ret$

      50  FF 8F 83   8B  1220  2546      leq_set4$:
      F8  56  F5 1225  2547      BICB3  (r3)+,#^XFF,r0
      64  01  D0 1228  2548      SOBGTR r6,leq_set4$
      04  122B 2550      MOVL   #1,(r4)
      122B 2551      RET

      122C 2552
      122C 2553
      122C 2554      : Set Not Equal
      122C 2555      :
      122C 2556      neq_set_set:
      64  D4 122C 2557      CLRL   (r4)
      55  D4 122E 2558      CLRL   r5
      56  D4 1230  2559      CLRL   r6
      55  00000030'FF  B0 1232  2560      MOVW   @arg1_desc,r5
      56  00000038'FF  B0 1239  2561      MOVW   @arg2_desc,r6
      50  D4 1240  2562      CLRL   r0
      51  D4 1242  2563      CLRL   r1
      50  55  D0 1244  2564      MOVL   r5,r0
      56  55  D1 1247  2565      CMPL   r5,r6
      03  18 124A  2566      BGEQ   neq_set1$
      50  56  D0 124C  2567      MOVL   r6,r0
      82  83  91 124F  2568      neq_set1$:
      02  12 1252  2569      CMPB   (r3)+(r2)+neq_set1_1$
      51  D6 1254  2570      BNEQ   neq_set1_1$      INCL   r1
      55  D7 1256  2571      neq_set1_1$:
      56  D7 1258  2572      DECL   r5
      55  D5 125A  2573      DECL   r6
      06  12 125C  2574      TSTL   r5
      56  D5 125E  2575      TSTL   r6
      12  12 1260  2576      BNEQ   neq_set2$
      1A  11 1262  2577      TSTL   r6
      1262 2578      BNEQ   neq_set4$
      1262 2579      BRB    neq_set$
      1264 2580      neq_set2$:
      56  D5 1264  2581      TSTL   r6
      E7  12 1266  2582      BNEQ   neq_set1$      INCL   r1
      82  00  91 1268  2583      neq_set3$:
      02  12 126B  2584      CMPB   #^X00,(r2)+neq_set3_1$
      51  D6 126D  2585      BNEQ   neq_set3_1$      INCL   r1
      126D 2586      neq_set3_1$:
      F6  55  F5 126F  2587      TSTL   r6
      0A  11 1272  2588      SOBGTR r5,neq_set3$
      1272 2589      BRB    neq_set$
      00  83  91 1274  2590      neq_set4$:
      02  12 1277  2591      CMPB   (r3)+,#^X00neq_set4_1$
      51  D6 1279  2592      BNEQ   neq_set4_1$      INCL   r1
      1279 2593      neq_set4_1$:
      F6  56  F5 127B  2594      CMPB   (r3)+,#^X00neq_set4_1$      INCL   r1
      127B 2595      SOBGTR r6,neq_set4$      INCL   r1
      127E 2596      neq_set$:
  
```

dbg\$perform_operator

```

51 50 D1 127E 2597 CMPL r0,r1
      03 13 1281 2598 BEQL neq_set_ret$#
64 01 D0 1283 2599 MOVL #1,(r4)
      04 1286 2600 neq_set_ret$:
      1286 2601 RET
      1287 2602
      1287 2603
      1287 2604 : Union or Two Sets
      1287 2605 :
      1287 2606 union_set_set:
      55 D4 1287 2607 CRL r5
      56 D4 1289 2608 CLRL r6
00000040'FF 00000030'FF B0 128B 2609 MOVW @arg1_desc,r5
      56 00000038'FF B0 1292 2610 MOVW @arg2_desc,r6
      50 00000030'FF B0 1299 2611 MOVW @arg1_desc,@result_desc
      54 D0 12A4 2612 MOVL r4,r0
      12A7 2613 union_set1$:
      80 82 83 12A7 2614 BISB3 (r3)+,(r2)+,(r0)+
      55 D7 12AB 2615 DECL r5
      56 D7 12AD 2616 DECL r6
      55 D5 12AF 2617 TSTL r5
      06 12 12B1 2618 BNEQ union_set2$#
      56 D5 12B3 2619 TSTL r6
      0E 12 12B5 2620 BNEQ union_set4$#
      1D 11 12B7 2621 BRB union_set_ret$#
      12B9 2622 union_set2$:
      56 D5 12B9 2623 TSTL r6
      EA 12 12BB 2624 BNEQ union_set1$#
      12BD 2625 union_set3$:
      80 82 90 12BD 2626 MOVB (r2)+,(r0)+
      FA 55 F5 12C0 2627 SOBGTR r5,union_set3$#
      11 11 12C3 2628 BRB union_set_ret$#
      12C5 2629 union_set4$:
      80 83 90 12C5 2630 MOVB (r3)+,(r0)+
      FA 56 F5 12C8 2631 SOBGTR r6,union_set4$#
      00000040'FF 00000038'FF B0 12CB 2632 MOVW @arg2_desc,@result_desc
      12D6 2633 union_set_ret$:
      04 12D6 2634 RET
      12D7 2635
      12D7 2636 : C address-of operator.
      12D7 2637 : We pass in the entire value descriptor to the C_ADDRESS_OF routine,
      12D7 2638 : because it will need to look at the typeid. We also pass in a
      12D7 2639 : pointer to the result value descriptor. This routine will fill
      12D7 2640 : in the result value descriptor.
      12D7 2641 :
      12D7 2642 address_l:
      00000044'EF DD 12D7 2643 PUSHL result_valdesc
      00000034'EF DD 12DD 2644 PUSHL arg1_valdesc
00000000'EF 02 FB 12E3 2645 CALLS #2,dbg$c_address_of
      04 12EA 2646 RET
      12EB 2647
      12EB 2648
      12EB 2649 : C SIZEOF operator
      12EB 2650 : Pass in the entire value descriptor to the C_SIZEOF routine. (It will
      12EB 2651 : have to look at the typeid.) This routine will return the size in R0.
      12EB 2652 :
      12EB 2653 sizeof_l:

```

dbg\$perform_operator

```

00000034'EF    DD 12EB 2654      PUSHL  arg1_valdesc
00000000'EF 01  FB 12F1 2655      CALLS  #1,dbg$c_sizeof
64   50  D0 12F8 2656      MOVL   r0,(r4)
          04 12FB 2657      RET

          12FC 2658
          12FC 2659 : Addition of typed pointer and integer in C.
          12FC 2660 :
          12FC 2661 add_tptr_l:
00000044'EF    DD 12FC 2662      PUSHL  result_valdesc
0000003C'EF    DD 1302 2663      PUSHL  arg2_valdesc
00000034'EF    DD 1308 2664      PUSHL  arg1_valdesc
00000000'EF 03  FB 130E 2665      CALLS  #3,dbg$c_add_tptr_l
          04 1315 2666      RET

          1316 2667
          1316 2668 : Subtraction of typed pointer and integer in C.
          1316 2669 :
          1316 2670 sub_tptr_l:
00000044'EF    DD 1316 2671      PUSHL  result_valdesc
0000003C'EF    DD 131C 2672      PUSHL  arg2_valdesc
00000034'EF    DD 1322 2673      PUSHL  arg1_valdesc
00000000'EF 03  FB 1328 2674      CALLS  #3,dbg$c_sub_tptr_l
          04 132F 2675      RET

          1330 2676
          1330 2677 : Subtraction of two typed pointers in C.
          1330 2678 :
          1330 2679 sub_tptr_tptr:
00000044'EF    DD 1330 2680      PUSHL  result_valdesc
0000003C'EF    DD 1336 2681      PUSHL  arg2_valdesc
00000034'EF    DD 133C 2682      PUSHL  arg1_valdesc
00000000'EF 03  FB 1342 2683      CALLS  #3,dbg$c_sub_tptr_tptr
          04 1349 2684      RET

          134A 2685
          134A 2686 : increment and decrement in C (++X X++ --X X--)
          134A 2687 :
          134A 2688 pre_incr_l:
          134A 2689 pre_incr_lu:
00028723 8F    DD 134A 2690      PUSHL  #dbg$cpreincr
00000000'GF 01  FB 1350 2691      CALLS  #1,G^lib$signal
64   62  D0 1357 2692      MOVL   (r2),(r4)
64   64  D6 135A 2693      INCL   (r4)
          04 135C 2694      RE1

          135D 2695
          135D 2696 pre_incr_d:
00028723 8F    DD 135D 2697      PUSHL  #dbg$cpreincr
00000000'GF 01  FB 1363 2698      CALLS  #1,G^lib$signal
64   62  70 136A 2699      MOVD   (r2),(r4)
64   08  60 136D 2700      ADDD2  #1.,(r4)
          04 1370 2701      RET

          1371 2702
          1371 2703 pre_incr_tptr:
00028723 8F    DD 1371 2704      PUSHL  #dbg$cpreincr
00000000'GF 01  FB 1377 2705      CALLS  #1,G^lib$signal
00000034'EF    DD 137E 2706      PUSHL  arg1_valdesc
00000000'EF 01  FB 1384 2707      CALLS  #1,dbg$c_pre_incr_tptr
64   50  D0 138B 2708      MOVL   r0,(r4)
          04 138E 2709      RET
          138F 2710

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dbg\$perform_operator

		138F	2711	post_incr_l:	
		138F	2712	post_incr_lu:	
		138F	2713	post_incr_tptr:	
0002872B	8F	DD	138F	PUSHL #dbg\$cpostincr	
00000000	'GF	01	FB	1395	CALLS #1,G^lib\$signal
64	62	DO	139C	MOVL (r2),(r4)	
	04		139F	RET	
			13A0	2718	
0002872B	8F	DD	13A0	2719 post_incr_d:	
00000000	'GF	01	FB	13A6	PUSHL #dbg\$cpostincr
64	62	70	13AD	CALLS #1,G^lib\$signal	
	04		13B0	MOVD (r2),(r4)	
			13B1	2723 RET	
			13B1	2724	
00028733	8F	DD	13B1	2725 pre_decr_l:	
00000000	'GF	01	FB	13B7	pre_decr_lu:
64	62	DO	13BE	PUSHL #dbg\$cpredecr	
	64	D7	13C1	CALLS #1,G^lib\$signal	
	04		13C3	MOVL (r2),(r4)	
			13C4	2729 DECL (r4)	
00028733	8F	DD	13C4	2731 RET	
00000000	'GF	01	FB	13CA	2732
64	62	70	13D1	2733 pre_decr_d:	
	64	08	62	13D4	PUSHL #dbg\$cpredecr
	04		13D7	CALLS #1,G^lib\$signal	
			13D8	MOVD (r2),(r4)	
			13D8	2737 SUBD2 #1.,(r4)	
			13D8	2738 RET	
00028733	8F	DD	13D8	2739 pre_decr_tptr:	
00000000	'GF	01	FB	13DE	PUSHL #dbg\$cpredecr
00000034	'EF	DD	13E5	CALLS #1,G^lib\$signal	
00000000	'EF	01	FB	13EB	PUSHL arg1_valdesc
64	50	DO	13F2	CALLS #1,dBgs\$pre_decr_tptr	
	04		13F5	MOVL r0,(r4)	
			13F6	2746 RET	
			13F6	2747	
0002873B	8F	DD	13F6	2748 post_decr_l:	
00000000	'GF	01	FB	13FC	post_decr_lu:
64	62	DO	1403	2750 post_decr_tptr:	
	04		1406	PUSHL #dbg\$cpostdecr	
			1407	CALLS #1,G^lib\$signal	
			1407	MOVL (r2),(r4)	
0002873B	8F	DD	1407	2755 RET	
00000000	'GF	01	FB	140D	2756 post_decr_d:
64	62	70	1414	PUSHL #dbg\$cpostdecr	
	04		1417	CALLS #1,G^lib\$signal	
			1418	MOVD (r2),(r4)	
			1418	2760 RET	
			1418	2761	
			1418	2762 :*****	
			1418	2763 :	
			1418	2764 P A C K E D D E C I M A L	
			1418	2765 :	
			1418	2766 :*****	
			1418	2767	

dbg\$perform_operator

```

      1418 2768
      1418 2769 ; Subtraction
      1418 2770
      1418 2771 sub_p_p:
56 00000030'EF  DO 1418 2772      MOVL arg1_desc, r6          ; Get left desc.
57 00000038'EF  DO 141F 2773      MOVL arg2_desc, r7          ; Get right desc.
58 00000040'EF  DO 1426 2774      MOVL result_desc, r8        ; Get result desc.
      50 67 3C 142D 2775      MOVZWL dsc$w_length(r7), r0
      50 FF 8F 1430 2776      ASHL #1, r0, r0
04 B740 01 8C 1435 2777      XORB2 #1, @dsc$a_pointer(r7)[r0]
      15 11 143A 2778      BRB addp$
      143C 2779
      143C 2780 ; Addition.
      143C 2781
      143C 2782 add_p_p:
56 00000030'EF  DO 143C 2783      MOVL arg1_desc, r6          ; Get left desc.
57 00000038'EF  DO 1443 2784      MOVL arg2_desc, r7          ; Get right desc.
58 00000040'EF  DO 144A 2785      MOVL result_desc, r8        ; Get result desc.
      5E B8 AE 9E 1451 2786 addp$: MOVAB -72(sp), sp           ; Workspace.
      56 DD 1455 2787      PUSHL r6
00001B58'EF 01 FB 1457 2788      CALLS #1, dbg$strip_zeroes   ; Strip leading/trailing
      57 DD 145E 2789      PUSHL r7
      00001B58'EF 01 FB 1460 2790      CALLS #1, dbg$strip_zeroes   ; zeroes.
      55 08 A6 08 A7 83 1467 2791      SUBB3 dsc$b_scale(r7), dsc$b_scale(r6), r5
      0C 18 146D 2792      BGEQ 1$           ; Get change of scale.
      55 55 8E 146F 2793      MNEG B r5, r5
      57 56 CC 1472 2794      XORL2 r6, r7
      56 57 CC 1475 2795      XORL2 r7, r6
      57 56 CC 1478 2796      XORL2 r6, r7
      50 66 55 81 147B 2797 1$: ADDB3 r5, dsc$w_length(r6), r0
      51 1E 50 83 147F 2798      SUBB3 r0, #30, r1           ; Is length in range?
      14 18 1483 2799      BGEQ 2$           ; Too long.
      55 51 80 1485 2800      ADDB2 r1, r5
      08 A7 51 82 1488 2801      SUBB2 r1, dsc$b_scale(r7)    ; Adjust scale.
      04 B7 67 51 F8 148C 2802      ASHP r1, dsc$w_length(r7), @dsc$a_pointer(r7), #0, dsc$w_length(r7), (sp)
      04 B7 6E 67 34 1494 2803      MOVP dsc$w_length(r7), (sp), @dsc$a_pointer(r7)
      6E 67 00 04 B7 67 51 F8 1499 2804 2$: ASHP r5, dsc$w_length(r6), @dsc$a_pointer(r6), #0, #31, (sp)
      6E 1F 00 04 B6 66 55 F8 14A1 2805      ADDP6 dsc$w_length(r7), @dsc$a_pointer(r7), -
      68 6E 1F 04 B7 67 21 14A1 2805      04 BB 14A8
      08 A8 08 A7 90 14AA 2806      #31, (sp), dsc$w_length(r8), @dsc$a_pointer(r8)
      09 A8 1F 90 14AA 2807      MOVB dsc$b_scale(r7), dsc$b_scale(r8)   ; Copy scale.
      04 14AF 2808      MOVB #31, dsc$b_digits(r8)
      14B3 2809      RET
      14B4 2810
      14B4 2811 ; Multiplication.
      14B4 2812 ;
      14B4 2813 mul_p_p:
56 00000030'EF  C2 14B4 2814      SUBL #16, sp             ; Work space
57 00000038'EF  DO 14B7 2815      MOVL arg1_desc, r6          ; Get descri
58 00000040'EF  DO 14BE 2816      MOVL arg2_desc, r7          ; Get descri
      56 DD 14CC 2817      MOVL result_desc, r8        ; Strip zero
00001B58'EF 01 FB 14CE 2818      PUSHL r6
      57 DD 14D5 2819      CALLS #1, dbg$strip_zeroes   ; length.
      01 FB 14D7 2820      PUSHL r7
      00001B58'EF 01 FB 14DE 2821      CALLS #1, dbg$strip_zeroes
      59 D4 14E0 2822      CLRL r9
      5A D4 14E0 2823      CLRL r10

```

DBGPERMOP
V04-000

dbg\$perform_operator

F 16

15-SEP-1984 23:45:18 VAX/VMS Macro V04-00
4-SEP-1984 23:56:47 [DEBUG.SRC]DBGPERMOP.MAR;1

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59	67	66	A1	14E2	2824	ADDW3	dsc\$w_length(r6), dsc\$w_length(r7), r9												Estimate l	
	59	1F	A2	14E6	2825	SUBW2	#31, r9												Will produ	
5A	66	67	A3	14EB	2827	BLEQ	mul_ps											No.		
	OC	18	14EF	2828	SUBW3	dsc\$w_length(r7), dsc\$w_length(r6), r10											Yes. Will			
	5A	5A	AE	14F1	2829	BGEQ	1\$											Want longe		
	51	56	D0	14F4	2830	MNEGW	r10, r10											Switch ope		
	56	57	D0	14F7	2831	MOVL	r6, r1													
	57	51	D0	14FA	2832	MOVL	r7, r6													
	5A	59	B1	14FD	2833	MOVL	r1, r7													
		27	15	1500	2834	CMPW	r9, r10											Algorithm		
	59	5A	A2	1502	2835	BLEQ	5\$										(1) r9			
		59	B6	1505	2836	SUBW2	r10, r9										(2) r10			
	59	59	FF	8F	2837	INCW	r9										If r9 <=			
		5B	67	32	2838	ASHL	#-1, r9, r9										(1)			
		67	59	A2	2839	CVTWL	dsc\$w_length(r7), r11										(2)			
	08	A7	59	80	2840	SUBW2	r9, dsc\$w_length(r7)										(3)			
		52	59	AE	2841	ADDB2	r9, dsc\$b_scale(r7)										If r9 >			
	6E	67	00	04 B7	2842	MNEGW	r9, r2										(1)			
		04 B7	5B	52	F8	ASHP	r2, r11, @dsc\$a_pointer(r7), #0, dsc\$w_length(r7), (sp)									(2)				
		6E	67	34	2843	MOVP	dsc\$w_length(r7), (sp), @dsc\$a_pointer(r7)									(3)				
		59	5A	A0	2844	ADDW2	r10, r9									(4)				
		5B	66	32	2845	CVTWL	dsc\$w_length(r6), r11									(5)				
		66	59	A2	2846	SUBW2	r9, dsc\$w_length(r6)													
	08	A6	59	80	2847	ADDB2	r9, dsc\$b_scale(r6)													
		59	59	AE	2848	MNEGW	r9, r9													
	6E	66	00	04 B6	2849	ASHP	r9, r11, @dsc\$a_pointer(r6), #0, dsc\$w_length(r6), (sp)													
		04 B6	5B	59	F8	MOVP	dsc\$w_length(r6), (sp), @dsc\$a_pointer(r6)													
			6E	66	34	2850	mul_ps:													
						1543	2851	ADDB3	dsc\$b_scale(r6), dsc\$b_scale(r7), dsc\$b_scale(r8)								Get final			
		08 A8	08 A7	08 A6	81	1543	2852	MOVB	#31, dsc\$b_digits(r8)								Number of			
		09 A8	1F	90	154A	2853	CVTBW	dsc\$b_digits(r8), dsc\$w_length(r8)								Fill in nu				
	1F	04 B7	67	04 B6	66	25	1552	MULP	dsc\$w_length(r6), @dsc\$a_pointer(r6), -							Multiply a				
				04 B8		155A	2855													
						155C	2856		dsc\$w_length(r7), @dsc\$a_pointer(r7), -											
						155C	2857		#31, @dsc\$a_pointer(r8)											
						04	155C	2858	RET											
							155D	2859												
							155D	2860	: Division.											
							155D	2861												
							155D	2862	div_p-p:											
									SUBL	#16, sp							Workspace.			
	56	00000030'EF	5E	10	C2	155D	2863	MOVL	arg1_desc, r6								Get descri			
	57	00000038'EF	DD	1560	2864	MOVL	#31, arg2_desc, r7									zeroes				
	58	00000040'EF	DD	1567	2865	MOVL	result_desc, r8													
						DD	1575	PUSHL	r6											
		00001B58'EF	01	FB	1577	2866	CALLS	#1, dbg\$strip_zeroes												
						57	157E	PUSHL	r7											
		00001B58'EF	01	FB	1580	2867	CALLS	#1, dbg\$strip_zeroes												
			5A	1F	66	A3	1587	SUBW3	dsc\$w_length(r6), #31, r10											
			08 A6	5A	82	158B	2871	SUBB2	r10, dsc\$b_scale(r6)											
			04 B6	6E	1F	34	1597	ASHP	r10, dsc\$w_length(r6), @dsc\$a_pointer(r6), #0, #31, (sp)							Dividend m				
							159C	2874	MOVP	#31, (sp), @dsc\$a_pointer(r6)						Adjust				
							159F	2875	MOVW	#31, dsc\$w_length(r6)						Shift t				
							15A2	2876	MOVW	#31, dsc\$w_length(r8)										
	08 A8	08 A6	08 A7	83	15A6	2877	CVTWB	dsc\$w_length(r8), dsc\$b_scale(r8)												
						7E	67	SUBB3	dsc\$b_scale(r7), dsc\$b_scale(r6), dsc\$b_scale(r8)											
						3C	15AD	MOVZWL	dsc\$w_length(r7), -(sp)											

dbg\$perform_operator

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    00  DD 15B0 2880  PUSHL #0
    68  3C 15B2 2881  MOVZWL dsc$w_length(r8), -(sp)
    04  AB 15B5 2882  PUSHL dsc$a_pointer(r8)
    67  3C 15B8 2883  MOVZWL dsc$w_length(r7), -(sp)
    A7  DD 15BB 2884  PUSHL dsc$a_pointer(r7)
    A6  DD 15BE 2885  PUSHL dsc$a_pointer(r6)
00000000'GF  07  FB 15C1 2886  CALLS #7, G*PLI$DIV_PK_LONG
                04 15C8 2887  RET
                15C9 2888
                15C9 2889
                15C9 2890 ; Unary minus.
                15C9 2891 ;
                15C9 2892 unary_minus_p:
56  00000030'EF  D0 15C9 2893  MOVL arg1_desc, r6
58  00000040'EF  D0 15D0 2894  MOVL result_desc, r8
                50  66 3C 15D7 2895  MOVZWL dsc$w_length(r6), r0
                50  FF 8F 78 15DA 2896  ASHL #1, r0, r0
04 B640  01 8C 15DF 2897  XORB2 #1, @dsc$a_pointer(r6)[r0]
                OE 11 15E4 2898  BRB unary_ps
                15E6 2899
                15E6 2900 ; Unary plus.
                15E6 2901 ;
                15E6 2902 unary_plus_p:
56  00000030'EF  D0 15E6 2903  MOVL arg1_desc, r6
58  00000040'EF  D0 15ED 2904  MOVL result_desc, r8
                15F4 2905 unary_ps:
00001B58'EF  56  DD 15F4 2906  PUSHL r6
                01  FB 15F6 2907  CALLS #1, dbg$strip_zeroes
04 B8  04 B6 66 34 15FD 2908  MOVP dsc$w_length(r6), @dsc$a_pointer(r6), @dsc$a_pointer(r8); Move to re
                68  66 B0 1603 2909  MOVW dsc$w_length(r6), dsc$w_length(r8); Adjust len
                08 A8  08 A6 90 1606 2910  MOVB dsc$b_scale(r6), dsc$b_scale(r8)
                09 A8  68 33 160B 2911  CVTWB dsc$w_length(r8), dsc$b_digits(r8)
                04 160F 2912  RET
                1610 2913
                1610 2914 : EQL, NEQ, GTR, GEQ, LSS, and LEQ.
                1610 2915 :
                1610 2916 eql_p_p:
56  00000030'EF  D0 1610 2917  MOVL arg1_desc, r6
57  00000038'EF  D0 1617 2918  MOVL arg2_desc, r7
                56  DD 161E 2919  PUSHL r6
00001B58'EF  01  FB 1620 2920  CALLS #1, dbg$strip_zeroes
                57  DD 1627 2921  PUSHL r7
00001B58'EF  01  FB 1629 2922  CALLS #1, dbg$strip_zeroes
                64  D4 1630 2923  CLRL (r4)
04 B7  67  04 B6 66 37 1632 2924  CMP4 dsc$w_length(r6), @dsc$a_pointer(r6), -
                1639 2925  BNEQ dsc$w_length(r7), @dsc$a_pointer(r7); Do the com
                0A  12 1639 2926  eql_p5
                08 A7  08 A6 91 163B 2927  CMPB dsc$b_scale(r6), dsc$b_scale(r7); be sure
                03  12 1640 2928  BNEQ eql_p5
                64  01  D0 1642 2929  MOVL #1, -(r4)
                ECBD 31 1645 2930  eql_ps:
                1648 2931  BRW branch_ret
                1648 2932
                1648 2933 neq_p_p:
56  00000030'EF  D0 1648 2934  MOVL arg1_desc, r6
57  00000038'EF  D0 164F 2935  MOVL arg2_desc, r7
                56  DD 1656 2936  PUSHL r6
                1648 2937
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dbg\$perform_operator								
04 B7	67 04 B6	01 57 01 64 09 02 64 EC85	FB DD 01 00 12 1672 167D 31	1658 1661 1668 166B 1672 1674 1679 167B 167D	2937 2938 2939 2940 2941 2943 2945 2946 2947	CALLS PUSHL CALLS MOVL CMPP4 BNEQ CMPB BNEQ CLRL neq_ps: BRW gtr_p_p: BSBW MOVL CMPP4 BGTR CLRL neq_ps: BRW geq_p_p: BSBW MOVL CMPP4 BGEQ CLRL geq_ps: BRW lss_p_p: BSBW MOVL CMPP4 BLSS CLRL lss_ps: BRW leq_p_p: BSBW MOVL CMPP4 BLEQ CLRL leq_ps: BRW setup_packed_numbers\$: CLRL	#1, dbg\$strip_zeroes r7 #1, dbg\$strip_zeroes #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) neq_ps dsc\$b_scale(r6), dsc\$b_scale(r7) neq_ps (r4) branch_ret setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) gtr_ps (r4) branch_ret setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) geq_ps (r4) branch_ret setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) lss_ps (r4) branch_ret setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) lss_ps (r4) branch_ret setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) leq_ps (r4) branch_ret setup_packed_numbers\$: CLRL r8 CLRL r9 MOVL arg1_desc, r6	; zeroes. ; Same again ; Assume NEQ ; Do the com sure to ; Failure. ; Assume GTR ; Scales wer ; Failure. ; Assume GEQ ; Scales wer ; Failure. ; Scales wer ; Failure. ; Assume LEQ ; Scales wer ; Failure. ; Use as a adjustment scale ; Use as a adjustment digits ; Get descriptors
04 B7	67 04 B6	004D 64 01 66 37 02 64 EC71	00 14 D4	1680 1683 1686 168D 168F 1691	2950 2951 2952 2953 2954 2957	BSBW MOVL CMPP4 BGTR CLRL neq_ps: BRW	setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) gtr_ps (r4) branch_ret	
04 B7	67 04 B6	0039 64 01 66 37 02 64 EC5D	30 18 D4	1694 1697 169A 16A1 16A1 16A5	2960 2961 2962 2963 2964 2967	BSBW MOVL CMPP4 BGEQ CLRL geq_ps: BRW	setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) geq_ps (r4) branch_ret	
04 B7	67 04 B6	0025 64 01 66 37 02 64 EC49	30 19 D4	16A8 16AB 16AE 16B5 16B5 16B9	2970 2971 2972 2973 2974 2977	BSBW MOVL CMPP4 BLSS CLRL lss_ps: BRW	setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) lss_ps (r4) branch_ret	
04 B7	67 04 B6	0011 64 01 66 37 02 64 EC35	30 15 D4	16BC 16BF 16C2 16C9 16C9 16CD	2980 2981 2982 2983 2984 2987	BSBW MOVL CMPP4 BLEQ CLRL leq_ps: BRW	setup_packed_numbers\$ #1, (r4) dsc\$w_length(r6), adsc\$a_pointer(r6), - dsc\$w_length(r7), adsc\$a_pointer(r7) leq_ps (r4) branch_ret	
56	00000030'EF	58 59 D4 D4	16D0 16D0 16D2 16D4	2990 2991 2992 2993	2990	setup_packed_numbers\$: CLRL CLRL MOVL	setup_packed_numbers\$: CLRL r8 CLRL r9 MOVL arg1_desc, r6	

dbg\$perform_operator

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57 00000038'EF DO 16DB 2994      MOVL arg2_desc, r7
                  DD 16E2 2995      PUSHL r6
00001B58'EF 01 FB 16E4 2996      CALLS #1, dbg$strip_zeroes ; Strip leading/trailing
57 DD 16EB 2997      PUSHL r7
00001B58'EF 01 FB 16ED 2998      CALLS #1, dbg$strip_zeroes ; zeroes
58 08 A7 08 A6 83 16F4 2999      SUBB3 dsc$b_scale(r6),dsc$b_scale(r7),r8; Same again
16FA 3000
58 95 16FA 3001      TSTB r8
76 13 16FC 3002      BEQL setup_packed_rsb$ ; They are, simply return
05 14 16FE 3003      BGTR scale_arg2$ ; Adjust the second operand
58 58 8E 1700 3005      MNGB r8, r8
0E 11 1703 3006      BRB scale_arg1$ ; (first has larger scaling)
1705 3007
56 00000038'EF DO 1705 3008      scale_arg2$: MOVL arg2_desc, r6 ; Adjust the first operand
170C 3009
170C 3010
1713 3011      MOVL arg1_desc, r7 ; (second has larger scaling)
1713 3012
1713 3013      scale_arg1$: ADDB3 dsc$b_digits(r6), r8, r9 ; Use r6 to point to the
1713 3014          CMPB r9, #31 operand needs adjustment
1718 3015          BGTR truncate_the_other$ ; (the one has smaller scaling)
1718 3016
171B 3017
25 14 171B 3018      BRB r7 points to the operand
171D 3019
171D 3020
171D 3021
171D 3022
59 00 04 B6 66 58 F8 171D 3023      ASHP r8, dsc$w_length(r6), @dsc$a_pointer(r6), -
00000048'EF 1724
00 00000048'EF 59 00 F8 1729 3024      ASHP #0, r9, operand
04 B6 59 00 F8 1729 3025      ASHP #0, r9, operand, #0, r9, @dsc$a_pointer(r6)
66 59 B0 1735 3026      MOVW r9, dsc$w_length(r6)
09 A6 59 90 1738 3027      MOVB r9, dsc$b_digits(r6)
08 A6 58 82 173C 3028      SUBB2 r8, dsc$b_scale(r6)
32 11 1740 3029      BRB setup_packed_rsb$ ; If we try to adjust the
5A 58 97 1742 3030      DECB r8 smaller scale will cause
67 3C 1744 3031      MOVZWL dsc$w_length(r7), r10 overflow, so we truncate the
5A B7 1747 3032      DECW r10 other scale instead
5A B7 1749 3033      ASHP #-1, dsc$w_length(r7), @dsc$a_pointer(r7), -
00000048'EF 1751
5A 00 04 B7 67 FF 8F F8 1756 3035      ASHP #0, r10, operand
04 B7 5A 00 F8 1756 3036      ASHP #0, r10, operand, #0, r10, @dsc$a_pointer(r7)
5A 5A 175F
08 A7 97 1762 3037      DECB dsc$b_scale(r7)
5A B5 1765 3038      TSTW r10 ; If we got done to zero
1767 3039
0B 13 1767 3040      BEQL setup_packed_rsb$ ; digit, then we are all done
67 5A B0 1769 3041      MOVW r10, dsc$w_length(r7)
09 A7 5A 90 176C 3042      MOVB r10, dsc$b_digits(r7)
58 95 1770 3043      TSTB r8
9F 12 1772 3044      BNEQ scale_arg1$ ; setup_packed_rsb$:
56 00000030'EF DO 1774 3045      MOVL arg1_desc, r6

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57 00000038'EF D0 1778 3047 MOVL arg2_desc, r7
 05 1782 3048 RSB
 1783 3049
 1783 3050
 1783 3051 ; PLI bit-string operations.
 1783 3052 ;
 1783 3053 concat_tf_tf:
 0179 30 1783 3054 BSBW setup_pli_interface\$
 51 54 D0 1786 3055 MOVL r4, r7
 0000000C'EF DF 1789 3056 PUSHAL dope2
 53 DD 178F 3057 PUSHL r3
 00000008'EF DF 1791 3058 PUSHAL dope1
 52 DD 1797 3059 PUSHL r2
 00000000'GF 04 FB 1799 3060 CALLS #4, G^PLI\$CATBIT
 04 17A0 3061 RET
 17A1 3062
 17A1 3063 eql_tf_tf:
 015B 30 17A1 3064 BSBW setup_pli_interface\$
 64 01 D0 17A4 3065 MOVL #1, (r4)
 0000000C'EF DF 17A7 3066 PUSHAL dope2
 53 DD 17AD 3067 PUSHL r3
 00000008'EF DF 17AF 3068 PUSHAL dope1
 52 DD 17B5 3069 PUSHL r2
 00000000'GF 04 FB 17B7 3070 CALLS #4, G^PLI\$CMPBIT
 50 D5 17BE 3071 TSTL r0
 02 13 17C0 3072 BEQL eql_tf\$
 64 D4 17C2 3073 CLRL (r4)
 EB3E 31 17C4 3074 eql_tf\$:
 17C4 3075 BRW branch_ret
 17C7 3076
 17C7 3077 geq_tf_tf:
 0135 30 17C7 3078 BSBW setup_pli_interface\$
 64 01 D0 17CA 3079 MOVL #1, (r4)
 0000000C'EF DF 17CD 3080 PUSHAL dope2
 53 DD 17D3 3081 PUSHL r3
 00000008'EF DF 17D5 3082 PUSHAL dope1
 52 DD 17DB 3083 PUSHL r2
 00000000'GF 04 FB 17DD 3084 CALLS #4, G^PLI\$CMPBIT
 50 D5 17E4 3085 TSTL r0
 08 13 17E6 3086 BEQL geq_tf\$
 FFFFFFFFFF 8F 50 D1 17E8 3087 CMPL r0, #^xFFFFFFFF
 02 12 17EF 3088 BNEQ geq_tf\$
 64 D4 17F1 3089 CLRL (r4)
 EB0F 31 17F3 3090 geq_tf\$:
 17F3 3091 BRW branch_ret
 17F6 3092
 17F6 3093 gtr_tf_tf:
 0106 30 17F6 3094 BSBW setup_pli_interface\$
 64 01 D0 17F9 3095 MOVL #1, (r4)
 0000000C'EF DF 17FC 3096 PUSHAL dope2
 53 DD 1802 3097 PUSHL r3
 00000008'EF DF 1804 3098 PUSHAL dope1
 52 DD 180A 3099 PUSHL r2
 00000000'GF 04 FB 180C 3100 CALLS #4, G^PLI\$CMPBIT
 50 D5 1813 3101 TSTL r0
 08 13 1815 3102 BEQL not_gtrs\$
 FFFFFFFFFF 8F 50 D1 1817 3103 CMPL r0, #^xFFFFFFFF

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02	13	181E	3104	BEQL	not_gtrs\$	
02	11	1820	3105	BRB	gtr_tf\$	
64	D4	1822	3106	not_gtrs\$:		
		1822	3107	CLRL	(r4)	
EADE	31	1824	3108	gtr_tf\$:		
		1824	3109	BRW	branch_ret	
		1827	3110			
		1827	3111	leq_tf_tf\$:		
00D5	30	1827	3112	BSBW	setup_pli_interface\$	
64	01	D0	182A	MOVL	#1,(r4)	
0000000C'EF	DF	182D	3113	PUSHAL	dope2	
53	DD	1833	3114	PUSHL	r3	
00000008'EF	DF	1835	3115	PUSHAL	dope1	
52	DD	183B	3116	PUSHL	r2	
00000000'GF	04	FB	183D	CALLS	#4, G^PLI\$CMPBIT	
50	D5	1844	3118	TSTL	r0	
OB	13	1846	3120	BEQL	leq_tf\$	
FFFFFFFFFF 8F	50	D1	1848	3121	CMPL	r0, #^xFFFFFFFF
02	13	184F	3122	BEQL	leq_tf\$	
64	D4	1851	3123	CLRL	(r4)	
		1853	3124	leq_tf\$:		
EAAF	31	1853	3125	BRW	branch_ret	
		1856	3126			
		1856	3127	lss_tf_tf\$:		
00A6	30	1856	3128	BSBW	setup_pli_interface\$	
64	01	D0	1859	MOVL	#1,(r4)	
0000000C'EF	DF	185C	3129	PUSHAL	dope2	
53	DD	1862	3130	PUSHL	r3	
00000008'EF	DF	1864	3131	PUSHAL	dope1	
52	DD	186A	3132	PUSHL	r2	
00000000'GF	04	FB	186C	CALLS	#4, G^PLI\$CMPBIT	
50	D5	1873	3134	TSTL	r0	
OB	13	1875	3135	BEQL	not_lsss\$	
FFFFFFFFFF 8F	50	D1	1877	3137	CMPL	r0, #^xFFFFFFFF
02	12	187E	3138	BNEQ	not_lsss\$	
02	11	1880	3139	BRB	lss_tf\$	
		1882	3140	not_lsss\$:		
64	D4	1882	3141	CLRL	(r4)	
		1884	3142	lss_tf\$:		
EA7E	31	1884	3143	BRW	branch_ret	
		1887	3144			
		1887	3145	neq_tf_tf\$:		
0075	30	1887	3146	BSBW	setup_pli_interface\$	
64	01	D0	188A	MOVL	#1,(r4)	
0000000C'EF	DF	188D	3147	PUSHAL	dope2	
53	DD	1893	3148	PUSHL	r3	
00000008'EF	DF	1895	3149	PUSHAL	dope1	
52	DD	189B	3150	PUSHL	r2	
00000000'GF	04	FB	189D	CALLS	#4, G^PLI\$CMPBIT	
50	D5	18A4	3152	TSTL	r0	
02	12	18A6	3153	BNEQ	neq_tf\$	
64	D4	18A8	3154	CLRL	(r4)	
		18AA	3155	neq_tf\$:		
EA58	31	18AA	3156	BRW	branch_ret	
		18AD	3157			
		18AD	3158			
004F	30	18AD	3159	bit_not_tf_tf\$:		
		18AD	3160	BSBW	setup_pli_interface\$	

dbg\$perform_operator

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      51 54   DO 1880 3161      MOVL r4, r1
00000008'EF DF 1883 3162      PUSHAL dope1
      52 54   DD 1889 3163      PUSHAL r2
00000000'GF 02 FB 188B 3164      CALLS #2, G^PLI$NOTBIT
      04 18C2 3165      RET
      18C3 3166
      18C3 3167 bit_and_tf_tf:
      0039 30 18C3 3168      BSBW setup_pli_interface$
      51 54   DO 18C6 3169      MOVL r4, r1
0000000C'EF DF 18C9 3170      PUSHAL dope2
      53 54   DD 18CF 3171      PUSHAL r3
00000008'EF DF 18D1 3172      PUSHAL dope1
      52 54   DD 18D7 3173      PUSHAL r2
00000000'GF 04 FB 18D9 3174      CALLS #4, G^PLI$ANDBIT
      04 18E0 3175      RET
      18E1 3176
      18E1 3177 bit_or_tf_tf:
      001B 30 18E1 3178      BSBW setup_pli_interface$
      51 54   DO 18E4 3179      MOVL r4, r1
0000000C'EF DF 18E7 3180      PUSHAL dope2
      53 54   DD 18ED 3181      PUSHAL r3
00000008'EF DF 18EF 3182      PUSHAL dope1
      52 54   DD 18F5 3183      PUSHAL r2
00000000'GF 04 FB 18F7 3184      CALLS #4, G^PLI$ORBIT
      04 18FE 3185      RET
      18FF 3186
      18FF 3187
      18FF 3188 : This subroutine sets up the call interface required for the PL/I RTL
      18FF 3189 : bit-string routines. Those routines require the following for both
      18FF 3190 : operands:
      18FF 3191
      18FF 3192 : A dope vector of the form:
      18FF 3193
      18FF 3194
      18FF 3195
      18FF 3196
      18FF 3197
      18FF 3198 : DSC$K_DTYPE_V maps into DBG$K_PLI_ABIT,
      18FF 3199 : DSC$K_DTYPE_VU maps into DBG$R_PLI_UBIT.
      18FF 3200
      18FF 3201 : Length is in bits.
      18FF 3202 :
      18FF 3203 setup_pli_interface$:
      52 00000030'EF DO 18FF 3204      MOVL arg1_desc, r2 : r2 points left vms descriptor
0000000A'EF 62 B0 1906 3205      MOVW dsc$w_length(r2), dope1+2: get length
      01 02 A2 91 190D 3206      CMPB dsc$b_dtype(r2), #dsc$k_dtype_v
      0D 13 1911 3207      BEQL setup_pli_abit1$
      00 0C B0 1913 3208      MOVW #dbg$K_pli_ubit, dope1 : map into pli data type
      52 04 A2 DE 191A 3209      MOVAL 4(r2), r2 : Get the address of the 2nd longword
      191E 3210 : of the vms descriptor
      0B 11 191E 3211      BRB setup_pli_cont1$
      00 000008'EF 0E B0 1920 3212      setup_pli_abit1$:
      52 04 A2 D0 1920 3213      MOVW #dbg$K_pli_abit, dope1 : map into pli data type
      1927 3214      MOVL 4(r2), r2 : Get the address of the left value
      53 10 AC D0 192B 3215      setup_pli_cont1$:
      53 D5 192F 3216      MOVL right_arg(AP), r3 : Get the address of the right arg
      192F 3217      TSTL r3 : Test to see if it is present

```

dbg\$perform_operator

```

      2C   13 1931 3218    BEQL  setup_pli_result$ ; There is no right arg
      53 00000038'EF  D0 1933 3219    MOVL  arg2_desc, r3 ; r3 points right vms descriptor
      0000000E'EF  63  B0 193A 3220    MOVW  dsc$w_length(r3), dope2+2; get length
      01 02 A3  91 1941 3221    CMPB  dsc$b_dtype(r3), #dsc$k_dtype_v
      0D 13 1945 3222    BEQL  setup_pli_abit2$
      00U0000C'EF  OC  B0 1947 3223    MOVW  #dbg$k_pli_ubit, dope2 ; map into pli data type
      53 04 A3  DE 194E 3224    MOVAL 4(r3), r3 ; Get the address of the 2nd longword
      1952 3225
      0B 11 1952 3226    BRB   setup_pli_result$ ; of the vms descriptor
      0000000C'EF  0E  B0 1954 3227    setup_pli_abit2$:
      53 04 A3  D0 195B 3228    MOVW  #dbg$k_pli_abit, dope2 ; map into pli data type
      195F 3229    MOVL  4(r3), r3 ; Get the address of the right value
      54 00000040'EF  D0 195F 3231    setup_pli_result$:
      54 04 A4  D0 1966 3232    MOVL  result_desc, r4 ; r4 points to result vms descriptor
      196A 3233    MOVL  4(r4), r4 ; r4 points to the address of the result
      05 196A 3234    setup_rsb$:
      196B 3235    RSB
      196B 3236
      196B 3237    ; Record File Address data type, 6 bytes long.
      196B 3238    ;
      64  D4 196B 3239    eql_rfa_rfa:
      63 62  D1 196D 3240    CLRL  (r4)
      0A 12 1970 3241    CMPL  (r2),(r3)
      04 A3 04 A2  B1 1972 3242    BNEQ  egl_rfa$ ; r2 is not equal to r3
      03 12  , 3243    CMPW  4(r2),4(r3)
      64 01  D0 197C 3244    BNEQ  egl_rfa$ ; r2 is not equal to r3
      197F 3245    MOVL  #1,(r4)
      E986 31 197C 3246    eql_rfa$:
      197F 3247    BRW   branch_ret
      3248
      64  D4 197F 3249    neq_rfa_rfa:
      63 62  D1 1981 3250    CLRL  (r4)
      0A 13 1984 3251    CMPL  (r2),(r3)
      04 A3 04 A2  B1 1986 3252    BNEQ  neq_rfa$ ; r2 is not equal to r3
      03 13 1988 3253    CMPW  4(r2),4(r3)
      64 01  D0 198D 3254    BNEQ  neq_rfa$ ; r2 is not equal to r3
      1990 3255    MOVL  #1,(r4)
      E972 31 1990 3256    neq_rfa$:
      1993 3257    BRW   branch_ret
      3258
      64 62  7D 1993 3259    unary_plus_q:
      E96C 31 1996 3260    MOVQ  (r2),(r4)
      1999 3261    BRW   branch_ret
      3262
      64 62  D2 1999 3263    unary_minus_q:
      04 A4 04 A2  D2 199C 3264    MCOML (r2),(r4)
      64 01  C0 19A1 3265    MCOML 4(r2),4(r4)
      04 A4 00  D8 19A4 3266    ADDL2 #1,(r4)
      E95A 31 19A8 3267    ADWC  #0,4(r4)
      19AB 3268    BRW   branch_ret
      3269
      08 A4 64 62  7D 19AB 3270    unary_plus_q:
      08 A2 7D 19AE 3271    MOVQ  (r2),(r4)
      E94F 31 19B3 3272    MOVQ  8(r2),8(r4)
      19B6 3273    BRW   branch_ret
      3274

```

dbg\$perform_operator

```

      64   62    D2  19B6  3275 unary_minus_o:
04 A4   04 A2    D2  19B6  3276  MCOML  (r2), (r4)
08 A4   08 A2    D2  19B9  3277  MCOML  4(r2), 4(r4)
0C A4   0C A2    D2  19BE  3278  MCOML  8(r2), 8(r4)
          64   01    C0  19C8  3279  MCOML  12(r2), 12(r4)
04 A4   00    D8  19CB  3280  ADDL2  #1, (r4)
08 A4   00    D8  19CF  3281  ADWC   #0, 4(r4)
0C A4   00    D8  19D3  3282  ADWC   #0, 8(r4)
          E92B    31  19D7  3283  ADWC   #0, 12(r4)
                           3284  BRW    branch_ret
                           19DA  3285
                           19DA  3286 succ_enum:
00000044'EF    DD  19DA  3287  PUSHL   result_valdesc :BB001
00000034'EF    DD  19E0  3288  PUSHL   arg1_valdesc :BB001
00000000'EF  02    FB  19E6  3289  CALLS   #2, dbg$succ_enum :BB001
          04  19ED  3290  RET     :BB001
                           19EE  3291
                           19EE  3292 pred_enum:
00000044'EF    DD  19EE  3293  PUSHL   result_valdesc :BB001
00000034'EF    DD  19F4  3294  PUSHL   arg1_valdesc :BB001
00000000'EF  02    FB  19FA  3295  CALLS   #2, dbg$pred_enum :BB001
          04  1A01  3296  RET     :BB001
                           1A02  3297
                           1A02  3298 ; The following handle operations on fixed binary.
                           1A02  3299 ;
                           1A02  3300
                           1A02  3301 unary_plus_fixed:
00000044'EF    DD  1A02  3302  PUSHL   result_valdesc
00000034'EF    DD  1A08  3303  PUSHL   arg1_valdesc
00000000'EF  02    FB  1A0E  3304  CALLS   #2, dbg$unary_plus_fixed
          04  1A15  3305  RET     :
                           1A16  3306
                           1A16  3307 unary_minus_fixed:
00000044'EF    DD  1A16  3308  PUSHL   result_valdesc
00000034'EF    DD  1A1C  3309  PUSHL   arg1_valdesc
00000000'EF  02    FB  1A22  3310  CALLS   #2, dbg$unary_minus_fixed
          04  1A29  3311  RET     :
                           1A2A  3312
                           1A2A  3313 abs_fixed:
00000044'EF    DD  1A2A  3314  PUSHL   result_valdesc
00000034'EF    DD  1A30  3315  PUSHL   arg1_valdesc
00000000'EF  02    FB  1A36  3316  CALLS   #2, dbg$abs_fixed
          04  1A3D  3317  RET     :
                           1A3E  3318
                           1A3E  3319 add_fixed_fixed:
00000044'EF    DD  1A3E  3320  PUSHL   result_valdesc
0000003C'EF    DD  1A44  3321  PUSHL   arg2_valdesc
00000034'EF    DD  1A4A  3322  PUSHL   arg1_valdesc
00000000'EF  03    FB  1A50  3323  CALLS   #3, dbg$add_fixed_fixed
          04  1A57  3324  RET     :
                           1A58  3325
                           1A58  3326 sub_fixed_fixed:
00000044'EF    DD  1A58  3327  PUSHL   result_valdesc
0000003C'EF    DD  1A5E  3328  PUSHL   arg2_valdesc
00000034'EF    DD  1A64  3329  PUSHL   arg1_valdesc
00000000'EF  03    FB  1A6A  3330  CALLS   #3, dbg$sub_fixed_fixed
          04  1A71  3331  RET     :

```

dbg\$perform_operator

```

00000044'EF    DD 1A72 3332
0000003C'EF    DD 1A72 3333 mul_fixed_fixed:
00000034'EF    DD 1A72 3334      PUSHL result_valdesc
00000000'EF 03  FB 1A72 3335      PUSHL arg2_valdesc
00000000'EF 03  FB 1A78 3336      PUSHL arg1_valdesc
00000044'EF    DD 1A7E 3337      CALLS #3, dbg$mul_fixed_fixed
0000003C'EF    DD 1A84 3338      RET
00000034'EF    DD 1A8B 3339
00000000'EF 03  FB 1A8C 3340 div_fixed_fixed:
00000044'EF    DD 1A8C 3341      PUSHL result_valdesc
0000003C'EF    DD 1A92 3342      PUSHL arg2_valdesc
00000034'EF    DD 1A98 3343      PUSHL arg1_valdesc
00000000'EF 03  FB 1A9E 3344      CALLS #3, dbg$div_fixed_fixed
00000000'EF 03  FB 1AA5 3345      RET
00000044'EF    DD 1AA6 3346
0000003C'EF    DD 1AA6 3347 eql_fixed_fixed:
00000034'EF    DD 1AAC 3348      PUSHL result_valdesc
00000000'EF 03  FB 1AB2 3349      PUSHL arg2_valdesc
00000000'EF 03  FB 1AB8 3350      PUSHL arg1_valdesc
00000044'EF    DD 1AB8 3351      CALLS #3, dbg$eql_fixed_fixed
0000003C'EF    DD 1ABF 3352      RET
00000034'EF    DD 1AC0 3353
00000000'EF 03  FB 1AC0 3354 neq_fixed_fixed:
00000044'EF    DD 1AC0 3355      PUSHL result_valdesc
0000003C'EF    DD 1AC6 3356      PUSHL arg2_valdesc
00000034'EF    DD 1ACC 3357      PUSHL arg1_valdesc
00000000'EF 03  FB 1AD2 3358      CALLS #3, dbg$neq_fixed_fixed
00000000'EF 03  FB 1AD9 3359      RET
00000044'EF    DD 1ADA 3360
0000003C'EF    DD 1ADA 3361 lss_fixed_fixed:
00000034'EF    DD 1AE0 3362      PUSHL result_valdesc
00000000'EF 03  FB 1AE6 3363      PUSHL arg2_valdesc
00000000'EF 03  FB 1AE6 3364      PUSHL arg1_valdesc
00000044'EF    DD 1AE6 3365      CALLS #3, dbg$lss_fixed_fixed
0000003C'EF    DD 1AF3 3366      RET
00000034'EF    DD 1AF4 3367
00000000'EF 03  FB 1AF4 3368 gtr_fixed_fixed:
00000044'EF    DD 1AF4 3369      PUSHL result_valdesc
0000003C'EF    DD 1AFA 3370      PUSHL arg2_valdesc
00000034'EF    DD 1B00 3371      PUSHL arg1_valdesc
00000000'EF 03  FB 1B06 3372      CALLS #3, dbg$gtr_fixed_fixed
00000000'EF 03  FB 1B0D 3373      RET
00000044'EF    DD 1B0E 3374
0000003C'EF    DD 1B0E 3375 leq_fixed_fixed:
00000034'EF    DD 1B14 3376      PUSHL result_valdesc
00000000'EF 03  FB 1B14 3377      PUSHL arg2_valdesc
00000000'EF 03  FB 1B1A 3378      PUSHL arg1_valdesc
00000044'EF    DD 1B20 3379      CALLS #3, dbg$leq_fixed_fixed
0000003C'EF    DD 1B27 3380      RET
00000034'EF    DD 1B28 3381
00000000'EF 03  FB 1B28 3382 geq_fixed_fixed:
00000044'EF    DD 1B28 3383      PUSHL result_valdesc
0000003C'EF    DD 1B2E 3384      PUSHL arg2_valdesc
00000034'EF    DD 1B34 3385      PUSHL arg1_valdesc
00000000'EF 03  FB 1B3A 3386      CALLS #3, dbg$geq_fixed_fixed
00000000'EF 03  FB 1B41 3387      RET
00000044'EF    DD 1B42 3388

```

dbg\$perform_operator

1B42 3389 ; No corresponding routine index to perform the given operation, signal
1B42 3390 ; debug internal coding error.
1B42 3391 ;
1B42 3392 unknown_rout_index:
00000000'EF DF 1B42 3393 PUSHAL errmsg
01 DD 1B48 3394 PUSHL #1
00028362 8F DD 1B4A 3395 PUSHL #dbg\$ interr
00009000'GF 03 FB 1B50 3396 CALLS #3,G^IB\$SIGNAL
04 1B57 3397 RET

dbg\$strip_zeroes

```

1B58 3399 .SBTTL dbg$strip_zeroes
1B58 3400
1B58 3401 :++
1B58 3402 :GLOBAL ROUTINE dbg$strip_zeroes (VMS_DESC) =
1B58 3403
1B58 3404 :FUNCTION
1B58 3405     This routine strips leading and trailing zeroes from a packed
1B58 3406     decimal string.
1B58 3407
1B58 3408 :INPUTS
1B58 3409     VMS_DESC - A pointer to a VMS descriptor.
1B58 3410
1B58 3411 :OUTPUTS
1B58 3412     VMS_DESC is returned.
1B58 3413 :++
1B58 3414
1B58 3415 :Register usage:
1B58 3416
1B58 3417 :     r0,r1  temporaries
1B58 3418 :     r6    pointer to VMS descriptor
1B58 3419 :     r7    number of decimal digits
1B58 3420 :     r8    pointer to digit string
1B58 3421 :     r9    index
1B58 3422
1B58 3423 .ENTRY dbg$strip_zeroes, ^M<R2,R3,R4,R5,R6,R7,R8,R9>
1B5A 3424
1B5A 3425     SUBL #16,SP
1B5D 3426     MOVL 4(AP),R6
1B61 3427     CVTWL dsc$w_length(R6),R7
1B64 3428     MOVL dsc$w_pointer(R6),R8
1B68 3429 1$:   MOVP R7,(R8),(SP)
1B6C 3430     BEQL 5$
1B73 3431 2$:   ASHL #-1,R7,R9
1B75 3432     BEQL 6$
1B7A 3433     BITB #^XF0,(SP)[R9]
1B7C 3434     BNEQ 3$
1B7F 3435     MOVL R7,R0
1B81 3436     DECL R7
1B84 3437     INCB dsc$b_scale(R6)
1B8C 3438     ASHP #-1,R0,(SP),#0,R7,(R8)
1B8E 3439     BRB  1$
1B92 3440 3$:   ADDL3 #1,R9,R0
1B96 3441     SKPC #0,R0,(SP)
1B98 3442     DECL R0
1BA0 3443     ASHL #1,R0,R7
1BA4 3444     BITB #^XF0,(R1)
1BA2 3445     BEQL 4$
1BA4 3446     INCL R7
1BA8 3447 4$:   MOVP R7,(R1),(R8)
1BA8 3448     BRB  6$
1BAA 3449 5$:   MOVL #1,R7
1BAD 3450     CLRB dsc$b_scale(R6)
1BB0 3451     MOVL #^XOC,(R8)
1BB3 3452 6$:   CVTLW R7,dsc$w_length(R6)
1BB6 3453     CVTLB R7,dsc$b_digits(R6)
1BBA 3454     MOVL R6,R0
1BBD 3455     RET

      ; Local storage space
      ; Address of descriptor
      ; Number of decimal digits
      ; Address of digit string
      ; Copy decimal value to stack
      ; Special check for zero
      ; Get offset to sign byte
      ; Leave at least one digit
      ; Test high nibble of sign byte
      ; Branch if no trailing zeros
      ; Get original number of digits
      ; Count length down by one
      ; Remember scaling has changed
      ; Scale number by one digit
      ; Go repeat test for zeros
      ; Get number of bytes written
      ; Find first non-zero byte
      ; Get <# of bytes> minus 1
      ; Convert bytes to nibbles
      ; Check high nibble of byte
      ; Ignore high nibble if zero
      ; Otherwise increase length
      ; Copy over trailing digits
      ; Special handling if result
      ; is zero - scale factor is
      ; zero and sign is positive
      ; Set length in descriptor
      ; Insure digit count is set up
      ; All normalized - return

```

trap_msg_handler

```

1BBE 3457 .SBTTL trap_msg_handler
1BBE 3458 :++
1BBE 3459 :ROUTINE TRAP_MSG_HANDLER(SIGARG, MECHARG, ENBLARG): NOVALUE =
1BBE 3460
1BBE 3461 :FUNCTION
1BBE 3462   This is the handler routine for DBG$PERFORM_OPERATOR routine. It traps
1BBE 3463   overflow (V), decimal overflow (DV), floating underflow (FU), and
1BBE 3464   give an informational message to the user program. It also traps
1BBE 3465   the error condition such as divided by zero, or illegal operand type.
1BBE 3466
1BBE 3467 :INPUTS
1BBE 3468   SIGARG - The signal argument vector.
1BBE 3469
1BBE 3470   MECHARG - The mechanism argument vector.
1BBE 3471
1BBE 3472   ENBLARG - The enable argument vector.
1BBE 3473
1BBE 3474 :OUTPUTS
1BBE 3475   None.
1BBE 3476 :++
1BBE 3477
1BBE 3478
1BBE 3479 : Register usage
1BBE 3480
1BBE 3481   r2     Pointer to operator token entry
1BBE 3482   r3     Temporary
1BBE 3483
000C 1BBC 3484 .ENTRY trap_msg_handler,^M<r2,r3>
1BC0 3485
      50 04 AC  D0 1BC0 3486 MOVL chf$L_sigarglst(AP),r0 ; Pointer to Signal Arguments
      51 08 AC  D0 1BC4 3487 MOVL chf$L_mcharglst(AP),r1 ; Pointer to Mechanism Arguments
52 00000000'EF  D0 1BC8 3488 MOVL save_operator_entry,r2 ; Get the pointer to operator token
                           entry from saved area
      52 0C A2  DE 1BCF 3489 MOVAL token_name(r2),r2 ; Pointer to counted ascii string
000004BC 8F  04 A0  D1 1BD3 3490
      11 12 1BDB 3491
      52 DD 1BDD 3492 1$: CMPL chf$L_sig_name(r0),#ss$_fltovf
      01 DD 1BDF 3493 BNEQ 2$
      00028A02 8F  DD 1BE1 3494 PUSHL r2
      00000000'GF  03  FB 1BE7 3495 PUSHL #1
                           #dbg$_fltovf
                           CALLS #3,G^IB$SIGNAL
      1BEE 3496
0000049C 8F  04 A0  D1 1BEE 3497
      16 12 1BF6 3498 2$: CMPL chf$L_sig_name(r0),#ss$_fltund
      63 D4 1BFF 3500 BNEQ 3$
      52 DD 1C01 3501 MOVL save_result,r3
      01 DD 1C03 3502 CLRL (r3)
      0002869B 8F  DD 1C05 3503 PUSHL r2
      01D0 31 1C0B 3504 PUSHL #1
                           #dbg$_ifltund
                           BRW  give_info
      1COE 3505
000286A3 8F  04 A0  D1 1COE 3506 3$: CMPL chf$L_sig_name(r0),#dbg$_iintovf
      0D 12 1C16 3507 BNEQ 4$
      52 DD 1C18 3509 PUSHL r2
      01 DD 1C1A 3510 PUSHL #1
      000286A3 8F  DD 1C1C 3511 PUSHL #dbg$_iintovf
      01B9 31 1C22 3512 BRW  give_info

```

trap_msg_handler									
00028240	BF	04	A0	D1	1C25	3514		CMPL	chf\$!_sig_name(r0),#dbg\$_divbyzero
				OD	12	1C2D	3516	BNEQ	5\$
00028240	BF	DD		1C2F	3517		PUSHL	#dbg\$ divbyzero	
00000000'GF	01	FB		1C35	3518		CALLS	#1,G^[IB\$SIGNAL	
00028E00	BF	04	A0	D1	1C3C	3520	5\$:	CMPL	chf\$!_sig_name(r0),#dbg\$_sfcntneg
				OD	12	1C44	3521	BNEQ	6\$
00028E00	BF	DD		1C46	3522		PUSHL	#dbg\$ sfcntneg	
00000000'GF	01	FB		1C4C	3523		CALLS	#1,G^[IB\$SIGNAL	
000004A4	BF	04	A0	D1	1C53	3524		CMPL	chf\$!_sig_name(r0),#ss\$_decovf
				11	12	1C5B	3526	BNEQ	7\$
				52	DD	1C5D	3527	PUSHL	r2
				01	DD	1C5F	3528	PUSHL	#1
00028A3A	BF	DD		1C61	3529		PUSHL	#dbg\$ decovf	
00000000'GF	03	FB		1C67	3530		CALLS	#3,G^[IB\$SIGNAL	
000004BC	BF	04	A0	D1	1C6E	3531		CMPL	chf\$!_sig_name(r0),#ss\$_fltdiv_f
				OD	12	1C76	3533	BNEQ	8\$
00028240	BF	DD		1C78	3534		PUSHL	#dbg\$ divbyzero	
00000000'GF	01	FB		1C7E	3535		CALLS	#1,G^[IB\$SIGNAL	
000004B4	BF	04	A0	D1	1C85	3536		CMPL	chf\$!_sig_name(r0),#ss\$_fltovf_f
				11	12	1C8D	3538	BNEQ	9\$
				52	DD	1C8F	3539	PUSHL	r2
				01	DD	1C91	3540	PUSHL	#1
00028A02	BF	DD		1C93	3541		PUSHL	#dbg\$ fltovf	
00000000'GF	03	FB		1C99	3542		CALLS	#3,G^[IB\$SIGNAL	
000004C4	BF	04	A0	D1	1CA0	3544	9\$:	CMPL	chf\$!_sig_name(r0),#ss\$_fltund_f
				16	12	1CA8	3545	BNEQ	10\$
53 00000004'EF	DO			1CAA	3546		MOVL	save_result,r3	
				63	D4	1CB1	3547	CLRL	(r3)
				52	DD	1CB3	3548	PUSHL	r2
				01	DD	1CB5	3549	PUSHL	#1
0002869B	BF	DD		1CB7	3550		PUSHL	#dbg\$ ifltund	
011E	31	1CBD		3551			BRW	give_info	
00000484	BF	04	A0	D1	1CC0	3552		CMPL	chf\$!_sig_name(r0),#ss\$_intdiv
				OD	12	1CC8	3554	BNEQ	11\$
00028240	BF	DD		1CCA	3555		PUSHL	#dbg\$ divbyzero	
00000000'GF	01	FB		1CDO	3556		CALLS	#1,G^[IB\$SIGNAL	
00000494	BF	04	A0	D1	1CD7	3558	11\$:	CMPL	chf\$!_sig_name(r0),#ss\$_fltdiv
				OD	12	1CDF	3560	BNEQ	12\$
00028240	BF	DD		1CE1	3561		PUSHL	#dbg\$ divbyzero	
00000000'GF	01	FB		1CE7	3562		CALLS	#1,G^[IB\$SIGNAL	
001682C4	BF	04	A0	D1	1CEE	3564	12\$:	CMPL	chf\$!_sig_name(r0),#mth\$_floovemat
				11	12	1CF6	3566	BNEQ	13\$
				52	DD	1CF8	3567	PUSHL	r2
				01	DD	1CFA	3568	PUSHL	#1
00028A02	BF	DD		1CFc	3569		PUSHL	#dbg\$ fltovf	
00000000'GF	03	FB		1D02	3570		CALLS	#3,G^[IB\$SIGNAL	

trap_msg_handler

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(5)

			1D09	3571			
			1D09	3572	13\$:		
001682CC	BF 04 A0	D1	1D11	3574	CMPL	chf\$!_sig_name(r0),#mth\$_floundmat	
53	00000004'EF	16	DO	1D13	BNEQ	14\$	
		63	D4	1D1A	MOVL	save_result,r3	
		52	DD	1D1C	CLRL	(r3)	
		01	DD	1D1E	PUSHL	r2	
0002869B	BF 00B5	DD	1D20	3579	PUSHL	#1	
		31	1D26	3580	PUSHL	#dbg\$_ifltund	
			1D29	3581	BRW	give_info	
00168294	BF 04 A0	D1	1D29	3582	14\$:		
		0D	12	1D31	CMPL	chf\$!_sig_name(r0),#mth\$_undexp	
		52	DD	1D33	BNEQ	15\$	
		01	DD	1D35	PUSHL	r2	
00028ED8	BF 009E	DD	1D37	3586	PUSHL	#1	
		31	1D3D	3588	PUSHL	#dbg\$_undexpn	
			1D40	3589	BRW	give_info	
00000454	BF 04 A0	D1	1D40	3590	15\$:		
		11	12	1D48	CMPL	chf\$!_sig_name(r0),#ss\$_roprand	
		52	DD	1D4A	BNEQ	16\$	
		01	DD	1D4C	PUSHL	r2	
00028A0A	'EF	DD	1D4E	3595	PUSHL	#1	
00000000'GF	03	FB	1D54	3596	PUSHL	dbg\$_roprandf	
			1D5B	3597	CALLS	#3,G^LIB\$SIGNAL	
000286AB	BF 04 A0	D1	1D5B	3598	16\$:		
		0D	12	1D63	CMPL	chf\$!_sig_name(r0),#dbg\$_istrtru	
		52	DD	1D65	BNEQ	17\$	
		01	DD	1D67	PUSHL	r2	
000286AB	BF 006C	DD	1D69	3603	PUSHL	#1	
		31	1D6F	3604	PUSHL	#dbg\$_istrtru	
			1D72	3605	BRW	give_info	
0000043C	BF 04 A0	D1	1D72	3606	17\$:		
		11	12	1D7A	CMPL	chf\$!_sig_name(r0),#ss\$_opcdec	
		52	DD	1D7C	BNEQ	18\$	
		01	DD	1D7E	PUSHL	r2	
00028EE0	BF 0000'GF	DD	1D80	3611	PUSHL	#1	
00000000'GF	03	FB	1D86	3612	PUSHL	#dbg\$_opcdec	
			1D8D	3613	CALLS	#3,G^LIB\$SIGNAL	
0000047C	BF 04 A0	D1	1D8D	3614	18\$:		
		11	12	1D95	CMPL	chf\$!_sig_name(r0),#ss\$_intovf	
		52	DD	1D97	BNEQ	19\$	
		01	DD	1D99	PUSHL	r2	
00028A5A	BF 0000'GF	DD	1D9B	3619	PUSHL	#1	
00000000'GF	03	FB	1DA1	3620	PUSHL	#dbg\$_intovf	
			1DA8	3621	CALLS	#3,G^LIB\$SIGNAL	
00028EF0	BF 04 A0	D1	1DA8	3622	19\$:		
		0D	12	1DB0	CMPL	chf\$!_sig_name(r0),#dbg\$_cvtneguns	
		52	DD	1DB2	BNEQ	20\$	
		01	DD	1DB4	PUSHL	r2	
00028EF0	BF	DD	1DB6	3627	PUSHL	#1	
					PUSHL	#dbg\$_cvtneguns	

trap_msg_handler

	001F	31	1DBC	3628		
			1DBF	3629	BRW	give_info
			1DBF	3630	20\$:	
00028ED8	BF 04 A0	D1	1DBF	3631	CMPL	chf\$!_sig_name(r0),#dbg\$_undexpn
	0D	12	1DC7	3632	BNEQ	unknown_signal
	52	DD	1DC9	3633	PUSHL	r2
	01	DD	1DCB	3634	PUSHL	#1
00028ED8	BF	DD	1DCD	3635	PUSHL	#dbg\$_undexpn
0008		31	1DD3	3636	BRW	give_info
			1DD6	3637		
			1DD6	3638	unknown_signal:	
50	00000918	BF	D0	1DD6	3639	MOVL #ss\$_resignal,r0
			04	1DDD	3640	RET
			1DDE	3641		
00000000'GF	03	FB	1DDE	3642	give_info:	
			1DE5	3643	CALLS #3,G^LIB\$SIGNAL	
			04	1DF0	3644	\$UNWIND_S
				1DF1	3645	RET
					3646	

```

1DF1 3648 .SBTTL dbg$cvt_trfa_to_value
1DF1 3649 :++
1DF1 3650 :GLOBAL ROUTINE DBG$CVT_TRFA_TO_VALUE(DST_ARG, SRC_ARG, TOKENCODE): =
1DF1 3651 :FUNCTION
1DF1 3652 This routine accumulates the value in DST_ARG from SRC_ARG
1DF1 3653 depending on given radix.
1DF1 3654
1DF1 3655
1DF1 3656 This routine is called from the caller one byte at a time, ie.,
1DF1 3657 RFA value initialized to zero.
1DF1 3658 DO i FROM 1 to number of characters
1DF1 3659 RFA value = RFA value * radix + converted character value(i)
1DF1 3660
1DF1 3661 :INPUTS
1DF1 3662 DST_ARG - The address of the destination value (6 bytes).
1DF1 3663
1DF1 3664 SRC_ARG - The address of the source value (6 bytes).
1DF1 3665
1DF1 3666 TOKENCODE-Token code can be one of TOKEN$K_INTEGER,
1DF1 3667 TOKEN$K_HEX_INTEGER, TOKEN$K_BIN_INTEGER,
1DF1 3668 TOKEN$K_OCT_INTEGER.
1DF1 3669
1DF1 3670 :OUTPUTS
1DF1 3671 The result of the conversion is left in the destination value
1DF1 3672 address. Overflow status is returned.
1DF1 3673 :+
1DF1 3674 : Parameter Offsets
1DF1 3675 :
00000004 1DF1 3677 dst_arg = 4
00000008 1DF1 3678 src_arg = 8
0000000C 1DF1 3679 tokencode = 12
1DF1 3680
1DF1 3681 : Register usage
1DF1 3682 r2 Address of the dst_arg
1DF1 3683 r3 Address of the src_arg
1DF1 3684 r4,r5 quadword temporary result
1DF1 3685 r6,r7 quadword temporary result
1DF1 3686 :
1DF1 3687
1DF1 3688 .ENTRY dbg$cvt_trfa_to_value ^M<r2,r3,r4,r5,r6,r7>
52 04 AC 00FC 1DF3 3689 MOVL dst_arg(AP),r2 ; destination address of 6 bytes
53 08 AC 00 1DF7 3690 MOVL src_arg(AP),r3 ; source address of 6 bytes
54 62 00 1DFB 3691 MOVL (r2),r4 ; move the destination value
55 04 A2 3C 1DFE 3692 MOVZWL 4(r2),r5 ; into quadword (in r4,r5)
1E02 3693
1E02 3694 CMPL tokencode(AP),#token$K_integer
1E06 3695 BEQL shift_decimal$
1E08 3696 CMPL tokencode(AP),#token$K_hex_integer
1E0C 3697 BEQL shift_hexdecimal$
1E0E 3698 CMPL tokencode(AP),#token$K_bin_integer
1E12 3699 BEQL shift_binary$
1E14 3700 CMPL tokencode(AP),#token$K_oct_integer
1E18 3701 BEQL shift_octal$
0044 31 1E1A 3702 BRW report_errors
1E1D 3703
1E1D 3704 shift_decimal$: ; Multiply the value by 10

```

dbg\$cvt_trfa_to_value

```

56 54 01 79 1E1D 3705      ASHQ #1,r4,r6          ; multiply r4 by 2
54 54 03 79 1E21 3706      ASHQ #3,r4,r4          ; multiply r4 by 8
54 56 C0 1E25 3707      ADDL2 r6,r4             ; add result (= * 10)
55 57 DB 1E28 3708      ADWC r7,r5             ; Cannot be a overflow of 8
1E2B 3709
1E2B 3710
0015 31 1E2B 3711      BRW set_result$        ; bytes, it'll overflow 6
1E2E 3712
3713 shift_hexdecimal$:    ; Multiply the value by 16
54 54 04 79 1E2E 3714      ASHQ #4,r4,r4
000E 31 1E32 3715      BRW set_result$
1E35 3716
3717 shift_binary$:       ; Multiply the value by 2
54 54 01 79 1E35 3718      ASHQ #1,r4,r4
0007 31 1E39 3719      BRW set_result$
1E3C 3720
3721 shift_octals$:      ; Multiply the value by 8
54 54 03 79 1E3C 3722      ASHQ #3,r4,r4
0000 31 1E40 3723      BRW set_result$
1E43 3724
1E43 3725 set_result$:    ; Move it into destination
3726 MOVL r4,(r2)           (RFA)
55 04 A2 55 B0 1E46 3727      MOVW r5,4(r2)
0000FFFF 8F CA 1E4A 3728      BICL #^xFFFF,r5
24 12 1E51 3729      BNEQ rfa_overflow$       ; Test the high 2 bytes for
62 63 A0 1E53 3730      ADDW (r3),(r2)         overflow
02 A2 02 A3 D8 1E56 3731      ADWC 2(r3),2(r2)   ; Add the character value
1A 1F 1E5B 3732      BCS rfa_overflow$       ; into RFA (6 bytes addition)
50 01 D0 1E5D 3733      MOVL #1,r0            ; Check for overflow
04 1E60 3734      RET
1E61 3735
1E61 3736 report_error$:    ; Report error
00000035'EF DF 1E61 3737      PUSHAL errmsg1
01 DD 1E67 3738      PUSHAL #1
00028362 8F DD 1E69 3739      PUSHAL #dbg$ interr
00000000'GF 03 FB 1E6F 3740      CALLS #3,G^IB$SIGNAL
04 1E76 3741      RET
1E77 3742
1E77 3743 rfa_overflow$:    ; RFA overflow
50 D4 1E77 3744      CLRL r0
04 1E79 3745      RET
1E7A 3746

```

dbg\$cvt_tquadword_to_value

```

1E7A 3748 .SBTTL dbg$cvt_tquadword_to_value
1E7A 3749 ++
1E7A 3750 GLOBAL ROUTINE DBG$CVT_TQUADWORD_TO_VALUE(DST_ARG, SRC_ARG, TOKENCODE): =
1E7A 3751
1E7A 3752 FUNCTION
1E7A 3753 This routine accumulates the value in DST_ARG from SRC_ARG
1E7A 3754 depending on given radix.
1E7A 3755
1E7A 3756 This routine is called from the caller one byte at a time, ie.,
1E7A 3757 QUADWORD value initialized to zero.
1E7A 3758 DO i FROM 1 to number of characters
1E7A 3759 QUADWORD value = QUADWORD value * radix + converted character value(i)
1E7A 3760
1E7A 3761 NOTE: This routine assuming the dtype is Q, not QU, if dtype is QU,
1E7A 3762 then DBG$CVT_TUQUADWORD_TO_VALUE should be called instead.
1E7A 3763
1E7A 3764 INPUTS
1E7A 3765 DST_ARG - The address of the destination value (8 bytes).
1E7A 3766 SRC_ARG - The address of the source value (8 bytes).
1E7A 3767 TOKENCODE-Token code can be one of TOKEN$K_INTEGER,
1E7A 3768 TOKEN$K_HEX_INTEGER, TOKEN$K_BIN_INTEGER,
1E7A 3769 TOKEN$K_OCT_INTEGER.
1E7A 3770
1E7A 3771
1E7A 3772
1E7A 3773 OUTPUTS
1E7A 3774 The result of the conversion is left in the destination value
1E7A 3775 address. Overflow status is returned.
1E7A 3776 ++
1E7A 3777
1E7A 3778 Parameter Offsets
1E7A 3779
00000004 1E7A 3780 dst_arg = 4
00000008 1E7A 3781 src_arg = 8
0000000C 1E7A 3782 tokencode = 12
1E7A 3783
1E7A 3784 Register usage
1E7A 3785 r2 Address of the dst_arg
1E7A 3786 r3 Address of the src_arg
1E7A 3787 r4,r5 quadword temporary result
1E7A 3788 r6,r7 quadword temporary result
1E7A 3789
1E7A 3790
1E7A 3791 .ENTRY dbg$cvt_tquadword_to_value,^M<r2,r3,r4,r5,r6,r7>
52 04 AC 00FC 1E7C 3792 MOVL dst_arg(AP),r2 ; destination address of 8 bytes
53 08 AC D0 1E80 3793 MOVL src_arg(AP),r3 ; source address of 8 bytes
54 62 7D 1E84 3794 MOVQ (r2),r4 ; move the destination value
1E87 3795 into quadword (in r4,r5)
1E87 3796
04 0C AC D1 1E87 3797 CMPL tokencode(AP),#token$K_integer
15 13 1E8B 3798 BEQL shift_decimal1$
05 0C AC D1 1E8D 3799 CMPL tokencode(AP),#token$K_hex_integer
26 13 1E91 3800 BEQL shift_hexdecimal1$
0A 0C AC D1 1E93 3801 CMPL tokencode(AP),#token$K_bin_integer
29 13 1E97 3802 BEQL shift_binary1$
0B 0C AC D1 1E99 3803 CMPL tokencode(AP),#token$K_oct_integer
2C 13 1E9D 3804 BEQL shift_octal1$
```

dbg\$cvt_tquadword_to_value

```

0043 31 1E9F 3805      BRW    report_error1$  

          1EA2 3806  

          1EA2 3807 shift_decimal1$: ; Multiply the value by 10  

56 54 01 79 1EA2 3808      ASHQ   #1,r4,r6  

          53 1D 1EA6 3809      BVS    quad_overflows  

54 54 03 79 1EA8 3810      ASHQ   #3,r4,r4  

          4D 1D 1EAC 3811      BVS    quad_overflows  

54 56 C0 1EAE 3812      ADDL2  r6,r4  

55 57 D8 1EB1 3813      ADWC   r7,r5  

          45 1D 1EB4 3814      BVS    quad_overflows  

001B 31 1EB6 3815      BRW    set_result1$  

          1EB9 3816  

          1EB9 3817 shift_hexdecimal1$: ; Multiply the value by 16  

54 54 04 79 1EB9 3818      ASHQ   #4,r4,r4  

          3C 1D 1EBD 3819      BVS    quad_overflows  

          0012 31 1EBF 3820      BRW    set_result1$  

          1EC2 3821  

          1EC2 3822 shift_binary1$: ; Multiply the value by 2  

54 54 01 79 1EC2 3823      ASHQ   #1,r4,r4  

          33 1D 1EC6 3824      BVS    quad_overflows  

          0009 31 1EC8 3825      BRW    set_result1$  

          1ECB 3826  

          1ECB 3827 shift_octal1$: ; Multiply the value by 8  

54 54 03 79 1ECB 3828      ASHQ   #3,r4,r4  

          2A 1D 1ECF 3829      BVS    quad_overflows  

          0000 31 1ED1 3830      BRW    set_result1$  

          1ED4 3831  

          1ED4 3832 set_result1$: ; Move it into destination  

          1ED4 3833      MOVQ   r4,(r2) (QUADWORD)  

          1ED7 3834  

04 A2 62 63 C0 1ED7 3835      ADDL2  (r3),(r2) ; Add the character value  

          04 A3 D8 1EDA 3836      ADWC   4(r3),4(r2) ; into QUADWORD (8 bytes addition)  

          1A 1D 1EDF 3837      BVS    quad_overflows ; Check for overflow  

50 01 D0 1EE1 3838      MOVL   #1,r0  

          04 1EE4 3839      RET  

          1EE5 3840  

          1EE5 3841 report_error1$: ; Report error message  

          01 DF 1EE5 3842      PUSHAL errmsg2  

          00028362 8F DD 1EEB 3843      PUSHAL #1  

00000000'GF 03 FB 1EED 3844      PUSHAL #dbg$_interr  

          04 1EF3 3845      CALLS  #3,G^[_IB$SIGNAL]  

          04 1EFA 3846      RET  

          1EFB 3847  

          50 D4 1EFB 3848 quad_overflow$: ; Branch on signed overflow set  

          04 1efd 3849      CLRL   r0  

          1EFB 3850      RET

```

dbg\$cvt_tuquadword_to_value

1EFE 3852 .SBTTL dbg\$cvt_tuquadword_to_value
 1EFE 3853 ++
 1EFE 3854 GLOBAL ROUTINE DBG\$CVT_TUQUADWORD_TO_VALUE(DST_ARG, SRC_ARG, TOKENCODE): =
 1EFE 3855
 1EFE 3856 FUNCTION
 1EFE 3857 This routine accumulates the value in DST_ARG from SRC_ARG
 1EFE 3858 depending on given radix.
 1EFE 3859
 1EFE 3860 This routine is called from the caller one byte at a time, ie.,
 1EFE 3861 QUADWORD value initialized to zero.
 1EFE 3862 DO i FROM 1 to number of characters
 1EFE 3863 QUADWORD value = QUADWORD value * radix + converted character value(i)
 1EFE 3864
 1EFE 3865 NOTE: This routine assuming the dtype is QU, not Q, if dtype is Q,
 1EFE 3866 then DBG\$CVT_TQUADWORD_TO_VALUE should be called instead.
 1EFE 3867
 1EFE 3868 INPUTS
 1EFE 3869 DST_ARG - The address of the destination value (8 bytes).
 1EFE 3870 1EFE 3871 SRC_ARG - The address of the source value (8 bytes).
 1EFE 3872 1EFE 3873 TOKENCODE-Token code can be one of TOKEN\$K_INTEGER,
 1EFE 3874 TOKEN\$K_HEX_INTEGER, TOKEN\$K_BIN_INTEGER,
 1EFE 3875 TOKEN\$K_OCT_INTEGER.
 1EFE 3876
 1EFE 3877 OUTPUTS
 1EFE 3878 The result of the conversion is left in the destination value
 1EFE 3879 address. Overflow status is returned.
 1EFE 3880 ++
 1EFE 3881
 1EFE 3882 Parameter Offsets
 1EFE 3883
 00000004 1EFE 3884 dst_arg = 4
 00000008 1EFE 3885 src_arg = 8
 0000000C 1EFE 3886 tokencode = 12
 1EFE 3887
 1EFE 3888 Register usage
 1EFE 3889 r2 Address of the dst_arg
 1EFE 3890 r3 Address of the src_arg
 1EFE 3891 r4,r5 quadword temporary result
 1EFE 3892 r6,r7 quadword temporary result
 1EFE 3893
 1EFE 3894
 1EFE 3895 .ENTRY dbg\$cvt_tuquadword_to_value,^M<r2,r3,r4,r5,r6,r7>
 52 04 AC 00FC 1EFE 3896 MOVL dst_arg(AP),r2 ; destination address of 8 bytes
 53 08 AC D0 1F00 3897 MOVL src_arg(AP),r3 ; source address of 8 bytes
 54 62 7D 1F04 3898 MOVQ (r2),r4 ; move the destination value
 1F0B 3899
 1F0B 3900
 04 0C AC D1 1F0B 3901 CMPL tokencode(AP),#token\$K_integer
 15 13 1F0F 3902 BEQL shift_decimalu1\$
 05 0C AC D1 1F11 3903 CMPL tokencode(AP),#token\$K_hex_integer
 22 13 1F15 3904 BEQL shift_hexdecimalu1\$
 0A 0C AC D1 1F17 3905 CMPL tokencode(AP),#token\$K_bin_integer
 23 13 1F1B 3906 BEQL shift_binaryu1\$
 0B 0C AC D1 1F1D 3907 CMPL tokencode(AP),#token\$K_oct_integer
 24 13 1F21 3908 BEQL shift_octalu1\$

dbg\$cvt_tuquadword_to_value

```

0039 31 1F23 3909 BRW report_erroru1$  

      1F26 3910  

      1F26 3911 shift_decimalu1$: : Multiply the value by 10  

      56 54 01 79 1F26 3912 ASHQ #1,r4,r6 : multiply r4 by 2  

      54 54 03 79 1F2A 3913 ASHQ #3,r4,r4 : multiply r4 by 8  

      54 56 C0 1F2E 3914 ADDL2 r6,r4 : add result (= * 10)  

      55 57 D8 1F31 3915 ADWC r7,r5 : Add with carry  

      3F 1F 1F34 3916 BCS uquad_overflows : Branch on unsigned overflow set  

      0015 31 1F36 3917 BRW set_resultu1$  

      1F39 3918  

      1F39 3919 shift_hexdecimalu1$: : Multiply the value by 16  

      54 54 04 79 1F39 3920 ASHQ #4,r4,r4  

      000E 31 1F3D 3921 BRW set_resultu1$  

      1F40 3922  

      1F40 3923 shift_binaryu1$: : Multiply the value by 2  

      54 54 01 79 1F40 3924 ASHQ #1,r4,r4  

      0007 31 1F44 3925 BRW set_resultu1$  

      1F47 3926  

      1F47 3927 shift_octalu1$: : Multiply the value by 8  

      54 54 03 79 1F47 3928 ASHQ #3,r4,r4  

      0000 31 1F4B 3929 BRW set_resultu1$  

      1F4E 3930  

      1F4E 3931 set_resultu1$: : Move it into destination  

      62 54 7D 1F4E 3932 MOVQ r4,(r2) (QUADWORD)  

      1F51 3933  

      62 63 C0 1F51 3934 ADDL2 (r3),(r2) : Add the character value  

      04 A2 04 A3 D8 1F54 3935 ADWC 4(r3),4(r2) into QUADWORD (8 bytes addition)  

      1A 1F 1F59 3936 BCS uquad_overflows : Check for overflow  

      50 01 D0 1F5B 3937 MOVL #1,r0  

      04 1F5E 3938 RET  

      1F5F 3939  

      1F5F 3940 report_erroru1$:  

      0000009E'EF DF 1F5F 3941 PUSHAL errmsg3  

      01 DD 1F65 3942 PUSHL #1  

      00028362 8F DD 1F67 3943 PUSHL #dbg$ interr  

      00000000'GF 03 FB 1F6D 3944 CALLS #3,G^IB$SIGNAL  

      04 1F74 3945 RET  

      1F75 3946  

      1F75 3947 uquad_overflow$:  

      50 D4 1F75 3948 CLRL r0  

      04 1F77 3949 RET
    
```

dbg\$cvt_toctaword_to_value

```

1F78 3951 .SBTTL dbg$cvt_toctaword_to_value
1F78 3952 :++
1F78 3953 :GLOBAL ROUTINE DBG$CVT_TOCTAWORD_TO_VALUE(DST_ARG, SRC_ARG, TOKENCODE): =
1F78 3954 :
1F78 3955 :FUNCTION
1F78 3956   This routine accumulates the value in DST_ARG from SRC_ARG
1F78 3957   depending on given radix.
1F78 3958 :
1F78 3959   This routine is called from the caller one byte at a time, ie.,
1F78 3960   OCTAWORD value initialized to zero.
1F78 3961   DO i FROM 1 to number of characters
1F78 3962     OCTAWORD value = OCTAWORD value * radix + converted character value(i)
1F78 3963 :
1F78 3964   This routine is used for signed octaword.
1F78 3965 :
1F78 3966 :INPUTS
1F78 3967   DST_ARG - The address of the destination value (16 bytes).
1F78 3968   SRC_ARG - The address of the source value (16 bytes).
1F78 3969   TOKENCODE-Token code can be one of TOKEN$K_INTEGER,
1F78 3970             TOKEN$K_HEX_INTEGER, TOKEN$K_BIN_INTEGER,
1F78 3971             TOKEN$K_OCT_INTEGER.
1F78 3972 :
1F78 3973 :
1F78 3974 :
1F78 3975 :OUTPUTS
1F78 3976   The result of the conversion is left in the destination value
1F78 3977   address. Overflow status is returned.
1F78 3978 :++
1F78 3979 :
1F78 3980 : Parameter Offsets
1F78 3981 :
1F78 3982   dst_arg = 4
1F78 3983   src_arg = 8
1F78 3984   tokencode = 12
1F78 3985 :
1F78 3986 : Register usage
1F78 3987   r2      Address of the dst_arg
1F78 3988   r3      Address of the src_arg
1F78 3989 :
1F78 3990 :
1F78 3991 .ENTRY dbg$cvt_toctaword_to_value,^M<r2,r3,r4,r5,r6,r7,r8,r9,r10,r11>
1F78 3992 MOVL dst_arg(AP),r2 ; destination address of 16 bytes
1F78 3993 MOVL src_arg(AP),r3 ; source address of 16 bytes
1F78 3994 MOVQ (r2),work_octa ; move the destination value
1F78 3995           : into work_octa
00000004          OFFC
52 04 AC DD 1F7A 3996 MOVQ 8(r2),work_octa+8
53 08 AC DD 1F7E 3997 CLRO r4
0000005C'EF 62 7D 1F82 3998 CLRO r8
00000064'EF 08 A2 7D 1F89 3999 CMPL tokencode(AP),#token$K_integer
54 7CFD 1F91 3997 BEQL decimal$
58 7CFD 1F94 3998 CMPL tokencode(AP),#token$K_hex_integer
04 0C AC D1 1F97 3999 BEQL hexdecimal$
15 13 1F9B 4000 CMPL tokencode(AP),#token$K_bin_integer
05 0C AC D1 1F9D 4001 BEQL binary$
12 13 1FA1 4002 CMPL tokencode(AP),#token$K_oct_integer
0A 0C AC D1 1FA3 4003 BEQL octal$
0F 13 1FA7 4004 BRW report_error2$  

0B 0C AC D1 1FA9 4005
0C 13 1FAD 4006
0164 31 1FAF 4007

```

dbg\$cvt_toctaword_to_value

```

0009 31 1FB2 4008 decimal$:
          1FB2 4009 BRW shift_decimal2$
          1FB5 4010 hexdecimal$:
          1FB5 4011 BRW shift_hexdecimal2$
          1FB8 4012 binary$:
          1FB8 4013 BRW shift_binary2$
          1FBB 4014 octal$:
          1FBB 4015 BRW shift_octal2$
          1FBE 4016
          1FBE 4017 shift_decimal2$: ; Multiply the value by 10
          1FBE 4018
54 1F 01 0000005C'EF F0 1FBE 4019 INSV work_octa,#1,#31,r4 ; multiply work_octa by 2
          1FC7 4020
          1FC7 4021
          1FC7 4022
          1FC7 4023
          1FC7 4024
55 0000005C'EF 20 1F EF 1FC7 4025 EXTZV #31,#32,work_octa,r5 ; Move integer to bit-field
          1FD0 4026 move from work_octa into
          1FD0 4027 pos 1, length 31 of r4
          57 3F EF 1FD0 4028 r4 is zero out first,
          57 8F EF 1FD9 4029 EXTZV #63,#32,work_octa,r6 so bit 0 of r4 is zero.
          57 50 1FE5 EXTZV #95,#32,work_octa,r7 ; Move bit-field into integer
          50 8F EF 1FE6 4030 move from work_octa
          48 12 1FF2 4031 pos 31, length 32 to r5
          48 12 1FF3 4031 BNEQ decimal_ov$ ; Check to see if the leftover
          58 1D 03 0000005C'EF F0 1FF5 4033 INSV work_octa,#3,#29,r8 ; bits are zero, if not,
          59 0000005C'EF 20 1D EF 1FFE 4034 EXTZV #29,#32,work_octa,r9 we have overflow.
          5A 0000005C'EF 20 3D EF 2007 4035 EXTZV #61,#32,work_octa,r10 ; multiply work_octa by 8
          0000005C'EF 20 0000005D 8F EF 2010 4036 EXTZV #93,#32,work_octa,r11
          58 0000005C'EF 03 0000007D 8F EF 201D 4037 EXTZV #125,#3,work_octa,r0
          50 2029 11 12 202A 4038 BNEQ decimal_ov$ ; Add two *2 + *8 = *10
          58 54 C0 202C 4039 ADDL2 r4,r8
          59 55 D8 202F 4040 ADWC r5,r9
          5A 56 D8 2032 4041 ADWC r6,r10
          5B 57 D8 2035 4042 ADWC r7,r11 ; Add with carry
          03 1D 2038 4043 BVS decimal_ov$ ; Branch on signed overflow set
          00BA 31 203A 4044 BRW set_result2$
          00EC 31 203D 4045 decimal_ov$: ; Multiply the value by 16
          2040 4046 BRW octa_overflow$ ; :
          2040 4047
          58 1C 04 0000005C'EF F0 2040 4049 INSV work_octa,#4,#28,r8
          59 0000005C'EF 20 1C EF 2049 4050 EXTZV #28,#32,work_octa,r9
          5A 0000005C'EF 20 3C EF 2052 4051 EXTZV #60,#32,work_octa,r10
          0000005C'EF 20 0000005C 8F EF 2058 4052 EXTZV #92,#32,work_octa,r11
          5B 2067 03 12 2075 4054 BNEQ hexdecimal_ov$ ; :
          007D 31 2077 4055 BRW set_result2$ ; :
          00AF 31 207A 4056 hexdecimal_ov$: BRW octa_overflow$ ; :
          207D 4057

```

DB
VC

```

        .cvt_toctaword_to_value

      58 1F 01 0000005C'EF  FO 207D 4059 shift_binary2$:
      59 0000005C'EF 20 1F   EF 207D 4060 INSV work_octa,#1,#31,r8
      5A 0000005C'EF 20 3F   EF 2086 4061 EXTZV #31,#32,work_octa,r9
0000005C'EF 20 0000005F 8F   EF 208F 4062 EXTZV #63,#32,work_octa,r10
0000005C'EF 01 0000007F 8F   EF 2098 4063 EXTZV #95,#32,work_octa,r11
                                5B 20A4
                                50 20B1
                                03 12 20B2 4064 EXTZV #127,#1,work_octa,r0
                                0040 31 20B4 4065 BNEQ binary_ov$:
                                0072 31 20B7 4066 BRW set_result2$:
                                20B7 4067 binary_ov$:
                                20B7 4068 BRW octa_overflow$:
                                20BA 4069

      58 1D 03 0000005C'EF  FO 20BA 4070 shift_octal2$:
      59 0000005C'EF 20 1D   EF 20C3 4071 INSV work_octa,#3,#29,r8
      5A 0000005C'EF 20 3D   EF 20CC 4072 EXTZV #29,#32,work_octa,r9
0000005C'EF 20 0000005D 8F   EF 20D5 4073 EXTZV #61,#32,work_octa,r10
0000005C'EF 03 0000007D 8F   EF 20E1 4074 EXTZV #93,#32,work_octa,r11
                                5B 20E1
                                50 20EE
                                03 12 20EF 4075 EXTZV #125,#3,work_octa,r0
                                0003 31 20F1 4076 BNEQ octal_ov$:
                                0035 31 20F4 4077 BRW set_result2$:
                                20F4 4078 octal_ov$:
                                20F4 4079 BRW octa_overflow$:
                                20F7 4080
                                62 58 7D 20F7 4081 set_result2$:
                                20FA 4082 MOVQ r8,(r2)
                                20FA 4083
                                08 A2 5A 7D 20FA 4084 MOVQ r10,8(r2)
                                62 63 C0 20FE 4085 ADDL2 (r3),(r2)
04 A2 04 A3 D8 2101 4086 ADWC 4(r3),4(r2)
08 A2 08 A3 D8 2106 4087 ADWC 8(r3),8(r2)
OC A2 0C A3 D8 210B 4088 ADWC 12(r3),12(r2)
                                1A 1D 2110 4089 BVS octa_overflow$:
                                50 01 D0 2112 4090 MOVL #1,r0
                                04 2115 4091 RET
                                2116 4092
                                2116 4093 report_error2$:
000000D6'EF  DF 2116 4094 PUSHAL errmsg4
01 DD 211C 4095 PUSHAL #1
00028362 8F  DD 211E 4096 PUSHAL #dbg$,interr
00000000'GF  03 FB 2124 4097 CALLS #3,G^IB$SIGNAL
                                04 212B 4098 RET
                                212C 4099
                                212C 4100 octa_overflow$:
50 D4 212C 4101 CLRL r0
04 212E 4102 RET
212F 4103
212F 4104 .END

```

ABS_B	000001030	R	04	BIT_AND_W_W	00000E89	R	04
ABS_B_NEGATE	000001038	R	04	BIT_EQV_B_B	00000E99	R	04
ABS_D	000001060	R	04	BIT_EQV_L_L	00000EA9	R	04
ABS_D_NEGATE	000001068	R	04	BIT_EQV_W_W	00000EA1	R	04
ABS_F	000001054	R	04	BIT_IMP_B_B	00000EDB	R	04
ABS_FIXED	000001A2A	R	04	BIT_IMP_L_L	00000EEB	R	04
ABS_F_NEGATE	00000105C	R	04	BIT_IMP_W_W	00000EE3	R	04
ABS_G	00000106C	R	04	BIT_NOT_B	00000EB1	R	04
ABS_G_NEGATE	000001076	R	04	BIT_NOT_L	00000EB9	R	04
ABS_H	00000107B	R	04	BIT_NOT_TF_TF	000018AD	R	04
ABS_H_NEGATE	000001085	R	04	BIT_NOT_W	00000EB5	R	04
ABS_L	000001048	R	04	BIT_OR_B_B	00000EBD	R	04
ABS_L_NEGATE	000001050	R	04	BIT_OR_L_L	00000EC7	R	04
ABS_W	00000103C	R	04	BIT_OR_TF_TF	000018E1	R	04
ABS_W_NEGATE	000001044	R	04	BIT_OR_W_W	00000EC2	R	04
ADDPS	000001451	R	04	BIT_XOR_B_B	00000ECC	R	04
ADDRESS_L	0000012D7	R	04	BIT_XOR_L_L	00000ED6	R	04
ADD_BS	00000031A	R	04	BIT_XOR_W_W	00000ED1	R	04
ADD_BUS	000000324	R	04	BRANCH RET	00000305	R	04
ADD_BU_BU	00000031D	R	04	CHFSL_MCHARGLST	= 00000008		
ADD_B_B	000000313	R	04	CHFSL_SIGARGLST	= 00000004		
ADD_DC_DC	000000371	R	04	CHFSL_SIG_NAME	= 00000004		
ADD_D_D	000000354	R	04	CONCAT_0K\$	00000A50	R	04
ADD_FC_FC	000000365	R	04	CONCAT_TS	00000A30	R	04
ADD_FIXED_FIXED	000001A3E	R	04	CONCAT_TF_TF	00001783	R	04
ADD_F_F	00000034F	R	04	CONCAT_T_T	00000A11	R	04
ADD_GC_GC	00000037D	R	04	DBG\$ABS_FIXED	***** X 00		
ADD_G_G	000000359	R	04	DBG\$ADD_FIXED_FIXED	***** X 00		
ADD_HC_HC	00000038B	R	04	DBG\$BLISS_BITSELECT	***** X 00		
ADD_H_H	00000035F	R	04	DBG\$BLISS_INDIRECTION	***** X 00		
ADD_LS	000000342	R	04	DBG\$B_BPT_INS	00000060		
ADD_LUS	00000034C	R	04	DBG\$B_PREV_PRO1	0000005E		
ADD_LU_LU	000000345	R	04	DBG\$B_PREV_PRO2	0000005F		
ADD_L_E	00000033B	R	04	DBG\$B_USER_OPCODE	00000040		
ADD_PP	00000143C	R	04	DBG\$CVT_TOCTAWORD_TO_VALUE	00001F78 RG	04	
ADD_TPTR_L	0000012FC	R	04	DBG\$CVT_TQUADWORD_TO_VALUE	00001E7A RG	04	
ADD_WS	00000032E	R	04	DBG\$CVT_TRFA_TO_VALUE	00001DF1 RG	04	
ADD_WUS	000000338	R	04	DBG\$CVT_TUQUADWORD_TO_VALUE	00001EFE RG	04	
ADD_WU_WU	000000331	R	04	DBG\$C_ADDRESS_OF	***** X 00		
ADD_W_W	000000327	R	04	DBG\$C_ADD_TPTR_L	***** X 00		
AND_B_B	000000EF3	R	04	DBG\$C_INDIRECTION	***** X 00		
AND_D_D	000000F17	R	04	DBG\$C_PRE_DECR_TPTR	***** X 04		
AND_L_L	000000F0B	R	04	DBG\$C_PRE_INCR_TPTR	***** X 04		
AND_W_W	000000EFF	R	04	DBG\$C_RUNFR_LEN	00000065		
ARGT_DESC	000000030	R	03	DBG\$C_SIZEOF	***** X 00		
ARG1_VALDESC	000000034	R	03	DBG\$C_SUB_TPTR_L	***** X 00		
ARG2_DESC	000000038	R	03	DBG\$C_SUB_TPTR_TPTR	***** X 00		
ARG2_VALDESC	00000003C	R	03	DBG\$DIV_FIXED_FIXED	***** X 00		
BASIC\$	00000030F	R	04	DBG\$EQ_FIXED_FIXED	***** X 00		
BGN	000000075	R	04	DBG\$GB_LANGUAGE	***** X 00		
BINARYS	000001FB8	R	04	DBG\$GEQ_FIXED_FIXED	***** X 00		
BINARY_OVS	0000020B7	R	04	DBG\$GTR_FIXED_FIXED	***** X 00		
BITPOS	= 000000002			DBG\$K_BASIC	= 00000004		
BITSELECT	0000010AD	R	04	DBG\$K_PLI_ABIT	= 0000000E		
BIT_AND_B_B	000000E81	R	04	DBG\$K_PLI_UBIT	= 0000000C		
BIT_AND_L_L	000000E91	R	04	DBG\$K_RUNFR_LEN	00000065		
BIT_AND_TF_TF	0000018C3	R	04	DBG\$LEQ_FIXED_FIXED	***** X 00		

DBG\$LSS FIXED_FIXED		X 00	DIFFERENCE_SET2\$	000010F6 R 04
DBG\$L_BPT PC	0000004A		DIFFERENCE_SET3\$	000010FA R 04
DBG\$L_CALL_ADDR	00000052		DIFFERENCE_SET4\$	00001104 R 04
DBG\$L_FRAME_PTR	0000004E		DIFFERENCE_SET_RET\$	00001117 R 04
DBG\$L_NEXT_LINK	00000000		DIFFERENCE_SET_SET	000010C4 R 04
DBG\$L_SAVE_FLD	00000061		DIV_B\$	00000426 R 04
DBG\$L_USER_AP	00000034		DIV_BUS	00000439 R 04
DBG\$L_USER_FP	00000038		DIV_BU_BU	00000429 R 04
DBG\$L_USER_PC	00000040		DIV_BY_ZERO	000002CD R 04
DBG\$L_USER_PSL	00000044		DIV_B_B	0000041F R 04
DBG\$L_USER_RO	00000004		DIV_D\$	00000548 R 04
DBG\$L_USER_R1	00000008		DIV_DC_DC	000004DA R 04
DBG\$L_USER_R10	0000002C		DIV_D_D	00000490 R 04
DBG\$L_USER_R11	00000030		DIV_FCS	000004D7 R 04
DBG\$L_USER_R2	0000000C		DIV_FC_FC	000004A1 R 04
DBG\$L_USER_R3	00000010		DIV_FIXED_FIXED	00001A8C R 04
DBG\$L_USER_R4	00000014		DIV_F_F	0000048B R 04
DBG\$L_USER_R5	00000018		DIV_GCS	000005C7 R 04
DBG\$L_USER_R6	0000001C		DIV_GC_GC	0000054B R 04
DBG\$L_USER_R7	00000020		DIV_G_G	00000495 R 04
DBG\$L_USER_R8	00000024		DIV_HCS	00000646 R 04
DBG\$L_USER_R9	00000028		DIV_HC_HC	000005CA R 04
DBG\$L_USER_REGS	00000004		DIV_H_R	0000049B R 04
DBG\$L_USER_SP	0000003C		DIV_L\$	00000460 R 04
DBG\$L_WATCHPT	00000056		DIV_LU1\$	00000481 R 04
DBG\$L_WATCHPTEN	0000005A		DIV_LU2\$	00000484 R 04
DBG\$MUL_FIXED_FIXED	***** X 00		DIV_LU_LU	00000463 R 04
DBG\$NEQ_FIXED_FIXED	***** X 00		DIV_L_L	00000459 R 04
DBG\$PERFORM OPERATOR	00000000 RG 04		DIV_P_P	000155D R 04
DBG\$PRED_ENUM	***** X 00		DIV_W\$	00000443 R 04
DBG\$STRIP_ZEROES	00001B58 RG 04		DIV_WWS	00000456 R 04
DBG\$SUB_FIXED_FIXED	***** X 00		DIV_WU_WU	00000446 R 04
DBG\$SUCC_ENUM	***** X 00		DIV_W_W	0000043C R 04
DBG\$UNARY_MINUS_FIXED	***** X 00		DOPE1	00000008 R 03
DBG\$UNARY_PLUS_FIXED	***** X 00		DOPE2	0000000C R 03
DBG\$W_RUN_STAT	00000048		DSC\$A_POINTER	= 00000004
DBG\$_CPOSTDECR	= 0002873B		DSC\$B_DIGITS	= 00000009
DBG\$_CPOSTINCR	= 0002872B		DSC\$B_DTYPE	= 00000002
DBG\$_CPREDECR	= 00028733		DSC\$B_SCALE	= 00000008
DBG\$_CPREINCR	= 00028723		DSC\$K_DTYPE_V	= 00000001
DBG\$_CVTNEGUNS	= 00028EF0		DSC\$W_LENGTH	= 00000000
DBG\$_DECOVF	= 00028A3A		DST_ARG	= 00000004
DBG\$_DIVBYZERO	= 00028240		EQL_B\$	00000B81 R 04
DBG\$_FLTTOVF	= 00028A02		EQL_B_B	00000B77 R 04
DBG\$_IFLTUND	= 0002869B		EQL_D\$	00000BB5 R 04
DBG\$_IINTOVF	= 000286A3		EQL_DCS	00000BF9 R 04
DBG\$_INTERR	= 00028362		EQL_DC_DC	00000BE8 R 04
DBG\$_INTOVF	= 00028A5A		EQL_D_D	00000BAB R 04
DBG\$_ISTRTRU	= 000286AB		EQL_F\$	00000BA8 R 04
DBG\$_OPCDEC	= 00028EE0		EQL_FCS	00000BE5 R 04
DBG\$_ROPRANDF	= 00028A0A		EQL_FC_FC	00000BD4 R 04
DBG\$_SF_CNTNEG	= 00028EC0		EQL_FIXED_FIXED	00001AA6 R 04
DBG\$_STRNGPAD	= 0002866B		EQL_F_F	00000B9E R 04
DBG\$_UNDEXPN	= 00028ED8		EQL_G\$	00000BC3 R 04
DECIMALS	00001FB2 R 04		EQL_GCS	00000C0F R 04
DECIMAL_OVS	0000203D R 04		EQL_GC_GC	00000BFC R 04
DIFFERENCE_SET1\$	000010E4 R 04		EQL_G_G	00000BB8 R 04

EQL_H\$	00000BD1	R	04	GTR_B\$
EQL_HCS	00000C25	R	04	GTR_B B
EQL_HC HC	00000C12	R	04	GTR_D\$
EQL_H R	00000BC6	R	04	GTR_D D
EQL_L\$	00000B9B	R	04	GTR_F\$
EQL_L L	00000B91	R	04	GTR_FIXED_FIXED
EQL_P\$	00001645	R	04	GTR_F F
EQL_P P	00001610	R	04	GTR_G\$
EQL_RFAS	0000197C	R	04	GTR_G G
EQL_RFA RFA	0000196B	R	04	GTR_H\$
EQL_SET\$	0000112C	R	04	GTR_H H
EQL_SET2\$	00001142	R	04	GTR_L\$
EQL_SET3\$	00001146	R	04	GTR_LUS
EQL_SET4\$	00001153	R	04	GTR_LU LU
EQL_SET_RET\$	0000115E	R	04	GTR_LL
EQL_SET_SET	00001118	R	04	GTR_P\$
EQL_T\$	00000A7F	R	04	GTR_P P
EQL_TFS	000017C4	R	04	GTR_TS
EQL_TF TF	000017A1	R	04	GTR_TFS
EQL_T T	00000A63	R	04	GTR_TF TF
EQL_VT VT	00000A51	R	04	GTR_T T
EQL_WS	00000B8E	R	04	GTR_VT VT
EQL_W W	00000B84	R	04	GTR_WS
ERRMSG	00000000	R	02	GTR_W W
ERRMSG1	00000035	R	02	HEXDECIMALS
ERRMSG2	00000067	R	02	HEXDECIMAL_OVS
ERRMSG3	0000009E	R	02	INDIRECT LU
ERRMSG4	000000D6	R	02	INDIRECT_TPTR
ERRMSG5	0000010D	R	02	INTERSECT_SET1\$
EXT_PREC_DIV	00000474	R	04	INTERSECT_SET2\$
GEQ_B\$	00000CE3	R	04	INTERSECT_SET3\$
GEQ_B B	00000CD9	R	04	INTERSECT_SET4\$
GEQ_D\$	00000D24	R	04	INTERSECT_SET_RET\$
GEQ_D D	00000D1A	R	04	INTERSECT_SET_SET
GEQ_F\$	00000D17	R	04	INT_OVERFLOW
GEQ_FIXED_FIXED	00001B28	R	04	IN_SET\$
GEQ_F F	00000D0D	R	04	IN_SET SET
GEQ_G\$	00000D32	R	04	LEFT_ARG
GEQ_G G	00000D27	R	04	LEQ_B\$
GEQ_H\$	00000D40	R	04	LEQ_B B
GEQ_H H	00000D35	R	04	LEQ_D\$
GEQ_L\$	00000CFD	R	04	LEQ_D D
GEQ_LUS	00000D0A	R	04	LEQ_F\$
GEQ_LU LU	00000D00	R	04	LEQ_FIXED_FIXED
GEQ_L L	00000CF3	R	04	LEQ_F F
GEQ_P\$	000016A5	R	04	LEQ_G\$
GEQ_P P	00001694	R	04	LEQ_G G
GEQ_SET_SET	0000115F	R	04	LEQ_H\$
GEQ_TS	00000AB0	R	04	LEQ_H H
GEQ_TFS	000017F3	R	04	LEQ_L\$
GEQ_TF TF	000017C7	R	04	LEQ_LUS
GEQ_T T	00000A94	R	04	LEQ_LU LU
GEQ_VT VT	00000A82	R	04	LEQ_LL
GEQ_WS	00000CF0	R	04	LEQ_P\$
GEQ_W W	00000CE6	R	04	LEQ_P P
GET_RESULT_ADDRS	0000004B	R	04	LEQ_SET1\$
GIVE_INFO	00001DDE	R	04	LEQ_SET2\$

00000D4D	R	04
00000D43	R	04
00000D8E	R	04
00000D84	R	04
00000D81	R	04
00001AF4	R	04
00000D77	R	04
00000D9C	R	04
00000D91	R	04
00000DAA	R	04
00000D9F	R	04
00000D67	R	04
00000D74	R	04
00000D6A	R	04
00000D5D	R	04
00001691	R	04
00001680	R	04
00000AE1	R	04
00001824	R	04
000017F6	R	04
00000AC5	R	04
00000AB3	R	04
00000D5A	R	04
00000D50	R	04
00001FB5	R	04
0000207A	R	04
0000108A	R	04
0000109B	R	04
000011A9	R	04
000011BE	R	04
000011C2	R	04
000011CB	R	04
000011DD	R	04
00001189	R	04
000002B0	R	04
00001188	R	04
0000117E	R	04
= 0000000C		
00000DB7	R	04
00000DAD	R	04
00000DF8	R	04
00000DEE	R	04
00000DEB	R	04
00001B0E	R	04
00000DE1	R	04
00000E06	R	04
00000DFB	R	04
00000E14	R	04
00000E09	R	04
00000DD1	R	04
00000DDE	R	04
00000DD4	R	04
00000DC7	R	04
000016CD	R	04
000016BC	R	04
000011F2	R	04
0000120B	R	04

DBGPERMOP
Symbol table

LEQ_SET3\$	0000120F	R	04	MUL_L\$	00000696	R	04
LEQ_SET4\$	00001220	R	04	MUL_LU\$	00000684	R	04
LEQ_SET_RET\$	0000122B	R	04	MUL_LU LU	00000699	R	04
LEQ_SET_SET	000011DE	R	04	MUL_L_C	0000068F	R	04
LEQ_TS	00000B12	R	04	MUL_P\$	00001543	R	04
LEQ_TFS	00001853	R	04	MUL_P P	000014B4	R	04
LEQ_TF TF	00001827	R	04	MUL_W\$	00000673	R	04
LEQ_T T	00000AF6	R	04	MUL_WU\$	0000068C	R	04
LEQ_VT VT	00000AE4	R	04	MUL_WU WU	00000676	R	04
LEQ_WS	00000DC4	R	04	MUL_W Q	0000066C	R	04
LEQ_W W	00000DBA	R	04	NEQ_B\$	00000C32	R	04
LIB\$SIGNAL	*****	X	04	NEQ_B B	00000C28	R	04
LSS_BS	00000E21	R	04	NEQ_D\$	00000C66	R	04
LSS_B B	00000E17	R	04	NEQ_DCS	00000CAA	R	04
LSS_D\$	00000E62	R	04	NEQ_DC DC	00000C99	R	04
LSS_D D	00000E58	R	04	NEQ_D D	00000C5C	R	04
LSS_F\$	00000E55	R	04	NEQ_F\$	00000C59	R	04
LSS_FIXED_FIXED	00001ADA	R	04	NEQ_FCS	00000C96	R	04
LSS_FF	00000E4B	R	04	NEQ_FC FC	00000C85	R	04
LSS_G\$	00000E70	R	04	NEQ_FIXED_FIXED	00001AC0	R	04
LSS_G G	00000E65	R	04	NEQ_F F	00000C4F	R	04
LSS_H\$	00000E7E	R	04	NEQ_G\$	00000C74	R	04
LSS_H H	00000E73	R	04	NEQ_GCS	00000CC0	R	04
LSS_L\$	00000E3B	R	04	NEQ_GC GC	00000CAD	R	04
LSS_LUS	00000E48	R	04	NEQ_G G	00000C69	R	04
LSS_LU LU	00000E3E	R	04	NEQ_H\$	00000C82	R	04
LSS_L_L	00000E31	R	04	NEQ_HCS	00000CD6	R	04
LSS_P\$	000016B9	R	04	NEQ_HC HC	00000CC3	R	04
LSS_PP	000016A8	R	04	NEQ_H H	00000C77	R	04
LSS_TS	00000B43	R	04	NEQ_L\$	00000C4C	R	04
LSS_TFS	00001884	R	04	NEQ_L L	00000C42	R	04
LSS_TF TF	00001856	R	04	NEQ_P\$	0000167D	R	04
LSS_T T	00000B27	R	04	NEQ_P P	00001648	R	04
LSS_VT VT	00000B15	R	04	NEQ_RFAS	00001990	R	04
LSS_WS	00000E2E	R	04	NEQ_RFA RFA	0000197F	R	04
LSS_W W	00000E24	R	04	NEQ_SET\$	0000127E	R	04
MOD_LUS	000007DA	R	04	NEQ_SET1\$	0000124F	R	04
MOD_LU LU	000007CB	R	04	NEQ_SET11\$	00001256	R	04
MOD_LU_RET\$	000007E2	R	04	NEQ_SET2\$	00001264	R	04
MOD_L_C	000007B1	R	04	NEQ_SET3\$	00001268	R	04
MOD_L RETS	000007CA	R	04	NEQ_SET3_1\$	0000126F	R	04
MTHS_FLOOVEMAT	= 001682C4			NEQ_SET4\$	00001274	R	04
MTHS_FLOUNDMAT	= 001682CC			NEQ_SET4_1\$	0000127B	R	04
MTHS_UNDEXP	= 00168294			NEQ_SET_RET\$	00001286	R	04
MUL_BS	00000650	R	04	NEQ_SET_SET	0000122C	R	04
MUL_BUS	00000669	R	04	NEQ_TS	00000B74	R	04
MUL_BU_BU	00000653	R	04	NEQ_TFS	000018AA	R	04
MUL_B_B	00000649	R	04	NEQ_TF TF	00001887	R	04
MUL_DC_DC	000006EB	R	04	NEQ_T T	00000B58	R	04
MUL_D_D	000006BC	R	04	NEQ_VT VT	00000B46	R	04
MUL_FC_FC	000006CD	R	04	NEQ_WS	00000C3F	R	04
MUL_FIXED_FIXED	00001A72	R	04	NEQ_W_W	00000C35	R	04
MUL_FF	000006B7	R	04	NOT_B	00000F26	R	04
MUL_GC_GC	00000729	R	04	NOT_D	00000F3B	R	04
MUL_G_G	000006C1	R	04	NOT_GTRS	00001822	R	04
MUL_HC_HC	0000076D	R	04	NOT_L	00000F34	R	04
MUL_H_A	000006C7	R	04	NOT_LSSS	00001882	R	04

NOT_W	00000F2D	R	04	POWER_GC_L	000008DF	R	04
OCTALS	00001FBB	R	04	POWER_G_G	00000940	R	04
OCTAL_OVS	000020F4	R	04	POWER_G_L	00000887	R	04
OCTA_OVERFLOW\$	0000212C	R	04	POWER_H_H	00000954	R	04
OPERAND	= 00000048	R	03	POWER_H_L	0000089A	R	04
OPERATOR_ENTRY	= 00000004			POWER_L_L	00000856	R	04
ORT\$K_MAX_ROUT	= 0000011C			POWER_W_W	00000845	R	04
ORT\$K_MIN_ROUT	= 00000001			PRED_ENUM	000019EE	R	04
OR_B_B	00000F46	R	04	PRE_DECR_D	000013C4	R	04
OR_D_D	00000F67	R	04	PRE_DECR_L	000013B1	R	04
OR_L_L	00000F5C	R	04	PRE_DECR_LU	000013B1	R	04
OR_W_W	00000F51	R	04	PRE_DECR_TPTR	000013D8	R	04
OT\$SPOWCC	*****	X	04	PRE_INCR_D	0000135D	R	04
OT\$SPOWCDCD_R3	*****	X	04	PRE_INCR_L	0000134A	R	04
OT\$SPOWCDJ_R3	*****	X	04	PRE_INCR_LU	0000134A	R	04
OT\$SPOWGCG_R3	*****	X	04	PRE_INCR_TPTR	00001371	R	04
OT\$SPOWCGJ_R3	*****	X	04	QUAD_OVERFLOW\$	00001EFB	R	04
OT\$SPOWCJ	*****	X	04	REM_CUS	000007FD	R	04
OT\$SPOWDD	*****	X	04	REM_LU_LU	000007EE	R	04
OT\$SPOWDJ	*****	X	04	REM_LU_RET\$	00000805	R	04
OT\$SPOWDR	*****	X	04	REM_L_C	000007E3	R	04
OT\$SPOWGG	*****	X	04	REPORT_ERRORS	00001E61	R	04
OT\$SPOWGJ	*****	X	04	REPORT_ERROR1\$	00001EE5	R	04
OT\$SPOWHH_R3	*****	X	04	REPORT_ERROR2\$	00002116	R	04
OT\$SPOWHJ_R3	*****	X	04	REPORT_ERRORU1\$	00001F5F	R	04
OT\$SPOWII	*****	X	04	RESULT_ADDR	= 00000014		
OT\$POWJJ	*****	X	04	RESULT_DESC	00000040	R	03
OT\$POWRD	*****	X	04	RESULT_VALDESC	00000044	R	03
OT\$POWRJ	*****	X	04	RFA_OVERFLOW\$	00001E77	R	04
OT\$POWRR	*****	X	04	RIGHT_ARG	= 00000010		
PLISANDBIT	*****	X	00	ROUT_INDEX	= 00000008		
PLISCATBIT	*****	X	00	SAVE_OPERATOR_ENTRY	00000000	R	03
PLISCMPBIT	*****	X	00	SAVE_RESULT	00000004	R	03
PLISDIV_PK_LONG	*****	X	00	SCALE_ARG1\$	00001713	R	04
PLISNOTBIT	*****	X	00	SCALE_ARG2\$	00001705	R	04
PLISORBIT	*****	X	00	SCRATCH1	00000010	R	03
POSITIVE_MULD	000006AC	R	04	SCRATCH2	00000020	R	03
POSITIVE_MULR	000006A5	R	04	SETUP_PACKED_NUMBERS\$	000016D0	R	04
POST_DECR_D	00001407	R	04	SETUP_PACKED_RSBS\$	00001774	R	04
POST_DECR_L	000013F6	R	04	SETUP_PLI_AB1T1\$	00001920	R	04
POST_DECR_LU	000013F6	R	04	SETUP_PLI_AB1T2\$	00001954	R	04
POST_DECR_TPTR	000013F6	R	04	SETUP_PLI_CONT1\$	0000192B	R	04
POST_INCR_D	000013A0	R	04	SETUP_PLI_INTERFACES\$	000018FF	R	04
POST_INCR_L	0000138F	R	04	SETUP_PLI_RESULTS	0000195F	R	04
POST_INCR_LU	0000138F	R	04	SETUP_RSBS\$	0000196A	R	04
POST_INCR_TPTR	0000138F	R	04	SET_AND_RESULT	00000F23	R	04
POWER_DC_DC	0000099E	R	04	SET_NOT_RESULT	00000F42	R	04
POWER_DC_L	000008C6	R	04	SET_OR_RESULT	00000F72	R	04
POWER_D_D	0000092F	R	04	SET_QUOTIENT	00000487	R	04
POWER_D_F	0000090D	R	04	SET_RESULTS	00001E43	R	04
POWER_D_L	00000876	R	04	SET_RESULT1\$	00001ED4	R	04
POWER_FC_FC	00000968	R	04	SET_RESULT2\$	000020F7	R	04
POWER_FC_L	000008AD	R	04	SET_RESULTU1\$	00001F4E	R	04
POWER_F_D	0000091E	R	04	SET_SHIFT_RESULT	0000083E	R	04
POWER_F_F	000008FC	R	04	SET_XOR_RESULT	00000F88	R	04
POWER_F_L	00000865	R	04	SHIFT_BINARY\$	00001E35	R	04
POWER_GC_GC	000009D4	R	04	SHIFT_BINARY1\$	00001EC2	R	04

DBGPERMOP
Symbol table

K 2

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SHIFT_BINARY2\$	0000207D	R	04	SUB_TPTR_L	00001316	R	04
SHIFT_BINARYU1\$	00001F40	R	04	SUB_TPTR_TPTR	00001330	R	04
SHIFT_COUNT_NEGATIVE	000002DB	R	04	SUB_WS	000003B4	R	04
SHIFT_DECIMAL\$	00001E1D	R	04	SUB_WUS	000003BE	R	04
SHIFT_DECIMAL1\$	00001EA2	R	04	SUB_WU_WU	000003B7	R	04
SHIFT_DECIMAL2\$	00001FBE	R	04	SUB_W_Q	000003AD	R	C4
SHIFT_DECIMALU1\$	00001F26	R	04	SUCCE_ENUM	000019DA	R	04
SHIFT_HEXDECIMAL\$	00001E2E	R	04	SYSSUNWIND	*****	GX	04
SHIFT_HEXDECIMAL1\$	00001EB9	R	04	TEST_IMAGINARYD	00000CA0	R	04
SHIFT_HEXDECIMAL2\$	00002040	R	04	TEST_IMAGINARYF	00000C8C	R	04
SHIFT_HEXDECIMALU1\$	00001F39	R	04	TEST_IMAGINARYG	00000CB5	R	04
SHIFT_LEFT_LS	0000080B	R	04	TEST_IMAGINARYH	00000CCB	R	04
SHIFT_LEFT_LL	00000806	R	04	TOKENSK_BIN_INTEGER	= 0000000A		
SHIFT_OCTAL\$	00001E3C	R	04	TOKENSK_HEX_INTEGER	= 00000005		
SHIFT_OCTAL1\$	00001ECB	R	04	TOKENSK_INTEGER	= 00000004		
SHIFT_OCTAL2\$	000020BA	R	04	TOKENSK_OCT_INTEGER	= 0000000B		
SHIFT_OCTALU1\$	00001F47	R	04	TOKENCODE	= 0000000C		
SHIFT_RT_LS	0000081A	R	04	TOKEN_NAME	= 0000000C		
SHIFT_RT_LUS	00000842	R	04	TRAP_MSG_HANDLER	00001BBE	RG	04
SHIFT_RT_LU_LU	0000081D	R	04	TRUNCATE_THE_OTHERS	00001742	R	04
SHIFT_RT_LL	0000080E	R	04	UMBS	00000F92	R	04
SIZEOF_L	000012EB	R	04	UMLS	00000FA4	R	04
SRC_ARG	= 00000008			UMWS	00000F9B	R	04
SS\$_DECOVF	= 000004A4			UNARY_MINUS_B	00000F8C	R	04
SS\$_FLTDIV	= 00000494			UNARY_MINUS_D	00000FB4	R	04
SS\$_FLTDIV_F	= 000004BC			UNARY_MINUS_DC	00000FCB	R	04
SS\$_FLTOVF	= 0000048C			UNARY_MINUS_F	00000FB0	R	04
SS\$_FLTOVF_F	= 000004B4			UNARY_MINUS_FC	00000FC2	R	04
SS\$_FLTUND	= 0000049C			UNARY_MINUS_FIXED	00001A16	R	04
SS\$_FLTUND_F	= 000004C4			UNARY_MINUS_G	00000FB8	R	04
SS\$_INTDIV	= 00000484			UNARY_MINUS_GC	00000FD4	R	04
SS\$_INTOVF	= 0000047C			UNARY_MINUS_H	00000FBD	R	04
SS\$_NORMAL	= 00000001			UNARY_MINUS_HC	00000FDF	R	04
SS\$_OPCDEC	= 0000043C			UNARY_MINUS_L	00000F9E	R	04
SS\$_RESIGNAL	= 00000918			UNARY_MINUS LU	00000FA7	R	04
SS\$_ROPRAND	= 00000454			UNARY_MINUS_O	000019B6	R	04
STR\$COMPARE	*****	X	04	UNARY_MINUS_P	000015C9	R	04
STR\$CONCAT	*****	X	04	UNARY_MINUS_Q	00001999	R	04
STRING_TRUNCATE	000002E9	R	04	UNARY_MINUS_W	00000F95	R	04
SUB_B\$	000003A0	R	04	UNARY_PS	000015F4	R	04
SUB_BUS	000003AA	R	04	UNARY_PLUS_B	00000FEA	R	04
SUB_BU_BU	000003A3	R	04	UNARY_PLUS_D	00000FFA	R	04
SUB_B_B	00000399	R	04	UNARY_PLUS_DC	00001011	R	04
SUB_DC_DC	000003F7	R	04	UNARY_PLUS_F	00000FF6	R	04
SUB_D_D	000003DA	R	04	UNARY_PLUS_FC	00001008	R	04
SUB_FC_FC	000003EB	R	04	UNARY_PLUS_FIXED	00001A02	R	04
SUB_FIXED_FIXED	00001A58	R	04	UNARY_PLUS_G	00000FFE	R	04
SUB_F_F	000003D5	R	04	UNARY_PLUS_GC	0000101A	R	04
SUB_GC_GC	00000403	R	04	UNARY_PLUS_H	00001003	R	04
SUB_G_G	000003DF	R	04	UNARY_PLUS_HC	00001025	R	04
SUB_HC_HC	00000411	R	04	UNARY_PLUS_L	00000FF2	R	04
SUB_H_A	000003E5	R	04	UNARY_PLUS_O	000019AB	R	04
SUB_L\$	000003C8	R	04	UNARY_PLUS_P	000015E6	R	04
SUB_LUS	000003D2	R	04	UNARY_PLUS_Q	00001993	R	04
SUB_LU_LU	000003CB	R	04	UNARY_PLUS_W	00000FEE	R	04
SUB_L_L	000003C1	R	04	UNION_SET1\$	000012A7	R	04
SUB_P_P	00001418	R	04	UNION_SET2\$	000012B9	R	04

DBGPERMOP
Symbol table

UNION_SET3\$	000012BD	R	04
UNION_SET4\$	000012C5	R	04
UNION_SET_RET\$	000012D6	R	04
UNION_SET_SET	00001287	R	04
UNKNOWN_ROUT_INDEX	00001B42	R	04
UNKNOWN_SIGNAL	00001DD6	R	04
UQUAD_OVERFLOW\$	00001F75	R	04
WORK_OCTA	0000005C	R	03
XOR_L_L	00000F76	R	04
XOR_L_L_1\$	00000F81	R	04

+-----+
! Psect synopsis !
+-----+

PSECT name

PSECT name	Allocation	PSECT No.	Attributes
. ABS .	00000000 (0.)	00 (0.)	NOPIC USR CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE
\$ABSS	00000065 (101.)	01 (1.)	NOPIC USR CON ABS LCL NOSHR EXE RD WRT NOVEC BYTE
DBG\$PLIT	00000145 (325.)	02 (2.)	PIC USR CON REL LCL SHR EXE RD NOWRT NOVEC BYTE
DBG\$OWN	0000006C (108.)	03 (3.)	PIC USR CON REL LCL NOSHR NOEXE RD WRT NOVEC LONG
DBG\$CODE	0000212F (8495.)	04 (4.)	PIC USR CON REL LCL SHR EXE RD NOWRT NOVEC BYTE

+-----+
! Performance indicators !
+-----+

Phase

Phase	Page faults	CPU Time	Elapsed Time
Initialization	10	00:00:00.12	00:00:00.39
Command processing	83	00:00:00.81	00:00:03.75
Pass 1	536	00:00:22.40	00:01:11.19
Symbol table sort	7	00:00:02.65	00:00:12.27
Pass 2	535	00:00:09.06	00:00:36.38
Symbol table output	1	00:00:00.52	00:00:01.27
Psect synopsis output	1	00:00:00.03	00:00:00.03
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	1168	00:00:35.59	00:02:05.29

The working set limit was 1500 pages.

137763 bytes (270 pages) of virtual memory were used to buffer the intermediate code.

There were 90 pages of symbol table space allocated to hold 1722 non-local and 36 local symbols.

4104 source lines were read in Pass 1, producing 64 object records in Pass 2.

17 pages of virtual memory were used to define 16 macros.

+-----+
! Macro library statistics !
+-----+

Macro library name

\$255\$DUA28:[DEBUG.OBJ]DBGMSG.MLB;1	1
\$255\$DUA28:[SYSLIB]STARLET.MLB;2	12
TOTALS (all libraries)	13

Macros defined

1264 GETS were required to define 13 macros.

DBGPERMOP
VAX-11 Macro Run Statistics

M 2

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There were no errors, warnings or information messages.

MACRO/LIS=LI\$S:DBGPERMOP/OBJ=OBJ\$:DBGPERMOP MSRC\$S:DBGPERMOP/UPDATE=(ENH\$S:DBGPERMOP)+LIB\$S:DBGMSG/LIB

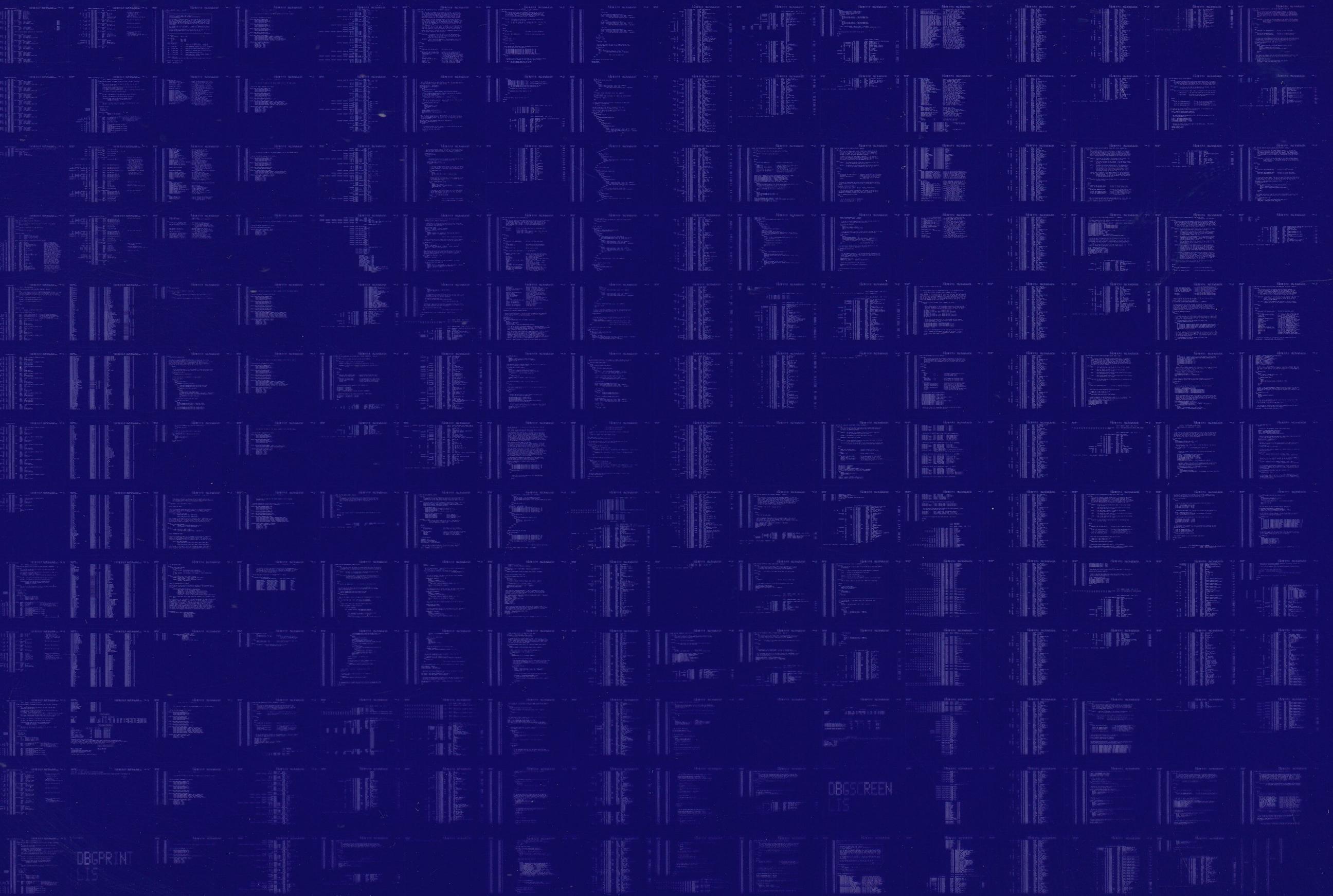
0091 AH-BT13A-SE
VAX/VMS V4.0

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DBGPERMOP
LIS

0092 AH-BT13A-SE
VAX/VMS V4.0

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DBGPRINT
LIS

DBGSCREEN
LIS