Firefox Workstation I/O Module Functional Specification

Revision 3.0

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Revision History

Date	Version	Content/Changes
3 Nov 87	3.0	Listed cover assembly requirements Miscellaneous clarifications for design review questions Corrected cover connector pinout Corrected manufacturing-mode polarity in FBICSR Added IOCSR<MRUN> bit Correct access of IOCSR to be word only Added module-reset description Added ESAR test pattern values
17 Aug 87	2.1	Separated disk and network interfaces Network buffer address changed Deleted IOCSR<RSTSSC,RSTDSK,RSTNET,RSTSER> bits Cover-status outputs reduced to 5 bits Power-up MRESET assertion reduced to 70 ms Added section listing resource access times
30 Apr 87	2.0	Dropped CDMA Selected DZ serial interface
27 Jan 87	1.1	Integrated with system specification
24 Jan 87	1.0	First external release
10 Jan 87	0.0	Preliminary draft

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7. Firefox Workstation I/O Module (L2003)

This chapter contains the functional specification for the Firefox workstation I/O module (L2003). It describes the functionality of the module, presents the specific implementation that achieves that function, and lists required software initialization and programming guidelines. It does not describe the detailed function of VLSI devices on the module; this information can be found in the appendices of the *Firefox Designer's Guide*.

The Firefox workstation I/O module implements all of the workstation I/O and support functions in a single L-series-quad module. These functions are as follow:

- Time-of-year clock
- Interval timers
- 1-Kbyte battery-backed-up (BBU) RAM
- Base workstation ROM
- Serial lines for keyboard, mouse/tablet, modem, and printer/console
- Disk/tape interface for RF/TF series drives
- Network interface for ThickWire Ethernet
- Software-controlled device-reset register
- M-bus interface
- M-bus MRESET logic
- M-bus MCLKI interval clock

The L2003 requires a cover assembly to implement the serial line EIA drivers, receivers, and connectors; an Ethernet transceiver cable connector and/or ThinWire Ethernet transceiver; a hexadecimal-digit status display; and a battery for the 1-Kbyte BBU RAM and time-of-year clock. Detailed descriptions of these functions can be found in the *Firefox Workstation I/O Cover Module Functional Specification*.

The L2003 has been designed specifically for use in Firefox SMP systems. All module devices are accessible from the M-bus to any M-bus master. Nonatomic operations on VLSI device interfaces may require operating system interlocks.

A Firefox workstation must contain the L2003 or an equivalent module that implements the logic for the M-bus MCLKI and MRESET signals. There is no logical or electrical constraint that prohibits multiple L2003 modules in the workstation, although such configurations require some software coordination as discussed in the section on programming examples later in this chapter.

7.1. Functionality

The following is a description of the functionality of the L2003 without specific reference to the actual implementation, which is discussed in Section 7.2 of this chapter.

7.1.1. Time-of-Year Clock

The L2003 implements a time-of-year clock compatible with the VAX SRM specification.

The time-of-year clock is a single longword register that represents an unsigned 32-bit binary counter. The least significant bit of the counter represents a resolution of 10 milliseconds.

The counter has battery backup that will sustain its operation for at least 100 hours. The battery is recharged automatically. If the battery has failed, the counter clears at workstation reset.

The time-of-year clock register is accessible to software via an I/O-space reference.

7.1.2. Interval Timers

The L2003 implements an interval timer compatible with the VAX SRM specification.

The Interval Count register is a single longword register that represents an unsigned 32-bit binary counter. The least significant bit of the counter represents a resolution of one microsecond. When the interval count overflows, the interval timer generates a vectored interrupt under control of the Interval Clock Control and Status register.

The Interval Count register, Next Interval Count register, and Interval Clock Control and Status register are accessible to software through I/O-space references.

7.1.3. Battery-Backed-Up RAM

The L2003 implements 1 Kbyte of battery-backed-up RAM with byte, word, and longword access that allows storage of workstation configuration parameters and the setting of soft console switches. It is accessible to software through I/O-space references.

7.1.4. Base Workstation ROM

The L2003 implements 256 Kbytes of ROM for use as base workstation ROM. The ROM, which is in sockets, is accessible to software through I/O-space references.

7.1.5. Serial Interface

The L2003 implements four asynchronous serial lines for use by a keyboard, mouse/tablet, modem, and printer/console with a DZ-compatible software interface. The serial lines which are compatible with the LK201 keyboard, the VSXXX-AA mouse, and the VSXXX-AB tablet, conform to RS-423 electrical specifications.

The keyboard, mouse/tablet, and printer/control serial lines are data-leads-only (RX/TX). The modem serial line supports the CTS, RTS, DTR, DSR, RI, CD, DSRS, SPDMI, TMI, and LLPBK asynchronous modem control signals.

The baud rate of the serial lines is independently programmable to 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, or 9600 bits per second.

The character width of the serial lines is independently programmable to 5, 6, 7, or 8 bits. Parity of the serial lines is independently programmable to odd, even, or none. Stop bit length of the serial lines is independently programmable to 1 or 1.5/2 bits.

The serial interface has a shared, 64-character, receiver FIFO to buffer serial line input. The serial interface supports generation of vectored interrupts after character reception/transmission.

When operating in console mode, as specified by a bit in the IOCSR, break conditions on the printer/console serial line assert the M-bus MHALT signal.

The serial interface registers are accessible via I/O-space references.

7.1.6. Disk/Tape Interface

The L2003 implements a disk/tape interface compatible with the RF/TF series disk/tape drives.

The disk/tape interface uses signal levels and conventions for the physical link as specified by DIGITAL Small Storage Interconnect (DSSI) architecture. The interface supports data transfers on the DSSI bus at the maximum DSSI bandwidth of 4 Mbytes/sec without processor intervention. Because of latency constraints, the DSSI interface transfers data only between DSSI devices and a local 128-Kbyte RAM disk buffer. Because of implementation constraints, the RAM buffer is not parity protected. Operating system device drivers must explicitly copy data between the RAM buffer and host memory. Processors can achieve 2-Mbyte/sec transfer rates with block-move instructions. The disk/tape interface generates vectored interrupts in response to completion of DSSI packet transmission.

The DSSI cable connector position allows cable routing entirely within the EMI enclosure of the Firefox cabinet.

The disk/tape interface control and status registers, and the local disk buffer, are accessible to software through I/O-space references.

7.1.7. Network Interface

The L2003 implements a network interface compatible with the physical-link specification for the DIGITAL ThickWire Ethernet, as well as the data-link specification for DIGITAL ThickWire Ethernet and IEEE 802.3.

The network interface supports data transfers at the maximum signaling rate of 10 Mbits/sec. Because of latency constraints, the network interface only transfers data between the Ethernet and a local 128-Kbyte RAM network buffer. Because of implementation constraints, the RAM buffer is not parity protected. Operating system device drivers must explicitly copy data between the RAM buffer and host memory. Processors can achieve 2-Mbyte/sec transfer rates with block-move instructions. The network interface generates vectored interrupts in response to completion of packet reception or transmission. Note that the network buffer and disk buffer are two separate buffers, each 128 Kbytes in size.

The network interface has a fixed 48-bit station address in ROM. The ROM is in a socket.

The network interface Control and Status registers, the local network buffer, and the station-address ROM are accessible to software through I/O-space references.

7.1.8. IOCSR

The L2003 implements the IOCSR which allows hardware reinitialization of the entire Firefox workstation, controls whether the L2003 drives the M-bus MCLKI signal, controls illumination of the front-panel system-running indicator, specifies whether the printer/console serial line is in console mode, and provides access to the Ethernet station-address ROM. The IOCSR is accessible via I/O-space references.

7.1.9. M-Bus Interface

The L2003 implements an M-bus interface that conforms to the *Firefox Workstation M-Bus Specification.*

In addition to satisfying the M-bus interface requirements, the M-bus interface also supports the following:

- Slave access to the Control and Status registers of the time-of-year clock, interval clock, interval timer, serial interface, disk/tape interface, network interface, battery-backed-up RAM, local disk and network buffers, base workstation ROM, and the IOCSR
- Generation and acknowledgement of interrupts for the interval timers, serial interface, disk/tape interface, and network interface

The serial interface, disk/tape interface, network interface, local disk and network buffers, base workstation ROM, and IOCSR reside in the 32-Mbyte I/O-space region associated with the M-bus slot of the L2003. The time-of-year clock, interval clock, interval timers, and battery-backed-up RAM reside at a fixed address in I/O space.

7.1.10. M-Bus MRESET Logic

The L2003 implements the logic to drive the M-bus MRESET signal during powerup, when the MDCOK signal is deasserted, or under software control via the IOCSR. The minimum MRESET assertion pulse width is 16 M-bus clock cycles. After powerup, the logic asserts MRESET for at least 70 milliseconds.

7.1.11. M-Bus MCLKI Interval Clock

The L2003 implements an interval clock that generates a 100-Hz square wave onto the M-bus MCLKI signal for use by processors as an interval-clock interrupt. The L2003 must be explicitly enabled to drive the M-bus MCLKI signal via the IOCSR.

7.1.12. Status-Indicator Outputs

The L2003 supports a 5-bit status indicator on its cover. The status-indicator value is set by a register that is accessible via I/O space. The most significant bit of the status output is also displayed via a green LED on the L2003 itself. The LED is automatically turned off by workstation reset (M-bus MRESET asserted).

7.1.13. Manufacturing-Mode Inputs

From its cover, the L2003 supports a 2-bit manufacturing-mode specification with external loopback connectors or jumpers. The manufacturing mode is available in a register that is accessible via I/O space.

7.1.14. External Connections

The L2003 connects to the module cover assembly through a 50-conductor ribbon cable for the following:

- Keyboard serial line
- Mouse/tablet serial line
- Modem serial line
- Printer/console serial line
- Ethernet transceiver
- Status-indicator outputs
- Manufacturing-mode inputs

The L2003 has a 50-pin ribbon connector for the DSSI disk/tape cable and a backplane connection to the M-bus.

7.1.15. Addressing

Table 7-1 lists the address regions of the L2003. In the table, the SLOT value is the number of the M-bus slot in which the module resides. For example, a module in M-bus slot 1 has its IOCSR at M-bus address 92800000#16. As discussed in the sections that follow, the FBIC range-decoder function must be programmed to access the System Support Chip (SSC) registers.

Table 7-1: L2003 Address-Space Map

Name	VAX Address	M-Bus Address
SSC Registers	20140000#16 . . . 201407FF#16	80140000#16 . . . 801407FF#16
Disk Registers	3X000000#16 . . . 3X00006F#16	9X000000#16 . . . 9X00006F#16
Network Registers	3X200000#16 . . . 3X200007#16	9X200000#16 . . . 9X200007#16
Disk Buffer	3X400000#16 . . . 3X41FFFF#16	9X400000#16 . . . 9X41FFFF#16
Serial Registers	3X600000#16 . . . 3X60000F#16	9X600000#16 . . . 9X60000F#16
IOCSR	3X800000#16 . . . 3X80007F#16	9X800000#16 . . . 9X80007F#16
Network Buffer	3XA00000#16 . . . 3XA1FFFF#16	9XA00000#16 . . . 9XA1FFFF#16
Base System ROM	3YE00000#16 . . . 3YE7FFFF#16	9YE00000#16 . . . 9Y7FFFFF#16
FBIC Registers	3YFFFFC4#16 . . . 3YFFFFFF#16	9YFFFFC4#16 . . . 9YFFFFFF#16

X = 2*SLOT
Y = 2*SLOT+1

7.1.16. Interrupt Priority Levels

Table 7-2 lists the interrupt priority levels of the L2003. As discussed in the sections that follow, the FBIC device-interrupt function must be programmed to enable disk, network, and serial interrupts and to specify the interrupt vector.

Table 7-2: L2003 Interrupt-Priority-Level (IPL) Map

IPL	Source
14#16	Disk interface and SSC
15#16	Network interface
16#16	Serial interface
17#16	FBIC MEMERR

7.1.17. L2003 Power Requirements

Table 7-3 lists the preliminary power consumption estimates for the L2003. The –12-volt supply is required only if the I/O cover module used with the L2003 does not implement a charge pump to generate the negative supply.

Table 7-3: L2003 Preliminary Power Estimates

Supply (V)	Typical Current (A)	Max Current (A)	Max Power (W)
+5	5.6	9.2	46
+12	0.7	1.3	16
–12	0.1	0.2	2

7.2. Implementation

The following is a description of the implementation of the L2003 used to achieve the specified functionality of workstation support services and workstation I/O. Figure 7-1 shows a block diagram of the L2003.

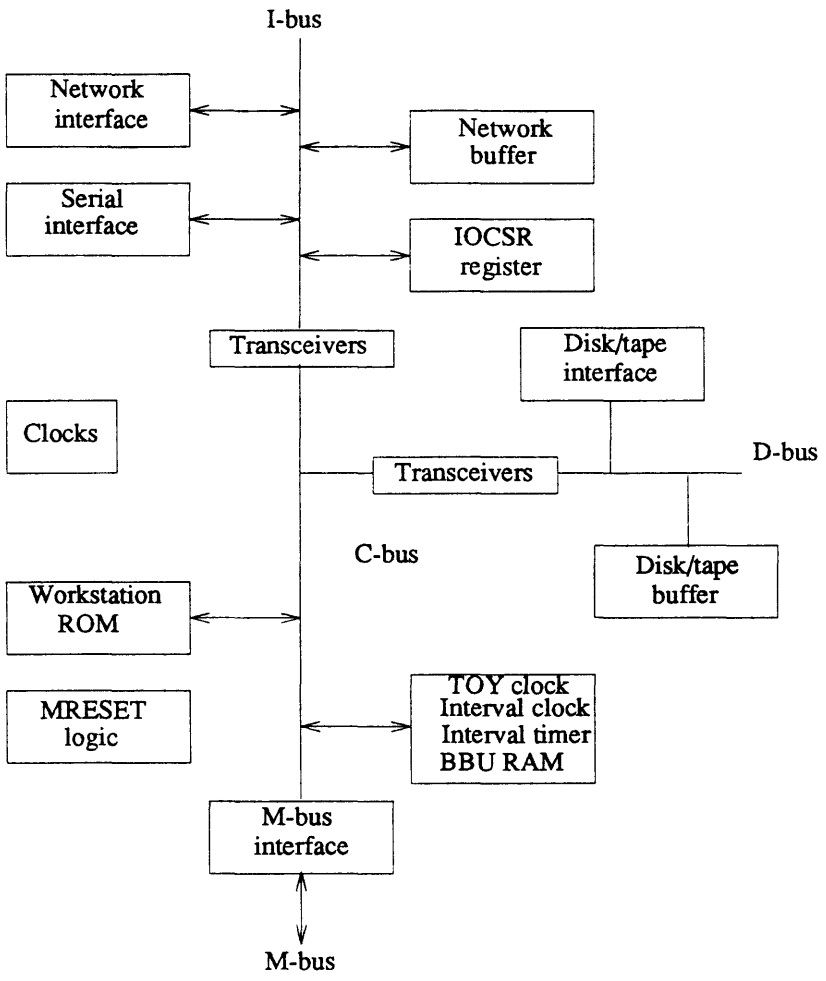

Figure 7-1: Firefox Workstation I/O Module Block Diagram

The only means to achieve the specified functionality of workstation support services and workstation I/O in the 70 square inches of logic area available on a single L-series-quad module is through VLSI interface chips. For example, the System Support Chip (SSC) of the CVAX chipset implements the time-of-year clock, interval clock, interval timer, and battery-backed-up (BBU) RAM.

In the ideal case, each functional block of the L2003 reduces to a single VLSI controller chip, which attaches directly to a CVAX pin-bus, and a transceiver chip, which interfaces to the device's physical media. The L2003 falls short of this goal for the serial, disk/tape, and network functional blocks.

There is no single-chip DZ serial interface. The interface is constructed from the DC7085 gate array and approximately five SSI/MSI interface chips. In addition, the DC7085 requires external, vectored-interrupt logic.

For the disk/tape interface, the SII gate array implements all of the required control functions but is not directly CVAX pin-bus compatible. For the network interface, the LANCE (Local Area Network Controller For Ethernet) chip implements all of the required control functions, but is not directly CVAX pin-bus compatible. Incompatibility arises from stringent latency constraints, the 16-bit data bus, lack of bus-cycle retry capability when operating as a bus master, and lack of vectored-interrupt logic.

The FBIC M-bus interface implements the vectored-interrupt logic for the serial, disk/tape, and network interfaces.

The following sections describe in further detail the features of each of the functional blocks that compose the L2003, including the features of the chip; connectivity to busses, interrupt signals, and reset signals; and CSR/RAM/ROM addressing. These sections are intended to describe the specific use and addressing of the VLSI controllers on the L2003 and not to completely describe each chip's function, control and status registers, and programming. For information on specific chips, refer to the chip specifications included in the appendices to the *Firefox Designers' Guide*.

7.2.1. Time-of-Year Clock, Interval Clock, Interval Timers, BBU RAM

The System Support Chip (SSC), DC511, implements the time-of-year clock, interval clock, interval timer, and battery-backed-up (BBU) RAM functional blocks of the L2003. The SSC requires a 25.6 KHz oscillator for the time-of-year clock.

7.2.1.1. Device Features

The SSC implements the workstation support functions listed here. Items marked with an asterisk indicate features used by the L2003. All other features are superseded by other devices or not applicable; software must not use unsupported features.

- 100-Hz interval clock*
- VAX-SRM-compatible time-of-year clock*
- 2 VAX-SRM-compatible programmable timers*
- 1 Kbyte of battery-backed-up RAM*
- VAX-SRM-compatible console UARTs (Universal Asynchronous Receiver/Transmitters)
- Support for 8-, 16-, or 32-bit external ROM
- Bus-reset support
- Programmable bus-timeout support
- Halt arbitration logic
- 2 programmable address-decode strobes
- 4-bit output port

The interval-clock output drives the M-bus MCLKI signal when the IOCSR<CLKIEN> bit is set.

The time-of-year (TOY) clock consists of a single 32-bit register that is accessible via I/O-space references. The clock, which can generate a vectored interrupt when it overflows, is powered by a battery in the module cover assembly when AC power fails.

The two interval timers are each controlled by four registers that are accessible through I/O-space references. Each timer can generate a vectored interrupt when it overflows.

The SSC contains 1 Kbyte of battery-backed-up RAM that is accessible via I/O reads and writes.

The Control and Status registers for these functions are accessible only via I/O-space references; IPR access to the registers is not supported.

Detailed descriptions of the operation and register formats of the time-of-year clock, interval clock, and interval timers can be found in Appendix I, "SSC Chip Specification," in the *Firefox Designers' Guide*.

7.2.1.2. Bus Connection

The SSC resides on the C-bus. The time-of-year clock, interval clock, interval timers, and battery-backed-up RAM are accessible through I/O-space reads and writes on the M-bus. The SSC is a bus slave; it never initiates C-bus transactions.

7.2.1.3. Interrupts

The SSC interrupt output connects to the C-bus IRQ0 signal. Software must program IPL14 interrupts for the SSC. The SSC asserts its IRQ output when the time-of-year clock or interval timer interrupts. If the SSC is asserting its IRQ output and a C-bus interrupt-acknowledge transaction for level 14 occurs, the SSC responds with a vector that is specific to the highest priority internal device generating an interrupt.

7.2.1.4. External Connection

The SSC receives its battery power from the cover connector.

7.2.1.5. SSC Address Map

Table 7-4 lists the addresses for the internal registers of the SSC. All of these registers are longword aligned and must always be referenced as longwords. As can be seen in Table 7-4 for example, to read the TOY clock register, a VAX issues a longword read to address 2014006C#16. Byte or word accesses yield unpredictable results. The RAM can be accessed via byte, word, or longword references. As discussed in Subsection 7.1.9, "M-Bus Interface," the FBIC address decoder must be programmed to respond to M-bus addresses 8014XXXX#16 before the SSC is accessible. Registers with unsupported access should not be referenced because the L2003 does not use these functions of the SSC.

Table 7-4: SSC Address Map

Name	VAX Address	M-Bus Address	Access
SSC Base Address Register	20140000#16	80140000#16	R/W
SSC Config. register	20140010#16	80140010#16	R/W
SSC TOY Clock Register	2014006C#16	8014006C#16	R/W
SSC Console Strg Rcvr Status	20140070#16	80140070#16	Unsupported
SSC Console Strg Rcvr Data	20140074#16	80140074#16	Unsupported
SSC Console Strg Xmit Status	20140078#16	80140078#16	Unsupported
SSC Console Strg Xmit Data	2014007C#16	8014007C#16	Unsupported
SSC Console Rcvr Ctrl/Status	20140080#16	80140080#16	Unsupported
SSC Console Rcvr Data Buffer	20140084#16	80140084#16	Unsupported
SSC Console Xmtr Ctrl/Stat	20140088#16	80140088#16	Unsupported
SSC Console Xmtr Data Buffer	2014008C#16	8014008C#16	Unsupported
SSC Timer 0 Control Register	20140100#16	80140100#16	R/W
SSC Timer 0 Interval Register	20140104#16	80140104#16	R/W
SSC Timer 0 Nxt Int Register	20140108#16	80140108#16	R/W
SSC Timer 0 Interrupt Vector	2014010C#16	8014010C#16	R/W
SSC Timer 1 Control Register	20140110#16	80140110#16	R/W
SSC Timer 1 Interval Register	20140114#16	80140114#16	R/W
SSC Timer 1 Nxt Int Register	20140118#16	80140118#16	R/W
SSC Timer 1 Interrupt Vector	2014011C#16	8014011C#16	R/W
SSC Channel 0 Match Register	20140130#16	80140130#16	Unsupported
SSC Channel 0 Mask Register	20140134#16	80140134#16	Unsupported
SSC Channel 1 Match Register	20140140#16	80140140#16	Unsupported
SSC Channel 1 Mask Register	20140144#16	80140144#16	Unsupported
SSC RAM Start	20140400#16	80140400#16	R/W
SSC RAM End	201407FF#16	801407FF#16	R/W

7.2.2. Serial Lines

The serial interface consists of the DC7085 DZ gate array, one 1K-by-4 static RAM for the receiver FIFO, one octal driver, one octal receiver, one modem status signal buffer, one 15.2064 MHz oscillator, and miscellaneous SSI/MSI control logic.

7.2.2.1. Device Features

The DC7085 gate array implements a DZQ11-compatible quad serial line interface. Serial line 0 is for the keyboard, serial line 1 for the mouse/tablet, serial line 2 for the modem, and serial line 3 for the printer/console.

For a detailed description of the operation and register formats of the DC7085, see Appendix K, "DZ11-DC7085 Chip Specification," in the *Firefox Designers' Guide*.

7.2.2.2. Bus Connection

The DC7085 connects to the I-bus, and operates strictly as a slave device.

7.2.2.3. Interrupts

The DC7085 interrupt signal connects to the FBIC DEVIRQ2 pin. The FBIC generates and acknowledges IPL16 interrupts in response to assertion of the DEVIRQ2 pin.

Because the FBIC DEVIRQ2 input is falling-edge sensitive, whereas the DC7085 interrupt output is level active, the device driver must disable and reenable DC7085 interrupts at the end of the interrupt service routine to prevent loss of new interrupts from the DC7085 generated during the interrupt service routine.

7.2.2.4. External Connections

The DC7085 serial line signals connect to the L2003 cover assembly via a 50-conductor ribbon cable.

7.2.2.5. DC7085 Address Map

Table 7-5 lists the I-bus address offset of the registers within the DC7085. The L2003 base address must be added to the offset to compute the actual address. All registers are longword aligned. Registers must be accessed with word references; byte and longword accesses yield unpredictable results. For example, to read the MSR register when the L2003 is in backplane slot 3, a VAX issues a word read to address 3660000C#16.

Table 7-5: DC7085 CSR I-bus Offsets

Name	Offset	R/W
CSR	00600000#16	R/W
RBUF	00600004#16	R
LPR	00600004#16	W
TCR	00600008#16	R/W
MSR	0060000C#16	R
TDR	0060000C#16	W

7.2.3. Disk/Tape Interface

The disk/tape interface, which connects DSSI RF/TF-series drives to a Firefox workstation, consists of the SII (DC7061) gate array, a DXX (DC563) transceiver, a 16-bit address register/counter, a local 128-Kbyte RAM disk buffer, and miscellaneous SSI/MSI glue logic for the SII gate array and disk buffer.

7.2.3.1. Device Features

The SII implements the physical- and link-level layers of DSSI. Communication with RF/TF drives is via linked lists of command blocks stored in the disk buffer and host interrupts. The SII automatically performs all the DSSI bus operations necessary to transfer DSSI packets between the disk buffer and an RF/TF drive.

The SII supports both an arbitrated and a nonarbitrated host bus. The L2003 supports only the arbitrated bus mode, and software must always program the SII for operation in this mode. All of the control and data buffers required by the SII reside in the disk buffer. The SII accepts host bus transactions to access its control and status registers between each of its disk-buffer transactions.

The SII has a 16-bit data bus. SSI/MSI logic interfaces the SII to the 32-bit L2003 D-bus. The SII uses an external 16-bit counter to perform block transfers to and from its buffer. By issuing a single address and then performing multiple data transfers, the SII requires less than 50 percent of the disk buffer's bandwidth. The disk buffer is not parity protected because the SII does not support parity on its host interface. SII register data is always transferred on D-bus DAL<15:0>.

For a detailed description of the operation and register formats of the SII, see Appendix J, "SII Chip Specification," in the *Firefox Designers' Guide*.

The DXX (DC563) DSSI transceiver implements high-power 100 mA open-drain drivers and high-noise-immunity receivers for the DSSI cable and also implements decoding logic for the DSSI physical ID during DSSI arbitration. The DXX's SII port uses conventional TTL signal levels.

7.2.3.2. Bus Connection

The SII connects to the D-bus for access to its disk buffer. The D-bus has sufficient bandwidth to support the peak DSSI bus bandwidth of 4 Mbytes/sec. For host access to the SII's CSRs and to the disk buffer, C-bus transactions are forwarded onto the D-bus under control of the SII. The SII never functions as a C-bus master.

7.2.3.3. Interrupts

The SII interrupt signal connects to the FBIC DEVIRQ0 pin. The FBIC generates and acknowledges IPL14 interrupts in response to assertion of the DEVIRQ0 pin.

Because the FBIC DEVIRQ0 input is falling-edge sensitive, whereas the SII interrupt output is level active, the device driver must disable and reenable SII interrupts at the end of the interrupt service routine to prevent loss of new interrupts from the SII generated during the interrupt service routine.

7.2.3.4. External Connection

The SII connects to a DSSI 50-conductor ribbon cable through the DXX transceiver. The cable connector is mounted on the L2003 such that the cable can be routed entirely within the EMI confines of the workstation cabinet.

7.2.3.5. SII Address Map

Table 7-6 lists the D-bus address offset of the registers within the SII. To compute the actual address, the L2003 base address must be added to the offset. All registers are longword aligned. Registers must be accessed with word references; for example, to write the ILP register when the L2003 is in backplane slot 3, a VAX issues a word write to address 36000040#16. Byte and longword accesses yield unpredictable results.

Table 7-6: SII CSR D-bus Offsets

Name	Offset	R/W
SDB	00000000#16	R/W
SC1	00000004#16	R/W
SC2	00000008#16	R/W
CSR	0000000C#16	R/W
ID	00000010#16	R/W
SLCSR	00000014#16	R/W
DESTAT	00000018#16	R/O
DSTMO	0000001C#16	R/W
DATA	00000020#16	R/W
DMCTRL	00000024#16	R/W
DMLOTC	00000028#16	R/W
DMADDRL	0000002C#16	R/W
DMADDRH	00000030#16	R/W
DMABYTE	00000034#16	R/W
STLP	00000038#16	R/W
LTLP	0000003C#16	R/W
ILP	00000040#16	R/W
DSCTRL	00000044#16	R/W
CSTAT	00000048#16	R/W1TC
DSTAT	0000004C#16	R/W1TC
COMM	00000050#16	R/W
DICTRL	00000054#16	R/W
CLOCK	00000058#16	W/O
BHDIAG	0000005C#16	R/W
SIDIAG	00000060#16	R/O
DMDIAG	00000064#16	R/O
MCDIAG	00000068#16	R/O
IIDIAG	0000006C#16	R/W

The disk/tape interface disk buffer occupies offset range 00400000#16 through 0041FFFF#16.

7.2.4. Network Interface

The network interface connects the Firefox workstation to a DIGITAL ThickWire Ethernet. The network interface consists of an AM7990 Local Area Network Controller for Ethernet (LANCE), an AM7992 Serial Interface Adapter (SIA), a local 128-Kbyte RAM network buffer, miscellaneous SSI/MSI glue logic for the LANCE, and a 32-by-8-bit Ethernet station address ROM.

7.2.4.1. Device Features

The LANCE and its related components implement most of the logic necessary for a network interface. These features include a self-contained DMA engine to transfer packets between the Ethernet cable and linked lists of packet buffers, packet error reporting, and address-filtering capabilities.

The LANCE communicates with the host through memory data structures and interrupts. These data structures, known as transmit and receive descriptor rings, are organized as ring buffers with each entry in a ring buffer containing status of that entry, current ownership of the buffer entry, and the location of the data buffer. The LANCE routinely polls the transmit descriptor ring for outgoing packets when there are no incoming packets.

Because the LANCE is not CVAX pin-bus compatible, it resides on the I-bus along with its network buffer. All of the control and data buffers the LANCE requires reside in the network buffer. The LANCE accepts

host bus transactions to access its control and status registers between each of its network buffer transactions.

The LANCE has a 16-bit data bus. SSI/MSI logic interfaces the LANCE to the 32-bit L2003 I-bus. The network buffer is not parity protected because the LANCE does not support parity on its host interface. LANCE register data is always transferred on I-bus DAL<15:0>.

For a detailed description of the operation and register formats of the LANCE, see Appendix L, "Lance Chip Specification," in the *Firefox Designers' Guide*.

7.2.4.2. Bus Connection

The LANCE chip connects with and arbitrates for access to the I-bus, which has sufficient bandwidth to support the peak Ethernet bandwidth of 10 Mbits/sec. For host access to the LANCE's CSRs and to the network buffer, C-bus transactions are forwarded onto the I-bus under control of a PAL state machine. The LANCE never functions as a C-bus master.

7.2.4.3. Interrupts

The LANCE interrupt signal connects to the FBIC DEVIRQ1 pin. The FBIC generates and acknowledges IPL15 vectored interrupts in response to assertion of the DEVIRQ1 pin.

Because the FBIC DEVIRQ1 input is falling-edge sensitive, whereas the LANCE interrupt output is level active, the device driver must disable and re-enable LANCE interrupts at the end of the interrupt service routine to prevent loss of new interrupts generated from the LANCE during that routine.

7.2.4.4. External Connection

The ThickWire transceiver connects to the L2003 cover assembly via a 50-conductor ribbon cable.

7.2.4.5. LANCE Address Map

Table 7-7 lists the I-bus address offset of the LANCE registers. To compute the actual address, the L2003 base address must be added to the offset. All registers are longword aligned and must be accessed with word references; for example, to read the RDP register when the L2003 is in backplane slot 3, a VAX issues a word read to address 36200000#16. Byte and longword accesses yield unpredictable results.

Table 7-7: LANCE CSR I-Bus Offsets

Name	Offset	R/W
RDP	00200000#16	R/W
RAP	00200004#16	R/W

The network interface network buffer occupies offset range 00A00000#16 through 00A1FFFF#16.

7.2.4.6. Station Address ROM

The L2003 implements an Ethernet Station Address ROM (ESAR) so software can determine the workstation's Ethernet address. The ROM is organized as 32 locations by 8 bits in width. In addition to the Ethernet address, the ROM contains checksum and test pattern data. The Ethernet Station Address ROM is accessible via the IOCSR<ESAR> field. Table 7-8 lists the address offsets from the IOCSR base address of the locations contained within the Ethernet Station Address ROM. All locations are aligned on longword boundaries.

Table 7-8: Station Address ROM Offsets

Name			Offset	Value
Address	Octet	0	00000002#16	
"	"	1	00000006#16	
"	"	2	0000000A#16	
"	"	3	0000000E#16	
"	"	4	00000012#16	
"	"	5	00000016#16	
Chksum	Octet	1	0000001A#16	
"	"	2	0000001E#16	
"	"	2	00000022#16	
"	"	1	00000026#16	
Address	Octet	5	0000002A#16	
"	"	4	0000002E#16	
"	"	3	00000032#16	
"	"	2	00000036#16	
"	"	1	0000003A#16	
"	"	0	0000003E#16	
Address	Octet	0	00000042#16	
"	"	1	00000046#16	
"	"	2	0000004A#16	
"	"	3	0000004E#16	
"	"	4	00000052#16	
"	"	5	00000056#16	
Chksum	Octet	1	0000005A#16	
"	"	2	0000005E#16	
TEST	Pattern	0	00000062#16	FF#16
"	"	1	00000066#16	00#16
"	"	2	0000006A#16	55#16
"	"	3	0000006E#16	AA#16
"	"	4	00000072#16	FF#16
"	"	5	00000076#16	00#16
"	"	6	0000007A#16	55#16
"	"	7	0000007E#16	AA#16

For example, to read the second octet of the station address when the L2003 is in backplane slot 3, a VAX issues a byte read to address 36800006#16.

7.2.5. I/O Control and Status Register (IOCSR)

The IOCSR provides a means by which software can reset the entire workstation. It also provides access to the Ethernet Station Address ROM, controls whether the L2003 drives the M-bus MCLKI signal, controls assertion of the backplane MRUN signal, and specifies whether the printer/console serial line is in console mode. The IOCSR resides at offset 00800002#16 on the I-bus; for example, to read the IOCSR when the L2003 is in slot 3, a VAX issues a word read to address 36800002#16. The IOCSR only supports byte and word access; longword access yields unpredictable results. Upon powerup, the IOCSR is initialized with all writable bits (CNSL, MRUN, CLKIEN, and RSTWS) 0.

The bit configuration of the IOCSR appears in Figure 7-2.

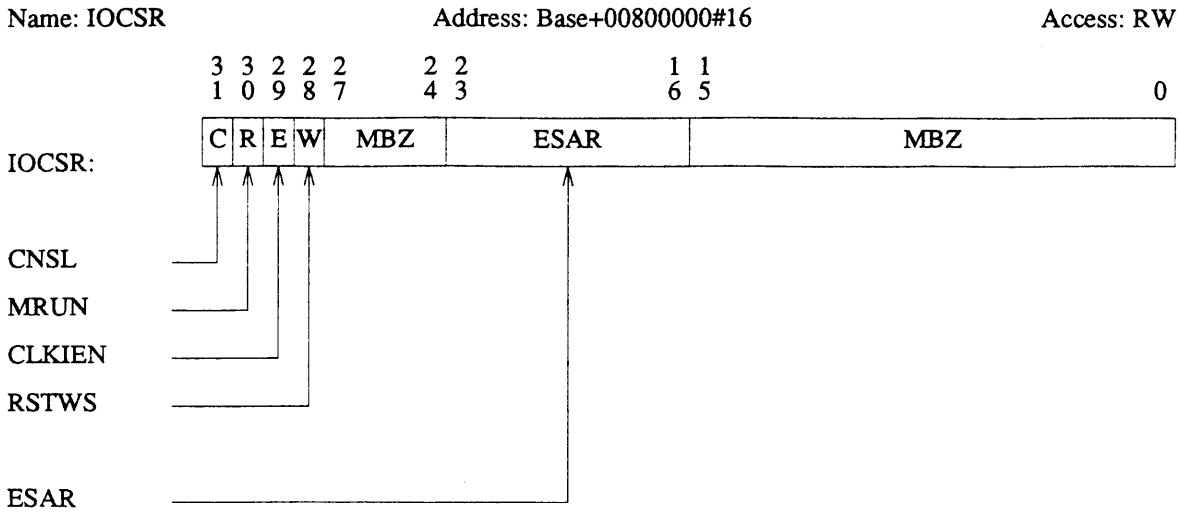

Figure 7-2: IOCSR

CNSL

Writing the CNSL bit with a 1 causes breaks on the L2003 printer/console serial line to assert the M-bus MHALT signal. When CNSL is 0, breaks have no effect.

MRUN

Writing the MRUN bit with a 1 asserts the backplane MRUN signal. When MRUN is 0, the backplane MRUN signal is deasserted.

CLKIEN

When CLKIEN is 1, the L2003 drives the M-bus MCLKI signal. When it is 0, the L2003 does not drive the M-bus MCLKI signal.

RSTWS

Writing the RSTWS bit with a 1 activates the MRESET logic and resets the entire workstation. The MRESET sequence will automatically clear the RSTWS bit.

ESAR

The ESAR field is the output of the Ethernet Station Address ROM. The IOCSR must be read at 32 consecutive addresses to read the entire ROM contents, that is, for slot 3 at 36800002#16, 36800006#16, 3680000A#16, and so on.

7.2.6. M-Bus Interface

The M-bus interface consists of the Firefox Bus Interface Chip (FBIC), seven 74F245 M-bus transceivers, one 74F244 M-bus driver, two 74AS760 open collector M-bus drivers, and one 74ALS240 status-indicator driver.

7.2.6.1. Device Features

The FBIC, designed by the WSE group in Palo Alto, is a multipurpose, bus interface and cache controller that connects a CVAX pin-bus to the M-bus and supports an optional snoopy cache. The chip functions both as a CVAX pin-bus master and as a CVAX pin-bus slave, depending on the needs of the particular module on which it resides. On the L2003, it is always the C-bus master. The FBIC also supports the M-bus write-back snoopy cache protocol, as defined in the *Firefox System Specification*, for an on-chip single-entry cache or an optional external cache. The L2003 does not use the cache option of the FBIC.

The FBIC implements all of the M-bus interface functions necessary to access L2003 control and status registers, RAM, and ROM from the M-bus. It connects the CVAX pin-bus interrupt request signals to the M-bus and forwards M-bus interrupt-acknowledge cycles onto the CVAX pin-bus. In addition, the FBIC controls the 32-bit base workstation ROM, a 5-bit status indicator, and a 2-bit manufacturing-mode input.

A detailed description of the chip's operation and of the format of its control and status registers can be found in the *FBIC Functional Specification*.

7.2.6.2. Bus Connections

The FBIC connects to both the M-bus and the C-bus and forwards transactions from the M-bus to the C-bus as appropriate. Table 7-9 lists the FBIC's response to M-bus transactions. For I/O space transactions, a reference is in range if it is in the 32-Mbyte region assigned for the slot or if the FBIC address decoder matches. The address decoder is used to accept M-bus I/O-space references for the SSC and after every workstation reset, must be programmed to match M-bus addresses 8014XXXX#16 (VAX addresses 2014XXXX#16). For interrupt-acknowledge transactions, a C-bus interrupt-acknowledge transaction is initiated if the IRQ signal for the specified interrupt level is asserted on the C-bus.

Table 7-9: FBIC Response to M-bus Transactions.

M-bus Transaction	FBIC Response
Memory read	None
Memory read interlocked	None
Memory write	None
Memory write unlock	None
I/O read	C-bus I/O read if in address range
I/O read interlocked	C-bus I/O read if in address range (interlock ignored)
I/O write	C-bus I/O write if in address range
I/O write unlock	C-bus I/O write if in address range (unlock ignored)
Interrupt acknowledge	C-bus interrupt acknowledge if IRQ<n>

The L2003 does not support any interlocking of local devices with respect to the M-bus. Software must not issue interlocked references to device registers or the RAM buffers; if it does, an M-bus timeout will result. Software may use interlocked instructions to reference FBIC registers.

7.2.6.3. Interrupts

The FBIC monitors the C-bus IRQ signals and, if enabled via the FBIC FBICSR register, asserts the corresponding MIRQ signals. When an M-bus interrupt-acknowledge transaction for an asserted IRQ signal occurs, the FBIC generates a C-bus interrupt-acknowledge transaction. The SSC generates interrupts on the C-bus IRQ0 signal.

The FBIC also generates and acknowledges interrupts when its DEVIRQ inputs are asserted. The serial, disk/tape, and network interfaces generate vectored interrupts via the DEVIRQ inputs.

The FBIC MEMERR output, asserted when the FBIC generates or receives an M-bus MABORT, is looped back to the FBIC as DEVIRQ<3>. This results in an IPL 17#16 M-bus interrupt.

7.2.6.4. External Connection

The FBIC connects to the M-bus.

7.2.6.5. FBIC Address Map

Table 7-10 lists the address offsets of the FBIC control and status registers.

Table 7-10: FBIC Register Map

Name	Address	R/W	Description
MODTYPE	01FFFFFC#16	R	Module-type register
BUSCSR	01FFFFF8#16	R/W	M-bus error-status register
BUSCTL	01FFFFF4#16	R/W	M-bus error-control-signal-log register
BUSADR	01FFFFF0#16	R/W	M-bus error-address-signal-log register
BUSDAT	01FFFFEC#16	R/W	M-bus error-data-signal-log register
FBICSR	01FFFFE8#16	R/W	FBIC control-status register
RANGE	01FFFFE4#16	R/W	I/O space range decode register
IPDVINT	01FFFFE0#16	R/W	Interprocessor/device-interrupt register
WHAMI	01FFFFDC#16	R/W	Unique software ID register
CPUID	01FFFFD8#16	R	Unique hardware ID register
IADR1	01FFFFD4#16	R/W	Interlock-1 address register
IADR2	01FFFFD0#16	R/W	Interlock-2 address register
SAVGPR	01FFFFC4#16	R/W	Scratch register for halt code

Table 7-11 lists the base addresses for the various M-bus backplane slots. For example, to read the MODTYPE CSR when the L2003 is in backplane slot 3, a VAX issues a longword read to address 37FFFFFC#16.

Table 7-11: FBIC Slot Base Addresses

Slot	M-bus Address	VAX Address
0	90000000#16	30000000#16
1	92000000#16	32000000#16
2	94000000#16	34000000#16
3	96000000#16	36000000#16
4	98000000#16	38000000#16
5	9A000000#16	3A000000#16
6	9C000000#16	3C000000#16
7	9E000000#16	3E000000#16

7.2.7. Base Workstation ROM

The base workstation ROM consists of two 27210 64K-by-16 EPROMs and two 74ALS373 address latches. This yields a total of 256 Kbytes of ROM. The FBIC controls the EPROMs, which are in sockets and physically reside on the C-bus. The base address of the EPROMs is defined by the FBIC at slot offset range 01E00000#16 through 01E7FFFF#16.

7.2.8. L2003 Status-Indicator Outputs

The FBIC status-indicator outputs drive a hexadecimal-digit display in the L2003 cover. In addition, the most significant bit of the status output is displayed via a green LED on the L2003 itself.

The least significant five bits of the FBIC FBICSR<LEDS> register specify the value of the status indicators. The least significant four bits of the FBICSR<LEDS> field drive the hexadecimal-digit; the digit displays the complement of the value in the register. Bit 4 of FBICSR<LEDS> register field drives the hexadecimal display left decimal point and the green LED; the decimal point and LED are illuminated when the bit is set.

The FBICSR<LEDS> bits are automatically cleared by workstation reset (M-bus MRESET asserted). This results in the hexadecimal digit displaying F#16 with its decimal points off and the module green LED off. Writing all 1's to the FBIC FBICSR<LEDS> register field will display a 0 on the hexadecimal digit and

illuminate the left decimal point and the green LED.

7.2.9. L2003 Manufacturing-Mode Inputs

The FBIC manufacturing-mode inputs from the L2003 cover are connected to the FBIC manufacturing-mode input pins. The FBIC FBICSR<MFMD> register bits reflect the value of the manufacturing-mode inputs.

The cover cable MFNMOD signals are open collector signals that are pulled up to +5 volts by the L2003. Either, or both, of the MFNMOD signals can be shorted to ground by external cables or jumpers. The FBIC FBICSR<MFMD> register field continuously indicates the complement of the MNFMOD signals. That is, without a jumper, the corresponding register bit is set; and with a jumper to ground, the corresponding register bit is clear.

7.2.10. M-Bus MRESET Logic

The L2003 generates the M-bus MRESET signal from the M-bus MDCOK signal and powerup logic. The power-up reset logic uses the delayed assertion of MPOK to assert MRESET for approximately 70 milliseconds after powerup. The logic controls a simple-state machine to guarantee a minimum MRESET assertion width of 16 M-bus cycles. The MRESET signal can also be asserted by setting the IOCSR<RSTWS> bit.

7.2.11. Clocks

The L2003 requires the following clocks:

- 20-MHz, 2-phase clocks for the FBIC
- 40-MHz clock for the SSC bus interface
- 25.6-KHz oscillator for the SSC time-of-year clock
- 20-MHz clock for the SII
- 20-MHz crystal for the SIA
- 20-MHz clock for the local RAM buffer control
- 15.2064-MHz clock for the DZ

A single oscillator is used to generate the 40-MHz and 20-MHz clocks. A separate 25.6-KHz oscillator, on battery backup, drives the SSC time-of-year clock, a separate 20-MHz crystal drives the SIA, and a separate 15.2064-MHz oscillator drives the DZ.

7.2.12. Cover Assembly Cable Connector

A 50-conductor ribbon cable connects the L2003 serial line signals, Ethernet transceiver signals, status output signals, and manufacturing-mode input signals to the cover assembly. Table 7-12 lists the pin assignments for the cable.

Table 7-12: L2003 Cover Assembly Cable Signal Assignments

Signal	Pin	Pin	Signal
+12V	50	49	+12V
GND	48	47	GND
TX0	46	45	RX0
CTS2	44	43	GND
RTS2	42	41	DTR2
TX1	40	39	RX1
DSR2	38	37	GND
RI2	36	35	CD2
TX2	34	33	RX2
DSRS2	32	31	GND
SPDMI2	30	29	TMI2
TX3	28	27	RX3
+5V	26	25	+5VBAT
LLPBK2	24	23	GND
–12V	22	21	–12V
MFMD0	20	19	MFMD1
LED0	18	17	LED1
LED2	16	15	LED3
TX+	14	13	TX–
LED4	12	11	SPARE
COL+	10	9	COL–
GND	8	7	GND
RX+	6	5	RX–
GND	4	3	GND
+12V	2	1	+12V

The +12-volt outputs have a PTC current limit device that changes from low to high resistance if more than 2.0 amperes are drawn. The +5-volt output has a PTC current limit device that changes from low to high resistance if more than 1.0 ampere is drawn. The –12-volt outputs have a PTC current limit device that changes from low to high resistance if more than 0.5 ampere is drawn.

7.2.13. DSSI Cable Connector

A 50-conductor ribbon cable connects the L2003 disk interface to DSSI drives. Table 7-13 lists the pin assignments for the cable.

Table 7-13: L2003 DSSI Cable Signal Assignments

Signal	Pin	Pin	Signal
DATA<0>	1	2	GND
DATA<1>	3	4	GND
DATA<2>	5	6	GND
DATA<3>	7	8	GND
DATA<4>	9	10	GND
DATA<5>	11	12	GND
DATA<6>	13	14	GND
DATA<7>	15	16	GND
PARITY	17	18	GND
<NC>	19	20	GND
<NC>	21	22	GND
TERMPWR	23	24	TERMPWR
TERMPWR	25	26	TERMPWR
TERMPWR	27	28	TERMPWR
GND	29	30	<NC>
GND	31	32	<NC>
GND	33	34	<NC>
GND	35	36	BSY
GND	37	38	ACK
GND	39	40	RST
GND	41	42	<NC>
GND	43	44	SEL
GND	45	46	CD
GND	47	48	REQ
GND	49	50	IO

All signals have 120/280-Ohm parallel termination and decoupling as specified by the DSSI physical specification. The TERMPWR output supplies up to 1.5 amperes of +5 volts through a series diode. There is a PTC current limit device that changes from low to high resistance if more than 1.5 amperes are drawn.

7.2.14. Printed Circuit Board

The L2003 uses an 8-layer L-series-quad printed circuit board with uncontrolled impedance. There are two 1-oz pad layers, four 1-oz signal layers, one 1-oz +5-volt layer, and one 1-oz ground layer. Layer construction is PS - SS + SP.

7.3. Programming

In this section, required initialization of the L2003 is described, and some programming guidelines are presented. The examples used herein are based on an L2003 in M-bus slot 1. All addresses are VAX physical addresses.

7.3.1. Locating Modules

After a workstation reset (M-bus MRESET asserted), console and diagnostic software must determine the workstation configuration. The FBIC saves the value of the M-bus MBRQ signals during MRESET in its BUSCTL register. Software may use this as a module-present indication to identify backplane M-bus slots that contain Firefox modules. To interpret the BUSCTL<MBRM> bits, a module must first determine its own M-bus slot by reading its FBIC CPUID<MID> register field. Table 7-14 lists the interpretation of BUSCTL<MBRM> as a function of a module's M-bus slot (from its CPUID<MID>). For example, if a module reads its CPUID<MID> register field and obtains 4, it is in M-bus slot 4. If it then reads its

BUSCTL<6:0> register field and obtains 1011001#2, there are modules in M-bus slots 0, 3, 5, and 7. Software must use or save the value of BUSCTL<MBRM> before it enables FBIC error logging, or the information will be lost.

Table 7-14: Interpretation Of FBIC BUSCTL<MBRM> Field

CPUID<MID>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
0	7	6	5	4	3	2	1
1	7	6	5	4	3	2	0
2	7	6	5	4	3	1	0
3	7	6	5	4	2	1	0
4	7	6	5	3	2	1	0
5	7	6	4	3	2	1	0
6	7	5	4	3	2	1	0
7	6	5	4	3	2	1	0

To confirm presence of a module in each slot, software should read the MODTYPE register of each slot. In the preceding example, the MODTYPE registers would be at VAX addresses 31FFFFFC#16, 37FFFFFC#16, 3BFFFFFC#16, and 3FFFFFFC#16. Reading the L2003's MODTYPE register will return the value 01010004. L2003 ROM should have a known location that identifies it as an L2003 I/O class module.

7.3.2. Addressing

Except for SSC access, software must calculate L2003 device addresses from the M-bus slot of the module and the device offset addresses specified in this chapter. The VAX physical address calculation is

```
I/O-ADDRESS = 30000000#16 + (SLOT << 25) + OFFSET
```

where the << notation represents a logical left shift.

7.3.3. Initialization

After workstation reset, the L2003 requires initialization of the FBIC and SII devices before normal operation can commence. Software must generate the following register writes:

1. MOVL FFFFFFFF#16, (33FFFFF8#16) to write the FBIC BUSCSR register to enable error logging.
2. MOVL 0011003E#16, (33FFFFE8#16) to write the FBIC FBICSR register to connect the CVAX pin-bus CIRQ0 signal to the M-bus MIRQ0 signal for SSC interrupts, and enter normal operating mode.
3. MOVL 80148000#16, (33FFFFE4#16) to write the FBIC RANGE register to make the SSC accessible.
4. MOVL 20#16, (32800000#16) to set the IOCSR<CLKIEN> bit to drive the M-bus MCLKI signal.
5. MOVL 0001VVVV#16, (33FFFFE0#16) to write the FBIC IPDVINT register to enable device interrupts from the SII and LANCE chips, where VVVV is the desired interrupt vector(s).
6. MOVW 0010#16, (3300000C#16) to write the SII CSR register to operate in arbitrated-bus mode.

Software must not access the disk buffer until after the SII is put into arbitrated-bus mode, or M-bus aborts and unpredictable SII register content modifications will result.

7.3.4. Multiple Firefox Workstation I/O Modules

There are no logical or electrical restrictions that prohibit configurations with more than one L2003. However, only one of the modules can allow access to the SSC and drive the M-bus MCLKI signal. Software must select one of the modules as the primary L2003 and program the FBIC range decoder and set the

IOCSR<CLKIEN> register bit on only that primary module.

7.3.5. Base Workstation ROM

The L2003 ROM is intended for L2003 self-test code and workstation disk/tape/network bootstrap code. Access to the ROM from other modules is relatively slow, typically two microseconds per access. Copying frequently used or time-critical code to memory is recommended.

7.3.6. Interlocked References

The L2003 does not support interlocked references to its internal device interface registers or disk/network buffers; bus errors will result if software generates interlocked references. The FBIC does support interlocked references to its own registers.

7.3.7. Device Interrupts

As discussed in the serial, disk, and network interface sections earlier in this chapter, the FBIC functions as a vectored interrupt controller for the DZ (DC7085), SII (DC7061), and LANCE (AM7990) device controllers.

These devices all have level-sensitive, nonvectored, interrupt-request outputs, whereas the FBIC DEVIRQ inputs are falling-edge sensitive. Consequently, to avoid missing additional interrupts generated by a given device controller between the time a processor acknowledges the FBIC vectored interrupt-request from that device and the time it clears the interrupt condition within the device controller, software must guarantee deassertion of the device-interrupt-request output. Software can accomplish this by disabling interrupts from the device at the end of the interrupt-service routine. In the case of the DZ, write the CSR<TIE> and CSR<RIE> bits with a 0, and then write them with a 1 (if transmitter/receiver interrupts are to be reenabled). In the case of the SII, write the CSR<IE> bit with a 0, and then write it with a 1 (if disk interrupts are to be reenabled). In the case of the LANCE, write the CSR0<INEA> bit with a 0, and then write it with a 1 (if network interrupts are to be reenabled).

The FBIC device interrupt vectors can be set to any naturally aligned block of four contiguous vectors; SII interrupts vector to VVV0#16, LANCE interrupts vector to VVV4#16, DZ interrupts vector to VVV8#16, and FBIC MEMERR interrupts vector to VVVC#16. For example, if the FBIC IPDVINT register is written with 00010300#16, device interrupts are enabled and the DZ, LANCE, and SII have vectors 0308#16, 0304#16, and 0300#16.

7.3.8. Disk/Network Buffers

The disk and network interfaces each have local 128-Kbyte buffers to meet latency constraints of the SII and LANCE device controllers. Access to these buffers is time multiplexed between the FBIC and the device controllers. Due to the long I/O-space reference service times (relative to memory space) it is recommended that device drivers minimize access to the buffers. This results in reduced M-bus bandwidth and improved device-controller performance. In particular, it is recommended that network and disk packets be composed/decomposed in memory buffers and then copied between the memory buffer and the L2003 device buffer.

7.3.9. Module Reset

L2003 reset, from either a workstation reset (MRESET asserted) or an FBIC module reset, causes the following actions:

- FBIC C-bus interface initialized
- SSC initialized
- I-bus control logic initialized
- IOCSR<CNSL+MRUN+CLKIEN+RSTWS> bits cleared

- DZ initialized with all serial lines disabled and all modem control outputs deasserted
- LANCE initialized with Ethernet packet transfers disabled
- Network RAM buffer contents undefined
- D-bus control logic initialized
- SII initialized with DSSI packet transfers disabled
- Disk RAM buffer contents undefined

In the case of a workstation reset, the FBIC M-bus interface is also initialized and left in diagnostic isolate mode. When the FBIC M-bus interface is initialized, the FBIC LEDs outputs are deasserted causing the cover assembly hexadecimal-display to indicate 'F' with the hexadecimal-display decimal point and L2003 green LED off.

To generate a module reset, software should perform the following:

- Set the FBIC FBICSR<RESET> bit.
- Clear the FBIC FBICSR<LEDS> field if it wishes the FBIC LEDS outputs to deassert during a module reset.
- Clear the FBIC FBICSR<RESET> bit.

Software must not access any L2003 address other than the FBIC FBICSR register during module reset.

7.4. Access Time

System processor access time to L2003 resources is a function of three factors:

- Processor M-bus interface implementation
- M-bus cycle time
- L2003 implementation

Table 7-15 lists the number of M-bus and L2003 cycles that elapse accessing the various L2003 resources from the M-bus. L2003 cycles are 100 ns in length. Total processor access time requires processor timing and is thus beyond the scope of this section.

Table 7-15: L2003 Access Cycles

Component	M-bus Cycles	L2003 Cycles
FBIC registers	5	-
FBIC overhead	6*	5*
Internal ROM read	-	8
Internal SSC access	-	5
Internal IOCSR access	-	5**
Internal DZ access	-	9**
Internal LANCE CSR0/CSR3/RAP access	-	8**
Internal LANCE CSR1/CSR2 access	-	16**
Internal net buffer access	-	5**
Internal SII access	-	10***
Internal disk buffer access	-	6***

* ±0.5 cycles due to synchronizer uncertainty
** With LANCE idle, 50-cycle maximum latency
*** With SII idle, 6-cycle maximum latency

All M-bus transactions that reference internal L2003 resources have two components, the FBIC overhead and the internal access, that must be added to determine the total M-bus access time. For example, an M-bus reference to the IOCSR requires 6 M-bus cycles plus 10 L2003 cycles; with a 70-ns M-bus, this is a total of 1420 ns.

LANCE DMA access to the network buffer completes in the minimum LANCE transaction length. This results in 100 ns ±25-ns arbitration overhead and 600-ns I-bus buffer read/write cycles. If there is an M-bus reference to the IOCSR, DZ, LANCE CSR, or network buffer at the time of a LANCE DMA request, the LANCE is stalled until the M-bus reference completes.

As indicated in Table 7-15, L2003 cycles for IOCSR, DZ, LANCE, and the net buffer are with the LANCE idle. If LANCE DMA is in progress when an internal reference to the IOCSR, DZ, LANCE, or network buffer starts, the internal reference is stalled until the LANCE completes its DMA. The LANCE uses 8-transfer burst DMA during packet data transfer, resulting in a maximum stall of approximately 50 cycles (5000 ns).

SII DMA access to the disk buffer completes in the minimum SII transaction length. SII address cycles complete in 300 ns. SII data cycles complete in 200 ns.

As indicated in Table 7-15, L2003 cycles for the SII and disk buffer are with the SII idle. If SII DMA is in progress when an internal reference to the SII or disk-buffer start, the internal reference is stalled until the SII completes its DMA. The SII services pending CSR access and bus requests (for disk-buffer access) after each of its transfers, resulting in a maximum stall of approximately six cycles (600 ns).