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 1980

COMPONENT SIDE VIEW

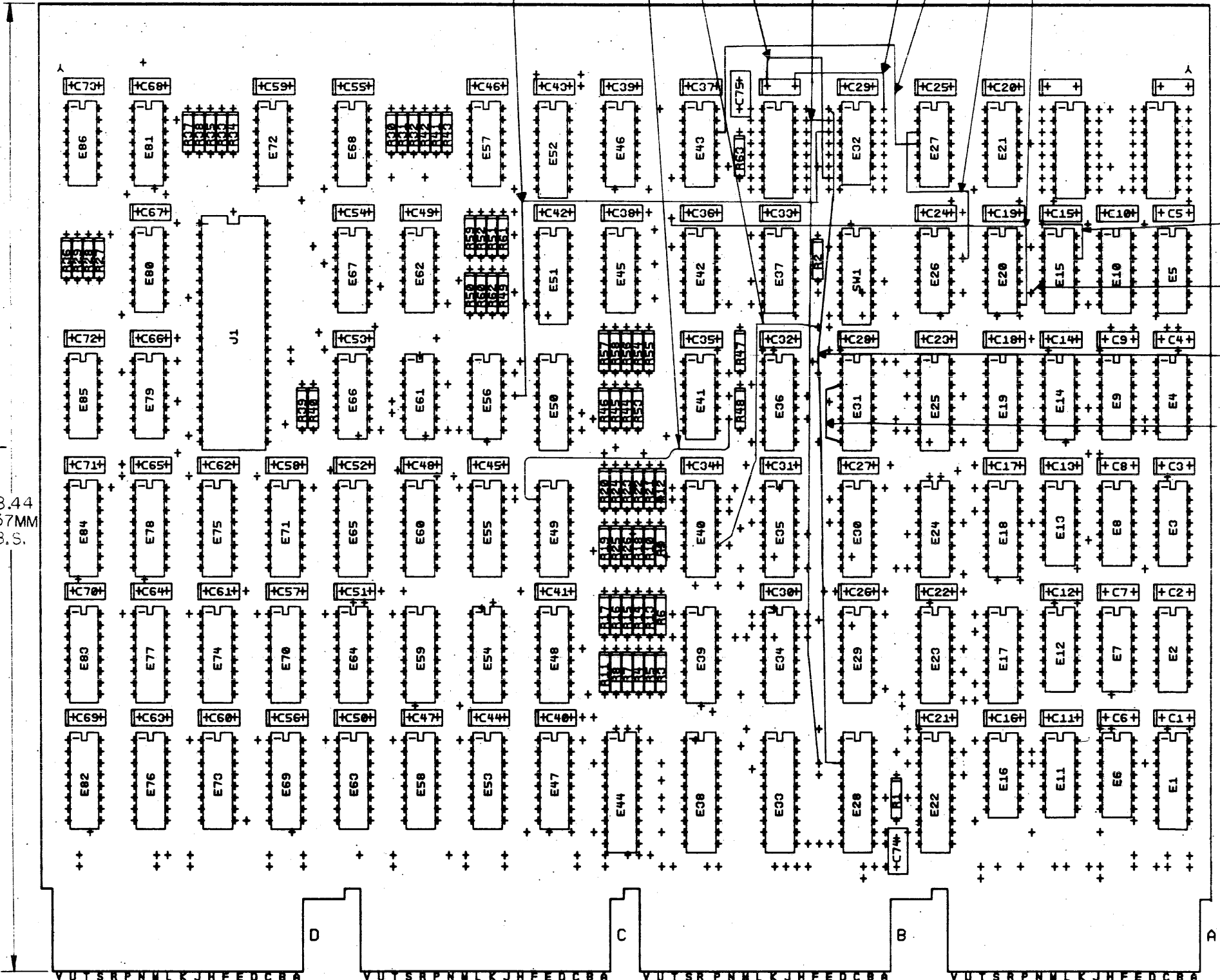
MODE	SW1								MICRO ADDRESS RESPONSE
	S1	S2	S3	S4	S5	S6	S7	S8	
I	ON	OFF	OFF	ON	OFF	ON	OFF		MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777
II	OFF	ON	OFF	ON	OFF	OFF	ON		INITIAL MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 0-777. TOGGLED MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 1000-1777
III	OFF	OFF	ON	ON	OFF	ON	OFF		MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777. THIS IS IDENTICAL TO MODE I, EXCEPT THE TWO 512 WORD BLOCKS OF RAM ARE SWAPPED.
IV	ON	OFF	OFF	OFF	ON	ON	OFF		MICRO ADDRESSES 0-1777 CORRESPOND TO WCS RAM ADDRESSES 0-1777

WCS COMMAND/STATUS REGISTER (177540)	
BIT	FUNCTION
15	WHEN SET TO A 1 THE TRACE RAM ADDRESS IS INITIALIZED TO 0 AND THE PAGING LOGIC IS INITIALIZED TO THE LOWER 512 WORDS OF RAM. SUBSEQUENTLY CLEARING THIS BIT TO A 0 ENABLES THE TRACE RAM AND PAGING LOGIC.
14	WHEN SET TO A 1, THE DATA AT THE CURRENT TRACE RAM LOCATION CAN BE READ (ONLY) AT ADDRESS 177542.
13	WHEN SET TO A 1 AND THEN CLEARED TO A 0, THE NEXT TRACE RAM LOCATION IS ADDRESSED TO BE ACCESSED USING CSR BIT (14).
12	WHEN SET TO A 1, THE WCS IS ENABLED TO RESPOND TO THE LSI-11 MID. WHEN CLEARED TO A 0, THE WCS WILL NOT RESPOND TO THE LSI-11 MID AND THE RAM LOCATION POINTED TO BY CSR BITS 9, 8 CAN BE READ OR WRITTEN (RAM BITS <23:16> AT 177544 AND RAM BITS <15:8> AT 177542).
11-10	UNUSED, WILL ALWAYS BE READ AS CLEARED TO 0.
9-0	THE WCS RAM ADDRESS THAT CAN BE ACCESSED WHEN BITS <14,12> ARE CLEARED TO A 0.

IC	8	16
2115-02	8	16
74298	8	16
74174	8	16
74LS253	8	16
74193	8	16
7489	8	16
8640	1	8
74148	8	16
SD5101	4	11
DC005	10	20
DC004	10	20
ICTYPE	GND	+5V

GND AND +5V ARE USUALLY PIN 7 AND 14, RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

IC PIN LOCATIONS



8.44  
214.37MM  
F.B.S.

- NOTES: Ø-1: ADD WIRE FROM E31-3 TO E31-8.  
 Ø-2: ADD WIRE FROM E32-14 TO NEAR CAPACITOR PAD OVER SPARE IC LEFT OF E32.  
 Ø-3: ADD WIRE FROM E32-7 TO FAR CAPACITOR PAD OVER SPARE IC LEFT OF E32.  
 Ø-4: ADD WIRE FROM E32-2 TO PTH RIGHT OF E33-18.  
 Ø-5: ADD WIRE FROM E32-3 TO PTH LEFT OF E50-4.  
 Ø-6: ADD WIRE FROM E32-1 TO E28-3.  
 1-3: FROM E40-11 TO PTH TO THE RIGHT OF C32.

CHANGE NO. REV  
 P.S. M8018-0001 C  
 A. DENKARD  
 JOHN CURTIS  
 DATE

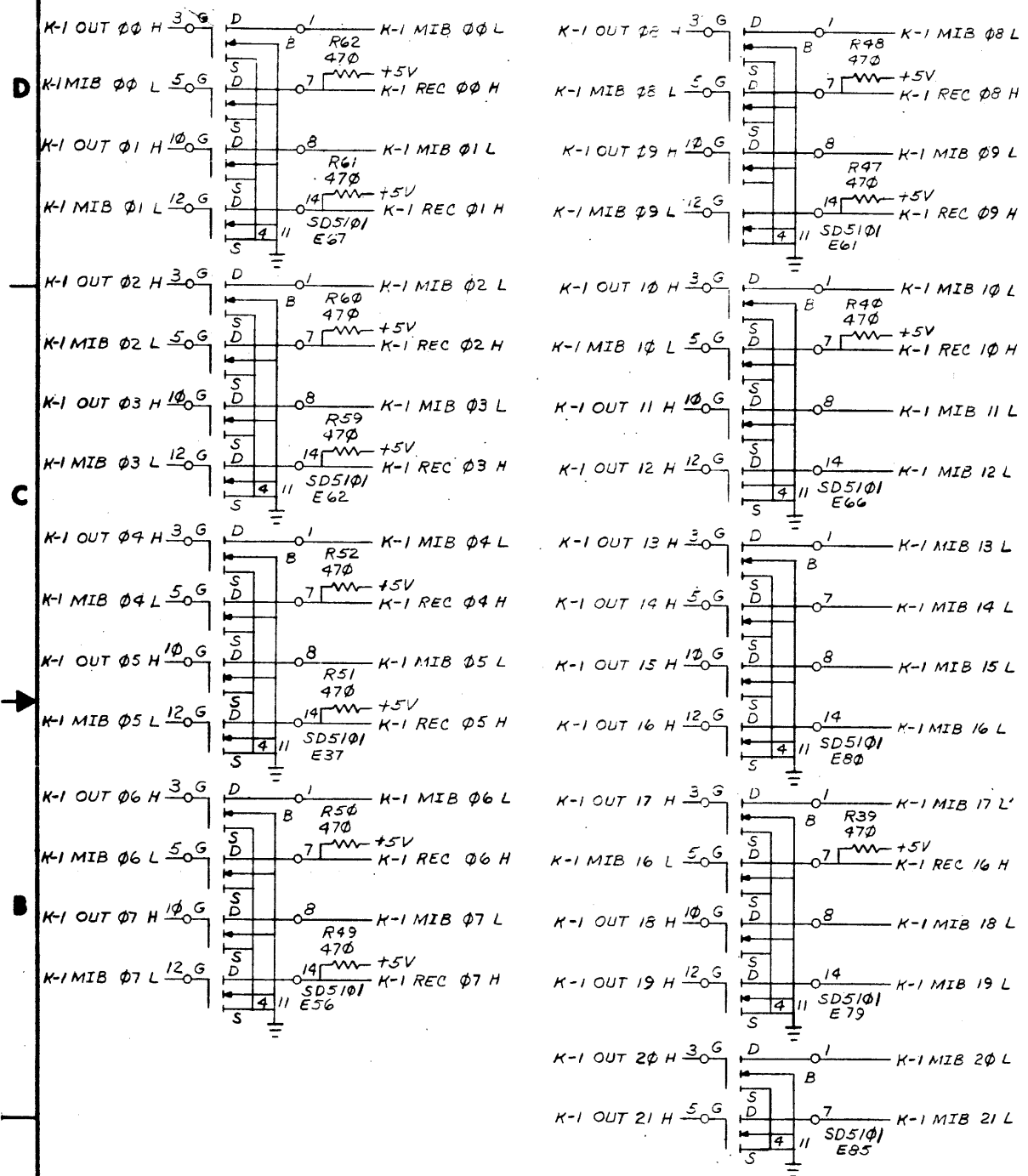
- NOTES: Ø-8: ADD WIRE FROM E15-5 TO PTH LEFT OF E15-6.  
 Ø-9: SIDE ETCH CUT FROM E15-4 AND PTH ABOVE E15-1.  
 Ø-10: SIDE ETCH AFTER PTH ABOVE LEFT OF E42-1.  
 Ø-11: SIDE ETCH CUT AFTER E43-12.  
 Ø-12: ADD WIRE FROM E15-12 TO PTH ABOVE E15-1.  
 Ø-13: ADD WIRE FROM E20-8 TO PTH ABOVE LEFT OF E42-1.  
 Ø-14: ADD WIRE FROM E27-4 TO E43-12.  
 Ø-15: ADD WIRE FROM E27-3 TO PTH RIGHT OF E26-12.  
 1-4: FROM E49-2 TO PTH TO THE RIGHT OF E49.

BOARD FABRICATION INFORMATION	
PANEL SIZE	
PANEL DATA DWG.#	
PANEL MAT'L	
QTY. OF LAYERS	
COPPER THICKNESS	
PTH. X PRINT AND ETCH	
MODULE INSERTED 100 TIMES OR MORE	

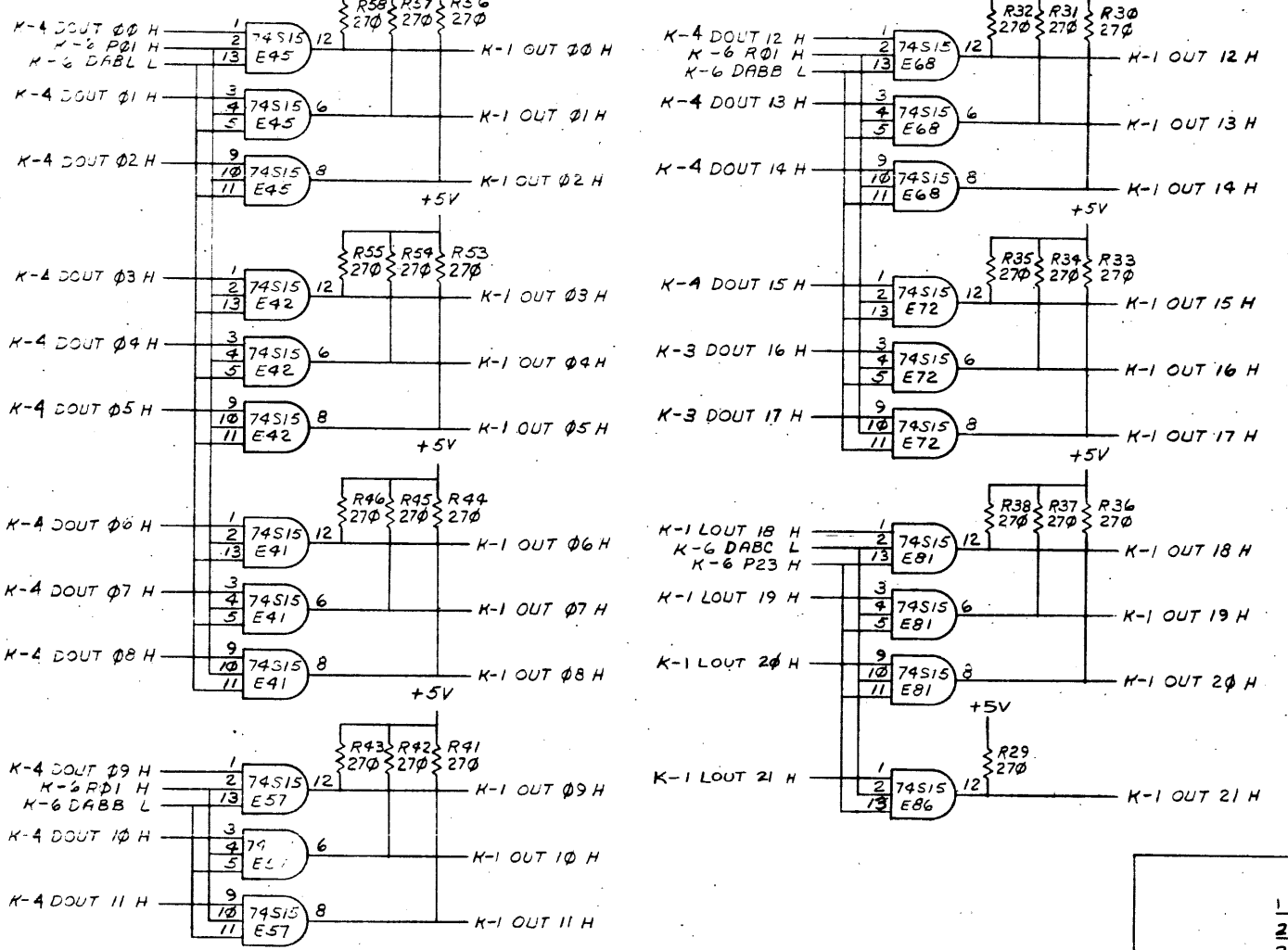
SIGNATURES	DATE	digital
DRN. <i>[Signature]</i>	12-27-77	
CHK'D. <i>[Signature]</i>	1-6-78	
ENG. <i>[Signature]</i>	8-22-77	
PROJ. ENG. <i>[Signature]</i>	8-22-77	
PROD. <i>[Signature]</i>	12-1-77	
SCALE 2/1		TITLE WRITEABLE CONTROL STORE
SHT. 1 OF 1		SIZE CODE NUMBER REV
NEXT HIGHER ASSY. B-DD-M8018-0		0 UA M8018-0-0 D

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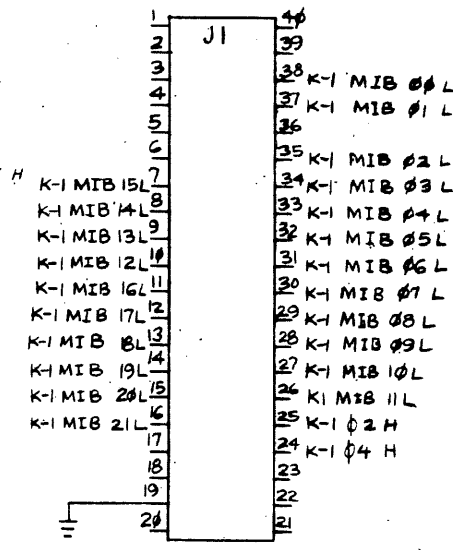
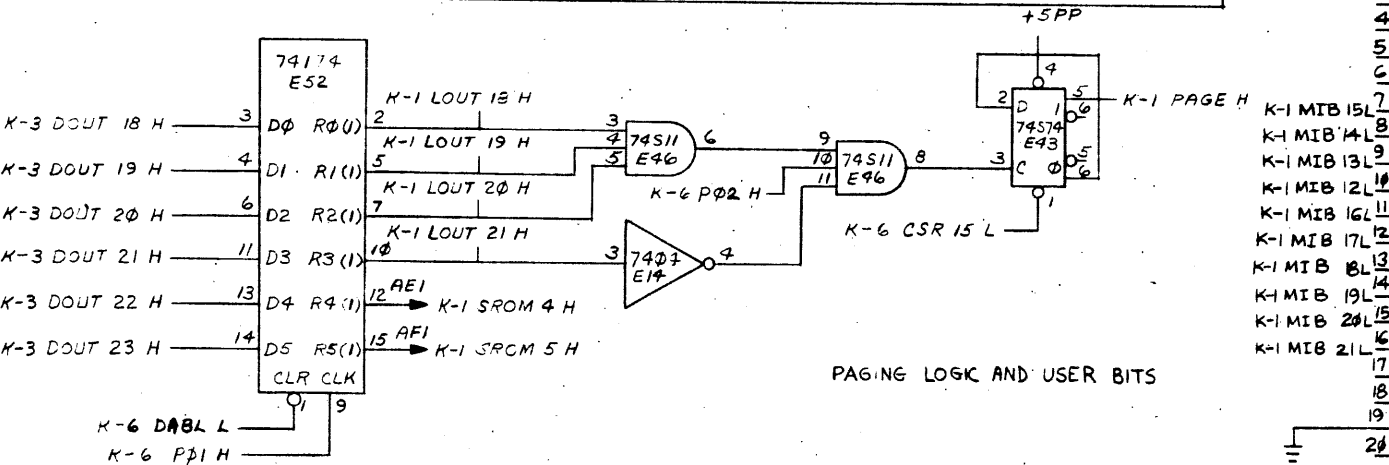
MIB INTERFACE TRANSCEIEVERS



MIB DATA OUT SELECTION



PAGING LOGIC AND USER BITS



REV.	DATE	BY	CHK'D
1	1/18/76	J.W. CURTIS	
2	2/16/76	J.W. CURTIS	
3	3/1/76	J.W. CURTIS	
4	3/1/76	J.W. CURTIS	
5	3/1/76	J.W. CURTIS	
6	3/1/76	J.W. CURTIS	
7	3/1/76	J.W. CURTIS	
8	3/1/76	J.W. CURTIS	

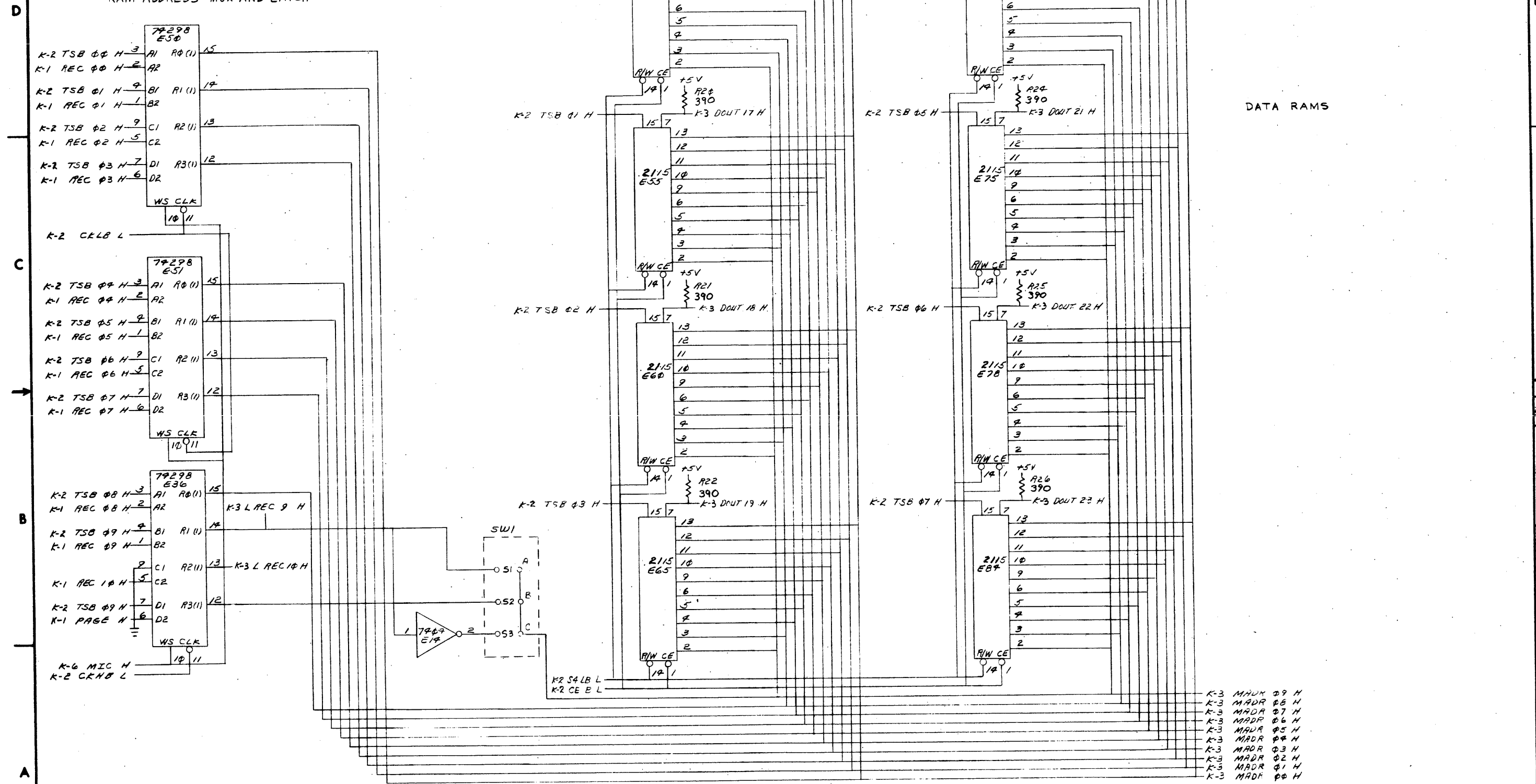
DRN. J. J. CURTIS	8-3-76	FIRST USED ON	
CHK'D		TITLE	WRITEABLE CONTROL STORE (WCS-LSI-II)
ENG. J. J. CURTIS	8-22-76	SIZE	D CS M8018-0-1
PROL. ENG. J. J. CURTIS	8-22-76	NUMBER	REV. E
PROD. J. J. CURTIS	12-1-77	SHEET	1 OF 6
NEXT HIGHER ASSY.		DIST.	



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RAM ADDRESS MUX AND LATCH

DATA RAMS



- K-3 MADR 09 H
- K-3 MADR 08 H
- K-3 MADR 07 H
- K-3 MADR 06 H
- K-3 MADR 05 H
- K-3 MADR 04 H
- K-3 MADR 03 H
- K-3 MADR 02 H
- K-3 MADR 01 H
- K-3 MADR 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

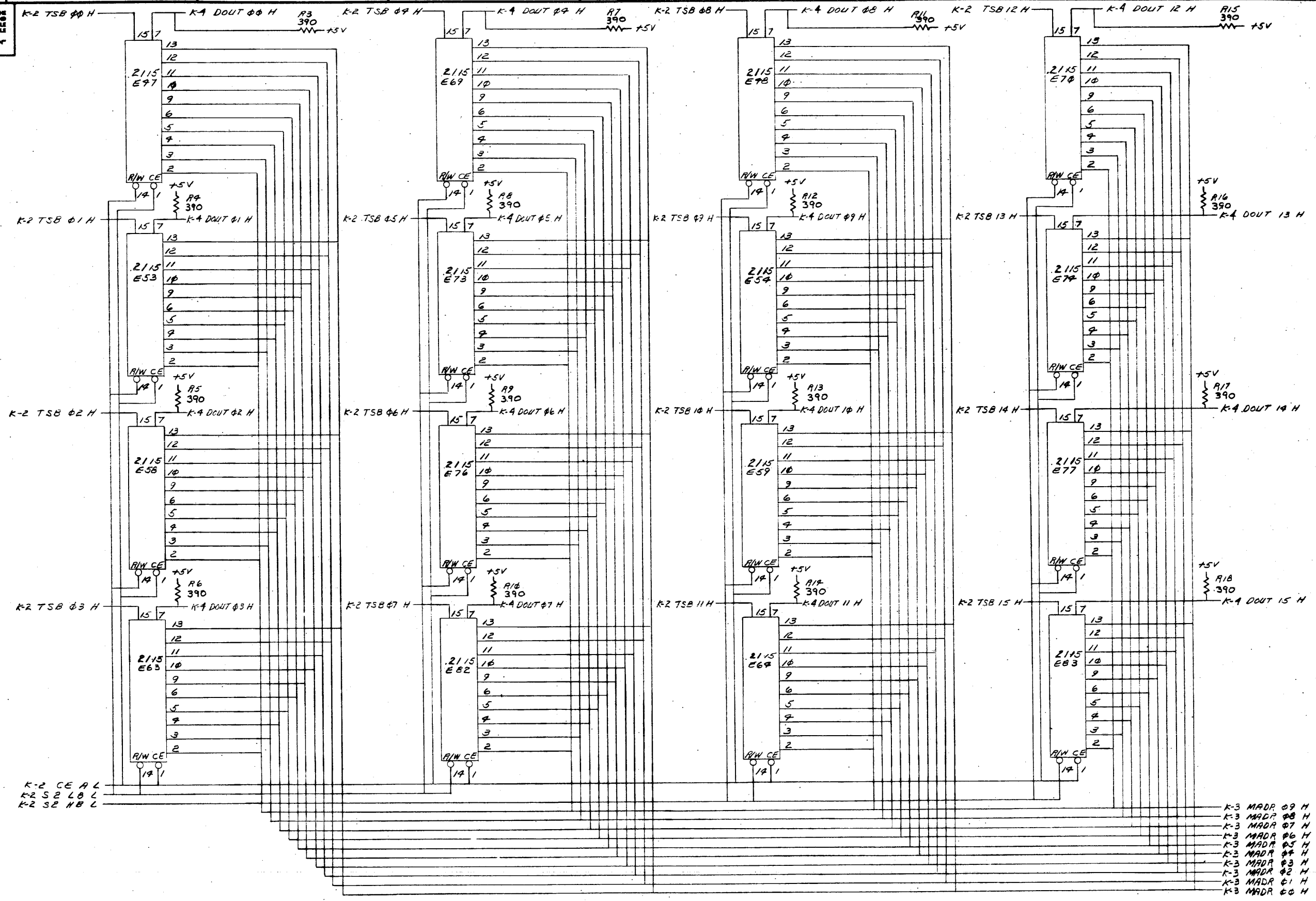
TITLE WRITEABLE CONTROL STORE (WCS-LSI-II)		SIZE CODE DCS	NUMBER M8018-0-1	REV. E
SCALE	SHEET 3 OF 6	DIST.		

DRAWING NO. DCS M8018-0-1 E

(K-3)

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DATA RAMS



K-2 CE A L  
K-2 S 2 L 0 L  
K-2 S 2 H 0 L

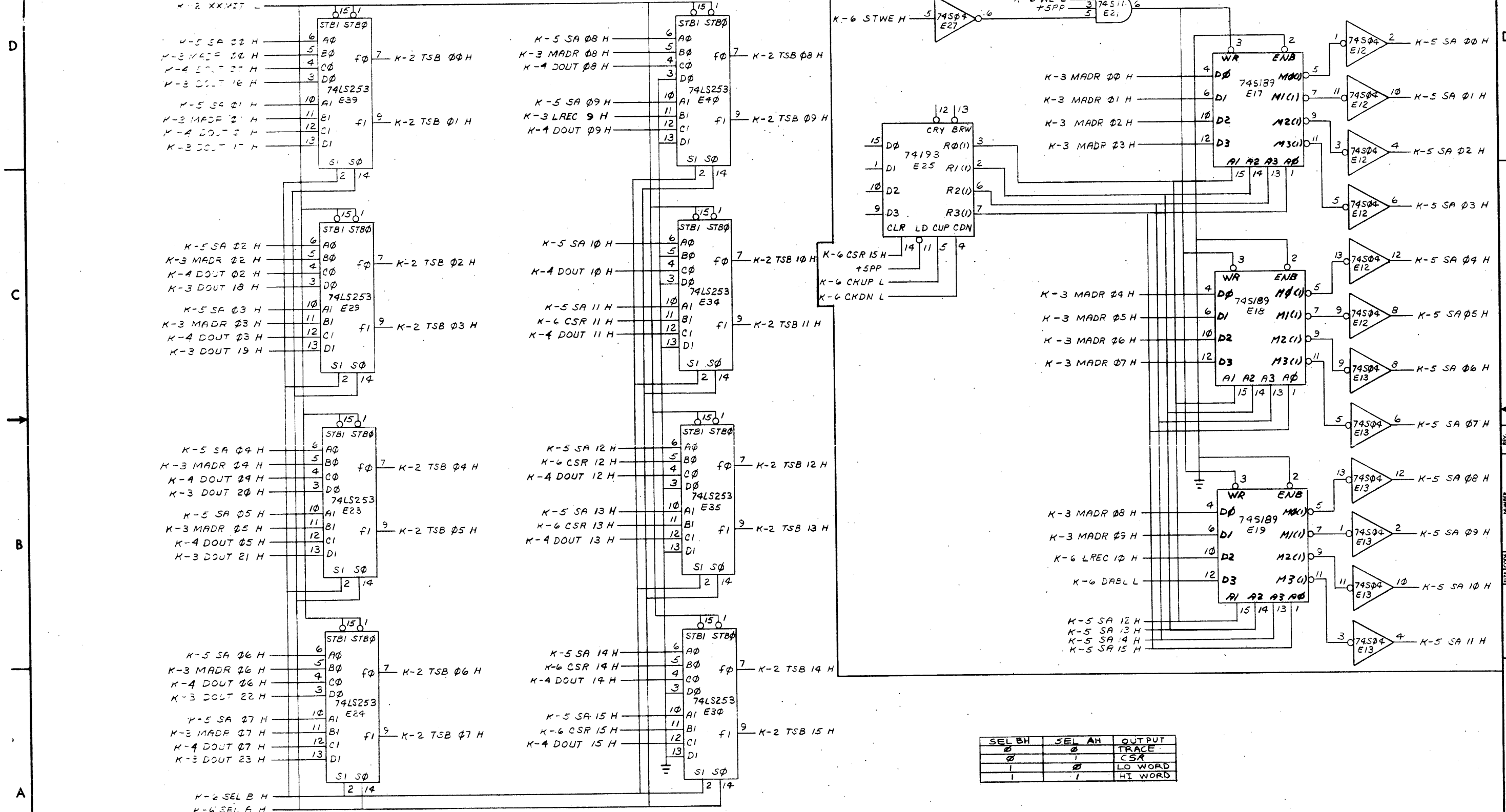
K-3 MADR 09 H  
K-3 MADR 08 H  
K-3 MADR 07 H  
K-3 MADR 06 H  
K-3 MADR 05 H  
K-3 MADR 04 H  
K-3 MADR 03 H  
K-3 MADR 02 H  
K-3 MADR 01 H  
K-3 MADR 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

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DAL OUTPUT MUX'S (TO DCΦΦ5's)

TRACE MODE LOGIC



SEL B H	SEL A H	OUTPUT
0	0	TRACE
0	1	CSA
1	0	LO WORD
1	1	HI WORD

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	WRITEABLE CONTROL STORE (WCS-LSI-II)	SIZE CODE	D CS	NUMBER	M8018-0-1	REV.	E
SCALE	1/8"	SHEET	5 OF 6	DIST.			

