CORE FUNDAMENTALS

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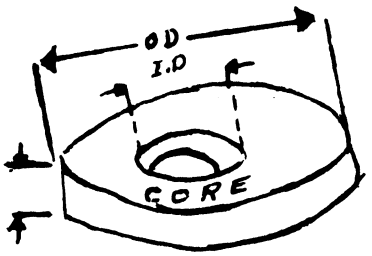
First of all, this being a 2½D memory system and thus different from all other DEC memory systems, it is important that we appreciate the difference between it and the conventional 3D.

Before I go into comparisons, I would like to recap some basic core memory fundamentals which are probably familiar to everyone. Ferrite cores are toroidal (donut shaped) in shape, the core size being denoted by the outer diameter of the toroid (Figure 1) EMI's #31-115 core which we use has:



O. D.	≙	0.30"
I. D.	≙	0.20"
Height	≙	.007"

Figure 1

All the ferrite cores that we use in memory systems have square loop characteristics. I will point out later why the squarer the core characteristic, the lesser the noise. (Noise is defined as unwanted signal).

Core Fundamentals

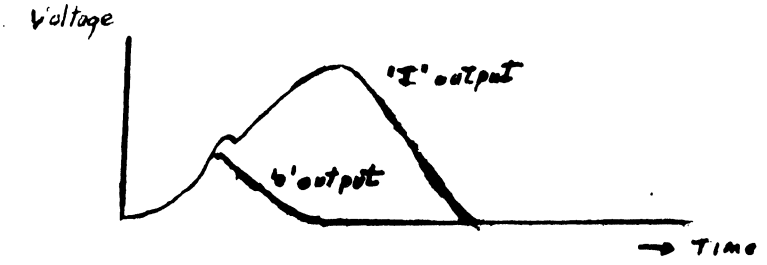


Figure 2

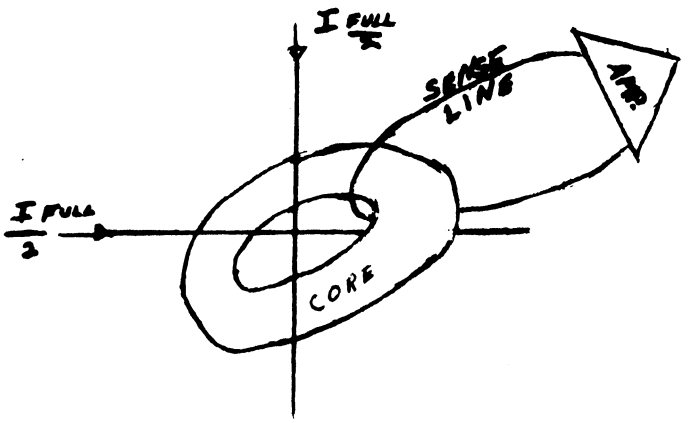


Figure 3

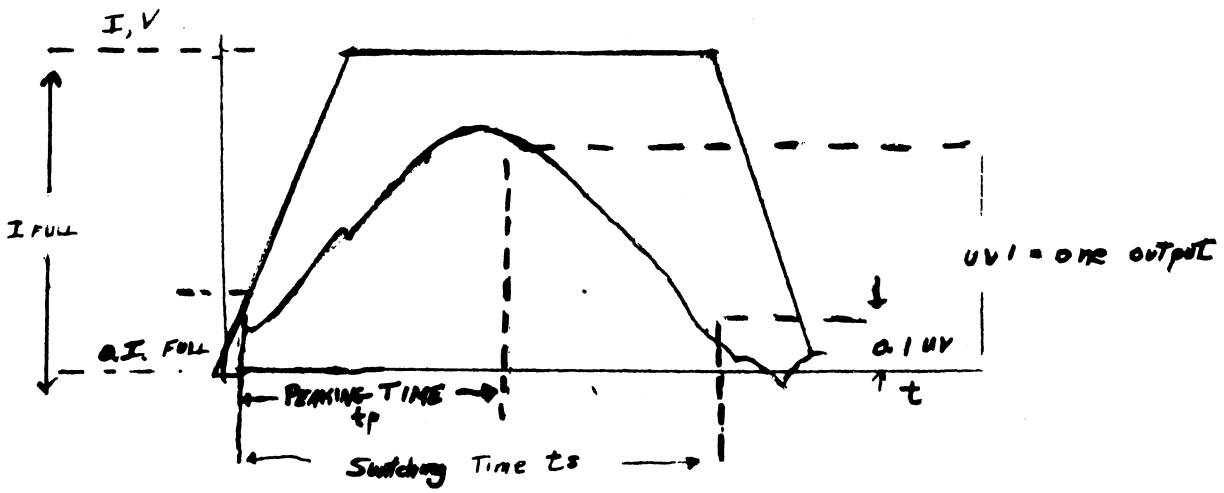


Figure 4

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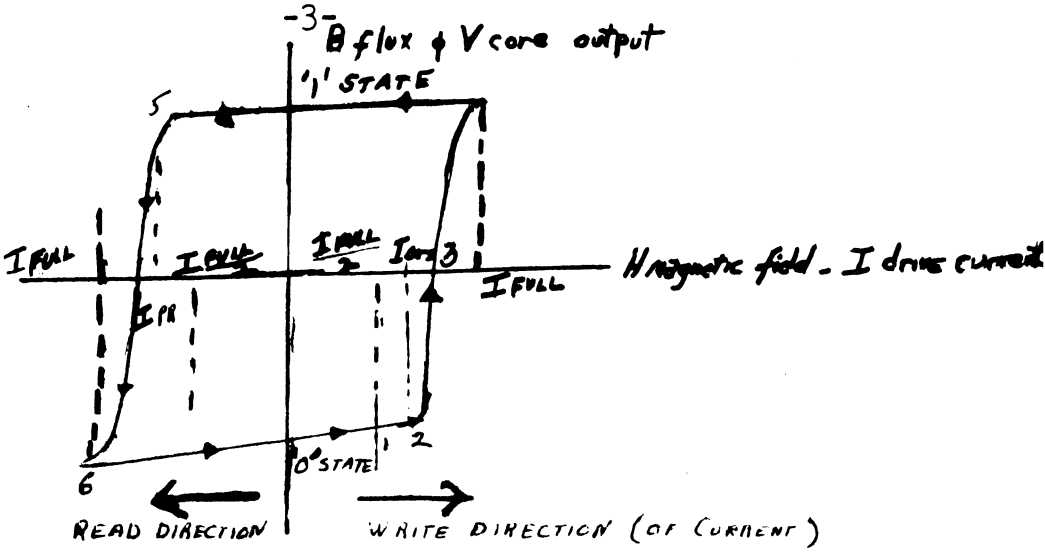

Figure 5

The core characteristic is referred to as a 'square' loop or B/H loop.

When the core is in the '0' state and current is applied in the write direction, you move out along the loop (Figure 5). If only $\frac{IFull}{2}$ (half select current) is applied, then you stop at pt. 1 on the loop and remain there while the current is sustained. When current is shut off, you return to the zero state. The flux change associated with this current is termed reversible flux change since when current is shut off, the flux changes reverse and core returns to the original state. If the applied current is greater than Ipw (partial write), you go over the 'knee' (pt.2) of the loop and you get into the region of nonreversible flux changes. This means that on shutting off current you return to some pt. other than the original state. The exact location of this point is fairly undefined but depends on the length of time for which current is sustained. Applying current which is greater than Ipw or Ipr (partial read) but less than IFull is referred

to as partial switching and is something which we never dare do in our systems.

If full select current is applied, then we move from initial state ('0') through pts 1, 2, 3 and 4 and remain at pt. 4 until the current is shut off at which time it returns to '1' state. In traversing along the loop from '0' state to '1' state, we have caused flux changes which give us a voltage output on the sense winding (see Figure 2). This core output is a regular one output. The first peak in the one output is the voltage associated with going from '0' state to pt. 2. These are reversible flux changes and because reversible flux changes are characterized by different magnetic domain movement in the core they occur faster than the irreversible changes and thus peak faster. Again in going from '0' state to one state we get the fastest rate of change of flux at pt. 3 and thus the maximum voltage output (core peak) at this point. On getting to pt. 4 the flux changes are over and so the voltage out is zero and the core is said to have been switched. As long as the current is sustained, the voltage out remains zero but shutting off the current causes us to move from pt. 4 to 1 state which causes a small flux change in the opposite direction and therefore a small voltage in the opposite polarity. This effect is not important and scarcely visible in stacks.

It is appropriate at this time to define two very important core paramenters:

PEAKING TIME: The time between the 10% point of the input current and the peak amplitude of the 1 output.

SWITCHING TIME: The time between the 10% pt. of input current and the second 10% pt. of the '1' output signal.

The cycle that I just went through is termed a write cycle as it's the one associated with passing full write current through the core.

The read cycle is the one associated with passing full current in the opposite direction through the core or that is in going from '1' state to '0' state. In this case exactly the same thing happens except that the flux changes are in the opposite direction and therefore the signal induced on the sense wire will be of opposite polarity. So from a core pulsed with full read and write current the output would look like (Figure 6).

Before I go on to talk about cores in memory stacks, I should mention something about temperature characteristics of cores. Basically it is this that the B/H loop of a core shrinks as the temperature increases and it gets larger as the temperature decreases.

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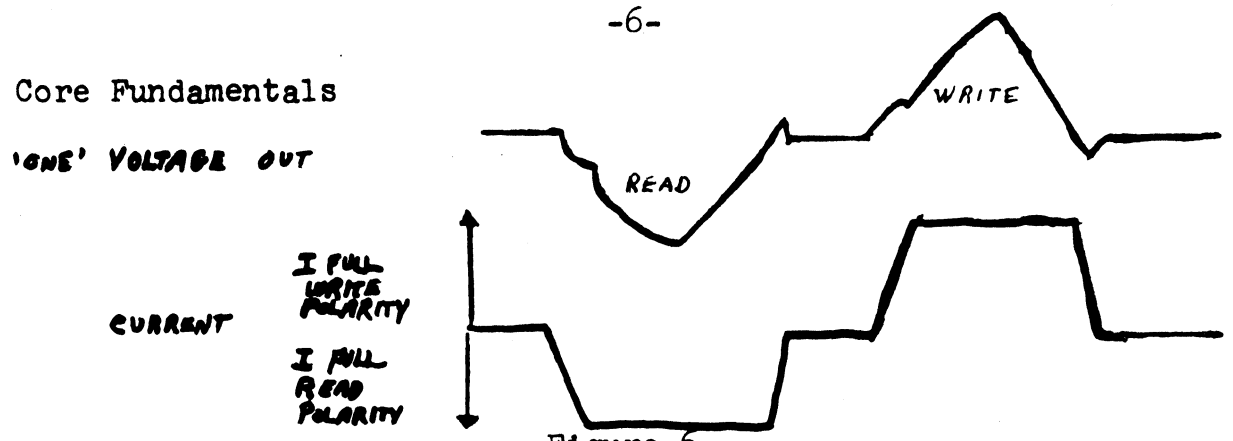

Figure 6

Obviously if we want to drive the core with the currents of the same relative magnitudes than we have to control our current ampltd. according to temperature. The amount of change in the loop is specified by the core manufacturer in %/OC of the driving current. Cores made of different materials have different temperature coefficients, the ones with the smallest T.C.'s of about 0.4 + 0.6%/oc.

I have only talked about one outputs - there are also zero outputs and when we come to cores in stacks, half-disturb outputs.

Zero Output: If we apply full read current to a core in the zero state then we move back along the loop to pt. 6 (Figure 5) but no matter how long we sustain the current, we will never move up to pt. 6 as 6 to 5 is an irreversible flux path in the opposite direction. However, since cores B/H loops are NOT square, the path from 0 state to pt. 6 has a slope and thus going from '0' to 6 cause flux change and voltage

on sense line. Obviously, the voltage peaks faster and is much smaller than the one output. (see Figure 2).

Cores in Stacked Arrays

All our core memories employ the coincident current technique. Assuming a 4K memory i.e. (4,096 memory words) we arrange 4,096 cores in a 64 X 64 array (see Figure 7).

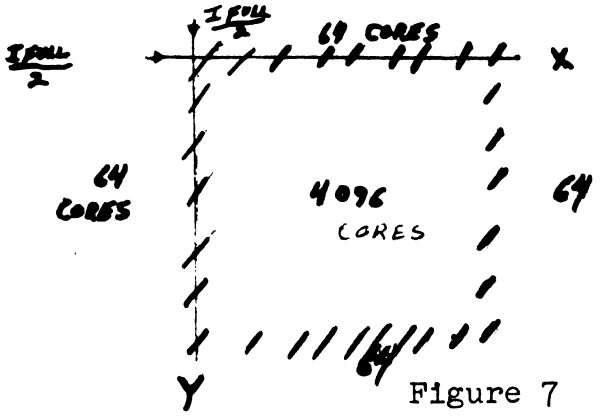

Figure 7

There are 64 horizontal and 64 vertical current carrying drive lines. We pass half current through them as shown and only the core at the intersection or coincidence of the two lines will see full select current. The other 63 cores on each axis see only half current and therefore don't change from their existing state. Any core in the 4,096 array can be uniquely selected by enabling the appropriate horizontal and vertical line. The direction of the current is controlled by switches which drive the lines. Current goes in one direction for a read and the opposite direction for a write.

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A sense winding which passes through the aperture of each core in the array senses the signal caused by the read current in the selected core. Knowing the '1' outputs are larger than '0' outputs we can establish a discriminating level and distinguish ones from zeros. So much for reading, with the same technique we can write ones the only difference being that we must reverse the current polarity. To write a zero in the selected core we must apply half current in the opposite direction to one of the drives so that the total current that the core sees is $\frac{1}{2} + \frac{1}{2} - \frac{1}{2} = \frac{1}{2}$ select and therefore, will remain in the zero state. The wire that carries this opposing or inhibiting current is called the INHIBIT and is wired in parallel to either the horizontal or vertical (X or Y) and threading all 4,096 cores.

Another alternative is to have no inhibit winding and not activate one of the X or Y lines so the core only sees a half select. This by the way, is one of the fundamentals of $2\frac{1}{2}D$.

READING:

When we select one core in a 64 X 64 array 63 cores in each of the X and Y lines see half current and are half-disturbed. We know that half selecting a core causes a core output which for a single core is small compared to the one output. Typical figures for a 30 mil core might be one output = 36 mv half distrub = 2 mv. Now we have 126 cores in the array give 2 my outputs and the

polarity of this output depends on whether the half disturbed cores store ones or zeros. Suppose they contain all ones or all zeros then in order that the 126 2mv outputs not be cumulative, we should pass the sense winding through half the cores in one direction and the other half in the opposite direction. This causes two 126 mv signals of opposite polarity on the sense line and therefore the sense winding sees a net effect of nothing. This is the basic idea employed in winding a sense wire and there are many crazy patterns possible to achieve it. Remember that it must fulfill this function for any combination of an X and Y line in the 4,096 array.

Now, if we open out the sense winding it becomes a long wire (typically = 20' for 4K) with 4,096 cores on it, 2,048 in one direction and 2,048 in the other (see Figure 8).

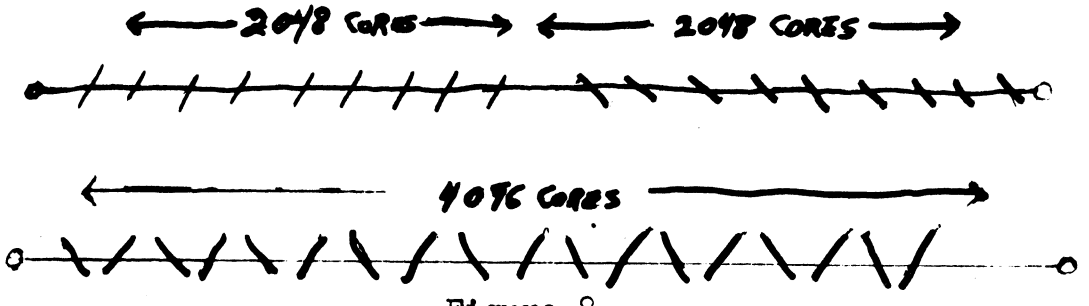

Figure 8

I haven't mentioned yet but in reading we like to examine the sense wire at the point in time where a 'one' peaks because at this time we get the greatest one ampltd. to zero ampltd. ratio and thus its easiest to discriminate at this point. We call this

sample time strobe time. What would happen if the sense wire went through all cores in the same direction?

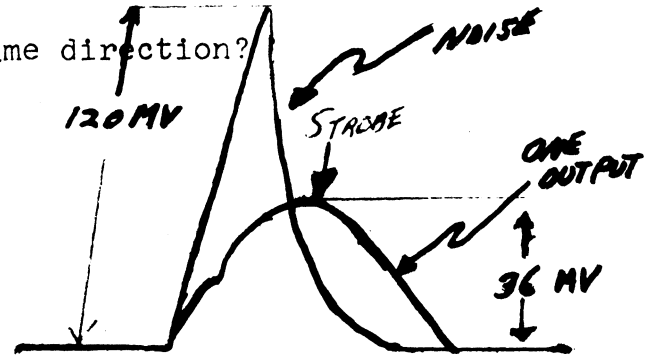

Figure 9

The cumulative half-disturbs would peak much faster than a one output (if you go back to the B/H loop, you can appreciate this). They would be much larger than the one (126/36) and due to the RC constant of the sense line would take a long time to fall down to zero. If the core we were reading out of stored a zero then the sense line would see the noise spike (Figure 9), plus a zero voltage. If it contained a one, it would see the same noise plus a one output. It is obvious that it would be impossible to discriminate between a one and a zero at any point, with this scheme.

Going back to the practical way of threading half the cores in different directions its numerous variations have each their own merits. If we used the scheme (Figure 8A) where the first 2,048 were in one direction, and the second 2,048 in the opposite direction, this has the disadvantage that it takes time for the current to propogate from one end of the drive line to the other (about 20 feet at the speed of light i.e., about

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INS per ft.) and therefore the outputs from the first 2,048 of one polarity would be displaced in time from the opposite polarity outputs of the second 2,048 and would not be perfectly cancelling. So the ideal way to arrange it would be as in (Figure 8B) where every other core was in the opposite direction and thus almost perfectly cancelling. Diagonal sense windings usually achieve this on every other pair, while rectangular or 'bow-tie' windings don't do as well, typically every other 64 or 128. More about these later.

WORST CASE PATTERN (WCP)

Now if every half-disturbed core is cancelled so nicely, how do we dream up a worst case pattern?

Well, the fact is that a half-disturbed one is slightly larger than a half-disturbed zero (typically about 0.3 mv for 30 mil core). This means that if we take our sense line with 4,096 cores, every other core in the opposite direction or polarity and drive current down an X and Y winding

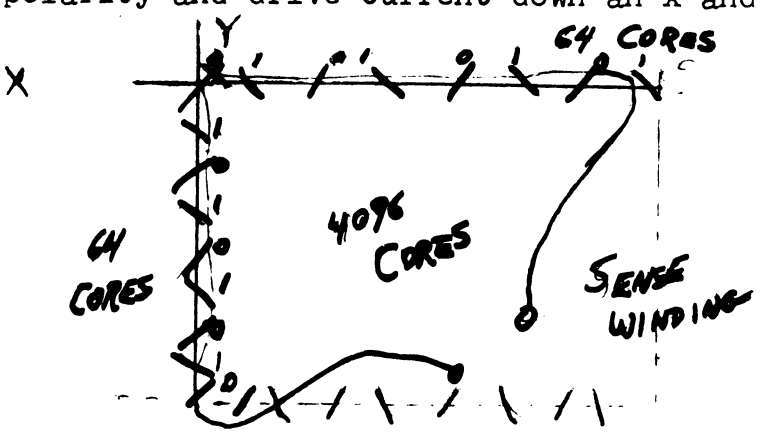

Figure 10

and already having the illustrated pattern in the 127 cores (this pattern is WCP). The 63 half-disturbed ones will appear as a pos. or neg. polarity signal, and the 63 half-disturbed zeros will appear as a neg. or pos. polarity signal and again, because taken singly each pair of ones and zeros don't cancel we will have a difference voltage of the same polarity as the ones, whose amplitude would be (0.3 mv) x 63 $\cong$ 19 mv. This unwanted signal is referred to as DELTA NOISE and as it is inherent in the cores. There is no way of getting rid of it even though there are ways of minimizing its effect. Because of the definition of WCP, it is implied that delta noise (Δ noise) will always be of the same polarity as the one output, when the WCP is stored in all cores. (4K)

A : WORST CASE PATTERN ONE

Because the noise is of the same polarity as the legitimate signal, the net output will be the sum of the two - this is why WCP ones are larger than a one output of all ones pattern.

A WORST CASE PATTERN ZERO

If the intersected core contains a zero, then the net output from this core will be Δ noise - zero output (typically 6mv) that is about 13 mv.

It is obvious from above that the effect of WCP is to

better the one outputs but worsen the zero outputs - hence it is appropriate that in margining a system we only use WCP to generate the maximum zeros. Any pattern between the'all-cancelling' ones patterns and the extreme of WCP contains a certain amount of delta noise which I said before was additive to the ones so that again in margining a system, the minimum ones are generated by an all one pattern.

This is all theoretical and in certain systems other constraints mask these theories.

Now suppose we can count through the 4,096 cores and read and write:

(1) All zeros

(2) All ones

(3) WCP

what should we see on the sense winding -:

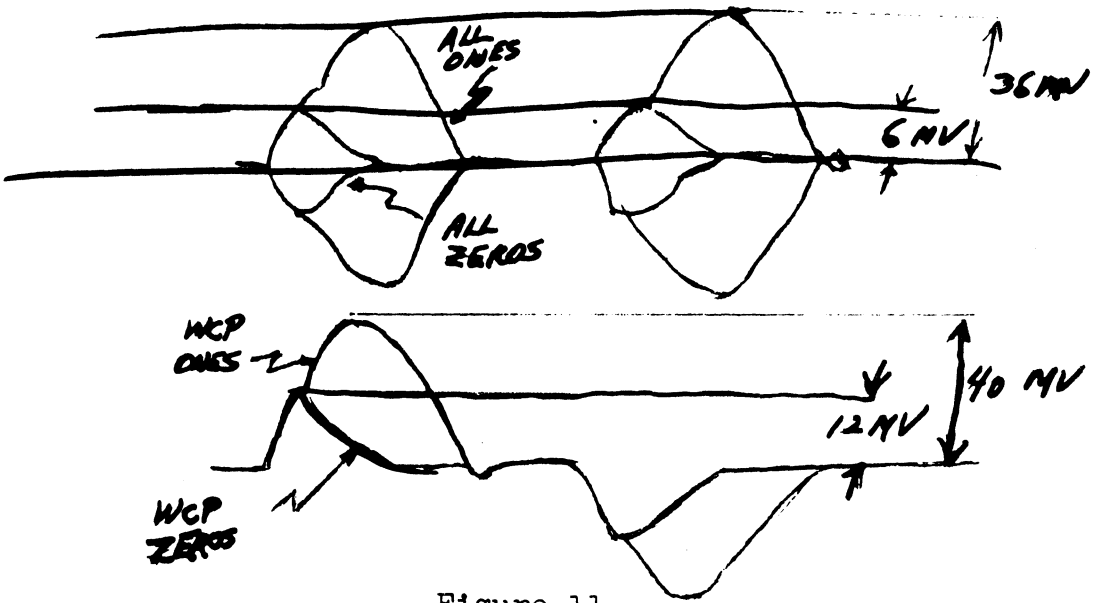

Figure 11

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These outputs are not real life outputs as you also see noise spikes on the output associated with read and write currents turning on and off, and much more so inhibit current turning on and off, that is if there be an inhibit in the particular organization (3D has one $2\frac{1}{4}$D does not)

These spikes are caused by transients (i.e. current turn on and off) in the drive lines which are indutively and capac itevly coupled to the sense line through the air and also through the cores themselves. Read and write transients never hurt too much because the common intersection of each to the sense line is that going through one horizontal and vertical drive line and 127 cores that are common to both. Because of the small intersection, the amplitude of the spike is small and it happens at turn on and off which is not near peak, and therefore is not critical.

However, because inhibit threads all 4K which sense threads its effect could be sid to be $\frac{4,096}{127} \simeq 32$ as great. As inhibit only happens at write time, this cannot affect the read voltage output, but inhibit current turning off induces a very large spike into sense amplifier; maybe 75 mv and the amplifier has to recover before it can accept the read output of the next cycle. A cycle is defined as a read write sequence in one address.

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A 2½D MEMORY

On 'pure' memory organizations, coincident current and linear select, the dimensions of the system may be clearly identified as being either address or data dimensions. For example, in all our core memory systems the X and Y dimensions are address and the inhibit, data. In 2½D there are only two dimensions X (word) and Y (digit or bit). The X dimension is address, but the Y serves the dual function of both address and data. This requires that the data be inserted on the address lines in onedimension during the write cycle requiring an independent driving system in one dimension for every bit or digit, hence this is called the bit or digit dimension.

ORGANIZATION

Each bit in this memory is not 64x128 as we would have in a 3D, 8K memory. The reason being that we would like to make both word and digit the same electrical length so that we get approximately equal rise time in both. By arranging each bit in 16x512, we attain this..

The stack is a two sided planar array rather than stacks of planes - it could be also assembled in a stacked or cubic array but planar is more economical. Unfolding the stack, it looks like this -:

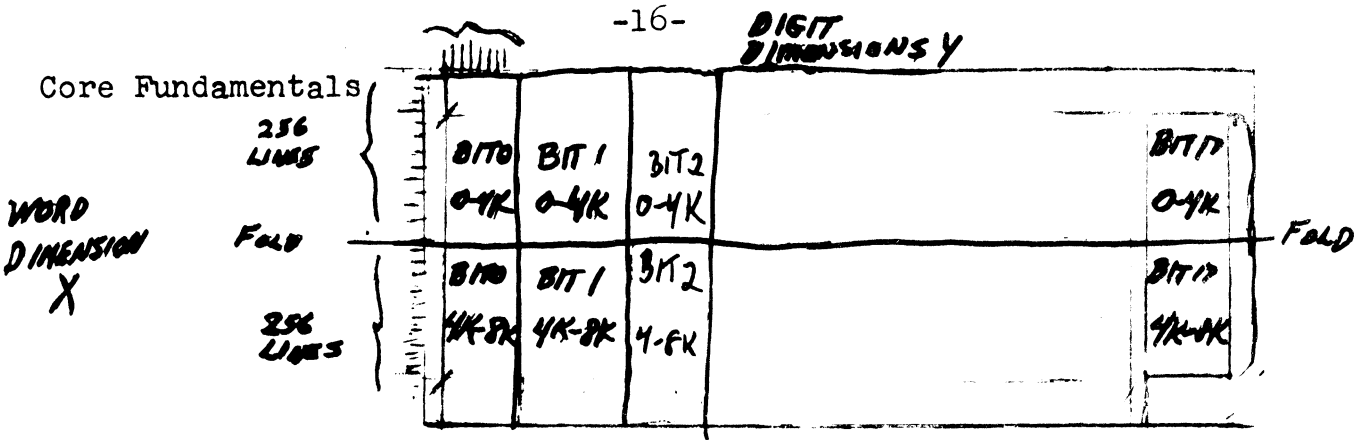

Figure 12

From this we can see that the word line has 16x18x2 = 576 cores on it and the digit 256x2 = 512 so that they are approximately balanced.

X (WORD) DIMENSION

This drive line is very similar to either the X or Y line in our conventional memory systems. It passes through a number of cores (32) in each of the 18 bits. Passing current down this line half selects 32 cores in each bit.

Y (BIT OR DIGIT) DIMENSION

This is the drive line with the dual function. Its address function can be likened to the word drive line and during read time it performs the same function, namely half selecting 512 cores in the bit. If this were its only function, it could be common for all bits but because during write it has to perform the function of an AUGMENT (or additive, opposite of INHIBIT) it has to be unique for each bit. Unique because we may want

different data in different bits.

Reading is characterized by applying a full select current to the intersected core. Writing of a one is the same but a zero causes no current to flow in the appropriate digit line.

SENSE WINDING:

There are two sense windings per bit or one per 4K cores. The sense winding is rectangular or 'bow-tie' as distinguished from the diagonal one in all our other memories. As far as I have seen, it is electrically much the same except that the noise induced by the digit turn on and off is larger than if it were diagonal. This is because it runs parallel to the digit drive for quite aways. It is less complicated to string and thus results in cheaper stacks.

STAGGER

Refer back to the Δ noise notes, we find that the squarer the bit plane or the closer the aspect ratio ($\frac{X}{Y}$) is to unity, the less the delta noise. So while we have 'balanced' electrical lines the Δ noise has greatly increased. The word drive half disturbs 15 cores outside the unselected one and this generates only seven pairs of Δ noise voltages plus one unmatched halfdisturb i.e. (7 x .3 mv) + 2mv $\cong$ 4 mv. The digit cause (127 x .3) + 2 mv $\cong$ 40 mv. So while the total Δ noise is

44 mv, the digit generates 95% of it. If we were to turn on digit and word read together, WCP zeros would be huge and undistinguishable from ones, so what we do is turn on digit 75 ns before word. This generates 95% of the Δ noise, but the core doesn't start to switch for 75 ns later by which time the Δ noise has decayed to a reasonable value. The time between digit read on and word read on is called STAGGER. As we only strobe read out-put and couldn't care about write, we don't waste the time staggering the writes.

WORD CURRENT PHASING

Looking again at fig. 12, you will notice that picking any word and any digit line you will have coincidence in not one but two cores. This does not mean that two cores will be switched each time, for the cores are arranged so that while the currents are coincident (additive) in one core, they are anti-coincident (subtractive) in the other and visa versa. This means that each word line drives two addresses, which one the currents are co-incident in, being determined by the PHASING (direction) of the word current. Current in one direction makes coincidence in an address in the first 4K, while current in the opposite direction makes coincidence in the corresponding address of the second 4K.

This means that we can drive 512 addresses with 256 lines.

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The most economical way to drive 256 lines is to break it up into a 16x16 matrix. Besides the normal memory address and read/write decoding on the matrix, we have to have an extra level for the phasing. Since the phase of the current is governed by whether we are addressing the upper or lower 4K, the extra level of decoding is MA BIT 5; the most significant bit of the 8K memory address bits.

PAUSE

The cycle times of most memories is specified as the read-rewrite cycle time. Most all of them can do a read pause write but its cycle is slower. Read-rewrite is where sense amp information is read into the memory buffer and immediately read is over it is rewritten. Read pause write is where the information is snet to the CP, modified, sent back and written, also called a read modify write. Our memory has no MB, so it can't rewrite and every cycle is a read pause write with a fixed pause. The length of the pause is governed by the cable delay to and from memory to CP and how long it takes the CP to increment the data (total $\cong$ 300 ns). Whether or not the data is incremented, we pause for this time between read and write.