





801

EOF1DZDQBCSEQ

00010000

770325

PDP10 411

20HDR1DZDQCDSEQ

00010000

770325



CO1

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDQC-D-D  
PRODUCT NAME: DQ11 INTERRUPT LOGIC TESTS  
DATE: MARCH 1977  
MAINTAINER: DIAGNOSTIC GROUP

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## 1. ABSTRACT

THE FUNCTION OF THE D011 DIAGNOSTICS ARE TO VERIFY THAT THE OPTION OPERATES ACCORDING TO SPECIFICATIONS.

THIS TEST CHECKS ALL POSSIBLE INTERRUPTS VERIFYING THAT AN INTERRUPT OCCURS WHEN IT SHOULD AND THAT ONE DOESN'T HAPPEN WHEN IT SHOULDN'T. ALSO THAT THE INTERRUPTS OCCUR TO THE CORRECT VECTOR. BASIC NPR FUNCTIONS ARE ALSO INCLUDED IN THIS TEST.

CURRENTLY THERE ARE SEVEN OFF LINE DIAGNOSTICS THAT ARE TO BE RUN IN SEQUENCE TO INSURE THAT IF AN ERROR SHOULD OCCUR IT WILL BE DETECTED AT AN EARLY STAGE AND INSURING THAT DIAGNOSIS OF ERROR WILL BE IMMEDIATE TO PROBLEM  
NOTE: ADDITIONAL DIAGNOSTICS MAY BE ADDED IN THE FUTURE.

## THE SEVEN DIAGNOSTICS ARE:

1. DZDQA [REV] BASIS R/W TEST #1
2. DZDQB [REV] BASIC R/W TEST #2
3. DZDQC [REV] BASIC NPR AND INTERRUPT TEST
4. DZDQD [REV] RECEIVER TRANSMITTER EXERCISER TEST
5. DZDQE [REV] MISC. RX AND TX TESTS. PLUS BCC TESTS.
6. DZDQF [REV] CHARACTER DETECT TESTS.
7. DZDQH [REV] CHARACTER LENGTH AND INTERRUPT TESTS.

THERE IS ALSO AN ONLINE TEST TO BE DISCUSSED LATER.

1. DZDQO [REV] ONLINE TEST. (ITEP OVERLAY)

AND A PARAMETER INPUT PROGRAM IS AVAILABLE

1. DZDQG [REV] D011 TRIAL PROGRAM (PARAMETER INPUT)

## 2. REQUIREMENTS

## 2.1 EQUIPMENT

ANY PDP11 FAMILY CPU (WITH MINIMUM 4K MEMORY)-WITH OR WITHOUT A HARDWARE SWITCH REGISTER (LOC. 177570) ASR 33 (OR EQUIVALENT)  
D011  
SYNC MODEM (ONLY REQUIRED FOR ONLINE TEST)

## 2.2 STORAGE

PROGRAM WILL LOAD AND RUN IN 4K OF MEMORY.



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LOCATION 1400 THRU 1600 ARE ESPECIALLY TO  
 BE NOTED AND TO BE UNTOUCHED BY OPERATOR  
 AFTER DQ11 TRIAL PROGRAM HAS BEEN EXECUTED.  
 OR AFTER THE "AUTO SIZING" HAS BEEN DONE.

### 3. LOADING PROCEEDURE

#### 3.1 METHOD

ALL PROGRAMS ARE IN ABSOLUTE FORMAT AND  
 ARE LOADED USING THE ABSOLUTE LOADER.

ABSOLUTE LOADER STARTING ADDRESS \*500

MEMORY \*  
 SIZE

4K	17
8K	37
12K	57
16K	77
20K	117
24K	137
28K	157

3.1.1 LOAD THE ADDRESS OF ABS. LOADER (LOC.XXX500)

3.1.2 THEN START

### 4. STARTING PROCEEDURE

A. LOAD LOC. 200

B. SET SWR TO ZERO FOR "AUTO SIZING" OR LEAVE  
 LEAVE SWR BIT 7=1 TO USE EXISTING PARAMETERS SET UP  
 BY DQ11 TRIAL PROGRAM OR A PREVIOUSLY RUN DQ11 DIAGNOSTIC  
 THAT USED THE "AUTO SIZING".  
 \*\*\*\*REFER TO SECTION 4.1 FOR SOFTWARE SWITCH REGISTER OPERATION  
 AND OPTIONS.\*\*\*\*

NOTE: THE SOFTWARE SWITCH REGISTER IS LOCATED AT LOC.176  
 SOFTWARE DISPLAY REGISTER IS LOCATED AT LOC.174

C. THEN START

THE PROGRAM WILL TYPE MAINDEC NAME AND PROGRAM NAME  
 IF THIS WAS THE FIRST START UP OF THE PROGRAM) AND ALSO  
 THE FOLLOWING:

"MAP OF DQ11 STATUS"  
 1400 160010  
 1402 152300  
 1404 160020  
 1406 150310

THE ABOVE IS ONLY AN EXAMPLE!



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THIS WOULD INDICATE THE STATUS TABLE STARTING AT ADD.  
 1400 IN THE PROGRAM. THE STATUS TABLE MUST BE VERIFIED BY THE  
 USER IF AUTO SIZING IS DONE. FOR INFORMATION OF STATUS  
 TABLE SEE SECTION 8.4 FOR HELP.

\*\*\*\*IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING  
 WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:  
 SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR'S OPTION)\*\*\*\*  
 NOTE: IF USING THE SOFTWARE SWITCH REGISTER WHEN A HARDWARE  
 SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL NOT  
 TYPE OUT THE TITLE.

THE PROGRAM WILL TYPE "R"  
 AND PROCEED TO RUN THE DIAGNOSTIC

#### 4.1 CONTROL SWITCH SETTINGS

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH  
 REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS  
 THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.  
 IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES  
 AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH  
 REGISTER (LOC. 176) IS USED.

#### CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH  
 REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY  
 DOING THE FOLLOWING:

- 1) TYPE CONTROL G (<G>); THIS WILL ALLOW THE TTY TO ENTER DATA INTO  
 LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS  
 OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE ''NEW=''' HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE  
 OF THE FOLLOWING AT THE TTY:
  - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>  
 (ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS  
 WILL BE ALLOWED)  
 IF A <CR> IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH  
 REGISTER CONTENTS WILL NOT BE CHANGED.
  - B) IF A CONTROL U (<U>) IS DEPRESSED THEN THE PROGRAM WILL SEND YOU  
 BACK TO STEP 2.

SW 15 SET: HALT ON ERROR  
 SW 14 SET: LOOP ON CURRENT TEST  
 SW 13 SET: INHIBIT ERROR PRINT OUT  
 SW 12 SET: INHIBIT TYPE OUT/BELL ON ERROR.  
 SW 11 SET: INHIBIT ITERATIONS



SW 10 SET: ESCAPE TO NEXT TEST  
 SW 09 SET: LOOP WITH CURRENT DATA  
 SW 08 SET: CATCH ERROR AND LOOP ON IT  
 SW 07 SET: USE PREVIOUS STATUS TABLE. CLR-DO AUTO SIZE.  
 SW 06 SET:  
 SW 05 SET:  
 SW 04 SET:  
 SW 03 SET:  
 SW 02 SET: LOCK ON SELECTED TEST  
 SW 01 SET: RESTART PROGRAM AT SELECTED TEST  
 SW 00 SET: RESELECT DQ11'S DESIRED ACTIVE.

## 4.1.2 SWITCH REGISTER RESTRICTIONS

SW 00 RESELECT DQ11'S DESIRED ACTIVE.  
 PLEASE NOTE THAT A MESSAGE IS TYPED  
 OUT FOR SWITCH REGISTER BEING EQUAL TO DQ11'S  
 ACTIVE. THIS MEANS IF THE SYSTEM HAS  
 FOUR DQ11S; BITS 00, 01, 02, 03 WILL  
 BE SET IN LOC "DQACTV". USING THIS  
 SWITCH ALTERS THAT LOCATION; THEREFORE  
 IF FOUR DQ11S ARE IN THE SYSTEM  
 \*\*\*DO NOT\*\*\* SET SWITCHS GREATER THAN  
 SW 03 IN THE UP POSITION. THIS WOULD BE  
 A FATAL ERROR. DO NOT SELECT MORE ACTIVE  
 DQ11S THAN HAS BEEN GIVEN INFORMATION  
 ABOUT IN TRIAL PROGRAM.

METHOD: A: LOAD ADDRESS 200  
 B: START WITH SW 00=1  
 C: PROGRAM WILL TYPE MESSAGE  
 D: CONTINUE THE BINARY NUMBER OF DQ11S DESIRED ACTIVE  
 EXAMPLE: 1=1 DQ11; 3=2 DQ11; 7=3 DQ11; 17=4 DQ11 37=5 DQ11 ETC.  
 E: NUMBER (IF VALID) WILL BE IN DATA LIGHTS (EXCLUDING 11/05, 11/04, 11/34)  
 F: CONTINUE WITH ANY OTHER SWITCH SETTINGS DESIRED.

SW 01 IT IS STRONGLY SUGGESTED THAT  
 AT LEAST ONE PASS HAS BEEN MADE  
 BEFORE TRYING TO SELECT A TEST  
 THAT IS NOT IN THE ORDER OF SEQUENCE  
 THE REASON BEING IS THAT THE  
 PROGRAM HAS TO CLEAR AREAS AND SET  
 UP PARAMETERS. ALSO WHEN A TEST IS  
 SELECTED ALWAYS START AT THE VERY  
 BEGINNING OF THAT TEST.

SW 09 LOOP ON CURRENT DATA:  
 THIS SWITCH WILL ONLY WORK IF  
 CALL "SCOPI" IS IN THAT TEST.  
 THE REASON BEING THAT MOST TESTS  
 DEAL WITH BLOCKS OF DIFFERENT DATA  
 TO BE SENT OR RECEIVED ALL AT ONCE  
 THUS IN BLOCK DATA; ONE PATTERN CANN'T BE SINGLED OUT.

## 4.1.3 SWITCH REGISTER PRIORITYS



## ERROR SWITCHES

1. SW 12 DELETE PRINT OUT/BELL ON ERROR.
2. SW 13 DELETE ERROR PRINTOUT.
3. SW 15 HALT ON THE ERROR.
4. SW 08 GOTO BEGINNING OF THE TEST.
5. SW 10 GOTO NEXT TEST ON ERROR.

\*\*\*\*HLT (ERROR) ROUTINE SUPPORTS <↑G> OPERATION\*\*\*\*

## SCOPE SWITCHES

1. SW 09 (IF ENABLED BY "SCOPI")
2. SW 14
3. SW 11

\*\*\*\*SCOPE ROUTINE WILL SUPPORT <↑G> OPERATION\*\*\*\*

## 4.2 STARTING ADDRESS

STARTING ADDRESS IS AT 000200  
THERE ARE NO OTHER STARTING ADDRESSES  
FOR THE DQ11 DIAGNOSTICS PREVIOUSLY MENTIONED

NOTE: IF ADDRESS 000042 IS NON-ZERO  
THE PROGRAM ASSUMES IT IS UNDER  
ACT11 OR DDP CONTROL AND WILL ACT ACCORDINGLY  
AFTER \*ALL\* AVAILABLE DQ11'S ARE TESTED  
THE PROGRAM WILL RETURN TO "DDP2" OR "ACT-11".

## 5. OPERATING PROCEDURE

WHEN PROGRAM IS INITIALLY STARTED MESSAGES AS DESCRIBED IN SECTION  
FOUR WILL BE PRINTED.

AND PROGRAM WILL BEGIN RUNNING THE  
DIAGNOSTIC

## 5.2 PROGRAM AND/OR OPERATOR ACTION

THE TYPICAL APPROACH SHOULD BE

1. HALT ON ERROR (VIA SW 15=1)  
WHEN EVER AN ERROR OCCURS
2. CLEAR SW 15
3. SET SW 14: (LOOP ON THIS TEST)
4. SET SW 13: (INHIBIT ERROR PRINT OUT)

THE TEST NUMBER AND PC WILL BE TYPED OUT AND  
POSSIBLY AN ERROR MESSAGE (THIS DEPENDS ON THE TEST)  
TO GIVE THE OPERATOR AN IDEA AS TO THE SOURCE OF THE  
PROBLEM. IF IT IS NECESSARY TO KNOW MORE INFORMATION  
CONCERNING THE ERROR REPORT; LOOK IN THE LISTING  
FOR THAT TEST NUMBER WHICH WAS TYPED OUT  
AND THEN NOTE THE PC OF THE ERROR REPORT  
THIS WAY THE EXACT FUNCTIONING OF THE TEST



CAN BE INTERPEDITED

## 6. ERRORS

AS DESCRIBED PREVIOUSLY THERE WILL ALWAYS BE A TEST NUMBER AND PC TYPED OUT AT THE TIME OF AN ERROR (PROVIDING SW 13=0 AND SW 12=0). IN MOST CASES ADDITIONAL INFORMATION WILL BE SUPPLIED THE THE ERROR MESSAGE WHICH IS TO GIVE THE OPERATOR AN INDICATION OF THE ERROR.

### 6.2 ERROR RECOVERY

IF FOR SOME REASON THE DQ11 SHOULD "HANG THE BUS" (GAIN CONTROL OF BUS SO THAT CONSOLE MANUAL FUNCTIONS ARE INHIBITED) AN INIT OR POWER DOWN/UP IS NECESSARY FOR OPERATOR TO REGAIN CONTROL OF CPU.  
IF THIS SHOULD HAPPEN; LOOK IN LOCATION "TSTNO" (ADDRESS 1226) FOR THE NUMBER OF THE TEST THAT WAS RUNNING AT THE TIME OF THE CATASTROPHIC ERROR.  
IN THIS WAY THE OPERATOR WILL HAVE AN IDEA AS TO WHAT THE DQ11 WAS DOING AT THE TIME OF THE ERROR.

### 6.3 \*\*\*\*HALT RECOVERY WHEN USING SOFTWARE SWITCH REGISTER\*\*\*\*

IF THE SOFTWARE SWITCH REGISTER IS TO BE CHANGED AFTER A HALT THE THE OPERATOR IS REQUIRED TO TYPE A <↑G> BEFORE DEPRESSING CONTINUE.  
THE FOLLOWING WILL BE TYPED:  
SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR OPTION)

## 7. RESTRICTIONS

### 7.1 STARTING RESTRICTIONS

SEE SECTION 4. (PLEASE)

### 7.2 OPERATING RESTRICTIONS

DQ11 TRIAL PROGRAM MUST BE RUN PRIOR TO THE FIRST AND ONLY THE FIRST RUNNING OF ANY DQ11 DIAGNOSTIC  
NOTE: IF NO PROGRAM OTHER THAN A DQ11 DIAGNOSTIC WAS LOADED AFTER DQ11 TRIAL OR IF CORE MEMORY HAS NOT BEEN CHANGED; OR IF THERE IS NO DQ11 CONFIGURATION CHANGES; THE DQ11 TRIAL PROGRAM NEED NEVER BE RUN AGAIN.  
HOWEVER IF ANY OF THE ABOVE HAVE BEEN VIOLATED THE DQ11 TRIAL PROGRAM MUST BE RUN AGAIN BEFORE RUNNING THE DIAGNOSTICS  
NOTE: AN ALTERNATIVE TO THE ABOVE IS ATTEMPTING THE "AUTO SIZING" WHEN PROGRAM IS INITIALLY STARTED WITH SW07=0.

## 8. MISCELLANEOUS



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8.1 EXECUTION TIME

8.2 PASS COMPLETE

WHEN THE DIAGNOSTIC HAS COMPLETED  
 A PASS THE FOLLOWING IS AN EXAMPLE  
 OF THE PRINT OUT TO BE EXPECTED.

END PASS DZDQC-D CSR: 160000 VEC: 300 PASSES: 000001 ERRORS: 000000

NOTE: THE NUMBERS FOR CSR AND VEC ARE  
 NOT NECESSARILY THE VALUES FOR THE DEVICE  
 THEY ARE ONLY FOR THIS EXAMPLE.

8.3 TST1 (MINI MONITOR)

THE VERY FIRST "TEST" (TST1)  
 IS \*NOT\* A TEST OF THE DQ11 HARDWARE  
 IT IS A MINI-MONITOR USED TO CYCLE DQ11 IN THE  
 SYSTEM THROUGH THE DIAGNOSTIC.

REMEMBER: TST1 IS NOT A TEST OF DQ11 HARDWARE!!!!!!!

8.4 KEY LOCATIONS

RETURN (1214) CONTAINS THE ADDRESS WHERE PROGRAM WILL  
 RETURN WHEN ITERATION COUNT IS REACHED  
 OR IF LOOP ON TEST IS ASSERTED.  
 NEXT (1216) CONTAINS THE ADDRESS OF THE NEXT TEST  
 TO BE PERFORMED.  
 TSTNO (1226) CONTAINS THE NUMBER OF THE TEST NOW  
 BEING PERFORMED.  
 RUN (1304) THE BIT IN "RUN" ALWAYS POINTS ONE  
 PAST THE DQ11 CURRENTLY BEING TESTED.  
 EXAMPLE:  
 (RUN) 1304/0000000001000000  
 MEANS THAT DQ11 NO.05 IS THE DQ11 NOW  
 RUNNING.

DQCROO-DQCR17  
 DQSTOO-DQST17  
 (1400)-(1476)

THESE LOCATIONS CONTAIN THE INFORMATION  
 NEEDED TO TEST UP TO 16 (DECIMAL) DQ11S  
 SEQUENTIALY. THEY CONTAIN THE CSR VECTOR  
 AND STATUS CONCERNING THE CONFIGURATION  
 OF EACH DQ11.

DQACTV (1500) EACH BIT SET IN THIS LOCATION INDICATES  
 THAT THE ASSOCIATED DQ11 WILL BE TESTED  
 IN TURN.

EXAMPLE:  
 (DQACTV) 1500/0000000000011111  
 MEANS THAT DQ11 NO. 00,01,02,03,04  
 WILL BE TESTED.

EXAMPLE:  
 (DQACTV) 1500/0000000000010001  
 MEANS THAT DQ11 NO. 00,04



DQCSR (1506) WILL BE TESTED.  
 CONTAINS THE RECEIVER CSR OF THE  
 CURRENT DQ11 UNDER TEST.  
 DQSTAT (1510) CONTAINS THE STATUS OF THE CURRENT  
 DQ11 UNDER TEST.  
 BIT 15 SET: TWO SYNC CHARS/ONE SYNC CHAR  
 BIT 14 SET: TEST JUMPER INSTALLED/NOT INSTALLED  
 BIT 13 SET: BB OPTION INSTALLED/NOT INSTALLED  
 BIT 12 SET: BA OPTION INSTALLED/NOT INSTALLED  
 BIT 11 SET: ACTIVE ON FIRST NON-SYNC/ACTIVE AFTER NO. OF SYNC  
 BIT 10 SET: AB OPTION INSTALLED/NOT INSTALLED  
 BIT 09 SET: ODD VRC/EVEN VRC  
 BIT 00-08 VECTOR "A" OF DEVICE

### B.5 \*\*\* METHOD OF AUTO SIZING \*\*\*

#### B.5.1 FINDING THE CONTROL STATUS REGISTER.

WHEN LOOKING FOR THE CSR IT IS NECESSARY TO TAKE CARE  
 THAT WHEN A CSR IS FOUND THAT IT IS INDEED A DQ11. THAT  
 IS THE METHOD OF MY MADNESS FOR THIS ROUTINE.  
 AN ATTEMPT TO CLEAR THE MISC. REGISTER IS TRIED  
 IF A TIME-OUT TRAP OCCURS POINTERS ARE UPDATED  
 AND ATTEMPTED AGAIN. IF NO TIME-OUT, THE RECEIVER "ACTIVE BIT" (BIT 12)  
 IS SET AND A #COMPARE# FOR BOTH SYNC1 AND SYNC 2 IS DONE  
 AT THE MISC. REGISTER. IF THEY ARE THERE THIS IS  
 A DQ11. THE INFORMATION IS STORED AWAY.

#### B.5.2 ONE SYNC BIT OR TWO?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE THE  
 PRESENTS OF ONE SYNC OR TWO. THE PROGRAM ASSUMES TWO SYNC  
 CHARS. NOTE: THIS ASSUMPTION MAY BE ALTERED AFTER AUTO SIZING  
 BY ALTERING BIT 15 IN APPRIOATE DQSTXX: LOCATION.

#### B.5.3 "BB" OPTION INSTALLED?

TO SENSE FOR THE "BB" OPTION THE PROGRAM SELECTS THE  
 CHARACTER DET. REGISTER AND THE LOADS IN ALL 1'S. IF  
 ANY ONE OR COMBINATION OF BITS ARE SET THE BB OPTION  
 IS ASSUMED TO EXIST.

#### B.5.4 "AB" OPTION INSTALLED?

TO SENSE FOR THE "AB" OPTION THE PROGRAM SELECTS THE  
 POLYNOMIAL REGISTER AND WRITES ALL 1'S INTO IT. IF ANY  
 ONE OR COMBINATION OF BITS ARE SET THE AB OPTION IS ASSUMED  
 TO EXIST.

#### B.5.5 "BA" OPTION INSTALLED?

TO SENSE FOR "BA" OPTION REQUEST TO SEND AND DATA TERMINAL  
 READY ARE SET. IF EITHER ONE OR BOTH ARE SET THE PROGRAM  
 ASSUMES THE BA OPTION EXISTES

#### B.5.6 JUMPER ON END OF CABLE?

THE PROGRAM CHECKS TO SEE IF EITHER OR BOTH CLEAR TO SEND AND CARRIER ARE SET; IF SO THE PROGRAM ASSUMES THE TEST JUMPER IS ON THE END OF THE CABLE.

8.5.7 ACTIVE ON FIRST NON-SYNC?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE FOR WHEN THE DQ11 GOES ACTIVE THE PROGRAM ASSUMES "ACTIVE ON FIRST NON-SYNC". NOTE: THIS CAN BE CHANGED BY ALTERING BIT 11 IN THE APPRIORATE DQSTXX: AFTER AUTO SIZING

8.5.8 SET FOR ODD OR EVEN PARITY?

AS ABOVE TOO MUCH HARDWARE IS NEED TO SENSE WHICH PARITY WAS SELECTED. SO THE PROGRAM ASSEMES ODD PARITY. NOTE: THIS CAN BE CHANGED BY ALTERING BIT 9 IN APPRIORATE DQSTXX: LOCATION. AFTER AUTO SIZING

8.5.9 FINDING THE VECTOR.

THE PROGRAM SETS "PRIMARY DONE" "SECONDAY DONE" AND "INTERUPT ENABLE" AND LOOKS FOR AN INTERUPT. IF IT INTERUPTS IT IS PICKED UP AND STORED AWAY. IF NO INTERUPT OCCURES THE PROGRAM ASSUMES VECTOR =300. THIS PROBLEM WILL BE FIXED IN ONE OF THE DIAGNOSTICS AND \*AUTO SIZING\* SHOULD BE REDONE TO GET THE CORRECT VECTOR.

9. PROGRAM DESCRIPTION

CONTAINED WITHIN LISTING

10. LISTING

FOLLOWING



MO1

532  
533  
534  
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542  
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567  
568  
569

177320

NON.EX=177320  
.ENABLE AMA

;MAINDEC-11-DZDQC-D/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST  
;COPYRIGHT 1975, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

;REVISED 16-DEC-76 BY R. BLACK

.; A)SUPPORTS SOFTWARE SWITCH REGISTER  
.; B)SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH REGISTER  
.; BY <IG>.

;STARTING PROCEDURE

;LOAD PROGRAM

;LOAD ADDRESS 000200

;PRESS START

;PROGRAM WILL TYPE "MAINDEC-11-DZDQC-D/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST"

;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED

;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE

;AND THEN RESUME TESTING

;SWITCH REGISTER OPTIONS

100000  
040000  
020000  
010000  
004000  
002000  
001000  
000400  
000100  
000040  
000020  
000010  
000004  
000002  
000001

SW15=100000

SW14=40000

SW13=20000

SW12=10000

SW11=4000

SW10=2000

SW09=1000

SW08=400

SW06=100

SW05=40

SW04=20

SW03=10

SW02=4

SW01=2

SW00=1

:=1,HALT ON ERROR  
:=1,LOOP ON CURRENT TEST  
:=1,INHIBIT ERROR TYPEOUT  
:=1,DELETE TYPEOUT/BELL ON ERROR.  
:=1,INHIBIT ITERATIONS  
:=1,ESCAPE TO NEXT TEST ON ERROR  
:=1,LOOP WITH CURRENT DATA  
:=1,LOOP ON ERROR

;LOCK ON TEST SELECT  
;RESTART PROGRAM AT SELECTED TEST  
;RESELECT DQ11 DESIRED ACTIVE  
;NOTE: THIS MUST NOT EXCEED ORIGINAL COUNT

```

570
571
572           ;REGISTER DEFINITIONS
573
574           000000      R0=%0           ;GENERAL REGISTER
575           000001      R1=%1           ;GENERAL REGISTER
576           000002      R2=%2           ;GENERAL REGISTER
577           000003      R3=%3           ;GENERAL REGISTER
578           000004      R4=%4           ;GENERAL REGISTER
579           000005      R5=%5           ;GENERAL REGISTER
580           000006      SP=%6          ;PROCESSOR STACK POINTER
581           000007      PC=%7          ;PROGRAM COUNTER
582
583           ;LOCATION EQUIVALENCIES
584
585           177570      DSWR= 177570    ;HARDWARE SWITCH REGISTER LOC.
586           177570      DLIGHTS=177570 ;HARDWARE DISPLAY REGISTER LOC.
587           177776      PS=177776     ;PROCESSOR STATUS WORD
588           001200      STACK=1200     ;START OF PROCESSOR STACK
589
590           ;INSTRUCTION DEFINITIONS
591
592           005746      PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
593           005726      POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
594           010046      PUSHRO=10046    ;SAVE R0 ON STACK
595           012600      POPRO=12600     ;RESTORE R0 FROM STACK
596           024646      PUSH2SP=24646  ;DECREMENT STACK TWICE
597           022626      POP2SP=22626   ;INCREMENT STACK TWICE
598           .EQUIV EMT,HLT ;BASIC DEFINITION OF ERROR CALL
599
600
601           100000      BIT15=100000
602           040000      BIT14=40000
603           020000      BIT13=20000
604           010000      BIT12=10000
605           004000      BIT11=4000
606           002000      BIT10=2000
607           001000      BIT9=1000
608           000400      BIT8=400
609           000200      BIT7=200
610           000100      BIT6=100
611           000040      BIT5=40
612           000020      BIT4=20
613           000010      BIT3=10
614           000004      BIT2=4
615           000002      BIT1=2
616           000001      BIT0=1
617
618           ;DQ11 OPTIONAL DEFINITIONS
619
620
621           002000      ABBIT=2000
622           004000      ACTBIT=4000
623           010000      BABIT=10000
624           020000      BBBIT=20000
625           040000      JMBIT=40000
  
```



626 001000 ODDBIT=1000  
 627 100000 SYNBIT=100000  
 628  
 629  
 630

;DQ11 SECONDARY REGISTER DEFINATIONS

631			
632	000000	RXBA.P=0	;RECEIVER BUS ADDRESS PRIMARY.
633	000001	RXWC.P=1	;RECEIVER WORD COUNT PRIMARY.
634	000002	TXBA.P=2	;TRANSMITTER BUS ADDRESS PRIMARY.
635	000003	TXWC.P=3	;TRANSMITTER BUS ADDRESS PRIMARY.
636	000004	RXBA.S=4	;RECEIVER BUS ADDRESS SECONDARY.
637	000005	RXWC.S=5	;RECEIVER WORD COUNT SECONDARY.
638	000006	TXBA.S=6	;TRANSMITTER BUS ADDRESS SECONDARY.
639	000007	TXWC.S=7	;TRANSMITTER WORD COUNT SECONDARY.
640			
641	000010	CHARDT=10	;CHARACTER DETECT REGISTER.
642	000011	SYNC.=11	;SYNC REGISTER.
643	000012	MISC.=12	;MISCELLANEOUS REGISTER.
644	000013	TX.MUX=13	;TRANSMITTER MUX REGISTER.
645	000014	SEQ.=14	;SEQUENCE REGISTER.
646	000015	RX.BCC=15	;RECEIVER BCC REGISTER.
647	000016	TX.BCC=16	;TRANSMITTER BCC REGISTER.
648	000017	POLY.=17	;POLYNOMIAL REGISTER.
649			
650			

```

        ;TRAPCATCAER FOR ILLEGAL INTERRUPTS
651      .=0
652      000000 000000
653      000000 000002      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
654      000002 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
655      000004 000006      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
656      000006 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
657      000010 000012      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
658      000012 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
659      000014 000016      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
660      000016 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
661      000020 000022      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
662      000022 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
663      000024 000026      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
664      000026 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
665      000030 000032      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
666      000032 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
667      000034 000036      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
668      000036 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
669      000040 000042      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
670      000042 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
671      000044 000046      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
672      000046 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
673      000050 000052      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
674      000052 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
675      000054 000056      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
676      000056 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
677      000060 000062      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
678      000062 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
679      000064 000066      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
680      000066 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
681      000070 000072      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
682      000072 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
683      000074 000076      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
684      000076 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
685      000100 000102      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
686      000102 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
687      000104 000106      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
688      000106 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
689      000110 000112      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
690      000112 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
691      000114 000116      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
692      000116 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
693      000120 000122      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
694      000122 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
695      000124 000126      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
696      000126 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
697      000130 000132      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
698      000132 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
699      000134 000136      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
700      000136 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
701      000140 000142      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
702      000142 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
703      000144 000146      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
704      000146 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
705      000150 000152      .+2      ; UNEXPECTED TRAP TO THIS LOCATION
706      000152 000000      HALT      ; EXAMINE STACK TO FIND CAUSE
    
```



707	000154	000156	.+2	:UNEXPECTED TRAP TO THIS LOCATION
708	000156	000000	HALT	:EXAMINE STACK TO FIND CAUSE
709	000160	000162	.+2	:UNEXPECTED TRAP TO THIS LOCATION
710	000162	000000	HALT	:EXAMINE STACK TO FIND CAUSE
711	000164	000166	.+2	:UNEXPECTED TRAP TO THIS LOCATION
712	000166	000000	HALT	:EXAMINE STACK TO FIND CAUSE
713	000170	000172	.+2	:UNEXPECTED TRAP TO THIS LOCATION
714	000172	000000	HALT	:EXAMINE STACK TO FIND CAUSE
715	000174	000176	.+2	:UNEXPECTED TRAP TO THIS LOCATION
716	000176	000000	HALT	:EXAMINE STACK TO FIND CAUSE
717	000200	000202	.+2	:UNEXPECTED TRAP TO THIS LOCATION
718	000202	000000	HALT	:EXAMINE STACK TO FIND CAUSE
719	000204	000206	.+2	:UNEXPECTED TRAP TO THIS LOCATION
720	000206	000000	HALT	:EXAMINE STACK TO FIND CAUSE
721	000210	000212	.+2	:UNEXPECTED TRAP TO THIS LOCATION
722	000212	000000	HALT	:EXAMINE STACK TO FIND CAUSE
723	000214	000216	.+2	:UNEXPECTED TRAP TO THIS LOCATION
724	000216	000000	HALT	:EXAMINE STACK TO FIND CAUSE
725	000220	000222	.+2	:UNEXPECTED TRAP TO THIS LOCATION
726	000222	000000	HALT	:EXAMINE STACK TO FIND CAUSE
727	000224	000226	.+2	:UNEXPECTED TRAP TO THIS LOCATION
728	000226	000000	HALT	:EXAMINE STACK TO FIND CAUSE
729	000230	000232	.+2	:UNEXPECTED TRAP TO THIS LOCATION
730	000232	000000	HALT	:EXAMINE STACK TO FIND CAUSE
731	000234	000236	.+2	:UNEXPECTED TRAP TO THIS LOCATION
732	000236	000000	HALT	:EXAMINE STACK TO FIND CAUSE
733	000240	000242	.+2	:UNEXPECTED TRAP TO THIS LOCATION
734	000242	000000	HALT	:EXAMINE STACK TO FIND CAUSE
735	000244	000246	.+2	:UNEXPECTED TRAP TO THIS LOCATION
736	000246	000000	HALT	:EXAMINE STACK TO FIND CAUSE
737	000250	000252	.+2	:UNEXPECTED TRAP TO THIS LOCATION
738	000252	000000	HALT	:EXAMINE STACK TO FIND CAUSE
739	000254	000256	.+2	:UNEXPECTED TRAP TO THIS LOCATION
740	000256	000000	HALT	:EXAMINE STACK TO FIND CAUSE
741	000260	000262	.+2	:UNEXPECTED TRAP TO THIS LOCATION
742	000262	000000	HALT	:EXAMINE STACK TO FIND CAUSE
743	000264	000266	.+2	:UNEXPECTED TRAP TO THIS LOCATION
744	000266	000000	HALT	:EXAMINE STACK TO FIND CAUSE
745	000270	000272	.+2	:UNEXPECTED TRAP TO THIS LOCATION
746	000272	000000	HALT	:EXAMINE STACK TO FIND CAUSE
747	000274	000276	.+2	:UNEXPECTED TRAP TO THIS LOCATION
748	000276	000000	HALT	:EXAMINE STACK TO FIND CAUSE
749	000300	000302	.+2	:UNEXPECTED TRAP TO THIS LOCATION
750	000302	000000	HALT	:EXAMINE STACK TO FIND CAUSE
751	000304	000306	.+2	:UNEXPECTED TRAP TO THIS LOCATION
752	000306	000000	HALT	:EXAMINE STACK TO FIND CAUSE
753	000310	000312	.+2	:UNEXPECTED TRAP TO THIS LOCATION
754	000312	000000	HALT	:EXAMINE STACK TO FIND CAUSE
755	000314	000316	.+2	:UNEXPECTED TRAP TO THIS LOCATION
756	000316	000000	HALT	:EXAMINE STACK TO FIND CAUSE
757	000320	000322	.+2	:UNEXPECTED TRAP TO THIS LOCATION
758	000322	000000	HALT	:EXAMINE STACK TO FIND CAUSE
759	000324	000326	.+2	:UNEXPECTED TRAP TO THIS LOCATION
760	000326	000000	HALT	:EXAMINE STACK TO FIND CAUSE
761	000330	000332	.+2	:UNEXPECTED TRAP TO THIS LOCATION
762	000332	000000	HALT	:EXAMINE STACK TO FIND CAUSE

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## TRAPCATCHER FOR UNEXPECTED INTERRUPTS

763	000334	000336	.+2	:UNEXPECTED TRAP TO THIS LOCATION
764	000336	000000	HALT	:EXAMINE STACK TO FIND CAUSE
765	000340	000342	.+2	:UNEXPECTED TRAP TO THIS LOCATION
766	000342	000000	HALT	:EXAMINE STACK TO FIND CAUSE
767	000344	000346	.+2	:UNEXPECTED TRAP TO THIS LOCATION
768	000346	000000	HALT	:EXAMINE STACK TO FIND CAUSE
769	000350	000352	.+2	:UNEXPECTED TRAP TO THIS LOCATION
770	000352	000000	HALT	:EXAMINE STACK TO FIND CAUSE
771	000354	000356	.+2	:UNEXPECTED TRAP TO THIS LOCATION
772	000356	000000	HALT	:EXAMINE STACK TO FIND CAUSE
773	000360	000362	.+2	:UNEXPECTED TRAP TO THIS LOCATION
774	000362	000000	HALT	:EXAMINE STACK TO FIND CAUSE
775	000364	000366	.+2	:UNEXPECTED TRAP TO THIS LOCATION
776	000366	000000	HALT	:EXAMINE STACK TO FIND CAUSE
777	000370	000372	.+2	:UNEXPECTED TRAP TO THIS LOCATION
778	000372	000000	HALT	:EXAMINE STACK TO FIND CAUSE
779	000374	000376	.+2	:UNEXPECTED TRAP TO THIS LOCATION
780	000376	000000	HALT	:EXAMINE STACK TO FIND CAUSE
781	000400	000402	.+2	:UNEXPECTED TRAP TO THIS LOCATION
782	000402	000000	HALT	:EXAMINE STACK TO FIND CAUSE
783	000404	000406	.+2	:UNEXPECTED TRAP TO THIS LOCATION
784	000406	000000	HALT	:EXAMINE STACK TO FIND CAUSE
785	000410	000412	.+2	:UNEXPECTED TRAP TO THIS LOCATION
786	000412	000000	HALT	:EXAMINE STACK TO FIND CAUSE
787	000414	000416	.+2	:UNEXPECTED TRAP TO THIS LOCATION
788	000416	000000	HALT	:EXAMINE STACK TO FIND CAUSE
789	000420	000422	.+2	:UNEXPECTED TRAP TO THIS LOCATION
790	000422	000000	HALT	:EXAMINE STACK TO FIND CAUSE
791	000424	000426	.+2	:UNEXPECTED TRAP TO THIS LOCATION
792	000426	000000	HALT	:EXAMINE STACK TO FIND CAUSE
793	000430	000432	.+2	:UNEXPECTED TRAP TO THIS LOCATION
794	000432	000000	HALT	:EXAMINE STACK TO FIND CAUSE
795	000434	000436	.+2	:UNEXPECTED TRAP TO THIS LOCATION
796	000436	000000	HALT	:EXAMINE STACK TO FIND CAUSE
797	000440	000442	.+2	:UNEXPECTED TRAP TO THIS LOCATION
798	000442	000000	HALT	:EXAMINE STACK TO FIND CAUSE
799	000444	000446	.+2	:UNEXPECTED TRAP TO THIS LOCATION
800	000446	000000	HALT	:EXAMINE STACK TO FIND CAUSE
801	000450	000452	.+2	:UNEXPECTED TRAP TO THIS LOCATION
802	000452	000000	HALT	:EXAMINE STACK TO FIND CAUSE
803	000454	000456	.+2	:UNEXPECTED TRAP TO THIS LOCATION
804	000456	000000	HALT	:EXAMINE STACK TO FIND CAUSE
805	000460	000462	.+2	:UNEXPECTED TRAP TO THIS LOCATION
806	000462	000000	HALT	:EXAMINE STACK TO FIND CAUSE
807	000464	000466	.+2	:UNEXPECTED TRAP TO THIS LOCATION
808	000466	000000	HALT	:EXAMINE STACK TO FIND CAUSE
809	000470	000472	.+2	:UNEXPECTED TRAP TO THIS LOCATION
810	000472	000000	HALT	:EXAMINE STACK TO FIND CAUSE
811	000474	000476	.+2	:UNEXPECTED TRAP TO THIS LOCATION
812	000476	000000	HALT	:EXAMINE STACK TO FIND CAUSE
813	000500	000502	.+2	:UNEXPECTED TRAP TO THIS LOCATION
814	000502	000000	HALT	:EXAMINE STACK TO FIND CAUSE
815	000504	000506	.+2	:UNEXPECTED TRAP TO THIS LOCATION
816	000506	000000	HALT	:EXAMINE STACK TO FIND CAUSE
817	000510	000512	.+2	:UNEXPECTED TRAP TO THIS LOCATION
818	000512	000000	HALT	:EXAMINE STACK TO FIND CAUSE



819	000514	000516	.+2	: UNEXPECTED TRAP TO THIS LOCATION
820	000516	000000	HALT	: EXAMINE STACK TO FIND CAUSE
821	000520	000522	.+2	: UNEXPECTED TRAP TO THIS LOCATION
822	000522	000000	HALT	: EXAMINE STACK TO FIND CAUSE
823	000524	000526	.+2	: UNEXPECTED TRAP TO THIS LOCATION
824	000526	000000	HALT	: EXAMINE STACK TO FIND CAUSE
825	000530	000532	.+2	: UNEXPECTED TRAP TO THIS LOCATION
826	000532	000000	HALT	: EXAMINE STACK TO FIND CAUSE
827	000534	000536	.+2	: UNEXPECTED TRAP TO THIS LOCATION
828	000536	000000	HALT	: EXAMINE STACK TO FIND CAUSE
829	000540	000542	.+2	: UNEXPECTED TRAP TO THIS LOCATION
830	000542	000000	HALT	: EXAMINE STACK TO FIND CAUSE
831	000544	000546	.+2	: UNEXPECTED TRAP TO THIS LOCATION
832	000546	000000	HALT	: EXAMINE STACK TO FIND CAUSE
833	000550	000552	.+2	: UNEXPECTED TRAP TO THIS LOCATION
834	000552	000000	HALT	: EXAMINE STACK TO FIND CAUSE
835	000554	000556	.+2	: UNEXPECTED TRAP TO THIS LOCATION
836	000556	000000	HALT	: EXAMINE STACK TO FIND CAUSE
837	000560	000562	.+2	: UNEXPECTED TRAP TO THIS LOCATION
838	000562	000000	HALT	: EXAMINE STACK TO FIND CAUSE
839	000564	000566	.+2	: UNEXPECTED TRAP TO THIS LOCATION
840	000566	000000	HALT	: EXAMINE STACK TO FIND CAUSE
841	000570	000572	.+2	: UNEXPECTED TRAP TO THIS LOCATION
842	000572	000000	HALT	: EXAMINE STACK TO FIND CAUSE
843	000574	000576	.+2	: UNEXPECTED TRAP TO THIS LOCATION
844	000576	000000	HALT	: EXAMINE STACK TO FIND CAUSE
845	000600	000602	.+2	: UNEXPECTED TRAP TO THIS LOCATION
846	000602	000000	HALT	: EXAMINE STACK TO FIND CAUSE
847	000604	000606	.+2	: UNEXPECTED TRAP TO THIS LOCATION
848	000606	000000	HALT	: EXAMINE STACK TO FIND CAUSE
849	000610	000612	.+2	: UNEXPECTED TRAP TO THIS LOCATION
850	000612	000000	HALT	: EXAMINE STACK TO FIND CAUSE
851	000614	000616	.+2	: UNEXPECTED TRAP TO THIS LOCATION
852	000616	000000	HALT	: EXAMINE STACK TO FIND CAUSE
853	000620	000622	.+2	: UNEXPECTED TRAP TO THIS LOCATION
854	000622	000000	HALT	: EXAMINE STACK TO FIND CAUSE
855	000624	000626	.+2	: UNEXPECTED TRAP TO THIS LOCATION
856	000626	000000	HALT	: EXAMINE STACK TO FIND CAUSE
857	000630	000632	.+2	: UNEXPECTED TRAP TO THIS LOCATION
858	000632	000000	HALT	: EXAMINE STACK TO FIND CAUSE
859	000634	000636	.+2	: UNEXPECTED TRAP TO THIS LOCATION
860	000636	000000	HALT	: EXAMINE STACK TO FIND CAUSE
861	000640	000642	.+2	: UNEXPECTED TRAP TO THIS LOCATION
862	000642	000000	HALT	: EXAMINE STACK TO FIND CAUSE
863	000644	000646	.+2	: UNEXPECTED TRAP TO THIS LOCATION
864	000646	000000	HALT	: EXAMINE STACK TO FIND CAUSE
865	000650	000652	.+2	: UNEXPECTED TRAP TO THIS LOCATION
866	000652	000000	HALT	: EXAMINE STACK TO FIND CAUSE
867	000654	000656	.+2	: UNEXPECTED TRAP TO THIS LOCATION
868	000656	000000	HALT	: EXAMINE STACK TO FIND CAUSE
869	000660	000662	.+2	: UNEXPECTED TRAP TO THIS LOCATION
870	000662	000000	HALT	: EXAMINE STACK TO FIND CAUSE
871	000664	000666	.+2	: UNEXPECTED TRAP TO THIS LOCATION
872	000666	000000	HALT	: EXAMINE STACK TO FIND CAUSE
873	000670	000672	.+2	: UNEXPECTED TRAP TO THIS LOCATION
874	000672	000000	HALT	: EXAMINE STACK TO FIND CAUSE

875	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
876	000676	000000	HALT	:EXAMINE STACK TO FIND CAUSE
877	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
878	000702	000000	HALT	:EXAMINE STACK TO FIND CAUSE
879	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
880	000706	000000	HALT	:EXAMINE STACK TO FIND CAUSE
881	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
882	000712	000000	HALT	:EXAMINE STACK TO FIND CAUSE
883	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
884	000716	000000	HALT	:EXAMINE STACK TO FIND CAUSE
885	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
886	000722	000000	HALT	:EXAMINE STACK TO FIND CAUSE
887	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
888	000726	000000	HALT	:EXAMINE STACK TO FIND CAUSE
889	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
890	000732	000000	HALT	:EXAMINE STACK TO FIND CAUSE
891	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
892	000736	000000	HALT	:EXAMINE STACK TO FIND CAUSE
893	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
894	000742	000000	HALT	:EXAMINE STACK TO FIND CAUSE
895	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
896	000746	000000	HALT	:EXAMINE STACK TO FIND CAUSE
897	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
898	000752	000000	HALT	:EXAMINE STACK TO FIND CAUSE
899	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
900	000756	000000	HALT	:EXAMINE STACK TO FIND CAUSE
901	000758	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
902	000762	000000	HALT	:EXAMINE STACK TO FIND CAUSE
903	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
904	000766	000000	HALT	:EXAMINE STACK TO FIND CAUSE
905	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
906	000772	000000	HALT	:EXAMINE STACK TO FIND CAUSE
907	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
908	000776	000000	HALT	:EXAMINE STACK TO FIND CAUSE



# H02

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 DZDQCD.P11 16-DEC-76 13:26 ROUTINES USED FOR AUTO SIZING.

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909                                     ;STANDARD INTERRUPT VECTORS
910
911                                     .=24
912 000024 014564                       .PFAIL                       ;POWER FAIL HANDLER
913 000026 000340                       340                          ;SERVICE AT LEVEL 7
914 000030 014234                       .HLT                          ;ERROR HANDLER
915 000032 000340                       340                          ;SERVICE AT LEVEL 7
916 000034 014202                       .TRPSRV                       ;GENERAL HANDLER DISPATCH SERVICE
917 000036 000340                       340                          ;SERVICE AT LEVEL 7
918                                     .=46
919 000046 012762                       LOGICAL                       ;ACT HOOKS
920                                     .=52
921 000052 000000                       .WORD 0
922                                     ;THIS ROUTINE TRIES TO FORCE THE RECEIVER TO INTERRUPT
923                                     ;TO ITS VECTOR WHERE IT WILL PICK UP THE STATUS LOCATION
924                                     ;FOR ITS NEW PC; AND PICK UP AN IOT INSTRUCTION FOR ITS
925                                     ;NEW PS. WHEN THE NEW PC IS FETCHED AN IOT INSTRUCTION IS
926                                     ;EXECUTED, TRAPPING TO LOCATION 20 WHERE A ROUTINE IS EXECUTED
927                                     ;TO TAKE THE PC FROM THE STACK AND US IT AS THE VECTOR ADDRESS
928 000056                                     .=56
929
930 VECMAP:
931 000056 010120 000004 1$           MOV R1,(R0)+                ;START FILLING THE VECTOR AREA
932 000060 012721 000004 1$           MOV #4,(R1)+                ;WITH +2; IOT (4)
933 000064 022021 001000 1$           CMP (R0)+,(R1)+            ;UPDATE THE POINTERS
934 000066 020127 001000 1$           CMP R1,#1000                ;IS ALL FLOATING VECTOR AREA DONE
935 000072 101771 000020 000020 1$   BLOS #4$,#20                ;BR IF NOT ALL DONE
936 000074 012737 000146 000020 1$   MOV #4$,#20                 ;SET FOR IOT TRAP BY DQ11
937 000102 013737 001500 001244 2$   MOV DQACTV,TEMP1           ;GET THE ACTIVE DQ11 S
938 000110 006037 001244 2$           ROR TEMP1                   ;ARE YOU ACTIVE.. DQ11
939 000114 103023 177776 2$           BCC 5$                      ;IF CARRY CLEAR.. NO MORE DQ11S
940 000116 005037 177776 2$           CLR PS                      ;CLEAR PS
941 000122 005722 000340 177776 3$   TST (R2)+                   ;PUT POINTER TO STATUS TABLE
942 000124 012772 000340 177776 3$   MOV #340,#-2(R2)           ;TRY AND SET PRI/SEC DONE AND IE
943 000132 105200 000300 3$           INCB RO                     ;DELAY.....
944 000134 001376 000300 3$           BNE #-2                     ;.....DELAY
945 000136 112712 000300 3$           MOVB #300,(R2)              ;NO INTERRUPT ASSUME 300 FIX IN TEST C
946 000142 005722 000142 4$           TST (R2)+                   ;UPDATE POINTERS
947 000144 000761 000142 4$           BR 2$                       ;GO DO IT AGAIN
948 000146 051612 000007 4$           BIS (SP),(R2)               ;ENTERD BY IOT TRAP BY DQ11
949 000150 042712 000007 4$           BIC #7,(R2)                 ;CLEAR UNWANTED BITS
950 000154 022626 000142 5$           CMP (SP)+,(SP)+            ;POP IOT JUNK OFF STACK
951 000156 012716 000142 5$           MOV #3$, (SP)              ;SET RETURN PC ON STACK
952 000162 000002 000142 5$           RTI                         ;GO HOME
953 000164 000207 000142 5$           RTS PC                      ;ALL SIZING IS DONE
954
955 ;***SOFTWARE SWITCH REGISTER***
956                                     .=174
957 000174 000000 000174 5$           DISPREG: 0                  ;SOFTWARE DISPLAY REGISTER
958 000176 000000 000174 5$           SWREG: 0                    ;SOFTWARE SWITCH REGISTER
959
960 ;PROGRAM START
961
962                                     .=200
963 000200 000137 001512 200           JMP .START                  ;GO TO START OF PROGRAM
964

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1021 000540 012737 000006 000004      MOV      #6, R4      ;RESET TIME OUT VECTOR
1022 000546 013737 001500 001502      MOV      DQACTV, SAVACT ;SAVE ACTIVE
1023 000554 012737 000340 000022      MOV      #340, R22   ;SET IOT TRAP PRIO: TO 7
1024 000562 012702 001400      MOV      #1400, R2   ;SET TABLE POINTER
1025 000566 012700 000300      MOV      #300, R0    ;SET VECTOR START
1026 000572 012701 000302      MOV      #302, R1    ;SET VECTOR+2 START
1027 000576 000137 000056      JMP      VECMAP      ;GO FIND THE VECTORS
1028 000602 104402      4S:     TYPE        ;TYPE MESSAGE
1029 000604 015125      MERR2    ;I DIDN'T FIND ANY DQ11S. DON'T USE AUTO SIZE.
1030 000606 005000      CLR      R0
1031 000610 000000      HALT
1032 000612 000776      BR      -2           ;HOW CAN I TEST NO DQ11S
1033 000614 012716 000466      5S:     MOV      #25, (SP) ;DON'T LET OPR HIT CONT. SW
1034 000620 000002      RTI          ;ENTERED BY TIME OUT TRAP
1035
1036
1037
1038 001000 005377 040515 047111      .=1000  ;MTITLE: .ASCIZ <377><12>/MAINDEC-11-DZDQC-D/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST/<37
1039 001006 042504 026503 030461
1040 001014 042055 042132 041521
1041 001022 042055 042377 030521
1042 001030 020061 047111 042524
1043 001036 051122 050125 020124
1044 001044 047101 020104 050116
1045 001052 020122 047514 044507
1046 001060 020103 042524 052123
1047 001066 000377
1048
1049      001200      .=1200
1050      ;INDIRECT POINTERS
1051
1052 001200 177570      SWR:     177570      ;SWITCH REGISTER POINTER
1053 001202 177570      LIGHTS: 177570      ;DISPLAY REGISTER POINTER
1054 001204 177560      TKCSR:   177560      ;TELETYPE KEYBOARD CONTROL REGISTER
1055 001206 177562      TKDBR:   177562      ;TELETYPE KEYBOARD DATA BUFFER
1056 001210 177564      TPCSR:   177564      ;TELEPRINTER CONTROL REGISTER
1057 001212 177566      TPDBR:   177566      ;TELEPRINTER DATA BUFFER
1058
1059      ;PROGRAM CONTROL PARAMETERS
1060
1061 001214 000000      RETURN:  0           ;SCOPE ADDRESS FOR LOOP ON TEST
1062 001216 000000      NEXT:    0           ;ADDRESS OF NEXT TEST TO BE EXECUTED
1063 001220 000000      LOCK:    0           ;ADDRESS FOR LOCK ON CURRENT DATA
1064 001222 000003      ICOUNT:  3           ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE EXECUTED
1065 001224 000000      LPCNT:   0           ;NUMBER OF ITERATIONS COMPLETED
1066 001226 000000      TSTNO:   0           ;NUMBER OF TEST IN PROGRESS
1067 001230 000000      PASCNT:  0           ;NUMBER OF PASSES COMPLETED
1068 001232 000000      ERRCNT:  0           ;TOTAL NUMBER OF ERRORS
1069 001234 000000      LSTERR:  0           ;PC OF LAST ERROR CALL
1070
1071      ;PROGRAM VARIABLES
1072
1073 001236 000000      CHAR1:   0
1074 001240 000000      CHAR2:   0
1075 001242 000000      CHAR3:   0
1076 001244 000000      TEMP1:   0           ;TEMPORARY STORAGE
    
```

K02

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PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

1077	001246	000000	TEMP2:	0	: TEMPORARY STORAGE
1078	001250	000000	TEMP3:	0	: TEMPORARY STORAGE
1079	001252	000000	TEMP4:	0	: TEMPORARY STORAGE
1080	001254	000000	TEMP5:	0	: TEMPORARY STORAGE
1081	001256	000000	SAVR0:	0	: R0 STORAGE
1082	001260	000000	SAVR1:	0	: R1 STORAGE
1083	001262	000000	SAVR2:	0	: R2 STORAGE
1084	001264	000000	SAVR3:	0	: R3 STORAGE
1085	001266	000000	SAVR4:	0	: R4 STORAGE
1086	001270	000000	SAVR5:	0	: R5 STORAGE
1087	001272	000000	SAVSP:	0	: STACK POINTER STORAGE
1088	001274	000000	SAVPC:	0	: PROGRAM COUNTER STORAGE
1089	001276	000000	SAVNUM:	0	
1090	001300	000001	CREAM:	.BLKW 1	
1091	001302	000000	RUNFLG:	0	
1092	001304	000000	RUN:	0	
1093	001306	000000	RUNCNT:	0	



```

1094
1095
1096
1097 001310 000
1098 001311 000
1099 001312 000
1100 001313 000
1101 000000
1102
1103
1104
1105
1106
1107
1108
1109 001314
1110 104400
1111 001314 013036
1112 104401
1113 001316 013150
1114 104402
1115 001320 013170
1116 104403
1117 001322 013276
1118 104404
1119 001324 013414
1120 104405
1121 001326 013446
1122 104406
1123 001330 013662
1124 104407
1125 001332 013722
1126 104410
1127 001334 013754
1128 104411
1129 001336 013760
1130 104412
1131 001340 015620
1132 104413
1133 001342 015636
1134 104414
1135 001344 014662
1136 104415
1137 001346 014736
1138
1139
1140
1141
1142
1143
1144 001350 000000
1145 001352 000000
1146 001354 000000
1147 001356 000000
1148 001360 000000
1149 001362 000000

;PROGRAM CONTROL FLAGS
INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
STFLG: .BYTE 0 ;TEST START FLAG
ERRFLG: .BYTE 0 ;ERROR OCCURED FLAG
LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
SY=0

;DEFINITIONS FOR TRAP SUBROUTINE CALLS
;POINTERS TO SUBROUTINES CAN BE FOUND
;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

;*****
;*****
TRPTAB:
SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
;SCOPE
SCOPI=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
;SCOPI
TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
;TYPE
INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
;INSTR
INSTER=TRAP+4 ;CALL TO INPUT ERROR HANDLER
;INSTER
PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
;PARAM
SAVDS=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
;SAVDS
RESOS=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
;RESOS
CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
;CONVRT
CNVRT=TRAP+11 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF.
;CNVRT
MSTCLR=TRAP+12 ;CALL TO ISSUE MASTER CLEAR
;MSTCLR
MEMCLR=TRAP+13 ;CALL TO CLEAR ALL SCRATCH PAD MEMORIES
;MEMCLR
CKSWR=TRAP+14 ;CALL TO ALLOW SWREG TO BE LOADED FROM TTY
;CKSWR
CNTLU=TRAP+15 ;CALL TO ALLOW LOADING OF SWREG FROM TTY
;CNTLU

;*****
;*****

;DQ11 VECTOR AND REGISTER INDIRECT POINTERS
DQVVEC: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT VECTOR
DQRLVL: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT SERVICE PS
DQTVVEC: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT VECTOR
DQTLVL: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT SERVICE PS
DQRCR: 0 ;POINTER TO DQ11 RECEIVER CONTROL REGISTER
DQRCSH: 0 ;POINTER TO HIGH BYTE OF DQ11 RECEIVER CONTROL REGISTER

```

# M02

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PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

1150	001364	000000	DQTCR:	0	: POINTER TO DQ11 TRANSMITTER CONTROL REGISTER
1151	001366	000000	DQERR:	0	: POINTER TO DQ11 ERROR REGISTER
1152	001370	000000	DQREG:	0	: POINTER TO HIGH BYTE OF ERROR REGISTER
1153	001372	000000	DQSEC:	0	: POINTER TO DQ11 SECONDARY REGISTER
1154	001374	000000	DQSECH:	0	: POINTER TO HIGH BYTE OF DQ11 SECONDARY REGISTER

;DQ11 STATUS TABLE AND ADDRESS ASSIGNMENTS

1160		001400	.=1400			
1161	001400	000001	DQCR00:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 00
1162	001402	000001	DQST00:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 00
1163	001404	000001	DQCR01:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 01
1164	001406	000001	DQST01:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 01
1165	001410	000001	DQCR02:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 02
1166	001412	000001	DQST02:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 02
1167	001414	000001	DQCR03:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 03
1168	001416	000001	DQST03:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 03
1169	001420	000001	DQCR04:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 04
1170	001422	000001	DQST04:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 04
1171	001424	000001	DQCR05:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 05
1172	001426	000001	DQST05:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 05
1173	001430	000001	DQCR06:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 06
1174	001432	000001	DQST06:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 06
1175	001434	000001	DQCR07:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 07
1176	001436	000001	DQST07:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 07
1177	001440	000001	DQCR10:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 10
1178	001442	000001	DQST10:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 10
1179	001444	000001	DQCR11:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 11
1180	001446	000001	DQST11:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 11
1181	001450	000001	DQCR12:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 12
1182	001452	000001	DQST12:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 12
1183	001454	000001	DQCR13:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 13
1184	001456	000001	DQST13:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 13
1185	001460	000001	DQCR14:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 14
1186	001462	000001	DQST14:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 14
1187	001464	000001	DQCR15:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 15
1188	001466	000001	DQST15:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 15
1189	001470	000001	DQCR16:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 16
1190	001472	000001	DQST16:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 16
1191	001474	000001	DQCR17:	.BLKW	1	: CONTROL STATUS REGISTER FOR DEVICE NO: 17
1192	001476	000001	DQST17:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS FOR DEVICE NO: 17
1193	001500	000001	DQACTV:	.BLKW	1	: HOLD ACTIVE BITS FOR TESTING
1194	001502	000001	SAVACT:	.BLKW	1	: SAVE NUMBER OF ACTIVE DQ11S
1195	001504	000001	DQNUM:	.BLKW	1	: OCTAL NUMBER OF TOTAL NUMBER OF DQ11S
1196	001506	000001	DQCSR:	.BLKW	1	: CSR OF DQ11 UNDER TEST
1197	001510	000001	DQSTAT:	.BLKW	1	: VECTOR AND CONFIGURATION STATUS OF DQ11 UNDER TEST

1198						
1199						
1200						
1201						
1202						
1203						
1204						
1205						

;PROGRAM INITIALIZATION  
 ;LOCK OUT INTERRUPTS  
 ;SET UP PROCESSOR STACK  
 ;SET UP POWER FAIL VECTOR  
 ;CLEAR PROGRAM CONTROL FLAGS AND COUNTS  
 ;TYPE TITLE MESSAGE



1206	001512	012737	000340	177776	.START:	MOV	#340, PS	; LOCK OUT INTERRUPTS
1207	001520	012706	001200			MOV	#STACK, SP	; SET UP STACK
1208	001524	012737	014564	000024		MOV	#.PFAIL, @#24	; SET UP POWER FAIL VECTOR
1209	001532	013737	001504	001276		MOV	DQNUM, SAVNUM	
1210	001540	105037	001311			CLRB	STFLG	; CLEAR START FLAG
1211	001544	005037	001230			CLR	PASCNT	; CLEAR PASS COUNT
1212	001550	105037	001312			CLRB	ERRFLG	; CLEAR ERROR FLAG
1213	001554	005037	001302			CLR	RUNFLG	
1214	001560	012737	001400	001300		MOV	#1400, CREAM	
1215	001566	005037	001232			CLR	ERRCNT	; CLEAR ERROR COUNT
1216	001572	005037	001234			CLR	LSTERR	; CLEAR LAST ERROR POINTER
1217	001576	012737	000001	001226		MOV	#1, TSTNO	; SET UP FOR TEST 1
1218	001604	012737	001512	001214		MOV	#.START, RETURN	; SET UP FOR POWER FAIL BEFORE TESTING STARTS
1219								; HAS INITIALIZATION BEEN PERFORMED
1220	001612	105737	001310			TSTB	INIFLG	
1221	001616	001075				BNE	12\$	
1222	001620	104402	001000			TYPE	MTITLE	; TYPE TITLE MESSAGE
1223	001624	105137	001310			COMB	INIFLG	; IF NOT SET FLAG AND DO
1224								
1225	001630	012737	177570	001200		MOV	#DSWR, SWR	; MOV HARDWARE SWR TO SWR
1226	001636	012737	177570	001202		MOV	#DLIGHTS, LIGHTS	; MOV DISPLAY LIGHTS TO LIGHTS
1227	001644	013746	000006			MOV	@#6, -(SP)	; SAVE VECTORS
1228	001650	013746	000004			MOV	@#4, -(SP)	
1229	001654	012737	001674	000004		MOV	@#4\$, @#4	
1230	001662	022777	177777	177310		CMP	#-1, @SWR	; SET UP FOR TIMEOUT
1231	001670	001402				BEQ	65\$	; REFERENCE HARDWARE SWITCH REGISTER
1232	001672	000407				BR	66\$	
1233	001674	022626			64\$:	CMP	(SP)+, (SP)+	; ADJUST STACK
1234	001676	012737	000176	001200	65\$:	MOV	#SWREG, SWR	; POINT TO SOFTWARE SWITCH REG
1235	001704	012737	000174	001202		MOV	#DISPREG, LIGHTS	; POINT TO SOFT DISPLAY REG
1236	001712	012637	000004		66\$:	MOV	(SP)+, @#4	; RESTORE VECTORS
1237	001716	012637	000006			MOV	(SP)+, @#6	
1238	001722	005737	000042			TST	@#42	; UNDER MONITOR
1239	001726	001005				BNE	67\$	
1240	001730	022737	000176	001200		CMP	#SWREG, SWR	; IS SWREG USED
1241	001736	001001				BNE	67\$	
1242	001740	104415				CNTLU		
1243	001742	105777	177232		67\$:	TSTB	@SWR	
1244	001746	100402				BMI	+6	
1245	001750	004737	000220			JSR	PC, CSRMAP	
1246	001754	104402	015412			TYPE	XHEAD	
1247	001760	012737	001400	001244		MOV	#1400, TEMP1	
1248	001766	017737	177252	001246		MOV	@TEMP1, TEMP2	
1249	001774	001406				BEQ	+.16	
1250	001776	104410				CONVRT		
1251	002000	015440				XSTATQ		
1252	002002	062737	000002	001244		ADD	#2, TEMP1	
1253	002010	000766				BR	.-22	
1254	002012	032777	000001	177160	12\$:	BIT	#SW00, @SWR	
1255	002020	001424				BEQ	1\$	
1256	002022	104402				TYPE		
1257	002024	015333				MNEW		
1258	002026	005000				CLR	RO	
1259	002030	000000				HALT		
1260	002032	104414				CKSWR		
1261	002034	027737	177140	001502		CMP	@SWR, SAVACT	

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1262 002042 101404 BLOS 11S
1263 002044 104402 TYPE
1264 002046 015174 MERR3
1265 002050 000000 HALT
1266 002052 000776 BR -2
1267 002054 017737 177120 C01500 11S: MOV @SWR,DQACTV
1268 002062 013700 001500 MOV DQACTV,RO
1269 002066 000000 HALT
1270 002070 104414 CKSWR
1271 002072 012700 000300 1S: MOV #300,RO
1272 002076 012701 000302 MOV #302,R1
1273 002102 010120 2S: MOV R1,(R0)+
1274 002104 005021 CLR (R1)+
1275 002106 022021 CMP (R0)+,(R1)+
1276 002110 022700 001000 CMP #1000,RO
1277 002114 001372 BNE 2S
1278
1279 ;TEST START AND RESTART
1280
1281 002116 012737 000340 177776 .BEGIN: MOV #340,PS ;LOCK OUT INTERRUPTS
1282 002124 012706 001200 MOV #STACK,SP ;SET UP STACK
1283 002130 005737 000042 TST @#42 ;IS PROGRAM UNDER MONITOR CONTROL
1284 002134 001040 BNE 3S
1285 002136 104414 CKSWR ;CHECK FOR <↑G>
1286 002140 032777 000004 177032 BIT #BIT2,@SWR ;CHECK FOR LOCK ON TEST
1287 002146 001411 BEQ 1S
1288 002150 104402 015232 TYPE MLOCK
1289 002154 012737 000240 013046 MOV #NOP,TTST
1290 002162 012737 000240 013050 MOV #NOP,TTST+2 ;SET UP TO LOCK
1291 002170 000406 BR 2S
1292 002172 013737 013144 013046 1S: MOV BRW,TTST
1293 002200 013737 013146 013050 MOV BRX,TTST+2 ;LOCK NOT SELECTED, SET UP FOR NORMAL SCOPE LOOP
1294 002206 032777 000002 176764 2S: BIT #SW01,@SWR ;IF SW01=1, GET STARTING PC
1295 002214 001410 BEQ 3S
1296 002216 104403 INSTR
1297 002220 015220 MTSTPC
1298 002222 104405 PARAM
1299 002224 002254 TST1
1300 002226 012442 TLAST
1301 002230 001214 #RETURN
1302 002232 001 .BYTE 1
1303 002233 001 .BYTE 1
1304 002234 000403 BR 4S
1305 002236 012737 002254 001214 3S: MOV #TST1,RETURN ;START AT TEST 1
1306 002244 104402 015122 4S: TYPE MR ;TYPE R
1307 002250 000177 176740 JMP @RETURN ;START TESTING
1308 ; TEST 1
1309 ;*****
1310 002254 012737 000001 001226 TST1: MOV #1,TSTNO
1311 002262 012737 002644 001214 MOV #TST2,RETURN
1312 002270 012737 002644 001216 MOV #TST2,NEXT
1313 002276 105737 001302 TSTB RUNFLG ;IS THIS MY FIRST TIME HERE?
1314 002302 001010 BNE 1S ;BR IF FLAG IS SET
1315 002304 012737 000001 001304 MOV #BIT0,RUN ;SET RUN POINTER.
1316 002312 012737 000020 001306 MOV #16,RUNCNT ;SET FOR MAX OF 16 DQ11'S PER SYSTEM
1317 002320 105137 001302 COMB RUNFLG ;SET RUN FLAG

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 DZDQCD.P11 16-DEC-76 13:26 PROGRAM INITIALIZATION AND START UP.

1318	002324	033737	001304	001500	1S:	BIT	RUN,DQACTV	;FIND AN ACTIVE DQ11 TO TEST.
1319	002332	001032				BNE	3S	;BR IF I FOUND ONE TO TEST.
1320	002334	005737	001500			TST	DQACTV	;FIND OUT IF THERE ARE NO DQ11 ACTIVE.
1321	002340	001423				BEG	2S	;BR TO FATAL ERROR. WHY AM I HERE IF NO ACTIVE DQ11'S???
1322	002342	000257				CCC		;CLEAR ALL THE CONDITION CODES OF CPU
1323	002344	006137	001304			ROL	RUN	;UPDATE RUN POINTER
1324	002350	062737	000004	001300		ADD	#4,CREAM	;UPDATE ADDRESS POINTER.
1325	002356	005337	001306			DEC	RUNCNT	;DEC NUMBER OF TIMES I LOOKED AT ACTIVE.
1326	002362	001360				BNE	1S	;BR AND KEEP LOOKING.
1327	002364	012737	000020	001306		MOV	#16, RUNCNT	;START RESTORING MY POINTERS.
1328	002372	012737	001400	001300		MOV	#1400,CREAM	;RESTORE ADDRESS POINTER
1329	002400	012737	000001	001304		MOV	#1,RUN	;RESTORE RUN POINTER.
1330	002406	000746				BR	1S	;KEEP ON TESTING.
1331	002410	104402			2S:	TYPE		;ALLERT OPERATOR OF FATAL ERROR
1332	002412	015125				MERR2		;NO DQ11 ACTIVE. WHY AM I HERE???
1333	002414	000000				HALT		;YOU MUST RELOAD DQ11 DIAGNOSTIC!!
1334	002416	000776				BR	.-2	;STICK HERE ON CONT.
1335	002420	000257			3S:	CCC		;CLEAR CPU COND. CODES
1336	002422	006137	001304			ROL	RUN	;UPDATE RUN. ACTIVE DQ11 FOUND.
1337	002426	017737	176646	001506		MOV	@CREAM,DQCSR	;PLACE ADDRESS OF DQ11 AT DQCSR
1338	002434	062737	000002	001300		ADD	#2,CREAM	;UPDATE ADDRESS POINTER
1339	002442	017737	176632	001510		MOV	@CREAM,DQSTAT	;PLACE STATUS OF DQ11 AT DQSTAT
1340	002450	062737	000002	001300		ADD	#2,CREAM	;UPDATE ADDRESS POINTER
1341	002456	013737	001506	001360		MOV	DQCSR,DQCSR	
1342	002464	013737	001510	001350		MOV	DQSTAT,DQVEC	
1343	002472	042737	177007	001350		BIC	#177007,DQVEC	
1344	002500	013737	001350	001352		MOV	DQVEC,DQRLVL	;GENERATE ADDRESS OF RECEIVER INTERRUPT SERVICE PS
1345	002506	062737	000002	001352		ADD	#2,DQRLVL	
1346	002514	013737	001352	001354		MOV	DQRLVL,DQTEC	;GENERATE ADDRESS OF TRANSMITTER INTERRUPT VECTOR
1347	002522	062737	000002	001354		ADD	#2,DQTEC	
1348	002530	013737	001354	001356		MOV	DQTEC,DQTLVL	;GENERATE ADDRESS OF TRANSMITTER INTERRUPT SERVICE PS
1349	002536	062737	000002	001356		ADD	#2,DQTLVL	
1350	002544	013737	001360	001362		MOV	DQCSR,DQCSH	
1351	002552	005237	001362			INC	DQCSH	;GENERATE ADDRESS OF HIGH BYTE
1352	002556	013737	001360	001364		MOV	DQCSR,DQTCR	;GENERATE ADDRESS OF TRANSMITTER CONTROL REGISTER
1353	002564	062737	000002	001364		ADD	#2,DQTCR	
1354	002572	013737	001364	001366		MOV	DQTCR,DQERR	;GENERATE ADDRESS OF ERROR REGISTER
1355	002600	062737	000002	001366		ADD	#2,DQERR	
1356	002606	013737	001366	001370		MOV	DQERR,DQREG	;GENERATE ADDRESS OF HIGH BYTE OF ERROR REGISTER
1357	002614	005237	001370			INC	DQREG	
1358	002620	013737	001370	001372		MOV	DQREG,DQSEC	;GENERATE ADDRESS OF SECONDARY REGISTER
1359	002626	005237	001372			INC	DQSEC	
1360	002632	013737	001372	001374		MOV	DQSEC,DQSECH	;GENERATE ADDRESS OF HIGH BYTE
1361	002640	005237	001374			INC	DQSECH	

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1371
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1378 002644 012737 000002 001226
1379 002652 012737 000010 001222
1380 002660 012737 003014 001216
1381 002666 012737 000340 177776
1382 002674 104413
1383 002676 104412
1384 002700 005037 001244
1385 002704 012737 000010 001246
1386 002712 112777 000012 176450
1387 002720 012777 000002 176444
1388 002726 012777 010001 176424
1389 002734 012777 000001 176422
1390 002742 005277 176424
1391 002746 005377 176420
1392 002752 005237 001244
1393 002756 001375
1394 002760 042777 010000 176372
1395 002766 005337 001246
1396 002772 001367
1397 002774 012705 000003
1398 003000 117704 176362
1399 003004 020504
1400 003006 001401
1401 003010 104013
1402 003012 104400
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1404
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1413 003014 012737 000003 001226
1414 003022 012737 000010 001222
1415 003030 012737 003142 001216
1416 003036 104413
1417 003040 012737 000340 177776

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;STEP MODE VERIFICATION AND CLOCK LOSS TEST
;SET STEP MODE
;SET RECEIVER GO
;SET TRANSMITTER GO
;EXPECTED RESULTS (AFTER DELAY)
;TRANSMITTER CLOCK LOSS = 1
;RECEIVER CLOCK LOSS = 1
;****NOTE: AS THE "CLOCK UP" OCCURS
;AN "NPR" SHOULD BE EXECUTED.
;THEREFORE IF THE DQ11 IS GOING TO "HANG"
;THE BUS DUE TO NPR'S THIS IS THE
;FIRST TEST IT WILL HAPPEN IN!!****

```

```

; TEST 2
;*****
TST2: MOV #2,TSTNO
      MOV #10,ICOUNT
      MOV #TST3,NEXT
      MOV #340,PS
      MEMCLR
      MSTCLR
      CLR TEMP1
      MOV #10,TEMP2
      MOVB #12,DQREG
      MOV #BIT1,DQSEC
      MOV #BIT12+BIT0,DQRCR
      MOV #BIT0,DQTCR
      INC DQSEC
      DEC DQSEC
15:   INC TEMP1
      BNE 15
      BIC #BIT12,DQRCR
      DEC TEMP2
      BNE 15
      MOV #3,R5
      MOVB DQERR,R4
      CMP R5,R4
      BEQ 25
      HLT 13
25:   SCOPE
      ;TEST LOOP VERIFICATION
      ;SET STEP MODE AND TEST LOOP
      ;SET RECEIVER GO
      ;SET TRANSMITTER GO
      ;EXPECTED RESULTS (AFTER DELAY)
      ;TRANSMITTER CLOCK LOSS=0
      ;RECEIVER CLOCK LOSS=0
      ;LOCK OUT INTERRUPTS
      ;CLEAR MEMORY
      ;INIT DQ11
      ;ZERO DELAY COUNTER
      ;DELAY 8 X 65535 TIMES
      ;SELECT MISC REG
      ;SET AUTO STEP
      ;SET RX GO!!
      ;SET TX GO!!
      ;CLOCK UP!!
      ;CLOCK DN!!
      ;DO THE DELAY....
      ;DELAY.....
      ;CLEAR RX ACTIVE
      ;DELAY.....
      ;DELAY.....
      ;SET FOR EXPECTED
      ;READ THE DQERR REGISTER (SEL4)
      ;CLOCK LOSS WORKING??
      ;BR IF YES.
      ;TX AND RX CLOCK LOSS ERROR
      ;SCOPE THIS TEST.
; TEST 3
;*****
TST3: MOV #3,TSTNO
      MOV #10,ICOUNT
      MOV #TST4,NEXT
      MEMCLR
      MOV #340,PS
      ;SET PS =7 LOCK OUT INTERRUPTS

```





# F03

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```

1435
1436           ; INDIVIDUAL INTERRUPT ENABLE TESTS
1437           ; SET SELECTED INTERRUPT ENABLE
1438           ; VERIFY THAT NO INTERRUPT OCCURS
1439
1440           ; INTERRUPT LOGIC TEST
1441           ; SET CHARACTER DETECT INTERRUPT ENABLE
1442           ; VERIFY THAT NO INTERRUPT OCCURS
1443
1444           ; TEST 4
1445           ; *****
1446 003142 012737 000004 001226 TST4: MOV #4,TSTNO
1447 003150 012737 003226 001216      MOV #TST5,NEXT
1448 003156 104412      MSTCLR           ; CLEAR INTERFACE
1449 003160 004737 016042      JSR PC,SETV      ; SET UP INTERRUPT VECTORS
1450 003164 003206      1$           ; RECEIVER WILL INTERRUPT TO 1$
1451 003166 003212      2$           ; TRANSMITTER WILL INTERRUPT TO 2$
1452 003170 052777 000020 176162  BIS #BIT4,DQRCR  ; SET CHARACTER DETECT INTERRUPT ENABL
1453 003176 005037 177776      CLR PS           ; SET PROCESSOR PRIORITY TO 0
1454 003202 000240      NOP           ; WINDOW FOR INTERRUPTS
1455 003204 000403      BR 3$
1456 003206 104003 15: HLT 3           ; UNEXPECTED RECEIVER INTERRUPT
1457 003210 000401      BR 3$
1458 003212 104002 2$: HLT 2           ; UNEXPECTED TRANSMITTER INTERRUPT
1459 003214 012706 001200 3$: MOV #STACK,SP      ; RESTORE STACK
1460 003220 004737 016074      JSR PC,RECAT     ; RESTORE TRAPCATCHER
1461 003224 104400 4$: SCOPE           ; CHECK FOR ITERATIONS, LOOP
1462
1463           ; INTERRUPT LOGIC TEST
1464           ; SET RECEIVE DONE INTERRUPT ENABLE
1465           ; VERIFY THAT NO INTERRUPT OCCURS
1466
1467           ; TEST 5
1468           ; *****
1469 003226 012737 000005 001226 TST5: MOV #5,TSTNO
1470 003234 012737 003312 001216      MOV #TST6,NEXT
1471 003242 104412      MSTCLR           ; CLEAR INTERFACE
1472 003244 004737 016042      JSR PC,SETV      ; SET UP INTERRUPT VECTORS
1473 003250 003272      1$           ; RECEIVER WILL INTERRUPT TO 1$
1474 003252 003276      2$           ; TRANSMITTER WILL INTERRUPT TO 2$
1475 003254 052777 000040 176076  BIS #BIT5,DQRCR  ; SET RECEIVE DONE INTERRUPT ENABL
1476 003262 005037 177776      CLR PS           ; SET PROCESSOR PRIORITY TO 0
1477 003266 000240      NOP           ; WINDOW FOR INTERRUPTS
1478 003270 000403      BR 3$
1479 003272 104003 15: HLT 3           ; UNEXPECTED RECEIVER INTERRUPT
1480 003274 000401      BR 3$
1481 003276 104002 2$: HLT 2           ; UNEXPECTED TRANSMITTER INTERRUPT
1482 003300 012706 001200 3$: MOV #STACK,SP      ; RESTORE STACK
1483 003304 004737 016074      JSR PC,RECAT     ; RESTORE TRAPCATCHER
1484 003310 104400 4$: SCOPE           ; CHECK FOR ITERATIONS, LOOP
1485
1486           ; INTERRUPT LOGIC TEST
1487           ; SET ERROR INTERRUPT ENABLE
1488           ; VERIFY THAT NO INTERRUPT OCCURS
1489
1490           ; TEST 6

```



# G03

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```

1491
1492 003312 012737 000006 001226
1493 003320 012737 003376 001216
1494 003326 104412
1495 003330 004737 016042
1496 003334 003356
1497 003336 003362
1498 003340 052777 000010 176016
1499 003346 005037 177776
1500 003352 000240
1501 003354 000403
1502 003356 104003
1503 003360 000401
1504 003362 104002
1505 003364 012706 001200
1506 003370 004737 016074
1507 003374 104400
1508
1509
1510
1511
1512
1513
1514
1515 003376 012737 000007 001226
1516 003404 012737 003462 001216
1517 003412 104412
1518 003414 004737 016042
1519 003420 003442
1520 003422 003446
1521 003424 052777 000020 175732
1522 003432 005037 177776
1523 003436 000240
1524 003440 000403
1525 003442 104003
1526 003444 000401
1527 003446 104002
1528 003450 012706 001200
1529 003454 004737 016074
1530 003460 104400
1531
1532
1533
1534
1535
1536
1537
1538 003462 012737 000010 001226
1539 003470 012737 003546 001216
1540 003476 104412
1541 003500 004737 016042
1542 003504 003526
1543 003506 003532
1544 003510 052777 000040 175646
1545 003516 005037 177776
1546 003522 000240

; *****
TST6:  MOV    #6,TSTNO
      MOV    #TST7,NEXT
      MSTCLR
      JSR    PC,SETV
      1$
      2$
      BIS    #BIT3,DDQTCR
      CLR    PS
      NOP
      BR     3$
1$:   HLT    3
      BR     3$
2$:   HLT    2
3$:   MOV    #STACK,SP
      JSR    PC,RECAT
4$:   SCOPE

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET ERROR INTERRUPT ENABL
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS

; UNEXPECTED RECEIVER INTERRUPT

; UNEXPECTED TRANSMITTER INTERRUPT
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

; INTERRUPT LOGIC TEST
; SET DATASET INTERRUPT ENABLE
; VERIFY THAT NO INTERRUPT OCCURS

; TEST 7
; *****
TST7:  MOV    #7,TSTNO
      MOV    #TST10,NEXT
      MSTCLR
      JSR    PC,SETV
      1$
      2$
      BIS    #BIT4,DDQTCR
      CLR    PS
      NOP
      BR     3$
1$:   HLT    3
      BR     3$
2$:   HLT    2
3$:   MOV    #STACK,SP
      JSR    PC,RECAT
4$:   SCOPE

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET DATASET INTERRUPT ENABL
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS

; UNEXPECTED RECEIVER INTERRUPT

; UNEXPECTED TRANSMITTER INTERRUPT
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

; INTERRUPT LOGIC TEST
; SET TRANSMIT DONE INTERRUPT ENABLE
; VERIFY THAT NO INTERRUPT OCCURS

; TEST 10
; *****
TST10: MOV    #10,TSTNO
      MOV    #TST11,NEXT
      MSTCLR
      JSR    PC,SETV
      1$
      2$
      BIS    #BIT5,DDQTCR
      CLR    PS
      NOP

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET TRANSMIT DONE INTERRUPT ENABL
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
  
```

# H03

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```

1547 003524 000403          BR      3$
1548 003526 104003          1$:   HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1549 003530 000401          BR      3$
1550 003532 104002          2$:   HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1551 003534 012706 001200      3$:   MOV      #STACK, SP    ;RESTORE STACK
1552 003540 004737 016074      JSR     PC,REC@T         ;RESTORE TRAPCATCHER
1553 003544 104400          4$:   SCOPE          ;CHECK FOR ITERATIONS, LOOP
1554
1555          ;INDIVIDUAL INTERRUPT FLAG TESTS
1556          ;SET SELECTED INTERRUPT FLAG
1557          ;VERIFY THAT NO INTERRUPT OCCURS
1558
1559
1560          ;INTERRUPT LOGIC TEST
1561          ;SET RECEIVE DONE S INTERRUPT FLAG
1562          ;VERIFY THAT NO INTERRUPT OCCURS
1563
1564          ; TEST 11
1565          ;*****
1566 003546 012737 000011 001226 1$T11:  MOV      #11,TSTNO
1567 003554 012737 003632 001216      MOV      #T$T12,NEXT
1568 003562 104412          MSTCLR          ;CLEAR INTERFACE
1569 003564 004737 016042      JSR     PC,SETV        ;SET UP INTERRUPT VECTORS
1570 003570 003612          1$:   HLT      3          ;RECEIVER WILL INTERRUPT TO 1$
1571 003572 003616          2$:   HLT      2          ;TRANSMITTER WILL INTERRUPT TO 2$
1572 003574 052777 000100 175556      BIS     #BIT6,@DQRCSR  ;SET RECEIVE DONE S INTERRUPT FLAG
1573 003602 005037 177776      CLR     PS            ;SET PROCESSOR PRIORITY TO 0
1574 003606 000240          NOP            ;WINDOW FOR INTERRUPTS
1575 003610 000403          BR      3$
1576 003612 104003          1$:   HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1577 003614 000401          BR      3$
1578 003616 104002          2$:   HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1579 003620 012706 001200      3$:   MOV      #STACK, SP    ;RESTORE STACK
1580 003624 004737 016074      JSR     PC,REC@T         ;RESTORE TRAPCATCHER
1581 003630 104400          4$:   SCOPE          ;CHECK FOR ITERATIONS, LOOP
1582
1583          ;INTERRUPT LOGIC TEST
1584          ;SET RECEIVE DONE P INTERRUPT FLAG
1585          ;VERIFY THAT NO INTERRUPT OCCURS
1586
1587          ; TEST 12
1588          ;*****
1589 003632 012737 000012 001226 1$T12:  MOV      #12,TSTNO
1590 003640 012737 003716 001216      MOV      #T$T13,NEXT
1591 003646 104412          MSTCLR          ;CLEAR INTERFACE
1592 003650 004737 016042      JSR     PC,SETV        ;SET UP INTERRUPT VECTORS
1593 003654 003676          1$:   HLT      3          ;RECEIVER WILL INTERRUPT TO 1$
1594 003656 003702          2$:   HLT      2          ;TRANSMITTER WILL INTERRUPT TO 2$
1595 003660 052777 000200 175472      BIS     #BIT7,@DQRCSR  ;SET RECEIVE DONE P INTERRUPT FLAG
1596 003666 005037 177776      CLR     PS            ;SET PROCESSOR PRIORITY TO 0
1597 003672 000240          NOP            ;WINDOW FOR INTERRUPTS
1598 003674 000403          BR      3$
1599 003676 104003          1$:   HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1600 003700 000401          BR      3$
1601 003702 104002          2$:   HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1602 003704 012706 001200      3$:   MOV      #STACK, SP    ;RESTORE STACK

```



```

1603 003710 004737 016074      JSR    PC,RECAT      ;RESTORE TRAPCATCHER
1604 003714 104400      4$:    SCOPE        ;CHECK FOR ITERATIONS, LOOP
1605
1606      ; INTERRUPT LOGIC TEST
1607      ; SET TRANSMIT DONE S INTERRUPT FLAG
1608      ; VERIFY THAT NO INTERRUPT OCCURS
1609
1610      ; TEST 13
1611      ; *****
1612 003716 012737 000013 001226  TST13: MOV    #13,TSTNO
1613 003724 012737 004002 001216      MOV    #TST14,NEXT
1614 003732 104412      MSTCLR
1615 003734 004737 016042      JSR    PC,SETV      ;CLEAR INTERFACE
1616 003740 003762      1$      ;SET UP INTERRUPT VECTORS
1617 003742 003766      2$      ;RECEIVER WILL INTERRUPT TO 1$
1618 003744 052777 000100 175412  BIS    #BIT6,JDQTCR ;TRANSMITTER WILL INTERRUPT TO 2$
1619 003752 005037 177776      CLR    PS          ;SET TRANSMIT DONE S INTERRUPT FLAG
1620 003756 000240      NOP              ;SET PROCESSOR PRIORITY TO C
1621 003760 000403      BR     3$        ;WINDOW FOR INTERRUPTS
1622 003762 104003      1$:    HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1623 003764 000401      BR     3$
1624 003766 104002      2$:    HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1625 003770 012706 001200      3$:    MOV    #STACK,SP ;RESTORE STACK
1626 003774 004737 016074      JSR    PC,RECAT    ;RESTORE TRAPCATCHER
1627 004000 104400      4$:    SCOPE        ;CHECK FOR ITERATIONS, LOOP
1628
1629      ; INTERRUPT LOGIC TEST
1630      ; SET RECEIVE DONE S INTERRUPT FLAG
1631      ; VERIFY THAT NO INTERRUPT OCCURS
1632
1633      ; TEST 14
1634      ; *****
1635 004002 012737 000014 001226  TST14: MOV    #14,TSTNO
1636 004010 012737 004066 001216      MOV    #TST15,NEXT
1637 004016 104412      MSTCLR
1638 004020 004737 016042      JSR    PC,SETV      ;CLEAR INTERFACE
1639 004024 004046      1$      ;SET UP INTERRUPT VECTORS
1640 004026 004052      2$      ;RECEIVER WILL INTERRUPT TO 1$
1641 004030 052777 000200 175326  BIS    #BIT7,JDQTCR ;TRANSMITTER WILL INTERRUPT TO 2$
1642 004036 005037 177776      CLR    PS          ;SET RECEIVE DONE S INTERRUPT FLAG
1643 004042 000240      NOP              ;SET PROCESSOR PRIORITY TO 0
1644 004044 000403      BR     3$        ;WINDOW FOR INTERRUPTS
1645 004046 104003      1$:    HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1646 004050 000401      BR     3$
1647 004052 104002      2$:    HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1648 004054 012706 001200      3$:    MOV    #STACK,SP ;RESTORE STACK
1649 004060 004737 016074      JSR    PC,RECAT    ;RESTORE TRAPCATCHER
1650 004064 104400      4$:    SCOPE        ;CHECK FOR ITERATIONS, LOOP
1651
1652      ; INTERRUPT LOGIC TEST
1653      ; SET DATA SET INTERRUPT FLAG
1654      ; VERIFY THAT NO INTERRUPT OCCURS
1655
1656      ; TEST 15
1657      ; *****
1658 004066 012737 000015 001226  TST15: MOV    #15,TSTNO
    
```

```

1659 004074 012737 004152 001216      MOV      #TST16,NEXT
1660 004102 104412      MSTCLR
1661 004104 004737 016042      JSR      PC,SETV
1662 004110 004132      1$
1663 004112 004136      2$
1664 004114 052777 100000 175242  BIS      #BIT15,ADQTCR
1665 004122 005037 177776      CLR      PS
1666 004126 000240      NOP
1667 004130 000403      BR      3$
1668 004132 104003      1$: HLT      3
1669 004134 000401      BR      3$
1670 004136 104002      2$: HLT      2
1671 004140 012706 001200 3$: MOV      #STACK,SP
1672 004144 004737 016074      JSR      PC,RECAT
1673 004150 104400      4$: SCOPE

```

```

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET DATA SET INTERRUPT FLAG
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
; UNEXPECTED RECEIVER INTERRUPT
; UNEXPECTED TRANSMITTER INTERRUPT
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET T CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT NO INTERRUPT OCCURS

```

; TEST 16

\*\*\*\*\*

```

1681 004152 012737 000016 001226 1681: MOV      #16,TSTNO
1682 004160 012737 004236 001216 1682: MOV      #TST17,NEXT
1683 004166 104412      MSTCLR
1684 004170 004737 016042      JSR      PC,SETV
1685 004174 004216      1$
1686 004176 004222      2$
1687 004200 052777 000001 175160  BIS      #BIT0,ADQERR
1688 004206 005037 177776      CLR      PS
1689 004212 000240      NOP
1690 004214 000403      BR      3$
1691 004216 104003      1$: HLT      3
1692 004220 000401      BR      3$
1693 004222 104002      2$: HLT      2
1694 004224 012706 001200 3$: MOV      #STACK,SP
1695 004230 004737 016074      JSR      PC,RECAT
1696 004234 104400      4$: SCOPE

```

```

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET T CLOCK LOSS INTERRUPT FLAG
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
; UNEXPECTED RECEIVER INTERRUPT
; UNEXPECTED TRANSMITTER INTERRUPT
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET R CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT NO INTERRUPT OCCURS

```

; TEST 17

\*\*\*\*\*

```

1704 004236 012737 000017 001226 1704: MOV      #17,TSTNO
1705 004244 012737 004322 001216 1705: MOV      #TST20,NEXT
1706 004252 104412      MSTCLR
1707 004254 004737 016042      JSR      PC,SETV
1708 004260 004302      1$
1709 004262 004306      2$
1710 004264 052777 000002 175074  BIS      #BIT1,ADQERR
1711 004272 005037 177776      CLR      PS
1712 004276 000240      NOP
1713 004300 000403      BR      3$
1714 004302 104003      1$: HLT      3

```

```

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1$
; TRANSMITTER WILL INTERRUPT TO 2$
; SET R CLOCK LOSS INTERRUPT FLAG
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
; UNEXPECTED RECEIVER INTERRUPT

```



# K03

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```

1715 004304 000401          BR      3$
1716 004306 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1717 004310 012706 001200          3$:    MOV      #STACK,SP      ;RESTORE STACK
1718 004314 004737 016074          JSR      PC,RECAT          ;RESTORE TRAPCATCHER
1719 004320 104400          4$:    SCOPE          ;CHECK FOR ITERATIONS, LOOP
1720
1721          ; INTERRUPT LOGIC TEST
1722          ; SET T LATENCY INTERRUPT FLAG
1723          ; VERIFY THAT NO INTERRUPT OCCURS
1724
1725          ; TEST 20
1726          ; *****
1727 004322 012737 000020 001226 1$TST20: MOV      #20,TSTNO
1728 004330 012737 004406 001216          MOV      #TST21,NEXT
1729 004336 104412          MSTCLR          ; CLEAR INTERFACE
1730 004340 004737 016042          JSR      PC,SETV          ; SET UP INTERRUPT VECTORS
1731 004344 004366          1$          ; RECEIVER WILL INTERRUPT TO 1$
1732 004346 004372          2$          ; TRANSMITTER WILL INTERRUPT TO 2$
1733 004350 052777 000004 175010          BIS      #BIT2,JDGERR      ; SET T LATENCY INTERRUPT FLAG
1734 004356 005037 177776          CLR      PS          ; SET PROCESSOR PRIORITY TO 0
1735 004362 000240          NOP          ; WINDOW FOR INTERRUPTS
1736 004364 000403          BR      3$
1737 004366 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1738 004370 000401          BR      3$
1739 004372 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1740 004374 012706 001200          3$:    MOV      #STACK,SP      ;RESTORE STACK
1741 004400 004737 016074          JSR      PC,RECAT          ;RESTORE TRAPCATCHER
1742 004404 104400          4$:    SCOPE          ;CHECK FOR ITERATIONS, LOOP
1743
1744          ; INTERRUPT LOGIC TEST
1745          ; SET R LATENCY INTERRUPT FLAG
1746          ; VERIFY THAT NO INTERRUPT OCCURS
1747
1748          ; TEST 21
1749          ; *****
1750 004406 012737 000021 001226 1$TST21: MOV      #21,TSTNO
1751 004414 012737 004472 001216          MOV      #TST22,NEXT
1752 004422 104412          MSTCLR          ; CLEAR INTERFACE
1753 004424 004737 016042          JSR      PC,SETV          ; SET UP INTERRUPT VECTORS
1754 004430 004452          1$          ; RECEIVER WILL INTERRUPT TO 1$
1755 004432 004456          2$          ; TRANSMITTER WILL INTERRUPT TO 2$
1756 004434 052777 000010 174724          BIS      #BIT3,JDGERR      ; SET R LATENCY INTERRUPT FLAG
1757 004442 005037 177776          CLR      PS          ; SET PROCESSOR PRIORITY TO 0
1758 004446 000240          NOP          ; WINDOW FOR INTERRUPTS
1759 004450 000403          BR      3$
1760 004452 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1761 004454 000401          BR      3$
1762 004456 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1763 004460 012706 001200          3$:    MOV      #STACK,SP      ;RESTORE STACK
1764 004464 004737 016074          JSR      PC,RECAT          ;RESTORE TRAPCATCHER
1765 004470 104400          4$:    SCOPE          ;CHECK FOR ITERATIONS, LOOP
1766
1767          ; INTERRUPT LOGIC TEST
1768          ; SET T NON-EX MEM INTERRUPT FLAG
1769          ; VERIFY THAT NO INTERRUPT OCCURS
1770

```

```

1771 ; TEST 22
1772 ;*****
1773 004472 012737 000022 001226 TST22: MOV #22,TSTNO
1774 004500 012737 004556 001216 MOV #TST23,NEXT
1775 004506 104412 MSTCLR ;CLEAR INTERFACE
1776 004510 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1777 004514 004536 1S ;RECEIVER WILL INTERRUPT TO 1S
1778 004516 004542 2S ;TRANSMITTER WILL INTERRUPT TO 2S
1779 004520 052777 000020 174640 BIS #BIT4,JDQERR ;SET T NON-EX MEM INTERRUPT FLAG
1780 004526 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1781 004532 000240 NOP ;WINDOW FOR INTERRUPTS
1782 004534 000403 BR 3S
1783 004536 104003 1S: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1784 004540 000401 BR 3S
1785 004542 104002 2S: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1786 004544 012706 001200 3S: MOV #STACK,SP ;RESTORE STACK
1787 004550 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1788 004554 104400 4S: SCOPE ;CHECK FOR ITERATIONS, LOOP
1789
1790 ; INTERRUPT LOGIC TEST
1791 ; SET R NON-EX MEM INTERRUPT FLAG
1792 ; VERIFY THAT NO INTERRUPT OCCURS
1793
1794 ; TEST 23
1795 ;*****
1796 004556 012737 000023 001226 TST23: MOV #23,TSTNO
1797 004564 012737 004642 001216 MOV #TST24,NEXT
1798 004572 104412 MSTCLR ;CLEAR INTERFACE
1799 004574 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1800 004600 004622 1S ;RECEIVER WILL INTERRUPT TO 1S
1801 004602 004626 2S ;TRANSMITTER WILL INTERRUPT TO 2S
1802 004604 052777 000040 174554 BIS #BIT5,JDQERR ;SET R NON-EX MEM INTERRUPT FLAG
1803 004612 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1804 004616 000240 NOP ;WINDOW FOR INTERRUPTS
1805 004620 000403 BR 3S
1806 004622 104003 1S: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1807 004624 000401 BR 3S
1808 004626 104002 2S: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1809 004630 012706 001200 3S: MOV #STACK,SP ;RESTORE STACK
1810 004634 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1811 004640 104400 4S: SCOPE ;CHECK FOR ITERATIONS, LOOP
1812
1813 ; INTERRUPT LOGIC TEST
1814 ; SET R BCC ERROR INTERRUPT FLAG
1815 ; VERIFY THAT NO INTERRUPT OCCURS
1816
1817 ; TEST 24
1818 ;*****
1819 004642 012737 000024 001226 TST24: MOV #24,TSTNO
1820 004650 012737 004726 001216 MOV #TST25,NEXT
1821 004656 104412 MSTCLR ;CLEAR INTERFACE
1822 004660 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1823 004664 004706 1S ;RECEIVER WILL INTERRUPT TO 1S
1824 004666 004712 2S ;TRANSMITTER WILL INTERRUPT TO 2S
1825 004670 052777 000100 174470 BIS #BIT6,JDQERR ;SET R BCC ERROR INTERRUPT FLAG
1826 004676 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
    
```



# MO3

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```

1827 004702 000240          NOP          ;WINDOW FOR INTERRUPTS
1828 004704 000403          BR           3$
1829 004706 104003          1$: HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1830 004710 000401          BR           3$
1831 004712 104002          2$: HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1832 004714 012706 001200    3$: MOV      #STACK, SP ;RESTORE STACK
1833 004720 004737 016074    JSR      PC,RECAT    ;RESTORE TRAPCATCHER
1834 004724 104400          4$: SCOPE          ;CHECK FOR ITERATIONS, LOOP
1835
1836          ; INTERRUPT LOGIC TEST
1837          ; SET R VRC ERROR INTERRUPT FLAG
1838          ; VERIFY THAT NO INTERRUPT OCCURS
1839
1840          ; TEST 25
1841          ; *****
1842 004726 012737 000025 001226  TST25: MOV      #25, TSTNO
1843 004734 012737 005012 001216    MOV      #TST26, NEXT
1844 004742 104412          MSTCLR
1845 004744 004737 016042          JSR      PC, SETV    ; CLEAR INTERFACE
1846 004750 004772          1$          ; SET UP INTERRUPT VECTORS
1847 004752 004776          2$          ; RECEIVER WILL INTERRUPT TO 1$
1848 004754 052777 000200 174404    BIS      #BIT7, JDQERR ; TRANSMITTER WILL INTERRUPT TO 2$
1849 004762 005037 177776          CLR      PS          ; SET R VRC ERROR INTERRUPT FLAG
1850 004766 000240          NOP          ; SET PROCESSOR PRIORITY TO 0
1851 004770 000403          BR           3$      ; WINDOW FOR INTERRUPTS
1852 004772 104003          1$: HLT      3          ; UNEXPECTED RECEIVER INTERRUPT
1853 004774 000401          BR           3$
1854 004776 104002          2$: HLT      2          ; UNEXPECTED TRANSMITTER INTERRUPT
1855 005000 012706 001200    3$: MOV      #STACK, SP ; RESTORE STACK
1856 005004 004737 016074    JSR      PC, RECAT   ; RESTORE TRAPCATCHER
1857 005010 104400          4$: SCOPE          ; CHECK FOR ITERATIONS, LOOP
1858
1859          ; INDIVIDUAL INTERRUPT TESTS
1860          ; SET SELECTED INTERRUPT ENABLE AND FLAG
1861          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT ADDRESS
1862
1863          ; INTERRUPT LOGIC TEST
1864          ; SET CHARACTER DETECT INTERRUPT ENABLE
1865          ; SET CHARACTER DETECT INTERRUPT FLAG
1866          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1867
1868          ; TEST 26
1869          ; *****
1870          ; *****
1871 005012 012737 000026 001226  TST26: MOV      #26, TSTNO
1872 005020 012737 005102 001216    MOV      #TST27, NEXT
1873 005026 104412          MSTCLR
1874 005030 004737 016042          JSR      PC, SETV    ; CLEAR INTERFACE
1875 005034 005064          1$          ; SET UP INTERRUPT VECTORS
1876 005036 005066          2$          ; RECEIVER WILL INTERRUPT TO 1$
1877 005040 052777 000020 174312    BIS      #BIT4, JDQCSR ; TRANSMITTER WILL INTERRUPT TO 2$
1878 005046 052777 100000 174304    BIS      #BIT15, JDQCSR ; SET CHARACTER DETECT INTERRUPT ENABL
1879 005054 005037 177776          CLR      PS          ; SET CHARACTER DETECT INTERRUPT FLAG
1880 005060 000240          NOP          ; SET PROCESSOR PRIORITY TO 0
1881 005062 104000          HLT      0          ; WINDOW FOR INTERRUPTS
1882 005064 000401          1$: BR           3$      ; RECEIVER DID NOT INTERRUPT
                                ; RECEIVER SHOULD INTERRUPT TO THIS LOCATION

```

# N03

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```

1883 005066 104002          2S:   HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1884 005070 012706 001200  3S:   MOV     #STACK,SP ;RESTORE STACK
1885 005074 004737 016074          JSR     PC,RECAT   ;RESTORE TRAPCATCHER
1886 005100 104400          4S:   SCOPE                ;CHECK FOR ITERATIONS, LOOP
1887
1888          ; INTERRUPT LOGIC TEST
1889          ; SET RECEIVE DONE INTERRUPT ENABLE
1890          ; SET RECEIVE DONE S INTERRUPT FLAG
1891          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1892
1893          ; TEST 27
1894          ; *****
1895 005102 012737 000027 001226  TST27: MOV     #27,TSTNO
1896 005110 012737 005172 001216          MOV     #TST30,NEXT
1897 005116 104412          MSTCLR
1898 005120 004737 016042          JSR     PC,SETV    ; CLEAR INTERFACE
1899 005124 005154          IS          ; SET UP INTERRUPT VECTORS
1900 005126 005156          2S          ; RECEIVER WILL INTERRUPT TO IS
1901 005130 052777 000040 174222  BIS     #BITS,ADQRCSR ; TRANSMITTER WILL INTERRUPT TO 2S
1902 005136 052777 000100 174214  BIS     #BIT6,ADQRCSR ; SET RECEIVE DONE INTERRUPT ENABL
1903 005144 005037 177776          CLR     PS         ; SET RECEIVE DONE S INTERRUPT FLAG
1904 005150 000240          NOP
1905 005152 104000          HLT     0          ; SET PROCESSOR PRIORITY TO 0
1906 005154 000401          1S:   BR      3S      ; WINDOW FOR INTERRUPTS
1907 005156 104002          2S:   HLT     2          ; RECEIVER DID NOT INTERRUPT
1908 005160 012706 001200  3S:   MOV     #STACK,SP ; RECEIVER SHOULD INTERRUPT TO THIS LOCATION
1909 005164 004737 016074          JSR     PC,RECAT   ; UNEXPECTED TRANSMITTER INTERRUPT
1910 005170 104400          4S:   SCOPE                ; RESTORE STACK
1911          ; CHECK FOR ITERATIONS, LOOP
1912          ; INTERRUPT LOGIC TEST
1913          ; SET RECEIVE DONE INTERRUPT ENABLE
1914          ; SET RECEIVE DONE P INTERRUPT FLAG
1915          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1916
1917          ; TEST 30
1918          ; *****
1919 005172 012737 000030 001226  TST30: MOV     #30,TSTNO
1920 005200 012737 005262 001216          MOV     #TST31,NEXT
1921 005206 104412          MSTCLR
1922 005210 004737 016042          JSR     PC,SETV    ; CLEAR INTERFACE
1923 005214 005244          IS          ; SET UP INTERRUPT VECTORS
1924 005216 005246          2S          ; RECEIVER WILL INTERRUPT TO IS
1925 005220 052777 000040 174132  BIS     #BITS,ADQRCSR ; TRANSMITTER WILL INTERRUPT TO 2S
1926 005226 052777 000200 174124  BIS     #BIT7,ADQRCSR ; SET RECEIVE DONE INTERRUPT ENABL
1927 005234 005037 177776          CLR     PS         ; SET RECEIVE DONE P INTERRUPT FLAG
1928 005240 000240          NOP
1929 005242 104000          HLT     0          ; SET PROCESSOR PRIORITY TO 0
1930 005244 000401          1S:   BR      3S      ; WINDOW FOR INTERRUPTS
1931 005246 104002          2S:   HLT     2          ; RECEIVER DID NOT INTERRUPT
1932 005250 012706 001200  3S:   MOV     #STACK,SP ; RECEIVER SHOULD INTERRUPT TO THIS LOCATION
1933 005254 004737 016074          JSR     PC,RECAT   ; UNEXPECTED TRANSMITTER INTERRUPT
1934 005260 104400          4S:   SCOPE                ; RESTORE STACK
1935          ; CHECK FOR ITERATIONS, LOOP
1936          ; INTERRUPT LOGIC TEST
1937          ; SET TRANSMIT DONE INTERRUPT ENABLE
1938          ; SET TRANSMIT DONE S INTERRUPT FLAG

```



```

1939
1940
1941
1942
1943 005262 012737 000031 001226
1944 005270 012737 005354 001216
1945 005276 104412
1946 005300 004737 016042
1947 005304 005336
1948 005306 005340
1949 005310 052777 000040 174046
1950 005316 052777 000100 174040
1951 005324 005037 177776
1952 005330 000240
1953 005332 104001
1954 005334 000402
1955
1956 005336 104003
1957 005340 000240
1958 005342 012706 001200
1959 005346 004737 016074
1960 005352 104400
1961
1962
1963
1964
1965
1966
1967
1968
1969 005354 012737 000032 001226
1970 005362 012737 005446 001216
1971 005370 104412
1972 005372 004737 016042
1973 005376 005430
1974 005400 005432
1975 005402 052777 000040 173754
1976 005410 052777 000200 173746
1977 005416 005037 177776
1978 005422 000240
1979 005424 104001
1980 005426 000402
1981
1982 005430 104003
1983 005432 000240
1984 005434 012706 001200
1985 005440 004737 016074
1986 005444 104400
1987
1988
1989
1990
1991
1992
1993
1994

```

;VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

; TEST 31

\*\*\*\*\*

```

TST31: MOV #31,TSTNO
      MOV #TST32,NEXT
      MSTCLR
      JSR PC,SETV
      IS
      2S
      BIS #BITS,JDQTCR
      BIS #BIT6,JDQTCR
      CLR PS
      NOP
      HLT 1
      BR 3S
1S:   HLT 3
2S:   NOP
3S:   MOV #STACK,SP
      JSR PC,RECAT
4S:   SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1S
;TRANSMITTER WILL INTERRUPT TO 2S
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE S INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE S INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

;INTERRUPT LOGIC TEST
;SET TRANSMIT DONE INTERRUPT ENABLE
;SET TRANSMIT DONE P INTERRUPT FLAG
;VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

; TEST 32

\*\*\*\*\*

```

TST32: MOV #32,TSTNO
      MOV #TST33,NEXT
      MSTCLR
      JSR PC,SETV
      IS
      2S
      BIS #BITS,JDQTCR
      BIS #BIT7,JDQTCR
      CLR PS
      NOP
      HLT 1
      BR 3S
1S:   HLT 3
2S:   NOP
3S:   MOV #STACK,SP
      JSR PC,RECAT
4S:   SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1S
;TRANSMITTER WILL INTERRUPT TO 2S
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE P INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE P INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

;INTERRUPT LOGIC TEST
;SET ERROR INTERRUPT ENABLE
;SET T CLOCK LOSS INTERRUPT FLAG
;VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

; TEST 33

\*\*\*\*\*

```

1995 005446 012737 000033 001226 TST33: MOV #33,TSTNO
1996 005454 012737 005540 001216 MOV #TST34,NEXT
1997 005462 104412 MSTCLR ;CLEAR INTERFACE
1998 005464 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1999 005470 005522 1$ ;RECEIVER WILL INTERRUPT TO 1$
2000 005472 005524 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
2001 005474 052777 000010 173662 BIS #BIT3,JDQTCR ;SET ERROR INTERRUPT ENABL
2002 005502 052777 000001 173656 BIS #BIT0,JDQERR ;SET T CLOCK LOSS INTERRUPT FLAG
2003 005510 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2004 005514 000240 NOP ;WINDOW FOR INTERRUPTS
2005 005516 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2006 005520 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND
;T CLOCK LOSS INTERRUPT FLAG SET
2007 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2008 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2009 3$: MOV #STACK,SP ;RESTORE STACK
2010 005526 012706 001200 JSR PC,RECAT ;RESTORE TRAPCATCHER
2011 005532 004737 016074 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2012 005536 104400
2013
2014 ; INTERRUPT LOGIC TEST
2015 ; SET ERROR INTERRUPT ENABLE
2016 ; SET R CLOCK LOSS INTERRUPT FLAG
2017 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2018
2019 ; TEST 34
2020 ; *****
2021 005540 012737 000034 001226 TST34: MOV #34,TSTNO
2022 005546 012737 005632 001216 MOV #TST35,NEXT
2023 005554 104412 MSTCLR ;CLEAR INTERFACE
2024 005556 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2025 005562 005614 1$ ;RECEIVER WILL INTERRUPT TO 1$
2026 005564 005616 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
2027 005566 052777 000010 173570 BIS #BIT3,JDQTCR ;SET ERROR INTERRUPT ENABL
2028 005574 052777 000002 173564 BIS #BIT1,JDQERR ;SET R CLOCK LOSS INTERRUPT FLAG
2029 005602 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2030 005606 000240 NOP ;WINDOW FOR INTERRUPTS
2031 005610 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2032 005612 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND
;R CLOCK LOSS INTERRUPT FLAG SET
2033 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2034 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2035 3$: MOV #STACK,SP ;RESTORE STACK
2036 005620 012706 001200 JSR PC,RECAT ;RESTORE TRAPCATCHER
2037 005624 004737 016074 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2038 005630 104400
2039
2040 ; INTERRUPT LOGIC TEST
2041 ; SET ERROR INTERRUPT ENABLE
2042 ; SET T LATENCY INTERRUPT FLAG
2043 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2044
2045 ; TEST 35
2046 ; *****
2047 005632 012737 000035 001226 TST35: MOV #35,TSTNO
2048 005640 012737 005724 001216 MOV #TST36,NEXT
2049 005646 104412 MSTCLR ;CLEAR INTERFACE
2050 005650 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS

```



```

2051 005654 005706 1S
2052 005656 005710 2S
2053 005660 052777 000010 173476 BIS #BIT3, @DQTCR
2054 005666 052777 000004 173472 BIS #BIT2, @DQERR
2055 005674 005037 177776 CLR PS
2056 005700 000240 NOP
2057 005702 104001 HLT 1
2058 005704 000402 BR 3S
2059
2060 005706 104003 1S: HLT 3
2061 005710 000240 2S: NOP
2062 005712 012706 001200 3S: MOV #STACK, SP
2063 005716 004737 016074 JSR PC, RECAT
2064 005722 104400 4S: SCOPE
2065
2066 ; INTERRUPT LOGIC TEST
2067 ; SET ERROR INTERRUPT ENABLE
2068 ; SET R LATENCY INTERRUPT FLAG
2069 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2070
2071 ; TEST 36
2072 ; *****
2073 005724 012737 000036 001226 TST36: MOV #36, TSTNO
2074 005732 012737 006016 001216 MOV #TST37, NEXT
2075 005740 104412 MSTCLR
2076 005742 004737 016042 JSR PC, SETV
2077 005746 006000 1S
2078 005750 006002 2S
2079 005752 052777 000010 173404 BIS #BIT3, @DQTCR
2080 005760 052777 000010 173400 BIS #BIT3, @DQERR
2081 005766 005037 177776 CLR PS
2082 005772 000240 NOP
2083 005774 104001 HLT 1
2084 005776 000402 BR 3S
2085
2086 006000 104003 1S: HLT 3
2087 006002 000240 2S: NOP
2088 006004 012706 001200 3S: MOV #STACK, SP
2089 006010 004737 016074 JSR PC, RECAT
2090 006014 104400 4S: SCOPE
2091
2092 ; INTERRUPT LOGIC TEST
2093 ; SET ERROR INTERRUPT ENABLE
2094 ; SET T NON-EX MEM INTERRUPT FLAG
2095 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2096
2097 ; TEST 37
2098 ; *****
2099 006016 012737 000037 001226 TST37: MOV #37, TSTNO
2100 006024 012737 006110 001216 MOV #TST40, NEXT
2101 006032 104412 MSTCLR
2102 006034 004737 016042 JSR PC, SETV
2103 006040 006072 1S
2104 006042 006074 2S
2105 006044 052777 000010 173312 BIS #BIT3, @DQTCR
2106 006052 052777 000020 173306 BIS #BIT4, @DQERR

```

```

; RECEIVER WILL INTERRUPT TO 1S
; TRANSMITTER WILL INTERRUPT TO 2S
; SET ERROR INTERRUPT ENABL
; SET T LATENCY INTERRUPT FLAG
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
; TRANSMITTER DID NOT INTERRUPT
; WITH ERROR INTERRUPT ENABL AND
; T LATENCY INTERRUPT FLAG SET
; UNEXPECTED RECEIVER INTERRUPT
; TRANSMITTER SHOULD INTERRUPT TO HERE
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1S
; TRANSMITTER WILL INTERRUPT TO 2S
; SET R LATENCY INTERRUPT FLAG
; SET PROCESSOR PRIORITY TO 0
; WINDOW FOR INTERRUPTS
; TRANSMITTER DID NOT INTERRUPT
; WITH ERROR INTERRUPT ENABL AND
; R LATENCY INTERRUPT FLAG SET
; UNEXPECTED RECEIVER INTERRUPT
; TRANSMITTER SHOULD INTERRUPT TO HERE
; RESTORE STACK
; RESTORE TRAPCATCHER
; CHECK FOR ITERATIONS, LOOP

; CLEAR INTERFACE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 1S
; TRANSMITTER WILL INTERRUPT TO 2S
; SET ERROR INTERRUPT ENABL
; SET T NON-EX MEM INTERRUPT FLAG

```

# E04

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```

2107 006060 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2108 006064 000240 NOP ;WINDOW FOR INTERRUPTS
2109 006066 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2110 006070 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND
2111 ;T NON-EX MEM INTERRUPT FLAG SET
2112 006072 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2113 006074 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2114 006076 012706 001200 3$: MOV #STACK, SP ;RESTORE STACK
2115 006102 004737 016074 JSR PC, RECAT ;RESTORE TRAPCATCHER
2116 006106 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2117
2118 ; INTERRUPT LOGIC TEST
2119 ; SET ERROR INTERRUPT ENABLE
2120 ; SET R NON-EX MEM INTERRUPT FLAG
2121 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2122
2123 ; TEST 40
2124 ; *****
2125 006110 012737 000040 001226 TST40: MOV #40, TSTNO
2126 006116 012737 006202 001216 MOV #TST41, NEXT
2127 006124 104412 MSTCLR ; CLEAR INTERFACE
2128 006126 004737 016042 JSR PC, SETV ; SET UP INTERRUPT VECTORS
2129 006132 006164 1$ ; RECEIVER WILL INTERRUPT TO 1$
2130 006134 006166 2$ ; TRANSMITTER WILL INTERRUPT TO 2$
2131 006136 052777 000010 173220 BIS #BIT3, DQTCR ; SET ERROR INTERRUPT ENABL
2132 006144 052777 000040 173214 BIS #BIT5, DQERR ; SET R NON-EX MEM INTERRUPT FLAG
2133 006152 005037 177776 CLR PS ; SET PROCESSOR PRIORITY TO 0
2134 006156 000240 NOP ; WINDOW FOR INTERRUPTS
2135 006160 104001 HLT 1 ; TRANSMITTER DID NOT INTERRUPT
2136 006162 000402 BR 3$ ; WITH ERROR INTERRUPT ENABL AND
2137 ; R NON-EX MEM INTERRUPT FLAG SET
2138 006164 104003 1$: HLT 3 ; UNEXPECTED RECEIVER INTERRUPT
2139 006166 000240 2$: NOP ; TRANSMITTER SHOULD INTERRUPT TO HERE
2140 006170 012706 001200 3$: MOV #STACK, SP ; RESTORE STACK
2141 006174 004737 016074 JSR PC, RECAT ; RESTORE TRAPCATCHER
2142 006200 104400 4$: SCOPE ; CHECK FOR ITERATIONS, LOOP
2143
2144 ; INTERRUPT LOGIC TEST
2145 ; SET ERROR INTERRUPT ENABLE
2146 ; SET R BCC ERROR INTERRUPT FLAG
2147 ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
2148
2149 ; TEST 41
2150 ; *****
2151 006202 012737 000041 001226 TST41: MOV #41, TSTNO
2152 006210 012737 006274 001216 MOV #TST42, NEXT
2153 006216 104412 MSTCLR ; CLEAR INTERFACE
2154 006220 004737 016042 JSR PC, SETV ; SET UP INTERRUPT VECTORS
2155 006224 006256 1$ ; RECEIVER WILL INTERRUPT TO 1$
2156 006226 006260 2$ ; TRANSMITTER WILL INTERRUPT TO 2$
2157 006230 052777 000010 173126 BIS #BIT3, DQTCR ; SET ERROR INTERRUPT ENABL
2158 006236 052777 000100 173122 BIS #BIT6, DQERR ; SET R BCC ERROR INTERRUPT FLAG
2159 006244 005037 177776 CLR PS ; SET PROCESSOR PRIORITY TO 0
2160 006250 000240 NOP ; WINDOW FOR INTERRUPTS
2161 006252 104001 HLT 1 ; TRANSMITTER DID NOT INTERRUPT
2162 006254 000402 BR 3$ ; WITH ERROR INTERRUPT ENABL AND
  
```





G04

2219	006454	000401		1S:	BR	3S			:GOOD FOR RX
2220	006456	104002		2S:	HLT	2			:TX SHOULD NOT HAVE INTERRUPTED
2221	006460	005077	172674	3S:	CLR	JDQRCR			:CLEAR RXCSR
2222	006464	005077	172674		CLR	JDQTCR			:CLEAR TX CSR
2223	006470	012706	001200		MOV	#STACK, SP			:RESTORE STACK POINTER
2224	006474	004737	016074		JSR	PC, RECAT			:RESET VECTORS
2225	006500	104400			SCOPE				:SCOPE THE TEST

:VERIFY THAT THE TRANSMITTER INTERUPTS  
:ONLY ONCE WHEN IT IS ENABLED.

: TEST 44  
:\*\*\*\*\*

2233	006502	012737	000044	001226	TST44:	MOV	#44, TSTNO		
2234	006510	012737	006606	001216		MOV	#TST45, NEXT		
2235	006516	104412				MSTCLR			
2236	006520	004737	016042			JSR	PC, SETV		
2237	006524	006572				1S			
2238	006526	006576				2S			
2239	006530	012737	000340	177776		MOV	#340, PS		
2240	006536	012777	000240	172620		MOV	#240, JDQTCR		
2241	006544	012700	177777			MOV	#-1, R0		
2242	006550	005002				CLR	R2		
2243	006552	005037	177776			CLR	PS		
2244	006556	105202				INCB	R2		
2245	006560	001376				BNE	.-2		
2246	006562	005700				TST	R0		
2247	006564	001401				BEQ	+.4		
2248	006566	104001				HLT	1		
2249	006570	104400				SCOPE			
2250	006572	104003			1S:	HLT	3		
2251	006574	000002				RTI			
2252	006576	005100			2S:	COM	R0		
2253	006600	001401				BEQ	+.4		
2254	006602	104002				HLT	2		
2255	006604	000002				RTI			

:VERIFY THAT THE RECEIVER INTERUPTS  
:ONLY ONCE WHEN IT IS ENABLED.

: TEST 45  
:\*\*\*\*\*

2261	006606	012737	000045	001226	TST45:	MOV	#45, TSTNO		
2262	006614	012737	006712	001216		MOV	#TST46, NEXT		
2263	006622	104412				MSTCLR			
2264	006624	004737	016042			JSR	PC, SETV		:INIT DQ11
2265	006630	006676				1S			:GO AND SET VECTORS
2266	006632	006706				2S			:RX TO 1S
2267	006634	012737	000340	177776		MOV	#340, PS		:TX TO 2S
2268	006642	012777	000240	172510		MOV	#240, JDQRCR		:LOCK OUT INTERUPTS
2269	006650	012700	177777			MOV	#-1, R0		:SET RX PRI DONE AND IE
2270	006654	005002				CLR	R2		:SET FOR CKECK
2271	006656	005037	177776			CLR	PS		:ZERO COUNTER
2272	006662	105202				INCB	R2		:ENABLE INTERUPTS
2273	006664	001376				BNE	.-2		:START COUNTING
2274	006666	005700				TST	R0		:LOOP HERE

:IS CHECKER 0



# H04

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```
2275 006670 001401 BEQ +4 ;BR IF YES
2276 006672 104000 HLT 0 ;EITHER RX DID NOT INTERRUPT; OR MORE THAN ONCE
2277 006674 104400 SCOPE ;SCOPE THE TEST
2278 006676 005100 1S: COM R0 ;CHECK INTERRUPT
2279 006700 001401 BEQ +4 ;BR IF FIRST TIME HERE
2280 006702 104003 HLT 3 ;RX INTERRUPTED MORE THAN ONCE
2281 006704 000002 RTI ;GO BACK AND DELAY
2282 006706 104002 2S: HLT 2 ;UNEXPECTED TX INTERRUPT
2283 006710 000002 RTI ;RETURN
```

```
;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 7 PRIORITY.
```

## ; TEST 46

```
;*****
2294 006712 012737 000046 001226 TST46: MOV #46,TSTNO
2295 006720 012737 007014 001216 MOV #TST47,NEXT
2296 006726 104412 MSTCLR
2297 006730 004737 016042 JSR PC,SETV
2298 006734 006766 1S:
2299 006736 006772 2S:
2300 006740 012700 177777 MOV #-1,R0
2301 006744 012737 000340 177776 MOV #340,PS ;SET PRIORITY
2302 006752 012777 000240 172404 MOV #240,ADQTCR ;SET PRI DONE AND IE
2303 006760 000240 NOP
2304 006762 000240 NOP
2305 006764 000403 BR 3S
2306 006766 104003 1S: HLT 3 ;CONTINUE TEST
2307 006770 000002 RTI ;UNEXPECTED RX INTERRUPT
2308 006772 005100 2S: COM R0 ;CONTINUE TEST
2309 006774 012706 001200 3S: MOV #STACK,SP ;CHECK INTERRUPT
2310 007000 005700 TST R0 ;SET STACK POINTER
2311 007002 001001 BNE +4 ;CHECK INTERRUPT POINTER
2312 007004 104002 HLT 2
2313 007006 005077 172352 CLR ADQTCR
2314 007012 104400 SCOPE
```

```
;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 6 PRIORITY.
```

## ; TEST 47

```
;*****
2324 007014 012737 000047 001226 TST47: MOV #47,TSTNO
2325 007022 012737 007116 001216 MOV #TST50,NEXT
2326 007030 104412 MSTCLR
2327 007032 004737 016042 JSR PC,SETV
2328 007036 007070 1S:
2329 007040 007074 2S:
2330 007042 012700 177777 MOV #-1,R0
```





J04

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```

2387 007236 004737 016042 JSR PC,SETV ;SET VECTORS
2388 007242 007274 1S ;RX INTERRUPTS TO 1S
2389 007244 007300 2S ;TX INTERRUPTS TO 2S
2390 007246 012700 177777 MOV #1,RO ;SET CHECKER
2391 007252 012737 000200 177776 MOV #200,PS ;SET PRIORITY
2392 007260 012777 000240 172076 MOV #240,ADQTCR ;SET PRI DONE AND IE
2393 007266 000240 NOP ;
2394 007270 000240 NOP ;
2395 007272 000403 BR 3S ;CONTINUE TEST
2396 007274 104003 1S: HLT 3 ;UNEXPECTED RX INTERRUPT
2397 007276 000002 RTI ;CONTINUE TEST
2398 007300 005100 2S: COM RO ;CHECK INTERRUPT
2399 007302 012706 001200 3S: MOV #STACK,SP ;SET STACK POINTER
2400 007306 005700 TST RO ;CHECK INTERRUPT POINTER
2401 007310 001401 BEQ +4 ;
2402 007312 104001 HLT 1 ;
2403 007314 005077 172044 CLR ADQTCR ;
2404 007320 104400 SCOPE ;
;
; IF THE DATA SET CONTROL OPTION IS INSTALLED,
; TEST 52 WILL BE EXECUTED
2412 007322 032737 010000 001510 CHKBA: BIT #BABIT,DQSTAT
2413 007330 001435 BEQ CHKCA1
;
; INTERRUPT LOGIC TEST
; SET DATA SET INTERRUPT ENABLE
; SET DATA SET INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
;
; TEST 52
; *****
2422 007332 012737 000052 001226 tst52: MOV #52,TSTNO
2423 007340 012737 007426 001216 MOV #TST53,NEXT
2424 007346 104412 MSTCLR ;CLEAR INTERFACE
2425 007350 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2426 007354 007406 1S ;RECEIVER WILL INTERRUPT TO 1S
2427 007356 007410 2S ;TRANSMITTER WILL INTERRUPT TO 2S
2428 007360 052777 000020 171776 BIS #BIT4,ADQTCR ;SET DATA SET INTERRUPT ENABL
2429 007366 052777 100000 171770 BIS #BIT15,ADQTCR ;SET DATA SET INTERRUPT FLAG
2430 007374 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2431 007400 000240 NOP ;WINDOW FOR INTERRUPTS
2432 007402 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2433 007404 000402 BR 3S ;WITH DATA SET INTERRUPT ENABL AND
;DATA SET INTERRUPT FLAG SET
2435 007406 104003 1S: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2436 007410 000240 2S: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2437 007412 012706 001200 3S: MOV #STACK,SP ;RESTORE STACK
2438 007416 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
2439 007422 104400 4S: SCOPE ;CHECK FOR ITERATIONS, LOOP

```













```

2664 ; DONE (SECONDARY)=1, INTERRUPT ENEABLE=1,
2665 ; P/S=1
2666 010544 017704 170610 MOV 2DQRCR,R4 ;(R4)=ACTUAL DATA IN RECEIVER CONTROL REGISTER
2667 010550 042704 177400 BIC #177400,R4 ;CLEAR UNWANTED BITS
2668 010554 020504 CMP R5,R4 ;ARE EXPECTED AND RECEIVED DATA THE SAME
2669 010556 001401 BEQ 6$
2670 010560 104004 HLT 4 ;RECEIVER STATUS ERROR
2671 010562 005005 6$: CLR R5 ;(R5)=EXPECTED DATA IN ERROR REGISTER, 0
2672 010564 013703 001366 MOV DQERR,R3 ;ADDRESS OF ERROR REGISTER
2673 010570 117704 170572 MOVB 2DQERR,R4 ;(R4)TUAL DATA IN ERROR REGISTER
2674 010574 001401 BEQ 7$
2675 010576 104006 HLT 6 ;ERROR FLAG(S) SET
2676 010600 112777 000004 170562 7$: MOVB #4,2DQREG ;SELECT RECEIVER BUS ADDRESS (SECONDARY)
2677 010606 012702 000004 MOV #4,R2 ;ADDRESS OF RECEIVER BUS ADDRESS
2678 ;SECONDARY REGISTER
2679 010612 013703 001372 MOV DQSEC,R3 ;ADDRESS OF SECONDARY REGISTER
2680 010616 012705 017167 MOV #RBUF+1,R5 ;(R5)=EXPECTED DATA IN
2681 ;RECEIVER BUS ADDRESS (SECONDARY) REGISTER,
2682 ;RBUF+1
2683 010622 017704 170544 MOV 2DQSEC,R4 ;(R4)=ACTUAL DATA IN RECEIVER
2684 ;BUS ADDRESS REGISTER (SECONDARY)
2685 010626 020504 CMP R5,R4 ;ARE EXPECTED AND RECEIVED DATA THE SAME
2686 010630 001401 BEQ 10$
2687 010632 104007 HLT 7 ;BUS ADDRESS ERROR
2688 010634 105277 170530 10$: INCB 2DQREG
2689 010640 005202 INC R2
2690 010642 012705 000000 MOV #0,R5
2691 010646 017704 170520 MOV 2DQSEC,R4
2692 010652 020504 CMP R5,R4
2693 010654 001401 BEQ 11$
2694 010656 104010 HLT 10 ;CHARACTER COUNT ERROR
2695 010660 012705 000000 11$: MOV #0,R5
2696 010664 012703 017166 MOV #RBUF,R3
2697 010670 013704 017166 MOV RBUF,R4
2698 010674 020504 CMP R5,R4
2699 010676 001401 BEQ QZX
2700 010700 104011 HLT 11
2701 010702 104400 QZX: SCOPE
2702
2703 ; TRANSMITTER BASIC NPR LOGIC TEST (USING SECONDARY BUS ADDRESS AND CHARACTER COU
2704 ; EXPECTED RESULTS
2705 ; TRANSMITTER DONE INTERRUPT OCCURS
2706 ; TRANSMITTER DONE (SECONDARY) = 1
2707 ; TRANSMITTER GO = 0
2708 ; TRANSMITTER P/S = 1
2709 ; NO ERROR FLAGS ARE SET
2710
2711 ; TRANSMITTER BUS ADDRESS (SECONDARY) = TBUF+1
2712 ; TRANSMITTER CHARACTER COUNT (SECONDARY) = 0
2713 ; CONTENTS OF TRANSMITTER BUFFER = 177777
2714
2715 ; TEST 56
2716 ; *****
2717 010704 012737 000056 001226 TST56: MOV #56,TSTNO
2718 010712 012737 010730 001214 MOV #15,RETURN
2719 010720 012737 011330 001216 MOV #TST57,NEXT

```





```

2776 011224 012702 000006      MOV      #6,R2          ;ADDRESS OF TRANSMITTER BUS ADDRESS
2777                                ;SECONDARY REGISTER
2778 011230 013703 001372      MOV      DQSEC,R3      ;ADDRESS OF SECONDARY REGISTER
2779 011234 012705 017171      MOV      #TBUF+1,R5    ;(R5)=EXPECTED DATA IN
2780                                ;TRANSMITTER BUS ADDRESS (SECONDARY) REGISTER,
2781                                ;TBUF+1
2782 011240 017704 170126      MOV      @DQSEC,R4     ;(R4)=ACTUAL DATA IN TRANSMITTER
2783                                ;BUS ADDRESS REGISTER (SECONDARY)
2784 011244 020504                CMP      R5,R4         ;ARE EXPECTED AND RECEIVED DATA THE SAME
2785 011246 001401                BEQ     10$
2786 011250 104007                HLT     7              ;BUS ADDRESS ERROR
2787 011252 105277 170112      10$: INCB   @DQREG
2788 011256 005202                INC     R2
2789 011260 012705 000000      MOV      #0,R5
2790 011264 017704 170102      MOV      @DQSEC,R4
2791 011270 020504                CMP      R5,R4
2792 011272 001401                BEQ     11$
2793 011274 104010                HLT     10            ;CHARACTER COUNT ERROR
2794 011276 012705 177777      11$: MOV      #177777,R5
2795 011302 112777 000013 170060  MOVB    #13,@DQREG
2796 011310 012702 000013      MOV      #13,R2
2797 011314 017704 170052      MOV      @DQSEC,R4
2798 011320 020504                CMP      R5,R4
2799 011322 001401                BEQ     12$
2800 011324 104012                HLT     12
2801 011326 104400      12$: SCOPE
2802
2803                                ;RECEIVER NON-EXISTANT MEMORY TIMEOUT TEST
2804                                ; (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
2805                                ;EXPECTED RESULTS
2806                                ;RECEIVER DONE INTERRUPT OCCURS
2807                                ;RECEIVER DONE (PRIMARY) = 1
2808                                ;RECEIVER GO = 0
2809                                ;RECEIVER P/S = 1
2810                                ;RECEIVER NON EXISTANT MEMORY ERROR FLAG = 1
2811                                ;
2812                                ;RECEIVER BUS ADDRESS (PRIMARY) = RBUF+1
2813                                ;RECEIVER CHARACTER COUNT (PRIMARY) = 0
2814
2815                                ; TEST 57
2816                                ;*****
2817 011330 012737 000057 001226  TST57: MOV      #57,TSTNO
2818 011336 012737 011362 001214      MOV      #1$,RETURN
2819 011344 012737 011624 001216      MOV      #TST60,NEXT
2820 011352 012737 000340 177776      MOV      #340,PS
2821 011360 104413                MEMCLR
2822 011362 104412      1$: MSTCLR
2823 011364 004737 016024      JSR     PC,SETMNT
2824 011370 004737 016042      JSR     PC,SETV
2825 011374 011472                3$
2826 011376 011474                4$
2827 011400 004737 016122      JSR     PC,SETBABC
2828 011404 000 140      .BYTE 0,140
2829 011406 177320                NON.EX
2830 011410 177777                -1
2831 011412 012777 000040 167740      MOV      #BITS,@DQRCR ;SET RECEIVER PRIMARY INTERRUPT ENABLE

```



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```

2832 011420 052777 000001 167732      BIS      #BIT0, DQRCR
2833 011426 112777 000012 167734      MOVB    #12, DQREG
2834 011434 052777 000020 167730      BIS      #BIT4, DQSEC
2835 011442 005037 177776      CLR     PS
2836 011446 012737 002000 001244      MOV     #2000, TEMP1
2837 011454 005337 001244      2$:    DEC     TEMP1
2838 011460 001375      BNE     2$
2839 011462 012737 000340 177776      MOV     #340, PS
2840 011470 104000      HLT     0
2841 011472 000401      3$:    BR     5$
2842 011474 104002      4$:    HLT     2
2843 011476 012706 001200      5$:    MOV     #STACK, SP
2844 011502 012705 000244      MOV     #244, R5
2845
2846
2847 011506 017704 167646      MOV     DQRCR, R4
2848 011512 042704 177400      BIC     #177400, R4
2849 011516 020504      CMP     R5, R4
2850 011520 001401      BEQ     6$
2851 011522 104004      HLT     4
2852 011524 005005      6$:    CLR     R5
2853 011526 013703 001366      MOV     DQERR, R3
2854 011532 017704 167630      MOV     DQERR, R4
2855 011536 100401      BMI     7$
2856 011540 104006      HLT     6
2857 011542 112777 000000 167620      7$:    MOVB    #0, DQREG
2858 011550 012702 000000      MOV     #0, R2
2859
2860 011554 013703 001372      MOV     DQSEC, R3
2861 011560 012705 177321      MOV     #NON.EX+1, R5
2862
2863
2864 011564 017704 167602      MOV     DQSEC, R4
2865
2866 011570 020504      CMP     R5, R4
2867 011572 001401      BEQ     10$
2868 011574 104007      HLT     7
2869 011576 105277 167566      10$:   INCB   DQREG
2870 011602 005202      INC     R2
2871 011604 012705 000000      MOV     #0, R5
2872 011610 017704 167556      MOV     DQSEC, R4
2873 011614 020504      CMP     R5, R4
2874 011616 001401      BEQ     11$
2875 011620 104010      HLT     10
2876 011622 104400      11$:   SCOPE
2877
2878      ; TRANSMITTER NON-EXISTANT MEMORY TIMEOUT TEST
2879      ; (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
2880      ; EXPECTED RESULTS
2881      ;
2882      ; TRANSMITTER DONE INTERRUPT OCCURS
2883      ; TRANSMITTER DONE (PRIMARY) = 1
2884      ; TRANSMITTER GO = 0
2885      ; TRANSMITTER P/S = 1
2886      ; TRANSMITTER NON EXISTANT MEMORY ERROR FLAG = 1
2887      ;
      ; TRANSMITTER BUS ADDRESS (PRIMARY) = TBUF+1

```

# F05

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```

2888                                     ;          TRANSMITTER CHARACTER COUNT (PRIMARY) = 0
2889
2890                                     ; TEST 60
2891                                     ; *****
2892 011624 012737 000060 001226 TST60: MOV      #60,TSTNO
2893 011632 012737 011656 001214      MOV      #1$,RETURN
2894 011640 012737 012106 001216      MOV      #TST61,NEXT
2895 011646 012737 000340 177776      MOV      #340,PS
2896 011654 104413          MEMCLR
2897 011656 104412          1$: MSTCLR
2898 011660 004737 016024          JSR      PC,SETMNT
2899 011664 004737 016042          JSR      PC,SETV
2900 011670 011754          3$:
2901 011672 011756          4$:
2902 011674 004737 016122          JSR      PC,SETBABC
2903 011700 002          .BYTE 2,140
2904 011702 177320          NON.EX
2905 011704 177777          -1
2906 011706 012777 000040 167450      MOV      #BITS,ADQTCR
2907 011714 052777 000001 167442      BIS      #BIT0,ADQTCR
2908 011722 005037 177776          CLR      PS
2909 011726 012737 002000 001244      MOV      #2000,TEMP1
2910 011734 005337 001244          2$: DEC      TEMP1
2911 011740 001375          BNE
2912 011742 012737 000340 177776      MOV      #340,PS
2913 011750 104001          HLT      1
2914 011752 000402          BR
2915 011754 104003          3$: HLT      3
2916 011756 000240          4$: NOP
2917 011760 012706 001200          5$: MOV      #STACK,SP
2918 011764 012705 000244          MOV      #244,R5
2919
2920
2921 011770 017704 167370          MOV      ADQTCR,R4
2922 011774 042704 177400          BIC      #177400,R4
2923 012000 020504          CMP      R5,R4
2924 012002 001401          BEQ      6$
2925 012004 104005          HLT      5
2926 012006 005005          6$: CLR      R5
2927 012010 013703 001366          MOV      DQERR,R3
2928 012014 017704 167346          MOV      ADQERR,R4
2929 012020 100401          BMI      7$
2930 012022 104006          HLT      6
2931 012024 112777 000002 167336          7$: MOVB   #2,ADQREG
2932 012032 012702 000002          MOV      #2,R2
2933
2934 012036 013703 001372          MOV      DQSEC,R3
2935 012042 012705 177321          MOV      #NON.EX+1,R5
2936
2937
2938 012046 017704 167320          MOV      ADQSEC,R4
2939
2940 012052 020504          CMP      R5,R4
2941 012054 001401          BEQ      10$
2942 012056 104007          HLT      7
2943 012060 105277 167304          10$: INCB  ADQREG

```

```

; LOCK OUT INTERRUPTS
; CLEAR INTERFACE MEMORIES
; MASTER CLEAR INTERFACE
; SET MAINTENANCE MODE
; SET UP INTERRUPT VECTORS
; RECEIVER WILL INTERRUPT TO 3$
; TRANSMITTER WILL INTERRUPT TO 4$

; SET TRANSMITTER PRIMARY INTERRUPT ENABLE
; SET TRANSMITTER GO
; ENABLE INTERRUPTS
; SET UP DELAY
; WAIT FOR INTERRUPTS AND NPRS

; LOCK OUT INTERRUPTS
; TRANSMITTER DID NOT INTERRUPT

; UNEXPECTED RECEIVER INTERRUPT

; RESTORE PROCESSOR STACK
; (R5)=EXPECTED DATA IN TRANSMITTER CONTROL REGIS
; DONE (PRIMARY)=1, INTERRUPT ENEABLE=1,
; P/S=1
; (R4)=ACTUAL DATA IN TRANSMITTER CONTROL REGISTE
; CLEAR UNWANTED BITS
; ARE EXPECTED AND RECEIVED DATA THE SAME

; TRANSMITTER STATUS ERROR
; (R5)=EXPECTED DATA IN ERROR REGISTER, 0
; ADDRESS OF ERROR REGISTER
; (R4)TUAL DATA IN ERROR REGISTER

; ERROR FLAG(S) NOT SET
; SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
; ADDRESS OF TRANSMITTER BUS ADDRESS
; SECONDARY REGISTER
; ADDRESS OF SECONDARY REGISTER
; (R5)=EXPECTED DATA IN
; TRANSMITTER BUS ADDRESS (PRIMARY) REGISTER,
; TBUF+1
; (R4)=ACTUAL DATA IN TRANSMITTER
; BUS ADDRESS REGISTER (PRIMARY)
; ARE EXPECTED AND RECEIVED DATA THE SAME

; BUS ADDRESS ERROR

```



# G05

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```

2944 012064 005202          INC      R2
2945 012066 012705 000000    MOV      #0,R5
2946 012072 017704 167274    MOV      @DQSEC,R4
2947 012076 020504          CMP      R5,R4
2948 012100 001401          BEQ      11$
2949 012102 104010          HLT      10          ;CHARACTER COUNT ERROR
2950 012104 104400          11$: SCOPE
2951
2952          ;RECEIVER P/S MASTER CLEAR TEST
2953          ;EXECUTE 1 NPR CYCLE TO FORCE RECEIVER P/S TO A 1
2954          ;ISSUE MASTER CLEAR
2955          ;VERIFY THAT RECEIVER P/S WAS CLEARED
2956
2957          ; TEST 61
2958          ;*****
2959 012106 012737 000061 001226 1$T61: MOV      #61,TSTNO
2960 012114 012737 012140 001214    MOV      #1$,RETURN
2961 012122 012737 012272 001216    MOV      #TST62,NEXT
2962 012130 012737 000340 177776    MOV      #340,P$          ;LOCK OUT INTERRUPTS.
2963 012136 104413          MEMCLR
2964 012140 104412          1$: MSTCLR          ;MASTER CLEAR INTERFACE
2965 012142 004737 016024          JSR      PC,SETMNT        ;SET MAINTENANCE MODE
2966 012146 004737 016122          JSR      PC,SETBABC
2967 012152 000          .BYTE 0,0
2968 012154 017166          RBUF
2969 012156 177777          -1
2970 012160 052777 000001 167172    BIS      #BIT0,@DQRCR
2971 012166 112777 000012 167174    MOV      #12,@DQREG
2972 012174 052777 000020 167170    BIS      #BIT4,@DQSEC
2973 012202 012737 002000 001244    MOV      #2000,TEMP1
2974 012210 105777 167144          2$: TSTB     @DQRCR
2975 012214 100412          BMI      3$
2976 012216 005337 001244          DEC      TEMP1
2977 012222 001372          BNE      2$
2978 012224 017704 167130          MOV      @DQRCR,R4
2979 012230 042704 177400          BIC      #177400,R4
2980 012234 012705 000204          MOV      #204,R5
2981 012240 104004          HLT      4          ;SELECT MISC REGISTER
2982 012242 104412          3$: MSTCLR          ;FORCE RX NPR
2983 012244 032777 000020 167106    BIT      #BIT4,@DQRCR
2984 012252 001406          BEQ      4$
2985 012254 005005          CLR      R5
2986 012256 017704 167076          MOV      @DQRCR,R4
2987 012262 042704 177400          BIC      #177400,R4
2988 012266 104004          HLT      4          ;SET FOR TIME OUT
2989 012270 104400          4$: SCOPE          ;PRIMARY DONE UP
2990          ;BR IF PRI DONE SET.
2991          ;DELAY.....
2992          ;KEEP WAITING
2993          ;SAVE THE CSR
2994          ;CLEAR UNWANTED BITS.
2995          ;SET EXPECTED.
2996
2997          ; TRANSMITTER P/S MASTER CLEAR TEST
2998          ;EXECUTE 1 NPR CYCLE TO FORCE TRANSMITTER P/S TO A 1
2999          ;ISSUE MASTER CLEAR
3000          ;VERIFY THAT TRANSMITTER P/S WAS CLEARED
3001
3002          ; TEST 62
3003          ;*****
3004 012272 012737 000062 001226 1$T62: MOV      #62,TSTNO
3005 012300 012737 012324 001214    MOV      #1$,RETURN
  
```

# H05

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```

3000 012306 012737 012442 001216      MOV      #TST63,NEXT
3001 012314 012737 000340 177776      MOV      #340,PS                ;LOCK OUT INTERRUPTS.
3002 012322 104413
3003 012324 104412      1S:     MEMCLR
3004 012326 004737 016024      MSTCLR                ;MASTER CLEAR INTERFACE
3005 012332 004737 016122      JSR      PC,SETMNT      ;SET MAINTENANCE MODE
3006 012336 002      .BYTE   2,0
3007 012340 017170      TBUF
3008 012342 177777      -1
3009 012344 052777 000001 167012      BIS      #BIT0,ADQTCR
3010 012352 012737 002000 001244      MOV      #2000,TEMP1          ;SET FOR TIME OUT
3011 012360 105777 167000      2S:     TSTB      ADQTCR        ;PRIMARY DONE UP
3012 012364 100412      BMI      3S                ;BR IF PRI DONE SET.
3013 012366 005337 001244      DEC      TEMP1              ;DELAY.....
3014 012372 001372      BNE      2S                ;KEEP WAITING
3015 012374 017704 166764      MOV      ADQTCR,R4          ;SAVE THE CSR
3016 012400 042704 177400      BIC      #177400,R4        ;CLEAR UNWANTED BITS.
3017 012404 012705 000204      MOV      #204,R5           ;SET EXPECTED.
3018 012410 104005      HLT      5
3019 012412 104412      3S:     MSTCLR
3020 012414 032777 000020 166742      BIT      #BIT4,ADQTCR
3021 012422 001406      BEQ      4S
3022 012424 005005      CLR      R5
3023 012426 017704 166732      MOV      ADQTCR,R4
3024 012432 042704 177400      BIC      #177400,R4
3025 012436 104005      HLT      5
3026 012440 104400      4S:     SCOPE
3027
3028      ;TRANSMITTER NPR DATA TEST (STEP MODE)
3029      ;EXECUTE 1 TRANSMITTER NPR CYCLE FOR EACH DATA PATTERN 0-177777
3030      ;VERIFY THAT TRANSMITTER BUFFER CONTAINS THE CORRECT DATA
3031
3032      ; TEST 63
3033      ;*****
3034 012442 012737 000063 001226      TST63: MOV      #63,TSTNO
3035 012450 012737 012510 001214      MOV      #1S,RETURN
3036 012456 012737 000010 001222      MOV      #10,ICOUNT
3037 012464 012737 012650 001216      MOV      #.EOP,NEXT
3038 012472 012737 012532 001220      MOV      #2S,LOCK
3039 012500 012737 000340 177776      MOV      #340,PS                ;LOCK OUT INTERRUPTS.
3040 012506 104413      MEMCLR                ;CLEAR ALL MEMEORIES
3041 012510 104412      1S:     MSTCLR          ;INITIALIZE DEVICE
3042 012512 005037 017172      CLR      ZDATA          ;CLEAR POINTER
3043 012516 012700 000000      MOV      #0,R0
3044 012522 013703 001372      MOV      DQSEC,R3        ;SET FOR ERROR
3045 012526 012702 000013      MOV      #13,R2         ;SET FOR ERROR (TX MUX)
3046 012532 104412      2S:     MSTCLR          ;GIVE ANOTHER MASTER CLEAR
3047 012534 004737 015770      JSR      PC,SETSTP
3048 012540 004737 016122      JSR      PC,SETBABC      ;SET BUS ADDR. AND WC
3049 012544 002      .BYTE   2,0
3050 012546 017170      TBUF
3051 012550 177777      -1
3052 012552 013705 017172      MOV      ZDATA,R5        ;SET EXPECTED
3053 012556 010537 017170      MOV      R5,TBUF        ;LOAD CHARACTER
3054 012562 012777 000001 166574      MOV      #BIT0,ADQTCR    ;SET TX GO.
3055 012570 012737 002000 001244      MOV      #2000,TEMP1     ;SET FOR DELAY
  
```



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```

3056 012576 105777 166562      3S:  TSTB  3DQTCRS      ;TX PRI DONE?
3057 012602 100404              BMI   4S          ;BR IF YES
3058 012604 005337 001244      DEC   TEMP1      ;DELAY.
3059 012610 001372              BNE   3S          ;KEEP DELAYING
3060 012612 104003              HLT   3           ;TX PRI DONE FAILED TO SET
3061 012614 112777 000013 166546 4S:  MOVB  813,3DQREG  ;SELECT TX MUX REG.
3062 012622 017704 166544      MOV   3DQSEC,R4  ;READ MUX
3063 012626 020504              CMP   R5,R4      ;GOOD CHARACTER?
3064 012630 001401              BEQ   5S          ;BR IF GOOD
3065 012632 104012              HLT   12          ;DATA COMPARISON ERROR
3066 012634 104401              5S:  SCOP1        ;LOCK ON DATA (SW09=1)
3067 012636 005237 017172      INC   ZDATA      ;UPDATE CHARACTER
3068 012642 005300              DEC   R0          ;UPDATE COUNTER
3069 012644 001332              BNE   2S          ;GO DO MORE CHARACTERS
3070 012646 104400              6S:  SCOPE        ;SCOPE THIS TEST.
3071
3072              ;END OF PASS
3073              ;TYPE NAME OF TEST
3074              ;UPDATE PASS COUNT
3075              ;CHECK FOR EXIT TO ACT-11
3076              ;RESTART TEST
3077
3078 012650 005037 001234      .EOP: CLR   LSTERR      ;CLEAR LAST ERROR PC
3079 012654 005037 001312      CLR   ERRFLG     ;CLEAR ERROR FLAG
3080 012660 005237 001230      INC   PASCNT     ;UPDATE PASS COUNT
3081 012664 104402              TYPE
3082 012666 015100              MEPASS
3083 012670 104402              TYPE
3084 012672 015261              MCSRX
3085 012674 104411              CNVRT
3086 012676 013006              XCSR
3087 012700 104402              TYPE
3088 012702 015267              MVECX
3089 012704 104411              CNVRT
3090 012706 013014              XVEC
3091 012710 104402              TYPE
3092 012712 015275              MPASSX
3093 012714 104411              CNVRT
3094 012716 013022              XPASS
3095 012720 104402              TYPE
3096 012722 015306              MERRX
3097 012724 104411              CNVRT
3098 012726 013030              XERR
3099 012730 013777 001230 166244      MOV   PASCNT,2LIGHTS ;DISPLAY PASS COUNT
3100 012736 005337 001276      DEC   SAVNUM
3101 012742 001013              BNE   RESTRT
3102 012744 013737 001504 001276      MOV   DQNUM,SAVNUM
3103 012752 013701 000042      MOV   2#42,R1
3104 012756 001405              BEQ   RESTRT     ;CHECK FOR ACT-11 OR DDP
3105 012760 000005              RESTRT          ;IF NOT, CONTINUE TESTING
3106 012762
3107 012762 004711      LOGICAL: JSR   PC,(R1)
3108 012764 000240              NOP
3109 012766 000240              NOP
3110 012770 000240              NOP
3111 012772 104414      RESTRT: CKSWR
    
```

3112	012774	012737	002254	001214		MOV	#TST1, RETURN
3113	013002	000137	002254			JMP	TST1
3114	013006	000001			XCSR:	1	
3115	013010	006	002			.BYTE	6,2
3116	013012	001360				DQRCSR	
3117	013014	000001			XVEC:	1	
3118	013016	003	002			.BYTE	3,2
3119	013020	001350				DQRVEC	
3120	013022	000001			XPASS:	1	
3121	013024	006	002			.BYTE	6,2
3122	013026	001230				PASCNT	
3123	013030	000001			XERR:	1	
3124	013032	006	002			.BYTE	6,2
3125	013034	001232				ERRCNT	
3126							
3127							
3128							
3129	013036	104414			.SCOPE:	CKSWR	
3130	013040	032777	040000	166132	TTST:	BIT	#BIT14, ASWR
3131	013046	001407				BEQ	1\$
3132	013050	000432				BR	3\$
3133	013052	105777	166126			TSTB	@TKCSR
3134	013056	100027				BPL	3\$
3135	013060	017700	166122			MOV	@TKDBR, R0
3136	013064	000412				BR	2\$
3137	013066	032777	004000	166104	1\$:	BIT	#SW11, ASWR
3138	013074	001006				BNE	2\$
3139	013076	005237	001224			INC	LPCNT
3140	013102	023737	001224	001222		CMP	LPCNT, ICOUNT
3141	013110	001012				BNE	3\$
3142	013112	105037	001312		2\$:	CLRB	ERRFLG
3143	013116	005037	001224			CLR	LPCNT
3144	013122	012737	000012	001222		MOV	#10., ICOUNT
3145	013130	013737	001216	001214		MOV	NEXT, RETURN
3146	013136	013716	001214		3\$:	MOV	RETURN, (SP)
3147	013142	000002				RTI	
3148	013144	001407			BRW:	1407	
3149	013146	000432			BRX:	432	
3150							
3151							
3152							
3153	013150	104414			.SCOPE1:	CKSWR	
3154	013152	032777	001000	166020		BIT	#SW09, ASWR
3155	013160	001402				BEQ	1\$
3156	013162	013716	001220			MOV	LOCK, (SP)
3157	013166	000002			1\$:	RTI	
3158							
3159							
3160							
3161	013170	010546			.TYPE:	MOV	R5, -(SP)
3162	013172	017605	000002			MOV	@2(SP), R5
3163	013176	062766	000002	000002		ADD	#2, 2(SP)
3164	013204	005737	014660		1\$:	TST	@RDSW
3165	013210	001004				BNE	300\$
3166	013212	032777	010000	165760		BIT	#SW12, ASWR
3167	013220	001024				BNE	3\$

;SCOPE LOOP AND INTERATION HANDLER

;CHECK FOR FREEZE ON CURRENT DATA

;TELETYPE OUTPUT ROUTINE



3168	013222	105715			300\$:	TSTB	(R5)	
3169	013224	100014				BPL	2\$	
3170	013226	105777	165756			TSTB	@TPCSR	
3171	013232	100375				BPL	.-4	
3172	013234	012777	000015	165750		MOV	#15,@TPDBR	
3173	013242	105777	165742			TSTB	@TPCSR	
3174	013246	100375				BPL	.-4	
3175	013250	012777	000012	165734		MOV	#12,@TPDBR	
3176	013256	105777	165726		2\$:	TSTB	@TPCSR	
3177	013262	100375				BPL	2\$	
3178	013264	112577	165722			MOVB	(R5)+,@TPDBR	
3179	013270	001345				BNE	1\$	
3180	013272	012605			3\$:	MOV	(SP)+,R5	
3181	013274	000002				RTI		
3182								
3183								
3184								
3185	013276	010346						
3186	013300	010446			.INSTR:	MOV	R3,-(SP)	
3187	013302	017637	000004	013320		MOV	R4,-(SP)	
3188	013310	062766	000002	000004		MOV	@4(SP),MSG	
3189	013316	104402				ADD	#2,4(SP)	
3190	013320	000000			.INST1:	TYPE		
3191	013322	012704	015452		.MSG:	0		
3192	013326	012703	000007			MOV	#INBUF,R4	
3193	013332	105777	165646		1\$:	MOV	#7,R3	
3194	013336	100375				TSTB	@TKCSR	
3195	013340	117714	165642			BPL	1\$	
3196	013344	142714	000200			MOVB	@TKDBR,(R4)	
3197	013350	121427	000025			BICB	#200,(R4)	
3198	013354	001003				CMPB	(R4),#25	
3199	013356	104402	015040			BNE	200\$	
3200	013362	000755				TYPE,MCRLF		
3201	013364	122427	000015		200\$:	BR	.INST1	
3202	013370	001423				CMPB	(R4)+,#15	
3203	013372	117777	165610	165612		BEQ	INSTR2	
3204	013400	105777	165604		2\$:	MOVB	@TKDBR,@TPDBR	
3205	013404	100375				TSTB	@TPCSR	
3206	013406	005303				BPL	2\$	
3207	013410	001350				DEC	R3	
3208	013412	000402				BNE	1\$	
3209	013414	010346			.INSTE:	BR	.INSTG	
3210	013416	010446				MOV	R3,-(SP)	
3211	013420	104402			.INSTG:	MOV	R4,-(SP)	
3212	013422	015034				TYPE		
3213	013424	005737	014660			MGM		
3214	013430	001402				TST	@RDSW	
3215	013432	104402	015040			BEQ	400\$	
3216	013436	000727			400\$:	TYPE,MCRLF		
3217	013440	012604			BR	.INST1		
3218	013442	012603			INSTR2:	MOV	(SP)+,R4	
3219	013444	000002				MOV	(SP)+,R3	
3220						RTI		
3221								
3222								
3223	013446	010546			.PARAM:	MOV	R5,-(SP)	

;CONVERT ASCII STRING TO OCTAL

;IS IT <↑G>

3224	013450	010446		MOV	R4, -(SP)	
3225	013452	016605	000004	MOV	4(SP), R5	
3226	013456	012537	013652	MOV	(R5)+, LOLIM	
3227	013462	012537	013654	MOV	(R5)+, HILIM	
3228	013466	012537	013656	MOV	(R5)+, DEVADR	
3229	013472	112537	013660	MOVB	(R5)+, LOBITS	
3230	013476	112537	013661	MOVB	(R5)+, ADRCNT	
3231	013502	010566	000004	MOV	R5, 4(SP)	
3232	013506	005005		PARAM1: CLR	R5	
3233	013510	012704	015452	MOV	#INBUF, R4	
3234	013514	122714	000015	CMPB	#15, (R4)	
3235	013520	001420		BEQ	PARERR	
3236	013522	121427	000060	15: CMPB	(R4), #60	
3237	013526	002415		BLT	PARERR	
3238	013530	121427	000067	CMPB	(R4), #67	
3239	013534	003012		BGT	PARERR	
3240	013536	142714	000060	BICB	#60, (R4)	
3241	013542	152405		BISB	(R4)+, R5	
3242	013544	122714	000015	CMPB	#15, (R4)	
3243	013550	001414		BEQ	LIMITS	
3244	013552	006305		ASL	R5	
3245	013554	006305		ASL	R5	
3246	013556	006305		ASL	R5	
3247	013560	000760		BR	15	
3248	013562	122714	000015	PARERR: CMPB	#15, (R4)	; IS FIRST CHARACTER A <CR>
3249	013566	001003		BNE	120\$	
3250	013570	005737	014660	TST	#RDSW	; IS CKSWR ROUTINE BEING USED
3251	013574	001023		BNE	PARTI	
3252	013576	104404		120\$: INSTER		
3253	013600	000742		BR	PARAM1	
3254						
3255						
3256						
3257	013602	020537	013654	LIMITS: CMP	R5, HILIM	
3258	013606	101365		BHI	PARERR	
3259	013610	020537	013652	CMP	R5, LOLIM	
3260	013614	103762		BLO	PARERR	
3261	013616	133705	013660	BITB	LOBITS, R5	
3262	013622	001357		BNE	PARERR	
3263						
3264						
3265						
3266	013624	013704	013656	15: MOV	DEVADR, R4	
3267	013630	010524		MOV	R5, (R4)+	
3268	013632	062705	000002	ADD	#2, R5	
3269	013636	105337	013661	DECB	ADRCNT	
3270	013642	001372		BNE	15	
3271	013644	012604		PARTI: MOV	(SP)+, R4	
3272	013646	012605		MOV	(SP)+, R5	
3273	013650	000002		RTI		
3274	013652	000000		LOLIM: 0		
3275	013654	000000		HILIM: 0		
3276	013656	000000		DEVADR: 0		
3277	013660	000000		LOBITS: 0		
3278		013661		ADRCNT=L0BITS+1		
3279						



# M05

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 DZDQCD.P11 16-DEC-76 13:26 GENERAL UTILITIES (TYPE OUT,ERROR,SCOPE,ETC.)

```

3280                                     ;SAVE PC OF TEST THAT FAILED AND RO-R5
3281
3282 013662 016637 000004 001274 .SAV05: MOV     4(SP),SAVPC
3283
3284                                     ;SAVE RO-R5
3285
3286 013670 010537 001270          SV05:  MOV     R5,SAVR5
3287 013674 010437 001266          MOV     R4,SAVR4
3288 013700 010337 001264          MOV     R3,SAVR3
3289 013704 010237 001262          MOV     R2,SAVR2
3290 013710 010137 001260          MOV     R1,SAVR1
3291 013714 010037 001256          MOV     R0,SAVR0
3292 013720 000002
3293
3294                                     ;RESTORE RO-R5
3295
3296 013722 013700 001256          .RES05: MOV     SAVR0,R0
3297 013726 013701 001260          MOV     SAVR1,R1
3298 013732 013702 001262          MOV     SAVR2,R2
3299 013736 013703 001264          MOV     SAVR3,R3
3300 013742 013704 001266          MOV     SAVR4,R4
3301 013746 013705 001270          MOV     SAVR5,R5
3302 013752 000002
3303
3304                                     ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3305
3306 013754 104402          .CONVR: TYPE
3307 013756 015040          MCRLF
3308 013760 010046          .CNVRT: MOV     RO,-(SP)
3309 013762 010146          MOV     R1,-(SP)
3310 013764 010346          MOV     R3,-(SP)
3311 013766 010446          MOV     R4,-(SP)
3312 013770 010546          MOV     R5,-(SP)
3313 013772 017601 000012          MOV     @12(SP),R1
3314 013776 013737 015514 001250          MOV     TEMP,TEMP3
3315 014004 062766 000002 000012          ADD     #2,12(SP)
3316 014012 012137 014174          MOV     (R1)+,WRDCNT
3317 014016 112137 014176          1S:  MOVB  (R1)+,CHRCNT
3318 014022 112137 014177          MOVB  (R1)+,SPACNT
3319 014026 013137 014200          MOV     @2(R1)+,BINWRD
3320 014032 013704 014200          2S:  MOV     BINWRD,R4
3321 014036 113705 014176          MOVB  CHRCNT,R5
3322 014042 012700 015514          MOV     #TEMP,R0
3323 014046 010403          3S:  MOV     R4,R3
3324 014050 042703 177770          BIC     #177770,R3
3325 014054 062703 000060          ADD     #060,R3
3326 014060 110320          MOVB  R3,(R0)+
3327 014062 000241          CLC
3328 014064 006004          ROR     R4
3329 014066 000241          CLC
3330 014070 006004          ROR     R4
3331 014072 000241          CLC
3332 014074 006004          ROR     R4
3333 014076 005305          DEC     R5
3334 014100 001362          BNE    3S
3335 014102 012703 015556          MOV     #MDATA,R3
  
```

3336	014106	114023			4S:	MOVB	-(R0),(R3)+	
3337	014110	105337	014176			DECB	CHRCNT	
3338	014114	001374				BNE	4S	
3339	014116	105737	014177			TSTB	SPACNT	
3340	014122	001405				BEQ	6S	
3341	014124	112723	000040		5S:	MOVB	#040,(R3)+	
3342	014130	105337	014177			DECB	SPACNT	
3343	014134	001373				BNE	5S	
3344	014136	105013			6S:	CLRB	(R3)	
3345	014140	104402				TYPE		
3346	014142	015556				MDATA		
3347	014144	005337	014174			DEC	WRDCNT	
3348	014150	001322				BNE	1S	
3349	014152	013737	001250	015514		MOV	TEMP3,TEMP	
3350	014160	012605				MOV	(SP)+,R5	
3351	014162	012604				MOV	(SP)+,R4	
3352	014164	012603				MOV	(SP)+,R3	
3353	014166	012601				MOV	(SP)+,R1	
3354	014170	012600				MOV	(SP)+,R0	
3355	014172	000002				RTI		
3356	014174	000000				WRDCNT:	0	
3357	014176	000000				CHRCNT:	0	
3358		014177				SPACNT=	CHRCNT+1	
3359	014200	000000				BINWRD:	0	
3360								;TRAP DISPATCH SERVICE
3361								;ARGUMENT OF TRAP IS EXTRACTED
3362								;AND USED AS OFFSET TO OBTAIN POINTER
3363								;TO SELECTED SUBROUTINE
3364								
3365	014202	011646			.TRPSR:	MOV	(SP),-(SP)	;GET PC OF RETURN
3366	014204	162716	000002			SUB	#2,(SP)	;=PC OF TRAP
3367	014210	017616	000000			MOV	2(SP),(SP)	;GET TRP
3368	014214	006316			TRPOK:	ASL	(SP)	;MULTIPLY TRAP ARG BY 2
3369	014216	042716	177001			BIC	#177001,(SP)	;CLEAR UNWANTED BITS
3370	014222	062716	001314			ADD	#.TRPTAB,(SP)	;POINTER TO SUBROUTINE ADDRESS
3371	014226	017616	000000			MOV	2(SP),(SP)	;SUBROUTINE ADDRESS
3372	014232	000136				JMP	2(SP)+	;GO TO SUBROUTINE
3373								
3374								
3375								;ERROR HANDLER
3376	014234	104414			.HLT:	CKSWR		
3377	014236	032777	010000	164734		BIT	#SW12,@SWR	
3378	014244	001406				BEQ	XBX	
3379	014246	105777	164736			TSTB	@TPCSR	
3380	014252	100003				BPL	XBX	
3381	014254	112777	000207	164730		MOVB	#207,@TPDBR	
3382	014262	032777	020000	164710	XBX:	BIT	#SW13,@SWR	
3383	014270	001074				BNE	HALTS	
3384	014272	021637	001234			CMP	(SP),LSTERR	
3385	014276	001404				BEQ	1S	
3386	014300	011637	001234			MOV	(SP),LSTERR	
3387	014304	105037	001312			CLRB	ERRFLG	
3388	014310	104406			1S:	SAVOS		
3389	014312	011605				MOV	(SP),R5	
3390	014314	162705	000002			SUB	#2,R5	
3391	014320	011504				MOV	(R5),R4	



3392	014322	006304		ASL	R4
3393	014324	061504		ADD	(R5), R4
3394	014326	006304		ASL	R4
3395	014330	042704	177001	BIC	#177001, R4
3396	014334	062704	016744	ADD	#.ERRTAB, R4
3397	014340	012437	014432	MOV	(R4)+, ERRMSG
3398	014344	012437	014444	MOV	(R4)+, DATAHD
3399	014350	011437	014456	MOV	(R4), DATABP
3400	014354	105737	001312	TSTB	ERRFLG
3401	014360	001403		BEQ	TYPMSG
3402	014362	005737	014456	TST	DATABP
3403	014366	001027		BNE	TYPDAT
3404	014370	104402		TYPMSG:	TYPE
3405	014372	015317			MTSTN
3406	014374	104411			CNVRT
3407	014376	014556			XTSTN
3408	014400	104402			TYPE
3409	014402	015405			MERRPC
3410	014404	104411			CNVRT
3411	014406	014550			ERTABO
3412	014410	104402			TYPE
3413	014412	015040			MCRLF
3414	014414	112737	177777 001312	MOVB	#-1, ERRFLG
3415	014422	005737	014432	TST	ERRMSG
3416	014426	001402		BEQ	WRKO.FM
3417	014430	104402		TYPE	
3418	014432	000000		ERRMSG:	0
3419	014434			WRKO.FM:	
3420	014434	005737	014444	TST	DATAHD
3421	014440	001402		BEQ	TYPDAT
3422	014442	104402		TYPE	
3423	014444	000000		DATAHD:	0
3424	014446	005737	014456	TYPDAT:	TST
3425	014452	001402		BEQ	DATABP
3426	014454	104410		CONVRT	RESREG
3427	014456	000000		DATABP:	0
3428	014460	104407		RESREG:	RESOS
3429	014462	005777	164512	HALTS:	TST
3430	014466	100005			@SWR
3431	014470	010046			EXITER
3432	014472	016600	000002		BPL
3433	014476	000000			PUSHRO
3434	014500	012600			MOV
3435	014502	104414			2(SP), RO
3436	014504	005237	001232	EXITER:	CKSWR
3437	014510	032777	000400 164462	INC	ERRCNT
3438	014516	001007		BIT	#SWOB, @SWR
3439	014520	032777	002000 164452	BNE	1\$
3440	014526	001407		BIT	#SW10, @SWR
3441	014530	013737	001216 001214	BEQ	2\$
3442	014536	012706	001200	MOV	NEXT RETURN
3443	014542	000177	164446	1\$:	MOV
3444	014546	000002			@STACK, SP
3445	014550	000001		2\$:	JMP
3446	014552	006	002		@RETURN
3447	014554	001274		ERTABO:	1
					.BYTE
					6,2
					SAVPC

```

3448 014556 000001          XTSTN: 1
3449 014560          003      002      .BYTE 3,2
3450 014562 001226          TSTNO
3451          .ENTER HERE ON POWER FAILURE
3452
3453
3454 014564          .PFAIL:
3455 014564 012737 014576 000024  MOV      #RESTART,24          ;SET UP FOR POWER UP TRAP
3456 014572 000000          HALT          ;HALT ON POWER DOWN NORMAL
3457 014574 000777          BR
3458
3459          ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
3460
3461 014576          RESTAR:
3462 014576 012737 014564 000024  MOV      #.PFAIL,24          ;SET UP FOR POWER FAILURE
3463 014604 012706 001200          MOV      #STACK,SP
3464 014610 005037 015514          CLR      TEMP
3465 014614 005237 015514          INC      TEMP
3466 014620 001375          BNE      -4
3467 014622 104402          TYPE
3468 014624 015042          MPFAIL
3469 014626 104411          CNVRT
3470 014630 014652          PFTAB
3471 014632 005037 001312          CLR      ERRFLG
3472 014636 005037 001234          CLR      LSTERR
3473 014642 104412          MSTCLR
3474 014644 104413          MEMCLR
3475 014646 000177 164342          JMP      @RETURN
3476 014652 000001          PFTAB: 1
3477 014654          003      002      .BYTE 3,2
3478 014656 001226          TSTNO
3479
3480
3481          ;CHECK SWITCH REGISTER ROUTINE. CHECKS FOR †G TO ALLOW CHANGING
3482          ;OF LOC.176.
3483          ;LOCATIONS USED:
3484 014660 000000          RDSW: .WORD 0
3485
3486
3487 014662 005737 000042          .CKSWR: TST      @#42
3488 014666 001042          BNE      OUT
3489 014670 022737 000176 001200          CMP      #SWREG,SWR          ;SOFTWARE SWITCH REGISTER PRESENT
3490 014676 001036          BNE      OUT          ;NO, GET OUT
3491 014700 105777 164300          TSTB    @TKCSR          ;YES, WAIT FOR
3492 014704 100033          BPL      OUT          ;READY, GET CHARACTER
3493 014706 017737 164274 013320          MOV      @TKDBR,.MSG          ;AND STRIP OFF
3494 014714 042737 177600 013320          BIC      @177600,.MSG          ;THE GARBAGE
3495 014722 122737 000007 013320          CMPB    @7,.MSG          ;IS IT A †G)
3496 014730 001021          BNE      OUT
3497 014732 104402 015010          TYPE,SCNTG
3498 014736 005137 014660          .CNTLU: COM      @RDSW
3499 014742 104402 015014          TYPE,SMSWR
3500 014746 104411 015002          CNVRT,SWREGC
3501 014752 104403 015023          INSTR,SMNEW
3502 014756 104405          PARAM
3503 014760 000000          0
    
```



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3504	014762	177777				177777
3505	014764	000176				SWREG
3506	014766	000	001		.BYTE	0,1
3507	014770	104402	015040			TYPE,MCRLF
3508	014774	005037	014660		OUT:	CLR 2#RDSW
3509	015000	000002				RTI
3510	015002	000001			SWREGC:	1
3511	015004	006	002		.BYTE	6,2
3512	015006	000176				SWREG
3513	015010	057377	000107		SCNTG:	.ASCIZ <377>/tG/
3514	015014	051777	051127	020075	SMSWR:	.ASCIZ <377>/SWR= /
3515	015022	000				
3516	015023	040	047040	053505	SMNEW:	.ASCIZ / NEW= /
3517	015030	020075	000			
3518		015034			.EVEN	
3519	015034	020040	000077		MGM:	.ASCIZ / ?/
3520	015040	000377			MCRLF:	.ASCIZ <377>
3521	015042	050377	051127	043040	MPFAIL:	.ASCIZ <377>/PWR FAILED. RESTART AT TEST /
3522	015050	044501	042514	027104		
3523	015056	051040	051505	040524		
3524	015064	052122	040440	020124		
3525	015072	042524	052123	000040		
3526	015100	042777	042116	050040	MEPASS:	.ASCIZ <377>/END PASS DZDQC /
3527	015106	051501	020123	055104		
3528	015114	050504	020103	000040		
3529	015122	051377	000		MR:	.ASCIZ <377>/R/
3530	015125	377	051120	043517	MERR2:	.ASCIZ <377>/PROGRAM INDICATES NO DEVICES PRESENT./
3531	015132	040522	020115	047111		
3532	015140	044504	040503	042524		
3533	015146	020123	047516	042040		
3534	015154	053105	041511	051505		
3535	015162	050040	042522	042523		
3536	015170	052116	000056			
3537	015174	044777	051516	043125	MERR3:	.ASCIZ <377>/INSUFFICIENT DATA! /
3538	015202	044506	044503	047105		
3539	015210	020124	040504	040524		
3540	015216	000041				
3541	015220	052377	051505	020124	MTSTPC:	.ASCIZ <377>/TEST PC-/
3542	015226	041520	000055			
3543	015232	046377	041517	020113	MLOCK:	.ASCIZ <377>/LOCK ON SELECTED TEST/
3544	015240	047117	051440	046105		
3545	015246	041505	042524	020104		
3546	015254	042524	052123	000		
3547	015261	103	051123	020072	MCSRX:	.ASCIZ /CSR: /
3548	015266	000				
3549	015267	126	041505	020072	MVECX:	.ASCIZ /VEC: /
3550	015274	000				
3551	015275	120	051501	042523	MPASSX:	.ASCIZ /PASSES: /
3552	015302	035123	000040			
3553	015306	051105	047522	051522	MERRX:	.ASCIZ /ERRORS: /
3554	015314	020072	000			
3555	015317	377	052377	051505	MTSTN:	.ASCIZ <377><377> /TEST NO: /
3556	015324	020124	047516	020072		
3557	015332	000				
3558	015333	377	042523	020124	MNEW:	.ASCIZ <377>/SET SWITCH REG TO DQ11'S DESIRED ACTIVE./
3559	015340	053523	052111	044103		

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3560 015346 051040 043505 052040
3561 015354 020117 050504 030461
3562 015362 051447 042040 051505
3563 015370 051111 042105 040440
3564 015376 052103 053111 027105
3565 015404 000
3566 015405 120 035103 000040 MERRPC: .ASCIZ /PC:/
3567 015412 046777 050101 047440 XHEAD: .ASCIZ <377>/MAP OF DQ11 STATUS/<377>
3568 015420 020106 050504 030461
3569 015426 051440 040524 052524
3570 015434 177523 000
3571 015440
3572 015440 000002 .EVEN
XSTATQ: 2
3573 015442 006 003 .BYTE 6,3
3574 015444 001244 TEMP1
3575 015446 006 002 .BYTE 6,2
3576 015450 001246 TEMP2
3577
3578 .EVEN
3579 ;BUFFERS FOR INPUT-OUTPUT
3580
3581 015452 000000 INBUF: 0
3582 015514 .=. +40
3583 015514 000000 TEMP: 0
3584 015556 015556 .=. +40
3585 015556 000000 MDATA: 0
3586 015620 .=. +40
3587
3588 ;MASTER CLEAR DQ11 INTERFACE
3589
3590 015620 .MSTCLR:
3591 015620 112777 000012 163542 MOVB #12,DQREG
3592 015626 012777 000040 163536 MOV #BITS,DQSEC
3593 015634 000002 RTI
3594
3595 ;CLEAR INTERFACE MEMORIES
3596
3597 015636 .MEMCLR:
3598 015636 105077 163526 CLRB DQREG
3599 015642 012700 000020 MOV #16,R0
3600 015646 152777 000020 163514 1$: BISB #BIT4,DQREG
3601 015654 142777 000140 163506 BICB #140,DQREG
3602 015662 005077 163504 CLR DQSEC
3603 015666 105277 163476 INCB DQREG
3604 015672 005300 DEC R0
3605 015674 001364 BNE 1$
3606 015676 105077 163466 CLRB DQREG
3607 015702 105077 163454 CLRB DQRC5H
3608 015706 012700 000020 MOV #16,R0
3609 015712 112777 000010 163450 2$: MOVB #10,DQREG
3610 015720 005077 163446 CLR DQSEC
3611 015724 112777 000014 163436 MOVB #14,DQREG
3612 015732 005077 163434 CLR DQSEC
3613 015736 105277 163420 INCB DQRC5H
3614 015742 005300 DEC R0
3615 015744 001362 BNE 2$

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```

3616 015746 105077 163410 CLR 3DQRC5H
3617 015752 005077 163402 CLR 3DQRC5R
3618 015756 005077 163402 CLR 3DQTC5R
3619 015762 005077 163400 CLR 3DQERR
3620 015766 000002 RTI
3621
3622 ;SET STEP MODE
3623
3624 015770 112777 000012 163372 SETSTP: MOV  #12,3DQREG
3625 015776 052777 000002 163366 BIS  #BIT1,3DQSEC
3626 016004 000207 RTS  PC
3627
3628 ;SET TEST LOOP
3629
3630 016006 112777 000012 163354 SETLOP: MOV  #12,3DQREG
3631 016014 052777 000010 163350 BIS  #BIT3,3DQSEC
3632 016022 000207 RTS  PC
3633
3634 ;SET MAINTENANCE MODE
3635
3636 016024 112777 000012 163336 SETMNT: MOV  #12,3DQREG
3637 016032 052777 000012 163332 BIS  #BIT1+BIT3,3DQSEC
3638 016040 000207 RTS  PC
3639
3640 ;SET INTERRUPT VECTORS
3641
3642 016042 011605 SETV:  MOV  (SP),R5
3643 016044 012577 163300 MOV  (R5)+,3DQREVC
3644 016050 012777 000340 163274 MOV  #340,3DQRLVL
3645 016056 012577 163272 MOV  (R5)+,3DQTVEC
3646 016062 012777 000340 163266 MOV  #340,3DQTLVL
3647 016070 010516 MOV  R5,(SP)
3648 016072 000207 RTS  PC
3649
3650 ;RESTORE TRAPCATCHER
3651
3652 016074 013777 001352 163246 RECAT: MOV  DQRLVL,3DQREVC
3653 016102 005077 163244 CLR  3DQRLVL
3654 016106 013777 001356 163240 MOV  DQTLVL,3DQTVEC
3655 016114 005077 163236 CLR  3DQTLVL
3656 016120 000207 RTS  PC
3657
3658 ;SET UP BUS ADDRESS AND CHARACTER COUNTS
3659 ;FOR SELECTED FUNCTION
3660
3661 016122 011605 SETBABC: MOV  (SP),R5
3662 016124 112577 163240 MOV  (R5)+,3DQREG
3663 016130 152777 000020 163232 BISB #BIT4,3DQREG
3664 016136 152577 163226 BISB (R5)+,3DQREG
3665 016142 012577 163224 MOV  (R5)+,3DQSEC
3666 016146 142777 000040 163214 BICB #BITS,3DQREG
3667 016154 105277 163210 INCB 3DQREG
3668 016160 012577 163206 MOV  (R5)+,3DQSEC
3669 016164 010516 MOV  R5,(SP)
3670 016166 000207 RTS  PC
3671

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3672  
 3673  
 3674  
 3675

;TABLE OF ERROR MESSAGES

016170	042522	042503	053111	EM0:	.ASCIZ	/RECEIVER DID NOT INTERRUPT/
016223	124	040522	051516	EM1:	.ASCIZ	/TRANSMITTER DID NOT INTERRUPT/
016261	125	042516	050130	EM2:	.ASCIZ	/UNEXPECTED TRANSMITTER INTERRUPT/
016322	047125	054105	042520	EM3:	.ASCIZ	/UNEXPECTED RECEIVER INTERRUPT/
016360	042522	042503	053111	EM4:	.ASCIZ	/RECEIVER STATUS ERROR/
016406	051124	047101	046523	EM5:	.ASCIZ	/TRANSMITTER STATUS ERROR/
016437	105	051122	051117	EM6:	.ASCIZ	/ERROR FLAG(S) SET/
016461	102	051525	040440	EM7:	.ASCIZ	/BUS ADDRESS ERROR/
016503	103	040510	040522	EM10:	.ASCIZ	/CHARACTER COUNT ERROR/
016531	122	041505	044505	EM11:	.ASCIZ	/RECEIVED DATA ERROR/
016555	124	040522	051516	EM12:	.ASCIZ	/TRANSMITTER BUFFER DATA ERROR/
016613	103	047514	045503	EM13:	.ASCIZ	/CLOCK LOSS ERROR/

;TABLE OF DATA HEADERS

016634	042777	050130	041505	DH0:	.ASCIZ	<377>/EXPECTED	RECEIVED	REG ADDRESS/
016675	377	054105	042520	DH1:	.ASCIZ	<377>/EXPECTED	RECEIVED	SEC ADR SEC REG/
				.EVEN				

3676  
 3677  
 3678  
 3679  
 3680  
 3681  
 3682  
 3683  
 3684  
 3685  
 3686  
 3687  
 3688  
 3689  
 3690  
 3691  
 3692  
 3693  
 3694  
 3695  
 3696  
 3697  
 3698  
 3699  
 3700  
 3701  
 3702  
 3703  
 3704  
 3705  
 3706  
 3707  
 3708  
 3709

;TABLE OF POINTERS FOR ERROR OUTPUT

.ERRTAB:EM0  
 0  
 0  
 EM1  
 0  
 0  
 EM2  
 0  
 0  
 EM3  
 0  
 0  
 EM4  
 DH0  
 DT0  
 EM5  
 DH0  
 DT1  
 EM6  
 DH0  
 DT4  
 EM7  
 DH1  
 DT3  
 EM10  
 DH1  
 DT3  
 EM11  
 DH0  
 DT4  
 EM12  
 DH1



# H06

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3710	017044	017126			DT3
3711	017046	016613			EM13
3712	017050	016634			DHO
3713	017052	017110			DT2
3714					
3715					;DATA TABLES FOR ERROR OUTPUT
3716					
3717	017054	000003			DT0: 3
3718	017056	006	004		.BYTE 6,4
3719	017060	001270			SAVR5
3720	017062	006	004		.BYTE 6,4
3721	017064	001266			SAVR4
3722	017066	006	004		.BYTE 6,4
3723	017070	001360			DQRCR
3724	017072	000003			DT1: 3
3725	017074	006	004		.BYTE 6,4
3726	017076	001270			SAVR5
3727	017100	006	004		.BYTE 6,4
3728	017102	001266			SAVR4
3729	017104	006	004		.BYTE 6,4
3730	017106	001364			DQTCR
3731	017110	000003			DT2: 3
3732	017112	003	007		.BYTE 3,7
3733	017114	001270			SAVR5
3734	017116	003	007		.BYTE 3,7
3735	017120	001266			SAVR4
3736	017122	006	000		.BYTE 6,0
3737	017124	001366			DQERR
3738	017126	000004			DT3: 4
3739	017130	006	004		.BYTE 6,4
3740	017132	001270			SAVR5
3741	017134	006	004		.BYTE 6,4
3742	017136	001266			SAVR4
3743	017140	006	004		.BYTE 6,4
3744	017142	001372			DQSEC
3745	017144	002	000		.BYTE 2,0
3746	017146	001262			SAVR2
3747	017150	000003			DT4: 3
3748	017152	006	004		.BYTE 6,4
3749	017154	001270			SAVR5
3750	017156	006	004		.BYTE 6,4
3751	017160	001266			SAVR4
3752	017162	006	004		.BYTE 6,4
3753	017164	001264			SAVR3
3754	017166	000000			RBUFF: 0
3755	017170	000000			TBUFF: 0
3756	017172	000000			ZDATA: 0
3757		000001			.END











LSTERR	001234	1069#	1216*	3078*	3384	3386*	3472*											
MCRLF	015040	3199	3215	3307	3413	3507	3520#											
MCSRX	015261	3084	3547#															
MDATA	015556	3335	3346	3585#														
MEMCLR=	104413	1132#	1382	1416	2459	2541	2641	2720	2722	2741	2821	2896	2963	3002				
		3040	3474															
MEPASS	015100	3082	3526#															
MERRPC	015405	3409	3566#															
MERRX	015306	3096	3553#															
MERR2	015125	1029	1332	3530#														
MERR3	015174	1264	3537#															
MISC. =	000012	643#																
MLOCK	015232	1288	3543#															
MNEW	015333	1257	3558#															
MPASSX	015275	3092	3551#															
MPFAIL	015042	3468	3521#															
MM	015034	3212	3519#															
MR	015122	1306	3529#															
MSTCLR=	104412	1130#	1383	1418	1448	1471	1494	1517	1540	1568	1591	1614	1637	1660				
		1683	1706	1729	1752	1775	1798	1821	1844	1873	1897	1921	1945	1971				
		1997	2023	2049	2075	2101	2127	2153	2179	2206	2235	2263	2296	2326				
		2356	2386	2424	2460	2542	2622	2721	2822	2897	2964	2982	3003	3019				
		3041	3046	3473														
MTITLE	001000	1038#	1222															
MTSTN	015317	3405	3555#															
MTSTPC	015220	1297	3541#															
MVECX	015267	3088	3549#															
NEXT	001216	1062#	1312*	1380*	1415*	1447*	1470*	1493*	1516*	1539*	1567*	1590*	1613*	1636*				
		1659#	1682*	1705*	1728*	1751*	1774*	1797*	1820*	1843*	1872*	1896*	1920*	1944*				
		1970#	1996*	2022*	2048*	2074*	2100*	2126*	2152*	2178*	2205*	2234*	2262*	2295*				
		2325#	2355*	2385*	2423*	2458*	2540*	2621*	2719*	2819*	2894*	2961*	3000*	3037*				
		3145	3441															
NON. EX=	177320	532#	2829	2861	2904	2935												
OOOBIT=	001000	626#	1000															
OUT	014774	3488	3490	3492	3496	3508#												
PARAM =	104405	1120#	1298	3502														
PARAM1	013506	3232#	3253															
PARERR	013562	3235	3237	3239	3248#	3258	3260	3262										
PARTI	013644	3251	3271#															
PASCNT	001230	1067#	1211*	3080*	3099	3122												
PFTAB	014652	3470	3476#															
POLY. =	000017	648#																
POPPO =	012600	595#	3434															
POP1SP=	005726	593#																
POP2SP=	022626	597#																
PS =	177776	587#	940*	1206*	1281*	1381*	1417*	1453*	1476*	1499*	1522*	1545*	1573*	1596*				
		1619#	1642*	1665*	1688*	1711*	1734*	1757*	1780*	1803*	1826*	1849*	1879*	1903*				
		1927#	1951*	1977*	2003*	2029*	2055*	2081*	2107*	2133*	2159*	2185*	2210*	2214*				
		2239#	2243*	2267*	2271*	2301*	2331*	2361*	2391*	2430*	2461*	2475*	2479*	2543*				
		2555#	2559*	2639*	2654*	2658*	2739*	2752*	2756*	2820*	2835*	2839*	2895*	2908*				
		2912#	2962*	3001*	3039*													
		594#	3431															
PUSHRO=	010046	592#																
PUSH1S=	005746	596#																
PUSH2S=	024646																	
QZX	010702	2699	2701#															
RBUFF	017166	2469	2501	2517	2518	2625	2648	2680	2696	2697	2968	3754#						













D07

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DZDQCD.P11 16-DEC-76 13:26 CROSS REFERENCE TABLE -- USER SYMBOLS

.PARAM	013446	1121	3223#		
.PFAIL	014564	912	1208	3454#	3462
.RESOS	013722	1125	3296#		
.SAVOS	013662	1123	3282#		
.SCOPE	013036	1111	3129#		
.SCOPI	013150	1113	3153#		
.START	001512	963	1206#	1218	
.TRPSR	014202	916	3365#		
.TRPTA	001314	1109#	3370		
.TYPE	013170	1115	3161#		





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DZDQC MACY11 27(1006) 22-DEC-76 11:09 PAGE 85  
 DZDQCD.P11 16-DEC-76 13:26 CROSS REFERENCE TABLE -- MACRO NAMES

STRAPS	18	1101													
STRPDE	18	1110	1112	1114	1116	1118	1120	1122	1124	1126	1128	1130	1132	1134	1136
STRPSR	18	3360													
STSTN	18	1308	1376	1411	1444	1467	1490	1513	1536	1564	1587	1610	1633	1656	1679
	1702	1725	1748	1771	1794	1817	1840	1869	1893	1917	1941	1967	1993	2019	2045
	2071	2097	2123	2149	2175	2202	2231	2259	2292	2322	2352	2382	2420	2454	2536
	2618	2715	2815	2890	2957	2996	3032								
STYPE	18	3158													
SVARIA	18	1036													

. ABS. 017174 000

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

MULE:DZDQCD.BIN, MULE:DZDQCD.SEQ/SOL/CRF=DSKZ:UNIV.P11, DSKZ:DZDQCD.P11  
 RUN-TIME: 29 43 3 SECONDS  
 RUN-TIME RATIO: 243/77=3.1  
 CORE USED: 24K (47 PAGES)