

# DLV11

DIAGNOSTIC TEST  
MD-11-DVKAE-B

EP-DVKAE-B-DL-A  
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**digital**  
MADE IN U.S.

Screen	Content Description
1	Header information and initial data points.
2	Series of numerical values and status indicators.
3	Table with multiple columns of data.
4	Table with multiple columns of data.
5	Table with multiple columns of data.
6	Table with multiple columns of data.
7	Table with multiple columns of data.
8	Table with multiple columns of data.
9	Table with multiple columns of data.
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12	Table with multiple columns of data.
13	Table with multiple columns of data.
14	Table with multiple columns of data.
15	Table with multiple columns of data.

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IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DVKAEB-D
PRODUCT NAME:	DLV11 TEST
DATE:	OCTOBER 1976
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	R.D. FIORENTINO
REVISION B:	D.J. CASALETTO

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1. ABSTRACT

THIS IS A LOGIC TEST OF THE DLV11 SERIAL LINE UNIT FOR  
THE LSI-11 COMPUTER. THIS TEST WILL OPERATE ON  
THE DLV11 WITHOUT ANY SPECIAL TEST DEVICES BY DEFAULT.  
HOWEVER, A SPECIAL WRAP MODULE CAN BE USED AND TESTED  
BY OPTION.

THIS IS A MULTIPLE DEVICE TEST WHICH WILL OPERATE ON THE  
CONSOLE DLV11 ADDRESSED AT 177560, AND UP TO 8 ADDITIONAL

DLV11 SERIAL LINE UNIT LOGIC TEST

DLV11'S WITH SPECIFIED ADDRESSES.

DEFAULT ADDRESSES FOR MULTIPLE DEVICE TESTING ARE:

177560 CONSOLE  
176500 BASE ADDRESS FOR ADDITIONAL DLV11'S

FOR COMPLETE INSTRUCTIONS ON MULTIPLE DEVICE TESTING SEE  
SECTION 5.5

2. REQUIREMENTS

2.1 EQUIPMENT

LSI-11 COMPUTER  
DLV11 SERIAL LINE UNIT  
TERMINAL FOR DLV11  
TEST MODULE (BY OPTION)

2.2 STORAGE REQUIREMENTS

4K MEMORY

3. LOADING PROCEDURE

3.1 METHOD

ABSOLUTE LOADER

4. STARTING PROCEDURE

200 - NORMAL ENTRY

TO LOAD AND EXECUTE

1. LOAD PROGRAM WITH THE ABSOLUTE LOADER.
2. IF ANY PROGRAM OPTIONS ARE REQUIRED, SET THE AP-  
PROPRIATE BIT IN THE SOFTWARE SWITCH REGISTER AT  
LOCATION 122. (REF. SECTION 5.1)
3. START PROGRAM AT 200.
4. PROGRAM WILL PRINT "END OF PASS" FOLLOWING EACH PASS.  
TO LOAD AND EXECUTE

STARTING ADDRESS:  
200 - NORMAL ENTRY

4.1 CONTROL SWITCH SETTING

THIS PROGRAM CONTAINS A SOFTWARE SWITCH REGISTER FOR  
OPTION SELECTION (LOC 422). FOR IT TO OPERATE THE OPERATOR  
MUST SELECT THE APPROPRIATE OPTION BY SETTING OR  
RESETTING THE RESPECTIVE BIT IN THE WORD.

TO DO THIS , THE LSI-11 MUST BE IN ODT MODE.

LSI-11 SERIAL LINE UNIT  
TERMINAL FOR DLV11  
TEST MODULE (BY OPTION)

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4.2 EXECUTION TIME

AT 110 BAUD, EXECUTION TIME FOR A SINGLE DEVICE IS APPROXIMATELY 30 SECONDS. FOR HIGHER BAUD RATES, EXECUTION TIME MUST BE REDUCED BY AN APPROPRIATE FACTOR.

5. GENERAL OPERATING PROCEDURE.

1. THE PROGRAM WILL CYCLE CONTINUOUSLY UNLESS HALTED BY THE OPERATOR, OR SOME ERROR CONDITION.
2. TO HALT THE PROGRAM, DEPRESS THE BREAK KEY. ODT WILL DISPLAY THE PC AT WHICH IT WAS HALTED.
3. IF NEW OPTIONS ARE TO BE SELECTED IN THE SMR, THEY MUST BE SET AT THIS TIME.
4. CONTINUE THE PROGRAM VIA A "P" OR A "G" COMMAND.

5.1 SOFTWARE SWITCH SETTINGS

BIT15 - CONTINUE ON ERROR	(100000)
BIT14 - LOOP ON CURRENT ERROR	(040000)
BIT13 - NOT USED	(020000)
BIT12 - NOT USED	(010000)
BIT11 - NOT USED	(004000)
BIT10 - LOOP ON CURRENT TEST	(002000)
BIT9 - RUN WRAP TEST	(001000)
BIT8 - SET DEVICE MAP MANUALLY	(000400)
BIT7 - NOT USED	(000200)
BIT6 - NOT USED	(000100)
BIT5 - NOT USED	(000040)
BIT4 - NOT USED	(000020)
BIT3 - NOT USED	(000010)
BIT2 - NOT USED	(000004)
BIT1 - NOT USED	(000002)
BIT0 - NOT USED	(000001)

5.2 SLU CONFIGURATION REQUIREMENTS

FOR BAUD RATE	#STOP BITS	#BITS
-----	-----	-----
110	2	8
ALL OTHERS	1	8

NO OTHER CONFIGURATION IS TESTED BY THIS PROGRAM  
 EIA IS TESTED WITH THE WRAP MODULE OPTION TEST.

5.3 OPERATION UNDER APT

THIS PROGRAM WILL OPERATE UNDER APT WITHOUT MODIFICATION TO THE SMR. HOWEVER, IN ORDER TO TEST THE FULL CAPABILITY OF THE DLV11, A TEST WITH THE TEST MODULE IS NECESSARY.  
 TO DO THIS, APT MUST SET BIT9 IN THE SWITCH REGISTER PRIOR TO EXECUTION.

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IMPORTANT ::::: THE TEST TIMES, PASS TIME CONSTANTS WITHIN  
THIS PROGRAM REFLECT OPERATION AT 9600 BAUD.  
A SLOWER BAUD RATE WILL CAUSE APT TO ABORT TESTING

5.4 TESTING A DLV11 AT A UNIQUE ADDRESS

1. TO SPECIFY A CONSOLE ADDRESS OTHER THAN 177560 OR VECTOR 60, THE OPERATOR MUST SUPPLY THE PROGRAM WITH THE CORRECT ADDRESSES BY INSERTING THEM AT THE TAG LABELED "RCSR". THE ADDRESSES MUST BE IN THE FOLLOWING ORDER:

RCSR: ADDRESS OF RECEIVER CSR  
 RBUF: ADDRESS OF RECEIVER BUFFER  
 TCSR: ADDRESS OF TRANSMITTER CSR  
 TBUF: ADDRESS OF TRANSMITTER BUFFER  
 RVECT: ADDRESS OF RECEIVER VECTOR  
 RPSW: ADDRESS OF ASSOCIATED PSW  
 TVECT: ADDRESS OF TRANSMITTER VECTOR  
 TPSW: ADDRESS OF ASSOCIATED PSW

2. TO TEST A SINGLE DLV11 AT A UNIQUE ADDRESS, INSERT THE ADDRESS OF THE RECEIVER CSR IN LOCATION SBASE, AND THE ADDRESS OF THE VECTOR IN LOCATION SVECT1, IN THE ETABLE. THE PROGRAM WILL GENERATE THE ADDITIONAL CSR, BUFFER, AND VECTOR ADDRESSES NEEDED FOR TESTING.

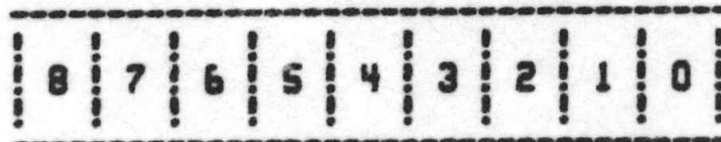
5.5 TESTING MULTIPLE DLV11 MODULES

ADDITIONAL DLV11'S MUST BE ADDRESSED WITHIN A RANGE OF 8 SEQUENTIAL ADDRESSES. A BASE ADDRESS MAY BE SPECIFIED BY THE OPERATOR OR A DEFAULT ADDRESS OF 176500 AND DEFAULT VECTOR OF 300 ARE USED. THE PROGRAM GENERATES A TABLE OF 8 ADDRESSES WITH EACH CSR GIVEN IN INCREMENTS OF 10. THE PROGRAM WILL THEN SIZE FOR DEVICES PRESENT.

5.6 THE DEVICE MAP

WHEN THE PROGRAM SIZES, A DEVICE MAP IS ESTABLISHED TO REPRESENT THOSE DEVICES PRESENT AND THEIR CORRESPONDING RECEIVER CSR ADDRESSES. THE DEVICE MAP CAN ALSO BE SET BY THE OPERATOR BY SELECTING THE APPROPRIATE BIT IN THE SWITCH REGISTER (SEE SECTION 5.1) AND PROCEEDING AS INDICATED BELOW.

THE DEVICE MAP IS A 16 BIT WORD WITH BITS 0-8 ARRANGED AS FOLLOWS:



DEVICE #0 = CONSOLE      DEFAULT ADDRESS = 177560; VECTOR = 60  
 DEVICES #1-#8 = ADDITIONAL DLV11'S  
 DEVICE #1 = BASE ADDRESS (SBASE); BASE VECTOR (SVECT1)  
 DEVICE #2 = BASE ADDRESS + 10; BASE VECTOR + 10



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\$TESTN	CURRENT TEST NUMBER
\$PASS	PASS COUNT OF THE PROGRAM WHEN ERROR WAS DETECTED OR PROGRAM HALTED
\$SMREG	SOFTWARE SWITCH REGISTER
RCSR	ADDRESS OF RECEIVER CSR UNDER TEST
RBUF	ADDRESS OF RECEIVER BUFFER UNDER TEST
TCSR	ADDRESS OF TRANSMITTER CSR UNDER TEST
TBUF	ADDRESS OF TRANSMITTER BUFFER UNDER TEST
RVECT	RECEIVER VECTOR ADDRESS BEING USED
TVECT	TRANSMITTER VECTOR ADDRESS BEING USED

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REVISION

- 1. IN TST12, FILLED SECOND BUFFER & CHECKED FOR "DONE" CLEAR BEFORE FLAGGING AN ERROR
- 2. REMOVED TEST THAT CHECKED "RESET" SETS "DONE" ON TRANSMITTER. (RESET DOES NOT SET DONE)
- 3. ADDED MULTIPLE SLU TEST CAPABILITY
- 4. CHANGED PROGRAM TO SKIP TST17 UNDER APT WHEN TESTING THE CONSOLE AFTER THE FIRST PASS

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314
315
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317
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319          000000
320 000000 000002
321 000002 000000
322 000004 000006
323 000006 000000
324 000010 000012
325 000012 000000
326 000014 000016
327 000016 000000
328 000020 000022
329 000022 000000
330          000030
331 000030 000032
332 000032 000000
333 000034 000036
334 000036 000000
335 000040 000042
336 000042 000000
337          000046
338 000046 000050
339 000050 000000
340 000054 000000
341 000054 000054
342 000054 000060
343 000054 000000
344 000054 000064
345 000054 000000
346 000054 000070
347 000054 000000
348 000070 000074
349 000072 000074
350 000074 000000

          000100
000100 000102
000102 000002

000200 012737 005426 000024
000206 012737 000340 000026
000214 005067 000166
000220 005067 000156
000224 005067 000154
000230 005067 000154
000234 005067 000152
000240 004767 005062
000244 005500
000246 000167 000726
          000400

          .ENABL ABS
          .NLIST MC,CND,MD
          .LIST ME
          =0
          +2                ;UNASSIGNED TRAP
          0
          +2                ;TIME-OUT, BUS ERROR
          0
          +2                ;RESERVED INSTRUCTION
          0
          +2                ;TRACE TRAP
          0
          +2
          =30
          +2                ;EMT TRAP
          0
          +2
          0
          +2
          =46
          +2
          0
          +2
          0
          +2
          0
          +2
          0
          +2
          0
          +2
          0
          .MCALL .STYPE, .STRAP, .SAPTCLS, .SAPTHDR, .SAPTYPE, STARS
          =100
          102
          RTI
          =200
          MOV @PWRFL,2824        ;SET POWER FAIL VECTOR
          MOV @340,2826         ;SET POWER FAIL PSM
          CLR SPASS              ;CLEAR PASS COUNT
          CLR SFATAL             ;STARTING POINT AFTER POWER FAIL
          CLR $TESTN            ;CLEAR TEST NUMBER
          CLR $DEVCT           ;CLEAR DEVICE COUNT
          CLR $UNIT             ;SET UNIT NUMBER TO ZERO
          JSR PC,MSGPRT         ;PRINT PROGRAM NAME
          .WORD M1
          JMP START             ;START DIAGNOSTIC
          =400
          .SBTTL APT MAILBOX-ETABLE

; *****
.EVEN

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370	000400		SMAIL:		:: APT MAILBOX
371	000400	000000	SMSGTY: .WORD	AMSGTY	:: MESSAGE TYPE CODE
372	000402	000000	SFATAL: .WORD	AFATAL	:: FATAL ERROR NUMBER
373	000404	000000	STESTN: .WORD	ATESTN	:: TEST NUMBER
374	000406	000000	SPASS: .WORD	APASS	:: PASS COUNT
375	000410	000000	SDEVCT: .WORD	ADEVCT	:: DEVICE COUNT
376	000412	000000	SUNIT: .WORD	AUNIT	:: I/O UNIT NUMBER
377	000414	000000	SMSGAD: .WORD	AMSGAD	:: MESSAGE ADDRESS
378	000416	000000	SMSGLG: .WORD	AMSGLG	:: MESSAGE LENGTH
379	000420		SETABLE:		:: APT ENVIRONMENT TABLE
380	000420	000	SENV: .BYTE	RENV	:: ENVIRONMENT BYTE
381	000421	000	SENVH: .BYTE	RENVH	:: ENVIRONMENT MODE BITS
382	000422	000000	SSMREG: .WORD	ASMREG	:: APT SWITCH REGISTER
383	000424	000000	SUSMR: .WORD	AUSMR	:: USER SWITCHES
384	000426	000000	SCPUOP: .WORD	ACPUOP	:: CPU TYPE, OPTIONS
385			::		BITS 15-11=CPU TYPE
386			::		11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
387			::		11/70=06, PD0=07, Q=10
388			::		BIT 10=REAL TIME CLOCK
389			::		BIT 9=FLOATING POINT PROCESSOR
390			::		BIT 8=MEMORY MANAGEMENT
391	000430	000	SMAMS1: .BYTE	AMAMS1	:: HIGH ADDRESS, M.S. BYTE
392	000431	000	SMTYP1: .BYTE	AMTYP1	:: MEM. TYPE, BLK#1
393			::		MEM. TYPE BYTE -- (HIGH BYTE)
394			::		900 NSEC CORE=001
395			::		300 NSEC BIPOLAR=002
396			::		500 NSEC MOS=003
397	000432	000000	SMADR1: .WORD	AMADR1	:: HIGH ADDRESS, BLK#1
398			::		MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
399	000434	000	SMAMS2: .BYTE	AMAMS2	:: HIGH ADDRESS, M.S. BYTE
400	000435	000	SMTYP2: .BYTE	AMTYP2	:: MEM. TYPE, BLK#2
401	000436	000000	SMADR2: .WORD	AMADR2	:: MEM. LAST ADDRESS, BLK#2
402	000440	000	SMAMS3: .BYTE	AMAMS3	:: HIGH ADDRESS, M.S. BYTE
403	000441	000	SMTYP3: .BYTE	AMTYP3	:: MEM. TYPE, BLK#3
404	000442	000000	SMADR3: .WORD	AMADR3	:: MEM. LAST ADDRESS, BLK#3
405	000444	000	SMAMS4: .BYTE	AMAMS4	:: HIGH ADDRESS, M.S. BYTE
406	000445	000	SMTYP4: .BYTE	AMTYP4	:: MEM. TYPE, BLK#4
407	000446	000000	SMADR4: .WORD	AMADR4	:: MEM. LAST ADDRESS, BLK#4
408	000450	000300	SVECT1: .WORD	AVECT1	:: INTERRUPT VECTOR#1, BUS PRIORITY#1
409	000452	000000	SVECT2: .WORD	AVECT2	:: INTERRUPT VECTOR#2, BUS PRIORITY#2
410	000454	176500	SBASE: .WORD	ABASE	:: BASE ADDRESS OF EQUIPMENT UNDER TEST
411	000456	000000	SDEVH: .WORD	ADEVH	:: DEVICE MAP
412	000460		SETEND:		
413			.MEXIT		

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415  
416  
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419 000460  
420 000024  
421 000024  
422 000044  
423 000044  
424 000460  
425 000460  
426  
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428  
429  
430  
431 000460  
432 000000  
433 000400  
434 000010  
435 000010  
436 000470  
437 000000  
438 000472  
439  
440  
441 000001  
442 000001  
443 000300  
444 176500  
445 001000  
446 177560  
447 100000  
448 040000  
449 020000  
450 010000  
451 004000  
452 002000  
453 001000  
454 000400  
455 000200  
456 000100  
457 000040  
458 000020  
459 000010  
460 000004  
000002  
000001

.SBTTL APT PARAMETER BLOCK

\*\*\*\*\*  
:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT  
\*\*\*\*\*  
: .SX= : SAVE CURRENT LOCATION  
: =24 : SET POWER FAIL TO POINT TO START OF PROGRAM  
: 200 : FOR APT START UP  
: =44 : POINT TO APT INDIRECT ADDRESS PNTR.  
: \$APTHDR : POINT TO APT HEADER BLOCK  
: =.SX : RESET LOCATION COUNTER  
\*\*\*\*\*  
:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC  
:INTERFACE SPEC.

\$APTHD: :  
\$BITS: .WORD 0 ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.  
\$MADR: .WORD \$MAIL ;; ADDRESS OF APT MAILBOX (BITS 0-15)  
\$STMT: .WORD 10 ;; RUN TIM OF LONGEST TEST  
\$PASTM: .WORD 10 ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)  
\$UNITH: .WORD 0 ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT  
: .WORD SETEND-\$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)

...  
EQUATES

X=1  
N=1  
AVECT1=300  
ABASE=176500  
STKPTR=1000  
CSR=177560  
BIT15=100000  
BIT14=40000  
BIT13=20000  
BIT12=10000  
BIT11=4000  
BIT10=2000  
BIT9=1000  
BIT8=400  
BIT7=200  
BIT6=100  
BIT5=40  
BIT4=20  
BIT3=10  
BIT2=4  
BIT1=2  
BIT0=1

;; DEFAULT BASE VECTOR FOR ADDITIONAL UNITS  
;; DEFAULT BASE DEVICE ADDRESS FOR ADDITIONAL UNITS  
;; DEFAULT CONSOLE DEVICE ADDRESS

461 000474 000000  
462 000476 000000  
463 000500 000000  
464 000502 000000  
465 000504 000000  
466  
467  
468

TMP0: .WORD 0  
TMP1: .WORD 0  
TMP2: .WORD 0  
TMP3: .WORD 0  
CTSTFL: .WORD 0

:LOCATION TO STORE TABLE OFFSETS  
:LOCATION TO KEEP NO. OF TEST DEVICES  
:LOCATION TO KEEP DEVICE MAP TEST MASK  
:FLAG TO INDICATE CURRENT TEST DEVICE IS CONSOLE

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469
470 ; REGISTER AND VECTOR ADDRESSES FOR THE DLV11 UNDER TEST
471 000506 177560 RCSR: CSR
472 000510 177562 RBUF: CSR+2
473 000512 177564 TCSR: CSR+4
474 000514 177566 TBUF: CSR+6
475 000516 000060 RVECT: 60
476 000520 000062 RPSM: 62
477 000522 000064 TVECT: 64
478 000524 000066 TPSM: 66
479
480 ; INITIAL REGISTER AND VECTOR ADDRESSES FOR THE CONSOLE DLV11
481
482 000526 177560 DRCSR: 177560 ; ADDRESS OF RECEIVER STATUS REGISTER
483 000530 177562 DRBUF: 177562 ; ADDRESS OF RECEIVER DATA BUFFER REGISTER
484 000532 177564 DTCSR: 177564 ; ADDRESS OF TRANSMITTER STATUS REGISTER
485 000534 177566 DTBUF: 177566 ; ADDRESS OF TRANSMITTER DATA BUFFER REGISTER
486 000536 000060 DRVECT: 60
487 000540 000062 DRPSM: 62
488 000542 000064 DTVECT: 64
489 000544 000066 DTPSM: 66
490
491
492 000600 000020 ADRTBL: .BLKW 20
493 000640 000010 VCTTBL: .BLKW 10

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494 001200 001200          START:  MOV    =1200          ; INITIALIZE STACK POINTER
495 001200 012706 001000          ;ROUTINE TO HANDLE THE TESTING OF MULTIPLE DLV11 MODULES
496
497
498
499 001204 005767 177176          TST     SPASS          ;CHECK IF ON FIRST PASS
500 001210 001161          BNE     SIZED          ;IF NOT ON FIRST PASS
501 001212 132767 000001 177200  BITB    #BIT0,SENV     ;CHECK IF ON APT
502 001220 001404          BEQ     MANL           ;IF NOT ON APT
503 001222 132767 000200 177171  BITB    #BIT7,SENV     ;DID APT SIZE?
504 001230 001067          BNE     APTSIZ        ;IF APT SIZED
505 001232 032767 000400 177162  MANL:   BIT     #BIT8,SSWREG ;MANUAL SETTING OF SDEVM?
506 001240 001402          BEQ     SETTBL        ;NO
507 001242 000000          HALT
508 001244 000461          BR     APTSIZ         ;INPUT DEVICE MAP
509 001246 004767 000104          SETTBL: JSR    PC,DEVADR ;CONT WHEN DEVICE MAP IS SET
510 001252 005067 177222          CLR     TMP2          ;GENERATE DEVICE ADDRESS TABLE
511 001254 005067 177174          CLR     SDEVM         ;CLEAR TEMP LOCATION TO COUNT DEVICES
512 001256 012737 001316 000004  MOV     #25,2#4        ;CLEAR DEVICE MAP
513 001270 016700 177160          MOV     SBASE,RO      ;SET TIMEOUT POINTER
514 001274 062700 000100          ADD     #100,RO        ;LOAD BASE ADDRESS
515 001300 162700 000010          1S:    SUB     #10,RO   ;POINT RO TO UNIT#8 (UNIT#0 = CONSOLE)
516 001304 005710          TST     (RO)          ;POINT RO TO THE NEXT UNIT ADDRESS
517 001306 005267 177144          INC     SDEVM         ;CHECK FOR DEVICE EXISTANCE
518 001312 005267 177162          INC     TMP2          ;NO TIMEOUT - INDICATE DEVICE IN DEVICE MAP
519 001316 006382 177134          2S:    ASL     SDEVM   ;INCREMENT DEVICE COUNT
520 001322 026700 177126          CMP     SBASE,RO      ;ADJUST DEVICE MAP FOR NEXT UNIT CHECK
521 001326 002764          BLT     1S            ;FINISHED SIZING?
522 001330 016700 177172          MOV     DRCSR,RO      ;BR IF NOT
523 001334 012737 001354 000004  MOV     #35,2#4        ;LOAD CONSOLE DEVICE ADDRESS
524 001342 005710          TST     (RO)          ;SET TIMEOUT VECTOR
525 001344 005267 177106          INC     SDEVM         ;TEST FOR CONSOLE EXISTANCE
526 001350 005267 177124          INC     TMP2          ;NO TIMEOUT - INDICATE CONSOLE IN DEVICE MAP
527 001354 000432          3S:    BR     VCTADR   ;INCREMENT DEVICE COUNT
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549
;ROUTINE TO GENERATE DEVICE ADDRESS TABLE
001356 012702 000600          DEVADR: MOV     #AORTBL,R2 ;POINT R2 TO TOP OF THE ADDRESS TABLE
001362 016700 177066          MOV     SBASE,RO      ;LOAD BASE ADDRESS IN RO
001366 010001          MOV     RO,R1         ;CALCULATE DEVICE ADDRESS LIMIT
001370 062701 000100          ADD     #100,R1
001374 010022          1S:    MOV     RO,(R2)+ ;MOVE DEVICE ADDRESS TO TABLE
001376 062700 000010          ADD     #10,RO        ;CALCULATE NEXT DEVICE ADDRESS
001402 020001          CMP     RO,R1         ;FINISHED?
001404 002773          BLT     1S            ;BR IF NOT
001406 000207          RTS     PC            ;RETURN
001410 005067 177064          APTSIZ: CLR     TMP2   ;CLEAR TEMP LOCATION TO KEEP DEVICE COUNT
001414 016702 177036          MOV     SDEVM,R2     ;GET DEVICE MAP
001420 005702          TSTDVM: TST     R2    ;TEST MSB OF DEVICE MAP
001422 100002          BPL     1S           ;BR, IF CLEAR
001424 005267 177050          INC     TMP2         ;IF SET, INCREMENT DEVICE COUNT
001430 006302          1S:    ASL     R2     ;SHIFT NEXT BIT INTO MSB POSITION
001432 001401          BEQ     DVADT        ;FINISHED (NO BITS LEFT SET IN MAP)?
001434 000771          BR     TSTDVM       ;BR, IF NOT

```

550	001436	004767	177714		DVADT: JSR	PC,DEVADR	:GENERATE DEVICE ADDRESS TABLE
551					VCTADR: MOV	#VCTTBL,R2	:GET LOCATION OF VECTOR TABLE
552	001442	012702	000640			CLR R1	:CLEAR DATA WORD
553	001446	005001				MOV SB	:COPY BASE VECTOR
554	001450	116700	176774			BIC #177400,R0	:CLEAR BYTE SIGN EXTENSION
555	001454	042700	177400		IS: MOV	R0,(R2)+	:PUT VECTOR ADDRESS IN THE TABLE
556	001460	010022				INC R1	:KEEP COUNT OF THE NO. OF ADDRESSES STORED
557	001462	005201				ADD #10,R0	:FORM NEXT SEQUENTIAL ADDRESS
558	001464	062700	000010			CMP #10,R1	:FINISHED?
559	001470	022701	000010			BGE IS	:IF NO
560	001474	002371					
561							
562	001476	016700	176776			MOV TMP2,R0	:COPY DEVICE COUNT INTO R0
563	001502	005001				CLR R1	:CLEAR AUXILIARY REGISTER
564	001504	000300				MOV SB	:PUT DEVICE COUNT IN UPPER BYTE OF R0
565	001506	006300				ASL R0	:MOVE MSB OF COUNT INTO
566	001510	006300				ASL R0	:MSB OF R0
567							
568	001512	006300			SHIFT: ASL	R0	:PUT MSB OF COUNT INTO CARRY
569	001514	106101				ROLB R1	:MOVE MSB OF COUNT INTO R1
570	001516	006300				ASL R0	:MOVE NEXT BIT OF COUNT
571	001520	106101				ROLB R1	:INTO R1
572	001522	006300				ASL R0	:MOVE LAST BIT OF DIGIT
573	001524	106101				ROLB R1	:INTO R1
574	001526	062701	000060			ADD #60,R1	:CONVERT TO ASCII
575	001528	000301				MOV SB	:MOVE DIGIT TO UPPER BYTE
576	001532	032701	000020			BIT #BIT4,R1	:HAVE BOTH DIGITS BEEN MAVED TOR1?
577	001540	001764				BEG SHIFT	:BR, IF NOT
578	001542	010167	003774			MOV R1,R2	:MOVE DEVICE COUNT TO OUTPUT MESSAGE
579	001546	004767	003554			JSR PC,MSGPRT	:PRINT MESSAGE DEFINING THE
580	001552	005542				MOV #2,R2	:NO. OF DEVICES SIZED
581	001554	005067	176716		SIZED: CLR	TMP1	:CLEAR TEMP LOCATION FOR TABLE OFFSETS
582	001560	012767	000002	176714		MOV #BIT1,TMP3	:SET UP BIT MASK FOR DEVICE MAP
583	001566	032767	000001	176662	TSTTY: BIT	#BIT0,SDEVN	:IS CONSOLE DEVICE TO BE TESTED?
584	001574	001001				BNE TCONSL	:IF YES
585	001576	000414				BR SETUP	:GO TEST ADDITIONAL DEVICES
586	001600	012700	000506		TCONSL: MOV	#RCSR,R0	:SET UP REGISTER ADDRESSES FOR CONSOLE
587	001604	012701	000526			MOV #RCSR,R1	:POINT R1 TO CONSOLE ADDRESS TABLE
588	001610	005267	176670			INC CTSTFL	:INDICATE THAT CONSOLE IS UNDER TEST
589	001614	012120			IS: MOV	(R1)+,(R0)+	:FORM CONSOLE ADDRESSES
590	001616	022700	000524			CMP #TPSW,R0	:FINISHED?
591	001622	002374				BGE IS	:IF NO
592	001624	000167	000116			JMP TST1	:GO TEST CONSOLE DEVICE
593							
594	001630	036767	176646	176620	SETUP: BIT	TMP3,SDEVN	:TEST DEVICE BIT IN DEVICE MAP
595	001636	001010				BNE SETADR	:BR, IF SET AND TEST DEVICE
596	001640	006367	176636			ASL TMP3	:IF CLEAR, UPDATE DEVICE MAP TEST MASK
597	001644	062767	000002	176624		ADD #2,TMP1	:INCREMENT TABLE OFFSET
598	001652	005267	176534			INC \$UNIT	:INCREMENT UNIT NUMBER
599	001656	000764				BR SETUP	:BR, TO TEST NEXT DEVICE MAP BIT
600	001660	005267	176526		SETADR: INC	\$UNIT	:INCREMENT UNIT NUMBER BEFORE TESTING DEVICE
601	001664	006367	176612			ASL TMP3	:UPDATE DEVICE MAP TEST MASK
602	001670	016702	176602			MOV TMP1,R2	:MOVE TABLE OFFSET TO R2
603	001674	062767	000002	176574		ADD #2,TMP1	:UPDATE TABLE OFFSET FOR NEXT DEVICE
604							
605							

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606 001702 016200 000600      MOV      ADRTAB(R2),R0      ;REGISTER ADDRESS OF NEXT DEVICE
607 001706 012701 000506      MOV      @RCSR,R1         ;LOCATION OF REGISTER ADDR.
608 001712 010021      ADR:    MOV      R0,(R1)+    ;CREATE ACTIVE DEVICE ADDRESS TABLE
609 001714 005720      TST     (R0)+
610 001716 030027 000006      BIT     R0,#000006       ;FINISHED?
611 001722 001373      BNE     ADR               ;BR, IF NOT
612
613 001724 016200 000640      MOV      VCTTAB(R2),R0    ;VECTOR ADDRESS OF NEXT DEVICE
614 001730 010021      VECT:  MOV      R0,(R1)+    ;CREATE ACTIVE VECTOR ADDRESS TABLE
615 001732 005720      TST     (R0)+
616 001734 030027 000006      BIT     R0,#000006       ;FINISHED?
617 001740 001373      BNE     VECT             ;BR, IF NOT
618 001742 000167 000000      JMP     TST1            ;GO TEST THIS DEVICE
619
620      ;TEST ABILITY TO REFERENCE RECEIVER CSR WITHOUT TRAPPING
621      TST1:
622 001746 012767 000001 176430      MOV      #1,STESTN        ; MOVE TEST NUMBER TO MAILBOX
623 001754 012737 001770 000004      LP1:    MOV      #25,2#4 ;SET TIME OUT VECTOR
624 001762 005777 176520      TST     @RCSR            ;REFERENCE THE CSR
625 001766 000416      BR      IS              ;GO TO NEXT TEST IF NO TRAP
626
627 001770 032767 040000 176424      2S:    BIT     #BIT14,SSMREG   ; CHECK FOR LOOP ON ERROR
628 001776 001366      BNE     LP1             ; GO TO LOOP ERROR
629 002000 012767 000001 176374      MOV      #1,SFATAL
630 002006 012767 000001 176364      MOV      #1,MSGTY
631 002014 005767 176402      TST     SSMREG          ; MOVE ERROR NUM TO MAILBOX
632 002020 100401      BMI     IS              ; CHECK FOR HALT ON ERROR
633 002022 000000      HALT                    ; HALT IF SET
634 002024 000000      ;<CANNOT ACCESS RCSR>
635
636 002024 032767 002000 176370      1S:    BIT     #BIT10,SSMREG   ; CHECK FOR LOOP ON TEST
637 002032 001345      BNE     TST1           ; GO TO LOOP ON TEST
638 002034 012737 000006 000004      MOV      #6,2#4 ;RESTORE TIMEOUT VECTOR
639
640      ;TEST ABILITY TO REFERENCE RECEIVER BUFFER WITHOUT TRAPPING
641      TST2:
642 002042 012767 000002 176334      MOV      #2,STESTN        ; MOVE TEST NUMBER TO MAILBOX
643 002050 012737 002064 000004      LP2:    MOV      #25,2#4 ;SET TIME OUT VECTOR
644 002056 005777 176426      TST     @RBUF           ;REFERENCE THE BUFFER
645 002062 000416      BR      IS              ;GO TO NEXT TEST
646
647 002064 032767 040000 176330      2S:    BIT     #BIT14,SSMREG   ; CHECK FOR LOOP ON ERROR
648 002072 001366      BNE     LP2             ; GO TO LOOP ERROR
649 002074 012767 000002 176300      MOV      #2,SFATAL
650 002102 012767 000001 176270      MOV      #1,MSGTY
651 002110 005767 176306      TST     SSMREG          ; MOVE ERROR NUM TO MAILBOX
652 002114 100401      BMI     IS              ; CHECK FOR HALT ON ERROR
653 002116 000000      HALT                    ; HALT IF SET
654 002120 000000      ;<CANNOT ACCESS RBUF>
655
656 002120 032767 002000 176274      1S:    BIT     #BIT10,SSMREG   ; CHECK FOR LOOP ON TEST
657 002126 001345      BNE     TST2           ; GO TO LOOP ON TEST
658 002130 012737 000006 000004      MOV      #6,2#4 ;RESTORE TIMEOUT VECTOR
659
660      ;TEST ABILITY TO REFERENCE TRANSMITTER CSR WITHOUT TRAPPING
661      TST3:
662 002136 012767 000003 176240      MOV      #3,STESTN        ; MOVE TEST NUMBER TO MAILBOX

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663 002144 012737 002160 000004 LP3: MOV #25,204 ;SET UP TIME OUT VECTOR
664 002153 005777 176334 TST @TCSR ;REFERENCE THE T CSR
665 002156 000416 BR IS ;GO TO NEXT TEST IF NO TIME-OUT
666 002160 032767 040000 176234 25: BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
667 002166 001366 BNE LP3 ; GO TO LOOP ERROR
668 002170 012767 000003 176204 MOV #3,SFATAL
669 002176 012767 000001 176174 MOV #1,SMSTY ; MOVE ERROR NUM TO MAILBOX
670 002204 005767 176212 TST SSWREG ; CHECK FOR HALT ON ERROR
671 002210 100401 BMI IS ; HALT IF SET
672 002212 000000 HALT ; <CANNOT ACCESS TCSR>
673 002214 032767 002000 176200 15: BIT #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
674 002222 001345 BNE TST3 ; GO TO LOOP ON TEST
675 002224 012737 000006 000004 MOV #6,204 ;RESTORE TIMEOUT VECTOR
676
677
678 ;TEST ABILITY TO REFERENCE TRANSMITTER BUFFER WITHOUT TRAPPING
679
680 ;TST4:
681 002232 012767 000004 176144 MOV #4,STESTN ; MOVE TEST NUMBER TO MAILBOX
682 002240 032767 000001 176152 BIT #BIT0,SENV ; CHECK IF ON APT
683 002246 001406 BEQ LP4 ; DO THIS TEST IF NOT ON APT
684 002250 005767 176132 TST SPASS ; CHECK IF FIRST PASS
685 002254 001403 BEQ LP4 ; BR IF FIRST PASS
686 002258 005767 176222 TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST
687 002262 001034 BNE TST5 ; IF CONSOLE IS UNDER TEST
688 002264 012737 002300 000004 LP4: MOV #25,204 ;SET UP TIME-OUT VECTOR
689 002272 005777 176216 TST @TBUF ;REFERENCE THE T BUFFER
690 002276 000416 BR IS ;GO TO NEXT TEST IF NO TIME-OUT
691 002300 032767 040000 176114 25: BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
692 002306 001366 BNE LP4 ; GO TO LOOP ERROR
693 002310 012767 000004 176064 MOV #4,SFATAL
694 002316 012767 000001 176054 MOV #1,SMSTY ; MOVE ERROR NUM TO MAILBOX
695 002324 005767 176072 TST SSWREG ; CHECK FOR HALT ON ERROR
696 002330 100401 BMI IS ; HALT IF SET
697 002332 000000 HALT ; <CANNOT ACCESS TBUF>
698
699
700 002334 032767 002000 176060 15: BIT #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
701 002342 001333 BNE TST4 ; GO TO LOOP ON TEST
702 002344 012737 000006 000004 MOV #6,204 ;RESTORE TIMEOUT VECTOR
703 002352 000240 NOP
704
705 ;TEST THAT "BREAK" BIT (BIT0) IN TCSR CAN BE SET AND CLEARED AND
706 ;THAT RESET CAN CLEAR IT.
707
708 ;TST5:
709 002354 012767 000005 176022 MOV #5,STESTN ; MOVE TEST NUMBER TO MAILBOX
710 002362 032767 000001 176030 BIT #BIT0,SENV ; CHECK IF ON APT
711 002370 001406 BEQ LPSA ; DO THIS TEST IF NOT ON APT
712 002372 005767 176010 TST SPASS ; CHECK IF FIRST PASS
713 002376 001403 BEQ LPSA ; BR IF FIRST PASS
714 002400 005767 176100 TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST
715 002404 001136 BNE TST6 ; IF CONSOLE IS UNDER TEST
716 002406 005004 LPSA: CLR R4 ; SET UP 300 NS COUNT
717 002410 005204 LPSB: INC R4
    
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718	002412	001376				BNE	LPSB		
719	002414	000005				RESET			: CLEAR EVERYTHING
720	002416	032777	000001	176066	LPS:	BIT	#BIT0, @TCSR		: CHECK BIT 0 (BREAK)
721	002424	001416				BEQ	TSCON		: CONTINUE IF NOT SET
722	002426	032767	040000	175766		BIT	#BIT14, SSMREG		: CHECK FOR LOOP ON ERROR
723	002434	001367				BNE	LPS		: GO TO LOOP ERROR
724	002436	012767	000005	175736		MOV	#5, SFATAL		
725	002444	012767	000001	175726		MOV	#1, SMSGTY		: MOVE ERROR NUM TO MAILBOX
726	002452	005767	175744			TST	SSMREG		: CHECK FOR HALT ON ERROR
727	002456	100401				BMI	IS		: HALT IF SET
728	002460	000000				HALT			: <BIT 0 IN TCSR SHOULD BE 0 AFTER RESET>
729	002464	000000			IS:				
730	002472	052777	000001	176022	TSCON:	BIS	#BIT0, @TCSR		: SET BIT0 (BREAK)
731	002470	032777	000001	176014		BIT	#BIT0, @TCSR		: CHECK IF SET
732	002476	001016				BNE	TSCON1		: CONTINUE IF SET
733	002500	032767	040000	175714		BIT	#BIT14, SSMREG		: CHECK FOR LOOP ON ERROR
734	002506	001365				BNE	TSCON		: GO TO LOOP ERROR
735	002510	012767	000006	175664		MOV	#6, SFATAL		
736	002516	012767	000001	175654		MOV	#1, SMSGTY		: MOVE ERROR NUM TO MAILBOX
737	002522	005767	175672			TST	SSMREG		: CHECK FOR HALT ON ERROR
738	002526	100401				BMI	IS		: HALT IF SET
739	002530	000000				HALT			: <CANNOT SET BIT0 IN TCSR>
740	002534	000000			IS:				
741	002542	042777	000001	175750	TSCON1:	BIC	#BIT0, @TCSR		: CLEAR BIT0
742	002546	032777	000001	175742		BIT	#BIT0, @TCSR		: CHECK TO SEE IF CLEAR
743	002550	001416				BEQ	TSCON2		: CONTINUE IF CLEAR
744	002556	032767	040000	175642		BIT	#BIT14, SSMREG		: CHECK FOR LOOP ON ERROR
745	002560	001365				BNE	TSCON1		: GO TO LOOP ERROR
746	002566	012767	000007	175612		MOV	#7, SFATAL		
747	002570	012767	000001	175602		MOV	#1, SMSGTY		: MOVE ERROR NUM TO MAILBOX
748	002576	005767	175620			TST	SSMREG		: CHECK FOR HALT ON ERROR
749	002580	100401				BMI	IS		: HALT IF SET
750	002584	000000				HALT			: <CANNOT CLEAR BIT0 IN TCSR>
751	002590	000000			IS:				
752	002596	012704	010000		TSCON2:	MOV	#10000, R4		: ; SET UP DELAY
753	002602	005304			TSDC:	DEC	R4		: DELAY
754	002608	001376				BNE	TSDC		
755	002614	052777	000001	175666		BIS	#BIT0, @TCSR		: SET IT AGAIN
756	002620	000005				RESET			: CHECK RESET CLEAR AGAIN
757	002626	032777	000001	175656		BIT	#BIT0, @TCSR		: CHECK BIT 0
758	002634	001416				BEQ	IS		: CONTINUE IF RESET
759	002636	032767	040000	175556		BIT	#BIT14, SSMREG		: CHECK FOR LOOP ON ERROR
760	002644	001360				BNE	TSCON2		: GO TO LOOP ERROR
761	002646	012767	000010	175526		MOV	#10, SFATAL		
762	002654	012767	000001	175516		MOV	#1, SMSGTY		: MOVE ERROR NUM TO MAILBOX
763	002662	005767	175534			TST	SSMREG		: CHECK FOR HALT ON ERROR
764	002666	100401				BMI	IS		: HALT IF SET
765	002670	000000				HALT			: <RESET DID NOT CLEAR BIT0 IN TCSR>
766	002672	000000			IS:				
767	002672	032767	002000	175522		BIT	#BIT10, SSMREG		: CHECK FOR LOOP ON TEST
768	002700	001225				BNE	TST5		: GO TO LOOP ON TEST

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 DVKREB.P11 ERROR 10 RESET DID NOT CLEAR BIT0 IN TCSR

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769
770
771
772
773 002702
774 002702 012767 000006 175474
775 002710 032767 000001 175502
776 002716 001406
777 002720 005767 175462
778 002724 001403
779 002726 005767 175552
780 002732 001152
781 002734
782 002734 000005
783 002736 012777 003014 175556
784 002744 106427 000200
785 002750 032777 000100 175534
786 002756 001434
787 002760 032767 040000 175434
788 002766 001362
789 002770 012767 000011 175404
790 002776 012767 000001 175374
791 003004 005767 175412
792 003010 100401
793 003012 000000
794 003014
795 003014
796 003014 032767 040000 175400
797 003022 001344
798 003024 012767 000012 175350
799 003032 012767 000001 175340
800 003040 005767 175356
801 003044 100401
802 003046 000000
803 003050
804 003050 052777 000100 175434
805 003056 032777 000100 175426
806 003064 001016
807 003066 032767 040000 175326
808 003074 001365
809 003076 012767 000013 175276
810 003104 012767 000001 175266
811 003112 005767 175304
812 003116 100401
813 003120 000000
814 003122
815 003122 042777 000100 175362
816 003130 032777 000100 175354
817 003136 001416
818 003140 032767 040000 175254
819 003146 001365
820 003150 012767 000014 175224
821 003156 012767 000001 175214
822 003164 005767 175232
823 003170 100401
824 003172 000000

```

: TEST THAT TCSR BIT6 (TRANSMITTER INTERRUPT ENABLE) CAN BE  
 : SET AND RESET AND THAT RESET CLEARS IT.  
 : TST6:  
 : MOV #6,STESTN ; MOVE TEST NUMBER TO MAILBOX  
 : BIT #BIT0,SENV ; CHECK IF ON APT  
 : BEQ TST6A ; IF NOT ON APT  
 : TST \$PASS ; CHECK IF ON FIRST PASS  
 : BEQ TST6A ; BR, IF FIRST PASS  
 : TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST  
 : BNE TST7 ; IF CONSOLE IS UNDER TEST  
 : TST6A:  
 : LP6: RESET ; SEND THE INITIAL RESET TO CLEAR  
 : MOV #ERR12,\$TVECT ; SET UP VECTOR IN CASE OF INTERRUPT  
 : MTPS #200 ; TURN OFF INTERRUPTS  
 : BIT #BIT6,\$TCSR ; CHECK IF BIT 6 IS ON  
 : BEQ T6CON1 ; CONTINUE IF NOT SET  
 : BIT #BIT14,\$SSWREG ; CHECK FOR LOOP ON ERROR  
 : BNE LP6 ; GO TO LOOP ERROR  
 : MOV #11,\$FATAL  
 : MOV #1,\$MSGTY ; MOVE ERROR NUM TO MAILBOX  
 : TST \$SSWREG ; CHECK FOR HALT ON ERROR  
 : BMI IS ; HALT IF SET  
 : HALT ; <BIT6 IN TCSR NOT CLEAR AFTER RESET>  
 : IS:  
 : ERR12: BIT #BIT14,\$SSWREG ; CHECK FOR LOOP ON ERROR  
 : BNE LP6 ; GO TO LOOP ERROR  
 : MOV #12,\$FATAL  
 : MOV #1,\$MSGTY ; MOVE ERROR NUM TO MAILBOX  
 : TST \$SSWREG ; CHECK FOR HALT ON ERROR  
 : BMI IS ; HALT IF SET  
 : HALT ; <DEVICE SHOULD NOT HAVE INTERRUPTED WITH PRIORITY BIT SET>  
 : IS:  
 : T6CON1: BIS #BIT6,\$TCSR ; SET BIT6  
 : BIT #BIT6,\$TCSR ; CHECK IF SET  
 : BNE T6CON2 ; CONTINUE IF SET.  
 : BIT #BIT14,\$SSWREG ; CHECK FOR LOOP ON ERROR  
 : BNE T6CON1 ; GO TO LOOP ERROR  
 : MOV #13,\$FATAL  
 : MOV #1,\$MSGTY ; MOVE ERROR NUM TO MAILBOX  
 : TST \$SSWREG ; CHECK FOR HALT ON ERROR  
 : BMI IS ; HALT IF SET  
 : HALT ; <CANNOT SET BIT6 IN TCSR>  
 : IS:  
 : T6CON2: BIC #BIT6,\$TCSR ; CLEAR BIT6  
 : BIT #BIT6,\$TCSR ; CHECK IF CLEAR  
 : BEQ T6CON3 ; CONTINUE IF CLEAR  
 : BIT #BIT14,\$SSWREG ; CHECK FOR LOOP ON ERROR  
 : BNE T6CON2 ; GO TO LOOP ERROR  
 : MOV #14,\$FATAL  
 : MOV #1,\$MSGTY ; MOVE ERROR NUM TO MAILBOX  
 : TST \$SSWREG ; CHECK FOR HALT ON ERROR  
 : BMI IS ; HALT IF SET  
 : HALT ; <CANNOT CLEAR BIT6 IN TCSR>

```

825 003174 052777 000100 175310 1S:
826 003174 000005 T6CON3: BIS #BIT6,TCSR ; SET BIT6 AGAIN
827 003202 000005 RESET ; TRY RESET AGAIN
828 003204 032777 000100 175300 BIT #BIT6,TCSR ; CHECK TO SEE IF CLEAR
829 003212 001416 BEQ 15 ; CONTINUE IF CLEAR
830 003214 032767 040000 175200 BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
831 003222 001364 BNE T6CON3 ; GO TO LOOP ERROR
832 003224 012767 000015 175150 MOV #15,SPATAL ;
833 003232 012767 000001 175140 MOV #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
834 003240 005767 175156 TST SSWREG ; CHECK FOR HALT ON ERROR
835 003244 100401 BHI 15 ; HALT IF SET
836 003246 000000 HALT ; <RESET DID NOT CLEAR BIT6 IN TCSR>
837 003250
838 003250 032767 002000 175144 1S: BIT #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
839 003256 001211 BNE TST6 ; GO TO LOOP ON TEST
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003260 012767 000007 175116
003266 032767 000001 175124
003274 001406
003276 005767 175104
003302 001403
003304 005767 175174
003310 001131
003312
003312 105427 000200
003316 000005
003320 032777 000100 175160
003326 001416
003330 032767 040000 175064
003336 001365
003340 012767 000016 175034
003346 012767 000001 175024
003354 005767 175042
003360 100401
003362 000000
003364
003364 052777 000100 175114
003372 032777 000100 175106
003400 001016
003402 032767 040000 175012
003410 001365
003412 012767 000017 174762
003420 012767 000001 174752
003426 005767 174770
003432 100401
003434 000000
003436
003436 042777 000100 175042
003444 032777 000100 175034
003452 001416
003454 032767 040000 174740
003462 001365
003464 012767 000020 174710
003472 012767 000001 174700
003500 005767 174716
003504 100401
003506 000000
003510
003510 052777 000100 174770
003516 000005
003520 032777 000100 174760
003526 001416
003530 032767 040000 174664
003536 001364
003540 012767 000021 174634
003546 012767 000001 174624
003554 005767 174642
    
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: TEST THAT RCSR BIT6 (RCVR INTERRUPT ENABLE) CAN BE SET AND
: CLEARED, AND THAT RESET CLEARS IT.
TST7:
MOV #7,STESTN ; MOVE TEST NUMBER TO MAILBOX
BIT #BIT0,SENV ; CHECK IF ON APT
BEQ TST7A ; IF NOT ON APT
TST SPASS ; CHECK IF IN FIRST PASS
BEQ TST7A ; BR, IF NOT FIRST PASS
TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST
BNE TST10 ; IF CONSOLE IS UNDER TEST

TST7A:
LP8: MTPS #200 ; DISABLE INTERRUPTS
RESET ; CLEAR EVERYTHING
BIT #BIT6,RCSR ; CHECK BIT6 FOR 0
BEQ TBCON1 ; CONTINUE IF RESET
BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
BNE LP8 ; GO TO LOOP ERROR
MOV #16,SFATAL
MOV #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
TST SSWREG ; CHECK FOR HALT ON ERROR
BMI IS ; HALT IF SET
HALT ; <BIT6 IN RCSR NOT CLEAR BY RESET>

IS:
TBCON1: BIS #BIT6,RCSR ; SET BIT6
BIT #BIT6,RCSR ; CHECK IF BIT SET
BNE TBCON2 ; CONTINUE IF SET
BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
BNE TBCON1 ; GO TO LOOP ERROR
MOV #17,SFATAL
MOV #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
TST SSWREG ; CHECK FOR HALT ON ERROR
BMI IS ; HALT IF SET
HALT ; <CANNOT SET BIT6 IN RCSR>

IS:
TBCON2: BIC #BIT6,RCSR ; CLEAR BIT6
BIT #BIT6,RCSR ; CHECK IF CLEAR
BEQ TBCON3 ; CONTINUE IF RESET
BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
BNE TBCON2 ; GO TO LOOP ERROR
MOV #20,SFATAL
MOV #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
TST SSWREG ; CHECK FOR HALT ON ERROR
BMI IS ; HALT IF SET
HALT ; <CANNOT CLEAR BIT6 IN RCSR>

IS:
TBCON3: BIS #BIT6,RCSR ; SET BIT6 AGAIN
RESET ; ISSUE ANOTHER RESET
BIT #BIT6,RCSR ; CHECK IF RESET CLEARED BIT6.
BEQ IS ; CONTINUE IF CLEAR
BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
BNE TBCON3 ; GO TO LOOP ERROR
MOV #21,SFATAL
MOV #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
TST SSWREG ; CHECK FOR HALT ON ERROR
    
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897 003560 100401      BMI      IS      ; HALT IF SET
898 003562 000000      HALT      ; <SECOND RESET DID NOT CLEAR BIT6>
899 003564 000000      IS:
900 003564 032767 002000 174630  BIT      #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
901 003572 001232      BNE      TST7      ; GO TO LOOP ON TEST
902
903      ; TEST THAT RCSR BIT7 (RCVR DONE) IS CLEAR (BY RESET) AND
904      ; CAN BE READ RELIABLY.
905
906      TST10:
907 003574 012767 000010 174602  MOV      #10,STESTN ; MOVE TEST NUMBER TO MAILBOX
908 003602 000005      RESET     ; CLEAR EVERYTHING
909 003604 032777 030000 174674  BIT      #BIT7,RCSR ; CHECK IF BIT7 CLEAR.
910 003612 001416      BEQ      IS      ; CONTINUE IF RESET
911 003614 032767 040000 174600  BIT      #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
912 003622 001367      BNE      LP9      ; GO TO LOOP ERROR
913 003624 012767 000022 174550  MOV      #22,SFATAL
914 003632 012767 000001 174540  MOV      #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
915 003640 005767 174556      TST      SSWREG ; CHECK FOR HALT ON ERROR
916 003644 100401      BMI      IS      ; HALT IF SET
917 003646 000000      HALT      ; <BIT7 IN RCSR NOT CLEAR BY RESET>
918
919 003650      IS:
920 003650 032767 002000 174544  BIT      #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
921 003656 001346      BNE      TST10 ; GO TO LOOP ON TEST
922
923      ; TEST THAT RCSR BIT15 (DATA SET STATUS) IS CLEAR (BY RESET)
924      ; AND CAN BE READ RELIABLY.
925
926      TST11:
927 003660 012767 000011 174516  MOV      #11,STESTN ; MOVE TEST NUMBER TO MAILBOX
928 003666 000005      RESET     ; CLEAR EVERYTHING
929 003670 032777 100000 174610  BIT      #BIT15,RCSR ; CHECK IF BIT15 IS CLEAR
930 003676 001416      BEQ      IS      ; CONTINUE IF CLEAR
931 003700 032767 040000 174514  BIT      #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
932 003706 001367      BNE      LP10 ; GO TO LOOP ERROR
933 003710 012767 000023 174464  MOV      #23,SFATAL
934 003716 012767 000001 174454  MOV      #1,MSGTY ; MOVE ERROR NUM TO MAILBOX
935 003724 005767 174472      TST      SSWREG ; CHECK FOR HALT ON ERROR
936 003730 100401      BMI      IS      ; HALT IF SET
937 003732 000000      HALT      ; <BIT15 IN RCSR NOT CLEAR BY RESET>
938
939 003734 032767 002000 174460  BIT      #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
940 003742 001346      BNE      TST11 ; GO TO LOOP ON TEST
    
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944 003744
945 003744 012767 000012 174432
946 003752 032767 000001 174440
947 003760 001406
948 003762 005767 174420
949 003766 001403
950 003770 005767 174510
951 003774 001066
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953 003776
954 003776 000005
955 004000 005077 174510
956 004004 032777 000200 174500
957 004012 001424
958
959 004014 005077 174474
960 004020 032777 000200 174464
961 004026 001416
962 004030 032767 040000 174364
963 004036 001357
964 004040 012767 000024 174334
965 004046 012767 000001 174324
966 004054 005767 174342
967 004060 100401
968 004062 000000
969 004064
970 004064 005001
971 004066 052701 010000
972 004072 005301
973 004074 001376
974 004076 032777 000200 174406
975 004104 001016
976 004106 032767 040000 174306
977 004114 001330
978 004116 012767 000025 174256
979 004124 012767 000001 174246
980 004132 005767 174264
981 004136 100401
982 004140 000000
983 004146
984 004146 032767 002000 174252
985 004150 001275
986
987
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991 004152
992 004152 012767 000013 174224
993 004160 032767 000001 174232
994 004166 001406
995 004170 005767 174212
996 004174 001403
997 004176 005767 174302
    
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; TEST THAT LOADING TBUF CLEARS TCSR BIT7 (READY) AND THAT  
 ; BIT7 IS SET AFTER THE TRANSMITTER IS DONE.  
 TST12:

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        MOV      #12,STESTN      ; MOVE TEST NUMBER TO MAILBOX
        BIT      @BIT0,SENV      ; CHECK IF ON APT
        BEQ      NOAPT           ; IF NOT
        TST      @PASS           ; CHECK IF IN FIRST PASS
        BEQ      NOAPT           ; OR IF NOT FIRST PASS
        TST      @CTSTFL         ; IF NOT FIRST PASS - SKIP TEST
        BNE      TST13          ; IF CONSOLE IS UNDER TEST

NOAPT:
LP11:  CLR      @TBUF           ; INITIALIZE (SET TCSR BIT7)
        CLR      @BIT7,@TCSR     ; MOVE ZEROS TO TBUFFER
        BEQ      T30CN1         ; CHECK IF BIT7 CLEAR.
        ; DO IT ONE MORE TIME IN CASE REFRESH BOMBED THE FIRST TEST
        CLR      @TBUF           ; DROP READY WITH THIS CHAR.
        BIT      @BIT7,@TCSR     ; CHECK FOR READY LOW
        BEQ      T30CN1         ; THIS IS A REAL ERROR IF NOT 0
        BIT      @BIT14,SSWREG   ; CHECK FOR LOOP ON ERROR
        BNE      LP11           ; GO TO LOOP ERROR
        MOV      @24,SFATAL      ; MOVE ERROR NUM TO MAILBOX
        MOV      @1,MSGTY        ; CHECK FOR HALT ON ERROR
        TST      @SSWREG         ; HALT IF SET
        BMI     IS              ; <TCSR BIT DID NOT CLEAR AFTER DATA XMIT>

IS:
T30CN1: CLR      R1            ; CLEAR COUNT REG.
        BIS      @10000,R1       ; SET COUNT
        DEC      R1             ; DECREMENT COUNT
        BNE     DECR           ; CONTINUE IF NOT 0
        BIT      @BIT7,@TCSR     ; CHECK IF READY IS BACK ON.
        BNE     IS             ; CONTINUE IF SET.
        BIT      @BIT14,SSWREG   ; CHECK FOR LOOP ON ERROR
        BNE     LP11           ; GO TO LOOP ERROR
        MOV      @25,SFATAL      ; MOVE ERROR NUM TO MAILBOX
        MOV      @1,MSGTY        ; CHECK FOR HALT ON ERROR
        TST      @SSWREG         ; HALT IF SET
        BMI     IS              ; <TCSR BIT7 DID NOT SET AFTER XMIT>

IS:
        BIT      @BIT10,SSWREG   ; CHECK FOR LOOP ON TEST
        BNE     TST12          ; GO TO LOOP ON TEST

; TEST THAT THE TRANSMITTER CAN INTERRUPT AT THE CORRECT VECTOR
TST13:
        MOV      #13,STESTN      ; MOVE TEST NUMBER TO MAILBOX
        BIT      @BIT0,SENV      ; CHECK IF ON APT
        BEQ      TST13A         ; IF NOT ON APT
        TST      @PASS           ; CHECK IF FIRST PASS
        BEQ      TST13A         ; OR, IF NOT FIRST PASS
        TST      @CTSTFL         ; IF NOT FIRST PASS - SKIP TEST
    
```

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996 004202 001043          BNE      TST14          ; IF CONSOLE IS UNDER TEST
997 004204          TST13A:          ;
998 004204 042777 000100 174300 LP12: BIC      #BIT6, #TCSR ; DISABLE XMITTER INTERRUPT
999 004212 012777 004304 174302      MOV      #T31CN1, #TVECT ; SET VECTOR ADDRESS
1000 004220 005077 174300          CLR      #TPSM          ; SET PSM FOR INTERRUPT
1001 004224 106427 000000          MTPS     #0            ; ALLOW INTERRUPTS
1002 004230 052777 000100 174254      BIS      #BIT6, #TCSR ; ENABLE INTERRUPTS
1003 004236 000240          NOP                      ; GIVE IT SOME TIME
1004 004240 032767 040000 174154      BIT      #BIT14, #SSWREG ; CHECK FOR LOOP ON ERROR
1005 004246 001356          BNE      LP12           ; GO TO LOOP ERROR
1006 004250 012767 000026 174124      MOV      #26, #SFATAL
1007 004256 012767 000001 174114      MOV      #1, #MSGTY    ; MOVE ERROR NUM TO MAILBOX
1008 004264 005767 174132          TST      #SSWREG       ; CHECK FOR HALT ON ERROR
1009 004270 100401          BMI     #15           ; HALT IF SET
1010 004272 000000          HALT                    ; <NO INTERRUPT FROM DEVICE>
1011 004274          IS:
1012 004274 032767 002000 174120      BIT      #BIT10, #SSWREG ; CHECK FOR LOOP ON TEST
1013 004302 001323          BNE      TST13         ; GO TO LOOP ON TEST
1014 004304 042777 000100 174200      T31CN1: BIC      #BIT6, #TCSR ; DISABLE INTERRUPT
1015          ;
1016          ; TEST THAT TRANSMITTER DOES NOT INTERRUPT WHEN PSM DISABLES
1017          ;
1018 004312          TST14:
1019 004312 012767 000014 174064      MOV      #14, #TESTN   ; MOVE TEST NUMBER TO MAILBOX
1020 004320 032767 000001 174072      BIT      #BIT0, #ENV   ; CHECK IF ON APT
1021 004326 001406          BEQ     #TST14A        ; IF NOT ON APT
1022 004330 005767 174052          TST      #SPASS        ; CHECK IF IN FIRST PASS
1023 004334 001403          BEQ     #TST14A        ; BR, IF NOT FIRST PASS
1024 004336 005767 174142          TST      #CTSTFL       ; IF NOT FIRST PASS - SKIP TEST
1025 004342 001041          BNE     #TST15         ; IF CONSOLE IS UNDER TEST
1026 004344          TST14A:
1027 004344 042777 000100 174140      LP13: BIC      #BIT6, #TCSR ; CLEAR INT ENABLE
1028 004352 106427 000200          MTPS     #200          ; DISABLE INTERRUPTS
1029 004356 012777 004402 174136      MOV      #25, #TVECT  ; VECTOR POINT TO ERROR
1030 004364 005077 174134          CLR      #TPSM          ; CLEAR PSM FOR INTERRUPT
1031 004370 052777 000100 174114      BIS      #BIT6, #TCSR ; ENABLE INTERRUPTS
1032 004376 000240          NOP                      ; GIVE IT SOME TIME
1033 004400 000416          BR      #15            ; CONTINUE IF NO INTERRUPT.
1034 004402          IS:
1035 004402 032767 040000 174012      BIT      #BIT14, #SSWREG ; CHECK FOR LOOP ON ERROR
1036 004410 001355          BNE      LP13         ; GO TO LOOP ERROR
1037 004412 012767 000027 173762      MOV      #27, #SFATAL
1038 004420 012767 000001 173752      MOV      #1, #MSGTY    ; MOVE ERROR NUM TO MAILBOX
1039 004426 005767 173770          TST      #SSWREG       ; CHECK FOR HALT ON ERROR
1040 004432 100401          BMI     #15           ; HALT IF SET
1041 004434 000000          HALT                    ; <DEVICE GAVE INTERRUPT WITH PSM DISABLE>
1042 004436          IS:
1043 004436 032767 002000 173756      BIT      #BIT10, #SSWREG ; CHECK FOR LOOP ON TEST
1044 004444 001322          BNE      TST14         ; GO TO LOOP ON TEST
1045          ;
1046          ; TEST THAT XMITTER DOES NOT RE-INTERRUPT AFTER THE FIRST
1047          ; INTERRUPT IS SERVICED.
1048          ;
1049 004446          TST15:
1050 004446 012767 000015 173730      MOV      #15, #TESTN   ; MOVE TEST NUMBER TO MAILBOX
1051 004454 032767 000001 173736      BIT      #BIT0, #ENV   ; CHECK IF ON APT
    
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 DVKREB.P11 ERROR 27 DEVICE GAVE INTERRUPT WITH PSM DISABLE

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1052 004462 001406          BEQ      TST15A      ; IF NOT ON APT
1053 004464 005767 173716  TST      SPASS      ; CHECK IF IN FIRST PASS
1054 004470 001403          BEQ      TST15A      ; BR, IF FIRST PASS
1055 004472 005767 174006  TST      CTSTFL     ; IF NOT FIRST PASS - SKIP TEST
1056 004476 001066          BNE      TST16      ; IF CONSOLE IS UNDER TEST
1057 004500          TST15A:
1058 004500 042777 000100 174004  LP14: BIC      @BIT6,@TCSR ; CLEAR INTERRUPT DISABLE
1059 004506 012777 004570 174006  MOV      @T33CN1,@TVECT ; SET UP VECTOR ADDRESS
1060 004514 005077 174004  CLR      @TPSW      ; PSM FOR VECTOR
1061 004520 106427 000000  MTPS    80         ; ALLOW INTERRUPTS
1062 004524 052777 000100 173760  BIS      @BIT6,@TCSR ; ENABLE INTERRUPT
1063 004532 000240          NOP          ; TIME
1064 004534 032767 040000 173660  BIT      @BIT14,@SSWREG ; CHECK FOR LOOP ON ERROR
1065 004542 001356          BNE      LP14      ; GO TO LOOP ERROR
1066 004544 012767 000030 173630  MOV      @30,@SFATAL ;
1067 004552 012767 000001 173620  MOV      @1,@MSGTY  ; MOVE ERROR NUM TO MAILBOX
1068 004560 005767 173636  TST      @SSWREG    ; CHECK FOR HALT ON ERROR
1069 004564 100401          BMI     IS        ; HALT IF SET
1070 004566 000000          HALT        ; <DEVICE FAILED TO INTERRUPT>
1071 004570          IS:
1072 004570 012777 004610 173724  T33CN1: MOV      @ERR26,@TVECT ; SET UP VECTOR FOR RE-INTERRUPT
1073 004576 005016          CLR      (SP)      ;
1074 004600 012746 004654  MOV      @TST16,-(SP) ; POINT TO NEXT TEST FOR RTI
1075 004604 000002          RTI        ; SERVICE INTERRUPT
1076 004606 000240          NOP          ;
1077 004610          ERR26:
1078 004610 032767 040000 173604  BIT      @BIT14,@SSWREG ; CHECK FOR LOOP ON ERROR
1079 004616 001364          BNE      T33CN1   ; GO TO LOOP ERROR
1080 004620 012767 000031 173554  MOV      @31,@SFATAL ;
1081 004626 012767 000001 173544  MOV      @1,@MSGTY  ; MOVE ERROR NUM TO MAILBOX
1082 004634 005767 173562  TST      @SSWREG    ; CHECK FOR HALT ON ERROR
1083 004640 100401          BMI     IS        ; HALT IF SET
1084 004642 000000          HALT        ; <DEVICE RE-INTERRUPTED AFTER FIRST INTERRUPT SERVICE>
1085 004644          IS:
1086 004644 032767 002000 173550  BIT      @BIT10,@SSWREG ; CHECK FOR LOOP ON TEST
1087 004652 001275          BNE      TST15     ; GO TO LOOP ON TEST
1088          ;
1089          ; TEST TRANSMITTER AND RECIEVER BUFFERS.
1090          ; NOTE: SPECIAL WRAP MODULE MUST BE INSTALLED TO RUN
1091          ; THIS TEST. THIS TEST WILL RUN IF BIT9 OF SSWREG =1.
1092          ;
1093          ; TST16:
1094 004654 012767 000016 173522  MOV      @16,@STESTN ; MOVE TEST NUMBER TO MAILBOX
1095 004662 032767 000001 173530  BIT      @BIT0,@SENV ; CHECK IF ON APT
1096 004670 001406          BEQ      NOAPT1    ; IF NOT
1097 004672 005767 173510  TST      SPASS      ; CHECK IF IN FIRST PASS
1098 004676 001403          BEQ      NOAPT1    ; BR, IF FIRST PASS
1099 004700 005767 173600  TST      CTSTFL     ; IF NOT FIRST PASS - SKIP TEST
1100 004704 001147          BNE      TST999    ; IF CONSOLE IS UNDER TEST
1101 004706          NOAPT1:
1102 004706 032767 001000 173506  BIT      @BIT9,@SSWREG ; CHECK IF THIS TEST IS ENABLED
1103 004714 001537          BEQ      TST17     ; SKIP IF NOT
1104 004716 000005          LP15: RESET        ; CLEAR EVERYTHING
1105 004720 106427 000200  MTPS    @200      ; DISABLE INTERRUPTS
1106 004724 012703 000020  MOV      @20,@R3    ; SET SYNC COUNTER
1107 004730 005777 173554  TST      @RBUF      ; CLEAR BUFFER

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1108 004734 005004          CLR      R4          ; CLEAR DELAY COUNTER
1109 004736 005204          INC      R4          ; DELAY 300 MS
1110 004740 001376          BNE     INCR4:      INCR4      ;
1111 004742 052777 000011 173536  BIT     #11,ARCSR   ; SET READER ENABLE
1112 004750 000240          NOP
1113 004752 000240          NOP
1114 004754 105777 173532          CHK1:  TSTB     @TCSR     ; CHECK FOR XMITTER DONE
1115 004760 100375          BPL     CHK1        ; WAIT TIL READY
1116 004762 012777 000125 173524  MOV     #125,@TBUF   ; SEND DATA
1117 004770 105777 173512          CHK2:  TSTB     @RCSR     ; WAIT FOR RCVR DONE
1118 004774 100375          BPL     CHK2
1119 004776 122777 000125 173504  CHKSYN: CMPB     #125,@RBUF   ; CHECK FOR SYNC BYTE
1120 005004 001426          BEQ     T34CON      ; CONTINUE IF FOUND
1121 005006 005303          DEC     R3          ; DECREMENT SYNC COUNTER
1122 005010 001367          BNE     CHK2        ; CONTINUE TIL SYNC UP
1123 005012 012777 000001 173466  MOV     #BIT0,@RCSR ; TURN OFF WRAP MODULE
1124 005020 000240          NOP
1125 005022 000240          NOP
1126 005024 000005          RESET
1127 005026 032767 040000 173366  BIT     #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
1128 005034 001330          BNE     LP15        ; GO TO LOOP ERROR
1129 005036 012767 000032 173336  MOV     #32,$FATAL
1130 005044 012767 000001 173326  MOV     #1,$MSGTY   ; MOVE ERROR NUM TO MAILBOX
1131 005052 005767 173344          TST     SSWREG      ; CHECK FOR HALT ON ERROR
1132 005056 100401          BMI     IS          ; HALT IF SET
1133 005060 000000          HALT               ; <CANNOT GET TEST MODULE IN SYNC>
1134 005062 005001          IS:  T34CON: CLR     R1          ; INITIALIZE DATA REG
1135 005064 012702 177777          MOV     @-1,R2      ; INITIALIZE R2
1136 005070 005777 173414          TST     @RBUF       ; FORCE BUFFER CLEAR
1137 005074 105777 173412          CHKT:  TSTB     @TCSR     ; CHECK XMITTER DONE
1138 005100 100375          BPL     CHKT        ; WAIT TIL DONE
1139 005102 010177 173406  SDATA:  MOV     R1,@TBUF   ; SEND DATA
1140 005106 105777 173374          CHKR:  TSTB     @RCSR     ; CHECK FOR RCVR DONE
1141 005112 100375          BPL     CHKR        ; WAIT TIL DONE
1142 005114 017702 173370          MOV     @RBUF,R2    ; GET WRAPPED DATA
1143 005120 020102          CMP     R1,R2       ; CHECK DATA
1144 005122 001012          BNE     25
1145 005124 005201          INC     R1          ; INCREMENT DATA
1146 005126 105701          TSTB     R1         ; CHECK FOR END OF DATA
1147 005130 001364          BNE     SDATA       ; CONTINUE LOOP
1148 005132 012777 000001 173346  MOV     #BIT0,@RCSR ; TURN OFF LOOP
1149 005140 000240          NOP
1150 005142 000240          NOP
1151 005144 000005          RESET
1152 005146 000422          BR     TST17
1153 005150 005150          25:  TST17
1154 005152 032767 040000 173244  BIT     #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
1155 005154 001353          BNE     CHKR        ; GO TO LOOP ERROR
1156 005160 012767 000033 173214  MOV     #33,$FATAL
1157 005166 012767 000001 173204  MOV     #1,$MSGTY   ; MOVE ERROR NUM TO MAILBOX
1158 005174 005767 173222          TST     SSWREG      ; CHECK FOR HALT ON ERROR
1159 005200 100401          BMI     IS          ; HALT IF SET
1160 005202 000000          HALT               ; <DATA DID NOT COMPARE ON SLU WRAP>
1161 005204 032767 002000 173210  IS:  BIT     #BIT10,SSWREG ; CHECK FOR LOOP ON TEST

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1164 005212 001220          BNE      TST16          ; GO TO LOOP ON TEST
1165 005214          TST17:          RESET
1166 005214 000005          CLR      R4
1167 005216 005004          T35DEC: DEC      R4          ; DEC TIMER
1168 005220 005304          BNE      T35DEC
1169 005222 001376          TST999:
1170 005224          INC      SDEVCT          ; INC DEVICE COUNTER
1171 005224 005267 173160 173152 T999A: CMP      TMP2,SDEVCT      ; ALL DEVICES TESTED?
1172 005230 026767          BEQ      T999B          ; IF YES
1173 005232 001404          CLR      CTSTFL        ; CLEAR CONSOLE UNDER TEST FLAG
1174 005240 005067 173240          JMP      SETUP          ; GO TEST NEXT DEVICE
1175 005244 000167 174360          T999B: INC      J8SPASS      ; INCREMENT PASS COUNT
1176 005250 005237 000406          JSR      PC,MSGPRT      ; PRINT END OF PASS
1177 005254 004767 000046          .WORD   M3
1178 005260 005572          ACT:     MOV      J842,RO  ; CHECK ACT
1179 005262 013700 000042          BEQ      GOAGIN        ; KEEP GOING
1180 005266 001405          RESET
1181 005270 000005          SENDAD: JSR      PC,(RO)  ; ACT HOOKS
1182 005272 004710          NOP
1183 005274 000240          NOP
1184 005276 000240          NOP
1185 005300 000240          GOAGIN: CLR      SDEVCT      ; RESET DEVICE COUNT
1186 005302 005067 173102          CMP      #1,TMP2      ; IS THIS THE ONLY DEVICE UNDER TEST?
1187 005306 022767 000001 173164          BNE      RSTRT        ; IF NO
1188 005314 001026          MOV      #STKPTR,SP    ; INITIALIZE STACK POINTER
1189          JMP      TST1          ; GO DO ANOTHER PASS
1190 005316 012706 001000          BITB    #40,SENVN      ; WILL APT ALLOW PRINTING?
1191 005322 000167 174420          BEQ      TYPE          ; YES
1192 005326 132767 000040 173065 MSGPRT: ADD     #2,(SP)          ; ADJUST RETURN
1193 005334 001403          RTS     PC              ; RETURN
1194 005336 062716 000002          TYPE:  MOV      (SP),RO  ; GET MESSAGE ADDRESS
1195 005342 000207          WAIT:  MOV      (RO),RO   ; GET READY TO PRINT
1196 005344 011600          TSTB   JTPS             ; CHECK IF TTY READY
1197 005346 011000          BPL    WAIT            ; IF NOT
1198 005350 105777 000030          MOVB   (RO),JTPB       ; PRINT THE CHARACTER
1199 005354 100375 000020          BNE    WAIT            ; NEXT IF NOT DONE
1200 005356 112077 000002          ADD    #2,(SP)        ; ADJUST RETURN
1201 005362 001372          RTS     PC              ; RETURN
1202 005364 062716 000002          RSTRT: CLR      SUNIT      ; START OVER
1203 005370 000207          JMP      START
1204 005372 005067 173014          .WORD   177566
1205 005376 000167 173576          .WORD   177564
1206 005402 177566          ENDTST: 0
1207 005404 177564          UINT:
1208 005406 000000          MOV      #34,SFATAL
1209 005410          MOV      #1,$MSGTY      ; MOVE ERROR NUM TO MAILBOX
1210 005410 012767 000034 172764          HALT    ; <UNEXPECTED INTERRUPT>
1211 005416 012767 000001 172754          15:
1212 005424 000000          PWRFL:  MOV      #PWRUP,J824  ; SET POWER UP VECTOR
1213 005426          MOV      #340,J826      ; SET POWER UP PSW
1214 005428 012737 005446 000024          HALT
1215 005434 012737 000340 000026          BR
1216 005442 000000          .-2
1217 005444 000776
1218
1219

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1220
1221 005446 012737 005426 000024 PWRUP: MOV @PWRFL, @#24 ;SET POWER FAIL VECTOR
1222 005454 005037 000026 CLR @#26 ;SET POWER UP PSM
1223 005460 005000 CLR R0 ;CLEAR TTY WAIT TIMER
1224 005462 005200 TTYWT: INC R0 ;INCREMENT TIMER
1225 005464 001376 BNE TTYWT ;WAIT FOR TTY POWER UP
1226 005466 C 4767 177634 JSR PC,MSGPRT ;TYPE "POWER" MESSAGE
1227 005472 005610 .WORD M4
1228 005474 000167 172520 JMP PRCONT ;START AT BEGINNING OF PRESENT PASS
1229
1230 005500 040515 047111 042504 M1: .ASCIZ .MAINDEC-11-DVKA-E-B DLVII TEST.<15><12>
1231 005506 026503 030461 042055
1232 005514 045526 042501 041055
1233 005522 020040 042011 053114
1234 005530 044511 052040 051505
1235 005536 006524 000012
1236 005542 020040 042040 053105 M2: .ASCIZ . DEVICES UNDER TEST.<15><12>
1237 005550 041511 051505 052440
1238 005556 042116 051105 052040
1239 005564 051505 006524 000012
1240 005572 047105 020104 043117 M3: .ASCIZ .END OF PASS.<15><12>
1241 005600 050040 051501 006523
1242 005606 000012
1243 005610 047520 042527 006522 M4: .ASCIZ .POWER.<15><12>
1244 005616 000012
1245 000001 .END
    
```

.MAIN, MACY11 27(732) 04-OCT-76 14:23 PAGE 29  
 DVKAE8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

Variable	Value	Symbol 1	Symbol 2	Symbol 3	Symbol 4	Symbol 5	Symbol 6	Symbol 7	Symbol 8	Symbol 9	Symbol 10	Symbol 11
RBASE	176500		410	4428								
ACOM1	000000											
ACOM2	000000											
ACUP	000000		384									
ACT	000000											
ROOM0	000000											
ROOM1	000000											
ROOM10	000000											
ROOM11	000000											
ROOM12	000000											
ROOM13	000000											
ROOM14	000000											
ROOM15	000000											
ROOM16	000000											
ROOM17	000000											
ROOM18	000000											
ROOM19	000000											
AEVCT	000000		375									
ADEVN	000000		411									
ADR	001712		611									
ARTBL	000600		531		606							
REW	000000		380									
REWH	000000		381									
AFATAL	000000		372									
AROR1	000000		409									
AROR2	000000		401									
AROR3	000000		404									
AROR4	000000		407									
AROR5	000000		391									
AROR6	000000		392									
AROR7	000000		393									
AROR8	000000		394									
AROR9	000000		395									
AROR10	000000		396									
AROR11	000000		397									
AROR12	000000		398									
AROR13	000000		399									
AROR14	000000		400									
AROR15	000000		401									
AROR16	000000		402									
AROR17	000000		403									
AROR18	000000		404									
AROR19	000000		405									
AROR20	000000		406									
AROR21	000000		407									
AROR22	000000		408									
AROR23	000000		409									
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AROR31	000000		417									
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AROR34	000000		420									
AROR35	000000		421									
AROR36	000000		422									
AROR37	000000		423									
AROR38	000000		424									
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AROR109	000000		495									
AROR110	000000		496									
AROR111	000000		497									
AROR112	000000		498									
AROR113	000000		499									
AROR114	000000		500									
AROR115	000000											













.SR2A2	10	
.SSAVE	10	
.SSB20	10	
.SSB20	10	
.SSCOP	10	
.SSIZE	10	
.SSUPR	10	
.STRAP	10	350#
.STYPB	10	
.STYPD	10	
.STYPE	10	350#
.STYPO	10	
.SHOCK	10	
.1170	10	

ADD	514	534	536	558	575	598	604	1194	1202										
ASL	519	547	566	567	569	571	573	597	602										
BEG	1023	848	548	578	683	685	711	713	721	743	758	776	778	786	817				
BCE	1023	1052	850	857	879	891	910	929	947	949	957	961	992	994	1021				
BIC	1023	741	815	877	998	1014	1027	1058											
BIS	1023	755	804	826	866	888	971	1002	1031	1062	1111								
BIT	1023	577	584	595	610	616	627	635	646	654	666	674	682	692	700				
BITB	1023	720	722	731	733	742	744	757	759	767	775	785	787	796	805				
BLT	1023	816	818	828	830	838	847	856	858	867	869	878	880	890	892				
BMI	1023	909	911	919	928	930	938	946	956	960	962	974	976	984	991				
BNE	1023	1012	1020	1035	1043	1051	1064	1078	1086	1095	1102	1127	1155	1163					
BPL	1023	503	1192																
BR	1023	538																	
CLR	1023	651	671	697	727	738	749	764	792	801	812	823	835	863	874				
CHP	1023	897	916	935	967	981	1009	1040	1069	1083	1132	1160							
CHPB	1023	504	585	596	611	617	628	636	647	655	667	675	687	693	701				
DEC	1023	718	723	732	734	745	754	760	768	780	788	797	806	808	819				
HLT	1023	839	852	859	868	870	881	893	901	912	920	931	939	951	963				
INC	1023	975	977	985	996	1005	1013	1025	1036	1044	1056	1065	1079	1087	1100				
JMP	1023	1122	1128	1145	1148	1156	1164	1169	1188	1201	1225								
JSR	1023	1115	1118	1139	1142	1199													
MOV	1023	527	549	586	600	625	644	664	690	1033	1153	1218							
NOVB	1023	358	359	360	361	510	511	542	553	564	582	716	955	959	970				
HTPS	1023	1030	1060	1073	1108	1135	1167	1174	1186	1204	1222	1223							
NOP	1023	537	559	591	1144	1172	1187												
RESET	1023	972	1121	1168															
ROLB	1023	633	652	672	698	728	739	750	765	793	802	813	824	836	864				
RTI	1023	886	898	917	936	968	982	1010	1041	1070	1084	1133	1161	1212	1217				
RTS	1023	518	525	526	546	557	589	599	601	717	1109	1146	1171	1176	1224				
SUB	1023	593	618	1175	1191	1205	1228												
SWAB	1023	509	550	580	588	590	603	606	607	608	613	614	622	623	629	630	630	630	630
TST	1023	356	495	512	513	522	523	531	532	533	535	543	552	556	563				
	1023	583	587	588	590	603	606	607	608	613	614	622	623	629	630	630	630	630	630
	1023	641	642	648	649	656	661	662	668	669	676	681	688	694	695	695	695	695	695
	1023	709	724	725	735	736	746	747	752	761	762	774	783	789	790	790	790	790	790
	1023	799	809	810	821	821	832	833	846	860	861	871	872	882	883	883	883	883	883
	1023	895	907	913	914	926	932	933	945	964	965	978	979	990	999	999	999	999	999
	1023	1006	1019	1029	1037	1038	1050	1059	1066	1067	1072	1074	1080	1081	1094	1094	1094	1094	1094
	1023	1106	1123	1129	1130	1136	1140	1143	1149	1157	1158	1179	1190	1196	1197	1197	1197	1197	1197
	1023	1210	1215	1216	1221														
	1023	554	1001	1028	1061	1105													
	1023	784	1032	1063	1076	1112	1113	1124	1125	1150	1151	1183	1184	1185					
	1023	703	782	827	855	889	908	927	954	1104	1126	1152	1166	1181					
	1023	719	574																
	1023	570																	
	1023	353																	
	1023	539	1203																
	1023	515																	
	1023	565																	
	1023	499	576	524	544	609	624	631	643	650	663	670	684	686	689				
	1023	696	516	714	726	737	763	777	777	791	800	811	822	834	849				
	1023	851	862	873	884	896	915	934	948	950	966	980	995	1008	1022				
	1023	1024	1039	1053	1055	1068	1082	1097	1099	1107	1131	1159							

TSTB	1114	1117	1138	1141	1147	1198											
.ASCIZ	1230	1236	1240	1243													
.BLKW	492	493															
.BYTE	360	381	391	392	399	400	402	403	405	406							
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.ENDC	369	391	399	402	405	408	409	410	411	414	417	419	426	629	633		
	637	648	652	656	668	672	676	694	698	702	724	728	730	735	739		
	741	746	750	752	761	765	769	789	793	795	798	802	804	809	813		
	815	820	824	826	832	836	840	860	864	866	871	875	877	882	886		
	888	894	898	902	913	917	921	932	936	940	964	968	970	978	982		
	986	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1084	1088	1129	1133		
	1135	1157	1161	1165	1210	1212	1214										
.EVEN	369																
.IF	368	391	399	402	405	408	409	410	411	412	414	416	418	425	627		
	631	635	646	650	654	666	670	674	692	696	700	722	726	730	733		
	737	741	744	748	752	759	763	767	787	791	795	796	800	804	807		
	811	815	818	822	826	830	834	838	858	862	866	869	873	877	880		
	884	888	892	896	900	911	915	919	930	934	938	962	966	970	976		
	980	984	1004	1008	1012	1035	1039	1043	1064	1068	1072	1078	1082	1086	1127		
	1131	1135	1155	1159	1163	1210	1212	1214									
.IFF	369	417	419	426													
.IIF	369																
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	710	724	725	735	736	746	747	761	762	775	789	790	798	799	809		
	810	820	821	832	833	847	860	861	871	872	882	883	894	895	908		
	913	914	927	932	933	946	964	965	978	979	991	1006	1007	1020	1037		
	1038	1051	1066	1067	1080	1081	1095	1129	1130	1157	1158	1210	1211				
.MACRO	1	467	468														
.MCALL	350																
.NEXT	413																
.NLIST	1	317	369	623	629	630	642	648	649	662	668	669	682	694	695		
	710	724	725	735	736	746	747	761	762	775	789	790	798	799	809		
	810	820	821	832	833	847	860	861	871	872	882	883	894	895	908		
	913	914	927	932	933	946	964	965	978	979	991	1006	1007	1020	1037		
	1038	1051	1066	1067	1080	1081	1095	1129	1130	1157	1158	1210	1211				
.PAGE	414	461	469	494	769	841	940										
.REM	1																
.REPT	340	414	629	648	668	694	724	735	746	761	789	798	809	820	832		
.SBTTL	366	871	882	894	913	932	964	978	1006	1037	1066	1080	1129	1157	1210		
	860	371	372	373	374	375	376	377	378	382	383	384	397	401	404		
.WORD	363	371	372	373	374	375	376	377	378	382	383	384	397	401	404		
	407	408	409	410	411	430	431	432	433	434	435	461	462	463	464		
	465	581	1178	1206	1207	1227											

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

\*.DVKREB.SEG/SOL/CRF/PAGNUM/NL:TOC=SYSMAC.CO,DVKREB.P11  
 RUN-TIME: 24 28 2 SECONDS  
 RUN-TIME RATIO: 217/56=3.8  
 CORE USED: 33K (65 PAGES)