

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell
John Leng

CC: Win Hindle
Bob Kleine
Ken Olsen ✓

DATE: December 14, 1976
FROM: Ulf Fagerquist/Ron Bingham
DEPT: LCDG *Ulf* *RHB*
EXT: 6408
LOC/MAIL STOP: MR 1-2/E78

SUBJ: SMALL MACHINE R & D

The results on the R & D project are encouraging. The first phase will be completed within the next eight weeks when we power-on the hardware - that is four weeks late. We can still meet the April "Software Ready" date, at which time we should have a complete system (similar in performance to KA10) for 20% of current CPU costs.

The decision was made last Friday by the Management Committee to request approval to order parts for fifty pilots, for building if we so decide, when the evaluation of the bread-board is done.

The biggest risk (to manage) is over optimism; it is too early to get carried away in thinking we have a significant system innovation in front of us, but it is not too early to start preparing for it!

The word is getting out - after twelve months of hiding in the back room - and more people are getting involved; the control/security issues are going to be most challenging. The best approach now is probably to create a state of high level of confusion.

The innovation or the rediscovery that a few of the right people can engineer simple products in a small way seems to work for 36-bit computers also. The only place we tried something new - the multiwire process - has cost us four weeks delay; everything else has been proven by others.

We believe that the innovative concepts should not stop with the engineering phase. Just a few thoughts that we would like to make real.....

The traditional way of looking at the QDP CPU memory system is that we have created a lower cost "engine" that is capable of running the complete TOPS-20 (also it turns out the TOPS-10) Software System, all languages, COBOL, FORTRAN, ALGOL, APL... full capability DBMS database management, transaction processing in network and distributed processing applications and an engine for our "leadership" in T/S products!

In short, we could have a complete system we now sell for \$300-500K for a portion of this price if we have to.

We think this way of thinking will give way very quickly considering the following concepts as a mental exercise:

The CPU and memory could be viewed as a very minor portion of the RK06 disk drive. This opens up the possibility of looking at TOPS-20 engines as options to DEC produced DISK Systems (intelligent controllers) that handle all DBMS administration of data as well as communication of data over DECNET; the same is true as part of tape systems and "word processing" KL-board in a letter perfect line printer.

The fact that these small systems have a very powerful software system with NETWORK CAPABILITY will allow customers to develop their own application systems at a very low cost. The TOPS-20/10 System is easy to program, maybe cheaper to program than a PDP-8. When the application is done, it can be attached to DECNET as part of the customer's distributed network.

These were product oriented thoughts, but there are just as many opportunities to explore in the process area:

- . Manufacturing

Our current estimate for man-hours necessary to assemble the QDP is twenty hours. Several improvements are possible; fewer boards, of course, but most important, design the machine for a "robot production process" 30 man-minutes/FA&T. What about using a "vertical production line" to save floor space. (= minimum number of DEC man-hours)

- . Field Service

Current KL20 has remote diagnostics capability; customer calls FS and a FS Engineer can call in to the computer and can remotely diagnose the whole machine, while another FS Engineer travels to the site to repair it, etc.

QDP will have the ultimate of remote repair - it includes an 8080 - and full parity checking internally and can be programmed to run its own diagnosis, and in effect, "call the FS office" to tell it's sick and needs a module replaced. It also has LED indications that will make it easier to locate what module to replace. In essence, let the machine diagnose itself, the customer replace faulty parts and DEC produce and sell the spares. (= minimum number of DEC man-hours)

. Marketing

The big success of this product can only come from a well disciplined/managed market plan. We have time now to do the right homework - MMT - Market Maturity Test project. This could be done by selling QDP internally to DEC "customers" and develop, monitor and perfect the whole "customer satisfaction", order processing, service, etc., processes before we sell it to real customers. In addition, we will save a lot on the capital investment side.

We have spent \$100K to date on the project since we started in April and expect to spend another \$80K through systems bread-board check-out.

Request:

We feel that the potential for a successful product exists and would like to have \$1.5M of corporate funds allocated for use in continued QDP R & D activities - product and process oriented - during FY 78. Our intent is to continue to keep the project as small as possible, but expand the scope and breadth of the goals.

The funding will be spent only after acceptance of proposals on an ongoing basis -- no blank check.

In summation, this project will give us an excellent opportunity to reevaluate a lot of traditional concepts and find a way to break some bottlenecks in our current system.

UF/ap

SM-10 PROJECT PLAN

SECTION I - SUMMARY

1.1 Identifying Information

| | |
|----------------|---|
| Project Name | SM10 |
| Project Number | ----- Revision Number Date - <u>5/18/76</u> |
| Author | Ron Bingham |

1.2 This project is currently budgeted

1.3 Overview

| | | |
|---------------|-------------|-----------------------------|
| <u>People</u> | R. Bingham | Project Manager |
| | B. Reid | Principle Designer |
| | S. Pomfret | Project Technician |
| | D. Lewine | Principle Software Designer |
| | | Microcoder |
| | | Logic Designer |
| | B. Bruckert | I/O Designer |

The goals of this project are:

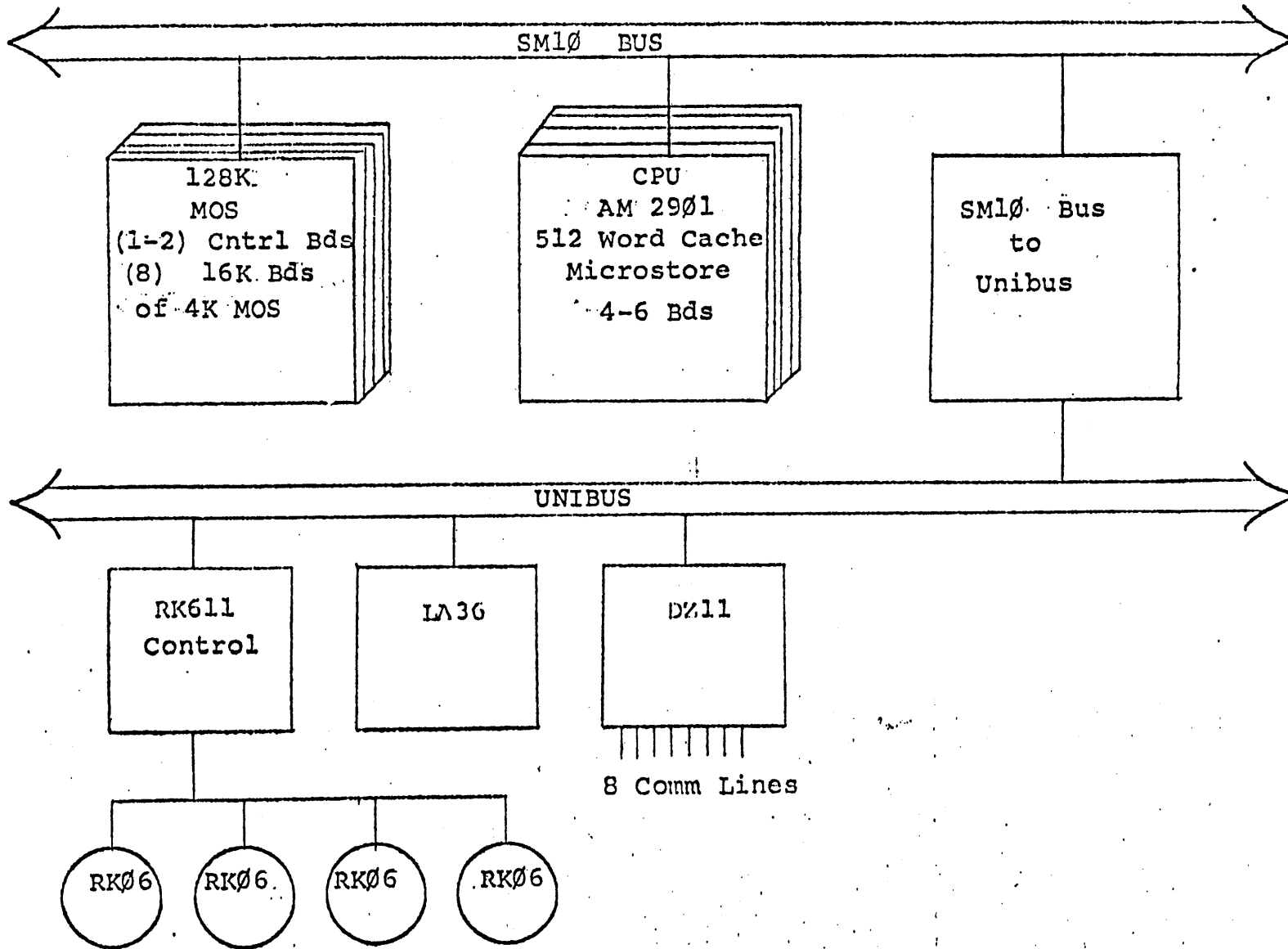
1. Prototype running monitor by 1 April 1977
2. Prototype cost of 15K for CPU, 64K MOS Memory, Console terminal, eight terminal controllers, and a 14 megabyte disk.
3. KA10 performance
4. Runs TOPS-20
5. KL10 instruction set - less I/O and KA double precision floating point
6. Development cost of \$350K to prototype running
7. An MTBF of 2000 hours

Type of Product: New Product Feasibility Demonstration (proto only)

Product Description: A PDP-10 based computer system for personal use (see diagram)

LOW COST 1Ø

LOW POWER SCHOTTKY



1.4 Summary Schedule

| | |
|------------------------------|-----------------------------|
| Start Design | April 1976 |
| Operate Prototype | Jan 1977 |
| Monitor Running | April 1977 |
| Planned Development Cost | \$350K to prototype running |
| Planned Development Manpower | 6 man years |

1.5 Development Strategy

Our development strategy departs from previous approaches in which all phases of the product were addressed simultaneously. For example, manufacturing people were in from the beginning on KLLØ development and there was a lot of wasted motion as Manufacturing and Engineering tried to solve problems and answer production related questions based on very little stable information.

What we are proposing here is to rather than try to solve every problem simultaneously we stage the development into three over lapping phases. A breadboard build, a limited production/manufacturability/supportability/marketability phase and finally a volume production phase.

1.5.1 Phase I

The goal of Phase I is to verify our initial design concepts, produce a running breadboard and build a data base for Phase II. In Phase I our task then is to take the shortest possible path to a running breadboard.

To implement Phase I we have put together a small but experienced group of designers with very few interfaces to other groups such as Mechanical Engineering, Circuit Analysis, Field Service, Drafting, Diagnostics, Power Supply Engineering and Production. Our belief is that by reducing the number of conflicting ideas and personalities the design will proceed rapidly, be cohesive and development cost will be held to a minimum. Since we have purposely limited our resources in Phase I we will force ourselves to take advantage of what already exists, will avoid technically risky approaches and won't be tempted to add unnecessary frills and features. This first phase has been affectionately referred to as "The Garage".

1.5.1 (Continued)

This phase will last from 4/76 until 4/77. Starting 10/76 planning will begin for Phase II and in 1/77 a review will be held on progress in Phase I and plans for Phase II.

1.5.2 Phase II

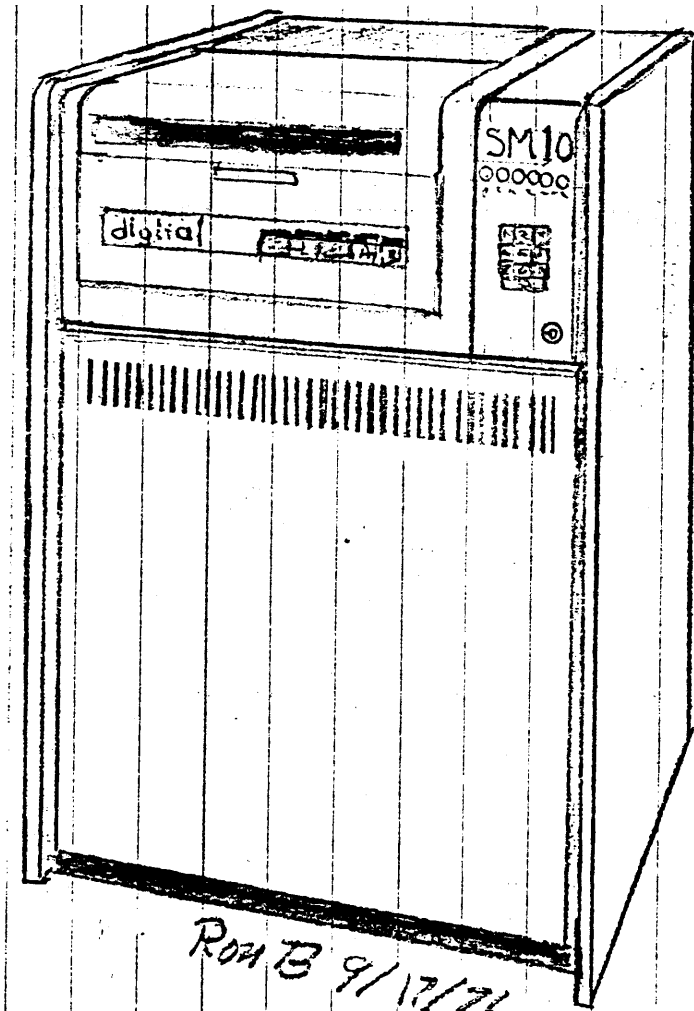
The goals of Phase II are to verify the manufacturability, field supportability and marketability of the design. This will be accomplished by manufacturing some quantity of units not to exceed 100 for sale to our friends in the academic and research community. Their evaluation and feed back will constitute a field test of the hardware. It is anticipated that this phase would begin 1/77. The first hardware would be shipped 6/77 and the last unit shipped before 1/78.

1.5.3 Phase III

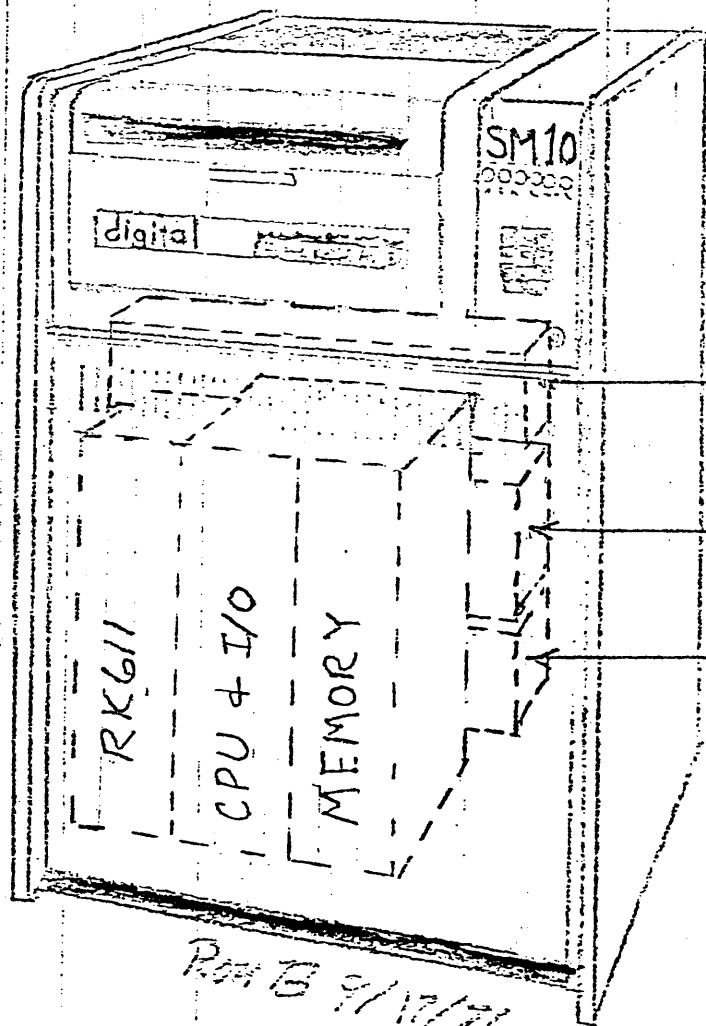
This would be the volume shipment phase. Preparations would probably begin 4/77 with the first ship starting 1/78.

1.6 Risks

This approach to development may be more time consuming. We may be faced with extensive redesign in Phase II.



ROA B 9/17/76



H317 TTY PANE

POWER SUPP.

POWER CONTROL

RMTB 9/17/76

APR | MAY | JUN | JUL | AUG | SEP | OCT | NOV | DEC | JAN | FEB | MAR

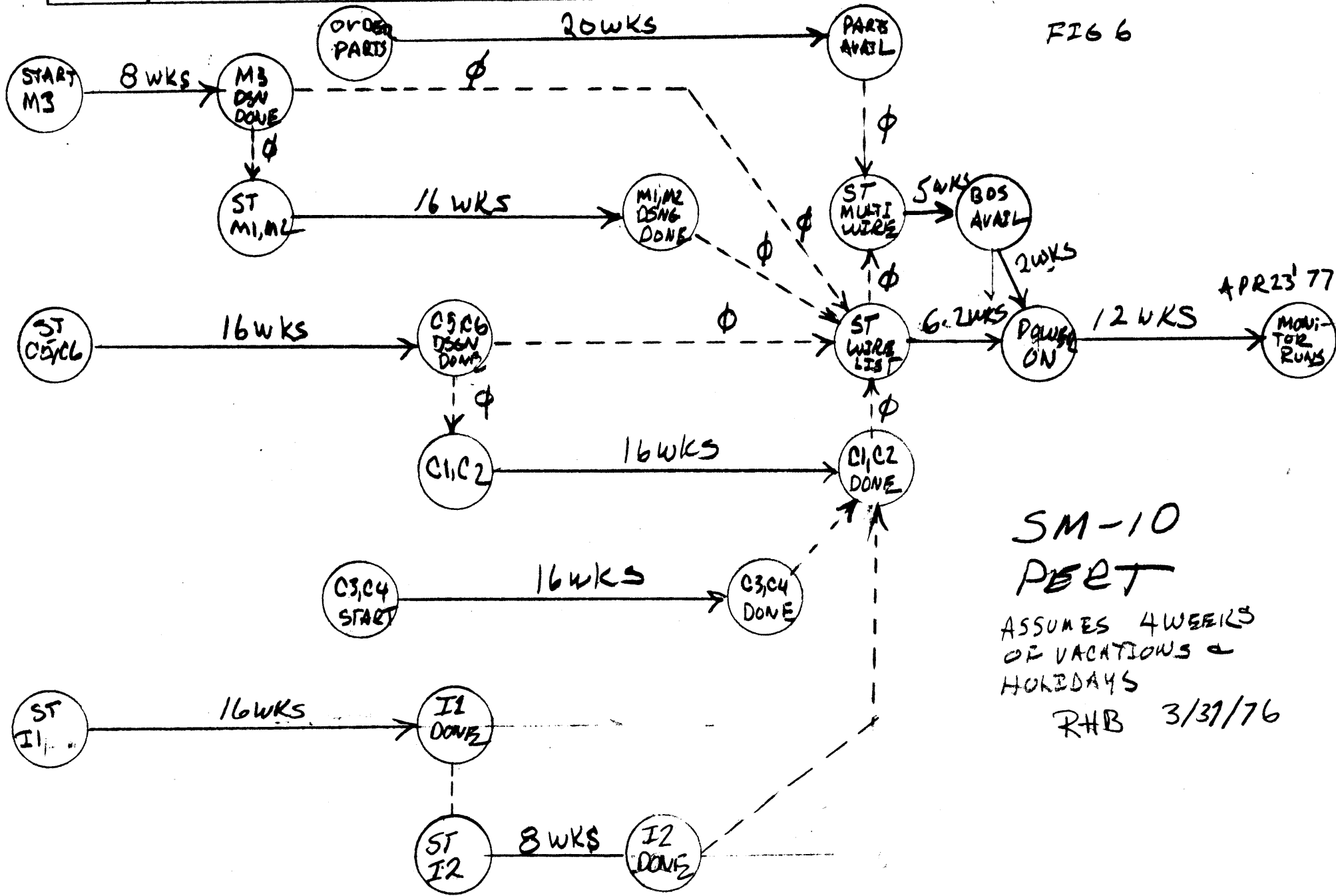


FIG 6

SM-10
 PERT
 ASSUMES 4 WEEKS
 OF VACATIONS &
 HOLIDAYS
 RHB 3/31/76

SM-10 MANPOWER NOMENCLATURE

| TOTAL | 3.58 Q ₁ | 5.75 Q ₁ | 6.75 Q ₂ | 7.25 Q ₃ |
|-------------------|------------------------------------|----------------------------------|----------------------------------|----------------------------------|
| CPU DESIGN | BOB REID LOGIC DESIGNER 1.5E | BOB REID LOGIC DESIGNER 2E | BOB REID LOGIC DESIGNER 2E | BOB REID LOGIC DESIGNER 2E |
| MEMORY DESIGN | STEVE POMFRET 1E | STEVE POMFRET 1E | STEVE POMFRET 1E | STEVE POMFRET 1E |
| I/O DESIGN | BILL BRUCKERT 1/3E | BILL BRUCKERT(?) 1E | BILL BRUCKERT(?) 1E | BILL BRUCKERT(?) 1E |
| MICRO CODE | DON LEWINE .25E | SOFTWARE ENGR. 1E | SOFTWARE ENGR. 1E | SOFTWARE ENGR. 1E |
| MONITOR DEV | DON LEWINE .25E | DON LEWINE .5E | DON LEWINE .5E | DON LEWINE 1E |
| STANFORD SYS SPT. | STANFORD TECH .25T | STANFORD TECH .25T | STANFORD TECH .25T | STANFORD TECH .25T |
| PROTO BUILD | | | STEVE WESTON 1T | STEVE WESTON 1T |

BACK PLANE ALLOCATION

12/3/76

