NIA-XX INTERFACE SPECIFICATION

The purpose of this document is to describe
The NIA interface to the proposed
ETHERNET CSMA/CD Communication Network.

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1.0 GENERAL

The PLI interface is the means through which data transfers and communications between the port and link/packet buffers (NIA) occur. The port has a master/slave relationship with the link packet buffer combination. All data traffic and PLI functions are controlled by the port.

2.0 PLI INTERFACE SIGNALS

SIGNAL/S	DIRECTION PORT LINK	LINES	LOGIC
DATA (7:0)	<--->	8	TRI-ST
SELECT	---->	1	TTL
RCVR ATTENTION	<----	1	TTL
END OF FRAME	<----	1	TTL
XMTR ATTENTION	<----	1	TTL
PLI/LINK CONTROL	---->	4	TTL
TRANSMIT PARITY	---->	1	TTL
RECEIVE DATA PARITY	<----	1	TTL
CLOCK	---->	1	TTL
INITIALIZE	---->	1	TTL
RECEIVER STATUS	<----	8	TTL
TRANSMIT STATUS	<----	8	TTL

2.1 DATA (7:0) (Asserted High)

These lines are used to transfer data to and from the packet buffers and to pass control and status information to and from the link/buffer module. The PLI/Link control lines determine the direction and type of information being transferred.

2.2 SELECT (Asserted Low)

The select line must be asserted by the port to execute all data transfers and control functions. This line acts as an enable for the PLI/Link control lines. The link will provide a pullup resistor on this signal so that, if the port is not installed, the link will not respond to the floating control lines.

2.3 RCVR ATTENTION (Asserted High)

Receiver Attention is a PLI signal to the port. When asserted, it indicates that the receive status register contains valid status on the next frame to be unloaded from the receive buffer. It also signifies that the frame buffer addresses are available on the used buffer list.

Receive Attention is asserted when the destination address of the frame is equal to the address stored in the physical address register or the multicast bit is set in the destination address of the frame. It is cleared by the reset receive attention command.

2.4 END OF FRAME (Asserted High)

End of Frame is a signal to the port data mover. When asserted it indicates that the previous byte of data read from receive memory was the last byte of the frame. End of frame signal timing is the same as the data. The signal is asserted for one port clock cycle.

2.5 XMTR ATTENTION (Asserted High)

Transmitter Attention is signal to the port processor. When asserted it indicates that the transmit status is available on the last frame transmitted and that the transmit buffer is available for the next frame to be loaded. Transmit Attention is cleared by the read transmit status command.

2.6 PLI/LINK CONTROL (Asserted High)

There are four PLI/Link control lines originating at the port which are used to control the interface activities of the packet buffer and link. Control lines denoted by (*) utilize the data lines to pass auxilary control information to the packet buffer and link. The select line must be asserted to make the control lines valid.

The control lines are encoded as follows:

	FUNCTION		:	PLI/LINK CONTROL
1.	WT XMIT BUF	(*)	:	1100
2.	XMIT ACTION	(*)	:	0110
3.	RD XMIT STATUS		:	1101
4.	RD REC BUF		:	0010
5.	RD REC STATUS		:	1110
6.	RD USED BUF LST		:	1011
7.	REC TO XMIT BUF		:	0011
8.	RESET REC ATT		:	0111
9.	ENABLE LINK CNTL	(*)	:	1000
10.	DISABLE LINK CNTL	(*)	:	1001
11.	WT REC BUF ADRS	(*)	:	0101
12.	WT FREE BUF LST	(*)	:	0100
13.	CLR RCV BUF		:	0001
14.	WT ADRS	(*)	:	1010
15.	RD REG		:	0000
16.	WT REG	(*)	:	1111

2.6.1 WT XMIT BUF (Write Transmit Buffer) -

The write transmit buffer function will cause the data presented on the data lines and its associated parity bit to be written into the transmit buffer. The end of frame bit will always be written as a zero. The buffer address counter will be incremented at the end of each cycle in which the load transmit buffer command is present. The load transmit buffer command is necessary for each byte transfer to the packet buffer.

2.6.2 XMIT ACTION (Four Command Group). -

The transmit action command is a set of four commands whose action depend upon the state of port data bits 0 and 1. The four transmit action commands and corresponding data bit coding are:

COMMAND NAME	PORT DATA BIT 1	0
XMIT FRAME	0	0
RESET TX BUF ADRS	0	1
TX BUF DEC	1	0
WT TX EOF	1	1

2.6.2.1 XMIT FRAME (Transmit Frame)

This command informs the NIA to begin transmission of the frame stored in the transmit buffer. It also clears the transmit status register.

2.6.2.2 RESET TX BUF ADRS (Reset Transmit Buffer Address)

This command resets the transmit buffer address counter to zero.

2.6.2.3 TX BUF DEC (Decrement Transmit Buffer Address)

This command causes the transmit buffer address counter to be decremented one count.

2.6.2.4 WT TX EOF (Write Transmit Buffer End Of Frame Flag)

This command causes the end of frame bit to be written as a one into the transmit buffer at the current address of the transmit buffer address counter.

2.6.3 RD XMIT STATUS (Read Transmit Status) -

This function will enable the contents of the transmit status register onto the data lines. The transmit attention signal is cleared. The transmit status register is described later in this document.

2.6.4 RD REC BUF (Read Receive Buffer) -

This function enables the contents of the currently addressed location in the receive buffer onto the data lines. The read address counter will be incremented at the end of each cycle in which this function is asserted. The parity bit for the read data will be passed to the port with the data on the receive data parity line.

The data is available from the receive buffer sequentially from the first byte received to the last byte received.

The port must, while reading the receive packet buffer, monitor the signal "end of frame" in order to determine when

the last byte of the frame has been read.

2.6.5 RD REC STATUS (Read Receiver Status Register) -

This function will enable the contents of the receive status register onto the data lines. NOTE: The receive attention signal must be asserted in order to obtain a valid receive status. The contents of the receive status register are described later in this document.

2.6.6 RD USED BUF LST (Read Receive Memory Used - Buffer Address List).

This command will enable the first byte of the used buffer address list onto the data lines. The list contains addresses of data buffers used by the NIA during frame reception. They are provided to the port in the order that they were used by the link.

2.6.7 REC TO XMIT BUF (Transfer Byte From Receive - Memory To The Transmit Buffer).

This command causes the NIA to transfer one byte of data and its parity bit from the currently addressed location in receive memory to the currently addressed location in the transmit buffer. Both address counters are incremented at the end of each cycle this command is executed.

2.6.8 RESET REC ATT (Reset Receive Attention) -

This command will clear the receive attention signal.

When this function is executed the current receive status is lost. If there is another frame in the receive buffer, the status for that frame will be available when the receive attention signal is reasserted.

2.6.9 ENABLE LINK CONTROL/DISABLE LINK CONTROL -

These functions are used to enable and disable certain long term functions in the link and packet buffer. A particular control may be set by executing "enable link control" with a 1 in the data line bit position corresponding to that control. A control may be cleared by executing "disable link control" with a 1 in the proper bit

position. Transfers with a 0 in any bit position will have no effect.

The link control register is described later in this document.

2.6.10 WT REC BUF RD ADRS REGISTER -
(Write Receive Memory Buffer Read Address To The Read Memory Address Register).

This command causes the data presented on the data lines to be written into the receive buffer read address register. The buffer address is combined with the read-receive-memory address counter to form a fourteen bit address. All of the lower order address bits are set to zero. The port must keep track of the number of bytes written into the memory and then write a new buffer address whenever a buffer boundary is encountered.

2.6.11 WT FREE BUF LST (Write Free Buffer List). -

This command will cause the data presented on the data lines and the PLI parity bit to be written into the free buffer list. It informs the NIA of free buffers in receive memory that are available (free) to store received data packets. The NIA uses the buffer addresses in the order they were received and combines them with the write-receive-memory address counter to form a fourteen bit address.

2.6.12 CLR RCV BUF (Clear Receive Buffer). -

This command will clear the entire free buffer list, used buffer list, and receive status fifo. The command must be executed whenever a free buffer list parity error error is detected. After the execution of this command the free buffer list must be reloaded with buffer entries.

2.6.13 WT ADRS REG (Write Address Register) -

When this function is executed the data lines must contain the address of the register or buffer to be accessed. The NIA will save the address. The transfer to/from the desired register will be executed when the "rd reg" or the "wt reg" command is given.

Registers and buffers available through the address register are:

ADRS (HEX)		REGISTER/BUFFER	WT REG	RD REG
00	*	PHY ADRS REG 0	x	-
01	*	PHY ADRS REG 1	x	-
02	*	PHY ADRS REG 2	x	-
03	*	PHY ADRS REG 3	x	-
04	*	PHY ADRS REG 4	x	-
05	*	PHY ADRS REG 5	x	-
06		n/a	-	-
07		n/a	-	-
08		PHY ADRS ROM 0	-	x
09		PHY ADRS ROM 1	-	x
0A		PHY ADRS ROM 2	-	x
0B		PHY ADRS ROM 3	-	x
0C		PHY ADRS ROM 4	-	x
0D		PHY ADRS ROM 5	-	x
0e		n/a	-	-
0f		n/a	-	-
10		XMIT BUF RD	-	x
11	*	REC MEMORY WT	x	-
12		TDR REG LO	-	x
13		TDR R HI	-	x
14		COLLISION TEST REG	x	-
15		n/a	-	-
16 thru 1F		n/a	-	-

* The enable link bit in the link control register must equal zero to access these addresses.

2.6.14 RD REG (Read Register) -

This function will place the data of the register/buffer, whose address is stored in the address register, onto the data lines.

2.6.15 WT REG (Write Register) -

This function will take the data placed onto the data lines and write it into the register/buffer whose address is stored in the address register.

2.7 TRANSMIT PARITY (odd) (TTL Asserted High)

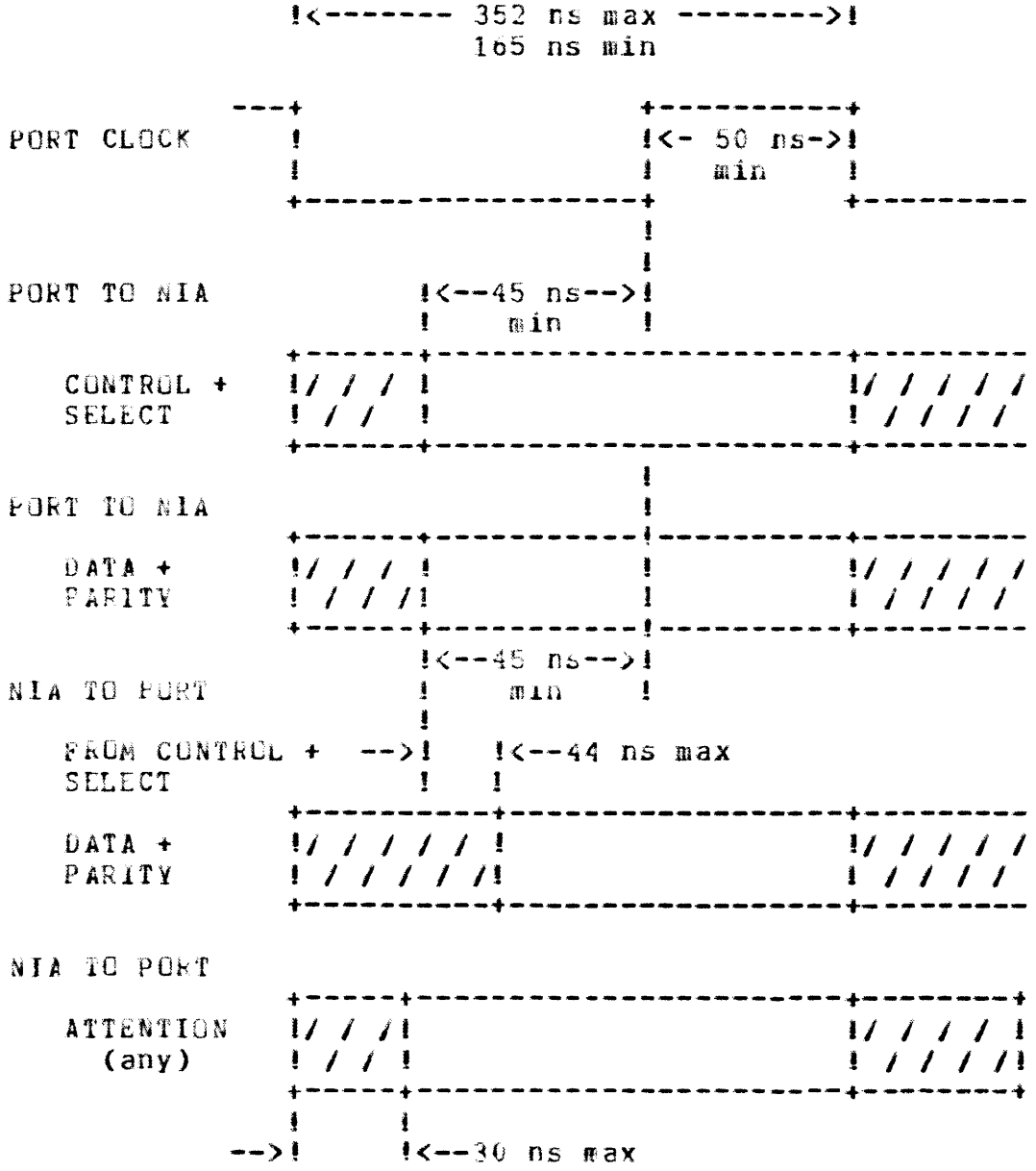
Odd parity is calculated by the port and transferred to the transmit buffer using this line. The transmit buffer will store the parity as supplied and the link will check parity when reading the buffer during a transmission.

2.8 RECEIVE DATA PARITY (odd) (TTL Asserted High)

Data being read from the receive buffer includes a parity bit which was generated before the data was written into the buffer. This parity bit will be conveyed to the port via the receive data parity line and must be checked by the port.

2.9 TIMING (PLI BUS)

The NIA interface requires a clock source from the port for its operation. The interface will operate with a minimum cycle period of 165 ns as shown below.



Note that the NIA20 can not be run at slow clock. This is due to the fact that the port must write a byte into receive memory every two port clocks. Since we are running on a 10 Megabit bus the byte is change every 800 nanoseconds. If the NIA is running at slow clock (F*72/2) the port clock is approximetly 320 nanoseconds and if a t field bit is set in the microinstruction being executed the two port clocks will be more than 800 nanoseconds causing missing bytes in memory.

2.10 INITIALIZE (TTL, Asserted high)

This signal from the port is used to initialize the link. A pullup resistor will be provided on this signal so that, if the port is not installed, the link will not interfere with the ni bus. The initialize signal must be asserted for a minimum (tbs) port clock cycles. The initialize signal must be asserted during power up and power down.

2.11 RECEIVER / TRANSMIT STATUS

These signals reflect the state of the receive and transmit status registers. They are brought out to backplane pins on the NIA link module. They are enabled with the receive and transmit attention signals.

3.0 TRANSMIT STATUS REGISTER

The transmit status register contains the necessary information:

1. For the port to determine if the link transmitted the last frame successfully.

2. For the detection of transmit errors.

3. To give some idea as to the level of activity on the medium at the time of the transmission.

All bits in this register are cleared by the PLI "initialize" signal and by the PLI/Link command "xmit frame".

The transmit status register bits are valid when the PLI signal "transmit attention" is asserted.

Transmit status register format:

7	6	5	4	3	2	1	0
TPE	CIFL	TOTL	DEF	LOCE	LCE	RB1	RB0

The transmit status register contains the following bits:

Bit

1. RB0 --- retry bit 0

2. RB1 --- retry bit 1

retry bit 1	retry bit 0	meaning
0	0	transmitted on first attempt
0	1	transmitted on second attempt
1	0	transmitted on > second attempt
1	1	failed to transmit in 16 attempts due to repeated collisions

3. LCE-late collision-When set indicates that a collision has occurred after the slot time of the channel has elapsed. In this case no retrys are attempted and the transmission is aborted.

4. LOCE-loss of carrier-When set indicates that carrier was not present on the channel during transmission. A loss of carrier will cause the transmission operation to be aborted. An end-of-frame signal will be generated and transmit status will be written.

5. DEF-defer-When set indicates that the link had to defer to existing traffic on the channel in order to transmit a frame.

6. TooTL-transmit on too long-When set indicates that the transmitter was on longer than it would take to transmit the longest valid frame. This bit is asserted after 1536 bytes have been transmitted.

7. CIF-collision input failed-When set indicates that the tranceiver failed to assert the collision heartbeat signal at the end of the frame transmission.

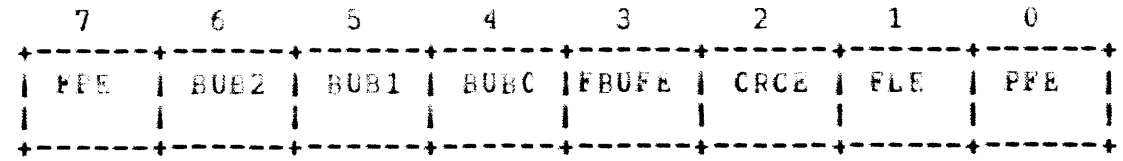
8. TPE-transmit parity error-When set indicates that the link has detected a parity error while reading data from the transmit buffer. When a parity error is detected, the remainder of the transmission is aborted.

4.0 RECEIVE STATUS REGISTER

The receive status registers are cleared by the PLI signal "initialize" or the PLI command Reset Buffers. The current receive status is lost when the PLI/Link function "reset receive attention" is executed.

The receive status register contains the neccessary information for the port to determine if the incoming frame was received and stored properly. The bits are:

receive status register format:



BIT

1. PFE-packet framing error-when set indicates that the incoming frame contained a non-integer multiple of 8 bits and the crc value at the last byte boundary was in error.

2. FLE-frame length error-when set indicates that the frame received is longer then the longest valid frame.

3. CRCE-CRC error-when set indicates that the CRC circuit calculated bad CRC on the incoming frame.

4. FBUFE-free buffer list empty, -ther set indicates that the NIA could not store or completely store the incomming frame due no buffers available from the free buffer list.

5. BUB0-buffer used bit 0

6. BUB1-buffer used bit 1

7. BUB2-buffer used bit 2

BUFFER USED FIELD---these bits indicate the number of receive buffers used tc store the received frame.

BUB 2	BUB 1	BUB 0	number of received buffers
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	n/a
1	1	1	n/a

8. FPE-free buffer list parity error-This bit, when set, indicates that the link has stopped receiving frames due to corrupt data from the free buffer list.

5.0 FREE BUF LIST

The means by which the port transfers free buffer addresses to the NIA receive memory. The free buffer list is implemented using fifo memory. It is 64 bytes deep. Free buffer addresses are written by the port, in any order, and the NIA will use them in the order given. When a buffer is filled or the end of frame is reached, the NIA transfers the buffer address from the free list to the used buffer list. The free buffer list is cleared by the PLI initialize signal or the PLI reset buffer command.

BUFFER ADDRESS FORMAT:

Receive memory organization (see link control register).

```
          7   6   5   4   3   2   1   0
        -------------------------------
        ! m ! m !   !   !   !   !   !   !
64/256  ! b ! b ! a ! a ! a ! a ! a ! a !
        ! z ! z !   !   !   !   !   !   !
        -------------------------------
              where a's = 0 - 63

        -------------------------------
        ! m ! m !   !   !   !   !   ! m !
32/512  ! b ! b ! a ! a ! a ! a ! a ! b !
        ! z ! z !   !   !   !   !   ! z !
        -------------------------------
              where a's = 0 - 31

        -------------------------------
        ! m ! m !   !   !   !   ! m ! m !
16/1024 ! b ! b ! a ! a ! a ! a ! b ! b !
        ! z ! z !   !   !   !   ! z ! z !
        -------------------------------
              where a's = 0 - 15
              note: mbz = must be zero.
```

6.0 RECEIVE BUFFER READ ADRESS REGISTER

The means by which the port selects a receive buffer to be read. (see RD REC BUF command). The buffer address is written by the port as previously read from the used buffer list. The port must count the bytes read from the NIA in order to determine buffer boundries. Buffer size is determined by the receive memory organizatior selected in the link control register. The address register is cleared by the PLI initialize signal.

7.0 USED BUFFER LIST

The means by which the port obtains the used buffer addresses from the NIA.

Up to 6 used buffer list accesses may be required per receive attention. The number of buffers used to store a frame is obtained from the receive status register.

The used buffer list format is the same as the the free buffer list format.

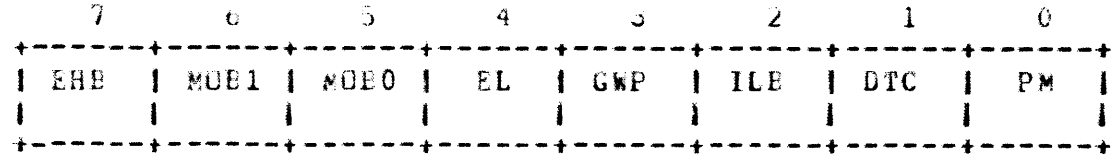
The used buffer list is cleared by the PLI initialize signal or the PLI reset buffer command.

8.0 LINK CONTROL REGISTER

The link control register bits are set and cleared as described in the enable link control/disable link control section.

Once a bit has been set it will remain set until cleared. The PLI signal "initialize" will also clear the link control register. The bits are:

link control register format:



BIT

1. PM-Promiscuous Mode-When set the link will not reject a frame because of its destination address.

2. DTC-Disable Transmit CRC-When set CRC will not be generated on outgoing frames (used in loopback mode). The CRC generator circuit is dedicated to the receiver.

3. ILB-Internal Loopback-When set internal loopback will occur when the frame is transmitted.

4. GWP-Generate Wrong Parity-When set the parity generator will generate wrong parity or the data to be written in the receive buffer.

5. EL-Enable Link-When set, allows the link to transmit or receive frames. This bit must be clear when writing the physical address ram or writing the receive memory.

6. BIT 5 MOB0 Receive memory organization select bit 0

7. BIT 6 MOB1 Receive memory organization select bit 1

MOB 1	MOB 0	BUFFER ORGANIZATION
0	0	64 buffers x 256 bytes
0	1	32 buffers x 512 bytes
1	0	16 buffers x 1024 bytes
1	1	n/a

8. ENB-Enable heartbeat-When set, the heartbeat signal is enabled. When this bit is cleared heartbeat is disabled. The heartbeat signal is unique to the H4000 transceiver and it is generated at the end of each transmission when the collision presence oscillator is turned on for a short duration. It is intended to test the collision presence circuit and its absence indicates a faulty H4000 collision sensing circuit or that the transceiver is not an H4000 model.

9.0 TDR REGISTER

BITS <09:00>: TDR: Time Domain Reflectometry. Valid only if retry or loss of carrier is set. TDR reflects the state of a counter that counts from the start of transmission to the occurrence of a collision or loss of carrier. TDR is useful in locating defective sections of cable.

100 nsclks, I think

The TDR register is accessed via the address register and is a read only register.

TDR register format:

	7	6	5	4	3	2	1	0
TDR/lo	7	6	5	4	3	2	1	0

	7	6	5	4	3	2	1	0
TDR/hi	0	0	0	0	PWR OK	0	9	8

The transceiver power status bit (PWR OK) is set to zero if the xcvr power supply voltage is equal to or greater than +11.4 volts. The xcvr power supply is nominally +15.0 volts.

10.0 PHYSICAL ADDRESS ROM

The physical address ROM contains the unique 48 bit ETHERNET port address. The ROM is readable by the port.

11.0 PHYSICAL ADDRESS REGISTER

The physical address register is used to store the physical address for NIA operation. It is used by the NIA for screening the destination address of receive data frames. The register is organized as 6 words of 8 bits each. It is writable by the port and must only be written when link enable equals zero (link disabled).

Physical Address Format:

NOTE: Both the physical address rom and physical address register have the same format.

	7	6	5	4	3	2	1	0
PAR 0	7							0
PAR 1	15							8
PAR 2	23							16
PAR 3	31							24
PAR 4	39							32
PAR 5	47							40

12.0 COLLISION TEST REGISTER

The collision test register can be utilized only in internal loopback mode. The collision test register is accessed through the write address register (address 14 hex) and the wt reg command. It is cleared by the initialize signal or by writing zeros to the two control bits. The collision test register is controlled by port data bits 0 and 1.

bit 0 Force collision bit

This bit when set will cause a collision to occur whenever the low order three bits of a transmit data byte are all ones. Note however that due to a synchronization problem between NIAC FORCE CLSN H (clocked by port clock) and NIAE 64TH BYTE L (clocked by 10 mhz clock)

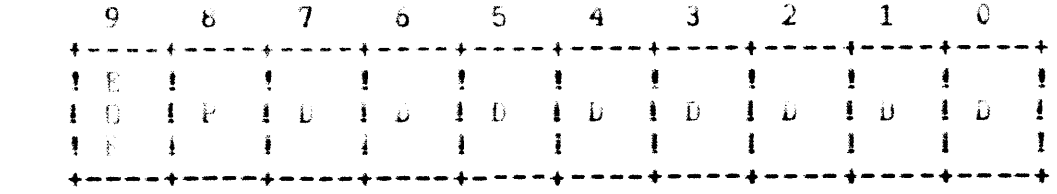
that a collision forced at byte 65 (low order bits set in 65th byte) is not guaranteed to be a late collision.

BIT 1 Preset random number generator
This bit, when set, will cause all bits in the random number generator to be all ones.

13.0 TRANSMIT BUFFER

The transmit buffer is 2048 words by 10 bits. It can store one frame at a time. The buffer is loaded by the port using the write transmit buffer command and it is read by the NIA link while transmitting the frame. Availability of the transmit buffer to the port is determined by the transmit attention signal.

TRANSMIT BUFFER WORD FORMAT.



WHERE: D = data bits
P = parity bit
EOF = end of frame bit

The write transmit buffer command causes the data, parity bit, and end of frame bit to be written into the buffer. That is, all ten bits of a transmit buffer word are written into the buffer location addressed by the transmit buffer address counter. The end of frame bit will always be written as zero with this command. At the end of the command cycle the address counter is automatically incremented one count.

The transmit action commands are used for controlling the NIA transmit functions. The four commands which are defined under PLI Interface signals are:

1. XMIT FRAME
2. RESET TX BUF ADRS
3. TX BUF DEC
4. WT TX EOF

The port should execute the WT TX EOF command -(Write Transmit Buffer End of Frame Bit)- Immediately after completion of transmit buffer data loading. The command causes the end of frame bit to be written as a one at the transmit buffer location currently addressed by the address counter.

THE XMIT FRAME -(Transmit Frame)- Command initiates the transmit function. At this time the transmit buffer should contain the frame to be transmitted with end of frame bit set (see frame format). The transmit buffer address counter is initialized by the MIA. The MIA after obtaining the line, will transmit the preamble, the complete datagram contained in the transmit buffer, and the four byte CRC field. Regardless of the success or failure of the transmit operation, transmit attention will be set and the port may read the transmit status.

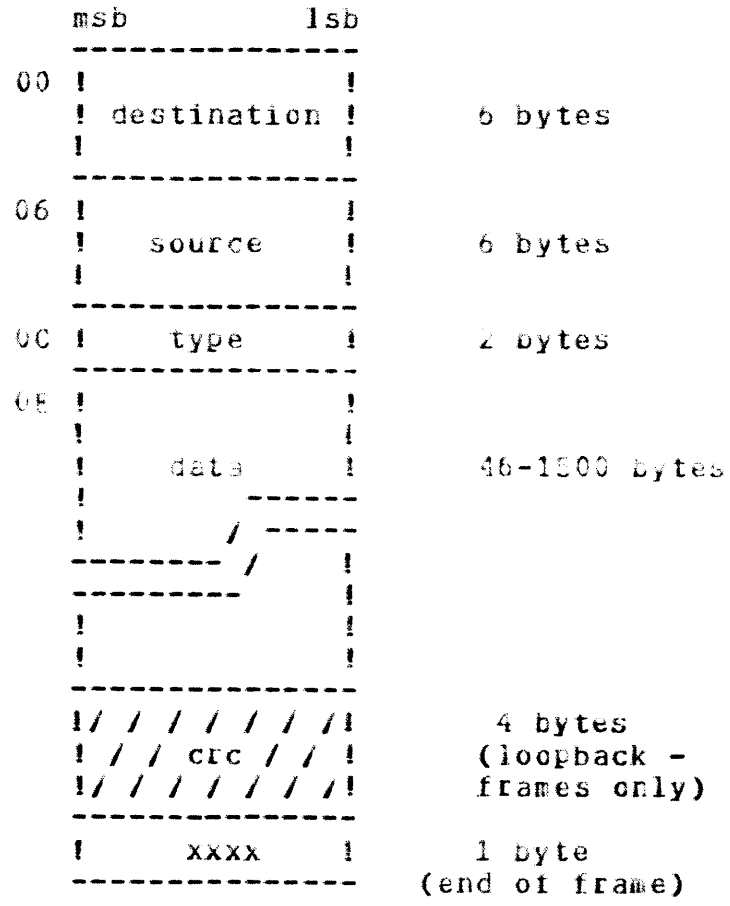
The RESET TX BUF ADRS -(Reset Transmit Buffer Address)- command initializes the transmit buffer address counter to zero. The port should insure that the counter is reset prior to loading a frame into the transmit buffer.

The transmit buffer can be read by the port. This function is useful for diagnostic purposes and while transmitting frames to oneself.

13.1 FRAME FORMAT

The transmit buffer must be loaded sequentially from the first byte of the frame to the last byte of the frame. The frames loaded into the transmit buffer by the port do not include the CRC field except for loopback frames.

The frame written into the transmit buffer must comply with the following format



13.2 PARITY

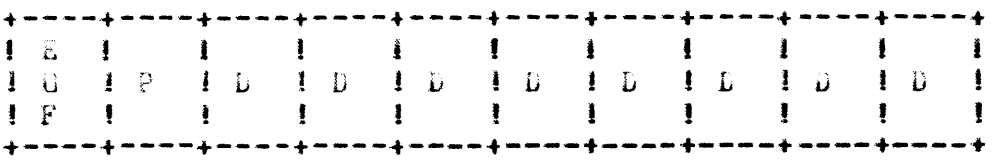
The link will check parity as the data is being read from the transmit buffer. If an error is detected, the parity error bit in the transmit status register will be set and the remainder of the transmission will be aborted.

To test the parity circuits the port must be capable of generating wrong parity when loading the transmit buffer.

14.0 RECEIVE BUFFER

The receive memory is implemented with high speed static ram and is 16,384 bytes by 10 bits. The memory is organized as 64 buffers of 256 bytes each (see note). It can store from 10 to 64 frames depending on their size. For each frame stored in the receive memory, there is a receive status byte stored in the receive status buffer and from 1 to 6 buffer addresses stored in the used buffer list. The status buffer can store as many status words as there are frames stored in the receive memory.

The receive memory word format.



Where: D = data bits
P = parity bits
EOF = end of frame bit

The receive memory requires fourteen bit addresses. The organization of receive memory which is normally 64 buffers of 256 bytes each minimizes memory management overhead by the port. The port need only specify the buffer address, with six bits at most, and the NIA will increment automatically through the byte addresses sequentially.

NOTE:
The receive memory may be optionally organized as 32 buffers of 512 bytes or as 16 buffers of 1024 bytes each. Again, the port specifies only buffer addresses and the NIA automatically increments the byte addresses. All operations remain essentially the same as for the 64 by 256 organization

For clarity, all discussion of the receive memory operation in this specification will refer to the 64 buffer by 256 byte organization.Statements relating to number and capacity of data buffers must be apropriately modified if another receive memory organization is utilized.

There are two address counters for addressing bytes in the receive buffers that are automatically incremented after a read or write operation. One counter is used for writing received data bytes into the receive buffers and the second address counter is used for reading data out of the receive buffers. These two address counters are controlled by the NIA and are used for automatically sequencing byte addresses.

After power up and/or initialization and before the NIA has begun operation, the port must specify to the NIA that all receive buffers in memory are available by writing buffer addresses to the free buffer list (FIFO). The NIA utilizes the buffer addresses in the order received from the port along with eight address bits from the write memory address counter to form a fourteen bit address for writing receive memory. During frame reception when a buffer boundry is encountered i.e.,256 bytes have been received, the NIA will transfer the current buffer address from the free buffer list to the used buffer list (FIFO) and use the next buffer address on the free buffer list to continue writing received bytes into memory. The NIA will continue in this manner until either the end of frame bit is detected or there is no more available buffer space in which case the free buffer list empty (FBLE) bit in the receive status register will be set.

Whenever the port receives receiver attention from the NIA, it must read receive status, the used buffer list addresses, and before issuing read receive buffer commands, it must specify to the NIA the receive buffer to be transferred by writing the buffer address into the receive memory read address register.

The port reads a receive buffer by writing the buffer address to the receive memory read address register and executing the "read receive buffer" command. The address counter is post incremented each time the command is executed. While reading the receive buffer, the port must monitor the end of frame bit to determine the last byte of the frame. The port must keep track of the number of bytes read out of the receive buffer. If 256 bytes have been read out and the end of frame bit was not detected, the port must write the next buffer address pointer to the memory read address register before reading more receive data bytes. When end of frame becomes asserted,the previous read command contains the last byte of the frame.

The NIA receive control does not keep track of how full the receive memory is. It is the responsibility of the port to maintain the free buffer list and to read or discard received frames. If there are no buffer addresses on the free buffer list the NIA will indicate free buffer list empty (FRELE) in the receive status.

14.1 PARITY

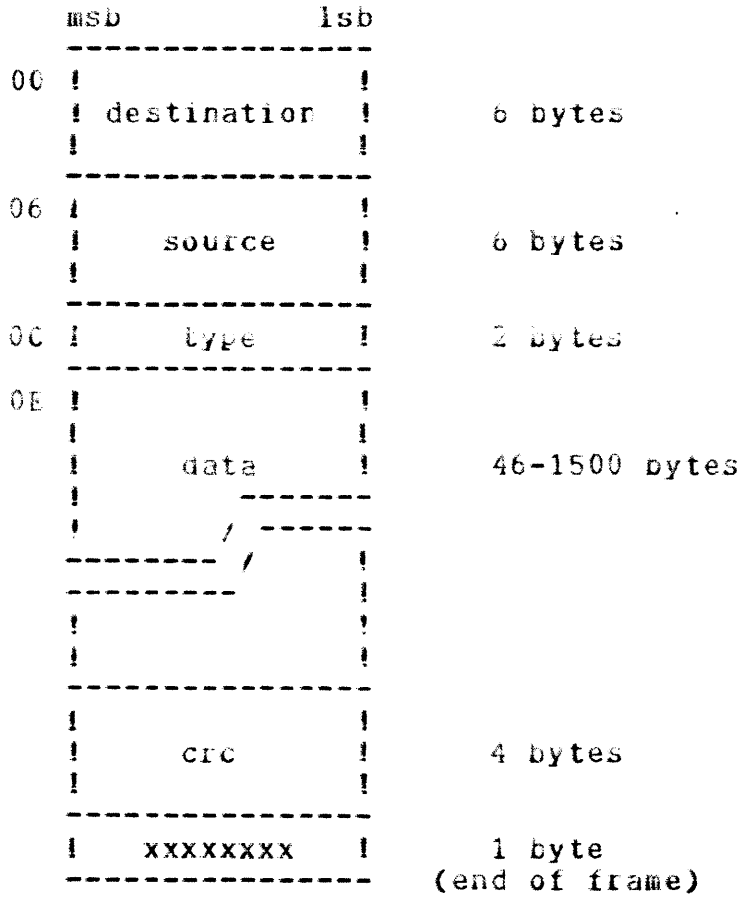
A parity bit is generated on the data prior to the receive buffer being written. The port must check the parity when reading the receive buffer. To test the parity circuits, the parity generator will generate wrong parity when the wrong parity bit is set in the link control register.

14.2 PORT WRITE TO RECEIVE BUFFER

For diagnostic purrposes the receive buffer can be written by the port when the link enable bit in the link control register is equal to one (link disabled).Note nowever the parity logic in this mode will generate incorrect parity when reading a location that was written with a data pattern containing an even number of ones. This problem is overcome in the diagnostics by expecting parity errors when reading a location that was written with an even number of ones and expecting no error when reading a location that was written with an odd number of ones.

14.3 FRAME FORMAT

When reading a frame from the receive buffer the data will be presented sequentially from the first byte of the frame to the last byte of the frame.



15.0 TRANSMITTING MULTICAST FRAMES

When transmitting multicast frames, the port must determine if this port is included in the multicast address.

If this port is not included, no additional action is required after the frame has been transmitted.

If this port is included, the frame must be read from the transmit buffer and appended with 4 bytes of 0 data (to account for the CRC) after the frame has been transmitted (transmit attention asserted).

The multicast frame will, if transmitted and received correctly, be stored in this ports receive buffer. The receive status will include a CRC error.

16.0 RECEIVING LOOPBACK TYPE FRAMES

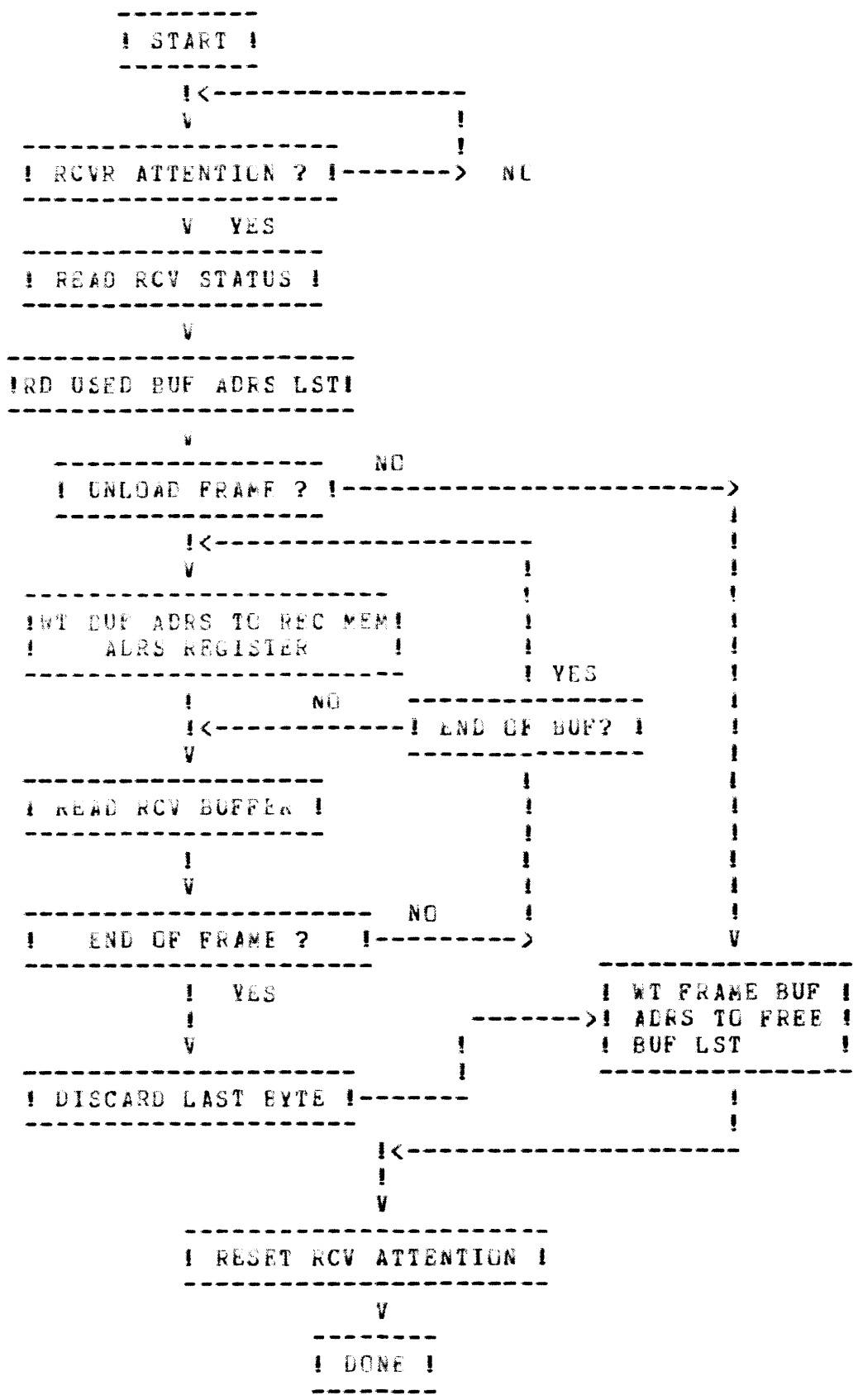
These loopback type frames are frames that are received from the NI bus and must be turned around and transmitted back to the sender.

When a loopback frame is received the port can leave it in the receive buffer until the transmit buffer becomes available. When the transmit buffer becomes available the port can move the majority of the frame to the transmit buffer using the "rec to xmit buf" command. This command allows the port to move the data at a 1 byte per cycle rate.

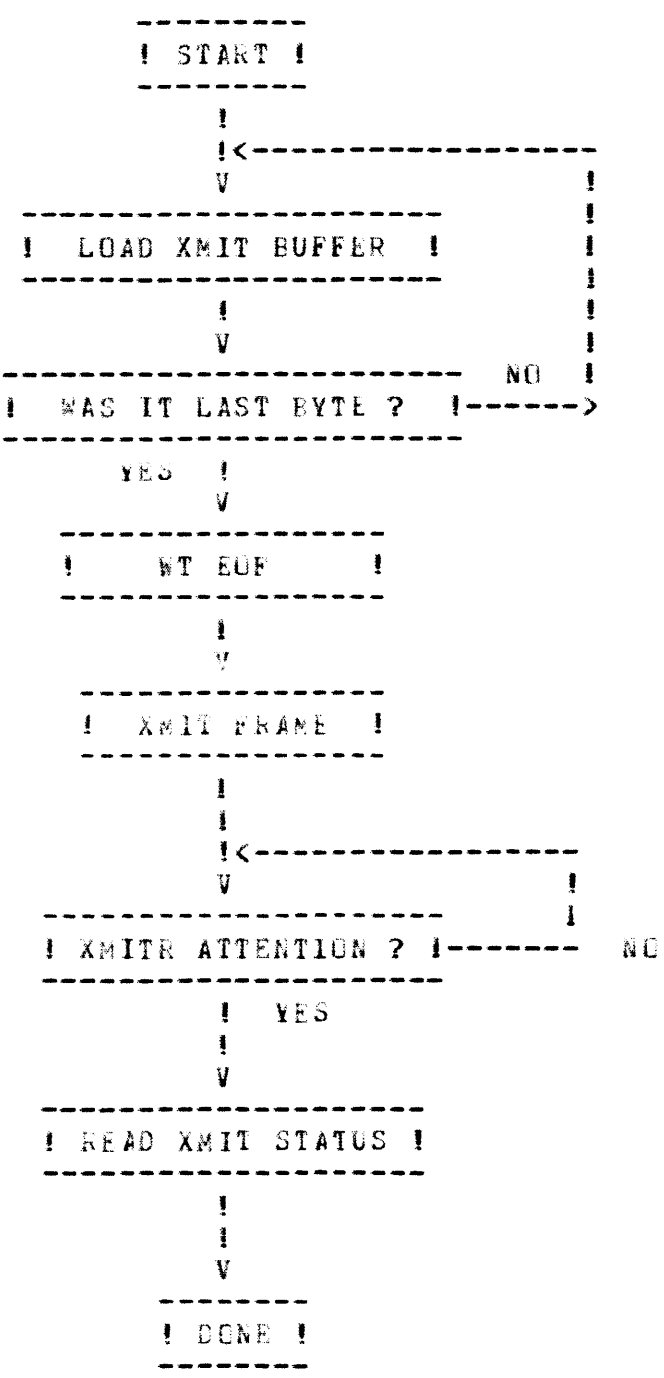
The port monitors the end of frame signal while moving the loopback frame from the receive buffer to the transmit buffer. When the end of frame signal becomes asserted it means that the loopback frame with the CRC and 1 byte of miscellaneous data have been written into the transmit buffer. At this point, the transmit buffer address counter must be moved back 5 counts before the wt end of frame and xmit frame commands are given. This is done by the port by executing the "dec xmit adrs" command for five cycles. This function is necessary to prevent the CRC from being transmitted as part of the frame.

17.0 PLI-XX INTERFACE RECEIVE SEQUENCE FLOW DIAGRAM

THE FLOW DIAGRAM IS PROVIDED TO SHOW THE STEPS NECESSARY FOR RECEIVING A FRAME. IT DOES NOT TAKE INTO CONSIDERATION THE OPTIMAL USE OF THE FREE BUFFER LIST AND USED BUFFER LIST.


START
RCVR ATTENTION ?
NO
YES
READ RCV STATUS
RD USED BUF ADRS LST
UNLOAD FRAME ?
NO
WT BUF ADRS TO REC MEM ADRS REGISTER
YES
END OF BUF?
NO
READ RCV BUFFER
END OF FRAME ?
NO
YES
DISCARD LAST BYTE
WT FRAME BUF ADRS TO FREE BUF LST
RESET RCV ATTENTION
DONE

18.0 PL1-XX INTERFACE TRANSMIT SEQUENCE FLOW DIAGRAM



19.0 NI-LINK MODULE FINGER PIN SIGNAL ASSIGNMENTS

NOTE: SIGNAL NAMES GIVEN IN PARENTHESIS ARE THE NI-LINK MODULE SIGNAL NAME ONLY. ALL OTHERS ARE THE BACKPLANE SIGNAL NAME USED ON THE JUPITER SYSTEM.

I/O PINS

PIN	PREFIX	POS	TYPES	SIGNAL NAME
A1	NIA			NC
A2	NIA		TIG	GND
A3	NIA		TIV	+5.0V
A4	NIA		TIV	+5.0V
A13	NIA		TIG	GND
A16	NIA		TIG	GND
A23	NIA		TIG	GND
A33	NIA		TIG	GND
A43	NIA		TIG	GND
A51	NIA		TIG	GND
A61	NIA		TIG	GND
A72	NIA		TIG	GND
A79	NIA		TIG	GND
A82	NIA		TIG	GND
A86	NIA			(B,NC,GND)
A90	NIA			(B,NC,+15.0V)
A91	NIA		TIV	+5.0V
A92	NIA		TIG	GND

==========

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B1	NIA	TIG	GND
B3	NIA	TIV	+5.0V
B4	NIA	TIV	+5.0V
B13	NIA	TIG	GND
B16	NIA	TIG	GND
B20	NIA	TOI	PORT (S,,(N))DATA 0 H
B21	NIA	TOI	PORT (S,,(N))DATA 1 H
B22	NIA	TOI	PORT (S,,(N))DATA 2 H
B23	NIA	TIG	GND
B24	NIA	TOI	PORT (S,,(N))DATA 3 H
B25	NIA	TOI	PORT (S,,(N))DATA 5 H
B26	NIA	TOI	PORT (S,,(N))DATA 4 H
B27	NIA	TOI	PORT (S,,(N))DATA 7 H
B28	NIA	TOI	PORT (S,,(N))DATA 6 H
B31	NIA	TI	LINK (S,,(N))CONTROL 0 H
B32	NIA	TI	LINK (S,,(N))CONTROL 1 H
B33	NIA	TIG	GND
B34	NIA	TI	LINK (S,,(N))CONTROL 2 H
B35	NIA	TI	INITIALIZE (S,,(N))B
B36	NIA	TI	LINK (S,,(N))CONTROL 3 H
B37	NIA	TI	
B46	NIA	TIV	+5.0V

```
        B47     NIA             TIV     +5.0V
        B61     NIA             TIG     GND
        B63     NIA             TI      ILIL [S,,[N] ]XMIT STATUS 0 H
                                        (SB7 H)
        B64     NIA             TI      ILIL [S,,[N] ]XMIT ATTENTION (1)H
                                        (XMIT ATTENTION (1) H)
        B71     NIA             TI      PORT [S,,[N] ]CLK H
        B72     NIA             TIG     GND
        B79     NIA             TIG     GND
*       B88     NIA             TI      [,NC,PLI [S,,[N] ]END OF FRAME H]
                                        (END OF FRAME H)
        B90     NIA             TIG     GND
        B91     NIA             TIV     +5.0V
        B92     NIA             TIV     +5.0V
        B93     NIA             TIG     GND
        B94     NIA             TIG     GND

================================================================

================================================================

        C1      NIA             TIG     GND
        C2      NIA             TIV     +5.0V
        C4      NIA             TIV     +5.0V
        C5      NIA             TI      [B,,PLI ]INITIALIZE [S,,[N] ]H
        C6      NIA             TI      -PLI [S,,[N] ]SELECT H
        C7      NIA             TI      [B,,PLI ]LINK [S,,[N] ]CONTROL 0 H
        C8      NIA             TI      [B,,PLI ]LINK [S,,[N] ]CONTROL 1 H
        C9      NIA             TI      [B,,PLI ]LINK [S,,[N] ]CONTROL 2 H
        C10     NIA             TI      [B,,PLI ]LINK [S,,[N] ]CONTROL 3 H
        C11     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 0 H
        C12     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 1 H
        C14     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 3 H
        C15     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 4 H
        C16     NIA             TIG     GND
        C17     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 6 H
        C18     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 7 H
        C19     NIA             TI      PLI [S,,[N] ]TRANSMIT DATA PAR H
                                        (XMIT PARITY H)
        C20     NIA             TI      PLI [S,,[N] ]RECEIVE DATA PAR H
                                        (L RCV PARITY H)
        C21     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 5 H
        C22     NIA             TOTI    [B,PORT,PLI] [S,,[N] ]DATA 2 H
        C23     NIA             TIG     GND
        C24     NIA             TI    [B,PORT [S,,[N] ]CLK,PLI [S,,[N] ]CLK] H
        C25     NIA             TI      PLI BUSE BUFFER B H
                                        (PFE H)
        C26     NIA             TI      PLI [S,,[N] ]XMTR ATTENTION (1)H
        C27     NIA             TI      RCVR BUF A FULL H
                                        (REC ATTN)
        C28     NIA             TI      PLI RCVR BUF B FULL H
                                        (FLE H)
----------------------------------------------------------------
        C28 TO BECOME [B,NC,PLI [S,,[N] ]END OF FRAME H]
----------------------------------------------------------------
```

	C31	NIA	TI	PLI FIRST BUFF H (CRCE H)
	C32	NIA	TI	PLI BUSE BUFFER A H (FBUFE H)
	C33	NIA	TIG	GND
	C35	NIA	TI	PLI CRC ERR H (LCE H)
	C37	NIA	TOTI	XMTR CS,,CN] IBUSY H (FPE H)
	C38	NIA	TI	ACK CS,,CN] IH (LCC H)
	C41	NIA	TI	XMIT CS,,CN] IABORT H (DE H)
	C42	NIA	TI	CDA CS,,CN] IH (SB5 H)
*	C43	NIA	TI	PLI CDB H (CIF H)
	C44	NIA	TI	XBUF CS,,CN] IPE H (TPE H)
	C45	NIA	TIV	-5.2V
	C46	NIA	TIV	-5.2V
	C47	NIA	TIV	-5.2V
	C48	NIA	TIG	GND
	C51	NIA	TOTI	CDB CS,,CN] IH (CIF H)

```
!       THE FOLLOWING PINS ARE THE CONNECTOR FOR THE BACKPLANE  !
!       TO BULKHEAD TRANSCEIVER CABLE.                          !
```

C53	NIA	Z	SHIELD
C54	NIA	TWP1	RX DATA IN [N] H
C55	NIA	-	RESERVED
C56	NIA	TWP2	-RX DATA IN [N] H
C57	NIA	-	RESERVED
C58	NIA	-	RESERVED
C59	NIA	TWP1	DET [N] H
C63	NIA	-	FREE
C60	NIA	TWP1	CLSN DET [N] H
C61	NIA	TIG	GND
C62	NIA	TWP2	-CLSN DET [N] H
C64	NIA	-	CB,-DET H,POWER RETURN XCVR [N] NEG]
C65	NIA	-	POWER XCVR [N] POS
C66	NIA	TWP1	TX DATA OUT [N] H
C67	NIA	-	POWER RETURN XCVR [N] NEG
C68	NIA	TWP2	-TX DATA OUT [N] H

```
!       END BACKPLANE TO BULKHEAD CABLE PINS.                   !
```

C72	NIA	TIG	GND
C79	NIA	TIG	GND
C81	NIA		LB,NC,ALAPTER LS,,[N]]CODE 0 H]
C83	NIA		LB,NC,ALAPTER LS,,[N]]CODE 1 H]
C85	NIA		LB,NC,ALAPTER LS,,[N]]CODE 2 H]
C87	NIA		LB,NC,ALAPTER LS,,[N]]CODE 3 H]
C89	NIA	TIV	-5.2V
C90	NIA	TIV	-5.2V
C91	NIA	TIV	+5.0V
C92	NIA	TIV	+5.0V
C94	NIA	TISG	GND

20.0 TRANSCEIVER CABLE CONNECTORS

THE CONNECTORS USED AT THE ENDS OF THE TRANSCEIVER CABLE SHALL BE 15 CONDUCTOR 'D' SUBMINIATURE TYPES (CINCH TYPE DASM-15). THE END OF THE CABLE THAT MATES WITH THE TRANSCEIVER MUST USE A FEMALE CONNECTOR WITH A SLIDE LOCK ASSEMBLY (CINCH TYPE DA 51220-1 OR EQUIVALENT). THE TRANSCEIVER MUST PROVIDE A MATING MALE CONNECTOR WITH LOCKING POSTS. THE OTHER END OF THE TRANSCEIVER CABLE (WHICH MATES WITH A FEMALE CONNECTOR AT THE STATION) MUST USE A MALE CONNECTOR WITH LOCKING POSTS (CINCH TYPE D 53018 OR EQUIVALENT). THE STATION MUST PROVIDE A FEMALE CONNECTOR WITH THE SLIDE LOCK ASSEMBLY.

20.1 TRANSCEIVER CABLE CONNECTOR PIN ASSIGNMENT

THE PIN ASSIGNMENT IS GIVEN IN THE FOLLOWING TABLE:

1.	SHIELD (SEE NOTE)		
2.	COLLISION PRESENCE +	9.	COLLISION PRESENCE -
3.	TRANSMIT +	10.	TRANSMIT -
4.	RESERVED	11.	RESERVED
5.	RECEIVE +	12.	RECEIVE -
6.	POWER RETURN	13.	POWER
7.	RESERVED	14.	RESERVED
8.	RESERVED	15.	RESERVED

NOTE: SHIELD MUST BE TERMINATED TO CONNECTOR SHELL AS WELL AS PIN 1.