Emerging Technologies Multi/Parallel Processing

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ABSTRACT

Corporate Research and Architecture sponsored a project in 1984 to collect information on emerging multi/parallel processors. The report, published by this author, contained company/product profiles on 45 companies broken out into a number of different categories. Since that time, a lot of activity in multi/parallel processing has taken place. This report, "Emerging Technologies: Multi/Parallel Processing," provides updated company/product profiles for those players in the scientific/engineering market and includes some analysis of what has happened since 1984.

EXECUTIVE SUMMARY

Emerging Technologies: Multi/Parallel Processing is an update of a report published in January 1985 which profiled multi/parallel processing companies. This report provides updated profiles of companies/products in the scientific/engineering market in the following categories: multi/parallel processors, massively parallel processors, nearsuper uniprocessors, personal supercomputers, IBM, and other major computer companies. This report also includes some analysis of how this market has changed since 1984. Company/product material has been taken from public sources of information. The following findings are discussed further in the Analysis section.

- The number of companies competing (or will be competing) for market share in the scientific/engineering area has increased from about 12 to 26.
- A new class of machine, the massively parallel (characterized for this report as being able to connect 100 or more CPUs), has become available to the market. It has also dramatically changed the number of CPUs that can be connected since the largest configurations for smaller multi/parallel processors are 30-40 CPUs.
- Some larger companies, such as Perkin-Elmer and Bolt, Beranek & Newman, have created spin-offs to focus on multiprocessing efforts.
- Some companies have gone out of business already while one has been acquired.
- Most of the first start-ups have recently issued initial public stock offerings.
- Strategic alliances are being created between these companies and other, more established companies. In some instances, liaisons are being created among themselves. Sun, Apollo, and Silicon Graphics lead in number of alliances created with these companies. Alliances are being created with U.S., European, and Japanese companies. These alliances are enabling companies to offer more of a total solution rather than just a system.
- Revenue for 1986 has been estimated to be approximately \$505.9M compared to \$314.1M for 1984. Units installed to date have risen from 330 to 1521.

- Some leaders have emerged. Concurrent, Floating Point, Sequent, Convex, and Alliant have installed bases of over 100 machines. BBN and NCube lead the massively parallels in installations with 85 and 60 respectively.
- Competition in Europe should intensify as a number of companies expand their efforts to concentrate on the European market.
- Those few companies that have only uniprocessor machines may move toward multiprocessor versions.
- No one predominant chip but rather a variety of chips are being used for these systems: proprietary, Motorola, National Semiconductor, Intel, and Transputer. Dana has been the only company to indicate that it will use a RISC chip from MIPS.
- A variety of system connection methods now exists, rather than a standard bus. Bus speeds have not changed much since introduction of products with the exception of Sequent which introduced a faster bus in 1986. Bus speeds range greatly.
- Many companies have incorporated vector processing rather than relying solely on multi/parallel processing to increase performance. Some are using very long instruction words for greater speed.
- Most companies offer a version of Unix for their operating system. Those that offer a proprietary system are shifting to some form of Unix. They either continue to offer the proprietary system as well or have dropped it completely.
- Many companies are making their machine as VAX-compatible as possible.
- Fortran and C are still the dominant languages being offered.
- Demand for third-party applications is increasing. Most recent announcements concern support of database management packages.
- Some companies have recently cut prices on their product for the first time as they prepare to announce second generation products. Sequent and Encore have already announced their second product line.
- Digital's customer base has been the target for many of these companies. This has been a key marketing strategy which some, Convex in particular, have quite aggressively stated and pursued. While most still target the scientific/engineering area, some are now shifting to markets in the business area. Sequent and Encore both are shifting away from scientific/ engineering areas to business area.
- IBM and most other major companies do not have product in the minisupercomputer area. IBM offers a vector facility to attach to its 3090 mainframes. Gould recently announced the NPL family of vector/scalar minisupercomputers. Prime will jointly market Cydrome's processor.

6 EXECUTIVE SUMMARY

I. ANALYSIS

Corporate Research and Architecture sponsored a project in 1984 to collect information on emerging multi/parallel processors. The report, published by this author, contained company/product profiles on 45 companies. These 45 companies were categorized as follows: Multi/parallel processors, supercomputers, fault tolerant computers, array processors, Japanese supercomputers, and "Other."

A lot of activity in multi/parallel processing has taken place since 1984. This report, "Emerging Technologies: Multi/Parallel Processing," updates the 1984 report, however, it focuses only on those companies in the multi/parallel processor category. Companies have been grouped as follows:

- 1. Multi/Parallel
- 2. Massively Parallel
- 3. Near Super Uniprocessors
- 4. Personal Supercomputers
- 5. IBM
- 6. Other Major Computer Companies
- 7. Companies that have gone out of business

Information is current as of October 1987 and has been obtained from public sources.

The near super uniprocessor category has been included because the companies mentioned (Convex, Scientific Computer and Supertek) have vector processing capability and compete or will compete for market share with the multi/parallel processors in the engineering/scientific marketplace.

The following analysis consists of five sections. Section A, The Players, focuses on general aspects of these companies while Section B talks about product. Section C mentions efforts of IBM and Other Major Computer Companies. Section D. Why Success? Why Failure?, is an attempt to look at some companies and address why they have been a success or a failure. Section E, Future Directions, speculates on what might happen during the next few years.

Most of the analysis excludes IBM and other major computer companies, except where noted, since they are discussed in separate section.

What has happened since 1984?

A. The Players

1. Number and Status

The quickest reflection of growth in this area shows in the number of companies that have or will have product. The 1984 report profiled twelve companies:

Multi/Parallel	Minisupercomputer
Denelcor	Convex
Elxsi	Scientific Computer
Encore	-
Flexible	Other
IBM	Dataflow*
Sequent	Intel
•	Perkin-Elmer
Array	
Floating Point	

(*Alliant. Name was changed from Dataflow in 1985. There had been a rumor in 1984 that Dataflow was having trouble building its boards. It was questionnable whether or not the company would be able to get its product off the ground.)

Today the number of players in each category looks like this:

Multi/Parallel	16	Out of Business	3
Massively Parallel	6		
Near Super Uniprocessor	3		
Personal Supercomputers	2		
Total	27*		

(Refer to the Table of Contents for companies represented in each category.)

*Floating Point has been included in two categories since it sells products which have been classified as Multi/Parallel and Massively Parallel. Table 1 compares the status of companies from 1984 to June 1987 (includes IBM).

TABLE 1 STATUS

<u>.</u>	Number of Companies	
	1 9 84	1987
Total reported	12	29
Shipping product	7	19
To Ship	5	7
Closed	0	3*
Purchased	0	1
Public	5	15

*Culler's assets, not the company, were purchased by Saxpy and so is included in the "Closed" category.

Some of the larger companies which offer a variety of products chose to focus more attention on their multi/parallel products by creating spin-offs. Concurrent (parent -Perkin-Elmer) and BBN Advanced Computers (parent - BBN) were both formed to develop and market products in this area. BBN's Butterfly product had been primarily for the government market, however, the goal of BBN Advanced Computers is to commercialize the product. Both Concurrent and BBN Advanced Computers sought outside sources of funding. Concurrent had its own stock offering and BBN recently created a \$32M limited partnership with Paine Webber. Although not spun-off into a separate entity, Intel created the Scientific Computer Division to concentrate on the iPSC hypercube work.

Three companies have closed: Culler Scientific Systems, Denelcor, and Vitesse (computer products division). For further information on why these companies closed see Section IV - Why Success? Why Failure?

Elxsi is the only company to have been purchased by another company. Trilogy bought the company in 1986 infusing much-needed cash into Elxsi.

2. Funding

As noted in Table 1, 15 of the 26 existing companies are public while 11 are private. The investment community has raised over \$410M in funding for these companies since they began. That figure does not include money companies have received through their initial public stock offerings.

Companies that have gone public since 1984 include:

Alliant	Elxsi
Convex	Encore
Concurrent	Sequent

10 A. The Players

Concurrent is placed in this category because it was spun-off from P-E in 1985 and shortly followed with an initial public stock offering.

Alliant, Convex, and Sequent have all gone public since October 1986. Sequent has just completed its offering. Encore was first of this group to have gone public, doing so with no product in the market, unlike the others.

Private companies include:

Cydrome	Thinking Machines
International Parallel	Scientific Computer
Meiko (British firm)	Supertek
Multiflow	Dana
NCube	Stellar

Possible initial public stock offerings:

mid-1988 - Scientific Computer (timing of their offering continues to be pushed back) 1988 - Ncube 1988-89 - Cydrome

The three companies that went out of business were all privately held.

One interesting note: NCube is the only company not to have gone to the investment community for any funding during its lifetime. Shell Oil owns 5% of the company but the rest of the company is still controlled by the owners and original investors. It remains a small company with only 20 employees yet its last six quarters have been profitable and, in the massively parallel category, it has the second highest number of machines installed.

3. Strategic Alliances

Alliances, through a variety of agreements, are forming between these companies and other major computer companies as well as between themselves in one case. Two examples of these alliances include those with workstation vendors Sun and Apollo and those with graphics vendor Silicon Graphics.

Benefits from these alliances differ for the newer and more established companies. Newer companies have the chance to tap into new markets and an established customer base via an established sales force. They are also able to offer a more complete solution as opposed to just a single computer. More established companies are also able to take advantage of the opportunity to offer a more complete solution thus enabling both new and more established companies to compete more strongly against Digital and IBM. In the cases of Sun and Apollo, both are offering compute servers with their workstations. These companies benefit by quickly filling holes in their product lines, if necessary. Sometimes those relationships have not worked out as satisfactorily as hoped. Alliant has just altered its relationship with Apollo because Alliant had been hoping to capitalize on Apollo's European presence to bring European sales to Alliant. Sales were not what Alliant had anticipated so Alliant has created its own European subsidiary. Culler was not able to capitalize on its relationship with Sun to increase Culler's sales. Relationships are not limited to U.S.-based companies either. These alliances are being created with European and Japanese companies as well. Table 2 outlines some alliances created to date.

TABLE 2STRATEGIC ALLIANCES

U.S.		Type of Agreement
Apollo	Alliant Concurrent Convex Multiflow	OEM Joint Marketing and Sales Joint Marketing Joint Marketing and Development
Sun	Alliant Convex Culler	Joint Marketing and Development Joint Marketing and Development Joint Marketing
Silicon Graphics	Alliant Convex Cydrome	Joint Marketing Joint Marketing and Development Joint Sales and Service
Boeing Computer Services	Scientific Computer	Joint Marketing and Sales
Sky Computer	Elxsi	Joint agreement to integrate vector pro- cessing into Elxsi systems
MAI Basic	Sequent	Joint Development
Convex	Stellar Cray	Technology Swap and Joint Marketing Cross-licensing agreement
Prime	Cydrome	Joint Marketing and Development Investment funds from Prime
Digital	Floating Point	Agency Agreement (joint marketing and sales)
JAPAN		
Kubota Ltd.	Dana	Manufacturing and Marketing deal Investment of \$20M in Dana
Nippon Steel	Concurrent	Joint venture
EUROPE		
Siemens	Sequent	Joint product development and OEM
Matra Datasystems	Encore	Joint product development

4. Sales

a. Revenue/Units Installed

Convex predicted in 1984 that it would be a \$100M company by 1986. Encore expected to be more than \$35M. However, reality fell short of predictions. Convex actually brought in \$40M in 1986. Encore has yet to have a profitable quarter. What does the overall picture look like for these companies? Analysts are predicting a \$1B market by 1990. How close are they to this figure? Table 3 compares revenue from 1984 to 1986 and units installed from 1984 to June 1987.

Revenue	1984 \$314.1m	1986 \$505.9m
	1984	June 1987

TABLE 3REVENUE/UNITS INSTALLED

Notes:

- Revenue figures are based on company's fiscal year.
- Revenue figures, if not known, are based on best-guess estimates using an average (or best-guess) sales price.
- All machines installed may not have been revenue machines.
- A reminder that IBM and other major computer companies are not included in these figures.

The massively parallel (100 or more CPUs) portion of the market includes 213 units installed with 1986 revenue of approximately \$40.3M.

Who are the leaders? Table 4 ranks companies by number of units installed (cutoff of 50 units).

TABLE 4 RANKING BY INSTALLATION

Multi/Parallel		
350		
300		
164		
163		
142		
70		
59		

BBN Advanced Computer85NCube60

Massively Parallel

Table 5 lists those companies which have either profitable quarters or years. The quarter in parenthesis indicates the first profitable quarter for these companies. The companies listed are those whose major source of revenue comes from its computers.

TABLE 5 PROFITABILITY

Yearly

Quarterly

Alliant (4Q85) Convex (4Q85) FPS (loss 1986) Masscomp (1985) NCube (last six quarters) Elxsi (1Q87) Sequent (2Q86)

b. European Sales

Expect competition to intensify in Europe. These companies are expanding their efforts to concentrate on the European market. Three of the leaders have just taken actions to strengthen their positions there.

Alliant recently announced the decision to create a European subsidiary to be headed up by John Harte, former Vice President of Marketing and Sales with Floating Point. Alliant had depended on an alliance with Apollo to bring in European sales but that arrangement did not work out.

Sequent decided to create a European subsidiary to be headquartered in Amsterdam. Amsterdam will also serve as a European development center for parallel processing technology. A training center has been opened in Britain and operations are to be established for each major European country, with new centers in Paris and Munich.

Convex has been devoting effort to line up OEMs and opening new offices in Europe.

14 A. The Players

B. The Product

1. CPUs

The number of CPUs that can be connected has increased with the introduction of the massively parallel processors from:

Ametek	Intel
BBN	NCube
Floating Point	Thinking Machines

Thinking Machines' largest configuration connects 64,000 processors. The largest configurations offered by non-massively parallel processors are those of Sequent (30 CPUs) and Flexible (40 CPUs). The majority of massively parallels are found in university and government settings, however, more are finding a place at commercial sites. The largest configurations, with the exception of NCube (1024 processors), for these machines have yet to be ordered. Shell Oil will be upgrading its NCube to a 1024 processor system over time.

Some of the uniprocessor companies have made moves to multiprocessors. Convex announced multiple processor configurations in October 1986. Scientific Computer has a dual processor development effort going on in-house which may or may not be introduced as a new product.

2. Chip

A variety of chips are used for these machines. A few companies such as Elxsi, Ncube, and Convex use proprietary chips. Most other companies use Motorola 68020 and NS 32032. Encore is the first company to use the new NS 32332 in its machines. Sequent is the first to use the new Intel 80386. Floating Point (T Series), Kodak, and Meiko use the Transputer.

Although some machines offer RISC-like features, only one company has announced intentions to use a RISC chip. Dana will be incorporating a RISC chip from MIPS, probably MIPS' new 16-MHz chip.

3. Bus

Bus speeds have not changed since companies introduced their product with their proprietary buses. The exception is Sequent which brought out a new bus in 1986 with an effective speed of 53 MB/sec., theoretical speed of 80 MB/sec. The old bus's effective speed was 26.7 MB/sec., theoretical speed of 40 MB/sec.

The personal supercomputer companies Dana and Stellar have announced that their bus speeds will be several hundred MB/sec. (Dana) and 80-120 MB/sec. (Stellar). Multiflow's bus operates at 492 MB/sec. Convex's new fiber optic interconnect operates at 80 MB/sec.

Processors are also being connected in other ways. Massively parallel processors use a hypercube configuration to connect individual processors into one large scheme. These individual processors include individual memories as opposed to one large shared memory. BBN's Butterfly connects processors via a switch connection. Loral utilizes a data-flo architecture to connect processors.

4. Vector Processing

Rather than relying solely on multi/parallel processing to provide increased performance, many companies also use vector processing. The following companies offer vector processing now:

Alliant	Intel
Convex	International Parallel
Floating Point - T Series	Scientific Computer
IBM	

These companies plan to offer vector processing:

Dana	Stellar
Flexible	Supertek
Elxsi	_

The manner in which the vector processing is provided differs. Alliant, Convex, Floating Point T Series, SCS, and Supertek have incorporated the vector processing into the architecture. Dana has designed its own 64-bit vector processors which will work in parallel on a bus. Stellar will also incorporate vector processing into its architecture.

IBM and Intel both offer vector facilities which can be added to the 3090 and iPSC computers respectively. Elxsi will provide vector processing via a board from Sky Computer. Flexible was to have been developing an add-on vector accelerator. International Parallel claims that its system "can be programmed to act like a vector processor by allowing the master processor to synchronize slave processors so that they can all process different datastreams simultaneously."

Cydrome and Multiflow both process faster using very long instruction words rather than using vector processing. Cydrome calls its approach a modified data-flow.

5. Operating System

Most of the companies profiled in this report have a version of Unix as their operating system. Companies which offered a proprietary operating system have moved away from that proprietary system to a version of Unix.

16 B. The Product

Three companies, Floating Point, Meiko and Eastman Kodak, are using Occam. Floating Point uses it for its T Series. However, FPS has decided this is not a successful strategy and is preparing to implement a version of Unix.

Many of these companies are making their machines as VAX-compatible as possible making migration from a VAX to these machines much easier for the user. This includes VAX-compatible shells. Elxsi, for example, has incorporated VMS-like features into its operating system and offers a group of software products that allow users of VMS to migrate easily to Elxsi's hardware. Convex has its own VAX-compatible shell. Companies also offer VAX-compatible Fortran and C.

6. Languages

Table 6 indicates the number of companies that offer/will offer what languages. Fortran and C are the most popular. Ada, usually a version from Verdix, is being introduced as more companies try to compete for government contracts. FPS offers Occam and Stellar is the only company to mention Prolog as a potential offering.

TABLE 6 LANGUAGES

	Offer	Will Offer	Total
Fortran	18	5	23
C	17	2	19
Pascal	8	2	10
Ada	7	4	11
Lisp	6	2	8
Cobol	6	-	6
Basic	4	-	4
Occam	1	-	1
Prolog	-	1	1

7. Third-Party Applications

The demand for third-party applications continues to increase. Listed below is some information on how many packages some companies are offering and new fields on which they are concentrating:

Alliant	64 120 by year-end 1987 Newest area: visualization (3-D computer graphics, image process- ing, animation)
Convex	140200 by year-end 1987Newest areas: computational chemistry; design, test and manufacturing integration; animationAgreement with Polygen for molecular simulation and modeling
Concurrent	Increasing software development effort because of need for soft- ware to use on Concurrent's proprietary operating system
Cydrome	8 in CAD/CAM, computational fluid dynamics
Dana	Working to get third-party application packages in the following target areas: mechanical CAE, computational fluid dynamics, computational chemistry
Encore	Trying to encourage third-party software development
SCS	50, mainly in structural analysis and computational chemistry

A recent round of announcements for support of database management packages came from the following companies:

Oracle - Convex, Elxsi, Encore, Sequent Relational Technology - Elxsi, Sequent INGRES - Elxsi

8. Pricing

Some companies have had price cuts since their products first came out. Some cuts came when a new product was introduced. Other cuts are taking place prior to new product introduction. Sequent lowered its price on the Balance when the Symmetry series was announced this spring. Convex and Alliant have both lowered their prices recently in anticipation of second generation product to be brought out. Convex price cuts came on the CPU and memory while Alliant's cuts only came on memory. Alliant has also just introduced the FX/4, an interim product. Elxsi is said to be revising its prices. Elxsi had changed its pricing in December 1986 to encourage purchase of multiple CPU systems.

C. IBM and Other Major Computer Companies

(AT&T, Data General, Gould, Honeywell, Prime, Unisys)

The emphasis of this report has been on newly formed companies and their products. However, there is some research effort going on at IBM and other major computer companies in the multi/parallel area. Gould and IBM are the only companies to have announced a product in this category. The other companies have not indicated plans for a commercial product.

<u>IBM</u> has several groups of computers that operate with more than one processor. The 3090 series is the most powerful of these groups. IBM began regular shipments of the 3090-600E, a six-processor version, in July 1987. There had been speculation that an eight-processor version might become available. However, that may no longer be the case.

IBM's 3090 Vector Facility, announced October 1985, was installed by 100 customers during 1986.

IBM also has several projects in-house to learn about parallel processing. IBM has no public plans for immediately coming out with a strictly parallel processor.

<u>Gould's</u> NPL family of vector/scalar minisupers was announced in March 1987. First customer shipments were scheduled to begin July 1987. The NPL family consists of 1-8 CPUs and runs from 40-320 Mflops, 10-96 Mips and has a 154 MB/sec. bus.

Data General may begin development of a vector facility for its machines.

<u>Prime</u> is the only one of these companies to have announced a joint marketing/ development agreement with a newer company. Prime and Cydrome will both sell Cydrome's parallel processor.

Prior to the merger, both <u>Burroughs</u> and <u>Sperry</u> had research efforts underway on multiprocessors.

D. Why Success? Why Failure?

It is interesting to look at how the early companies have fared since 1984 because they run the gamut of success to failure. This section focuses on the state of these companies today and includes some comments on why they have attained the status they have. Companies mentioned include:

Alliant	Culler
Convex	Vitesse
Denelcor	
Elxsi	
Encore	
Flexible	
Sequent	

Of all the companies profiled in this report, three closed. <u>Denelcor</u>, the grandparent of the multi/parallel processing companies, was the first to close its doors in 1985 after it failed to receive further funding. Denelcor had taken seven years to develop its product, the HEP machine, however, revenue was not forthcoming and Denelcor found itself with a severe working capital shortage. Only one machine had been sold while ten were leased and two were tested and returned.

The HEP was complex, using state-of-the-art technology, custom processor elements and custom operating system. The price was extremely high for the performance it provided. An entry-level system cost \$1.3M while the performance range for the machine was only 10-160 Mips. Some users did not feel the machine matched claims made by the company.

<u>Vitesse</u> was the only company to have decided to build a machine based on Gallium Arsenide. The company promised a complex machine based on this new technology within a short time frame. Vitesse was unable to attract the investment dollars it needed to keep going and closed in January 1987.

<u>Culler Scientific's</u> assets have been purchased by Saxpy Computer, a matrix computer company. Saxpy just introduced its product in 1987 and only has one installation to date. The deal was complicated because Saxpy did not want to assume Culler's debts. Culler was unable to manufacture product according to demand. The company had concentrated on its marketing efforts but was unable to supply product. <u>Elxsi</u> has installed more than 70 systems to date. However, Elxsi's product took 4.5 years to develop at a cost of \$30M and has been shipping since 1983. Elxsi has just recently had some profitable quarters and it was rescued in 1986 when Trilogy purchased the company, infusing it with much-needed cash.

Elxsi had, for the most part, been selling uniprocessor versions of its machines. Elxsi recently tried to stimulate demand for multiprocessor configurations by repackaging and lowering prices for multiple processor configurations. The product, the 6400, has custom processing elements and a custom operating system (EMBOS). Elxsi also offers versions of Unix since it felt that offering a proprietary operating system was inhibiting its ability to sell systems. It offers a very fast bus (320 MB/sec.) and up to 2 GB of memory.

Elxsi has undergone a restructuring while it has lowered its operating expenses and repositioned itself as the "first real-time supercomputer." Elxsi had previously marketed itself as a general purpose machine however now it has targeted market niches for its product. Elxsi will offer vector processing and an integrated vectorizing Fortran compiler with VMS extensions, as part of its strategy to make the 6400 as VAX-compatible as possible. Part of the restructuring during 1986 was recruitment and expansion of the management team with emphasis on marketing and sales. A number of sales people were replaced with people knowledgable about Elxsi's current markets. Elxsi acknowledges that while it offers about 100 third-party applications packages, the software that takes advantage of parallel processing capability of the 6400 is limited. The number of third-party applications offered are expected to increase slowly because of such a small installed base. Elxsi is also currently revising its pricing structure.

<u>Encore</u> has a unique history compared with the other companies. It has also only installed about 59 systems to date and has yet to have a profitable quarter. It was one of the few start-ups to receive substantial funding without having a product. Not only did it not have a product but it has since changed its business plan several times. Encore is, once again, in the process of redirecting its marketing strategy this time shifting from general purpose machine to one that suits the transaction processing market.

Management has changed and the company had several layoffs. Encore had also decided to rely on a rather large contract with Sperry to OEM its machine. Encore's inability to deliver a machine on time to Sperry cost Encore the contract. A \$10.7M, three-year contract from DARPA for advanced product development and private funding from Ken Fisher, Founder and Chairman, have helped sustain Encore. However, Encore has recently issued a prospectus indicating that it is seeking to make a private placement of stock.

Encore has emphasized its 100 MB/sec. bus as its most unique feature. The Multimax is a multiprocessor, using off-the-shelf technology and a Unix-based operating system. Encore's product lacks third-party applications.

<u>Flexible</u> has sold only a few systems and is still operating at a loss. The company had overstated revenue figures for 1985 and 1986 which had to be restated causing even greater losses than first indicated. Larry Samartin, Chairman of the Board and co-founder, was asked recently to resign. A shortage of working capital was relieved temporarily by loans in 1987.

22 D. Why Success? Why Failure?

Gartner Group analysts speculate that Flexible's problem has not been with its product but rather with Flexible's inability to differentiate themselves from other companies through applications and skilled marketing and distribution.

Flexible offers a multiprocessor but no vector processing capability yet. Its design consists of modules that can be linked together from very small to very large configurations. The structure uses four different buses. It has the ability to mix CPUs from National Semiconductor and Motorola. It has a Unix-based operating system.

The three companies that took the lead in sales, <u>Alliant, Convex</u>, and <u>Sequent</u>, have several features in common. All of them were able to deliver product when they said they would. They all use off-the-shelf-technology and offer a Unix-based operating system. They all began with a market plan from which they have not deviated until recently. Sequent has shifted its focus away from the scientific/engineering market toward the transaction-processing market. Alliant and Convex are going after new areas without abandoning the scientific/engineering market. All of them are now able to offer over 100 third-party applications. They have also all offered a low price for the performance. All of these companies targeted Digital's market. Convex, in particular, has been the most aggressive about stating and following through on that goal.

Alliant's unique feature has been its vectorizing Fortran compiler as well as an ability to do parallel processing. Convex offers vector processing in a uniprocessor version. Although several Convex processors can be hooked together, these do not function as true multiprocessors. Sequent is a multiprocessor but without vector processing capability.

E. Future Directions

ETA just introduced a machine for under \$1M with an estimated peak performance of 375 Mflops. It is clear that these companies will have to continue to upgrade performance if they hope to stay in business. We speculate that next round of products should be in the 200-250 Mflops range. This section includes what information has appeared in the press about future products from the company and from analysts.

<u>Alliant</u> just introduced the FX/4 as a precursor to its second generation products. "This is the rollout of a new strategy, including a new family of machines with processors below the FX/4 in performance as well as above it." (Ron Gruner, President) Performance for the FX/4 ranges from 11.8-47.2 Mflops and is priced from \$99,900-\$600,000. The FX/4 uses a 32-bit VMEbus rather than a Multibus, which Convex may also use for its second generation product.

The National Center for Supercomputing Applications at the University of Illinois said earlier this year that it intended to upgrade to a 200 Mflop machine by January 1988. The NCSA currently uses an FX/8, a 94 Mflop machine. David Kuck, at the University of Illinois, has been developing a high-end parallel processor incorporating 16 of Alliant's high-end FX/8 models. Dave played a role in the development of the FX/Series so Dave's present development work may be a good indicator of what to expect next from Alliant.

<u>BBN</u> will be upgrading its Butterfly machine. A full 256-processor machine is expected to offer peak performance of 640 Mips compared to 256 Mips now available.

<u>Concurrent</u> has recently been given the rights by Princeton to the technology of the Navier-Stokes Computer which had been developed at Princeton. Concurrent will be evaluating the machine as a potential commercial product.

<u>Convex</u> is also getting ready to announce a second generation. When Convex upgraded its system in October 1986, that upgrade doubled the price/performance of the original system. Convex says this product will provide about twice the price/performance of the C1 systems. It will probably be a tightly coupled architecture with a large shared memory and a clock speed of 40-50 nsec. The processors will probably do multitasking. It may have 50,000-gate CMOS gate arrays. Convex may be switching from a 16-bit Multibus controller to a 32-bit VMEbus controller. C2 software will be compatible with the C1. We believe that since Alliant sounds like it will be in the 200 Mflops range. Convex must offer that same, if not better, performance. Elxsi is looking at a new pricing structure for its products. The next product announcement from Elxsi should be multiple integrated vector processors configured into the system via boards from Sky Computer. Each vector processor will provide 20 Mflops peak performance (32-bit), 10 peak (64-bit). Elxsi expects to begin delivery in early 1988.

<u>Floating Point</u> will be introducing an upgrade to the T Series. No public information has been released as to other future product plans. Floating Point has had a difficult year and is trying to regain some momentum.

Intel will be introducing a new version of its hypercube family in 1988. No details have been announced.

<u>Sequent</u> has already brought out its new system - the Symmetry series. There have been problems with the new cache so the system delivery schedule has been altered. Symmetry's peak performance is 81 Mips.

II. Company/Product Profiles

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A. Multi/Parallel Processors

Alliant Astronautics Concurrent Cydrome Eastman Kodak Elxsi Encore Flexible FPS - M64 Line International Parallel Loral Masscomp Meiko Multiflow Sequent

Littleton, MA

Public company formed 1982

Product	FX/1 — a single pro with vector processing	cessor, non- g capability	expandable	e supermin	icomputer
	FX/4 — newest produ	ct in the F	X family.		
	FX/8 — a high-perfor cessor with vector/sca	mance, ger llar capabili	neral-purpos ty.	se, parallel	multipro-
Market	Principal markets: m financial companies; ernment and defense	ajor indust national re suppliers; u	rial, resean esearch lab universities	rch, engine oratories;	ering and U.S. gov-
# Employees	325				
Facilities	250,000 sq. ft.				
Financing	\$26.3M - 3 rounds of	financing 1	982-1985.		
	December 1986 - Rai ing of 1.5M shares.	ised \$23M	in an initi	al public st	tock offer-
	May 1987 - Offered be converted into con to be used for workin	\$50M 25-ye nmon stock g capital.	ear subord at \$39.75	inated deb per share	entures to . Proceeds
Sales		1985	1986	1 Q 87	2 Q 87
	Revenue Net Income (loss) # Units installed	\$4.4M (\$4.8M) 9	\$30.8M \$4.5M 82	\$12.0M \$2.5M 110	\$13.4M \$1.7M 142
	142 units installed for	more than	62 custome	ers.	
	Product announced Ju First commercial unit FX/4 announced Octo	ıly 1985. shipped Se ber 1987.	ptember 19	85.	
	• FX/1 has been	outselling l	FX/8 by 4	to 1 (IDC a	analyst).
	• Average system	n price · \$7	50,000		·
	• 63% gross prof	it margin			

Agreements	٠	OEM agreement with Apollo worth \$35M over three years. Apollo is reselling Alliant computers as central servers in Domain workstation networks. As of May 1987, Apollo had resold few Alliant processors to domes- tic customers. Agreement will be renegotiated.
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- Joint marketing and development agreement with Sun. Sun will use Alliant machines as computational servers in Sun station networks.
- Joint marketing agreement with Silicon Graphics.

Personnel/ Background Ronald Gruner, President and co-founder Data General

Rich McAndrew, VP of Engineering and co-founder

Craig Mundie, VP of Marketing and co-founder Data General

David Micciche, VP of Marketing, Sales and Customer Service

Barry Fidelman, head of international division Apollo

David McDonald, VP of North American Sales Floating Point, eastern regional manager

John Harte, President of European Operations Floating Point, VP of Sales, Service and Marketing

FX/1 and FX/8 (64-bit machines)

	FX /1	FX /8	FX/4	
# CPUs*	1	1 - 8	1 - 4	
Mips	4.2	32		
Mflops (32-bit)	11.8	94.4	47.2	
Memory (Mbytes)	8 - 16	8 - 256	160	
Cache (KB)	32	512	256	
Price	\$99,900	\$270,000 - \$1M	\$99,900 - \$600,000	
O/S	Concentrix	(version of Unix 4.2)		
Language	FX/Fortrar C, Pascal (Ada - Licer	FX/Fortran 77 (compiler developed by Dave Kuck) C, Pascal (only in a single computational element) Ada - Licensed Verdix's Ada		
CPU Chip	Weitek (Co Motorola 6	Weitek (Computational Element) Motorola 68020 (Interactive Processor)		
I/O	Via Multibus adapters - FX/1 and FX/8 32-bit VMEbus - FX/4			
Follow-on Product	Develop more parallel-based compilers (Lisp, C)			
Other	• Created Alliant Network Supercomputing Resources (ANSR) environment which is designed to allow Alliant users to access network supercomputing from existing minicomputers, mainframes, supercomputers and wide- area X.25 networks through PCs and workstations.			
	• Intro impr user	oduced 4-way disk str ovement in disk I/O s with high I/O require	riping which provides a 400% throughput. Advantageous to ements.	
	• Intro mult signo proc mair	oduced a job schedulir iprocessing capability. ed for parallel process essors, while smaller ing processors.	ng feature that gives the FX/8 Large computational jobs de- sing can be run on a group of tasks are assigned to the re-	
	• Prop	orietary 8,000 gate CM	IOS gate arrays.	
	• Com cross	puting elements are o sbar.	connected with a 176 MB/sec.	

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Other (cont.)

Alliant has bundled two FX/1 configurations so that senior scientists can afford to buy their own systems. These configurations are targeted to Fortune 500 companies' research labs, university professors and government labs.

\$99,500 - 8-user version \$130,500 - 16-user version

- Alliant now offers 64 application packages from 43 suppliers. Expect to offer twice as many over the next year.
- Alliant is selling its system to Wall Street firms bundled with a software package designed for linear programming done by AT&T.

Further Explanation

*CPUs

There are two types of processors in the FX series. The Computational Elements (CEs) are the number crunchers and they run concurrently. The Interactive Processors (IPs) execute interactive user jobs, input/output and other operating system activities. The IPs do not run concurrently.

Two IPs can be configured in the FX/1 and 1-12 in the FX/8.

Each IP interfaces with the IP cache which provides access to global memory and to a Multibus to access I/O devices. The IP has 512KB local memory.

Memory

There is global shared memory in 8MB modules.

The *memory bus* consists of two 72-bit-wide data paths, a 28-bit address bus and a control bus. Total bandwidth is 188MB/sec. read data; 150MB/sec. write data.

Cache

Cache is coherent, write-back.

Astronautics Corporation

Madison, WI

Product	Astronautics' major product is aircraft equipment. In addition, the company also produces minicomputers.
Sales	\$110M
# Employees	1,250
Personnel	Norma Paige, Chairman
	R.E. Zelazo, President and Treasurer
	Nathaniel Zelazo, CEO

Has begun development of a tightly coupled multiprocessor which will be Unix-based with a Fortran compiler.

The compiler will generate code for parallel execution on multiple processors equipped with special high-speed synchronization hardware which allows fine-grained parallelism.

Kernal code will execute symmetrically as there will be no master processor.

(Information taken from a job description circulated February 1986.)

Another job ad circulated in Spring 1987 indicates that Astronautics is looking for an individual to "lead the development effort in multiprocessor system implementation for a supercomputer with unique architectural features."

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Concurrent Computer Corp. (Perkin-Elmer)

Holmdel, NJ

November 1985 - Perkin-Elmer spun out its Data Systems group into an 82% owned subsidiary.

Reason for Spinout	Project a stronger image in 32-bit and multiprocessor markets and enhance attractiveness of parent and Concurrent to finan- cial investors.				
Product	3200 line of 32-	bit superminico	omputers		
Markets	Traditional man tions. A strateg on selling com market.	Traditional markets are real-time and highly dedicated applica- tions. A strategic business unit has been formed to concentrate on selling computers into the on-line transaction processing market.			
Facilities	270,000 sq. ft.	in Holmdel, Oc	eanport and	Trenton Falls	, NJ
	80,000 sq. ft. Ireland	development	and producti	on facility in	Cork,
# Employees	2790				
Financing	Closed initial p of common sto general corpora asset requireme	public offering i ock at \$20 per nte purposes inc ents.	n February 2 share. Proc cluding work	1986 of 1.8M eeds to be u ing capital an	shares sed for d fixed
Sales		1-3Q87	1986	1985	
	Revenue Net Income	\$179.1M \$4.7M	\$244.8M \$6.0M	\$259.2M \$24.2M	
	• Revenue OLTP. F customer	splits into 65- l'iscal 1986 bus rs.	70% from re iness came	eal-time and mainly from	30-35% present

- 50 U.S. and 30 international sales and service offices.
- 35-40% of sales are currently multiprocessors.
- Over 350 multiprocessors have been installed to date.

Concurrent Computer Corp.

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Sales (cont.)

- Reevaluating sales channels and products. Interested in forming strategic partnerships with outsiders. Will look for fewer and tighter relationships as mode of selling to VARs and systems integrators is being analyzed.
- Signed a joint marketing and sales agreement with Apollo in February 1987. Concurrent is counting on this relationship for expansion into new markets particularly financial markets. Other target applications include: simulation, process control and earth resource engineering.
- Established joint venture with Nippon Steel Corp. (NSC), May 1986. Will introduce 32-bit supermini in 1988 or 1989. Concurrent holds 60% and NSC 40% of the company which is called Concurrent - Nippon Corp. and is located in Trenton Falls, NJ. Anticipate \$600,000 sales in 1988. Corporation will concentrate on importing and marketing Concurrent's 32-bit machines for the Japanese market.
- Has a \$10M deal to supply superminis for seismic exploration in Chinese oil fields.

Personnel/ J Background

James Sims, President, and CEO

Was Perkin-Elmer's Sales Vice President and Data Systems Group General Manager.

Charles Farrell, Vice President, Marketing IBM, Wang

Henry Firey, Division Vice President and General Manager of North American Sales

PENTA Systems International

Joseph Rechner, Vice President of Operations Concurrent's Vice President of Customer Service

Concurrent Computer Corp.

3280 MPS

High-end 32-bit multiprocessor of the 3200 supermini line.

# CPUs	Up to 6 (tightly coupled) 1 - CPU 2-5 - auxiliary processing units or I/O processors
Mips	6 - 33.8
Memory	2 - 16 Mbytes (shared)
Cache	Two 8Kbyte caches per processor
0/8	OS/32 (Concurrent's system) Xelos (used in uniprocessor configurations) version of Unix V release 5.2
Language	Fortran, COBOL, C, Pascal, Basic, Ada
System Bus	64MB/sec. (called the S-Bus)
Status	Introduced September 1985. First delivered November 1985, but volume shipments were de- layed until fall of 1986.
	Distributed through VARs and system integrators.
Price	\$250,000 - \$1M
	\$150,000 - OEM price in quantities of 100
Other	Software development efforts are being increased because of need for custom applications software due to the combination of a proprietary operating system and parallel processing architecture.
	Princeton agreed to transfer to Concurrent the technology of the Navier -Stokes Computer so that Concurrent can move the computer from a research project to a commercial product.

Cydrome Inc.

Milpitas, CA

Privately held company founded 1984.

Product	Cydra 5 — A 64-bit minisupercomputer incorporating the Synchronous Parallel Computer (SPARC) (statically-scheduled dataflow) architecture, multiple tightly-integrated processors and parallel processing.	
Target Market	Scientific and engineering users who need speeds of a VAX or IBM 370 general-purpose computer. Company is aiming to fill gap between superminis and supercomputers with a computer system that will combine ease of use and high-speed processing with low cost.	
# Employees	137	
Facilities	Leases 36,000 sq. ft. facility plus 20,000 sq. ft. for production facility expansion.	
Financing	\$33M to date - seed plus three rounds.	
	Prime is one of the investors (10%).	
	Cydrome plans to obtain limited additional private financing ei- ther later in 1987 or early 1988. Plans to make a public offer- ing during 1988-89.	
Status	To be introduced. Product shipments to beta sites scheduled for second half of 1987.	
Agreements	Cydrome and Prime signed a joint non-exclusive development and marketing agreement under which both companies will sell the product.	
	Announced a sales and service agreement with Silicon Graphics.	
Cydrome, Inc.

Personnel/ Background	Andre Schwager, President and Chief Executive Officer Dataquest, Inc. and Hewlett-Packard					
	Dr. B. Ramakrishna Rau, Vice President, Engineering, and Chief Scientist Elxsi - managed development of all peripheral equipment development					
	Arun M. Kumar, Vice President, Finance and Administration, and Chief Financial Officer Elxsi					
	William D. Walton, Vice President, Hardware Digital					
	Joseph Avery, Vice President, Manufacturing Activision and Hewlett-Packard					
	Kent Winton, Vice President, Sales Systems Industries, Inc.					
	Dr. David Yen, hardware development (logic design) IBM San Jose Research Laboratory					
	Dr. Wei Yen, systems software Hewlett-Packard Laboratories - chief architect of the HP fast-path protocol					
	Dr. Ross A. Towle, compiler development Honeywell, Burroughs					
	Dr. Michael Schlansker, Manager of Architecture University of Illinois					

42 A. Multi/Parallel Processors

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Cydrome, Inc.

Cydra 5

The Cydra 5 has a proprietary architecture called the Synchronous Parallel Computer (SPARC) which is a dataflow architecture that moves as much as possible of the decision-making from run-time into compile-time.

Processors	There are three types of processors:
	Numeric — embodies the SPARC architecture. It has an in- struction cache but does not do data caching. It is tightly inte- grated with the
	General-Purpose processors which provide the majority of oper- ating system services and jobs which the numeric processor cannot do. 1-8 processors can be configured.
Memory	Both processors share 256 MB of memory.
I/O	The third type of processor is the I/O. 1-2 processors per sys- tem can be configured. Each processor can support up to 3 VME buses and has a sustained transfer rate of 40 MB/sec.
Mflops	6 - 20 (sustained)
O/S	CYDRIX (Unix V.3)
Language	Fortran 77 compiler with IBM and DEC extensions.
Software	Has eight agreements for third-party applications, mostly in CAD/CAM and computational fluid dynamics.
CPU	Motorola 86020 (General Purpose Processors)
Price	\$600,000 - \$900,000

Eastman Kodak Co.

Rochester, NY

A pilot project is underway to allow Kodak to gain experience in the application, design, and programming of a parallel network of Transputers. Goal is to produce a MIMD machine with distributed memory.

Eight processors have been arranged in a one-dimensional ring. There is no shared memory. Processors communicate via point-to-point serial links. Each board contains 2MB RAM. One board serves as the control board and is connected to a VAX750 and VT100 terminal.

Adding extra processors does not increase execution speed unless enough processors are added to reduce load on every processor.

(Electronics Engineering Times, March 17, 1986, p. T15, for project description)

Elxsi

San Jose, CA

(Trilogy and Elxsi are now the same company. Elxsi Ltd. is the parent company, Elxsi-California refers to the original Elxsi.)

Founded 1979

Product	System 6400 - an expandable, general-purpose, tightly coupled, 64-bit multiprocessor.					
Target	Sells into a large-scale U	aerospace, electroni Jnix sites.	cs, DOD/government labs and			
	Elxsi has n which will u	noted an increase i se the machine for (n number of new installations data processing applications.			
Other	Marketing a ing and gen three CPUs ate that way	Marketing approach: 6400 allows simultaneous parallel process- ing and general purpose computing. Must have minimum of three CPUs to do this and must be specifically set up to oper- ate that way.				
# Employees	230 Layoffs - Fa	ll 1985 and March	1986.			
Financing	Purchased by shares of st	Purchased by Trilogy in 10/85 in a deal worth \$52.3M for 38M shares of stock.				
	\$8M private placement of stock - August 1987.					
Sales		Sales	Net Profit (Loss)			
	1984 1985 1986 1Q87 2Q87 (Note that t	\$18.5M \$22.0M \$16.4M \$ 6.2M \$8M be figures for 1984-	(\$7.0M) (\$17.0M) (\$13.4M) \$0.2M \$0.27M 86 are for Elxsi-California.)			
Personnel/ Background	Peter Apple Cray	ton-Jones, President Research, Executive	& CEO of Elxsi Ltd. Vice President			
	Joseph Rizzi, Vice Chairman of the Board, Elxsi Ltd.					
	Christopher Drahos, VP of Marketing, Elxsi-California Gould					
	Leonard Eschweiler, VP of Sales, Elxsi-California Encore					
	Leonard Sha Hewle	ar, VP of Developme ett-Packard	nt, Elxsi-California			
	Robert Olson, VP of Software, Elxsi-California Hewlett-Packard					

Elxsi

System 6400

Elxsi now offers two CPUs: M6410 and M6420. These two processors can be mixed with no hardware or software modifications.

Note that a joint agreement has been announced with Sky Computers to integrate vector processing into Elxsi's system. Multiple vector processors will have peak performance of 20 Mflops (32 bit) and 10 Mflops (64 bit). Demo available 4Q87, customer shipments 1988.

# CPUs	1 - 12 Largest configuration to date: 10 CPUs					
MIP Range	M6410M64206-7210 (for single CPU)-100					
Memory	Main memory 16MB-2GB The 2GB memory expansion using a 1 Megabit chip has just been announced. Customer shipments to begin August 1987. 4GB virtual memory					
System Bus	Gigabus bandwidth of 320MB/sec. with transfer rate of 160-213MB/sec.					
Cache	64 Kbytes					
	Cache is not coherent even though system is tightly coupled. All shared data is communicated via message-passing.					
O/S	• EMBOS					
	• EMS- VMS-like features which have been integrated into EMBOS. Increases chances of competing in Digital's market.					
	• Unix System V and BSD 4.2					
	Elxsi claims that all four of these systems can run simultaneously.					

Elxsi						
Language	Pascal, C, COBOL 74, Fortran 77 (VMS compatible), Lisp, Ada					
	A vectorizing compiler Fortran compiler for bo Delivery in 1988.	A vectorizing compiler will be integrated into the current Fortran compiler for both versions of Unix, EMS and EMBOS. Delivery in 1988.				
CPU Chip	Semi-custom VLSI (EC)	L) 256K-bit chip				
I/O Capacity	Drive 2MB/sec. subchan 50ns processed cycle tir 1-4 OPS	nnels. ne.				
# Systems Installed	70 - about 50% are unip 25% have four or more Introduced first model i	processors CPUs n 1983.				
Price	Based on M6420 CPU:	\$399,000 - \$3M.				
	Additional memory in 16 Mbytes increment: \$52,000.					
	Cost to upgrade from M6410 to M6420: \$140,000					
	Comparison prices:					
		M6410	M6420			
	CPU alone	\$140,000	\$200,000			
	2CPU with 32MB memory	\$475,000	\$6 25,000			
	Elxsi had previously repackaged the basic 6400 modules to en- courage more multiple-processor sales. Prices were dropped for uni, dual, and quad processors.					
Performance Claims	• Outperforms VAX8650 by 10-50%.					
	• A 12-processor configuration is reportedly comparable to a Cray-1 in performance for some applications.					
	• A typical application M6420 as on the	ation mix runs t M6410.	wice as fast on the			

Elxsi

Other

Introduced Fortran compiler to automatically take advantage of parallel processing. Price: \$10,000.

Introduced package of new software products called the EMS Environment that allows users of VMS to migrate easily to Elxsi's hardware, providing an alternative to VAX clusters. Products include:

- 1. EMS/ECL a DCL emulator
- 2. EMS/ERT VMS system service and run-time library emulation
- 3. CLXCI an EDT-compatible text editor
- Price: ECL & ERT \$20,000 or \$12,500 apiece CLXCI - \$2,000

Introduced 1Q87 CommUnity-DECnet Phase IV end-node emulation over Ethernet. Price: \$15,000

Will add Record Management Service (RMS) support in 4Q87 for EMS.

Introduced CPU Failsoft software package that allows processes to migrate off a CPU having trouble.

Released a family of disk subsystems that includes an 823. Mbyte disk drive and a high-performance disk controller with a 2.4 Mbytes/sec. transfer rate.

Will market INGRES and Oracle.

Encore Computer Corporation

Marlboro, MA

Public company founded in 1983.

Product	Multimax — a general purpose multiprocessor. Also sells Annex terminal server products.						
Target Market	Striving to move away from scientific/engineering sales to in- dustries and application areas that require high-speed, on-line transaction processing and rapid response to systems.						
# Employees	200						
Facilities	Consolidated	d all work into 75,0	00 sq. ft. building	in Marlboro.			
Financing	\$3M investe	d by Ken Fisher -	April 1987.				
	Raised \$25M	A in IPO, April 198	35.				
	\$52.5M original funding 1984. Schlumberger and Sperry were among first investors.						
	Multimax p	roject partially fund	led by DARPA.				
Sales		1- 3Q87	1986	1985			
	Revenue	\$9.3M	\$4.8M	\$0.49M			
	Loss	(\$6 .1 M)	(\$11.9M)	(\$24.0M)			
	First Multimax sales occurred in 2Q86.						
	59 systems have been sold to 38 customers, mainly govern- ment and university sites.						
	Average revenue has been about \$160,000 per system.						
	Awarded a \$10.7M, 3-year contract from DARPA to develop a 1 Bips general-purpose computer with 128-256 CPUs. Announced October 1986.						
	Distribution agreements						
	 Tecex Inc., California Rikei Corp., Japan World Business Machines, Korea 						

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Encore	
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Sales (cont.)

OEM agreements

- Gould Annex terminals
- Proteon to supply Annex terminals
- Matra Datasystems (France) joint product development

Personnel/ Background Ken Fischer, Founder and Chairman Prime

James Pompa, President and COO Honeywell

Peter Gyenes, Senior Vice President of Marketing and Sales BBN Communications Corp.

William Avery, Senior Vice President of Product Development Data General

Isaac Nassi, Vice President of Research

Robert DiNanno, Vice President of Operations Adage, Inc.

Frank Pinto, Vice President of Marketing Data General

Robert Clarissen, Corporate Business Development Vice President

Many executives resigned fall of 1985 including Henry Burkhardt and Gordon Bell.

Encore

Multimax 120 and Multimax 320 (upgrade of 120)

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	1 20	320			
# CPUs	2 - 20	2 - 20			
MIP Range	1.5 - 15	4 - 40			
CPU Chips	NS32032	NS32332			
Price	\$100,000 (entry)	\$131,000 - over \$750,000			
Status	The 320 began ship The 120 began ship	nent August 1987. nent February 1986.			
Memory	4 - 128MB				
System Bus	Nanobus - 100MB/se	æ.			
Cache	32 Kbyte write-throu 64 Kbyte - 320	ıgh - 120			
O/S	Umax - compatible v	with Unix V.3 or Berkeley 4.2			
Language	Fortran 77, COBOL Will offer Verdix's A	, Pascal, C, Basic. ADA.			
I/O	Up to 60 Mbytes/see	2.			
Other	Bus has separate as bus cycle, maximum limit them to 12 ca Card size is about 20	ddress and data lines, 64 bits of data per a bus length of less than one foot which will ards per system unless build bus couplers. $0'' \ge 20''$, 1/3 of it is bus "logic."			
	Encore is trying to encourage third-party software developers to write packages for the Multimax. 60 packages are currently available.				
	A low-end version of	the Multimax may be introduced.			

Flexible Computer Corp.

Dallas, TX

Public company founded 1983.

Product	Flex 32 - Multiple co are bused (expandable	- a mo omputers together configur	ulticompu , each w in multis rations.	ater with a p with memory, alot cabinets to	parallel archit 32-bit CPU ar accommodate	ecture. nd I/O, highly			
Target Market	Goal was t scientific n and softwa	Goal was to market initially to industrial OEMs, real-time and scientific markets then expand to other segments such as Unix and software developers.							
Facilities	20,400 sq.	20,400 sq. ft. (6,000 sq. ft. for manufacturing)							
# Employees	65	65							
Financing	January 1987 - received \$1.3M of a contemplated \$3.9M in subordinated loans from Swiss and U.S. investment groups.								
	\$16.7M th	rough sto	ock offeri	ngs, debt flota	tions, and loan	s.			
Sales	Restated \$\$M				Origina	Original \$\$M			
		1 984	1 985	1986 (1st 9 months)	1985)	1986			
	Revenue	0	0.8	1.03	2.5	4.2			
	Net Loss	(2.4)	(8.67)	(5.04)	(7.6)	(3.0)			
	Flexible's pany repor contracts.	revenue : rted sale	figures h s before	ave been resta it completed	ted because th the terms of	e com- certain			
	Flexible ar	nd its in	dependen	t auditor. Art	hur Anderson	& Co			

have been charged with conspiring to inflate stock prices.

Average system installed: 5-6 processors Average system price: \$220,000 As of September, 1986, 12 were sold.

Flexible has nine domestic sales offices and one office in Canada.

Flexible Computer Corp.

Sales (cont.)

Some Sales Orders

- \$1.8M order for a 40-processor installation and service contract at MCC in Texas.
- 16-processor installation at Naval Weapons Center, China Lake, CA.

OEM agreements as announced by Flexible including value of the agreement

- Martin Marietta up to \$10M, two-year contract announced August, 1986.
- AICON (defense systems integrator), Falls Church, VA up to \$5M, two-year contract
- Burtek (subsidiary of French conglomerate Thomsom-CSF), Tulsa, OK up to \$5M, two-year
- Baham Corp., Columbia, MD (engineering and system integrators) up to \$5M, two-year
- Automation Engineering Inc., Memphis, TN up to \$2.5M

Distribution agreement

• C. Itoh and Co., Japan

Personnel/ Background Nicholas Matelan, President and CEO Honeywell Communications Products

Gerald Rodts, VP of Marketing Gould

Mac Nartirossian, VP of Administration & Controller Price Waterhouse

Dr. Michael Dertouzos, member, Board of Directors Director, MIT Laboratory for Computer Science

Lawrence Samartin. Chairman of the Board. has recently left Flexible at the insistence of some of Flexible's investors.

Flexible Computer Corp.

Flex 32

Series	600	1200	2000	3000	6000		
# CPUs	2-4	2-8	4-10	6-20	30 or 40		
	Largest configuration to date: 40 CPUs						
Memory (Mbytes)	2-24.5	2-56.5	4-40	6-85	46-169		
I/O bandwith (MB/sec.)		_	40-100	60-200	300-400		
Starting Price	\$46,000- \$100,000	\$56,000- \$190,000	\$150,000	\$230,000	\$1M		
Mips	32032: .75	68020: 2.5-3	5	(see CPU Cl	nip)		
System Bus	4 buses per cabinet: 2 common (dual redundant) 160MB/sec. 10 local buses connect 3 levels 160 MB/sec. 10 VME I/O buses Self-test bus (RS 422 bus) connects to all cards.						
	Aggregate bu	ıs bandwidth	per cabinet: 6	396 MB/sec.			
O/S	Unix V - program development MMOS - realtime execution						
Language	Concurrent C, Concurrent Fortran 77, Concurrent Pascal, Concurrent Ada						
CPU Chip	NS32032 - C1C Motorola 68020 - C2C (introduced 4/86) 68881 floating point						
	Processor boa	ards can be i	nixed and ma	tched.			
Follow-on Product	Development of an add-on vector floating point accelerator and an array processing card. This will boost performance to 150 Mflops per 32-bit cabinet. Each array card will perform 15 Mflops. The accelerator will offer .5-1 Mflops. Work supported by \$500,000 grant from NASA.						
Other	Preparing a parallel debugger and an automatic decomposition tool.						
	Application software will be supplied by third party software firms and consulting firms, or by customers.						
	Memory is l memory can	ocal to com be accessed	puters, or sh by all compute	ared as nee ers.	ded, but all		

Floating Point Systems, Inc.

Beaverton, OR

Public company founded 1970.

Product	Series of scientific/engineering minisupercomputers, high- performance array processors and the T Series supercomputer.							
Facilities	337,000 sq. ft Beaverton 50,000 sq. ft Ireland recently closed							
# Employees	800 Approximately 850 workers laid off since summer 1986.							
Sales		1- 3Q 87	1986	1985	1984			
	Revenue Net Income (loss)	\$66.1M (\$14.3M)	\$88.6M (\$14.3M)	\$126.6M \$14.4M	\$118.4M \$15.2M			
	FPS restated its revenues for 1986 (lowered) and is now pre- dicting break-even for the next 1-2 years.							
	Installed Base Scientific computers - over 300 First introduced - 1981							
	Array processors - o First introduc	over 7,500 ced - 1975						
R & D	12-14% of revenues							
Personnel	October 1986 - Lloyd Turner, President and CEO resigned.							
	Milton Smith, Founder, President and CEO							
	C. N. Winningstad,	Chairman						
	George O'Leary, October 1987.	Founder,	President	and CO	0, resigned			
	Lance Johnson, VP Product Development Division IBM							
	John Harte, Vice President, Sales and Service just joined Alliant as President of European Operations							
	John Gustafson, (NCube.	Chief Scier	ntist for	T Series	left to join			
Other	Digital has agreed processors with VA	to resell F X compute	PS M64/6 rs.	0 and M64	1/30 attached			

Floating Point Systems, Inc.

M64 Product Line (includes 64 and 64/MAX series — renamed in August 1986)

	M64/10	M64/20	M64/30	M64/40	M64/50	M64/60	M64/140	M64/145
Previous Name				364	264/20	264/max	364/max	164/max
# Acceler- ators	—	_					8	154
Peak Megaflops	6	6	12	11	20	38	187*	341*
Memory Mwords	1—4	1—4	14	1—9	1-4.5	1-4.5	1—8	1—15
I/O Bus Mbytes/Sec	-	12	12	44	38	38	44	44
Announced	8/86	8/86	8/86	1985	2/86	1985	2/86	1984
Languages	F 77	F77	F 77	C, F 77	C, F 77	C, F 77	C, F 77	C, F 77
Price: \$100,	000 — \$	51 M			:			
*CPU - 11 1	Mflops; e	each appl	ication a	ccelerator	— 22 Mi	lops		

F 77 = FORTRAN 77

Other: 60-65% of FPS systems are hosted by VAX machines.

See Part II, Massively Parallel Computers for T Series product information.

60 A. Multi/Parallel Processors

International Parallel Machines

New Bedford, MA

Private Company founded 1980

Product	IP-1 — an MIMD, 32 or 64-bit, general purpose, parallel processing minicomputer which can be programmed to function as a vector or array processor.
Financing	Started with \$2 million seed money. No institutional investors are involved.
Personnel	Robin Chang, President and founder
IP-1	
# CPUs	Basic configuration of 9 processors (one master processor, eight slave processors)
Mips	4 to 20 (basic configuration) Upgradable to more processors for up to 60 Mips.
Memory	10MB (basic configuration) Upgradable to 40MB
0/S	Runix (company developed version of Unix)
Language	C (modified version), Fortran, Ada
I/O	Over 50 I/O ports
Status	Product introduced. Delivery began October 1985. 3 installed in 1985. Quote a delivery time of two-four months after receipt of order.
Price	\$49,950 - \$400,000
Other	The FPA-32, a 20 to 160 Mflops floating point accelerator, available for \$74,000.
	Machine uses local memory and multiaccess memory modules (MAM) to allow simultaneous access by different processors. One memory module can be accessed by different processors, but one processor can also access different memory modules si- multaneously. An intelligent disk interface allows data transfers while the processor runs at full speed.
	Company is still in business, but no updated information has been available.

Loral Instrumentation

San Diego, CA

Subsidiary of Loral Corporation

Product	Loral Data Flo LDF 100 - (32-bit) "A fifth generation mini- supercomputer" for real-time and computation intensive appli- cations which employs dataflow architecture.
Target	Product is being sold to OEMs and end-users for such applica- tions as flight simulation, data acquisition and physical model- ing (military and aerospace sectors)
# CPUs	5-256
Mips	5-256 (1 per processor node)
Memory	128KB or 512KB
O/S	Genix (Unix derived)
Language	C and Fortran Ada to be offered
Chip	National 32016
Status	Announced September 29, 1985. First system shipped in April 1986.
	Manufacturer reps are now marketing the product. A direct sales force will be established in 1987.
Bus	FLObus - pathway between node processors and I/O system; 4 megatokens/second per chassis.
	LDFbus - administers overall system; I/O data rate 8MB/sec.
Price	\$67,000 for basic 5 processor configuration up to \$2M.
Other	Loral Instrumentation has been selling a dataflow architecture product, the ADS 100, for use in dedicated data acquisition and real-time processing applications. Over 300 ADS 100s have been installed.

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Masscomp

Westford, MA

Public company formed in 1981.

Product	MC5000 series of micro supercomputers			
Target	Real-time data acquisition and technical computing needs.			
# CPUs	1 - 8			
Mips	.7 - 20			
Mflops	Up to 14			
Memory	2M - 10Mbytes			
Cache	8Kb two-way associative			
O/S	Masscomp's Real time Unix			
Language	Fortran, C, Pascal, Lisp, Ada			
CPU	68020 68881 - floating point processor			
Bus	Systems have a proprietary triple bus consisting of:			
	1. High-Speed proprietary bus for Unix processor connection			
	2. Multibus - access to common peripherals			
	3. STD bus - real-time data acquisition			
Status	Introduced 10/85. Available since April 1986.			
Price	\$15,000 - \$350,000			
Sales	1987 1986 1985 1984			
	Revenue \$64.4M \$50.9M \$45M \$21.9M Income (loss) \$6.3M (\$1.5M) \$0.98M (\$1.2M)			
Other	Will implement Sun's Network File System in 1988.			

Meiko Ltd.

Bristol, England	
Product	Multiprocessor containing 311 Inmos Transputers.
Mips	Up to 3,000
Memory	256 Kbytes per chip
Status	Introduced at Siggraph '86 conference in August 1986.
Price	\$850,000
Other	MicroVAX functions as a file server for the machine.
	The system demonstrated at the conference was set up for ray tracing. Rate was 8.5M ray intersections in 47 seconds.
	This product is a larger version of Meiko's Computing Surface, a switched array of 150 transputers, which was introduced in 1985.

Machine is based on a supervisor bus which is reconfigurable either manually or electronically.

System was built primarily for use in database applications.

Multiflow Computer Inc.

Branford, CT

Private company founded 1984

Product	Trace series of general purpose 64-bit computers which use very long instruction words and a Trace Scheduling compiler. Product is based on Joseph Fisher's work at Yale.		
Status	Product introduction 1987.		
	Beta sites: United Technologies Sikorsky Aircraft Div. Grumman Supercomputing Research Center		
Target Market	Scientific and engineering users that need speed greater than a VAX or IBM 370 general purpose computer.		
Competitors	Companies with machines operating over 10 mips.		
# Employees	100		
Facilities	Rents 14,200 square feet		
Financing	 \$7 million first round - Apollo invested some money. \$10.6 - second round, May 1986 - Apollo not included. \$18M - May 1987, private placement of stock. 		
Sales	Signed a joint marketing and development agreement with Apollo.		
Personnel/ Background	Donald Eckdahl, President and CEO NCR		
	Joseph Fisher, Executive VP and Founder Yale University		
	John O'Donnell, VP of Engineering and Founder Yale University		
	John Ruttenberg, VP of Software Development and Founder Yale University		
	Robert Smith, VP of Sales and Marketing Prime		
	Robert Nix, Director of Operating Systems Development Xerox Palo Alto Research Center		
	John Rockwell, Director of Product Marketing McDonnell Douglas Automation		
	Robert Rose, VP of Manufacturing Paradyne		
	Jan Brundin, VP of Product Management Sperry		

Multiflow Computer Inc.

Trace Family

	7/200	1 4/200	28/200	
Mips	53	107	215	
Mflops (peak)	30	60	120	
# Operations per Instruction Word	7	14	28	
Instruction Word Width (Bits)	256	512	1024	
Memory (Mbytes)	32-512	32-512	64-512	
Available	July 1987	4Q87	4 Q 87	
O/S	Trace/Unix 4.3 B	SD		
Language	Fortran, C			
Cache	Large, full-width in all Trace confi with cache perfor	instruction cache y gurations. Trace 2 mance of 984 MB/	which holds 8K inst 8/200s have 1 MB sec.	tructions of cache
Bus	492 MB/sec.			
Price	\$299,500 - \$1M			
Other	Supports variety TCP/IP, Sun's No	of connectivity alt etwork File System	ernatives such as E and DECnet.	thernet,

70 A. Multi/Parallel Processors

Beaverton, OR

Private company founded 1983.

Product	Balance and Symmetry families 32-bit, high performance, general purpose multiprocessors.					
Market	Sequent has shifted its strategy to address the on-line transac- tion processing market while maintaining a commitment to cer- tain technical markets (parallel computing research, software development, computer-based instruction in education and engi- neering simulation).					
# Employees	212 (69 in	product	developmen	t)		
Facilities	86,000 sq.	ft.				
Financing	\$12.7M -	April 19	83 and Spri	ing 1984		
	\$ 7.2M -	Fall 198	5			
	\$ 6.0M -	January ture ca Europe	1987, from pital group	MIP Equity , to help fi	Fund, a Du und expans	itch ven- ion into
	\$22.0M -	May 19 Received	987, from d \$17/share	initial pub for 1.3M sha	olic stock ares.	offering.
Sales	(\$\$M)		1985	1986	1- 2Q 87	
	Revenue		\$4.3	\$20.0	\$16.6	
	Profit (Los	(S)	(\$7.8)	(\$0.9)	\$2 .1	
	\$6.8M of 3	1986 reve	enue came f	rom Siemens	ł.	
	Over 164	systems i	nstalled for	115 custome	ers as of 4/4	/87.
	Sequent h mance to market.	as shifted through	d its image put to app	from near-su peal to the	percompute transaction	er perfor- -oriented
	Major OE	M agreen	ents to dat	e include:		
	• Am \$20	perif Corj M four-ye	o., Chatswor ar agreeme	rth, CA nt for Balanc	ce 8000	
	• Sier 3-5 Will mar	nens A.G year agre l market nufacture	ement wort Balance 80 the 8000 un	h \$50M 00 in Europe nder a techno	e and will e blogy exchar	ventually nge.

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Sales (cont.)

- Teradyne 3-year agreement worth \$10M Also entered a joint development agreement to develop future Teradyne products.
- CliniCom
- CLSI
- MAI Basic Four Joint development agreement to develop a system based around the Symmetry system.
- Announced joint marketing agreements with Oracle and Relational Technology.

Europe

A new company called Sequent Europe B.V. will be established and a European headquarters will open in Amsterdam. Amsterdam will also serve as a European development center for parallel processing technology. Sequent has installed more than 20 machines in Europe. Sequent also opened a British office at Hounslow, near Heathrow Airport. The office will also serve as the European training center. Operations are to be established for each major European country, with new centers in Paris and Munich.

Personnel/ Background Casey Powell, President and Chief Executive Intel

Scott Gibson, Executive Vice President and COO Intel

David Rodgers, VP Engineering Digital

Stuart Bagshaw, European general manager Apple - #2 person in U.K. office

Michael Simon, VP Marketing EnMasse Computer Corp.

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Balance and Symmetry Families (fully compatible)

	Balance		Symmetry	
	B8	B2 1	S27	S8 1
# CPUs	2-12	4-30	2-10	2-30
Mips	1.5-8	2.8-21	6-27	6-81
Memory (MBytes)	2-16	8-48	8-80	8-240
Chip	NS32000		Intel 80386	
Price (\$K)	\$50-250	\$139-500	\$89-450	\$164-800
Introduced	9/84	2/86		5/87
Cache	64 KByte, t	wo way set-associa	te cache.	
System Bus	A new bus	was introduced Sep	ptember 1986	3.
			Mbytes/sec.	
		New bus		Old bus
	Theoretical	80		40
	Effective	53		26.7
O/S	Dynix 3.0 just released May 1987 This version features support for System V and Sequent NFS (based on Sun's Network File System).			
Language	Fortran 77,	C, Pascal, Ada, Li	isp, Basic, CO	OBOL
Status	Balance 210 Symmetry 1987 with copy-back c the S27 an write-throug shipment in	000 - production sh had been schedule volume production ache has resulted i ad S81 will ship N gh cache scheme. April 1988.	ipments star of for beta s n in 4Q87. n a schedule lovember 198 The copy-ba	ted July 1986. hipments September A problem with the change. A version of 87 using the current ack cache will begin

Other

LLNL is also using Sequent equipment to develop a simulation of a Cray-style multiprocessor system.

Announced a PDBX debugger for debugging multiple processes as a group in a parallel computing environment. Works with Fortran, C and Pascal.

Can now add PC-Shells and PC-GKS to Balance Station software. Cost: \$1,000 and \$1,500 respectively.

Runs parallel version of Spice and Linpack.

More than 200 software packages now available from over 70 vendors.

74 A. Multi/Parallel Processors

B. Massively Parallel Computers

Ametek Bolt Beranek & Newman FPS - T Series Intel NCube Thinking Machines

Ametek, Computer Research Division

Arcadia, CA

Product	Hypernet System 14/n hypercube		
	Ametek manufactures precision instruments, electromechanical components, industrial materials, and process equipment. In 1983, Ametek invested in computer research and that later evolved into the Computer Research Division.		
# CPUs	16 - 256		
Mips	Up to 2 per node (200 Mips fully configured)		
Mflops	Up to 12 for 256-node (64-bit arithmetic)		
Memory	16 - 256 Mbytes		
0/S	VMS, Ultrix, Unix 4.2 bsd-interface HOS (Hypernet Operating System) - node		
Language	Fortran 77, C		
Applications	Linpack, Eispack, Matrix Iterative Routines, FFTS		
I/O	8 - 3Mbit/sec. bidirectional communications channels Total communications channel throughput is cumulative to 4Mbits/sec.		
Host	VAX family		
Chip	80286 - CPU 80287 - numeric co-processor		
Status	Introduced 1985 First shipments early 1986 to colleges and universities. Commercial shipments started July.		
	About a dozen installed to date.		
Price	\$75,000 - \$890,000		
Other	No common memory or common bus.		

BBN Advanced Computers, Inc.

Cambridge, MA

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Wholly-owned subsidiary of Bolt Beranek and Newman formed in 1986.

Product	Butterfly — a tightly-coupled massively parallel processor which uses a packet-switching network (called the Butterfly) to connect processors.
Market	Market for simulation, image understanding and real-time mon- itoring applications.
# Employees	125
Financing	BBN Advanced Computers closed a \$32M limited partnership May 1987, underwritten by Paine Webber, to develop a "new generation of high-performance parallel processing computer systems" based on the Butterfly architecture.
Sales	Machine was created through funding from DARPA as part of DARPA's Strategic Computing Initiative. DARPA is BBN's largest customer for this machine. Academic institutions also account for a large portion of sales. DARPA actively encour- ages academic researchers to look at the Butterfly. Universities have purchased the Butterfly through National Science Foundation - supported programs. Some commercial installa- tions include: RCA, Dupont, GTE, Northrop and Lockheed.
	About 85 Butterflys installed as of May 1987. First field installments - 1981 256-processor Butterfly announced 1985.
Personnel/ Background	Paul Castelman, President BBN Software Products Corp.

BBN Advanced Computers, Inc.

Butterfly

# CPUs	128-256	Largest configuration to date: 128
Memory	Each processor has lel interconnection ory on other proces	s local memory plus a very high-speed paral- structure to permit access to the local mem- ssors.
	1MB per processor	with expansion memory up to 4MB.
Mips	.5 per processor (68 1 per processor (68	3000) 020)
Cache	No	
O/S	Chrysalis (similar t	o Unix)
Language	Fortran 77, C, Lisp	
CPU Chip	Motorola 68020 - n Motorola 68000 - fi Motorola 68881 - f the system.	ew offering rst offering floating-point coprocessor has been added to
Price	Basic configuration	with 68020 chip
	4 CPU - \$ 40 32 CPU - \$3 128 CPU - \$	0,000 75,000 800,000
	Additional CPUs -	68020 - \$9,500 each 68000 - \$6,500 each
	New Fortran 77 co	mpiler - \$9,000
Other	Bandwidth throug Butterfly switch is	h each processor-to-processor path in the 32 Megabits/sec.
	Interprocessor com	munication capacity of 8 Gigabits/sec.
	A "Uniform Syste vided above the C	em" multitasking kernal is now being pro- hrysalis operating system for simpler soft-

Announced a VMEbus adapter designed to provide an I/O bandwidth of 6-300 Mbytes/sec. Allows the Butterfly system to expand to large configurations and maintain high throughput for I/O devices such as array processors, graphics systems and high-speed disk interfaces.

ware development.

BBN Advanced Computers, Inc.

Follow-on Product Monarch — Development sponsored by DARPA with a threeyear, \$4.8M research contract announced August 1986.

> This is an 8,000 processor, 8 Bip version with several Gigabytes of shared global memory. Rather than the packetswitching network, memory chips are organized in an interleaving scheme that mimics a single large memory. A special chip, called the Dynamic Delay Adjustment Circuit, has been built which adjusts for different signal delays resulting from different wire lengths. It will have a 1 Gbyte/sec. I/O capacity and a design that eliminates cabling among the switch, memory and processors.

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Floating Point Systems

T Series

Product	The T Series is a line of computers ranging from workstation- sized Class VI machines to a massively parallel supercomputer. The machine has a RISC-like instruction set, is based on a hy- percube configuration and is the first to be based on Inmos's Transputer.		
# CPUs	8-16,384 Largest configuration to date: 128 nodes		
Mips	7.5 per processor		
Mflops	128 Mflops - 262 Gflops (peak) (16 Mflops per processor) Sustained rates will probably be 50% of peak rate.		
Memory	1 MB/processor All memory is real RAM. Programs can directly access any area of memory.		
I/O	Aggregate external bandwidth for one node is 4 MB/sec.		
O/S and Language	Occam C and Fortran to be available later in 1987.		
	A standard operating system is also under development.		
CPU Chip	Transputer		
Status	Announced April 1986 (project began 1982).		
	14 systems installed to date. Some sites:		
	 Los Alamos - largest system — 128 processors Michigan Technological University Cornell University Cal Tech Northrop Research and Technology Center Daresbury Laboratory, Science & Engineering Research Council, Warrington, England 		
Price	\$500,000 (smallest configuration) 16 Gflop model - \$30M.		
Other	• Funds for the T Series program are being reduced.		
	• Chief scientist for this program, John Gustafson, left to join NCube.		

SEE SECTION A, MULTI/PARALLEL PROCESSORS, FOR COMPANY AND M64 SERIES INFORMATION.

Intel Corporation

Beaverton, OR

Public company founded 1968.

Product	IPSC and IPSC-VX series of concurrent computers designed by Scientific Computer Division.				
# Employees	21,300 Laid off 3300 workers in 1985 and early 1986.				
Sales		1 986	1985	1984	
	Revenue Net Income (Loss)	\$1.27B (\$173.2M)	\$1.3B \$1.5M	\$1.6B \$198M	
	R & D spending 1985: \$195M or 14.3% of revenues.				
Personnel	Gordon Moore, Chairman of the Board				
	Andrew Grove, CEO, COO and President				
	Justin Rattr Computers	ner, Director	of Tech	nology, Intel	Scientific

Intel Corp.

IPSC Series - hypercube

# CPUs	32, 64 or 128	Largest configuration to date: 128
Mflops	2-8	
Memory	512 Kbytes RAM	A per node - local memory
O/S	Xenix 3.0 - deriv from Berkeley, 1 sion 7.	vative of Unix III which includes enhancements Microsoft and Intel; compatible with Unix ver-
Language	Fortran, C	
Chip	Intel 80286 - CF Intel 80287 - nu	U meric processing unit
Price	\$150,000 - \$520	,000
Status	Announced Febr Sales to date: 32 Original goal: ov	uary 1985. 2 er 100 in 1985
Other	Nodes are connustrial communication	ected via 10 Mbit/sec. point-to-point internode ation channels.
	The Cube Manag hosts the progr nected to each n	ger provides the user interface to the cube and am tools and system diagnostics. It is con- ode via an Ethernet communications channel.

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Intel Corp.

IPSC-VX Series

Hypercube with vector processing capability. To be used for scientific computations such as circuit simulation, structural analysis, fluid dynamics and oil reservoir modeling.

# CPUs	16, 32, 64
Mflops	106, 212, 424
Memory	24, 48, 96MB 1.5MB per node
O/S	Xenix MBOS - message based O/S on each node
Language	Fortran
Chip	80286 - CPU 80287 - floating point numeric processor unit
Price	\$25,000 - \$450,000 - \$850,000
Status	Announced April 1986 Available summer 1986
Other	Software support: LINcube and EIScube which are parallel ver- sions of Linpack and Eispack
	Gold Hill Computer is developing concurrent computing version of Common Lisp.
	Each node processor is supported by a high-performance vector coprocessor board which occupies an adjacent card slot in the system. The board was developed together with Sky Computer. The nodes and vector boards are connected via a private iLBX II bus. They are tightly coupled with shared memory.
	Use of the vector processors increases each node's floating point performance 100 times for 64-bit vector operations and up to 10 times for scalar operations.

NCube Corp.

Beaverton, OR

Private company started 1983 by three engineers from Intel.

Product	NCube/Ten architecture.	hypercube	using	medium-grain	dataflow
Targeted application areas	Seismic proces database mana element analys	ssing, robotics agement, mole sis.	s, CAD,, r ecular mo	eal-time graphics deling and finite	9
# Employees	20				
Financing	Starting capita 100% of stock	al of \$1.2M. owned by off	ficers.		
	70% employe Shell.	e-owned; 259	% origina	l personal inve	stors; 5%
	May have an i	nitial public o	offering in	1988	
Sales	Revenue figur been profitable according to t	es unavailabl e. Revenue is he chairman.	e, howev growing	er, last six quan at about 300%	ters have per year,
	About 60 syst approximately	ems have bee 4000 nodes.	en sold a	nd installed with	a total of
	Customer ba companies.	ase is 50%	6 univer	sities, 50% c	ommercial
	Major users include:				
	Shell, Amoco, Bell Labs, Oal (Japan), Nippo universities.	Exxon, Mar k Ridge Labs, on Steel, Swa	tin Marie Sandia I edish Def	etta, Litton, RCA Labs, VERAC, CA fense Departmen	A, Unisys, ARB, ATR At, and 12
Personnel/					
Background	John Palmer,	Chairman, CE	O and co-	founder	
	Stephen Colley	y, President a	nd co-foun	lder	
	Bill Richardson	n, CFO and co	-founder		
	John Gustafso Floating	n 7 Point Syster	ns, T Ser	ies Chief Scientis	st
	Robert Hausm Star Te	an, Vice Presi chnologies, Fl	dent, Mar oating Po	rketing vint Systems	

NCube Corp.

NCube/Ten

# CPUs	16-64 nodes per board Up to 16 boards Total of 1024 nodes		
	Largest configuration to date: 256 nodes, however Shell will eventually have a 1024 node configuration. Their system is be- ing enlarged in increments.		
Mflops	Up to 500 .5 per node		
Memory	128 Kbyte per node		
Language	Fortran, C		
0/8	Vertex — program in each node which handles communication facilities, debugging and process management.		
	Axis — provides user interface and disk access. Based on Unix and written in assembly language. Treats processor configura- tion as a single device so Vertex can then split movement and control tasks equally among processors. Runs on Intel 80286.		
Chip	Proprietary 32-bit microprocessor made by VLSI Technology. Contains 160,000 transistors and has on-chip 32- and 64-bit floating point units (IEEE).		
I/O	Eight I/O channels - 90 Mbytes/sec. each		
	22 DMA channels per node.20 of these are paired into 10 bidirectional communications links to connect nodes to neighbors.Two are used for system I/O.		
Status	Introduced November 1985. Shipped first system December 1985.		
Price	\$100,000 - \$2M		
Other	Offers a plug-in four processor board for IBM's personal computers.		
Thinking Machines Corp.

Cambridge, MA

Private company founded June 1983

Product	The Connection Machine is a r grained processor which allows rectly with any other processor hardware and software. Processor processors with machine suppor processors. All shipments to da Symbolics 3600.	massively parallel, SIMD, fine- any processor to connect di- r in any arrangement through ors can also function as virtual rting up to one million virtual te have been front-ended by a
Target	Large computational users in un ment settings.	niversity, industry and govern-
Financing	\$16M Majority of funding came from from William Paley, founder a Stanton, President Emeritus of the Rand Corp. Rumored to be looking for more	n DARPA. Other funds came and chair of CBS, and Frank CBS and former chairman of financing.
Sales	10 computers have already be more. Some have gone to:	en shipped with orders for 7
	MIT - 2 (AI Lab and Media Lab) DARPA - 2 U.S. Naval Research Laboratory - 1	Whitney Demos Productions - 1 Yale - 1 Perkin-Elmer - 2
	Other customers:	
	Martin Marietta Science Applications Corp. Advanced Decision Systems U. of Southern California	U. of Maryland Syracuse U. Supercomputer Research Center
Personnel/ Background	Sheryl Handler, founder and Pres MIT Danny Hillis, chief architect and MIT Marvin Minsky, founding scientis MIT Marvin Denicoff, founding scient Office of Naval Research Richard Clayton, VP of Operation Digital John Mucci, VP of Marketing and	sident founding scientist st ist ns d Sales

Thinking Machines Corp.

Connection Machine - the CM-1 and CM-2

(Note: the CM-1 model will be discontinued.)

# CPUs	16,000 or 64,000 processor configurations Largest configuration to date: 16,000				
Mips	CM-1: 1 Bips CM-2 2.5 Bips				
Mflops	CM-2: 3500 (single precision) 2500 (double precision)				
Memory	CM-1: 32 Mbytes CM-2: 128-512 Mbytes				
Cache	No				
O/S	Front-end provides operating system environment				
Language	C* (has minimal extensions to the C language itself) CM-Lisp and *Lisp REL-2 Fortran 77 with vector and control extensions meeting Fortran 8x standards				
Status	CM-1 introduced April 1986 CM-2 introduced May 1987, available 3Q87.				
I/O	Through the front end or direct to a 1.2 Gigabyte disk. 500 megabits/sec.				
Price	\$1-\$6M				
Other	Air-cooled				
	Machine works best with 10,000 - 1M data elements.				
	Data is transmitted via a router with overall capacity of 3 Gigabits/sec.				
	Software is very complicated and very difficult to write.				
	Housed in a 2,600 lb., 56' X 56' X 26' cube containing 153 multilayer printed circuit boards.				
	High resolution graphics display loads from Connection Machine memory at 1 Gigabit per sec.				
	Introduced the Data Vault, a mass storage unit which houses 42 disk drives acting as a 5 GB system (expandable to 10 GB) with a 40 MB/sec. transfer rate.				
	Signed a VAR agreement with Symbolics.				

C. Near Super Uniprocessors

Convex Scientific Computer Supertek

Convex Computer Corporation

Richardson, TX

Public company founded 1982

Product	The C1 series - a 64-bit, general-purpose, vector/scalar proces- sor with Cray-like architecture. "One-third the performance of a Cray at 10% of the cost."					
Target Market	Digital's current engineering installed base.					
Facilities	108,000 sq. ft	•				
# Employees	435					
Financing	Raised \$32M of credit for w	in three orking ca	rounds of apital and e	financing. Equipment.	Secured	\$24M line
	Received \$231	a in IPO	of 3,135,0	00 shares i	in October	r 1 986 .
	Completed a debentures, A	\$ 53.5M pril 1987	offering of	6% conv	ertible sul	bordinated
Sales		1984	1985	1986	1 Q87	2 Q 87
	Revenue Profit (loss)	\$.5M	\$13.5M (\$5.5M)	\$40.2M \$ 4.0M	\$14.4M \$ 2.1M	\$16.7M \$2.2M
	(Note: original goal had been \$100M by 1986.)					
	163 systems had been installed as of 2Q87 for 102 customers in 14 countries.					
	Machines sold either directly or through OEMs. Anticipate third party sales to account for 50% of revenue by end of 1987.					
	Current business:					
	30% CAE 24% government/aerospace 14% computational chemistry/biology 11% geophysical 21% distributors/OEMs and "other"					
	New markets that have been targeted:					
	• c • t • a	omputation otal designimation	onal chemis m, test and	stry manufact	uring inte	gration

Convex Computer Corporation

Sales (cont.)

24 sales o	ffices in	North	America	and	sales	locations	in	London
and Frank	furt.							

OEMs in Japan: Tokyo Electronic Ltd. Digital Computer Ltd.

Europe: Plan to line-up OEMs in 1986.

Signed joint marketing and development agreement with Sun in January, 1986.

Created an OEM support program called Convoy and introduced two new models of the C1 to enter the OEM market in the U.S. (January, 1986).

Robert Paluck, President Sevin Rosen Ltd.

Steve Wallach, Vice President of Technology Data General

Other

Personnel/

Background

Signed joint marketing agreement with Apollo.

Will jointly market Polygen's CHARMm molecular simulation and modeling software.

Signed a joint development and cooperative marketing agreement with Silicon Graphics. Will pair the Silicon Graphics Iris workstation with the C1 series.

Signed an agreement with Stellar Computer to swap Convex's language compiler and vectorizing hardware designs for Stellar's Unix System V based operating system and communications technology. Convex and Stellar will also conduct joint marketing activities. Announced September 1986.

Convex and Cray signed cross-licensing agreements giving access to existing hardware patents. It does not signal access to future development work.

Established a Technical Advisory Group to provide feedback and direction on current and future products. Outside members are:

- Jon Claerbout, Geophysics, Stanford University
- Dr. Antony Jameson, Aerospace Engineering and Applied Mathematics, Princeton University
- Dr. Ken Kennedy, Computer Science, Rice University

Established the Advanced Supercomputing Technology Research Associates Center at the University of Texas at Dallas for development and application of algorithms for parallel processing.

Convex Computer Corp.

C1 Series

# CPUs 1 1 1-4 Mips 4 4 6.4 - 25.6 (6.4/CPU) Mflops 40 40 40 - 160 (40/CPU) Memory 64MB 64MB 1 - 4GB (1GB/CPU) Price - \$240,000 \$320,000 - 1 \$495,000 - 2 \$820,000 - 4 I/O Channels 3 3 5 I/O Bandwidth - 80 80 - 320 Introduced 10/84 10/86 10/86		C1 XE	C1 XL	C1 XP
Mips 4 6.4 - 25.6 (6.4/CPU) Mflops 40 40 - 160 (40/CPU) Memory 64MB 64MB 1 - 4GB (1GB/CPU) Price - \$240,000 \$320,000 - 1 \$495,000 - 2 \$820,000 - 4 I/O Channels 3 3 5 I/O Bandwidth - 80 80 - 320 Introduced 10/84 10/86 10/86	# CPUs	1	1	1-4
Mflops 40 40 - 160 (40/CPU) Memory 64MB 64MB 1 - 4GB (1GB/CPU) Price - \$240,000 \$320,000 - 1 \$495,000 - 2 \$820,000 - 4 I/O Channels 3 3 5 \$80 - 320 Introduced 10/84 10/86 10/86	Mips	4	4	6.4 - 25.6 (6.4/CPU)
Memory 64MB 64MB 1 - 4GB (1GB/CPU) Price - \$240,000 \$320,000 - 1 I/O Channels 3 3 \$240,000 I/O Bandwidth 80 \$0 - 320 Introduced 10/84 10/86 10/86	Mflops	40	40	40 - 160 (40/CPU)
Price - \$240,000 \$320,000 - 1 I/O Channels 3 3 5 I/O Bandwidth 80 80 - 320 Introduced 10/84 10/86 10/86	Memory	64MB	64MB	1 - 4GB (1GB/CPU)
I/O Channels 3 3 5 I/O Bandwidth 80 80 - 320 Introduced 10/84 10/86	Price	_	\$240,000	\$320,000 - 1 \$495,000 - 2 \$820,000 - 4
I/O Bandwidth 80 80 - 320 Introduced 10/84 10/86 10/86	I/O Channels	3	3	5
Introduced 10/84 10/86 10/86	I/O Bandwidth		80	80 - 320
	Introduced	10/84	10/86	10/86

0/S	Convex Unix (enhanced 4.2 bsd)
Language	VAX-compatible, vectorizing Fortran Vectorizing C Vectorizing Ada (2Q88)
Bus	80 MB/sec. fiber-optic interconnect 2-32 processors can be connected
CPU Chip	Proprietary
Follow-on Product	Possibly a tightly-coupled parallel processor with shared mem- ory that can quickly solve one problem.
Other	• The C1 XP has 20,000-gate CMOS arrays made by Fujitsu. The original C1 had 8,000-gate arrays.
	• Features a RISC-based implementation of the architecture.
	• Supports more than 140 third-party software application packages. Anticipate more than 200 available by end of 1987.
	• COVUE Net - software package that connects C1 to a DECnet network.

Scientific Computer Systems

San Diego, CA

Founded October 1983 - Private

Product	SCS-40 - a 64-bit vector/scalar uniprocessor which utilizes the Cray-XMP instruction set. "25% performance of Cray XMP/1 for about 10% of the cost."
Target Market	Universities, independent research labs, and industries that use computer simulation to solve scientific and engineering prob- lems. Cray and VAX users.
# Employees	180
Facilities	38,000 sq. ft. in San Diego
Financing	\$2.7M - first round May 1984 \$15M - second round May 1985 \$15M - third round 1986
	May file initial public offering mid-1988.
Sales	Projected Sales (fiscal year runs May 1-April 30)
	 \$13M - 1st fiscal year \$50M - 2nd fiscal year \$130M - 3rd fiscal year
	Six U.S. sales offices Twelve salespeople (number should double in 1987) One consultant in France
	19 systems installed to date. Some sites:
	• San Diego Supercomputer Center, shipped July 1986. Computer was donated.
	Boeing Computer Services
	Boeing Military
	Arizona University
	• Software Development, Portland, OR

Scientific Computer Systems

Sales (cont.)

Boeing Computer Systems and SCS have agreed to joint marketing/sales activities. Boeing will provide operating system software (COS 1.13, public version of Cray's operating system) and will offer its line of engineering and scientific software packages to run on the SCS-40.

Personnel/ Background Jack Hugus, CEO and COO GE, IBM

Barry Rosenbaum, President Convex, VP of International Operations

Hanan Potash, co-founder and Vice President of Engineering Burroughs Chief architect of SEL/Gould 32 minicomputer

Timothy Pettibone, Vice President of Software

Floating Point Systems

Donald McBeath, Vice President of Operations Headed Intel's systems engineering council

Bob Robertson, Sales Vice President ETA Systems Marketing Vice President

Sid Fernbach, Board of Directors

Supercomputer Consultant and former director of the Lawrence Livermore National Laboratory Computer Center.

Scientific Computer Systems

SCS-40

# CPUs	One
Mips	18
Mflops	Up to 44
Memory	1, 2, or 4 Megaword Memory configurations 8, 16, or 32MB addressable Memory
System Bus Speed	Multiple 64-bit data buses are used to take data from memory to arithmetic units
	Memory busing - four words/clock period (88.9 MW/sec. or 711.1 MB/sec.)
-	Processor busing - six words/clock period (133.3 MW/sec. or 1.067 GB/sec.)
O/S	Fully compatible with Cray X-MP operating system
	Software allows VAX users to run applications without exiting the VMS environment.
	Will have Unix O/S by end of 1987.
Language	Cray Fortran compiler
I/O Capacity	Two to ten I/O channels each of which has 32K byte high- speed I/O buffer and supports data transfers with external de- vices at data rates up to 20MB/second.
Status	Announced March 1986.
Price	\$595,000 - entry
Other	Using ECL technology but may use VLSI in later models.
	50 applications available, mostly for structural analysis and computational chemistry.
Follow-on Product	Working in-house on loosely coupled parallel systems. R & D project underway to expand memory and adjust instruction set.

Supertek, Inc.

Santa Clara, CA

Private company started 1984.

Product	STK-6401: "the affordable mini-supercomputer with muscle". Cray X/MP compatible to be targeted directly at SCS's computer.			
# Employees	25			
Financing	\$1.5 - \$2M first round. \$150,000 seed money			
	70% of capital stock owned by Michael Fung. 30% owned by 12 outside investors.			
Personnel/ Background	Michael Fung, President and Founder Hewlett-Packard, Spectrum project Goddard Space Center, designed and holds patent on Goodyear Aerospace's Massively Parallel Processor.			
	Roger Dellor, Director of Engineering Elxsi			
	Gordon Seybold, Director of Software Cyber Systems, ETA, CDC			
	Chester McIntosh, Vice President of Marketing/Sales Scientific Computer Systems			
	Mike Humphrey, Director of Software Support ETA, CDC			

Supertek, Inc.

STK-6401

# CPUs	One			
Mips	20 - peak			
Mflops	40 - peak 10.5 - average			
Memory	8 Mbytes - first prototype 128 Mbytes - first product 1GB - eventually			
	640 MB/sec. aggregate bandwidth 160 MB/sec. bandwidth to I/O			
0/S	CTSS (Cray Time Sharing System)			
Language	Fortran (Cray Fortran compiler with VMS Fortran extensions)			
I/O	I/O subsystem communicates with central memory via a high- speed port with a bandwidth of 160 MB/sec. The port is avail- able to multiple data paths with individual bandwidths of up to 50 MB/sec.			
Status	Prototype is running in the lab. Beta test to begin October or November 1987.			
Price	\$200,000 - \$300,000			
Other	• Uses off-the-shelf TTL and CMOS parts.			
	• No gate arrays or other semicustom VLSI circuits.			
	• Hardware support for scatter/gather.			
	• File-cabinet sized system which is front-ended by a MicroVAX.			
	• Will manufacture in Japan a model about the size of an IBM personal computer.			

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D. Personal Supercomputers

Dana Stellar

Dana Computer Inc.

Sunnyvale, CA

Private company formed Fall 1985 by five people from Convergent Technologies.

Product	Titan — a single-user workstation which will be capable of near-supercomputer performance based on parallel architecture and RISC-based microprocessors from MIPS Computer System.
# Employees	40
Facilities	11,000 sq. ft. leasing
Financing	\$11M seed funding - March 1986.
	Kubota Ltd. of Japan has invested \$20M in Dana and agreed to manufacture and market the systems once development is completed - October 1986.
Personnel/ Background	Allen Michels, co-founder Convergent Technologies
	Other founders: Ben Wegbreit, Matthew Sanders, Robert Van Naarden, Richard Lowenthal
	Gordon Bell, Consultant, assisted in defining workstation architecture. Now VP of Research and Development
	William Worley Hewlett-Packard, Manager of Spectrum software prod- ucts and a principal designer of Spectrum's RISC architecture.
	Steve Johnson, compiler development Bell Labs
	Way Ting, Unix O/S development Bell Labs
	Tom Bentley, product design Hewlett-Packard Labs
	Carl Hegenmeyer, I/O and subsystem development Burroughs
	Steve Jenness, communications and network software Digital and Valid Logic
	Dana Group has also recruited people from MIPS Computer System and Silicon Graphics.

Dana Computer Inc.

Titan

# CPUs	3 and up			
Mips	20 - 30			
Mflops	6 (64 bit double-precision)			
Memory	8-128 Mbytes Accessible at 200 Mbytes/sec.			
Cache	yes - per processor			
0/S	Unix-based			
Language	Fortran, C			
System Bus	Capable of handling hundreds of MB/sec.			
Status	To be introduced 1Q88.			
Price	\$50,000 - \$80,000			
Other	• Each processor will contain a scalar and a vector chip.			
	• Scalar engine will be a new 16-MHz RISC chip from MIPS Computer.			
	• 50-million-pixel/s display is integrated with the CPU.			
	• All the gate arrays and full custom designed chips will be CMOS.			
	• Concentrating on third-party applications for three areas:			
	 Mechanical CAE Computational fluid dynamics Computational chemistry 			

108 D. Personal Supercomputers

Stellar Computer Inc.

Newton, MA

Private company founded 1986 by William Poduska, founder of Prime and Apollo.

•

Product	Graphics Supercomputer GS 1000 — high performance engi- neering workstation featuring an integrated real-time graphics processor.	
# Employees	97	
Facilities	22,000 sq. ft. renting	
Financing	\$30M	
Sales	Polygen Corp. (Joel Schwartz, President and COO) has become Stellar's first value-added reseller. The companies will jointly develop a system for use in the chemical and pharmaceutical industry.	
Personnel/ Background	William Poduska, Chairman and CEO Apollo, COB (1980-85) Prime, VP Engineering	
	Arthur Carr, President Codex/Motorola	
	Ian Edmonds, VP of Marketing Prime	
	Paul Jones, Corporate Vice President for Engineering Prime, VP Hardware Development	
	Daniel Murray, Vice President of OEM and Intnl. Sales Masscomp, VP International Sales and Marketing	
	Recruited other personnel from Prime and Apollo.	
	Andy VanDam has taken a leave of absence from Brown University to work with this company. He has been heavily in- volved with product development.	
Other	Apollo has the option to reacquire Stellar Computer if it chooses to do so.	

Stellar Computer Inc.

Mips	20 - 30	
Mflops	Up to 40 (double precision)	
Memory	16 - 128MB	
Cache	1 MB	
O/S	Unix V.3 with Berkeley 4.3 extensions	
Language	Fortran, C Later on will introduce Pascal, Ada, Lisp and Prolog	
Bus	80 - 120 Mbit/sec.	
Status	To be shipped 1Q88.	
Price	\$75,000 - \$125,000	
Other	• Will use 45 custom VLSI components.	
	BICMUS ASIC semi-custom layout	
	• CISC architecture (supports four concurrent "processes" within the CPU)	
	• Will have up to 30 gate arrays.	
	• High performance graphics with 500 to 1000 vector transforms per second and a 4K by 4K buffer which is bit mapped and "z-buffered" to store three dimensional images. 150,000 3-D shaded polygons/sec.	
	• Will support X-Windows and PHIGS graphics standards. Later support will be for GKS and VDI.	
	• Convex and Stellar have agreed to conduct joint market- ing activities. Convex has agreed to swap its language compiler and vectorizing hardware designs for Stellar's System V-based operating system and communications technology. Announced September 1986.	

E. IBM

IBM

Multiprocessors

IBM has several groups of computers which operate with more than one processor. The 3090 series is the most powerful of these groups.

	200E	300E	400E	600E
# CPUs	2	3	4	6
Mips	31	43	53	71
Main Memory	128	128	256	256
Price	\$4.6M	\$6.2M	\$8.4M	\$11.5M
Availability	May 87	3 Q 87	May 87	3Q87

There had been speculation that an eight-processor version of the 3090 would be added to the product line. The six-processor version may be the top of the line because of software complexities encountered in upgrades.

American Express in Phoenix, Arizona is the first to receive a 600E. Aetna Insurance in Hartford, CT will receive the first 300E.

3090 Vector Facility — announced October 1985

Performance increases 1.5 - 3 times that of the base CPU when the Vector Facility is used.

Each CPU may have a Vector Facility.

Price: \$370,000 for one \$600,000 for two

Performance per processor: 108 Mflops

Estimated number of customers who installed vector facilities during 1986: 100

IBM

Parallel Processors

RP3 project (Research Parallel Processing Project) underway at Thomas J. Watson Research Center, started in 1981. IBM is using this project to determine whether the RP3 - and other multiple parallel processors - can be used for multipurpose, broadspectrum applications. It is also a tool for computer scientists to study parallel processing. A strictly parallel system probably won't be released for at least 4-5 years.

Machine itself has standard component technology. It is a MIMD general purpose machine.

RP3 Project

# CPUs	512 (64 largest version to date)	
Mips	1,000	
Mflops	800	
Memory	2.4 Mbytes per processor 1.2 Gigabytes (maximum)	
O/S	Unix-based	
Language	Fortran, C, Lisp	
I/O	192 Mbytes/sec.	
Status	The first 64-processor unit is being readied for assembly. Should be in operation with minimal operating system support within one year.	
Other	Each node has a RISC processor with floating point unit.	
	Same microprocessor as developed for the IBM RT PC.	
	Memory can be globally or locally shared, or both, at the pro- grammer's discretion.	
Problems	1. "Hot Spots" - memory locations for which all data paths in the network were more likely to go for data. This caused data buffers to jam.	
	2. Application development tools.	
	3. Programmer retraining.	

IBM

GF11 Processor

A modified SIMD machine in which a central controller sends instructions to all processors at the same time. Machine will initially be used for numerical evaluation of predictions of quantum chromodynamics. However, the machine's designers believe it can eventually be used for a wider range of scientific and engineering problems. The computer is expected to be in operation by the end of 1987. It will eventually use 576 floating-point processors.

F. Major Computer Companies

AT&T Data General Gould Honeywell Prime Unisys

AT&T

A parallel processing project is underway in the systems architecture research department. An 8-processor, loosely coupled prototype has been put together which utilizes one VAX750 and seven separate 68000 microprocessors. The processors communicate via S/net, a high speed network with a parallel bus developed from the project. A Unix-like operating system called Meglos has also resulted from this research. A goal of the project is to broaden the processors' capacity to handle general, rather than specific, problems.

AT&T and Yale University researchers are joining forces to produce a high-speed parallel computer that is also relatively easy to program. Merging Linda, a set of software primitives developed at Yale that supports parallel programs written in C or any other conventional language, with S/Net, a prototype parallel architecture, researchers are now working to improve performance by producing a custom Linda chip—a very-largescale integrated circuit that essentially incorporates Linda in hardware. The Linda primitives provide for a kind of shared memory called "tuple space," which is available simultaneously to multiple processors. But the AT&T-Yale implementation has no shared memory bank; rather, it is made up of multiple nodes in a communications network. (*Electronics*, 10/16/86)

Data General

Tom West, Vice President of Data General's Systems Group speaks about parallel processors. (*Electronics*, 10/16/86)

"We do a lot of things in the lab that don't become products." "Parallel machines fall into this category - Perhaps some day we will leverage these into the main-line products. Multiprocessor things will come along in a few years."

Reportedly has been recruiting software developers with experience vectorizing code. It is likely that DG will be producing a vector facility for its machines, similar to what Convex and Alliant offer.

Gould

NPL family of minisupers was introduced March 1987 beginning with the NP1.

# CPUs	1 - 8
Mflops	40 - 320
Mips	10 - 96
Memory	64 - 512MB
Bus	154 MB/sec. A new bus must be added for every two processors so an eight- processor configuration needs four buses.
O/S	Proprietary real-time version of Unix.
Status	First customer shipments of single- and dual-processor versions are scheduled to be shipped July 1987; quantity delivery by September.
Price	\$400,000 - \$3M
Follow-on Product	NP2, to come out in a couple of years, will have three times the scalar and four times the vector performance of the NP1. NP3 and NP4 are in early design stages.

Honeywell

Honeywell and NEC Corp. agreed to establish a joint venture called HNS to market NEC's SX series of supercomputers in the U.S. and Canada.

Honeywell spun off its computer operations into a joint venture with NEC and Groupe Bull S.A. of France (December 1986). Honeywell is now effectively no longer directly in the general purpose computer business.

Prime

Introduced a RISC-based workstation incorporating MIPS computer and Silicon Graphics technology.

Invested money in Cydrome (Axiom) 3/86 and has signed a joint development and marketing agreement under which both companies will sell Cydrome's parallel/vector processor. See Cydrome profile for details.

Unisys

Some efforts were underway at Burroughs and Sperry before the companies merged.

Burroughs had undertaken parallel processing research for a potential product with a new language, a microprocessor-based parallel architecture and an interconnection scheme.

Sperry had a group which was working to tie together from 4-16 processors into a multiprocessor configuration.

The Integrated Scientific Processor System (ISPS) (Sperry product), is a supercomputer intended for compute-bound, vector-intensive, scientific applications. It will be integrated into the 1100/90 system. (The Univac 1100 series has mainframe capability with up to four processors.) The ISPS has 1-2 processors, 1-4 I/O processors and a Fortran compiler. Peak performances are 133 Mflops (36 bits) and 67 Mflops (72 bits).

Sperry had signed an OEM contract with Aretė. Aretė makes a 32-bit uni/ multiprocessor marketed for departmental computing and OLTP applications. Sperry has accounted for 60% of Arete's sales. Unisys is presently renegotiating that contract.

G. Out of Business

Culler Denelcor Vitesse (computer group)

Culler Scientific Systems Corp.

Santa Barbara, CA

Closed May 29, 1987. Assets purchased by Saxpy Computer October 1987. Private company named Chi Systems founded by Dr. Glen Culler in 1969 to produce special purpose scientific computers for universities, research groups, the DOD and government organizations such as DARPA and NSF. Company name was changed to Culler in 1985 and a new product line was produced.

Products	Culler 7 family of vector/scalar scientific and engineering com- pute servers which feature built-in math functions.	
	The Culler PSC — a personal supercomputer (compute server) introduced May 1986 to provide parallel processing on a net- work of workstations either as a computer system or a com- pute server. Designed to run with Sun Microsystems workstations.	
Target	Simulation and modeling segment of scientific/engineering com- puter market.	
# Employees	85	
Financing	\$24M — four rounds (last round completed 11/86) Investors: F. Eberstadt, Adler & Company	
Sales	Initial shipments began June 1986. 15-20 systems were shipped in total.	
	C. Itoh & Co., Tokyo, Japan, signed an agreement to distribute the Culler PSC. (May 1986)	
	Joint marketing agreement with Sun Microsystems.	
Personnel/ Background	Glen Culler, Chairman of the Board	
	Jerry Butler, President and CEO left Culler in March 1987. He was replaced by David Folger, formerly with Ridge.	
	James Clark, Vice President and CFO Applied Magnetics Corp.	
	Ward Davidson, Vice President, Sales Digital, IBM	
	Larry Evans, Vice President, Manufacturing and Engineering Tandem, Xerox, Data General, Digital, BBN	
	Michael McCammon, Vice President, Hardware Engineering Washington State University	
	David Probert, Vice President, Software Engineering Burroughs	
Other	Culler had been interested in a joint marketing agreement with Digital.	

Culler Scientific Systems Corp.

Culler PSC (Personal Supercomputer)

# CPUs	1-2
Mips	Up to 18
Mflops	Up to 11
Memory	8-16MB
O/S	CSD
Price	\$98,500 with discounts up to 40%. Price does not include cost of a Sun workstation which powers the system.
Other	The PSC does not have a kernal processor like the Culler 7 models. It only has a 12-slot backplane. The Sun workstation, with which it is designed to run, functions as the kernal processor.
	Developed a new compiler which incorporates expert system techniques to increase performance. The compiler uses a knowl- edge base comprised of system capabilities and programmer coding techniques to come up with the swiftest code sequence. The compiler still reverts to a serial format for some sections of code such as conditional jumps.

Culler 7 Family (4 models)

# CPUs	1-4	
Mips	7-36	
Mflops	4-15	
Memory	8-96MB real; 4GB virtual	
O/S	CSD - enhanced Berkeley 4.2	
Language	Fortran 77, C	
Bus	2 high-speed data and instructions 64-bit system buses with a 50MB bandwidth	
Price	\$275,000 - \$750,000	
Other	 VMS source code compatible Contains a kernal processor which is used to execute the O/S and systems resource management. 27-slot backplane TTL technology Segregated paths for addresses and for data and instructions. Uses register-to-register operations instead of longer pipelines. 	

Denelcor

Aurora, CO

Closed October 1985 after failing to obtain more funding.

13 HEP-1s had been shipped.

Leased

4 to National Security Agency
4 to U.S. Army Ballistic Research Laboratory
1 to DOE (Los Alamos Laboratories)
1 to Shoko Co. Ltd., Japan

Sold

1 to MESSERSCHMITT - BOELKOW BLOHM in West Germany

Tested and Returned

1 to Argonne National Laboratory

1 to University of Georgia Computer Center

Denelcor had charged a maintenance fee of \$1,000/day to federal departments leasing the HEP.

Largest system ever built was a four-PEM (Process Execution Module) version. A one-PEM configuration cost about \$3M.

Vitesse Electronics Corp.

Camarillo, CA

Closed computer group January, 1987

Private company founded 1984.

Product	Had been developing family of high-speed numerical computers and GaAs chips. The first product, a uniprocessor was to be introduced in 1987. This was to be followed by the multiproces- sor called the Vitesse Numerical Processor (VNP).	
# Employees	100	
Facilities	60,000 sq. ft.	
Financing	\$30M - 1985 Norton Co. provided over half the money. Vitesse was seeking additional money and strategic relationships.	
Personnel/ Background	Alfred Joseph, Founder and Chairman Rockwell	
	Allan Edwin, President of Digital Products Division (computer portion of Vitesse)	
	Peter Schay, Marketing Digital	
	Leonard Hughes, Vice President of Operations Encore	

VNP

First multiprocessor was to have had up to 8 processors. No global, shared memory per se. No shared bus.

Each processor would have attached memory however, selective memory sharing would be available to all processors through a system of buses for which the company was seeking patents. Each execution unit would have had nearly 4GB of local memory. The company hoped to take advantage of dropping cost of RAM to keep product price low.

Language: Fortran, Pascal, C

Processors, such as database or Lisp processors, could be integrated on the VNP "nonbus." Vector number crunchers could not.

By 1989 hoped to use GaAs chips which Vitesse was to produce.