All About Superminis

Superminis—those higher-powered, higher-priced computers that have evolved from the conventional 16-bit minicomputers—now represent the fastest-growing segment of the thriving minicomputer market. Now available from more than a dozen suppliers, the superminis feature a longer word length (usually 32 bits) that leads to increased throughput, more precise computations, and easier program development. Originally aimed at scientific "number-crunching" and real-time control applications, the superminis are gaining rapid acceptance in conventional data processing applications as well. As a result, supermini sales are expected to continue to grow at an annual rate exceeding 40 percent.

This report is designed to bring you, in concise comparison-chart form, an up-to-date compilation of the hardware and software characteristics of the superminis that are currently being marketed in the United States. You'll also find some background information on the evolution and current status of the supermini market, detailed explanations of the chart entries, and guidance in selecting a supermini whose characteristics match the requirements of your applications.

By means of detailed comparison charts, this report presents the salient characteristics of 30 superminis from 13 vendors. The accompanying text explains the chart entries, describes the evolution and current status of the rapidly growing supermini market, and provides selection guidelines.

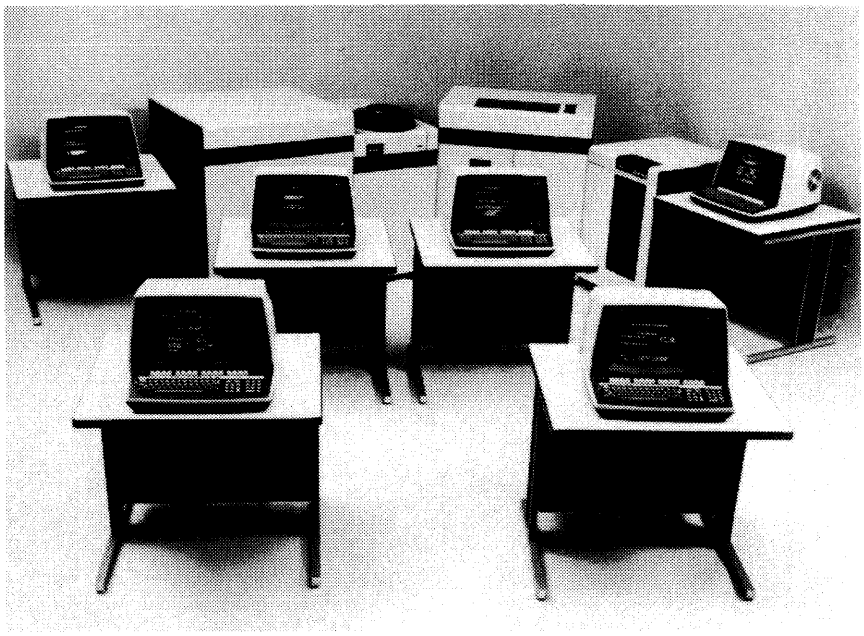
WHAT'S A SUPERMINI?

A supermini, for the purposes of this report, can generally be characterized as a computer that is distinguished by:

- A word length of more than 16 bits,
- A main storage capacity of one million bytes or more,
- An architecture that represents an extension of the architecture used in the vendor's smaller minicomputers,
- And a purchase price, for the basic CPU and minimum main storage, in the range of approximately $30,000 to $150,000.

The great majority of the current superminis uses a 32-bit word length. A 32-bit word neatly holds four 8-bit bytes or two of the 16-bit words used in most of the smaller minicomputers. What's more, the 32-bit word length has been shown to yield an attractive balance between performance and cost in a broad range of applications. As a result, this word length has become so nearly universal among supermini designers that the terms "superminis" and "32-bit minicomputers" have become virtually synonymous.

In this report, for the sake of completeness, we have covered not only all of the known 32-bit superminis, but also the 24-bit and 48-bit computers produced by Harris Corporation—the one significant holdout against the 32-bit tide. We have also included the IBM-compatible 32-bit computer produced by Formation; although this computer has been designed specifically to execute the ➢



The Wang VS 100 features 2M bytes of main memory, 32K bytes of cache memory, and supports up to 4.6 billion bytes of disk storage and 128 workstations. Base-priced at $19,000, the VS 100 supports Wang's FORTRAN, PL/1, COBOL, RPG II, BASIC, Assembler, and Procedure programming languages.

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IBM System/370 instruction repertoire, its architecture, performance, and price place it in the same class as the other current superminis.

Conversely, to focus attention on the true superminis and avoid redundancy with other Datapro reports, we have deliberately *excluded* two categories of computers from this report: 1) the high-powered 16-bit minicomputers produced by companies such as Data General, DEC, Hewlett-Packard, and Modcomp; and 2) the 32-bit computers produced by established mainframe manufacturers such as IBM and Sperry Univac. Prospective buyers should note that there are sizeable overlaps in both performance and price between the superminis and some of the systems in these two excluded categories. As an example, the IBM 4331 Model Group 1, the smallest mainframe in the IBM 4300 Series, is dwarfed in performance and also exceeded in price by many of the current superminis. On the other hand, the most powerful members of Hewlett-Packard's 16-bit HP 3000 Series are in the same price/performance class as some of the superminis. As a result of these overlaps, computer buyers who want to be certain they are selecting the most suitable system for their needs must be increasingly painstaking and broad-minded.

SUPERMINI ADVANTAGES

The principal advantages of the superminis are a direct result of their extended word lengths. A longer word length generally leads to:

- *Increased addressability.* If an entire 16-bit word is used to specify a memory address, the maximum number of storage locations that can be directly addressed is only 2^{16} or 65,536. A 32-bit address, by contrast, can specify up to 2^{32} or *4.29 billion* distinct storage locations. Thus, the longer word length greatly increases a system's "logical address space" (i.e., the total amount of storage that can be directly addressed), permitting effective use of both the large physical main storage capacities and the virtual memory facilities that characterize most of the superminis. Virtual memory, in turn, can greatly facilitate the development of programs for execution on multiprogrammed computers by enabling each programmer to act as if he had a very large single-level storage space totally at his disposal.

- *Increased precision.* A single 32-bit word provides enough precision to satisfy the demands of most scientific and commercial computations, and most of the superminis are also capable of processing double-precision (64-bit) operands. Conversely, the common 16-bit minicomputer word length is too short to provide the required precision in many applications, necessitating the use of time-consuming multiple-word operations.

- *Increased instruction sets.* The longer word length typically makes more bits available for specifying the operation code of each instruction, as well as for specifying index registers, multiple accumulators, indirect addressing, and other parameters. Thus, the superminis can—and usually do—have larger and more powerful instruction repertoires than their 16-bit counterparts. As a result, a single supermini instruction can often do the work of several 16-bit instructions.

- *Increased performance.* A 32-bit supermini normally transfers twice as much information to or from main storage during each cycle as a 16-bit minicomputer, and this inherent performance advantage is further enhanced in many cases through the use of storage interleaving, cache memories, and other power-boosting features. The three previously discussed advantages (increased addressability, greater precision, and more powerful instruction sets) also lead directly to increased performance in most applications.

All of these impressive advantages of the superminis can be achieved only at the expense of increased hardware complexity, which inevitably leads to increased equipment costs. Thus, the superminis tend to have substantially higher price tags than most 16-bit minicomputers, and will prove to be cost-effective only in applications which impose clear-cut *requirements* for one or more of the supermini advantages discussed above. To put it another way, if a 16-bit minicomputer can handle the job, a supermini will usually prove to be an expensive luxury.

THE SUPERMINI MARKET

Credit for launching the supermini market can be claimed by two companies: Systems Engineering Laboratories (which now identifies itself as SYSTEMS rather than SEL) and Perkin-Elmer (formerly Interdata). SYSTEMS introduced the initial models of its 32 Series of 32-bit minicomputers in January 1975, while Perkin-Elmer announced the 8/32, its first true 32-bit processor, just two months later.

There was nothing new about 32-bit computers, of course. The IBM System/360 and System/370 computers are 32-bit machines, and SYSTEMS itself had marketed the 32-bit 8500 and 8600 computers in the late 1960's. But none of these systems could, by any stretch of the imagination, have been called minicomputers. On the other hand, companies such as Perkin-Elmer and Modular Computer Systems (Modcomp) had introduced earlier minicomputers that offered many of the characteristics of 32-bit machines but lacked a true 32-bit access path to main storage. Thus, the SYSTEMS 32 Series and the Perkin-Elmer 8/32 were the first commercially available computers that combined a true 32-bit processing capability with minicomputer-style architecture, compact physical size, and an attractively low price tag.

These two supermini pioneers have been steadily improving their product lines and doing a fairly brisk business ever since 1975. But the supermini market really began to take off when the undisputed king of minicomputers, Digital Equipment Corporation, announced its first 32-bit computer in October 1977. DEC's VAX-11/780, described as an upward extension

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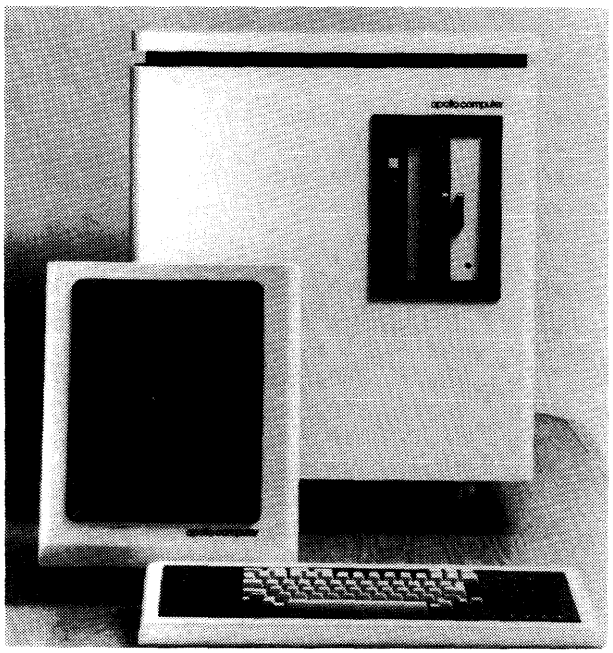

The Apollo Computer provides 256K to 1 million bytes of main memory and 16M bytes of virtual memory, and supports the APOLLO Ring network architecture. A basic Apollo system costs $34,000.

of its PDP-11 architecture, offers up to 8 million bytes of error-correcting MOS main storage, a virtual memory system with a 4-billion-byte logical address space and a full demand-paging facility, and a steadily growing complement of software. This impressive entry by the industry leader ensured the rapid growth of the supermini market.

The VAX-11/780 introduction was followed by the BTI 8000 in June 1978, by the Prime Series 50 family in January 1979, and by the Wang VS-100 in June 1979. Data General, which had long been assuring its users that it would enter the 32-bit computer market "when the time is right," took the wraps off its high-powered Eclipse MV/8000 in April 1980. Six months later, DEC added the VAX-11/750, which offers 60 percent of the VAX-11/780's performance at less than 40 percent of its CPU price. And in December 1980, Honeywell unveiled its first superminis, the 32-bit DPS 6/92 and 6/96.

These and other product announcements have kept the supermini market in a state of rapid flux for the past few years, and the turbulence is likely to continue as new vendors enter the field and the existing suppliers keep adjusting their offerings to meet the demands of the marketplace.

One good bet is that the superminis will continue to be the fastest-growing segment of the dynamic minicomputer industry. According to Data General Corporation's market research staff, 32-bit systems accounted for about 7 percent of worldwide minicomputer revenues in 1980, and that figure will grow to over 15 percent of total minicomputer revenues by 1983. The 32-bit market sector is expected to grow at an annual rate of at least 40 percent through 1983, and to become a billion-dollar annual market by then.

An even more bullish forecast comes from MSRA, Inc., which expects 32-bit minicomputers to experience a 56 percent yearly growth rate until 1985. By that time, MSRA expects total minicomputer revenues to be $25 billion, with 32-bit systems accounting for 22 percent of the total, or $5.5 billion. (In 1980, MSRA says the 32-bit systems accounted for 8 percent of a $7.65 billion minicomputer market, or about $600 million.)

The superminis are being marketed for—and finding widespread user acceptance in—a broad spectrum of applications. Data General, for example, says the applications for its superminis fall into three broad categories: scientific/technical, commercial, and combinations of the two. Scientific/technical uses typically require the handling of large programs and/or large volumes of data, in applications such as simulation, modeling, weather forecasting, telemetry, and seismic data reduction. Commercial applications include distributed processing networks, off-loading of applications from large batch-oriented data centers, and installations where large numbers of users must be supported simultaneously. In mixed technical/commercial environments, the superminis are used for a wide range of interactive applications, as well as for operations research functions that can help an organization improve its operations, allocate its resources, and sharpen its decisions.

An important trend in the supermini field is the rapidly increasing emphasis on the use of these systems for business data processing. Although more superminis are currently being used for scientific/technical work than for business applications, the business segment is growing faster and offers a far greater growth potential for the future. Recognizing this, the supermini vendors are hastening to provide the appropriate software tools to turn their systems into efficient business data processors. DEC, for example, has recently delivered a 32-bit COBOL compiler for its VAX systems, and Data General has indicated that it will soon follow suit. Prime Computer already boasts a relatively strong complement of business-oriented software. And, of course, the IBM-compatible superminis, such as those produced by Formation and Two Pi (currently not listed in the supermini specifications columns), can utilize the full spectrum of software that has been written for the IBM System/370 computers.

THE COMPARISON CHARTS

The key functional characteristics of 30 commercially available superminis from 13 manufacturers are presented in the accompanying comparison charts. Most of the information in the charts was supplied and/or verified by the manufacturers during the months of January and February 1981; their cooperation with the Datapro Research staff in the preparation of these charts is greatly appreciated.

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Regular Datapro users will probably notice that the supermini comparison charts represent a "compatible superset" of Datapro's minicomputer comparison charts; that is, the supermini charts contain all of the entries found in the minicomputer charts plus 11 additional entries which describe the expanded addressing, processing, input/output, and software facilities of the superminis. These additional entries are as follows:

Storage interleaving
Maximum data rate (to/from main storage)
Virtual memory
Logical address space
Maximum program size
Page size
Number of instructions
16/32-bit compatibility
Cache memory
Other I/O channels or ports
Data base management system

All of the comparison chart entries are explained in the following paragraphs, together with discussions of their significance to prospective buyers and some guidelines for selecting the most appropriate superminis for specific applications.

Word Length

Probably the single most important distinguishing characteristic of a computer is its *word length, bits;* i.e., the number of bits (binary digits) that can be stored in or retrieved from main storage during a single cycle. In general, the longer the word length, the greater the efficiency and accuracy of a computer's internal operations—and the higher its price tag. Nearly all of the superminis currently on the market have a 32-bit word length. This size neatly accommodates four 8-bit bytes or two of the 16-bit words used in most of the smaller minicomputers, and yields an attractive balance between economy and performance in many applications. Indeed, the 32-bit word length is the most frequently used criterion for distinguishing between the superminis and their smaller relatives. The entries also indicate the presence of additional bits used for parity checking or error correction purposes (e.g., the entry "32 + 5" indicates that each word location in main storage consists of 32 data bits and 5 error correction bits).

Number of Workstations Supported

A very important consideration for many users who are considering the acquisition of a computer is the number of workstations it can support. Workstations, in this case, can mean most any type of device which can input and/or receive data from the computer. When the computer is used in a business environment, for instance, the workstation would normally be a CRT display terminal or teletypewriter, but in a manufacturing or distribution environment the workstation could be a sensor or transmission unit that simply transmits signals back to the computer for processing.

Main Storage

The *storage type* generally falls into one of two basic categories, magnetic core or semiconductor memory. Most of the superminis employ MOS (metal oxide semiconductor) memory because of its compactness, reliability, and low price. However, bipolar semiconductor technology, a type of transistor-transistor logic, offers a classic trade-off—higher speed at the expense of more space and greater power consumed, as well as greater cost.

The *cycle time* for a storage device is a minimum time interval that must elapse between the starts of two successive accesses to any one storage location. Though cycle time ranks with word length as one of the most significant individual indicators of a computer's performance potential, it is definitely *not* safe to assume that the computer with the fastest cycle time will be the best overall performer in a particular application. Other parameters that have an important effect on a computer's performance include the flexibility and power of its instruction repertoire, the number of storage cycles it requires to execute each instruction, its input/output capabilities, etc.

Access time is the actual elapsed time between the CPU's request for data and the time when that data is received (read). In core memory, the access time is usually one-half the cycle time; semiconductor memories do not display a similar relationship.

The min./max. capacity entry shows the minimum and maximum amount of main storage available for each computer, expressed in thousands (K) or millions (M) of bytes. (Remember, each 32-bit word is capable of holding four 8-bit bytes. Most vendors now express storage capacities in terms of bytes rather than words.)

Storage interleaving is a feature that improves the performance of a computer system by permitting overlapped accesses to two or more independently operating banks of main storage. Four-way interleaving, for example, can effectively quadruple the maximum rate at which data can be transferred between a central processor and its associated main storage.

Maximum data rate, sometimes called the "memory bandwidth," is the maximum rate at which data can be transferred into or out of main storage, expressed in thousands (K) or millions (M) of bytes per second.

Virtual memory is a facility that simplifies programming by providing a large addressable space on a high-speed disk or drum storage unit that appears to the user as real main storage, and from which instructions and data are transferred into real main storage locations as required. Specialized hardware and/or software is required to

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perform the translations between virtual and real storage addresses, and to perform the necessary transfers of instructions and data between auxiliary (disk or drum) storage and main storage.

The *logical address space* is the total amount of storage that can be directly addressed. It is usually limited by the capacity of the system's real main storage, or, in the case of systems with virtual memory facilities, by the number of address bits in each machine-language instruction. For example, a 32-bit address can specify up to 2^{32} or 4.29 billion distinct storage locations.

The *maximum program size* (i.e., the maximum length of any one program) may be the same as the logical address space, or it may be a smaller figure because of limitations imposed by storage protection and management schemes or other factors.

The *page size* entry expresses the size of the fixed-length blocks of instructions and/or data which are transferred between auxiliary (disk or drum) storage and main storage in systems which utilize the popular "paging" approach to virtual memory management. (An alternative approach is the transfer of logical "segments" of varying length.)

Parity checking is a standard feature of some computers and an extra-cost option for others. In some systems, a more powerful technique called "error correction" (below) is used in place of, or in addition to, parity checking. In still other cases, the manufacturers maintain—with some justification—that the reliability of modern magnetic core and semiconductor memories is so high that parity checking is an unnecessary luxury unless absolute accuracy is a must. Parity checking requires the addition of one more bit to each main storage location. This added bit is set to the appropriate value (0 to 1) whenever a word is written into main storage and checked each time the word is read out; the technique permits detection of most, though not all, read and write errors.

Error correction is a more powerful memory-checking technique that involves appending five or more check bits to each word of memory. The check bits, called a Hamming code, and special algorithms allow a system to detect and correct single-bit errors, and also to detect a fair proportion of the multiple-bit errors that occur.

Storage protection is a feature that prevents unauthorized writing in and/or reading from certain areas of main storage. The protection can be accomplished by hardware means, software means, or a combination of both. Though unnecessary in simple dedicated systems, an effective storage protection scheme is an essential element in multiprogramming and time-sharing environments. Some of the superminis feature elaborate storage protection schemes that divide the total logical address space into hierarchical segments or "rings" with varying degrees of protection against unauthorized access.

Central Processor

Although there are many variations in their internal architecture, the great majority of currently available superminis are parallel, binary processors with a fixed word length of 32 bits.

The *number of directly addressable bytes* of main storage is one of the principal distinguishing features between the superminis and the smaller minicomputers. The short word lengths used in most minicomputers impose serious limitations upon the number of bits that can be assigned to hold the address part of each instruction. A typical 16-bit minicomputer instruction might consist of three parts: operation code, address mode field, and the address itself. If 6 bits are assigned to hold the operation code (permitting up to 64 distinct operations) and 2 bits are used to designate the addressing mode (permitting specification of indexing and/or indirect addressing), then only 8 bits are left to hold the address field. Since these 8 bits permit direct addressing of only 256 distinct memory locations, it is clear that other means will need to be employed to access most regions of the computer's main storage. The most common solutions to the problem are the use of multi-word instructions, indexing, and/or indirect addressing.

The 32-bit word length used in most of today's superminis effectively removes this limitation. If just 16 of the 32 bits in each instruction word are used to hold the address field, up to 2^{16} or 65,536 distinct memory locations can be addressed. If a full 32-bit word is used to hold the address field, up to 2^{32} or 4.29 billion distinct locations (most of which would necessarily be in virtual memory rather than in real main storage) can be directly addressed.

The number of instructions provides an indication of the power of a computer's instruction set. Systems with large, powerful instruction sets tend to require fewer instructions to perform a given task, thereby saving both storage space and execution time. Some instructions, such as floating-point arithmetic instructions, may be extra-cost options.

The *16/32-bit compatibility* entry indicates the extent of program compatibility between a supermini and the same vendor's 16-bit minicomputers (if any). "Direct" indicates that the vendor claims that the supermini's instruction set is a "compatible superset" of the instruction set used in the vendor's 16-bit computers, so that all programs written for the 16-bit computers can be executed without modification on the supermini. "Via mode bit" indicates that the supermini can be switched from its native operational mode into a "compatibility mode" in which it can execute some—but perhaps not all—programs written for the vendor's 16-bit computers.

A *cache memory* is a high-speed storage unit that can signficantly increase the performance of a computer by serving as a fast-access buffer between main storage and

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the central processor and/or input/output subsystem. The entry indicates the capacity of the cache memory unit, if any.

Control storage provides an indication of the microprogrammability of a computer. Microprogrammability is a trait that enables the vendor and/or the user to tailor a computer's internal processing capabilities to suit his particular needs. In place of conventional hard-wired logic, a microprogrammed computer uses sequences of microinstructions, usually stored in a special read-only memory (ROM), programmable read-only memory (PROM), or bipolar read-only memory (BROM) unit, to define the effects of each instruction in its repertoire. In some cases, the microprograms can be altered by the user himself, while in others, they are accessible only to the vendor. Microprogrammability can greatly increase the flexibility of a computer, but its presence may involve a trade-off in terms of reduced performance or increased price. Entries here indicate both the type and the size of control storage.

Although it is undeniably dangerous to make inferences about a computer's overall performance capability on the basis of instruction execution times, our charts show the basic *add time, microseconds* to give a first-level indication of fixed-point arithmetic speeds. In general, the indicated add times are the times required to retrieve a one-word operand from main storage and add it to another operand already contained in an accumulator, with no indexing or indirect addressing. Comparisons based on add times can easily be misleading, however, because of differences in word lengths and instruction repertoires.

Hardware multiply/divide facilities are standard in most superminis. In cases where no hardware facilities are present, multiplication and division must be performed by means of programmed subroutines at a signficant reduction in execution speeds.

Hardware floating-point facilities are also included in the standard instruction repertoires of most of the currently available superminis, and are optional in others. Where no hardware facilities are present, floating-point arithmetic must be performed by means of time-consuming subroutines.

Hardware byte manipulation is the ability to conveniently process information expressed in the 8-bit character codes which are rapidly becoming an industry standard. Many of the superminis have special instructions that permit 8-bit segments of a word to be processed efficiently as individual bytes or byte strings.

Battery backup is a feature that is valuable in computers with semiconductor memory, which is volatile and requires refreshing at regular intervals to retain the data that has been written into it. In the event of a power failure, the contents of memory would be lost if the regulator power supply were not backed up by the battery pack.

A *real-time clock or timer* is another essential element in most "time-conscious" systems. A real-time clock enables the program to determine the time of day, while an interval timer usually indicates the amount of time that has elapsed since the occurrence of some significant event. In many cases the timer can trigger an interrupt signal when a predetermined interval of time has elapsed.

Input/Output Control

A *direct memory access channel (DMA)* permits direct transfer of I/O data between main storage and a peripheral controller. When a DMA channel is used, the I/O data bypasses the computer's main hardware registers, and the I/O operation proceeds independently of program control once it has been initiated by the program. In minicomputers that lack a DMA channel, I/O data transfers are generally carried out under direct program control, with each word being transferred by way of the processor's registers. Generally speaking, the DMA channel has two significant advantages over program-controlled I/O; it can accommodate higher I/O data rates, and it causes far less interference with internal procesing operations.

Other I/O channels or ports describes the I/O control facilities, if any, that are provided in addition to one or more DMA channels. Some superminis offer multiplexer channels, which enable multiple peripheral devices to transfer data to or from main storage simultaneously, while others include special high-speed channels designed to accommodate high-performance disk or tape subsystems.

Maximum I/O rate, sometimes called the "I/O bandwidth," is a measure of each computer's potential ability to transfer data to and from peripheral devices or other external sources via all of the available I/O channels, buses, and/or ports. It should be noted that in practical applications, I/O data rates approaching the indicated maximum rates can usually be handled only in short bursts, if at all.

The *number of external interrupt levels* provides a reasonable indication of the power of a computer's interrupt system. It shows the number of different external devices whose interrupt signals can be identified by the processor—though it should be noted that this identification process may require a fairly complex and time-consuming sequence of instructions. Some computers offer additional external interrupt levels as extra-cost options, and in these cases our charts show the available range, from minimum to maximum.

Communications

Maximum number of lines indicates how many data communications lines can be handled by a particular

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system. The types of lines are specified in the next two entries.

Synchronous and *asynchronous* have entries of standard, optional, or no, indicating their availability, and also a notation as to the speed of each line in bits per second (bps). Most entries will be of the type "to 9600 bps," indicating one or more transmission speeds up to a maximum of 9600 bps.

Protocols supported indicates which of the common data communications protocols, if any, are supported through the availability of appropriate hardware and software facilities.

Network architectures supported indicates which of the standardized data communications network architectures, if any, are supported through the availability of appropriate hardware and software facilities.

RJE terminals emulated indicates which of the popular remote job entry terminals, if any, the system can be equipped to emulate. Programs that emulate the functions of the IBM 2780, 3780, and HASP terminals, for example, are available for many of the current superminis.

IBM 3270 emulation indicates whether the system can be equipped to emulate the functions of the widely used IBM 3270 display terminals.

Peripheral Equipment

The comparison charts summarize the standard peripheral devices that are available for use with each computer.

Floppy disk (diskette) drives indicates whether this type of low-cost storage is available and the minimum and maximum on-line capacities that are offered.

Disk pack/cartridge drives signifies whether one or the other, or both of these types of auxiliary storage devices can be interfaced to the system and the minimum and maximum on-line capacities available.

Drum/fixed-head disk storage informs the reader as to the availability of a drum or head-per-track (fixed-head) disk drive and the minimum and maximum on-line capacities offered.

The indicated maximum storage capacities are shown in thousands (K) or millions (M) of bytes and may be the capacity of a single disk drive or the total capacity of two or more (typically, four to eight) drives that can be connected to the system.

Magnetic tape cassettes/cartridges indicates the availability and transfer rates in characters per second (cps) of I/O devices that accommodate low-cost magnetic tape cassettes or cartridges.

Magnetic tape, 1/2-inch indicates the availability and transfer rate in thousands of bytes per second (KBS) of tape drives that accommodate industry-standard 1/2-inch-wide magnetic tape.

Serial (character-at-a-time) printers can provide excellent-quality hard-copy reports for far less money than the line-at-a-time printers usually used with large computers. However, for users who require faster printing capabilities, *line printers* are also available for use with most superminis. Serial printers generally range in speed from about 30 to 600 or more characters per second (cps), while line printers operate at speeds of 100 to 2000 or more lines per minute (lpm).

Data communications interface describes the computer's capabilities, if any, to send and receive data over a common-carrier communications link. The entry indicates whether an interface is available and gives the range of data rates or the maximum data rate in bits per second (bps).

CRT indicates the availability of a CRT display unit and describes its standard screen size in characters per line and number of lines per screen (e.g., 80 char. x 24 lines).

Other standard peripheral units lists the additional peripheral devices that are available for each system. Typical entries include analog/digital (A/D) converters, paper tape readers, paper tape punches, plotters, etc.

Software

A critically important area to be evaluated is *software* — the programming packages and languages used to program the computer and thereby direct its operations. It is important that you carefully investigate the available software. This investigation should include the operating systems, programming languages, preprogrammed utility packages such as sorts and file maintenance, and application packages such as payroll, inventory control, general ledger, etc. Prospective buyers should carefully note whether the software they will require is included in the cost of the system or offered at extra cost.

Vendors' claims and promises concerning the availability and capability of software should be carefully checked. This is particularly true of software that has been announced but not yet released. Vendors have frequently failed to live up to their marketing publicity.

An *assembler* is a special-purpose program that uses the computer's power to facilitate the preparation of other programs. It enables the programmer to write his own program in a simplified format that uses mnemonic operation codes and symbolic operand addresses. The assembler program then converts these symbolic instructions into their machine-language equivalents, producing computer programs ready for loading and execution. Entries here indicate the availability of an assembler or, in some cases, a macro assembler, or both.

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A macro assembler is another software tool to aid the programmer and make his job a little easier. Macro routines can be called by the programmer and copied right into his program. This saves the programmer from having to recode the routine each time it is used and also eliminates the possibility of keying errors when that part of the program is entered. As usual, there is a price to pay: the use of macros usually wastes memory space.

A *compiler* is a software tool designed to shift part of the program preparation task from the user to the computer itself by converting programs written in a simplified, procedure-oriented language into machine-language object programs. Compilers are now used in virutally all large and medium-scale computer installations because of their demonstrated ability to slash programming costs—and they are becoming increasingly available for minicomputers. This trend is possible because of the more powerful central processors now being used, since compilation is an intricate process that requires more storage space and processing power than the earlier minicomputers provided.

Entries in this section of the charts may include widely used high-level programming languages such as *COBOL,* (COmmon Business Oriented Language), *RPG* (Report Program Generator), *FORTRAN* (FORmula TRANSslator), *BASIC* (Beginners All-purpose Symbolic Instruction Code), *ALGOL* (ALGOrithmic Language), *APL, PL/1* or *Pascal;* or proprietary languages that are available from a vendor for use on a particular system. The key word of warning here is that if you use a language that is unique to a vendor, you will be faced with a big problem if someday you decide to change vendors. Your investment in software will be lost, since the programs will not operate on any other system.

An *operating system* facilitates the operation of a computer by handling functions such as: (1) scheduling, loading, and supervising the execution of programs; (2) allocating storage and I/O devices; (3) initiating and controlling I/O operations; (4) analyzing interrupt signals and dealing with errors; (5) handling communications between the system and its human operator; and (6) controlling multiprogramming or time-sharing operations.

Typical entries describing the available operating systems include "batch," which means that the system processes one or more jobs sequentially and requires all data to be supplied before initiation; "interactive," which means that the system allows data, parameters, etc., to be entered as the job is executing; "real-time," which means that the system responds to external demands on a priority basis; or "time-sharing," which means that the system allows multiple users to access the system and share all its resources at the same time. The operating systems for many of the current superminis are capable of supporting two, three, or all four of the above modes of operation simultaneously.

A *data base management system (DBMS)* is a software facility designed to manage and maintain data in a nonredundant structure so that the data will be conveniently available for processing by multiple applications. The DBMS organizes data elements in some predefined structure and keeps track of the relationships among the data elements, thereby facilitating information retrieval and report generation. The availability of an effective DBMS can greatly simplify the applications programming task and increase the overall value of a data processing system.

Language implemented in firmware and *operating system implemented in firmware* tell the reader whether or not the language processor and/or the operating system are contained in microcode. The entries stipulate "fully," "partially," or "no" to indicate the extent of firmware implementation. An advantage to the user is that a language and/or operating system implemented in firmware frees up more memory space for the user's programs and data. Also, the microcode is usually inaccessible to the user (generally contained in read-only memory), eliminating any possible tampering with the language processor or operating system and reducing chances for error. A third advantage derived from firmware implementation is the ability to create more sophisticated and complex system functions at the hardware level. Microcode routines can be substituted for often-used subroutines, thereby increasing system performance.

Pricing and Availability

The comparison charts show the *price of CPU, power supply, front panel, and minimum memory in chassis* along with the memory size in parentheses. *Price of memory increment* stipulates the costs of various sizes (when available) of memory increments, with the actual sizes in parentheses.

If you'll need two or more computers, it's also worth noting that most of the manufacturers offer sizeable discounts from their list prices on orders for multiple computers. Discounts of up to 40 percent are not unusual on large orders.

Date of first delivery indicates when the first production model of each computer was delivered (or is scheduled to be delivered) to a customer.

Number installed to date shows how many systems of each type had been delivered to customers as of approximately January 1981.

Comments

This final entry on the comparison charts is used to explain or amplify the preceding entries and to provide

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▷ other pertinent information about each system's hardware, software, pricing, or applications.

SUPERMINI MANUFACTURERS

Listed below, for your convenience in obtaining additional information, are the full names, addresses, and telephone numbers of the suppliers whose products are listed in the comparison charts that follow.

Apollo Computer, Inc., 5 Executive Park Drive, N. Billerica, Massachusetts 01862. Telephone (617) 667-8800.

BTI Computer Systems, Inc., 870 West Maude Avenue, Sunnyvale, California 94086. Telephone (408) 733-1122.

Computer Design Systems, Inc., 10911 Olson Memorial Highway, Minneapolis, Minnesota 55441. Telephone (612) 545-2855.

Data General Corporation, 4400 Computer Drive, Westboro, Massachusetts 01581. Telephone (617) 366-8911.

Digital Equipment Corporation, 129 Parker Street, Maynard, Massachusetts 01754. Telephone (617) 897-5111.

Formation, 823 East Gate Drive, Mt. Laurel, New Jersey 08054. Telephone (609) 234-5020.

Harris Corporation, Computer Systems Division, 2101 West Cypress Creek Road, Fort Lauderdale, Florida 33309. Telephone (305) 974-1700.

Honeywell Information Systems, Inc., 200 Smith Street, Waltham, Massachusetts 02154. Telephone (617) 895-6000.

Perkin-Elmer, Computer Systems Division, 2 Crescent Place, Oceanport, New Jersey 07757. Telephone (201) 870-4500.

Prime Computer, Inc., Prime Park, Natick, Massachusetts 01760. Telephone (617) 655-8000.

Systems Engineering Laboratories, Inc., 6901 West Sunrise Boulevard, Fort Lauderdale, Florida 33313. Telephone (305) 587-2900.

Wang Laboratories, Inc., One Industrial Avenue, Lowell, Massachusetts 01851. Telephone (617) 459-5000.□

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MANUFACTURER AND MODEL	Apollo Computer, Inc. Apollo Computer	BTI 8000	Computer Designed Systems Adviser IV/900	Data General Eclipse MV/8000	Digital Equipment VAX-11/750
WORD LENGTH, BITS	32	32	32 + 4	32 + 7	32 + 8
NO. WORKSTATIONS SUPPORTED	Unlimited	200	128	128	80
MAIN STORAGE					
Storage type	MOS	Semiconductor	MOS	MOS	MOS
Cycle/access time, microseconds	.75	0.67	.35, .68/.03	0.88/16-byte block	0.64/0.32
Min./Max. capacity, bytes	256K/1M	256K/16M	32K/8,000K	512K/2M	512K/2M
Storage interleaving	NA	—	Std.; 4-way	4-way	—
Maximum data rate, bytes/sec.	2M	60M	Variable	36.4M	—
Virtual memory	Std.; 16M	Standard	Standard	Standard	Standard
Logical address space, bytes	Std.; 16M	512K	Variable	4 billion	4 billion
Maximum program size, bytes	16M	—	256K	512M	2 billion
Page size, bytes	1024	4096	256K	2048	512
Parity checking	NA	Standard	Optional	No	No
Error correction	Standard	No	Optional	Standard	Standard
Storage protection	Standard	Standard	Optional	Standard; 8 hierarchical rings	Standard; 4 hierarchical modes
CENTRAL PROCESSOR					
No. of directly addressable bytes	1M	—	256K	4 billion	4 billion
No. of instructions	65	174	144	467	244
16/32-bit compatibility	—	—	Optional	Direct	Via mode bit
Cache memory	NA	—	Up to 4M	16K bytes	4K bytes
Control storage	NA	PROM	ROM; 16K x 56 bits	RAM; 4K x 75 bits	Opt.; 1K x 80 bits
Add time, microseconds	—	3.5	0.4	0.66	0.92
Hardware multiply/divide	—	Standard	Standard	Standard	Standard
Hardware floating point	No	Standard	Optional	Standard	Standard
Hardware byte manipulation	—	Standard	Standard	Standard	Standard
Battery backup	No	Standard	Optional	Standard	Optional
Real-time clock or timer	Standard	Standard	Standard	Standard	Standard
INPUT/OUTPUT CONTROL					
Direct memory access channel	Standard	4 to 32	Standard	Standard	Std. (Unibus)
Other I/O channels or ports	See Comments	—	Opt. 128 ports for peripherals	High-speed burst multiplexer	Up to 3 optional Massbus adapters
Maximum I/O rate, bytes/sec.	1.5M	10M	2.91M	18.2M	5.0M
No. of external interrupt levels	8	—	—	16	32
COMMUNICATIONS					
Maximum number of lines	3	200	128	128	80
Synchronous	Std.; 1 line	No	Opt.; 9600 bps	Up to 56,000 bps	Up to 1M bps
Asynchronous	Standard	Std.; to 19,200 bps	Opt.; 9600 bps	Up to 9600 bps	Up to 9600 bps
Protocols supported	NA	Async	2780/3780, SNA/SDLC	BSC, X.25	DDCMP, X.25
Network architectures supported	APOLLO Ring	No	SNA (opt.)	X.25	DNA, X.25
RJE terminals emulated	NA	No	2780/3780	2780/3780, HASP	—
IBM 3270 emulation	NA	No	Optional	Yes	—
PERIPHERAL EQUIPMENT					
Floppy disk (diskette) drives	Std.; 1M bytes	No	No	315K-2.5M bytes	1 in console std.
Disk pack/cartridge drives	—	Pack; 67MB to 254MB	Both; 4.8B bytes	Pack & cartridge; 10-6648M bytes	Pack & cartridge; 14-2400M bytes
Drum/fixed-head disk storage	Std.; 33M byte-Winchester	No	No	Fixed-head; 1-48M bytes	No
Magnetic tape cassettes/cartridges	—	No	No	No	No
Magnetic tape, ½-inch	Standard	200KBS (9-trk.)	120KBS	42-468 KBS	36-200 KBS
Serial printer	Std.; 300 lpm	No	200 cps	10-180 cps	30-180 cps
Line printer	Std.; 600 lpm	300, 600, 900 lpm	300-1200 lpm	240-900 lpm	240-1250 lpm
Data communications interface	RS-232-C; 19.2K bps	19.2K bps; async	To 9600 bps	56,000 bps (max.)	Up to 56K bps
CRT	Standard	24 x 80 char.	80 x 24 char.	80 char. x 24 lines	80 char. x 24 lines
Other supported peripheral units	—	None	A/D-D/A conv., plotters, graphics	Card readers, plotter, A/D & D/A subsystems	Card readers
SOFTWARE					
Assembler	—	—	Macro assembler	Macro assembler; 16-bit assembler	Macro assembler (BLISS-32)
Compilers	FORTRAN, PASCAL	BASIC, FORTRAN, COBOL, PASCAL	PASCAL, COBOL, BASIC, FORTRAN	FORTRAN, BASIC, PL/1; 16-bit COBOL	FORTRAN, BASIC, COBOL, CORAL
Operating system	Network Operating System	Time-sharing, batch	Batch, real-time, multi-task, interactive	Time-sharing, multiple-batch, on-line	Time-sharing, batch, on-line
Data base management system	No	—	Yes (DBMS)	16-bit only (DBMS)	16-bit only (DBMS-11)
Language implemented in firmware	No	No	Partially	No	No
Operating system implemented in firmware	No	Partially	Partially	No	No
PRICING & AVAILABILITY					
Price of CPU, power supply, frt. panel and minimum memory in chassis, $	34,000	75,500	100,000 (64K bytes)	151,200 (512K bytes & 96MB disk drive)	89,900 (512K bytes & two 28MB disks)
Monthly maint. of basic configuration above for on-site contract, $	340	827	5,400	892	
Discounts available	Yes	Quantity	Quantity	Various types	Yes
Price of memory increment, $	16,000 (1M bytes)	16,000 (512K bytes)	18,000 (64K bytes)	8,500 (256K bytes)	9,100 (256K)
Date of first delivery	March 1981	April 1981	November 1978	October 1980	November 1980
Number installed to date	NA	NA	NA	NA	NA
COMMENTS	Other I/O controls: 1 block multiplexer channel, 1 multibus controller	Packaged system for interactive and multi-stream batch workload	Single source responsibility, turnkey interactive, direct processing system	Uses a compatible superset of the 16-bit Eclipse instruction set	Uses gate array technology; 488 logic gates per chip

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MANUFACTURER AND MODEL	Digital Equipment VAX-11/780	Formation 4000 Information System	Harris 500	Harris 800	Honeywell DPS 6/92
WORD LENGTH, BITS	32 + 8	32	24	48	32
NO. WORKSTATIONS SUPPORTED	112	36	Appl. dependent	Appl. dependent	64
MAIN STORAGE					
Storage type	MOS	MOS	MOS	MOS	MOS
Cycle/access time, microseconds	0.600/0.290	1.2/.8	0.40/0.29	0.40/0.29	.55
Min./Max. capacity, bytes	512K/12M	256K/8M	384K/3072K	384K/3072K	1024K-4096K
Storage interleaving	2-way (optional)	No	Std.; 4-way	Std.; 4-way	Standard
Maximum data rate, bytes/sec.	13.3M	500M	19M	19M	1.3M
Virtual memory	Standard	Standard	Standard	Standard	No
Logical address space, bytes	4 billion	4.2 billion	12M	12M	16M
Maximum program size, bytes	2 billion		—	—	—
Page size, bytes	512	OS dependent	—	—	—
Parity checking	No	Standard	No	No	Standard
Error correction	Standard	Standard	Standard	Standard	Standard
Storage protection	Standard; 4 hierarchical modes	Standard	Standard	Standard	Standard
CENTRAL PROCESSOR					
No. of directly addressable bytes	4 billion	4.2 billion	3072K	3072K	16M
No. of instructions	244	IBM/370 inst. set	241	241	237
16/32-bit compatibility	Via mode bit	—	—	—	Direct
Cache memory	8K bytes	—	6K	6K	8K bytes
Control storage	Opt.; 1K x 99 bits	ROM 16K x 8 bytes	No	No	RAM, 2K x 96 bits
Add time, microseconds	0.4	1.4	NA	NA	0.4
Hardware multiply/divide	Standard	No	Standard	Standard	Standard
Hardware floating point	Standard	No	Optional	Standard	Standard
Hardware byte manipulation	Standard	No	Standard	Standard	Standard
Battery backup	Optional	No	Optional	No	Optional
Real-time clock or timer	Standard	Standard	Optional	Optional	Standard
INPUT/OUTPUT CONTROL					
Direct memory access channel	1 to 4 Unibuses	Standard	Optional	Optional	Standard
Other I/O channels or ports	Up to 4 optional Massbus adapters	—	—	Up to 31 logical I/O channels	Sync, async, broadband
Maximum I/O rate, bytes/sec.	13.3M	5M	To 19M bps	To 19M bps	16M
No. of external interrupt levels	32	256	16-48	16-72	64
COMMUNICATIONS					
Maximum number of lines	112	64	64	128	64
Synchronous	Up to 1M bps	Std.; 19.2K bps	Opt.; 56K bps	Opt.; 56K bps	Up to 72,000 bps
Asynchronous	Up to 9600 bps	Std.; 28.8K bps	Opt.; 19.2K bps	Opt.; 19.2 bps	Up to 9600 bps
Protocols supported	DDCMP, X.25	2780/3780, HASP, 3270	Async, bisync	Async, bisync	VIP, BSC, HDLC
Network architectures supported	DNA, X.25	VM Pass Thru, PSCS	None	None	DSS
RJE terminals emulated	—	2780/3780	See Comments	See Comments	2780/3780, HASP
IBM 3270 emulation	—	Yes	Yes	Yes	Yes
PERIPHERAL EQUIPMENT					
Floppy disk (diskette) drives	1 in console std.	2M bytes	No	No	512K to 1024 KB
Disk pack/cartridge drives	Pack & cartridge; 14-2400M bytes	—	Opt.; 40M-124B bytes	Opt.; 40M-162B bytes	Pack & catridge 67 to 2092MB
Drum/fixed-head disk storage	No	Fixed; 70M bytes (8 drives)	No	No	No
Magnetic tape cassettes/cartridges	No	No	No	No	No
Magnetic tape, ½-inch	36-200 KBS	1600 bpi (8 drives)	469K bps	469K bytes	800, 1600 bpi
Serial printer	30-180 cps	180 cps	165 cps	165 cps	120-160 cps
Line printer	240-1250 lpm	300, 600 lpm	240-1200 lpm	240-1200 lpm	300-900 lpm
Data communications interface	Up to 56K bps	To 19.2K bps	56K bps	56K bps	72,000 bps (max.)
CRT	80 char. x 24 lines	80 x 24 char.	1920 char.	1920 char.	80 char. x 24 lines
Other supported peripheral units	Card readers	—	Printer/plotters	Printer/plotters	Card reader, document handler, factory ter.
SOFTWARE					
Assembler	Macro assembler (BLISS-32)	IBM/370 compatible	Macro assembler	Macro assembler	Macro assembler
Compilers	FORTRAN, BASIC, COBOL, CORAL	IBM/370 compatible	FORTRAN 77, BASIC, APL, COBOL, RPG II	FORTRAN 77, BASIC, APL, COBOL, RPG II	COBOL, FORTRAN, BASIC, RPG
Operating system	Time-sharing, batch, on-line	IBM/370 compatible	Batch, real-time, time-sharing	Batch, real-time, time-sharing	Time-sharing, on-line, batch
Data base management system	16-bit only (DBMS-11)	Yes (TMS)	Tes (TOTAL)	Yes (TOTAL)	I-D-S/II, TOTAL
Language implemented in firmware	No	No	No	No	No
Operating system implemented in firmware	No	No	No	No	No
PRICING & AVAILABILITY					
Price of CPU, power supply, frt. panel, and minimum memory in chassis, $	128,000 (512K bytes & two 28MB disks)	42,500	99,600 (384K bytes)	165,990 (384K bytes)	100,000 (1024KB)
Monthly maint. of basic configuration above for on-site contract, $	753	290	Special quote	Special quote	940
Discounts available	Yes	Quantity	Yes	Yes	Yes
Price of memory increment, $	9,100 (256K bytes)	5,000 (256K)	31,300 (1.9M bytes)	31,300 (1.9M bytes)	28,000 (1024KB)
Date of first delivery	Feburary 1978	August 1980	First qtr. 1979	First qtr. 1980	4th quarter 1981
Number installed to date	2000+	9	NA	NA	NA
COMMENTS	High-performance floating-point accelerator is optional	IBM/370 software-compatible with integrated controllers and peripherals	RJE terminals emulated: 2780/3780, HASP, UT-200, U-1004	RJE terminals emulated; 2780/3780, HASP, UT-200, U-1004	Fully compatible with 16-bit members of DPS 6 line

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MANUFACTURER AND MODEL	Honeywell DPS 6/96	Perkin-Elmer 3220	Perkin-Elmer 3240	Prime 150	Prime 250
WORD LENGTH, BITS	32	32 + 7	32 + 7	32	32
NO. WORKSTATIONS SUPPORTED	112	32 (for interactive programming)	32 (for interactive programming)	16	16
MAIN STORAGE					
Storage type	MOS	MOS	MOS	MOS	MOS
Cycle/access time, microseconds	.55	0.34/NA	0.25/NA	0.75/0.54	0.75/0.54
Min./Max. capacity, bytes	1024K-16M	256K/4M	256K/16M	256K/1M	512K/1M
Storage interleaving	Standard	None	Up to 4-way	Std.; 2-way	Std.; 2-way
Maximum data rate, bytes/sec.	13M	NA	64M	2.5M	2.5M
Virtual memory	No	None	None	Standard	Standard
Logical address space, bytes	16M	4M	16M	32M	32M
Maximum program size, bytes	—	4M	16M	32M	32M
Page size, bytes	—	—	—	2K	2K
Parity checking	Standard	No	No	Standard	Standard
Error correction	Standard	Standard	Standard	Standard	Standard
Storage protection	Standard	—	—	Standard	Standard
CENTRAL PROCESSOR					
No. of directly addressable bytes	16M	4M	16M	64K	64K
No. of instructions	237	206 std., 52 opt.	206 std.; 52 opt.	300+	300+
16/32-bit compatibility	Direct	Direct	Direct	Direct	Direct
Cache memory	8K bytes	Opt.; 1K bytes	Std., 8K bytes	Standard; 2KB	Standard; 2KB
Control storage	RAM, 2K x 96 bits	ROM; 2K x 32 bits	ROM; 2K x 32 bits	4K x 64	4 x 64
Add time, microseconds	0.4	0.45	NA	1.1	1.1
Hardware multiply/divide	Standard	Standard	Standard	Standard	Standard
Hardware floating point	Standard	Optional	Optional	Standard	Standard
Hardware byte manipulation	Standard	Standard	Standard	Standard	Standard
Battery backup	Optional	Standard	Standard	Optional	Optional
Real-time clock or timer	Standard	Standard	Standard	Standard	Standard
INPUT/OUTPUT CONTROL					
Direct memory access channel	Standard	7-channel DMA bus	1 to 4 DMA buses	Standard	Standard
Other I/O channels or ports	Sync, async, broadband	Multiplexer bus	Multiplexer bus	—	—
Maximum I/O rate, bytes/sec.	16M	8M	40M	2.5M	2.5M
No. of external interrupt levels	64	1-1023	1-1023	64	64
COMMUNICATIONS					
Maximum number of lines	112	63	63	18	18
Synchronous	Up to 72,000 bps	Up to 2M bps	Up to 2M bps	9600 bps (2 lines)	9600 bps
Asynchronous	Up to 9600 bps	Up to 9600 bps	Up to 9600 bps	9600 bps (16 lines)	9600 bps
Protocols supported	VIP, BSC, HDLC	SDLC, HDLC, ADCCP, BSC	SDLC, HDLC, ADCCP, BSC	See Comments	See Comments
Network architectures supported	DSS	—	—	PrimeNET	PrimeNET
RJE terminals emulated	2780/3780, HASP	2780/3780, HASP	2780/3780, HASP	2780/3780, HASP	2780/3780, HASP
IBM 3270 emulation	Yes	Yes	Yes	No	No
PERIPHERAL EQUIPMENT					
Floppy disk (diskette) drives	512K to 1024KB	No	No	512K-2M bytes	512K-2M bytes
Disk pack/cartridge drives	Pack & cartridge 61 to 3072M bytes	Pack & cartridge; 10-1024M bytes	Pack & cartridge; 10-1024M bytes	Both; 12-2400M bytes	Both; 12-2400M bytes
Drum/fixed-head disk storage	No	No	No	Fixed; 1M bytes	Fixed; 1M bytes
Magnetic tape cassettes/cartridges	No	Cassette; 1 KBS	Cassette; 1 KBS	No	No
Magnetic tape, ½-inch	800, 1600 bpi	36-120 KBS	36-120 KBS	To 488K bps	To 488K bps
Serial printer	120-160 cps	30-180 cps	30-180 cps	300 lpm	300 lpm
Line printer	300-900 lpm	300-600 lpm	300-600 lpm	To 1000 lpm	To 1000 lpm
Data communications interface	72,000 bps (max.)	To 2M bps	To 2M bps	To 56K bps	To 56K bps
CRT	80 char. x 24 lines	80 char. x 24 lines	80 char. x 24 lines	80 char. x 25 lines	80 char. x 25 lines
Other supported peripheral units	Card reader, document handler, factory terminals	Card readers, A/D- and D/A	Card readers, A/D and D/A	PT, card reader, printer/plotter, letter-qual. printer	PT, card reader, printer/plotter, letter-qual. printer
SOFTWARE					
Assembler	Macro assembler	Assembler, macro assembler	Assembler, macro assembler	Macro & micro assembler	Macro & micro assembler
Compilers	COBOL, FORTRAN, BASIC, RPG	BASIC, COBOL, RPG II, FORTRAN, PASCAL	BASIC, COBOL, RPG II, FORTRAN, PASCAL	BASIC, FORTRAN, COBOL, RPG II	BASIC, FORTRAN, COBOL, RPG II
Operating system	Time-sharing, on-line, batch	Batch, real-time, multi-tasking	Batch, real-time, multi-tasking	Multi-user, virtual memory	Multi-user, virtual memory
Data base management system	I-D-S/II, TOTAL,	DMS/32	DMS/32	Yes, DBMS	Yes, DBMS
Language implemented in firmware	No	No	No	Partially	Partially
Operating system implemented in firmware	No	No	No	Partially	Partially
PRICING & AVAILABILITY					
Price of CPU, power supply, frt. panel, and minimum memory in chassis, $	120,000 (1024KB)	36,000 (256K bytes)	91,000 (256K bytes)	49,000 (256K bytes)	59,500 (512K bytes)
Monthly maint. of basic configuration above for on-site contract, $	980	330	600	340	460
Discounts available	Yes	Quantity	Quantity	Volume	Volume
Price of memory increment, $	28,000 (1024KB)	8,000 (256K bytes)	8,000 (256K bytes)	15,000 (256K bytes)	15,000 (256K bytes)
Date of first delivery	4th quarter 1981	May 1979	September 1979	February 1980	February 1980
Number installed to date	NA	1000	500	NA	NA
COMMENTS	Fully compatible with 16-bit members of DPS 6 line	128 32-bit general registers; optional 2K-word writable control store	128 32-bit general registers; optional 2K-word writable control store	Protocols supported include most IBM, Univac, Honeywell, and ICL	Protocols supported include most IBM, Univac, Honeywell, and ICL

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MANUFACTURER AND MODEL	Prime 450	Prime 550	Prime 650	Prime 750	Systems Engineering Laboratories 32/27
WORD LENGTH, BITS	32	32	32	32	32
NO. WORKSTATIONS SUPPORTED	32	63	63	63	64
MAIN STORAGE					
Storage type	MOS	MOS	MOS	MOS	MOS
Cycle/access time, microseconds	0.75/0.54	0.75/0.54	0.75/0.54	0.75/0.54	.6/.6
Min./Max. capacity, bytes	256K/1024K	512K/2048K	512K/4096K	512K/8192K	256K/1M
Storage interleaving	Std.; 2-way	Std.; 2-way	Std.; 2-way	Std.; 2-way	Standard
Maximum data rate, bytes/sec.	2.5M	2.5M	2.5M	2.5M	26.67M
Virtual memory	Standard	Standard	Standard	Standard	NA
Logical address space, bytes	32M	32M	32M	32M	2M
Maximum program size, bytes	32M	32M	32M	32M	2M
Page size, bytes	2K	2K	2K	2K	32K
Parity checking	Standard	Standard	Standard	Standard	No, but ECC
Error correction	Standard	Standard	Standard	Standard	Standard
Storage protection	Std.; 3 levels	Std.; 3 levels	Std.; 3 levels	Std.; 3 levels	Standard
CENTRAL PROCESSOR					
No. of directly addressable bytes	64K	64K	64K	64K	128K (words)
No. of instructions	300+	300+	300+	300+	180
16/32-bit compatibility	Direct	Direct	Direct	Direct	NA
Cache memory	Standard; 2KB	Standard; 2KB	Std.; 2KB	Std.; 16KB	NA
Control storage	4K x 64	4K x 64	5K x 64	7K x 64	PROM/ROM
Add time, microseconds	1.1	1.1	1.1	0.5	.6/1.2
Hardware multiply/divide	Standard	Standard	Standard	Standard	Standard
Hardware floating point	Standard	Standard	Standard	Standard	Standard
Hardware byte manipulation	Standard	Standard	Standard	Standard	Standard
Battery backup	Optional	Optional	Optional	Optional	Optional
Real-time clock or timer	Standard	Standard	Standard	Standard	Standard
INPUT/OUTPUT CONTROL					
Direct memory access channel	Standard	Standard	Standard	Standard	Standard
Other I/O channels or ports	—	—	—	—	I/O processor, PPU, HSD
Maximum I/O rate, bytes/sec.	2.5M	2.5M	2.5M	8M	1.2M-3.2M
No. of external interrupt levels	64	64	64	64	16-112
COMMUNICATIONS					
Maximum number of lines	Async (32); Sync (4)	Async (63); Sync (8)	Async (63); Sync (8)	Async (63); Sync (8)	64
Synchronous	Std.; to 56K bps	Std.; to 56K bps	Std.; to 56K bps	Std.; to 56K bps	Opt.; to 9600 bps
Asynchronous	Std.; to 9600 bps	Std.; to 9600 bps	Std.; to 9600 bps	Std.; to 9600 bps	Opt.; 38.4K bps
Protocols supported	HASP, 2780/3780	HASP, 2780/3780	HASP, 2780/3780	HASP, 2780/3780	Bisync
Network architectures supported	PrimeNET, X.25	PrimeNET, X.25	PrimeNET, X.25	PrimeNET, X.25	—
RJE terminals emulated	HASP, 2780/3780	HASP, 2780/3780	HASP, 2780/3780	HASP, 2780/3780	HASP
IBM 3270 emulation	Emulate & support	Emulate & support	Emulate & support	Emulate & support	—
PERIPHERAL EQUIPMENT					
Floppy disk (diskette) drives	512K-2M bytes	512K-2M bytes	512K-2M bytes	512K-2M bytes	Opt.; 1.6M bytes
Disk pack/cartridge drives	Both; 12-2400M bytes	Both; 12-2400M bytes	Both; 12-2400M bytes	Both; 12-2400M bytes	Both; 10M-19.2B bytes
Drum/fixed-head disk storage	Fixed; 1M bytes	Fixed; 1M bytes	Fixed; 1M bytes	Fixed; 1M bytes	Fixed; 5-40M bytes
Magnetic tape cassettes/cartridges	No	No	No	No	No
Magnetic tape, ½-inch	To 488K bps	To 488K bps	To 488K bps	To 488K bps	36K-1.2M bytes
Serial printer	300 lpm	300 lpm	300 lpm	300 lpm	340 cps
Line printer	To 1000 lpm	To 1000 lpm	To 1000 lpm	To 1000 lpm	300-900 lpm
Data communications interface	To 56K bps	To 56K bps	To 56K bps	To 56K bps	40K bps
CRT	80 char. x 25 lines	80 char. x 25 lines	80 char. x 25 lines	80 char. x 25 lines	1920 characters
Other supported peripheral units	PT, card reader, printer/plotter, letter-qual. printer	PT, card reader, printer/plotter, letter-qual. printer	PT, card reader, printer/plotter, letter-qual. printer	PT, card reader, printer/plotter, letter-qual. printer	I/O, high-speed data interface
SOFTWARE					
Assembler	Macro & micro assembler	Macro & micro assembler	Macro & micro assembler	Macro & micro assembler	Assembler, macro assembler
Compilers	BASIC, FORTRAN, COBOL, RPG II	BASIC, FORTRAN, COBOL, RPG II	BASIC, FORTRAN, COBOL, RPG II	BASIC, FORTRAN, COBOL, RPG II	FORTRAN, COBOL, BASIC
Operating system	Multi-user, virtual memory	Multi-user, virtual memory	Multi-user, virtual memory	Multi-user, virtual memory	Real-time, interactive, multi-batch
Data base management system	Yes, DBMS	Yes, DBMS	Yes, DBMS	Yes, DBMS	Yes, TOTAL
Language implemented in firmware	Partially	Partially	Partially	Partially	FORTRAN RTL (part.)
Operating system implemented in firmware	Partially	Partially	Partially	Partially	No
PRICING & AVAILABILITY					
Price of CPU, power supply, frt. panel, and minimum memory in chassis, $	65,000 (450 QMB) 73,000 (450 HMB)	80,000 (550 HMB)	105,000 (650 HMB)	130,000 (750 HMB) 149,000 (750 1MB)	25,000
Monthly maint. of basic configuration above for on-site contract, $	500 (450 QMB) 590 (450 HMB)	578 (550 HMB)	685 (650 HMB)	785 (HMB) 965 (750 1MB)	225
Discounts available	Volume	Volume	Volume	Volume	Yes
Price of memory increment, $	—	40,000 (1M bytes)	40,000 (1M bytes)	40,000 (1M bytes)	9,000 (256K bytes)
Date of first delivery	1979	1979	1979	1979	March 1980
Number installed to date	77	201	11	55	40
COMMENTS					7 slots available for memory and I/O expansion; five additional IOP controller slots

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MANUFACTURER AND MODEL	Systems Engineering Laboratories 32/2750	Systems Engineering Laboratories 32/30A	Systems Engineering Laboratories 32/57	Systems Engineering Laboratories 32/77	Systems Engineering Laboratories 32/75
WORD LENGTH, BITS	32	32 + 7	32 + 7	32 + 7	32 + 4
NO. WORKSTATIONS SUPPORTED	64	16	64	64	64
MAIN STORAGE					
Storage type	MOS	MOS	MOS	MOS	MOS
Cycle/access time, microseconds	.6/.6	.6/.3	0.6/0.3	0.6/0.3	0.6/0.3
Min./Max. capacity, bytes	256K/4M	32K, 64K/256K	64K/256K	64K/4096K	32K/2048K
Storage interleaving	Standard	Standard	Standard	Standard	Standard
Maximum data rate, bytes/sec.	26.67M	26.67M	26.67M	26.67M	26.67M
Virtual memory	NA	NA	NA	NA	NA
Logical address space, bytes	2M	1M	1M	1M	1M
Maximum program size, bytes	2M	1M	1M	1M	1M
Page size, bytes	32K	—	—	—	—
Parity checking	No, but ECC	No	No	No	Standard
Error correction	Standard	Standard	Standard	Standard	No
Storage protection	Standard	Standard	Standard	Standard	Standard
CENTRAL PROCESSOR					
No. of directly addressable bytes	128K (words)	128K (words)	128K	128K	128K (words)
No. of instructions	180	160 (PSW); 189 (PSD)	160 (PSW); 189 (PSD)	161 (PSW); 187 (PSD)	161 (PSW); 187 (PSD)
16/32-bit compatibility	NA	NA	NA	NA	NA
Cache memory	NA	NA	NA	NA	NA
Control storage	PROM/ROM	PROM/ROM	PROM/ROM	PROM/ROM	PROM/ROM
Add time, microseconds	.6/1.2	.6/1.2	0.6/1.2	0.6/1.2	0.6/1.2
Hardware multiply/divide	Standard	Standard	Standard	Standard	Standard
Hardware floating point	Standard	Standard	Standard	Standard	Standard
Hardware byte manipulation	Standard	Standard	Standard	Standard	Standard
Battery backup	Optional	Standard	Optional	Optional	No
Real-time clock or timer	Standard	Standard	Standard	Standard	Standard
INPUT/OUTPUT CONTROL					
Direct memory access channel	Standard	Standard	Standard	Standard	Standard
Other I/O channels or ports	I/O processor, PPU, HSD	I/O processor, PPU, HSD	I/O processor, PPU, HSD	I/O processor, PPU, HSD	I/O processor, PPU, HSD
Maximum I/O rate, bytes/sec.	1.2M-3.2M	6.67M (words)	6.67M (words)	6.67M (words)	6.67M (words)
No. of external interrupt levels	16-112	16-112	16-112	16-112	16-112
COMMUNICATIONS					
Maximum number of lines	64	16	64	64	64
Synchronous	Opt.; to 9600 bps	Opt.; to 9600 bps	Opt.; to 9600 bps	Opt.; to 9600 bps	Opt.; to 9600 bps
Asynchronous	Opt.; 38.4K bps	Opt.; 38.4K bps	Opt.; 38.4K bps	Opt.; 38.4K bps	Opt.; 38.4K bps
Protocols supported	Bisync	Bisync	Bisync	Bisync	Bisync
Network architectures supported	—	—	—	—	—
RJE terminals emulated	HASP	HASP	HASP terminals	HASP terminals	HASP terminals
IBM 3270 emulation	—	—	—	—	—
PERIPHERAL EQUIPMENT					
Floppy disk (diskette) drives	Opt.; 1.6M bytes	No	No	No	No
Disk pack/cartridge drives	Both; 10M-19.2B bytes	Both; 10-1200M bytes	Both; 10M-19.2B bytes	Both; 10M-19.2B bytes	Both 10M-19B bytes
Drum/fixed-head disk storage	Fixed; 5-40M bytes	Fixed; 5-40M bytes	Fixed-head; 5-40M bytes	Fixed-head; 5-40M bytes	Fixed-head; 5-40M bytes
Magnetic tape cassettes/cartridges	No	No	No	No	No
Magnetic tape, ½-inch	36K-1.2M bytes	36K-1.2M bytes	36K-1.2M bytes	36K-1.2M bytes	36-1.2M bytes
Serial printer	340 cps	340 cps	340 cps	340 cps	340 cps
Line printer	300-900 lpm	300-400 lpm	300-900 lpm	300-900 lpm	300-900 lpm
Data communications interface	40K bps	40K bps	40K bps	40K bps	40K bps
CRT	1920 characters	1920 characters	1920 characters	1920 characters	1920 characters
Other supported peripheral units	I/O, high-speed data interface	I/O, high-speed data interface	A/D, D/A, Digital I/O, high-speed data interface	A/D, D/A, Digital I/O, high-speed data interface	A/D & D/A, Digital I/O, high-speed data interface
SOFTWARE					
Assembler	Assembler, macro assembler	Assembler, macro assembler	Assembler & macro assembler	Assembler & macro assembler	Assembler & macro assembler
Compilers	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC
Operating system	Real-time, inter-active, multi-batch	Real-time, inter-active, multi-batch	Real-time, inter-active, multi-batch	Real-time, inter-active, multi-batch	Real-time, inter-active, multi-batch
Data base management system	Yes, TOTAL	Yes, TOTAL	Yes, TOTAL	Yes, TOTAL	Yes, TOTAL
Language implemented in firmware	FORTRAN RTL (part.)	FORTRAN RTL (part.)	FORTRAN RTL (part.)	FORTRAN RTL (part.)	FORTRAN RTL (part.)
Operating system implemented in firmware	No	No	No	No	No
PRICING & AVAILABILITY					
Price of CPU, power supply, frt. panel, and minimum memory in chassis, $	Contact vendor	25,100 (128K bytes)	39,500 (256K bytes)	46,300 (256K bytes)	72,300 (128K bytes)
Monthly maint. of basic configuration above for on-site contract, $	Contact vendor	200	295	330	470
Discounts available	Yes	See 32/57 Comm.	See Comments	See 32/57 Comm.	See 32/57 Comm.
Price of memory increment, $	Contact vendor	Contact vendor	12,500 (256K bytes)	13,500 (256K bytes)	6,300 (32K bytes)
Date of first delivery	March 1980	September 1979	April 1979	June 1978	January 1978
Number installed to date	NA	10	10	275	325
COMMENTS	Packaged in 2 chassis providing 4M bytes of memory and 18 slots for I/O expansion	Single chassis system, memory map, multiprocessor configurations	OEM, volume, end-user, and educational discounts are available	4M-byte memory in double cabinet, memory map, and multiprocessor configurations	Double-cabinet system, memory map, multiprocessor configurations

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MANUFACTURER AND MODEL	Systems Engineering Laboratories VPS 3200CM	Systems Engineering Laboratories VPS 3300CM	Systems Engineering Laboratories VPS 6400CM	Wang VS 100
WORD LENGTH, BITS	32 + 7	32 + 7	32 + 4	32
NO. WORKSTATIONS SUPPORTED	64	64	64	128
MAIN STORAGE				
Storage type	MOS	MOS	MOS	MOS
Cycle/access time, microseconds	0.6/0.3	0.6/0.3	0.6/0.3	0.66
Min./Max. capacity, bytes	64K/4096K	64K/4096K	64K/4096K	128K/2048K
Storage interleaving	Standard	Standard	Standard	No
Maximum data rate, bytes/sec.	26.67M	26.67M	26.67M	NA
Virtual memory	NA	NA	NA	Standard
Logical address space, bytes	1M	1M	1M	2M
Maximum program size, bytes	1M	1M	1M	1M
Page size, bytes	—	—	—	2048
Parity checking	No	No	No	Standard
Error correction	Standard	Standard	Standard	Standard
Storage protection	Standard	Standard	Standard	Standard
CENTRAL PROCESSOR				
No. of directly addressable bytes	128K (words)	128K (words)	128K (words)	512K
No. of instructions	161 (PSW); 187 (PSD)	161 (PSW); 187 (PSD)	161 (PSW); 187 (PSD)	170
16/32-bit compatibility	NA	NA	NA	Direct
Cache memory	NA	NA	NA	32K
Control storage	PROM/ROM	PROM/ROM; 4096	PROM/ROM; 4096	—
Add time, microseconds	420 ns.	420 ns.	1.0	—
Hardware multiply/divide	Standard	Standard	Standard	—
Hardware floating point	Standard	Standard	Standard	Standard
Hardware byte manipulation	Standard	Standard	Standard	Standard
Battery backup	Optional	Optional	Optional	No
Real-time clock or timer	Standard	Standard	Standard	Optional
INPUT/OUTPUT CONTROL				
Direct memory access channel	Standard	Standard	Standard	Standard
Other I/O channels or ports	I/O processor, PPU, HSD	I/O processor, PPU, HSD	I/O processor, PPU, HSD	—
Maximum I/O rate, bytes/sec.	6.67M (words)	6.67M (words)	6.67M (words)	—
No. of external interrupt levels	16-112/192	16-112/192	16-112/192	5
COMMUNICATIONS				
Maximum number of lines	64	64	64	16
Synchronous	Opt.; to 40.8K bps	Opt.; to 40.8K bps	Opt.; to 40.8K bps	No
Asynchronous	Opt.; 38.4K bps	Opt.; 38.4K bps	Opt.; 38.4K bps	Up to 9600 bps
Protocols supported	—	—	—	Bisync
Network architectures supported	—	—	—	SNA
RJE terminals emulated	HASP terminals	HASP terminals	HASP terminals	2780/3780
IBM 3270 emulation	—	—	—	Yes
PERIPHERAL EQUIPMENT				
Floppy disk (diskette) drives	No	No	No	3154K bytes
Disk pack/cartridge drives	Both; .1-19.26B bytes	Both; 1-19.26B bytes	Both; .1-19.26B bytes	Removable; to 90MB
Drum/fixed-head disk storage	Fixed-head; 5-40M bytes	Fixed-head; 5-40M bytes	Fixed-head; 5-40M bytes	Fixed; 288M bytes
Magnetic tape cassettes/cartridges	No	No	No	No
Magnetic tape, ½-inch	36K-1.2M bps	36K-1.2M bps	36K-1.2M bps	120 KBS
Serial printer	340 cps	340 cps	340 cps	30, 120, 200 cps
Line printer	300-900 lpm	300-900 lpm	300-900 lpm	250, 600 lpm
Data communications interface	40K bps	40K bps	40K bps	To 9600 bps
CRT	1920 characters	1920 characters	1920 characters	80 x 16 characters
Other supported peripheral units	A/D, D/A, digital I/O, high-speed data interface	A/D, D/A, digital I/O, high-speed data interface	A/D, D/A, digital I/O, high-speed data interface	None
SOFTWARE				
Assembler	Assembler & macro assembler	Assembler & macro assembler	Assembler & macro assembler	Assembler & macro assembler
Compilers	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC	FORTRAN, COBOL, BASIC	BASIC, COBOL, RPG II, PL/1, FORTRAN
Operating system	Real-time, interactive, multi-/vector batch	Real-time, interactive, multi-/vector batch	Real-time, interactive, multi-/vector batch	Interactive, multi-user
Data base management system	Yes, TOTAL	Yes, TOTAL	Yes, TOTAL	Yes (ADMS, BDMS)
Language implemented in firmware	FORTRAN RTL (part.)	FORTRAN RTL (part.)	FORTRAN RTL (part.)	Fully
Operating system implemented in firmware	No	No	No	Partially
PRICING & AVAILABILITY				
Price of CPU, power supply, frt. panel, and minimum memory in chassis, $	87,500	85,000	146,000	19,000 (128K)
Monthly maint. of basic configuration above for on-site contract, $	788	842	1,314	240
Discounts available	See 32/57 Comments	See 32/57 Comments	See 32/57 Comments	—
Price of memory increment, $	13,500 (256K bytes)	13,500 (256K bytes)	17,000 (16K x 64-bit)	7,000 (128K)
Date of first delivery	—	—	—	December 1977
Number installed to date	6	6	6	NA
COMMENTS	Includes a 32/77 CPU for scalar arithmetic and a VPU for vector arithmetic	See VPS 3200CM Comments	See VPS 3200CM Comments	Includes 128KB mem., one 308KB floppy disk, 7-slot chassis, cabinets, operating system, plus