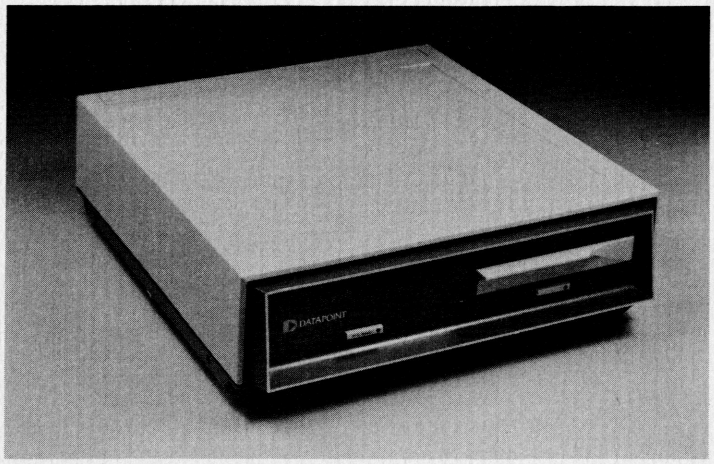
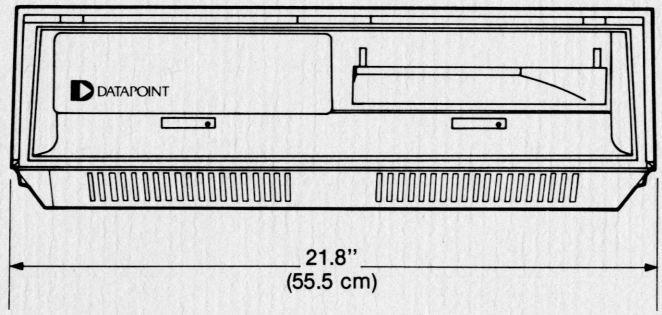
DATAPOINT



Disk Drive

9313/9315



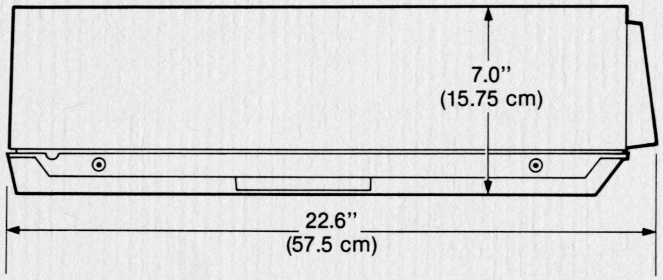


Table of Contents

1.0 GENERAL DESCRIPTION

The Datapoint® 9313/9315 Disk Drive is designed to provide 5 or 10MB of on-line storage capability for Datapoint 1560 and 8600 processors. Both disk drives contain fixed 5.25" Winchester disk drives, disk controllers, and a 1MB floppy diskette for backup. The 9314 and 9316 provide 5 and 10MB of fixed disk storage respectively and do not contain a diskette drive.

In the 9313/9315 drive, the disk drive and controller communicate with the processor via the microbus. Selectable addresses for the controller permit the processor to support up to four 9313/9315 disk drives on the microbus.

The 9313/9315 uses a 5.25" diameter oxide-coated disk. The disk is supplied ready for use; no formatting is necessary.

The diskette drive contained in the 9313/9315 is designed to provide backup on double-sided, double-density diskettes.

2.0 SYSTEM REQUIREMENTS

All communications between the 9313/9315 and the processor are via the I/O microbus. The I/O microbus is composed of an eight-bit command and data bus, two command strobes, an interrupt request line, and an interrupt acknowledge line.

The cable used on the I/O microbus is a 26-conductor flat cable having an integral shield. The connectors are 26-pin locking sockets with integral strain relief. The daisy-chaining of peripherals is accomplished by having two connectors on each disk drive. The connectors on the flat cable are female at both ends.

The maximum I/O microbus length is 10 feet, measured from the microbus connector of the processor to the microbus connector of the last peripheral on line.

3.0

TECHNICAL DESCRIPTION

3.1

Disk Characteristics

	5 or 10MB Disk Drives
Rotational Speed	3600 RPM
Bytes/Sector	256
Sectors/Track	32
Bytes/Disk	4,997,120
Disks/unit:	
9313/9314	1
9315/9316	2
Head Positioning:	
Average	85 ms
Maximum	205 ms
Drive Start/Stop	20 seconds
Average Latency	8.33 ms

3.2

Diskette Characteristics

Rotational Speed	360 RPM
Average Latency	83 ms
Access Time	10 ms (track-to-track)
Settling Time	50 ms
Bytes/Sector	256
Sectors/Track	26
Tracks/Side	77
Bytes/Diskette	1,025,024
Bits/Inch	6600
Buffer Size	256

3.3

Operator Controls and Indicators

3.3.1

Main AC Power Switch

A three-position switch is located inside the rear access panel of the disk cabinet. This switch controls primary AC power for the disk drive. Push the switch to the local position if the disk drive is to be powered on manually. Push the switch to the remote position if the drive is to be powered on or off by the Datapoint processor. Push the switch to the OFF position if the drive is to be powered off manually.

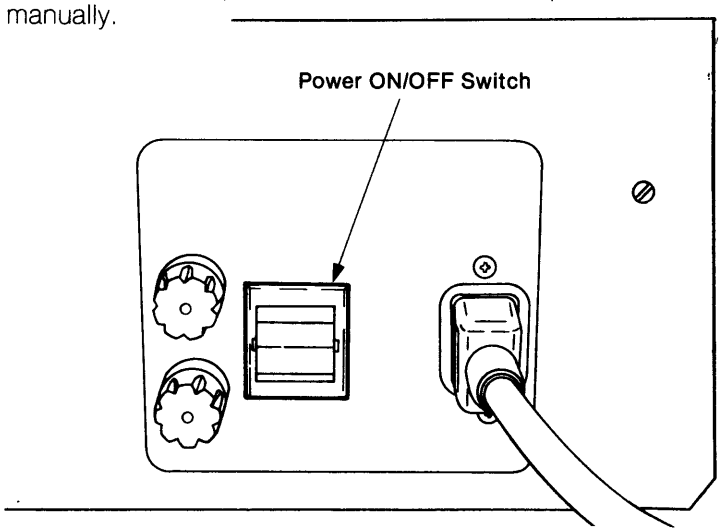


Figure 3-1: Main AC Power Switch

3.3.2

Write Protect

A Write Protect switch and indicator light are provided on the front of the cabinet. When the Write Protect switch is in the Protect position and the indicator light is on, the controller inhibits all write functions to the disk and the drive becomes a read-only drive. The write-protect function will not be activated until all data transfer operations in progress have been completed. See Figure 3-2.

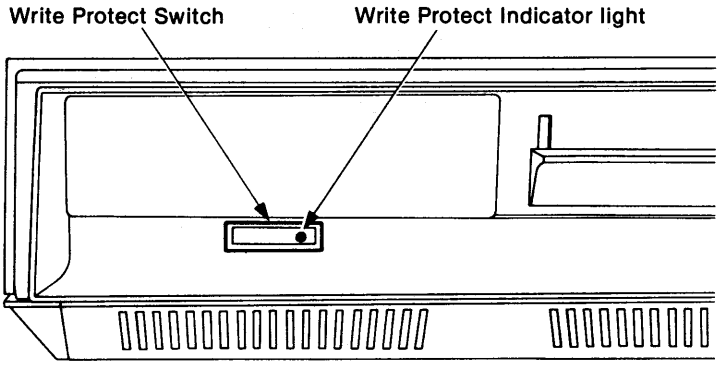


Figure 3-2: Write Protect Switch and Indicator Light

3.4

Disk Operations

In a typical sequence of operations, the disk drive is powered-up, the spindle motor starts and, when the speed reaches 3600 rpm, the read and write heads are positioned over track 000 and the ready signal is sent to the controller.

The processor addresses the disk over the parallel I/O microbus.

3.4.1

Write Operations

The processor selects the disk surface and track on which the data is to be stored. When the sector position read from the disk agrees with the sector address from the processor, data is read from the controller buffer, one byte at a time, and is sent to the disk drive to be written to the sector. The entire content of the buffer is written onto one sector.

3.4.2

Read Operations

The read process is the inverse of the write process. The processor addresses the disk surface, track, and sector from which it wishes to read data and commands the controller to read data from the disk. When the addressed sector is reached, the data is transferred from the disk, deserialized into 8 bit-parallel form, and loaded into the buffer. All 256 bytes in the sector are read into the buffer. The processor then reads the buffer, one byte at a time.

3.4.3

Disk Format

The disk is shipped with formatting already recorded. The formatted disk contains 32 sectors per track, each sector containing 256 bytes. In addition, there are six bytes per sector allowed for the Error Correcting Code (ECC), which is calculated by the controller. The beginning of each track is indicated with an index mark.

3.5

Disk Controller Commands

All communications between the disk controller and the processor are via the microbus using the External Command instructions and the I/O register of the processor.

The eight-bit command bus carries four bits of address and four bits of command from the processor to the disk controller. The command format is as follows:

Processor register

CMD3	CMD2	CMD1	CMD0	A3	A2	A1	A0

CMD0 through CMD3 contain the command and A0 through A3 contain the disk controller address. The controller address is specified by four bits in an eight-position, dual in-line package (DIP) switch on the controller board. The command bits correspond to the following commands:

Basic Command Set

CMD3	CMD2	CMD1	CMD0	Command
0	0	0	0	READ STATUS BYTE 1
0	0	0	1	READ BUFFER
0	0	1	0	READ STATUS BYTE 2
0	0	1	1	READ SYSTEM ID BYTE 1
0	1	0	0	READ SYSTEM ID BYTE 2
0	1	0	1	SET BUFFER POINTER
0	1	1	0	SET TRACK MSB & HEAD
0	1	1	1	SET TRACK LSB
1	0	0	0	ESCAPE
1	0	0	1	Not Used (ignored by the controller)
1	0	1	0	WRITE BUFFER
1	0	1	1	RESTORE
1	1	0	0	RESET
1	1	0	1	READ SECTOR
1	1	1	0	WRITE SECTOR
1	1	1	1	WRITE/VERIFY SECTOR

Augmented Command Set

CMD3	CMD2	CMD1	CMD0	Command
0	0	0	0	Not defined
0	0	0	1	Not defined
0	0	1	0	Not defined
0	0	1	1	Not defined
0	1	0	0	Not defined
0	1	0	1	Not defined
0	1	1	0	INTERRUPT MASK ON/OFF
0	1	1	1	LOAD DRIVE NUMBER
1	0	0	0	PHYSICAL SEEK
1	0	0	1	FORMAT TRACK
1	0	1	0	SET BUFFER PAGE
1	0	1	1	WRITE LONG
1	1	0	0	READ LONG
1	1	0	1	READ SECTOR WITHOUT MAPPING
1	1	1	0	WRITE SECTOR WITHOUT MAPPING
1	1	1	1	WRITE/VERIFY SECTOR WITHOUT MAPPING

Bits A0-A3 of the command byte address the controller. Legal addresses are the following:

A3	A2	A1	A0	Decimal Address
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11

3.5.1

INPUT Commands

The specific Input Command is placed on the COM0 through COM3 lines of the microbus. The controller address is placed on the Address 0 through Address 3 lines of the microbus. When Strobe 1 is issued, the contents of the D0-D7 lines of the microbus are transferred to a register in the processor. The command bits correspond to the following instructions:

READ STATUS 1-Transfers the contents of the controller's status byte 1 through the microbus to a processor register. Bit values in STATUS BYTE 1 have the following meanings:

READ STATUS BYTE 1 Bit Settings

Bit	Status	Description
0	ON-LINE	Sets when drive indicates READY to SEEK/READ/WRITE. Clears when the READY signal is off.
1	TRANSFER IN PROGRESS	Sets when a READ, WRITE, or WRITE/VERIFY command is given. Clears when: -operation is complete -SECTOR NOT FOUND is set -TRANSFER ERROR is set.
2	UNIT BUSY	Sets when the RESTORE command is given. Clears when operation is complete or a seek error is detected.
3	SEEK ERROR	Sets when: -SEEK TIME-OUT ERROR occurs. -ADDRESS PARITY ERROR occurs. -DISK FAULT occurs. Clears when a RESTORE command is given.
4	TRANSFER ERROR	Sets when: -DATA ECC ERROR occurs. -DISK FAULT ERROR occurs. -WRITE PROTECT ERROR occurs. -BUFFER PARITY ERROR occurs. Clears when any of the preceding conditions is cleared. **Note:**STATUS BYTE 2 indicates which condition caused the TRANSFER ERROR.
5	WRITE PROTECTED	Sets when the disk is write protected (if the WRITE PROTECT switch is on).

		Note: The WRITE PROTECT error status bit will be set if a WRITE SECTOR or WRITE/VERIFY SECTOR command is issued when the WRITE PROTECT bit is set. Clears when the WRITE PROTECT switch is off.
6	SECTOR NOT FOUND	Sets when a TRANSFER IN PROGRESS has been on for 16 revolutions without finding the correct sector. Clears when a READ, WRITE, or WRITE/VERIFY SECTOR command is given, or when a RESET or RESTORE occurs.
7	DEVICE RESTART	Sets when power on reset from the power supply occurs. Resets when a RESTORE occurs. **Note:** When the disk is first powered up, the Device Restart Latch is set. The first command to the disk must be a RESTORE in order to reset this latch. This latch will disable WRITE ENABLE when set.

READ BUFFER-Transfers the contents of the buffer location specified by the buffer address pointer in the controller through the microbus into a register in the processor. The buffer address pointer is incremented. Note: This command should not be issued when a TRANSFER IN PROGRESS status is indicated.

READ STATUS 2-Transfers the contents of STATUS BYTE 2 through the microbus to the processor register. Bit values in STATUS BYTE 2 have the following meanings:

READ STATUS BYTE 2 Bit Settings

Bit	Status	Description
0	WRITE PROTECT ERROR	Sets when the WRITE PROTECT switch is on and a WRITE SECTOR or WRITE/VERIFY SECTOR command is given. (The WRITE commands are not executed.) Clears when a RESET is given, a WRITE SECTOR or WRITE/VERIFY SECTOR is given after the WRITE PROTECT switch is off or a RESTORE is given.
1	TRANSFER TIME-OUT ERROR	Not implemented-Always 0.
2	SECTOR OVERRUN ERROR	Not implemented-Always 0.
3	ECC ERROR	Sets when an uncorrectable error occurs on a READ SECTOR or WRITE/VERIFY SECTOR command. Clears when a READ, WRITE, WRITE/VERIFY SECTOR, RESET, or RESTORE command is given.
4	DISK FAULT	Sets when the drive indicates any of the following fault conditions: •Seek fault or illegal seek address •Write fault: -No Write Current with Write Enable -No Write Clock transition after Write Enable -Write Current on without Write Enable •Illegal Procedure -Disk Strobe 1 or Strobe 2 given when ready to seek; read or write is not valid or during a sector mark. -Read or Write command given when drive is not ready. -Write command given when WRITE PROTECT is on. -Read Enable and Write Enable on simultaneously. •Power loss to,the drive. •Fault line broken. •Device malfunction. Clears when a RESTORE command is given.
5	ID ECC ERROR	Sets when an error is detected in the ID field.
6	SEEK TIME-OUT ERROR	Sets when a SEEK or RESTORE command is not complete within 256 revolutions. Clears when a RESTORE command is given.
7	BUFFER PARITY ERROR	Sets when a parity error occurs on a READ BUFFER, WRITE SECTOR, or WRITE/VERIFY SECTOR command. Clears when a RESTORE or RESET command is given.

READ SYSTEM ID-Transfers the device identification code to a processor register. The identification code for the disk controller is 00000001.

READ ID BYTE 2-This command will transfer the device identification code through the micro I/O bus lines to the processor. The ID byte 2 code for the 9313/9315 is 00000001.

3.5.2

OUTPUT Commands

The output command uses the command and address bits in the same manner as the input command. The processor register contains the data to be sent to the controller via the D0-D7 lines of the microbus.

3.5.2.1

Buffer Commands

Buffer commands must not be issued if the TRANSFER IN PROGRESS status is indicated by the controller.

SET BUFFER POINTER-Sets the controller's buffer address pointer to the contents of the appropriate processor register. The next WRITE BUFFER or READ BUFFER command will go to the pointed buffer location. After the disk read or write sector operation, the buffer address pointer is set to 000.

SET BUFFER PAGE-Transfers the contents of the data bus to the Buffer Page Register. Valid page numbers are 0, 1, and 2. Page 3 is reserved for the controller's internal use. The page number is set to 0 at power-on initialization. It is changed only by execution of this command; it is not affected by buffer pointer overflow. The Page Pointer addresses the buffer both for disk operations and for processor operations.

WRITE BUFFER-Transfers the contents of the appropriate processor register to the buffer location specified by the buffer address pointer and increments the pointer.

3.5.2.2

Disk Commands

These commands interact with the controller and the disk and should not be issued if UNIT BUSY, SEEK ERROR, or TRANSFER IN PROGRESS status is indicated or if ONLINE is not true.

SET TRACK MSB-Transfers the two low-order bits of the processor register to the two high-order bits of the controller's ten-bit Track Address register.

SET TRACK LSB-Transfers the contents of the processor register to the eight low-order bits in the controller's Track Address register.

ESCAPE-The ESCAPE command points the controller to the Augmented Command Set. The next command from the processor will be from the Augmented Commands.

RESTORE-Must be issued whenever a SEEK ERROR condition is detected. The RESTORE command resets the following error flags:

SEEK ERROR
TRANSFER ERROR
WRITE PROTECT ERROR
ECC ERROR
DISK FAULT
ADDRESS PARITY ERROR
SEEK TIME-OUT ERROR
SECTOR NOT FOUND
BUFFER PARITY ERROR
DEVICE RESTART

The RESTORE command resets the disk drive to track 000, surface 0. The RESTORE command can be issued only when ON-LINE is active, TRANSFER IN PROGRESS is inactive, and UNIT BUSY is inactive.

READ SECTOR-Transfers the contents of a processor register to the controller's Sector Address register and causes the controller to read that sector into its buffer. Valid sectors are 0 to 47 (decimal).

The data transfer is preceded by an implied seek to the proper cylinder if the heads are not already properly positioned. Firmware sector mapping is used.

While the READ operation is taking place, the TRANSFER IN PROGRESS bit is set true. If the sector specified is not found, the TRANSFER IN PROGRESS status bit is set false and the SECTOR NOT FOUND status bit is set true.

If a DATA error occurs and the ECC check is unsuccessful, the TRANSFER IN PROGRESS status is removed and the ECC ERROR and TRANSFER ERROR status bits are set.

WRITE SECTOR-Transfers the contents of the processor register to the controller's Sector Address register and causes the controller to write the contents of its buffer to that sector. Valid sectors are 0 to 47 (decimal).

The TRANSFER IN PROGRESS status bit is set while the write operation is in progress.

If the specified sector is not found, the TRANSFER IN PROGRESS status is removed and SECTOR NOT FOUND status is set.

WRITE/VERIFY SECTOR-Transfers the contents of the processor register to the controller's Sector Address register and causes the controller to perform a write operation on the specified sector as described under WRITE SECTOR. The controller then performs a READ operation on the same sector on the next revolution and performs a ECC check without transferring any data back from the disk sector to the controller's buffer. The data transfer is preceded by an implied seek, if necessary.

The TRANSFER IN PROGRESS status bit is true while the WRITE/VERIFY operation is in progress.

If the target sector is not found on either phase of the command, the TRANSFER IN PROGRESS status is removed and the SECTOR NOT FOUND status bit is set.

If a data error occurs during a read-back and the ECC check is unsuccessful, the TRANSFER IN PROGRESS status is removed and ECC ERROR and TRANSFER ERROR status is set.

3.5.3
RESET Command

The RESET command resets error status bits within the controller. The following error status bits are set false:
WRITE PROTECT ERROR
ECC ERROR

3.6
Diskette Operations

3.6.1
Write Operations

Before double-density data is written to a sector, a two-byte DC Gap is written to the ID field to identify the sector as a double-density sector.

When writing a DC Gap to a sector, the first nine bytes of hex FF in the ID field are identified and skipped; then the Write Gap is enabled for a period of two bytes (FM). During this period, no pulses will be on the Write Data output. When writing double-density data to a double-density sector, the controller will search for a DC Gap. After the DC Gap is found, 12 bytes of hex AA (MFM) will be written, followed by a two-byte (MFM) Data Address Mark. The controller will then write 256 bytes of MFM data followed by two CRC bytes (FM, computed from the Data Address Mark through the last data byte) and one byte of hex FF. Note: The Data Address Mark and the two-byte CRC will be written in FM mode, the equivalent of 2 and 4 bytes respectively in MFM mode.

Figure 3-3 contains a diagram of sector formats after initialization and after writing double-density data.

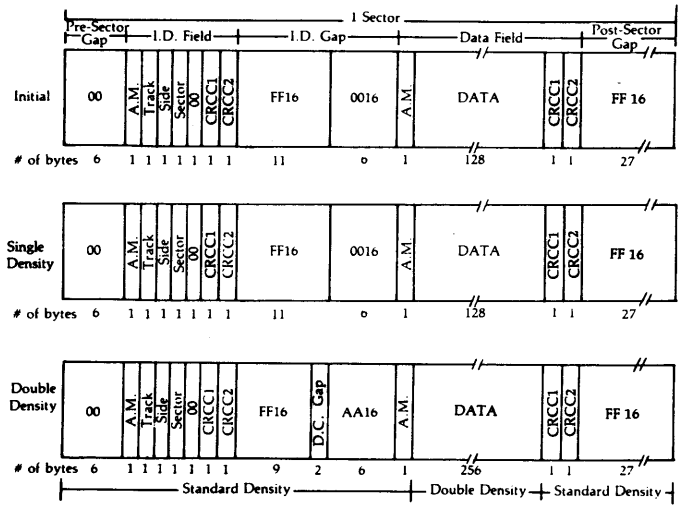


Figure 3-3: Diagram of Sector Formats

3.6.2

Buffer Operations

The internal data buffer in the controller matches transfer speeds of the I/O microbus and diskette drive electronics. The buffer holds 256 eight-bit bytes and can be randomly or sequentially accessed.

Addressing is accomplished with two pointers called the Processor Pointer and the Disk Pointer. The Processor Pointer can be loaded from the I/O microbus using the OUTPUT PROCESSOR POINTER command (see Section 3.7.13). After each processor access of the buffer, the processor pointer is incremented.

The Disk Pointer can be initialized to the beginning of either of the two 128 byte pages. Execution of the OUTPUT DISK PAGE COMMAND (Section 3.7.14) loads the value of bit 7 of the I/O microbus into the Disk Page register and resets the Disk Pointer to zero.

When either buffer pointer is incremented by the diskette controller from location 255, the new location will become 0. Do not depend on this wrap-around for resetting the pointers to zero, since any addressing error will affect every buffer access following the error.

Data transfers to or from the processor can occur at the same time that transfers are being made to or from the diskette. Contention for buffer accesses is resolved by the diskette controller.

3.7

Diskette Controller Commands

Actual control of the diskette is provided by a controller chip which contains track, sector, command, and data registers referred to in Table 3-1.

D7	D6	D5	D4	Command
0	0	0	0	INPUT STATUS
0	0	0	1	INPUT DATA
0	0	1	0	OUTPUT SECTOR NUMBER
0	0	1	1	INPUT ID BYTE
0	1	0	0	FETCH STATUS
0	1	0	1	FETCH TRACK
0	1	1	0	FETCH SECTOR
0	1	1	1	FETCH DATA
1	0	0	0	MASTER COMMANDS
1	0	0	1	OUTPUT TRACK NUMBER
1	0	1	0	OUTPUT DATA
1	0	1	1	OUTPUT SEEK NUMBER
1	1	0	0	OUTPUT PROCESSOR POINTER
1	1	0	1	OUTPUT DISK PAGE
1	1	1	0	SELECT DRIVE
1	1	1	1	INTERRUPT MASK

Table 3-1: Command/Address Bus Bits

3.7.1

Control Commands

INPUT STATUS
Places device status on the I/O microbus data lines. Definition of status bits depends upon the previously executed instruction.

INPUT ID BYTE
The ID byte is defined as octal 041 for the single-sided diskette and octal 042 for the double-sided diskette.

OUTPUT DATA
Transfers the contents of the I/O microbus data lines to the buffer location specified by the processor pointer. The pointer is incremented at the completion of the instruction.

INPUT DATA
Transfers data from the buffer location specified by the processor pointer to the microbus data lines. The processor pointer is incremented at the completion of this instruction.

FETCH STATUS
Sets up the status word for the INPUT STATUS command. FETCH STATUS must precede an INPUT STATUS command for valid status.

FETCH TRACK
When followed by the INPUT STATUS command, allows the processor to examine the track register in the controller chip.

FETCH SECTOR
When followed by the INPUT STATUS command, allows the processor to examine the sector register on the controller chip.

FETCH DATA
When followed by the INPUT STATUS command, allows the processor to examine the data register in the controller chip.

MASTER COMMAND
Transfers the contents of the I/O microbus data lines to the command register of the controller chip. Do not issue the MASTER COMMAND if Status Bit 0 (Busy) is set, or an undetermined condition will result. Loading the command register causes Status Bit 0 to be set until the specified operation is completed. (Minimum duration of the busy state is 12 microseconds.) The operations that are performed are determined by the value of the data lines. For a detailed description of the operations and their corresponding codes, see Section 3.7.2.

OUTPUT TRACK NUMBER
Writes the value on the I/O microbus data lines into the track register in the controller chip.

OUTPUT SECTOR NUMBER
Writes the value on the I/O microbus data lines into the sector register in the controller chip.

OUTPUT SEEK NUMBER
Loads the value of the I/O microbus data lines into a temporary disk register. That value is the desired track position when executing a SEEK command.

OUTPUT PROCESSOR POINTER
Loads the value of the I/O microbus data lines into the Processor Pointer register. Following execution of the command, the contents of the buffer are transferred to the

input data register. The processor pointer is not incremented.

OUTPUT DISK PAGE
Loads the value of I/O microbus line 7 into the disk page register and resets the disk pointer to zero.

SELECT DRIVE
Loads the value of the I/O microbus data lines 0, 1, 2, and 3 into the Drive Select/Light Register. A zero on data line 0 selects drive 0; a one on data line 0 selects drive 1. Data line 1 must be zero. A one on data line 2 illuminates the drive 0 indicator; a one on data line 3 illuminates the drive 1 indicator.

INTERRUPT MASK.
The interrupt sources will be either enabled or disabled, depending on the value of the I/O microbus data lines. A one bit will enable interrupting, and a zero bit will inhibit interrupts from that source. Interrupts are inhibited at power-up, until enabled by the processor. Interrupt bit assignments are as follows:

Bit Interrupt
0 Controller chip
1 Processor pointer equal to disk pointer
2 Not used
3 Enable interrupt mask (Mask flip-flops will be unchanged except when bit 3 is a one)
4 Clear controller chip interrupt request flip-flop

3.7.2

Master Commands

The controller chip in the diskette drive accepts master commands from the processor. Command words should not be loaded into the command register when the Busy status bit is on (status bit 0). The one exception is the Force Interrupt command. Whenever a command is executed, the Busy status bit is set.

When a command is completed, an interrupt is generated and the Busy status bit is reset. The status register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types and are summarized in Table 3-2.

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	RESTORE	0	0	0	0	1	V	1	0
I	SEEK	0	0	0	1	1	1	1	0
I	STEP IN	0	1	0	1	1	1	1	0
I	STEP OUT	0	1	1	1	1	1	1	0
II	READ SECTOR FM	1	0	0	0	$\overline{S}$	0	0	0
II	READ SECTOR MFM	1	0	0	0	$\overline{S}$	0	1	0
II	WRITE SECTOR FM	1	0	1	0	$\overline{S}$	0	0	a0
II	WRITE SECTOR MFM	1	0	1	0	$\overline{S}$	0	1	0
II	WRITE DC GAP	1	1	1	0	$\overline{S}$	0	0	0
III	READ ADDRESS	1	1	0	0	$\overline{S}$	0	0	0
IV	FORCE INTERRUPT	1	1	0	1	I3	I2	I1	I0

Note: Bits shown in TRUE form.

Table 3-2: Master Command Summary

Type I Master Commands
The Type I commands include the RESTORE, SEEK, STEP IN, and STEP OUT commands. The head is loaded at the beginning of the command. If the controller is idle for 15 revolutions of the diskette, the head will be automatically disengaged.

The RESTORE command contains a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed. If V = 0, no verification is performed.

After a SEEK, STEP IN, or STEP OUT is finished, the first encountered ID field is read off the diskette. The track address of the ID field is then compared with the track register. If there is a match and a valid ID CRC, the verification is complete; an interrupt is generated, and the Seek Error status bit (0) is reset. If there is a match but not a valid CRC, the CRC error status bit (status bit 3) is set, and the next encountered ID field is read from the diskette for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the diskette, the controller chip terminates the operation and sends an interrupt (INTRQ).

The STEP IN and STEP OUT commands update that track register by one for each step.

RESTORE
Upon receipt of this command, the Track 00 Detector is sampled. If the Read-Write head is positioned over track 0, the track register is loaded with zeroes and an interrupt is generated. If track 0 is not detected, stepping pulses are issued until track 0 is detected. At this time the track register is loaded with zeroes, and an interrupt is generated. If track 0 is not detected after 255 stepping pulses, the controller will terminate the operation and set the Seek Error status bit.

SEEK
The SEEK command assumes that the track register contains the track number of the current position of the Read/Write head and the data register contains the desired track number. The controller will update the track register and issue stepping pulses in the appropriate direction until the contents of the track register are equal to the contents of the data register (the desired track location). A verification operation then takes place.

The head will be loaded at the start of the command. An interrupt is generated at the completion of the command.

If a SEEK command is issued to the current track, the busy status bit will be set and will remain set for approximately 250 microseconds. When the operation is complete, the busy status bit will be reset, and a command-complete controller chip interrupt will be generated.

If a SEEK command is attempted to a track number greater than 76, the head will be moved to track 76 and step pulses will be generated as if the track number is valid with the motor against a hard stop. If the verify flag is set, a seek error status bit will be set. If the verify flag is not set, the next read or write operation will probably fail.

STEP IN

Upon receipt of this command, the controller will issue one stepping pulse in the direction toward track 76. The track register is incremented by one. After a 30 msec delay, a verification takes place. The head will still be loaded at the completion of the command.

STEP OUT

Upon receipt of this command, the controller will issue one stepping pulse in the direction toward track 0. The track register is decremented by one. After a 30 msec delay, a verification takes place. The head will still be loaded at the completion of the command.

TYPE II MASTER COMMANDS

The Type II commands are the READ SECTOR and WRITE SECTOR commands. Prior to loading the Type II command into the command register, the processor must load the sector register with the desired sector number. Upon receipt of the Type II command, the busy status is set.

When an ID field is located on the diskette, the controller compares the track number of the ID field with the track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the sector number of the ID field is compared with the sector register. If there is not a sector match, the next encountered ID field is read off the diskette and comparisons again are made. If the ID field CRC is correct, the data field is then located and either written into or read from, depending on the command. The controller must find an ID field with a track number, sector number, and CRC within five revolutions of the diskette; otherwise, the Record Not Found status bit (status bit 4) is set and the command is terminated with an interrupt.

READ FM SECTOR

Upon receipt of this command, the head is loaded and the Busy status is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the 128 bytes are transferred to the buffer. The data address mark of the data field must be found within 30 bytes of the last ID field CRC byte. If not, the Record Not Found status bit is set and the operation is terminated.

If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated. At the end of the read operation, the type of data address mark encountered in the data field is recorded in the status register (bit 5) as shown below:

Status Bit 5	**Type of Address Mark**
1	Deleted Data Mark
0	Data Mark

READ MFM SECTOR

Upon receipt of this command, the head is loaded and the busy status bit is set, and when an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the controller then searches for a field at least 32 microseconds long having no transitions (DC gap). If this gap is located within 30 MFM bytes (480 microseconds) after the header CRC, the controller then searches for a Data ID Sync byte. This byte must be found within 20 MFM bytes (320 microseconds) after the DC gap. If neither DC gap nor sync is found in time, the Record Not Found status bit is set and the operation is terminated. When the controller finds a sector which has a correct track number, correct side bit, correct sector number, correct CRC, a proper DC gap, and correct data ID mark, then 256 bytes of data are transferred to the buffer. If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated.

WRITE FM SECTOR

Upon receipt of this command, the head is loaded and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, a data sector is written. The controller counts nine bytes from the CRC field, the Write Gate (WG) output is made active, and eight bytes of zeroes are then written on the diskette. At this time the data address mark is written on the diskette as determined by the a0 field of the command as shown below:

a0	**Type of Address Mark**
1	Deleted Data Mark
0	Data Mark

The controller then writes the data field from the buffer. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of logic ones. The Write Gate output is then deactivated.

WRITE MFM SECTOR

Upon receipt of this command, the head is loaded, the Read Gate is set, and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the controller then counts off the equivalent of 11 bytes (FM) from the CRC field and the Write Gate output is made active if a DC Gap has been detected (at least 32 microseconds with no transitions). If a DC Gap is not detected, the command is terminated and the Record Not Found status bit is set. If a DC Gap has been detected, the Write Gate is made active and 12 bytes of hex AA are written on the diskette. This is followed by a two-byte MFM data address mark.

The controller then writes the data field. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of hex FF. The Write Gate output is then deactivated.

Note: The address mark and the two-byte CRC are written in FM mode, the equivalent of 2 and 4 bytes, respectively, in MFM. The CRC calculation includes the one-byte FM data address mark.

WRITE DC GAP

Upon receipt of this command, the head is loaded, the Busy status bit is set, and the Read Gate is enabled. When the ID field is encountered that has the correct track number, correct side bit, correct sector number,

and correct CRC, the controller counts 9 bytes (FM) and turns on the Write Gate for a period of 2 bytes (64 usec). During the period that the Write Gate is on, there are no pulses on the Write Data output.

Bit	Description
a0	Data Address Mark (Bit 0) a0 = 0, FB (Data Mark) a0 = 1, F8 (Deleted Data Mark)
s	Side Bit (Bit 3) (negative true) s = 0, Side One s = 1, Side Zero

Table 3-3: Type II Command Bit Summary

TYPE III MASTER COMMANDS

READ ADDRESS

Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read in from the diskette, and the six data bytes of the ID field are assembled and transferred to the buffer at the location addressed by the disk pointer. The six bytes of the ID are as follows:

1 Track Address
2 Side Number (0 = side zero; 1 = side one)
3 Sector Address
4 Sector Length
5 CRC1
6 CRC2

Although the CRC characters are transferred to the buffer, the controller checks for validity and the CRC error status bit is set if there is a CRC error. The track address of the ID field is written into the sector register in the controller chip. At the end of the operation, an interrupt is generated and the Busy status bit is reset.

The only command bit for a Type III command is the Side Bit (bit 3). The side bit equals 0 for side one; one for side zero.

TYPE IV MASTER COMMANDS

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy status bit set), the command will be terminated and an interrupt generated when the condition specified in the I0 through I3 field is detected. The interrupt conditions are shown in Table 3-4.

Interrupt Bits	Description
I0 = 1	Not-ready to Ready transition
I1 = 1	Ready to Not-ready transition
I2 = 1	Index Pulse
I3 = 1	Immediate Interrupt

Note: If I0 through I3 are zero, there is no interrupt generated, but the current command is terminated and the Busy status bit is reset. FORCE INTERRUPT is the only command that will clear the immediate interrupt.

Table 3-4: Type IV Commands Summary

STATUS DESCRIPTION

Upon receipt of any command, except the FORCE INTERRUPT command, the Busy status bit is set and the rest of the status bits are updated or cleared for the new command. If the FORCE INTERRUPT command is received when there is a current command under execution, the Busy status bit is reset and the rest of the status bits remain unchanged. If the FORCE INTERRUPT command is received when there is not a current command under execution, the Busy status bit is reset and the rest of the status bits are updated or cleared. In this case, the Busy status bit reflects the Type I commands.

The significance of each bit in the status register varies with the command being executed. Status bits, when set, have the following meanings:

TYPE I COMMAND

Status Bit	Meaning
7	Drive not ready
6	Write protection activated
5	Head loaded and engaged
4	SEEK ERROR-desired track not verified
3	CRC error in either the ID or data field
2	Read/Write head positioned to track 0
1	Index mark detected from the drive (true only for duration of index pulse)
0	Busy-command in progress

READ FM

Status Bit	Meaning
7	Drive not ready
6	Same as bit 5
5	Indicates the record type code from the data field address mark
4	Record not found (desired track and sector not found)
3	CRC error in either the ID or data field
2	Lost data
1	DRQ
0	Busy-command in progress

READ MFM

Status Bit	Meaning
7	Drive not ready
6	Same as bit 5
5	Indicates the record type code from the data field address mark
4	Record not found (track and sector not found)
3	CRC error in either the ID or data field
2	Lost data
1	DRQ
0	Busy-command in progress

WRITE FM

Status Bit	Meaning
7	Drive not ready
6	Write protection activated
5	Write fault
4	Record not found (track and sector not found)
3	CRC error in either the ID or data field
2	Lost data
1	DRQ
0	Busy-command in progress

WRITE MFM

Status Bit	Meaning
7	Drive not ready
6	Write protection activated
5	Write fault
4	Record not found (track and sector not found)
3	CRC error in either ID or data field
2	Lost data
1	DRQ
0	Busy-command in progress

READ ADDRESS

Status Bit	Meaning
7	Drive not ready
6	Two-sided diskette inserted in drive
5	Wide Gap detected within 11 byte times (FM)following the last address field CRC byte
4	Record not found (track and sector not found)
3	CRC error in either the ID or data field
2	Lost data
1	DRQ
0	Busy-command in progress

WRITE DC GAP

Status Bit	Meaning
7	Drive not ready
6	Write protection activated
5	Write fault
4	Record not found (track and sector not found)
3	CRC error in either ID or data field
2	Always 0
1	DRQ
0	Busy-command in progress

INTERRUPT REQUESTS

There are two sources for the "Interrupt Request" signal in the diskette controller, the Pointers Equal interrupt and the Controller Chip interrupt.

CONTROLLER CHIP INTERRUPT

This interrupt request is generated from the controller chip if mask bit 0 is set and any of the following conditions occur:

1. Not-ready to Ready transition
2. Ready to Not-ready transition
3. Index pulse
4. Immediate
5. Command complete

With the exception of the command complete interrupt, these interrupts can be individually masked with a FORCE INTERRUPT master command. If any of the preceding conditions occurs, or a controller chip interrupt master command is completed, an Interrupt Request will be generated.

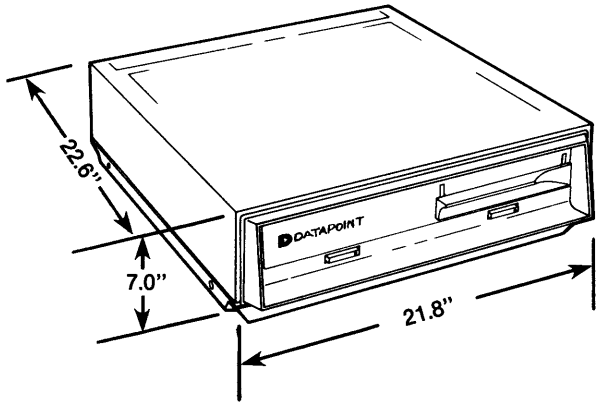
INTERRUPT ACKNOWLEDGE

The diskette controller will respond to the Interrupt Acknowledge signal from the processor if it has previously generated an Interrupt Request by not forwarding the Interrupt Acknowledge (IACK) signal to additional peripheral devices and by placing an interrupt status byte on the I/O microbus data lines as follows:

Bit 0-3	Peripheral device address
Bit 4	Processor pointer equal to disk pointer interrupt
Bit 5	Controller chip interrupt
Bit 6	Drive number
Bit 7	Head number

If no Interrupt Request signal is generated, the diskette controller will generate an IACK OUT signal in response to the IACK IN signal. The IACK OUT then becomes an IACK IN to the next device on the I/O microbus. The priority of interrupting devices on the I/O microbus is the same as the order in which they appear on the microbus daisy chain beginning at the processor.

4.0 PHYSICAL DESCRIPTION



Width:	*21.8 inches (55.5 cm)*
Height:	*7.0 inches (15.75 cm)*
Depth:	*22.6 inches (57.5 cm)*
Weight:	*75 pounds (34.1 kg)*

5.0 ENVIRONMENTAL REQUIREMENTS

Temperature:	50 — 100° F (10 — 38° C)
Humidity:	10 — 90% non-condensing
Heat Dissipation:	855 BTU/hr

WARNING: This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a

residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

6.0

INTERFACE REQUIREMENTS

6.1

Microbus Pin Assignments

Pin	Signal
1	Ground
2	Strobe 1
3	Ground
4	Strobe 2
5	Ground
6	IACK
7	Ground
8	Address 0
9	Address 1
10	Address 2
11	Address 3
12	Comm 0
13	Comm 1
14	Comm 2
15	Comm 3
16	Spare
17	Interrupt Request
18	Data 0
19	Data 1
20	Data 2
21	Data 3
22	Data 4
23	Data 5
24	Data 6
25	Data 7
26	+ 5 V (Power Indicator)

6.2

Power Requirements

Power:	115 or 220 VAC, 50 or 60 Hz, +/-3 Hz
Current:	2.2 amps@ 115 VAC 1.2 amps @ 220 VAC
Power Consumption:	250 watts, maximum

7.0

OPTIONS

The 9313/9315 Disk Drive is available in 115 and 220 VAC models. The 9313/9315 is also available in a variety of system configurations.

9313	5MB Disk Drive with 1MB Diskette
9314	5MB Extension Disk Drive
9315	10MB Disk Drive with 1MB Diskette
9316	10MB Extension Disk Drive

8.0

SHIPPING LIST

Quantity	Item
1	*Disk/Diskette Drive*
1	*Diskette*
1	*Product Specification (Document no. 61382)*


DATAPOINT