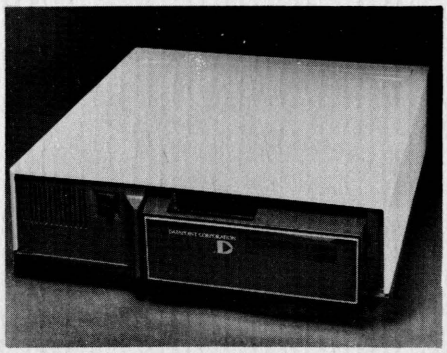
DATAPOINT
Product Specifications

Cartridge Disk Drive
9310/9320



The 9310/9320 Cartridge Disk Drive

December 19, 1980 Document No. 60876

1.0 General Description

The Datapoint 9310/9320 Cartridge Disk Drive is designed to provide extended storage capability for Datapoint entry-level users with 1500 and 1800 Dispersed Processors. The 9310 drive consists of a disk drive and controller. The 9320 drive consists of a disk drive, controller and four-terminal serial interface. The serial interface permits either the 1500 or 1800 processor to be used as a DATASHARE® Business Timesharing system.

The compact, easy-to-handle disk cartridge can store nearly 10 Megabytes (9,633,792 bytes formatted under DOS). Upon removal, a plastic band seals the access opening to keep out dust and smoke particles. The compact (11.1" x 11.2" x .9") cartridges are easily stored and shipped.

In the 9320 drive, the disk drive, controller and serial interface communicate with the processor via the 1500/1800 micro bus. Selectable addresses for the controller and serial interface permit the processor to support up to four 9320 Disk Drive Systems on its micro bus.

Each surface of the cartridge disk contains 392 tracks, each divided into 48 sectors. Each sector is capable of storing 256 bytes of 8-bit data. Data bits are serially written along the sector.

The cartridge contains a 10.5 inch diameter disk, oxide coated on both sides. The cartridge disk is supplied ready for use; no formatting is necessary. The disk is shipped with head and servo data, track address, address parity, and a defective sector flag already recorded.

A 1500 processor with one 9320 Disk Drive and 64K of memory can support up to four workstations, including the console. An 1800 processor with 64K and one 9320 Disk Drive can support up to five workstations, including the console. With 128K and two 9320 drives, the 1800 can support up to nine workstations, including the console. In addition, the 1800 with 64K or 128K and an external Resource Interface Module (RIM) can participate in an Attached Resource Computer™ system as an applications processor.

An 1800 processor with 128K of memory and an external Resource Interface Module can use the 9310 or 9320 to function as an ARC™ file processor.

2.0 System Configuration

2.1 9310/9320 to Processor Interface

All communications between the controller and the processor are via the processor micro bus. The micro bus is composed of an eight-bit command bus, an eight-bit data bus, two command strobes, an interrupt acknowledge line, and an interrupt request line. The micro bus cable is a 26 conductor, flat cable containing an integral ground plane of expanded copper shield. Connection is via 26-pin, female sockets with integral strain relief. Two connectors on each drive permit daisy chaining of peripherals. Maximum cable length is 10 feet.

2.2 9320 to Terminals

The serial interface integral to the 9320 connects to Datapoint 3600 or 8200 Datastations via shielded twisted pair cable. Connection at the interface is through an Amphenol RS-232-C compatible 25-pin female connector. Connection at the Datastation is via an RS-232-C compatible 50-pin male connector.

The integral serial interface is capable of driving 250 feet of shielded twisted pair cable at 9600 baud.

2.3 9310/9320 to Diskette

The 1500 system configuration includes a single-density diskette drive; the 1800 configurations (with 64 or 128K or memory) include the dual-density diskette drive. Connection between the disk drive and back up diskette is via a micro bus.

3.0 Technical Description

3.1 Disk Drive

3.1.1 Cartridge Disk Characteristics

Bit Density	4758 BPI (inner track)
Track Density	508 TPI
Model Code	80501
Bit Transfer Rate	7.35 MHz (to and from buffer)
Byte Transfer Rate	.920 MHz (to and from buffer)

3.1.2 Disk Timing Characteristics

Rotation	3600 RPM
Average Latency Time:	8.33 milliseconds
Head Postioning:	
Average:	75 milliseconds
Maximum:	200 milliseconds
Drive Start/Stop time:	20 seconds

Continued....

3.1.3 Cartridge Disk Format

Bytes/Sector	256
Sectors/Track	48
Tracks/Surface	392
Surfaces/Disk	2
Bytes/Disk	9,633,792
Under DOS:	
Bytes/Sector	256
Sectors/Cluster	24
Clusters/Track	2
Clusters/Cylinder	8
Tracks/Cylinder	4
Cylinders/Logical Drive	49
Logical Drives/Disk	4 (2 per surface)
Bytes/Disk	9,633,792

3.2 Operator Controls and Indicators

3.2.1 Main AC Power Switch

A three-position switch located inside the rear access panel of the disk cabinet. This switch controls primary AC power for the disk drive. Push the switch to the LOCAL position if the disk drive is to be powered on manually. Push the switch to the REMOTE position if the drive is to be powered on or off by the Datapoint processor. Push the switch to the OFF position if the drive is to be powered off manually.

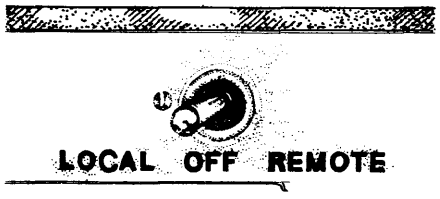


Figure 3-1: Main AC Power Switch

3.2.2 RUN/LOAD Switch

A two-position switch with indicator lights located on the front of the disk cabinet. Push the switch to the LOAD position for cartridge access. The cartridge may be removed when the LOAD indicator light comes on. Push the switch to the RUN position to ready the drive to seek, read, and write. The drive is ready for disk operations when the RUN indicator light comes on.

3.2.3 WRITE PROTECT Switch

A two-position switch with indicator lights located on the front of the disk cabinet. Push the switch to the ON position to enable the WRITE PROTECT feature. The WRITE PROTECT indicator light will come on when this feature is enabled. Note that the WRITE PROTECT feature may be specified either by the switch or by the WRITE PROTECT tag on the cartridge disk.

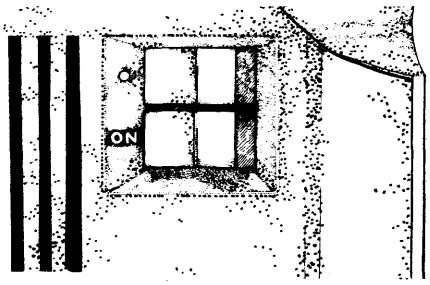


Figure 3-2: RUN/LOAD and WRITE PROTECT Switches

3.2.4 WRITE PROTECT Tag

The WRITE PROTECT tag is a removable metal disk that can be positioned over the write access of the cartridge disk to enable the WRITE PROTECT feature for the specific cartridge.

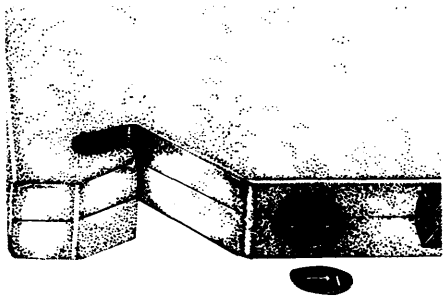


Figure 3-3: WRITE PROTECT Tag

3.3 Cartridge Disk Loading

With the RUN/LOAD switch set to LOAD, open the cartridge compartment on the front right of the drive housing by pulling the cartridge access door toward you. Hold the cartridge disk as shown in Figure 3-4 and carefully insert the cartridge into the compartment. Close the compartment and set the RUN/LOAD switch to RUN. The cartridge will reach operating speed within twenty seconds.

To remove the cartridge disk, set the RUN/LOAD switch to LOAD. When the LOAD indicator light comes on, open the cartridge compartment and remove the cartridge disk.

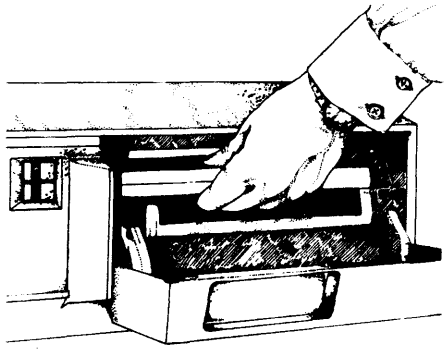


Figure 3-4:Cartridge Disk Loading

3.4 Cartridge Disk Operations

In a typical sequence of operations, the cartridge disk is loaded into the disk drive and the RUN/LOAD switch on the front panel is set to RUN. The disk drive latches the cartridge access door closed, starts the spindle motor, and, when the speed reaches 3600 rpm, positions the read and write heads over track 000 and sends the ready signal to the controller.

3.4.1 Disk Write Operations

The processor then selects the disk surface and track on which the data is to be stored. The disk drive enables the selected read/write head, positions it over the addressed track, and sends a ready signal to the Buffer/Disk Interface (BDI). On command from the processor, the Control/CPU Interface (CCI) enables the write circuits in the controller and tells the BDI to transfer data. When the sector counter on the CCI agrees with the sector address from the processor, data is read from the buffer, one byte at a time, and is sent to the disk drive to be written to the sector. The entire content of the buffer is written onto one sector.

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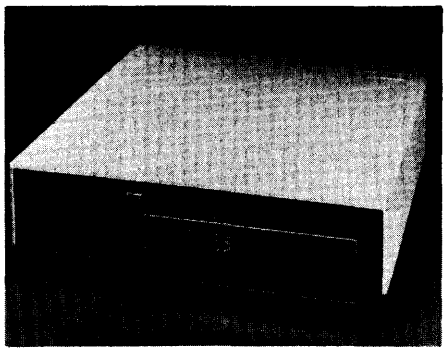
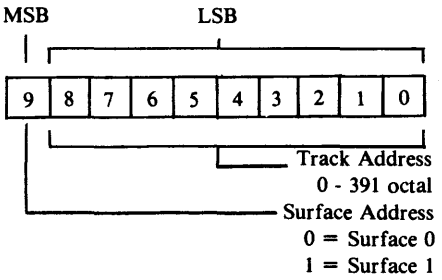


3.4.2 Disk Read Operations

The read process is the inverse of the write process. The processor addresses the disk surface, track, and sector from which it wishes to read data and commands the controller to read data from the disk. When the sector counter reaches the addressed sector, data is transferred from the disk to the BDI where it is deserialized into bit-parallel form and loaded into the buffer. All 256 bytes in the sector are read into the buffer. The processor then reads the buffer, one byte at a time.

The processor addresses the cartridge disk with a 10-bit command. The most significant bit specifies the surface and the nine least significant bits specify the track address.

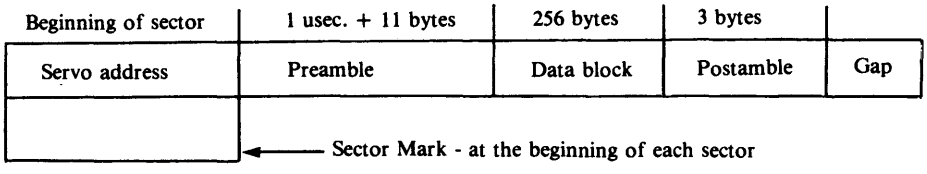
Controller Track Address Register



3.5 Cartridge Disk Format

The cartridge disk is shipped with formatting and servo information already recorded at the beginning of each sector. The formatted disk contains 50 sectors per track, each sector containing 256 bytes. In addition, there are two bytes per sector allowed for CRC, which is calculated by the controller. The beginning of each track is indicated with an index mark.

The sector format is fixed. Each sector contains a servo address zone at the beginning of the sector, followed by a Preamble of 1 usec. + 11 bytes. The Preamble is followed by 256 bytes of data and 3 bytes of Postamble containing a two byte data check field. Following the Postamble is a write turn off and disk-speed tolerance gap.



Servo address zone - contains the track address, servo data, address parity bit, and the valid sector bit.

Preamble - Provides a gap for the controller to send WRITE ENABLE or READ ENABLE, write switching-on time, VFO synchronization, and the data mark.

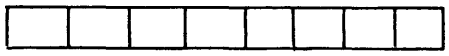
Postamble - Provides a gap for write switching-off time and disk speed tolerance.

3.6 I/O Command Set

All communications between the 9310/9320 disk controller and the Datapoint processor are via the micro bus using the External Command instructions and the I/O register (A register) of the processor. The micro bus is composed of an eight-bit command bus, an eight-bit data bus, two command strobes, an interrupt acknowledge line, and an interrupt request line. For pin assignments, see section 6.0, Interface Requirements.

The eight-bit command bus carries four bits of address and four bits of command from the processor to the 9310/9320 controller. The command format is as follows:

Processor A Register



where CMD0 through CMD3 contain the command and A0 through A3 contain the disk controller address. The controller address is specified by the 4-bit dual in-line package (DIP) switch on the CCI board. The command bits correspond to the following commands:

CMD3	CMD2	CMD1	CMD0	Command
0	0	0	0	READ STATUS BYTE 1
0	0	0	1	READ BUFFER
0	0	1	0	READ STATUS BYTE 2
0	0	1	1	READ SYSTEM ID
0	1	0	0	Not Used (ignored by the controller)
0	1	0	1	SET BUFFER POINTER
0	1	1	0	SET TRACK MSB
0	1	1	1	SET SEEK
1	0	0	0	Not Used (ignored by the controller)
1	0	0	1	Not Used (ignored by the controller)
1	0	1	0	WRITE BUFFER
1	0	1	1	RESTORE
1	1	0	0	RESET
1	1	0	1	READ SECTOR
1	1	1	0	WRITE SECTOR
1	1	1	1	WRITE/VERIFY SECTOR

Bits A0 - A3 of the command byte address the controller. Legal addresses are the following:

A3	A2	A1	A0	Decimal Address
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14

3.6.1 INPUT Commands

When an input command (uBIN) is issued, the contents of the processor A register are transferred to the address/command lines of the micro bus. The four high-order bits of the A register contain the sub-command and are put on the COM0 through COM3 lines of the micro bus. The four low order bits contain the controller address and are put on the Address0 through Address3 lines of the micro bus. When Strobe 1 is issued, the contents of the D0 - D7 lines of the micro bus are transferred to the B register of the processor. The command bits correspond to the following instructions:

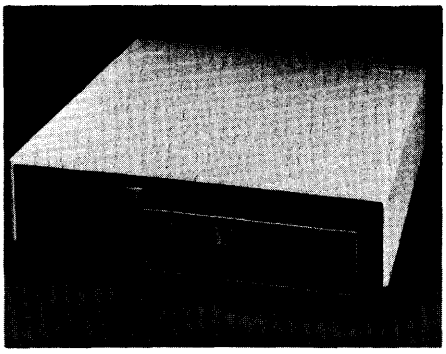
Continued....

READ BUFFER - Transfers the contents of the buffer location specified by the buffer address pointer in the controller through the micro bus into the B register of the processor. The buffer address pointer is incremented. Note: this command should not be issued when a TRANSFER IN PROGRESS status is indicated.

READ STATUS 1 - Transfers the contents of the controller's status byte 1 through the micro bus to the B register of the processor. Bit values in STATUS BYTE 1 have the following meanings:

READ STATUS BYTE 1 Bit Settings

Bit	Status	
0	ON-LINE -	Sets when ...e disk cartridge is loaded, the RUN signal is on, and the drive is ready. Clears when the RUN signal is off.
1	TRANSFER IN PROGRESS -	Sets when a READ, WRITE, or WRITE/VERIFY command is given. Clears when: - operation is complete - SECTOR NOT FOUND is set - TRANSFER ERROR is set
2	UNIT BUSY -	Sets when the SEEK command is given. Clears when operation is complete or a SEEK ERROR is detected.
3	SEEK ERROR -	Sets when: - SEEK TIME-OUT ERROR - ADDRESS PARITY ERROR - DISK FAULT Clears when a RESTORE command is given.
4	TRANSFER ERROR -	Sets when: - TRANSFER TIME-OUT ERROR - CRC ERROR - SECTOR OVERRUN ERROR - DISK FAULT ERROR - WRITE PROTECT ERROR - BUFFER PARITY ERROR Clears when any of the preceding conditions is cleared. Note: STATUS BYTE 2 indicates which condition caused the TRANSFER ERROR.
5	WRITE PROTECTED -	Sets when the disk is write protected (if the WRITE PROTECT switch is on or the WRITE PROTECT tag on the cartridge disk is detected). Note: The WRITE PROTECT error status bit will be set if a WRITE SECTOR or WRITE/VERIFY SECTOR command is issued when the WRITE PROTECT bit is set. Clears when the WRITE PROTECT switch is off and the WRITE PROTECT tag is not detected on the disk cartridge.
6	SECTOR NOT FOUND -	Sets when a TRANSFER IN PROGRESS has been on for 22 milliseconds without finding the correct sector. Clears when a READ, WRITE, or WRITE/VERIFY SECTOR command is given, or when a RESET or RESTORE occurs.
7	DEVICE RESTART -	Sets when power on reset from the power supply occurs or a static discharge to the subsystem chassis is detected. Resets when a RESTORE occurs.



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READ STATUS 2 - Transfers the contents of STATUS BYTE 2 through the micro bus to the B register of the processor. Bit values in STATUS BYTE 2 have the following meanings:

READ STATUS BYTE 2 Bit Settings

Bit	Description	
0	WRITE PROTECT ERROR -	Sets when the WRITE PROTECT switch is on or the WRITE PROTECT tag on the cartridge disk is detected and a WRITE SECTOR or WRITE/VERIFY SECTOR command is given. Clears when a RESET is given, a WRITE SECTOR or WRITE/VERIFY SECTOR command is given after the WRITE PROTECT switch is off or the WRITE PROTECT tag is removed from the cartridge, or a RESTORE is given.
1	TRANSFER TIME-OUT ERROR -	Sets when a READ, WRITE, or WRITE/VERIFY SECTOR command is not completed within 200 milliseconds. Clears when a RESET or RESTORE command is given.
2	SECTOR OVERRUN ERROR -	Sets when the next sector pulse before the data transfer operation is completed during a READ SECTOR, WRITE SECTOR, or WRITE/VERIFY SECTOR command. Clears when a READ, WRITE, WRITE/VERIFY SECTOR, RESET or RESTORE command is given.
3	CRC ERROR -	Sets when a CRC error occurs on READ SECTOR or WRITE/VERIFY SECTOR command is given. Clears when a READ, WRITE, WRITE/VERIFY SECTOR RESET or RESTORE command is given.
4	DISK FAULT -	Sets when the drive indicates any of the following fault conditions: ● Seek fault or illegal seek address ● Write fault - No write current with write enable - No Write Clock transition after Write Enable - Write Current on without Write Enable ● Illegal Procedure - Disk Strobe 1 or Strobe 2 given when ready to seek,read or write is not valid or during a sector mark. - Read or Write command given when drive is not ready. - Write command given when WRITE PROTECT is on. - Read Enable and Write Enable on simultaneously. ● Power loss to the drive. ● Fault line broken ● Device malfuntion Clears when a RESTORE command is given.
5	ADDRESS PARITY ERROR -	Sets when the drive indicates a ready condition and the address parity bit in the servo address zone indicates a positioning error. Clears when a RESTORE command is given.
6	SEEK TIME-OUT ERROR -	Sets when a SEEK or RESTORE command is not complete within 200 milliseconds. Clears when a RESTORE command is given.
7	BUFFER PARITY ERROR -	Sets when a parity error occurs on a READ BUFFER, WRITE SECTOR, WRITE/VERIFY SECTOR command. Clears when a RESTORE command is given.

READ SYSTEM ID - Transfers the device identification code to the B register of the processor. The identification code for the disk controller is 00000001.

Continued....

3.6.2 OUTPUT Commands

The output command (uBOUT) uses the A register of the processor in the same manner as the input command. The B register contains the data to be sent to the controller via the D0 - D7 lines of the micro bus.

3.6.2.1 Buffer Commands

Buffer commands are not issued if the TRANSFER IN PROGRESS status is indicated by the controller.

SET BUFFER POINTER - Sets the controller's buffer address pointer to the contents of the B register. The next WRITE BUFFER or READ BUFFER command will go to the pointed buffer location. After the disk read or write sector operation, the buffer address pointer is set to 000.

WRITE BUFFER - Transfers the contents of the B register to the buffer location specified by the buffer address pointer and increments the pointer.

3.6.2.2 Disk Commands

These commands interact with the controller and the disk and should not be issued if UNIT BUSY, SEEK ERROR, or TRANSFER IN PROGRESS status is indicated or if on-line is not true. RESTORE may be issued any time.

SET TRACK MSB - Transfers the two low-order bits of the B register to the two high-order bits of the controller's ten-bit Track Address register. (See 3.4 Cartridge Disk Operations).

SEEK - Transfers the contents of the B register to the eight low-order bits in the controller's Track Address register (see section 3.4) and causes the controller to perform a SEEK operation. The UNIT BUSY status bit is true during a SEEK operation. If an error occurs, the UNIT BUSY status bit goes false.

RESTORE - Must be issued whenever a SEEK ERROR condition is detected. The RESTORE command resets the following error flags:

SEEK ERROR
TRANSFER ERROR
WRITE PROTECT ERROR
TRANSFER TIME-OUT ERROR
SECTOR OVERRUN ERROR
CRC ERROR
DISK FAULT
ADDRESS PARITY ERROR
SEEK TIME-OUT ERROR
SECTOR NOT FOUND
BUFFER PARITY ERROR
DEVICE RESTART

The RESTORE command resets the disk drive to track 000, surface 0. The RESTORE command can be issued only when the following conditions are met:

- ON-LINE is active, TRANSFER IN PROGRESS is inactive, and UNIT BUSY is inactive,

or

- ON-LINE is active and DISK FAULT is active.

READ SECTOR - Transfers the contents of the B register to the controller's Sector Address register and causes the controller to read that sector into its buffer. Valid sectors are 0 - 47 (decimal).

While the READ operation is taking place, the TRANSFER IN PROGRESS bit is set true. If the sector specified is not found, the TRANSFER IN PROGRESS status bit is set false and the SECTOR NOT FOUND status bit is set true. If a timing error occurs and data transfer overruns the sector length, the TRANSFER IN PROGRESS status is removed and TRANSFER ERROR and SECTOR OVERRUN ERROR status bits are set.

If a DATA error occurs and the CRC check is unsuccessful, the TRANSFER IN PROGRESS status is removed and the CRC ERROR and TRANSFER ERROR status bits are set.

If data transfer is not completed within 200 milliseconds, the TRANSFER IN PROGRESS status is removed and the TRANSFER ERROR and TRANSFER TIMEOUT ERROR status is set.

WRITE SECTOR - Transfers the contents of the B register to the controller's Sector Address register and causes the controller to write the contents of its buffer to that sector.

The TRANSFER IN PROGESS status bit is set while the write operation is in progress.

If the specified sector is not found, TRANSFER IN PROGRESS is removed and SECTOR NOT FOUND is set.

If a timing error occurs and the data transfer overruns the sector length, the TRANSFER IN PROGRESS status is removed and TRANSFER ERROR and SECTOR OVERRUN ERROR status is set.

If the data transfer is not completed within 200 milliseconds, the TRANSFER IN PROGRESS status is removed and TRANSFER ERROR and TRANSFER TIME-OUT ERROR status is set.

WRITE/VERIFY SECTOR - Transfers the contents of the B register to the controller's Sector Address register and causes the controller to perform a write operation on the specified sector as described under WRITE SECTOR. The controller then performs a READ operation on the same sector on the next revolution and performs a CRC check without transferring any data back from the disk sector to the controller's buffer.

The TRANSFER IN PROGRESS status bit is true while the WRITE/VERIFY operation is in progress.

If the target sector is not found on either phase of the command, the TRANSFER IN PROGRESS status is removed and the SECTOR NOT FOUND status bit is set.

If a timing error occurs and data transfer overruns the sector, the TRANSFER IN PROGRESS status is removed and TRANSFER ERROR and SECTOR OVERRUN ERROR status is set.

If a data error occurs during a read-back and the CRC check is unsuccessful, the TRANSFER IN PROGRESS status is removed and CRC ERROR and TRANSFER ERROR status is set.

If the WRITE/VERIFY SECTOR operation is not completed within 200 milliseconds, the TRANSFER IN PROGRESS status is removed and TIME-OUT ERROR and TRANSFER ERROR status is set.

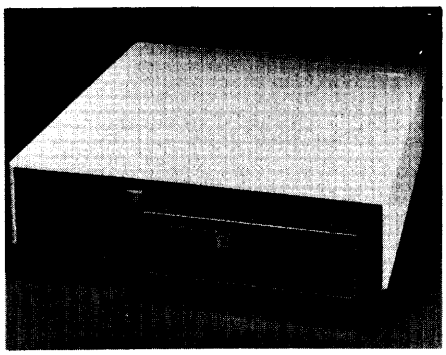
3.6.3 RESET Command

The RESET command resets error status bits within the controller. The following error status bits are set false:

WRITE PROTECT ERROR
TRANSFER TIME-OUT ERROR
SECTOR OVERRUN ERROR
CRC ERROR
SECTOR NOT FOUND

3.7 Serial Interface Addressing

The four-terminal serial interface address is specified through the four slide switches, labeled A0 through A3, located on the printed circuit board. The slide switches correspond to the processor address/command byte bits (A register) A0 through A3, respectively. The serial interface responds to only one of the sixteen possible combinations that can be formed through the binary combination of A0 through A3.



The interface accepts logic zero when the switch is set in the 0 or closed position. The interface accepts logic one when the switch is in the 1 or open position. The processor address/command byte (A register) is diagrammed in section 3.6, I/O Command Set.

3.7.1 Serial Interface Commands

The four-terminal serial interface address is selected by setting the four slide switches, labeled A0 through A3, located on the interface circuit card. The switches correspond to the A0 through A3 bits of the processor address/command byte (A register). Commands and corresponding bit assignments are as follows:

A Register Command Bit Combinations

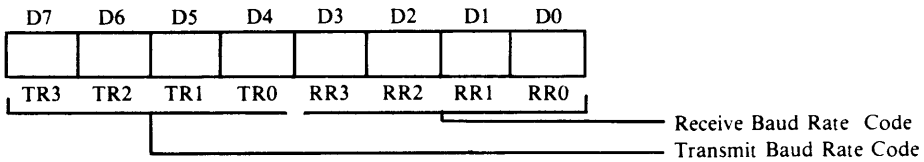
CMD3	CMD2	CMD1	CMD0	Strobe 1 (uBIN)	CMD3	CMD2	CMD1	CMD0	Strobe 2 (uBOUT2)
0	0	0	0	Unassigned	0	0	0	0	Loads port 0 baud rate
0	0	0	1	Unassigned	0	0	0	1	Loads port 1 baud rate
0	0	1	0	Unassigned	0	0	1	0	Loads port 2 baud rate
0	0	1	1	Unassigned	0	0	1	1	Loads port 3 baud rate
0	1	0	0	Port 0 status put on micro bus	0	1	0	0	Loads mode/command byte to port 0
0	1	0	1	Port 1 status put on micro bus	0	1	0	1	Loads mode/command byte to port 1
0	1	1	0	Port 2 status put on micro bus	0	1	1	0	Loads mode/command byte to port 2
0	1	1	1	Port 3 status put on micro bus	0	1	1	1	Loads mode/command byte to port 3
1	0	0	0	Port 0 data put on micro bus	1	0	0	0	Loads data to be transmitted to port 0
1	0	0	1	Port 1 data put on micro bus	1	0	0	1	Loads data to be transmitted to port 1
1	0	1	0	Port 2 data put on micro bus	1	0	1	0	Loads data to be transmitted to port 2
1	0	1	1	Port 3 data put on micro bus	1	0	1	1	Loads data to be transmitted to port 3
1	1	0	0	Port status byte A put on micro bus	1	1	0	0	Unassigned
1	1	0	1	Port status byte B put on micro bus	1	1	0	1	Unassigned
1	1	1	0	Port status byte C put on micro bus	1	1	1	0	Unassigned
1	1	1	1	Port status byte D put on micro bus	1	1	1	1	Generates power on reset

Once the interface is addressed, the command and strobe lines from the B register of the processor can write transmit and receive rate, modes/commands, or data to any of the ports on the data-in lines and read data or status from any of the data-out lines. When a port is strapped for asynchronous operation, any one of fourteen baud rates from 50 to 9600 can be programmed into the port from the processor. In the synchronous mode, the port receives clock signals from the connecting transmission link. Mode instructions from the processor include character length, parity enable, and type and number of stop bits or sync characters. Command instructions operate the standard RS-232-C interface signals. Eight status bytes inform the processor when any of the ports are ready to transmit or receive, or have transmitted or received, a character.

3.7.2 Transmit and Receive Baud Rates

Transmit and receive baud rates are specified via the B register of the processor. Baud rates specified by bit combinations are as follows:

Processor B Register



Baud Rate Codes

TR3 or RR3	TR2 or RR2	TR1 or RR1	TR0 or RR0	BAUD RATE
0	0	0	0	Zero Baud
0	0	0	1	Zero Baud
0	0	1	0	50 Baud
0	0	1	1	75 Baud
0	1	0	0	134.5 Baud
0	1	0	1	200 Baud
0	1	1	0	600 Baud
0	1	1	1	2400 Baud
1	0	0	0	9600 Baud
1	0	0	1	4800 Baud
1	0	1	0	1800 Baud
1	0	1	1	1200 Baud
1	1	0	0	2400 Baud
1	1	0	1	300 Baud
1	1	1	0	150 Baud
1	1	1	1	110 Baud

Continued....

In the asynchronous mode the transmit and receive baud rates may be programmed for the interface by writing a baud rate byte to each port. A given port can be programmed with different transmit and receive baud rates.

Data written to the four-terminal interface will hold true until it is written over or the power to the 9320 is turned off. Power on reset or software generated reset have no effect on the baud rate previously specified.

3.7.3 Mode Instructions

The first data byte to be written to a port must be a mode instruction.

3.7.3.1 Asynchronous Mode Instruction

The asynchronous mode instruction specifies the serial word or character length, type of parity (if any), and number of stop bits. If the word length is specified as less than eight bits, the least significant data bus bits will hold the data and the unused bits will be zero. The parity bit, if used, will not be considered as part of the programmed character length, and, when received, cannot be read on the data bus.

Processor B Register
Asynchronous Mode Instruction

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EP	PEN	L2	L1	1	0

S1 and S2 specify the number of stop bits as follows:

S2	S1	Number of Stop Bits
0	0	No preference
0	1	1 stop bit
1	0	1.5 stop bits
1	1	2 stop bits

EP indicates the type of parity:
1 = even, 0 = odd.

PEN specifies parity checking:
1 = enable, 0 = disable

L1 and L2 specify character length as follows:

L2	L1	Length in Bits
0	0	5
0	1	6
1	0	7
1	1	8

1 in position D1 and 0 in position D0 indicate that this is an asynchronus mode instruction.

3.7.3.2 Synchronous Mode Instruction

The synchronous mode instruction format is the same as that of the asynchronous mode instruction except that instead of specifying the number of stop bits, the number of synchronization characters is specified. Following the mode instruction, the sync characters are sent serially at the start of a transmission to enable the receiving device to synchronize with the transmitting device. The format of the synchronous mode instruction is as follows:

Processor B Register
Synchronous Mode Instruction

D7	D6	D5	D4	D3	D2	D1	D0
SCS	0	EP	PEN	L2	L1	0	0

SCS indicates the number of synchronization characters: 1 = one, 0 = two
0 in position D6 is required.
EP indicates type of parity: 1 = even, 0 = odd
PEN specifies parity checking: 1 = enable, 0 = disable
L2 and L1 specify character length as follows:

L2	L1	Character length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

0 in position D1 and 0 in position D0 indicate this is a synchronous mode instruction.

3.7.4 Serial Interface Command Instruction

The serial interface command instruction byte is sent following the mode instruction in asynchronus mode and following the sync characters in synchronous mode. A command byte may be written to any port on the serial interface following proper initialization of that port. The command byte format is as follows:

Processor B Register
Serial Interface Command Instruction

D7	D6	D5	D4	D3	D2	D1	D0
EH	IR	RTS	ER	SEEK	RXEN	DTR	TXEN

EH - Enter hunt mode: 1 = enables sync character search, 0 = disables search (EH has no effect in asynchronous mode).

IR - Internal reset: 1 = Prepares interface to receive another mode instruction, 0 = Leaves the interface in the data mode.

RTS - Request to send: 1 = RTS true, 0 = RTS false.

ER - Error flag reset: 1 = Reset error flags, 0 = do not reset flags

SEEK - Send break character: 1 = TXD output forced to zero, 0 = no effect

RXEN - Receive enable: 1 = enable, 0 = disable

DTR - data terminal ready: 1 = DTR output forced true (high), 0 = DTR output false

TXEN - Transmit enable: 1 = enable, 0 = disable

3.7.5 Serial Interface Port Status

Two types of status information are available through the serial interface: internal and combinational.

3.7.5.1 Internal Status Byte

Each port on the serial interface has one internal status byte which may be read at any time. The format and description of the internal status byte is as follows:

Processor B Register

Serial Interface Port Internal Status Byte

D7	D6	D5	D4
DSR	SYN/BRK DET	FE	OE

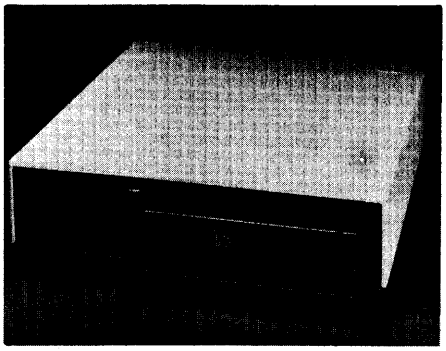
D3	D2	D1	D0
PE	TX EMPTY	RX RDY	TX RDY

DSR - Data set ready has been set high

SYN/BRK DET - Indicates detection of sync characters in synchronous mode and break characters in asynchronous mode.

FE - Indicates a framing error has occurred (stop bit not found in the correct position). A framing error is normal anytime a break character is received in the asynchronous mode. This bit is reset by the ER bit of command byte.

OE - Indicates an overrun error has occurred. The character that was overrun is lost. Reset by the ER bit of the command byte.



PE - Indicates a parity error has been detected in a received serial character. Reset by the ER bit of the command byte.

TX EMPTY - Indicates that the port does not have any data characters ready for serial transmission. When TXEMPTY is false and TXRDY is true, the data buffer and not the transmit buffer is empty.

RX RDY - Indicates that the port has received a serial character and has a parallel version ready to be read.

TX RDY - Indicates that the port is ready to receive another parallel character for serial transmission.

3.7.5.2 Combinational Status Byte

The serial interface combinational status byte is formatted as follows:

Processor B Register
Combinational Status Byte

	D7	D6	D5	D4	D3	D2	D1	D0
Status Byte A	RGDET 1	CRDET 1	TXRDY 1	RXRDY 1	RGDET 0	CRDET 0	TXRDY 0	RXRDY 0
Status Byte B	RGDET 3	CRDET 3	TXRDY 3	RXRDY 3	RGDET 2	CRDET 2	TXRDY 2	RXRDY 2
Status Byte C	TXRDY 3	RXRDY 3	TXRDY 2	RXRDY 2	TXRDY 1	RXRDY 1	TXRDY 0	RXRDY 0
Status Byte D	TXMT 3	TXMT 2	TXMT 1	TXMT 0	SYN/BRK DET 3	SYN/BRK DET 2	SYN/BRK DET 1	SYN/BRK DET 0

The numbers 0 through 3 indicate the specific port.

RGDET - A true signal has been detected on the RING indicator pin of the connector.

CRDET - Received status, indicates a true signal has been detected on the Carrier Detect line of the connector.

TXRDY - Indicates the port is ready to receive a parallel character for serial transmission. TXRDY is false if CTS is not active or the transmit-enable bit is not set.

RXRDY - Indicates a serial character has been received and the parallel version is ready to be used.

SYN/BRK DET - Indicates that sync character requirements have been met when the port is in synchronous mode. When the port is in asynchronous mode, indicates that no characters are being sent and the communications line is being held in the spacing condition.

TXMT - Indicates that the transmitter has no character to send (asynchronous mode). In synchronous mode, this bit indicates that sync characters are being (or have been) transferred.

4.0 Physical Description

4.1 9310/9320 Disk Drive

Height:	7.0 in. (15.75 cm)
Width:	21.875 in. (55.56 cm)
Depth:	22.625 in. (57.46 cm)
Weight:	65.0 lbs. (29.48 kg)

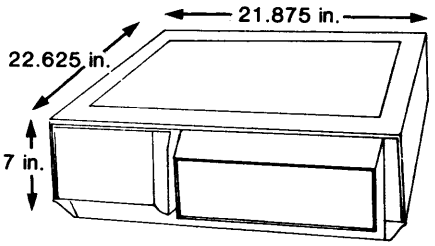


Figure 4-1: 9310/9320 Physical Dimensions

4.2 80501 Cartridge Disk

Height:	0.9 in. (2.3 cm)
Width:	11.1 in. (28.2 cm)
Depth:	11.2 in. (28.4 cm)
Weight:	2.8 lbs.(1.3 kg)

5.0 Environmental Requirements

Temperature:	50 to 100 degrees F 10 to 38 degrees C
Humidity:	10 to 90% relative, noncondensing
Heat Dissipation:	855 BTU/Hour

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Continued....

6.0 Interface Requirements

6.1 Micro Bus Pin Assignments

Pin	Signal
1	Ground
2	Strobe 1
3	Ground
4	Strobe 2
5	Ground
6	IACK
7	Ground
8	Address 0
9	Address 1
10	Address 2
11	Address 3
12	Comm 0
13	Comm 1
14	Comm 2
15	Comm 3
16	Not used
17	Interrupt Request
18	Data 0
19	Data 1
20	Data 2
21	Data 3
22	Data 4
23	Data 5
24	Data 6
25	Data 7
26	+5 Volts

6.2 Serial Interface Port Pin Assignments

Each port on the four-terminal serial interface provides ten RS-232-C defined data and control signals. Each port connects via a 25 pin Amphenol male connector. Pin assignments are as follows:

Pin	Description
1	Protective Ground
2	Transmitted Data
3	Received Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7,11,18,25	Signal Ground
8	Carrier Detect
15	Transmit Clock
17	Receive Clock
20	Data Terminal Ready
22	Ring Indicator

Note: Clear to Send must be set high for the port to transmit.

6.3 Power Requirements

Power:	115 or 220 VAC, 50 or 60 Hz, ± 3 Hz
Current:	2.2 amps @ 115 VAC 1.2 amps @ 220 VAC
Power Consumption:	250 watts, maximum

7.0 Options

The 9310/9320 Cartridge Disk Drive is available in 115 and 220 VAC models. The 9310/9320 is also available in a variety of system configurations.

8.0 Shipping List

Quantity	Item
1	9310/9320 Cartridge Disk Drive
1	80501 Cartridge Disk
1	9310/9320 Cartridge Disk Product Specification (Document No. 60876)

Note: This shipping list is provided for information purposes only and may be amended from time to time by Datapoint Corporation.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