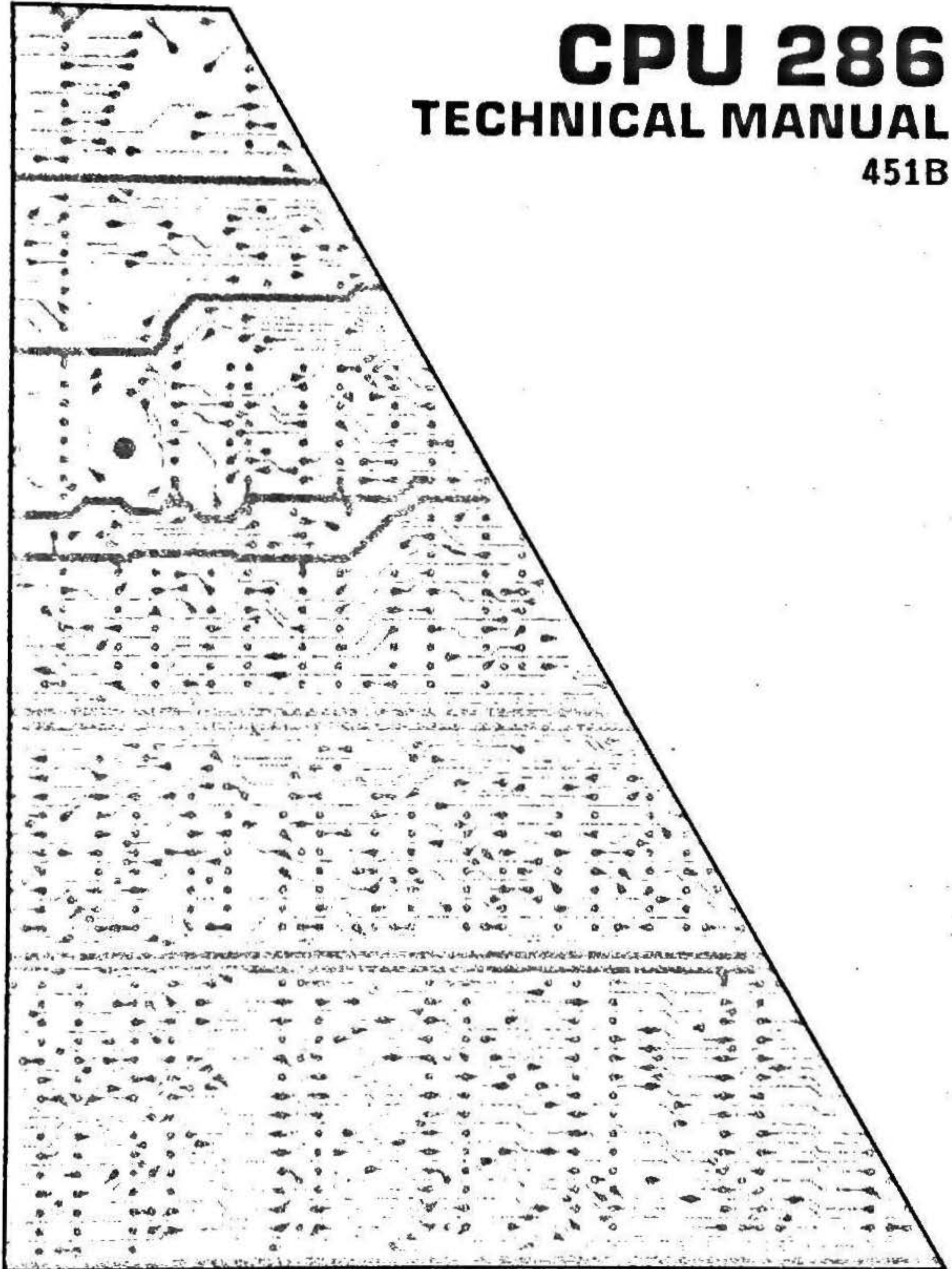


**CompuPro™**

# **CPU 286**

## **TECHNICAL MANUAL**

**451B**



**CPU 286  
TECHNICAL MANUAL**

**HIGH-PERFORMANCE 16-BIT 80286  
80287 NUMERIC PROCESSOR EXTENSION  
EPROM/SRAM/EEPROM SOCKETS  
FOR UP TO 64K**

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CPU 286 Technical Manual 451B  
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## Specifications

Timing	Meets all IEEE 696/S-100 Specifications
Clock Rate	Can support up to a 12.5 MHz 80286
Address Bus	24 Bits; addresses 16 Mbytes
Memory Manager	A23-A20 programmable
Data Bus Width	16-bit memory or I/O; also supports 8-bit devices
Wait State Generator	Flexible; can insert 0 to 3 wait states into I/O or memory cycles independently
Master Status	Implemented as a permanent master
On-board Memory	Can support up to 64K of EPROM, SRAM, or EEPROM
Math Coprocessor	80287; clock speed is independent of 80286
Power Consumption	2500mA maximum at 8 VDC

## About the CPU 286

The CPU 286 from CompuPro is one of the most advanced 16-bit processors available for the IEEE 696/S-100 Bus. Based on the high performance 80286 16-bit microprocessor, the CPU 286 includes sockets for optional on-board EPROM, SRAM, and/or EEPROM memory and for Intel's 80287 High Speed Numeric Processor Extension.

Features of the CPU 286 include:

- The 80286 16-bit processor with an integrated memory management unit, virtual memory support, and an instruction set optimized for multi-user operation.
- A hardware byte serializer that allows mixing of any 8-bit and 16-bit memory and I/O devices that conform to the IEEE 696/S-100 protocol for 8-bit and 16-bit transfers; the CPU 286 dynamically adjusts itself to the proper bus width for 8-bit or 16-bit operation.
- The 80287 Numeric Processor Extension with an independent clock generator, adding fast number crunching capability while appearing to the software just like an 8087.
- Compatibility with all TMA devices conforming to the IEEE 696/S-100 specification.

In the protected virtual address mode, the 80286 has integrated memory management and four-level memory protection for operating systems employing virtual memory. The address space in the protected virtual address mode extends to 16 Megabytes of physical addressing (24 bits), and a full Gigabyte (30 bits) of virtual addressing per task.

In the real address mode, the 80286 runs all software written for the 8086/8088. In addition, the on-board memory manager gives 24 address lines for access to up to 16 megabytes of memory.

Designed to work at clock speeds up to 12.5 MHz, the CPU 286 may always be used with the fastest processor available.

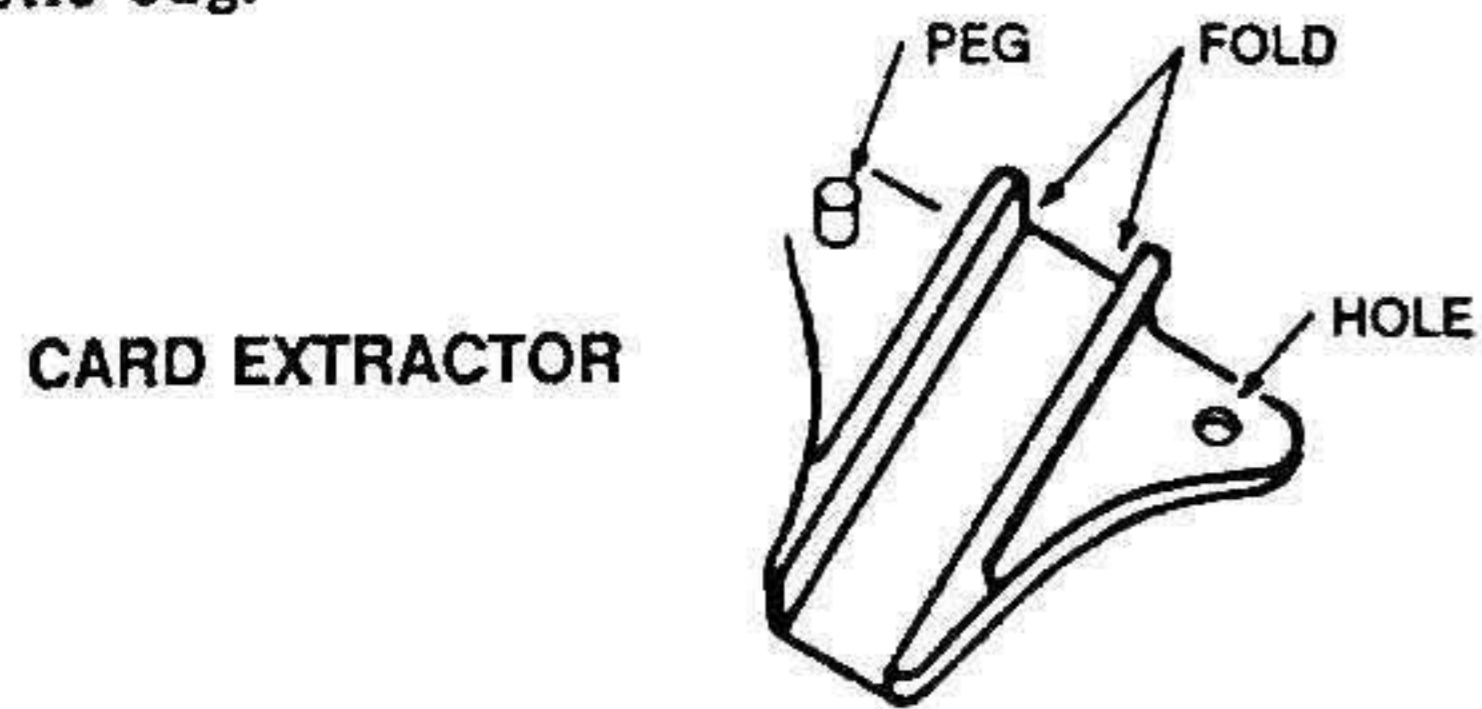
When you couple high speed operation with the power of the 80286/80287 pair, the CPU 286 is truly a processor board for advanced computing systems of the eighties. Thank you for choosing a CompuPro product.

## Installing the CPU 286

### Basic Installation

#### Step 1. Unpack the CPU 286 Board.

Along with the board, you will find two card extractors in the plastic bag.



#### Step 2. Install Card Extractors.

1. Hold the board so the component side is toward you.
2. Insert the peg on the card extractor into the hole in the right corner of the board. Fold the extractor over the board's edge until the extractor's hole snaps over the peg.

NOTE: Make sure the long edge of the extractor is along the top edge of the board.

3. Repeat for the left extractor.

#### Step 3. Check Jumper Settings

For standard jumper settings for use with a CompuPro operating system, check the operating system Installation Guide. In addition, jumper settings are described in detail in the Jumper Settings section of this manual.

#### Step 4. Insert the CPU 286 into the S-100 Bus.

The power to the system must be off. Place the board into a slot towards the front of the enclosure. The edge connector is offset, so the CPU 286 will fit only one way. Push down GENTLY until the board is firmly installed.

### Jumper Summary

The following summary of jumpers explains the function and logic of each option. For help in locating a jumper, refer to the drawing on the following page.

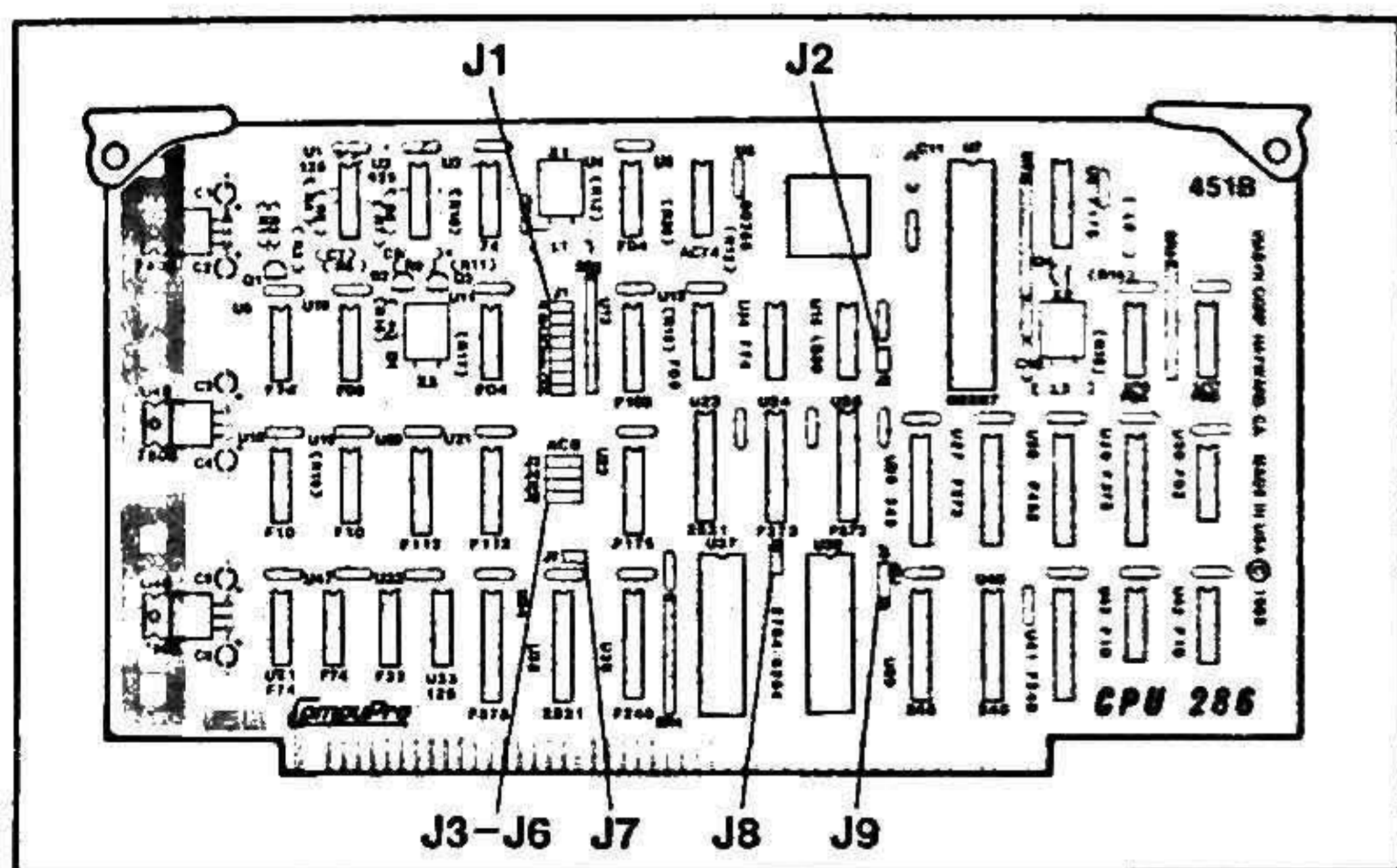
Table 1: Jumper Summary

J	Position	Function
1	A	1 Memory wait state
	B	1 I/O wait state
	C	1 Wait state for all cycles
	D	2 Memory wait states
	E	2 I/O wait states
	F	2 Wait states for all cycles
	G	4 EPROM/SRAM/EEPROM wait states
	H	1 Memory WRITE and 1 I/O wait state
2		80287 NPX/memory manager disable
3	A-C	A23 from memory manager
	B-C	A23 from 80286
4	A-C	A22 from memory manager
	B-C	A22 from 80286
5	A-C	A21 from memory manager
	B-C	A21 from 80286
6	A-C	A20 from memory manager
	B-C	A20 from 80286
7		EPROM/SRAM/EEPROM socket master enable
8		Select EEPROM
9	A-C	EPROM/SRAM/EEPROM size select
	B-C	See Table 2

The following table lists all the possible devices that can be installed in U37 and U38, and gives the settings for J7, J8, and J9 for each.

Table 2: EPROM/SRAM/EEPROM Jumper Selection

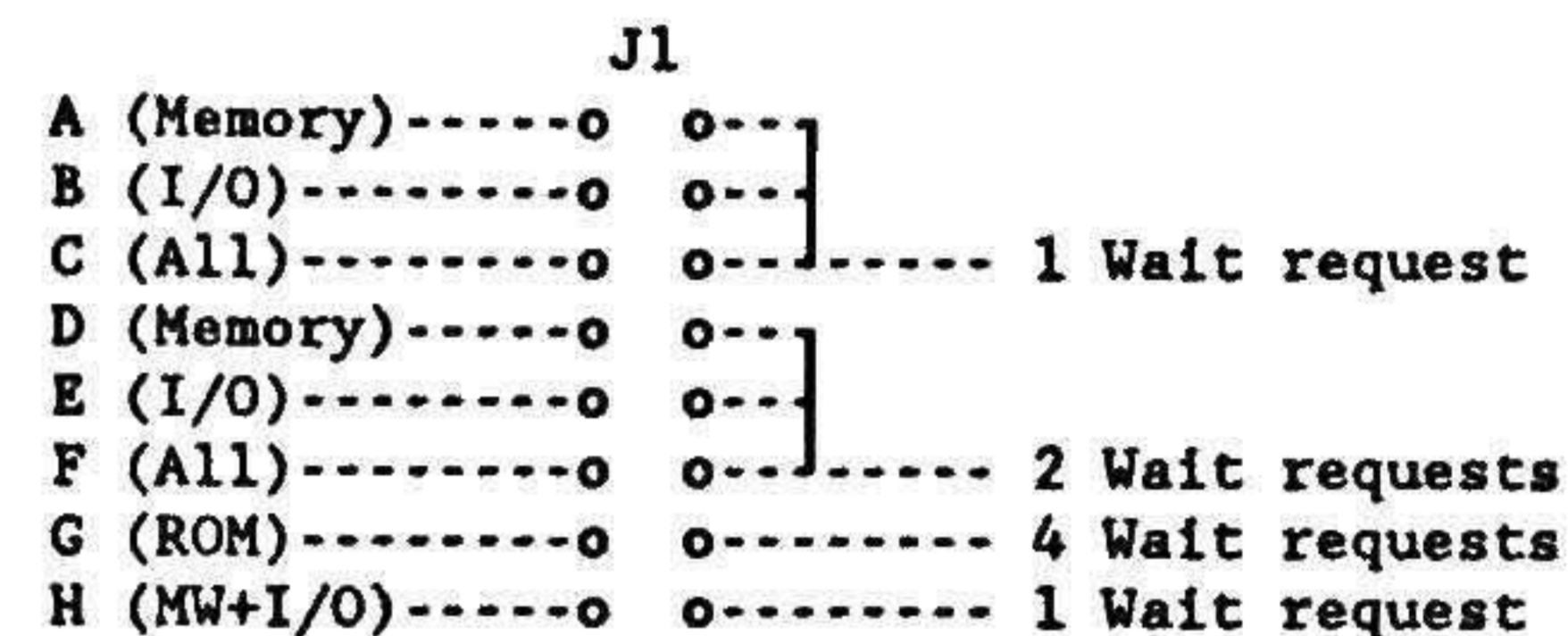
	EPROM 2764	EPROM 27128	EPROM 27256	SRAM 6264	EEPROM 2817A
J7	Inserted	Inserted	Inserted	Inserted	Inserted
J8	Inserted	Inserted	Inserted	Don't care	Removed
J9	Removed	Removed	B-C	A-C	A-C



## Jumper Settings

### J1 Wait State Select

Below is a physical diagram of J1. The inputs from the left reflect the current cycle type, and the outputs to the right request automatic hardware insertion of the given number of wait states.



To select the number of wait states the given space (I/O, Memory, I/O and Memory Writes, RAM/ROM Sockets) has, jumpers must be installed in the proper location(s).

Use the following rules for jumper selection:

- Placing no jumpers on any positions of J1 results in no wait states for any accesses.
- No more than one jumper may select a given number of wait states; i.e., a jumper may be placed on either position A, B, C, or H but not more than one of these positions may be jumpered.
- The wait states are additive; i.e., if I/O is jumpered for both one and two wait states, a total of three will be inserted for I/O cycles.
- The RAM/ROM sockets are part of memory space. Therefore, a jumper should only be inserted into position G if the on-board RAM/ROM need more wait states than the off-board memory.

The following are several examples of possible wait state configurations for memory reads (MR), memory writes (MW), Input/Output (I/O), and the EPROM/SRAM/EEPROM sockets (ROM):

J1		J1		J1		J1	
A	o o	A	o o	A	o o	A	o o
B	o—o	B	o o	B	o—o	B	o o
C	o o	C	o—o	C	o o	C	o o
D	o o	D	o o	D	o o	D	o o
E	o o	E	o—o	E	o o	E	o o
F	o o	F	o o	F	o—o	F	o o
G	o o	G	o o	G	o o	G	o—o
H	o o	H	o o	H	o o	H	o—o
Example 1		Example 2		Example 3		Example 4	
MR:	0	1	2	0	0	1	1
MW:	0	1	2	1	1	1	1
I/O:	1	3	3	1	1	1	1
ROM:	0	1	2	1	1	1	1

NOTE: A no wait state cycle is an illegal S-100 bus cycle. If J1 is jumpered for no memory waits (two-cycle operation), the CPU 286 may be too fast for some system components. Zero memory wait states should only be used if all CompuPro components are used in a system and the installation manual suggests zero wait states. At least one wait state should always be inserted for I/O cycles.

In a system with only CompuPro boards the following are the minimum jumper positions supported:

- A 12.5 MHz CPU 286 with RAM 24<sup>tm</sup> memory must have at least 1 wait on memory write operations (position H).
- An 8 or 10 MHz CPU 286 with RAM 24 memory does not need memory waits (position B).
- An 8 MHz CPU 286 with B or C revision RAM 22<sup>tm</sup> memory does not need memory waits (position B).
- Any CPU 286 with RAM 16<sup>tm</sup>, RAM 17<sup>tm</sup>, RAM 21<sup>tm</sup>, or A revision RAM 22 memory needs a memory wait (position C).

All other combinations should be jumpered for at least one memory wait (position C or F).

### J2 80287 NPX and Memory Manager Disable

This jumper is normally not used.

The CPU 286 decodes sixteen I/O addresses (00F8h through 00FFh and 01F8h through 01FFh) of the 64K I/O port map to its internal devices: the 80287, and the memory manager. Whenever these addresses are accessed (and J2 is removed) the data bus buffers from the S-100 bus are disabled, allowing data to be read from or written to the 80287 or the memory manager. Any peripherals residing on the S-100 bus at these addresses cannot be correctly accessed. If it is imperative to have peripherals at these addresses and neither the NPX nor the memory manager is going to be used, jumper J2 can be installed, allowing the ports back onto the S-100 bus. For more information, refer to the Port Map in the Programming Considerations section of this manual.

### J3 through J6 Memory Manager Select

These four jumpers choose whether the high four bits (A20 through A23) come from the 80286 or from the memory manager. When position B-C is shunted, the address lines come directly from the 80286; when position A-C is shunted, they come from the memory manager. J3 through J6 correspond to A23 through A20 respectively.

As shipped from the factory, jumpers J3 through J6 are connected by small traces on the component side of the board across A-C so that the default is to bring A20 through A23 from the memory manager. To connect the 80286 bits, cut the small traces on the component side of the board from J3 through J6, install pins, and place shunts across B-C.

The on-board memory manager allows the CPU 286 to set the high nibble (A20 through A23) of its physical address.

The 80286 has two address modes: real mode and protected virtual address mode.

- In real address mode, the 80286 is limited to 1 Mbyte (20 bit) addressing. The CPU 286 memory manager can extend the 20 bit limit up to 24 bits.

Software written to take advantage of the memory manager requires J3 through J6 to be set A-C (as shipped). Software that does not use the memory manager generally does not care about how J3 through J6 are set.



- When in protected mode, the 80286 can produce 24 bits of address (memory up to 16 Mbytes), and the memory manager is not used. In this case J3 through J6 should all be set to B-C.

The Programming Considerations section provides more information about the programming and effects of the memory manager.

#### *J7 EPROM/SRAM/EEPROM Master Socket Enable*

With this jumper removed, the EPROM/SRAM/EEPROM sockets do not respond, the 64K window in page 0FFh appears as memory on the S-100 bus, and the wait state jumpers for the sockets have no effect.

To enable the sockets to respond, pins and a shunt should be installed. When the jumper is installed, the 64K window at page 0FFh (memory addresses 0FF0000h through 0FFFFFFh) is located in the sockets. If no devices are placed in the universal sockets U37 and U38, this jumper should be left disconnected (as shipped).

#### *J8 Select EEPROM*

This jumper is shipped with a normally closed connection that allows for 2764, 27128, 27256 EPROMs, and 6264 SRAMs in sockets U37 and U38.

Since pin 1 of some EPROMs is required to be tied to power (Vcc), and pin 1 of 2817A type EEPROMs is an open drain output, a socket meant to support both requires the ability to connect and disconnect pin 1 from Vcc.

If 2817A or compatible EEPROMs are to be inserted in the sockets, this jumper connection must be cut. Note that because of this, EPROMs and EEPROMs can't be mixed (unless pin 1 of the EEPROM is removed from the socket).

**CAUTION:** Permanent damage may occur to EEPROMs if J8 is left connected.

#### *J9 Select Memory Chip Type*

This jumper selects the proper pinout for the various EPROM/SRAM/EEPROMs that can be installed in the on-board sockets.

Jumper J9 as follows:

- A-C for 6264 type SRAMs and 2817A type EEPROMs
- B-C for 27256 type EPROMs
- No shunt for 2764 or 27128 type EPROMs

## The 80287

### Numeric Processor Extension

Due to the several speeds of 80287 parts available, CPU 286 boards not factory equipped with an 80287 do not have the 80287 clock components installed. To get an 80287, you must return your board to CompuPro for a factory upgrade. We will run a complete confidence test on the board and numeric processor.

Call the RMA desk at CompuPro for information and current pricing.

## Programming Considerations

### 80286 Compatibility with 8086/8088

The 80286 is upward software compatible with the 8086 and 8088. This feature makes the 80286 very attractive to users who have an investment in 8086/8088 code and who need a higher performance processor. While we were able to bring up 99% of our existing 8086/8088 software with the 80286, problems did emerge in timing, port mapping, and 24-bit addressing. The following discussion outlines the problems and their solutions.

#### *Timing Compatibility*

Because the 80286 is substantially faster than the 8086, and due to the optimization of the pre-fetch queue, the 80286 often executes bus cycles in a different order than the 8086. To see where this is a problem, consider initializing a part such as Intel's 8259A interrupt controller.

The 8086 executes the three-byte initialization sequence as follows:

1. Fetch first operand
2. Output first operand
3. Fetch second operand
4. Output second operand
5. Fetch third operand
6. Output third operand

The 80286 executes this sequence:

1. Fetch first operand
2. Fetch second operand
3. Output first operand
4. Fetch third operand
5. Output second operand
6. Output third operand.

Although the actual order in which the 8259A receives the bytes is the same for both (as it must be), the minimum time between outputs is reduced, since no bus cycle is run between the second and third outputs. The 8259A requires a minimum time between command bytes, and with the faster 80286 this time is not met.

One solution to this problem is to force the 80286 to run a bus cycle between every output. The above example used immediate operands as initialization bytes, allowing the 80286 to pre-fetch and use them quickly. By putting the initialization bytes into a small table and fetching them individually for every output, the 80286 is forced to run at least one bus cycle (the operand fetch) between every output. This easily satisfies the 8259A minimum.

#### *Port Mapping*

80287 Numeric Processor Extension is I/O mapped into ports 00F8h through 00FFh of the 80286. From a hardware standpoint, this is a logical thing to do, as it allows the NPX and CPU to run at different speeds. The problem is that any software that accesses peripherals at these ports not only messes up the 80287, but it cannot access the peripherals correctly. There is a similar potential conflict in port mapping for the memory manager, which is mapped to ports 01F8h through 01FFh.

The best solution is to relocate the conflicting S-100 boards in the system to different ports. This is the only solution if the NPX is to be used. If it is impossible to relocate these ports and if the 80287 and the memory manager will never be used, jumper J2 can be installed. In this case, be very careful not to execute any NPX "ESCAPE" instructions, as the bus peripherals could get corrupted when the 80286 accesses these ports.

Table 3: CPU 286 Port Map (J2 removed)

<u>I/O Address</u>	<u>Device</u>
0000h-00F7h	Mapped to S-100 bus
00F8h-00FFh	Mapped to 80287
0100h-01F7h	Mapped to S-100 bus
01F8h-01FFh	Mapped to memory manager
0200h-FFFFh	Mapped to S-100 bus.

#### *24-Bit Addressing*

The 80286 initializes and starts execution at location 0FFFFFF0h. Notice that this is a 24-bit address, not a 20-bit address as produced by the 8086/8088. This is not a problem in complete CompuPro systems, as the boot EPROM on the DISK 1A<sup>tm</sup> appears in every page while PHANTOM\* is asserted during boot up.

While in real address mode, since the 80286 does not know what to do with the most significant four bits (A20 through A23), it leaves them high on boot until a long jump (one that loads the code segment) is executed, at which time it sets the four bits low. This means that if the boot code is in the on-board EPROM, that code cannot execute any long jumps, or it will jump right out of the EPROM's address space. Once out of the EPROM, the program can never get back without going into the protected address mode.

#### **Programming for the Memory Manager**

The memory manager on this board allows the CPU 286 to set the high nibble (A20 through A23) of its physical address.

In real address mode, the memory manager can be used to extend the limit of 20 bits (memory up to 1 Mbyte) that the 80286 can produce up to 24 bits (approaching 16 Mbytes).

The memory manager is reset to all 0. Thus A20 through A23 go low on a reset, and stay low until something else is written to the memory manager. To write to the memory manager, place the value into the low nibble of 80286 register AL and write a byte to any even port in the range 01F8h to 01FEh. Reading from any port in this range is not mapped to the S-100 bus and does not affect the memory manager. Writing a byte or word to an odd address in this range puts random data into the memory manager.

A general model for using the memory manager to extend the accessible memory space of a 80286 in real address mode is to divide the memory into global memory which is always visible to the 80286 and into banked memory which is banked or switched on and off depending on the memory manager output. Usually the banked memory space would be much larger than the global memory space.

The global memory addressing does not involve lines A20 through A23 and thus global memory is always visible to the 80286. The bits that are written to the memory manager on lines A20 to A23 choose which of the banked memory pages are visible to the 80286. The addressing must be set up to make sure that this banked memory does not collide with global memory.

Following is an example of how to use the memory manager to address both global and banked memory. This example is only an outline; the details depend upon the memory boards and operating system being used.

This example uses memory in 256 Kbyte blocks. The desired result is to have 256 Kbytes of global memory at the bottom (00h) of memory space, and allow the upper 768 Kbytes of memory to be used for banking into or out of up to 16 banks. Using a 256 Kbyte global memory space in this way, over 12 Mbytes of memory is accessible to the 80286.

Note: Each bank need not contain the full 768 Kbytes of memory.

**Global Memory** A23 through A20 are disabled on the memory board. A19 through A18 are set to low. Thus, the global memory board appears at:

000000h-03FFFFh  
 and 100000h-13FFFFh  
 and 200000h-23FFFFh  
 ...  
 and F00000h-FFFFFFh.

**Banked Memory** Each bank requires three 256K memory boards to make 768K. Address each board within the bank with A19 and A18. On the first board, set A19 low and A18 high. On the second board set A19 high and A18 low. On the third board, set A19 high and A18 high. In no case should any board be set with both A19 and A18 low, as that would conflict with the global board.

**Bank 0** On all three boards, set A23 through A20 to respond to low. Set A19 and A18 as described in the description of Banked Memory. Thus, the memory appears at:

Board 1 040000h-07FFFFh  
 Board 2 080000h-0BFFFFh  
 Board 3 0C0000h-0FFFFFh

**Bank 1** On all three boards, set A23 through A21 to respond to low, and A20 to respond to high. A19 and A18 are set the same as in bank 0. Thus, the memory appears at:

Board 1 0140000h-017FFFFh  
 Board 2 0180000h-01BFFFFh  
 Board 3 01C0000h-01FFFFFh

This pattern could continue up through Bank 0Fh. The table below shows how to set A23 through A20 for all the possible banks. For all banks, A19 through A18 are set to select the three boards within the bank.

Table 4: Memory Bank Addressing

BANK	A23	A22	A21	A20
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
...				
E	1	1	1	0
F	1	1	1	1

Another possible configuration would be 256 Kbytes of global memory and 256 Kbytes of banked memory in each bank. Each user could then have a separate 256 Kbyte bank, and would not be able to access other user programs.

## Theory of Operation

In the following discussion, it is helpful to refer to the schematic diagrams at the end of this manual.

The CPU 286 is based on the 80286 CPU and the Intel 80287 NPX.

### 80286 Clock Circuitry

This circuitry is shown on page 1 of the schematics.

The clock for the CPU is generated by crystal X1 and divided by U5, a 74AC74. The crystal is four times the desired speed of the processor. If the crystal value is changed, the value of L1 and C9 must also be changed.

Unlike the 8086/8087 pair, the 80287 can run at any speed with respect to the 80286. Crystal X2 is three times the desired speed of the 80287. If the crystal value is changed, the value of L3 and C10 must also change.

### Numeric Coprocessor

This circuitry is shown on pages 1 and 2 of the schematics.

The 80286 and the 80287 communicate via eight I/O mapped ports, the PEREQ and PEACK\* (peripheral request and acknowledge), BUSY\* and ERROR\*. When the 80286 sees an ESC instruction dealing with the 80287, it checks the status of the BUSY\* input; if the 80287 is not currently busy, the 80286 instructs the NPX to execute a command. When the 80287 requires data from memory, it can assert PEREQ at which time the 80286 performs the transfer.

### Memory Manager

This circuitry is shown on page 5 of the schematics.

When any port from 01F8H through 01FFH is written to, the data that appears on data bus lines D0 through D3 is loaded into the memory manager. When the board is reset, the memory manager is loaded with a 0, causing A20 through A23 to be low. This is different from the 80286, which asserts A20 through A23 high on reset. To load the memory manager, place the desired page into the low nibble of register AL, and run an OUT to port 01F8h.

### 80287 and Memory Manager I/O Mapping

This circuitry is shown on pages 1 and 2 of the schematics.

Intel has defined the 80287 I/O ports to reside at 00F8H to 00FFH. CompuPro defined the memory manager I/O ports to reside at 01F8H to 01FFH. The I/O ports that the 80287 and memory manager occupy are excluded on the S-100 bus. To get these to map back to the S-100 bus, J2 can be installed.

### Timing

This circuitry is shown on page 3 of the schematics.

The two 74F112 JK and one 74F74 D Flip Flops (U20, U21, and U9), along with their respective input logic, generate the S-100 strobes from the 80286 output signals.

### 8-Bit and 16-Bit Byte Serializer

This circuitry is shown on pages 3 and 4 of the schematics.

The CPU 286 includes all the logic necessary to handle both onecycle and twocycle fetches. A onecycle fetch is when the processor requests either 8 or 16 bits from memory and the memory is able to handle the transfer in one S-100 bus cycle. A twocycle fetch is when the processor requests 16 bits from the memory but the memory is only able to transfer 8 bits, forcing the internal finite state machine (U31) to complete two S-100 bus cycles to fetch two bytes before allowing the 80286 to complete its cycle. A twocycle fetch is also called a byte serial fetch. The decision to execute either a onecycle transfer or a twocycle transfer is controlled by the S-100 signals sXTRQ\* and SIXTN\* in conformance with the IEEE 696 specification.

### Data Bus

This circuitry is shown on page 4 of the schematics.

The data bus is buffered, multiplexed and latched (depending on what is required) by U26, U39, and U40 (all 74LS245), and U27 (74F373). The control of these buffers and latches is performed by a PAL 452 (U23).

### Status Bus

This circuitry is shown on page 4 of the schematics.

The status lines from the 80286 (S0\*, S1\*, C/I\*, M/IO\*, BHE\*) are latched by U29 (74F373). The outputs of U29 go to the inputs of the gates. The logic then decodes the proper status and feeds that to U41 (74F240) to drive the S-100 status lines.

### Wait Circuitry

This circuitry is shown on page 1 of the schematics.

The internal wait state generator is controlled by the 4-bit counter U12 (74F163). The number of internal wait states inserted into each bus cycle is determined by the status of the cycle and the setting of J1.

The different types of status that can be used are:

- all memory cycles,
- all I/O cycles,
- memory write and I/O cycles, and,
- accesses of the on-board sockets.

By selecting the proper position on J1, different wait states can be selected for the different spaces (memory, I/O, ROM). Some position must always be jumpered on J1.

NOTE: A no wait state cycle does not meet the IEEE 696 specification for bus cycles. Zero memory wait states should only be used if all CompuPro components are used in a system and the installation manual suggests zero wait states. At least one wait state should always be inserted into I/O cycles.

### Memory Addressing

This circuitry is shown on page 5 of the schematics.

The on-board EPROM/SRAM/EEPROM sockets are decoded by U35 (25LS2521). This puts the memory in sockets U37 and U38 into the highest memory page, 0FFh.

Installing J7 enables the memory in the sockets to be accessed.

# Notes on Using the CPU 286

## With Certain Other CompuPro Products

Revision D-2 or earlier of Concurrent DOS 8-16 Version 4.1

If you will be using this CPU 286 with Concurrent DOS 8-16 4.1D-2 or earlier, you may need to install a patch to RTM.CON

### Problem:

A bug has been identified in RTM.CON that causes system lock-up when files are opened in "unlocked mode" (FCB attribute bit F5=1, F6=0). This lock-up is caused by a specific location in memory being uninitialized, which allows the CPU to execute an illegal instruction. This problem is often seen running NEWWORD.

### Solution:

The solution to this problem is to patch the RTM.CON module and if desired, the CCPMSYS file being used on the system. If possible, we recommend that you patch RTM.CON and use this corrected module to GENCCPM a new system file, rather than perform the more difficult patch on your CCPMSYS file. The procedure for this patch is listed below:

NOTE: This patch is not a Digital Research patch, however, they have been informed of the procedure.

### Patch Procedure:

Make a back-up copy of RTM.CON and your CCPMSYS files before using SID86.CMD to make the changes on the following pages. User entries are underlined.

## Patch to RTM.CON

```
0A>SID86
SID86 1.0
#RTM.CON
    START    END
XXXX:0000 XXXX:1DFF
#L41A,41E
XXXX:041A MOV  [0052],DX
XXXX:041E MOV  DS,[001E]
#a41A
XXXX:041A CALL 1110
XXXX:041D NOP
XXXX:041E ┘
#L1110,1112
XXXX:1110 NOP
XXXX:1111 NOP
XXXX:1112 NOP
XXXX:1113 NOP
XXXX:1114 NOP
XXXX:1115 NOP
XXXX:1116 NOP
XXXX:1117 NOP
XXXX:1118 NOP
XXXX:1119 NOP
#a1110
XXXX:1110 MOV [52],DX
XXXX:1114 MOV [54],DX
XXXX:1118 RET
XXXX:1119 ┘
#L41A,41E
XXXX:041A CALL 1110
XXXX:041D NOP
XXXX:041E MOV DS,[001E]
#L1110,1118
XXXX:1110 MOV [0052],DX
XXXX:1114 MOV [0054],DX
XXXX:1118 RET
#RTM.CON
#^C
0A>
```

Save this new corrected copy of RTM.CON so that the next time you GENCCPM a system, you will use the corrected module. At this time, you can regenerate your CCPMSYS file as described in your documentation, or patch the CCPMSYS file as shown on the following page.

## Patch to CCPM.SYS

```
OA>SID86
SID86 1.0
#rCCPM_SYS
  START      END
XXXX:0000 YYY:ZZZZ
#s01
XXXX:0001 08A6 <CR>
XXXX:0003 0060 _
#hWXYZ,8A6      (WHERE WXYZ=XXXX+8)
+ WWW - 7777 * 77777777 / 777777 (7777)
#dWWW,0,F
WWW:0000 0003 0060 0000 0060 0003 VVVV 0000 01C7 ...'...'.....
#hVVVV,0060
+ 7777 - UUUU * 77777777 / 777777 (7777)
#hWXYZ,UUUU
+ MMM - 7777 * 77777777 / 777777 (7777)
#LMMM:39A,39E
MMM:039A MOV [0052],DX
MMM:039E MOV DS,[001E]
#aMMM:39A
MMM:039A CALL 1090
MMM:039D NOP
MMM:039E _
#LMMM:1090,1099
MMM:1090 NOP
MMM:1091 NOP
MMM:1092 NOP
MMM:1093 NOP
MMM:1094 NOP
MMM:1095 NOP
MMM:1096 NOP
MMM:1098 NOP
MMM:1099 NOP
#aMMM:1090
MMM:1090 MOV [52],DX
MMM:1094 MOV [54],DX
MMM:1098 RET
MMM:1099 _
#LMMM:39A,39E
MMM:039A CALL 1090
MMM:039D NOP
MMM:039E MOV DS,[001E]
#LMMM:1090,1098
MMM:1090 MOV [0052],DX
MMM:1094 MOV [0054],DX
MMM:1098 RET
#wCCPM_SYS
#^C
OA>
```

This completes the patch procedure.

## System Support 1 without ECO 179:

ECO (Engineering Change Order) 179 eliminates the possibility of the System Support 1 board's 8259A interrupt controllers missing an interrupt acknowledge from the CPU, thus crashing the system. ECO 179 speeds up the interrupt acknowledge path on the System Support 1 board. ECO 178 is documented in CompuPro Product Assurance Technical Bulletin #35, dated March 6, 1986.

ECO 179 may be applied only to revision 162G of the System Support 1 board. Earlier revisions of the System Support 1 board must be returned to the factory for an upgrade. The "ECO 179" label found on the component side of the board assures that this change has been made at the factory.

System Support 1 boards without ECO 179 already installed at the factory may be upgraded in one of two ways. The board may be easily ECOed in the field, or it may be returned to the factory for modification. For factory modification, contact the RMA desk for return authorization prior to returning the board.

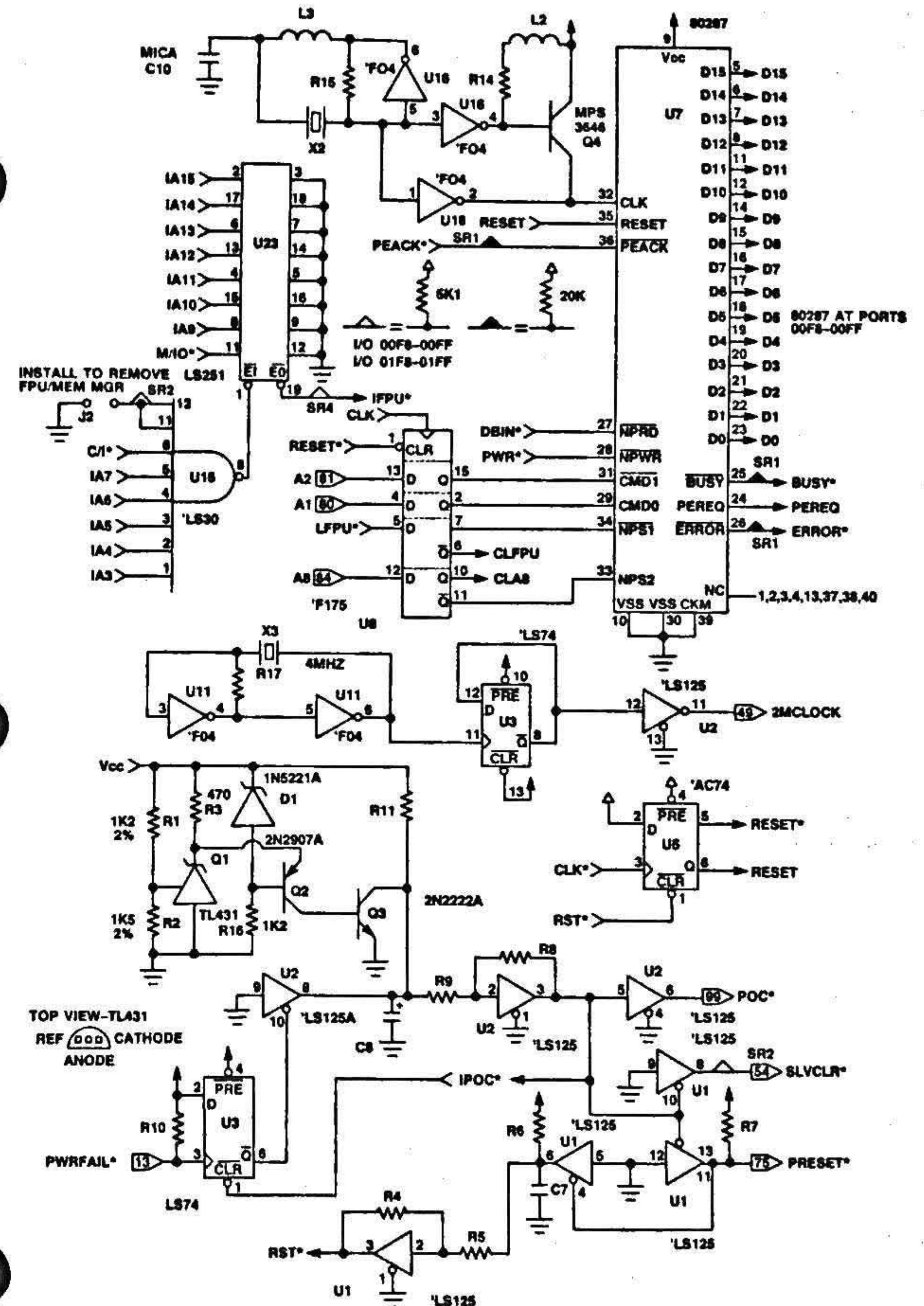
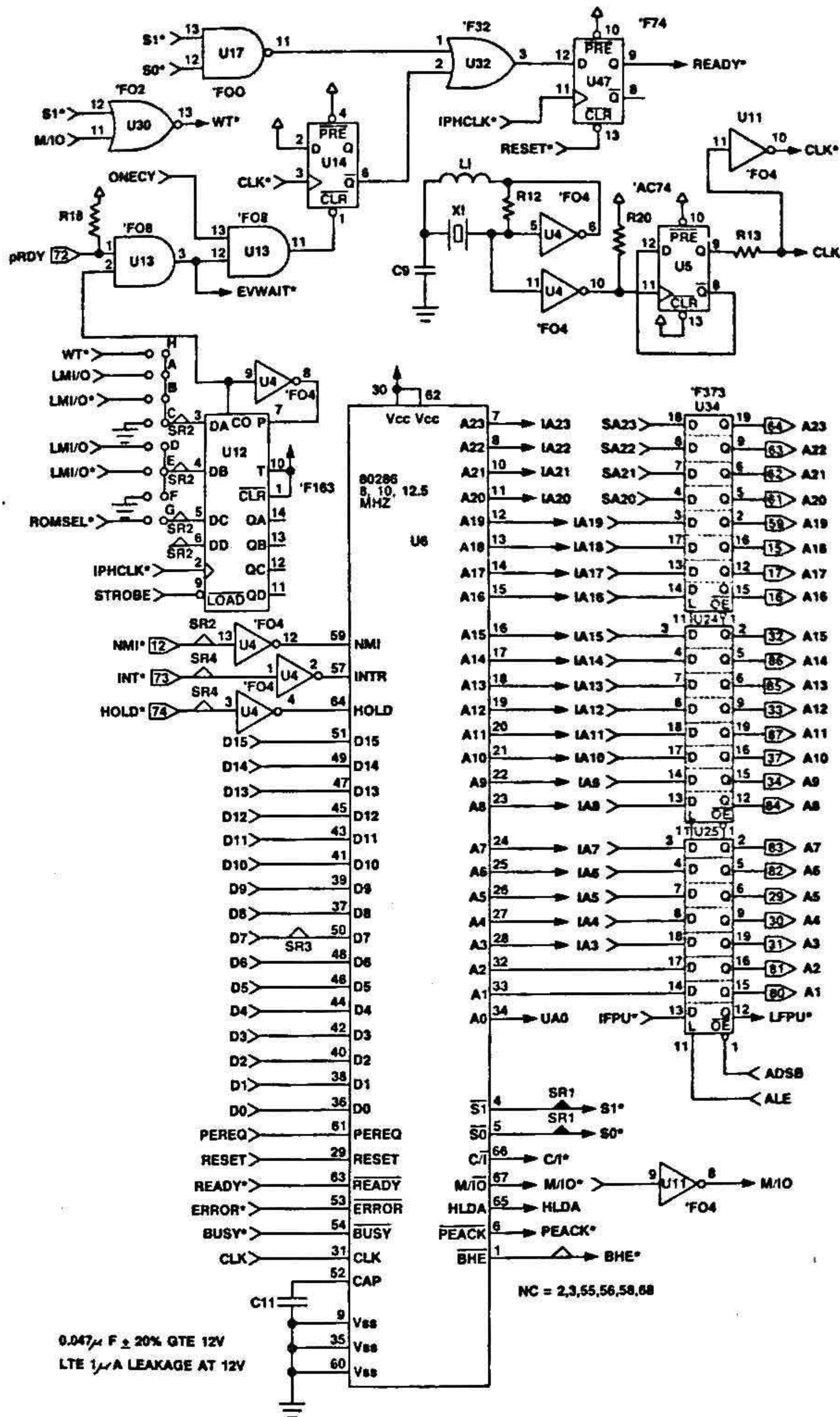
### Field Modification

The field modification of this board is very simple, and requires only 2 wires to be soldered to the board. If you do not feel comfortable making this modification after reading the instructions below, return the board to CompuPro for factory modification.

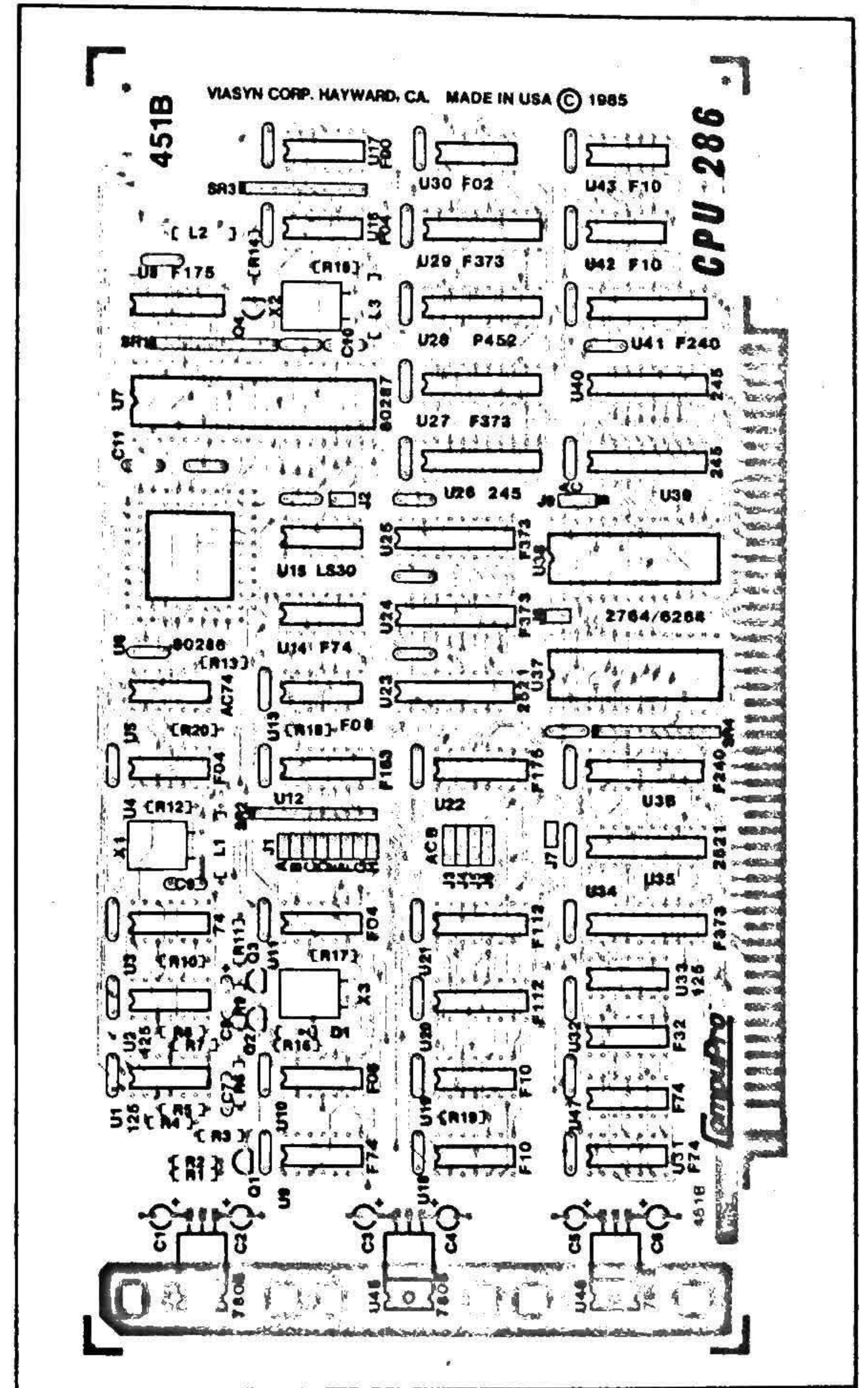
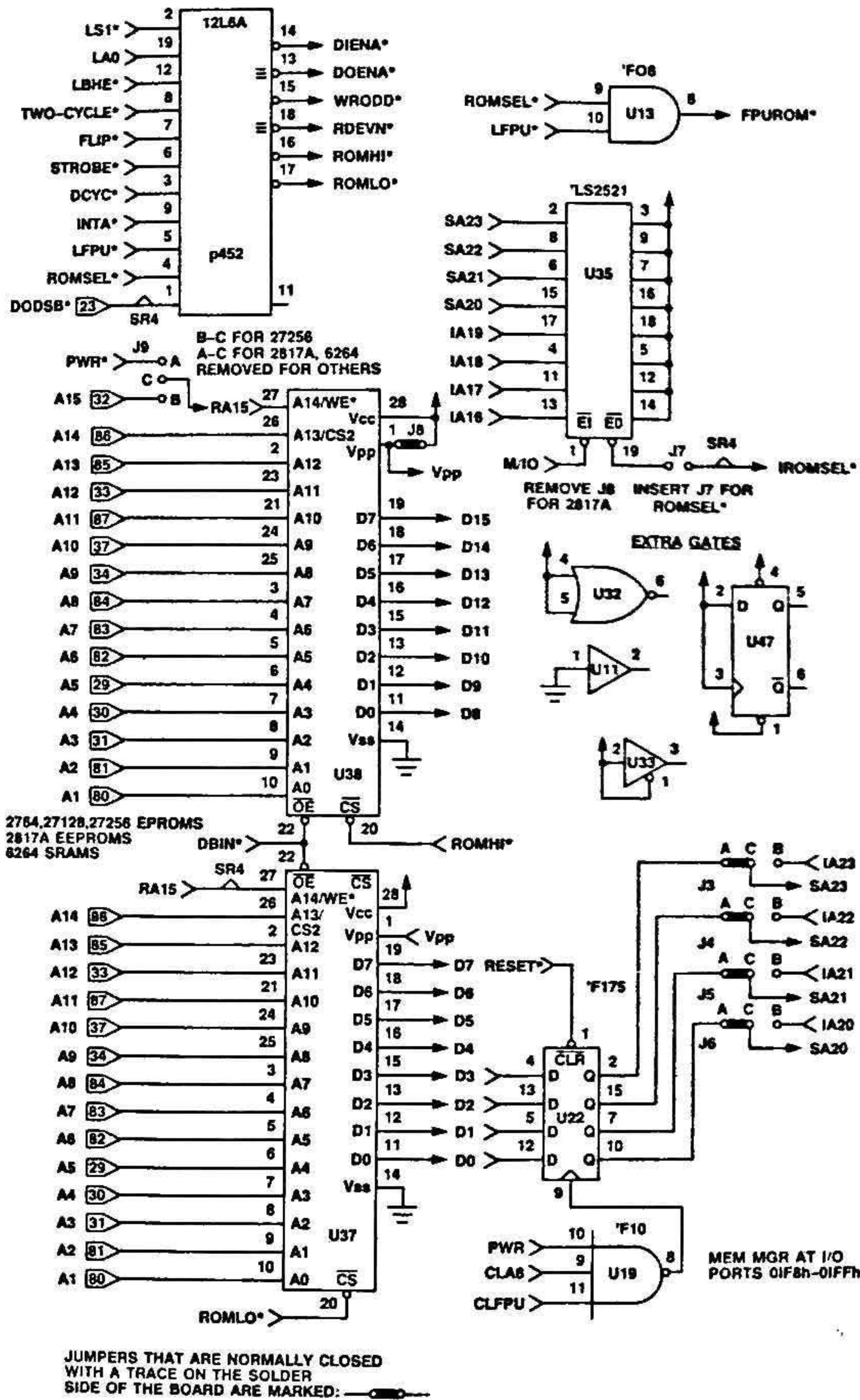
- 1) Locate U44 (74LS74) and remove it from its socket. Carefully bend pin 9 out so that when the IC is replaced, pin 9 will not make contact with the socket or anything else. Replace IC U44 back in its socket and verify that each pin is back in its hole.
- 2) Locate U18 (74LS32) and remove it from its socket. Carefully Bend pin 11 out so that when the IC is replaced, pin 11 will not make contact with the socket or anything else. Replace IC U18 back in its socket and verify that each pin is back in its hole.
- 3) On the solder side of the board, solder a short jumper wire (26 to 30 gauge) between pins 9 and 10 of IC U44.
- 4) On the solder side of the board, solder a short jumper wire between pins 1 and 8 of IC U46.
- 5) Attach a small white sticker to the board that says "ECO 179".

Be careful not to short the jumper wires to any other pins or traces, and use good soldering practices.









## LIMITED WARRANTY

Viasyn Corporation warrants this computer product to be in good working order for a period of ninety days from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, VIASYN will, at its option, repair or replace the item at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of VIASYN. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your System Center or dealer first. System Center technicians are trained to provide prompt diagnosis and repair of equipment failures. If you are not satisfied by the actions taken by your System Center or dealer, please call VIASYN at (415) 786-0909 to obtain a Return Material Authorization (RMA) number, or write to VIASYN at 26538 Danti Court, Hayward, CA, 94545-3999, Attn: RMA. Be sure to include a copy of the original bill of sale to establish a purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location and to use the original shipping container or equivalent. Be sure to mark the RMA number on the outside of the shipping container or delivery may be refused. Contact your System Center/dealer or write to VIASYN at the above address for further information.

All expressed and implied warranties for this product, including the warranties of merchantability and fitness for a particular purpose, are limited in duration to the above listed periods from the date of purchase and no warranties, either expressed or implied will apply after this period.

If this product is not in good working order as warranted above, your sole remedy shall be repair or replacement as provided above. In no event shall VIASYN be liable to you for any damages, including any lost profits, lost savings or other incidental or consequential damages arising out of the use of or inability to use such product, even if VIASYN or a System Center/dealer has been advised of the possibility of such damages, or for any claim by any other party.

If this product is out of warranty, please call or write the VIASYN RMA department to obtain a quotation for factory service. If this product was sold as a system by VIASYN, it may be eligible and you may elect to purchase on site/depot maintenance from SPERRY. Contact your System Center/Dealer, your nearest SPERRY office or VIASYN for more details.

If you have purchased a SPERRY service and maintenance agreement, the following two paragraphs also apply.

If VIASYN or its service contractor fails after repeated attempts to perform any of its obligations set forth in this agreement, VIASYN's or its service contractor's entire liability and VIASYN's customer's sole and exclusive remedy for claims related to or arising out of this agreement for any cause and regardless of the form of action, whether in contract or tort, including negligence and strict liability, shall be Viasyn's customer's actual, direct damages such as would be provable in a court of law, but not to exceed the cost of the item of equipment involved.

In no event shall VIASYN or its service contractor be liable for any incidental, indirect, special or consequential damages, including but not limited to loss of use, revenue or profit, even if VIASYN or its service contractor has been advised, knew or should have known of the possibility of such damages; or damages caused by VIASYN's customer's failure to perform its obligations under this agreement, or claims, demands or actions against VIASYN's customer by any other party.

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**EFFECTIVE 9/1/86.** This warranty supersedes all previous warranties. All previous editions are obsolete.

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