Century Data Systems
A Xerox Company

Marksman

Marksman Performance Specification M20, M40, M80, M160

76220-306

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March 1982

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the technical manuals, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

RECORD OF REVISIONS	
REVISION	**NOTES**
0	ORIGINAL ISSUE
1	Revised — December 1978
2	Major changes incorporated in the revision are:
	—Modification of start time
	—Addition of expanded status
	—Updating of command flow charts
	—Expanded on the HEAD ADVANCE command
	—Updating of timing charts
	—Addition of spec for interfaces lines with PIA chip
3	Addition of Diagnostics
	—Update to include M40
	—Add Section 11
4	Addition of M80 and M160 Specifications — July/81
5	Corrections — reprint — Aug/81
6	Incorporate TMC — reprint — Mar/82

CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

TABLES

SECTION 1
INTRODUCTION

1.1 PURPOSE

This manual contains information necessary to interface a MARKSMAN disk drive to a controller and ultimately to a computer system and provides the technical specifications for reference in OEM contracts.

1.2 RELATED DOCUMENTS

Companion documents on MARKSMAN that are available include:

Intelligent Marksman Performance Specification	P/N 76222-9XX
Marksman Installation Manual	P/N 76220-2XX
Intelligent Marksman Maintenance Diagrams	P/N 76222-7XX
Model T2004A Exerciser Installation & Operation	P/N 76221-2XX
Marksman Controller Technical Manual	P/N 76222-1XX
Marksman Disk Drive Technical Manual	P/N 76220-10X
Basic Marksman Installation Recommendations	P/N 23603-XXX

1.3 GENERAL DESCRIPTION

Data integrity comparable to that found in large disk systems is assured by the use of Winchester style heads and media. System reliability is maximized by the sealed contaminiation controlled disk compartment and the reduction in the parts count achieved by the use of a microprocessor.

The economy is achieved by the use of a band positioner driven by a stepper or torque motor, allowing it to slew at high speeds, thus creating significant improvements in motor performance.

MARKSMAN is designed to enable the OEM systems manufacturer to achieve a high degree of flexibility and the largest practical percentage of added value in the memory subsystem. The drive electronics include all of the analog functions, and those digital functions that are intimately related to the mechanics such as position motor control and fault monitoring. The interface to the drive is by direct connection to the microprocessor, Parallel Interface Adaptor (PIA), or a version of the ANSI standard SMD Interface.

- 20MB, 40MB, 80MB, or 160MB of low cost, high performance storage.
- Winchester Technology Heads and Media provide state-of-the-art performance.
- High speed Start/Stop, head landing zones and a spindle motor brake maximize head/media life.
- Microprocessor Based Electronics provide flexibility and simplify maintenance.
- VFO Data Separator standard.
- No Preventive Maintenance required.
- Provision for Mounting embedded customer designed formatters and controllers.

SECTION 2
SPECIFICATIONS

2.1 OPERATIONAL SPECIFICATIONS

2.1.1

Operational specifications for MARKSMAN Disk Drives are listed in Table 2-1 below.

2.2 RELIABILITY

2.2.1 Mean Time Between Failures

MTBF is defined by the expression:

$$\text{MTBF} = \frac{\text{Operating Hrs.}}{\text{No. of Equipment Failures}}$$

Operating hours relate to the total "AC Power On" hours less any maintenance time. Equipment failures are defined as those failures requiring repairs, adjustments or replacements on an unscheduled basis, i.e., emergency maintenance required because of hardware failure or substandard performance. Excluded is downtime or substandard performance due to operator error, adverse environment, power failure, controller failure, cable failure or other failures not caused by the drive.

The basic MARKSMAN has a designed MTBF of 8000 hours. The sealed mechanism alone has a designed MTBF of 25,000 hours.

To establish a meaningful MTBF, operating hours must be greater than 20,000 hours and include all sites where the drives are used.

2.2.2 Mean Time To Repair

MTTR is defined as the time for an adequately trained and competent serviceman to diagnose and correct a malfunction at the subassembly level. MARKSMAN is designed so that the MTTR is to be less than 1.0 man-

Table 2-1. Disk Drive Specifications

Model	M-20	M-40	M-80	M-160
Bytes per track	24,000	24,000	24,000	32,000
Tracks per cylinder	4	8	6	6
Number of cylinders	210	210	560	837
Bytes per drive	20.16M	40.32M	80.64M	160.70M
Single track positioning time	20 ms	20 ms	12 ms	12 ms
Average positioning time	65 ms	65 ms	50 ms	50 ms
Maximum positioning time	130 ms	130 ms	100 ms	100 ms
Rotational speed (nominal)	2400 RPM	2400 RPM	2400 RPM	2400 RPM
Average latency time	12.5 ms	12.5 ms	12.5 ms	12.5 ms
Recording density	7,545 BPI	7,545 BPI	7,545 BPI	10,000 BPI
Track density	182 TPI	182 TPI	480 TPI	712 TPI
I/O Transfer rate	960 Kilobytes/sec 7.68 MHz	960 Kilobytes/sec 7.68 MHz	960 Kilobytes/sec 7.68 MHz	1.28 Megabytes/sec 10.24 MHz
Bit Cell time	130 ns	130 ns	130 ns	97.65 ns
Recording code	MFM	MFM	MFM	MFM
Interface code (data)	NRZ Serial	NRZ Serial	NRZ Serial	NRZ Serial
Positioning method	Stepper Motor Band Positioner	Stepper Motor Band Positioner	Torquer Motor Band Positioner	Torquer Motor Band Positioner
Start time (nominal)	3 minutes	3 minutes	3 minutes	3 minutes
Write-to-Read Delay	16 microseconds	16 microseconds	16 microseconds	16 microseconds
Read-to-Write Delay	100 nanoseconds	100 nanoseconds	100 nanoseconds	100 nanoseconds

hours. The sealed portion of the drive is not field repairable and must be returned to the factory for repair in a special clean room environment.

2.2.3 Preventive Maintenance Time

No preventive maintenance is required.

2.3 DATA INTEGRITY

2.3.1 Recoverable Errors

A recoverable error is one which may be corrected by no more than 9 attempts to read the record. Any combination of seek-write, seek-read, seek-rezero is allowed without limitation of combination or duty cycle. Data patterns and track position do not affect data error rate performance. The recoverable read error rate for MARKSMAN is less than one error in 10^{10} bits read.

2.3.2 Non-Recoverable Errors

A non-recoverable error is one which remains after 9 attempts to read the record in which an error is located. The non-recoverable error rate for MARKSMAN is less than one error in 10^{13} bits read.

2.3.3 Positioning Errors

The positioning error rate is less than one error in 10^{6} seek executions.

2.3.4 Media

Century Data Systems guarantees 210 of 213 available cylinders on the M20 and M40, 560 of 569 available cylinders on the M80, and 837 of 845 available cylinders on the M160, including cylinder zero (0), head zero (0) to be error free. This is based upon twelve data read passes over the entire surface. All media defects will be identified to the customer by a written notice attached to the disk drive.

SECTION 3
CDS INTERFACE

3.1 DISK DRIVE INTERFACE SIGNALS

Signals appearing at the MARKSMAN Disk Drive CDS interface and their use are shown in Tables 3-1 and 3-2. Refer to Section 6 for connector and pin numbers.

Table 3-1. Control Signals

Signal Name	Mnemonic	I/O	Description
Control/Data Bus	CBUSO-7	Both	A high active 8 bit wide bus used to transfer commands from the interface and status to the interface.
Control Request	CREQ	I	A high active line from the interface, used in conjunction with the CACK line to form a handshake between the Interface and the Drive, CREQ indicates to the Drive: 1. The interface has placed a byte of command or a byte of data on the Interface Data Bus. 2. The Interface has accepted the ending status from the Drive.
Control Acknowledge	CACK	O	A high active line from the drive to the Interface to: 1. Acknowledge receipt of a byte of command or data from the Interface. 2. Notify the Interface the drive has placed a byte of status information on the Control/Data Bus.
Control Ready	CRDY	O	A high active line from the Drive to the Interface indicating the drive is in the input mode and is waiting for a command.
Control Status	CSTAT	O	A high active line from the Drive to the interface indicating that the drive has placed a byte of status information on the Control/Data Bus. This line is up along with CACK.
Drive Ready	DRDY	O	A positive true line from the drive to the interface indicates that the drive is up to speed, DC power is safe, and no drive faults.
Reset	RST/	I	A low active signal from the interface which provides the drive with an unconditional reset and causes the heads to be relocated to Track zero. The pulse width must be ⩾10 microseconds. The drive will start the rezero when RST/ goes high. It requires 2 seconds maximum to move to Track zero.
Index	IDX	O	A high active line from the drive used to indicate the physical beginning of a track of data. The INDEX pulse width is nominally 100 microseconds for the M20/M40 and 2 microseconds for the M80 and M160. The leading edge of index is the beginning of the first sector.

Table 3-1. Control Signals (Continued)

Signal Name	Mnemonic	I/O	Description
Sector	SEC	O	A high active line from the drive used to indicate the physical beginning to the data record within a track. The SECTOR pulse width is nominally 1.02 microseconds. Note that there is no sector pulse at the beginning of the first sector (See Index).
Write Unsafe	WRTUSF	O	A positive true line from the drive to the interface used to indicate an unsafe write process was attempted. (i.e., multiple heads selected, DC unsafe, write on protected head). It is cleared when status is presented.

Table 3-2. Read/Write Signals

Signal Name	Mnemonic	I/O	Description
Write Data	NRZIN	I	A positive true line from the interface to the drive used to transmit serial write data to the drive.
Write Clock	WRTCLK	O	A positive true line from the drive to the interface used to clock write data from the interface. This clock is phase locked to the spindle rotation at all times. The leading edge of the pulse signifies a bit, and the nominal pulse duration is 130 nanoseconds.
Write Gate	WRTGATE/	I	A negative true line from the interface to the drive used to write data on the selected head.
Read Data	NRZOUT	O	A positive true line from the drive to the interface used to transmit serial read data to the interface. This output is connected to the interface only, after RDGATE becomes true. All other conditions provide a clamped logic zero output state.
Read Clock	RDCLK	O	A positive true line from the drive to the interface used to clock read data from the drive. The leading edge of the pulse signifies the beginning of a bit cell, and the nominal pulse duration is 130 nanoseconds.
Read Gate	RDGATE	I	A positive true line from the interface to the drive shall start lock-up of the phase lock loop (PLL) in the Data Separator (which controls the RDCLK output). Read Gate true must not be raised over write splice (read gap) areas and must occur after seek complete. Read Gate false must occur prior to any write splice and must be maintained 4 bytes at the Read Cap.
MPU Clock	1MHZ	O	This one megahertz clock is provided for use by the controller in functions that do not require syncronization to the disk speed.

3.2 INTERFACE FUNCTIONS

The controller interface functions may be divided into five areas:

- Single Byte Commands (SEQUENCE, REZERO, STATUS REQUEST, ADVANCE HEAD, DIAGNOSE)
- Two Byte Commands (SEEK-M20/M40, SET SECTOR)
- Three Byte Command (SEEK-M80/M160)
- Data Transfer (READ & WRITE operations)
- Drive Malfunctions and Controller Errors

3.3 ONE BYTE COMMANDS (Figures 3-1 thru 3-4)

3.3.1 Sequence

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	X

Bit 0 = 0 Sequence Up

Bit 0 = 1 Sequence Down

The SEQUENCE command causes the disk drive motor to power up (Bit 0 = 0) or power down (Bit 0 = 1). During a power up, the speed of the disk is checked and when speed is within tolerance, the heads are positioned to cylinder zero, head zero. DRDY and CRDY are both held inactive for 3 minutes. This allows time for the air circulation and read/write heads in the sealed unit to stabilize. During a power down, the heads are positioned to the landing zone before power is removed from the drive motor. A sequence UP command must be used to bring the drive up to speed and ready. If power fails, the heads land where they are.

3.3.2 Rezero

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0

The rezero command causes the heads to be repositioned to cylinder zero, head zero.

3.3.3 Status Request

7	6	5	4	3	2	1	0
0	0	0	0	0	X	X	X

XXXX

0000 Ending Status of the drive returned to the interface (Table 3-3).
0001 Illegality Error Status (Table 3-4).
0010 Last Command (MSB-1st or only byte) M20, M40.
Hardware Error Status (Table 3-5) M80, M160.
0011 Last Command (LSB-2nd byte on 2 byte commands) M20, M40.
Last Command (MSB) M80, M160.
0100 Current Cylinder Number. M20, M40
Last Command (NMSB). M80, M160.
0101 Sector Per Track. M20, M40.
Last Command (LSB) M80, M160.
0110 Diagnostic Status. M20, M40.
Current Cylinder Number (MSB). M80, M160.
0111 Diagnostic Status. M20, M40.
Current Cylinder Number (LSB). M80, M160.
1000 Sector Per Track. M80, M160.
1001 Diagnostic Status. M80, M160.
1010 Diagnostic Status. M80, M160.

Table 3-3. Ending Status Bit Significance

Bit 0	Track zero: Heads are located over track zero.
1	Landing zone: Heads are located over landing zone.
2	Illegal Conditions. See Illegality Error Status.
3	Drive Ready. Disk is up to speed.
4	Spin acceleration/deceleration out of limit. M20, M40. Hardware Error (M80, M160). See Hardware Error Status.
5	End of cylinder
6	Diagnostic error
7	Track zero error. M20, M40. Unsolicited interrupt. M80, M160.

Table 3-4. Illegality Error Status

Bit 0	Sector Length Switch (S2)
1	Sector Length Switch (S1)
2	Illegal Set Sector
3	Sector Per Track set by 0 = Sector Length Switches 1 = Set Sector Command
4	Illegal Rezero or Illegal Seek (Drive not up to speed or attempted from landing zone)
5	Illegal cylinder or head
6	Illegal Command
7	Attempted Write on a Write Protected Head

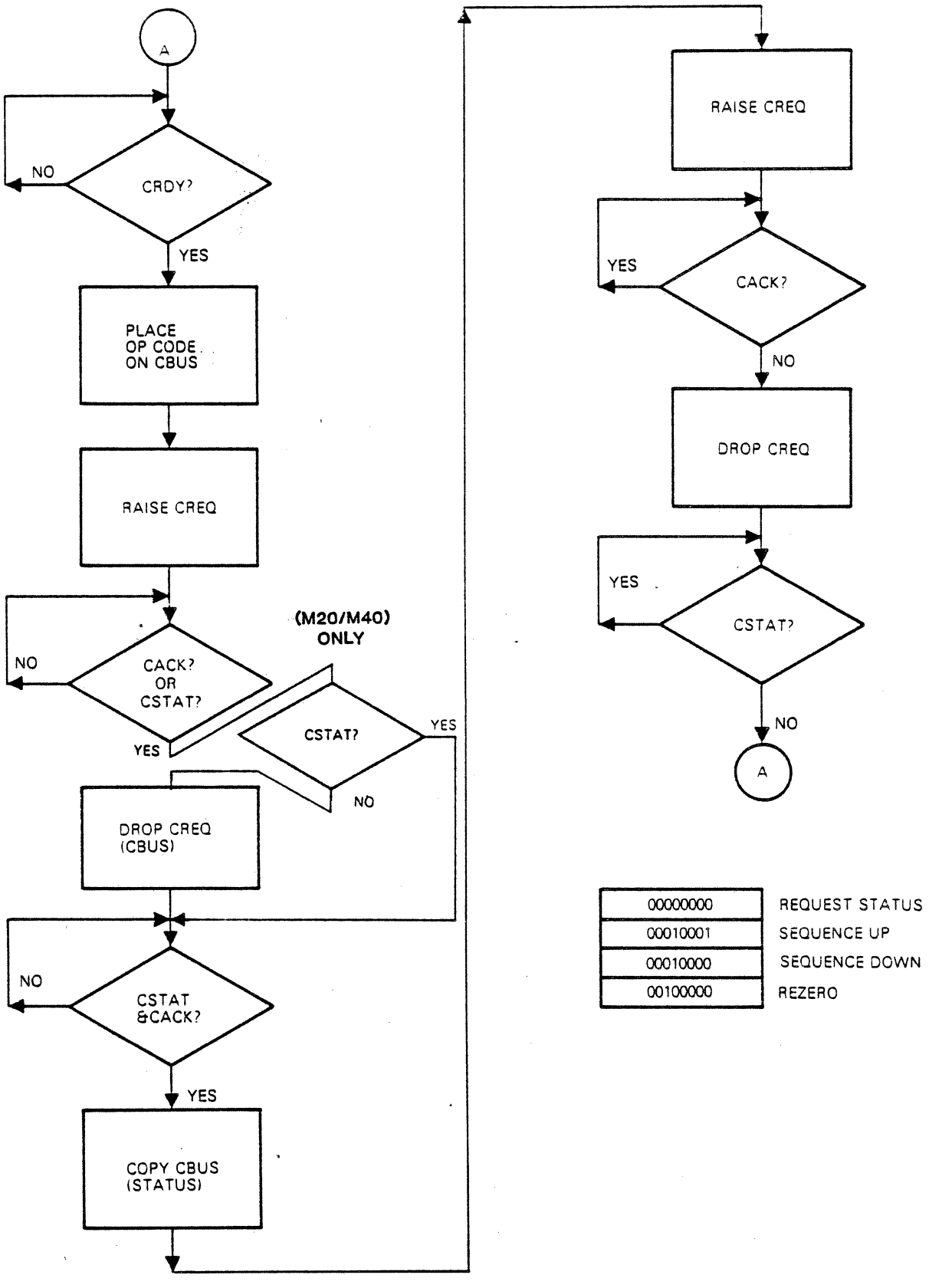


Figure 3-1. One Byte Commands (Except Head Advance) Flow Chart (Suggested Procedure for User)

Table 3-5. Hardware Error Status (M80 and M160 only)

Bit 0	Read/Write Fault (Multiple Head Select)
1	Over Temperature Error
2	Power Amplifier Unsafe
3	DC Unsafe
4	UTH Error
5	Seek Incomplete
6	Disk Spin Stopped
7	Spin Speed out of limit

The Status Request command causes the current status of the drive to be returned to the interface. Status bits are cleared after being presented to user except for bits 0, 1, 3 and 5. Illegality Error status bits are cleared after a specific request for Illegality Error status except bits 0, 1, and 3.

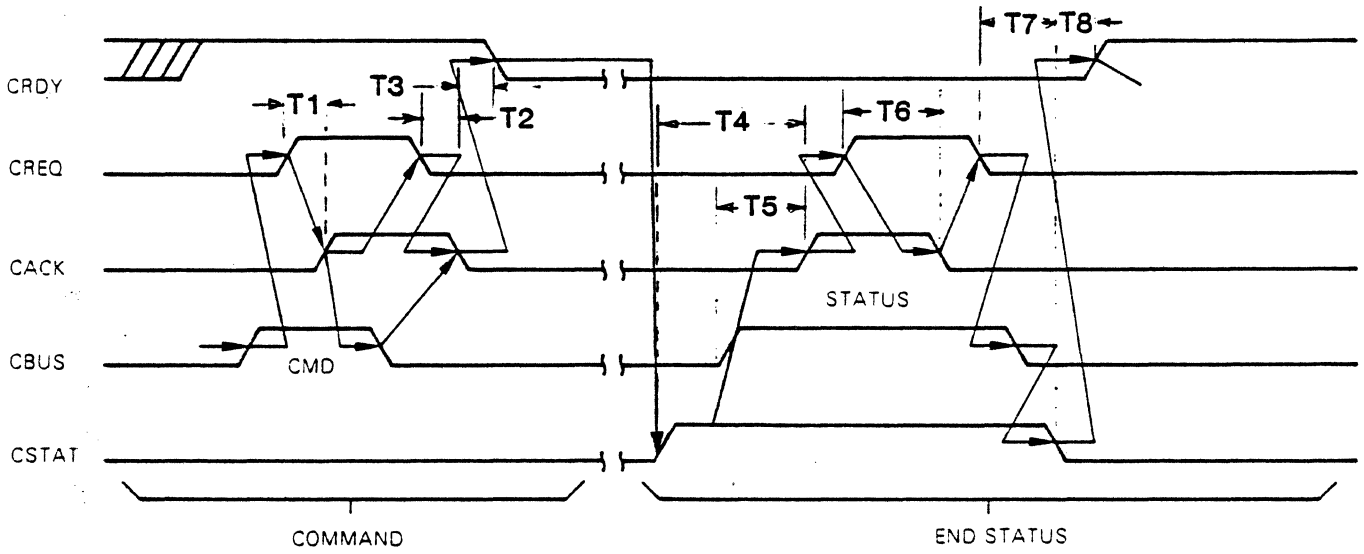


Figure 3-2. One Byte, Commands (Except Head Advance) — Timing Diagram

Table 3-6. One Byte Command (Except Head Advance) Timing Transaction

HANDSHAKE TRANSACTION	TIME	MINIMUM	TYPICAL	MAXIMUM	UNIT
REQ ↑ — ACK ↑ (Command Byte)	T1	20	60	300	µs
REQ ↓ — ACK ↓ (Command Byte)	T2	8	17	40	µs
ACK ↓ — CRDY ↓ (Command Byte)	T3	8	14	30	µs
STAT ↑ — ACK ↑ (Status Byte)	T4	8	38	60	µs
BUS STABLE — ACK ↑ (Status Byte)	T5	4	6		µs
REQ ↑ — ACK ↓ (Status Byte)	T6	8	17	40	µs
REQ ↓ — STAT ↓ (Status Byte)	T7	8	50	100	µs
STAT ↓ — CRDY ↑ (Status Byte)	T8	−1	0	+1	µs

*For motion commands, mechanical delay times must be added.

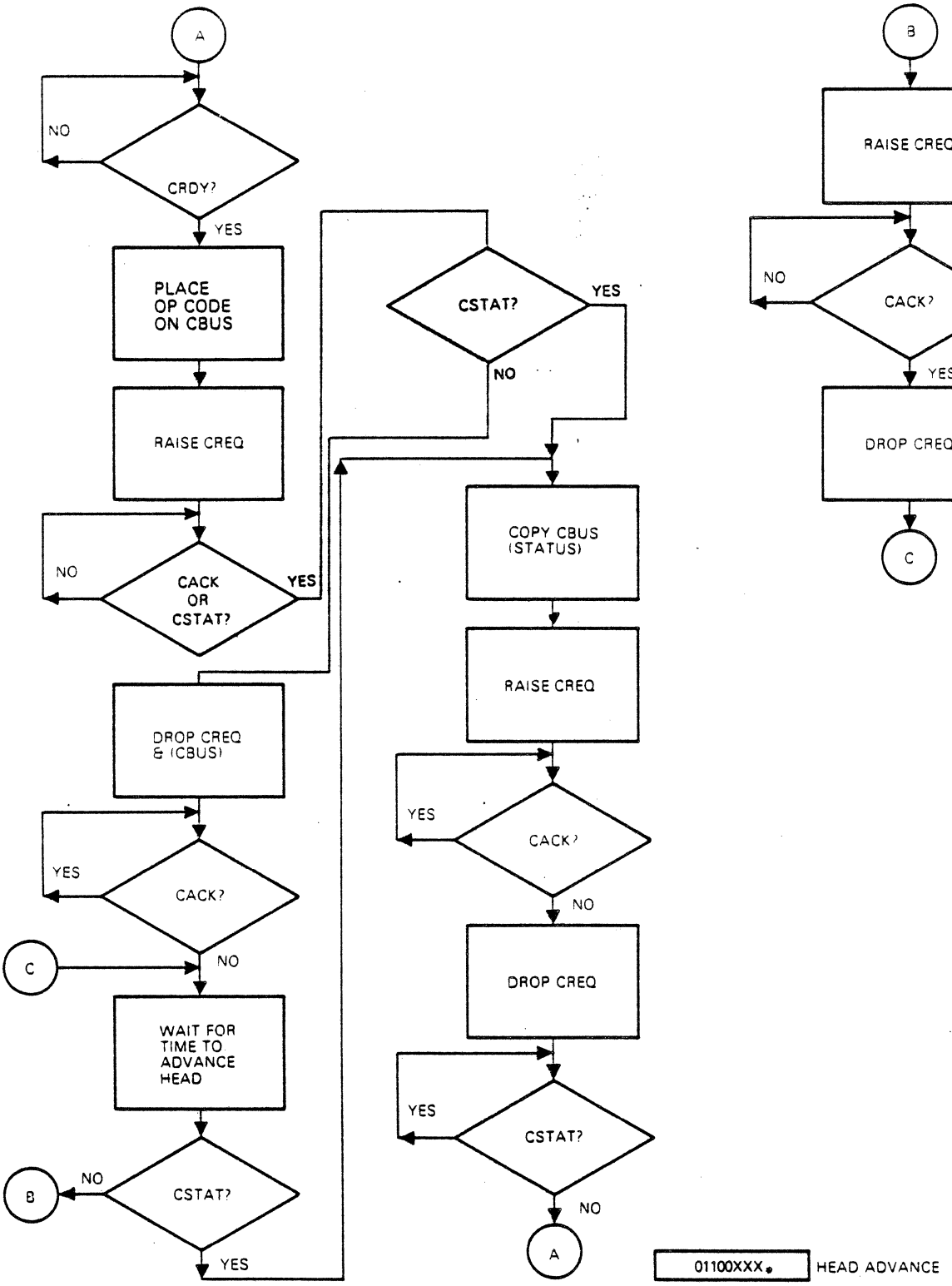
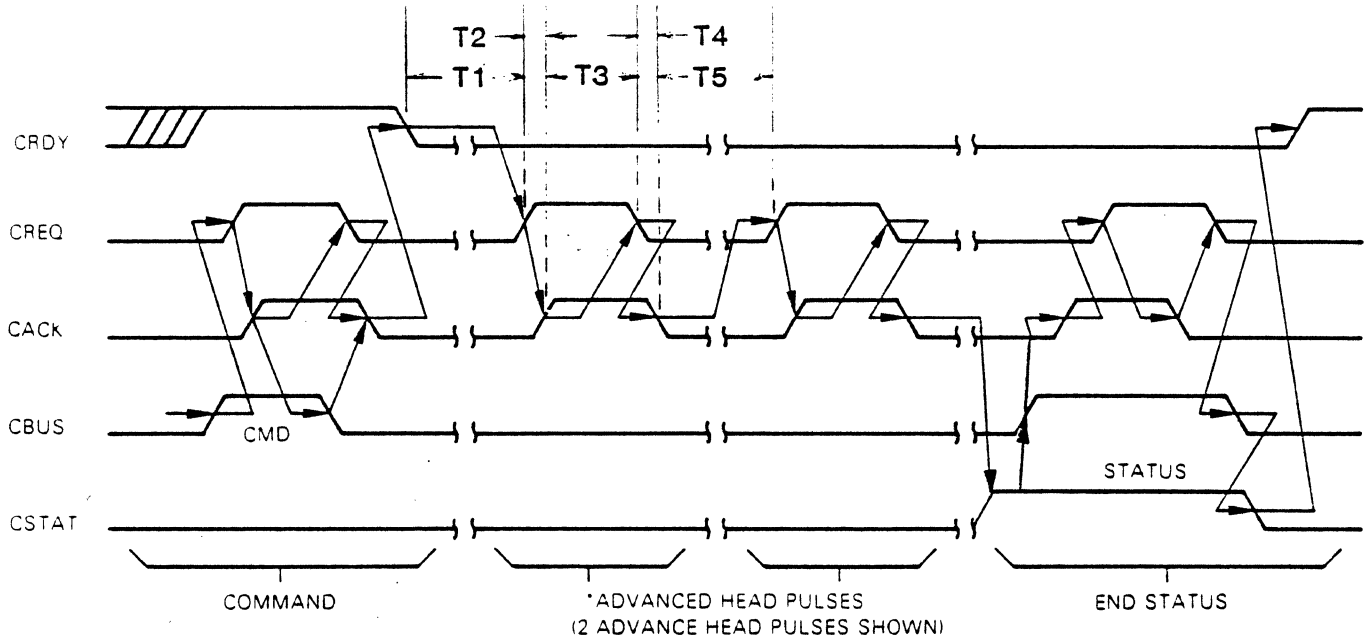


Figure 3-3. One Byte Command Head Advance Command Flow Chart (Suggested Procedure for User)



*NOTE: The head advance operation is still performed prior to the rise of CACK.

Figure 3-4. One Byte Command Head Advance Command — Timing Diagram

Table 3-7. Head Advance Command — Timing Transaction

TRANSACTION	TIME	MINIMUM
CRDY ↓ — CREQ ↑	T1	80 μs
CREQ ↑ — CACK ↑	T2	22 μs
CACK ↑ — CREQ ↓	T3	7 μs
CREQ ↓ — CACK ↓	T4	16 μs
CACK ↓ — CREQ ↑	T5	44 μs

3.3.4 Head Advance

7	6	5	4	3	2	1	0
0	1	1	0	0	X	X	X

XXX

000 NO OP
001 Advance Head One Time
010 Advance Head Two Times
011 Advance Head Three Times
100 Advance Head Four Times
101 Advance Head Five Times
110 Advance Head Six Times
111 Advance Head Seven Times

This command provides a means of advancing the head address more rapidly than can be done using the SEEK COMMAND thereby allowing sequential sector accesses across head boundaries.

The HEAD ADVANCE COMMAND places the drive in a state where it waits for the rise of CREQ. The drive advances the head address in 11μs to 23μs after CREQ goes active. During the CREQ-CACK handshake, the drive does not copy the CBUS. STATUS is presented when either the commanded head advance count is depleted or the head address is advanced to the last head. CRDY will remain inactive (and the drive incapable of accepting another command) until the STATUS is delivered. The end cylinder bit (bit 5) in the STATUS word will be active whenever the last head is selected.

The command sequence for a no-motion seek takes over 500 μs (500 bytes) to complete, measured from the initial rise of CREQ to the rise of CRDY after end status. (The actual time depends on the controller's contribution to sequence delays.) The target head is selected no earlier than 300 μs (300 bytes) after the initial rise of CREQ. The end-of-track pad for seek is, therefore, very large.

The use of the HEAD ADVANCE command sequence yields selection of the target head 11 μs to 23 μs after CREQ rises. READ gate must be delayed 16 bytes after head selection, but does not occur (in the specified formats) until 16 bytes after the sector pulse, hence, the head-advancing CREQ must rise 23 μs before the sector

pulse. It may rise as early as 10 μs (10 bytes at low disk speed) before the end of the last data to be read. The minimum end-of-track pad for head advance is, therefore, 13 bytes. The total sector length calculation in paragraph 5-3 shows that most sector formats provide some inherent pad in the last sector.

3.3.5 Diagnose

7	6	5	4	3	2	1	0
1	0	0	0	X	X	X	X

Where XXXX is the diagnostic test number.
Status is returned in status bytes 6 and 7 by the M20, M40 and status bytes 9 and 10 by the M80, M160.

Test No.

XXXX = 0
RAM Test — stores 55_{16} in all RAM locations and checks contents of all locations. Stores AA_{16} in all locations and checks contents of all locations. Stores incrementing pattern in successive locations and checks contents of all locations. Exits with status bytes clear if OK. If bad, exits with diagnostic error flag set in status byte 0, address of bit failure in status byte 6 and bit pattern in byte 7. M80 and M160 uses status bytes 9 and 10.

XXXX = 1
Real Time Clock Test — checks real time clock timeouts against programmed timeouts. Exits with status bytes clear if OK. If bad, exits with diagnostic error flag set in status byte 0 and appropriate bits set in status byte 6 (byte 9 for M80, M160) as follows: bit 4 = timeout; bit 5 = unsolicited; bit 6 = interrupt; bit 7 = error. Status word 7 (word 10 for M80, M160) is always clear.

XXXX = 2
Track Zero Test (M20, M40 only) — checks track at which track zero flag resets while stepping in and the track at which the flag sets while stepping out. Exits with extended status byte 6 containing track number at which track zero flag reset; status byte 7 contains track number at which it is set. If bad, track zero error bit is set in status byte 0 and status bytes 6 and 7 are cleared.

XXXX = 3
Disk Speed Test — The M20 and M40 measures time between index pulses with real time clock. Exits with MSB of speed in status byte 6 and LSB in status byte 7. If bad, both exit with diagnostic error bit set. M80 and M160 do not perform this test.

XXXX = 4
Read RAM — The contents of RAM are sequentially output to the user starting with address 0.

XXXX = 5
ROM Test — builds a checksum for each 256 bytes of program PROM and compares it to a checksum table. Exits with status bytes clear if OK. If bad, diagnostic error bit is set and upper address of bad block is in status byte 6 and lower address is in byte 7. M80 and M160 uses bytes 9 and 10.

XXXX = 6
MPU Test — a non-exhaustive MPU exercise which checks stack manipulation, addressing modes, interrupt and sub-routine linkage. Exits with the status bytes clear if OK. If bad, the diagnostic error bit is set and the condition code is returned in diagnostic status byte 6. Status byte 7 is clear. (M80 and M160 uses bytes 9 and 10).

XXXX = 7
Handshake Test — This is a two-byte command. The second byte will be echoed to the user as status. Normal status will not be presented and the diagnostic status bytes will not be changed. For effective testing of the user interface, the following sequence will test all data lines. 00, 01, 02, 04, 08, 10, 20, 40, 80, FF, FE, FD, FB, F7, EF, DF, BF, 7F (all in hex).

XXXX = 8
Seek Test — The seek test will seek from track 00 to track N. N being track one and incrementing until N equals track 212 (M20, M40), 568 (M80), and 844 (M160). It will verify that the carriage returns to track zero each time by looking at the track 00 bit. If test fails, the last track that was successfully restored from N to rezero will be stored in status byte 6. Byte 7 will be cleared and the diagnostic error bit will be set in status byte 0. If test passes, status byte 6 and 7 and the diagnostic error bit in status byte 0 will all be cleared. M80 and M160 uses status bytes 9 and 10.

On power up or reset, the following diagnostic tests will be performed automatically:

RAM Test
ROM Test
MPU Test
RTC Test

If an error occurs, the diagnostic status bit in status byte 0 will be set, however the diagnostic status bytes (status bytes 6 and 7 or 9 and 10 for M80 and M160) will be unaffected. The user must then run each test to determine which test(s) failed.

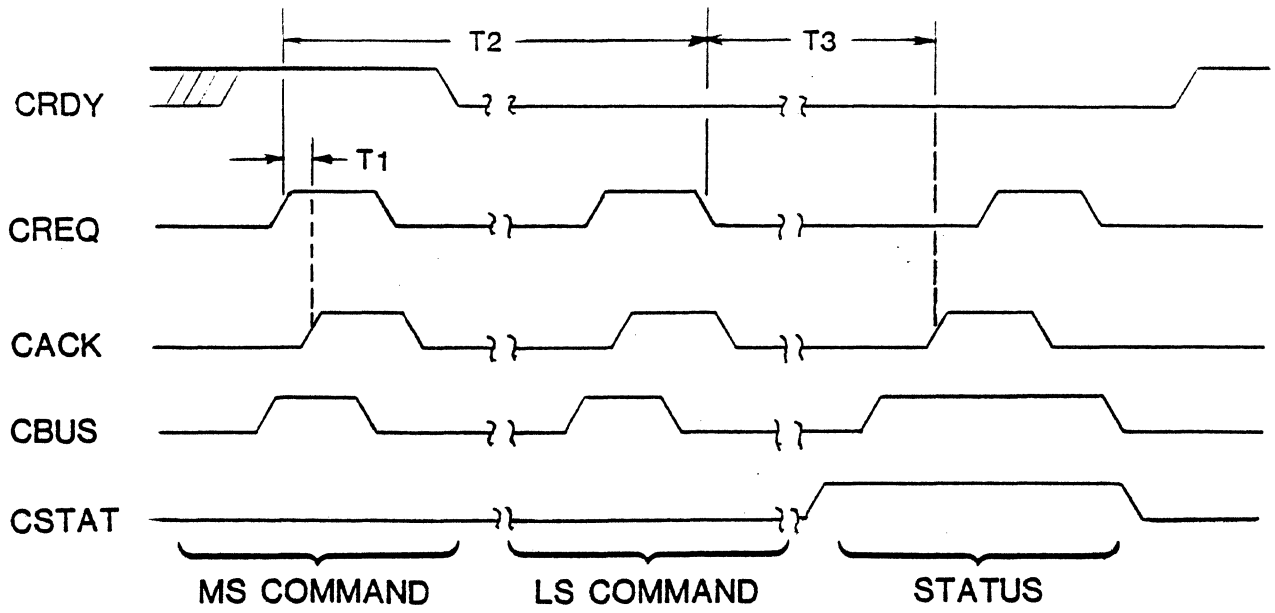


Figure 3-5. Diagnostic Timing Diagram

Table 3-8. Diagnostic — Timing Transaction

TRANSACTION	TIME	
CREQ↑ – CACK↑	T1	Max 204 μs; min 57 μs (approximate)
CREQ↑(1) – CREQ↓(2)	T2	Avg 235.41 ±5% ms; max 246.3 ms (approximate)
CREQ↑(2) – CACK↑(3)	T3	(approximate for each test) **Test** 0 9.038 ms 1 70.49 ms 2 739.0 ms 3 47.71 ms 4 16.07 ms 5 31.26 ms 6 317.9 μs 7 255.0 μs 8 32.82 sec 9 114.7 ms A 120.3 ms

3.4 TWO BYTE COMMANDS (Figures 3-6 and 3-7)

3.4.1 Seek (M20, M40)

7	6	5	4	3	2	1	0
0	1	0	0	0	H	H	H
Cylinder Address							

The SEEK command is used to position the heads over the specified cylinder and select the head addressed by the low order bits of the command byte. The SEEK command requires one Byte transferred with the command to specify the cylinder. Bit 3 is reserved.

3.4.2 Set Sector

7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0
Sector Count							

This command is used to override the switch setting of S1 and define the number of sector pulses from 3 to 255.

This selection will remain until another SET SECTOR command is issued or upon re-powering-up, at which time, it will use the switch settings.

See paragraph 5.3 for sector calculations.

3.5 THREE BYTE COMMAND

3.5.1 Seek (M80 and M160)

7	6	5	4	3	2	1	0
0	1	0	0	0	H	H	H
CYL ADDR. (MSB)							
CYL ADDR. (LSB)							

The SEEK command is used to position the heads over the specified cylinder and select the head addressed by the low order bits of the command byte. The SEEK command requires two bytes to be transferred with the command to specify the cylinder. Bit 3 is reserved.

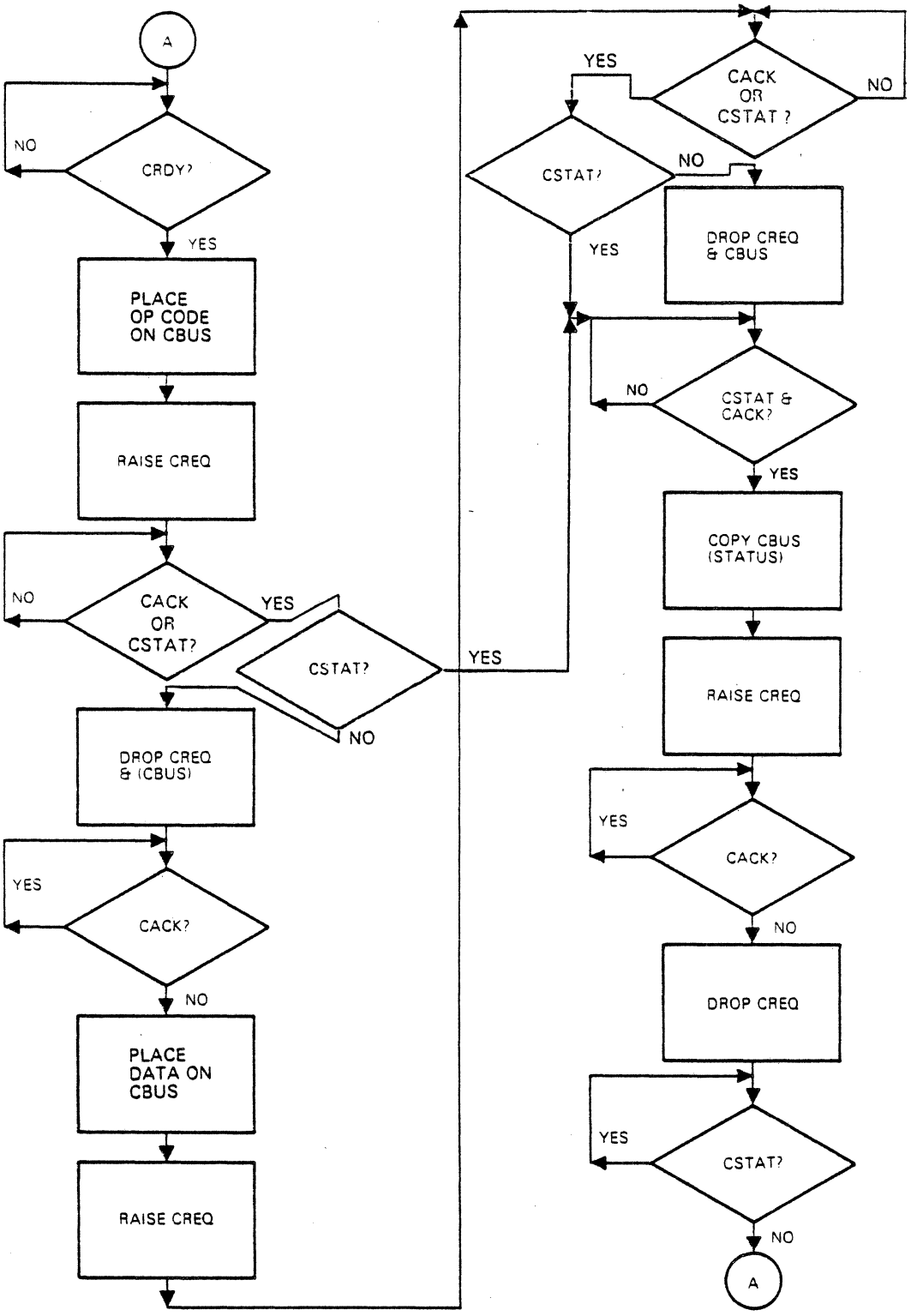


Figure 3-6. Two Byte Commands — Flow Chart (Suggested Procedure for User)

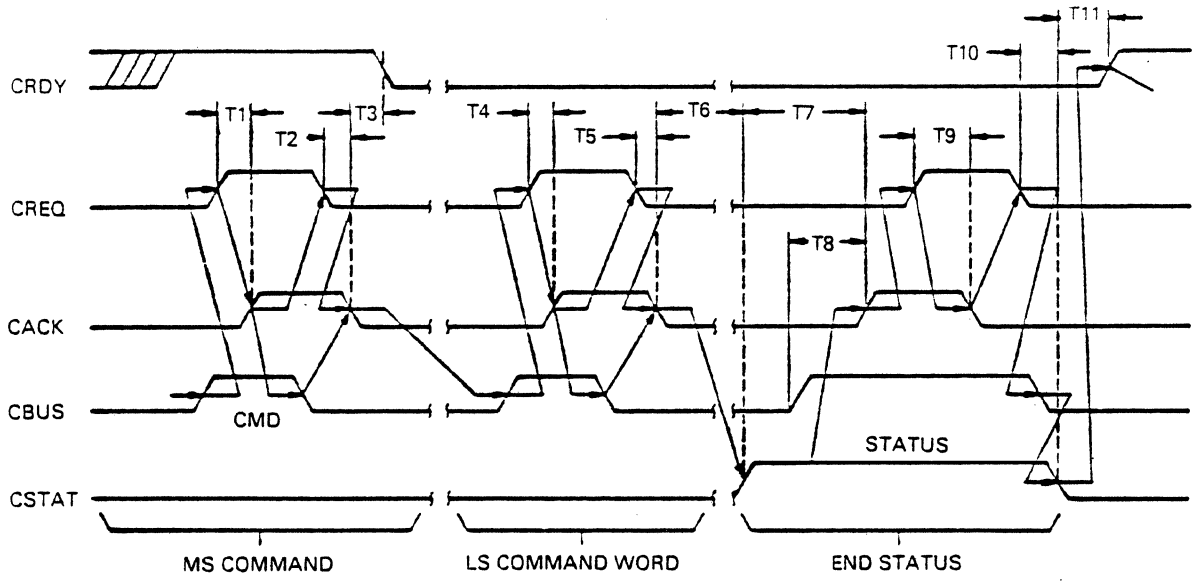


Figure 3-7. Two Byte Commands — Timing Diagram

Table 3-9. Two Byte Commands — Timing Transaction

HANDSHAKE TRANSACTION	TIME	MINIMUM	TYPICAL	MAXIMUM	UNIT
REQ ↑ — ACK ↑ (Command Byte)	T1	20	60	300	µs
REQ ↓ — ACK ↓ (Command Byte)	T2	8	17	40	µs
ACK ↓ — CRDY ↓ (Command Byte)	T3	8	14	30	µs
REQ ↑ — ACK ↑ (Argument Byte)	T4	8	30	50	µs
REQ ↓ — ACK ↓ (Argument Byte)	T5	8	17	40	µs
ACK ↓ — STAT ↑ (Status Request)	T6	20	100	150	µs
ACK ↓ — STAT ↑ (No-Motion Seek)*	T6	50*	200*	300*	µs
ACK ↓ — STAT ↑ (Set Sector)	T6		47,000		µs
STAT ↑ — ACK ↑ (Status Byte)	T7	8	38	60	µs
BUS STABLE — ACK ↑ (Status Byte)	T8	4	6		µs
REQ ↑ — ACK ↓ (Status Byte)	T9	8	17	40	µs
REQ ↓ — STAT ↓ (Status Byte)	T10	8	50	100	µs
STAT ↓ — CRDY ↑ (Status Byte)	T11	−1	0	+1	µs

*For motion commands, mechanical delay times must be added.

3.6 DATA TRANSFER

3.6.1 Media Initialization (Figure 3-9)

New media or media which has had a format change must first be formatted before data can be written onto the disk. Please refer to Section 5 for format requirements.

The cylinder and track are selected in accordance with the previously mentioned procedure. At INDEX time, WRITE gate is activated and the appropriate data is written.

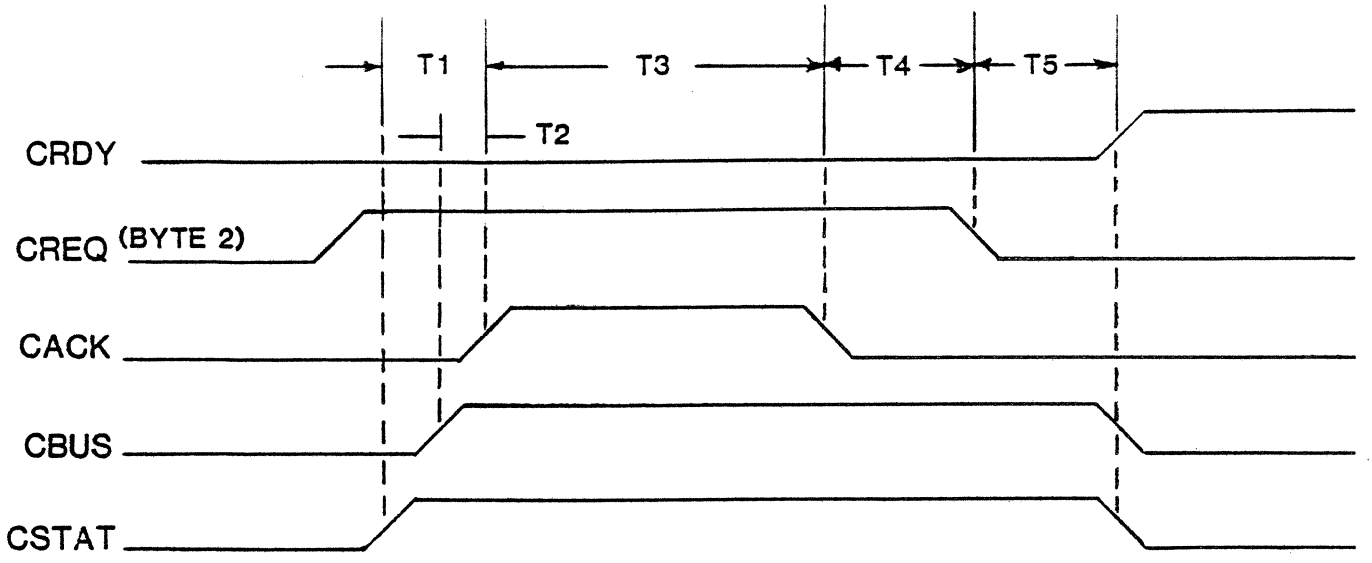


Figure 3-8. Two Byte Command Found Illegal — Timing Diagram

Table 3-10. Two Byte Command Found Illegal-Timing Transaction

TRANSACTION	TIME	MINIMUM
CSTAT ↑ — CACK ↑	T1	38 μs
CBUS ↑ — CACK ↑	T2	6 μs
CACK ↑ — CACK ↓	T3	16 μs
CACK ↓ — CREQ ↓	T4	7 μs
CREQ ↓ — CRDY ↑	T5	47 μs

3.6.2 Reading (Figures 3-10, 3-11)

A. **Non-Imbedded ID Field**

Sixteen bytes after the SECTOR pulse, READ gate is activated. Zeros appear on the NRZ data out signal until the PLL is in sync or locked. Immediately following the SYNC byte is the ID or header field. At the end of the ID field, READ gate must be deactivated for a four byte time period and reactivated. This action enables the read circuitry to reaquire lock before the SYNC byte.

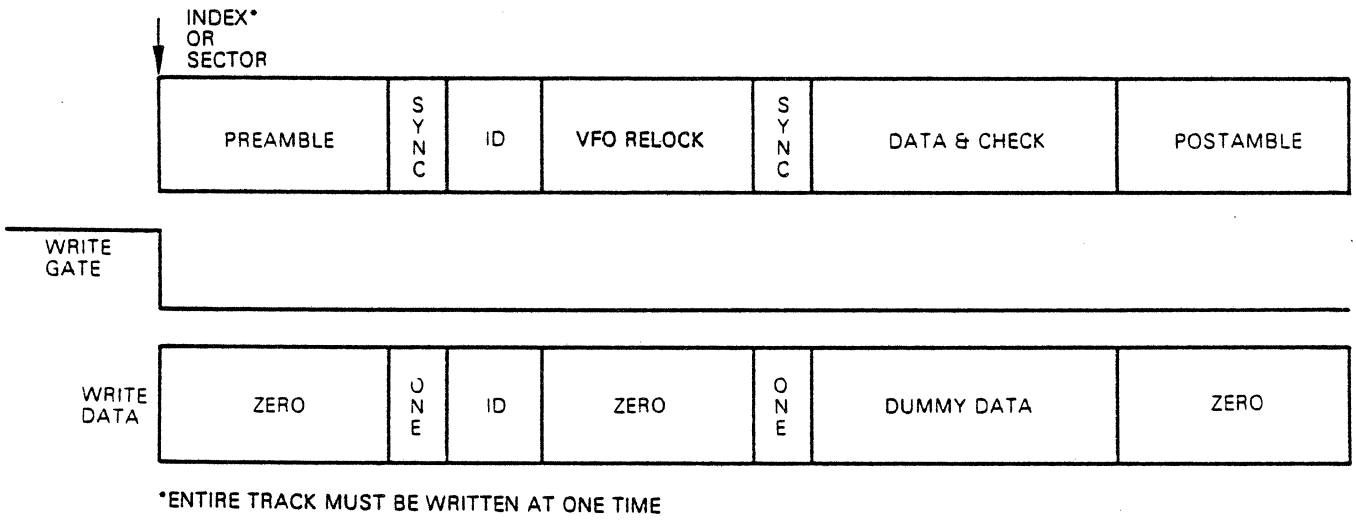


Figure 3-9. Media Initialization

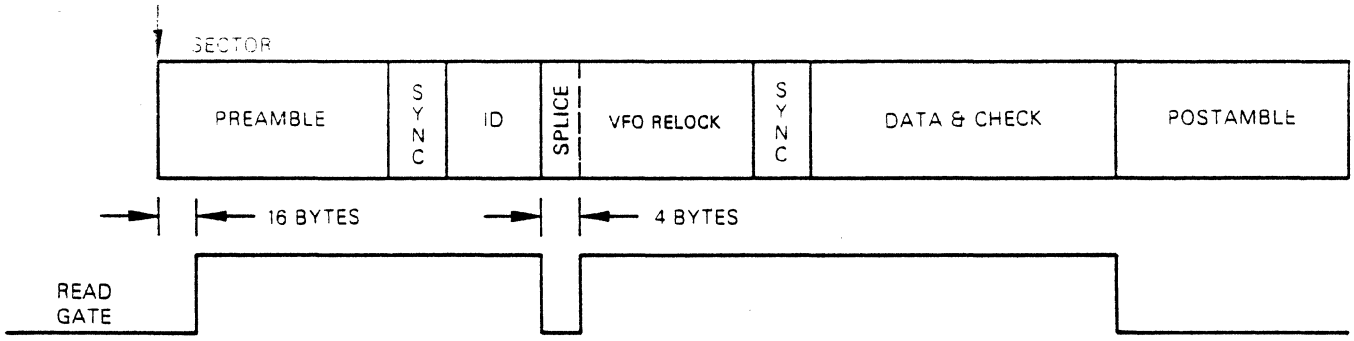


Figure 3-10. Non-Imbedded ID Field Read Timing

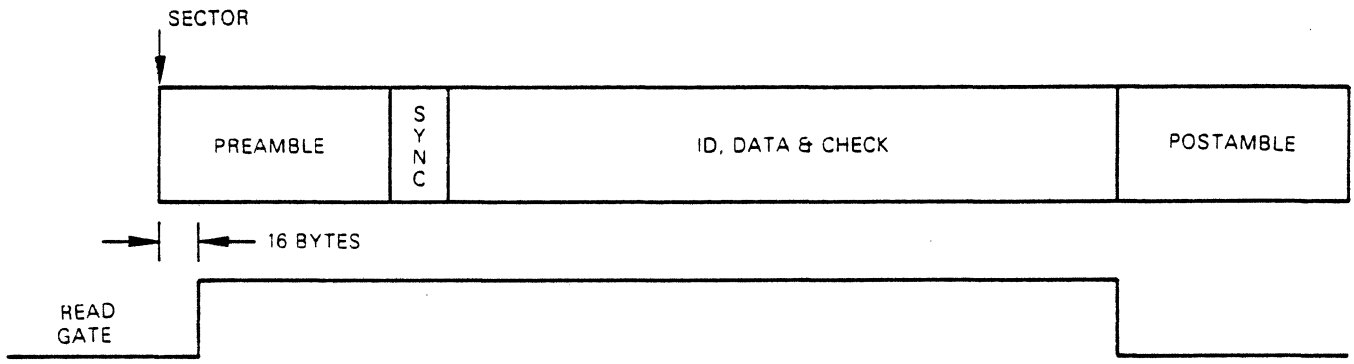


Figure 3-11. Imbedded ID Field Read Timing

B. **Imbedded ID Field**

The READ gate is activated sixteen bytes after the SECTOR or INDEX pulse and deactivated after the data field. READ gate must not be activated until at least 16 μs have passed after WRITE gate is deactivated or the head is selected.

3.6.3 Writing (Figures 3-12, 3-13)

A. **Non-Imbedded ID Field**

The READ gate must be activated sixteen bytes after the SECTOR pulse. At the end of ID field, READ gate is deactivated, WRITE gate is activated (within a maximum of 1 byte), and the appropriate data is written. WRITE gate is deactivated one byte into the postamble.

B. **Imbedded ID Field**

The WRITE gate is activated at SECTOR pulse time and deactivated one byte into the postamble.

3.6.4 Read Clock Phasing

The positive going transition of read clock should be used as the data strobe.

3.6.5 Write Clock Phasing

Since the MARKSMAN provides the write clock, the data/clock phase relationship is a function of the cable length and internal controller delays. This relationship, *measured at the disk drive*, should have the positive transition of the internal capture clock, occurring nearest the center of the NRZ data. Should this not be true, the write clock can be inverted by changing strapping between test points. Refer to the Installation and Operation Manual.

3.7 DRIVE MALFUNCTIONS & CONTROLLER ERRORS

The MARKSMAN internal logic monitors a number of conditions which, if they occur, will compromise data integrity. They are as follows:

(D) = Drive (C) = Controller

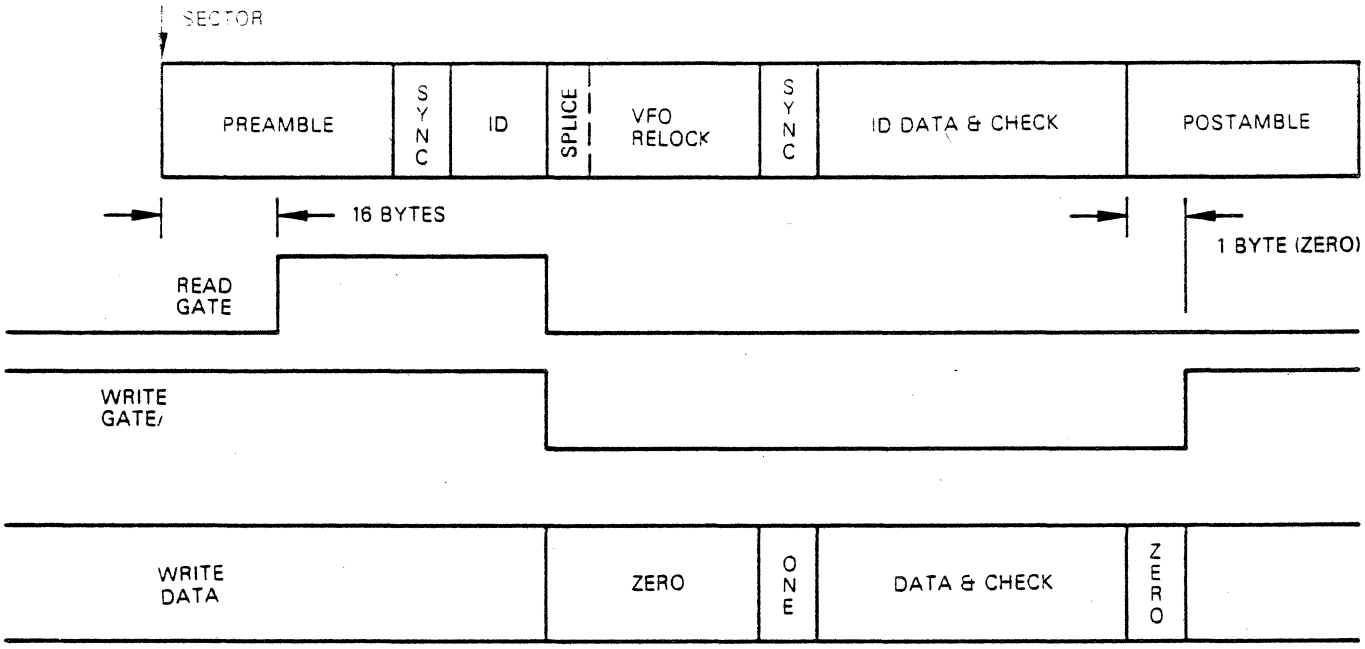


Figure 3-12. Non-Imbedded ID Field Write Timing

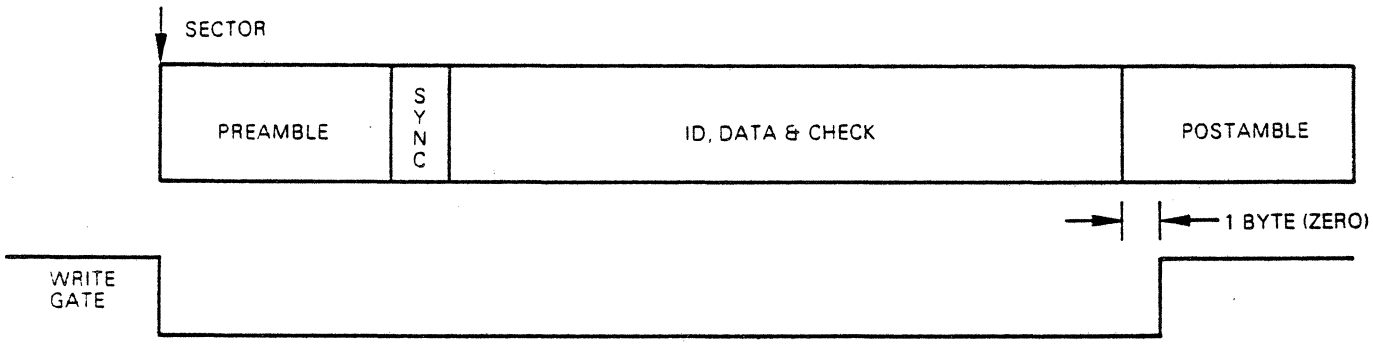


Figure 3-13. Imbedded ID Field Write Timing

Multiple Heads Selected D)
Write Unsafe (WRTUSF) signal is set. Resets when status is presented.

Write Command to Protected Head (C)
Write Unsafe (WRTUSF) signal is set. Resets when status is presented.

Power Fault (D)
Write Unsafe (WRTUSF) signal is set. Resets when status is presented.

Illegal Address Received (C & D)
Bit 2 of status word is set. Resets when status is presented.

Spin Acceleration/Deceleration Out of Limit (D)
Bit 4 of status word is set. Resets when status is read. Repeated operation when this condition exists could lead to excessive wear of the head and disk and result in data loss over a period of time.

UTH Fault (D)
A servo position fault has occurred. The drive will go not ready.

SECTION 4
SMD (ANSI) INTERFACE (M80, M160)

4.1 DISK DRIVE INTERFACE SIGNALS

Signals appearing at the MARKSMAN Disk Drive SMD (ANSI) interface and their use are shown in Tables 4-1, 4-2, 4-3, and 4.4. Refer to Section 6 for connector and pin numbers and signal levels.

Table 4-1. Radial Cable Signals

Signal Name	Mnemonic	I/O	Description
Selected	SELECTED+ SELECTED–	O	When active this line indicates the drive is selected. This line will be active within 400 nanoseconds of the leading edge of unit select tag when the four unit select bits compare with the address of the drive and the degate switch is in the normal operating position.
Seek End	SEEKEND+ SEEKEND–	O	When active this line indicates "ON CYLINDER" or SEEK ERROR (i.e., seek operation has terminated). If a cylinder address is illegal "SEEK END" and "SEEK ERROR" will interupt for 30 microseconds nominally.
Index	IDX+ IDX–	O	When active indicates the starting point of a data track. INDEX is nominally 2 microseconds wide. Timing integrity is maintained during seek operations.
Sector	SEC+ SEC–	O	When active indicates the start of a sector. The pulse is nominally 1 microsecond wide, with the leading edge occurring at the beginning of a sector.
Write Data	WRITEDATA+ WRITEDATA–	I	This line carries NRZ data to be written on the disk pack.
Servo Clock	SERVCLK+ SERVCLK–	O	This line transmits 7.68 MHz (M80), 10.24 MHz (M160) ± the percent of speed variation. Clock phase is locked to the servo dibit pattern. Servo Clock is available to the controller at all times (not gated with Select) and is used to form Write Clock.
Read Data	RDDATA+ RDDATA–	O	This line carries NRZ data recovered from the disk.
Read Clock	RDCLK+ RDCLK–	O	This line transmits 7.68 MHz (M80), 10.24 MHz (M160) clock that is phased locked to the recovered data. It is internally derived and is synchronized with the detected data.
Write Clock	WRTCLK+ WRTCLK–	I	The line is retransmitted "SERVO CLOCK".

Table 4-2. Bussed Cable Signals

Signal Name	Mneumonic	I/O	Description
Unit Ready	UNITREADY+ UNITREADY−	O	When active this line indicates that the selected drive is up to speed, and no fault condition exists.
On Cylinder	ONCYLINDER+ ONCYLINDER−	O	When active this line indicates the R/W heads are positioned on a track. ON CYLINDER goes inactive with any seek command.
Index Mark	INDEX+ INDEX−	O	When active indicates the starting point of a data track. INDEX is nominally 2 microseconds wide. Timing integrity is maintained during seek operations.
Device Select Enable	DEVSEL+ DEVSEL−	I	When active this line gates the 4 unit select lines into the logical address compare circuit.
Device Select 1, 2, 4 & 8	UNITSEL1, 2, 4 & 8+ UNITSEL1, 2, 4 & 8−	I	These four lines are binary coded to select one of 16 logical units (0-15). The unit number is selected via a set of address selector DIP switches located on the Logic Control PWB. The operator must verify that unique unit numbers are assigned to each drive on the same control bus.
Tag 1 (Set Cylinder)	TAG1+ TAG1−	I	When active the bus lines are decoded as the next cylinder address and the trailing edge of TAG 1 is the command to move the heads to the new address. TAG 1 is not to be issued if the drive is busy (not on cylinder).
Tag 2 (SETHD Tag)	TAG2+ TAG2−	I	When active, Bus Lines 0 through 3 are decoded as the next head address. Bus 0 is the LSB.
Tag 3 (Control Tag)	TAG3+ TAG3−	I	When active, bus lines are decoded as commands.
Sector Mark	SECTOR+ SECTOR−	O	When active indicates the start of a sector. The pulse is nominally 1 microsecond wide, with the leading edge occurring at the beginning of a sector.
Seek Error	SEEKERROR+ SEEKERROR−	O	When active indicates that the unit was unable to complete a servo operation within (TBD) milliseconds or that an illegal cylinder address was issued. It is reset by rezero.
Bus 0 thru Bus 9	BUS0. . . 9+ BUS0. . . 9−	I	The 10 bus lines are interpreted according to the current tag. The drive must be selected at least 200 nanoseconds before any bus lines are active. The bus lines must be active at least 200 nanoseconds before the tag line and 200 nanoseconds after the tag line. The tag lines must be active at least 800 nanoseconds.

The 10 bus lines are decoded by the three tag lines as defined below:

Table 4-3. Tag and Bus Decode

	Tag 1 (Set Cyl)	Tag 2 (Set Hd)	Tag 3 (Control Select)
Bus Bit	Cylinder Bit	HAR BIT	
0	1	1	Write Gate
1	2	2	Read Gate
2	4	4	
3	8		
4	16		Fault Clear
5	32		
6	64		Return to Zero
7	128		
8	256		
9	512		

There shall only be one tag line active at any given time. There shall be at least a 1.0 microsecond delay after the trailing edge of a tag signal before the leading edge of another tag.

4.2 TAG 3 (CONTROL TAG) INTERPRETATIONS

4.2.1 Bus 0 — Write Gate

This bit turns on the write circuits.

4.2.2 Bus 1 — Read Gate

This bit turns on the Read circuits. The leading edge of Read Gate instructs the data separator to synchronize on a previously written all zeros pattern in a gap.

4.2.3 Bus 2 — Servo Offset Forward

This bit will position the R/W heads off-track towards the spindle.

Table 4-4. Interface Signals

Signal Name	Mnemonic	I/O	Description
Fault	FAULT+ FAULT–	O	When active, this line indicates that at least one of the following error conditions is active in the drive. a. Read or write and not on cylinder b. Write with offset active c. Writing with more than 1 head selected or no transitions detected d. Write with heads off track e. Write Gate and Read Gate active simultaneously f. DC voltages unsafe g. Excessive servo temperature h. Read or write and not ready
Address Mark Found	AMDET+ AMDET–	O	This line is maintained unasserted — Address Marks are not used on this machine.
Interface Enable	CABLEIN+ CABLEIN–	I	When open or inactive indicates an open bussed interface cable or loss of controller power: Drive receivers and the transmitters are inhibited and the drive will sequence down.
Pick	PICK/	I	The PICK signal is normally used to start one drive at a time when several drives are daisy chained together. But since the M160 spindle motor is controlled only by the application of AC power, the PICK signal is ignored. The M160 does not propagate PICK while its motor is spinning up to speed.
Power Sequence Hold	HOLD/	I	The HOLD signal is normally maintained active low. It should be taken inactive high at least 1 second prior to turning off AC power to allow the heads to return to the landing zone.
Sequence Disable	SEQDIS/	O	Sequence Disable is held low while the motor is spinning up to speed. This is the same physical line as HOLD/ and is a jumper selected option.

4.2.4 Bus 3 — Servo Offset Reverse

This bit will position the R/W heads off-track away from the spindle.

4.2.5 Bus 4 — Fault Clear

This bit will reset the following fault conditions in the drive provided the condition is not currently active. A 100 nanosecond minimum pulse is required.

a) Not ready and read or write.
b) Write and not on cylinder.
c) Offset and write.
d) Write and no DC write current.
e) Write and no write data transitions.
f) Write and read only active.
g) Illegal head address, multiple heads selected or no head selected when the drive is ready.

4.2.6 Bus 5 — Reserved

4.2.7 Bus 6 — Return to Zero (RTZ)

This bit will reposition the heads to cylinder zero if the heads are loaded on the disk. Rezero will reset: 1) "Seek incomplete," 2) an illegal cylinder address. A 100 nanosecond minimum pulse is required.

4.2.8 Bus 7 — Reserved

4.2.9 Bus 8 — Reserved

4.2.10 Bus 9 — Reserved

4.3 INTERFACE DESCRIPTION

The M80 and M160 disk drive SMD interface characteristics may be divided into six areas:

Power Sequencing
Positioning
Data Handling
Error Correction
Fault Indication
Recovery Times

4.3.1 Power Sequencing

Figure 4-1 illustrates the power sequence.

Applying AC power will cause the drive to sequence up. PICK is not propagated while the drive is coming up to speed. The heads will be returned to the landing zone if HOLD is dropped at least one second prior to removing AC power.

4.3.2 Positioning

The positioning logic moves the heads to the desired cylinder and selects the proper track. The sequence is illustrated in Figure 4-2. During the time that the actuator is moving, the ON CYLINDER signal goes inactive. At the end of a seek, ON CYLINDER becomes true and SEEK END is set. SEEK END is then reset by the next seek command.

If the seek is not finished within (TBD) milliseconds, the SEEK ERROR flag is set. If an illegal cylinder address is given SEEK ERROR status is set. If either of these conditions occur, a Rezero command must be given to clear the fault and re-establish a reference point.

4.3.3 Data Handling

Before writing on a new pack, the pack must be formatted. A format from Section 5 must be selected and the sector size decided upon. Figures 4-3 and 4-4 illustrate this procedure. Figures 4-5 through 4-8 illustrate reading and writing.

4.3.4 Faults

The following illegal conditions will cause a fault:

Writing while not ready

Writing and off track for any reason

Writing and no heads or multiple heads selected

Writing and no current transitions detected

Writing and ready only active

Write current and not writing

DC voltages unsafe

Servo over temperature

If error condition is no longer present, the fault may be reset by: Fault Reset (Tag 3 and Bus 4) or a Unit Resequence.

4.3.5 Recovery Times

a) Drive must be ready, and HAR not changed at least 10 microseconds before read and 5 microseconds before write.

b) Switching from write to read a 10 microsecond delay is required.

c) Switching from not reading to reading, good data will be at the interface within 5 microseconds.

d) Switching from not writing or reading to writing, good data will be written within 1 microsecond.

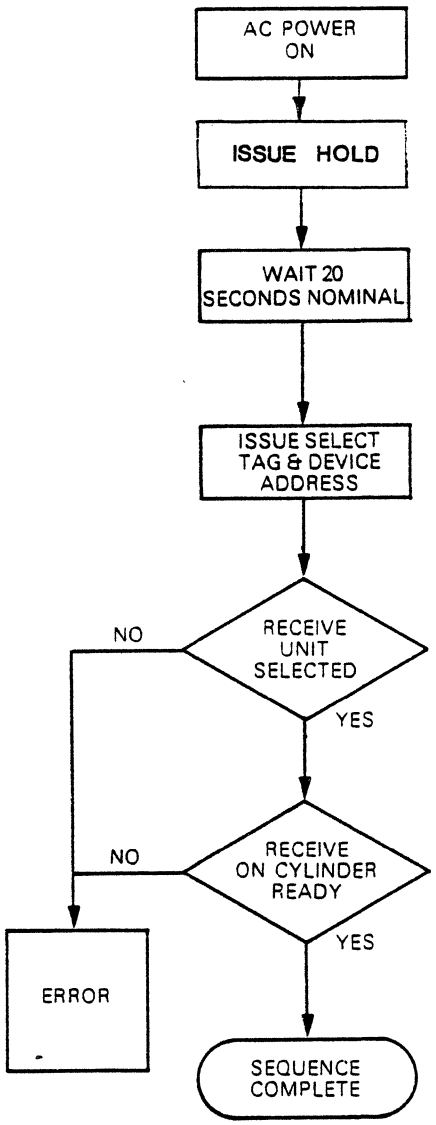


Figure 4-1. Power Sequence

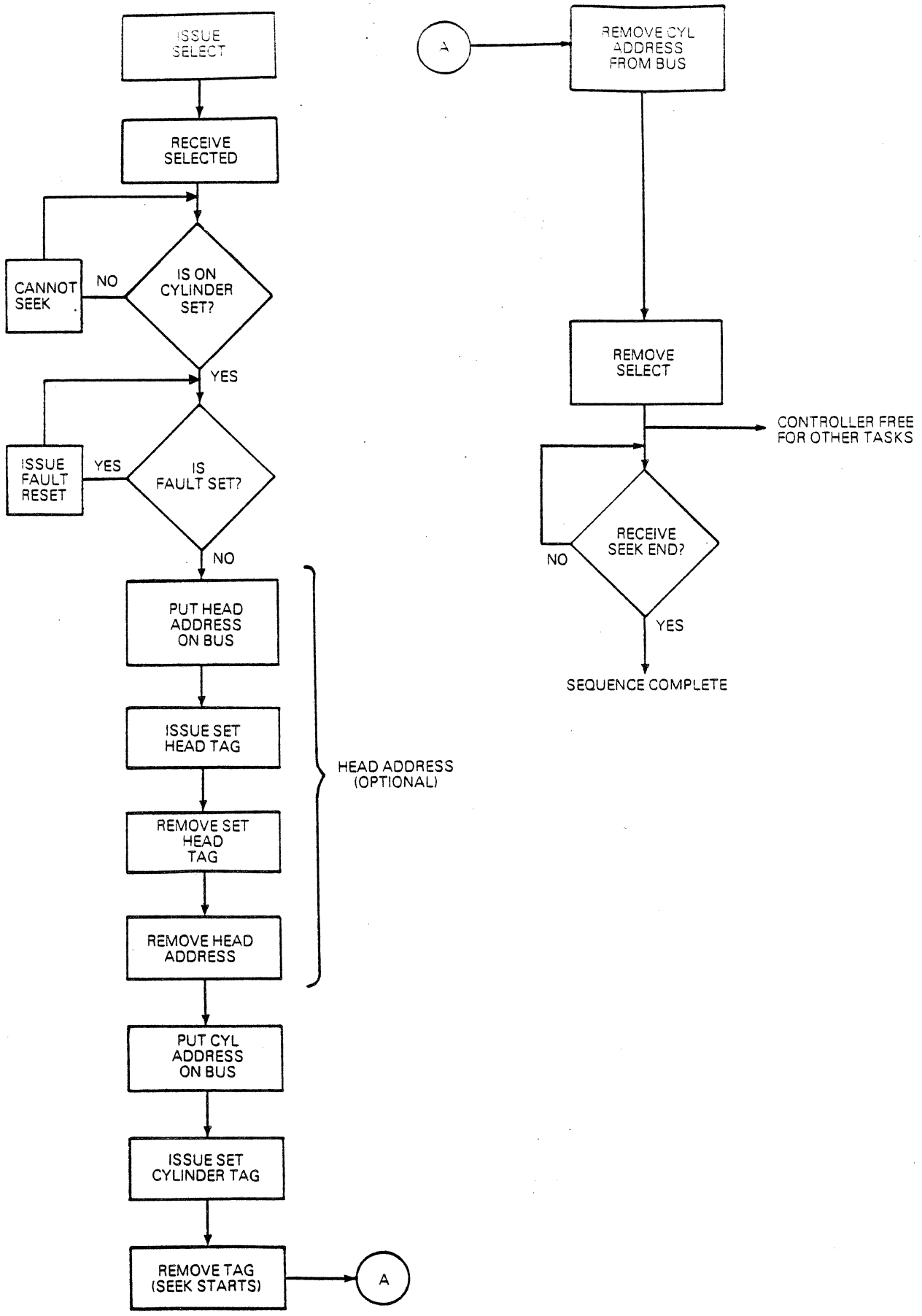


Figure 4-2. Seek Sequence

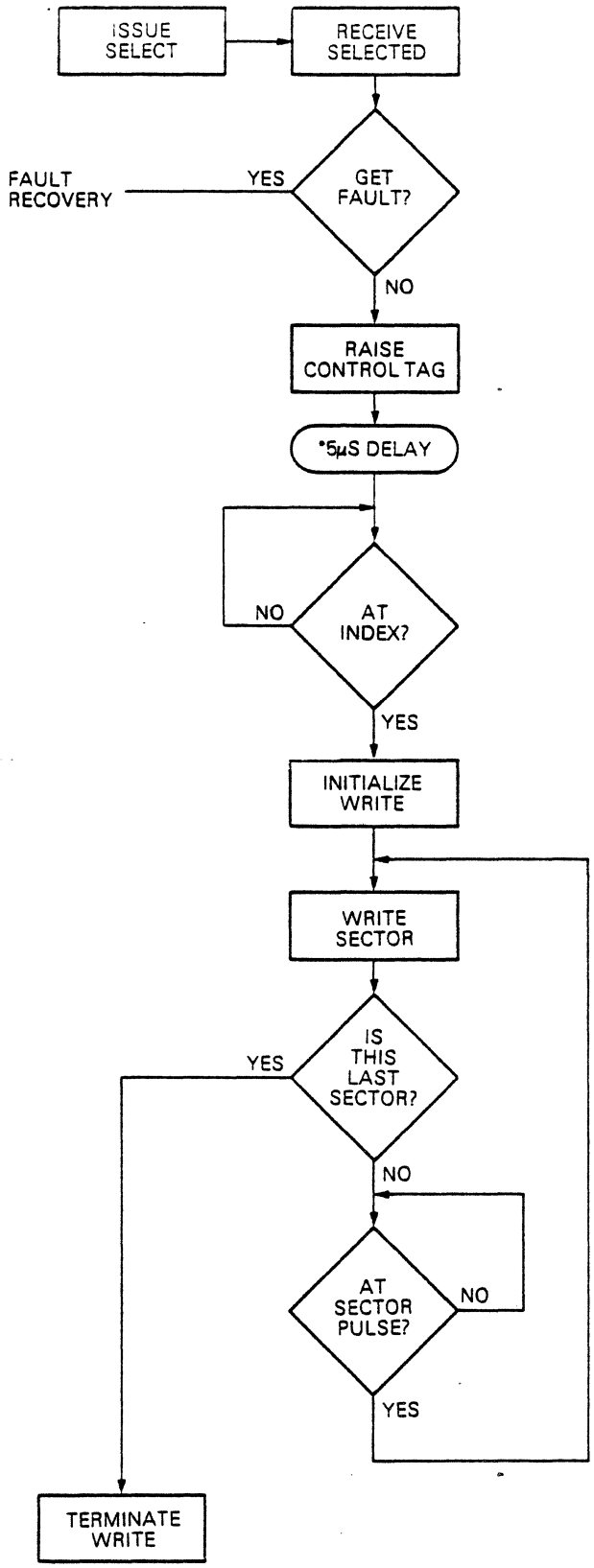


Figure 4-3. Track Initialization

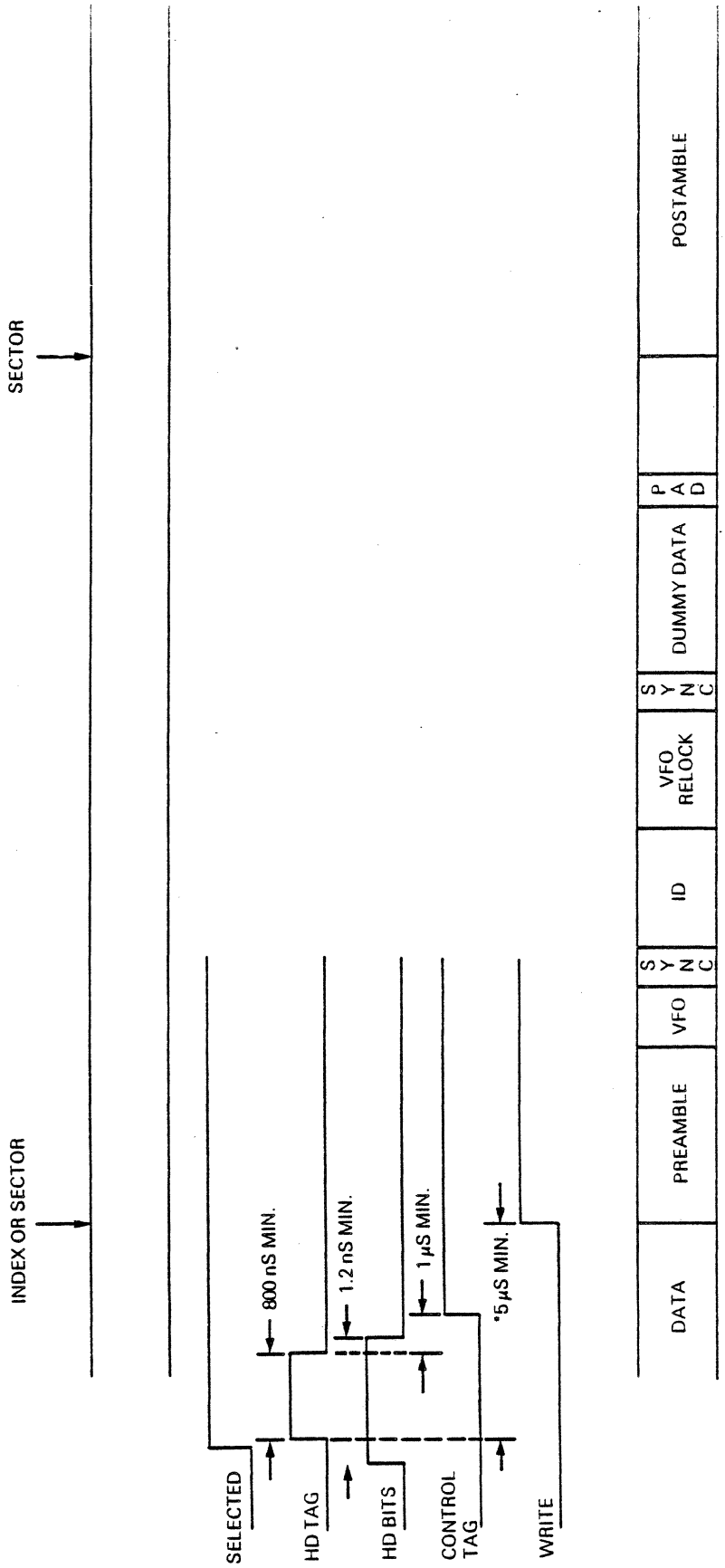


Figure 4-4. Initializing for Electronic Sectoring (Format II)

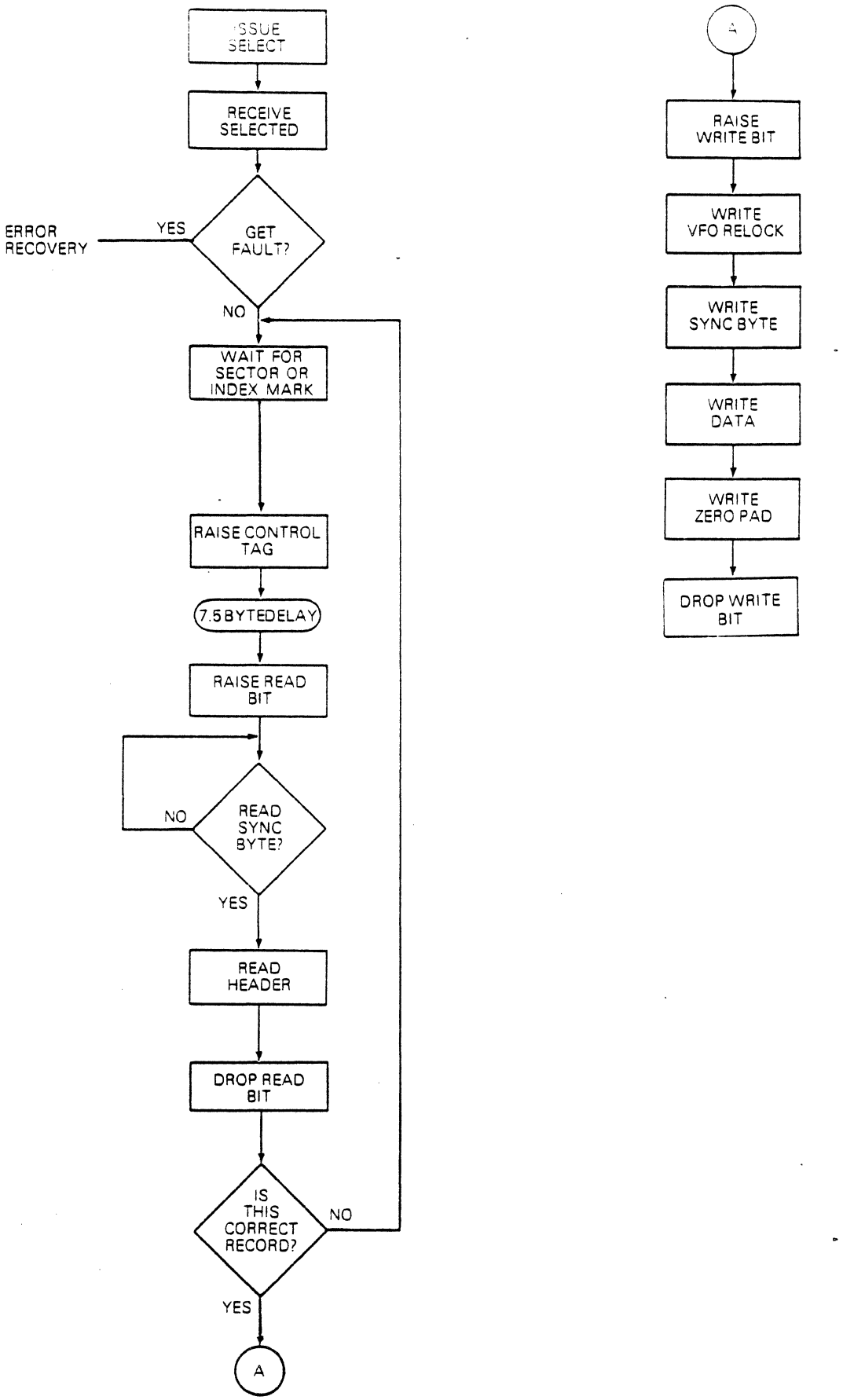


Figure 4-5. Write Using Electronic Sectoring

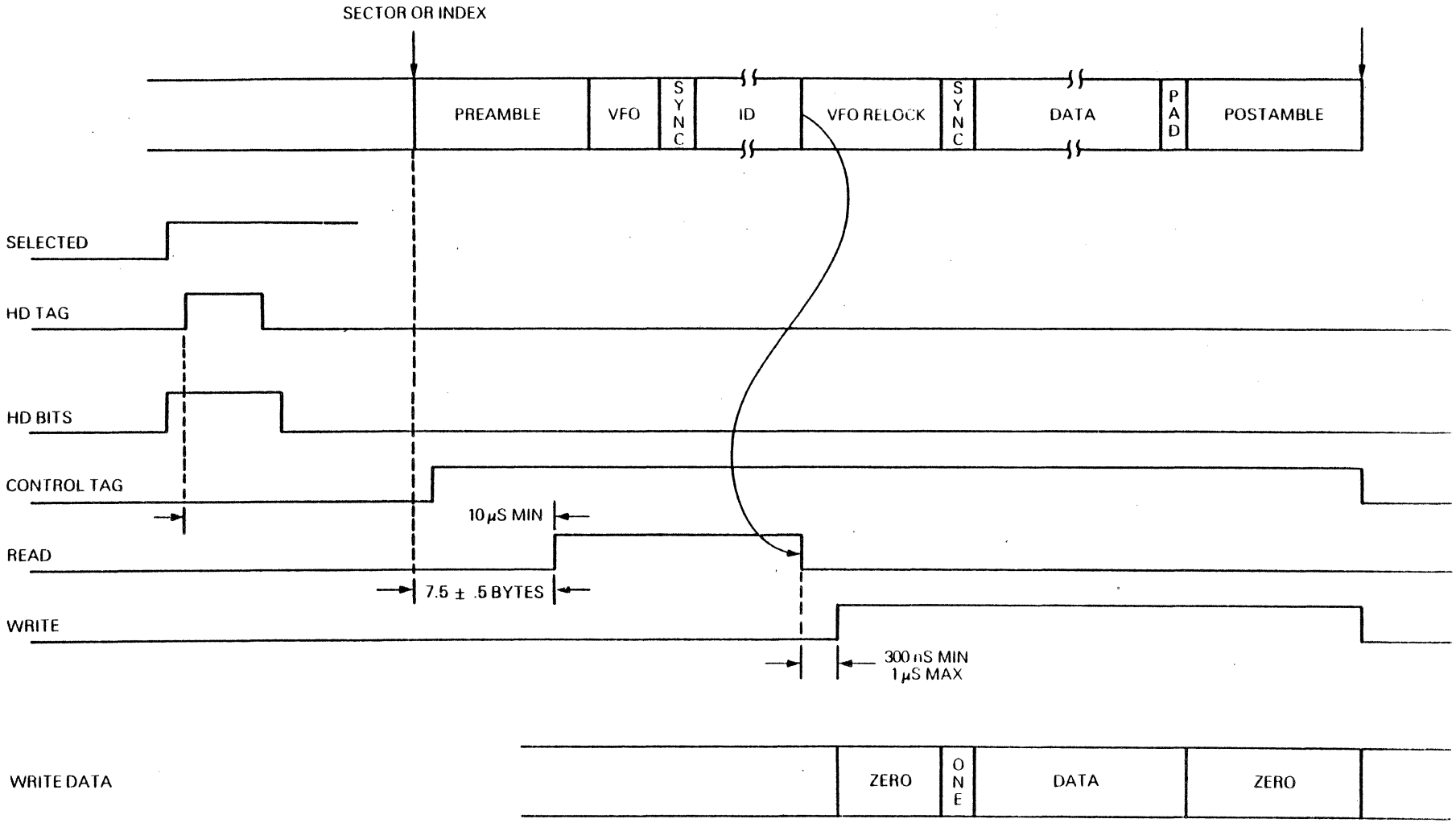


Figure 4-6. Write Using Electronic Sectoring (Format II)

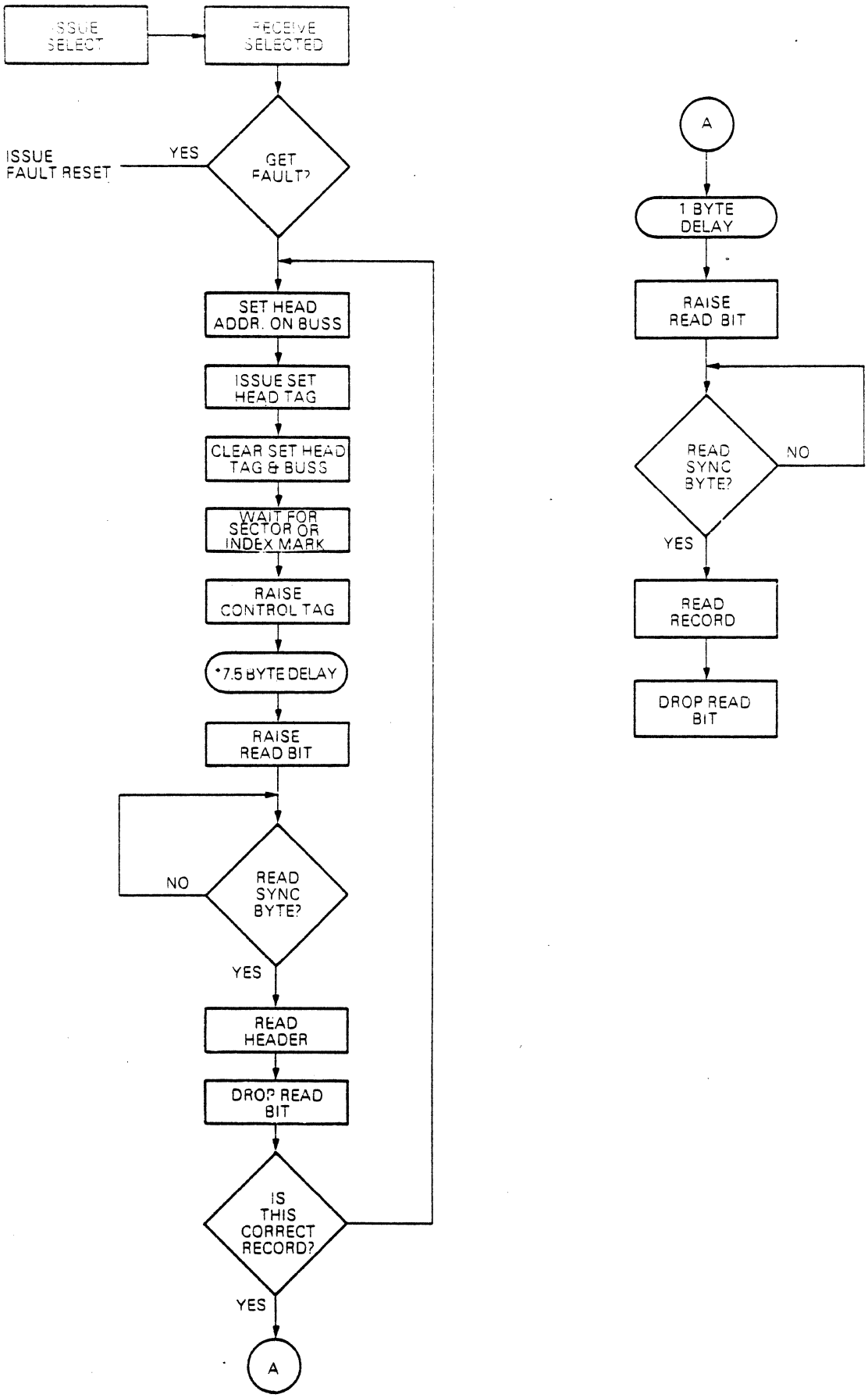


Figure 4-7. Read Using Electronic Sectoring

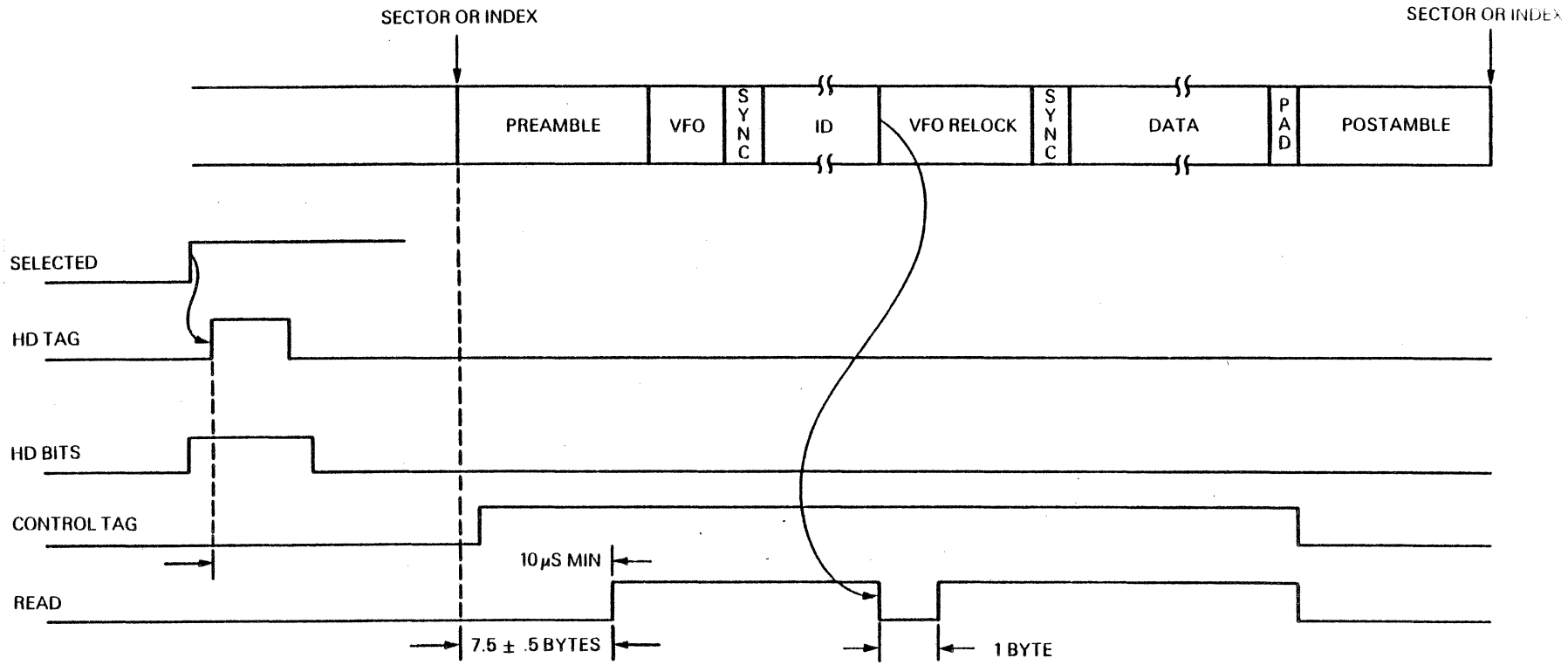


Figure 4-8. Read Using Electronic Sectoring (Format II)

SECTION 5
FORMAT REQUIREMENTS

5.1 GENERAL

In order to guarantee operations over the entire temperature range, allow for component tolerances and compensate for cable and controller delays, all disk drives must have a preamble and postamble attached to each sector. The amount of overhead is a function of the electrical and mechanical tolerances and the bit transfer rate as well as the system requirements. The preamble and postamble contain all ZEROS. The SYNC byte, should be a minimum of 1 byte.

5.2 FORMAT DEFINITIONS

Three different formats have been suggested for MARKSMAN. They are illustrated in Figure 5-1. Format I requires the least amount of overhead. Format II is similar, but separates the header (ID) field from the data, allowing the data to be updated without rewriting the header. They are both designed for sequential operation, however, with format II, it is possible to miss the succeeding sector when a head advanced command is issued or may receive a sector or index mark prior to completion of read or write. Should this be undesirable, Formats I and III have a larger postamble to insure that after a head advanced command is issued the succeeding sector is not missed, and that read or write is completed before receiving a sector or index mark.

Note

The M80 and M160 'overhead field' is reduced by 20 bytes due to the positioning accuracy of INDEX.

5.3 SECTOR CALCULATIONS

The following formulas are used to calculate the number of sectors for any given sector size. Formula A is used with Models M20, M40, and M80. Formula B is for Model M160.

I

PREAMBLE		SYNC	ID DATA & CHECK	POSTAMBLE	
M20/M40	39	1	VAR	19	BYTES
M80/M160	19	1	VAR	19	BYTES

II

PREAMBLE		SYNC	ID	SPLICE	VFO RELOCK	SYNC	DATA & CHECK	POST AMBLE	
M20/M40	39	1	VAR		15	1	VAR	4	BYTES
M80/M160	19	1	VAR		15	1	VAR	4	BYTES

III

PREAMBLE		SYNC	ID	SPLICE	VFO RELOCK	SYNC	DATA & CHECK	POSTAMBLE	
M20/M40	39	1	VAR		15	1	VAR	19	BYTES
M80/M160	19	1	VAR		15	1	VAR	19	BYTES

Figure 5-1. Sector Formats

$$N = INT\left(\frac{24000}{DATA + ID + OH}\right) \quad (A)$$

$$N = INT\left(\frac{32000}{DATA + ID + OH}\right) \quad (B)$$

WHERE: INT (Number) - Greatest (whole number) Integer Contained Within Number

N = number of sectors
Data = length of data field plus check characters
ID = length of header
OH = Length of overhead field
= Format I = 59 (M20, M40); 39 (M80, M160)
= Format II = 60 (M20, M40); 40 (M80, M160)
= Format III = 75 (M20, M40); 55 (M80, M160)

Whenever it is necessary to change heads at the end of a track and continue operation without losing a revolution, an end-of-track pad, which accommodates the command execution and head switching, must be provided. (Refer to paragraph 3.3.4.)

Tables 5-1 and 5-2 show the number of sectors per track and net capacity, respectively, for the M20. Double the capacity for the M40. For the M80, refer to Tables 5-3 and 5-4 and for the M160 use Tables 5-5 and 5-6.

Table 5-1. Number of Sectors Per Track

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	119	119	111
256 Bytes	72	72	69
512 Bytes	41	41	40
1024 Bytes	21	21	21

Assuming an 8 byte ID field and a 5 byte check character.

Table 5-2. Net Capacity (20 Megabytes)

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	12.79	12.79	11.93
256 Bytes	15.48	15.48	14.84
512 Bytes	17.63	17.63	17.20
1024 Bytes	18.06	18.06	18.06

Table 5-3. Number of Sectors Per Track (M80)

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	133	132	122
256 Bytes	77	77	74
512 Bytes	42	42	41
1024 Bytes	22	22	21

Table 5-4. Net Capacity Megabytes (M80)

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	57.20	56.77	52.46
256 Bytes	66.23	66.23	63.65
512 Bytes	72.25	72.25	70.53
1024 Bytes	75.69	75.69	72.25

Table 5-5. Number of Sectors Per Track (M160)

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	177	177	163
256 Bytes	103	103	98
512 Bytes	56	56	55
1024 Bytes	29	29	29

Table 5-6. Net Capacity Megabytes (M160)

Sector Size (Data Field)	Format		
	I	II	III
128 Bytes	113.77	113.77	104.77
256 Bytes	132.42	132.42	125.99
512 Bytes	143.99	143.99	141.41
1024 Bytes	149.13	149.13	149.13

5.4 SECTOR SELECTION

The Sector Length switches (described in Section 7) determine the number of sector pulses that occur without the use of the SET SECTOR command. The number of sectors per track selected assumes data format III is being used. Switches are set for the size data field required.

SECTION 6
SIGNAL LEVELS

6.1 CDS INTERFACE

The M20/M40 uses different logic elements than the M80/M160 although the interface functions the same for all models.

6.1.1 CBUS 0-7, CREQ, CACK (M20/M40)

These signals interface directly to the Motorola MC6821 Peripheral Interface Adaptor (PIA).

Electrical Characteristics (Table 6-1) (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted)

6.1.2. All Other Interface Signals (M20/40)

All other signals interface to 74LSXXX Logic. Refer to the IC manufacturer's literature for drive capability. Table 6-2 shows cable pin numbers and IC's used.

6.1.3 M80/M160 Interface Signals

Table 6-3 shows the interface signals, cable pin numbers, and IC used as a source or load.

6.1.4 Cable Length

The drive control board is supplied with a 4.0 inch interface cable. The controller logic must be placed in close proximity to this cable. If additional cable length is required, the Driver/Receiver Option described in Appendix A or equivalent must be used.

6.1.5 Read/Write Data, Clock Driver/Receiver

Figure 6-1 shows the recommended driver/receiver configuration for the Read/Write Data and Clock lines.

Table 6-1. Electrical Characteristics

Characteristics		Symbol	Min	Typ	Max	Unit
Input Leakage Current CRQ (V_{in} = 0 to 5.25 Vdc)		I_{in}	–	1.0	2.5	Adc
Input High Current (V_{IH} = 2.4 Vdc)	CBUS0-7 CACK	I_{IH}	−200	−400	–	Adc
Input Low Current (V_{IL} = 0.4 Vdc)	CACK	I_{IL}	–	1.3	−2.4	mAdc
Output High Voltage (I_{load} = −200 μ Adc) (I_{load} = −10 μ Adc)	CBUS0-7 CACK	V_{OH}	V_{SS} +2.4 V_{CC} −1.0	– –	– –	Vdc
Output Low Voltage (I_{load} = 3.2 MAdc)		V_{OL}	–	0	V_{SS} +0.4	Vdc
Capacitance (V_{in} = 0, T_A = 25° C, F = 1.0 MHz		C_{in}	–	–	10	pF

Table 6-2. M20/M40 CDS Interface

SIGNAL	CABLE PIN #	ACTIVE H/L	SOURCE	LOAD	COMMENTS
CACK	J1-01	H	MC6821		Acknowledge Signal to User
RST/	J1-02	L		74LS08	Reset from User
CBUSO	J1-03	H	MC6821	MC6821	Bidirectional Data Line
CBUS1	J1-04	H	MC6821	MC6821	Bidirectional Data Line
SPARE	J1-05				
CREQ	J1-06	H		MC6821	Request from User
GRD	J1-07				
CBUS2	J1-08	H	MC6821	MC6821	Bidirectional Data Line
CBUS6	J1-09	H	MC6821	MC6821	Bidirectional Data Line
CBUS7	J1-10	H	MC6821	MC6821	Bidirectional Data Line
CBUS5	J1-11	H	MC6821	MC6821	Bidirectional Data Line
CBUS3	J1-12	H	MC6821	MC6821	Bidirectional Data Line
SPARE	J1-13				
IDX	J1-14	H	74LS74		Index Pulse to User
GRD	J1-15				
DRDY	J1-16	H	74LS175		Drive Ready to User
CRDY	J1-17	H	74LS175		Control Ready to User
GRD	J1-18				
1MHZ	J1-19	CLOCK	74LS04		MPU Clock to User
GRD	J1-20				
SEC	J1-21	H	74LS04		Sector Pulse to User
GRD	J1-22				
CSTAT	J1-23	H	74LS175		Control Status to User
GRD	J1-24				
WRTCLK	J1-25	CLOCK	74LS132		Write Clock to User
GRD	J1-26				
NRZIN	J1-27	H		74S74	NRZ Data from User
GRD	J1-28				
RDCLK	J1-29	CLOCK	74S08		Read Clock to User
GRD	J1-30				
NRZOUT	J1-31	H	74S37		NRZ Data to User
GRD	J1-32				
WRTGATE/	J1-33	L		7414	Write Gate from User
GRD	J1-34				
RDGATE	J1-35	H		74S00	Read Gate from User
SPARE	J1-36				
SPARE	J1-37				
SPARE	J1-38				
WRTSUSF	J1-39	H	74S74		Write Unsafe to User
CBUS4	J1-40	H	MC6821	MC6821	Bidirectional Data Line

Table 6-3. M80/M160 CDS Interface

SIGNAL	CABLE PIN #	ACTIVE H/L	SOURCE	LOAD	COMMENTS
/CACK/	J3-01	H	74LS244		Acknowledge Signal to User
/NRST/	J3-02	L		74LS244	Reset from User
CD00	J3-03	H	74LS374	74LS374	Bidirectional Data Line
CD01	J3-04	H	74LS374	74LS374	Bidirectional Data Line
SPARE	J3-05				
/CREQ/	J3-06	H		74LS244	Request from User
GROUND	J3-07				
CD02	J3-08	H	74LS374	74LS374	Bidirectional Data Line
CD06	J3-09	H	74LS374	74LS374	Bidirectional Data Line
CD07	J3-10	H	74LS374	74LS374	Bidirectional Data Line
CD05	J3-11	H	74LS374	47LS374	Bidirectional Data Line
CD03	J3-12	H	74LS374	74LS374	Bidirectional Data Line
SPARE	J3-13				
/IDX/	J3-14	H	74LS244		Index Pulse to User
GROUND	J3-15				
/DRDY/	J3-16	H	74LS244		Drive Ready to User
/CRDY/	J3-17	H	74LS244		Control Ready to User
GROUND	J3-18				
/IMHZ/	J3-19	CLOCK	74LS244		MPU Clock to User
GROUND	J3-20				
/SEC/	J3-21	H	74LS244		Sector Pulse to User
GROUND	J3-22				
/CSTAT/	J3-23	H	74LS244		Control Status to User
GROUND	J3-24				
/WRTCLK/	J3-25	H	8304B		Write Clock to User
GROUND	J3-26				
/NRZIN/	J3-27	H		8304B	NRZ Data from User
GROUND	J3-28				
/RDCLK/	J3-29	H	8304B		NRZ Data to User
GROUND	J3-30				
/NRZOUT/	J3-31	H	8304B		NRZ Data to User
GROUND	J3-32				
/NWRTGATEIN/	J3-33	L		8304B	Write Gate from User
GROUND	J3-34				
/RDGATEIN/	J3-35	H		8304B	Read Gate from User
SPARE	J3-36				
NRZ/MILLER	J3-37	H			NRZ or Miller Data Switch
SPARE	J3-38				
/WRTUNF/	J3-39	H	74LS244		Write Unsafe to User
CD04	J3-40	H		74LS374	Bidirectional Data Line

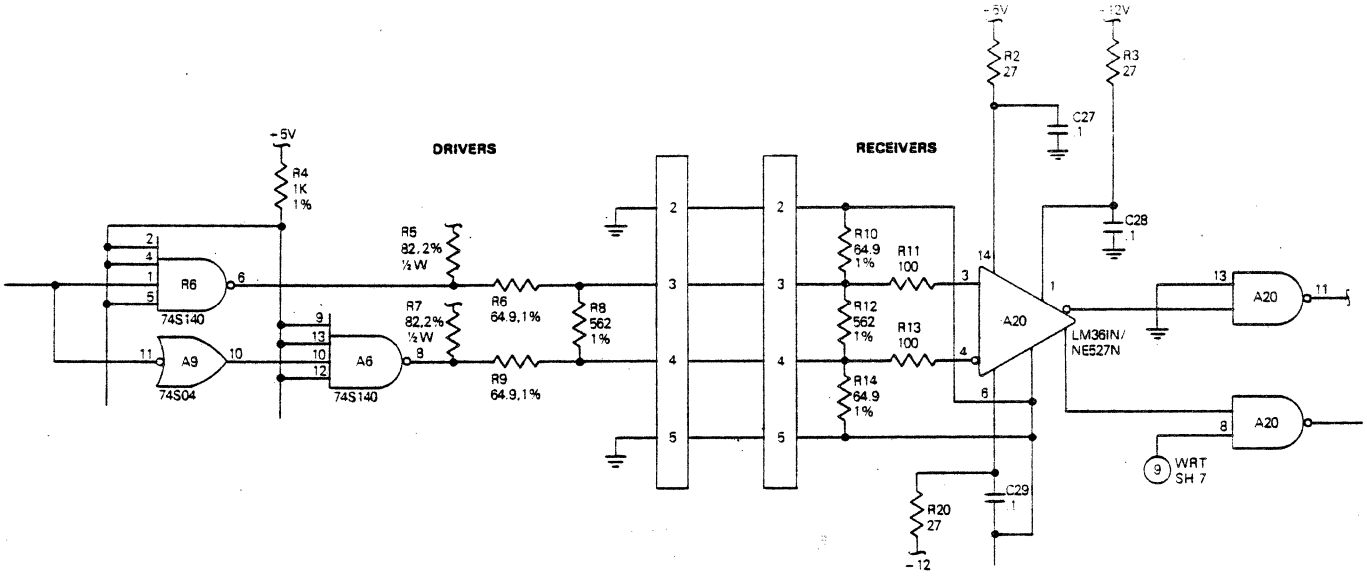


Figure 6-1. Recommended Read/Write Data, Clock Driver/Receiver and Terminator

6.2 SMD INTERFACE (M80/M160)

6.2.1 Radial or Data Cable (Table 6-5)

Type	26 Conductor, flat cable with ground plane and drain wire
Part Numbers	CDS 19706-026 3M 3476/26 BRAND-REX TC1033/26
Wire Size	No. 28 AWG, 7 strand
Impedance	130 OHM, ±15Ω
Termination	82 OHMS ±5% (See Figure 6-1)
High Level	OV (Ground)
Low Level	−0.62V Max., −0.26V Min. (includes Max. line loss)
Logical States	P Line High: M Line Low — Logical 1 P Line Low; M Line High — Logical 0
Maximum Cable Length	50 Ft.

6.2.2 Bussed or Signal Cable (Table 6-4)

Type	60 Conductor, Flat Cable
Part Number	CDS 19153-060 3M 3365/60 BRAND-REX TC1008/60
Wire Size	28 AWG, 7 Strands
Impedance	105 OHMS, ±10%
Termination	56 OHMS (See Figure 6-2)
High Level	OV (Ground)
Low Level	−0.40V Max., −0.26V Min. at Receiver input (includes Max. Line loss)
Logical States	P Line High; M Line Low — Logic 1 P Line Low; M Line High — Logicl 0
Maximum Cable Length	100 Ft. Cumulative (All drives on the BUS)

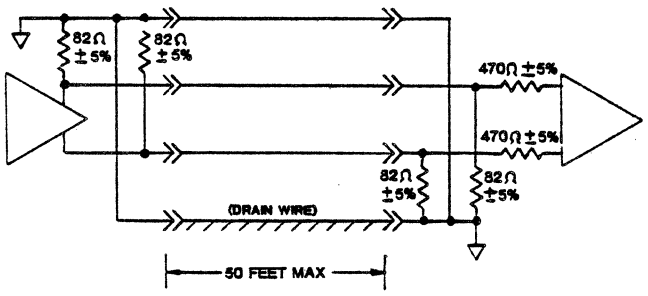


Figure 6-2. Recommended Driver/Receiver Cable Termination Circuit for Read/Write Data and Clock

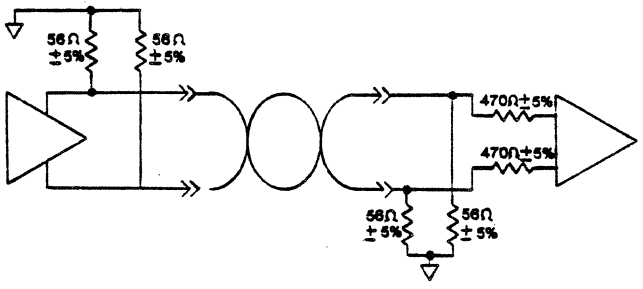


Figure 6-3. Bussed (Signal) Cable Recommended Driver/Receiver Cable Termination Circuit

6.2.3 Recommended Line Receivers and Drivers

Line Receivers: (Ref. Fig. 6.1 and 6.2)	Signetics	SN75107A
	Signetics	SN75108A
	National	
Line Driver: (Ref. Fig. 6.1 and 6.2)	Texas Inst.	SN75110J
	Fairchild	SN75110J

6.2.4 Mating Connectors

Bussed (Signal) Connector Flat Cable	CDS 17266-160
	3M 3334-6000
Radial (Data) Connector Flat Cable	CDS 17266-126
	3M 3399-6000

6.3 MATING POWER CONNECTORS

Mating connectors for both ac and dc power connectors are shown in Tables 6-6 and 6-7.

Note

The terminator goes in J22 & J23 if used, if not, these jacks are not used.

Table 6-4. Bus Interface Connector and Pins

CDS Pin Numbers J1/J17		ANSI Pin Assignments		Signal Name	Source
Active Low	Active High	Active Low	Active High		
		22	52	DEVICE SELECT ENABLE	CONTROLLER
1	2	1	31	TAG 1 (SET CYLINDER)	CONTROLLER
3	4	2	32	TAG 2 (SETHDTAG)	CONTROLLER
5	6	3	33	TAG 3 (CONTROL TAG)	CONTROLLER
7	8	4	34	BUS BIT 0	CONTROLLER
9	10	5	35	BUS BIT 1	CONTROLLER
11	12	6	36	BUS BIT 2	CONTROLLER
13	14	7	37	BUS BIT 3	CONTROLLER
15	16	8	38	BUS BIT 4	CONTROLLER
17	18	9	39	BUS BIT 5	CONTROLLER
19	20	10	40	BUS BIT 6	CONTROLLER
21	22	11	41	BUS BIT 7	CONTROLLER
23	24	12	42	BUS BIT 8	CONTROLLER
25	26	13	43	BUS BIT 9	CONTROLLER
45	46	23	53	UNIT SELECT 1	CONTROLLER
47	48	24	54	UNIT SELECT 2	CONTROLLER
51	52	26	56	UNIT SELECT 4	CONTROLLER
53	54	27	57	UNIT SELECT 8	CONTROLLER
35	36	18	48	INDEX	DRIVE
49	50	25	55	SECTOR	DRIVE
29	30	15	45	FAULT	DRIVE
31	32	16	46	SEEK ERROR	DRIVE
33	34	17	47	ON CYLINDER	DRIVE
27	28	14	44	INTERFACE ENABLE	CONTROLLER
37	38	19	49	UNIT READY	DRIVE
39	40	20	50	RESERVED	DRIVE
55	56	28	58	WRITE PROTECTED	DRIVE
	57		29	POWER SEQUENCE PICK	CONTROLLER
	58		59	POWER SEQUENCE HOLD OR SEQUENCE DISABLE	CONTROLLER OR DRIVE
59	60	30	60	RPS	
41	42	21	51		DRIVE

Table 6-5. Radial Cable Connector and Pins

CDS		Pin Number (J20)		ANSI	
Active Low	Active High	Active Low	Active High	Signal Name	Source
15	14	8	20	WRITE DATA	CONTROLLER
3	2	2	14	SERVO CLOCK	DRIVE
5	6	3	16	READ DATA	DRIVE
9	8	5	17	READ CLOCK	DRIVE
11	12	6	19	WRITE CLOCK	CONTROLLER
19	20	10	23	SEEK END	DRIVE
18	17	22	9	UNIT SELECTED	DRIVE
23	22	12	24	INDEX	DRIVE
25	26	13	26	SECTOR	DRIVE
	1		7		
	4		18		
	7		1		
	10		15	GROUND	
	13		4		
	16		21		
	21		11		
	24		25		

Table 6-6. AC Mating Connectors

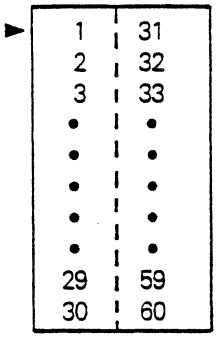
UNIT	CDS PART NUMBER				MOLEX PART NUMBER			
	CONNECTOR	QTY	PINS	QTY	CONNECTOR	QTY	PINS	QTY
Basic Drive Without Enclosure	13954-004	1	90441-002	4	19-04-1091	1	02-09-1119	4
Basic Drive With Enclosure (125V)	19224-001 (Cable Set) NEMA 5-15P	1	N/A		N/A		N/A/	
Basic Drive With Enclosure (250V)	19229-001 (Cable Set) NEMA 6-15P	1	N/A		N/A		N/A	

Table 6-7. DC Mating Connectors

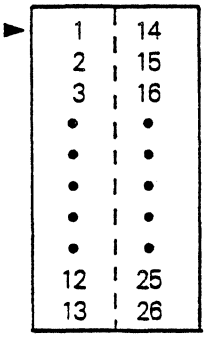
TYPE	CDS PART NUMBER				MOLEX PART NUMBER			
	CONNECTOR	QTY	PINS	QTY	CONNECTOR	QTY	PINS	QTY
5 PIN	22386-005	1	19690-001	5	09-50-3051	1	08-50-0106	5
6 PIN	22386-006	1	19690-001	6	09-50-3061	1	08-50-0106	6
8 PIN	22386-008	1	19690-001	8	09-50-3081	1	08-50-0106	8
9 PIN	90606-009	1	90441-002	9	03-09-1091	1	02-09-1119	9
10 PIN	22386-010	1	19690-001	10	09-50-3101	1	08-50-0106	10

WARNING

The pin number designators for the ANSI SMD interface follow the designation shown below.



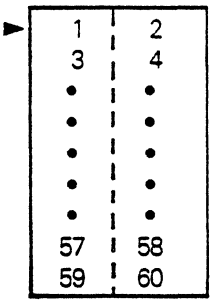
60 Pin Connector



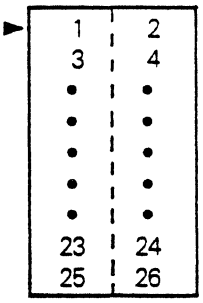
26 Pin Connector

► This is the arrow moulded in the connector.

The Century Data Systems pin number designators follow the designation shown below.



60 Pin Connector



26 Pin Connector

Note that the signals are on the same physical pins, regardless of the numbering system used. Use the CDS system in conjunction with CDS schematics and logics.

SECTION 7
CONTROLS AND INDICATORS

7.1 CDS INTERFACE

Front Panel
None

Rear Panel
None

Internal
Location of the dip switch, S-1, used for sector length selection and write protection is as follows:

M20 — Basic Control PCB
M40 — Piggyback PCB

M80/M160 — Logic and Control PCB U-38 (CDS Interface)

Table 7-1. Number of Sector Switches

Switch S1		Sector Length (Data Field)
-1	-2	
Closed	Closed	128 Bytes
Closed	Open	256 Bytes
Open	Closed	512 Bytes
Open	Open	1024 Bytes

Table 7-2. Write Protect Switches

SWITCH S-1								PROTECTED HEAD	
-3	-4	-5	-6	-7	-8	-9	-10	M20	M40
CLOSED	—	—	—	—	—	—	—	1	0
—	CLOSED	—	—	—	—	—	—	2	1
—	—	CLOSED	—	—	—	—	—	3	2
—	—	—	CLOSED	—	—	—	—	0	3
—	—	—	—	CLOSED	—	—	—	—	4
—	—	—	—	—	CLOSED	—	—	—	5
—	—	—	—	—	—	CLOSED	—	—	6
—	—	—	—	—	—	—	CLOSED	—	7

Table 7-3. Write Protect Switches

SWITCH S-1								PROTECTED HEAD
-3	-4	-5	-6	-7	-8	-9	-10	M80/M160
OPEN	—	—	—	—	—	—	—	0
—	OPEN	—	—	—	—	—	—	1
—	—	OPEN	—	—	—	—	—	2
—	—	—	OPEN	—	—	—	—	3
—	—	—	—	OPEN	—	—	—	4
—	—	—	—	—	OPEN	—	—	5

7.2 SMD INTERFACE

Front Panel
None

Rear Panel
None

Internal
Locations of the dip switches used for sector length selection and unit select is on the SMD and I/O Control PWB as follows:

Location A1 = Unit Select
Locations A3, A4, A5 = Sector Length

Table 7-4. Sector Switches

Binary* Weight	Switch Location	Switch Position
2048	A3	1
1024	A3	2
512	A3	3
256	A3	4
128	A4	1
64	A4	2
32	A4	3
16	A4	4
8	A5	1
4	A5	2
2	A5	3
1	A5	4

*SWITCH OPEN = ONE
SWITCH CLOSED = ZERO

Total binary weight equals total bytes per sector (Data, Check, ID, and OH).

Table 7-5. Unit Select Switches

Binary* Weight	Switch Location	Switch Position
1	A1	1
2	A1	2
4	A1	3
8	A1	4

*SWITCH OPEN = ONE
SWITCH CLOSED = ZERO

Degate Switch

a. Located on the SMD/IO Control PWB P/N 24520-001

b. Switch location A2

Table 7-6. MTC Port Connector and Pins (J21)

Pin Number	Signal Name	Source
1	GND	LOGIC CONTROL
2	VMA	LOGIC CONTROL
3	GND	LOGIC CONTROL
4	E	LOGIC CONTROL
5	VCC	LOGIC CONTROL
6	HALT/	EXTERNAL
7	R/W	LOGIC CONTROL
8	MA0	LOGIC CONTROL
9	MA1	LOGIC CONTROL
10	MA2	LOGIC CONTROL
11	MA3	LOGIC CONTROL
12	MA4	LOGIC CONTROL
13	MA5	LOGIC CONTROL
14	MA6	LOGIC CONTROL
15	MA7	LOGIC CONTROL
16	MA8	LOGIC CONTROL
17	MA9	LOGIC CONTROL
18	MA10	LOGIC CONTROL
19	MA11	LOGIC CONTROL
20	MA12	LOGIC CONTROL
21	MA13	LOGIC CONTROL
22	MA14	LOGIC CONTROL
23	MA15	LOGIC CONTROL
24	MD0	LOGIC CONTROL
25	MD1	LOGIC CONTROL
26	MD2	LOGIC CONTROL
27	MD3	LOGIC CONTROL
28	MD4	LOGIC CONTROL
29	MD5	LOGIC CONTROL
30	MD6	LOGIC CONTROL
31	MD7	LOGIC CONTROL
32	NMI/	EXTERNAL
33	(NOT USED)	
34	BA	LOGIC CONTROL
35	INPUTDEV/	EXTERNAL
36	VCC	LOGIC CONTROL
37	EXSEL/	LOGIC CONTROL
38	GND	LOGIC CONTROL
39	CLEAR/	EXTERNAL
40	GND	LOGIC CONTROL

The connector for the MTC Port is a 40 pin flat cable receptacle, CDS P/N (TBD).

Jumpers

a. Located on the SMD/IO Control PWB P/N 24520-001

b. "READ ONLY MODE", jumper test point one to test point two to protect all data on the unit. Controller must check write protect line.

Note

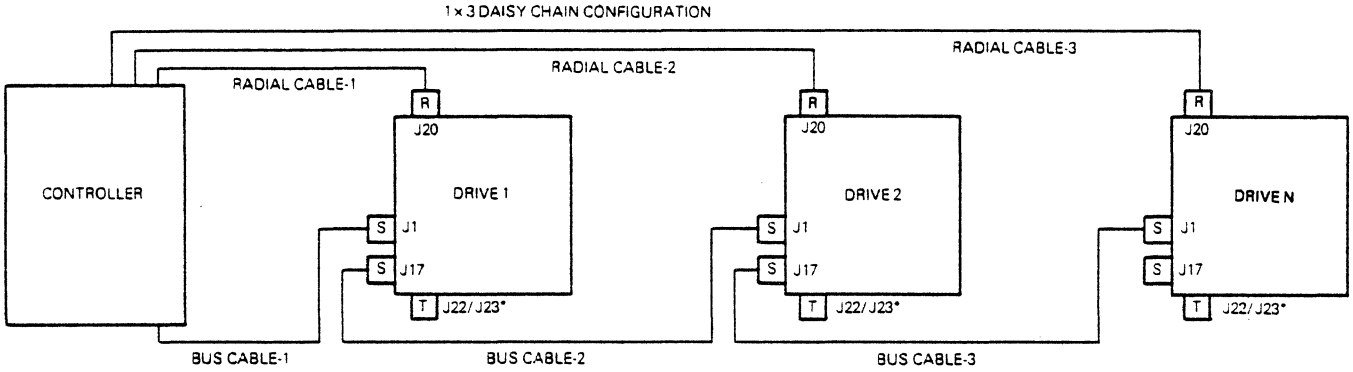
A remote Read Only switch may be connected to test points 1 and 2. When installed the protect status can change only when the drive is selected (or deselected and reselect).

c. "HOLD, or ANSI SEQUENCE DISABLE"

1. Jumper test point 4 to test point 3 to convert the HOLD/ signal to an ANSI compatible sequence disable signal.

Note

The normal mode of operation is with the jumper not installed. See the Technical Manual for Theory of Operation.



*Only last drive on BUS has a terminator in J22/J23.

Figure 7-1. SMD Cabling Diagram

SECTION 8
ENVIRONMENTAL CHARACTERISTICS

8.1 TEMPERATURE (with or without optional enclosure)*

Equipment Operational:	50°F to 104°F (10°C to 40°C) with a max. gradient of 18°F (10°C) per hour (M80/M160 to 104°F)
Equipment Non-Operational:	−40°F to 140°F (−40°C to 60°C)
Temperature Cycling:	No condensation shall result.

8.2 HUMIDITY (with or without optional enclosure)

Equipment Operational:	10% to 90% R.H., with a wet bulb temp. limit of 80°F (27°C) (provided there is no condensation).
Equipment Non-Operational:	5% to 95% R.H., provided there is no condensation.

8.3 ALTITUDE (with or without optional enclosure)*

Equipment Operational:	From 1000 feet below sea level to 10,000 feet above sea leave.

*without enclosure, 80 feet/minute air flow must be maintained over the base casting.

8.4 VIBRATION (with optional enclosure)

Equipment Operational:	The equipment shall withstand a peak displacement of ±0.006 in. (.015 cm) for the frequency range of 20 Hz to 40 Hz and ±1g for the 40 Hz to 200 Hz range.
Equipment Non-Operational:	The equipment when packed for shipment shall withstand ±1.5g from 5 Hz to 500 Hz for one hour along each of the three mutually perpendicular axes, with a 12 minute sweep time.

8.5 SHOCK

The equipment shall perform all read/write operations (no seek) according to specifications, while being subjected to 18 impact shocks of 5g (±10%) consisting of 3 shocks along each direction fo three mutually perpendicular axes. Each shock impulse shall be half sine wave with a time duration of 11 (±1) msec.

8.6 SERVO OVERTEMPERATURE (M80, M160)

If the Torquer Motor exceeds a preset temperature, the seek rate will decrease inversely to the temperature rise. A continuing rise in temperature will cause a drive FAULT.

SECTION 9
POWER REQUIREMENTS

9.1 BASIC DRIVE

9.1.1 AC Power

100/115V (+10%, −15%), 50/60 Hz (±1Hz)
Running: 1.5A
Starting: 11.0A

200/220/240V (+10%, −15%), 50/60 Hz (±1Hz)
Running: 0.8A
Starting: 5.5A

9.1.2 DC Power

M20/M40	M80
+24V, ±5%, 2.7A*	+24V, ±5%, 3.3A
−12V, ±5%, 0.3A**	+12V, ±5%, 1.0A
+5V, ±5%, 2.5A**	−12V, ±5%, 1.0A
	+5V, ±5%, 7.0A

M160
+24V, ±7%, 2.7A
+12V, ±3%, 1.0A
−12V, ±3%, 3.0A
+5V, ±5%, 7.0A

*Tolerance includes ripple less than 10 KHz. Greater than 10 KHz ripple should be less than 0.5%.

**Ripple must be less than 0.5%, 10 KHz or greater.

9.1.3 HEAT DISSIPATION

Basic Drive — 1195 BTU/HR (M20, M40)
650 BTU/HR (M80)
M160 (TBS)

Driver/Receiver — 18 BTU/HR

9.2 POWER SUPPLY AND DRIVE

9.2.1 AC Power (M20, M40)

100/115 *(+10%, −15%) 50/60 Hz (±1Hz)
Running: 3.5A (M80 =)
Starting: 13.0A (M80 =)

*115V available only for 60 Hz operation

200/220/240V (+10%, −15%) 50 Hz (±1Hz)
Running: 2A (M80 =)
Starting 6A (M80 =)

9.2.2 AC Power (M80, M160)

100/115/200/220/240 (+10%, −15%) 50/60 Hz (±1 Hz)
Running .5KVA
Starting 1.6KVA

9.2.3 Heat Dissipation

1485 BTU/HR

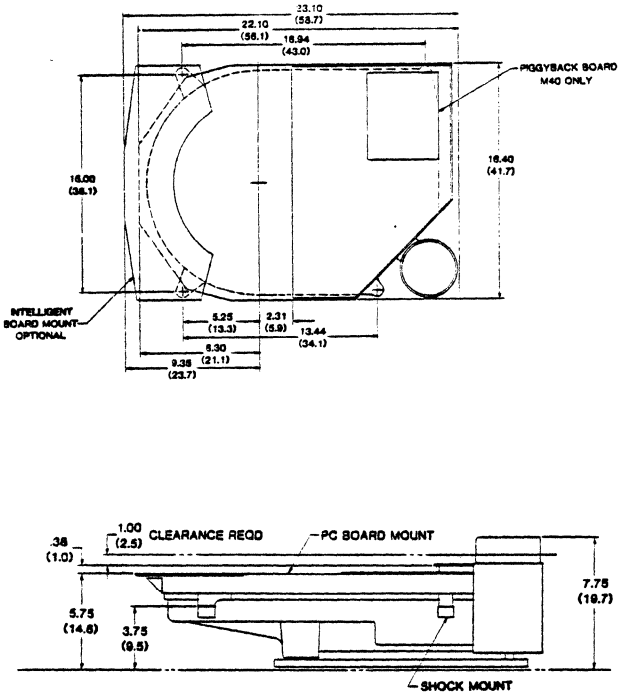
SECTION 10
PHYSICAL CHARACTERISTICS

10.1 PHYSICAL SIZE

	Basic Drive	Enclosure Option
Height		8 inches (203mm)
Width		16.5 inches (419mm)
Depth		23.5 inches (596mm)
Weight		40 pounds (20kg)
Shipping Weight		60 pounds (27kg)
Heat dissipation		1485 BTU/hour

10.2 MOUNTING ATTITUDES

Horizontal – spindle pulley down
Vertical – unit on side motor on top.



With optional enclosure:

Height	8.75 inches (222mm)
Width	17.5 inches (445mm)
Depth	27.5 inches (698mm)
Weight	110 pounds (50kg)
Shipping Weight	130 pounds (58kg)

Figure 10-1. M20, M40 Basic Drive Dimensions

SECTION 11
MARKSMAN ENCLOSURES

11.1 OPTIONAL ENCLOSURES

There are three optional enclosures available for use with the MARKSMAN drives.

- Desk Top Enclosure (See Figure 11-1).
- Rack Mounted (Fixed) Enclosure (See Figure 11-2).
- Slide Mounted Enclosure (See Figure 11-3).

11.2 ENCLOSURE AND AC DISTRIBUTION

Each enclosure provides mounting for the sealed mechanical assembly, drive control board, interface board and optional power supply. If the power supply is ordered, the AC distribution is located on the back panel of the enclosure. The enclosure also provides all necessary cooling required by the MARKSMAN drive, when ordered with the Power Supply.

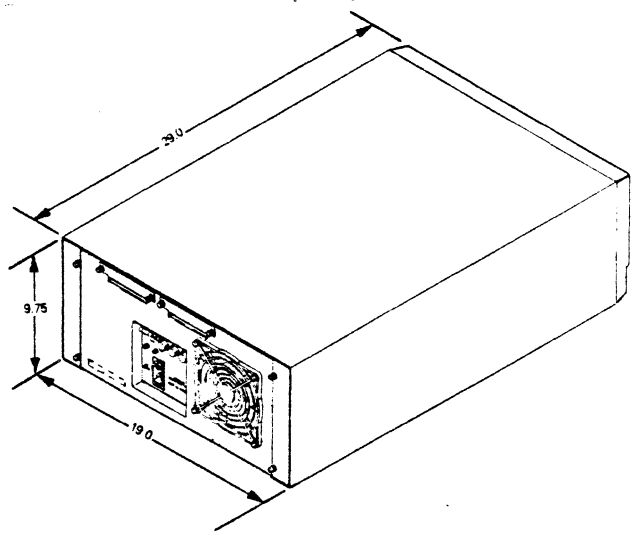


Figure 11-1. Desk Top Enclosure

11.3 RACK MOUNT SLIDES

This enclosure can be ordered with a set of slides that mount between the enclosure and a standard RETMA rack and provides forward travel of the drive to extend clear of the rack for ease of maintenance and installation. Enclosures fit in a standard 19 in. × 30 in. × 9 in. rack.

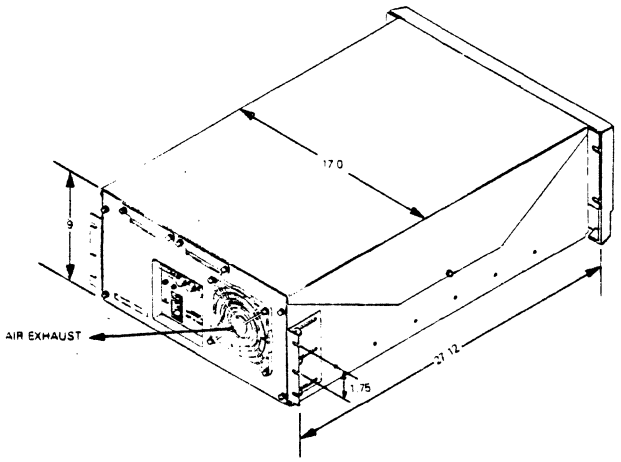


Figure 11-2. Rack Mounted (Fixed) Enclosure)

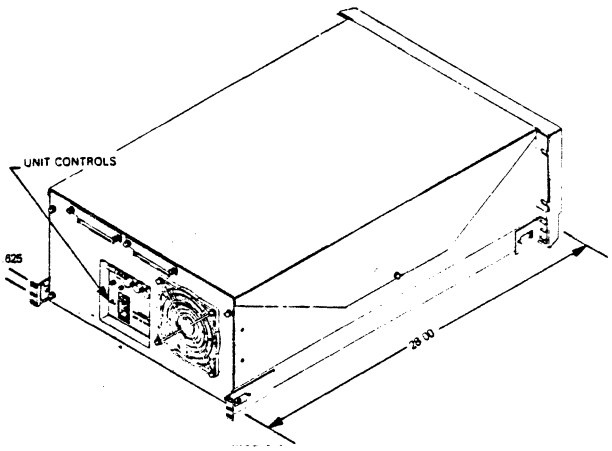


Figure 11-3. Slide Mounted Enclosure

APPENDIX A
DRIVER/RECEIVER OPTION

GENERAL

The MARKSMAN Driver/Receiver Feature increases the allowable interface cable length of the MARKSMAN from 4 inches to 50 feet. It also provides the means by which drives may be daisy chained.

INTERFACE

Refer to Tables A-1 through A-4 for interface pin assignments.

Table A-1. Interface Pin Assignments — Bus

J1-	J2-	Serial Name	Source Ckt	Dest Ckt
1	1	GRD		
2	2	ICBUS 6/	75462	74LS240
3	3	ICBUS 5/	75462	74LS240
4	4	ICBUS 7/	75462	74LS240
5	5	ICBUS 2/	75462	74LS240
6	6	ICBUS 4/	75462	74LS240
7	7	ICBUS 0/	75462	74LS240
8	8	ICBUS 3/	75462	74LS240
9	9	ICBUS 1/	75462	74LS240
10	10	GRD		
11	11	GRD		
12	12	IRST/		74S367
13	13	GRD		
14	14	SPARE		

Table A-2. Interface Pin Assignments — Signal

J1-	J2-	Serial Name	Source Ckt	Dest Ckt
15	15	GRD		
16	16	IRDGATE/		74S367
17	17	GRD		
18	18	IWRGATE/		74S367
19	19	GRD		
20	20	ICREQ/		74S367
21	21	GRD		
22	22	IDRDY/	75462	
23	23	GRD		
24	24	ICRDY/	75462	
25	25	GRD		
26	26	IWRTSUF/	75462	
27	27	GRD		
28	28	ICACK/	75462	
29	29	GRD		
30	30	ISEC/	75462	
31	31	GRD		
32	32	IIDX/	74562	
33	33	GRD		
34	34	ICSTAT/	75462	
35	35	GRD		
36	36	TERMIN		
37	37			
38	38			
39	39			
40	40			

Table A-3. Interface Pin Assignments – Data

J3-	Serial Name	Source Ckt	Dest Ckt
1	GRD		
2	GRD		
3	IWDATAP	**	
4	IWDATAM	**	
5	GRD		
6	ISELECT		74LS132,
7	GRD		
8	IRDATAM	*	
9	IRDATAP	*	
10	GRD		
11	IRDCLKM	*	
12	IRDCLKP	*	
13	GRD		
14	IWRTCLKM	*	
15	IWRTCLKP	*	
16	GRD		
17	RCRDY	75462	
18	+5V		
19	+5V		
20	RSEC/	75462	
21	RIDX/	75462	
22	RSELECTED/	75462	
23			
24			
25			
26	GRD		

*See Table A-1
**See Table A-2

Table A-4. DC Pin Assignments

J6-	Serial Name
-1	+5V
-2	GRD
-3	-12V
-4	+12V
-5	GRD

Table A-5. DC Pin Assignment (Flat Cable)

Pin	Serial Name	Pin	Serial Name
1	DC GND	6	+24V GND*
2	DC GND	7	+24V GND*
3	KEY	8	+5V
4	DC GND	9	+5V
5	+12V	10	-12V

* = not connected

APPENDIX B

Customer Designed Printed Circuit Board

Customer designed PCB's should meet the specifications in figure B-1. Since the T-2004 exerciser receives its power from the same cable which feeds this PCB, the power connector location and pin numbers (Figure 6-1) must be located as on the drawing. The MARKSMAN optional enclosure expects the I/O cables to exit from the locations shown for the 40 pin and 60 pin connectors. If this enclosure is not used, these connectors may be relocated. M20/M40 shown.

Customer designed PCB specifications are the same for M80/M160.

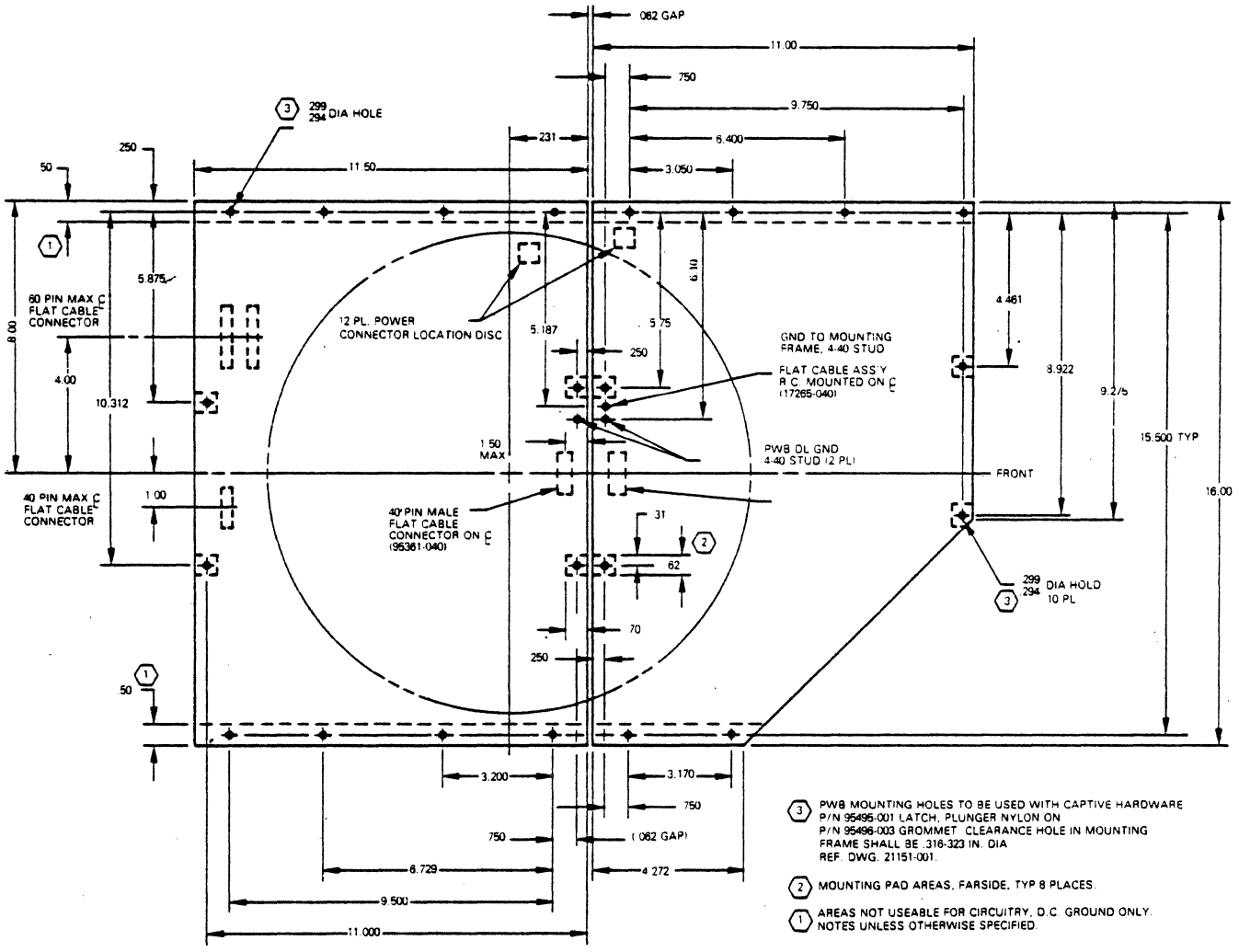


Figure B.1. Customer Designed PCB Physical Requirements

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