Hardware Reference Manual

32K-128K Dynamic RAM Board

Central Data Corporation

713 Edgebrook Drive, Champaign, IL 61820 Phone: (217) 359-8010

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Central Data Corporation
P.O. Box 2530, Station A
Champaign, Il 61820
Phone: (217) 359-8010

TABLE OF CONTENTS

Section		Page
1	General Information	1
2	Functional Description	3
3	Principles of Operation	5
	Addressing and Buffering	5
	RAM Group Selection	7
	8- and 16-bit Operation	8
	Timing	10
	Parity Checking	12
4	Installation/User Selectable Options	14
	Addressing	14
	XACK and AACK Generation	15
	Interrupt Selection	16
5	Specifications	17
6	Schematics	20

1. General Information

The Central Data 32K-128K Dynamic RAM board is designed to be used with any standard Multibus* system. The board has an access time of 330ns under normal conditions, and a cycle time of 450ns. If an access is started just after a refresh has begun, the access time can then be as long as 880ns. Normally, refresh cycles are inserted by the board so that they will avoid all access cycles, thus providing the fastest possible access time.

The board is divided into two 64K sections, each independently addressable on a 64K boundary in the system. Also, a dip-switch is provided to enable or disable individual 16K banks of each 64K section. Thus, the board can appear to the system as anywhere from 16K-128K of memory, although using some combinations causes part of the memory on the board to be wasted (16K, for example, is below the 32K minimum capacity of the board). Dip-switch addressing allows the user to address the board in a 16-megabyte address space, due to the 24 address lines decoded by the board. Since the normal Multibus allows only 20 address lines, Central Data has defined four pins of the P2 connector as address lines A20 through A23 on all of its memory boards and bus masters.

The board has a standard feature of parity checking which can be used to alert the user or host computer of a memory error. When a parity error occurs, the group of RAMs which caused the error can be determined by three LEDs mounted on the top of the board. An error reset button is also provided to clear the error condition. The user can also select that the occurance of a parity error will generate an interrupt on any of the vectored interrupt lines of the Multibus.

When the processor is interrupted because of a parity error, it can read an input port on the board to determine which group of RAMs failed. By writing to the same port address, the error condition can be cleared and the interrupt removed. This I/O port address can be decoded using either an 8- or 16-bit address. This allows for full compatibility with older processors which generate only 8-bit addresses as well as the new Multibus specification which calls for full 16-bit I/O addressing capabilities. The selection of the

I/O addressing mode is made with a shorting plug.

The board drives both the XACK and AACK lines of the Multibus to allow for the greatest flexibility. It returns XACK when the data transfer is complete, normally within 330ns of the start of the command. The AACK can be strapped by the user to return from 0-100ns after an access cycle is started on the board. When AACK is strapped properly, it allows the fastest possible system operation.

* Multibus is a trademark of Intel Corporation and is used throughout this manual.

2. Functional Description

The 32K-128K Dynamic RAM board is divided into several major sections. A brief description of each section is provided in this chapter, with more detailed information given in the Principles of Operation chapter.

The addressing of the board consists of both memory and I/O decoding circuitry. For both of the possible 64K sections of memory, a 8-position dip-switch is provided to select the address space that the bank is to occupy. The I/O address decoder consists of two 8-position dip-switches, one for address lines A0-A7 and the other for lines A8-A15. The upper address lines are only used in the address comparison process if a shorting plug is placed on the "Extended I/O" pins on the board.

For each 64K section there are four groups of RAMs, split between the upper and lower bytes (for even and odd addresses) and split in the middle of the 64K section (since 16K RAMs are used). Each group of RAMs has 9 chips, with one being used by the parity circuitry. Address A0 and the BHEN line determine whether the upper or lower data chips (or both) get enabled, while A15 is used to select which 32K half is to be used.

Since the board is designed to work in 8- or 16-bit systems, a "byte swapping" circuit was needed to allow 8-bit transfers to any location in the memory as well as to allow 16-bit transfers to any word location. This circuit, in 16-bit mode, transfers data between the 16-bit Multibus data bus and the 16 data RAMs currently selected. During 8-bit transfers, the board must always operate with the Multibus D0-D7 lines, requiring odd bytes to be shifted to these lower data lines.

The timing section of the board controls the generation of all timing signals needed by the dynamic RAM chips. It also makes sure that refresh cycles are performed when needed, and places these cycles after access cycles are completed so that a minimum of interference is generated. In most systems, refresh cycles will never hold up an access, thus the board will operate at its maximum speed.

Finally, the parity section of the board generates odd parity check bits and stores them into memory on write cycles. The memory is checked on read cycles for proper values. Parity errors can simply illuminate an LED, or may also generate an interrupt to the processor for further diagnostics.

3. Principles of Operation

This chapter details the operation of the entire memory board. Any signals named in this text followed by a slash (/) indicates that the signal is active-low.

As in all Central Data schematics, a grid system is provided to help locate sources and destinations of signals. The source of any named signal will have references to all locations on the schematics where the signal is used. Each location where a signal is used, a reference is given to where it was generated.

If the location is on the same sheet as it is being referenced, it will show only a grid location (i.e. D2). If, however, the referenced signal appears on a separate page, it will have the grid location preceded by the sheet number (i.e. 2-B5).

Furthermore, if a group of signals is commonly routed together, that group may be cross-referenced together. It is not necessary that all members of the group go to each destination listed, since the purpose of the cross reference system is only to guide a user through the schematics.

Addressing and Buffering

This board allows two independent dip-switch addressable 64K memory sections. Also, the parity I/O port requires address decoding on the lower 16 address lines.

Since all Central Data Multibus products are designed to address a full 16-megabytes of memory, four additional address lines had to be added to the standard bus specification. These four lines are found on P2 as shown below:

P2 Pin	Signal
57	A20/
58	A21/
59	A22/
60	A23/

On sheet 3 of the schematics, all of the address lines from the Multibus are buffered through 74LS04 gates. The Central Data Mother board provides standard termination and bussing for the upper four addresses on P2 so that they stay at logic "0", provided no other board drives them to a "1".

The memory command lines (MRDC and MWRC) and the RAM inhibit line (INH1) are also buffered on this sheet. All of the buffered signals are then routed to sheet 1 of the schematics.

The buffered address lines go to three address comapartor circuits. Each circuit consists of a number of 74LS266 open collector exclusive-NOR gates. For each circuit, all of the outputs of the gates are tied together. In this manner, each two-input gate pulls the common output low if its inputs do not match. If all of the pairs of inputs match, the common output is pulled high by a resistor to +5V.

The I/O port address comparator consists of 16 such gates, each having one input going to a buffered address line, and the other going to a dip-switch. This dip-switch, when closed, causes the corresponding gate input to become grounded. Under this circumstance, the address line leading to the same gate must also be low for the port to be addressed. If the switch position is left open, the input to the gate goes to a high state, thus comparing for a high address line.

For I/O addressing, the sixteen gates are divided into two equal groups. This is done so that the user has the option of decoding only the lower eight address lines instead of the normal sixteen. When this option is exercised, the outputs of the gates relating to the upper eight I/O address lines (BA8-BA15) are disconnected from the line which determines if addresses are equal.

The I/O address equal line (found on pins 2 and 4 of IC88) is gated with the IORC and IOWC lines (which are buffered from the Multibus). The outputs of these two gates are the RD PARITY/ and CLR PARITY/ signals which are used to gate error information onto the bus and to clear the error condition, respectively. If either of the two lines goes low, it activates the SEL PORT/ signal which is used to generate an XACK to the processor.

The two 64K banks of memory are addressed with the comparator circuits shown on the left side of sheet 1. Both of these comparators operate with the same group of address lines as inputs, but each has a different dip-switch. The operation of both comparators is the same as that of the I/O

comparator described earlier.

When either of the two memory address comparators finds that the board is being addressed, its corresponding output (pin 1 or 2 of IC105) goes high. Pin 12 of IC93 then goes low whenever the board is selected, in either bank. Note that if the RAM inhibit signal (INH1) ever goes high it prevents either bank from being selected.

The board generates two command acknowledge signals. The first, XACK, indicates when a memory transfer is complete and the processor can go to the next cycle. The other, AACK, gives the processor advance information concerning when a transfer will be complete.

The circuitry which generates the acknowledge signals is found on sheet 3 of the schematics. For AACK, it consists of a shift register which is kept cleared until the board starts an access cycle (any cycle on the board except a refresh). When this occurs, pin 5 of IC76 is clocked high, allowing the register to shift 1's through at the system clock (CCLK) rate. The eight outputs of the shift register, which go high from 100-800ns after the time an access cycle starts, can be jumpered to the AACK driver (IC94). Note that since the start of a cycle is asynchronous with respect to the bus clock the outputs may vary up to one clock cycle (i.e. the second output can occur anywhere from 100-200ns after the cycles starts). The user can also select that AACK be returned immediately after the cycle is started on the board (by strapping "0") or setup the board so it never returns AACK (by strapping "NU").

The XACK signal is generated when an access cycle is finished. T5 signals when the access time of the RAM chips has been met, and that data is available on the Multibus data lines during a read cycle. The REF CYC/ signal on the inputs to the flip-flops prevents the board from acknowledging the cycle if it is busy with a refresh.

For any I/O operation to the board, XACK/ is immediately driven low by a seperate driver, since the I/O circuitry is fast acting.

RAM Group Selection

Once the comparator circuits determine that the board is being selected, a multiplexer is used to determine if the addressed 16K bank in the section is enabled. This device (IC92 on sheet 1) is enabled when either the top or bottom sections of RAMs are addressed. The eight inputs to the device correspond to the possible 16K sections that the board can contain. If the board is to respond to commands

for a particular 16K section, the corresponding dip-switch position must be left open. This gates a high signal to the multiplexer, allowing the Y output to go high. This output is used in conjunction with the MCOMD signal to generate BD SEL. This output is used to start every access cycle on the board. The address inputs to the multiplexer (pins 9-11) select which input pin is gated to the outputs. On sheet 2, the 3480 controller chip contains a one-of four decoder that determines which row of RAMs should be enabled. Since there are four rows, each row can hold 32K bytes of data. When the top address comparator was the one found equal, one of the top two rows of RAMs is enabled. Likewise, when the bottom comparator finds an equal combination, one of the lower two rows is enabled.

The buffered address line BA15 is fed into pin 18 of IC80 to pick the row in the top or bottom half which is to be selected. When A15 is low, the top row of the half is enabled. When it is high, the bottom row is enabled. Note that none of the RAMs are enabled unless the proper input timing signals are present (T1-T5 and REF GRANT) to prevent any row from being enabled during refresh or when the board is not selected. Pin 17 of the controller is tied the the SEL LO line which is high when the bottom address comparator is equal, thus selecting one of the bottom two rows of RAMs.

The RAMs are further split into two halves, one for bytes on even address boundaries, and one for bytes on odd boundaries. During 16-bit operations, both halves are used, while during 8-bit operation only one is. Exactly how the different sides are selected is explained in the next section.

8- and 16-bit Operation

The Multibus provides a signal (BHEN) to indicate when 16-bit transfers are to take place. When it is high, 16-bit transfers occur over the full data bus, with even bytes appearing on the lower eight lines (D0-D7) and odd bytes on the upper eight (D8-D15). During 8-bit operation (when BHEN is low) all data transfers take place over the lower 8 data bus lines. If a word of data is written in two single byte operations, the even byte is written as normal--from the lower 8 Multibus data lines to the lower 8 RAMs. On the write of an odd byte, however, the lower eight Multibus data lines must be written to the upper eight RAM chips. This requires the use of an extra buffer to provide the capability to transfer 8-bit data between the lower Multibus data lines and the upper RAM chips.

On the center of sheet 1, the 74S226 Multibus data latches/buffers are found. The 18-bit internal data bus shown above the buffers is used to carry data between the RAMs, parity circuitry, and the data buffers. When pin 1 of the buffers are brought low, the internal data bus is latched. This data is latched during read cycles, so that it stays available even after the RAM's outputs change. When pin 7 of any buffer is brought high, data is gated from the buffer's internal latch to the Multibus. When pins 9 and 14 of any buffer are brought high, data is gated directly from the Multibus to the internal data bus.

Buffers IC112 and IC114 are used to gate data between the lower eight Multibus data lines and the lower eight RAM chips. IC119 and IC121 are used to gate data between the upper data lines and the upper chips. IC122 and IC123 are used for the swapping process, transfering data between the lower data lines and the upper RAMs.

One important thing to note is that the only condition where the swapping buffer is needed is when BHEN is low and BA0 is high, indicating an 8-bit transfer with an odd address. This combination causes SWAP (pin 11 of IC87 on sheet 2) to go high.

When a non-swapping memory read operation is in progress, pin 12 of IC84 will be driven high. This causes the normal buffers (all 16-bits) to drive data onto the Multibus. Note that during reads of even bytes, the odd byte appears on the upper data lines, although the processor will not use it.

When the bus master wishes to read a single odd byte, SWAP goes high, disabling the normal buffers and enabling the swapping buffer in the same manner as normal reads, with pin 6 of IC84 going high. During this type of transfer, the upper Multibus data lines are not driven.

During any read cycle, it should be noted that the entire row of RAMs associated with the address are read (although not necessarily gated to the Multibus). This is because the chip select pin (RAS/) of the RAMs is not broken between the even and odd halves. During write operations, however, if a single byte is being written, only that byte's write enable can go low. If this were not the case, the companion byte would also be written.

During write cycles, when data is being gated into the board, only the specific buffers needed are enabled. For 8-bit operations, only one of the three sets of buffers will gate data into the board. If data was simply gated the same as in read mode (except the direction), a conflict would arise between the data buffers and the RAM chips that are

not being written. This conflict results from the fact that the entire row of RAMs being accessed is enabled when a write operation occurs. If only one byte is being written, then only one half of the RAMs will have their write enable pins brought low. Since the other half of RAMs will not have their write enbable pins low, and since their chip select is low (it is in the same row as the accessed devices), it does a read cycle. Thus, if the buffers associated with those non-written RAMs are enabled, they will be forcing data from the Multibus to the internal data lines, as will the RAMs, which are doing a read cycle.

As shown on the schematics, there is one write enable line for each bank of RAMs (even and odd). WRLO/ is used when a write is to occur to an even (A0=0) byte, while WRHI/ is used when the system is writing to an odd byte (A0=1). The first line is generated when MWRC/ and SWAP are both low. SWAP will only be high on byte writes to odd addresses, thus being the only time that a write to the board will not access the even half.

The write enable for the odd bank is generated whenever A0/ is low (for odd bytes) or when BHEN/ is low (for both bytes), and when the system is doing a memory write.

The circuitry that determines which buffers are enabled, and brings their input enables (OCB and S2, pins 9 and 14) high is on sheet 1. Whenever an even byte of memory is being written, the buffers associated with it (IC112 and IC114) must be enabled. This is done by using the WRLO signal to enable these buffers. On writes to odd bytes, however, a determination must be made as to whether the data should come from the lower or upper data lines. On 8-bit transfers, the data comes from the lower eight lines. When BHEN is low along with WRHI/, the WRHL signal goes high, gating data from the lower Multibus data lines to the high-order RAM chips. This signal is used to enable IC122 and IC123. If a 16-bit transfer is occuring, then BHEN/ will be low, and it is gated with the odd write-enable signal to form the data buffer enable on IC119 and IC121.

Timing

The timing for the board is generated on sheet 4 of the schematics. Timing for the board includes the generation of proper signals for the memory devices as well as assuring that refreshes occur as necessary in order to guarantee data retention.

An oscillator on the sheet is used to indicate when a refresh cycle is needed. The period of the oscillator is about 15us, with pin 9 of IC75 clocked high every cycle.

This output indicates that a refresh cycle is needed, and is cleared when the refresh occurs. The second flip-flop is used to actually start a refresh cycle, normally at the end of a memory access cycle on the bus (MCOMD/). When a command is completed, this signal makes a rising transition, causing pin 5 of IC75 to go high if a refresh is needed. If a memory command is not present by the time the oscillator reaches the half-cycle point (with pin 4 of IC81 going high), then the REF RQ latch is forced high, causing an asynchronous refresh to start. Note that this can happen at any time with repect to the next memory command to the board, and refresh cycles started in this manner may cause a delay in the next access. Note that this design makes sure that the board will do refreshes when required, despite what the rest of the system is doing.

Access cycles are started when the BD SEL signal goes high, causing pin 9 of IC86 (ACCRQ) to follow. This signal is cleared when the access cycle is done (when XACK/ goes low).

The two request signals arrive at an arbiter circuit which determines if a refresh or an access cycle should be started. Normally, both request lines are low, and pins 8 and 11 of IC78 are high. When either request signal goes high, the corresponding output goes low, causing the circuit to latch in that state. If both signals go high at the same time, the latch will start a refresh cycle, because of the capacitor on pin 11. This capacitor is required to prevent the latch from oscillating with simultaneous request inputs.

Pin 3 of IC83 goes high when either type of cycle is requested and the previous cycle is complete. If a refresh cycle has been selected, REF GRANT will go high also, allowing refresh addresses to be gated to the RAM chips. After a small delay which guarantees that the latch has stabilized, the cycle is started with T1 going high. This causes CYCLE/ to go low, and T2 follows shortly afterward. A precision delay line is used to generate T3 and T5 to the memory controller, and another output is used to cause CYCLE/ to return high, allowing a new cycle to begin. The marking on the schematics for the delay line indicate the nominal delay (in nanoseconds) from the input signal to the respective output.

All of the timing signals are routed to the RAM array (sheet 2), which generates the addresses for the RAMs as well as the RAS/ and CAS/ signals. T1 starts the RAS/ signal, T2 causes the addresses to switch from row to column, T3 starts the CAS/ to the devices, and T5 causes RAS/ and CAS/ to return high. T2 is also routed to the T4 input to the controller, since this input is not used in this implementation. A refresh cycle is started if REF GRANT

went high just before T1, while an access cycle is started if it did not.

Complete information concerning the memory controller chips (the 3480 and the 3242) can be obtained from the manufacturer of the parts, Motorola.

Parity Checking

In order to minimize problems of improper data causing damage to an executing program, parity checking is a standard feature of the board. The parity circuitry generates an odd parity bit for any write cycle to the board, and checks that bit when any locations are read. Parity is generated on a byte basis (a requirement since the Multibus allows 8-bit or 16-bit transfers), with IC9, IC18, etc. being used to hold the parity data. Odd parity is defined as an odd number of bits being high in the data byte and its associated parity bit.

The parity generating/checking circuitry is shown on sheet 5 of the schematics, with the main elements being the 74180 parity generators. These circuits have eight inputs (which are tied to the data portions of the internal data bus), and one output. The output is high when the parity of the input lines is even (an even number of bits high). These outputs are run to the data in lines of the parity RAMs, and they cause odd parity to be stored (since it is storing a bit disruptive of the even parity).

On read cycles, the parity bit read from the RAMs is compared with the bit generated by the 74180. If the two bits do not match, one of the exclusive-OR gates (IC126) will show the error. Note that the error indication does not become valid until the access time of the RAM chips have been met. When the board is selected, and it is in a read cycle, and the access time has been met (with XACK high), pin 8 of IC84 will go high. This latches pertinent data into the 74LS174 latch (IC96).

The data stored in the parity latch allows the failing RAM to be traced to one of eight groups on the board. The output of the latch is a binary-coded pointer to the group of RAMs which failed.

The signals which are used as inputs to the latch are BA15, to determine which row in a 64K section triggered the error, SEL LO to indicate which 64K section was being accessed, and the parity error line from pin 3 of IC126, which is high when the error occured in an even byte of memory. When the three bits are used to form a BCD number, the group of RAMs which failed can be located by comparing to the group

numbers printed on the board.

When the parity error latch is clocked, it forces one output to go high, which is used to generate the interrupt, and prevents the latch from being clocked again. All four outputs of the latch are run to a 74LS125 tri-state buffer, which the processor uses to determine if this board had an error, and if so, which group of RAMs failed. The inverted outputs of the latch drive LED arrays which are located on the top of the board. This allows visual inspection of the error. Note that the LEDs marked "1, 2, and 4" can be going on and off during normal accesses. Only when the "ERROR" lamp comes on does it mean that an error occured.

When the processor reads the parity port, the lower 3 bits indicate the failing group, with the next higher bit reading low for an error, and high for no error. The lower three bits are inverted from their presentation on the LEDs, with all zeros indicating group 7.

An error reset button is provided on the top of the board to clear the outputs of the latch, and a write to the board's parity port will cause the same result. Also, on system initialization, the error latch is cleared.

It should be noted that for the parity circuit to work properly, each location of memory must be written before it is read, to prevent random errors from occuring. This can be done during initialization by clearing all memory locations.

4. Installation/User Selectable Options

The 32K-128K Dynamic RAM board is designed to operate in any standard Multibus system. The board can occupy any card position of the system, since it does not operate as a bus master.

Addressing

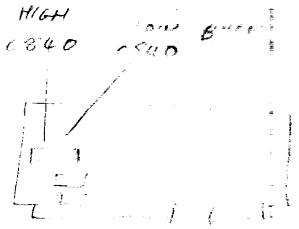
Each 64K section of the board is addressed independently by dip-switches. The 64K sections can be setup to start on any 64K boundary in a 16-megabyte system address space. Also, a parity I/O port is provided on the board so that the processor can read parity error status and clear parity errors.

The memory is addressed by setting switches for the top or bottom rows of memory. The top two rows are addressed with the dip-switch marked HIGH BANK. The bottom two rows of RAM are addressed with the switch marked LOW BANK. Also marked on the board are indications of the address line corresponding to each switch position, as well as the polarity of the switches. Address 23 is selected by the left-most switch, while address 16 is selected by the right-most. When a switch is up (on), the corresponding address line is compared for "0". When the switch is down (off), the line is compared for "1".

The I/O port is similarly addressed, except that it has two 8-position switches. One is used to select address lines 0-7 while the other is used for address lines 8-15. Furthermore, the wire-wrap pins marked EXTENDED I/O should be jumpered with a shorting plug if 16-bit I/O addressing is to be used, and left open if only 8-bit addressing is needed.

If the parity I/O port is not going to be used, its address should be set to an unused I/O location to prevent interference with other I/O ports on the bus.

For the memory addressing, the user must additionally determine which 16K sections in each 64K bank are to be used. The switch with the marking "C-8-4-0-C-8-4-0" is used for this purpose. The left half of the switch is used for the high bank, with the right half for the low bank. When a



switch is on (up), the 16K section with a start address corresponding to its marking is disabled. If switch positions are left open (down)(OFF), the corresponding 16K sections are enabled. For example, if you have a 32K board which you want to place in the address range of 8000-FFFF, all switches should be up except the ones marked HIGH 8 and HIGH C. Markings on the board should aid in setting these switches. When the switch is thrown toward the "1", the section is enabled, while if it is thrown toward the "0" it is disabled.

If only half of a 64K section is being used, then you must makes sure that the memory chips are in the proper sockets for selection. If the lower 32K half is desired (offset 0-H7FFF in the section), then the chips should reside in the top row for the section. If the upper 32K half if desired (offset H8000-HFFFF in the section), the chips should be moved to the bottom row of the section.

An example of a 96K board to be addressed from H8000-H1FFFF would be to address the high bank to start at H10000, using the full 64K. The bottom half should be addressed at H0000, with the lower two 16K sections disabled. The memory chips should be moved from the third row of sockets to the bottom row.

One final note--on boards where the bottom two rows are left empty, the LOW BANK address switch should be set to an unused portion of system memory. The reason for this is that it overides the HIGH BANK switches, possibly causing problems if both sets of switches are set to the same locations.

XACK and AACK Generation

In order for the board to acknowledge processor commands, two lines are provided to indicate when a memory transfer is complete. The XACK (transfer acknoweledge) line is driven by the board when the memory transfer is completely finished, and the processor is allowed to complete the cycle. The AACK (advanced acknowledge) is provided to allow systems to operate at their full speed potential (by preventing wait states), since it can be returned before XACK. Only XACK is used to indicate when a cycle can end, with the function of AACK to give advance information concerning the timing of the board.

XACK is returned to the processor automatically when a cycle is complete. AACK can be strap selectable to return to the processor from 0-800ns after a cycle is started, in 100ns increments. The selection of timing for AACK is done with shorting plugs placed over wire-wrap pins on the board.

A row of wire-wrap pins is provided to select the AACK timing. It consists of 10 pairs of pins, with each pair being one timing combination. To setup the board, the user needs to place a shorting plug under the timing number which he desires.

The timing numbers are marked to be the maximum return time for the signal involved (multiplied by 100ns). The minimum time is 100ns below the maximum time. For example, the pins marked "4" will return AACK from 300-400ns after a cycle is started. The pins marked "0" always return the signal immediately, and the pins marked with an infinity symbol cause AACK to be disabled. The setting of the AACK strap will have to be determined by the system designer, using the information presented here.

One note--the timing for the AACK line is dependent on the CCLK (constant clock) signal from the Multibus. It is assumed here that this clock is running at 10MHz, so if any other frequency is used on the system, the spacing between strap postions will be the period of the actual clock rather than 100ns. For example, a system with a 9.5MHz CCLK signal will have 105ns strap selection spacing.

Some processor boards (not manufactured by Central Data) may require special strapping in order to use AACK. The reference manual for your processor should be consulted for further information.

Interrupt Selection

The parity error interrupt can be gated to any of the vectored interrupt lines. The selection of which interrupt line is used is made with a shorting plug placed over the corresponding set of wire-wrap pins. These pins are marked 0-7, and are located near the LOW BANK address selection switch.

If the user does not desire parity errors to generate interrupts, he must leave the shorting plug off the interrupt pins.

5. Specifications

Word Size

8 or 16 bits, determined by the Multibus BHEN line

Memory Size

32,768 bytes (32K board)
65,536 bytes (64K board)
98,304 bytes (96K board)
131,072 bytes (128K board)

Access Time

330ns maximum

Cycle Time

450ns maximum

Address Selection

Dip-switch addressing for each 64K section to reside on any 64K memory boundary in the 16 megabyte address space. Four additional switches for both sections allow disabling of any 16K within the addressed space.

16-bit dip-switch addressing is provided for the parity I/O port. Optionally, the user can use only 8-bit I/O addresses for the port.

Interface

All P1 signals meet the IEEE Multibus proposed specification. In addition, to allow the full 24-bit address bus, the following pins of P2 are defined:

Pin	Function
57	A20
58	A21
59	A22
60	A23

Electrical Characteristics

Vcc= +5V ±5%
Vdd= +12V ±5%
Vbb= -12V ±5%
Icc= 1.41A typ, 1.75A max
Idd= 0.71A typ, 0.71A max
Ibb= 0.01A typ, 0.01A max

Environmental Characteristics

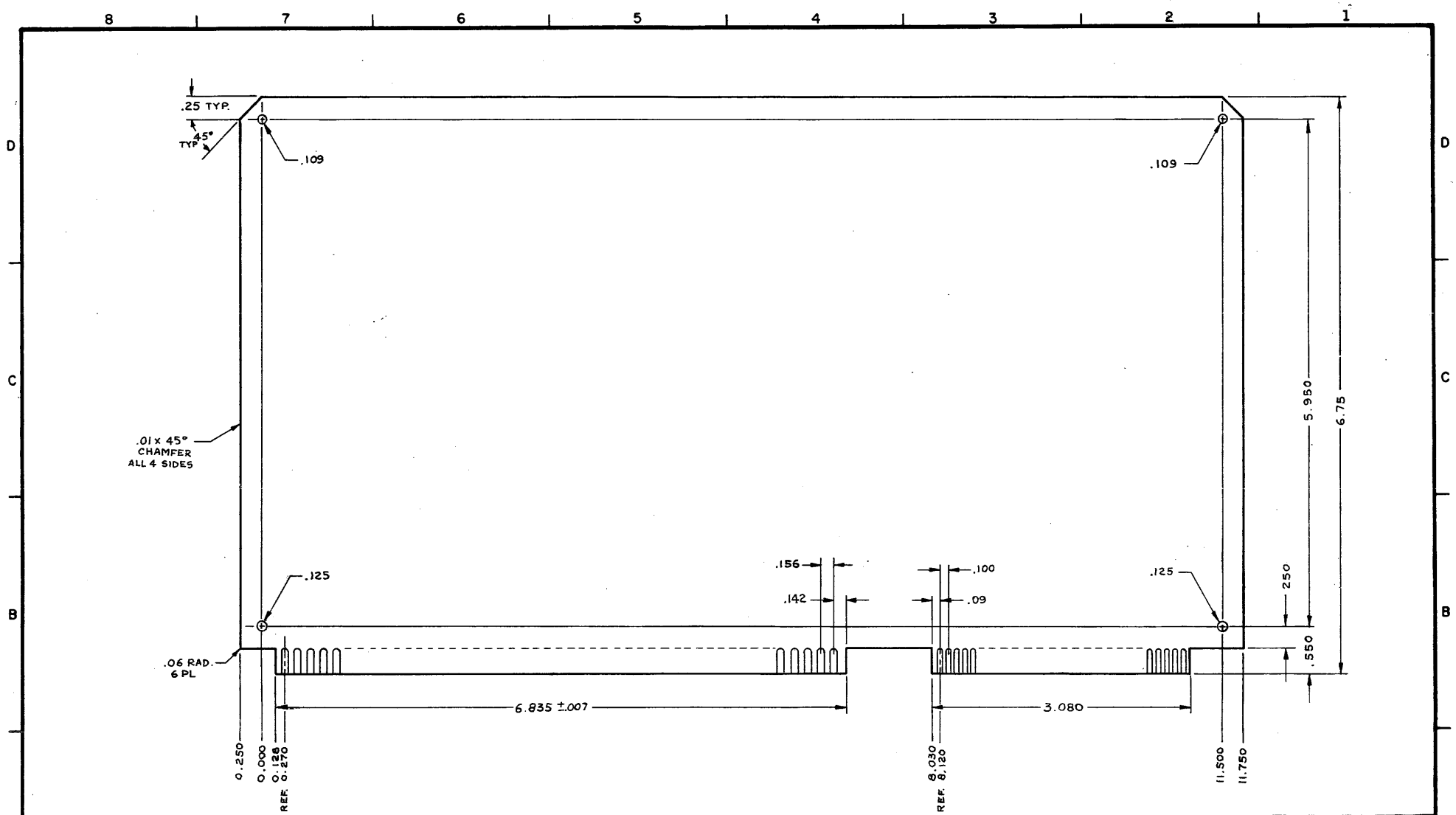
Operating Temperature: 0 C to +55 C
Relative Humidity: 0 to 90% (non-condensing)

Physical Characteristics

Dimensions: see the drawing one the following page
Weight: 16 oz (454gm)

Ordering Information

Part Number:	B1020	
Description:	Multibus Dynamic RAM Board	
Sizes:	/32K	32K size
	/64K	64K size
	/96K	96K size
	/128K	128K size
Example:	B1020/96K	Multibus 96K Dynamic RAM Board



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NO.

SHEET OF

MULTIBUS BOARD DIMENSIONS

6. Schematics

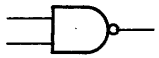
The following pages contain the schematics for the 32K-128K Dynamic RAM board. A full description of the circuitry is given in the Principles of Operation section of this manual.

3-INPUT 'AND' GATE

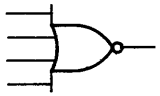
2-INPUT 'OR' GATE

INVERTER

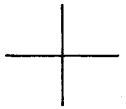
2-INPUT 'NAND' GATE



4-INPUT 'NOR' GATE

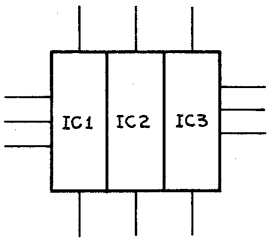


TWO LINES - NO CONNECTION

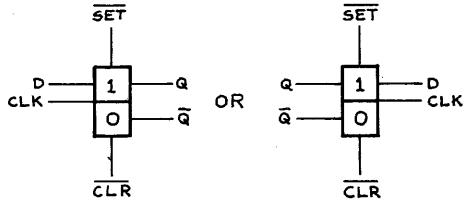


3 LINES - ALL CONNECTED

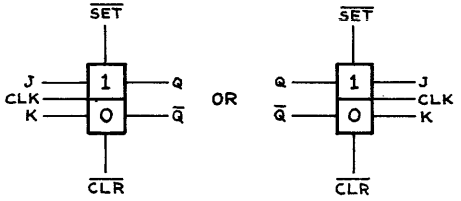
GROUP OF SIMILAR PARTS



D-TYPE FLIP-FLOP



J/K FLIP-FLOP



UNMARKED ARROWS GO TO +5V

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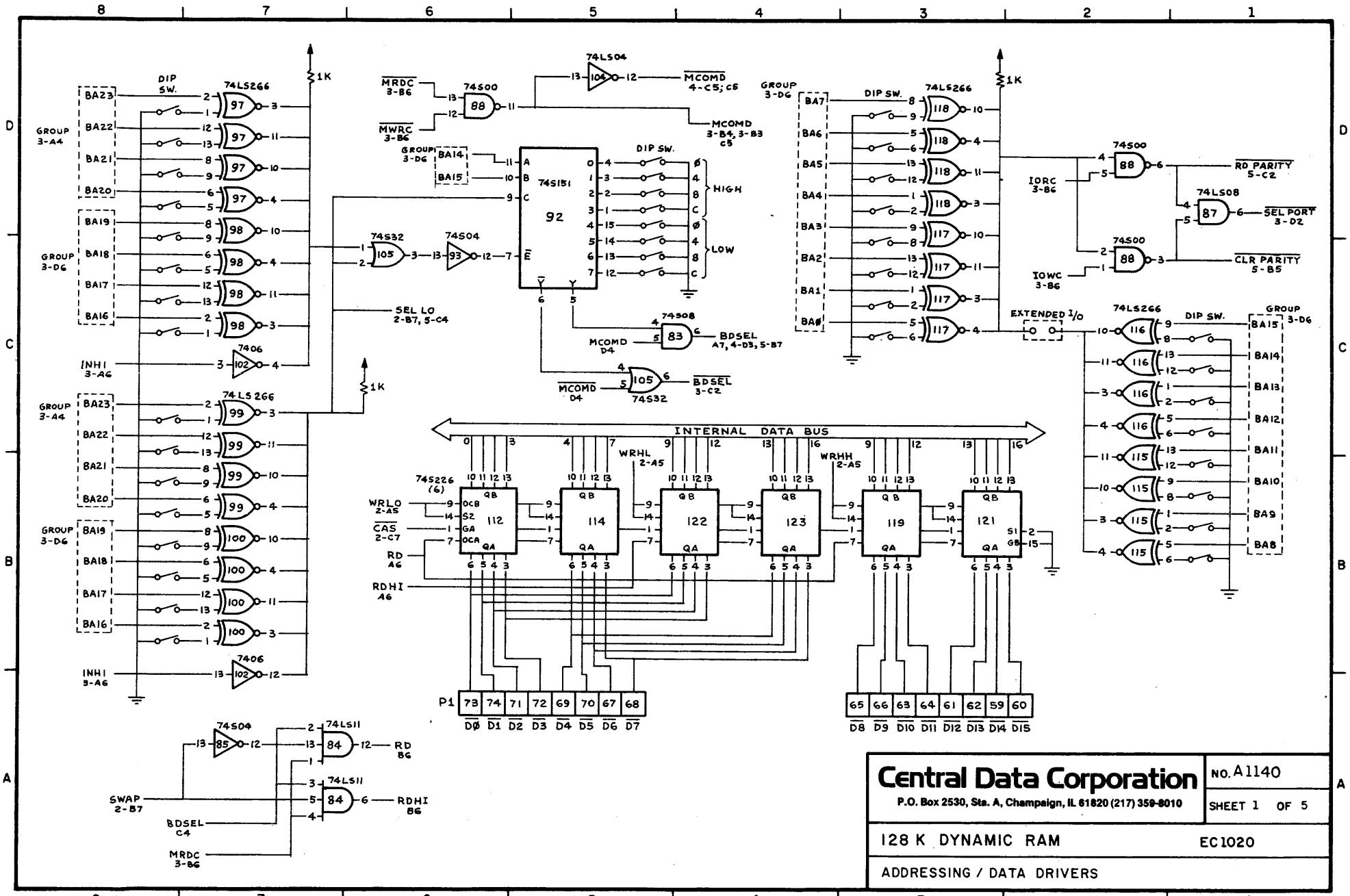
DRAWING CONVENTIONS	



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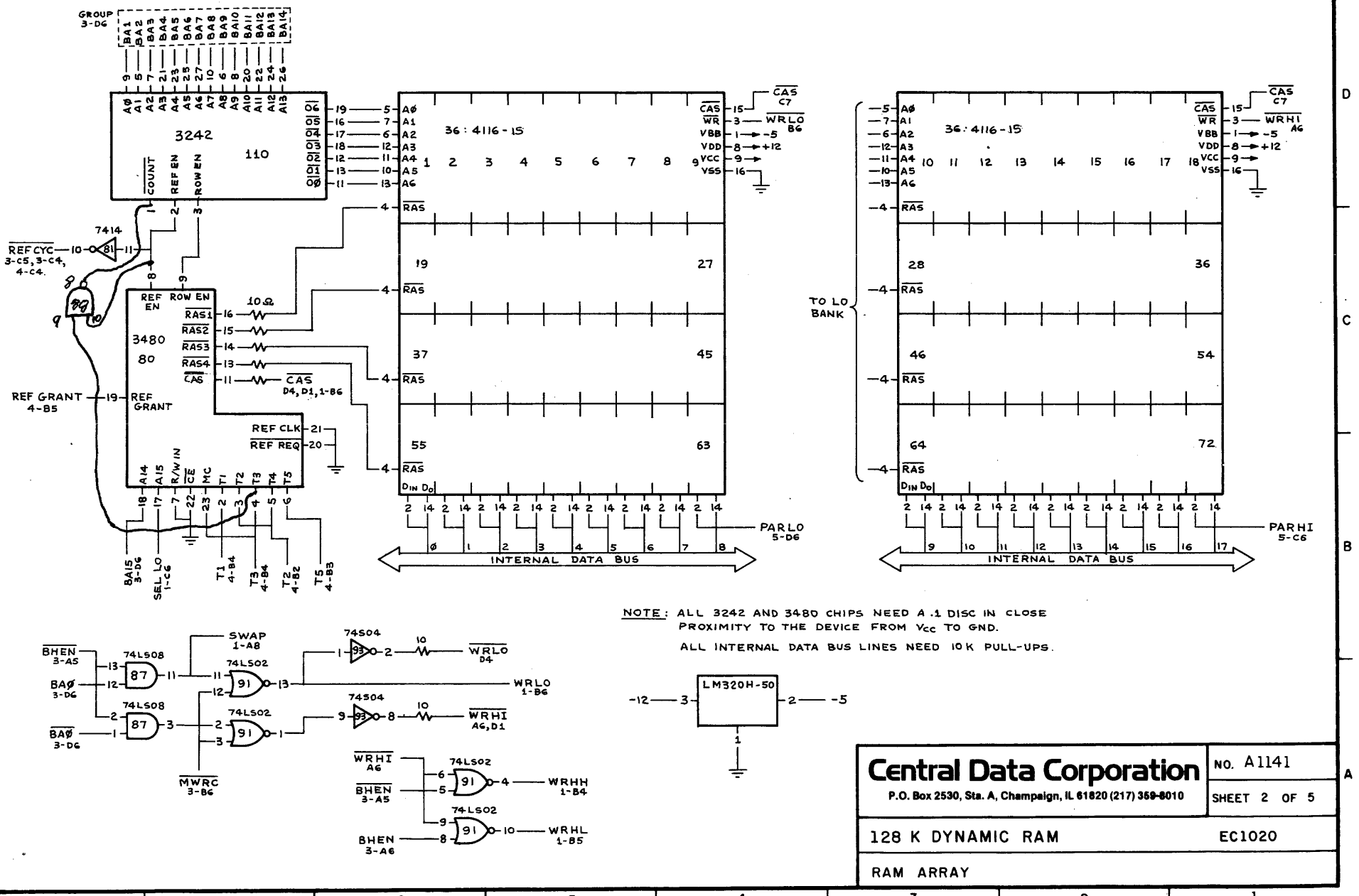
NO. A1140
SHEET 1 OF 5

128 K DYNAMIC RAM EC1020

ADDRESSING / DATA DRIVERS



NOTE: ALL 3242 AND 3480 CHIPS NEED A .1 DISC IN CLOSE PROXIMITY TO THE DEVICE FROM V_{CC} TO GND.

ALL INTERNAL DATA BUS LINES NEED 10K PULL-UPS.

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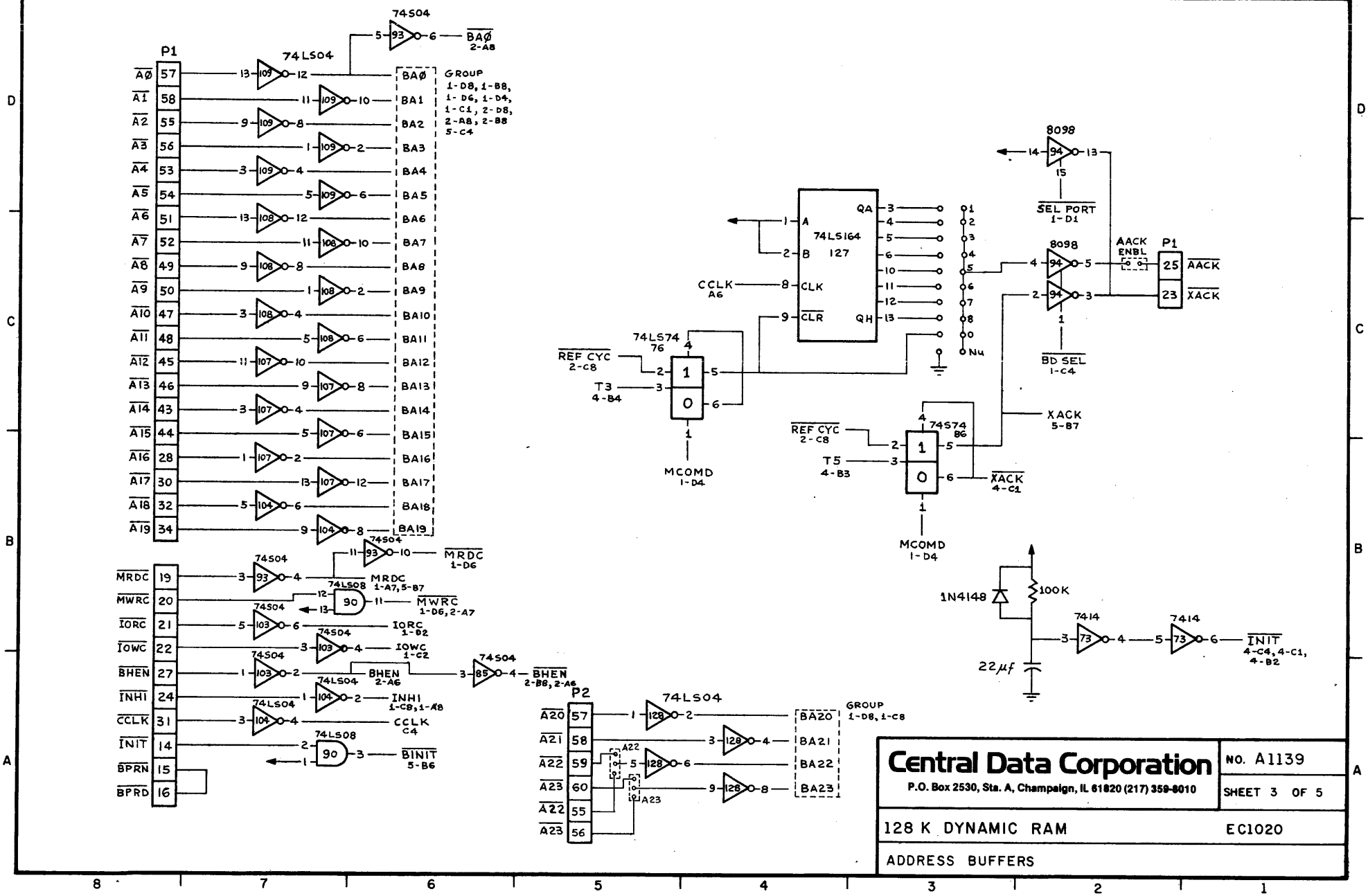
NO. A1141

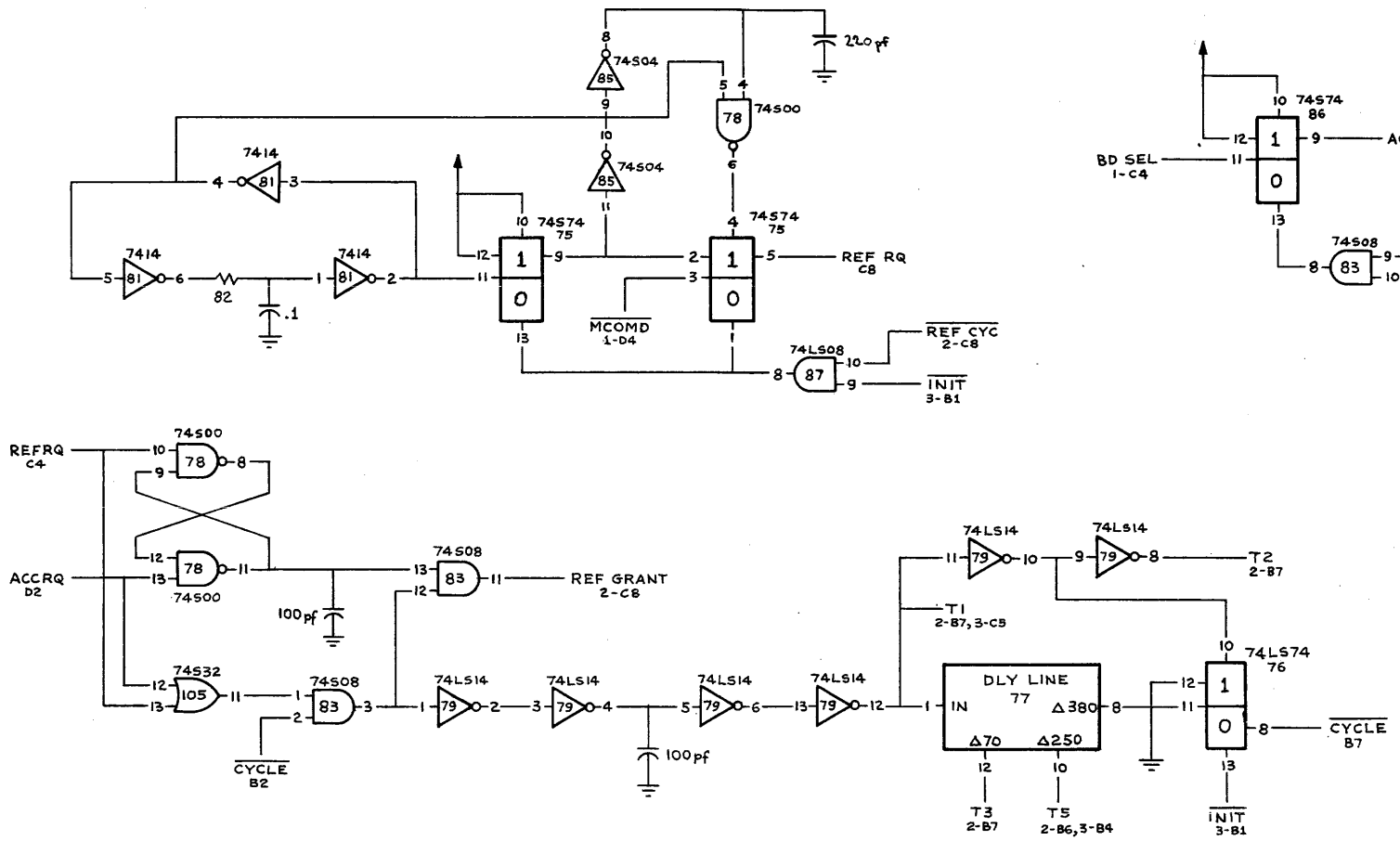
SHEET 2 OF 5

128 K DYNAMIC RAM EC1020

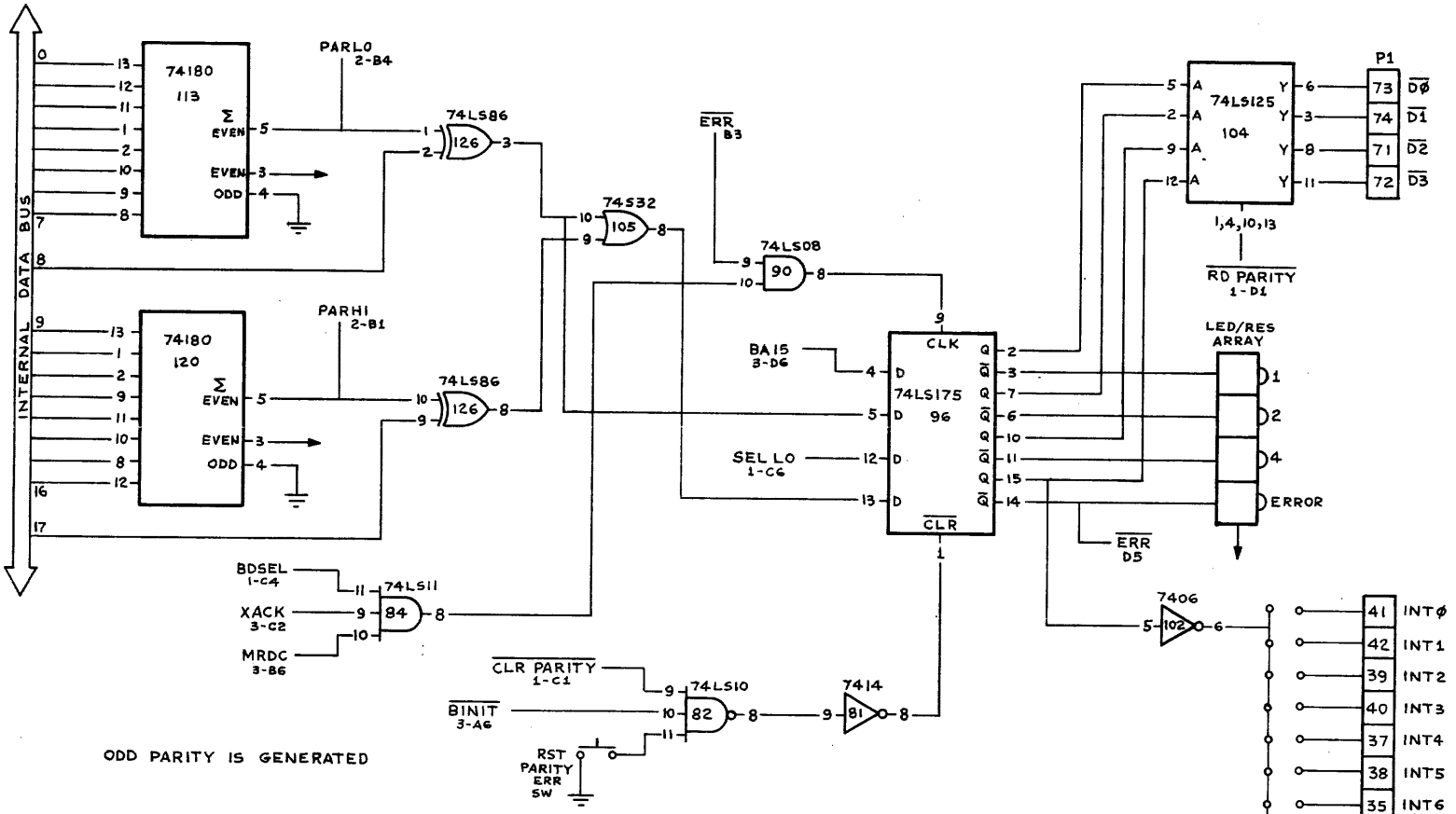
RAM ARRAY



Central Data Corporation	NO. A1139
P.O. Box 2530, Sta. A, Champaign, IL 61820 (217) 359-8010	SHEET 3 OF 5
128 K DYNAMIC RAM	EC1020
ADDRESS BUFFERS	



Central Data Corporation	NO. A1138
P.O. Box 2530, Sta. A, Champaign, IL 61820 (217) 359-8010	SHEET 4 OF 5
128 K DYNAMIC RAM	EC1020
CONTROL LOGIC	



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128 K DYNAMIC RAM	EC1020
PARITY CHECKING	

Central Data Corporation

Engineering Change Order

Product 128K Dynamic RAM Board

Number 1026

Part Number B1020

Previous No. 1020

Date 11/11/81 Approved J. Rodgers

- FOR INFORMATION ONLY
- NO CHANGE REQUIRED BY USER

Parts List Changes:

+1: 11-10410-105 .1 Capacitor

Manufacturing Specification Changes:

See attached sheet

Testing Specification Changes:

None

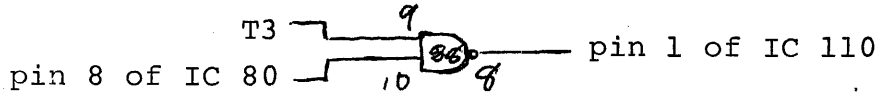
Description of Problem/Solution or Improvement:

3480 timing changed to meet data sheet exactly. Previous design met data sheet specs, but apparently the device prefers new timing.

Also, additional grounds decreased noise levels on the board.

Schematic Changes:

Drive pin 1 of IC 110 as follows:



Manufacturing Changes for ECO1026:

1) Cut trace leading to pin 1 of IC 110 on the top of the board.

2) Cut trace between pins 1 & 2 of IC 110 on the solder side.

3) Add .1 capacitor between pins 12 and 24 of IC 80.

4) Place a 26ga jumper from the ground hole above pins 82 and 84 of P1 to the feed thru above pins 24 and 25 of IC 110.

5) Place a 26ga jumper from the ground feed thru right of pin 1 of IC 83 to the feed thru left of pin 12 of IC80.

6) Install the following normal jumpers:

   a) pin 10 of IC 88 to feed thru ¼" above pin 11 of IC 85.
   b) pin 2 of IC 110 to feed thru 9/16" above pin 28 of IC 110.
   c) pin 9 of IC 88 to pin 4 of IC 80.
   d) pin 8 of IC 88 to pin 1 of IC 110.