48935300

CONTROL DATA
CORPORATION

CONTROL DATA®
CJ122 PAGE AND DOCUMENT READER CONTROLLER

Models E,G,H, and K

GENERAL DESCRIPTION
OPERATOR CONTROLS
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA
WIRE LISTS

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

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Address comments concerning this manual to:
Control Data Corporation
Washington Area Operations
1455 Research Boulevard
Rockville, Maryland 20850
or use Comment Sheet in the back of this manual.

PREFACE

This manual contains information necessary to install and maintain the CONTROL DATA® (CJ122) Page and Document Reader Controller and the DT213 Coupler, both of which are used with the CJ122 Page and Document Reader. Detailed information (diagrams, parts data, wire lists, and so on) for the buffer controller, normal channels, and storage module is not included in this manual, but may be found in the publications listed below. Other manuals which must be used in conjunction with the controller are also listed below.

- 955 Page and Document Reader Controller Reference Manual 60324600
- 955 Page and Document Reader OCR Media Manual 60216102
- 955 Page and Document Reader Controls and Indicators OCR Software Operator's Guide 48643305
- CJ122 Page and Document Reader Hardware Reference/Customer Engineering Manual 48430080
- FR113-A Buffer Controller Reference/Customer Engineering Manual 60335400
- BB372-A Customer Engineering Manual 60346500
- Buffer Controller Maintenance Console Customer Engineering Manual 58032700

Refer to the current Literature Distribution Services Catalog for the latest revision level for each of the above manuals.

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SECTION 1

GENERAL DESCRIPTION

GENERAL

The Control Data CJ122 Page and Document Reader Controller contains the control logic for the Control Data CJ122 (955) Page and Document Reader. The CJ122 is a multipurpose optical character recognition (OCR) peripheral device designed for business data processing (see Figure 1-1). The reader scans and optically reads printed pages and documents and is designed to handle a variety of form layouts and document sizes. It is a high-resolution optics reader capable of reading degraded or distorted print, unevenly spaced, unevenly printed and poorly inked impressions. The basic reader reads a subset of the American National Standards Institute (ANSI), Size A character set. Certain optional equipment, adaptable to the reader, enable it to read a number of other fonts, including handprint. The controller is a part of the CJ122 and after S/N 151 it is no longer identified as a separate equipment.

CONTROLLER

The controller consists of several component subassemblies contained within a common controller module attached to the reader. The following subassemblies are contained within the controller module.

FR113-A Buffer Controller (BC)
DT213 - 1700 A/Q Coupler (coupler)
DT156 - TTL Normal Output Half-channel
DT157 - TTL Normal Input Half-channel
BB372-A Storage Module
FV444-A Power Regulator Module
Power Supply
Switch Panel

PHYSICAL DESCRIPTION

The controller, power supply, feed-up table, and cooling fans are housed in the controller module which is bolted to the right-hand end of the reader module when the reader is assembled at the customer site. The BC, coupler, I/O channels, storage module, power regulator module, and a switch panel occupy space in the rear of the controller module. Figure 1-2 is a pictorial view of the physical arrangements for these units. The controller module is hinge-mounted to swing out for easy access to the back panel wiring when the rear skins are removed. Two fans located directly under the controller module and one fan located in the upper center section of the extreme right-hand controller panel provide cooling. The power supplies are hinge-mounted to the front of the controller module (observable with the front skins removed).

FUNCTIONAL DESCRIPTION

BUFFER CONTROLLER

The BC is an internally programmable, parallel mode control element. It can be used as an operating controller for peripheral equipment and it could also serve as a processor in a terminal or station environment. A special control program, reflecting the needs of the environment, is stored in a storage module to determine the BC function in its environment. (For more detailed discussion refer to Pub. No. 60335400.)

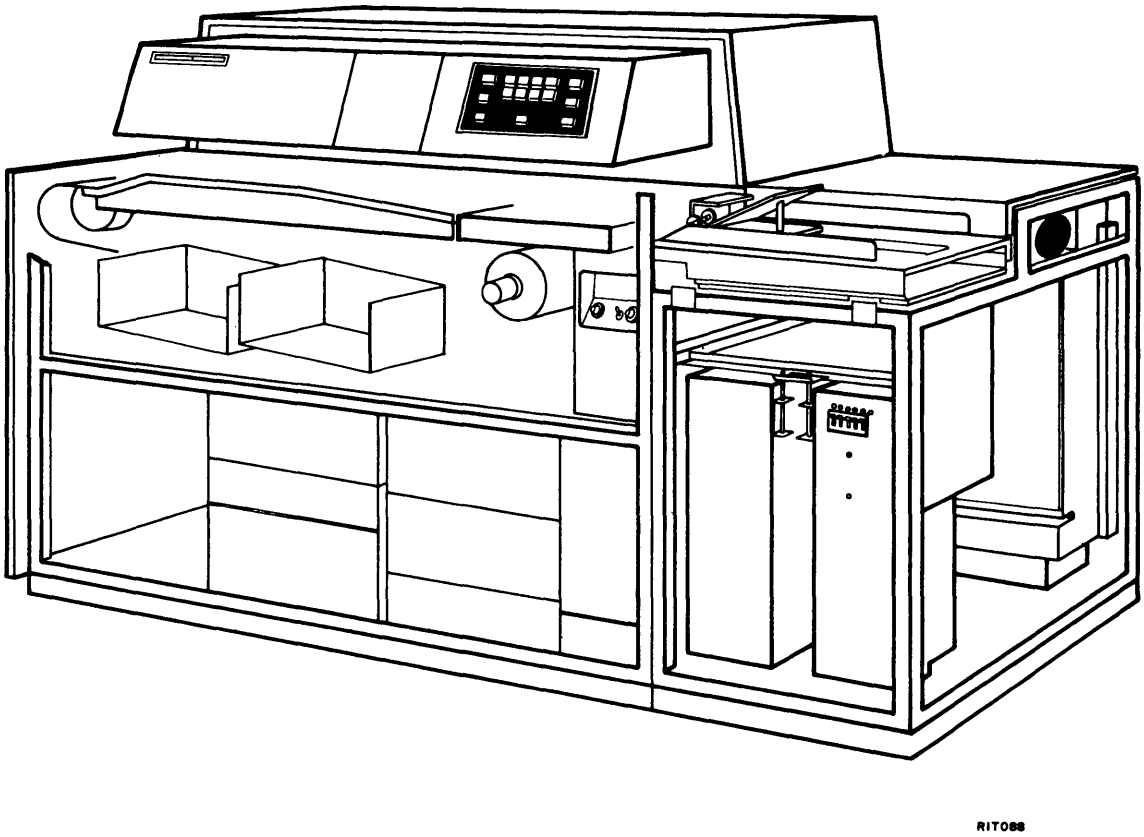


Figure 1-1. 955 Page and Document Reader

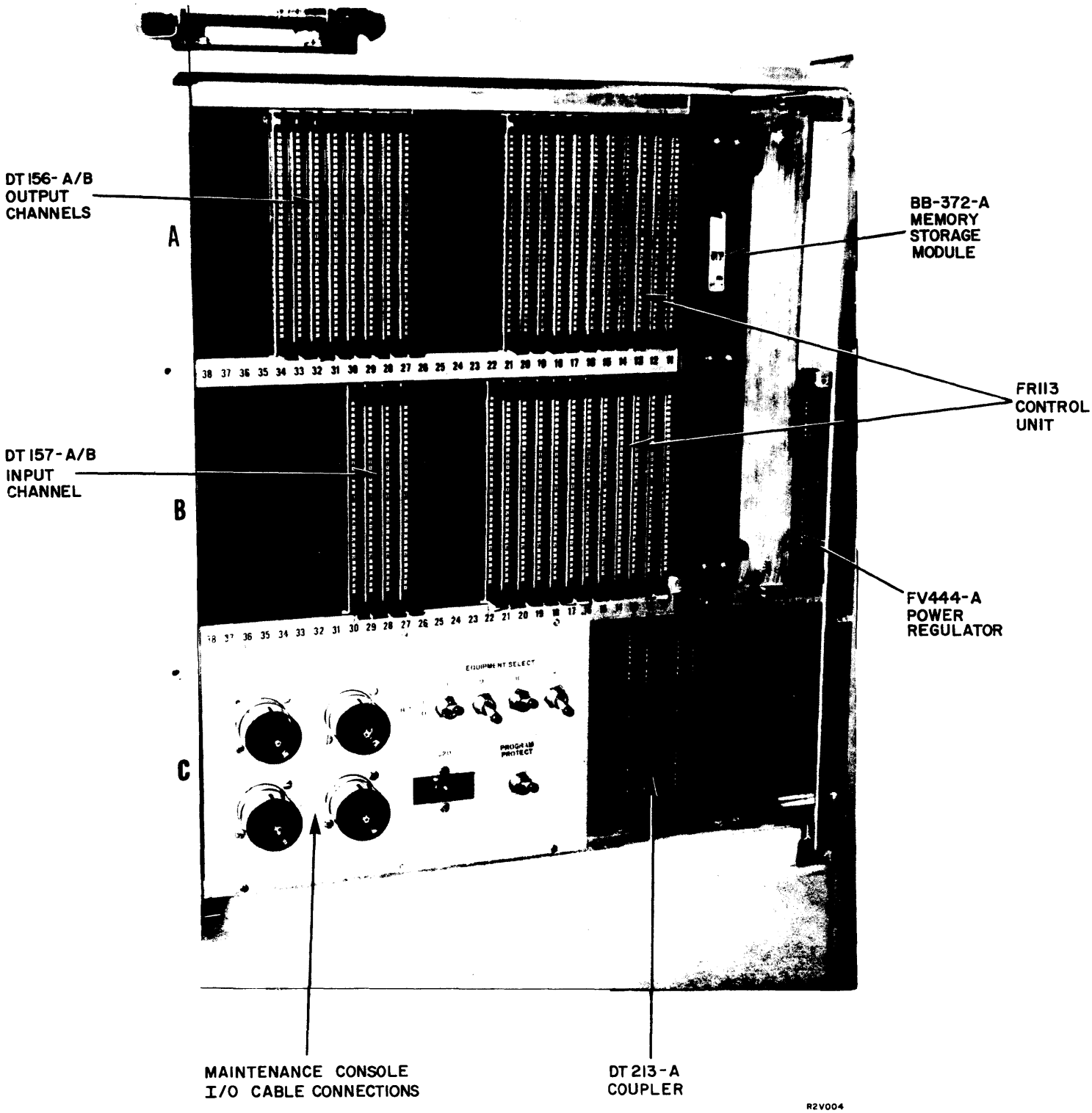


Figure 1-2. Controller Module (Rear Skins Removed)

COUPLER

The coupler provides the controller with an interface to the BC and the 1700 computer. Primary function of the coupler is to permit the use of normal channels for addressing and transfer of status data and the block transfer channels for parameter and read data. The coupler may be connected to either the A/Q channel or a 1706 buffered data channel. The coupler consists of 5-25 PAKS of TTL logic and is connected through the controller back panel.

The normal output channels consist of TTL logic on DT156-A 25 PAKS. Each 25-PAK contains two output half channels. Eight DT156-A PAKS are used to provide 128 buffered output lines. (For more detailed discussion refer to Pub. No. 60335400, Appendix A.)

The normal input channels consist of TTL logic on DT157-A/B 25-PAKS. Each 25-PAK provides fan-ins of 32 input signals to the BC. The 32 input signals are arranged as four half channels and four DT157-A/B 25-PAKS are used to provide 128 nonbuffered input lines. The input channels supply no storage and signals to the controller are directly dependent on the status of the input. (For more detailed discussion refer to Pub. No. 60335400, Appendix A.)

STORAGE MODULE

The storage module provides load, store, and load-modify-store capability for 4096, 18-bit words. The module has a 12-bit address register and an 18-bit data input and data output register. Read access time is about 1.1 μsec. The storage module is connected to the BC through standard 25 PAK wire wrap blocks. The power regulator module provides regulated voltages for the memory circuits. (For more detailed discussion refer to Pub. No. 60346500.)

POWER SUPPLIES

The controller power supply converts a 3-phase, 220-volt input into five direct current low voltages used throughout the controller module and the reader. Low voltage DC sources are +5 vdc, -5 vdc, +6 vdc, -6 vdc, and +30 vdc.

SWITCH PANEL

The switch panel provides four 61-pin connectors for use at the TF201 Maintenance Console and operator control switches for use during installation, check out, and maintenance. The switches consist of four equipment code selects and a program protect.

POWER REQUIREMENTS

1. Input power - 3-phase, 220 vac, 5 amps per phase

2. Low-voltage dc - +6 vdc, 1.3 amps
   -6 vdc, 1.1 amps
   +5 vdc, 14 amps
   -5 vdc 0.1 amp
   +30 vdc, 2.0 amps

SECTION 2

OPERATOR CONTROLS

Turn-on procedures, operating procedures, and adjustment procedures for the operator control panel, the document adjustment panel, the journal tape control panel, and feeder instructions are explained in the CJ122 Page and Document Reader Controller Reference Manual. The controller switch panel controls and indicators are explained below. For switch panel indicators and switch locations refer to Figure 2-1.

EQUIPMENT SELECT switches	Allow selections of any one of 16 equipment codes (hexadecimal 0 through F). The controller will be selected when the equipment code generated by the 1700 computer matches the setting of these switches.
PROGRAM PROTECT switch	Applies the "protected" condition in which the controller accepts only instructions that are accompanied by a logic "1" on the protect line.
End of Operation (EOPCC) (maintenance use only)	Clears auto-load condition. With power up, push to enable access to all registers.
J01 through J04	Provides cable connections for the TF201 Maintenance Console during maintenance operations.

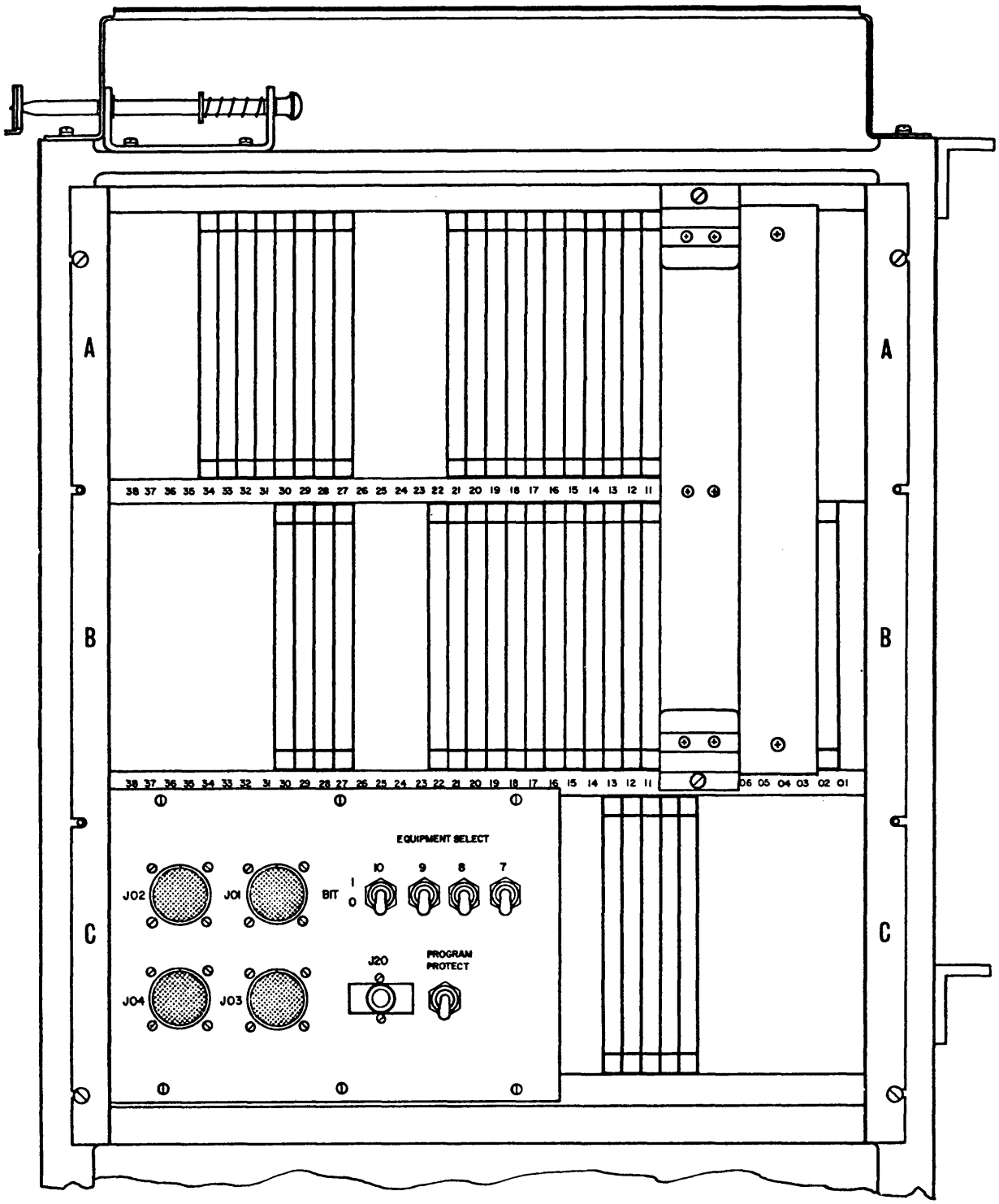


Figure 2-1. Switch Panel (Rear Skins Removed)

SECTION 3

INSTALLATION AND CHECKOUT

Section 3 contains a cabling diagram (Figure 3-1), instructions for connecting the controller to other equipments and interface connections. In addition, certain voltage check instructions are provided. For site preparation requirements, reader installation procedures, reader checkout procedures, crating and uncrating instructions, refer to the CJ122 Page and Document Reader Hardware Reference/Customer Engineering Manual (Pub. No. 48430080).

CABLING INSTALLATION

Install controller cables according to the following procedures.

1. After the controller module has been leveled and bolted to the reader module (with skins removed) unlatch the controller and swing it out for easy access to the back panel connectors.

2. Connect reader cables to connectors J12 through J18.

3. If used, connect buffer controller TF201 Maintenance Console I/O cables to connectors J01 through J04 (TTL modification kit, Part No. 59309500, must be installed in the TF201 Maintenance Console).

4. Connect the 1700 A/Q cables to connectors J06 and J08. Connect the 1700 interrupt cable to J21; install terminator assemblies or Daisy Chain 1700 A/Q cables on connectors J05 and J07.

5. Connect 3-phase regulator power supply to the power leads from the power control panel in the reader. Ensure that connections between the regulator and the dc power supplies are secure.

NOTE

Prior to performing the voltage checks, the reader must be in the maintenance mode and bypassed. (Refer to the hardware reference manual, Pub. No. 48430080.)

VOLTAGE CHECKS

1. Set the following circuit breakers on the reader power control panel to on:

Main circuit breaker	Power-up circuit breaker
System regulator circuit breaker	Buffer controller supply circuit breaker

2. Momentarily press the power enable, then the controller power pushbutton indicators on either the maintenance panel or the operator control panel.

3. Verify controller voltage levels at the controller power supply test jacks.

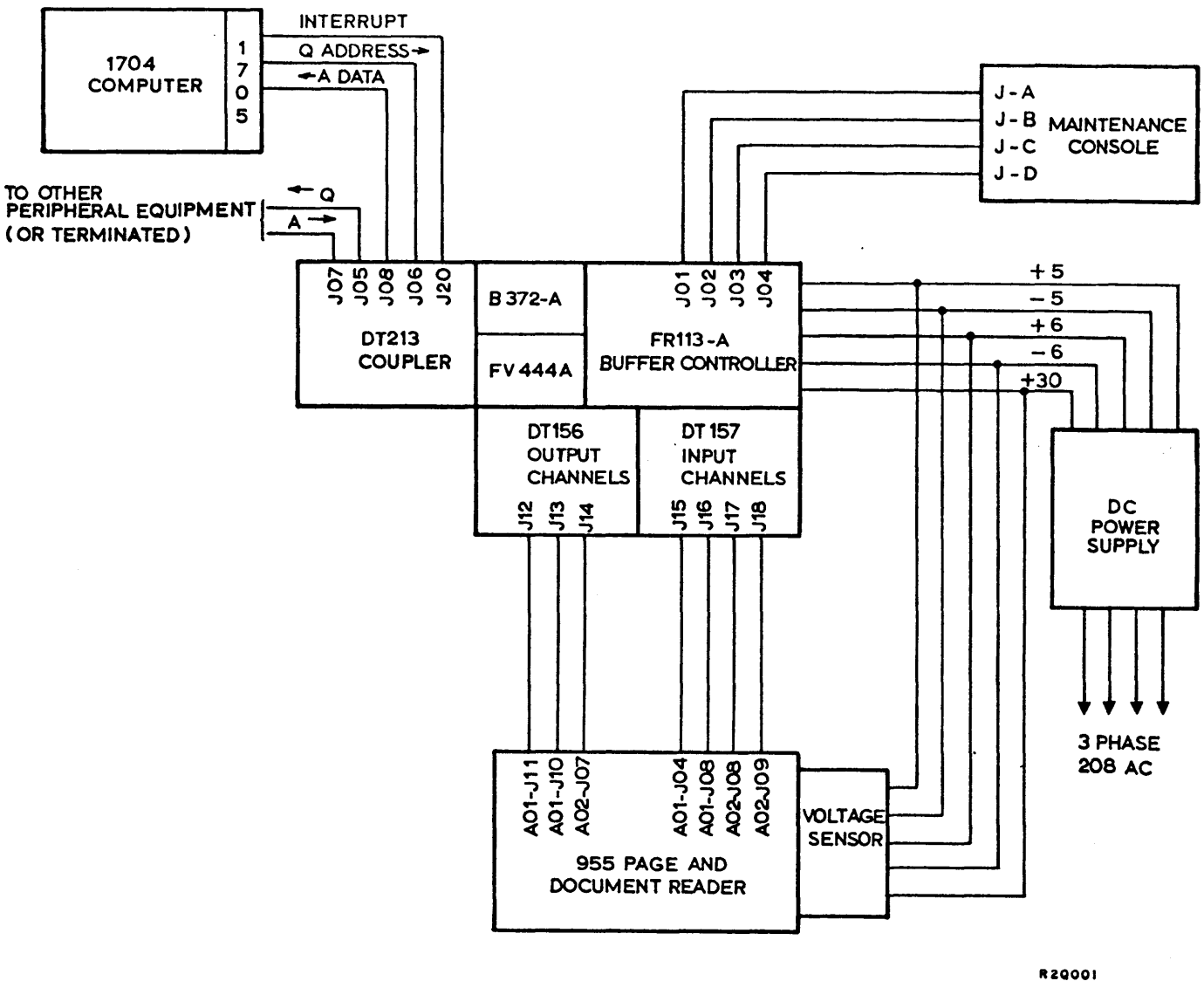


Figure 3-1. Cabling Diagram

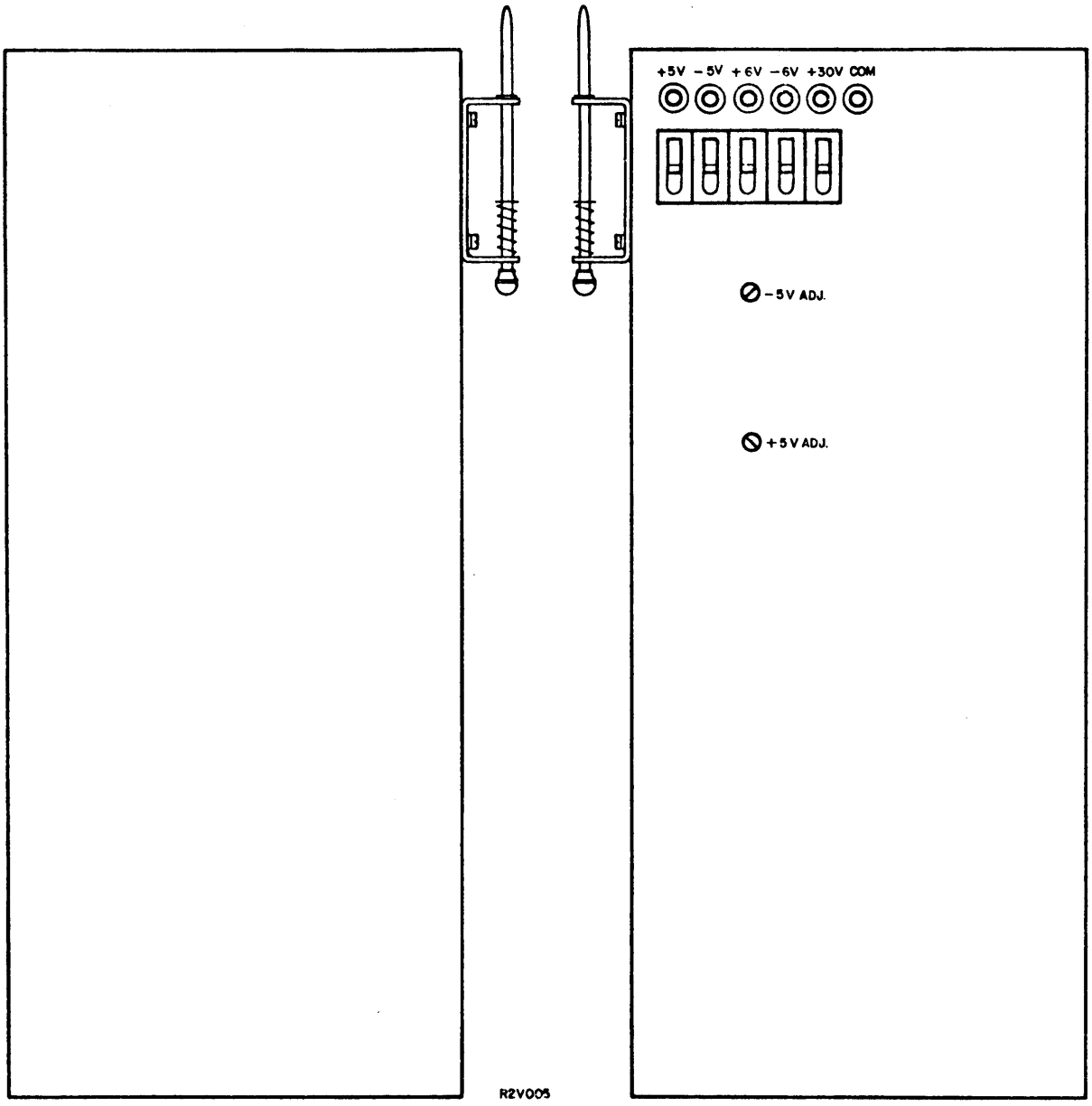


Figure 3-2. Power Supplies

SECTION 4

THEORY OF OPERATION

BUFFER CONTROLLER

The BC is an internally programmable, parallel mode control element which accepts and transmits information through four interfaces. Internally, it contains a control section and an arithmetic section. The BC has no internal memory. The storage interface provides the BC with access to a storage module which has the control stored in 4K of core memory. Interface also provides block transfer capability for communication with the 1700 A/Q coupler which interfaces with the 1700 computer. A normal channel interface provides a means through which the BC maintenance console communicates with the BC during installation, checkout, and maintenance. Refer to Figure 4-1 for interface connections. (For more detailed discussion of the BC refer to Pub. No. 60335400.)

NORMAL CHANNELS/INTERFACE

The normal I/O channels provide the communication links for the BC. Normal channel logic does not provide "Ready/Resume" flags. Dedicated program controlled normal channel lines must be used when "Ready/Resume" operation is required. The coupler uses the normal channels to receive and transmit signals of +3.50 volts for a logic "1" and +0.20 volts for a logic "0" to and from the BC. Status, buffered through the normal channels for transmission to the computer, is controlled by this gating logic. The normal channel output utilizes two 16-bit channels to present output data from the BC to the coupler. The two channels are used for system and transport status with bits being set or cleared by BC software control on an event basis. The coupler utilizes one 16-bit input channel to transfer coupler status to the BC. The channel bits are set asynchronously on an event basis at the coupler and are cleared by the input data or by bit direction controlled by the BC software. (For more detailed discussion of the normal channels refer to Pub. No. 60335400, Appendix A.)

STORAGE AND POWER REGULATOR MODULES

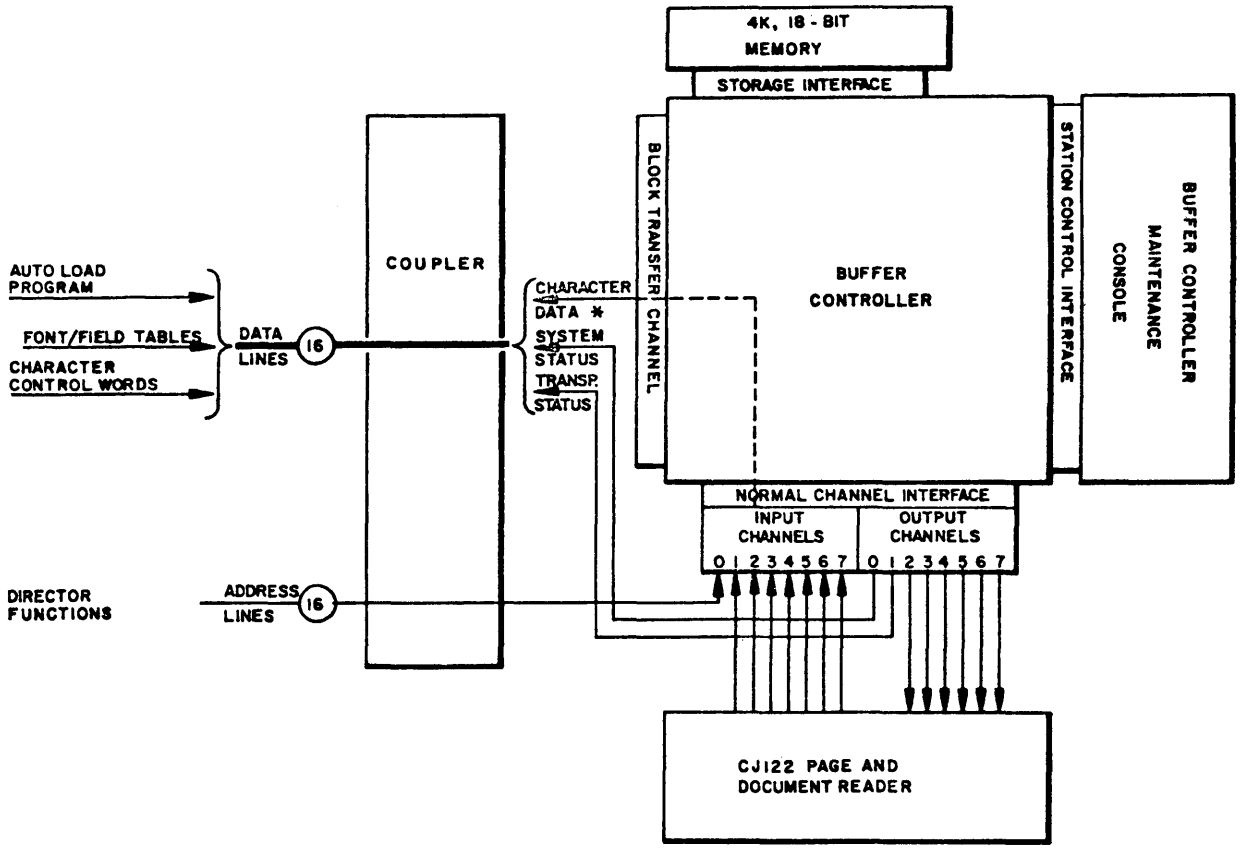
The storage module serves as the "internal" memory for the BC and provides the control logic. The power regulator module regulates the current and voltage utilized by the storage module core and logic circuits. (For complete detailed discussion of both modules refer to Pub. No. 60346500.)

1700 AQ/DT213 COUPLER INTERFACE

The coupler serves as the interface between the 1700 computer and the BC. Communications between the coupler and the 1700 are defined as control signals in the following manner.

READ/WRITE

The read/write signals utilize 16 bi-directional lines between the coupler and the computer A register. Upon a read/write request initiated by the computer, the coupler sends a reply within 1.2 microseconds if read data is available or if write data can be used. A reject signal is sent to the computer in 1.2 microseconds if read data is not available or if the write data cannot be used.



* FOR MAINTENANCE PURPOSES, SERVO DATA AND CHARACTER VOLTAGES CAN ALSO BE TRANSMITTED TO THE COMPUTER.

Figure 4-1. Controller Interfaces

PROGRAM PROTECT

Any instructions requiring access to a protected device will receive a reject signal unless it is accompanied by a discrete program protect signal which allows the instructions to be gated to the protected device.

ADDRESSING

The Q register in the computer utilizes 16 lines from the computer to specify the W, E and D addressing codes sent to the coupler. For the BC, Converter (W) must equal zero and is preset whenever bits 11, 12, 13, 14, and 15 of the address in the Q register are all zero. Equipment (E), address bits 7 through 10 contain the equipment number of the peripheral equipments or the channel (hexadecimal 0 through F). When the switch panel equipment number setting and the code in (E) match, the coupler responds.

COMMAND CODE (D)

Bits 0 through 3 of the Q register are the director bits and are available to meet specific requirements of the coupler and the controller. Information on the data cables are controlled and directed by these bits to specify the data transfer, direct the control functions and function level, direct the status and status level and to direct autoload function and data.

AUTOLOAD CODE

Bit 0 and Bit 3 of the Q register are available to control and direct information on the data cables to specify and prepare for autoload and transfer autoload data.

DATA TRANSFER

To transfer data, all bits of the director must equal "0". If the coupler can send or receive data to the 1700 computer channel, it will send a reply. If the coupler cannot send or receive data, it will send a Reject signal. A Reject will always be sent if the device is Not Ready or Not Busy.

INTERRUPT SIGNALS

Three types of interrupt signals may occur. Interrupt on data requests are set and cleared by director function codes. On a read operation, the interrupt occurs when the data has been loaded into the Data Hold register and is ready for transfer. On a write operation, the interrupt occurs when data can be loaded into the data hold register of the coupler. Either read or write interrupt response is cleared by the reply to data transfer. A status bit indicates the condition of the interrupt and a clear interrupt code will terminate data transfer. Interrupt on End of Operation requests are also sequentially cleared and set by the director function code. A status bit will indicate the condition of the interrupt. The interrupt cannot occur from an operation which has ended before the selection was made. However, the operation may or may not be in progress at the time of selection. An interrupt is cleared by the clearing of an interrupt request. Interrupt on Alarm is also controlled by the director function code which sequentially clears and sets the interrupt requests. Again, the interrupt is cleared by clearing the interrupt request. However, the alarm condition must be defined by each peripheral device and a status bit indicates the state of each alarm condition. Interrupt hardware is initiated when an interrupt places a logical 1 on the interrupt transmission cable. A signal cable carries the BC system interrupt to the 1705.

FR113 BUFFER CONTROL/DT213 COUPLER INTERFACE

NOTE

In the following descriptions, a pulse is considered to be from 35 to 65 nanoseconds wide.

The coupler interface consists of 43 single-ended TTL signals. The standard set of interface signals is described below. When additional control and status signals are required for a coupler, they may be wired through normal I/O channels.

During output block transfers, the leading edge of the output ready pulse indicates that controller storage data is ready for transfer. During input block transfers, the leading edge of the input request pulse indicates that the controller is prepared to store a data word from the coupler. A steady "1" on the ready line indicates to the controller that the coupler is able to provide an immediate response to a block transfer instruction. A "0" on this line indicates that the coupler is not able to provide an immediate response and initiation of a block transfer function will cause an immediate exit.

The leading edge of the reply pulse indicates to the controller that output data has been accepted by the coupler or that input data is available from the coupler. This signal occurs only in response to controller output ready or input request signals. The coupler issues a terminate pulse in place of a reply to halt data transfer and cause an exit from a block transfer instruction.

Input data lines carry input words from the coupler. Data transfers start at the leading edge of the reply pulse and end a maximum 600 nanoseconds later. Output data lines carry output data from the controller along with two parity bits. The leading edge of an output ready pulse indicates that the data is stable. Output data remains stable until at least 600 nanoseconds after the controller receives a reply or terminate signal. The master clear pulse for clearing registers and controls within the coupler is not originated by the BC, but is received and repeated by the central section for transmission to the coupler.

I/O CHANNEL PIN ASSIGNMENTS

The buffer controller controls the reader operation by monitoring data on the TTL normal input channels and by outputting data on the TTL normal output channels. Table 4-1 depicts signal and pin assignments for the 1700 I/O channel cables, Table 4-3 depicts the block transfer channel pin assignments, and Tables 4-4 and 4-5 provide a list of the input and output channel pin assignments for the interconnecting cables. The internal control signal connectors are hardwired through the back panel wiring and are shown in Table 4-2.

TABLE 4-1. SIGNAL AND PIN ASSIGNMENTS
1700 I/O CHANNEL CABLES

DATA CABLE SIGNAL	PIN	ADDRESS CABLE SIGNAL
Data Bit 00	A1, 2	Address Bit 00
01	3, 4	01
02	5, 6	02
03	7, 8	03
04	9, 10	04
05	B1, 2	05
06	3, 4	06
07	5, 6	07
08 To/From	7, 8	08
09	9, 10	09
10	C1, 2	10
11	3, 4	11
12	5, 6	12
13	7, 8	13
14	9, 10	14
15	D1, 2	15
Reply	3, 4	Read
Reject	5, 6	Write
Character Input*	7, 8	Master Clear
Priority*	9, 10	Program Protect
	E1, 2	Buffer Active*
	3, 4	Timing Pulse*
	5, 6	Spare
	7, 8	Spare
{Not Defined}	9, 10	{Not Defined}
	F1, 2	{Not Defined}
	3, 4	{Not Defined}
	5, 6	{Not Defined}
	7, 8	W = 0
Termination Power	9, 10	Termination Power
*Not Used		

TABLE 4-2. PLUGGABLE AND BLOCK TRANSFER CONTROL SIGNALS

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL CH. IN	CHANNEL NORMAL CH. OUT	CHANNEL BLOCK TRFR. IN	CHANNEL BLOCK TRFR. OUT	OTHER	COUPLER PIN NO.
Not Go	$\overline{GO}$					C27-A01	C11-A24
Not Stop	$\overline{STOP}$					C27-B01	C13-B29
Not Master Clear	$\overline{MC}$					C27-B02	C11-B09
Parity Error Clear	$\overline{CLRPE2}$					C27-A05	C13-B17
Parity Error	PE-ID					C27-A06	C13-A30
Clear Channel	$\overline{CLRCH2}$					C27-B04	C13-B30
Not Force Function	$\overline{FORCEF}$					C27-A03	C13-B18
Force Function Select	EN-OUT					C27-B03	Ground C13-B11
End of Block Transfer Status	EOP-CC					C27-B03	C13-B27
			BLOCK TRANSFER CONTROLS				
Output Ready	OUTRDY					C28-A01	C13-A05
Input Request	INPREQ					C28-B01	C13-B04
Master Clear	MC-CC					C28-A04	C13-A18
Ready	CREADY					C28-B02	C13-A04
Reply	CREPLY					C28-A03	C13-B06
Terminate	CCTERM					C28-B03	C13-A06

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL CH. IN	CHANNEL NORMAL CH. OUT	CHANNEL OTHER IN	CHANNEL OTHER OUT	COUPLER INTERFACE CONNECTOR IN	COUPLER PIN NO.
Coupler Input Data Bit 2^{15}	CCI-00			B18-A22	C09-B14	C28-A05	C09-B14
Coupler Input Data Bit 2^{14}	CCI-01			B18-B22	C10-B14	-A06	C10-B14
Coupler Input Data Bit 2^{13}	CCI-02			B18-A21	C09-B13	-A07	C09-B13
Coupler Input Data Bit 2^{12}	CCI-03			B18-A20	C10-B13	-08	C10-B13
Coupler Input Data Bit 2^{11}	CCI-04			B18-A24	C09-A15	-A09	C09-A15
Coupler Input Data Bit 2^{10}	CCI-05			B18-B24	C10-A15	-A10	C10-A15
Coupler Input Data Bit 2^{9}	CCI-06			B18-A23	C09-B15	-A12	C09-B15
Coupler Input Data Bit 2^{8}	CCI-07			B18-B23	C10-B15	-A13	C10-B15
Coupler Input Data Bit 2^{7}	CCI-08			B17-A22	C09-A13	-A14	C09-A13
Coupler Input Data Bit 2^{6}	CCI-09			B17-B22	C10-A13	-A15	C10-A13
Coupler Input Data Bit 2^{5}	CCI-10			B17-A21	C09-A14	-A16	C09-A14
Coupler Input Data Bit 2^{4}	CCI-11			B17-A20	C10-A14	-A17	C10-A14
Coupler Input Data Bit 2^{3}	CCI-12			B17-A24	C09-A16	-A18	C09-A16
Coupler Input Data Bit 2^{2}	CCI-13			B17-B24	C10-A16	-A19	C10-A16
Coupler Input Data Bit 2^{1}	CCI-14			B17-A23	C09-B16	-A20	C09-B16
Coupler Input Data Bit 2^{0}	CCI-15			B17-B23	C10-B16	C28-A22	C10-B16

TABLE 4-2. PLUGGABLE AND BLOCK TRANSFER CONTROL SIGNALS (CONT'D)

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL CH. IN	CHANNEL NORMAL CH. OUT	CHANNEL OTHER IN	CHANNEL OTHER OUT	COUPLER INTERFACE CONNECTOR OUT	COUPLER PIN NO.
Coupler Output Data Bit 2^{15}	CCO-00			B22-A16		C28-B05	C09-A02
Coupler Output Data Bit 2^{14}	CCO-01			B22-A22		-B06	C10-A02
Coupler Output Data Bit 2^{13}	CCO-02			B22-B23		-B07	C09-B02
Coupler Output Data Bit 2^{12}	CCO-03			B22-B24		-B08	C10-B02
Coupler Output Data Bit 2^{11}	CCO-04			B21-A16		-B09	C09-A09
Coupler Output Data Bit 2^{10}	CCO-05			B21-A22		-B10	C10-A09
Coupler Output Data Bit 2^{9}	CCO-06			B21-B23		-B12	C09-A07
Coupler Output Data Bit 2^{8}	CCO-07			B21-B24		-B13	C10-A07
Coupler Output Data Bit 2^{7}	CCO-08			B20-A16		-B14	C09-A19
Coupler Output Data Bit 2^{6}	CCO-09			B20-A23		-B15	C10-A19
Coupler Output Data Bit 2^{5}	CCO-10			B20-B23		-B16	C09-B24
Coupler Output Data Bit 2^{4}	CCO-11			B20-B24		-B17	C10-B24
Coupler Output Data Bit 2^{3}	CCO-12			B19-A16		-B18	C09-A25
Coupler Output Data Bit 2^{2}	CCO-13			B19-A22		-B19	C10-A25
Coupler Output Data Bit 2^{1}	CCO-14			B19-B23		-B20	C09-B25
Coupler Output Data Bit 2^{0}	CCO-15			B19-B24		C28-B22	C10-B25

TABLE 4-3. INPUT CHANNELS

INPUT CHANNEL 0 SIGNALS

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL CH. IN	CHANNEL NORMAL CH. OUT	CHANNEL BLOCK TRFR. IN	CHANNEL BLOCK TRFR. OUT	COUPLER INTERFACE CONNECTOR NORMAL-IN	COUPLER PIN NO.
Unused	IC-000						
	IC-001						
	IC-002						
	IC-003						
	IC-004						
	IC-005						
	IC-006						
	IC-007						
Unused	IC-008						
Director Bit 2	IC-009	B27-A05				C30-A10	C12-B25
Director Bit 1	IC-010	B27-B13				-A11	C12-A25
Director Bit 0	IC-011	B27-A12				-A12	C12-B24
Data Interrupt Timeout	IC-012	B27-A24				-A13	C13-B23
Master Clear/ Controller Clear	IC-013	B27-B25				-A14	C13-A27
Coupler Buffer Full	IC-014	B27-B31				-A15	C12-A26
Coupler Busy	IC-015	B27-B30				C30-A16	C12-B06

TABLE 4-3. INPUT CHANNELS (CONT'D)

INPUT CHANNEL 3

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
REAL TIME CLOCK	IC-300	B28-B2				J12-A2, B2	
SPARE	IC-301	B28-B3				J12-A3, B3	
SPARE	IC-302	B28-B7				J12-A4, B4	
SPARE	IC-303	B28-B8				J12-A5, B5	
SPARE	IC-304	B28-B20				J12-A6, B6	
SPARE	IC-305	B28-A21				J12-C2, D2	
$\overline{\text{PRINT ERROR}}$	IC-306	B28-A27				J12-C3, D3	
SORT POCKET 2 FULL	IC-307	B28-A28				J12-C4, D4	
SORT ENTRY SENSOR	IC-308	B27-B2				J12-C5, D5	
SORT POCKET 1 FULL	IC-309	B27-B3				J12-C6, D6	
SORT STATION 2 PHOTOCELL	IC-310	B27-B7				J12-C7, D7	
SORT STATION 1 PHOTOCELL	IC-311	B27-B8				J12-E1, F1	
READ ZONE SENSOR	OC-312	B27-B20				J12-E2, F2	
DOUBLES SENSOR	IC-313	B27-A21				J12-E6, F6	
MIRROR/TRANS-PORT FAULT	IC-314	B27-A27				J12-E7, F7	
READER READY	IC-315	B27-A28				J12-J1, K1	

TABLE 4-3. INPUT CHANNELS (CONT'D)

INPUT CHANNEL 4

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
$\overline{\text{6/INCH ENABLE}}$	IC-400	B30-A6				J13-A2, B2	
$\overline{\text{SCAN GATE}}$	IC-401	B30-A5				J13-A3, B3	
SPARE	IC-402	B30-B13				J13-A4, B4	
MIRROR VELOCITY FAULT	IC-403	B30-A12				J13-A5, B5	
PAGE NEAR ZERO VELOCITY	IC-404	B30-B26				J12-A6, B6	
PAGE ADVANCE COUNT BIT 2^2	IC-405	B30-B25				J13-C2, D2	
PAGE ADVANCE COUNT BIT 2^1	IC-406	B30-B21				J13-C3, D3	
PAGE ADVANCE COUNT BIT 2^0	IC-407	B30-B30				J13-C4, D4	
SCAN AREA GATE	IC-408	B29-A6				J13-C5, D5	
SPARE	IC-409	B29-A5				J13-C6, D6	
MIRROR STOP FAULT	IC-410	B29-B13				J13-C7, D7	
MIRROR NEAR ZERO VELOCITY	IC-411	B29-A12				J13-E1, F1	
MIRROR COUNT BIT 2^3	IC-412	B29-B26				J13-E2, F2	
MIRROR COUNT BIT 2^2	IC-413	B29-B25				J13-E6, F6	
MIRROR COUNT BIT 2^1	IC-414	B29-B21				J12-L3, M3	
MIRROR COUNT BIT 2^0	IC-415	B29-B30				J12-L4, M4	

TABLE 4-3. INPUT CHANNELS (CONT'D)

INPUT CHANNEL 5

SIGNAL NAME	MNE-MONIC	CHANNEL NORMAL IN	CHANNEL NORMAL OUT	CHANNEL BLOCK TRANSFER IN	CHANNEL BLOCK TRANSFER OUT	COUPLER PIN NO.	SIGNAL MULTIPLEXED HANDPRINT
LATE CHARACTER DATA	IC-500	B30-B5				J13-E7, F7	SPARE
SERVO DATA READY	IC-501	B30-B4				J13-J1, K1	HANDPRINT DATA READY
SERVO DATA 2^5	IC-502	B30-A11				J13-J2, K2	HANDPRINT CLEAR
SERVO DATA 2^4	IC-503	B30-B12				J13-J6, K6	HANDPRINT HIGH
SERVO DATA 2^3	IC-504	B30-A25				J13-J7, K7	HANDPRINT ERROR
SERVO DATA 2^2	IC-505	B30-A24				J13-L2, M2	HANDPRINT LOW
SERVO DATA 2^1	IC-506	B30-A30				J13-L3, M3	NUMERIC DATA 2^3
SERVO DATA 2^0	IC-507	B30-A29				J13-L4, M4	NUMERIC DATA 2^2
CHARACTER DATA READY	IC-508	B29-B5				J13-L5, M5	NUMERIC DATA 2^1
CHARACTER DATA 2^6	IC-509	B29-B4				J13-L6, M6	NUMERIC DATA 2^0
CHARACTER DATA 2^5	IC-510	B29-A11				J13-L7, M7	ALPHA DATA 2^2
CHARACTER DATA 2^4	IC-511	B29-B12				J13-M2, P2	ALPHA DATA 2^1
CHARACTER DATA 2^3	IC-512	B29-A25				J13-N3, P3	ALPHA DATA 2^0
CHARACTER DATA 2^2	IC-513	B29-A24				J13-N4, P4	SYMBOL DATA 2^2
CHARACTER DATA 2^1	IC-514	B29-A30				J12-L5, M5	SYMBOL DATA 2^1
CHARACTER DATA 2^0	IC-515	B29-A29				J12-L6, M6	SYMBOL DATA 2^0

TABLE 4-3. INPUT CHANNELS (CONT'D)

INPUT CHANNEL 6

SIGNAL NAME	MNE-MONIC	CHANNEL NORMAL IN	CHANNEL NORMAL OUT	CHANNEL BLOCK TRANSFER IN	CHANNEL BLOCK TRANSFER OUT	COUPLER PIN NO.	OTHER
IMAGE REG. COLUMN READY	IC-600	B30-B1				J14-A2, B2	
IDENT	IC-601	B30-A3				J14-A3, B3	
TOPLESS DATA	IC-602	B30-B6				J14-A4, B4	
BOTTOMLESS DATA	IC-603	B30-A8				J14-A5, B5	
CHAR. VOLTAGE BIT 2^3	IC-604	B30-B19				J14-A6, B6	
CHAR. VOLTAGE BIT 2^2	IC-605	B30-A20				J14-C2, D2	
CHAR. VOLTAGE BIT 2^1	IC-606	B30-A26				J14-C3, D3	
CHAR. VOLTAGE BIT 2^0	IC-607	B30-B28				J14-C4, D4	
IDENT ENABLE	IC-608	B29-B1				J14-C5, D5	
JOURNAL TAPE SWITCH	IC-609	B29-A3				J14-C6, D6	
PARAMETER ENTRY SWITCH	IC-610	B29-B6				J14-C7, D7	
READER TIMING CONTROL SWITCH	IC-611	B29-A8				J14-E1, F1	
END OF FILE SWITCH	IC-612	B29-B19				J14-E2, F2	
LOAD SWITCH	IC-613	B29-A20				J14-E6, F6	
STOP SWITCH	IC-614	B29-A26				J12-L7, M7	
READY SWITCH	IC-615	B29-B28				J12-N2, P2	

TABLE 4-3. INPUT CHANNELS (CONT'D)

INPUT CHANNEL 7

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
IMAGE REG. OUTPUT BIT 13	IC-700	B30-B2				J14-E7, F7	
IMAGE REG. OUTPUT BIT 12	IC-701	B30-B3				J14-J1, K1	
IMAGE REG. OUTPUT BIT 11	IC-702	B30-B7				J14-J2, K2	
IMAGE REG. OUTPUT BIT 10	IC-703	B30-B8				J14-J6, K6	
IMAGE REG. OUTPUT BIT 9	IC-704	B30-B20				J14-J7, K7	
IMAGE REG. OUTPUT BIT 8	IC-705	B30-A21				J14-L2, M2	
IMAGE REG. OUTPUT BIT 7	IC-706	B30-A27				J14-L3, M3	
IMAGE REG. OUTPUT BIT 6	IC-707	B30-A28				J14-L4, M4	
IMAGE REG. OUTPUT BIT 5	IC-708	B29-B2				J14-L5, M5	
IMAGE REG. OUTPUT BIT 4	IC-709	B29-B3				J14-L6, M6	
IMAGE REG. OUTPUT BIT 3	IC-710	B29-B7				J14-L7, M7	
IMAGE REG. OUTPUT BIT 2	IC-711	B29-B8				J14-N2, P2	
IMAGE REG. OUTPUT BIT 1	IC-712	B29-B20				J14-N3, P3	
IMAGE REG. OUTPUT BIT 0	IC-713	B29-A21				J14-N4, P4	
IMAGE REG. OUTPUT CTL 2^1	IC-714	B29-A27				J12-N3, P3	
IMAGE REG. OUTPUT CTL 2^0	IC-715	B29-A28				J12-N4, P4	

TABLE 4-4. OUTPUT CHANNELS

0 SIGNALS

SIGNAL		CHANNEL				COUPLER INTERFACE CONNECTOR NORMAL-OUT	COUPLER PIN NO.
NAME	MNE-MONIC	NORMAL CH.		BLOCK TRFR.			
		IN	OUT	IN	OUT		
System Status Bit 2^{15}	OC-000		A28-A02			C29-A01	C09-A04
System Status Bit 2^{14}	OC-001		A28-A03			-A02	C10-A04
System Status Bit 2^{13}	OC-002		A28-A07			-A03	C09-B04
System Status Bit 2^{12}	OC-003		A28-A12			-A04	C10-B04
System Status Bit 2^{11}	OC-004		A28-B24			-A05	C09-B10
System Status Bit 2^{10}	OC-005		A28-A25			-A06	C10-B10
System Status Bit 2^9	OC-006		A28-B27			-A07	C09-B09
Unused	OC-007		A28-B29			-A08	---
Controller Data Interrupt Enable	OC-008		A27-A02			-A09	C13-A02
System Status Bit 2^6	OC-009		A27-A03			-A10	C10-A24
Controller Alarm	OC-010		A27-A07			-A11	C13-A14
Controller End of Operation	OC-011		A27-A12			-A12	C13-B19
Controller Data Interrupt Timeout Reset	OC-012		A27-B24			-A13	C13-B25
Controller Master Clear Reset	OC-013		A27-A25			-A14	C13-B26
Controller Pulse	OC-014		A27-B27			-A15	C13-B12
System Status Bit 2^0	OC-015		A27-B27			C29-A16	C13-B12

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 1 SIGNALS

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL CH. IN	CHANNEL NORMAL CH. OUT	CHANNEL BLOCK TRFR. IN	CHANNEL BLOCK TRFR. OUT	COUPLER INTERFACE CONNECTOR NORMAL-OUT	COUPLER PIN NO.
Transport Status Bits 2^{15}	OC-100		A28-B01			C29-B01	C09-B05
Transport Status Bits 2^{14}	OC-101		A28-B03			-B02	C10-B05
Transport Status Bits 2^{13}	OC-102		A28-B12			-B03	C09-B07
Transport Status Bits 2^{12}	OC-103		A28-B13			-B04	C10-B07
Transport Status Bits 2^{11}	OC-104		A28-A24			-B05	C09-A11
Transport Status Bits 2^{10}	OC-105		A28-B26			-B06	C10-A11
Transport Status Bits 2^{9}	OC-106		A28-A28			-B07	C09-A10
Transport Status Bits 2^{8}	OC-107		A28-A29			-B08	C10-A10
Transport Status Bits 2^{7}	OC-108		A27-B01			-B09	C09-A27
Transport Status Bits 2^{6}	OC-109		A27-B03			-B10	C10-A27
Transport Status Bits 2^{5}	OC-110		A27-B12			-B11	C09-A23
Transport Status Bits 2^{4}	OC-111		A27-B13			-B12	C10-A23
Transport Status Bits 2^{3}	OC-112		A27-A24			-B13	C09-A21
Transport Status Bits 2^{2}	OC-113		A27-B26			-B14	C10-A21
Transport Status Bits 2^{1}	OC-114		A27-A28			-B15	C09-B26
Transport Status Bits 2^{0}	OC-115		A27-A29			C29-B16	C10-B26

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 2

SIGNAL NAME	MNEMONIC	CHANNEL NORMAL IN	CHANNEL NORMAL OUT	CHANNEL BLOCK TRANSFER IN	CHANNEL BLOCK TRANSFER OUT	COUPLER PIN NO.	OTHER
TRANSPORT CHECK 2	OC-200		A30-A2			J15-A2, B2	
TRANSPORT DROP POWER	OC-201		A30-A3			J15-A3, B3	
RESCAN	OC-202		A30-A7			J15-A4, B4	
NUMERIC 0-9+X	OC-203		A30-A12			J15-A5, B5	
SPARE	OC-204		A30-B24			J15-C2, D2	
SPARE	OC-205		A30-A25			J15-C3, D3	
SPARE	OC-206		A30-B27			J15-C4, D4	
PRINT DOCUMENT	OC-207		A30-B24			J15-C5, D5	
HP PITCH 2^{1}	OC-208		A19-A2			J16-A2, B2	
HP PITCH 2^{0}	OC-209		A29-A3			J16-A3, B3	
DISPLAY NOW	OC-210		A29-A7			J16-A4, B4	
MARKING PEN	OC-211		A19-A12			J16-A5, B5	
CHAR. PEAK REF. BIT 2^{3}	OC-212		A29-B4			J16-C2, D2	
CHAR. PEAK REF. BIT 2^{2}	OC-213		A29-A25			J16-C3, D3	
CHAR. PEAK REF. BIT 2^{1}	OC-214		A19-B27			J16-C4, D4	
CHAR. PEAK REF. BIT 2^{0}	OC-215		A29-B29			J16-L5, D5	

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 3

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
CONTROLLER RUNNING	OC-300		A30-B1			J15-C7, D7	
INHIBIT READER TIMING	OC-301		A30-B3			J15-E1, F1	
GENERAL SYNC 2	OC-302		A30-B12			J15-E2, F2	
GENERAL SYNC 1	OC-303		A30-B13			J15-E6, F6	
IMAGE REG. RECIRCULATE	OC-304		A30-A24			J15-J1, K1	
JOURNAL TAPE MOTOR	OC-305		A30-B26			J15-J2, K2	
PARAMETER ENTRY INDITR.	OC-306		A30-A28			J15-J6, K6	
SORT HOPPER FULL INDICATOR	OC-307		A30-A29			J15-J7, K7	
SORT CHECK INDICATOR	OC-308		A29-B1			J16-C7, D7	
MIRROR CHECK INDICATOR	OC-309		A29-B3			J16-E1, F1	
TRANSPORT CHK INDICATOR	OC-310		A29-B12			J16-E2, F2	
DOUBLES CHECK INDICATOR	OC-311		A29-B13			J16-E6, F6	
END OF FILE INDICATOR	OC-312		A29-A24			J16-J1, K1	
LOAD INDICATOR	OC-313		A29-B26			J16-J2, K2	
STOP INDICATOR	OC-314		A29-A28			J16-J6, K6	
READY INDICATOR	OC-315		A29-A29			J16-J7, K7	

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 4

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
READ	OC-400		A32-A2			J15-L3, M2	
SCAN MIRROR FORWARD	OC-401		A32-A3			J15-L4, M4	
ACCELERATE MIRROR REVERSE	OC-402		A32-A7			J15-L5, M5	
ZERO MIRROR	OC-403		A32-A12			J15-L6, M6	
STOP MIRROR	OC-404		A32-B24			J15-N2, P2	
SCAN RIGHT TO LEFT	OC-405		A32-A25			J15-N3, P3	
REVERSE SHIFT	OC-406		A32-B27			J15-N4, P4	
UP-SIDE DOWN	OC-407		A32-B29			J15-N5, P5	
CLEAR CHAR. DATA	OC-408		A31-A2			J15-L3, M3	
CLEAR SERVO DATA	OC-409		A31-A3			J16-L4, M4	
SORT GATE CONTROL	OC-410		A31-A7			J16-L5, M5	
SERVO DRIVE REVERSE	OC-411		A31-A12			J16-L6, M6	
PAGE ADVANCE 40 IPS	OC-412		A31-B24			J16-N2, P2	
PAGE ADVANCE 20 IPS	OC-413		A31-A25			J16-N3, P3	
PAGE ADVANCE 12.4 IPS	OC-414		A31-B27			J16-N4, P4	
PAGE ADVANCE 5 IPS	OC-415		A31-B29			J16-N5, P5	

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 5

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
		NORMAL		BLOCK TRANSFER			
NAME	MNE-MONIC	IN	OUT	IN	OUT		
MARK SENSE	0C-500		A32-B1			J17-A2, B2	
ANST NUMERIC	0C-501		A32-B3			J17-A3, B3	
ANSI CONTROL	0C-502		A32-B12			J17-A4, B4	
ANSI ALPHA 5	0C-503		A32-B13			J17-A5, B5	
ANSI ALPHA 21	0C-504		A32-A24			J17-C2, D2	
ANSI PUNC-TATION 1	0C-505		A32-B26			J17-C3, D3	
ANSI PUNC-TATION 2	0C-506		A32-A28			J17-C4, D4	
OPITCAL SCALING	0C-507		A32-A29			J17-C5, D5	
ALTERNATE FONT 1	0C-508		A31-B1			J18-A2, B2	EUROPEAN 1 & 7
ALTERNATE FONT 2	0C-509		A31-B3			J18-A3, B3	GOTHIC HP
ALTERNATE FONT 3	0C-510		A31-B12			J18-A4, B4	
CHARACTER PITCH 2^1	0C-511		A31-B13			J18-A5, B5	
CHARACTER PITCH 2^0	0C-512		A31-A24			J18-C2, D2	
HANDPRINT	0C-513		A31-B26			J18-C3, D3	
SUPER FILL FOR GOTHIC HP	0C-514		A31-A28			J18-C4, D4	
SCAN HEIGHT	0C-515		A31-A29			J18-C5, D5	

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 6

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
		NORMAL		BLOCK TRANSFER			
NAME	MNE-MONIC	IN	OUT	IN	OUT		
HORIZONTAL LINE THICKEN	0C-600		A34-A2			J17-C7, D7	
BLACK FILL	0C-601		A34-A3			J17-E1, F1	
VER. LINE ACCUM. COUNT BIT 2^5	0C-602		A34-A7			J17-E2, F2	
VER. LINE ACCUM. COUNT BIT 2^4	0C-603		A34-A12			J17-E6, F6	
VER. LINE ACCUM. COUNT BIT 2^3	0C-604		A34-B24			J17-J1, K1	
VER. LINE ACCUM. COUNT BIT 2^2	0C-605		A34-A25			J17-J2, K2	
VERT. LINE ACCUM. COUNT BIT 2^1	0C-606		A34-B27			J17-J6, K6	
VER. LINE ACCUM. COUNT BIT 2^0	0C-607		A34-B29			J17-J7, K7	
VIDEO QUANTI-ZING BIT 2^7	0C-608		A33-A2			J18-C7, D7	
VIDEO QUANTI-ZING BIT 2^6	0C-609		A33-A3			J18-E1, F1	
VIDEO QUANTI-ZING BIT 2^5	0C-610		A33-A7			J18-E2, F2	
VIDEO QUANTI-ZING BIT 2^4	0C-611		A33-A12			J18-E6, F6	
VIDEO QUANTI-ZING BIT 2^3	0C-612		A33-B24			J18-J1, K1	
VIDEO QUANTI-ZING BIT 2^2	0C-613		A33-A25			J18-J2, K2	
VIDEO QUANTI-ZING BIT 2^1	0C-614		A33-B27			J18-J6, K6	
VIDEO QUANTI-ZING BIT 2^0	0C-615		A33-B29			J18-J7, K7	

TABLE 4-4. OUTPUT CHANNELS (CONT'D)

OUTPUT CHANNEL 7

SIGNAL		CHANNEL				COUPLER PIN NO.	OTHER
NAME	MNE-MONIC	NORMAL		BLOCK TRANSFER			
		IN	OUT	IN	OUT		
IMAGE REG. INPUT BIT 13	OC-700		A34-B1			J17-L3, M3	
IMAGE REG. INPUT BIT 12	OC-701		A34-B3			J17-L4, M4	
IMAGE REG. INPUT BIT 11	OC-702		A34-B12			J17-L5, M5	
IMAGE REG. INPUT BIT 10	OC-703		A34-B13			J17-L6, M6	
IMAGE REG. INPUT BIT 9	OC-704		A34-A24			J17-N2, P2	
IMAGE REG. INPUT BIT 8	OC-705		A34-B26			J17-N3, P3	
IMAGE REG. INPUT BIT 7	OC-706		A34-A28			J17-N4, P4	
IMAGE REG. INPUT BIT 6	OC-707		A34-A29			J17-N5, P5	
IMAGE REG. INPUT BIT 5	OC-708		A33-B1			J18-L3, M3	
IMAGE REG. INPUT BIT 4	OC-709		A33-B3			J18-L4, M4	
IMAGE REG. INPUT BIT 3	OC-710		A33-B12			J18-L5, M5	
IMAGE REG. INPUT BIT 2	OC-711		A33-B13			J18-L6, M6	
IMAGE REG. INPUT BIT 1	OC-712		A33-A24			J18-N3, P3	
IMAGE REG. INPUT BIT 0	OC-713		A33-B26			J18-N4, P4	
IMAGE REG. INPUT CTL. 2^1	OC-714		A33-A28			J18-N5, P5	
IMAGE REG. INPUT CTL. 2^0	OC-715		A33-A29			J18-N6, P6	

CONTROLLER/READER SIGNALS

Controller/reader logic signals are presented in alphabetical order in Table 4-5.

NOTE

A logic 1 level = +2.0 vdc or greater and nominally a +2.4 vdc. A logic 0 level = 0.8 vdc or less.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS

Signal	Description
Accelerate Mirror Reverse	A logical 1 level, originating in the controller, causing the line scan mirror to travel toward zero coordinate in a constant acceleration mode where the acceleration is approximately 62,000 inches per second^2. Returning the Accelerate Mirror Reverse level to a logical 0 will cause the line scan mirror to decelerate at a rate of 62,000 inches per second^2, to a nominal velocity of 75 inches per second (ips). A Stop Mirror command is required to stop the mirror motion.
Alternate Font 1	A logical 1 originating in the controller used to enable the matrices of one of the standard optional character sets. The user can specify which alternate font select group an optional font is installed in.
Alternate Font 2	A logical 1 originating in the controller used to enable the matrices of one of the standard optional character sets. The user can specify which alternate font select group an optional font is installed in.
Alternate Font 3	A logical 1 originating in the controller used to enable the matrices of one of the standard optional character sets. The user can specify which alternate font select group an optional font is installed in.
ANSI Numeric	A logical 1 originating in the controller used to enable the ANSI-OCR numeric matrices 1 through 9. NOTE For full numeric selections, 0 through 9, mark sense must be selected.
ANSI Alpha 5	A logical 1 originating in the controller used to enable the ANSI-OCR alpha matrices C, S, T, X, and Z.
ANSI Alpha 21	A logical 1 originating in the controller used to enable the ANSI-OCR alpha matrices A, B, D through R, U through W, and Y.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
ANSI Punctuation 1	A logical 1 originating in the controller used to enable the ANSI-OCR punctuation matrices period, dollar, hyphen, slant, ampersand, and percent.
ANSI Punctuation 2	A logical 1 originating in the controller used to enable the ANSI-OCR punctuation matrices comma and asterisk.
ANSI Control	A logical 1 originating in the controller used to enable the ANSI-OCR control symbols matrices chair, fork, and hook.
Bottomless Data	A logical 1 level, originating in the reader, indicating that the line of data being scanned is misregistered and is extending beyond the lower boundary of the image register. Bottomless Data will be cleared by the CLR Data Ready signal.
Character Pitch	Two logic levels, originating in the controller, used to define Character Pitch to the reader. The bits are defined as follows: 00 = 10 characters/inch (Size I) 01 = 8 characters/inch 10 = 7 characters/inch (Size IV) 11 = open
Clear Character Data	A logical 1 pulse, originating in the controller, indicating that Character Data has been input by the controller and that the Character Data and Data Ready may be cleared.
Character Data	Sevel logical levels, originating in the reader, used for transmission of ASCII codes of recognized characters.
Character Data Ready	A logical 1 level, originating in the reader, indicating that Character Data is stable and may be sampled by the controller.
Character Peak Reference	Four levels, originating in the controller, making up a base 16 count. The value of this count will define to the reader a voltage comparison point to enable the character peak circuitry. An equal-or greater-than comparison will act as an enable.
Character Voltage	Four logic levels making up a hexadecimal valued word, originating in the reader, indicating a digital value of the best match matrix output. Character Voltage will be available with Character Data and will operate under control of Data Ready and Clear Data.
Display Now	A logical 1, originating in the controller to the OLCC option, indicating that the read coordinate has been reached where a reject was previously received. Used to flag reject character on display.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Controller Running	A logical 1 pulse, originating in the controller, for use by the fault interlock system. After system initiation and reader power control sequencing, Controller Running will indicate to the reader that the controller is operational. Controller Running will be an approximate 1-microsecond pulse given at least once every 100 milliseconds. Loss of Controller Running causes automatic reader/controller power shutdown.
Doubles Check	A logical 1 level, originating in the controller, indicating that a Double Document feed has been detected.
Doubles Sensor	A logical 1 level, originating in the reader indicating a multiple document thickness.
End of File Indicator	A logical 1 level, originating in the controller, energizing the End of File indicator. End of File will toggle on or off, based on its previous condition and the End of File switch being depressed.
End of File Switch	A logical 1, originating in the reader, indicating the EOF switch is depressed.
General Sync 1	A logical 1 pulse, originating in the controller, to allow maintenance personnel capability for scope triggering by firmware command. It currently monitors the coupler busy status.
General Sync 2	A logical 1 pulse, originating in the controller, to allow maintenance personnel capability for scope triggering by firmware command. NOTE General Sync 1 and 2 are available on the reader maintenance panel.
Handprint	A logical 1, originating in the controller, used to switch normal input channel 5 to Handprint mode. Channel 5 is multiplexed at the reader when the Handprint option is added.
Handprint Alpha Data	Three logical levels, originating in the reader, used for transmission of Handprint Alpha Data codes of recognized characters, space, and reject.
Handprint Clear	A logical 1 level, originating in the reader, indicating that the Reader Image Register contains no black data. This is an instantaneous signal and will toggle with the presence or absence of black data.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Handprint Data Ready	A logical 1 level, originating in the reader, indicating that handprint character data is stable and may be sampled by the controller. Handprint Data Ready is reset to a logical 0 by Clear Character Data.
Handprint Error	A logical 1 level, originating in the reader, indicating an electronic or logical malfunction in the Handprint option.
Handprint High	A logical 1 level, originating in the reader, indicating that line of handprint data being scanned is misregistered and is extending beyond the upper boundary of the image register. Handprint High will be cleared at the beginning of the next read cycle.
Handprint Low	A logical 1 level, originating in the reader, indicating that the line of handprint data being scanned is misregistered and beyond the lower boundary of the image register. Handprint Low will be cleared at the beginning of the next read cycle.
Handprint Numeric Data	Four logical levels, originating in the reader, used for transmission of Handprint Numeric Data codes of recognized characters, space and reject.
Handprint Symbol Data	Three logical levels, originating in the reader, used for transmission of Handprint Symbol Data codes of recognized characters, space, and reject.
Horizontal Line Accumulate	Six logic levels, originating in the controller, instructing the reader to accumulate black video information. The accumulation interval is specified in 60_{10} increments, 59_{10} being the shortest interval and 1_{10} being the longest accumulation interval.
Image[1] Register Input	Fourteen logic levels, originating in the controller for transfer to black or white video data into the Image Register. A logical 1 level will indicate black.
Image[1] Register Input Control	Two logic levels, originating in the controller for control monitoring of the Image Register Input.
Image[1] Register Output	Fourteen logic levels, originating in the reader for transfer of black and white data from the image register to the controller. A logical 1 level will indicate black.
Image[1] Register Output Control	Two logical levels originating in the reader for control monitoring of the Image Register Output.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Image[1] Register Column Ready	A logical 1 pulse, originating at the reader, indicating that the image register is ready to receive column video data from the Image Register Input lines.
Image[1] Register Recirculate	A logical 1 level, originating in the controller, causing the reader image register to trap whatever video information is available and recirculate it.
Indent	A logical 0 level, originating in the reader, from the **six-lines-per-inch option.** This signal will occur if a lower line of data is found first for reading, and if within 1 inch of the start of the lower line, an upper line of data is found. Indent enable will also be a logical 0 beforehand.
Indent Enable	A logical 0 level, originating in the reader, from the **six-lines-per-inch option.** This signal tells the controller that the line of data being read is positioned in the read window such that a second line, indented from the edge, may occur above or is possible above this line.
Inhibit Reader Timing	A logical 1 level, originating in the controller, instructing the reader to stop the image register at the next "column count zero."
Journal Tape Motor	A logical 1 level, originating in the controller to turn on the journal tape take-up spooler motor after a nominal 36 inches of transport belt motion has been measured since the leading edge of the journal tape was sensed at the read zone. The Journal Tape Motor level resets to a logical 0, turning off the take-up motor, after a nominal 12 inches of transport motor has been measured since the trailing edge of the journal tape was sensed.
Journal Tape Switch	A logical 1 level, originating in the reader, when the Journal Tape **Switch is toggled on to indicate** the Journal Tape option is to be used. The Journal Tape Switch level and indicator toggles when the switch is depressed.
Late Character Data	A logical 1 level, originating in the reader, indicating that Character Data Ready had been set, that the reader character buffer has overflowed, and that the overflowing character(s) has been lost. Late Character Data will be reset to a logical 0 by Clear Character Data.
Load Indicator	A logical 1 level, originating in the controller, energizing the Load Indicator. The Load Indicator will turn on with depression of the load switch and will remain on until the document is at the Ready position.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Load Switch	A logical 1 level, originating in the reader, indicating that the Load Switch is depressed and that document loading and clearing should be performed. The Load Switch will be active only during a Stop (Reader Not Ready) condition.
Mark Sense	A logical 1 originating in the controller used to enable Mark Sense, ANSI-OCR zero, and Character Cancel (Chinese Christmas tree and/or filled circle).
Marking Pen	A logical 1 level, originating in the controller energizing the Marking Pen drive solenoid.
Mechanical Servo	The Mechanical Servo signals are all those signals required to reposition the document for incorrectly registered lines of data, either on a line by line basis or within a line of data. Documents will not be mechanically servoed during a line read scan.
Mirror Check	A logical 1 level, originating in the controller, energizing the Mirror Check indicator when a detectable malfunction has occurred in the Line Scan Mirror system.
Mirror Control	The Mirror Control signals are all those signals required to position and track the line scanning mirror.
Mirror Count	Eight logic levels, originating in the reader, comprising a modulus 16 forward/backward counter, with each count equaling 0.048 inches. The counter will be reset to zero upon exceeding the boundaries of the Scan Area Gate.
Mirror Near Zero Velocity	A logical 1 level, originating in the reader, indicating that 4 to 6 milliseconds have elapsed since Stop Mirror was given.
Mirror/Transport Fault	A logical 1 level, originating in the reader, indicating that Reader Ready dropped to a logical 0 because of a noncorrectable malfunction in either the Mirror or Transport Drive logic. Mirror/Transport Fault is cleared by operator depression of the Reader Ready Switch.
Mirror Velocity Fault	A logical 1 level, originating in the reader, indicating that during a read scan a mirror velocity fault occurred. A mirror velocity fault is a velocity difference of greater than 4.8 percent of 75 ips. Mirror Velocity Fault will be cleared at the beginning of the next read cycle.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Optical Scaling	A logical 1 level, originating in the controller, used to enable Optical Scaling for the Size IV options (ANSI-OCR-A, 7B). In the zero condition it enables normal Size I Optical Scaling for ANSI-OCR-A Size I characters and handprint.
Page Advance 5 ips	A logical 1 level, originating in the controller to advance the page at a velocity of approximately 5 ips. Returning the level to zero will stop page motion.
Page Advance 12.5 ips	A logical 1 level, originating in the controller to advance the page at a velocity of approximately 12.5 ips. Returning the level to zero will require setting the page advance 5 ips line to a logical 1 to generate a velocity step function prior to stopping page motion.
Page Advance 20 ips	A logical 1 level, originating in the controller to advance the page at a velocity of approximately 20 ips. Page motion is to be halted using the step function as described in page advance 12.5 ips.
Page Advance 40 ips	A logical 1 level, originating in the controller to advance the page at a velocity of approximately 40 ips. Page motion is to be halted using the step function as described in page advance 12.5 ips.
Page Advance Count	Three logical levels, originating in the reader comprising a modulus 8 forward/backward counter with each count equaling 0.008 inch.
Page Near Zero Velocity	A logical 1 level, originating in the reader indicating that all belt and paper motion has reached a velocity of 0.35 ips or less.
Parameter Entry Indicator	A logical 1 level, originating in the controller, energizing the Parameter Entry Indicator and indicating that a parameter entry sequence can be started. The Parameter Entry Indicator level resets to a logical 0 at the beginning of a parameter entry.
Parameter Entry Switch	A logical 1 level, originating in the reader, indicating that the Parameter Entry Switch is depressed.
Read	A logical 1 level, originating in the controller, used to enable the recognition logic in the reader.
Read Control	Read Control signals are all those lines needed to enable reading and transfer of typed or printed read data.
Read Zone Sensor	A photocell sensing station at the reader in the area of the optical read zone. It will be 125 increments of 0.008 inch each upstream of the optical center line of the read zone. A logical 1 level when not covered.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Ready Indicator	A logical 1 level, originating in the controller, indicating that the Ready Switch has been (or is being) depressed and that Reader Ready and Controller Ready are present. The Ready Indicator is representative of the reader/controller being ready and on line to the computer.
Reader Ready	A logical 1 level, originating in the reader, indicating that the reader is mechanically and electrically ready for operation. Loss of Reader Ready will cause loss of System Ready and will generate a Stop condition.
Ready Switch	A logical 1 level, originating in the reader, indicating that Ready Switch is depressed.
Real Time Clock	A logical clock output, originating in the reader, with a symmetrical output and a frequency of 500 Hz ±2 percent.
Reader Timing Control Switch	A logical 1 level, originating in the reader, indicating that the Reader Timing Control Switch is in the "Controller" position and that the reader timing can be inhibited via controller software control.
Reverse Shift	A logical 1 level, originating in the controller, causing a scanned character to be loaded and shifted from left to right (or reverse of normal right to left). Used when scanning normal characters from right to left.
Scan Area Gate	A logical 1 level, originating in the reader, indicating that the line scan mirror is physically within the reader-defined limits for scanning. The leftmost limit will define mirror coordinate zero and the rightmost limit will define mirror coordinate FF_{16}. The Scan Area Gate will equal a logical 1 within approximately 45.9 degrees of mirror shaft rotation.
Scan Height	A logical 1 level, originating in the controller, used to enable a height reduction to 36 vertical cells from the normal 54 vertical cells. Normally used for reading at a line pitch of four to the inch when the six-lines-per-inch option is not installed or for normal Size IV reading.
Scan Mirror Forward	A logical 1 level, originating in the controller, causing the line scanning mirror to travel at a paper velocity of 75 ips.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Scan Right to Left	A logical 1 level, originating in the controller, causing the reader to reverse all control lines to the mirror and counter logic. Normally, the zero coordinate is at the left limit of the read zone and FF_{16} is at the right limit. This signal has the net effect of placing mirror coordinate 0 to the right limit and FF_{16} to the left limit of the read zone. Scan forward would be right to left, accelerate reverse and zero mirror from left to right.
Servo Data	Six logical levels, originating in the reader, containing the "1's" complement of a binary number equal to the vertical position of the character in the image register at character peak time, with each of the counts equaling 0.00585 inch for ANSI Size I characters and 0.00937 inch for ANSI Size IV characters.
Servo Data Ready	A logical 1 level originating in the reader indicating that servo data is available and may be sampled.
Servo Drive Reverse	A logical 1 level, originating in the controller, directing the transport to move the document in the reverse (upstream) direction. Reverse motion is restricted to a velocity of 5 ips.
Sort Check	A logical 1 level, originating in the controller, energizing the Sort Check Indicator when a detectable malfunction has occurred in the sort station.
Sort Control	Sort Control signals are those lines necessary to detect and sort documents, and to monitor the condition of the sort pockets.
Sort Entry Sensor	A photocell sensing station used to detect the edges of documents as they are entering the takeaway area of the transport. It will equal a logical 1 when not covered.
Sort Gate Control	A logical 1 level, originating in the controller, used to position the Sort Gate for document sorting to Sort Pocket 2. A logical 0 will cause the document to sort to Sort Pocket 1.
Sort Hopper Full	A logical 1 level, originating in the controller, energizing the Sort Full indicator when either of the output hoppers is full and requires operator intervention to empty.
Stop Mirror	A logical 1 level, originating in the controller, instructing the line scan mirror to come to a controlled halt within the distance specified by three mirror coordinates. Stop will be a logical 1 at all times other than mirror action time.
Sort Pocket 1 Full	A logical 1 level, originating in the reader, indicating that the Sort Pocket 1 Full sensor is not covered.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Sort Pocket 2 Full	A logical 1 level, originating in the reader, indicating that the Sort Pocket 2 Full sensor is not covered.
Sort Station 1 Photocell	A photocell sensing station used to detect the leading edge of a document at Sort Station 1. It will equal a logical 1 when not covered.
Sort Station 2 Photocell	A photocell sensing station used to detect the leading edge of the document at Sort Station 2. It will equal a logical 1 when not covered.
Stop Indicator	A logical 1 level, originating in the controller, energizing the Stop Indicator when the reader has lost its mechanical or functional ready condition or the Stop switch has been depressed. The Stop Indicator is representative of a "Reader Not Ready" status to the computer, and "Reader Off Line" to the operator.
Stop Switch	A logical 1 level, originating in the reader, indicating that Stop Switch is depressed.
Topless Data	A logical 1 level, originating in the reader, indicating that the line of data being scanned is misregistered and is extending beyond the upper boundary of the image register. Topless Data will be cleared by CLR Data Ready.
Transport	The transport signals are all those signals required to control document motion from the feeder to the sort station.
Transport Check 1	A logical 1 level, originating in the controller, energizing the Transport Check indicator when a detectable malfunction has occurred in the area of the transport bed or no more documents are available to be read.
Transport Check 2	A logical 1 level, originating in the controller, energizing the indicator on the reader maintenance panel, indicating that transport motion was initiated by the controller and no motion was detected after 5 milliseconds. The indicator is reset by the maintenance panel fault reset switch.
Transport Drop Power	A logical 1 level, originating in the controller used to disable the transport motors when Page Near Zero Velocity remains a logical 0 and there have been no Page Advance or Servo Drive Reverse signals set for 10 milliseconds. Transport Drop Power is cleared by operator depression of the Reader Ready switch.

TABLE 4-5. CONTROLLER/READER LOGIC SIGNALS (CONT'D)

Signal	Description
Upside-Down	A logical 1 level, originating in the controller, used to enable the loading of an upside-down character into the load and image registers.
Vertical Thicken	A logical 1 level, originating in the controller, instructing the reader to add black information to the bottom of a horizontal line, column by column, if it is only one black cell thick.
Video Quantizing	Eight logic levels, originating in the controller, used to select the desired character quantizing level, FF_{16} being the most white level and 00_{16} being the most black level.
Zero Mirror	A logical 1 level, originating in the controller, causing the line scan mirror to travel at a nominal scan velocity of 150 ips toward the zero limit.

BUFFER CONTROLLER MAINTENANCE CONSOLE

The buffer controller maintenance console is not a permanent part of the reader system. It is connected to the station control interface of the buffer controller to enable the customer engineer to perform off-line maintenance on the system (Tables 6-1 and 6-2). Four 61-conductor I/O cables connect the buffer controller maintenance console to controller connectors J1 through J4.

SECTION 5

DIAGRAMS

Figures 5-1 through 5-5 contain the card schematics.

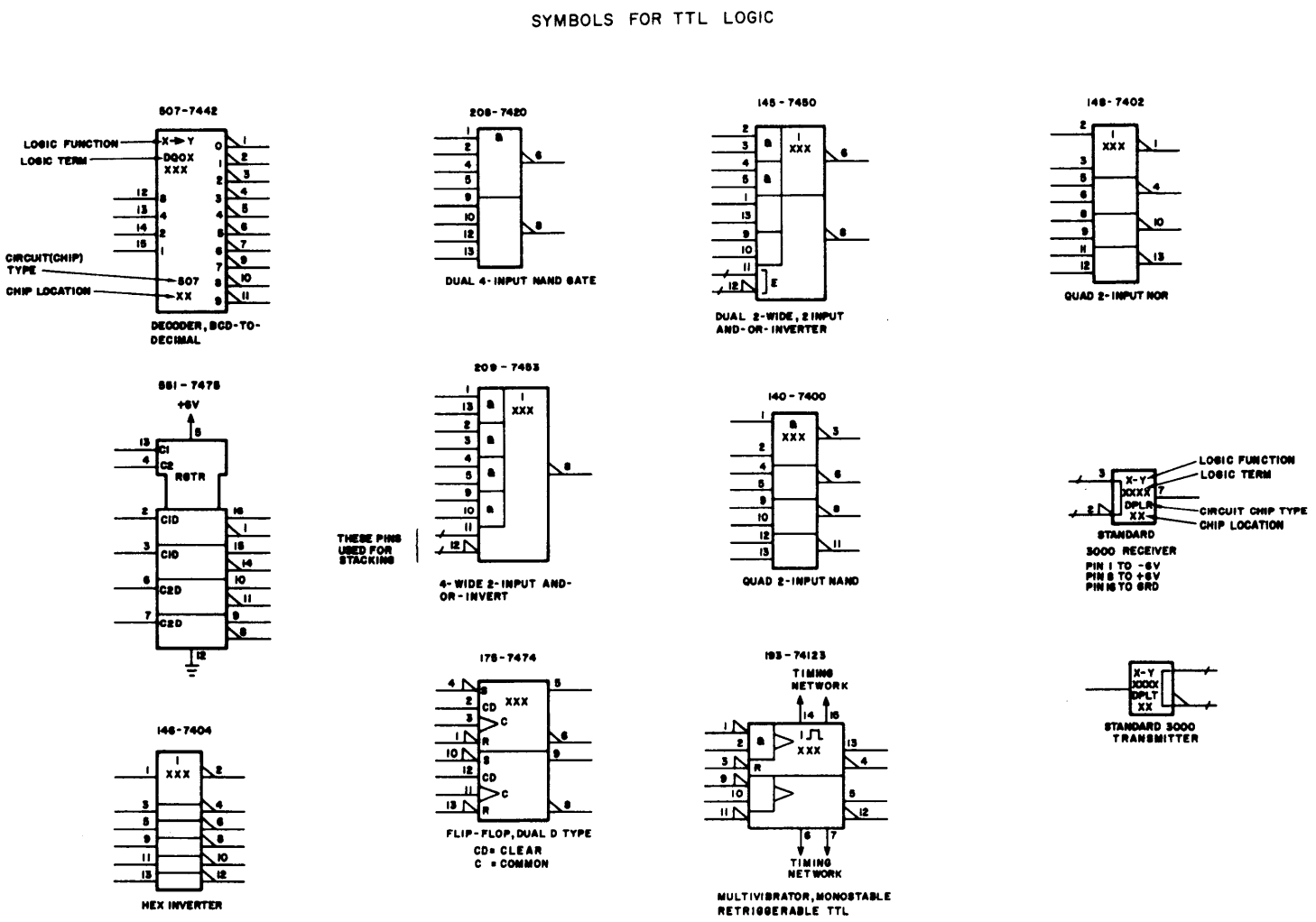


Figure 5-1. Controller Key to Logic Symbols

BLOCK TRANSFER

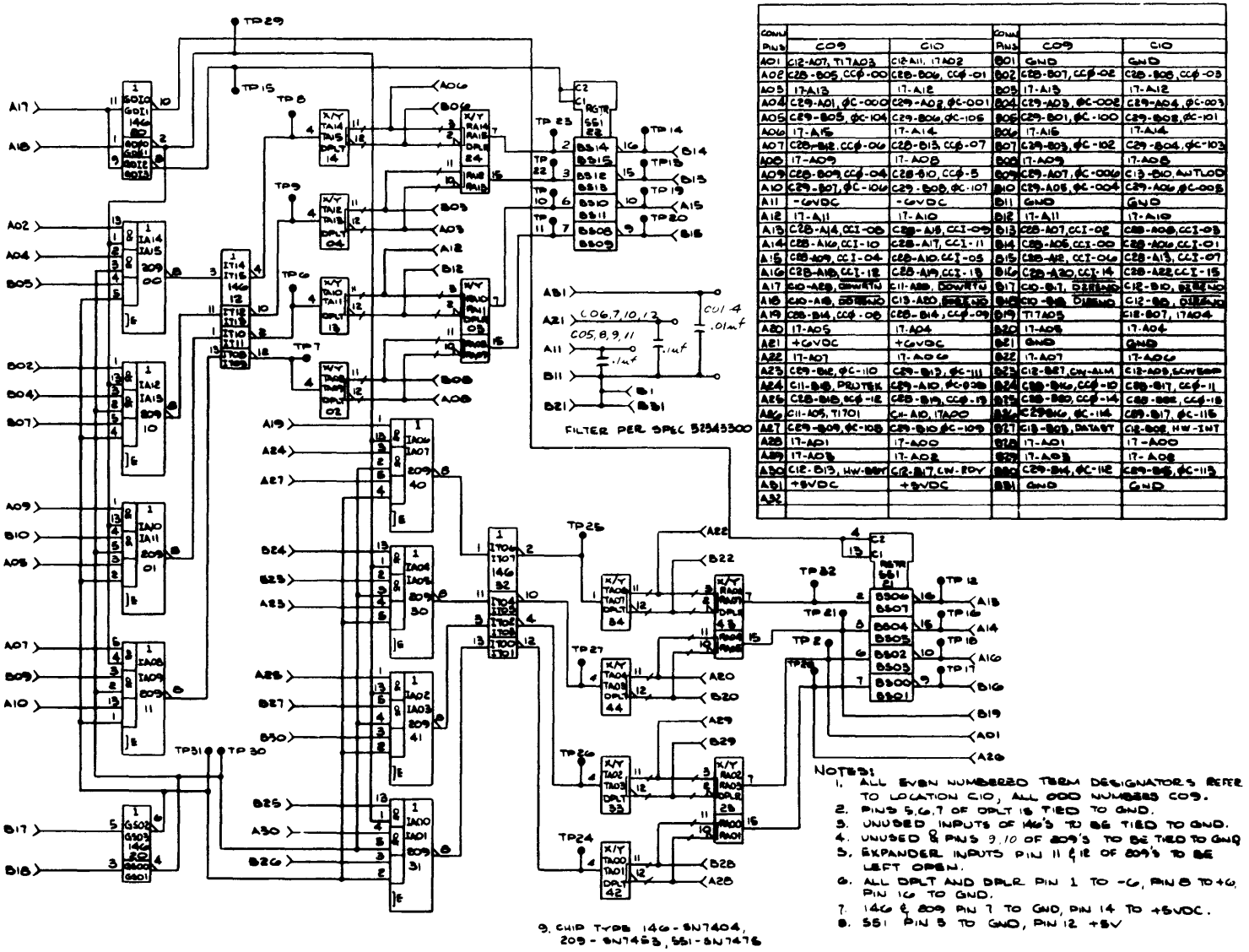
Block transfers within the coupler are accomplished through party line receivers and transmitters. The transmitters consist of 8 DPLT transmitter chips made up of TA00 through TA15. The receivers are contained in 4 chips (2 receivers each) made up of RA00 through RA15.

A17 provides the input for a Director 0 write signal. A "0" input on GDIO, pin 11 (GD12 pin 9) will be inverted and applied to BS00 through BS15. The signal will gate the output of the DPLR's from the 1700 to the coupler input channel 0.

A18 provides the input for a Direct 0 Read signal. A "0" input on GD00, pin 1, and GD01, pin 1, will be inverted and fanned out to the 209 AND gates which control the transfer from the BC coupler output channel CCO-XX. From there, it goes to terms IT00 through IT15 which invert and apply the signals to DPLT transmitters TA00 through TA15.

B17 provides the input for a Director 2 Status signal. A "0" input on GS02 & GS03, pin 5, will be inverted and applied to the AND gates to cause a transfer of output channel 1 from the BC to the 1700.

B18 provides the input for a Director 1 Status signal. A "0" input on GS00 and GS01, pin 3, will be inverted and applied to the AND gates to cause a transfer of output channel 0 from the BC to the 1700. Refer to Drawing 48870500 for the control logic of block transfers.



CONN PINS	C09	C10	CONN PINS	C09	C10
A01	C12-A07, T17A03	C12-A11, 17A02	B01	GND	GND
A02	C28-B05, CC#-00	C28-B06, CC#-01	B02	C28-B07, CC#-02	C28-B08, CC#-03
A03	17-A13	17-A12	B03	17-A13	17-A12
A04	C29-A01, #C-000	C29-A02, #C-001	B04	C29-A03, #C-002	C29-A04, #C-003
A05	C29-B05, #C-104	C29-B06, #C-105	B05	C29-B01, #C-100	C29-B02, #C-101
A06	17-A15	17-A14	B06	17-A15	17-A14
A07	C28-B12, CC#-06	C28-B13, CC#-07	B07	C29-B03, #C-102	C29-B04, #C-103
A08	17-A09	17-A08	B08	17-A09	17-A08
A09	C28-B09, CC#-04	C28-B10, CC#-5	B09	C29-A07, #C-006	C13-B10, AUTLOD
A10	C29-B07, #C-106	C29-B08, #C-107	B10	C29-A05, #C-004	C29-A06, #C-005
A11	-6VDC	-6VDC	B11	GND	GND
A12	17-A11	17-A10	B12	17-A11	17-A10
A13	C28-A14, CC1-06	C28-A15, CC1-09	B13	C28-A07, CC1-02	C28-A08, CC1-03
A14	C28-A16, CC1-10	C28-A17, CC1-11	B14	C28-A05, CC1-00	C28-A06, CC1-01
A15	C28-A09, CC1-04	C28-A10, CC1-05	B15	C28-A12, CC1-06	C28-A13, CC1-07
A16	C28-A18, CC1-12	C28-A19, CC1-13	B16	C28-A20, CC1-14	C28-A22, CC1-15	
A17	C10-A23, DSWRITN	C11-A23, DSWRITN	B17	C10-B17, DSREAD	C12-B10, DSREAD
A18	C10-A18, DSREAD	C13-A20, DSREAD	B18	C10-B18, DSWRI	C12-B8, DSWRI
A19	C28-B14, CC#-08	C28-B15, CC#-09	B19	T17A05	C18-B07, 17A04
A20	17-A05	17-A04	B20	17-A05	17-A04
A21	+6VDC	+6VDC	B21	GND	GND
A22	17-A07	17-A06	B22	17-A07	17-A06
A23	C29-B12, #C-110	C29-B13, #C-111	B23	C12-B27, CW-ALM	C13-A08, SCWEMP
A24	C11-B8, PROTEK	C29-A10, #C-010	B24	C28-B16, CC#-10	C28-B17, CC#-11
A25	C28-B10, CC#-12	C28-B11, CC#-13	B25	C28-B00, CC#-14	C28-B02, CC#-15
A26	C11-A05, T17D1	C4-A10, 17A00	B26	C29-B16, #C-114	C29-B17, #C-115
A27	C29-B09, #C-108	C29-B10 #C-109	B27	C13-B03, DATAST	C12-B08, HW-INT
A28	17-A01	17-A00	B28	17-A01	17-A00
A29	17-A03	17-A02	B29	17-A03	17-A02
A30	C12-B13, HW-BRT	C12-B17, CW-RDY	B30	C29-B14, #C-112	C29-B15, #C-113
A31	+5VDC	+5VDC	B31	GND	GND
A32					

Figure 5-2. Dwg. No. 48869600, Rev. C, (72IFR)

DRAWING 48870900

Select Equipment Code

At zone 8D the equipment select toggle switches are preset by the operator. The incoming 1700 code signal is contained in Q Bits 07 through 10. When the input signal matches the preset settings, a "0" is gated out of EQOD. At the same time, the 17WEQO signal at zone 17 1/2C will be a "0" and is applied to EQO1, pin 9 as a "0". TP15 becomes a "1" and applied to 1060, pin 10. I060, pin 9, receives a Read or Write signal from the 1700 at zone 8B. I060 feeds single shot Y060.

Timing

The timing chain starts when the Q bits match the preset switch settings, W equals a "0", a Read/Write signal is present and the proper equipment protect is set up on the console. MV1 time begins when Y060 turns on and generates a pulse to energize K061, zone 5D. This pulse lasts for approximately 520 nanoseconds. At the completion of MV1 time, Y062 is triggered to produce MV2 time and energize K063. A feedback to K061, pin 1, causes a reset at the completion of MV2 time. Output pin 6 (A) is fed to the Reply circuit to develop a reply to the 1700. Ⓑ K063 is used to clock Reject Flip/Flop K073 zone 5B.

Reply/Reject

The logic is designed to generate a Reply to the 1700 or a Reject. Due to delay circuits contained in the logic, a reject will be generated more rapidly if the reply cannot be generated. Assume at zone 6C, ID72 receives CRPYRD, the signal is fed to I075 which generates a "1" to set K071 and will send out a reply when MV1 time out occurs. If I075 outputs a "0", K072 will energize to indicate a Reject signal. An RC delay network consisting of R6 and C4 provides a 50-nanosecond delay to the Reply signal which insures the coupler to strobe stable Data lines.

Read/Write

At zone 8B a 1700 Read or Write signal occurs to start the timing chain. The signal passes through the inverter stages and enters an RC network consisting of R3 and C1. The RC network extends the signal 100 nanoseconds to allow for the Reply to remain up after the Read or Write signals drop. Outputs at pins B22 and B25 are sent to the 72DIR and 72BTR boards.

NOTE

At zone 6-1/2 B AND Gate ID72, CRPYRD on Pin 10 is the Reply Enable for an Output Block transfer. On Pin 5, CWRTEN is the Reply Enable for an Input Block Transfer. Pins 12 and 2 have DIREQO which must be present for both of the above conditions.

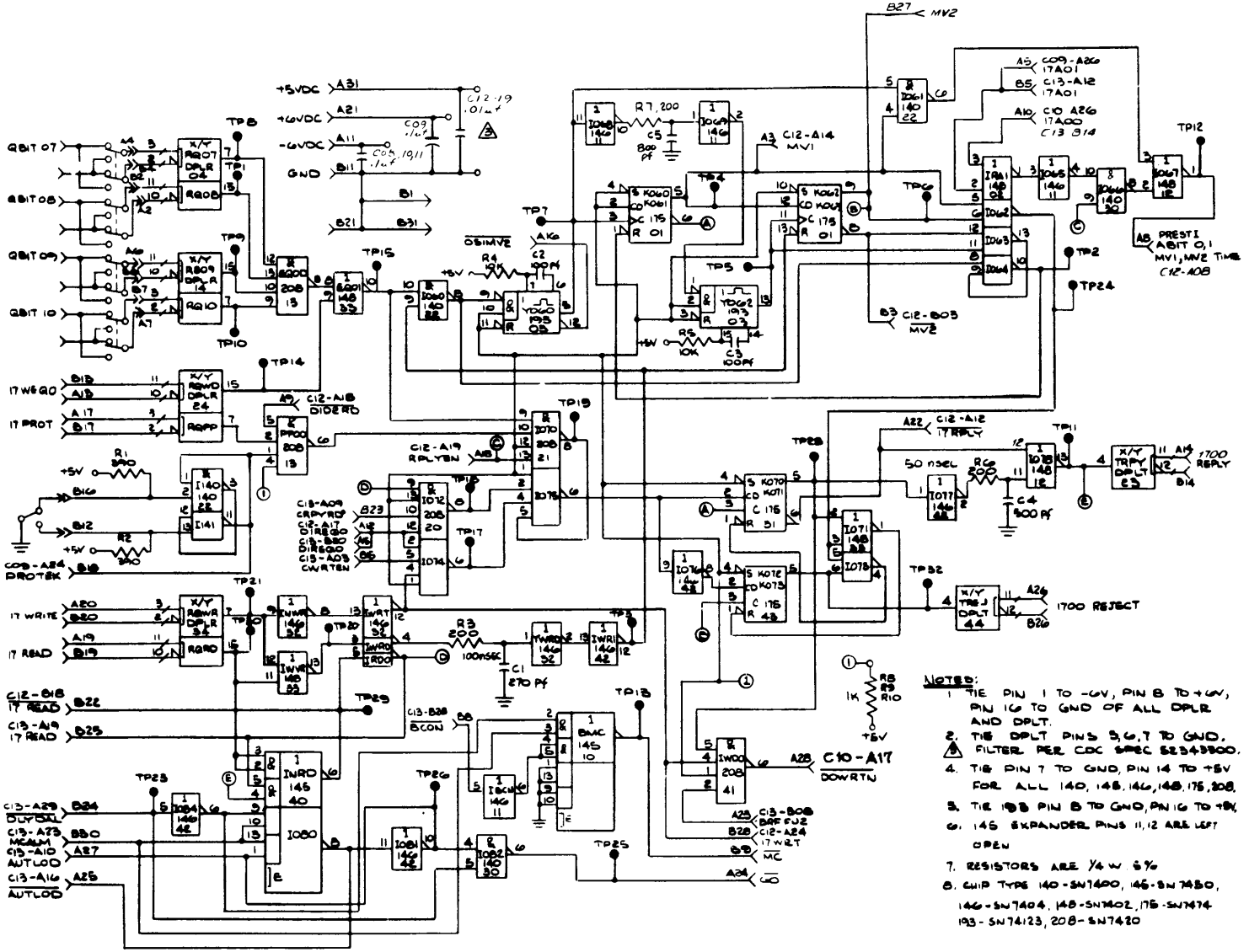


Figure 5-3. Dwg. No. 48870900, Rev. C, (72RWR)

DRAWING 48870700

Director Decode

Q bits 00 through 03 from the 1700 enter as Director Codes 0 through 9. DCDR decodes the input and feeds the four AND gates. IQ17 receives director codes 1 and 9, IQ37 receives codes 3, 5, 6, and 7, IQ24 receives codes 2 and 4, and IQ08 receives director codes 0 and 8. Director Code 1 requires only a 17 WRT signal at A24, Zone 6C, and an input on Q Bit 00 to generate a Reply Enable out of D040, pin 6 zone 5D. Directors 2 through 7 require a Ready, Write and $\overline{\text{Busy}}$ signals to generate the Reply Enable. The logic of I042, pins 4 and 5, zone 7C, senses these conditions. The Ready input is an internal BC programmed bit to I041, pin 2. Pin 4 input senses the output of Busy flip-flop K001, pin 9, zone 5D. The Busy Flip-Flop becomes set with a Ready or Write 1700 Reply signal input and a Director Code of 2 or greater. It is cleared by a BCMC or a controlware end of operation and a controlware pulse. Assume Q Bit 01 inputs a "1", it is decoded by DCDR43, applied to IQ24, gated to D020 as a "1" signal and makes the AND gate at D020 if we are Ready, $\overline{\text{Busy}}$, and have a Write signal. D020 goes to a "Ø" and gates a "1" out of D040, RPLVEN, which will generate a $\overline{\text{17RP1Y}}$ ("Ø" signal) at Ⓖ of D000. This puts Pin 6 of D000 to a "1" signal which sets K001 Busy F/F.

Buffer Full Flip-Flop

To set the Buffer Full Flip-Flop requires a 17WRT, Director 2 through 7 and a Reply. Assume Director 2 through 7 has caused a Reply Enable; I044, pin 10, zone 8C feeds I002, pin 10; pin 9 receives the 17WRT signal and pin 12 signifies Director 2 through 7. A "0" out of 1002 feeds K002 and gates a "1" out to K003, $\overline{\text{BCMC}}$ is a "1" and $\overline{\text{CRPPWR}}$ is a "1" which generates a "0" at pin 6. This generates BFRFul signal and latches K002. K003 will go to a "1" when $\overline{\text{CRPYWR}}$ goes to a "Ø" which will occur when the input block transfer is completed. A second means of clearing K002 and K003 is by controlware sending a BCMC on Pin 4 of K003.

Interrupt

When PRESTI and Reply Enable, D112, zone 5D, equal a "1", I023, zone 7B will output a "0". PRESTI is Preset Interrupt which means K011, K021, and K031 were all forced to set previous to the selected bits of the 1700 A Register being decoded. The "0" out of I023 will preset all Interrupt Flip-Flops. Assume the 1700 has selected bit A03 (End of Operation) and it is present on pin A7, zone 6B. A "1" at A03 and the D112 "1" at I020 will cause a "0" out to the Clock Data pin on K020-K021. I012 will gate a "1" at MV2 time if all previous interrupts have been cleared. I012, zone 4A, will clock K021 and reset it. Pin 6 of K021 will be a "1" to I021 and when the controlware toggles CW-EOP, I021 will gate a "0" to I022 which sends a "1" to K022 and K023, zone 4C. K023 will set when CW-PLS is toggled putting a "1" out of TINT DPLT which sends an interrupt to the 1700. At zone 3B, IINT sends an interrupt status "1" to the C10 board.

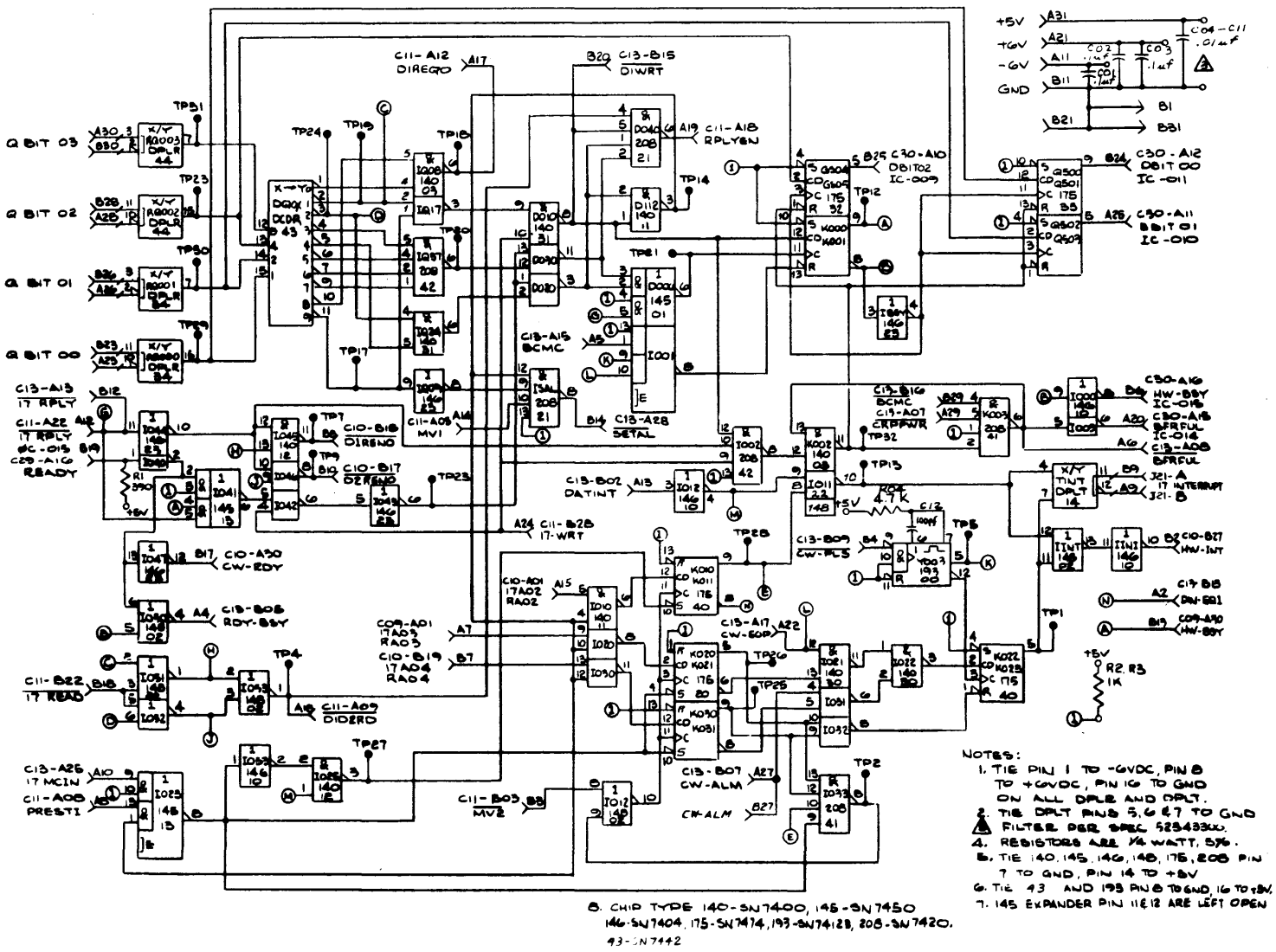


Figure 5-4. Dwg. No. 48870700, Rev. D, (72DIR)

Block Transfer Control

Before a block transfer is initiated an internal status check is completed to determine if a transfer can occur as follows.

The Buffer controller checks the CREADY line for a "1". At zone 5D, I203 input consists of RDYBSY and DATINTTIMEOUT (output of K204), I203, pin 6, becomes a "0" input to AND gate I204, pin 2. Ⓑ on I204, pin 1, completes the AND signal and pin 3 becomes a "1". I204 feeds I205 to I206, pin 4, which outputs a "1" (CREADY).

If the RDYBSY signal is lost or a data interrupt timeout occurs during a block transfer, the following will occur. The logic out of I203, I204, I205, and I206 will be reversed. The "1" out of I205 will cause a "0" out of I210 at zone 6D. I210 feeds I215 at zone 3-1/2C to cause CCTERM to become a "1" and terminate the transfer. After 40 nanoseconds, the network of I211, R10, C3, I212, and I213 will cause I215 to output a "0" and will also reset K201 or K203 via I214, pin 6. Director equals 1 and a Controller Clear or Interrupt Clear from the 1700 will also generate a CCTERM signal as follows. A bit 0 at I220, zone 7C gates a "0" to I222, DIWRT gates a "1" out of I224, which will gate a "0" out of I225 to I222. A "1" out of I222 feeds I210 and gates out a "0" to I215 causing CCTERM to become a "1".

Input Block Transfer Control

To complete an input block transfer, assume a Director 2 or greater has been issued from the 1700 and the Buffer Full Flip-Flop is set in the coupler. At zone 8D, K201 will set and feed a "1" to I229 at zone 5C. When Input Request, Buffer Full and 17RPLY equal "1", pin 8 of I229 will equal a "0" and gate "1" out of I207, pin 8. I207 feeds pin 12 of I217 to yield a "0" out (CRPYWR). CRPYWR is sent to the C12 board and clears the Buffer Full Flip-Flop. With the Buffer Full Flip-Flop reset, I227 pin 10, zone 6C yields a "0" and pin 8 will send a "1" to I201, zone 5-1/2C. The inputs to I201 are CRPYWR, BFRFUL, DIREQO or 17READ, all of which equal a "1" at this time to yield a "0" out of I201, pin 6. Pin 6 feeds I256 at zone 3C and I211 at zone 4C. I256 gates a "1" out on pin 10 which is CREPLY. A "1" out of I211, pin 11 enters an RC network of R10 and C13 which develops a 40-nanosecond time delay. After the 40-nanosecond time out, I212 feeds the signal to I213 which causes the CREPLY to drop. In addition, I213 gates a "0" out of I214, pin 6 which resets K201 Input Request Flip-Flop. This completes one complete word transfer from the 1700 to the buffer controller.

Output Block Transfer

At zone 7C, the OUTRDY signal K203, pin 5 feeds I216, zone 5C. I216 is controlled by Output Requests, OSIMVI time, 17 READ, and DIREQO signals. When a READ signal occurs from the 1700 and Director equals 0 at OSIMVI time, I216 gates a "0" to I207, zone 5C. I207 outputs a "1" which causes K206 to output a "0". K206 feeds I218 which also receives the output of K202. I218 outputs a "1" (CRPYRD). Simultaneously, K207, zone 5B equals a "0" (DORENO). DORENO is applied to C09 and C10 boards to strobe the Data lines from the coupler output channel CCO-XX to the 1700 lines. The CRPYRD signal enables REPLY to the 1700 which, in turn, drops the READ Line and gates a "1" out of I230, zone 7B. The output of I230 feeds I201, zone 4-1/2C. Pin 6 of I201 equals a "0" and enables CREPLY out of I256 (Refer to Input Request).

Autoload

Autoload can be initiated by BCON, PE-ID, MC-CC or SETAL as follows. Example, with a Director 9 from the 1700 SETAL at zone 7B goes to a "0" and gates a "1" out of I274. I274 feeds I275 and Y203, zone 5B. I275 outputs a "0" to set K209 (MCALM) which is felt on I279, pin 4. Signal Ⓑ, felt on I279 pin 5, is the AUTLOD signal. I279, pin 6 outputs a "0" to I280. I280, pin 2 outputs a "1" to I281 and I286. The outputs from I281 and I286 are "0" and the signals are STOP and CLRCH2. At Reply time, SETAL becomes a "1" and because of its RC circuit, Y203 begins a 4 USEC time pulse. At the end of Y203 time, Y204 time begins and the DYLDAL signal output goes to a "0". This signal is fed to the 72RWR Board, C11, zone 8A causing a "1" out of I084. MCALM is also a "1" and the output at I080 is a "0". In addition, I084 feeds BMC, zone 5B. A "0" out of BMC is the Master Clear signal. The "0" out of I080 is also the AUTLOD signal. I081 yields a "1" out, which is AUTOLOD. The AUTLOD signals feeds the 72BTR board, C13, and forces the STOP and CIRCH2 signals to a "1" and generates a CW-ALM status bit. The AUTLOD signals also feed the 72BTR board at zone 4C and generates the FORCE F CLRPE2 and CW-PLS signals. When Y204 times out, the DYLDAL signal returns to a "1". This causes I082 on C11, zone 6A to become a "0" or GO signal; BMC also becomes a "1" and removes MC from the line. The BCON and PE-ID signals operate in the same manner to complete Autoload.

Autoload Termination

At the completion of the load sequence an EOP-CC signal is received at zone 7Z on the 72BTR board. I278 outputs a "0" and resets K209 (MCALM) which resets the AUTLOD circuit on the 72RWR board at I080 and I081. EOP-CC will be generated by a 4096-word load, controller clear A bit 0 and Director 1 or A bit 1 Interrupt Clear and a Director 1 from the 1700. Controlware setting output channel 0, bit 13 can also clear the MCALM and AUTLOD Flip-Flops.

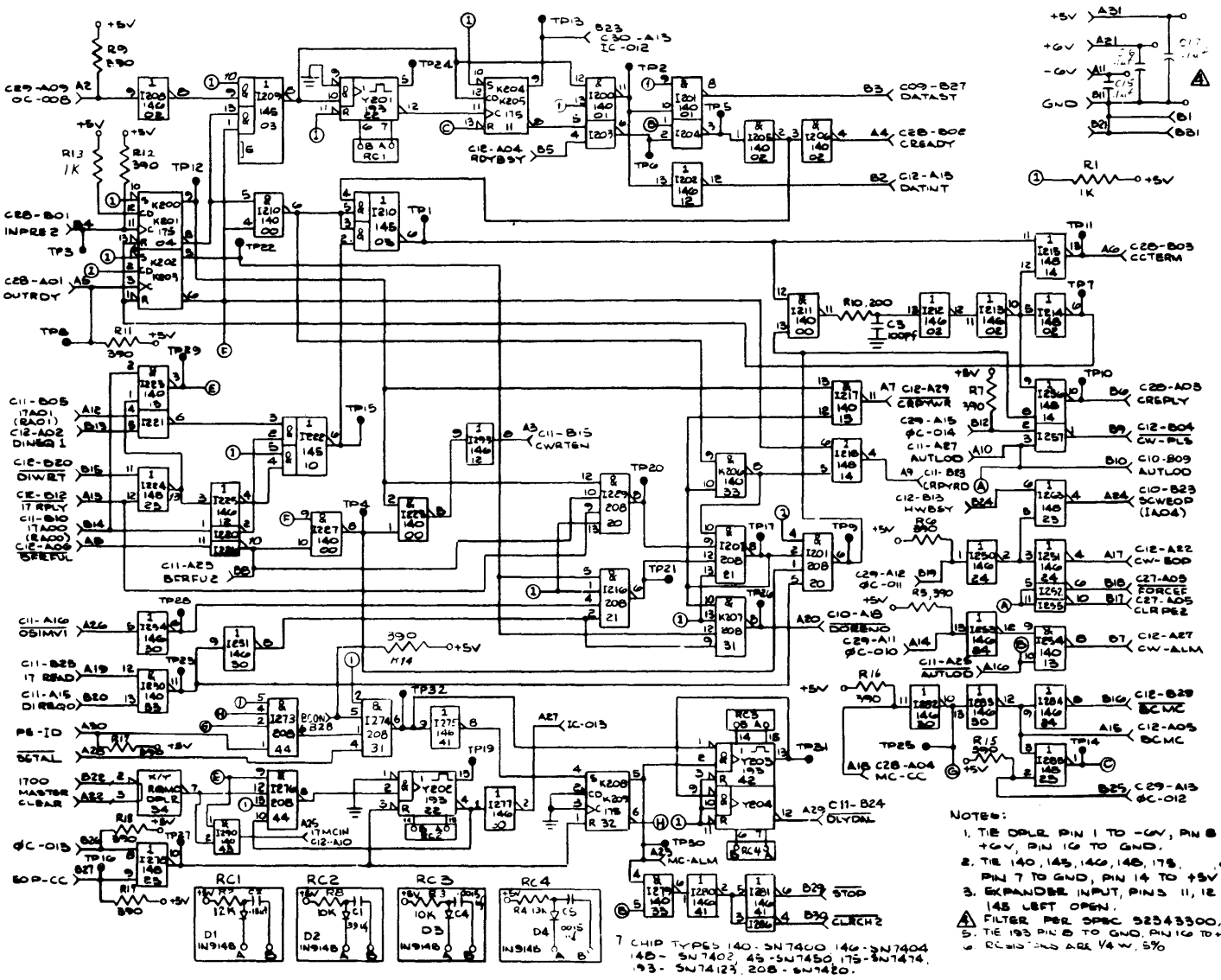


Figure 5-5. Dwg. No. 48870500, Rev. F, (72BTR)

SECTION 6

MAINTENANCE

General maintenance procedures for the Controller follow the same general routines used for other Control Data equipment. Refer to the CJ122 Page and Document Reader Hardware Reference/Customer Engineering Manual, Pub. No. 48430080 for information concerning the maintenance controls and indicators on the power control panel and the maintenance panel of the reader.

SECTION 7

MAINTENANCE AIDS

TABLE 7-1. SPECIAL TOOLS FOR CONTROLLER

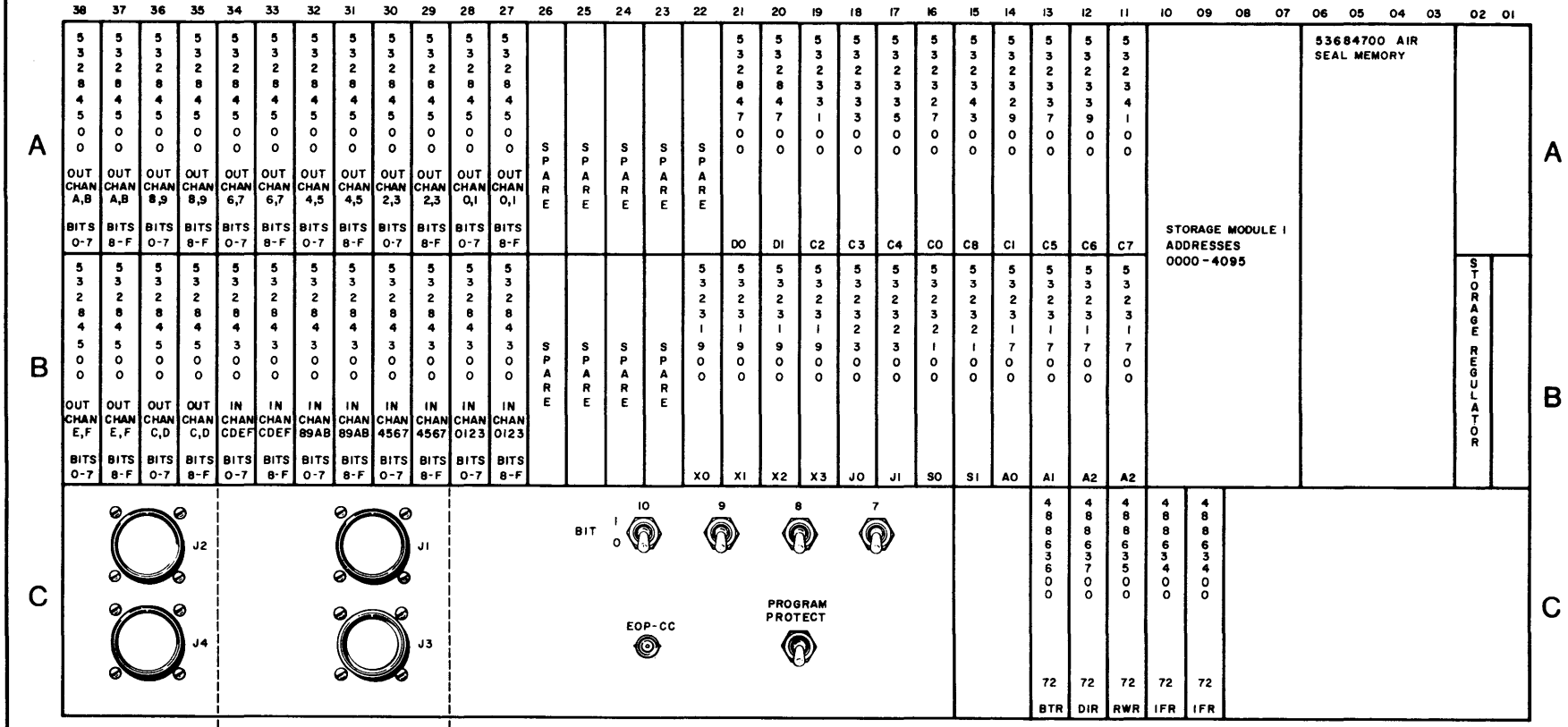
Part Number	Description	Quantity
12218402*	Wire Wrap Bit, 30 Gauge	0
12218403*	Wire Wrap Sleeve, 28-30 Gauge	0
12259111*	Wire Wrap Gun, Battery Powered	0
12269183*	Wire Unwrap Tool, 28-30 Gauge, L/R	0
18668500	Connector, Push-On	10
48446100*	Wire Stripper, (Ideal), 26-30 Gauge	0
48446200*	Wire Stripper Head, 26-30 Gauge	0
53093400	Pin Removal Tool, Plastic Block	1
53561800	Solder Removal Tool	1
53665802	Extender Board, 62 pin, TTL	1
59309500*	Maintenance Console Conversion Kit, TTL	0

* Not supplied with initial spare parts; must be ordered separately, as required.

TEST EQUIPMENT

The following test equipments, or equivalents, are used to maintain the reader:

Digital Voltmeter	-	Fairchild 7050, (CDC Part No. 18697518)
Maintenance Console, Buffer Controller	-	CDC Part No. 58021300
Oscilloscope	-	Tektronix 543 with dual-trace preamplifier, or Hewlett-Packard 180
Volt-Ohmmeter	-	Simpson 260, Series 5



NOTE:

TERMINATOR CARDS ARE LOCATED BEHIND THE MAINTENANCE PANEL.
THE BLANK 48893500 CARD ASSEMBLIES IN LOCATIONS C29, C31, AND C33 PERFORM THE FUNCTION OF INTERCONNECTING GROUND ON THE BACK PANEL OF THE OUTPUT CHANNELS.
THE 48893500 CARD ASSEMBLIES WITH CAPACITORS ARE USED FOR INPUT CHANNEL LOCATIONS C30, C32 AND C34. THE CAPACITORS REDUCE THE NOISE SUSCEPTIBILITY OF THE INPUT CHANNELS.

CONTROL DATA RABINOW ENGINEERING DIV.	TITLE: CARD PLACEMENT	PRODUCT	
		SIZE C	DRAWING NO.
		SHEET	PAGE

Figure 7-1. Card Placement

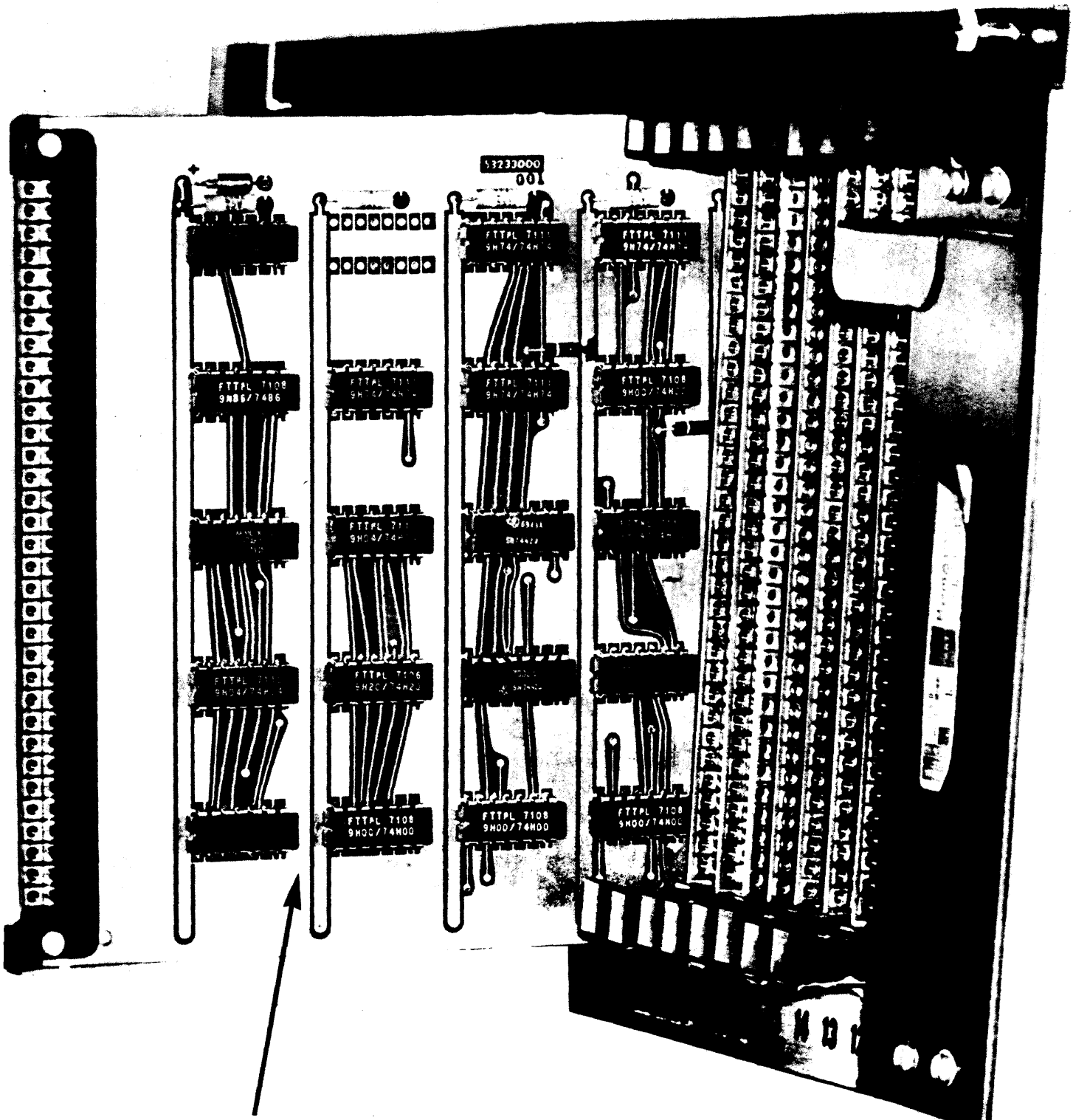


Figure 7-2. Controller Module Installation

SECTION 8

PARTS DATA

The parts data aids the customer engineer in ordering replacement parts. All assemblies, subassemblies, and parts used in the controller are illustrated in order of disassembly with their part numbers and descriptions listed. To order replacement parts, the part number and complete item description must be given.

Part information is presented in tabular format as shown in Example 1-1. The purpose of each column is described in the following paragraphs.

INDEX NUMBER

An index number, as shown in (1) of Example 1-1, is a composite of the chapter number, the figure number, and the callout number assigned to the assembly or part in the figure and list. (The callout "0", as shown in (1) of Example 1-1, is always assigned to the major assembly or figure title and is not found on the figure.)

PART NUMBER

The Control Data part number, as shown in (2) of Example 1-1, consists of eight digits and is used with the item description when ordering replacement parts. The notation "NP" appearing in the Part No. column means that the item is "not procurable" in that assembly level and must be purchased in the next higher assembly.

CHECK DIGIT

The (CD) column as shown in (3) of Example 1-1, is used for a check digit that will be used eventually in a computer program to update the parts list. It is not part of the part number and should not be used when replacement parts are ordered.

ITEM DESCRIPTION

The Item Description column is shown in (4) of Example 1-1. The relationship between parts and their next higher assembly is indicated by the level of indentation. The major assembly or figure title has an indent level of one. All assemblies and parts with an indent level of two are a part of level one; indent level three is a part of level two, etc. The indent levels are defined by using periods preceding each part description. Indent level one has no periods and is the figure title; indent level two has one period; indent level three has two periods, etc. Attaching hardware is listed under the same indent level as the item which is being attached.

Two types of figure references are used in the Item Description column:

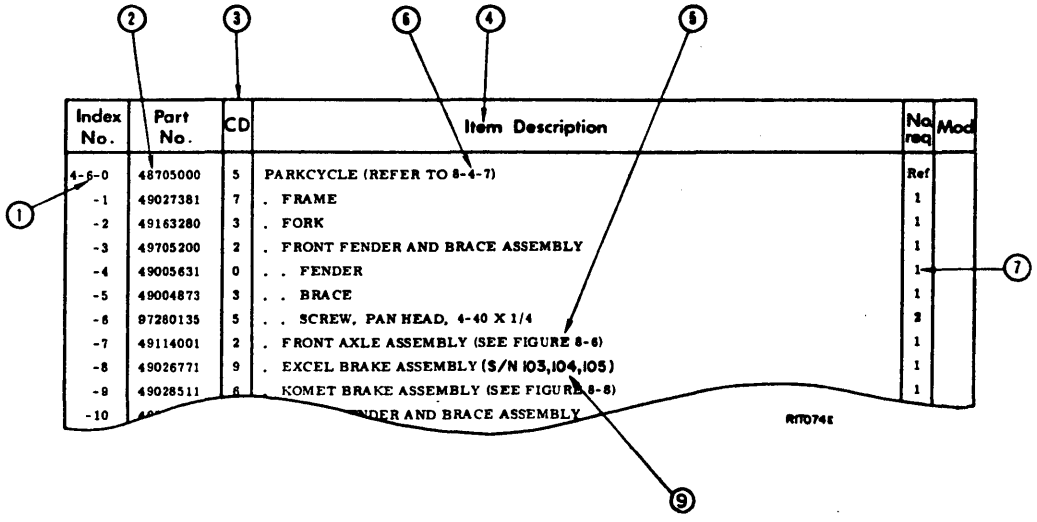
1. When an assembly is not broken down immediately after it is first listed, the statement "SEE FIGURE 8-6", as shown in (5) of Example 1-1, defines where the breakdown appears.
2. When "Ref" appears in the No. req column, the statement "REFER TO 8-4-7", as shown in (6) of Example 1-1, defines the figure where the item is shown as part of the next higher assembly. When attaching hardware appears with "Ref" but is not followed by the "REFER TO..." statement, the quantity is found in the next higher assembly.

NUMBER REQUIRED

The number shown in (7) of Example 1-1 is the quantity of the part that is required in its immediate assembly. The abbreviation "Ref" (reference) indicates that the item is called out initially on the major assembly whose figure is referenced in the Item Description column. The abbreviation A/R indicates that the part quantity is "as required" for assembly.

SERIAL NUMBER (S/N)

Machine serial numbers are shown in (9) of Example 1-1 and indicate part application. The absence of serial numbers indicates that the part is used on all equipment reflected in this volume.



Index No.	Part No.	CD	Item Description	No req	Mod
4-6-0	48705000	5	PARKCYCLE (REFER TO 8-4-7)	Ref	
-1	49027381	7	. FRAME	1	
-2	49163280	3	. FORK	1	
-3	49705200	2	. FRONT FENDER AND BRACE ASSEMBLY	1	
-4	49005631	0	. . FENDER	1	
-5	49004873	3	. . BRACE	1	
-6	97280135	5	. . SCREW, PAN HEAD, 4-40 X 1/4	2	
-7	49114001	2	. FRONT AXLE ASSEMBLY (SEE FIGURE 8-6)	1	
-8	49026771	9	. EXCEL BRAKE ASSEMBLY (S/N 103,104,105)	1	
-9	49028511	6	. KOMET BRAKE ASSEMBLY (SEE FIGURE 8-8)	1	
-10			DER AND BRACE ASSEMBLY		

RT10741

Example 1-1. Sample Parts List

CONTROLLER ASSEMBLY (S/N 151 AND UP)

Illustrations and listings of the basic controller assemblies for reader serial numbers 151 and up are contained in this chapter. Figure 8-1 locates the assemblies within the reader.

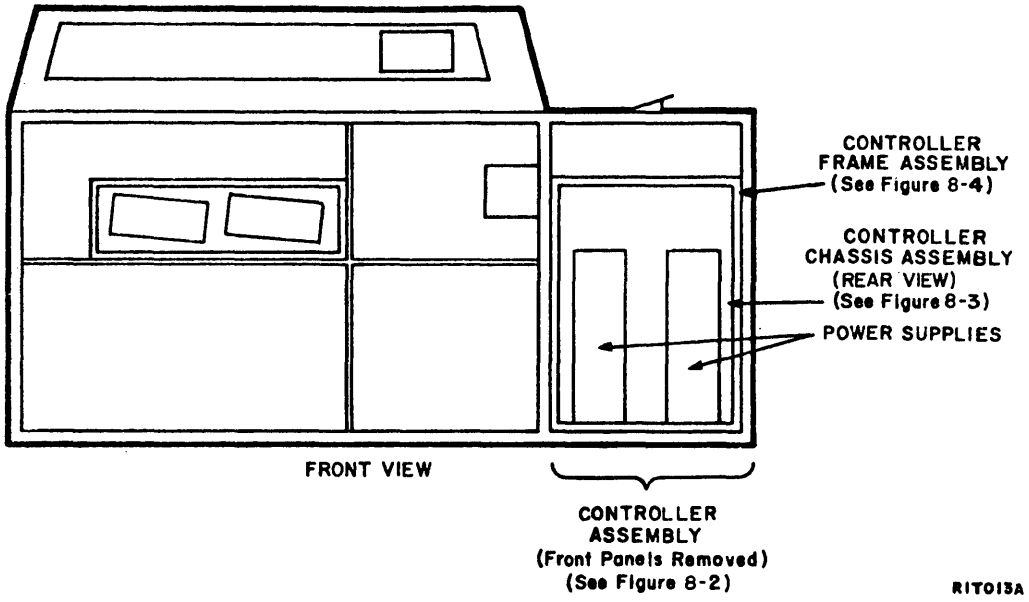


Figure 8-1. Controller Assembly (Locator)

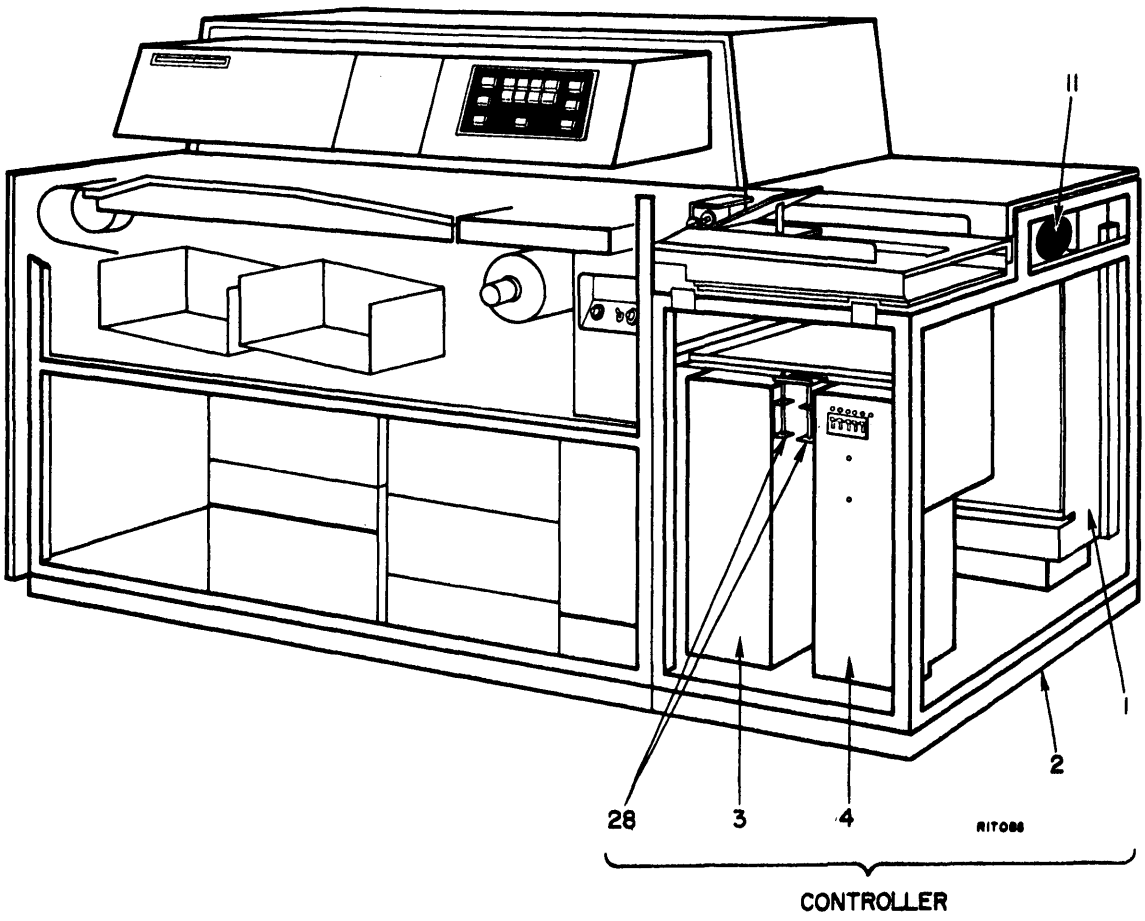
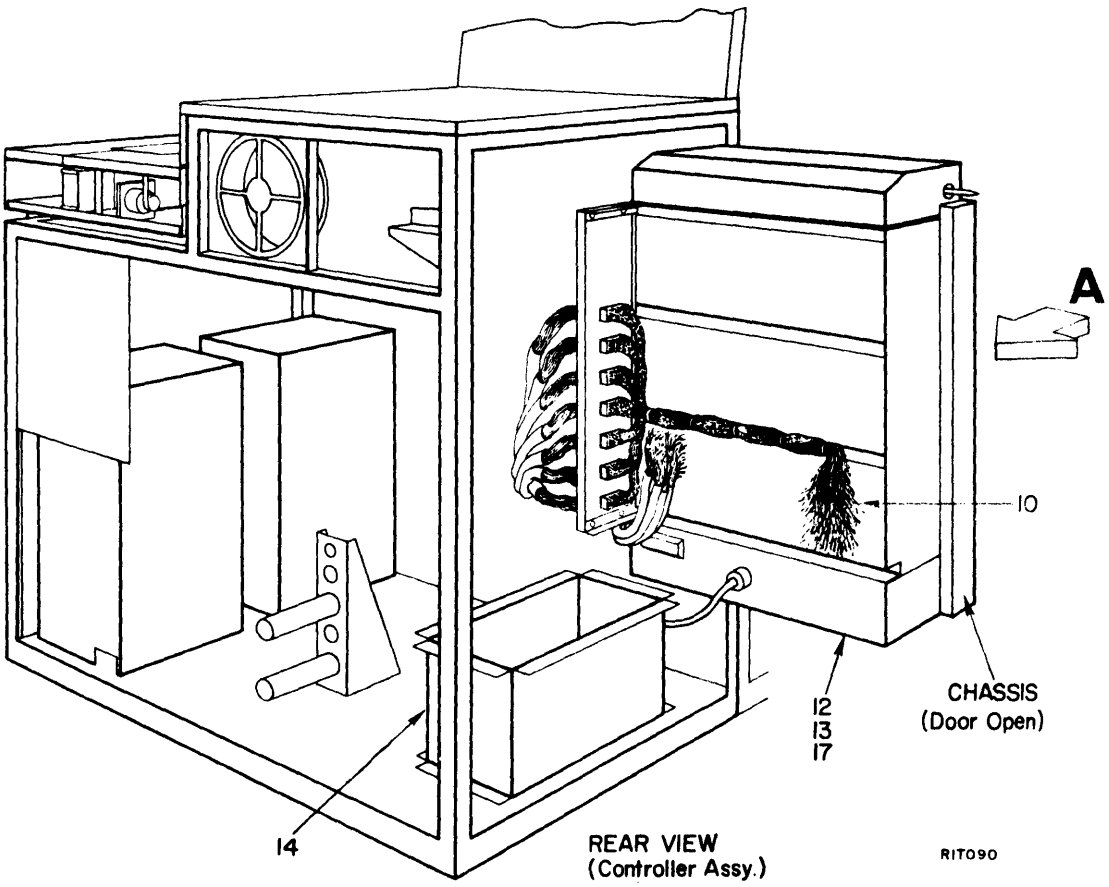


Figure 8-2. Controller Assembly (S/N 151 and Up)

Index No.	Part No.	CD	Item Description	No. req.	Mod
8-2-0	48817800	1	CONTROLLER ASSEMBLY (S/N 151 AND UP)	Ref	
-1	48818000	1	. CONTROLLER CHASSIS ASSEMBLY (SEE FIGURE 8-3)	1	
-2	48817900	3	. CONTROLLER FRAME ASSEMBLY	1	
-3	47351200	2	. REGULATOR POWER SUPPLY, FR113	1	
-4	47351000		. POWER SUPPLY, FR113	1	
-5			INTENTIONALLY BLANK		
-6	48832800	6	. CABLE, J21 INTERRUPT	1	
-7	92703005	6	. CASTER, SWIVEL	4	
-8	94931000	7	. PAD, LEVELING	4	
-9	00815411	4	. FILTER	1	
-10	94851918	6	. BEARING, FLANGED	2	
-11	94861403	7	. FAN, 115 VAC, 270 CFM	1	
-12	94861501	8	. GUARD, FINGER	1	
-13	94861502	6	. GUARD, FINGER	1	
-14	48437800	5	. COVER, CABLE	2	
-15	94862904	3	. STRIP, GROMMET	1	
-16	94869600	0	. CLAMP, FAN	3	
-17	94869601	8	. CLIP	3	
-18	24501601	9	. BLOCK, TERMINAL	1	
-19	15012412	1	. BUSHING, SNAP-IN	1	
-20	10125305	2	. NUT, HEX, 1/2-13	2	
-21	10126515	5	. SCREW, CAP, HEX, PLAIN	16	
-22	10125807	7	. WASHER, LOCK, SPRING, 5/16	16	
-23	10125302	9	. NUT, HEX, 5/16-18	16	
-24	93342324	6	. SCREW, ROUND HEAD, SLOTTED, NYLON, 10-32	2	
-25	48374200	3	. INSULATOR, PLATE	1	
-26	92615007	1	. WASHER, FIBER	4	
-27	48868800	3	. INSULATOR, BRACKET	2	
-28	25151201	8	. RIM LATCH	2	
-29	00843515		. . RING, RETAINING	3	
-30	00856000		. . KNOB	1	
-31	00856810		. . BEARING, NYLON	2	
-32	00856913		. . SPRING, COMPRESSION	1	



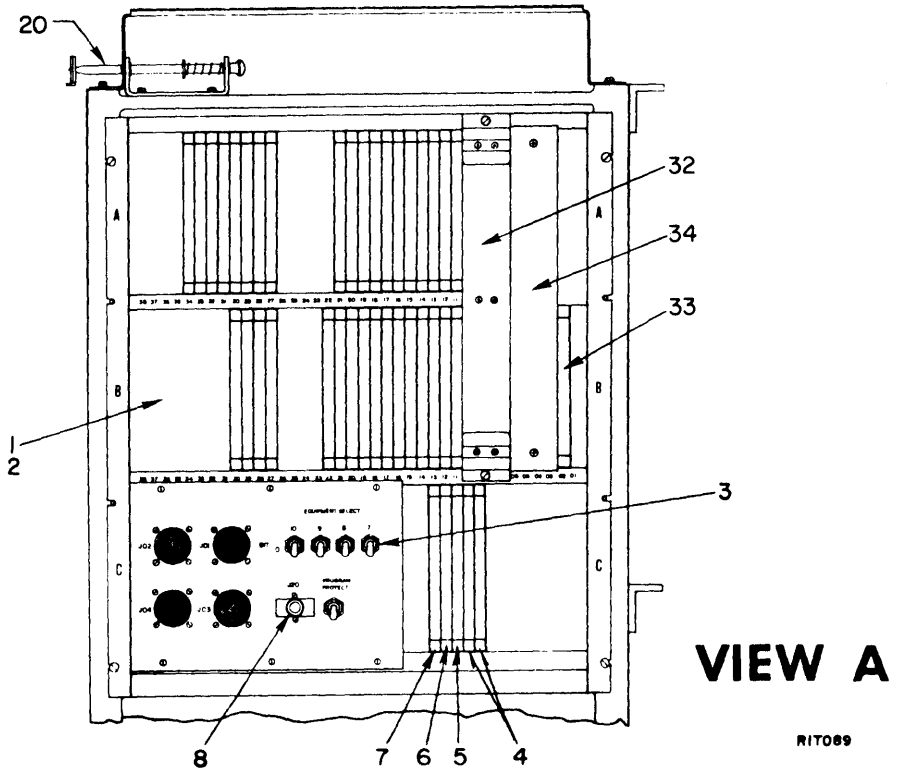


Figure 8-3. Controller Chassis Assembly

Index No.	Part No.	CD	Item Description	No. req.	Mod
8-3-0	48818000	1	CONTROLLER CHASSIS ASSEMBLY (REFER TO 8-2-1)	Ref	
-1	48831100	2	. CONTROLLER CHASSIS SUBASSEMBLY	1	
-2	48829600	5	. . BUFFER CONTROLLER, M04, MODIFIED	1	
-3	24571900	0	. . SWITCH, TOGGLE, 2 POSITION, OPDT	5	
-4	48863400	7	. . COUPLER ASSEMBLY, I/Q DTATA, PC TYPE 72IFR	2	
-5	48863500	4	. . COUPLER ASSEMBLY, 1700 I/Q CONT, PC TYPE 72RWR	1	
-6	48863700	2	. . COUPLER ASSEMBLY, 1700 DIR, PC TYPE, 72DIR	1	
-7	48863600	2	. . COUPLER ASSEMBLY, BC BLK TRFR, PC TYPE 72BTR	1	
-8	93126312	3	. . SWITCH, PUSHBUTTON, RED	1	
-9	52934110	9	. . CONNECTOR, CON-UP	3	
-10	48893200	5	. . CAPACITOR TERMINATOR BOARD	6	
-11	53784000		. . CONNECTOR, MAINT. PANEL LETTERED CONN. BLOCK	Ref	
-12	48818200		. CHASSIS, CONTROLLER	1	
-13	00815428		. FILTER	1	
-14	48817500	1	. BAFFLE, AIR	1	
-15	48817300	6	. PIN, HINGE	2	
-16	93041104		. TERMINAL STRIP, 2-3/16 INCH LONG	1	
-17	94861406	0	. FAN, REVERSIBLE AIR FLOW	3	
-18	94861505	9	. GUARD, FAN	3	
-19	93111242	9	. SPACER	4	
-20	25151201	8	. RIM LATCH	1	
-21	00843515		. . RING, RETAINING	3	
-22	00856000		. . KNOB	1	
-23	00856810		. . BEARING, NYLON	2	
-24	00856913		. . SPRING, COMPRESSION	1	
-25	10128000		. CONNECTOR, PLUG	1	
-26	30096312	1	. THERMOSTAT	1	
-27	93041108	7	. TERMINAL STRIP BARRIER TYPE, 3-15/16 INCH LONG	1	
-28	93106204		. MARKER STRIP, 2-3/16 LONG	1	
-29	93106208	7	. MARKER STRIP, 3-15/16 LONG	1	
-30	94897612	1	. SUPPORT CLAMP, CUSHIONED	1	
-31	94897618	8	. SUPPORT CLAMP, CUSHIONED	1	
-32	53670601		. BB372 4K MEMORY		
-33	53861600		. FV444A POWER REGULATOR MODULE		
-34	53250200		. AIR SEAL		

SECTION 9

WIRE LISTS

The wire lists consist of ac power wiring, dc power wiring, and cable wiring on standard corporate forms. In addition, Table 9-1 contains a Normal channel wire list in printout form. Columns one and three are ground lines and columns two and four are signal lines. Column five represents the signal name. Table 9-2 represents the back panel wire list in printout form. The first column represents origin of wires whose destinations are found in column two. Additional wiring information can be found in reference publication FR113-A Buffer Controller, Pub. No. 60335400.

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
	AC Power Wiring	WL	48869300	D
OCR DIVISION	PRODUCT FV454A TTL B.C.	SHEET 1 OF 5		

REVISION STATUS OF SHEETS												
1	2	3	4	5								
A	A	A	A	A								
B	B	B	B	A								
C	C	B	C	A								
D	C	B	D	A								

REVISIONS

REV.	ECO	DESCRIPTION	DRFT.	DATE	CHKD.	APPD.
A	4256	Class A Released	ROF	2/29/72	ZN	W.O.
B	4681	See ECO	EE	9/13/72	ZN	W.O.
C	4962	See ECO	RLC	2/2/73	RWB	W.L.O.
D	5055	See ECO	RLC	3/14/73	RWB	W.L.O.

NOTES:

COPIES TO				BY	W. Orr	DATE 2-28-72	CHKD.	ZN	DATE 3-1-72	APPD.	JW	DATE 3-9-72

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
	AC Power Wiring WIRE LISTING	WL	48869300	C
RAINBOW ENGINEERING DIVISION		SHEET 2 OF 5		

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	REMARKS
	4	16	0	48"	W11A33TB01	01	3	W39A54P03	A	5	OA
	4	16	2	48"		02	3		B	5	OB
	4	16	3	48"		03	3		C	5	OC
	4	16	6	48"		13	3		D	5	Switched A.C.
	4	16	9	48"		8	3		E	5	Neutral
	4	16	5	48"	GND	Lug	9	W39A54P03	F	5	AC GND
	2	16	5		W11A33	Shld	9	W39A33CASE	GND	9	Shield GND
	2	16	5		W11A54	Shld	9	W39A54CASE	GND	9	Shield GND
	4	16	0	48"	W11A33TB01	04	3	A54P02	A	6	Regulated OA
	4	16	2	48"		05	3		B	6	Regulated OB
	4	16	3	48"		06	3		C	6	Regulated OC
	4	16	9	48"		8	3		E	6	Neutral
	4	16	5	48"	Chassis GND	----	3	A54P02	F	6	AC GND
	2	16	5		W11A33	Shld	9	A33CASE	GND	9	Shield GND
	2	16	5		A54	Shld	9	A54CASE	GND	9	Shield GND
	8	16	0	12"	A33TB01	14	3	A33TB01	08	3	

FORM 305-2

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
RABINOW ENGINEERING DIVISION	AC Power Wiring WIRE LISTING	WL	48869300	B
		SHEET 3 OF 5		

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS. FIND NO.	REMARKS
	4	16	0	48"	A33TB01	04	3	A54P04	A	6	Regulated OA
	4	16	2	↑		05	3	↑	B	6	Regulated OB
	4	16	3	↕		06	3	↕	C	6	Regulated OC
	4	16	9	↓	A33TB01	08	3	↓	E	6	NEUT
	4	16	5	48"	CHASS GND	---	3	A54P04	F	6	AC GND
	2	16	5		A33	Shld	9	A33CASE	GND	9	Shield GND
	2	16	5		A54	Shld	9	A54CASE	GND	9	Shield GND

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
RABINOW ENGINEERING DIVISION	AC Power Wiring WIRE LISTING	WL	48869300	D
		SHEET 4 OF 5		

CONDUCTOR IDENT	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO	DESTINATION		ACCESS. FIND NO.	REMARKS
	1	16	0	40	A33TB01	09	3	A34TB01	01	3	OA
	1	16	2	40		10	3		02	3	OB
	1	16	3	40		11	3		03	3	OC
	1	16	6	40		12	3		04	3	OA C.T.
	1	16	9	40	A33TB01	8	3	A34TB01	05	3	Neutral AC Common
	1	16	5		A33SHLD	GND	9	A33CASE	GND	9	Shield GND
	1	16	5		A33SHLD	GND	9	A33CASE	GND	9	Shield GND
Cut	8	16	0	48	A33TB01	03	3	A31P22	X	3,16	FAN OC
Green	8	16	9	48	A33TB01	8	3	A31P22	Y	3,16	FAN NEUT
Wire	11	14	5	12"	A33SHLD	GND	12,14	FAN CABLE	SHLD	12,14	Cut green wire
Cut	8	16	0	48"	A33TB01	03	3	A54P23		13,15	FAN OC
Green	8	16	9	48"	A33TB01	8	3	A54P23	PLUG	13,15	FAN NEUT
Wire	11	14	5	12"	FAN CABLE	Shld	12,14	A54Frame	GND	12,14	SHLD GND
	17	16	0		A31TB02	01	3	A31J22	X	3,7	FAN OC
	18	16	9		A31TB02	02	3	A31J22	Y	3,7	FAN NEUT

FORM 385-2

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
RABINOW ENGINEERING DIVISION	AC Power Wiring	WIRE LISTING	WL 48869300	A
			SHEET 5 OF 5	

CONDUCTOR IDENT	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	REMARKS
	10		1		A31TB02	01	3	FAN			PLUG ASSEMBLY
			1		A31TB02	02	3	FAN			PLUG ASSEMBLY
	10		1		A31TB02	01	3				PLUG ASSEMBLY
			1		A31TB02	02	3				PLUG ASSEMBLY
	10		1		A31TB02	01	3				PLUG ASSEMBLY
			1		A31TB02	02	3	FAN			PLUG ASSEMBLY

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
OCR DIVISION	D.C. Power TTL P.C.	WL	488692000	H
	PRODUCT FV454 TTL B.C.		SHEET 1 OF 3	

REVISION STATUS OF SHEETS		
1	2	3
A	A	A
B	A	A
C	C	C
D	C	D
E	C	E
F	C	E
G	C	E
H	C	E

REVISIONS						
REV.	ECO	DESCRIPTION	DRFT.	DATE	CHKD.	APPD
A	4256	CLASS A RELEASED			ZW	
B	4401	SEE ECO				
C	4962	SEE ECO	RLC	2/2/73	RWB	AD6/73
D	5055	SEE ECO	RLC	3/14/73	RWB	AD6/73
E	5268	SEE ECO	MDR	6/7/73	RWB	AD7/73
F	5328	SEE ECO	MDR	7/16/73	ROF	AD1/74
G	5400	SEE ECO	MDR	7/19/73	ROF	AD1/74
H	5394	SEE ECO	MDR	7/19/73	ROF	AD1/74

NOTES:

1. SLEEVE WITH FIND #14.
2. USE FIND #15 ON ENDS OF SLEEVING.

COPIES TO				BY	W. Orr	DATE	2-28-72	CHKD.	ZW	DATE	3-1-72	APPD.	JW	DATE	3-9-72

FORM 4506

CONTROL DATA	TITLE	WL	DOCUMENT NO.	REV.
RABINOW ENGINEERING DIVISION	D. C. Power FV454A **WIRE LISTING**		48869200	H
		SHEET 2 OF 3		

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	REMARKS
	1	16	91	48"	A34TB01	12	8	A54P01	A	9	-5VDC
	2	16	92	48"		13	8		B	9	+6VDC
	3	16	3	48"		10	8		C	9	+5VDC
	4	16	920	48"		11	8		D	9	+30VDC
	1	16	91	48"		12	8		E	9	-5VDC
	3	16	3	48"		10	8		F	9	+5VDC
	4	16	920	48"		11	8		G	9	+30VDC
	2	16	92	48"		13	8		H	9	+6VDC
	5	16	0	48"		08	8		J	9	D. C. Common
	7	16	98	48"	A34TB01	14	8	A54P01	K	9	-6VDC

FORM 385-2

CONTROL DATA	TITLE	WL	DOCUMENT NO.	REV.
RABINOW ENGINEERING DIVISION	D. C. Power FV454A **WIRE LISTING**		48869200	H
		SHEET 3 OF 3		

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	REMARKS
	6	10	3	48"	A31+5V	BUSS	12	A34TB01	10	11	+5VDC
	4	16	920	48"	A31TB01	01	8		11	8	+30VDC
	7	16	98	48"		02	8		14	8	-6VDC
	2	16	92	48"		03	8		13	8	+6
	1	16	91	48"	A31TB01	04	8	A34TB01	12	8	-5VDC
	5	16	0	6	A31TB01	06	8	A31CHASSIS		8	USE EXISTING HARDWARE
	16				A31TB01	07	8, 14	A31TB01	06	8, 14	CAP
	16	20	3	8"	A31+5V	BUSS	12	A31C09	A31	13	+5VDC Back Panel
	17	20	98	8"	A31TB01	02	8	A31C09	A11	13	-6VDC
	18	20	92	5"	A31TB01	03	8	A31C09	A21	13	+6VDC
	19	20	91	16"	A31TB01	04	8	A31B04	A01	13	-5VDC
	19	20	91	16"	A31TB01	04	8	A31B08	A01	13	-5VDC
	19	20	91	22"	A31TB01	04	8	A31A15	A01	13	-5VDC
	20	20	920	15"	A31TB01	01	8	A31B02	B01	13	+30VDC
	21	20	0	60"	A31J15	E7	13	A34TB01	7	8	
	22	30	9	48"	A31 Thermostat			A31J15	A5		
		30	6	48"	A31 Thermostat			A31J15	B6		
	21	20	0	12"	A34TB01	6	8	A34TB01	9	8	
	16				A31TB01	08	8, 14	A31TB01	06	8, 14	CAP

FORM 385-2

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
	J21 INTERRUPT CABLE	WL	48832800	D
OCR DIVISION	PRODUCT FV454A TTL B.C.	SHEET 1 OF 2		

REVISION STATUS OF SHEETS	
1	2
A	A
B	A
C	A
D	A

REVISIONS						
REV.	ECO	DESCRIPTION	DRFT.	DATE	CHKD.	APPD
A	4256	CLASS A RELEASED	ROF	3-6-72	ZN	
B	4401	SEE ECO	ZN	8-17-72	ZN	AD
C	4564	SEE ECO	ZN	8-17-72	ZN	AD
D	5651A	SEE ECO	NBB	1-31-74	NB	MDB

NOTES:

1. USE 60/40 ROSIN CORE SOLDER
2. THE GROUND LEAD SHOULD BE ATTACHED FROM PIN C OF THE CONNECTOR TO THE FERRULE AND ANOTHER LEAD FROM THE FERRULE TO A CONNECTOR MOUNTING SCREW.

COPIES TO				BY	W. Orr	DATE	3-2-72	CHKD.	ROF	DATE	3-6-72	APPD.	JW MOB	DATE	3-9-72

FORM 4500

CONTROL DATA	TITLE		DOCUMENT NO.	REV.
	J21 INTERRUPT CABLE WIRE LISTING	WL	48832800	A
RABINOW ENGINEERING DIVISION		SHEET 2 OF 2		

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	REMARKS
	1	18	0	48"	J21	A	1 14	A31C12	B09	4, 5	(-) INTERRUPT
	1	18	2	48"	J21	B	1 4	A31C12	A09	4, 5	(+)
2	2	24	4	4"	J21	C	1 4, 6	A31C12	B11	2, 3, 4, 5	GROUND

FORM 389-2

TABLE 9-1. NORMAL CHANNEL WIRE LIST

J12A02	J12B02	C32A17	C32A01	IC300
C32A17	C32A02	J12A03	J12B03	IC301
J12A04	J12B04	C32A17	C32A03	IC302
C32A1A	C32A04	J12A05	J12B05	IC303
J12A06	J12B06	C32A1A	C32A05	IC304
C32A1A	C32A06	J12C02	J12D02	IC305
J12C03	J12D03	C32A27	C32A07	IC306
C32A27	C32A08	J12C04	J12D04	IC307
J12C05	J12D05	C32A27	C32A09	IC30A
C32A2A	C32A10	J12C06	J12D06	IC309
J12C07	J12D07	C32A2A	C32A11	IC310
C32A2A	C32A12	J12E01	J12F01	IC311
J12F02	J12F02	C32A29	C32A13	IC312
C32A29	C32A14	J12E06	J12F06	IC313
J12F07	J12F07	C32A29	C32A15	IC314
C32A30	C32A16	J12J01	J12K01	IC315
J12J02	J12K02	C30B1A	C30B16	IC114
C30B1A	C30B17	J12J06	J12K06	IC115
J12J07	J12K07	C30A27	C30A25	IC214
C30A27	C30A26	J12L02	J12M02	IC215
J12L03	J12M03	C32B1A	C32B16	IC414
C32B1A	C32B17	J12L04	J12M04	IC415
J12L05	J12M05	C32A30	C32A25	IC514
C32A30	C32A26	J12L06	J12M06	IC515
J12L07	J12M07	C34A17	C34A15	IC614
C34A17	C34A16	J12N02	J12P02	IC615
J12N03	J12P03	C34A17	C34B16	IC714
C34B1A	C34B17	J12N04	J12P04	IC715
J13A02	J13B02	C32B11	C32B01	IC400
C32B11	C32B02	J13A03	J13B03	IC401
J13A04	J13B04	C32B11	C32B03	IC402
C32B1A	C32B04	J13A05	J13B05	IC403
J13A06	J13B06	C32B21	C32B05	IC404
C32B21	C32B06	J13C02	J13D02	IC405
J13C03	J13D03	C32B21	C32B07	IC406
C32B2A	C32B0A	J13C04	J13D04	IC407
J13C05	J13D05	C32B2A	C32B09	IC40A
C32B2A	C32B10	J13C06	J13D06	IC409
J13C07	J13D07	C32B29	C32B12	IC410
C32B29	C32B13	J13E01	J13F01	IC411
J13F02	J13F02	C32B29	C32B14	IC412
C32B30	C32B15	J13E06	J13F06	IC413
J13E07	J13F07	C32B30	C32B19	IC500
C32B30	C32B20	J13F01	J13K01	IC501
J13J02	J13K02	C32B31	C32B22	IC502
C32B31	C32B23	J13J06	J13K06	IC503
J13J07	J13K07	C32B31	C32B24	IC504
C32A31	C32B25	J13L02	J13M02	IC505
J13L03	J13M03	C32A31	C32B26	IC506
C32A31	C32B27	J13L04	J13M04	IC507
J13L05	J13M05	C30A30	C32A19	IC50A
C30A30	C32A20	J13L06	J13M06	IC509
J13L07	J13M07	C30A30	C32A21	IC510
C30A31	C32A22	J13N02	J13P02	IC511
J13N03	J13P03	C30A31	C32A23	IC512
C30A31	C32A24	J13N04	J13P04	IC513
J14A02	J14B02	C34A1A	C34A01	IC600
C34A1A	C34A02	J14A03	J14B03	IC601
J14A04	J14B04	C34A1A	C34A03	IC602
C34A27	C34A04	J14A05	J14B05	IC603
J14A06	J14B06	C34A27	C34A05	IC604
C34A27	C34A06	J14C02	J14D02	IC605

TABLE 9-1. NORMAL CHANNEL WIRE LIST (CONT'D)

J14C03	J14D03	C34A28	C34A07	IC606
C34A2A	C34A08	J14C04	J14D04	IC607
J14C05	J14D05	C34A28	C34A09	IC608
C34A29	C34A10	J14C06	J14D06	IC609
J14C07	J14D07	C34A29	C34A11	IC610
C34A29	C34A12	J14E01	J14F01	IC611
J14E02	J14F02	C34A30	C34A13	IC612
C34A30	C34A14	J14E06	J14F06	IC613
J14E07	J14F07	C34B18	C34B01	IC700
C34B1A	C34B02	J14J01	J14K01	IC701
J14J02	J14K02	C34B11	C34B03	IC702
C34B11	C34B04	J14J06	J14K06	IC703
J14J07	J14K07	C34B11	C34B05	IC704
C34B2A	C34B06	J14L02	J14M02	IC705
J14L03	J14M03	C34B28	C34B07	IC706
C34B2A	C34B08	J14L04	J14M04	IC707
J14L05	J14M05	C34B29	C34B09	IC708
C34B29	C34B10	J14L06	J14M06	IC709
J14L07	J14M07	C34B29	C34B12	IC710
C34B30	C34B13	J14N02	J14P02	IC711
J14N03	J14P03	C34B30	C34B14	IC712
C34B30	C34B15	J14N04	J14P04	IC713
J15A02	J15B02	C29B21	C29B19	0C200
C29B21	C29B20	J15A03	J15B03	0C201
J15A04	J15B04	C29B21	C29B22	0C202
C29B2A	C29B23	J15A05	J15B05	0C203
J15C02	J15D02	C29B2A	C29B24	0C204
C29B2A	C29B25	J15C03	J15D03	0C205
J15C04	J15D04	C29B29	C29B26	0C206
C29B29	C29B27	J15C05	J15D05	0C207
J15C06	J15D06	C11B21	C11A30	NBCON
C31A17	C31A01	J15C07	J15D07	0C300
J15E01	J15F01	C31A17	C31A02	0C301
C31A17	C31A03	J15E02	J15F02	0C302
J15E06	J15F06	C31A1A	C31A04	0C303
C31A1A	C31A05	J15J01	J15K01	0C304
J15J02	J15K02	C31A27	C31A06	0C305
C31A27	C31A07	J15J06	J15K06	0C306
J15J07	J15K07	C31A27	C31A0A	0C307
C10B11	C10B09	J15L02	J15M02	AUTLOD
J15L03	J15M03	C31B11	C31B01	0C400
C31B11	C31B02	J15L04	J15M04	0C401
J15L05	J15M05	C31B11	C31B03	0C402
C31B1A	C31B04	J15L06	J15M06	0C403
J15N02	J15P02	C31B1A	C31B05	0C404
C31B1A	C31B06	J15N03	J15P03	0C405
J15N04	J15P04	C31B30	C31B07	0C406
C31B30	C31B08	J15N05	J15P05	0C407
J16A02	J16B02	C29A17	C29A19	0C208
C29A17	C29A20	J16A03	J16B03	0C209
J16A04	J16B04	C29A17	C29A21	0C210
C29A1A	C29A22	J16A05	J16B05	0C211
J16C02	J16D02	C29A1A	C29A23	0C212
C29A1A	C29A24	J16C03	J16D03	0C213
J16C04	J16D04	C29A27	C29A25	0C214
C29A27	C29A27	J16C05	J16D05	0C215
J16C07	J16D07	C31A28	C31A09	0C308
C31A2A	C31A10	J16E01	J16F01	0C309
J16E02	J16F02	C31A28	C31A11	0C310
C31A29	C31A12	J16E06	J16F06	0C311
J16J01	J16K01	C31A29	C31A13	0C312
C31A29	C31A14	J16J02	J16K02	0C313

TABLE 9-1. NORMAL CHANNEL WIRE LIST (CONT'D)

J16J06	J16K06	C31A30	C31A15	0C314
C31A30	C31A16	J16J07	J16K07	0C315
J16L03	J16M03	C31B21	C31B09	0C408
C31B21	C31B10	J16L04	J16M04	0C409
J16L05	J16M05	C31B21	C31B12	0C410
C31B28	C31B13	J16L06	J16M06	0C411
J16N02	J16P02	C31B28	C31B14	0C412
C31B28	C31B15	J16N03	J16P03	0C413
J16N04	J16P04	C31B29	C31B16	0C414
C31B29	C31B17	J16N05	J16P05	0C415
J17A02	J17B02	C31B29	C31B19	0C500
C31B30	C31B20	J17A03	J17B03	0C501
J17A04	J17B04	C30B30	C31B22	0C502
C30B31	C31B23	J17A05	J17B05	0C503
J17C02	J17D02	C31B31	C31B24	0C504
C31B31	C31B25	J17C03	J17D03	0C505
J17C04	J17D04	C31B31	C31B26	0C506
C30B31	C31B27	J17C05	J17D05	0C507
J17C07	J17D07	C33A17	C33A01	0C600
C33A17	C33A02	J17E01	J17F01	0C601
J17F02	J17E02	C33A17	C33A03	0C602
C33A18	C33A04	J17E04	J17F04	0C603
J17J01	J17K01	C33A18	C33A05	0C604
C33A18	C33A06	J17J02	J17K02	0C605
J17J05	J17K06	C33A27	C33A07	0C606
C33A27	C33A08	J17J07	J17K07	0C607
J17L03	J17M03	C33B11	C33B01	0C700
C33B11	C33B02	J17L04	J17M04	0C701
J17L05	J17M05	C33B11	C33B03	0C702
C33B18	C33B04	J17L06	J17M06	0C703
J17N02	J17P02	C33B18	C33B05	0C704
C33B18	C33B06	J17N03	J17P03	0C705
J17N04	J17P04	C33B21	C33B07	0C706
C33B22	C33B08	J17N05	J17P05	0C707
J18A02	J18A02	C31A30	C31A19	0C508
C31A31	C31A20	J18A03	J18B03	0C509
J18A04	J18B04	C31A31	C31A21	0C510
C31A31	C31A22	J18A05	J18B05	0C511
J18C02	J18D02	C30B28	C31A23	0C512
C30B28	C31A24	J18C03	J18D03	0C513
J18C04	J18D04	C30B28	C31A25	0C514
C30B29	C31A26	J18C05	J18D05	0C515
J18C07	J18D07	C33A27	C33A09	0C608
C33A28	C33A10	J18E01	J18F01	0C609
J18F02	J18F02	C33A28	C33A11	0C610
C33A28	C33A12	J18E04	J18F04	0C611
J18J01	J18K01	C33A29	C33A13	0C612
C33A29	C33A14	J18J02	J18K02	0C613
J18J05	J18K06	C33A29	C33A15	0C614
C33A30	C33A16	J18J07	J18K07	0C615
J18L03	J18M03	C33B21	C33B09	0C708
C33B28	C33B10	J18L04	J18M04	0C709
J18L05	J18M05	C33B28	C33B12	0C710
C33B28	C33B13	J18L06	J18M06	0C711
J18N02	J18P02	C33B29	C33B14	0C712
C33B29	C33B15	J18N03	J18P03	0C713
J18N04	J18P04	C33B29	C33B16	0C714
C33B30	C33B17	J18N05	J18P05	0C715

TABLE 9-2. BACK PANEL WIRE LIST

C05A01	C06A01
C05A02	C06A02
C05A03	C06A03
C05A04	C06A04
C05A05	C06A05
C05A06	C06A06
C05A07	C06A07
C05A08	C16A01
C05A09	C16A03
C05A10	C16A05
C05A12	C16A07
C05A13	C06A13
C05A14	C06A14
C05A15	C06A15
C05A16	C06A16
C05A17	C06A17
C05A18	C06A18
C05A19	C06A19
C05A20	C06A20
C05A21	C06A21
C05A22	C06A22
C05A23	C06A23
C05A24	C06A24
C05A25	C06A25
C05A26	C06A26
C05A27	C06A27
C05A28	C06A28
C05A29	C06A29
C05A30	C06A30
C05A31	C06A31
C05A31	C06A31
C05B01	C06B01
C05B02	C06B02
C05B03	C06B03
C05B04	C06B04
C05B05	C06B05
C05B06	C06B06
C05B07	C06B07
C05B08	C16B01
C05B09	C16B03
C05B10	C16B05
C05B12	C16B07
C05B13	C06B13
C05B14	C06B14
C05B15	C06B15
C05B16	C06B16
C05B17	C06B17
C05B18	C06B18
C05B19	C06B19
C05B20	C06B20
C05B21	C06B21
C05B22	C06B22
C05B23	C06B23
C05B24	C06B24
C05B25	C06B25
C05B26	C06B26
C05B27	C06B27
C05B28	C06B28
C05B29	C06B29
C05B30	C06B30
C05B31	C06B31
C05B31	C06B31
C06A01	C12B23
C06A02	C12B26
C06A03	C12B28
C06A04	C12A30
C06A08	C16A02
C06A09	C16A04
C06A10	C16A06
C06A12	C16A08
C06A18	C11A19
C06A19	C11A20
C06A20	C13B22
C06A21	C11B17
C06A30	C11A13
C06A31	C07A31
C06B01	C12A23
C06B02	C12A26
C06B03	C12A28
C06B04	C12B30
C06B08	C16B02
C06B09	C16B04
C06B10	C16B06
C06B12	C16B08
C06B18	C11B19
C06B19	C11B20
C06B20	C13A22
C06B21	C11A17
C06B30	C11B13
C06B31	C07B31
C07A01	C08A01
C07A02	C08A02
C07A03	C08A03
C07A04	C08A04
C07A05	C08A05
C07A06	C08A06
C07A07	C08A07
C07A08	C08A08
C07A09	C08A09

TABLE 9-2. BACK PANEL WIRE LIST (CONT'D)

C07A10	C08A10	C07B31	C08B31
C07A12	C08A12	C07B31	C08B31
C07A13	C08A13	C08A01	C10B28
C07A14	C08A14	C08A02	C09B28
C07A15	C08A15	C08A03	C10A29
C07A16	C08A16	C08A04	C09A29
C07A17	C08A17	C08A05	C10A20
C07A18	C08A18	C08A06	C09A20
C07A19	C08A19	C08A07	C10A22
C07A20	C08A20	C08A08	C09A22
C07A21	C08A21	C08A09	C10B08
C07A22	C08A22	C08A10	C09B08
C07A23	C08A23	C08A12	C10A12
C07A24	C08A24	C08A13	C09A12
C07A25	C08A25	C08A14	C10B03
C07A26	C08A26	C08A15	C09B03
C07A27	C08A27	C08A16	C10A06
C07A28	C08A28	C08A17	C09A06
C07A29	C08A29	C08A18	C11A14
C07A30	C08A30	C08A19	C11A26
C07A31	C08A31	C08A31	C16A31
C07A31	C08A31	C08B01	C10A28
C07B02	C08B02	C08B02	C09A28
C07B03	C08B03	C08B03	C10B29
C07B04	C08B04	C08B04	C09B29
C07B05	C08B05	C08B05	C10B20
C07B06	C08B06	C08B06	C09B20
C07B07	C08B07	C08B07	C10B22
C07B08	C08B08	C08B08	C09B22
C07B09	C08B09	C08B09	C10A08
C07B10	C08B10	C08B10	C09A08
C07B12	C08B12	C08B12	C10B12
C07B13	C08B13	C08B13	C09B12
C07B14	C08B14	C08B14	C10A03
C07B15	C08B15	C08B15	C09A03
C07B16	C08B16	C08B16	C10B06
C07B17	C08B17	C08B17	C09B06
C07B18	C08B18	C08B18	C11B14
C07B19	C08B19	C08B19	C11B26
C07B20	C08B20	C08B31	C16B31
C07B21	C08B21	C09A01	C12A07
C07B22	C08B22	C09A02	C28B05
C07B23	C08B23	C09A04	C29A01
C07B24	C08B24	C09A05	C29B05
C07B25	C08B25	C09A07	C28B12
C07B26	C08B26	C09A09	C28B09
C07B27	C08B27	C09A10	C29B07
C07B28	C08B28	C09A11	C10A11
C07B29	C08B29	C09A13	C28A14
C07B30	C08B30	C09A14	C28A16

TABLE 9-2. BACK PANEL WIRE LIST (CONT'D)

C09A15	C28A09
C09A16	C28A18
C09A17	C10A17
C09A18	C10A18
C09A19	C28B14
C09A21	C10A21
C09A23	C29B12
C09A24	C11B18
C09A25	C28B18
C09A26	C11A05
C09A27	C29B09
C09A30	C12B13
C09A31	C10A31
C09B02	C28B07
C09B04	C29A03
C09B05	C29B01
C09B07	C29B03
C09B09	C29A07
C09B10	C29A05
C09B11	C10B11
C09B13	C28A07
C09B14	C28A05
C09B15	C28A12
C09B16	C28A20
C09B17	C10B17
C09B18	C10B18
C09B21	C10B21
C09B23	C12B27
C09B24	C28B16
C09B25	C28B20
C09B26	C29B16
C09B27	C13B03
C09B30	C29B14
C10A01	C12A15
C10A02	C28B06
C10A04	C29A02
C10A05	C29B06
C10A07	C28B13
C10A09	C28B10
C10A10	C29B08
C10A11	C11A11
C10A13	C28A15
C10A14	C28A17
C10A15	C28A10
C10A16	C28A19
C10A17	C11A28
C10A18	C13A20
C10A19	C28B15
C10A21	C11A21
C10A23	C29B13
C10A24	C29A10
C10A25	C28B19
C10A26	C11A10
C10A27	C29B10
C10A30	C12B17
C10A31	C11A31
C10B02	C28B08
C10B04	C29A04
C10B05	C29B02
C10B07	C29B04
C10B09	C13B10
C10B10	C29A06
C10B11	C11B11
C10B13	C28A08
C10B14	C28A06
C10B15	C28A13
C10B16	C28A22
C10B17	C12B10
C10B18	C12B08
C10B19	C12B07
C10B21	C11B21
C10B23	C13A24
C10B24	C28B17
C10B25	C28B22
C10B26	C29B17
C10B27	C12B02
C10B30	C29B15
C11A02	C16B13
C11A03	C12A14
C11A04	C16A12
C11A06	C16A14
C11A07	C16B15
C11A08	C12A08
C11A09	C12A18
C11A10	C13B14
C11A11	C12A11
C11A12	C12A17
C11A15	C13B20
C11A16	C13A26
C11A18	C12A19
C11A21	C12A21
C11A22	C12A12
C11A23	C13B08
C11A24	C27A01
C11A25	C13A16
C11A27	C13A10
C11A31	C12A31
C11B02	C16A13
C11B03	C12B03
C11B04	C16B12

TABLE 9-2. BACK PANEL WIRE LIST (CONT'D)

C11B05	C13A12	C13A30	C27A06
C11B06	C16B14	C13A31	C30A31
C11B07	C16A15	C13B04	C28B01
C11B08	C13B28	C13B06	C28A03
C11B09	C27B02	C13B11	C23B11
C11B11	C12B11	C13B12	C29A15
C11B12	C16A16	C13B17	C27A05
C11B15	C13A03	C13B18	C27A03
C11B16	C16B16	C13B19	C29A12
C11B21	C12B21	C13B21	C16A11
C11B22	C12B18	C13B23	C30A13
C11B23	C13A09	C13B25	C29A13
C11B24	C13A29	C13B26	C29A14
C11B25	C13A19	C13B27	C16A09
C11B28	C12A24	C13B29	C27B01
C11B30	C13A23	C13B30	C27B04
C12A02	C13B13	C16A11	C23B21
C12A04	C13B05	C16B09	C27A04
C12A05	C13A15	C26B03	C27B03
C12A06	C13A08	C30A31	C32A31
C12A10	C13A25	C32A31	C34A31
C12A11	C13A11		
C12A13	C13B02		
C12A20	C30A15		
C12A21	C13A21		
C12A22	C13A17		
C12A25	C30A11		
C12A27	C13B07		
C12A29	C13A07		
C12A31	C13A31		
C12B04	C13B09		
C12B06	C30A16		
C12B11	C13B11		
C12B12	C13A13		
C12B13	C13B24		
C12B14	C13A28		
C12B19	C29A16		
C12B20	C13B15		
C12B21	C13B21		
C12B24	C30A12		
C12B25	C30A10		
C12B29	C13B16		
C13A02	C29A09		
C13A04	C28B02		
C13A05	C28A01		
C13A06	C28B03		
C13A14	C29A11		
C13A18	C28A04		
C13A27	C30A14		

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
7	1	48"	A1	6	A31C05	A01	36,37	Q Bit 00
	92	↑	A2	↑	↑	B01	↑	
8	1		A3			A02		01
	94		A4			B02		
9	1		A5			A03		02
	96		A6			B03		
10	1		A7			A04		03
	98		A8			B04		
11	1		A9			A05		04
	90		A10			B05		
12	2		B1			A06		05
	92		B2			B06		
13	2		B3			A07		06
	94		B4			B07		
14	2		B5			A08		07
	96		B6			B08		
15	2		B7			A09		08
	98		B8			B09		
16	2		B9			A10		09
	90		B10			B10		
17	3		C1			A12		10
	92		C2			B12		
18	3		C3			A13		11
	94		C4			B13		
19	3		C5			A14		12
	96		C6			B14		
20	3		C7			A15		13
	98		C8			B15		
21	3	↓	C9	↓	↓	A16	↓	Q Bit 14
	90	48"	C10	6	A31C05	B16	36,37	

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
22	4	48"	D1	6	A31C05	A17	36,37	
	92	↑	D2	↑	↑	B17	↑	Q Bit 15
23	4		D3			A18		
	94		D4			B18		READ
24	4		D5			A19		
	96		D6			B19		WRITE
25	4		D7			A20		
	98		D8			B20		1700-MC
26	4		D9			A21		
	90		D10			B21		PROG-PROTECT
27	5		E1			A22		BUFFER
	92		E2			B22		ACTIVE
28	5		E3			A23		
	94		E4			B23		TIMING
29	5		E5			A24		
	96		E6			B24		
30	5		E7			A25		
	98		E8			B25		
31	5		E9			A26		
	90		E10			B26		
32	6		F1			A27		
	92		F2			B27		
33	6		F3			A28		
	94		F4			B28		
34	6		F5			A29		
	96		F6		↓	B29		
35	6		F7			A30		
	98		F8		A31C05	B30		W=0
3	2	↓	F9	↓	TB C05	A31	↓	+20
2	6	48"	F10	6	TB C05	B31	36,37	-20
	0		61		TB			GRD

UNLESS OTHERWISE SPECIFIED
ALL WIRES TO BE 24 GAUGE

CONTROL DATA CORPORATION

TITLE
61-PIN CONNECTOR CABLE ASSEMBLY
J05-Q

PRODUCT
FV454

SIZE	DRAWING NO.	REV
A	48831700	A

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AA 2026

PRINTED IN U.S.A.

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
7	1	48"	A1	6	A31C06	A01	36,37	Q Bit 00
	92	↑	A2	↑	↑	B01	↑	
8	1		A3			A02		01
	94		A4			B02		
9	1		A5			A03		02
	96		A6			B03		
10	1		A7			A04		03
	98		A8			B04		
11	1		A9			A05		04
	90		A10			B05		
12	2		B1			A06		05
	92		B2			B06		
13	2		B3			A07		06
	94		B4			B07		
14	2		B5			A08		07
	96		B6			B08		
15	2		B7			A09		08
	98		B8			B09		
16	2		B9			A10		09
	90		B10			B10		
17	3		C1			A12		10
	92		C2			B12		
18	3		C3			A13		11
	94		C4			B13		
19	3		C5			A14		12
	96		C6			B14		
20	3		C7			A15		13
	98		C8			B15		
	3	↓	C9	↓	↓	A16	↓	
21	90	48"	C10	6	A31C06	B16	36,37	Q Bit 14

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
22	4	48"	D1	6	A31C06	A17	36,37	
	92	↑	D2	↑	↑	B17	↑	Q Bit 15
23	4		D3			A18		
	94		D4			B18		READ
24	4		D5			A19		
	96		D6			B19		WRITE
25	4		D7			A20		
	98		D8			B20		1700-MC
26	4		D9			A21		
	90		D10			B21		PROG-PROTECT
27	5		E1			A22		BUFFER
	92		E2			B22		ACTIVE
28	5		E3			A23		
	94		E4			B23		TIMING
29	5		E5			A24		
	96		E6			B24		
30	5		E7			A25		
	98		E8			B25		
31	5		E9			A26		
	90		E10			B26		
32	6		F1			A27		
	92		F2			B27		
33	6		F3			A28		
	94		F4			B28		
34	6		F5			A29		
	96		F6		↓	B29		
35	6		F7			A30		
	98		F8		A31C06	B30		W=0
3	2	↓	F9	↓	TB C06	A31	↓	+20
2	6	48"	F10	6	TB C06	B31	36,37	-20
	0		61		TB			GRD

UNLESS OTHERWISE SPECIFIED
ALL WIRES TO BE 24 GAUGE

CONTROL DATA

TITLE
61-PIN CONNECTOR CABLE ASSEMBLY
J06-Q

PRODUCT
FV454

SIZE	DRAWING NO.	REV
A	48831800	A

	SHEET	PAGE

AA 2026

PRINTED IN U.S.A.

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
7	1	48"	A1	6	A31C07	A01	3637	A DATA Bit 00
	92	↑	A2	↑		B01	↑	
8	1		A3			A02		01
	94		A4			B02		
9	1		A5			A03		02
	96		A6			B03		
10	1		A7			A04		03
	98		A8			B04		
11	1		A9			A05		04
	90		A10			B05		
12	2		B1			A06		05
	92		B2			B06		
13	2		B3			A07		06
	94		B4			B07		
14	2		B5			A08		07
	96		B6			B08		
15	2		B7			A09		08
	98		B8			B09		
16	2		B9			A10		09
	90		B10			B10		
17	3		C1			A12		10
	92		C2			B12		
18	3		C3			A13		11
	94		C4			B13		
19	3		C5			A14		12
	96		C6			B14		
20	3		C7			A15		13
	98		C8			B15		
21	3	↓	C9	↓		A16	↓	A DATA Bit 14
	90	48"	C10	6	A31C07	B16	3637	

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
22	4	48"	D1	6	A31C07	A17	3637	A DATA Bit 15
	92	↑	D2	↑		B17	↑	
23	4		D3			A18		REPLY
	94		D4			B18		
24	4		D5			A19		REJECT
	96		D6			B19		
25	4		D7			A20		PRIORITY
	98		D8			B20		
26	4		D9			A21		
	90		D10			B21		
27	5		E1			A22		
	92		E2			B22		
28	5		E3			A23		
	94		E4			B23		
29	5		E5			A24		
	96		E6			B24		
30	5		E7			A25		
	98		E8			B25		
31	5		E9			A26		
	90		E10			B26		
32	6		F1			A27		
	92		F2			B27		
33	6		F3			A28		
	94		F4			B28		
34	6		F5			A29		
	96		F6			B29		
35	6		F7			A30		
	98		F8		A31C07	B30		
3	2	V	F9	↓	TB C07	A31	↓	+20
2	6	48"	F10	6	TB C07	B31	3637	-20
	0		61		TB			GRD

UNLESS OTHERWISE SPECIFIED
ALL WIRES TO BE 24 GAUGE

CONTROL DATA
CORPORATION

TITLE
61-PIN CONNECTOR CABLE ASSEMBLY
JC7-A

PRODUCT
FV454

SIZE	DRAWING NO.	REV
A	4553/900	A

SHEET | PAGE

AA 2826

PRINTED IN U.S.A.

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
7	1	48"	A1	6	A31C08	A01	36,37	A DATA Bit 00
	92	↑	A2	↑	↑	B01	↑	
8	1		A3			A02		01
	94		A4			B02		
9	1		A5			A03		02
	96		A6			B03		
10	1		A7			A04		03
	98		A8			B04		
11	1		A9			A05		04
	90		A10			B05		
12	2		B1			A06		05
	92		B2			B06		
13	2		B3			A07		06
	94		B4			B07		
14	2		B5			A08		07
	96		B6			B08		
15	2		B7			A09		08
	98		B8			B09		
16	2		B9			A10		09
	90		B10			B10		
17	3		C1			A12		10
	92		C2			B12		
18	3		C3			A13		11
	94		C4			B13		
19	3		C5			A14		12
	96		C6			B14		
20	3		C7			A15		13
	98	↓	C8	↓	↓	B15	↓	
21	3		C9			A16		A DATA Bit 14
	90	48"	C10	6	A31C08	B16	36,37	

FIND NO.	COLOR (REF.)	L'NGTH	CONN PIN NO.	ACCESS. FIND NO.	DESTINATION		ACCESS. FIND NO.	FUNCTION
22	4	48"	D1	6	A31C08	A17	36,37	A DATA Bit 15
	92	↑	D2	↑	↑	B17	↑	
23	4		D3			A18		REPLY
	94		D4			B18		
24	4		D5			A19		REJECT
	96		D6			B19		
25	4		D7			A20		PRIORITY
	98		D8			B20		
26	4		D9			A21		
	90		D10			B21		
27	5		E1			A22		
	92		E2			B22		
28	5		E3			A23		
	94		E4			B23		
29	5		E5			A24		
	96		E6			B24		
30	5		E7			A25		
	98		E8			B25		
31	5		E9			A26		
	90		E10			B26		
32	6		F1			A27		
	92		F2			B27		
33	6		F3			A28		
	94		F4			B28		
34	6		F5			A29		
	96		F6			B29		
35	6		F7		↓	A30		
	98		F8		A31C08	B30		
3	2	↓	F9	↓	TB C08	A31	↓	+20
2	6	48"	F10	6	TB C08	B31	36,37	-20
	0		61		TB			GRD

UNLESS OTHERWISE SPECIFIED
ALL WIRES TO BE 24 GAUGE

CONTROL DATA
CORPORATION

TITLE
61-PIN CONNECTOR CABLE ASSEMBLY
J08-A

PRODUCT
FV454A

SIZE	DRAWING NO.	REV
A	48832000	A

	SHEET	PAGE

AA 2826

PRINTED IN U.S.A.

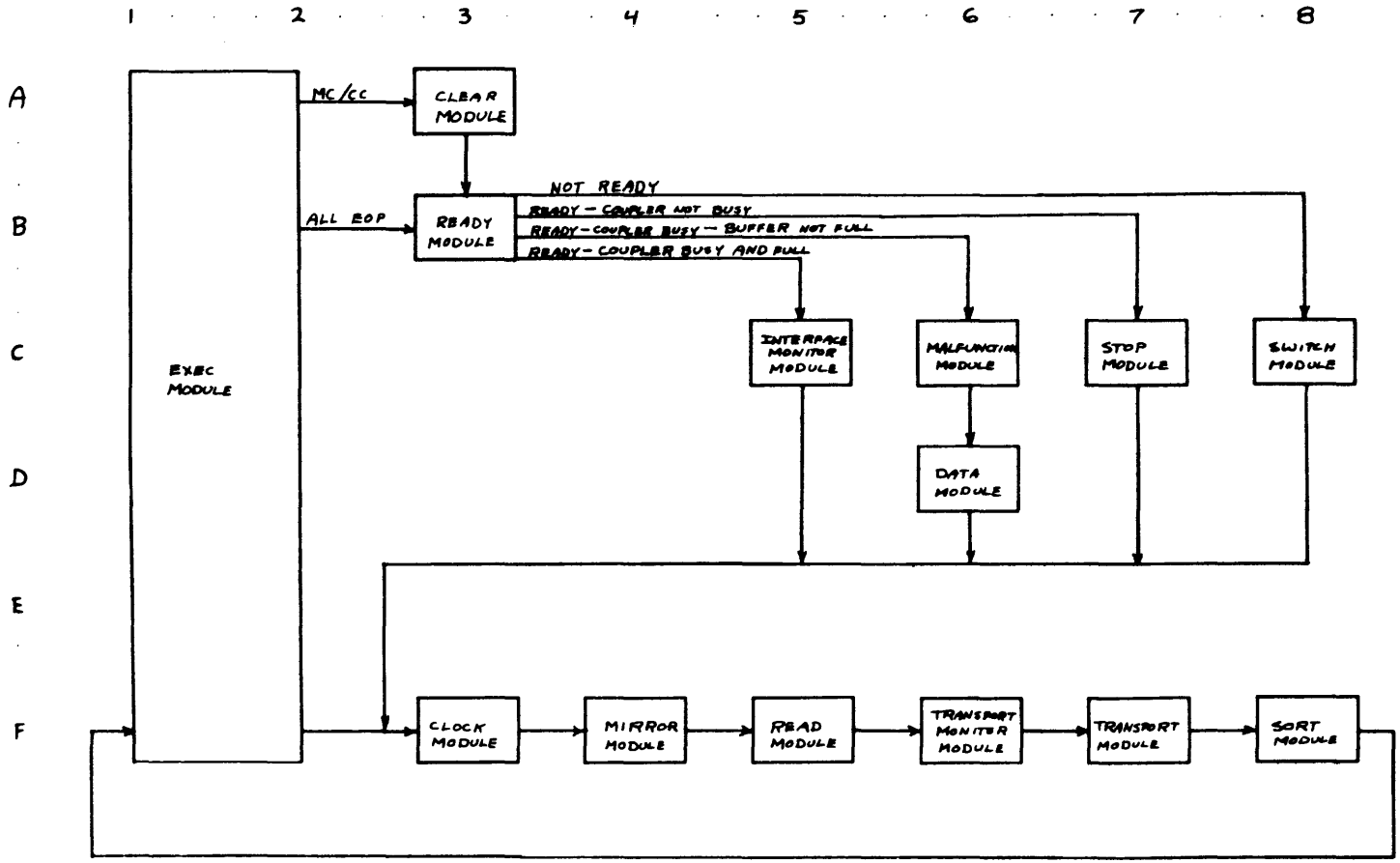
SECTION 10

EQUATION SUMMARY

Not Applicable

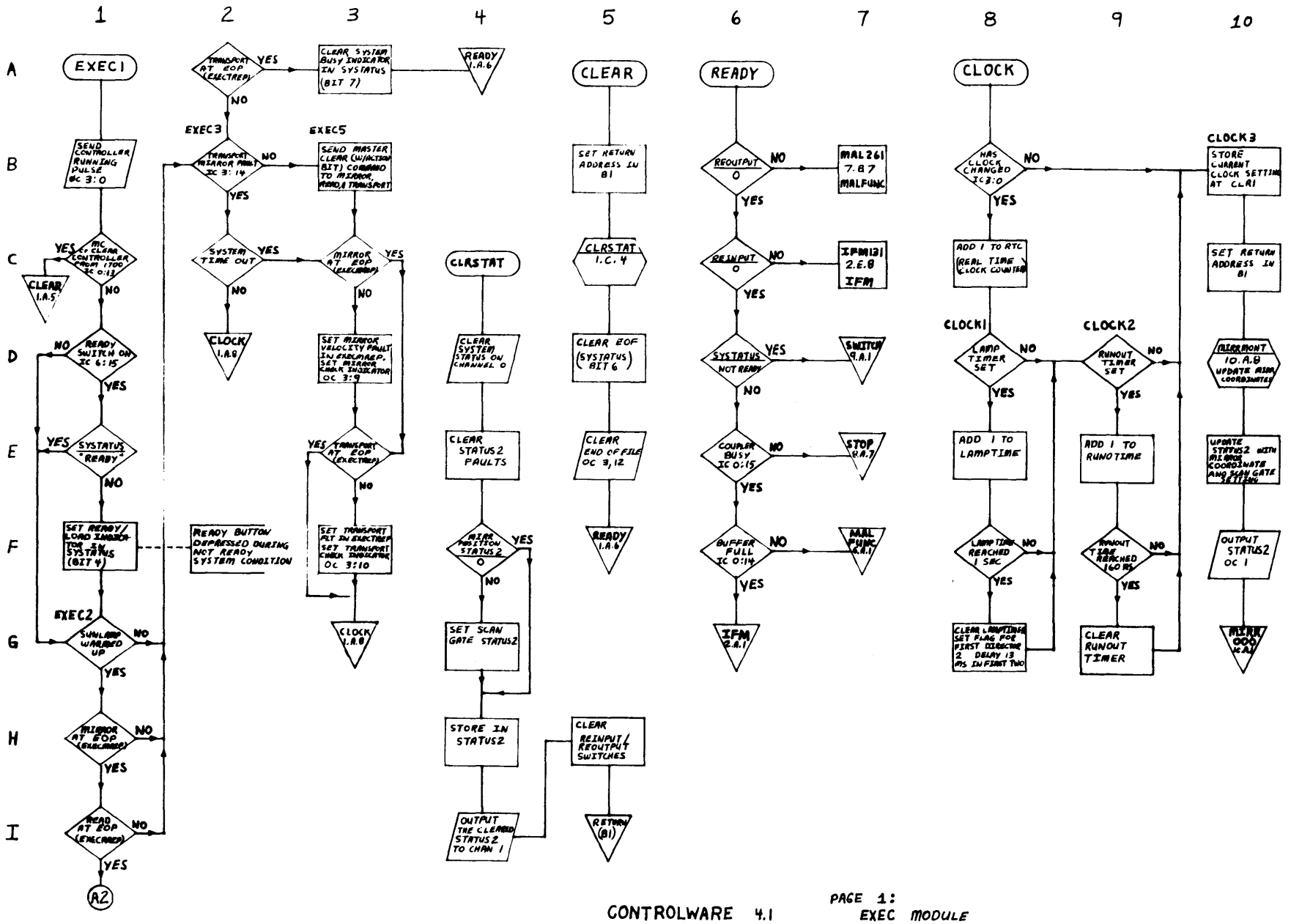
APPENDIX A

FLOW CHARTS



CONTROLWARE 4.1 BASIC STRUCTURE

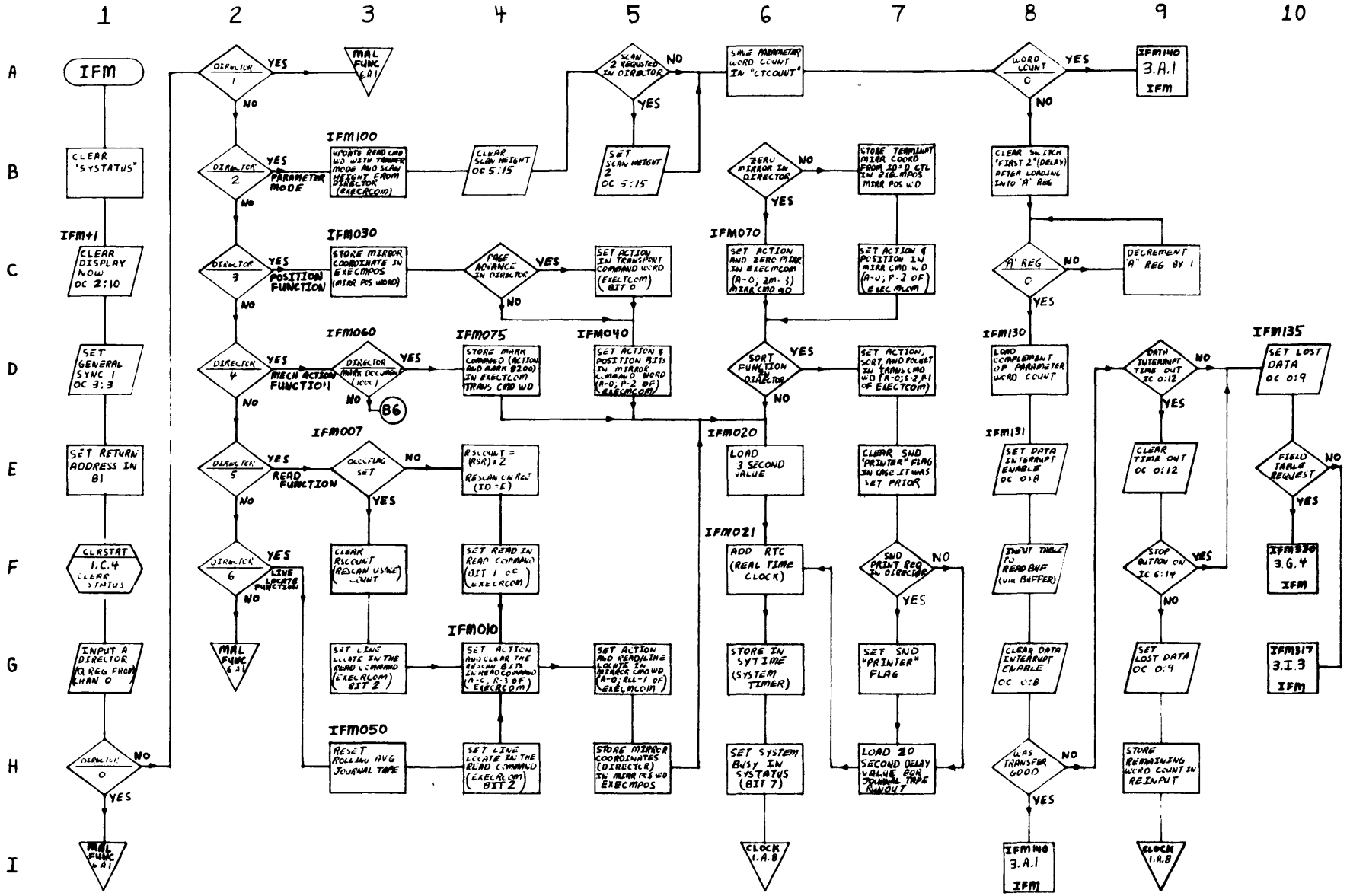
11-1-74



CONTROLWARE 4.1

11-1-74

PAGE 1:
EXEC MODULE
CLEAR MODULE - CLRSTAT SUBROUTINE
READY MODULE
CLOCK MODULE



CONTROLWARE 4.1

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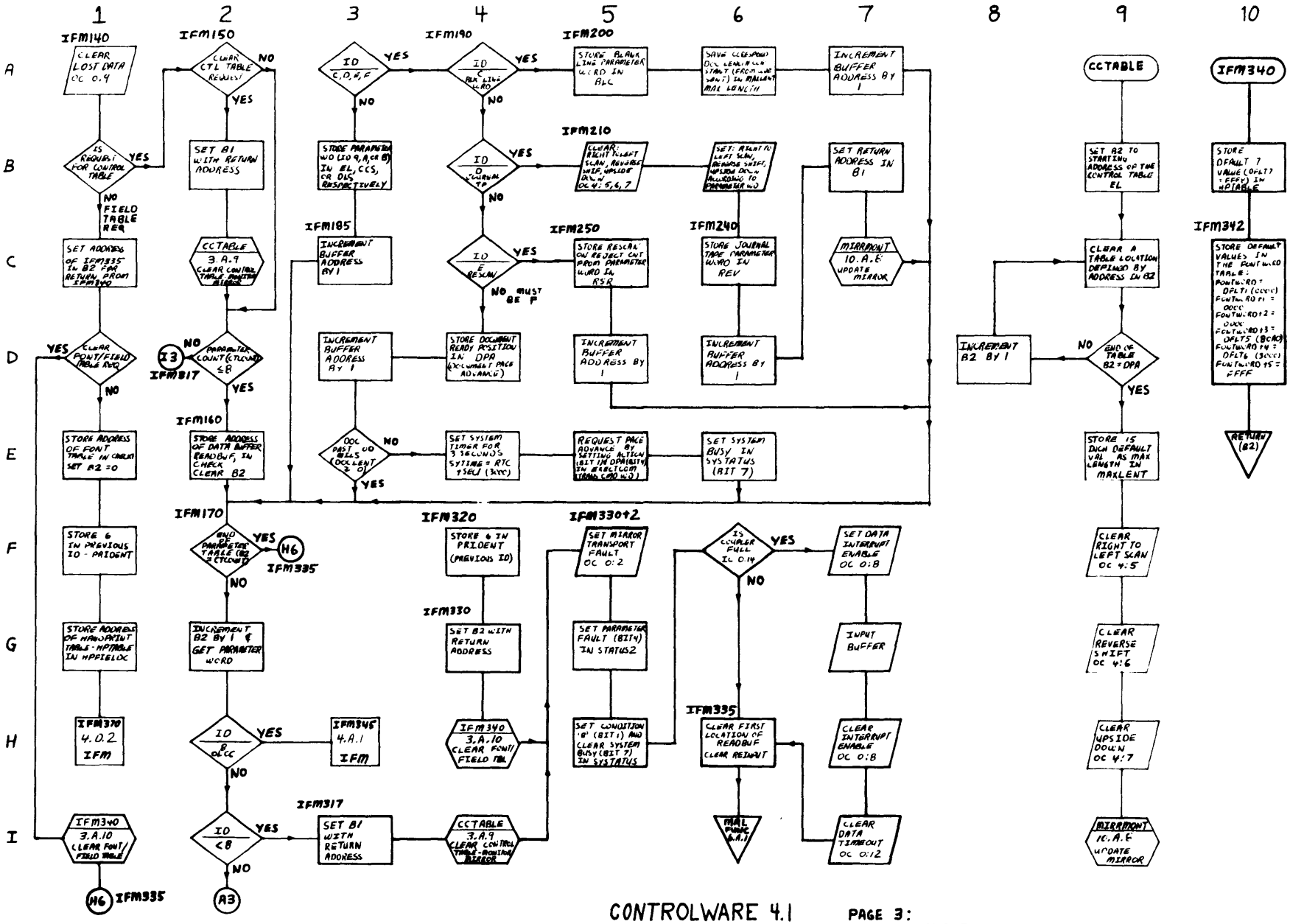
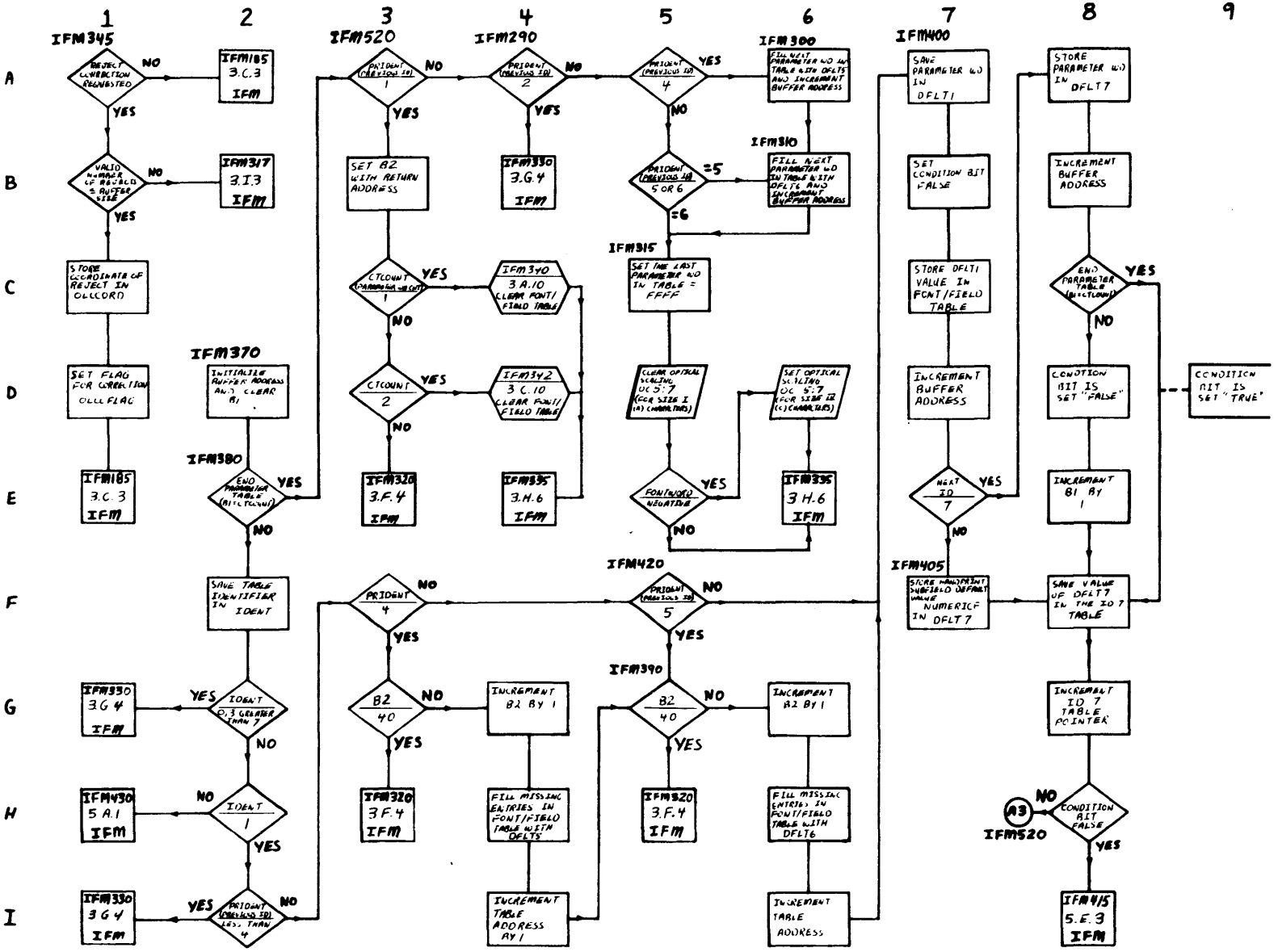
PAGE 2:
INTERFACE MONITOR MODULE



CONTROLWARE 4.1
11-1-74

PAGE 3:
INTERFACE MONITOR MODULE CONTINUED
IFM340 SUBROUTINE
CCTABLE SUBROUTINE



CONTROLWARE 4.1

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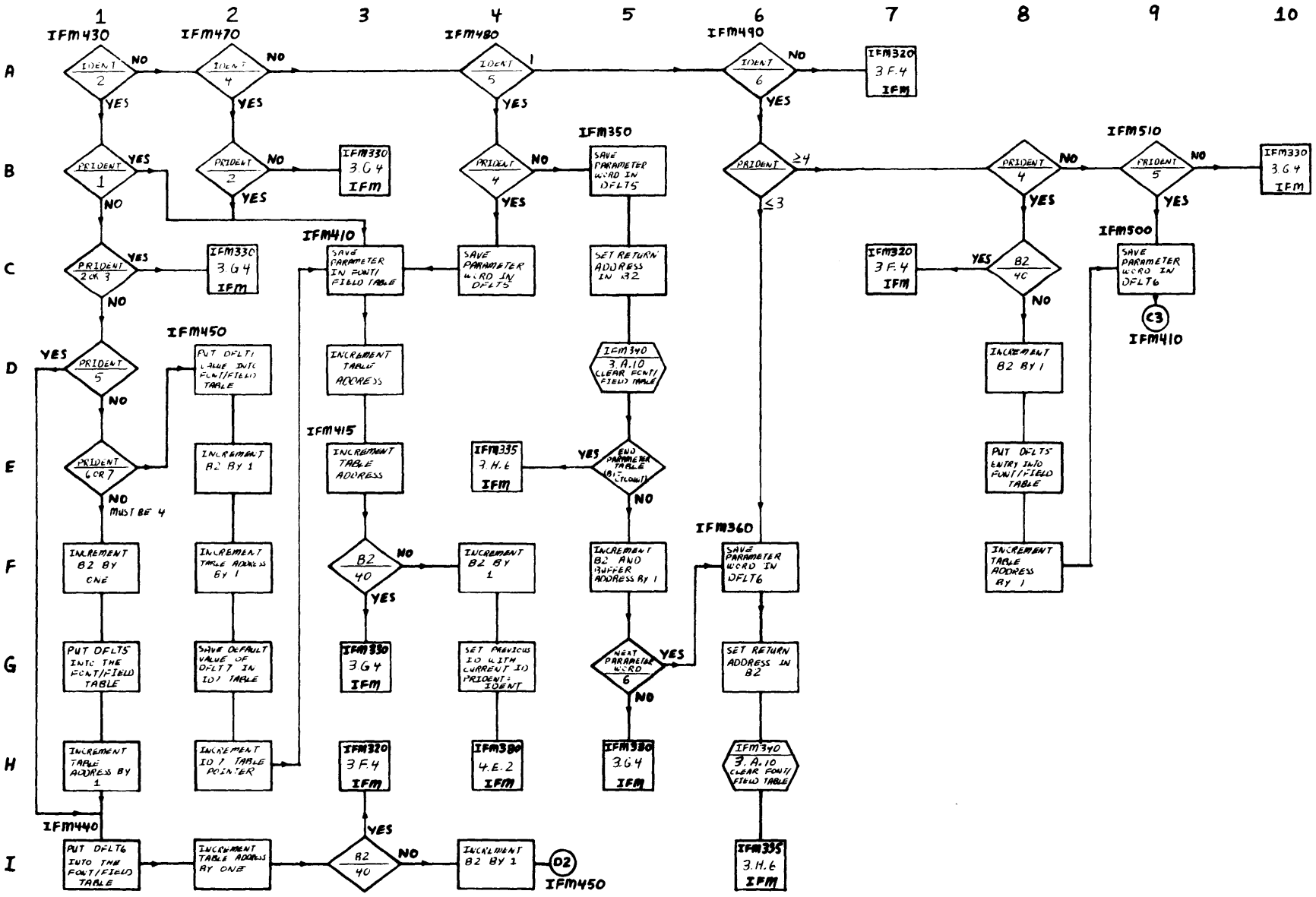
PAGE 4:
INTERFACE MONITOR MODULE CONTINUED



CONTROLWARE 4.1
11-1-74

PAGE 5:
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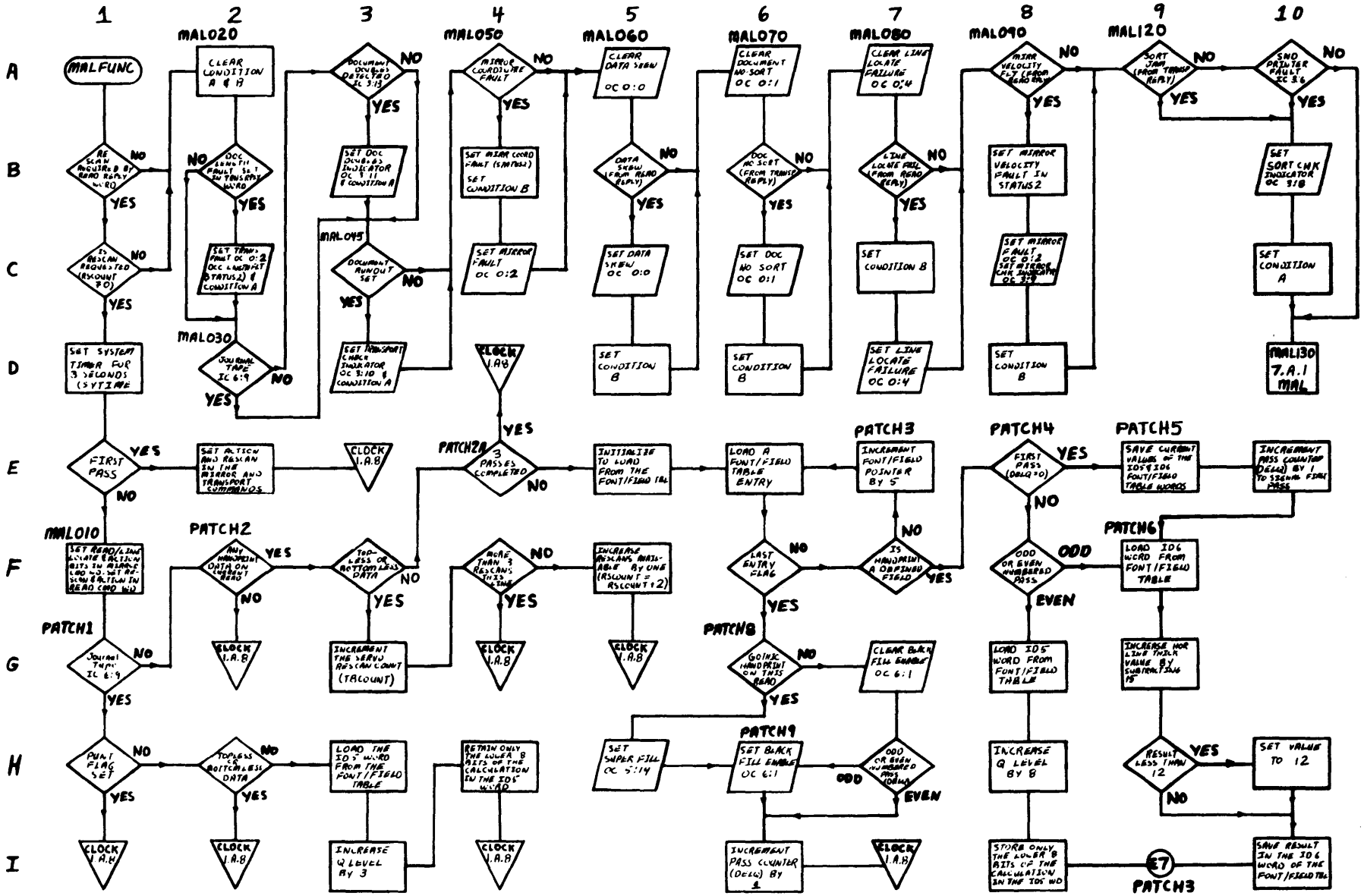
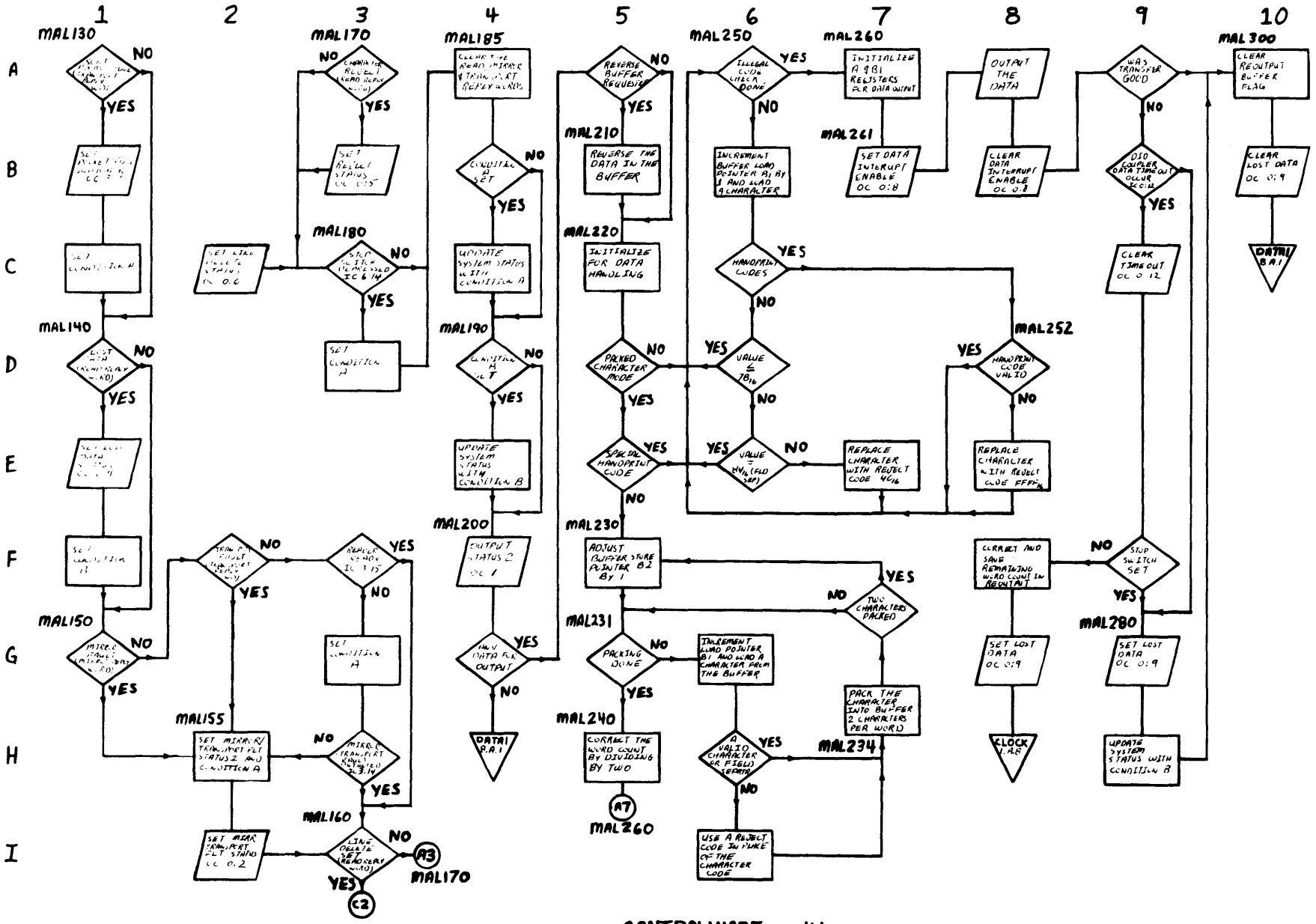


CONTROLWARE 4.1
11-1-74

PAGE 6:
MALFUNCTION MODULE



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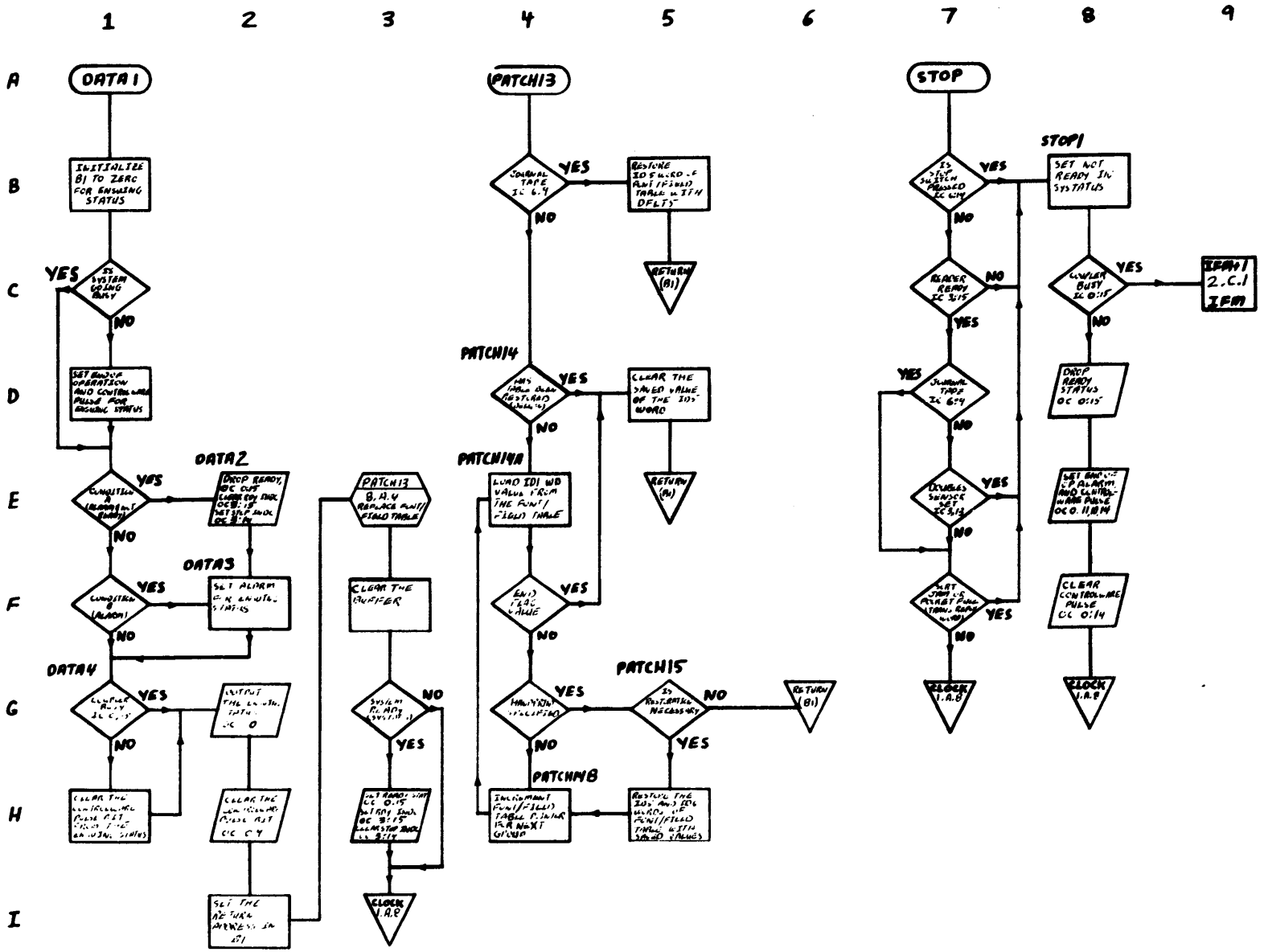
11-1-74

PAGE 7:
MALFUNCTION MODULE CONTINUED



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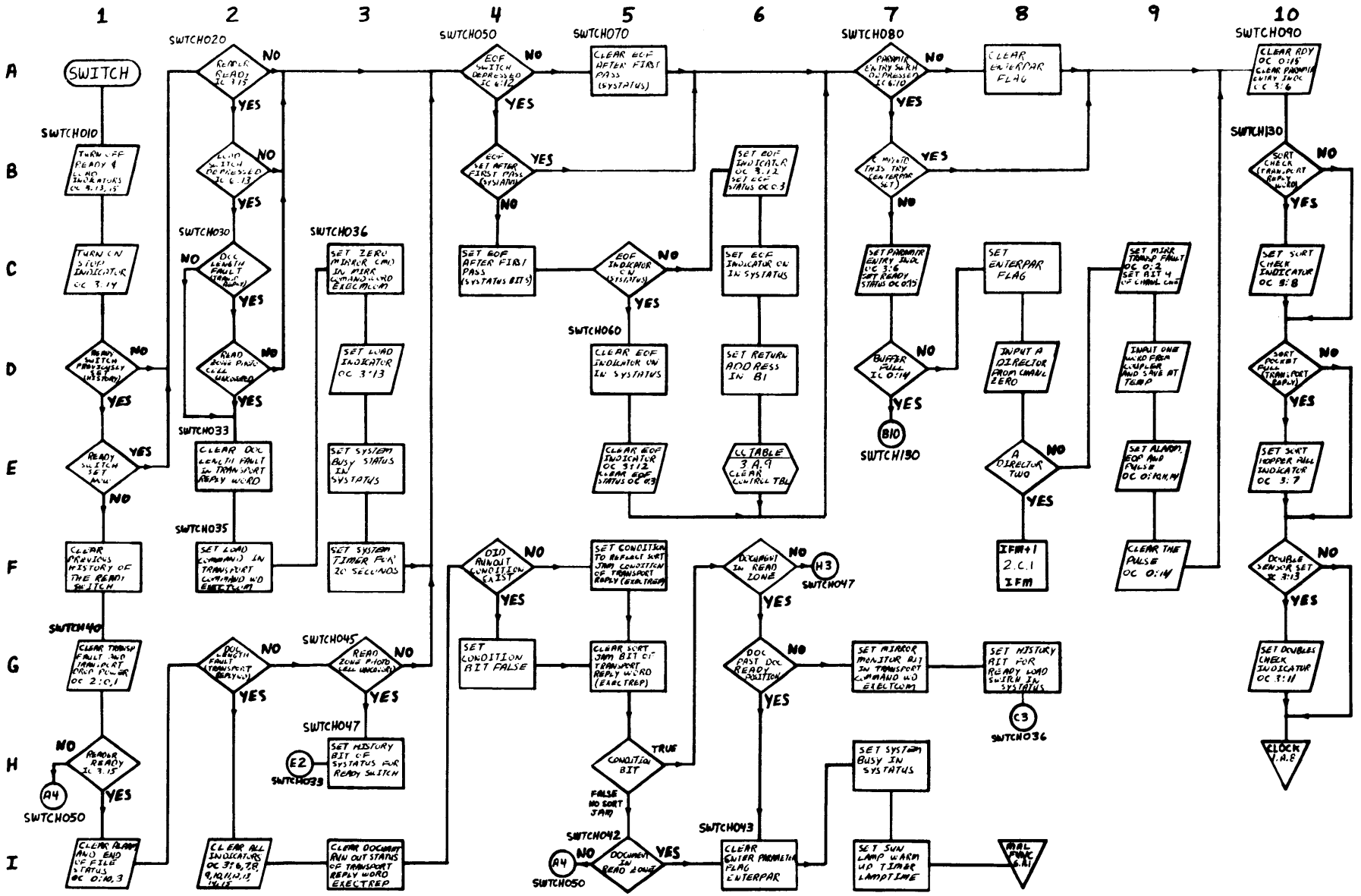
PAGE 8:
DATA MODULE - PATCH13 SUBROUTINE
STOP MODULE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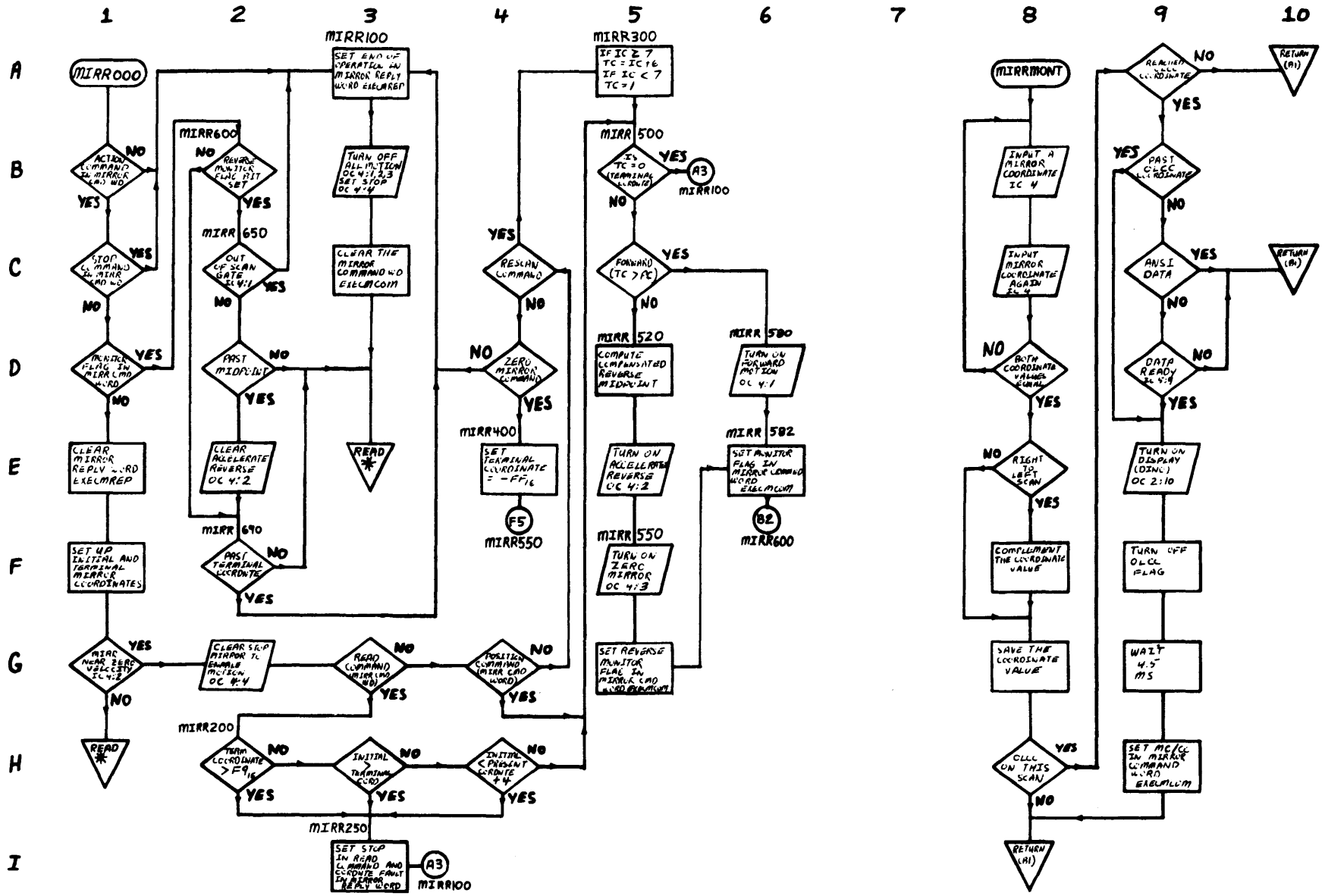
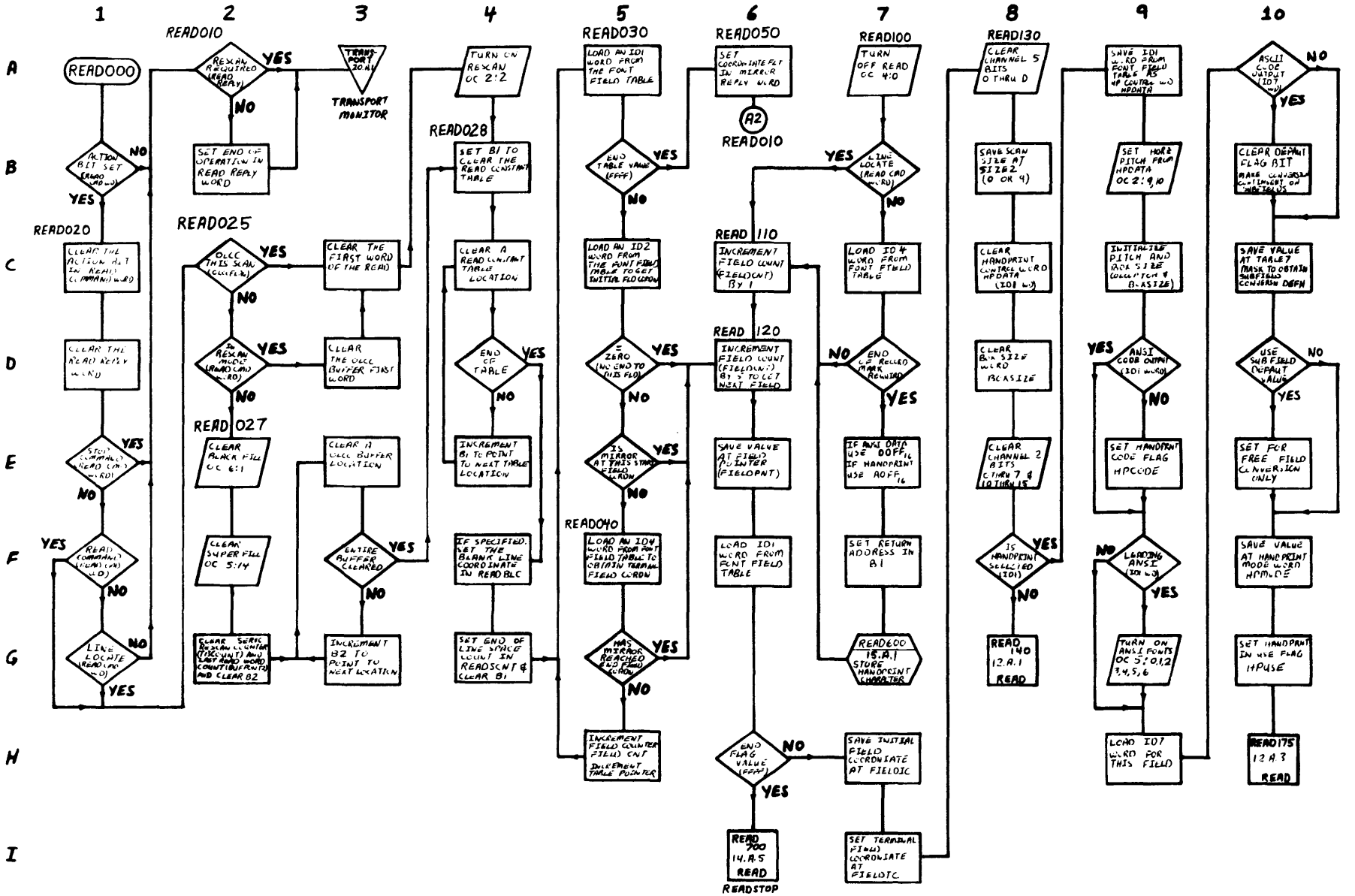
SWTCH010
SWTCH020
SWTCH030
SWTCH033
SWTCH035
SWTCH036
SWTCH040
SWTCH045
SWTCH047
SWTCH050
SWTCH060
SWTCH070
SWTCH080
SWTCH090
SWTCH130
SWTCH190
SWTCH042
SWTCH043
CONTROLWARE 4.1
11-1-74
PAGE 9:
SWITCH MODULE



* READ MODULE ENTRY POINT AS DETERMINED BY THE READ MODULE CAN BE: READ000 11.A.1
READ070 12.B.4
READ300 12.I.4
READ1200 18.A.1

CONTROLWARE 4.1

PAGE 10:
MIRROR MODULE
- MIRROR MONITOR SUBROUTINE



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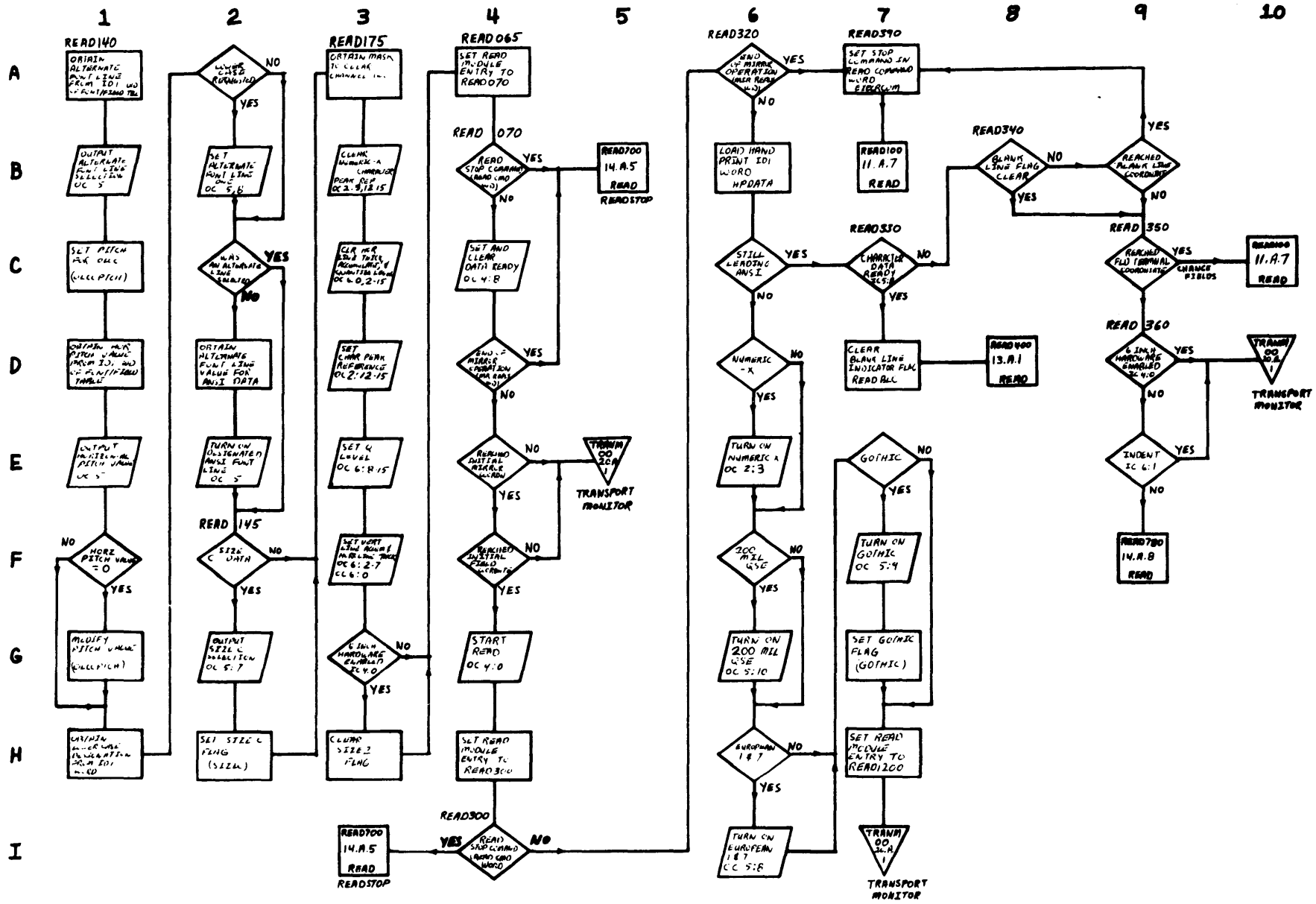
PAGE 11:
READ MODULE



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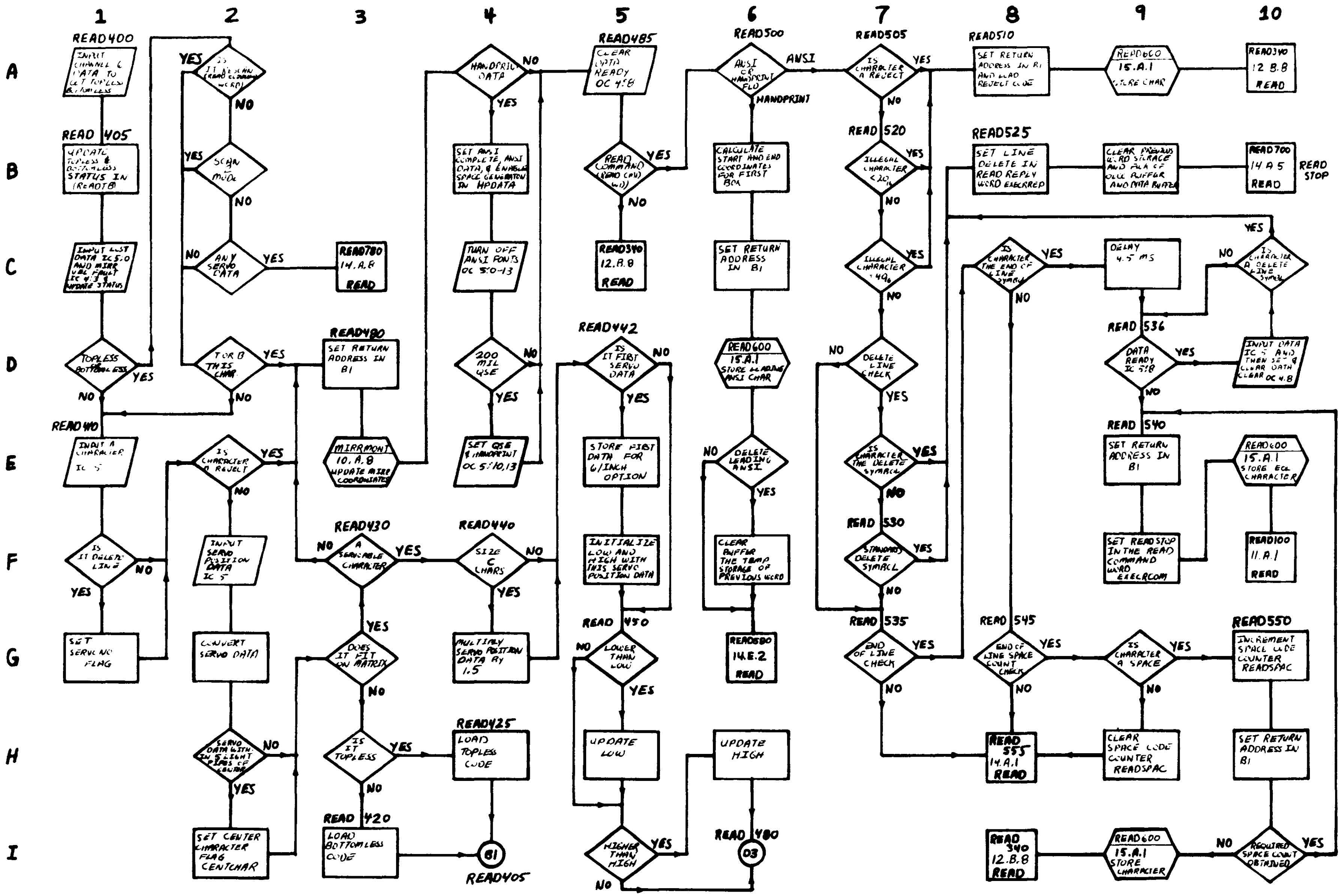
PAGE 12:
READ MODULE CONTINUED



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PAGE 13:
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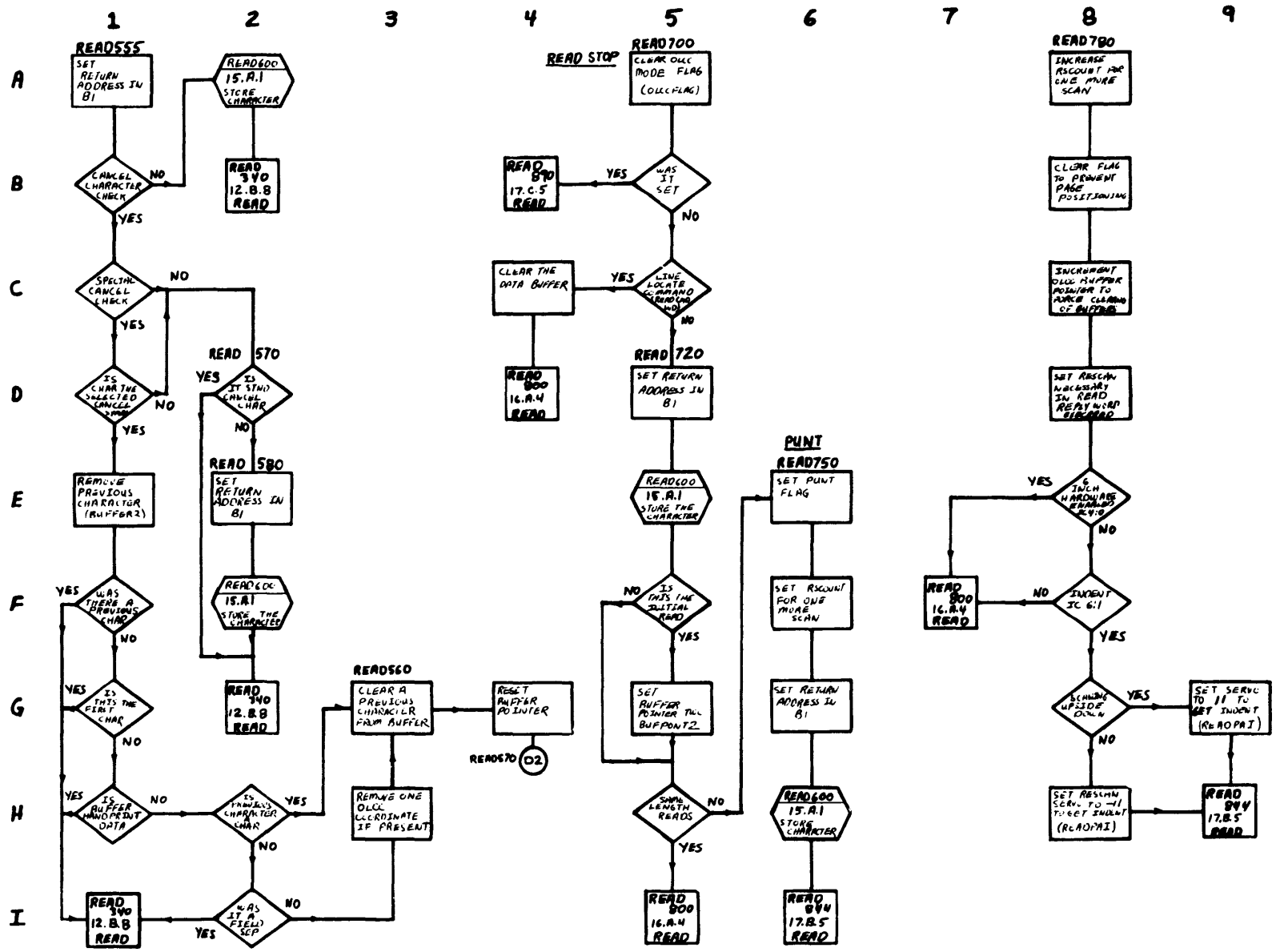

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PAGE 14:
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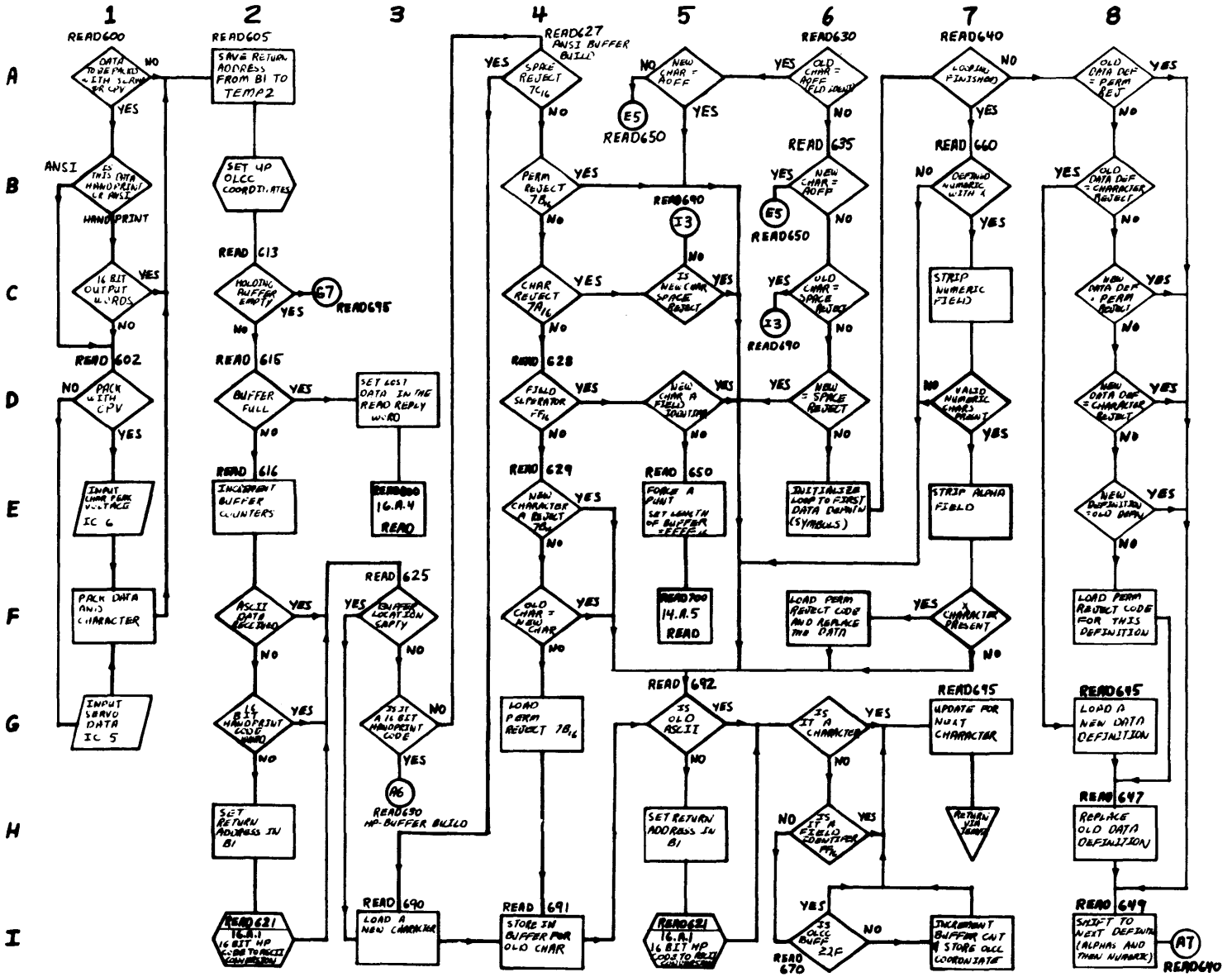

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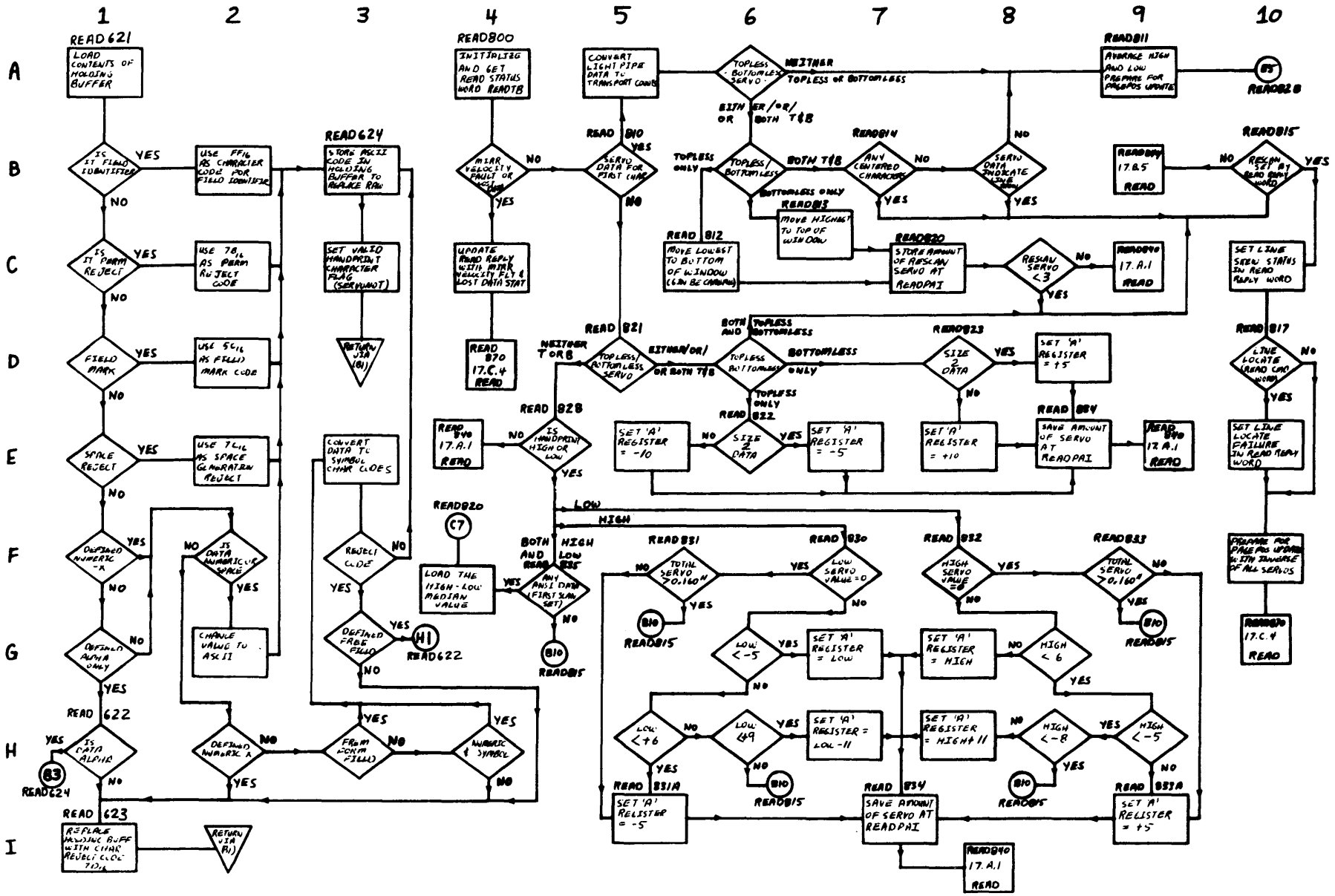
PAGE 15:
READ MODULE CONTINUED



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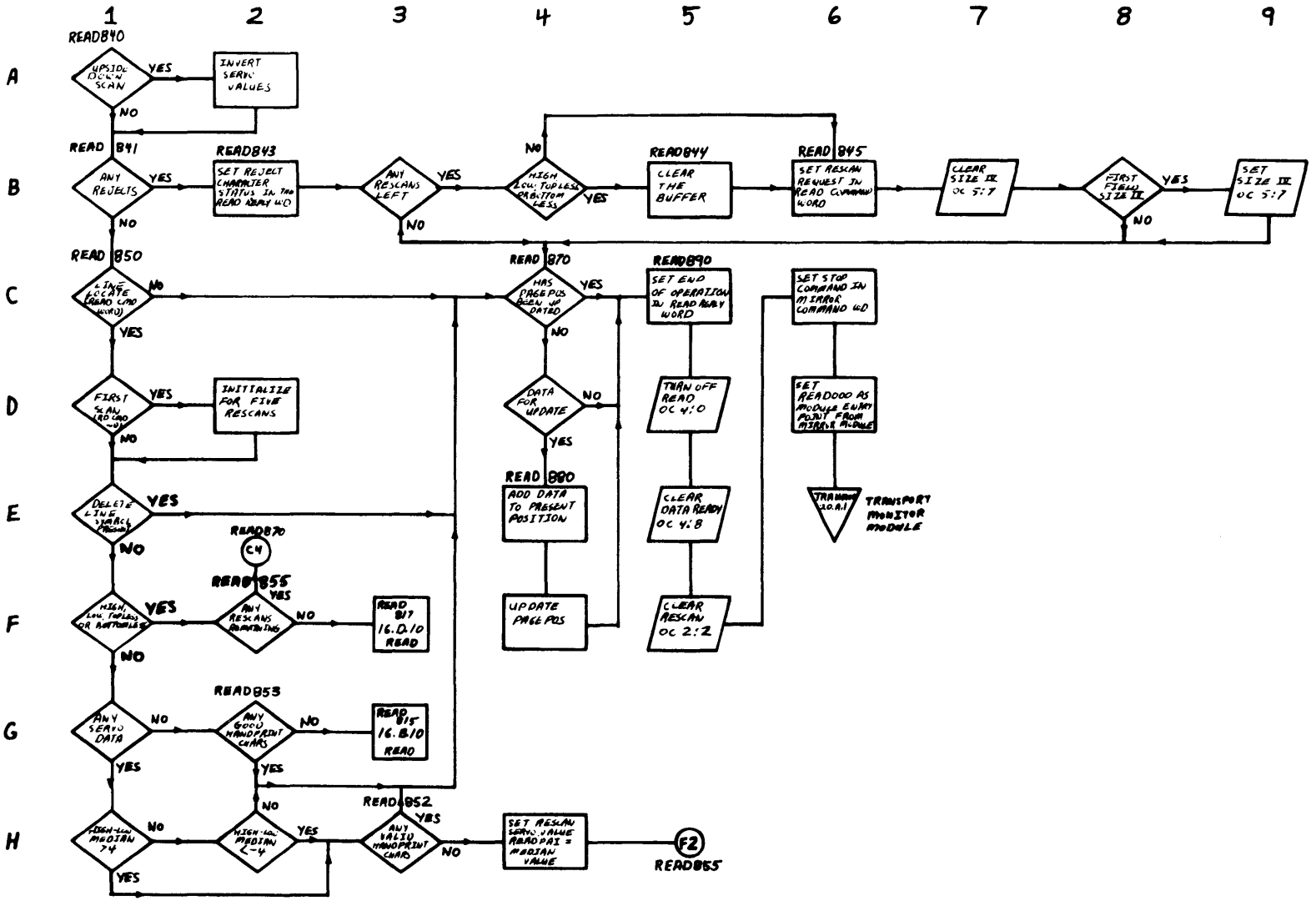
11-1-74

PAGE 16:
READ MODULE CONTINUED
READ621 SUBROUTINE



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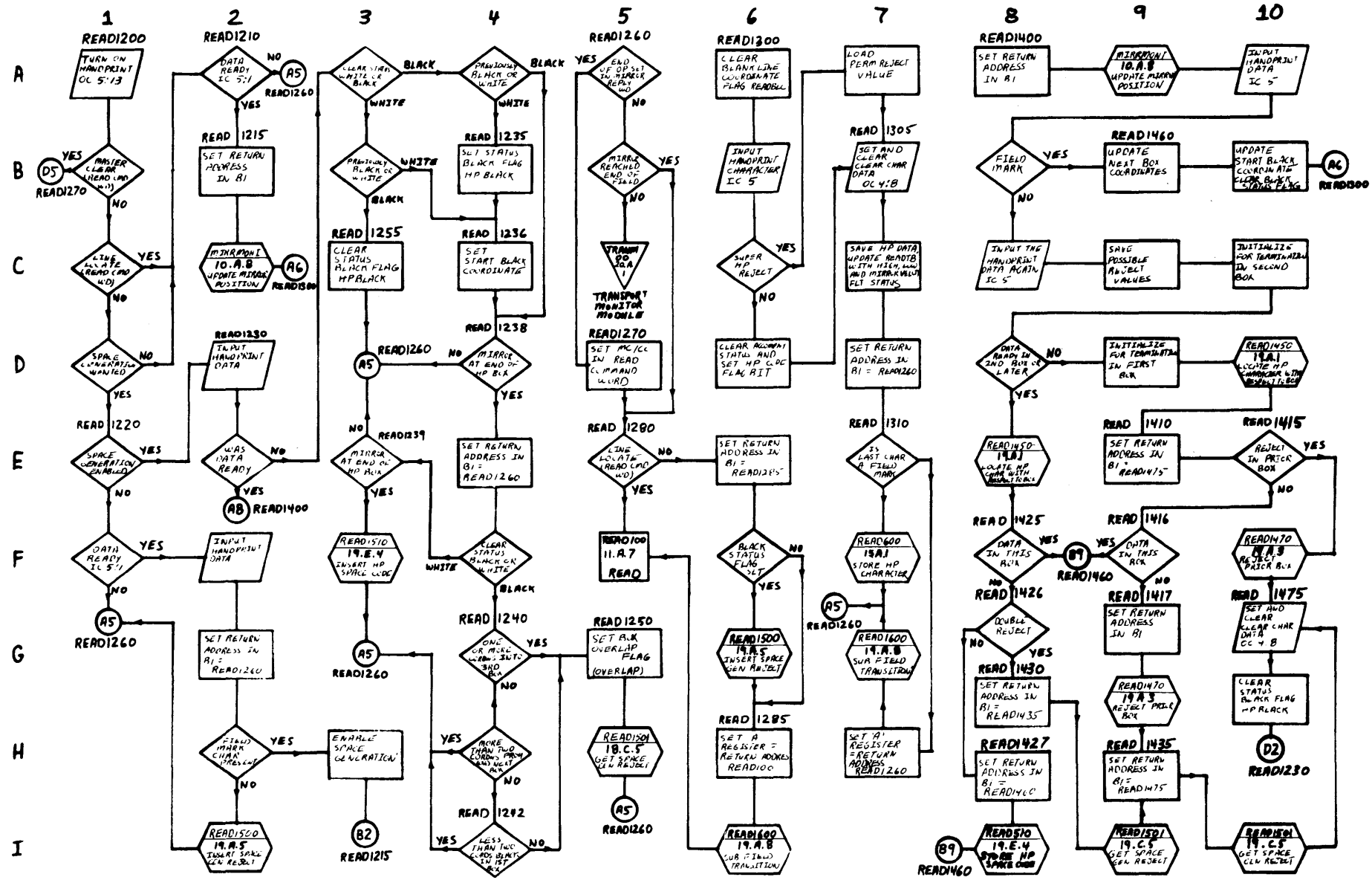
PAGE 17:
READ MODULE CONTINUED



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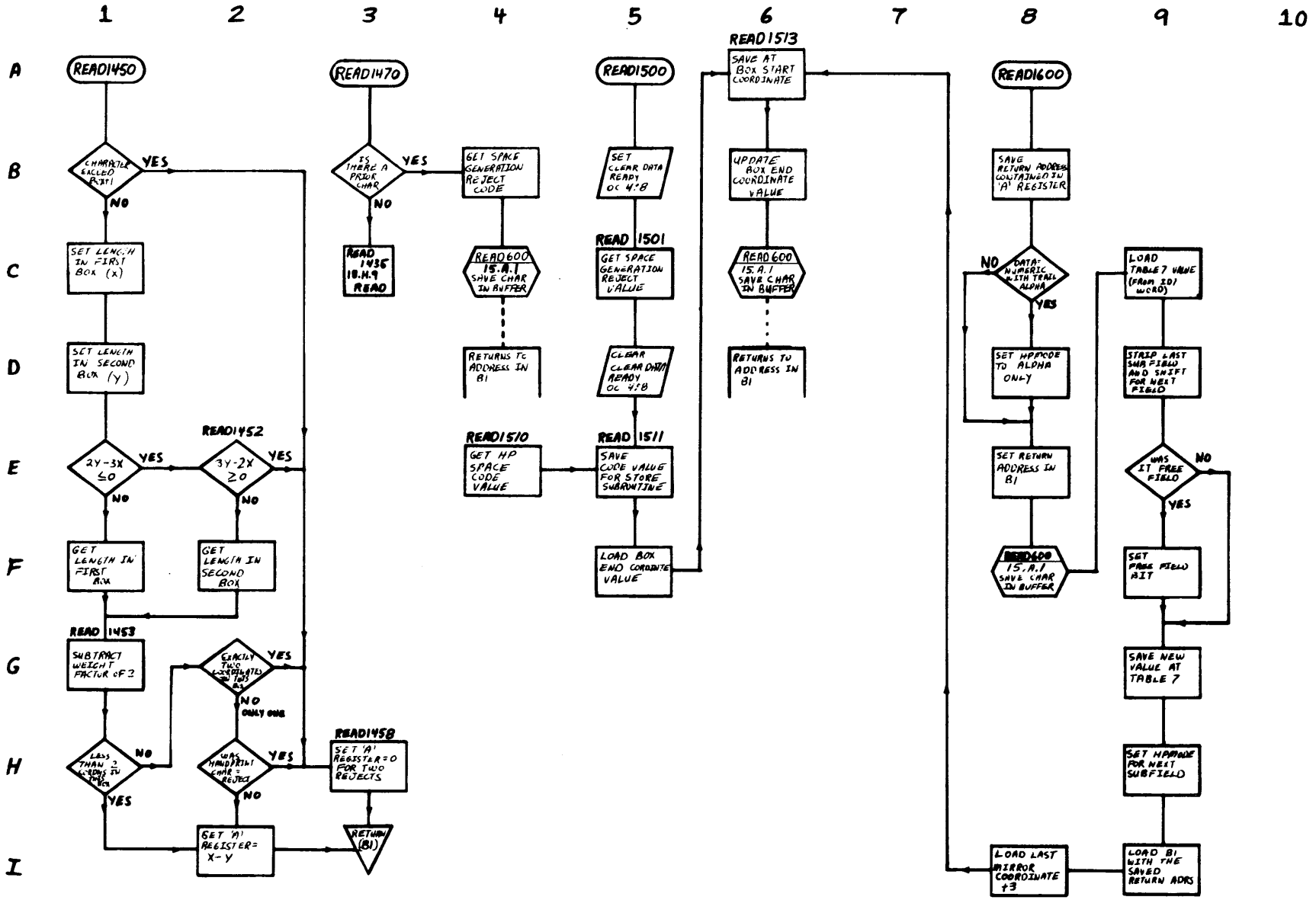
PAGE 18:
READ MODULE CONTINUED



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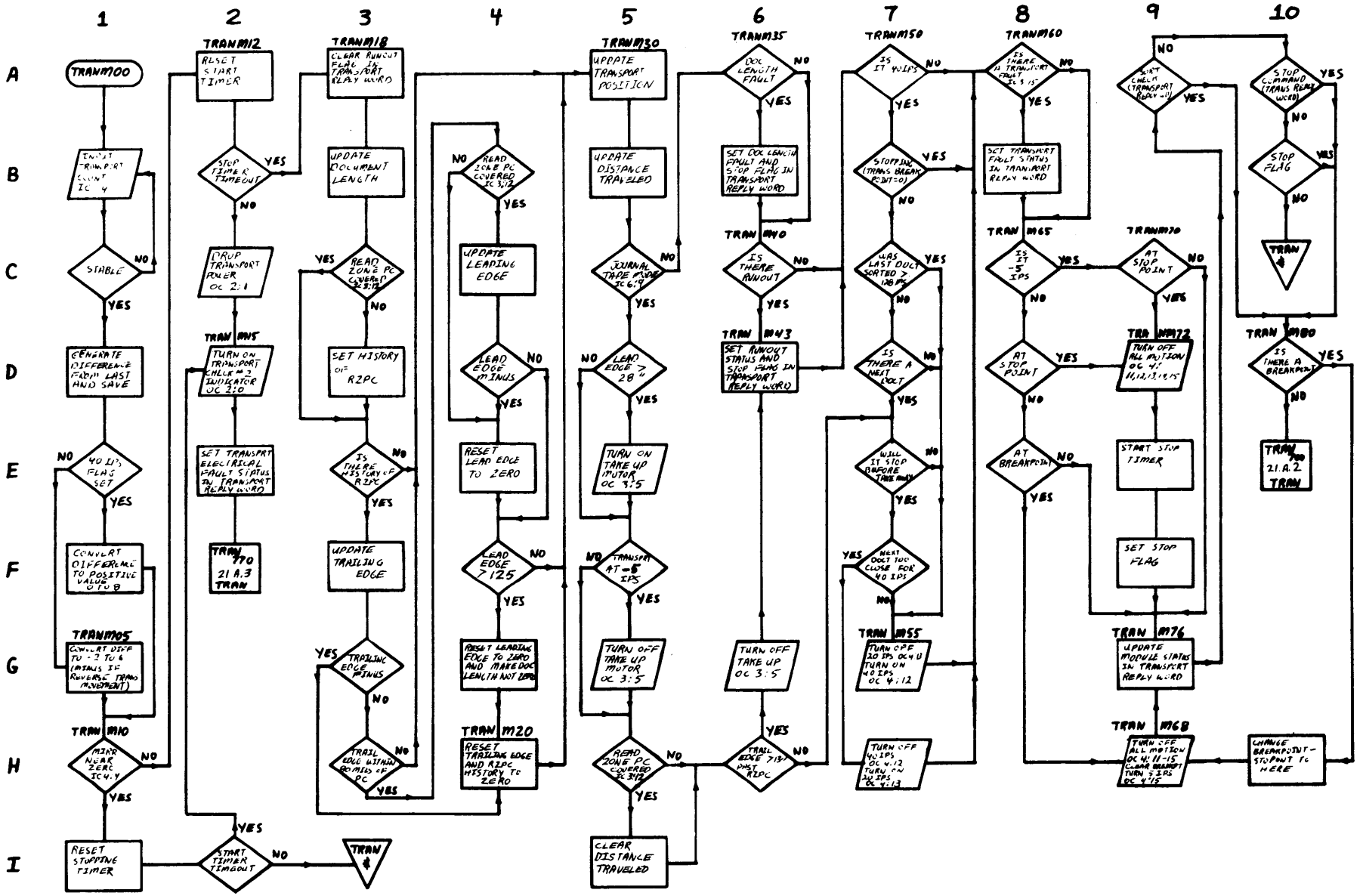
PAGE 19:
READ MODULE CONTINUED
READ1450, READ1470, READ1500, AND READ1600 SUBROUTINES



* TRANSPORT MODULE ENTRY POINT AS DETERMINED BY THE TRANSPORT MODULE CAN BE: TRAN000, 2.1.A.1 ; TRAN700+2, 2.1.B.2 TRAN450, 2.1.C.4 ; TRAN850, 2.1.D.7 TRAN650, 2.1.E.6

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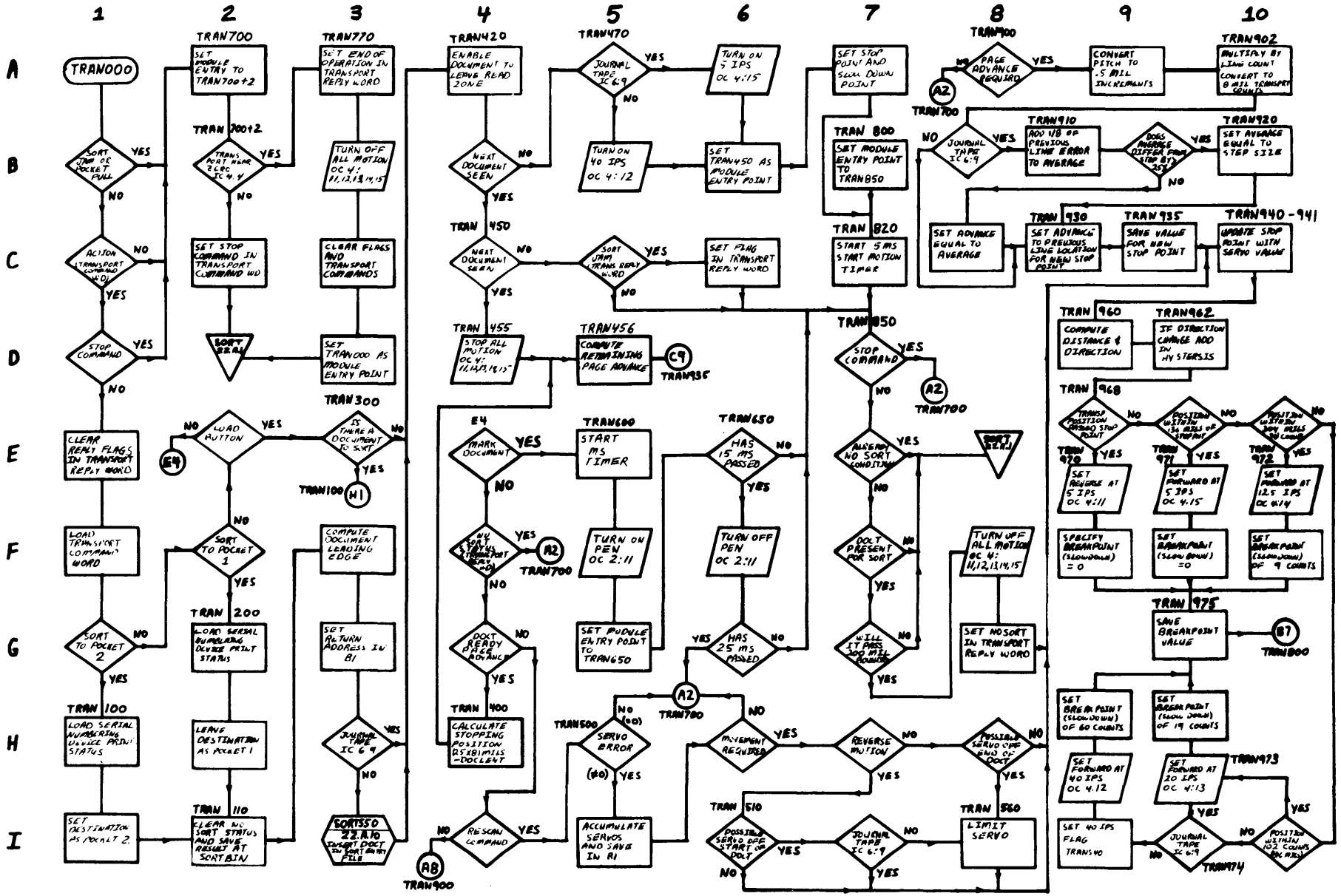
PAGE 20:
TRANSPORT MONITOR MODULE



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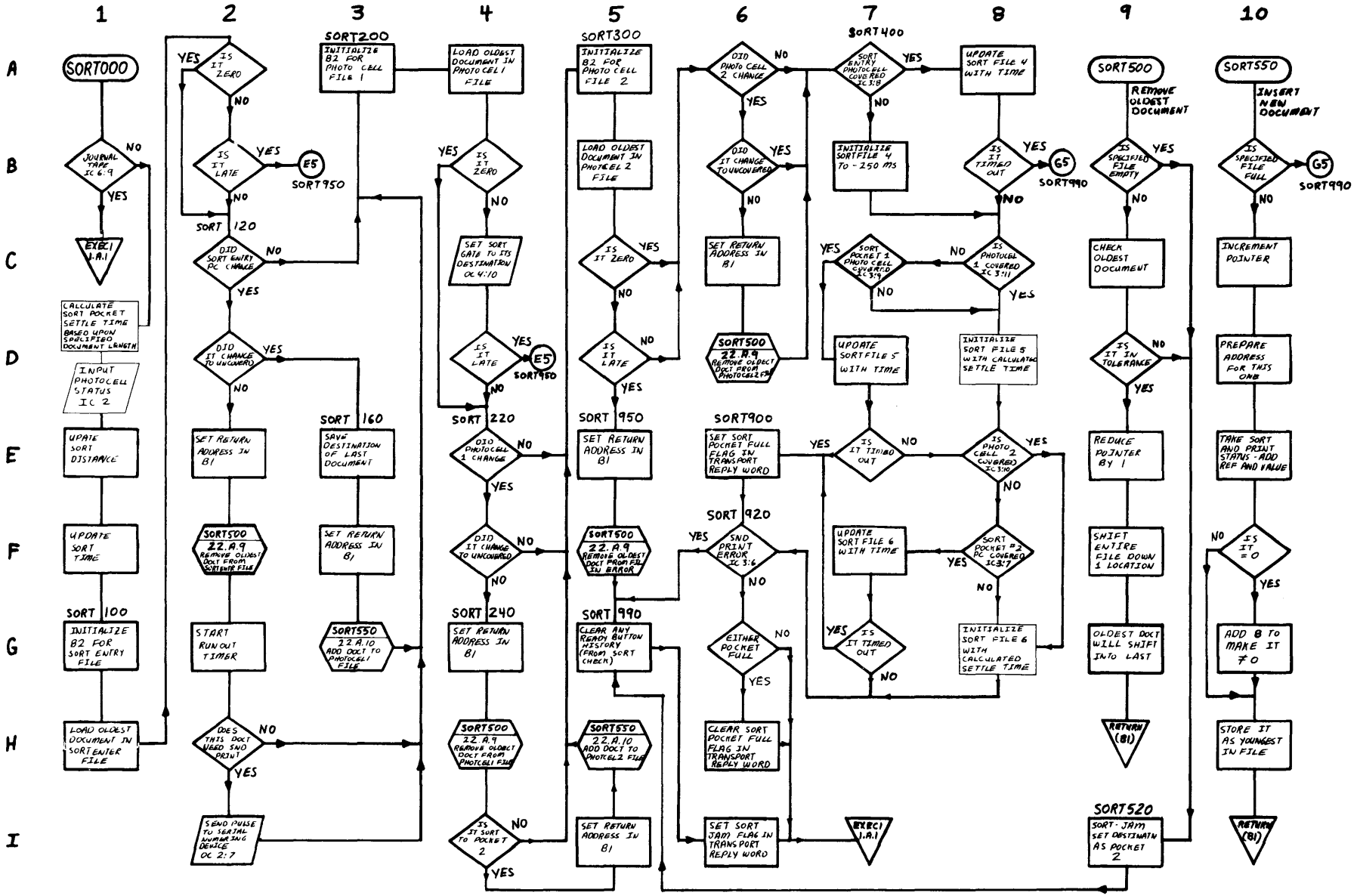
PAGE 21:
TRANSPORT MODULE



CONTROLWARE 4.2.4

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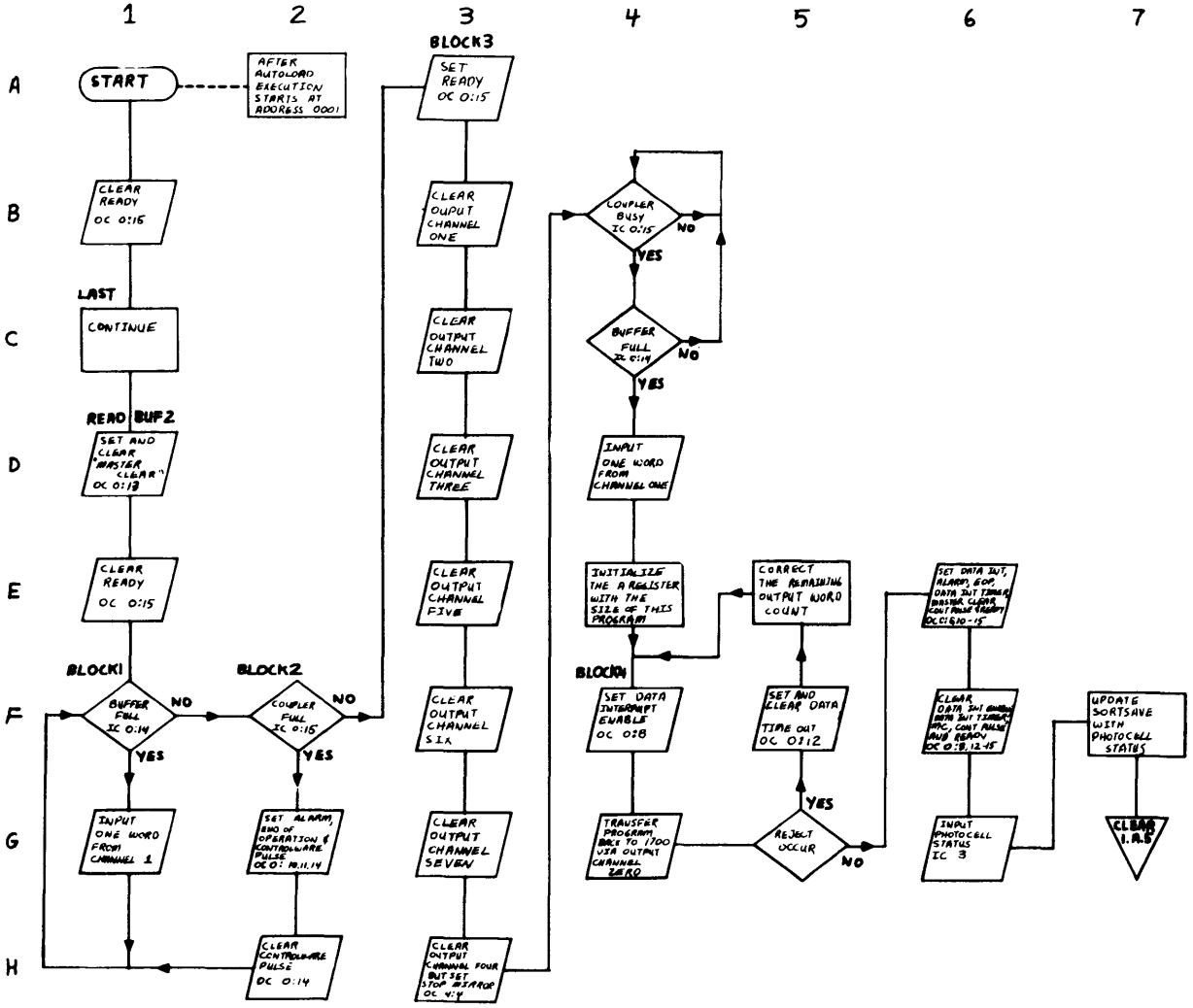
PAGE 22:
SORT MODULE
SORT500 SUBROUTINE
SORT550 SUBROUTINE



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PAGE 23:
AFTER-AUTOLOAD EXECUTION

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