

CONTROL DATA[®] CJ122 MODELS C, D, E, F, G, H, J, AND K PAGE AND DOCUMENT READER

Volume 1

HARDWARE MAINTENANCE MANUAL

	REVISION RECORD
REVISION	DESCRIPTION
01	Preliminary manual released.
8/15/70	
02	Manual revised.
10/1/70	
03	Sections 2 and 6 revised to incorporate latest technical information. PMP's 2.4, 3.2, 3.3, 3.4,
6/1/71	and 5.1 revised or added to Section 6. New and revised adjustment, replacement, and trouble-
	shooting procedures added to Section 6.
04	Sections 3 and 6 revised to incorporate latest technical information. Crating and uncrating,
6/15/71	installation and checkout procedures added to Section 3. Revamped PMP section and added
	troubleshooting procedures to Section 6. This revision includes the following ECO's: 2619, 2624,
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А	Manual released. Incorporated the following ECO's: 3370, 3372, 3374, 3385, 3497, 3548, and
10/30/71	3607.
в	Manual released. Incorporated the following ECO's/FCO's: 3609, 3613, 3615, 3616, 3618, 3621,
3/15/73	3622, 3623, 3629, 3630, 3631, 3632, 3646, 3648, 3650, 3655, 3666, 3667, 3683, 3712, 3713, 3717
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	3949, 3953, 3969, 3970, 3972, 3977, 3984, 4029, 4170, 4214, 4216, 4229, 4241, 4243, 4246, 4256
	4271, 4285, 4287, 4293, 4326, 4358, 4373, 4376, 4377, 4380, 4403, 4426, 4443, 4459, 4465, 4473,
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2/14/75	5565, 5629, 5742, 5773, 5862, 5922, 5931, 5943 and 6018. All sections updated to correct errors,
	to reflect latest technical information, to delete Model A, and to include Models E, F, G, H, J,
	and K.
D	Manual released. Incorporated ECO's 6215 and 6387, corrected errors.
6/19/75	Adds transport encoder disassembly proc e dure.
E	Adds transport encoder disassembly procedure.
1/12/75	
Publication No.	
48430080	

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

Sheet $_^1$				EQUIPM	ENTS		
Manual REV	FCO or ECO	CJ122 A	CJ122 C	CJ122 D	CJ122 E & K	CJ122 F & J	CJ122 G & H
D	5052						01-up
	5128				01-up	01-up	01-up
	5133				01-up		01-up
	5134				01-up	01-up	01-up
	5150				01-up	01-up	01-up
	5291		01-up	01	01-up	01-up	01-up
	5565			01	01-up	01-up	01-up
	5629					01-up	01-up
	5742						01-up
	5773		01-up	01	01-up	01-up	01-up
	5862				01-up	01-up	01-up
	5922	01	01-up	01	01-up	01-up	01-up
	5931	01	01-up	01	01-up	01-up	01-up
	5943					01-up	01-up
	6018				01-up		01-up
	6215				01-up	01-up	01-up
	6387				01-up	01-up	01-up
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PREFACE

The CJ122 Page and Document Reader Hardware Reference/Customer Engineering Manual contains the information necessary to operate, install, check out, maintain, and repair the page and document reader. The manual consists of three volumes.

Volume 1 (Pub. No. 48430080) contains the following sections:

1. General Description

- 4. Theory of Operation
- 2. Operation and Programming
- 6. Maintenance
- 3. Installation and Checkout
- 7. Maintenance Aids

Volume 2 consists of three parts and contains Section 5, Diagrams. Part 1 consists of introductory material, signal descriptions, and reader logic diagrams contained in Pub. No. 48948100. Part 2 consists of recognition rack diagrams, card schematics, and assert/ negate diagrams contained in Pub. No. 48948200. Part 3 consists of document transport system diagrams, optics system diagrams, panel and power diagrams, and option diagrams contained in Pub. No. 48430045.

Volume 3 contains Section 8, Parts Data. The Parts Data section contains introductory material, illustrations and listings of the assemblies, subassemblies and parts, and options used in the page and document reader. The parts list for a particular reader is in:

Volume 3A	Pub. No. 48430082	Mod A
Volume 3B	Pub. No. 48430087	Mod C
Volume 3C	Pub. No. 48430090	Mods D, E, K
Volume 3D	Pub. No. 91622100	Mods F, G, H, J

Manuals used in conjunction with the CJ122 Page and Document Reader are:

955 Page and Document Reader OCR Media Manual	60216102
955 Page and Document Reader/1700/SC1700 Computer Systems OCR Software Operator's Guide - Controls and Indicators	48643305
Page and Document Reader Controller Reference Manual $(S/N 97-150)$	60324700
Page and Document Reader Controller Reference Manual (S/N 151 and up)	48935300
1700 System Maintenance Monitor Manual	60182000
Printed Circuit Manual	60042000
CW150 1428 Alphanumeric Font Option Customer Engineering Manual	48804200
CW132 ANSI-OCR-A Size I Lower Case Font Option Customer Engineering Manual	48804201

CW141 1403 Font Option Manual	48804202
CW139 1428 Numeric Font Option Manual	48804203
CW149 Rabinow Font Option Manual	48804204
CW137 7B Font Option Manual	48804205
CW134 E13B Font Option Manual	48804206
CW138 12F Font Option Manual	48804207
CW150 1428 Alphameric Font Option Mod C	48804208
CW141C 407-1 Numerics Font Option	48804209
CC107-A On-Line Character Correction Option	48936600
CW126 Handprint Unit Model A Hardware Reference/Customer Engineering Manual (Volume 1)	48143980
CW126 Handprint Unit Models A, B Wire Lists Hardware Reference/ Customer Engineering Manual (Volume 3, Part 1)	48143940
CW126 Handprint Unit Models A through F Diagrams Hardware Reference/Customer Engineering Manual (Volume 2)	48143981
CW126 Handprint Unit Model B Hardware Reference/Customer Engineering Manual (Volume 4)	48143990
CW126 Handprint Unit Models E and F Hardware Reference/ Customer Engineering Manual (Volume 4B)	48991800
CW126F, CW193, CW207 Handprint Unit Logic Door Diagrams Hardware Reference/Customer Engineering Manual (Volume 2B)	48911900
CW207 Handprint Unit Model A01 Hardware Reference Manual (Volume 1)	91558900

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SECTION 1

GENERAL DESCRIPTION

The CONTROL DATA® CJ122 Page and Document Reader is a peripheral device that optically reads printed pages and documents. The basic reader reads a subset of the American National Standards Institute (ANSI) OCR-A or OCR-B Size I character set. Data to be read by the reader may be printed by typewriter, high-speed printer, or embossedcard imprinter. Available options are listed in table 1-1, and alternate character set options are listed in table 1-2.

This manual includes information on the operation, programming, installation, checkout, theory, and maintenance of the CJ122 reader and general information and interface logic for the following options: on-line character correction unit (OLCC), the standard six-lines-per-inch, and handprint unit.

SYSTEM OPERATION

A block diagram of a typical reader system is shown in figure 1-1. Documents to be read are loaded onto a feedup table on the reader and transported individually to the read area. At the read area, the document is scanned line by line. Light reflected from the area occupied by a single character is converted to electrical signals which are analyzed to determine the character read. After all characters in a line are read, the document is advanced and the next line is read. After all lines of a document are read, the document is sorted to the appropriate output hopper.

Control signals from the buffer controller enable reader functions such as document movement, reading, and sorting. Data read by the reader is routed to the buffer controller, along with sense signals that indicate the status of the reader. The computer is a generalpurpose digital computer programmed to control system operation and to provide output data in a format established by the user. Communication between the computer and the buffer controller, teletypewriter, and magnetic tape controller is maintained over bidirectional data and status channels. A teletypewriter enables communication with the computer for program altering and diagnosis of malfunctions. A magnetic tape transport enables loading of the program into the computer and stores data from the optically scanned documents on magnetic tape for further processing. The magnetic tape controller provides the interface between the computer and the magnetic tape transport.

The on-line character correction (OLCC) option provides on-line character correction for characters rejected by the reader recognition logic or the system edit software. This OLCC consists of interface logic added to reader logic door 2 and a CRT video display monitor and OLCC electronics. The display unit is mounted on the system teletypewriter or sits on the System 17 desk.

The active or inactive status of the OLCC is controlled by user application controlware. If the OLCC is active when the reader generates a character reject, audible and visible alarms are activated and the video display monitor displays the video as scanned by the reader. For ANSI Size I characters with a character pitch of 10 per inch, five characters are displayed with the rejected character centered and underlined.

The operator performs character correction by typing the correct character, followed by a

carriage return $_{\textcircled{B}}$, on the system teletypewriter. When the rejected character has been corrected, the display blanks out, the alarm turns off, and the reader resumes normal scanning.

Option	Description
Handprint Alphanumerics CW126 Model No. depends on S/N of CJ122.	Field or factory installed. Recognizes handprinted 0 through 9, upper case C S T X and Z, and symbols $+ - = $. Recognizes printed 3/16 inch gothic characters or European 1 and 7 by QSE only.
Handprint Alphanumerics CW207A. Available on CJ122, Models G and H.	Field or factory installed. Recognizes handprinted 0 through 9, upper case C S T X Z, symbols + - = , and European 1 and 7; also recognizes printed 3/16 inch gothic numerals. Font groups recognized are program-selectable.
ANSI-OCR-A Size IV CW131	Option that changes optical scaling of reader when installed and is selectable under program control. Factory installed only.
Marking Pen CK109	Solenoid-activated device with pen that places red, yellow, or blue dot on documents left margin, under program control. Field or factory installed.
Journal Tape CJ503	Option that allows reader to read cash register tape, consists of feed spindle and driven take-up spool with tape hold-down idler arms. Width ranges from 3 to 4-1/2 inches. Maximum roll diameter is 4 inches. Minimum character field is 12 inches. Requires a minimum trailer header of 30 inches. Factory installed only.
On-Line Character Correction CC107	Self-contained cathode ray tube video display which shows rejected character and character on either side of rejected character. Operator corrects on-line by code insertion via system teletype keyboard. Field or factory installed.
Six Lines/Inch CW133	Option that enables reader to read lines spaced or pitched at six lines to the inch. Modular logic assembly added to logic rack. Contains full character buffer memory, line tracking logic, and timing con- trol logic. Factory installed only.
Mirror Image	Program selectable electronics package which enables reader to read characters in normal position, inverted position, and mirror image of each: B , B , B , B . Provides right to left scan capabilities.

TABLE 1-1. READER OPTIONS

Option	Description
Alternate Character Sets	A maximum of three alternate character sets may be installed plus handprint; a fourth option may be in- stalled by QSE. When installed, each alternate char- acter set is controlled by a separate control line from the buffer controller. Field or factory installed

TABLE 1-1. READER OPTIONS (CONT'D)

Font Option	Description	Character Set Read
ANSI-OCR-A Lower Case Character Set CW132	Pluggable option	abcdefghijklmnopqrstuvwxyz
E13B Character Set CW134	ANSI standard for mag- netic ink character recog- nition (MICR)	01234567891
7B Character Set CW137	For credit card applica- tion. Requires ANSI- OCR-A Size IV option.	0123456789 EP
12F Character Set CW138	Pluggable option	0123456789 H-,
1428 Numeric Character Set CW139	Pluggable option	0123456789 H-
OCR-B (M65) Size I Character Set CW140	Pluggable option	0123456789 -+¤ #
407-1 Character Set CW141	Pluggable option	0123456789 ¤-
1428 Alphameric Charac- ter Set CW150	Pluggable option	0123456789CNSTXZ7
Rabinow Character Set CW149	Pluggable option	┙⋈⋬⋩⋩∜↑┇═╿
OCR-B (71) Numerics CW208	Pluggable option	0123456789 +<> = -
OCR-B (71) Alphanumerics CW195	Pluggable option	0123456789 +<>,=;-'*.

TABLE 1-2. READER OPTION ALTERNATE CHARACTER SETS

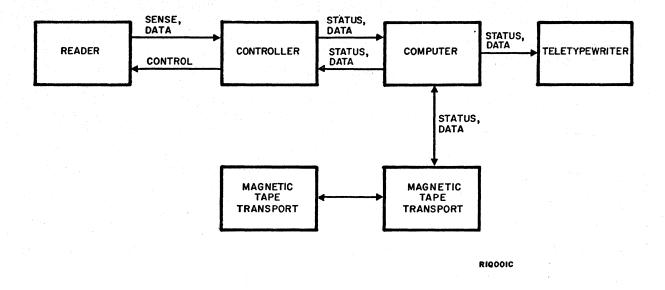
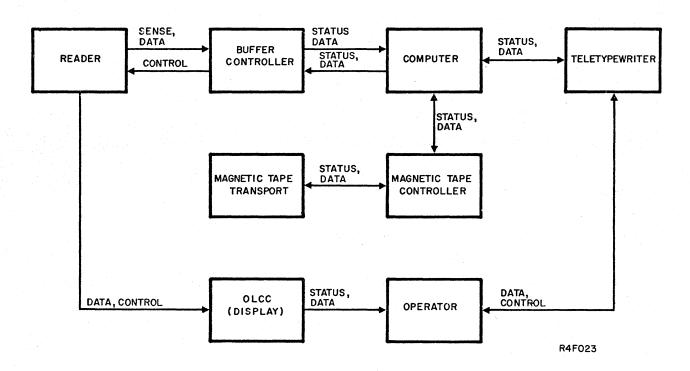
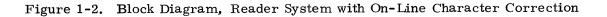


Figure 1-1. Typical Reader System

A block diagram of a reader system with on-line character correction is shown in Figure 1-2.





The six-lines-per-inch option enables the CJ122 to read pages or documents which contain single-spaced typed lines or lines preprinted at six to the inch. When installed, the option is selectable via the system controlware.

The six-lines-per-inch option is a factory-only installable option for the CJ122. It is packaged as a modular logic assembly which is added to the reader's logic rack. This logic module contains timing and control logic, line tracking logic, and a shift register buffer memory capable of buffering 0.2 inch of scanned information.

The handprint unit option enables the CJ122 to read certain handprinted characters (see table 1-1). Handprint operation is selectable by system controlware.

CONTROLWARE

Various controlware programs are available for use with the reader. These are listed in table 1-3.

The buffer controller module controls the operation of the reader and communication with the user system. Since the buffer controller is programmable, not hard-wired, a reader driver was developed as part of the SCOPE (Supervisory Control Of Program Execution) system.

OPERATING CHARACTERISTICS

Operating characteristics of the reader are listed in table 1-4; OLCC operating characteristics are listed in table 1-5.

Program	Function
GRASP (<u>G</u> eneralized <u>R</u> ead <u>A</u> nd <u>S</u> imulate <u>P</u> rogram)	Enables user to specify document reading format and magnetic tape output format by optically reading docu- ment specification sheets. Can be used on all reader systems.
Tape SCOPE	System supervisor program. Enables generation of object program from assembly language source pro- gram on magnetic tape. Requires two magnetic tape transports and 8K memory capability.
SETUP (Source Edit Tape Update Program)	Enables user to write onto magnetic tape an assembly language or DRAFT source statement program from optically read sheets. Source programs previously written on tape may be updated using SETUP. SETUP operates under control of Tape SCOPE. Requires two magnetic tape transports and 8K memory capability.
DRAFT (Document <u>R</u> ead <u>And</u> Format <u>T</u> ranslator)	Enables user to compile and execute an object program from optically read source statements and data. Requires two magnetic tape transports and 12K mem- ory capability.

TABLE 1-3. READER CONTROLWARE

Item	Specifications
Paper weight	18 to 38 pounds
Paper length 18 to 24 pound paper 24 to 38 pound paper	3-1/4 to 12-5/8 inches 3-1/4 to 5-1/4 inches
Paper width 18 to 24 pound paper 24 to 38 pound paper	4-7/8 to $11-1/8$ inches [†] or $4-7/8$ to 12 inches ^{††} $4-7/8$ to $8-1/2$ inches
Aspect (length/width) ratio	0.64 minimum except 3-1/4 by 7-3/8 inches standard tab cards or other sizes approved in advance by OCR Operations.
Double-feed prevention	Brushback roller on feeder. Photoelectric doubles detector at start of conveyor sense double-fed docu- ment and stops transport.
Recommended input hopper capacity Cards Pages	5-inch stack 3-1/2-inch stack
Paper transport velocity Forward (controller selected) Reverse	5 inches per second 12.5 inches per second 20 inches per second 40 inches per second 5 inches per second
Transport position accuracy	Maximum ±0.024 inch error per motion command at 20 ips or slower. Note: Controlware computes cen- terline of each line read and adjusts each line step taken so that error is noncumulative.
Instantaneous reading rate	750 characters per second for characters pitched at 10 per inch
Scan rate	75 inches per second
Ambient temperature range Operating Storage	60° to 80° F 30° to 150° F
Relative humidity Operating	30% to 60% 5% to 95% (no condensation)

TABLE 1-4. READER OPERATING CHARACTERISTICS

^{††}CJ122 Models D, E, F, G, H, and K

Item	Specifications
Heat dissipation	11,600 BTU/hour [†] or 9500 BTU/hour ^{††}
Altitude	-1,000 feet to 6,000 feet above mean sea level
Power	177-222 vac, 3 phase, 60 Hz 177-222 vac, 3 phase, 50 Hz
Maximum character substitu- tion rate Imprinter High-speed printer and journal tape Electric typewriter using plastic ribbon	1 per 20,000 characters 1 per 50,000 characters 1 per 100,000 characters
Maximum character reject rate Imprinter High-speed printer and journal tape Electric typewriter using plastic ribbon	1 per 2,000 characters 1 per 5,000 characters 1 per 10,000 characters
Type font (standard) OCR-A Alphanumerics OCR-B Alphanumerics	ABCDEFGHIJKLMN0P@RSTUVWXYZ ¬·/;=-?:+{}&%\$*"'■ 0123456789 +<>,=;-'*. ?\$:¤()&/%@# ABCDEFGHIJKLMN0P@RSTUVWXY7
OCR-B Alphanumerics [†] CJ122 Models C, D, F, and J ^{††} CJ122 Models E, G, H, and K	0123456789 +<>,=;-'*. ?\$:¤()&/%@# ABCDEFGHIJKLMNOPQRSTUVWXYZ

TABLE 1-4. READER OPERATING CHARACTERISTICS (CONT'D)

and the second

PHYSICAL DESCRIPTION

READER

The reader is housed in a pair of welded-frame modules. The reader module contains the edger, conveyor, optics system, read electronics, sorter, stacker, power control unit, power supplies, and the vacuum source. The controller module houses the buffer controller and associated power supplies, cooling system for the buffer controller, and the feedup table. During operation, both modules are bolted together. Casters are provided to facilitate placing the reader in position, and adjustable feet enable the equipment to be leveled. Physical characteristics are listed in table 1-6.

Item	Specifications
Power input voltage	115 vac nominal, single phase
Ambient temperature range	+60° to +90° F
Altitude	1,000 feet below to 6,000 feet above sea level
Relative humidity	20% to 60% (no condensation)
Display Size Refresh rate	4 x 5 inches 140 times per second
Clock frequency entering data 56 bits from reader 8 bits in OLCC Displaying data 64 bits	Reader Shift Clock 2. 5 MHz 1 MHz
Display scan width Size I Size IV Handprint	0.513 inch 0.747 inch 0.661 inch
Minimum number character positions dis- played Size I at 10 characters per inch Size IV at 7 characters per inch Handprint at 5 characters per inch	5 character positions of 0. 100 inch each 5 character positions of 0. 143 inch each 3 character positions of 0. 200 inch each

TABLE 1-5. OLCC OPERATING CHARACTERISTICS

TABLE 1-6. READER PHYSICAL CHARACTERISTICS

Item	Specification	Item	Specification
Weight Reader module Controller module Dimensions Reader module Height Width Depth	1400 pounds 400 pounds 57 inches 72 inches 34 inches	Dimensions (cont'd) Controller module Height Width Depth Reader assembled Height Width Depth	48-1/2 inches 26-1/4 inches 34 inches 57 inches 98-1/2 inches 34 inches

CC-107 OLCC

The OLCC consists of the following:

- a. a Tektronix 604 Display Monitor and OLCC electronics mounted on one chassis assembly
- b. reader interface logic

Five integrated circuit elements are added to the reader logic door 2, board 3 to interface the necessary signals to the OLCC electronics.

The chassis assembly is either mounted on the side of the system teletypewriter at 22 degrees from vertical (OLCC Models A, B, and C) or stands alone for desk mounting (OLCC Model D).

The OLCC electronics consists of the following components:

a. three dc power supplies

- e. four coaxial output cables to the display monitor
- b. two wire-wrap, printed circuit cards
- g. a buzzer

f.

a control panel

- c. a power connector and cable from the display monitor
- d. an input connector and cable from the reader

The three dc power supplies (PS01 through PS03) are mounted on the chassis assembly beneath the display monitor as shown in figure 1-3. AC power is received from the display monitor via cable W5 and converted to +5 vdc, -5 vdc, and -12 vdc required by the OLCC electronics.

Logic for the OLCC electronics is contained on two printed circuit cards (J02 and J03) mounted on the chassis assembly as shown in figure 1-3. Standard TTL logic elements, hybrid interface circuits, MOS shift registers, and discrete components are mounted on the two cards.

Input signals from the reader are received on a 24-pin connector and cable (J01) as shown in figure 1-3.

The vertical deflection (-Y), horizontal deflection (+X and -X), and beam intensity (+Z) outputs from the OLCC electronics are connected to the display monitor by four coaxial cables (W1 through W4) as shown in figure 1-3.

Operational control for both the display monitor and the OLCC electronics is provided at the control panel (see figure 2-22). A description of controls and indicators is contained in section 2, table 2-15. A buzzer (DS02), which sounds when the rejected character is displayed, is mounted on the chassis assembly as shown in figure 1-3.

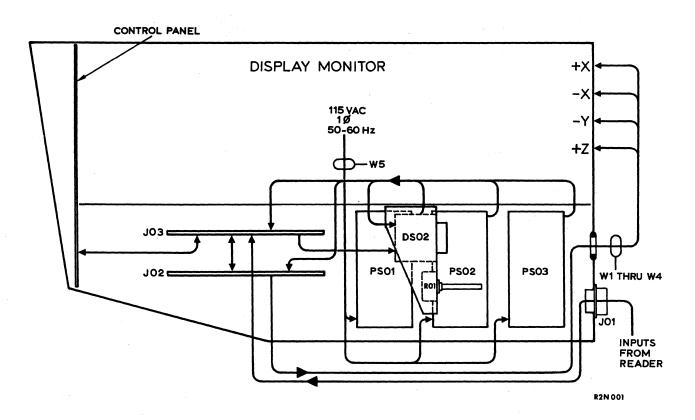


Figure 1-3. OLCC Components and Interconnections

CW133 SIX-LINES-PER-INCH

The six-lines-per-inch option is an addition to the reader's logic only. One modified IC panel must be added to logic door 1 (A02) with an additional cable to connect door 1 to door 2. Present cooling provided for the reader's logic and recognition racks will be adequate to handle any requirements for cooling the six-lines-per-inch option.

CW126 OR CW207 HANDPRINT UNIT

The handprint unit consists of four logic doors physically added to the reader frame and connected to the reader by power and logic cables. Appropriate interface logic is added to the reader logic rack. A ± 5 vdc power supply is added to the reader frame to supply handprint unit logic voltage and a rectifier-filter is added to the reader frame to convert sun gun ac voltage to dc.

ELECTRICAL DATA

Electrical requirements and power supply characteristics of the reader are listed in table 1-7; electrical characteristics of OLCC are listed in table 1-8, and electrical characteristics for six-lines-per-inch are listed in table 1-9. Electrical characteristics for the buffer controller power supply are listed in Reader Controller Manuals 60324700 (CJ122 Models C, D, F, and J) and 48935300 (CJ122 Models E, G, H, and K). Electrical characteristics for the handprint unit are listed in the appropriate handprint unit manual (see preface).

Item	Specifications
Reader Module	
Input voltage (60 Hz system)	177-222 vac $\pm 10\%$ vac, 30 amperes/ phase, 3 phase with ac neutral and earth ground (5 wire) 59 - 60.6 Hz
Input current Operating Start-up Standby	11.3 amperes/phase [†] or 10.6 amperes phase ^{††} 200 amperes/phase, single cycle 2 amperes, single phase
Operating power	4.07 kva, 3.4 kw [†] or 3.68 kva, 2.8 kw ^{††}
Input voltage (standard) (50 Hz system)	177-222 vac, 30 amperes, 3 phase, 5 wire
Input voltage (option)	408/380/220/195 vac (line-to-line), 3 phase, 5 wire, (wye), 4 wire (Delta)
Input power	30 amperes, 3 phase, 5 wire (wye), 4 wire (Delta)
Power Control Unit	
Input voltage	208 vac, 3 phase, 50 or 60 Hz
Input current	15 amperes/phase, maximum
Output voltages	208 vac, 3 phase and 120 vac, 1 phase
Output current	15 amperes/phase, maximum
3 Phase Regulator	
Input voltage	208 vac nominal, 3 phase, (177-222 vac)
Input frequency	60 Hz nominal (59.0 - 60.6 Hz) 50 Hz nominal (49.2 - 50.5 Hz)
[†] CJ122 Models C, D, F, and J ^{††} CJ122 Models E, G, H, and K	

TABLE 1-7. READER ELECTRICAL CHARACTERISTICS

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Item	Specifications
Input current	5 amperes/phase, maximum at nomina adjustment
Output voltages	Adjustable from 150 to 220 vac, 5 channels (line-to-neutral)
Regulated ac output	232 vac - 3 phase (line/neut) \pm 3.5 vac
Output current	5 amperes/phase absolute maximum regulated current
A Supply	
Input voltage	232 vac nominal, 3 phase (line-to-line) square wave regulated from 3 phase regulator
Input frequency	60 Hz nominal (59.0 - 60.6 Hz) 50 Hz nominal (49.2 - 50.5 Hz)
Input current	0.4 ampere/phase, maximum
Nominal output voltages	+5 $\pm 2\%$ vdc [†] $\pm 15 \pm 2\%$ vdc [†] +12 $\pm 10\%$ vdc nonadjustable +10 $\pm 10\%$ vdc nonadjustable 120 vac adjustable -0 to 120 vac
Output currents	+5 vdc: 16 to 22.0 amperes +15 vdc: 0.25 to 0.50 ampere -15 vdc: 1.0 to 2.0 amperes +12 vdc: 2.0 to 4.0 amperes +10 vdc: 0.165 to 0.33 ampere 120 vac: 0 to 10 amperes
B Supply	
Input voltage	232 vac nominal, 3 phase square wave regulated from 3 phase regulator
Input current	1.20 ampere/phase maximum
Output voltage	$\pm 20 \pm 3\%$ vdc nonadjustable
Output currents	+20 vdc: 4.0 to 8.0 amperes -20 vdc: 1.25 to 2.5 amperes

TABLE 1-7. READER ELECTRICAL CHARACTERISTICS (CONT'D)

Item	Specifications
High Voltage Power Supply	
Input voltage	120 vac nominal (102-128 vac), single phase (50 or 60 Hz) 220 vac nominal (187-235 vac), single phase (50 Hz)
Input frequency	60 Hz nominal (59.0 - 60.6 Hz) 50 Hz nominal (49.2 - 50.5 Hz)
Input current	1.7 amperes/phase, maximum 0.95 ampere/phase, maximum
Output voltage	-1450 vdc nominal (adjustable from -1150 to -1650 vdc)
Output currents	19 - 50 milliamperes up to -1650 vdc
Interlock Control Power Supply	
Input voltage	208 vac nominal (177-222 vac)
Input frequency	60 Hz nominal (59.0 - 60.6 Hz) 50 Hz nominal (49.2 - 50.5 Hz)
Input current	0.7 ampere
Nominal output voltages	+6 vdc nonadjustable +5 vdc nonadjustable
Output currents	+6 vdc: 6 amperes +5 vdc: 1.0 ampere
Transport Servo Power Supply	
Input voltage	208 vac nominal (177-222 vac)
Input current	2 amperes/phase maximum
Input frequency	60 Hz nominal (59.0 - 60.6 Hz) 50 Hz nominal (49.2 - 50.5 Hz)
Output voltages	±45 vdc nonadjustable
Output currents	+45 vdc: 0 - 12 amperes -45 vdc: 0 - 5 amperes

TABLE 1-7. READER ELECTRICAL CHARACTERISTICS (CONT'D)

Item	Specifications
Buffer Controller Power Supply (CJ122 Models C, D, F, and J)	
Input voltage	232 vac nominal, square wave, 3 phase
Input current	3.0 amperes/phase maximum
Input frequency	50/60 Hz nominal (49.2 - 60.6 Hz)
Output voltages	-2 vdc adjustable -1.7 vdc to -2.3 vdc +6 vdc adjustable +5.1 vdc to +6.9 vdc -6 vdc adjustable -5.1 vdc to -6.9 vdc +8 vdc adjustable +6.8 vdc to +9.15 vdc +16 vdc adjustable +13.6 vdc to +18.4 vdc
Output currents	-2 vdc channel = 11.25 to 15.0 amperes +6 vdc channel = 11.25 to 15.0 amperes -6 vdc channel = 52.5 to 70.0 amperes +8 vdc channel = 2.25 to 3 amperes +16 vdc channel = 0.75 to 1 amperes
Buffer Controller Power Supply (CJ122 Models E, G, H, and K)	
Input voltage	232 vac nominal, square wave, 3 phase
Input current	3.0 amperes/phase maximum
Input frequency	50/60 Hz nominal (49.2 - 60.6 Hz)
Output voltages	+30 vdc nonadjustable +6 vdc nonadjustable -6 vdc nonadjustable +5 vdc adjustable +4.5 vdc to 5.5 vdc -5 vdc adjustable -4.5 vdc to 5.5 vdc
Output currents	+30 vdc channel = 1 to 3A +6 vdc channel = 1 to 2A -6 vdc channel = 1 to 2A +5 vdc channel = 8 to 15A -5 vdc channel = 0 to 1/2A

TABLE 1-7. READER ELECTRICAL CHARACTERISTICS (CONT'D)

Item	Specifications	
AC Power		
Input voltage	115 vac nominal, single phase, 3 wire (1 phase, neutral, and ground)	
Frequency input current	50-60 Hz nominal, 1.5 amperes maximum	
Power Supply 1 and 2		
AC input	105 to 125 vac, 47 to 63 Hz	
DC output voltage	± 5 vdc adjustable (0 to ± 5 vdc)	
DC output current	3 amperes maximum	
Power Supply 3		
AC input	105 to 125 vac, 47 to 63 Hz	
DC output voltage	± 12 vdc adjustable (0 to ± 12 vdc)	
DC output current	1.5 amperes maximum	

TABLE 1-8. ELECTRICAL CHARACTERISTICS OF OLCC

TABLE 1-9. ELECTRICAL CHARACTERISTICS OF SIX-LINES-PER-INCH

Item	Specifications
Components	All electronic components are TTL MSI and SSI, and TTL I/O -compatible MOS.
Voltage Requirements	The six-lines-per-inch option utilizes +5 vdc and -15 vdc, both of which are provided by the basic reader.
Input/Output	Two signals are generated within the six-lines-per-inch option and are made available to the controller to facilitate line positioning.
Indent Enable	Logical 0 when the line being read is vertically low enough within the optics that another line (indented) could also lie wholly within the optics but above the line being read.
Indent	Logical 0 indicating that after an Indent Enable occurred, a full profile was found above the line being read and that the six-lines-per-inch option has adjusted to read the higher line.

1-15/1-16



SECTION 2

OPERATION AND PROGRAMMING

INTRODUCTION

A description of the controls, indicators, and test points as well as procedures for operating and programming the reader and On-Line Character Correction Unit (OLCC) are contained in this section. Operating procedures and descriptions of controls, indicators, and test points are in tabular form. Each table is keyed to a figure which shows the location of an assembly, control, indicator or test point. Figures 2-1, 2-2, 2-3, and 2-4 show the location of each assembly or panel discussed in section 2. The operating procedures contained in this section are limited to the turn-on and turn-off procedural steps required to apply power to the reader and OLCC, and document and journal tape loading.

PROGRAMMING

For detailed programming information, refer to the 955 Reader Controller Reference Manual (CJ122 Models C, D, F, and J) (Pub. No. 60324600), or the CJ122 Controller Customer Engineering Manual (CJ122 Models E, G, H, and K) (Pub. No. 48935300).

OPERATING PROCEDURE

In tables 2-14, 2-16, 2-17, and 2-18 of the operating procedures, the numbers in the Step column indicate the operating sequence, the Equipment column indicates the equipment panel at which each step is to be performed, and the Procedure column describes the action to be taken and the results of these actions. If the results are not as indicated, proceed to TROUBLESHOOTING under section 6.

Controls, Indicators, and Test Points

The controls, indicators, and test points for each panel of the reader and OLCC are described in tables 2-1 through 2-15. The tables are keyed to figures 2-5 through 2-22, which show the location of each control, indicator, and test point.

Power Turn-On/Turn-Off

Table 2-16 describes the switch operating sequence to energize the equipment. Table 2-18 describes the switch operating sequence to deenergize the equipment.

Document and Tape Loading

Table 2-17 describes the procedural steps to load a document into the reader. Table 2-14 describes the procedural steps to load Journal Tape (option) into the reader.

Operator's Control Panel

The operator's control panel is located above the edger (see figures 2-1 and 2-2). The controls and indicators are called out in table 2-1 and illustrated in figure 2-5. Except for POWER and FEEDUP ENABLE, indicators on the operator's control panel are directly concontrolled by the controller. Proper operation requires that the controller be loaded with the proper controlware. The functions of the control indicators and switches may be modified by maintenance mode switches. For details of these functions refer to table 2-2.

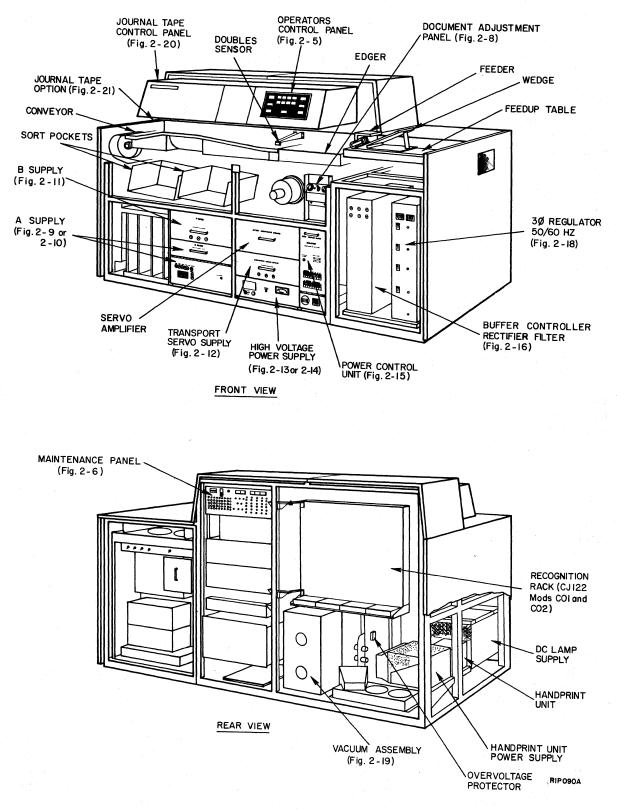


Figure 2-1. Page and Document Reader (CJ122 Models C, D, F, and J)

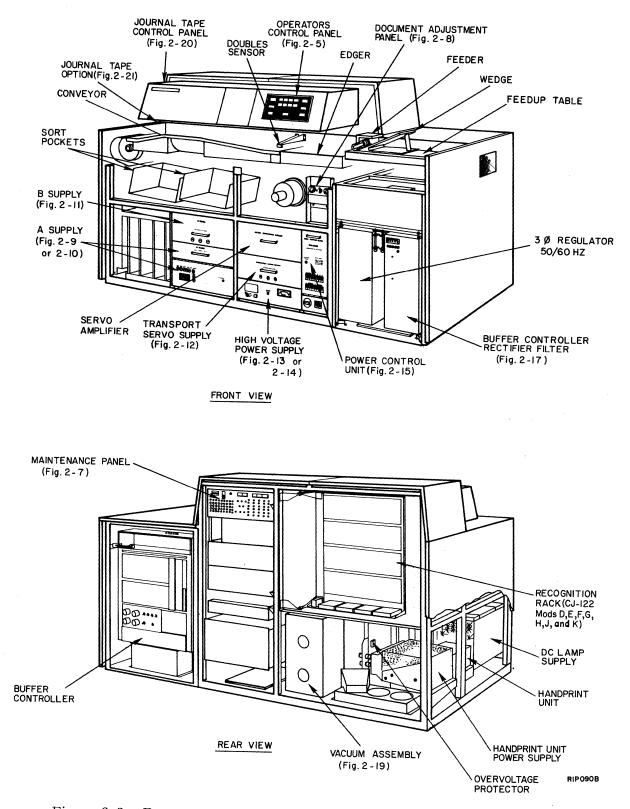


Figure 2-2. Page and Document Reader (CJ122 Models E, G, H, and K)

ON-LINE CHARACTER CORRECTION UNIT (FIGURE 2-29)

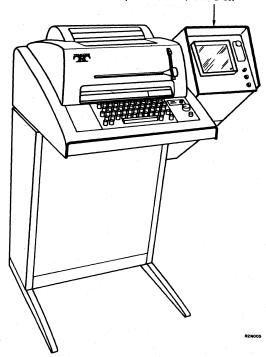


Figure 2-3. On-Line Character Correction Unit (OLCC) (CC-107 Model A, B, or C)

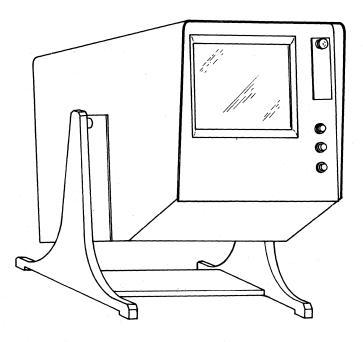


Figure 2-4. On-Line Character Correction Unit (OLCC) (CC-107 Model D)

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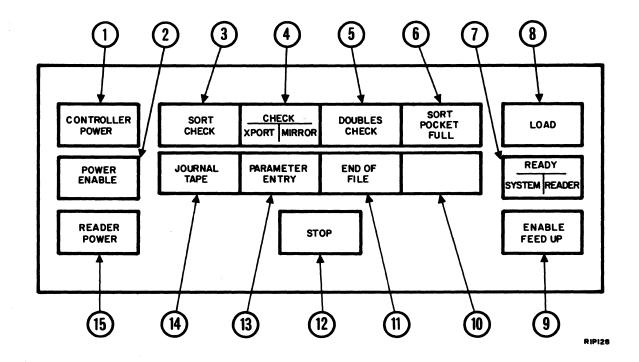


Figure 2-5. Operator's Control Panel Controls and Indicators

TABLE 2-1. OPERATOR CONTROL PANEL CONTROLS A	AND	D INDICATOR	\mathbf{S}
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Figure 2-5 Index No.	Reference Designation	Control or Indicator	Function
1	S09 DS07-DS08	CONTROLLER POWER pushbutton switch and indicator lamps	Enables and disables ac power to the controller power supplies if the POWER ENABLE switch is set to ON. The indi- cator lamps light when power to the con- troller is ON and all controller dc supplies are operational.
2	S06 DS19-DS20	POWER ENABLE pushbutton switch and indicator lamps	This switch enables ac power to the reader and controller and functions as an emergency off switch. When the POWER ENABLE switch is set to ON the POWER ENABLE indicator lamps light.
3	DS21-DS22	SORT CHECK indi- cator lamps	A logical 1 level, originating in the con- troller, energizes the SORT CHECK indi- cator lamps when a detectable malfunction has occurred at a sort station.

TABLE 2-1. OPERATOR CONTROL PANEL CONTROLS AND INDICATORS (CONT'D)

Figure 2-5 Index No.	Reference Designation	Control or Indicator	Function
4	DS23-DS24	CHECK XPORT/ MIRROR indicator lamps	A logical 1 level, originating in the con- troller, energizes the XPORT CHECK indicator lamps when a detectable mal- function has occurred in the transport area .
			A logical 1 level, originating in the con- troller, energizes the MIRROR CHECK indicator lamps when a detectable mal- function has occurred in the line scan mirror system.
5	DS25-DS26	DOUBLES CHECK indicator lamps	A logical 1 level, originating in the con- troller, energizes the DOUBLES CHECK indicator lamps, indicating that a double document feed has been detected.
6	DS27-DS28	SORT POCKET FULL indicator lamps	A logical 1 level, originating in the con- troller, energizes the SORT POCKET FULL indicator lamps when either of the output hoppers is full and requires oper- ator intervention to empty.
7	S05 DS17-DS18	READY SYSTEM/ READER pushbutton switch and indicator lamps	When the READY SYSTEM/READER switch is pressed, a logical 1 level, originating in the reader, indicates to the controller that the READY switch has been pressed.
			A logical 1 level, originating in the con- troller, energizes the READY indicator lamps, indicating that the READY switch was (or is being) pressed and that reader ready and controller ready are present. The READY indicator is repre- sentative of the READER/CONTROLLER being mechanically ready and on-line to the computer.
8	S08 DS29-DS30	LOAD pushbutton switch and indicator lamps	When the LOAD switch is pressed, a logi- cal 1 level, originating in the reader, indi- cates to the controller that the LOAD switch is depressed and that document loading and clearing should be performed.

Figure 2-5	Reference	Control or Indicator	Function
Index No.	Designation		The LOAD switch will be active only
(cont'd)			during a STOP (reader not ready) con- dition.
			Load function (switch held depressed for less than 2 seconds):
			A logical 1 level, originating in the controller, energizes the LOAD indicator lamps. The LOAD indicator lamps will light with depression of the LOAD switch and will remain on until a document is at ready position.
			Clear function (switch held depressed for more than 2 seconds):
			When the LOAD switch is held de- pressed for more than 2 seconds, the transport will start again (after normal load function) and will run continuously as long as the switch is depressed. This clears the transport of documents.
9	S04 DS05-DS06	ENABLE FEED UP pushbutton switch and indicator lamps	Enables and disables the feed-up table drive clutch. The indicator lamps light when the feed-up table is disabled for document loading.
10	DS15-DS16	Spare	Not used.
11	S03 DS13-DS14	END OF FILE push- button switch and indicator lamps	This switch permits data previously read to be stored in the 1700 computer. When the END OF FILE switch is pressed, a logical 1 level originates in the controller, energizing the END OF FILE indicator lamps; END OF FILE toggles ON or OFF, based on its previous condition and the END OF FILE switch being depressed. END OF FILE will also clear on clear controller or master clear. The END OF FILE indicator lamps will reflect the con- dition of END OF FILE status to the com- puter and will be active only during a STOP condition.

TABLE 2-1. OPERATOR CONTROL PANEL CONTROLS AND INDICATORS (CONT'D)

Figure 2-5 Index No.	Reference Designation	Control or Indicator	Function		
12	S07 DS03-DS04	STOP pushbutton switch and indicator lamps	When the STOP switch is pressed, a logi- cal 1 level originates in the reader, indi- cating to the controller that the STOP switch is depressed.		
			A logical 1 level, originating in the con- troller, energizes the STOP indicator lamps when the reader has lost its mechanical or functional ready condition or the STOP switch has been depressed. The STOP indicator is representative of a "reader not ready" status to the com- puter, and "reader off line" to the oper- ator.		
13	S10 DS11 - DS12	PARAMETER ENTRY pushbutton switch and indicator lamps	When the PARAMETER ENTRY switch is pressed, a logical 1 level originates in the reader, enabling PARAMETER ENTRY. Signal will cause controller to generate a parameter ready only condition.		
			A logical 1 level, originating in the con- troller, energizes the PARAMETER ENTRY indicator lamps. Indicator lamps light when switch is depressed and con- troller is holding parameter ready only condition.		
14	S02 DS09-DS10	JOURNAL TAPE pushbutton switch and indicator lamps (option only)	Enables and disables journal tape option. Light indicator lamps when switch is enabled.		
15	S01 DS01-DS02	READER POWER pushbutton switch and indicator lamps	Enables and disables reader ac power if the POWER ENABLE and CONTROLLER POWER switches are set to ON. The indicator lamps light when power to the reader is on and all dc supplies are operational.		

TABLE 2-1. OPERATOR CONTROL PANEL CONTROLS AND INDICATORS (CONT'D)

Maintenance Panel

The maintenance panel is located in the logic rack (see figures 2-1 and 2-2). The controls and indicators are called out in table 2-2 and illustrated in figures 2-6 and 2-7. The purpose of the maintenance panel is described in section 4.

Reader Interlock Status Switches

CAUTION

Only experienced service personnel should ever use the interlock bypass switches.

The READER INTERLOCK STATUS BYPASS switches are enabled only when the maintenance mode switch is set to MAINTENANCE. When any bypass switch is set to the BYPASS position, the READER INTERLOCK STATUS BYPASS indicator associated with the switch lights.

Interlock and Operational Failure Status Indicators

In normal operation, failure in the interlock system will cause automatic system power OFF with the exception of the interlock supplies which power the interlock, fault indicating, and other mode switches and indicating circuits.

The interlock and operational failure status indicators will light when a failure occurs as long as the POWER ENABLE switch is ON when the failure occurs, even though, in the case of interlock and controller running faults, all other parts of the system have been shut down automatically. In MAINTENANCE mode, fault sensors can be overridden by setting the corresponding READER INTERLOCK STATUS BYPASS or CONTROLLER INTERLOCK BY-PASS switches.

Voltage Monitor

The voltage monitor is a group of maintenance panel test points that monitor all system low voltage dc power supply voltages. Three test points are provided for dc common.

Timing and Control

The maintenance panel has 12 key signals available at test points to facilitate rapid fault isolation. The GEN SYNC #1 and #2 are program selectable via the buffer controller.

The following signal test points are available:

Phas
Char
Read
Data
Mair

Phase Generator Character Peak Read Data Ready Main Clock

To supplement the above, a READ TIMING CONTR/NORMAL switch is provided that in the CONTR position allows, under diagnostic software operation, the "freezing" of selected reader timing and control phases.

Image Register Control

The functions of the image register control circuits are to facilitate rapid fault isolation and provide diagnostic means for the reader's recognition and timing and control circuits.

Image register control is accomplished in the MAINTENANCE mode only by means of two switches (IMAGE REG CONTROL) which control data transfer into and out of the image register.

Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
1	CTR	TOTAL DOCUMENTS counter	This meter indicates the cumulative number of documents read as a function of the leading edge detector.
2	S24	MAINTENANCE/ NORMAL switch	In the MAINTENANCE position, this switch enables all the interlock by- pass switches, FAULT RESET switch, and recognition logic control switches. In the NORMAL position, all bypass switches are disabled.
3	S23	FAULT RESET push- button switch	Resets power control logic and the mirror and transport control logic in the maintenance mode only.
4	TP01	SERVO DATA READY test jack	Not used.
5	DS28	COMM FAULT indi- cator lamp	Lights when fault occurs in command signal inputs to mirror or conveyor drive circuits.
6	S19 DS24-DS25	READY pushbutton switch with indicator lamps	The READY indicator is representa- tive of the reader/controller being ready to process documents and read. This indicator is in parallel with READY indicator on the operator's control panel.
7	DS27	MIRROR CHECK indicator lamp	If a mirror overvelocity condition is detected and the mirror shaft comes to a controlled stop (MNZV = logic 1) within approximately 75 msec., the MIRROR CHECK lamp will light; the MIRROR FAULT lamp does not light and reader power is not dropped. If
			the mirror shaft is still moving (MNZV = logic 0) after approximately 75 msec., both the MIRROR CHECK and MIRROR FAULT lamps are lit and reader power is dropped.

TABLE 2-2.	MAINTENANCE	PANEL CONTROLS,	INDICATORS,	AND TEST	POINTS
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Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
8	DS22-DS23	READER READY indicator lamps	Indicates that the reader is ON and all electrical and mechanical ready and interlock systems are up.
9	DS26	XPORT CHECK indi- cator lamp	Indicates that one of the following conditions is sensed:
			 A transport motion command was given, but the transport did not start (NZV ≠ logic 0 within 5 ms).
			 A transport motion command was dropped, but the transport did not stop (NZV ≠ logic 1 within 10 ms).
			3. The transport started to move and exceeded a velocity of 0.35 inch per second (NZV goes to a logic 0) without a motion command being given.
10	S08 DS11	LOGIC RACK BYPASS switch	Not used.
11	S03 DS05-DS06	CONTROLLER POWER pushbutton switch and indicator lamps	Turns ac power ON and OFF to the controller power supplies and fans if the POWER ENABLE switch is ON. Indicator lamps light when ac power is ON.
12	S07	HIGH TEMP RECOG RACK BYPASS switch	Bypasses the recognition rack outlet high temperature interlock circuits.
	DS10	HIGH TEMP RECOG RACK STATUS indi- cator lamp	Indicates that output air from recognition rack exceeds 125° F.
13	S02 DS03-DS04	READER POWER pushbutton switch and indicator lamps	Turns ON or OFF reader power devices. Power indicator lamps are lighted if POWER ENABLE switch and READER POWER switches are on and all ac/dc power devices with- in reader module are energized.

TABLE 2-2.MAINTENANCE PANEL CONTROLS, INDICATORS
AND TEST POINTS (CONT'D)

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Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
14	S06 DS09	Spare	Not used.
15	S01 DS01-DS02	POWER ENABLE pushbutton switch and indicator lamps	Turns main ac system power ON and OFF, controlling power in both reader and controller. Performs emergency power-off for reader and controller. Indicators are lighted
			when the POWER ENABLE switch is ON and the reader is connected to ac power source with the interlock power supply ON.
16	S05	XPORT FAULT BYPASS switch	Bypasses transport fault interlock circuits.
17	DS08 S04 DS07	MIRROR FAULT STATUS indicator lamp MIRROR FAULT BYPASS switch MIRROR FAULT STATUS indicator lamp	Indicates that either a transport motion command was dropped and the transport did not stop (NZV ‡ logic 1 within 10 ms), or that the trans- port started to move and exceeded a velocity of 0. 35 inch per second (NZV goes to logic 0) without a motion command being given. The XPORT CHECK lamp lights when- ever the XPORT FAULT lamp lights. Bypasses mirror fault interlock circuits. Indicates that a mirror overvelocity condition was detected and that the mirror shaft did not come to a con- trolled stop within approximately 75 ms. The MIRROR CHECK lamp lights whenever the MIRROR FAULT lamp lights.
18	S09	VOLT CHECK BYPASS switch	Bypasses the low voltage reader dc voltage interlock system.
	DS12	VOLT CHECK STATUS indicator lamp	Indicates that one or more of the reader voltage power sources is less than its rating.
19	S14 DS17	Spare switch and indicator	Not used.

TABLE 2-2.MAINTENANCE PANEL CONTROLS, INDICATORS
AND TEST POINTS (CONT'D)

Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
20	S15	CONTROLLER INTERLOCK READY FAULT BYPASS switch	Bypasses automatic reader and con- troller shutdown when controller does not furnish a running pulse at least every 128 ms.
	DS18	CONTROLLER INTERLOCK READY FAULT STATUS indicator lamp	Indicates failure of the controller to furnish a running pulse at least every 128 ms.
21	S10	XPORT AMP BYPASS indicator lamp	Bypasses the PC card and cable interlocks.
	DS13	XPORT AMP STATUS switch	Indicates that either a PC board is not in place or that one of the chassis cables is not connected. Applies to both the mirror and transport servo system electronics.
22	S16	CONTROLLER INTERLOCK VOLT CHECK BYPASS switch	When in up position, bypasses buffer controller dc circuit breaker inter- lock system.
	DS19	CONTROLLER INTERLOCK VOLT CHECK STATUS indicator lamp	Indicates that one or more of the controller voltages is less than its volts dc rating.
23	S11	HIGH VOLT BYPASS switch	Bypasses the high voltage fault and allows reader to operate.
	DS14	HIGH VOLT STATUS indicator lamp	Indicates that an open circuit is present in the high voltage mechanical cover and cable interlock system.
			NOTE
			If high voltage is OFF this indicator will not light.
24	S17	CONTROLLER INTERLOCK HIGH TEMP BYPASS switch	Bypasses the controller's high tem- perature 125, F interlock circuit.

TABLE 2-2. MAINTENANCE PANEL CONTROLS, INDICATORS AND TEST POINTS (CONT'D)

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Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
	DS20	CONTROLLER INTERLOCK HIGH TEMP STATUS indi- cator lamp	Indicates that output air temperature from controller electronics exceeds 125°F.
25	S12	CIRCUIT BREAKER DC BYPASS	Bypasses the reader dc circuit breaker interlock circuits.
	DS15	CIRCUIT BREAKER DC STATUS indicator lamp	Indicates that the circuit breaker con- trolling ac power to dc supplies is OFF, or that the circuit breaker con- trolling dc current to logic loads is OFF.
26	S18	CONTROLLER INTERLOCK CRKT BRKR BYPASS switch	Bypasses the controller's ac circuit breaker interlock system.
	DS21	CONTROLLER INTERLOCK CRKT BRKR STATUS indicator lamp	Indicates that one or more controller ac or dc circuit breakers is OFF.
27	S13	CIRCUIT BREAKER AC BYPASS switch	Bypasses the reader circuit breaker interlock circuit.
	DS16	CIRCUIT BREAKER AC STATUS indicator lamp	Indicates that the circuit breakers controlling ac power to vacuum supply, vacuum pump, feed-up motor, take-away motor or reader fans is OFF.
28	S20	IMAGE REG CONTROL DUMP INPUT/OUTPUT switch	In the "input" position data is taken from the top bit of the load register. In the "output" position image register data sent to the controller is from the top bit of the 15th image register column via a 14-bit serial- to-parallel converter and buffer circuits.
29	DS29	POWER CONTROL STATUS TEMP WARN indicator lamp	Lights when input air temperature to recognition or buffer controller electronics exceeds 80°F.

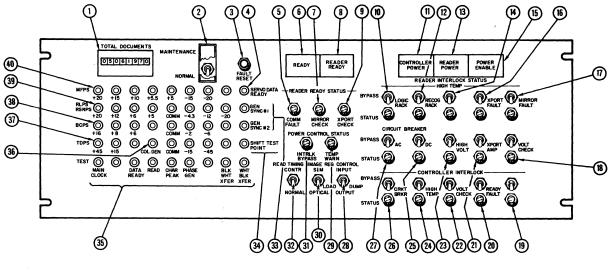
TABLE 2-2. MAINTENANCE PANEL CONTROLS, INDICATORS AND TEST POINTS (CONT'D)

Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
30	S21	IMAGE REG CONTROL LOAD SIM/OPTICAL switch	In the OPTICAL position, image register information is loaded via the optical input. In the SIM position, image register data is loaded via the controller.
			NOTE
			This switch requires the controller to be loaded with the proper control- ware, and MAINTENANCE/ NORMAL switch set to MAINTENANCE for simu- lated data.
31	DS30	POWER CONTROL STATUS INTERLK BYPASS indicator lamp	This indicator is lighted when any INTERLOCK BYPASS switch is ON and the MAINTENANCE/NORMAL switch is in MAINTENANCE.
32	S22	READ TIMING CONTR/NORMAL switch	When set to CONTR, reader clock timing can be started or stopped by buffer controller program. When set to NOR MAL, reader operates under normal reading conditions.
33	TP10 TP19	GEN SYNC #1 jack GEN SYNC #2 jack	Used for triggering oscilloscope by programming buffer controller.
34	TP28	SHIFT TEST POINT	Enables monitoring control shift pulse for 14-bit serial-to-parallel converter for data dump to buffer controller.
35	TP37, TP38, TP40 through TP43 and TP45	TEST jacks	Enables monitoring of following signals: main clock, data ready, read, character peak, phase genera- tor, black-white-transition, white- black-transition.
36	TP33	COL. GEN. test jack	Provides sawtooth for video blanking.

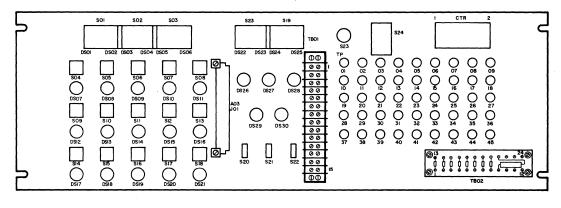
TABLE 2-2.MAINTENANCE PANEL CONTROLS, INDICATORS
AND TEST POINTS (CONT'D)

Figure 2-6/2-7 Index No.	Reference Designation	Control or Indicator	Function
37	TP36, TP35, TP31, TP30, and TP32	TDPS test jacks	Enables monitoring following voltages: +45 vdc, +15 vdc, -15 vdc, -45 vdc.
38	TP27, TP26, TP25, TP22, TP21, and TP23	BCPS test jacks	Enables monitoring following voltages: +16 vdc, +8 vdc, +6 vdc, -2 vdc, -6 vdc (CJ122 Models C, D, F, and J); +30 vdc, +5 vdc, +6 vdc, -5 vdc, -6 vdc (CJ122 Models E, G, H, and K).
39	TP18, TP17, TP16, TP15, TP13, TP12, TP11, and TP14	RLPS RSRPS test jacks	Enables monitoring following voltages: +20 vdc, +12 vdc, +6 vdc, +5 vdc, -4.3 vdc, -12 vdc, -20 vdc.
40	TP09, TP08, TP07, TP06, TP05, TP04, and TP03	MFPS test jacks	Enables monitoring following voltages: +20 vdc, +15 vdc, +10 vdc, +5.5 vdc, +5 vdc, -15 vdc, -20 vdc.

TABLE 2-2.MAINTENANCE PANEL CONTROLS, INDICATORS
AND TEST POINTS (CONT'D)



FRONT VIEW

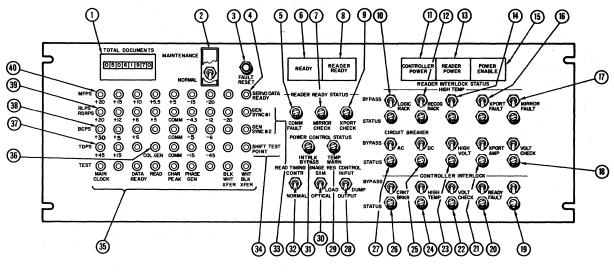


REAR VIEW

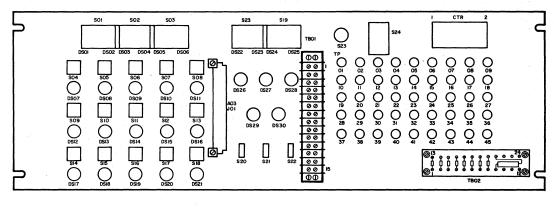
Figure 2-6. Maintenance Panel Controls, Indicators, and Test Points (CJ122 Models C, D, F, and J)

2-17

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FRONT VIEW



REAR VIEW

RIPI268

Figure 2-7. Maintenance Panel Controls, Indicators, and Test Points (CJ122 Models E, G, H, and K)

Document Adjustment Panel

The document adjustment panel is located below the edger (see figures 2-1 and 2-2). The controls and indicators are called out in table 2-3 and illustrated in figure 2-8.

TABLE 2-3. DOCUMENT ADJUSTMENT PANEL CONTROLS AND INDICATORS

Figure 2-8 Index No.	Reference Designation	Control or Indicator	Function
1	R01	DOUBLES ADJUST potentiometer	Adjusts doubles threshold level which is indicated by the DOUBLES INDICATOR.
2	CR01	DOUBLES INDICA- TOR	Lights when doubles are detected.
3	S01	PAPER GUIDE WIDTH ADJUST switch	Adjusts input hopper and edger guide plates.
4	C01	DOCUMENT THICKNESS ADJUST control	Controls position of brushback roller which is adjusted so that only one docu- ment will be fed at a time.

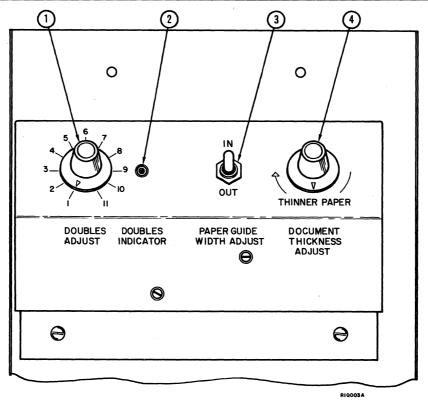


Figure 2-8. Document Adjustment Panel Controls and Indicators

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INTERNAL POWER SUPPLIES AND POWER DISTRIBUTION

The 955 power system is an integral system supplying power both for the reader and controller. This system is divided into an ac power control and distribution system and a dc power supply control and distribution system. A star point ground system is used (see figure 3-5).

NOTE

Maintenance personnel should use floating externally powered test equipment to avoid establishment of a ground loop which may cause faulty system operation.

The power system is housed in both the main frame and controller frame (see figures 2-1 and 2-2).

Main Frame Power System

The main frame power system consists of a power control unit and five power supplies. All power supplies are protected by input or output circuit breakers.

A-Power Supply

The A-power supply is a ferro-regulated power supply used to supply the dc power listed below. It is nonadjustable in CJ122 Models C, D, E, and K; ± 15 vdc and ± 5 vdc are adjustable in CJ122 Models F, G, H, and J. (The adjustable power supply is the listed spare for CJ122 Model CO1 and up). The controls and test points are called out in table 2-4 and illustrated in figures 2-9 and 2-10.

Figure 2-9/2-10 Index No.	Reference Designation	Controls and Test Points	Function
1	TP-1	+5 vdc test point	Used to monitor +5V supplied to logic and recognition racks.
2	TP - 2	+15 vdc test point	Used to monitor +15V supplied to logic and recognition racks.
3	TP - 3	-15 vdc test point	Used to monitor -15V supplied to logic and recognition racks.
4	TP-4	+12 vdc test point	Used to monitor +12V supplied to logic and recognition racks.
5	TP - 5	+10 vdc test point	Used to monitor +10V supplied to logic and recognition racks.
6	T0-4	LAMP ADJUST variac	Adjusts sun gun lamp voltage.

TABLE 2-4. A-SUPPLY CONTROLS AND TEST POINTS

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Figure 2-9/2-10 Index No.	Reference Designation	Controls and Test Points	Function
7	TP-6	COMMON test point	Common test jack for use with TPs-1 through 5, TP-7 and TP-8.
8	TP-7 TP-8	LAMP TEST test points	Used to monitor ac voltage supplied to sun gun lamp.
9	CB-5	+10 vdc circuit breaker	Controls +10V applied to logic and recog- nition racks.
10	CB-4	+12 vdc circuit breaker	Controls +12V applied to logic and recog- nition racks.
11	CB-3	-15 vdc circuit breaker	Controls -15V applied to logic and recog- nition racks.
12	CB-2	+15 vdc circuit breaker	Controls +15V applied to logic and recog- nition racks.
13	CB-1	+5 vdc circuit breaker	Controls +5V applied to logic and recog- nition racks.
14	R07	+15 ADJ potentiometer	Adjusts +15V applied to logic and recog- nition racks (CJ122 Models F, G, H, and J).
15	R08	-15 ADJ potentiometer	Adjusts -15V applied to logic and recog- nition racks (CJ122 Models F, G, H, and J).
16 •	R06	+5 vdc potentiometer	Adjusts +5 vdc applied to logic and recog- nition racks (CJ122 Models F, G, H, and J).

TABLE 2-4. A-SUPPLY CONTROLS AND TEST POINTS (CONT'D)

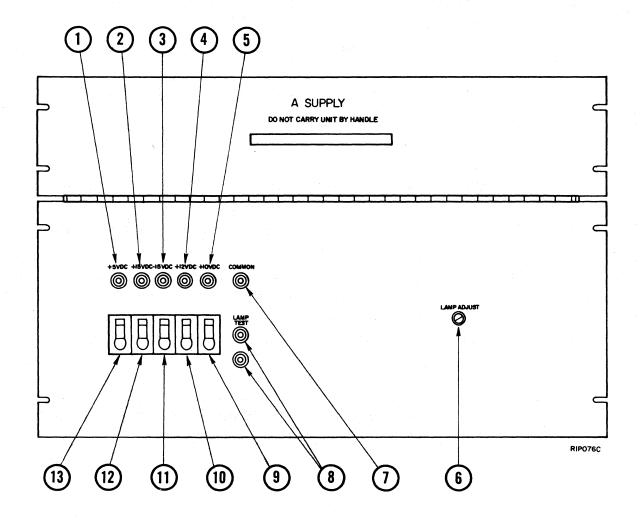
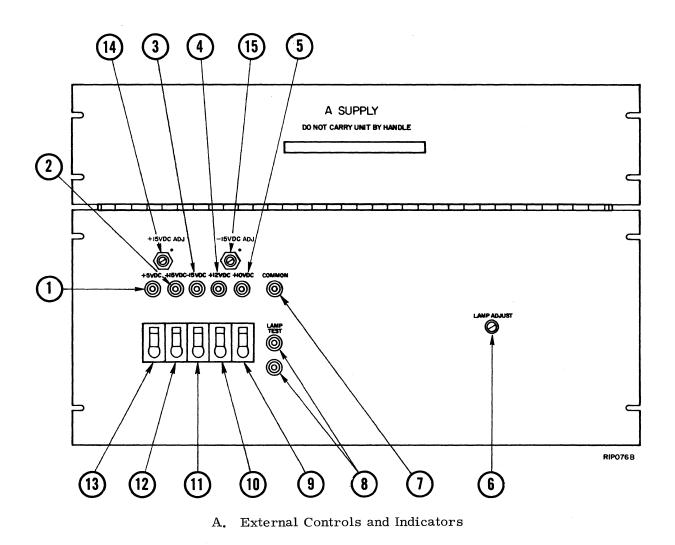


Figure 2-9. A-Supply Controls and Test Points (CJ122 Models C, D, E, and K)



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B. Internal Control (Bottom View)

Figure 2-10. A-Supply Controls and Test Points (CJ122 Models F, G, H, and J)

B-Supply

B-Supply is a regulated power supply and the output voltages are not adjustable. The test points are called out in table 2-5, and illustrated in figure 2-11.

Figure 2-11 Index No.	Reference Designation	Test Points	Function
1	TP03	-20 VDC test jack	Enables monitoring -20 vdc used by the mirror drive train.
2	TP02	COMM test jack	Common for other two test jacks.
3	TP01	+20 VDC test jack	Enables monitoring +20 vdc used by the mirror drive amplifier circuit and the solenoid driver circuits.

TABLE 2-	5. B-	SUPPL	Y TEST	POINTS
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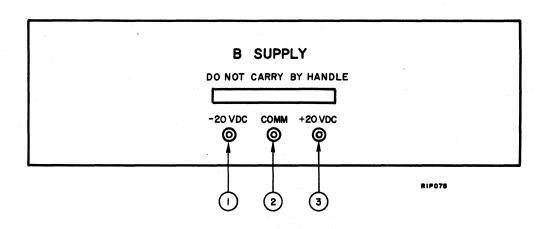


Figure 2-11. B-Supply Test Points

Transport Servo Supply

The transport servo power supply is a nonregulated dc power supply and the output voltages are not adjustable. The test points are called out in table 2-6 and illustrated in figure 2-12.

Figure 2-12 Index No.	Reference Designation	Test Points	Function
1	TP03	-45 VDC test jack	Enables monitoring -45 vdc used by the transport servo circuit.
2	TP02	COM test jack	Common test jack for other two jacks.
3	TP01	+45 VDC test jack	Enables monitoring +45 vdc used by the transport servo circuit.

TABLE 2-6. TRANSPORT SERVO SUPPLY TEST POINTS

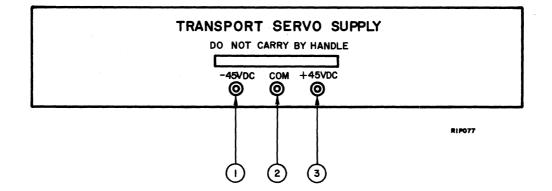


Figure 2-12. Transport Servo Supply Test Points

High Voltage Power Supply (HVPS)

The high-voltage power supply is a ferro-regulated dc power supply with the output adjustable by screwdriver adjustment from the front panel.

The controls and indicators are called out in table 2-7 and illustrated in figures 2-13 and 2-14.

Figure 2-13/2-14 Index No.	Reference Designation	Controls and Indicators	Function
1	S01	AC POWER switch	Controls ac power to high- voltage power supply.
2	DS01	AC POWER indicator	Lights when ac power is applied.
3	R01	VOLTAGE ADJUST potentiometer	Adjusts high-voltage output which is used for cathode- dynode potential on the photomultiplier tubes.
4	M01	DC VOLTS x 100 voltmeter	Indicates approximate high- voltage output.
5	N/A	NEG test point	Provides test point for negative high-voltage output (CJ122 Models F, G, H, and J).
6	N/A	POS test point	Provides test point for positive high-voltage output (CJ122 Models F, G, H, and J).

TABLE 2-7. HIGH-VOLTAGE POWER SUPPLY CONTROLS AND INDICATORS

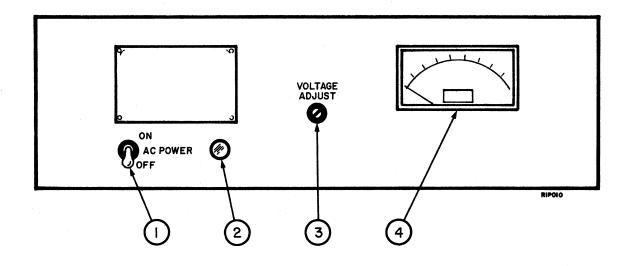


Figure 2-13. High-Voltage Power Supply Controls and Indicators (CJ122 Models C, D, E, and K)

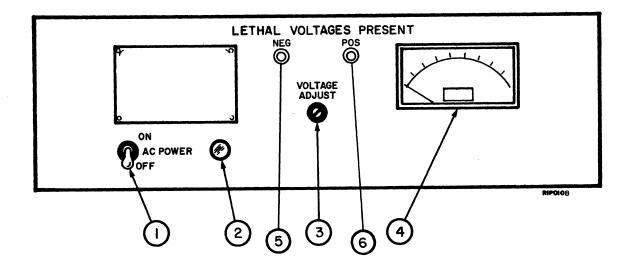


Figure 2-14. High-Voltage Power Supply Controls and Indicators (CJ122 Models F, G, H, and J)

Power Control Unit (PCU)

This unit contains the input power line filters, ac contactors, ac distribution, circuit breakers, interlock dc power supplies and the system elapsed time meter. The interlock dc power supplies are ferro-regulated with output voltages nonadjustable. Controls are called out in table 2-8 and illustrated in figure 2-15.

Figure 2-15 Index No.	Reference Designation	Control or Indicator	Function
1	CB11	6 VDC circuit breaker	Controls +6V to reader circuits.
2	CB02	POWER UP circuit breaker	Controls ac power to interlock power supply.
3	CB07	HIGH VOLTAGE circuit breaker	Controls ac power to high-voltage power supply.
4	CB06	WIDTH circuit breaker	Controls ac power to width adjust motor for feed-up table and edger.
5	CB09	TAKEAWAY circuit breaker	Controls ac power to take-away motor.
6	CB03	SYSTEM REGULA- TOR circuit breaker	Controls ac power to buffer controller.

TABLE 2-8. POWER CONTROL UNIT CONTROLS AND INDICATORS

TABLE 2-8. POWER CONTROL UNIT CONTROLS AND INDICATORS (CONT'D)

		and the second secon	
Figure 2-15 Index No.	Reference Designation	Control or mulcator	Function
7	CB01	MAIN CIRCUIT BREAKER	Controls main ac power from external source into reader.
8	M01	MAINTENANCE METER-TOTAL HOURS	Clocks time MAIN CIRCUIT BREAKER and POWER UP circuit breaker turned on and power applied to reader.
9	CB12	SPARE circuit breaker	Used for handprint option when installed. Labelled HANDPRINT in CJ122 Models F, G, H, J, and K.
10	CB04	TRANSPORT SERVO SUPPLY circuit breaker	Controls ac power to transport servo.
11	CB05	VACUUM circuit breaker	Controls ac power to vacuum motors.
12	CB10	FANS circuit breaker	Controls ac power to fans.
13	CB08	LAMP circuit breaker	Controls ac power to sun gun lamp,
14	R02	VACUUM MOTOR ADJUSTMENT potentiometer	Not used.

Controller Frame Power System

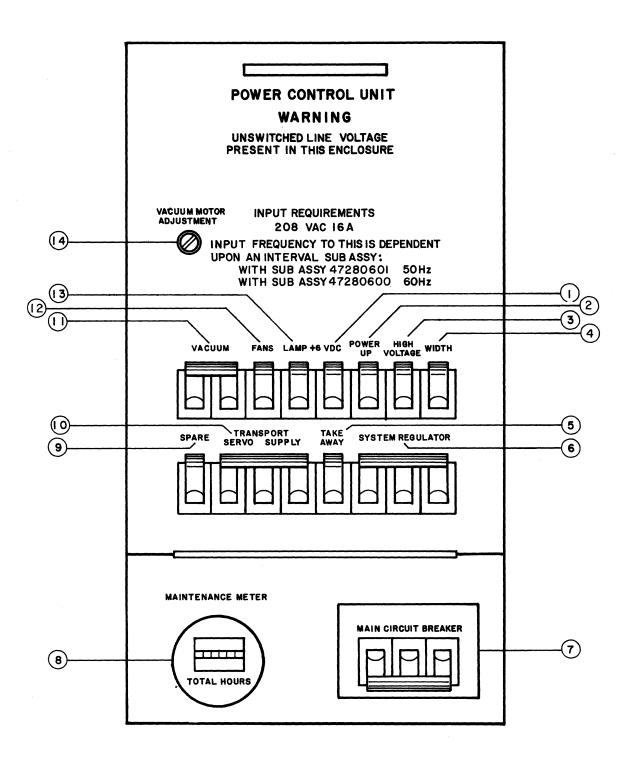
The control frame power supply consists of a 3-phase regulator 50/60 Hz system and a buffer controller rectifier/filter system. Both systems are located below the feed-up table (see figures 2-1 and 2-2).

Buffer Controller Rectifier/Filter System

The buffer controller rectifier/filter system is composed of a group of networks used to step down and filter the ac voltages from the 3-phase regulator 50/60 Hz system. The test points for the system are called out in table 2-9 and 2-10 and illustrated in figures 2-16 and 2-17.

3-Phase Regulator 50/60 Hz System

The 3-phase regulator 50/60 Hz system (CJ122 Models C, D, F, and J) contains six circuit breakers and five variacs to control and regulate the ac power into the buffer controller rectifier/filter system. The controls are called out in table 2-11 and illustrated in figure 2-18.



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Figure 2-15. Power Control Unit Controls and Indicators

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Figure 2-16 Index No.	Reference Designation	Controls	Function
1	TP04	-6 VDC test point	Used with TP02 DC COMMON to check the -6 vdc output of rectifier/filter network composed of T11, CR5, CR6, and C07 through C12.
2	TP05	+6 VDC test point	Used with TP02 DC COMMON to check the +6 vdc output of rectifier/filter network composed of T12, CR5, CR6, C13 through C16 and L01.
3	TP06	-2 VDC test point	Used with TP02 DC COMMON to check the -2 vdc output of rectifier/filter network composed of T13, CR9, CR10, C17 through C20 and L02.
4	TP03	+16 VDC test point	Used with TP02 DC COMMON to check the +16 vdc output of rectifier/filter network composed of T15, CR13 through CR16 and C23.
5	TP02	DC COMMON test	Used with other test points to check output of rectifier/filter networks.
6	TP01	+8 VDC test point	Used with TP02 DC COMMON to check the +8 vdc output of rectifier/filter network composed of T14, CR11, CR12, C21, and C22.

TABLE 2-9. BUFFER CONTROLLER RECTIFIER/FILTER TEST POINTS (CJ122 Models C, D, F, and J)

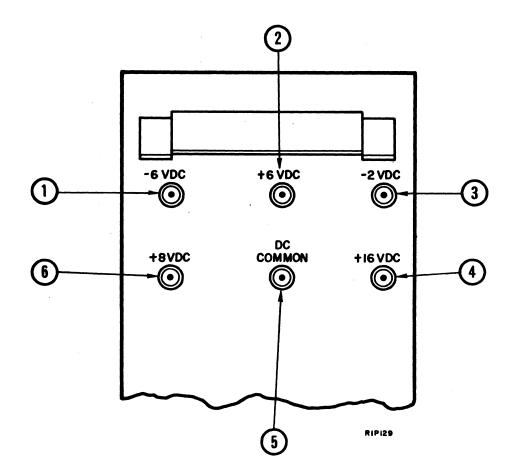


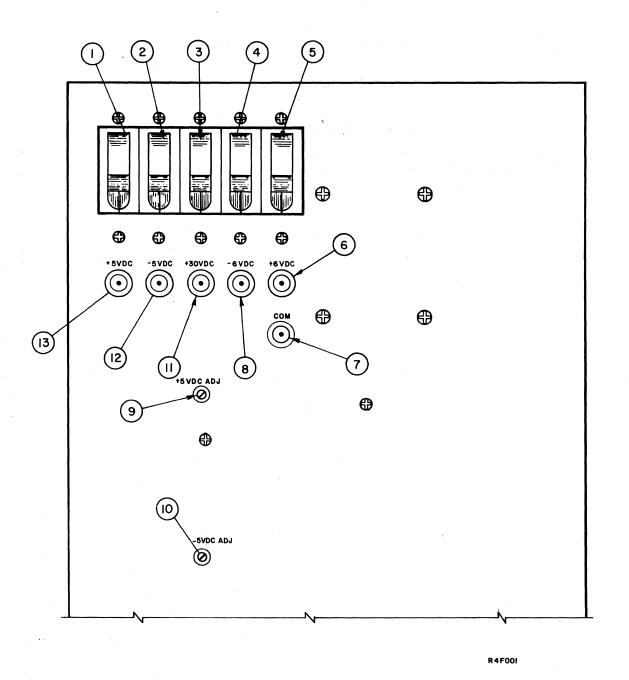
Figure 2-16. Buffer Controller Rectifier/Filter Test Points (CJ122 Models C, D, F, and J)

TABLE 2-10.	BUFFER CONTROLLER RECTIFIER/FILTER CONTROLS	
AND	TEST POINTS (CJ122 MODELS E, G, H, AND K)	

Figure 2-17 Index No.	Reference Designation	Controls	Function
1	CB01	+5 VDC circuit breaker	Switches +5 vdc output from T02 and rec- tifier/filter network to TB01.
2	CB02	-5 VDC circuit breaker	Switches ac power from T04 to -5 vdc recti- fier/filter network.
3	CB03	+30 VDC circuit breaker	Switches +30 vdc output from T03 and recti- fier/filter network to TB01.
4	CB04	-6 VDC circuit breaker	Switches -6 vdc output from T04 and recti- fier/filter network to TB01.

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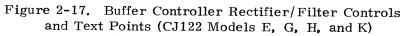


TABLE 2-10.BUFFER -CONTROLLER RECTIFIER/FILTER CONTROLSAND INDICATORS (CJ122 MODELS E, G, H, AND K) (CONT'D)

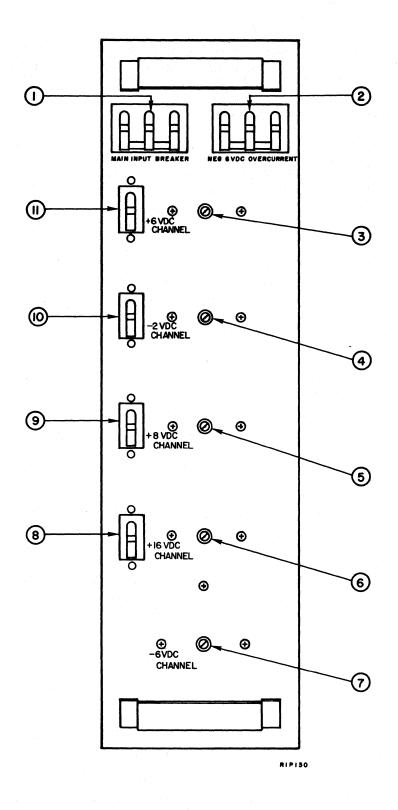
Figure 2-17 Index No.	Reference Designation	Controls	Function
5	CB05	+6 VDC circuit breaker	Switches +6 vdc output from T04 and recti- fier/filter network to TB01.
6	TP05	+6 VDC test point	Used with TP06 (dc common) to check posi- tive output of ±6 rectifier/filter network.
7	TP06	COM test point	Used as dc common reference point in con- junction with other test points when checking output voltages.
8	TP04	-6 VDC test point	Used with TP06 to check negative output of ± 6 vdc rectifier/filter network.
9	T01	+5 VDC ADJ variac	Adjusts +5 vdc output.
10	R3	-5 VDC ADJ potentiometer	Adjusts -5 vdc output.
11	TP03	+30 VDC test point	Used with TP06 to check output of +30 vdc rectifier/filter network.
12	TP02	-5 VDC test point	Used with TP06 to check output of -5 vdc rectifier/filter network.
13	TP01	+5 VDC test point	Used with TP06 to check output of +5 vdc rectifier/filter network.

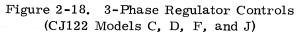
TABLE 2-11. 3-PHASE REGULATOR 50/60 HZ CONTROLS (CJ122 MODELS C, D, F, AND J)

Figure 2-18 Index No.	Reference Designation	Controls	Function
1	CB01	MAIN INPUT BREAKER circuit breaker	Switches input of ac power to 3-phase regulator 50/60 Hz system.
2	CB02	NEG 6 VDC OVER- CURRENT circuit breaker	Used to switch the 3-phase output power from the 3-phase regulator to the rectifier/ filter network.
3	T05	+6 VDC CHANNEL variac	Variac used to adjust the ac voltage output from T01 to +6 vdc rectifier/filter network in the buffer controller rectifier/filter system.

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TABLE 2-11. 3-PHASE REGULATOR 50/60 HZ CONTROLS (CJ122 MODELS C, D, F, AND J) (CONT'D)

Figure 2-18 Index No.	Reference Designation	Controls	Function
4	T06	-2 VDC CHANNEL variac	Variac used to adjust the ac voltage output from T02 to the -2 vdc rectifier/filter net- work in buffer controller rectifier/filter system.
5	T07	+8 VDC CHANNEL variac	Variac used to adjust the ac voltage output from T03 to the +8 vdc rectifier/filter system.
6	T08	+16 VDC CHAN- NEL variac	Variac used to adjust the ac voltage output from T03 to the +16 vdc rectifier/filter network in the buffer controller rectifier/ filter system.
7	T04	-6 VDC CHANNEL variac	Used to adjust the 3-phase power output from T1, T2, and T3.
8	CB06	+16 VDC CHANNEL circuit breaker	Used to switch the ac power output from T3 and T8 to the +16 vdc rectifier/filter network.
9	CB05	+8 VDC CHANNEL circuit breaker	Used to switch the ac power output from T3 and T7 to the +8 vdc rectifier/filter network.
10	CB04	-2 VDC CHANNEL circuit breaker	Used to switch the ac power output from T02 and T06 to the -3 vdc rectifier/filter.
11	CB03	+6 VDC CHANNEL circuit breaker	Used to switch the ac power output from T01 and T05 to the +6 vdc rectifier/filter network.

Vacuum Systems

The vacuum system is a low level, high volume vacuum system. The system's primary function is to provide vacuum to the document conveyor system for document hold-down and control. The vacuum also provides a means of cooling the transport drive motor. The controls are called out in table 2-12 and illustrated in figure 2-19.

TABLE 2-12. VACUUM SUPPI	LY ASSEMBLY	CONTROLS AND	INDICATORS
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Figure 2-19 Index No.	Reference Designation	Control or Indicator	Function
1			Indicates vacuum pressure in inches of water (8 inches nominal).

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TABLE 2-12.	VACUUM SUPPLY	ASSEMBLY	CONTROLS AND	INDICATORS (CONT'D)

Figure 2-19 Index No.	Reference Designation	Control or Indicator	Function
2		Vacuum relief adjust- ment screw	Adjusts high or low vacuum pressure by regulating air flow into chamber.
3		Low vacuum chamber pressure gauge	Indicates vacuum pressure in inches of water (1.5 - 2.0 inches).
4		Vacuum gate adjust- ment screw	Adjusts vacuum pressure ratio of two chambers by regulating opening between chambers.

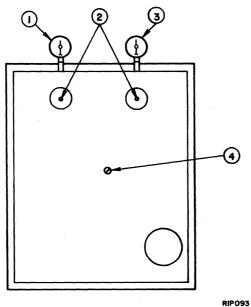


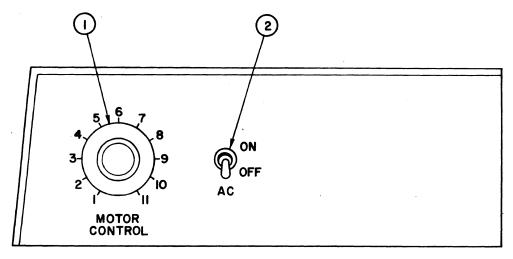
Figure 2-19. Vacuum Supply Assembly

Journal Tape Control Panel

The journal tape control panel is mounted above the journal tape option. (See figures 2-1 and 2-2.) The controls are called out in table 2-13 and illustrated in figure 2-20. Journal tape loading (option) is set forth in table 2-14.

Figure 2-20 Index No.	Reference Designation	Controls	Function
1	R01	MOTOR CONTROL potentiometer	Controls rpm of journal tape motor.
2	S01	AC toggle switch	Applies ac power to journal tape motor.

TABLE 2-13. JOURNAL TAPE CONTROL PANEL CONTROLS

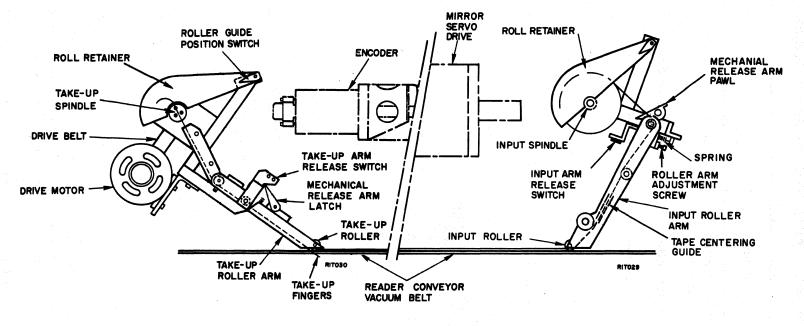


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Figure 2-20. Journal Tape Control Panel Controls

TABLE 2-14. JOUR	NALT.	APE (OP	PTION) L	OADING
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Step	Equipment	Procedure
1	Operator control	NOTE
	panel	If journal tape is under 3 inches wide, a leader at least 3 inches wide must be spliced to the tape before loading is attempted. Re- fer to table 6-21 for splicing instructions.
2	Journal Tape option	Refer to table 2-16 for power turn-on procedure. On journal tape assembly, lift and fasten read area cover. Push mechanical release arm pawl and arm latch to release both roller arms as shown in figure 2-21.
		Adjust spooler assembly roll retainer; lower take-up spindle.



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Step	Equipment	Procedure
2 (contd)		Place tape roll on input spindle and thread through tape center- ing guides to reader conveyor as shown in figure 2-21.
3	Operator control panel	Press JOURNAL TAPE pushbutton. JOURNAL TAPE indicator lights.
		Press LOAD pushbutton indicator.
		Tape moves to read area and stops.
		Press READY pushbutton indicator. READY lights.
4	Journal Tape option	Tape is picked off vacuum belt by take-up fingers and guided through take-up spindle. When tape is approximately 3 inches past take-up spindle, tape is automatically wound around spindle.
5	Take-up assembly	When tape has been read, lift roll retainer and remove roll of tape using slight counterclockwise twist.

TABLE 2-14. JOURNAL TAPE (OPTION) LOADING (CONT'D)

On-Line Character Correction Unit (OLCC) (Option)

The OLCC video display monitor and electronics are mounted on the system teletypewriter or sit on the System 17 desk. The controls are called out in table 2-15 and illustrated in figure 2-22.

TABLE 2-15. OLCC CONTROL PANEL CONTROLS AND INDICA	ATORS
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Figure 2-22 Index No.	Reference Designation	Control or Indicator	Function
1	CRT01	Display screen	Displays character images centered about rejected character.
2	R175	Vertical position con- trol knob	Adjusts vertical position of display (arrows next to knob indicate direction).
3	R375	Horizontal position control knob	Adjusts horizontal position of display (arrows next to knob indicate direction).
4	R562	INTENSITY control knob	Controls display brightness.
5	R595	FOCUS control knob	Controls display sharpness.
6	S800	POWER PULL-ON switch	Controls ac power to display monitor and OLCC electronics.

TABLE 2-15. OLCC CONTROL PANEL CONTROLS AND INDICATORS (CONT'D)

Figure 2-22 Index No.	Reference Design ati on	Control or Indicator	Function
7	DS01	POWER ON indica- tor	Indicates -5 vdc is available at OLCC power supply (PS02) output.
8	S01 DS03	ALARM PUSH-OFF pushbutton indicator	Indicator lights when Display Now signal is received from controller via reader.
			Pressing pushbutton resets audible alarm and ALARM indicator.

Power Turn-On Procedure

The power turn-on procedures are outlined in table 2-16. The reader should always be turned on in the sequence as outlined in this table.

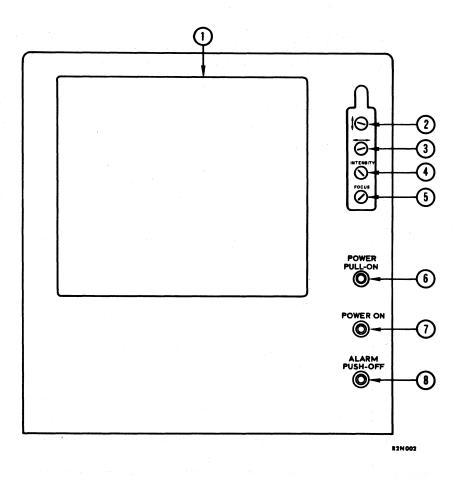


Figure 2-22. OLCC Control Panel, Controls and Indicators

Step	Equipment	Procedure
		NOTE
		If reader has been completely shut down refer to table 3-14.
1	Operator control panel	Press POWER ENABLE pushbutton indicator. Press CONTROLLER POWER pushbutton indicator. Press READER POWER pushbutton indicator.
		NOTE
		Reader will not come on unless buffer controller is turned on. Reader will not function unless controlware program is loaded in buffer controller. Program is not affected during normal shut- down of reader but must be reentered after reader is com- pletely shut down.

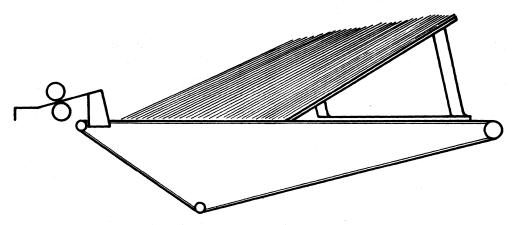
TABLE 2-16. POWER TURN-ON PROCEDURES

Reader Document Loading

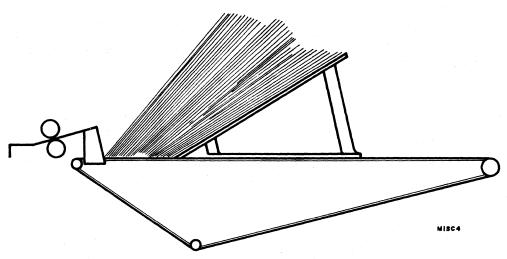
Documents may be passed through the system a maximum of four times without degradation of handling or character recognition error rates. Document jams will cause READY to drop. The proper document loading procedure is outlined in table 2-17 and illustrated in figure 2-23.

Step	Equipment	Procedure
1	Operator control panel	Ensure POWER ENABLE, READER POWER, and CONTROL- LER POWER indicators are lit. Refer to table 2-16 for power turn-on procedure.
2	Feed-up table (See figure 2-23.)	Disable feed-up. Pull wedge, as shown in figure 2-23, back far enough so that a shingled stack of documents will fit on the belt without hitting the stationary ramp on the feeder.
3	Feed-up table	Put sample document to be processed into feed-up table.
4	Document adjustment panel	Adjust guide walls to within 1/8 inch of document edge by manipulating PAPER GUIDE WIDTH ADJUST switch.
5	Sort pockets	Place sample document in both sort pockets and adjust back plate so that pocket length is approximately 1/2 inch longer than document.

TABLE 2-17. READER DOCUMENT LOADIN



- A. PROPER DOCUMENT LOADING :
 - 1. WEDGE PULLED SUFFICIENTLY BACK ON BELT.
 - 2. DOCUMENTS SHINGLED TO ANGLE OF WEDGE.



- B. IMPROPER DOCUMENT LOADING :
 - 1. WEDGE NOT PULLED BACK FAR ENOUGH.
 - 2. DOCUMENTS IMPROPERLY SHINGLED AND JAMMED TOGETHER.

Figure 2-23. Document Loading

Step	Equipment	Procedure
5 cont'd	· · · · · · · · · · · · · · · · · · ·	Adjust stacker width guides so that pocket width is approxi- mately 1/2 inch wider than document.
6	Feeder assembly	Place sample documents on feed-up table.
		Press ENABLE FEED UP pushbutton.
7	Document adjustment panel	Repeatedly press LOAD switch to advance documents from feed-up table while turning DOCUMENT THICKNESS ADJUST knob counterclockwise (thicker documents) until double docu- ment feed occurs.
		Then turn DOCUMENT THICKNESS ADJUST knob clockwise (thinner documents) until double document feed no longer occurs.
		Turn DOCUMENT THICKNESS ADJUST knob an additional two complete clockwise turns to obtain proper gap setting between the feed and dedoubler rollers.
		NOTE
		If double document feed or misfeed condition reoccurs, check that doc- uments are properly loaded on feed- up table.
8	Document adjustment	NOTE
	panel	Doubles check is not done unless firmware loaded in transport module.
		Turn DOUBLES ADJUST knob in counterclockwise direction until DOUBLES INDICATOR on document adjustment panel lights.
		Insert one document in doubles detect area.
		Turn DOUBLES ADJUST knob clockwise until DOUBLES INDICATOR goes out.
		Insert second document.
		Verify that DOUBLES CHECK and DOUBLES INDICATOR lamps light.
9	Feed-up table	Edge document stack.

TABLE 2-17. READER DOCUMENT LOADING (CONT'D)

1

Step	Equipment	Procedure
9 cont'd		Width and length of stack should be as close as possible to that of a single document before attempting to place stack on feed-up table.
		Place stack of documents, face up, on feed-up table so they rest on wedge, as shown in figure 2-23.
		If they fit too tightly between width guides, remove stack and edge it again.
		Shingle documents toward feeder so angle of all documents in stack is equal to or less than angle of wedge.
10	Operator control panel	Press ENABLE FEED UP pushbutton.
	parror	Belt and wedge carries stack of documents toward feeder.
		CAUTION
		Do NOT attempt to speed feed-in process by pushing wedge forward. Do NOT lift or touch pre-feed roller for any reason.
		When the wedge stops press the LOAD pushbutton to advance documents from feed-up table to read station.
		Press READY pushbutton indicator.
		READY lights.
		Documents are ready to be processed.
11	Feed-up table	To load more documents of the same size, wait until feed-up table is clear of all documents, then repeat procedure from step 9.
		CAUTION
		Extreme caution should be taken when loading more documents while previous load is still being fed in.
		To load more documents of the same size but different thickness, repeat procedure from step 6.
12	Take-away area	After reading, document sorted to either sort pocket.

TABLE 2-17. READER DOCUMENT LOADING (CONT'D)

Step	Equipment	Procedure
13	Operator control panel	When a sort pocket is full, SORT POCKET FULL indicator lights. Reader stops.
		Remove documents from sort pocket.
		SORT POCKET FULL indicator goes out when the READY or LOAD switch is pressed.
		NOTE
		Documents may be removed from sort pocket during operation.
		Repeat procedure from step 10.

TABLE 2-17. READER DOCUMENT LOADING (CONT'D)

Power Turn-Off Procedure

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Prior to power turn-off, assure that all documents are removed from reader. Proper procedure for turning off the reader is outlined in table 2-18.

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Step	Equipment	Procedure
	NORMAL SHUTDOWN	
1	Operator control panel	CAUTION
		In an emergency, press POWER ENABLE pushbutton indicator on operator control panel to turn off ac and dc power to reader and buffer controller. POWER ENABLE goes out.
		Press READER POWER pushbutton indicator.
		READER POWER indicator lamps go out.
	COMPLETE SHUTDOWN	
2	High-voltage power supply panel	Set AC POWER switch to OFF.
3	Power control unit	Set all circuit breakers to OFF.
4	Controller power supplies	Set all circuit breakers to OFF.
5	Power input unit	Set circuit breaker to OFF.

TABLE 2-18. POWER TURN-OFF PROCEDURES

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SECTION 3

INSTALLATION AND CHECKOUT

Crating and uncrating instructions, site preparation requirements, reader installation procedures, and reader checkout procedures are contained in this section.

C RA TING

The following paragraphs describe the procedures to be used for the internal blocking and packaging and external packaging of the reader and buffer controller. Observance of the procedures and use of the recommended materials will ensure adequate protection of the reader in transit.

SCOPE

These procedures have been prepared by the Traffic Section, Materials Department of the OCR Operations, Control Data Corporation. They must be followed to ensure safe movement and delivery of equipment under normal conditions of handling and transit.

Packaging instructions provide for:

- Internal blocking and packaging of equipment prior to shipment.
- External packaging for transportation by air-ride van.
- External packaging and crating for transportation by air freight.

INTERNAL BLOCKING AND PACKAGING

The procedures listed in tables 3-1 and 3-2 apply to either surface or air shipment of the reader only. Tables 3-3 and 3-4 list the packaging procedures for the buffer controller.

TABLE 3-1. READER INTERNAL BLOCKING AND PACKAGING PROCEDURES

Step	Procedure
1	Remove all covers and panels.
2.	Vacuum interior and horizontal exterior surfaces of reader.
3	Wipe all exposed surfaces of reader with 409 Cleaner or comparable household cleaner.
4	At left front of reader, remove journal tape cover (if Journal Tape option installed on reader) and pack cover separately.
5	Remove document wedge from feedup table and pack in separate carton.
6	Pack feedup table in separate carton.
	Mark carton: FRAGILE and DO NOT TOP LOAD.

Step	Procedure
7	Pad feed rollers.
8	Tape document hold-down covers of edger assembly to edger surface.
9	Tape all pushbuttons on the operator control and maintenance panels.
10	Tape cable harness at right front of reader frame.
11	Check that power supply modules are tight.
12	If lightpipes are shipped as spares, place lightpipes in plastic tube and tape tube to top of conveyor.
13	Remove leveling bolts from the reader and BC, place the bolts in a jiffy bag, and tape them to the frame.
14	Unbolt reader from BC.
15	Open logic doors and place loose cable connectors in jiffy bags.
	Tape bags to floor of reader.
	Check area around logic doors for loose screws, nuts, etc.
16	Close logic doors and block bottom of door No. 1 with two 3/4-inch plywood blocks wrapped in dunnage.
	Tape logic door latch to catch with filament tape.
17	Cover face of logic door No. 1 completely with foam (or acceptable equivalent) and tape sheet of cardboard over foam.
18	Open recognition door and check area for loose screws, nuts, etc.
	Close door and connect shipping bracket to frame and door.
19	Tape all logic cards in place on recognition door and cover with foam (or accept- able equivalent). Tape sheet of cardboard over foam.
20	Replace all covers and panels.
	Tape covers and panels to reader with filament tape.

TABLE 3-1. READER INTERNAL BLOCKING AND PACKAGING PROCEDURES (CONT'D)

TABLE 3-2. READER EXTERNAL PACKAGING PROCEDURES

Step	Procedure
1	Check that all skins are in place and are secure.
2	Install dust cover over reader.
3	Install corrugated sleeve over reader.
4	Install corrugated cap and band with plastic banding. Label front of carton: FRONT THIS SIDE TO VAN WALL.
5	Place power cable over top of reader from left side and tape to corrugated cap.
	NOTE
	Secure power cable to carton by placing banding over cable.
	Band cap with plastic strap.
	Band sleeve in center with plastic strap.

TABLE 3-3. BUFFER CONTROLLER INTERNAL BLOCKING AND PACKAGING PROCEDURES

Step	Procedure
1	Remove all panels from buffer controller.
2	Vacuum interior of buffer controller carefully.
3	Wipe all exposed surfaces of buffer controller with 409 Cleaner or comparable household cleaner.
4	Open swingframe at rear of buffer controller and carefully tape wiring harnesses to eliminate movement.
5	Remove terminators, place in jiffy bags and identify.
	Tape bag to floor of buffer controller (terminators are PC boards on S/N 151 and up).
6	Tape leveling bolts (inside buffer controller cabinet) to buffer controller frame.
7	Secure swingframe by taping latch to catch with filament tape.
8	Remove all 50-pack logic cards and wrap each card separately.
	Pack cards in separate carton and mark: FRAGILE and DO NOT TOP LOAD. (25-pack on CJ122 Models E, G, H, and K).
9	Replace all panels.
	Tape panels to buffer controller with filament tape.

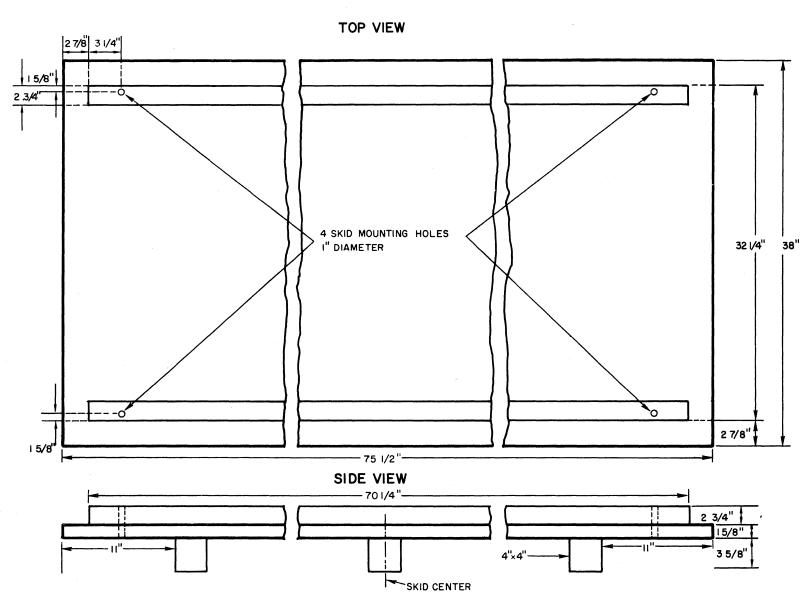
TABLE 3-4. BUFFER CONTROLLER EXTERNAL PACKAGING PROCEDURES

Step	Procedure
1	Cover buffer controller with dust cover.
2	Install corrugated sleeve and cap.
	Band cap with plastic strap.
	Band sleeve in center with plastic strap.

SKID MOUNTING

The procedure listed in tables 3-5 and 3-6 apply only when the reader and buffer controller are to be shipped by air or rigging is required.

Stop	Procedure
Step	
1	Perform steps 1 through 12 in table 3-1.
	Perform steps 14 through 19 in table 3-1.
2	Position skid, shown in figure 3-1 (Dwg No. 59105708), in front of reader.
3	Raise reader with a Rol-a-Lift to a height of $9-1/2$ inches.
	WARNING
	Reader must be securely strapped to Rol-a-Lift to prevent accidental injury to personnel or damage to equipment.
	Remove leveling pads and bolts.
4	Screw four $1/2-13 \ge 9$ inch mounting bolts into leveling pad mooring of reader until bottom of bolt is above the bottom of the caster.
5	Slide skid under reader.
	Lower reader to within 3 inches of skid top.
	Align skid mounting bolt holes with skid mounting bolts installed in reader.
	Unscrew skid mounting bolts until they are through skid mounting holes and can be felt on the underside of the skid.
6	Lower reader to skid.
	Fasten reader to skid using 1-inch flat washer, $1/2$ -inch lockwasher, and $1/2$ -13 nut on each skid mounting bolt. Tighten securely.
7	Unstrap reader from Rol-a-Lift.
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Figure 3-1. Reader Skid

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TABLE 3-6. BUFFER CONTROLLER SKID MOUNTING PROCEDURES

Step	Procedure
1	Perform steps 1 through 5 in table 3-3.
	Perform steps 7 through 9 in table 3-3.
2	Position skid, shown in figure 3-2 (Dwg No. 59105709), in front of buffer controller.
3	Perform steps 3 through 7 in table 3-5 for the buffer controller.

UNCRATING

Uncrating procedures for the reader and buffer controller are listed in tables 3-7 and 3-8.

Step	Procedure
1	If reader is skid-mounted, raise reader at both ends with Rol-a-Lifts and remove four bolts that secure skid.
2	Cut metal or nylon strapping using care to avoid whipping action of metal strapping.
- 3	Remove tape from power cable.
4	Remove corrugated top and sleeve.
	Remove dust cover.
5	Carefully remove tape from covers and panels.
	Remove tape residue, if any.
	Remove all covers and panels.
6	Remove cardboard and foam from recognition door.
	Carefully remove tape from logic cards.
	Remove shipping bracket from door and frame.
7	Remove cardboard and foam from logic door No. 1.
	Remove tape from latch.
	Remove plywood blocks from bottom of logic door.
	Remove cable connectors from jiffy bags and install.
8	Remove tube of spare lightpipes (if shipped with reader) from conveyor.
9	Remove tape from cable harness, pushbuttons on operator control and maintenance panels, and document hold-down covers of edger assembly.
10	Remove padding from feed rollers.
	(Table continued after figure 3-2.)

TABLE 3-7.READER UNCRATING PROCEDURES

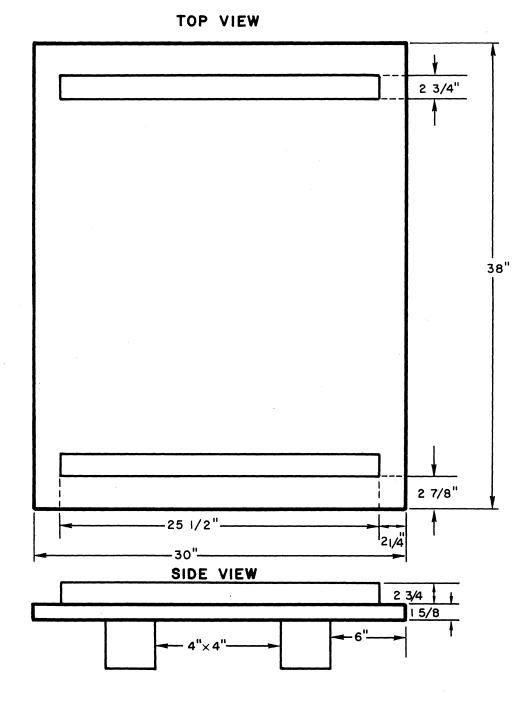


Figure 3-2. Buffer Controller Skid

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TABLE 3-7. READER UNCRATING PROCEDURES (CONT'D)

Step	Procedure
11	Remove journal tape cover (if option installed on reader) from carton and install.
12	Remove tape from leveling bolts if reader not skid mounted and install leveling bolts on reader.
13	Refer to mounting and leveling procedures listed in table 3-9.

TABLE 3-8. BUFFER CONTROLLER UNCRATING PROCEDURES

Step	Procedure	
1	If buffer controller is skid mounted, raise the buffer controller with a Rol-a-Lift and remove four bolts that secure skid.	
2	Cut metal or plastic strapping using care to avoid whipping action of metal straps.	
3	Remove corrugated sleeve and cap.	
4	Remove dust cover.	
5	Carefully remove tape from panels.	
	Remove tape residue, if any.	
	Remove all panels.	
6	Remove tape from logic rack latch.	
	CAUTION	
	Install cards carefully as back panel pins are easily bent or broken.	
	Unpack 50-pack logic cards and install in buffer controller (25-pack on CJ122 Models E, G, H, and K).	
8	Remove tape from leveling bolts (if not skid mounted) and install leveling bolts in buffer controller.	
9	Remove terminators from jiffy bag and install.	
10	Carefully remove tape from wiring harnesses on logic door.	

PREPARATION OF LOCATION

Power, environmental, and access space requirements must be met before the reader is installed.

POWER REQUIREMENTS

The reader operates on 177-222 vac, 3-phase, ± 10 percent. Reader current requirements are as follows:

Operating	11.3 amperes per phase (CJ122 Models C, D, F, and J); 10.6 amperes/phase (CJ122 Models E, G, H, and K)
Start-up	200 amperes per phase, single cycle
Standby	2 amperes, single phase

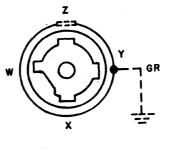
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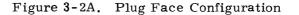
Input power wiring will provide a 3-phase circuit breaker at 30 amperes per phase.

A 30-ampere, 3-phase, 5-wire male plug (Control Data Part No. 15005700) on a 10-foot power cable is supplied with the reader. This plug requires a female receptacle on a drop cord (Control Data Part No. 15005900). Rubber boots (Control Data Part No. 94929400) may be placed on the connectors for added protection.

Phasing is to be wired as follows (see figure 3-2A):

Pin X	Pha se A	Black
Pin Y	Phase \mathbf{B}	Red
Pin Z	Phase C	Blue (Orange)
Pin W	Neutral	White
Case	Ground	Green





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ENVIRONMENTAL REQUIREMENTS

The reader operates in an ambient temperature of from 60° to 80° F. The maximum rate of temperature change (thermal shock) without affecting reader operation is 20° F per hour. The operating relative humidity range is from 30 percent to 60 percent.

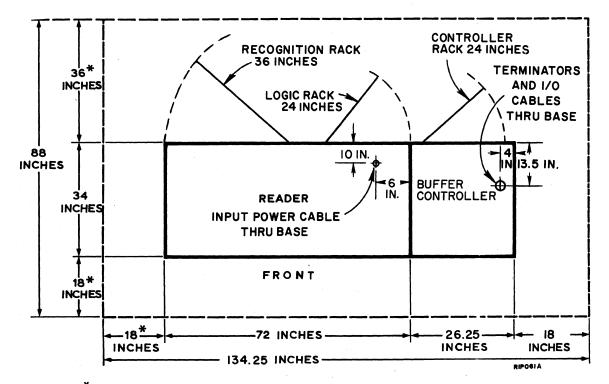
An environment with excessive dust, such as a keypunch area, will cause failures and require increased maintenance.

ACCESS SPACE REQUIREMENTS

The minimum amount of floor space required for the reader is an area 88 inches by 134.25 inches. Floor space dimensions and access space needed to operate, service, and maintain the reader are shown in figure 3-3. The floor loading is 115 pounds per square foot (average).

INSTALLATION

Position the reader in accordance with user site plans and refer to Access Space Requirements paragraph. Mounting and leveling procedures for the reader and buffer controller are listed in table 3-9.



NOTE: * INDICATES MINIMUM CLEAR MAINTENANCE AREA REQUIRED

Figure 3-3. Floor Space Requirements

Step	Procedure
1	Remove all panels and covers.
2	NOTE
	The buffer controller and reader frames are to be butted together with no spacers between frame members.
	Place buffer controller next to reader and bolt buffer controller frame to reader frame.
	Before tightening nuts, check that no cables or power wires are between frame members.
	Check that frames are aligned.
3	Level reader and controller vertically and horizontally.
	Tighten nuts on leveling bolts.
4	CAUTION
	Front nylon belt guides of feedup table may be damaged when positioning table between stationary ramp and feed roller.
	Unpack feedup table and position it on buffer controller frame.
	Ensure that feedup table is parallel to edger with approximately $1/8$ to $1/4$ inch between table and edger.
	Ensure that feedup table deck is 0.060 to 0.090 inch higher than edger surface and is level.
	Insert screws (2 each pad) into leveling pads and tighten.
5	Place side guide drive chain over sprockets on front of feedup table and adjust tension with chain idler sprocket.
6	Unpack wedge and attach to feedup belt on feedup table.

TABLE 3-9. READER AND BUFFER CONTROLLER MOUNTING AND LEVELING PROCEDURES

Main power enters the reader through the power control unit (A13) and is then cabled throughout the reader and buffer controller as shown in the power cabling diagram in figures 3-4, 3-5, and 3-6. A general system installation procedure is listed in table 3-10 and a system input/ output cabling diagram is shown in figure 3-7. Reader module locations (i. e., A01, A02, A03, etc.) are shown in figures 3-8 and 3-9 and called out in table 3-11. The procedures for connecting the power and input/output cabling of the reader and buffer controller are listed in table 3-12.

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Step	Procedure
1	Uncrate all equipment and inspect for any damage resulting from shipping.
	CAUTION
	Ensure that front console of computer is properly mounted (SC 1774 only). The two signal cards which remained with the panel during shipment must be returned to the proper location or wiring damage will occur. Card No. 526567 goes in location B36 and Card No. 526568 goes in location B35.
2	Position equipment to user site plans.
3	CAUTION
	Do not connect any power, input/ output, or terminator lines to reader until remainder of system has been checked out.
	Check all site power leads to ensure proper voltage.
4	Connect ground straps from each unit in the system to grid ground.
5	Connect terminator power (from terminator power supply) to each peripheral unit in the system, including the computer. (The terminator power supply input is supplied by the computer.)
6	Connect signal cable from teletypewriter to low-speed channel of computer (J24).
	Connect remaining input/output cables from computer to all peripheral units.
	Ensure that all unused input/output lines are terminated.
7	Connect all interrupt lines.
14	Wire or plug in all units, except reader.
8	Energize all units except reader.
9	Check all power supplies for proper voltages and adjust as required.
10	Run several passes of memory, command, and protect tests on computer.
11	Run SMM17 on all peripheral units included with system.
12	Perform procedures listed in table 3-12 when all units, except reader, are run- ning satisfactorily.

TABLE 3-10. GENERAL SYSTEM INSTALLATION

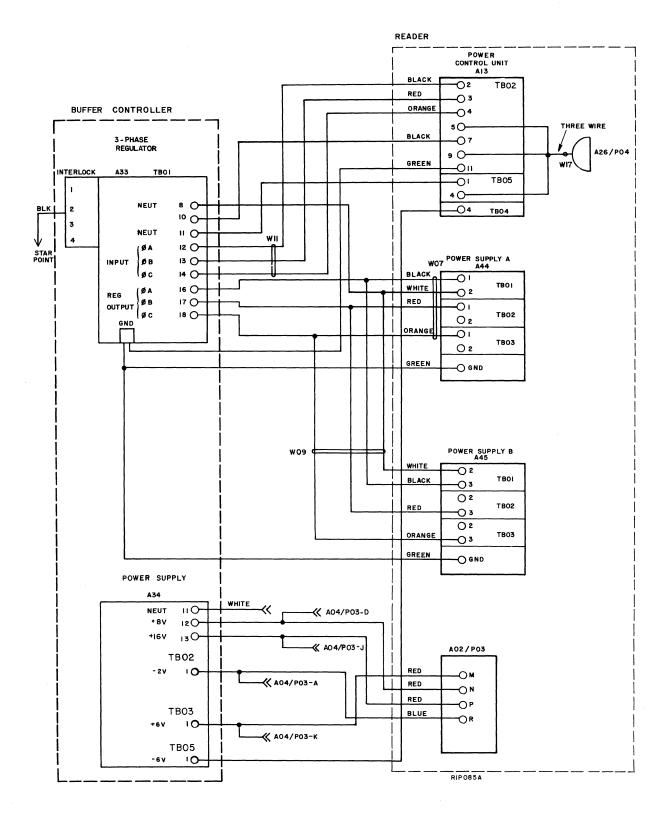


Figure 3-4. Power Cabling Diagram, CJ122, Model C

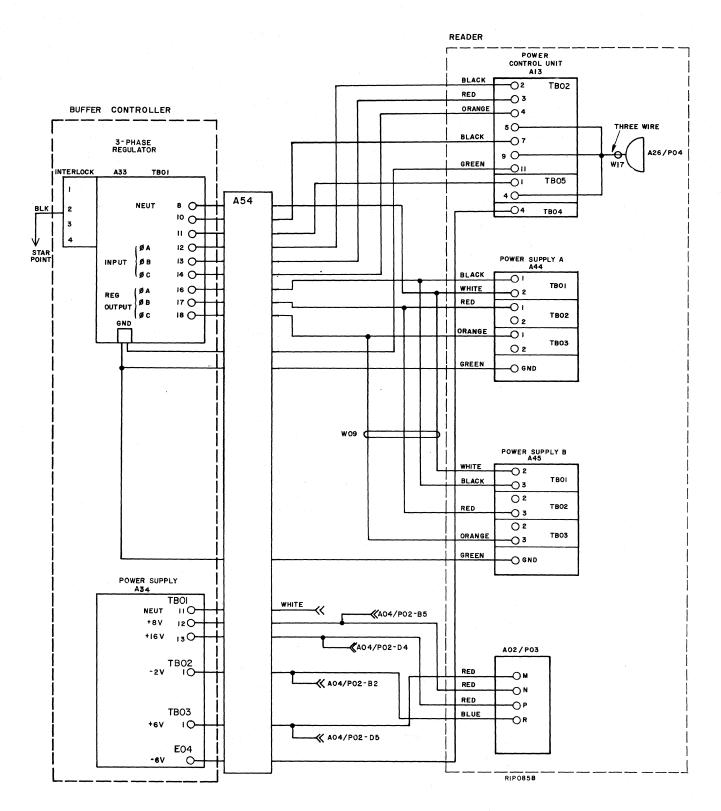


Figure 3-5. Power Cabling Diagram, CJ122, Models D, F, and J

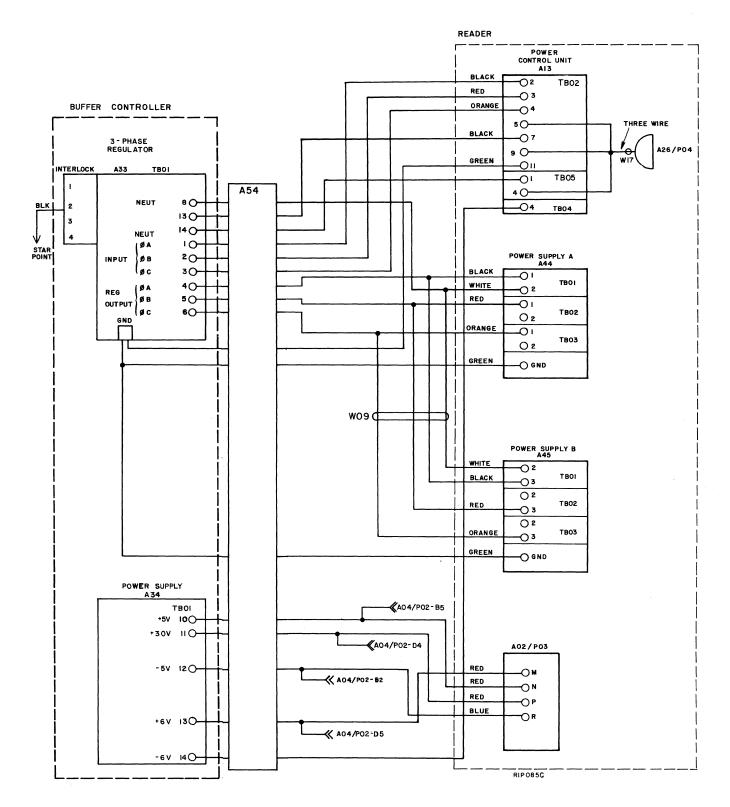
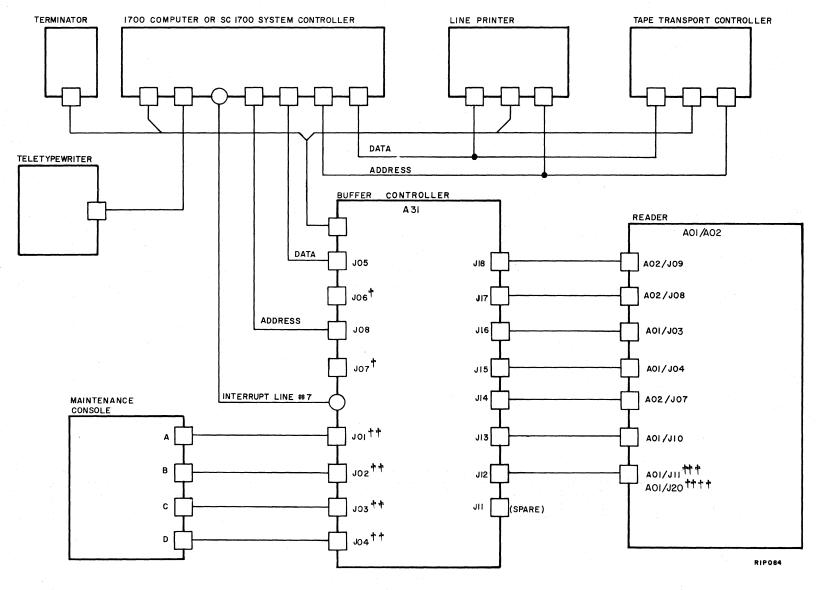


Figure 3-6. Power Cabling Diagram, CJ122, Models E, G, H, and K

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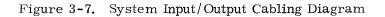
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* MUST BE TERMINATED WHEN SYSTEM IS CABLED UP

tt have special terminators when controller maintenance panel is not used on frioi/fv454. ttt cji22 models coi/co2

十十中中 CJI22 MODELS D,E,F,G,H,J, and K



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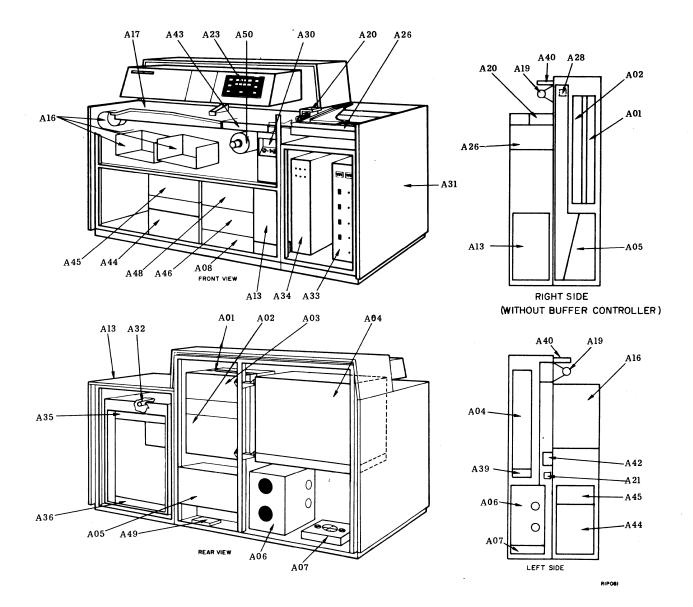


Figure 3-8. Reader Module Locations (CJ122, Models C, D, F, and J)

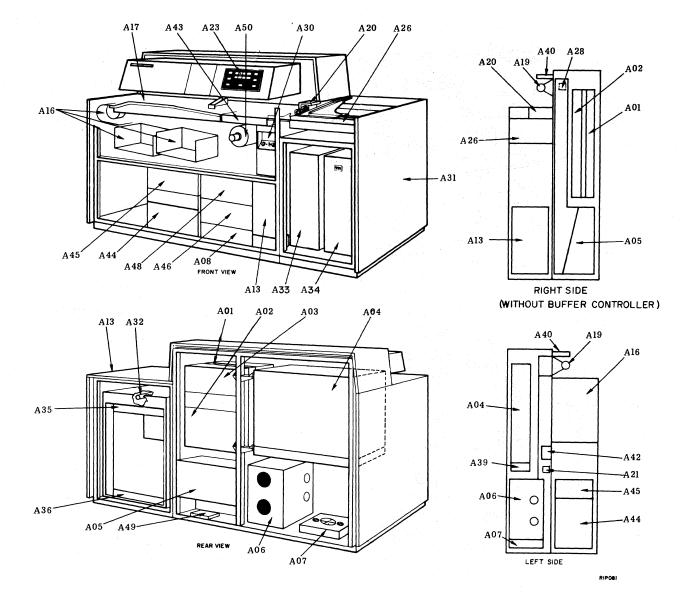


Figure 3-9. Reader Module Locations (CJ122, Models E, G, H, and K)

Module	Title	Module	Title
A01	Logic door No. 2	A 31	Controller
A02	Logic door No. 1	A32	Controller temperature sensor
A03	Maintenance panel	A 3 3	Controller regulator
A04	Recognition rack	A34	Controller power supply
A05	Photomultiplier box	A 35	Controller upper fans
A06	Conveyor vacuum supply	A36	Controller lower fans
A07	Main frame fans	A 3 9	Recognition rack fans
A08	High-voltage power supply	A 40	Read lamp fans
A13	Power control unit	A42	Take-away phase shift assembly
A16	Stacker	A43	Edger assembly
A17	Conveyor assembly	A44	"A" supply
A19	Mirror drive assembly	A 45	"B" supply
A 20	Feeder assembly	A46	Transport servo supply
A21	Vacuum pressure pump	A 48	Mirror/Transport drive elec-
A23	Operator control panel		tronics
A26	Feedup table	A49	DC common star point
A 28	Lightpipe shutter	A 50	Transport motor and plate
A30	Operator adjustment panel		assembly

TABLE 3-11. READER MODULES

GROUNDING THE READER SYSTEM

The intent of the following information is to acquaint the installation personnel and customer engineers concerned with the installation of the reader systems with the various techniques and options open to them for proper installation and maintenance of grounding systems. Most of the information presented here has been excerpted from Engineering Standard 1. 30. 023, Digital Computer System Grounding.

In order to build a common vocabulary, the following terms and definitions will be established.

Ground	A conducting connection, whether intentional or accidental, between an electrical circuit or equipment and earth, or to a conductor which serves in place of the earth (U.S. National Electrical Code Definition).
Logic Ground, DC Ground	The metallic portion or portions of an equipment containing digital circuitry that functions as the zero voltage reference. The circuit ground of the logic and any metallic framework electrically connected thereto. Associated with the EDP system digital circuits, this ground circuit takes the form of many paths from each circuit to the ground circuit. Unlike the analog circuit, the ground circuit uses as many paths to the ground circuit as feasible.

Frame Ground, Equipment Ground

Green Wire Ground, Green/Yellow Wire Ground, Safety Ground

Grid Ground

Multi-Point Ground (MPG)

Star Point Ground, Single-Point Ground (SPG)

Earth Electrode

The metallic framework of a cabinet or equipment enclosure. Always connected to safety ground through green or green/ yellow wire. In addition to safety ground, the frame shall be grounded to the grid, where available.

Connection from frame ground to earth electrode. Supplied by the green wire ground in power cables. Provides protection for circuits (and people) which could be exposed to high voltages in case of a phase shorting to frame, lightning strikes, and other electrical system failures or catastrophes.

A system grounding scheme consisting of a multitude of very low impedance circuit loops in metallic contact with one another, forming an effective ground plane at all frequencies of electromagnetic interference. Designed for digital computer systems.

A system ground plane that has different pieces of equipment terminated at various locations on the ground plane. Normally, a grid ground.

A system grounding scheme employing a branching technique for the avoidance of ground loops. Generally consists of large gauge wires radiating from a single point (star ground), each radial forming the ground conductor from an individual equipment. While effective for low frequencies, <u>generally</u> not suitable for reduction of high frequency interference. Recommended for analog computer systems using low level signal.

Metallic element (i. e., rods, pipes, plates) driven into, or buried in, the earth to provide a return for safety ground. Required at power service entry.

System Ground Reference Plane

Either a multi-point ground, or a single point ground.

Grounding is used for two purposes in installations of the reader system. The first and most important is for the safety of the personnel working with and around the reader system. For this reason, the green wire ground system is always left intact and connected. The second reason is to minimize the results of electromagnetic interference (EMI).

All logic grounds are connected to the system ground reference. Specific components of a complete computer ground system include a system ground reference, equipment EMI bonding, equipment safety conductors, system safety conductors, earth electrodes, and ground system interfaces. The system ground reference plane to be used on all Control Data computer installations is to be a grid ground system. In the case of an exemption, small systems shall be grounded to an acceptable non-grid ground.

The three acceptable ground systems are, in order of preference, the raised floor structure, the wire mesh grid, and the shielded logic cable non-grid. Although not recommended, a

fourth grounding system is available for use with unshielded logic cables in a non-grid environment.

The raised floor structure ground is made up of the supporting aluminum or steel structural members of the false floor, bonded at each crossing by welding, bolting, or electrical bond straps. The grid should be continuous under the entire system and extending 3 feet beyond the periphery of the system, with each square section of the grid being a nominal 2 feet by 2 feet.

Where the raised floor is not suitable for grounding, that is, wooden or an older poor conducting metal structure, a wire mesh grid is to be used. The wire mesh grid is made up of copper or aluminum wire, AWG 2 or larger, with the same system periphery and section requirements as the raised floor grid. The mesh is made of continuous wire lengths laid in squares and bonded at the junctions by welding or split-bolt clamps. Solder alone is NOT ACCEPTABLE for bondings, and the grid conductors shall be free of kinks, loops, and coils.

The shielded logic cable ground system offers considerable improvement over previous nongrid ground systems. Interconnection of the I/O lines between the central processor and the peripherals makes up the ground reference plane. If shielded logic cables are not available for system interconnection, then the least preferred ground system is used. This involves interconnecting the CPU and peripherals with flat, flexible, braided strap. Braided strap, as used in this context, specifically refers to Control Data Part No. 24534811, and is approximately 1-inch braid made up of 850 AWG 36 tinned copper wires. The braided strap is attached to the grounding terminal block or plate of each piece of equipment, and the connecting of one piece of equipment is permissible and recommended, with the object of minimizing the ground impedance.

The 955, or any other OCR device made by Control Data, is a hybrid machine; it is both analog (low level) and digital in operation. For this reason, the gounding for the system is multi-point in some areas and single-point in others. Eventually, all grounds find their way to the "star plate" mounted on (but electrically isolated from) the floor of the machine, under the photomultiplier box. (See item A49, figures 3-8, 3-9, and 3-10.) The star plate, then, is the central logic ground point of the reader transport, the buffer controller, the reader logic racks, and all of the power supply common busses or points. The frame ground (i.e., structural members, equipment chassis, skins and cabinet floor) is kept totally isolated from the star point, except for one short, heavy, braided strap connecting the floor and the star point. After disconnecting the shorting braid strap, greater than 10 megohms impedance should exist between frame and logic grounds. The safety ground is tied hard to the frame ground at the voltage entry box, and all internal safety grounds (fans, power supply inputs, etc.) are tied to frame ground as close as possible to the device. One other peculiarity of the reader system internal grounds is that, although the logic racks and power supply frames of the reader itself are frame ground, the buffer controller chassis and controller power supply chassis are held at logic ground. It is important that the BC and associated parts only go to frame ground through the star plate. Now, the reader system can be connected to ground. (See table 3-12 for proper sequence.) If the system is being installed on a grid ground plane, remove the braided strap connecting the frame ground and the star plate of the reader and drop separate short braided straps to the grid from both the frame ground and the star plate. Short means a maximum of 2 feet. If static electricity is a problem, tying all four corners (frame ground) of the machine will help.

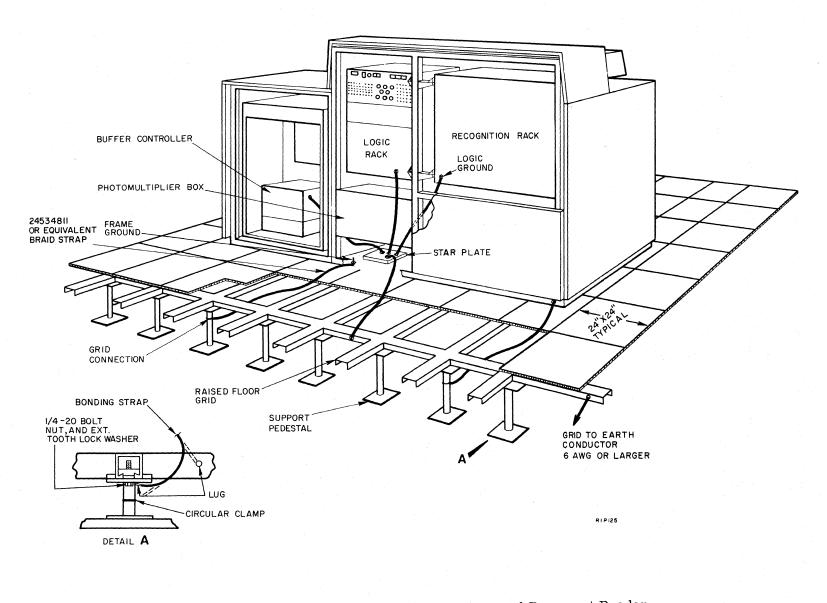


Figure 3-10. Star Grounding System, OCR Page and Document Reader

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If the reader is being installed in a non-grid environment, leave the frame ground/star point shorting strap in place and interconnect with shielded I/O cables. Check to be sure that the I/O connector plate goes to logic ground and not frame ground. And finally, if shielded I/O cables are not available, then interconnect the equipment with braided straps (Control Data Part No. 24534811) kept as short as possible and tied to the star point or its equivalent with multiconnections recommended.

The basic idea is that if the system is on a grid, all components of the system should have the frame ground/logic ground shorting straps removed and separate drops to the ground plane; if a non-grid ground is used, the shorting strap is left on and single point grounding is used by tying the system components together at their prime logic ground, be it star plate, white terminal block, or whatever.

Check the grid. Be sure of its connection to the earth electrode and earth ground. Test the junction bondings for good, tight connections, good welds, hold-down clamps torqued to a minimum of 20 foot/pounds; make sure that the junctions are free of insulation, grease, dirt, and anything capable of inhibiting conduction. Check and recheck. The initial time spent on the grounding system can save untold hours and the anguish of chasing noise problems.

TABLE 3-12.	POWER AND INPUT/OUTPUT CABLING PROCEDURES	
F	OR READER AND BUFFER CONTROLLER	

Step	Procedure
1	Connect ground wires from buffer controller swingframe to star point ground (A49, figure 3-6).
2	Connect -6 vdc power lead from reader to -6 vdc buss on back of buffer controller power supply.
3	Connect ac power wires from A13 to A33, TB01, pins 11 to 14 (CJ122 Model C); connect the corresponding plugs and jacks at A54 (CJ122 Models D, E, F, G, H, J, and K).
4	NOTE
	Buffer controller power supplies and swingframe are isolated from frame ground. Only ground leads going to star point (logic ground) should be con- nected to these units.
	Connect all green ground leads to frame ground.
5	Connect feedup table, doubles sensor, and drive cables (A30 /J01, A30/J02, A20/J02, A26/J01, A26/J03, and A26/J04).
6	Insert cable connectors A31/P12 through A31/P18 into respective jacks in buffer controller.

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TABLE 3-12.POWER AND INPUT/OUTPUT CABLING PROCEDURESFOR READER AND BUFFER CONTROLLER (CONT'D)

Step	Procedure	
7	Connect grounds as follows:	
	 a. Attach ground strap from buffer controller frame to reader frame. b. Attach four ground (logic) straps from buffer controller swingframe to reader star point ground. c. Perform steps in table 3-13. d. Attach ground strap from reader frame ground to grid. e. Attach ground strap from reader star point ground to grid. 	
8	Mount terminator power supply, shown in figure 3-7, near system and connect terminator power to buffer controller.	
9	Connect data and address cables from computer to buffer controller as shown in figure 3-7.	
10	Connect maintenance console to buffer controller as shown in figure 3-7.	
11	Connect interrupt line from computer to buffer controller and connect terminators J06 and J07 as shown in figure 3-7.	
12	Ensure that all internal signal cabling of the reader is secure (i.e., between logic rack and recognition rack).	
13	Ensure that all PC boards and IC elements are seated properly.	
14	Plug ac line of maintenance console into standard 110 vac line.	
15	Plug dc line of maintenance console into jack provided near J04 on buffer controller (CJ122 Models C, D, F, and J)	
	NOTE	
	Ensure that maintenance console is com- patible with local power frequency and with BC. For CJ122 Models E, G, H, and K, remove BC panel face and replace DTL logic cards with TTL logic cards as follows:	
	Location DTL TTL	
	A20AAF0AMFA39AWF0ALFA49AWF0ALF	
	Do not attempt to connect dc power jack of a TTL-converted maintenance console to any power source.	

GROUND AND SAFETY CHECK

A ground and safety check procedure is listed in table 3-13 and should be performed after any rework or repair. It must be performed completely when the reader is first installed and at periodic intervals thereafter.

INITIAL POWER CHECK

An initial power check procedure is listed in table 3-14 and should be performed at initial installation of reader. Step 5 should be observed at each power-up of the reader.

INTERLOCK TEST

An interlock test procedure is listed in table 3-15 and should be performed when a reader is first installed and does not operate properly. It should be used after initial installation only for troubleshooting purposes.

Step	Procedure			
1	Check continuity of earth ground from power plug (W27) to reader frame.			
2	Check continuity of each phase from plug to power control. Check for isolation of 10 megohms or greater, phase to phase, phase to neutral, and phase to ground. All circuit breakers should be off.			
3	Check for isolation of dc common to frame ground, measuring from star plate to frame at back of power control unit. Isolation must be 20 megohms or greater.			
4	Check continuity from ground (dc common) to star plate from recognition rack, logic door 1, logic door 2, maintenance panel, operator panel, BC, PM box terminal board and from each dc power supply.			
	NOTE			
	Recheck dc common to frame ground isolation after rework or repair.			
5	Check continuity from output of all supplies to all distribution points. Use Drawing No. 48950000, sheets 3B, 3C, 3H, and 3J (Pub. No. 48430081) or Drawing No. 48950100, sheets 3-4 and 3-5 (Pub. No. 48948100). Check for isolation, bus-to-bus and bus-to-ground, and verify that the +5V interlock line is isolated from the +5V logic line.			
	NOTE			
	Recheck after any rework or repair.			

TABLE 3-13. GROUND AND SAFETY CHECK PROCEDURES

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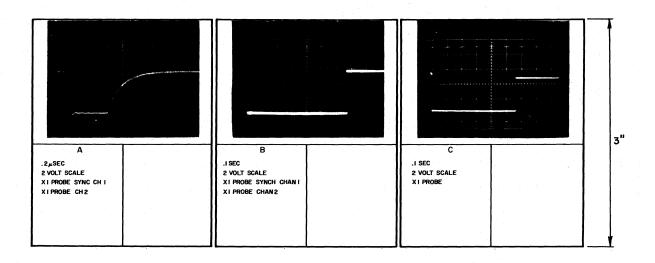
Step Procedure 1 With all circuit breakers set to OFF, connect power cable (W27) to power source. 2 Set MAIN, POWER UP, and FANS circuit breaker to ON. 3 Place the MAINTENANCE/NORMAL switch to MAINTENANCE and all BYPASS switches to BYPASS. 4 Press POWER ENABLE switches at the operators panel and the maintenance panel. 5 Press CONTROLLER POWER at maintenance panel. 6 Verify ac input to BC regulator. 7 Press READER POWER at maintenance panel and verify the following items for proper operation (set the appropriate circuit breakers to ON at the power control unit): Take-away motor a. b. Read lamp c. Vacuum motors d. Width motor e. Feedup motor 8 Set SYSTEM REGULATOR circuit breaker to ON at the power control panel and verify regulated ac output at the following points: a. CJ122 Models C, D, F, and J - A33, TB01 pins 16, 17, and 18. b. CJ122 Models E, G, H, and K - A33, TB01 pins 4, 5, and 6. Set dc circuit breakers to ON at A33 (CJ122 Models C, D, F, and J) or A34 (CJ122 Models E, G, H, and K). Verify dc output at test points on A33 or A34. 9 Set circuit breakers on A supply to ON. Verify dc outputs at A supply and B supply. Outputs should be 10-20 percent above nominal values. 10 Verify dc voltages, according to schematics, at the following locations: a. Logic rack d. Feedup solenoid driver b. Recognition rack e. Sort gate solenoid driver c. Maintenance panel f. PM box Set HIGH VOLTAGE and TRANSPORT SERVO SUPPLY circuit breakers on power 11 control unit to ON. Verify that high voltage supply output is 1650 volts and that transport servo supply output is ±45 volts.

TABLE 3-14. INITIAL POWER CHECK PROCEDURES

TABLE 3-15. INTERLOCK TEST PROCEDUR	TABLE 3-15.	. INTERLOCK	TEST	PROCEDURE
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Cton	Procedure		
Step			
1	Set the following circuit breakers at power control unit to ON: MAIN CIRCUIT BREAKER, FANS, POWER UP, and +6 VDC.		
2	At maintenance panel, set all BYPASS switches to BYPASS; set MAINTENANCE/ NORMAL switch to MAINTENANCE.		
3	Press POWER ENABLE switches on maintenance and operator panels.		
4	Alternately press and release CONTROLLER POWER switch on maintenance panel.		
5	With oscilloscope, verify a toggle with each press of the CONTROLLER POWER switch at the following locations:		
	5B27 pin 5 5C29 pin 5		
6	Set MAINTENANCE/NORMAL switch to NORMAL.		
7	Alternately press and release CONTROLLER POWER switch on operator's panel and repeat step 5.		
8	At operator's panel, alternately press and release READER POWER switch.		
9	With oscilloscope, verify a toggle with each press of the READER POWER switch at the following locations:		
	5B25 pin 5 5C30 pin 5		
10	Set MAINTENANCE/NORMAL switch to MAINTENANCE.		
11	At maintenance panel, alternately press and release READER POWER switch and repeat step 9.		
12	At A supply, set +5 VDC circuit breaker to ON.		
13	Connect oscilloscope CHAN 1 probe to 5B27 pin 6 and CHAN 2 probe to 5B24 pin 3.		
14	Observe waveform on CHAN1 (see figure 3-11A) while rapidly pressing and releasing CONTROLLER POWER switch on maintenance panel; CHAN 2 should show the inverse of this waveform.		
15	Move oscilloscope CHAN 2 probe to each of the following locations, observing the waveform (see figure 3-11B), rapidly pressing the CONTROLLER POWER switch on maintenance panel. Pulse duration should be 650 ms.		
	Board 5A20 pin 8Board 5D20 pin 9Board 5A29 pin 10Board 5D24 pin 5Board 5C29 pin 1Board 5E24 pin 10		
16	Disconnect oscilloscope CHAN 1 and CHAN 2 probe.		
17	Connect oscilloscope probe to boards 5C27 pin 6 and 5A28 pin 3, while rapidly pressing CONTROLLER POWER switch, verify they change state from "0" to "1" when power goes off or "1" to "0" when power goes on.		

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Figure 3-11. Interlock Test Procedure Waveforms

TABLE 3-15.	INTERLOCK	TEST	PROCEDURE	(CONT'D)
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Step	Procedure			
18	Verify CONTROLLER POWER indicator lamps go ON or OFF with each press of the switch. Leave in the ON position.			
19	Connect oscilloscope CHAN 1 probe to board 5B25 pin 6 and CHAN 2 probe to board 5B25 pin 1.			
20	Synchronize positive on CHAN 1 and observe waveform (see figure 3-11A) on CHAN 2 while rapidly pressing READER POWER switch on the maintenance panel; CHAN 1 should show the inverse of this waveform.			
21	Move CHAN 2 probe to board 5D20 pin 12 and repeat step 20.			
22	Disconnect oscilloscope probes.			
23	Ground 6C18 pin 13.			
24	Connect oscilloscope to the following boards and observe the waveform (see figure 3-10B). Negative pulse should last for 650 ms.			
	Board 5C30 pin 1Board 5C27 pin 10Board 5B24 pins 10 and 5Board 6C28 pin 12Board 5D27 pin 1Board 5D20 pin 6Board 5E23 pin 8Board 5A20 pin 8Board 6C11 pin 2Board 5A29 pin 4Board 6B12 pin 12 [†] Board 6B30 pin 13Board 3E14 pin 11 ^{††}			
	22 Models C and D only 22 Models D, E, F, G, H, J, and K			

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Step	Procedure			
25	Connect oscilloscope to boards 6C29 pin 3 and 6E19 pin 10 [†] . Verify both are at logic 1 levels.			
26	Connect oscilloscope to boards 5C27 pin 8 and 5A28 pin 4, verifying that they change state with every press of READER POWER switch and that the READER POWER indicator lamps go ON and OFF.			
		N	OTE	
		On all signals che to its destination.		
27	Set READER POWER switch at ON.			
28	Remove ground fr	rom board 6C18 pin 13	, installed in step 23.	
	Failure Latches	(sheet 14 of logic diagr	ams)	
29	Ground boards 51	319 pins 9 and 12 and 5	A20 pin 1.	
30	With oscilloscope set at AUTO TRIGGERING, probe the following locations and verify logic level as indicated:			ng locations and
	Location	Logic Level	Location	Logic Level
	5A20 pin 3	0	5C20 pin 11	1
	5C20 pin 6	1	pin 8	0
	pin 3	0	5E23 pin 8	1
	5C21 pin 11 pin 8	1 0	5S02 pin 6 1/6 pin 64/3	1 0
	5C22 pin 11	1	5S02 pin 4/11	1
	pin 8	0	pin 7/8	0
	5C22 pin 6 pin 3	1 0	5D28 pin 8 pin 6	1 0
1	5C21 pin 6	1	5C28 pin 8	1
	pin 3	0	pin 6	0
31	Connect oscilloscope to board 5E23 pin 8 and press FAULT RESET switch on maintenance panel. Verify that oscilloscope reading changes from a logic 1 to 0 when switch is pressed and from logic 0 to 1 when released.			
32	Momentarily ground the input to each R-S flip-flop (see sheet 14 of logic diagrams). This will set each flip-flop. Check that all the logic levels in step 30 (except 5E23 pin 8) are inverted.			
33	Press FAULT RI	ESET switch and repea	t step 30.	
34	Heat each of the following temperature sensors to 125° F and then check its corre- sponding indicator on maintenance panel. Location: At top of recognition rack (S01); at top of BC logic rack (S01).			
†C.112	22 Models C and D o	on]v		
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TABLE 3-15. INTERLOCK TEST PROCEDURE (CONT'D)

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TABLE 3-15. INTERLOCK TEST PROCEDURE (CONT'D)

Step	Procedure			
35	Remove grounds connected in step 29.			
36	Check voltage sensing network (sheets 20 and 20A logic diagrams). Check for $+5$ vdc at $5S02/42$ pin $25/14$ and $5S02/42$ pin $26/13$.			
	Controller Failure Gate (sheet 12 of logic diagrams)			
1	NOTE			
	If no recognition rack is installed, ground board 5A26 pin 12.			
37	Set all controller BYPASS switches to OFF, and ground 5D27 pin 6.			
38	Connect oscilloscope to board 5D20 pin 6 and verify a logic 1. Leave oscilloscope connected for further observations.			
39	Move ground from 5D27 pin 6 to 5D27 pin 4.			
40	Check oscilloscope and verify a logic 0.			
41	Move ground to 5C20 pin 1.			
42	Check oscilloscope and verify a logic 0.			
43	Remove ground installed in step 41. Check oscilloscope and verify a logic 1.			
44	Consecutively set each circuit breaker on the BC 3-phase regulator (CJ122 Models C, D, F, and J) or rectifier-filter (CJ122 Models E, G, H, and K), to OFF while verifying on oscilloscope that 5D20 pin 6 goes to a logic 0 when the breaker is set to OFF and a logic 1 when circuit breaker is set to ON.			
45	Verify that each time a circuit breaker is set to OFF in step 44 that VOLT CHECK indicator lamp on maintenance panel lights.			
46	Disconnect oscilloscope connected in step 38.			
	High Voltage Interlock (sheet 12 of logic diagrams)			
47	Set high voltage power supply switch to OFF.			
48	With oscilloscope, check board 5B26 pin 3 and verify a ground, also that HIGH VOLT indicator lamp on maintenance panel is lit.			
49	Set high voltage power supply switch at ON.			
50	Press FAULT RESET switch on maintenance panel.			
51	With oscilloscope check board 5B26 pin 3 and verify that reading goes from ground to -4.5 volts, also that the HIGH VOLT indicator lamp is out.			
	Reader Failure Gate (sheet 13 of logic diagrams)			
52	Set all READER INTERLOCK STATUS BYPASS switches at OFF, except FAULT and MIRROR FAULT switches.			

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Step	Procedure
53	Connect oscilloscope to 5B20 pin 8 and verify a logic 1.
54	Ground the following points separately and verify that board 5B20 pin 8 switches each time to a logic 0; then remove ground and verify that pin 8 switches back to logic 1.
	Board 5C22 pin 1 Board 5C20 pin 9 Board 5S02 pin 58/1
55	Connect oscilloscope to board 5B20 pin 8 and set VACUUM circuit breaker at Powe Control Unit to OFF; on maintenance panel, set CIRCUIT BREAKER-BYPASS/AC switch to BYPASS, verifying that 5B20 pin 8 switches to logic 1.
56	Set CIRCUIT BREAKER-BYPASS/AC switch to AC and verify that 5B20 pin 8 switches to logic 0 and STATUS indicator lamp goes out.
57	Set 6 VDC circuit breaker on Power Control Unit to OFF; set CIRCUIT BREAKER- BYPASS/DC switch to BYPASS, verify that board 5B20 pin 8 switches to logic 1.
58	Set Circuit Breaker-BYPASS/DC switch to DC, verify that pin 8 switches to logic 0
	500 Hz Fan Out
59	Check the following locations for presence of the 500 cycle/second signal:
	4S05-42/1 [†] 6B22-03 5A22-11 6A25-8 6C25-1 ^{††} 6B29-11
	Continuous Reply Logic (sheet 15 of logic diagrams)
60	Connect oscilloscope to the following boards consecutively; on POWER CONTROL UNIT set POWER UP circuit breaker to ON, then OFF, and verify that proper wave form is displayed (see figure 3-11C).
	5D27-5 5E21-1 5B22-5 5E24-12
	NOTE
	Ground board 5E22 piń 11 if there is no coupler installed.
61	On maintenance panel press CONTROLLER POWER and READER POWER switches to ON.

TABLE 3-15. INTERLOCK TEST PROCEDURE (CONT'D)

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	TABLE 3-15. INTERLOCK TEST PROCEDURE (CONT'D)		
Step	Procedure		
62	With oscilloscope, verify that board 5D22 pin 5 is a logic 0, and boards 5D29 pin 3 and 5D30 pin 9 are not toggling.		
63	Ground boards 5D27 pins 3 and 6, then 5D24 pin 12, and verify that the logic counter is counting. Each stage should be running at half the frequency of the previous stage.		
64	With oscilloscope, verify that board 5D22 pin 5 is a logic 1.		
65	Remove all grounds installed in step 63.		
66	Run the following program into BC MAINTENANCE CONSOLE and connect oscillo- scope to board 5D29 pin 4 and see that the counter gets reset when the Controller Running Reply signal comes over from the BC. Controller Running Reply signal will occur for 2 μ sec every 100 msec.		
	Models C, D, F, and J Models E, G, H, and K		
	P = 0000 X = 0A30 680A P = 0000 X = 0A30		
	0000 CF03 A809 0B30 B800 8809		
	A809 0000 C802		
	8809 3000 0B30		
	4009 A80A		
	880A		
	C806 B800		
	0000		
	0000		
	Ready Gate (sheet 18 of logic diagrams)		
67	On maintenance panel press READY switch.		
68	Connect oscilloscope to the following locations and verify they are a logic 1 and		
	MIRROR CHECK and XPORT CHECK indicator lamps on operator's control panel go out:		
	Board 5E27 pin 8 Board 5E27 pin 3 Board 5E28 pin 12		
69	Ground board 6D18 pin 8 and verify that READER READY indicator lamp goes out and MIRROR CHECK indicator lamp lights.		
70	Remove ground installed in step 69 and press READY switch, verify READER READY indicator lamp lights, and MIRROR CHECK indicator lamp goes out.		
71	Ground board 6B29 pin 8 and verify that READER READY indicator lamp goes out and XPORT CHECK indicator lamp is lit.		
72	Remove ground installed in step 71 and press READY switch. Verify READER READY indicator lamp lights and XPORT CHECK indicator lamp goes out.		

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TABLE 3-15. INTERLOCK TEST PROCEDURE (CONT'D)

Step	Procedure
	Operator's Control Panel Switches (sheet 16 of logic diagrams)
73	Connect oscilloscope to board 5E29 pin 2 and repeatedly press STOP switch. Verify that it is logic 1 with switch in and logic 0 with switch out.
74	Connect oscilloscope to board $5E29$ pin 4 and repeatedly press LOAD switch. Verify that a positive-going 450 μ sec pulse occurs when the switch is pressed.
75	Connect oscilloscope to board 5E29 pin 6 and repeatedly press READY-SYSTEM/ READER switch. Verify that it is logic 1 with switch in and logic 0 with switch out.
76	Connect oscilloscope to board 5E29 pin 8 and repeatedly press END OF FILE switch. Verify that it is logic 1 with switch in and logic 0 with switch out.
77	Connect oscilloscope to board 5B20 pin 2 and repeatedly press PARAMETER ENTRY switch. Verify that it is a logic 1 with switch in and logic 0 with switch out.
78	Ground board 5A20 pin 13, and repeatedly press ENABLE FEED UP switch. Verify that the following points are a logic 1 with switch in and logic 0 with switch out: 5E19 pin 9, 6B25 pin 6. Verify that the following points are logic 0 with switch in and logic 1 with switch out: 5E19 pin 8, 6S04 pin $66/1$.
79	Remove ground installed in step 78 and set all switches and circuit breakers at OFF.

MAINTENANCE PANEL TEST PROCEDURE

A maintenance panel test procedure is listed in table 3-16 and should be performed when a reader is first installed and does not operate properly. It should be used after initial installation only for troubleshooting purposes.

TABLE 3-16. MAINTENANCE PANEL TEST PROCEDURE

Step	Procedure
1	Connect maintenance console and set to ON.
2	On power control unit set all circuit breakers to ON.
3	On maintenance panel set all BYPASS switches up, MAINTENANCE/NORMAL switch to MAINTENANCE, and POWER ENABLE switch to OFF.
4	Verify that INTRLK BYPASS indicator lamps light.
5	Press CONTROLLER POWER switch; unit should not turn on.
6	Press READER POWER switch; unit should not turn on.
7	Press POWER ENABLE switch to ON; verify that indicator lamps light.
8	Press CONTROLLER POWER switch to ON; verify that indicator lamps light and BC turns on.
9	Press READER POWER switch to ON. Verify that the following conditions exist:

TABLE 3-16. MAINTENANCE PANEL TEST PROCEDURE (CONT'D)

Step

Procedure

9

- cont'd
- READER READY indicator lamps light.

Reader turns on.

- CONTROLLER POWER indicator lamps are lit.
- READER POWER indicator lamps light.
- POWER ENABLE indicator lamps are lit.

10 Using the digital voltmeter, measure the following power supply voltages (red and blue test points): (See table 1-7 for characteristics.)

NOTE

Not all test points are used on the maintenance panel. Therefore, voltages to be measured will be called out using row designations and terminal positioning from left to right, refer to figure 2-6 or 2-7.

Row	Terminal	Row	Terminal
MFPS	2 = +15V	BCPS (CJ122	1 = +16V
	3 = +10V	Models C, D,	2 = +8
	4 = +5.5V	F, and J)	3 = +6
	6 = -15V		6 = -2V
RLPS/RSRPS	1 = +20V	BCPS (CJ122	1 = +30V
	2 = +12V	Models E, G,	2 = +5V
	4 = +5V	H, and K)	3 = +6V
	8 = -20V		6 = -5V
			7 = -6V
		TDPS	1 = +45V
			7 = -45V

All other red and blue test points should read 0V.

NOTE

If maintenance console hangs in constant RNI mode, momentarily ground TP-AM on B00 in BC (CJ122 Models C, D, F, and J) or press EOP-CC switch (Models E, G, H, and K).

11 On BC maintenance console enter instructions 0A20 and run.

- 12 Verify the following conditions:
 - XPORT CHECK indicator lamp is lit.
 - READER REA DY indicator lamps go out.
- 13 Master clear BC console.
- 14 On maintenance panel press READY switch and verify READER READY indicator lamps light.
- 15 Press FAULT RESET switch and verify XPORT CHECK indicator lamp goes out.

Step	Procedure
16	On maintenance console enter instructions 0A21 and run.
17	Verify VOLT CHECK indicator lamp is lit.
1.	NOTE
	If coupler boards are installed in
	BC, READY FAULT indicator lamp will light.
18	Using the oscilloscope, verify the following:
	 Main clock TP is running at oscillator frequency. Column generator TP has a 5V P-P sawtooth waveform. Phase generator TP is running. Shift TP is running.
19	Enter the following in BC maintenance console:
	0A32 0B32 0A33 0B33 B800
	MASTER CLEAR and RUN.
20	Verify GEN SYNC #1 and GEN SYNC #2 test points are set and clear.
21	Verify that each time a document covers and uncovers the read zone sensor the counter increases by one count.
22	Ground board 6D20 pin 5; verify MIRROR CHECK indicator lamp lights and READER READY lamp goes out.
23	Remove ground installed in step 22.
24	Ground 6E22 pin 3; verify MIRROR FAULT indicator lamp light.
25	Monitor 2C12 pin 1; verify that by switching SIM/OPTICAL switch it changes state from logic 0 when set to SIM and a logic 1 when set to OPTICAL.
26	Monitor 4D29 pin 1; verify that when switching IMAGE REG CONTROL-INPUT / OUTPUT switch from OUTPUT to INPUT the output at pin 1 changes from logic 0 to logic 1.
27	Monitor 5C12 pin 13; verify that when switching READ TIMING-CONT/NORMAL switch from NORMAL to CONTR the output at pin 13 changes from a logic 1 to a logic 0 .
28	Using the 500 Hz signal as a reference, jumper 5A22 pin 11 (CJ122 Model C01 or 5B17 pin 5 (CJ122 Model C02, D, E, F, G, H, J, and K) to each of the following and verify 500 Hz at the respective test points.

TABLE 3-16. MAINTENANCE PANEL TEST PROCEDURE (CONT'D)

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Step	Procedure		
28	Test Point	Indication	
cont'd	5E12 pin 11 5C14 pin 11 5C14 pin 13 5E12 pin 09	Character peak Black-to-white transition White-to-black transition Read	
29	Remove jumper wire used in step 28.		
30	Enter a 0A3F instruction in maintenanc lights.	e console and verify READY indicator lamp	
	NC	ТЕ	
	On units with han installed SPARE is HANDPRINT c	circuit breaker	
31	If handprint option is not installed, on POWER CONTROL unit set SPARE circuit breaker to OFF; verify the AC FAULT indicator lamp lights.		
	NC	DTE	
	A wiring error exists on the power control unit such that the spare circuit breaker is in the dc interlock circuit on many systems.		
32	With SPARE circuit breaker set to OFF, set CIRCUIT BREAKER - BYPASS/AC to SC and verify system power is off and cannot be turned on.		
33	Set CIRCUIT BREAKER - BYPASS/AC can be turned on.	switch to BYPASS and verify system power	
34	Set MAINTENANCE/NORMAL switch to NORMAL and verify system power is off and cannot be turned on.		
	NO	DTE	
	The fault bypass 31 - 34 should ho faults.		
35	When PMP successfully completed retu	nn to nonmal opportion	

TABLE 3-16. MAINTENANCE PANEL TEST PROCEDURE (CONT'D)

CHECKOUT

The procedures in table 3-17 will completely check out the reader and ensure that the reader is functioning properly.

Step	Procedure				
1	Set AC switch on maintenance console to ON.				
2	Plug in reader.				
	Set MAINTENANCE/NORMAL switch on maintenance panel to MAINTENANCE.				
	Set BYPASS switches to up position (bypass fault).				
3	Set all circuit breakers on reader and buffer controller to OFF.				
4	Set MAIN circuit breaker on power control unit of reader to ON.				
5	Check for 5.5 vdc at 5A20-14.				
6	Set all circuit breakers on reader and buffer controller to ON.				
7	Press POWER ENABLE pushbutton on maintenance panel and operator control panel.				
8	Press CONTROLLER POWER pushbutton on maintenance panel.				
9	Check buffer controller voltages at test points on power supply with digital voltmeter Adjust as required.				
10	Load and run BC-2 and BC-3 from magnetic tape. (Refer to PMP 1.9, section 6.)				
	NOTE				
	Refer to step 19 for maintenance console switch settings except for SEL STOP which will be on.				
11	Replace all panels and covers on reader except rear vertical and rear upper panels.				
12	Press READER POWER pushbutton indicator on maintenance panel.				
13	Check all reader power supplies to ensure that proper voltages are present ($\pm 10\%$) and adjust as required. (Refer to PMP 4.1 or 4.2, section 6.)				
14	Press FAULT RESET pushbutton on maintenance panel. All indicators should go out except INTRLK BYPASS, COMM FAULT, MIRROR CHECK, and XPORT CHECK.				
	NOTE				
	All CHECK indicators should be out during document processing.				
15	Set MAINTENANCE/NORMAL switch to NORMAL.				
	Set all BYPASS switches to off (down position).				
	Ensure that reader and buffer controller remain energized.				

TABLE 3-17. READER CHECKOUT PROCEDURES

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TABLE 3-17	BEADEB	CHECKOUT	PROCEDURES	(CONTID)
17707070 - 110	TURADER	CHECKOUT	THOCHDOILED	(CONT D)

Step	Procedure			
15	NOTE			
cont'd		If either the reader troller, or both, b refer to CJ122 logi sheets 10 through 2 48430081 or Pub. 1	ecome deenergized, .c rack diagrams, 20 (Pub. No.	
16	Press READER F deenergize.	OWER pushbutton on op	erator control panel. Re	ader should
	Wait approximate	ly 10 seconds.		
	Press CONTROL		on operator control pane	1. Buffer control-
17	Press CONTROL		on operator control pane	1. Buffer control-
	Press READER POWER pushbutton on operator control panel. Reader should ener- gize. If reader does not energize, check the FAULT indicators on the maintenance panels.			
		NO'	$\Gamma \mathrm{E}$	
		When reader is in both reader and bu can be energized o the operator contro POWER ENABLE s tenance panel is se reader is in MAIN' the reader and buff only be energized f nance panel but can from both the oper maintenance panels	ffer controller r deenergized at ol panel only if switch on main- ot at ON. When FENANCE mode, fer controller can from the mainte- n be deenergized ator control and	
18		G CONTROL switch on switch to OUTPUT.	the maintenance panel to	SIM and the
	Set READ TIMINO	G switch to NORMAL.		
19	Check maintenand	e console for proper sv	vitch settings:	
	Switch	Position	Switch	Position
	SEL STOP TEST MODE TM CONTROL	OFF OFF NOT RUNNING	MODE CONTROL PARITY ERROR All others	CONT. OFF NORM
	Set key switch to	MAINTENANCE mode.		

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Step	Procedure			
19 cont'd	Set control switch to LAMP TEST to ensure that all indicators are operating. (Refer to Buffer Controller Maintenance Manual, Pub. No. 58032700.)			
20	Mount SMM17 tape on unit 0 and image tape on unit 1.			
	Load RX-3 and execute according to procedures in Module Test, Diagnostics, section 6.			
	 a. Run module 1: electronic read and verify for all character sets in reader b. Run module 2: page and document handling (see table 2-17) c. Run module 3: operator panel d. Run module 4: mirror test e. Run module 5: handprint electronic read and verify (if handprint option installed) 			
21	Set IMAGE REG CONTROL switch to OPTICAL.			
22	Perform RX-1 (test 30) according to PMP 1.7, section 6.			
	NOTE			
	Use standard test documents cut to maximum length of 12 inches. During RX-1 checkout, use varied parameters as outlined in test to ensure proper operation, i.e., ADV, LCT, EOL, and RSC.			
23	Check all options installed in reader with RX-1 after completing basic system check- out using RX-1.			
24	Replace rear vertical and rear upper panels.			
	Run user controlware.			

TABLE 3-17. READER CHECKOUT PROCEDURES (CONT'D)

2

SECTION 4

THEORY OF OPERATION

The mechanical and electronic operation of the reader is described in this section. A discussion of the reader is followed by a discussion of each system in the reader.

The reader converts printed, typed, or handprinted data into digital information for computer processing. The reader:

advances a document from the feedup table to the read area,

scans a line of text,

recognizes the characters on that line,

advances the document to succeeding lines until the entire document is read, and transports the document from the read area and sorts it into one of two sort pockets.

The reader systems which accomplish these functions are shown in figure 4-1 and are as follows:

Document transport system Optics system Character recognition system Supporting systems

The document transport system moves each document from the feedup table to the read area where the lines are scanned. The document is then sorted into one of two sort pockets.

The scanning system scans lines of characters on the document as it is advanced through the read area. Scanned characters are recognized by the character recognition system, which then outputs corresponding digital information to the buffer controller (BC). The BC also functions as an integral part of the reader timing and control logic.

The supporting systems are the vacuum, cooling, power distribution, and maintenance systems.

DOCUMENT TRANSPORT SYSTEM

After the power turn-on and document loading procedures have been completed, document flow is initiated by pressing the ENABLE FEED UP pushbutton on the operator control panel. The feedup clutch is engaged, the ENABLE FEED UP indicator lights, and the documents are moved to the feeder via a wedge on a feedup belt shown in figure 4-2.

The stack of documents is pushed to the top of a stationary ramp, raising the pre-feed roller which in turn moves a metal flag from between a photosensor and light source, stopping the feedup belt. When the LOAD pushbutton is pressed, the conveyor servo drive motor starts.

The pre-feed roller picks the first document off the stack and pulls the document towards the feed and dedoubler rollers. The feed roller pulls the document over the dedoubler roller and feeds the document onto the edger. If two or more documents are picked off the stack by the pre-feed roller, the bottom document(s) is pushed back by the dedoubler roller until the top document has been fed.

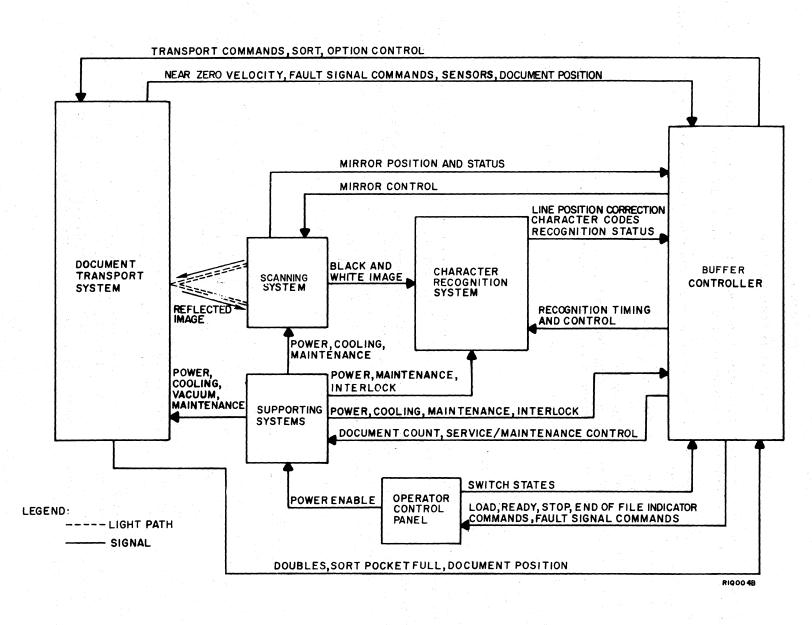


Figure 4-1. Reader Systems

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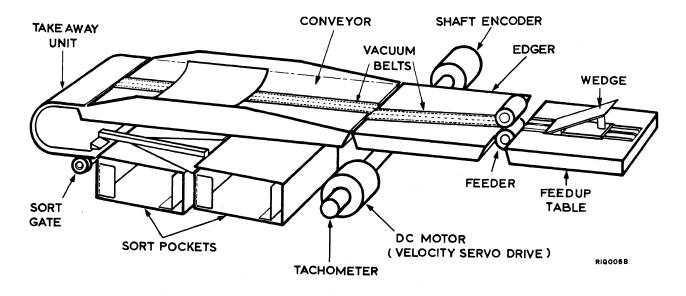


Figure 4-2. Document Transport System

The document is squared and centered with the conveyor vacuum belt by the edger. The edger vacuum belt, which is angled slightly to the left, takes hold of the document as it leaves the feeder and pulls the document towards an edging wall. Vacuum pressure on the belt allows for some document movement so that the document aligns itself as it is moved along the edging wall. A linear speed variation of approximately 7 percent between the edger and feeder causes a gap, proportional to document length, between documents.

In the document load mode the conveyor vacuum belt, moving at the same linear speed as the edger vacuum belt, transports the document to the read area at a speed of 40 inches per second. When the leading edge of the document passes the read zone photosensor (located approximately 1 inch upstream from the read station), the transport servo is commanded by the BC to stop the document at the document-ready position or first line position as determined by the controlware program.

The operator then presses the READY switch on the operator control panel, sending a Ready signal to the BC. If the reader and BC are in a ready condition (no fault conditions exist) signals from the BC light the system READY indicator. When the system READY indicator lights, the BC initiates program commands for the transport drive, takeaway drive (Models F, G, H, and J) and mirror drive servo motors. The document is scanned line-by-line while being stepped through the read zone.

When the document has passed through the read zone it is picked up by a pair of takeaway belts which accelerate the document to 70 inches per second. A solenoid-operated sort gate either allows the document to pass through on the takeaway belts to sort pocket 2 or peels the document off the takeaway belts, causing it to drop into sort pocket 1. The sort gate solenoid operates via BC commands. Photosensors provide the BC with signals which correspond to document position in the takeaway area. The LOAD indicator goes out after the last document has been processed.

FEEDUP TABLE

Documents are loaded manually onto the feedup table, face up, with the leading edge towards the feeder. The top document is fed first. A wedge, mounted on the feedup table drive belt, positions the stack of documents for proper feeding. The belt carries the stack of documents to the feeder and is driven via a friction roller which is connected through a clutch to a constantly running motor. The clutch solenoid is energized by a sensor on the feeder which senses the proximity of documents to the feeder rollers. Pressing the ENABLE FEED UP switch on the operator control panel deenergizes the clutch solenoid during loading. The feedup belt stops and the wedge is pulled back to make room for documents. The feedup guide plates are adjusted for different widths by the PAPER GUIDE WIDTH ADJUST switch on the document adjustment panel.

FEEDER

The feeder consists of three roller assemblies: the pre-feed, the feed, and the dedoubler rollers. The pre-feed roller assembly pulls the top document off the stack and feeds the document towards the feed roller, which feeds the document onto the edger. The feed roller is positioned over the dedoubler roller. Having a higher coefficient of friction on paper than the dedoubler roller, the feed roller will drive a single document towards the edger when the document passes between the two rollers. The feed and dedoubler rollers both turn in a clockwise direction. When more than one document is fed between the two rollers, the lower document comes in contact with the dedoubler roller and is driven back towards the feedup table because the friction of paper to paper is less than the friction of the dedoubler roller to paper.

Adjustment of the vertical position of the dedoubler roller is made by turning the DOCUMENT THICKNESS ADJUST knob on the document adjustment panel. Adjustment is required to compensate for variations in paper thickness and for roller wear.

The feed, pre-feed, and dedoubler roller assemblies are all driven by the same motor that drives the conveyor and edger. Linear speed of the feeder assembly rollers is approximately 7 percent less than the speed of the edger and conveyor belts, causing a gap to develop between documents.

EDGER

The edger centers and squares documents coming from the feeder before they are moved through the read station by the conveyor. The edger contains a vacuum belt inclined at a small angle and driven at the same speed as the conveyor. The angle of the vacuum belt tends to push the document to the left. The document comes in contact with an edging wall which is aligned parallel with the conveyor centerline. The vacuum on the edging belt is controlled so that, as the document slides along the edging wall, document movement on the belt is possible and the document aligns itself to the conveyor. A cover at the edging wall reduces buckling of the document.

The PAPER GUIDE WIDTH ADJUST switch on the document adjustment panel moves the edging wall simultaneously with the feedup table guide walls so that a document, when edged, is accurately centered on the conveyor.

CONVEYOR

The conveyor moves the squared and centered documents from the edger through the read area. At the read area documents are formed into a concave surface, accurately located to be in focus for scanning. The conveyor stops the document while a line is scanned, and then rapidly steps the document to the next line to be scanned.

The conveyor consists of a 2-inch wide vacuum belt, a two-sectioned trough, a bar which supports mylar fingers, and conveyor drive elements. The vacuum belt moves the documents over a vacuum chamber and between the two trough sections. The mylar fingers hold the documents in contact with the concave surface at the read area. The conveyor drive elements are as follows: driven and idler rollers, a belt tensioner, a transport velocity servo drive system, a shaft position encoder, and timing belts, pulleys, and bearings.

TRANSPORT SERVO DRIVE SYSTEM

The transport velocity servo drive system synchronously drives the feeder, edger, and conveyor through a system of notched timing belts, pulleys, and tensioners. The system operates under controlware resident in the BC which is subject to status signals from the operator control panel and document sensor system as shown in figure 4-3. For a discussion of the generation of servo command signals, refer to the Controller Customer Engineering Maintenance Manual, Pub. No. 60324700. Driving power for the system is provided by a dc motor with a tachometer generator fastened to the shaft. The tachometer generator provides velocity feedback signals to the BC servo system. A position encoder is attached to the shaft of the conveyor drive assembly which provides position feedback signals to the BC.

The transport velocity servo drive system advances the conveyor vacuum belt to provide line-by-line document motion. Transport commands, as shown in figure 4-3, are generated by the BC after receiving line position correction data from the character recognition system. The BC determines from the line position correction data if the line being scanned is either above or below the optical centerline. The document can be advanced a minimum step distance of 0.024 inch (24 mils). Other step distances possible are 24 mils plus integral multiples of 0.008 inch (8 mils). If the character line is above the optical center, the document would be advanced the normal step distance less the distance above optical center. If the character line is below the optical center, the document would be advanced the normal step distance plus the distance below the optical center.

Each of the five velocity commands from the BC is routed to a digital-to-analog converter circuit in the reader as shown in figure 4-4. A logical 1 on an input line produces an analog signal corresponding to the associated conveyor belt velocity. Five velocities may be enabled: 5, 12.5, 20, or 40 inches per second, or 5 inches per second reverse. The velocity profiles used are related to the distance the document must travel to position the character line in the center of the read zone. The distances versus velocity profiles are shown in figure 4-5.

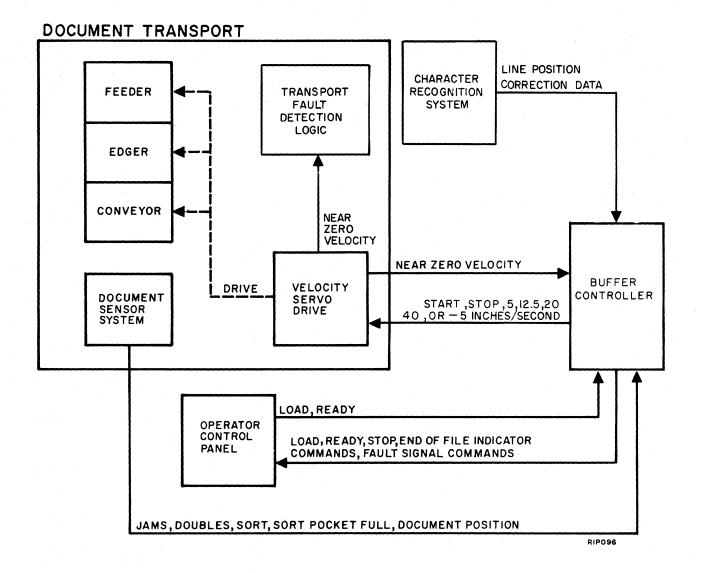


Figure 4-3. Document Travel Commands

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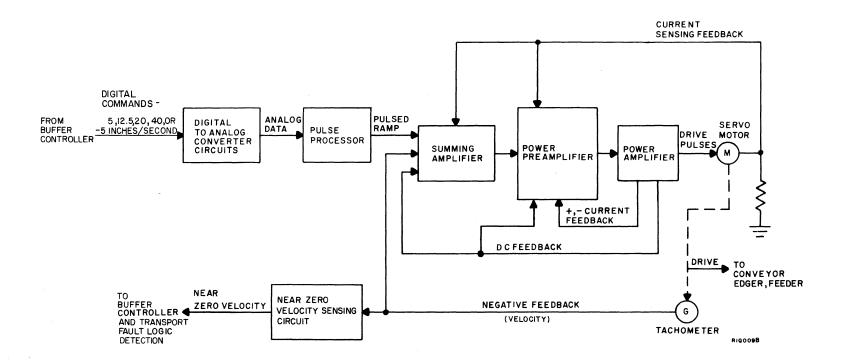
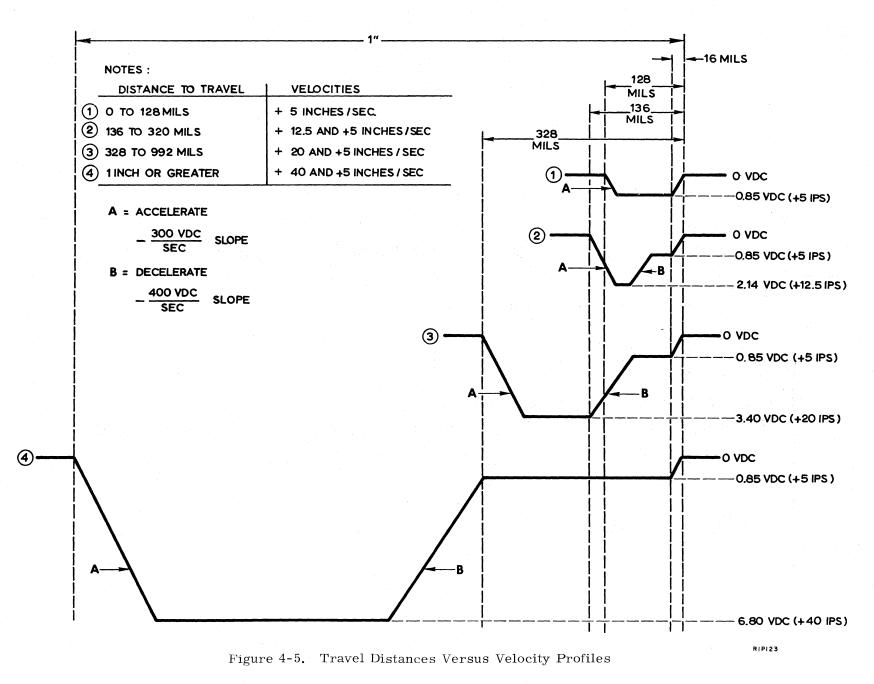


Figure 4-4. Transport Servo Block Diagram



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The analog data output of the digital-to-analog converter is routed to the pulse processor where a pulsed ramp signal is determined by the feed direction command. Negative-polarity ramp signals correspond to forward feed commands and positive-polarity ramp signals correspond to reverse feed commands.

The pulsed ramp signal is applied to the summing amplifier where it is summed with the tachometer output and a dc feedback signal from the power amplifier. Negative feedback signals from the tachometer are summed with the input reference signals to produce a servo error signal. The tachometer feedback also feeds a near-zero velocity sensing circuit which sends a status signal to the BC. A logical 0 status signal tells the BC that the conveyor belt is moving at a velocity of less than 0.35 inch per second in either the forward or reverse direction. A logical 1 status signal is sent to the BC when the conveyor belt velocity exceeds 0.35 inch per second. The dc feedback signal from the power amplifier provides additional servo compensation. Servo compensation assures that the desired mechanical output response is obtained, regardless of the nonlinear response of any of the elements within the servo loop.

The servo amplifier has a current limiting circuit which, when a predetermined current is exceeded, limits the power amplifier output by means of current feedback to the power preamplifier. Both positive and negative current limits are controlled.

A second current limiting circuit is preceded by a resistor in the drive motor return path, which provides a current sensing feedback voltage proportional to motor current. This voltage is routed to the summing amplifier and delay circuit which enables a clamp circuit when the motor current exceeds a predetermined safe value for a given length of time. The clamp circuit then limits the maximum continuous motor current.

The power amplifier generates high-current servo motor drive command signals.

TAKEAWAY SYSTEM

The takeaway system transports documents from the conveyor to the sort gate. The system consists of a pair of belts (one of which is a vacuum belt), a drum, a motor, and associated drive pulleys and bearings. The takeaway belts are driven at a constant rate of approximately 70 inches per second. As the document leaves the conveyor the pull of the takeaway belts, in combination with an input pinch roller, is enough to slide the document off the conveyor belt and transport the document to the sort gate. The takeaway system runs continually while the reader power is on in CJ122 Models C, D and E; the takeaway system is enabled by the Ready signal or the Load signal in CJ122 Models F, G, H, and J.

SORT GATE

The sort gate directs documents to either sort pocket 1 or sort pocket 2. The solenoidoperated sort gate is controlled by signals from the BC to either allow a document to be carried under a vacuum chamber by the takeaway belt to sort pocket 2 or to peel off the belt and drop into sort pocket 1.

SORT POCKETS

The two sort pockets receive documents from the sort gate. Each pocket holds a 5-inch stack of documents. Manually adjustable side and end guides within the sort pockets align the output documents as they are stacked to prevent paper jams. The end guides for both pockets are mechanically linked. Stacks of output documents can be removed by hand when the reader is in operation.

DOCUMENT SENSOR SYSTEM

The document sensor system provides signals to the BC corresponding to document position and status as shown in figure 4-6. The placement of the photosensor light source systems are shown in figure 6-72.

Feeder Sensor

The feeder sensor is activated by a metal flag mounted on the yoke of the pre-feed roller assembly and is positioned between the photosensor and light source. As the stack of documents contacts the pre-feed roller assembly and causes the assembly to rise, the metal flag moves from between the photosensor and light source. Contact is made and a signal is sent to the reader logic which disengages the feedup clutch, stopping the feedup belt.

Document Doubles Sensor

When more than one thickness of paper passes between the document doubles sensor and its light source, and the transport is moving forward, a doubles detect signal is sent to the BC. The DOUBLES CHECK indicator on the operator control panel (driven by the BC) and the DOUBLES INDICATOR on the document adjustment panel (driven by the reader) lights and the conveyor drive system is shut down until the double document condition is corrected by the operator. The DOUBLES ADJUST control on the document adjustment panel regulates the sensitivity of the document doubles photosensor to accommodate different types of paper. After the doubles condition is corrected, the doubles detect signal can be cleared by pressing FAULT RESET at the maintenance panel or STOP at the operator control panel; this will also clear the DOUBLES indicators.

Read Area Sensor

A read area sensor (document ready sensor) is located approximately 1 inch ahead of the read station as shown in figure 6-72. This sensor, when detecting a document, generates a Document Ready signal to the BC. The BC, through the transport velocity servo drive system, stops the document so that its leading edge is approximately 0. 214 inch past the optical center (document ready position) of the read area. The leading edge can also be at the document ready position plus an integral number of 40-mil steps and/or line steps. The signal (Document Ready) is also used by the BC to determine jams, to determine if the feedup table is empty, and to generate a signal which increments the TOTAL DOCUMENTS counter on the maintenance panel.

Sort Sensors

Sort entry, sort station 1, sort pocket 1 full, sort station 2, and sort pocket 2 full photosensors are located in the takeaway and sort pocket areas of the reader as shown in figure 6-72.

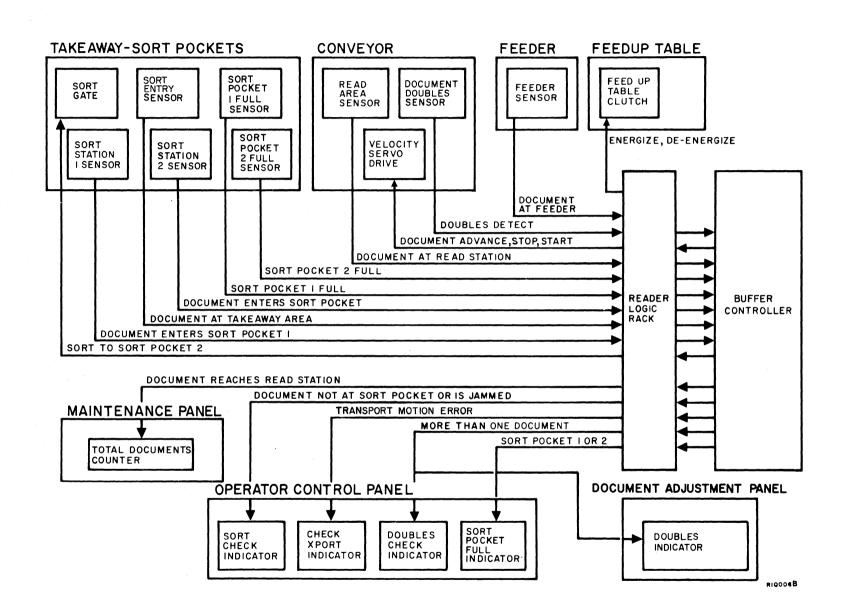


Figure 4-6. Document Sensor System

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These sensors provide the signals shown in figure 4-6 to the BC for sort control, sort pocket full, and paper jam detection.

SCANNING SYSTEM

When the READY switch on the operator control panel is pressed, a logical 1 signal goes to the BC, indicating that the document is at the read station. In normal operation, if no fault conditions exist in the reader and the reader and BC are "on line" to the computer, logic signals are sent from the BC to the reader. The reader turns the read lamp to full brightness and initiates command signals for the mirror velocity servo drive system which causes the scan mirror to scan a line of characters.

Light emitted by the lamp is reflected from an illuminating mirror onto the surface of the document being scanned as shown in figure 4-7. The illuminating mirror is attached to the same shaft as the scanning mirror to provide a moving spot of light synchronized to the spot on the document being scanned. The line scanning mirror system drives the mirrors under program commands from the BC. Velocity information is furnished to the mirror velocity servo circuits by a tachometer generator attached to the dc servo motor. Mirror position information is furnished to the BC by a mirror shaft incremental encoder that provides mirror position signals for every 0.048 inch (48 mils) of mirror travel in the document plane.

The line scanning mirror system causes the scanning mirror to sweep forward at a constant velocity of 75 inches per second over the line of characters being scanned. After the line of characters has been scanned and the sweep forward programmed start-stopping coordinate is reached, the mirror comes to a stop, and then sweeps back at a greater velocity to the next programmed flyback or zero mirror stopping coordinate. As the mirror sweeps back, the transport system conveyor belt advances the next line of characters to be scanned to the read area.

The scanning mirror reflects the image of each character scanned through a 240 mm lens. The image gathered by the lens is projected through a folded optics path consisting of one mirror, shown in figure 4-7, onto an image plane consisting of 54 plastic lightpipes. The optics path provides a magnification of 4.26. The image, as referenced to the scanned document, is seen on the image plane rotated 90 degrees to the right. As the scanning mirror moves from left to right in the document plane, the projected image moves in a vertical direction from top to bottom.

Each lightpipe in the image plane transmits a portion of the image to a photomultiplier tube. The photomultiplier tub**e** converts the light and dark image elements into electrical signals for processing by the character recognition system. For reading ANSI-OCR-A Size IV characters (optional) or for other optional character sets of comparable size, a second set of lightpipes and a program-controlled electromechanical shutter is installed which allows the selection of the proper set of lightpipes for reading either Size I or Size IV characters.

LIGHT SOURCE AND MIRRORS

Illumination for the line scanning mirror system is provided by a single 650-watt sun gun type lamp. The read lamp is normally in a half bright state and is only turned up to full bright during reading. The lamp operates at 500 watts to provide required illumination and to increase the life of the lamp. A variac enables adjustment of the lamp supply voltage to compensate for line voltage variations and aging of the lamp. Light emitted by the lamp is

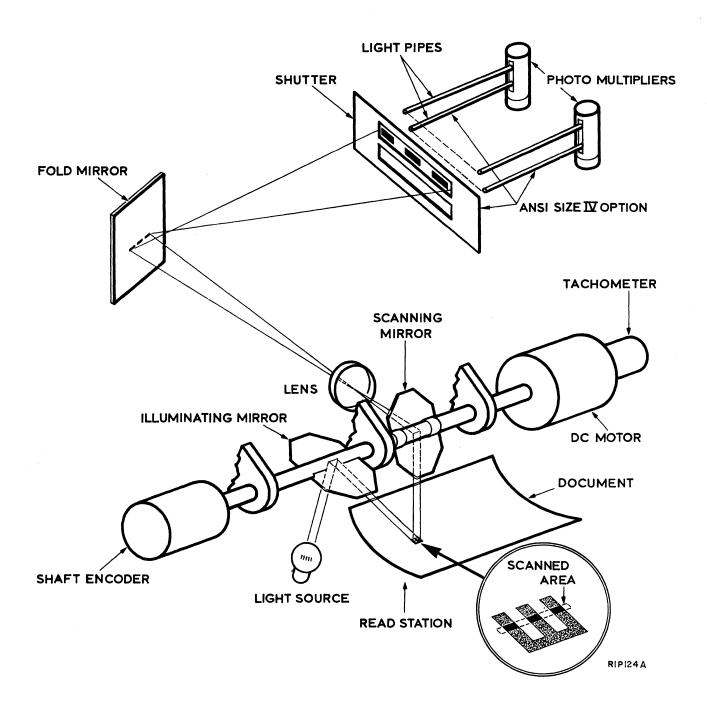


Figure 4-7. Scanning System

reflected from an illuminating mirror onto the surface of the document being scanned and the character image is reflected by a scanning mirror, mounted on the same shaft, through a lens.

READ STATION

The document is scanned on the concave surface at the read area. The surface of the scanning mirror is located at the center of the radius of the read area arc.

LINE SCANNING MIRROR SYSTEM

The line scanning mirror system consists of the following:

Mirror-BC Interface Logic Mirror Control Logic Mirror Velocity Servomechanism Mirror Velocity Sensing Circuits Mirror Velocity Error Detection Logic[†] Mirror Position Logic Mirror Fault Logic

A block diagram of the line scanning mirror system is shown in Figure 4-8.

Mirror-BC Interface Logic

The mirror-BC interface logic interfaces four programmed mirror commands from the BC to the mirror control logic. The four commands are Scan Forward, Accelerate Reverse, Zero Mirror, and Stop. These commands to the mirror control logic are inhibited during the initial power on sequence, during autoload sequences, and when the mirror fault logic registers an over-velocity condition. The line scanning mirror system is held in a standard stopped state when the mirror commands are inhibited by the interface logic.

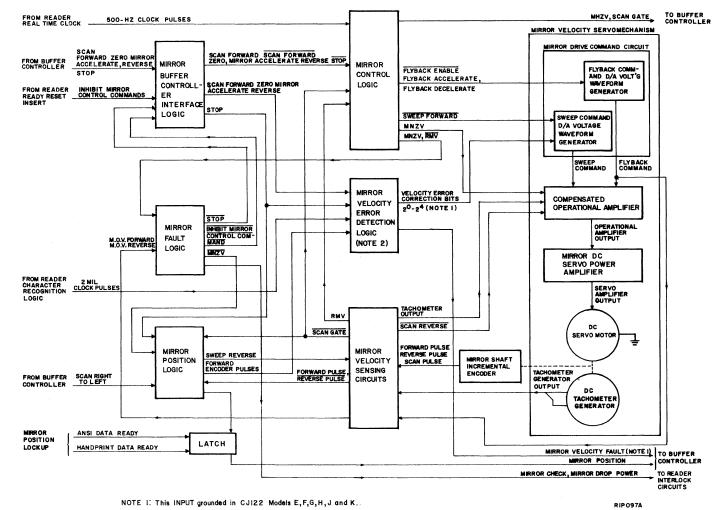
Mirror Control Logic and Mirror Velocity Servomechanism

The mirror control logic, under control of the programmed mirror commands from the BC, generates the control signals required for mirror motion functions. The Sweep Forward, Flyback Enable, Flyback Accelerate, Flyback Decelerate, and Delayed MNZV (Mirror Near Zero Velocity) signals are generated and sent to the mirror velocity servomechanism electronics to cause the line scanning mirror system to perform the following mirror motion functions:

Scan Forward Flyback Zero Mirror

The MNZV and Scan Gate signals are sent to the BC. The Scan Gate signal, originating in an incremental pulse encoder mounted on the mirror shaft assembly, is employed by the BC to clear its mirror coordinate storage location whenever the mirror is outside the 12.240inch long read area in the document plane. The MNZV signal is sent to the BC to indicate when a commanded mirror motion has been completed.

*CJ122 Models C and D



NOTE 2: CJ122 Models C and D only.

Figure 4-8. Line Scanning Mirror System Block Diagram

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The mirror velocity servomechanism consists of the following:

Mirror Drive Command Circuit Compensated Operational Amplifier Mirror DC Servo Amplifier DC Servo Motor and Tachometer Generator

Two digital-to-analog velocity command waveform generators in the mirror drive command circuit convert the time-varying mirror control signals into the Sweep Command and Flyback Command velocity command voltage waveforms required to perform the scan forward, flyback, and zero mirror motion functions. During scan forward mirror motions, the Sweep Command voltage waveform is the sum of the basic sweep voltage and the analog error correction voltage, which is converted from the five-bit digital output of the mirror velocity error detection logic.[†] The Sweep Command and Flyback Command voltage waveforms are applied to a compensated operational amplifier, which is the first stage of the mirror servo error amplifier. The compensated operational amplifier measures and amplifies the error between the commanded mirror velocity and actual mirror velocity as sensed by the tachometer generator mounted on the mirror shaft assembly. During mirror motions the feedback signal from the tachometer generator is opposite in polarity to the Sweep Command voltage input to the compensated operational amplifier. The compensated operational amplifier measures the sweep Command voltage input to the compensated operational amplifier.

For normal scanning, the mirror dc servo amplifier and servo motor are connected to cause the motor to turn clockwise as viewed from the motor shaft end, which results in the document being scanned from left to right; flyback or zero mirror motion functions will occur from right to left. For reverse scanning (mirror image option), the polarity of the compensated operational amplifier output is reversed to cause the motor to turn in the opposite direction, which results in the document being scanned from right to left; flyback or zero mirror motion functions will occur from left to right. Since the polarity of the command voltage waveforms is not changed for reverse scanning, but the direction of the servo motor is reversed, the Tachometer Generator Output signal is also reversed by the Scan Right to Left signal so that the feedback signal is again opposite in polarity to the input command voltage.

Sweep velocity in the document plane is directly proportional to the angular velocity of the servo motor. Ideally, the angular velocity of the servo motor is directly proportional to the Sweep Command and Flyback Command velocity command voltage waveforms applied to the compensated operational amplifier at every instant of time.

The Tachometer Generator Output signal is used also by the mirror velocity sensing circuits to detect forward and reverse over-velocity conditions. The corresponding fault signals are sent to the mirror fault logic.

An incremental pulse encoder, mounted on the mirror shaft as**s**embly, provides mirror position information to the mirror logic and to the BC. The encoder generates forward pulses when the mirror is scanning left to right, and it generates reverse pulses when

*CJ122 Models C and D

scanning right to left. Each encoder pulse period represents **0**.048 inch (48 mils) of mirror travel in the document plane. A logical 1 Scan Gate signal is also provided by the encoder when the mirror is sweeping within the read area. The BC uses the Scan Gate signal to determine the mirror coordinates at the far-left and far-right limits of the read area. For normal scanning, the far-left coordinate is 00_{16} and the far-right coordinate is FF_{16} . The distance between these coordinates in the document plane is 12.240 ($255_{10} \times 0.048$) inches. For reverse scanning (mirror image option), the mirror coordinates are reversed (the far-right coordinate is 00_{16}), because the mirror traverses right to left during scan forward and traverses left to right during flyback or zero mirror.

Scan Forward

The Scan Forward command from the BC enters the mirror control logic via the interface logic and is inverted and sent to the digital-to-analog sweep command waveform generator in the mirror drive command circuit as the Sweep Forward control signal. The mirror begins to move in the forward direction as the Sweep Command voltage output from the generator rises exponentially as shown in Figure 4-10. After an approximate 4-millisecond sweep startup time (approximately two encoder pulse counts), the Sweep Command voltage applied to the compensated operational amplifier results in a scan forward velocity of 75 inches per second. An additional 2.5 millisecond sweep settling time (four encoder pulse counts) is allowed for the mirror to achieve the nominal scanning velocity of 75 inches per second. At the end of the sweep settling time, the read operation is initiated by the BC and the line of characters is read.

As the mirror is sweeping forward, the Sweep Command voltage is summed with the analog error correction voltage, which is converted from the five-bit digital output of the mirror velocity error detection logic.[†] The resultant command voltage enables the mirror to maintain a nominal scanning velocity of 75 inches per second.

When the mirror reaches the programmed start stopping coordinate, the BC drops the Scan Forward command and generates the Stop command. The Sweep Command voltage waveform decays exponentially towards 0 vdc at this time and the mirror will be virtually stopped within 6 milliseconds.

Approximately 8 milliseconds after the BC issues the Stop command, the mirror control logic generates the MNZV signal which is sent to the BC as an end-of-operation signal.

The MNZV signal is also sent to the servo amplifier circuits where it causes the gain of the compensated operational amplifier to be reduced to approximately 5 and shunts to ground the input signal to the mirror dc servo power amplifier. This is done to prevent any mirror drift due to small offset voltages in the servo amplifier circuits. The effect of the gain reduction and shunt is to reduce the voltage that can appear across the servo motor to near zero; the motor and mirror shaft friction prevents the mirror from moving.

Flyback

After a scan forward mirror motion is completed and the mirror stops, the BC issues the Accelerate Reverse command which initiates the flyback mirror motion. During flyback, the

^{*}S/N 103 - 150 only.

mirror accelerates in the reverse direction until it reaches a programmed flyback switching coordinate, at which time it starts decelerating as shown in figure 4-9. The mirror decelerates until the velocity decreases to -125 inches per second and maintains this velocity for approximately 6 milliseconds until the start-stopping coordinate is reached. The mirror normally stops within 6 milliseconds after the start-stopping coordinate is reached, and is in the proper position to scan the next line of characters.

Upon receiving the Accelerate Reverse command from the BC, the mirror control logic sends the Flyback Enable and Flyback Accelerate control signals to the digital-to-analog flyback command voltage waveform generator in the mirror drive command circuit. The Flyback Enable signal releases an integrator in the waveform generator and the Flyback Accelerate signal causes a constant current to flow into the summing junction of the operational amplifier-integrator circuit in the waveform generator. The generator output (Flyback Command voltage waveform) increases negatively with a fixed slope of -350 vdc per second (adjustable), which corresponds to a mirror acceleration of -62,000 inches per second² in the document plane. Since the Flyback Command voltage polarity is opposite the Sweep Command voltage polarity, the compensated operational amplifier output causes the servo motor to turn counterclockwise as viewed from the motor shaft end, which results in a flyback motion from right to left. For reverse scanning (mirror image option), the polarity of the compensated operational amplifier output signal is reversed, which results in a flyback motion from left to right.

The Accelerate Reverse command terminates when the BC determines that the mirror has reached the flyback switching coordinate in the document plane where the mirror should start slowing in preparation for stopping. The exact switching coordinate depends on the total flyback distance to be traveled. Normally, the programmed switching coordinate is near the midpoint of the total distance the mirror is commanded to fly back. At this time the mirror control logic drops the Flyback Accelerate signal and sends the Flyback Decelerate signal to the digital-to-analog flyback command waveform generator in the mirror drive command circuit. The Flyback Decelerate signal causes current to flow out of the summing junction of the operational amplifier-integrator circuit in the waveform generator, thus decreasing the Flyback Command voltage with a fixed slope of +350V per second (adjustable), which corresponds to a mirror velocity deceleration of +62,000 inches per second² in the document plane. When the velocity decreases to -125 inches per second, the reverse mirror velocity (RMV) signal generated by the mirror velocity sensing circuit goes to a logical 0. This "1" to "0" transition causes the mirror control logic to drop the Flyback Decelerate control signal, which subsequently freezes the integrator in the flyback command voltage waveform generator, causing it to "hold" an output command voltage corresponding to -125 inches per second. Thus, a mirror velocity of -125 inches per second is maintained for approximately 5 milliseconds (back porch) until the flyback start-stopping coordinate is reached. At this time the BC issues the Stop command, which causes the mirror control logic to change the Flyback Enable control signal to logical 1. This action disables the integrator in the flyback command voltage waveform generator, causing the Flyback Command voltage to decay exponentially towards 0 vdc and stop the mirror servo motor.

Once the flyback stopped coordinate is reached, the MNZV signal functions as described for the scan forward mirror motion.

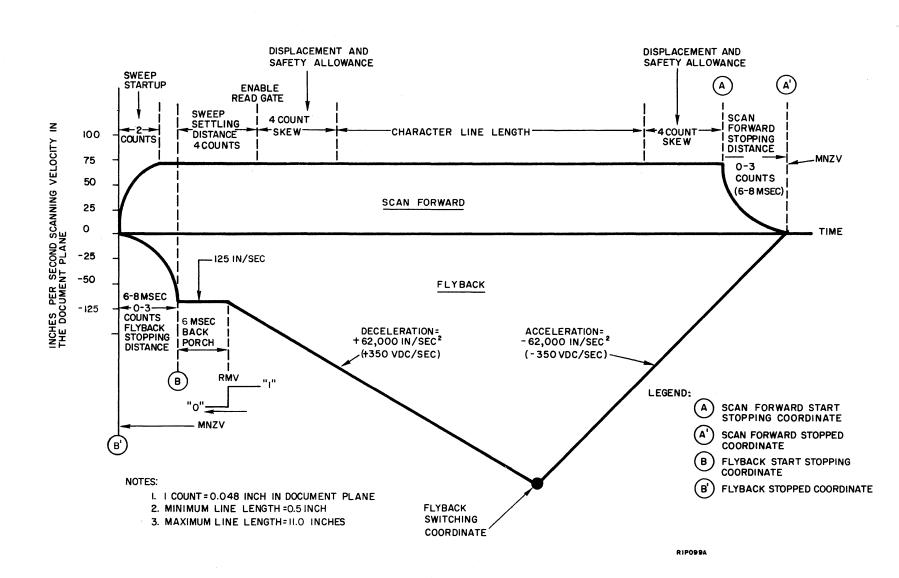


Figure 4-9. Scan Forward and Flyback Waveforms

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Zero Mirror

The zero mirror motion function is normally used for two purposes.

- 1. To establish the far-left document plane coordinate (or far-right coordinate for the mirror image option) of 00_{16} with the first mirror motion in order to initialize the BC and reader mirror logic.
- 2. To synchronize the BC and reader mirror logic with the exact mirror position when the BC has lost track of the mirror position.

The zero mirror motion functions similar to the flyback motion with basically three exceptions as shown in the waveform in figure 4-10. The first exception is that the mirror accelerates only to a reverse velocity of -125 inches per second, rather than to a programmed switching point.

The mirror maintains a constant velocity of -125 inches per second in the reverse direction until the start-stopping coordinate is reached. The second exception is that the zero mirror waveform contains no deceleration or back porch prior to the start-stopping coordinate. The third exception is that the start-stopping coordinate is determined by the logical 1 to 0 transition of the Scan Gate signal from the mirror shaft encoder, rather than a programmed start-stopping coordinate based on distance to be traveled.

Upon receiving the Zero Mirror command from the BC, the mirror control logic sends the Flyback Enable and Flyback Accelerate control signals to the mirror drive command circuit. Like flyback mirror motions, the Flyback Command voltage waveform increases negatively with a fixed slope of -350 vdc per second (adjustable), which corresponds to a mirror acceleration of -62,000 inches per second² in the document plane. When the mirror reaches a velocity of -125 inches per second, the RMV signal generated by the mirror velocity sensing circuit goes to a logical 1. This 0 to 1 transition causes the main control logic to drop the Flyback Accelerate control signal, which subsequently freezes the integrator in the flyback command voltage waveform generator, causing it to "hold" an output command voltage corresponding to -125 inches per second. Thus, a reverse mirror velocity of -125 inches per second is maintained until the mirror travels out of the read area. When this happens, the Scan Gate signal from the mirror shaft encoder goes to a logical 0. The BC immediately drops the Zero Mirror command and issues the Stop command, which causes the mirror control logic to switch the Flyback Enable control signal to a logical 1. Like flyback mirror motions, this action disables the integrator in the flyback command voltage waveform generator, which causes the Flyback Command voltage to decay exponentially towards 0 vdc and stop the mirror servo motor.

Once the zero mirror stopped coordinate is reached, the MNZV signal functions as described for the scan forward mirror motion.

Mirror Velocity Sensing Circuits

The dc tachometer generator output is connected to the mirror velocity sensing circuits, which send the Tachometer Output feedback signal to the compensated operational amplifier and, the M. O. V. (Mirror Over Velocity) Forward and M. O. V. Reverse signals to the mirror fault logic, as shown in figure 4-8. The M. O. V. Forward signal is generated if the mirror forward velocity exceeds +200 inches per second, and the M. O. V. Reverse signal is generated if the mirror reverse velocity exceeds -1160 inches per second. Either

over-velocity condition will immediately inhibit all mirror motion commands and initiate an orderly stop.

The Forward Pulse, Reverse Pulse, and Scan Gate signals from the mirror shaft incremental encoder are inverted and sent to the mirror position logic and mirror control logic.

The Flyback Command voltage waveform from the mirror drive command circuit is applied to a voltage comparator which generates the RMV signal used during Zero Mirror and Flyback mirror motions.

Mirror Velocity Error Detection Logic[†]

The mirror velocity error detection logic provides a five-bit digital error correction input to the sweep command voltage waveform generator in the mirror drive command circuit as shown in figure 4-8. This velocity error correction input assists the mirror velocity servomechanism in maintaining a forward velocity of nominal 75 inches per second.

The Scan Forward control signal from the mirror control logic enables a four-stage counter to count forward pulses generated by the mirror shaft encoder. When six forward pulses have been counted, a nine-stage counter is enabled to count 2-mil pulses from the crystal oscillator clock divider network in the character recognition logic. The six-count delay is incorporated so that the mirror will obtain the nominal sweep forward velocity of 75 inches per second before velocity error measurement and correction is initiated. The nine-stage counter counts 2-mil pulses during each interval of 15 mirror shaft encoder forward pulses, and resets after each successive 15 encoder pulse count interval. A predetermined count of 359 represents the number of 2-mil pulses that will be counted during each 15 encoder pulse count interval when the mirror forward velocity is exactly 75 inches per second. An adjustment is made to the Sweep Command voltage waveform if the count in the nine-stage counter is different from 359 at the end of any count interval. At the end of a scan forward mirror motion, any partial count obtained over less than a 15 mirror shaft encoder pulse period is discarded and no correction is made to the Sweep Command voltage waveform.

The count from the nine-stage counter represents the average velocity of the mirror during the time period the count is obtained. One-half the difference between the actual measured encoder pulse count and the reference count of 359 is either added to or subtracted from the contents of an error register. The five-bit digital output of the error register is sent to the analog-to-digital sweep command voltage waveform generator, where the analog error correction voltage is summed with the basic sweep voltage, thereby increasing or decreasing the total Sweep Command voltage applied to the command input of the compensated operational amplifier.

A Mirror Velocity Fault signal is sent to the BC if the count in the nine-stage counter is 16 counts lower or 15 counts higher than the predetermined count of 359 at the end of any 15 encoder pulse interval. The Mirror Velocity Fault signal indicates that the average forward velocity of the mirror over a 15 mirror shaft encoder pulse interval is approximately 4.5 percent higher or lower than nominal 75 inches per second.

[†]CJ122 Models C and D only.

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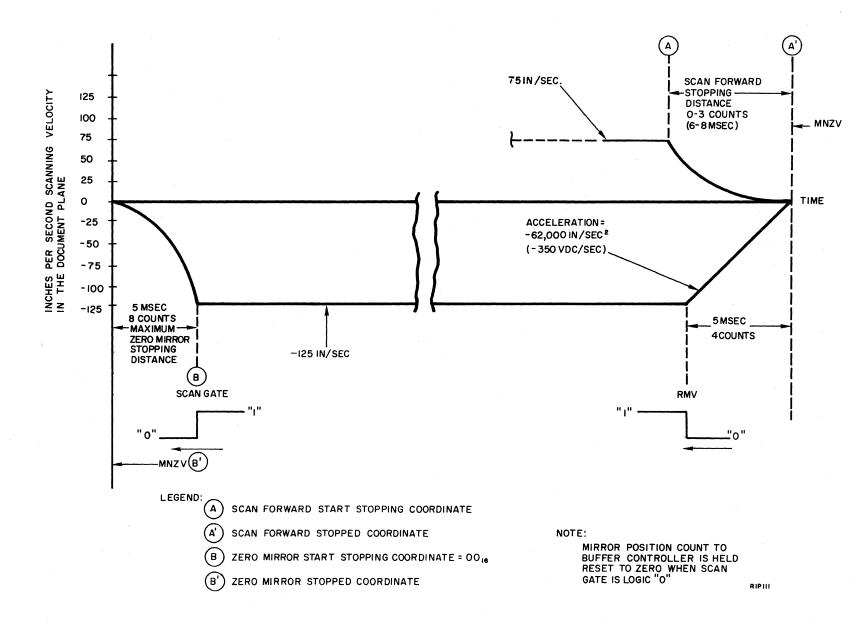


Figure 4-10. Zero Mirror Waveform

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Normally, any slight velocity errors during scan forward mirror motions are corrected through compensation provided by the Tachometer Output signal applied to the input summing circuit of the compensated operational amplifier.

Mirror Position Logic

The mirror position logic generates an 8-bit mirror position code which enables the BC to track the mirror position. During scanning operations, the BC uses this information to update its mirror position storage location during programmed motion command sequences. An 8-bit, up/down mirror position counter counts Forward Pulse and Reverse Pulse signals received from the mirror shaft encoder via the mirror velocity sensing circuits as shown in figure 4-8. The counter is enabled by the Scan Gate signal only when the mirror is positioned within the read area.

The mirror shaft encoder always generates forward pulses when the mirror moves from left to right. Reverse pulses are always generated when the mirror moves right to left. Consequently, the physical relationship between mirror direction and encoder pulses remain fixed.

During reverse scanning (mirror image option), the encoder will generate reverse pulses when the mirror is commanded to scan forward, and forward pulses when the mirror is commanded to flyback or zero mirror because the input to the mirror dc servo amplifier is reversed to cause the servo motor to turn in the opposite direction from normal. For this reason, the Scan Right to Left signal produced by the BC during reverse scanning is also used to reverse the Forward Pulse and Reverse Pulse signal inputs to the mirror position counter. Therefore, the mirror position counter always increments during scan forward mirror motions in either direction, and decrements during flyback or zero mirror motions in either direction.

Since the distance traveled per mirror encoder pulse equals 0.048 inch in the document plane, the BC can determine the mirror position by noting the change in the 8-bit mirror position code. An 8-bit register stores the mirror position count at Handprint Data Ready or Character Data Ready time. This stored position tags a character's position and is used by the BC for handprint space generation and OLCC underline determination.

Mirror Fault Logic

The mirror fault logic inhibits the mirror control commands from the BC and causes the line scanning mirror system to be held in a standard stopped state when either a forward or reverse over-velocity condition is detected by the mirror velocity sensing circuits as shown in figure 4-8. A forward over-velocity condition causes the mirror control logic to command the mirror system to an immediate stop. For a reverse over-velocity condition, the mirror starts decelerating when the Accelerate Reverse Command is inhibited. When the mirror reverse velocity decreases to -75 inches per second, the RMV signal causes the mirror fault logic to generate the Stop signal which forces the mirror system to a stopped state without producing a back porch in the flyback waveform. Reader power is dropped if the mirror does not stop within 75 milliseconds after an over-velocity condition is detected.

LIGHTPIPES

The image segment of the character being scanned is reflected onto an array of 54 lightpipes, arranged in a horizontal column (vertical column with respect to the scanned image). Each lightpipe is made of Lucite, is 25 mils in diameter, and is from 25 to 35.5 inches long. The lightpipes make a 90-degree radius bend from the image plane to the photomultiplier tubes. The lightpipes are supported in this 90-degree transition by a foam-covered shield assembly and a lightpipe net.

Although lightpipe number 2 senses the top of the viewing area on the document and lightpipe number 55 views the bottom of the viewing area (for ANSI-OCR-A Size I characters), only 17 lightpipes receive the character centerline image. The read zone or active read area in the document plane is 0.304 inches high when reading with a full-height read window. This read zone for ANSI-OCR-A Size I characters is equal to approximately three character heights. Thus, a character can fall anywhere within this read zone and still be projected onto the array of lightpipes or image plane. Each lightpipe transmits a 5.85 mil portion of the image (ANSI-OCR-A Size I optical scaling) to a photomultiplier tube in the analog video circuits of the character recognition system.

CHARACTER RECOGNITION SYSTEM

The character recognition system analyzes scanned character images and outputs corresponding character codes to the BC. Data flow within the system is shown in figure 4-11. The lightpipes receive a light image from the lens and mirrors. The image is then transmitted to the photomultiplier assembly which outputs electrical analog video signals corresponding to the light image. The quantizer circuits convert these analog video signals to digital form; a logical 0 representing black and a logical 1 representing white. The accumulator register also receives digital simulated video signals from the BC via the simulated optical data gates, and transfers the digital video signals to the load register through normal or mirror image gating. The mirror image gating, through BC commands, enables shifting from the top or bottom end of the load register for normal or upside-down image recognition. Video data is shifted serially from the load register to the image register via the vertical line thickening and scrubbing circuits. The digitized character is reconstructed in the image register, which consists of 15 rows of 56 bits each; the top 24 bits are tied to the register diode matrices. For diagnostic testing, data in the image register may be sent to the BC or recirculated within the image register. The BC causes certain character matrices to be inhibited through the font inhibit logic.

For each vertical shift period the character comparator selects the matrix whose output is the best character match or the character voltage which is nearest zero volts. The character encoder contains character encoder circuits which output the character code and voltage code corresponding to the recognized character. These character and voltage codes are transferred to the pre-character cycle logic which performs checks to correctly identify the character. The character centerline logic determines the nominal position of the character in the image register. Topless/bottomless data detection logic determines if the character is extending above or below the read zone. Space generation logic detects space between characters. Character output logic monitors signals from the system and outputs data of the BC.

The following paragraphs contain a detailed description of the functional circuits in the character recognition system.

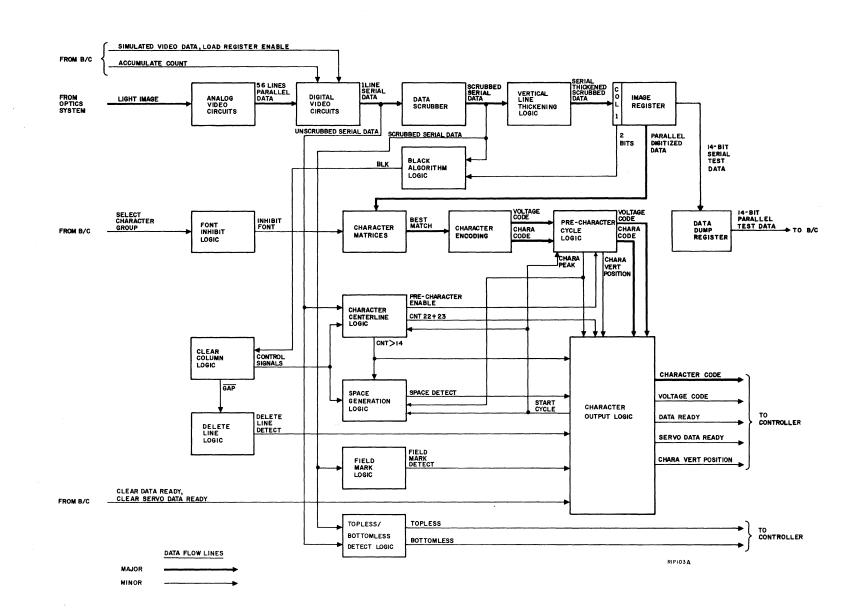


Figure 4-11. Character Recognition System

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ANALOG VIDEO CIRCUITS

The analog video circuits develop a digital output representing combinations of black and white information, as shown in figure 4-12. Diffuse light from a document is gathered by a lens system, projected onto a set of lightpipes, and transmitted via these lightpipes to 54 photomultiplier tubes.

Photomultipliers

A photomultiplier is a vacuum tube that converts light energy into electrical analog signals. When the light beam (photons) from the lightpipe strikes the cathode, the force of the collision causes the cathode to emit electrons in proportion to the amount of light energy received. The cathode electrons successively strike a series of dynodes which, in turn, emit electrons. When the electrons reach the final terminal (the anode), they have been multiplied many times to provide a usable current output. With a constant voltage across the tube, the output current is directly proportional to the light input. The output of the photomultiplier tube is applied to a photomultiplier pre-amplifier/servo board.

Photomultiplier Pre-Amplifier/Servo Board

The photomultiplier pre-amplifier/servo board amplifies the output of the photomultiplier tube to a voltage level that is usable by the character recognition system circuits. The servo board controls the gain of the photomultiplier tube by controlling the high voltage applied to cathode and dynodes in the photomultiplier tube. The output of the pre-amplifier is applied to an associated quantizer circuit, which has a video bandpass of 15 kHz.

Quantizer Circuits

The quantizer circuits compare the outputs of the pre-amplifiers with a program-selected quantize reference level. The quantize level is determined by an 8-bit quantize level select word from the BC. This 8-bit word controls the output of the data quantize level digital-to-analog converter which develops a video quantize reference level for the 54 quantizer circuits. Quantizer circuits 2 through 55 make the comparison between the associated video pre-amplifier output and the video quantize reference level and output either a logical 1 or 0 to the digital video circuits. Quantize circuits 1 and 56 receive a fixed input of -15 vdc which enables a constant logical 1 output from these circuits to the digital video circuits. For readers with handprint option, the quantizing level is automatically increased by 36_{16} (54_{10}) when handprint mode is enabled.

DIGITAL VIDEO CIRCUITS

The digital video circuits, shown in figure 4-13, perform the following functions: thicken vertical and horizontal lines, accumulate the data for discrete sampling or horizontal lines thickening, scrub unwanted black bits from the top and bottom of the vertical column of data, and transfer the data serially into the image register. The digital video data is transferred in 56 parallel channels from the analog video circuits via video select gates to the accumulator register. Simulated digital video data from the BC may also be sent to the accumulator register for diagnostic purposes. A switch on the maintenance panel enables the gates to allow either the optical data or simulated data to be sent to the accumulator register.

The horizontal line-thickening circuit thickens a vertical line horizontally by accumulating data from 1 to 59 shift clock periods under BC program control. (This circuit is referred

to in system software as vertical line thickening.) The BC tells the accumulator register the number of shift clock periods (from 1 to 59) to accumulate the data before parallel shifting the data to the load register. A count of 1 is maximum thicken, a count of 59 is minimum thicken and a count of 30 is nominal. This horizontal accumulation of data thickens a vertical line stroke. The contents of the accumulator register are transferred to the load register in parallel once every 60 shift clock periods. The data is transferred through an upside-down image gating structure. The normal gates are connected directly to channels 1 through 54 of the accumulator register and the upside-down image gates are connected to effect a reverse of the order as shown in figure 4-14. Upside-down image gating transfers either a normal or upside-down (if mirror image option is installed in reader) image of the accumulator register contents to the load register after receiving either a Load Normal Enable or Load Mirror Enable signal from the BC.

Load Register

The load register is a 56-bit shift register which converts the mode of data transfer from parallel to serial. The normal output of the load register is from the topmost bit, as shown in figure 4-14, and data is unloaded by clocking in 56 "0" bits from the bottom stage of the load register. The load register output is applied to a scrubbing circuit and to vertical line-thickening circuits controlled by the BC.

Scrubbing Circuit

The scrubbing circuit receives serial data from the load register and will change any black bit to a white bit if that bit is in a continuous vertical column extending to the edge of the read window or beyond.

Vertical Line-Thickening Circuit

The vertical line-thickening circuit thickens horizontal lines in a vertical direction. This circuit (referred to in system software as horizontal line thickening) samples three bits of information in a 1-2-3, 2-3-4, 3-4-5, etc., series as the load register output passes through the circuit to the image register. When the combination of white-black-white occurs, the last white or bottom bit of the three-bit series is converted to a black bit, or logical 1. The output of the vertical line-thickening circuits is normally fed to the bottom-most bit of the first column in the image register.

When the mirror image option is installed, the output of the vertical line-thickening circuits can be fed to the bottom bit of the 15th image register stage by selecting the left to right control line which will further reconnect the image register so that it will shift in a reverse direction. The vertical line-thickening circuits output can also be routed to the BC by maintenance panel switching.

IMAGE REGISTER

The image register is a group of 15 serial load shift registers. Each register is made up of 56 stages or bits, thus forming a 15 by 56 matrix. The output of the top bit of one shift register is connected to the input of the bottom stage of the left adjacent shift register or vice versa when left-to-right shift is enabled. The image register normally receives serial input data from the load register at the lowest bit of the right-most shift register column (column 1).

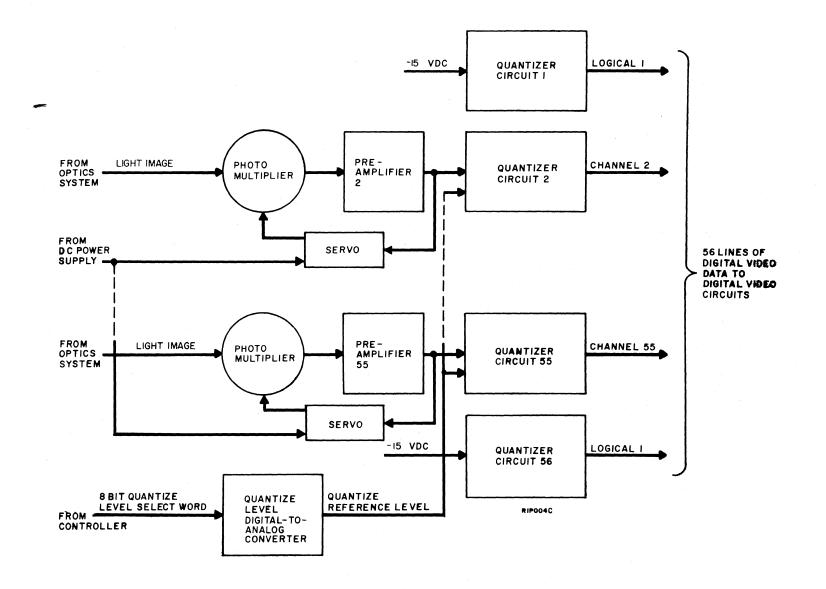
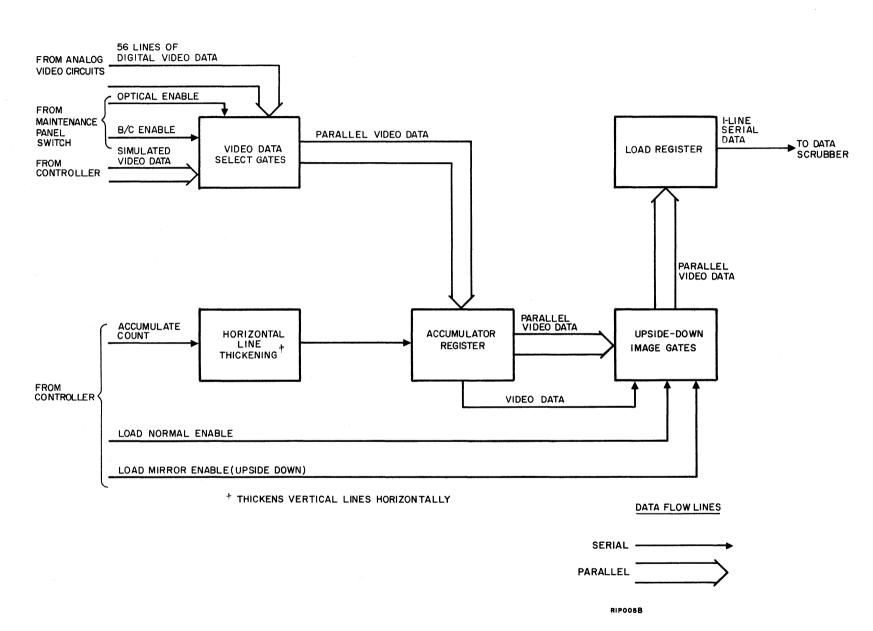
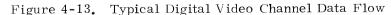


Figure 4-12. Analog Video Circuits

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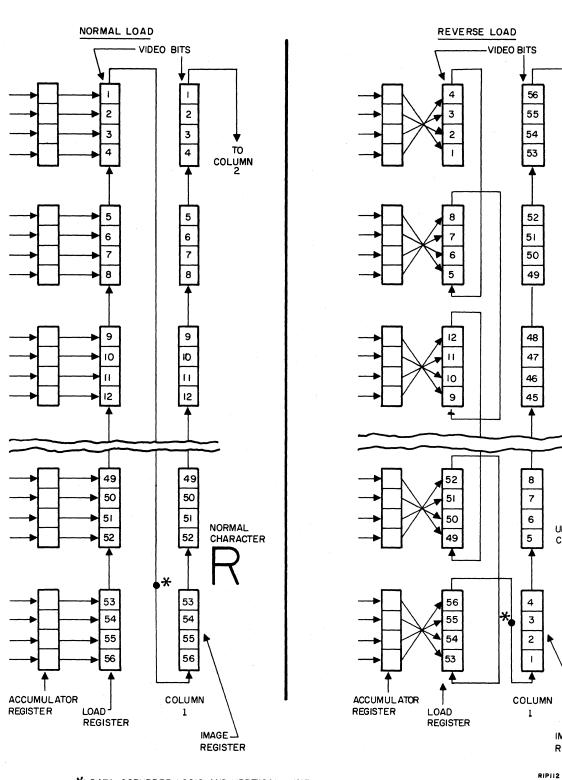
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* DATA SCRUBBER LOGIC AND VERTICAL LINE THICKENING LOGIC ARE NOT SHOWN.

Figure 4-14. Normal and Reverse Loading of Load Register

IMAGE -

REGISTER

TO COLUMN 2

UPSIDE-DOWN

CHARACTER

The character centerline image (ANSI Size I) can be represented within an area of about 13 by 17 bits or stages of the image register. Parallel outputs of the upper 24 by 15 bits are used to drive the resistor-diode character matrices. The image register provides a wide range of vertical image storage facilitating a simple means for reading images which are not in vertical registration. The character image in the image register is shifted through all stages. Since the character matrices are connected to the top 24 by 15 image register stages, an image must pass through a standard position and thus be correlated and processed for recognition.

For diagnostic testing, digitized character image data (optical or simulated) is sent to the BC, shown in figure 4-11, in a group of four 14-bit segments for each image register column (56 bits per column). The top bit of the left-most or 15th image register column or the top bit of the load register (maintenance mode) is connected to a 14-bit serial-to-parallel converter. The output of the serial-to-parallel converter is sent to a parallel-to-parallel buffer register. The buffer register output is available for sampling by the BC. The type of data loaded and the point of output (load register or image register) are controlled by either the BC program and maintenance panel switches or maintenance panel switches only.

CHARACTER MATRICES AND ASSERT-NEGATE DIAGRAMS DESCRIPTION (See figure 4-15)

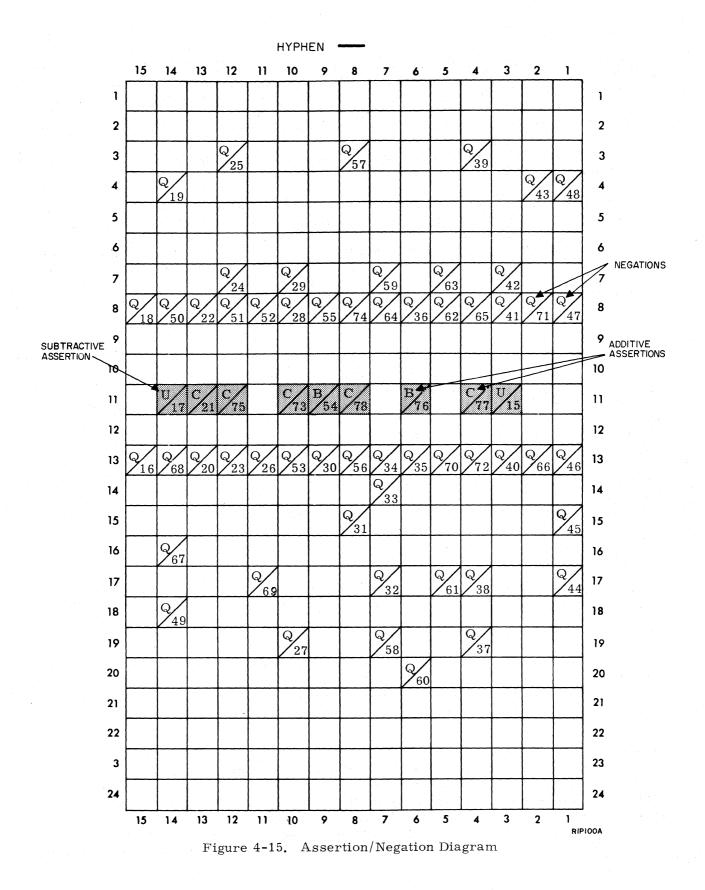
The electronic image of each scanned character is recreated in the image register and correlated with a set of stored character reference images, or matrices. The number of scanned sample points that can define a character image is a matrix of points 15 wide by 24 high. Image register points are selectively applied to the character matrices, i. e., only those points/areas which are required for recognition are used. Normally, one matrix is required for each character to be recognized. Each character matrix is a resistor-diode summation network which contains assertion and negation points. An assertion point is a positive image point and a negation point is a negative image point. When reading, each character matrix produces a correlation scalar voltage output which is processed by the recognition circuits to determine which matrix (character) is best matched.

Assertion Areas

Assertion areas are positive image points which in relationship to matrix summation networks are either additive, subtractive, or "don't care" image points. Image register assertion points are applied to the character matrix summation networks through resistor and resistor-diode inputs, or weights. These weights are represented on the assert-negate diagrams by the weight code symbol + or the weight code letters A, B, C, S, T, U, and V in shaded boxes. The weight codes +, A, B, and C represent a resistor only, and these weights are additive when an image register point is black: when the image register point is white, they are subtractive. The weight codes S, T, U, and V indicate diode assertions. Diode assertions are subtractive when the image register point is white; when the image register point is black, they are "don't cares" and have no effect on the summation network.

Negation Areas

Negation areas are negative image points which are subtractive when an image register point is black; when the image register point is white, there is no effect on the summation network. Negation points are applied to the character matrix summation networks through resistor-diode input, or weights. Negations are represented on the assert-negate diagrams by the weight code letters N, O, P, and Q in unshaded boxes. Boxes which do not contain weight code data represent areas that are not sampled as they are not critical for recognition.



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Weighting

The character matrix resistor values are weighted. The significance of the observed assertion and negation areas is varied as described in table 4-1.

Code	Weight	Network	Type of Image Point		
+ A B C S T U V N O P Q	1 2 3 4 1 2 3 4 1 2 3 4	12K Resistor 6. 2K Resistor 3. 9K Resistor 3K Resistor 12K Resistor-Diode 6. 2K Resistor-Diode 3 9K Resistor-Diode 12K Resistor-Diode 6. 2K Resistor-Diode 3. 9K Resistor-Diode 3K Resistor-Diode	Diode Assertion Diode Assertion Negation		
Assertion					

TABLE 4-1. ASSERT-NEGATE DIAGRAM SYMBOLOGY

The weight code depicted on the assert-negate diagram represents the relative weight assigned to a given assertion or negation area. For example, an "A" or a "T" is approximately twice the weight of a "+", and represents half the resistance of a "+". A "B" or a "U" is approximately three times the weight and represents one-third the resistance of a "+".

Character Matrix Connector Pin Numbers

Character matrix connector pin numbers, depicted below the diagonal line in each applicable box on the assert-negate diagrams, reference the connector input pin numbers associated with the assertion and negation areas. The input to the character matrix can be monitored at the appropriate pin. Because the card placement can vary with each reader, do not remove more than one matrix card at a time. Refer to the Diagrams Manual, volume 2 for assert/negate diagrams for the standard font used in the reader or to the applicable font option manual.

FONT INHIBIT LOGIC

Commands from the computer via the BC may inhibit select groups of matrices through the

font inhibit logic by disabling the character matrices which are not to be read (voltage clamping of matrices at worst case match voltage).

CHARACTER ENCODER

The character encoder digitizes the highest analog scalar product into two paths; a 7-bit character code and a 4-bit voltage code as shown in figure 4-16. Analog scalar products or best match voltage of from 0 to 5 volts (5 volts being worst character match) on the character matrix bus lines are applied to the common-emitter circuits. The matrix correlation voltage is a range limited to a 5-volt swing (clamped at 5 volts). Without being clamped, the swing would be from 0 to 10 volts. In conjunction with the constant current circuit, the common-emitter circuits function as a means for best match selection. For each vertical shift time one common-emitter circuit will indicate which character matrix had the best match. This best match selection is sent to the character encoder where it is converted into a 7-bit ASCII code. A character quantizer monitors the voltage level output of the common-emitter circuits to sense if a character double has occurred. The output (7-bit ASCII code) from the character quantizer/character encoder is sent to the pre-character cycle logic.

The common-emitter circuits also provide a buffered analog signal of the best match voltage to an analog-to-digital (A/D) converter. The A/D converter digitizes the analog voltage into 16 separate levels and outputs a 4-bit binary voltage code to the pre-character cycle logic. The 7-bit character code and the 4-bit voltage code enter the pre-character cycle logic for each image register shift (clock) time.

PRE-CHARACTER CYCLE LOGIC

The pre-character cycle logic selects the voltage code and character code of the character whose matrix has, over a period of time, the highest voltage code. The pre-character cycle logic also determines if the voltage codes and character codes, over a period of time, meet certain minimum standards. These standards must be exceeded for character code generation. If these standards are not met a reject code is generated.

At the start of each cycle, the pre-character logic is always cleared. At each image register shift time a 4-bit voltage code and a 7-bit character code enters the pre-character cycle logic. The 4-bit code is compared with the contents of the voltage code register N_2 which has been cleared at the start of the cycle. If the new voltage code stored in register N_1 is greater than the voltage code stored in register N_2 by at least one count, the new 4bit code is stored in register N_2 and the 7-bit character code is stored in register C_2 . If the new 4-bit voltage code is not larger, registers N_2 and C_2 will remain in their present state. This procedure continues until the end of the cycle, which is determined by the character cycle read logic. When the cycle ends, the character and voltage codes are stored in character code data flow logic and voltage code data flow logic.

The implementation of this process is accomplished by comparators which perform the algorithm of $N_1 = N_2$, $N_1 \ge N_2$, $N_1 \ge CPRL$, $C_1 = C_2$, and $N_1 = N_2 + DOUBLES$. The 4-bit voltage code (N_1) is compared in the $N_1 \ge CPRL$ comparator with a Character Peak Reference Level from the BC. When N_1 is greater than CPRL, and $N_1 \ge CPRL$ (or character peak) signal is sent to the character peak logic. N_1 and N_2 are compared in the $N_1 = N_2$ and $N_1 \ge N_2$ comparators and the results are sent to the pre-character cycle control logic.

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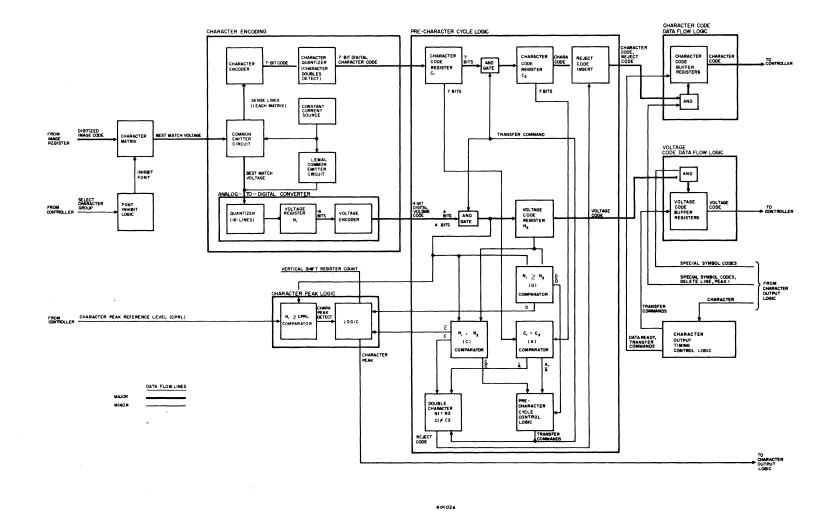


Figure 4-16. Character Matrix to Character Code Data Flow Block Diagram

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When N_1 is equal to or greater than N_2 , a D signal is sent to the character peak logic. When N_1 is equal to N_2 , a C signal is sent to the character peak logic. When N_1 , $D(N_1 \ge N_2)$, and C ($N_1 = N_2$) are present at the character peak logic for three column shifts, a Character Peak signal is sent to the character output logic.

Character codes C_1 and C_2 from the C_1 and C_2 registers are compared in the $C_1 = C_2$ comparator and either an $A(C_1 = C_2)$ or $\overline{A}(C_1 \neq C_2)$ signal is sent to the pre-character cycle control logic. A Transfer Command is generated by the pre-character cycle control logic upon receiving a $\overline{A}(C_1 \neq C_2)$, and a $D(N_1 \ge N_2)$ signal from the respective comparators. The Transfer Command clears the character code register C_2 and voltage code register N_2 and transfers the C_1 and N_1 codes into the appropriate registers.

If $C_1 \neq C_2$, the $C_1 = C_2$ comparator sends a \overline{A} to the double detect logic. If $N_1 = N_2$, the $N_1 = N_2$ comparator sends a \overline{C} signal to the double character detect logic. At the next Transfer Command from the pre-character cycle control logic, the double character detect logic generates a Reject code which inhibits transmission of the character code and instead sends the Reject code to a gate in the character code buffer register.

CHARACTER AND VOLTAGE CODE DATA FLOW LOGIC

The character and voltage code data flow logic serve as first in, first out, (FIFO) buffer memories for the character and voltage codes and special symbol codes, and provide control logic for outputting the codes to the BC. When the character code and a Peak 1 signal from the character output logic are present at the character code data flow logic, the character code is loaded into the first of three buffer registers. A data transfer signal (XFER1, XFER 2, or XFER 3) from the character output timing control logic controls loading each successive character code into the first buffer register. As each new character code enters the first buffer register, it automatically ripples forward. The character codes will continually transfer through each buffer register and then to the BC on receipt of a data transfer signal when Peak 1 and Character codes are present, and the special symbol codes signal is not present.

If a special symbol code signal such as a Field Mark or Space is present, the character code will be inhibited and the symbol code will be sent through the buffer registers.

The voltage code data flow logic operation is the same as described for the character code data flow logic. The voltage code sent to the BC is used only as a diagnostic aid.

CHARACTER TIMING

Character clocking signals are supplied by the oscillator and phase generators logic. The signals enable shifting of character data from the optics system to the character recognition system, correlation of characters, and the output of character codes. Selection of the proper oscillator is by program control. ANSI-OCR-A Size I characters use a 7.8546 MHz oscillator, ANSI-OCR-A Size IV characters use a 5.4001 MHz oscillator, and handprint characters use a 5.9944 MHz oscillator.

The oscillator pulses drive two clock generators: an 8-phase and a 4-phase. The 8-phase generator functions as a ring counter and produces 125-nanosecond clock pulses (T0 through T7) during each vertical shift period (Vnn). The 4-phase generator produces 250-nanosecond clock pulses (C0 through C3) during each vertical shift period.

CLEAR COLUMN LOGIC

A clear column of data is a column that has no adjacent sample points of black data. A clear column is determined by the black algorithm logic, shown on figure 4-11, which samples the top two bits of the load register preceding the line-thickening circuits and the top two bits shifted from the first column of the image register. A Black In Column signal is sent to the clear column logic when any one of the following conditions exist:

- 1. Two consecutive bits of black data in either column.
- 2. Two bits of black data in consecutive columns are horizontally adjacent.
- 3. Two bits of black data in consecutive columns are diagonally adjacent.

When the clear column logic receives the Black In Column signal the first of three flip-flops is set. At the next shift pulse this signal is transferred to the second flip-flop and the first flip-flop is reset. If, during the same shift pulse, a second Black In Column signal is received, the third flip-flop is set and remains set until the black algorithm logic samples two consecutive clear columns.

When the third flip-flop sets, a WHT TO BLK XITION (shite to black transition) signal (indicating the leading edge of a character) is sent to the character centerline logic. When the third flip-flop is cleared, a BLK TO WHT XITION signal (indicating the trailing edge of a character) is sent to the character centerline logic.

When the clear column logic receives a Field Mark 1 signal from the character output logic, the Black in Column signal is disabled and the first flip-flop is set by Unscrubbed Blk Data. When a field mark has been detected, unscrubbed data is sent to clear column logic to start a character cycle. A character cycle must be started to enable reading of a field mark.

CHARACTER CENTERLINE LOGIC

The character centerline logic determines the nominal position of the character in the image register. When the WHT TO BLK XITION signal is received from the clear column logic, a 5-stage counter starts to count one count for each column shift. When the counter reaches a count of 6 or 7, a Pre-Character Enable signal is sent to enable the pre-character cycle logic. This signal eliminates false character images formed by adjacent character strokes; e.g., the area between two characters AA might be recognized as a V. When the counter reaches a count of 14 or 15 and a character peak signal has been generated, the character is considered to be in the center of the image register.

The counter is cleared by one of the following:

- 1. A Chara Cycle Reset signal from the character output logic when a Chara Peak signal has been generated.
- 2. When the trailing edge of one character and the leading edge of a second character have both been detected.
- 3. When a field mark is very close to a character.

- 4. When two characters are touching.
- 5. The cycle was determined to be dirt and not a real character image.

A CCC Inhibit signal from the character output logic will also clear the counter. This signal is generated when black marks bordering a journal tape are being read.

TOPLESS/BOTTOMLESS DATA DETECTION

The topless/bottomless data detection logic monitors character data to determine if the characters are extending above or below the read zone. Topless/bottomless logic looks for horizontal character features extending into the read zone. Topless data requires that the first two bits from the top of the read zone in a column are black and an adjacent column contains a connecting black bit.

Bottomless data has the same requirements as topless data except that the last and next-tolast bits are black.

The Field Mark 1 signal (detection of a field mark) from the character output logic disables the Topless and Bottomless Data signals to the BC.

SPACE GENERATION LOGIC (S/N 120 AND UP)

A character space code is determined when the 8-bit space counter reaches a specific count indicating an interval of clear space has been detected. A detected space signal is sent to read logic. The space counter counts in 0.001-inch increments when clear column data or a character peak is detected and counts by 0.002-inch increments when clear column data or a character peak is not detected.

Space interval selection is preceded by a decoder which allows for space code selection of:

- a count of 100 or 0.100 inch of scan travel for 10 characters per inch
- a count of 125 or 0.125 inch of scan travel for 8 characters per inch
- a count of 143 or 0.143 inch of scan travel for 7 characters per inch

The counter is cleared when either a Read command is generated by the BC, a Space signal is generated (counter reaches a count of 100), when a WHT TO BLK XITION signal is sent from the clear column logic, or when the Delete Line logic has counted three columns of black. The space counter does not start counting until the character centerline counter has reached a count of 14 or 15. Character peak data presets the space counter to fourteen. The space counter is also reset in CJ122 Models E, F, G, H, J, and K by the black noise counter (see BLACK NOISE COUNTER following).

DELETE LINE DETECTION LOGIC

The delete line detection logic counts continuous black columns, makes a determination if a delete line symbol is present, and then either inhibits the character code data flow or resets a counter.

When the black column counter in the delete line detection logic reaches a count of 45, a Detect Delete Line signal is sent to the character output logic, which generates a Delete Line signal to the character code data flow logic. The Delete Line signal inhibits the entry of the character code into the first buffer register. The black column counter increments one count per column when the Gap signal is received from the clear column logic. (The Gap signal is generated after black data is detected in two consecutive columns.) The black column counter will continue to count until either a Read command is generated by the BC, a WAIT flip-flop is set by the Detect Delete Line signal (indicating that a character or field mark could be present in the image register), or a BLK TO WHT XITION signal is received from the clear column logic. If a black to white transition occurs before the black column counter reaches a count of three, a Reset CEC Logic signal is sent to the character center-line logic to reduce the probability of reading dirt as a period which is four columns wide. When the black column counter reaches a count of 3, the space generator logic is reset.

BLACK NOISE COUNTER

In CJ122 Models E, F, G, H, J, and K, C&C reset and space counter reset are controlled by the black noise counter, which counts continuous columns of black at the start of the character cycle. This counter counts either to 3 or 6, producing a CNT 3 or CNT 6 signal, depending on the punctuation font enabled by the BC. The space counter is reset when either of these terms is produced. The C&C counter is reset if the video changes from white to black and back to black before CNT 3 or CNT 6 occurs. The effect is to screen out dirt or any small mark not part of the character.

FIELD MARK DETECTION

A field mark, defined as 23 vertically-connected black bits (or 30 in mark sense mode) is detected by entering unscrubbed data into a 5-bit counter. When the count reaches 23 (10111) or 30 (11110), a latch sequence is initiated that produces an output only when the field mark is no longer detected (counter cleared). This field mark output is held in another latch until read out. At the same time an 8-bit counter is started that inhibits further field mark detection for eight columns.

E13B AND NOF CONTROL LOGIC (CJ122 Models E, F, G, H, J, and K)

When recognition is enabled of E13B or NOF (National Optical Font) characters, certain logic functions must be modified because of the open nature of the characters. The GAP signal, which is high during a character and low between characters, is latched to prevent toggling within an open character. In addition, the CQC reset term, normally bypassed by CNT 3 or CNT 6 from the black noise counter, is further bypassed via an OR gate by two additional terms, field mark count of 4 and the E13B/NOF font enable term. This ensures that the CQC logic will not reset during an open character.

HANDPRINT PRELOOK LOGIC

When the hand<u>print option</u> is installed, the reader examines the character video for possible dirt so that a HPCLR signal is only generated for valid video, i.e., DATA READY generated. The prelook logic counts columns of black data, both horizontally and vertically. The HPCLR signal is received at the end of the black data. The HPCLR signal is allowed to pass to the BC and OLCC if black is sensed in 15 vertical columns or 6 horizontal columns, indicating that a valid handprint character is present.

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SUPPORTING SYSTEMS

The systems which support the document transport system, optics system, and character recognition system are: the vacuum system, the cooling system, the power distribution system, and the maintenance system.

VACUUM SYSTEM

The vacuum system provides vacuum to the document transport system to aid in document hold-down and control. The vacuum system is a low level, high volume system which is a regulated dual system supplying two different vacuum levels. One vacuum source supplies vacuum at 1.5 - 2.0 inches of water and the second vacuum source supplies vacuum at 8 inches of water. The 1.5 - 2.0 inch vacuum source is supplied to the edger vacuum plenum which supplies vacuum for document hold-down and control via the vacuum belts. The 8.0 inch vacuum source also supplies vacuum to the conveyor dc servo motor for cooling. The 8-inch vacuum source also supplies vacuum to the conveyor and stacker vacuum plenums, which supply vacuum for document hold-down via vacuum belts.

COOLING SYSTEM

The cooling system provides cooling air to maintain an internal operating temperature of less than 125° F. The cooling system is divided into three basic groups: external air intakes, internal air directors, and special cooling.

External Air Intakes

External air intakes ensure that only dust-free air enters the reader and BC. Air is drawn through filters located at the bottom of the reader and BC. Three fans are located on the bottom panel of the reader. In CJ122 Models C, D, F, and J, two fans are located on the bottom of the BC rack door, and two fans are located on the bottom of the BC power supplies. In CJ122 Models E, G, H, and K, three fans are located under the BC. The slight pressure difference induced by the fans minimizes the infiltration of dirt and dust through panel openings, etc.

The main reader air flow direction is for air to enter the bottom and be exhausted at the top of the reader cabinet. Air flow for the BC is for air to enter the bottom and be exhausted at the rear and right side of the BC cabinet.

Internal Air Directors

The internal air directors are a group of fans which provide a high volume of cooling air flow over units with high heat dissipation. The number and location of fans used for this purpose are:

- 3 fans in recognition rack (Mod C);
- 4 fans in recognition rack Mods D, E, F, G, H, J, and K)
- 1 fan in servo amplifier unit

- 2 fans in top of BC rack (CJ122 Mods C, D, F, and J)
- 1 fan in top right side of BC cabinet (exhaust fan)

Special Cooling

The special cooling system cools the read area and the conveyor dc servo drive motor. Two fans over the read area prevent a large temperature rise in the read and scanning areas. The fan draws air from the read area and exhausts the air at the top of the scan cover housing.

The conveyor dc servo drive motor is cooled by an air flow of 8.0 inches of water drawn through the motor housing by the vacuum system and exhausted at the lower rear of the reader cabinet.

POWER DISTRIBUTION SYSTEM

The power distribution system for the reader and BC is divided into an ac power control and distribution system and a dc power supply, control, and distribution system. The power system is housed in both the reader main frame and the BC frame. Power supply characteristics are listed in section 1 and the functions of the controls and indicators of the power control unit and power supplies are listed in section 2.

A block diagram of the ac power distribution system is shown in figure 4-17.

Power Control Panel

The Power Control Panel receives primary power through internally mounted line filters and distributes it through circuit breakers to the connections that are used to power the various other power supplies in the reader and BC.

Transport Servo Supply

The transport servo supply receives 208 vac, 3-phase input power from the power control panel and converts it to ± 45 vdc.

A Power Supply

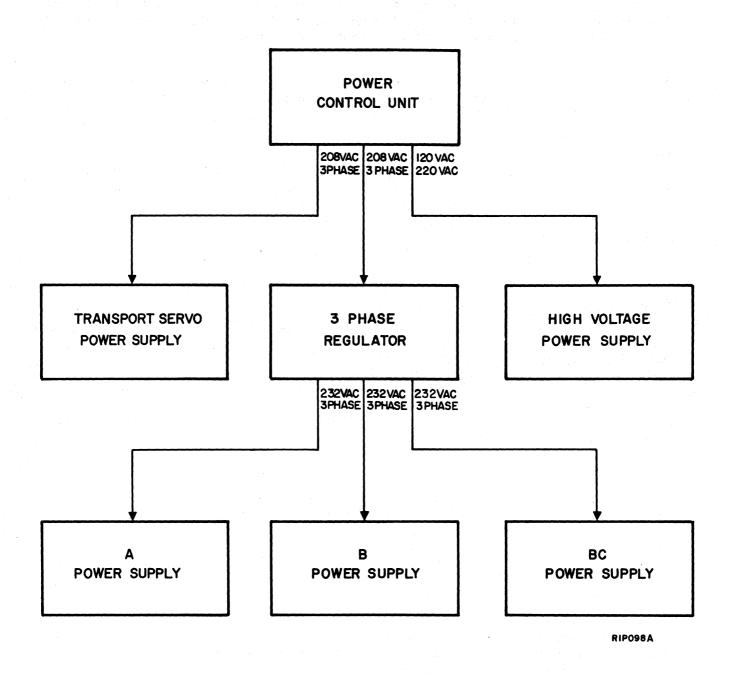
The A supply receives 32 vac, 3-phase regulated power from the 3-phase ac regulator. The regulated ac is connected to 3-phase stepdown transformers which supply ac power to 3-phase rectifier units. The outputs from the different full-wave rectifier units is filtered and produces the following dc voltages: $+5V^{\dagger}$, $\pm 15V^{\dagger}$, $\pm 12V$, and $\pm 10V$. The A supply also furnishes adjustable 120 vac for the read lamp, or to a dc read lamp power supply when hand-print (option) is installed.

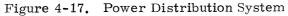
B Power Supply

The B supply receives 32 vac, 3-phase regulated power from the 3-phase ac regulator. The regulated ac is connected to a 3-phase stepdown transformer. The outputs from the transformer are full-wave rectified and filtered to produce ± 20 vdc.

[†]Adjustable on CJ122 Models F, G, H, and J.

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High Voltage Power Supply

The high voltage power supply receives 120 vac from the power control panel and converts it to nominal -1500 vdc. This voltage is adjustable.

BC Power Supply (CJ122 Models C, D, F, and J)

The BC power supply receives 232 vac, 3-phase regulated power from the 3-phase ac regulator. The dc output voltages from the power supply are -2V, $\pm 6V$, +8V, and +16V.

BC Power Supply (CJ122 Models E, G, H, and K)

The BC power supply receives 232 vac 3-phase square wave regulated power from the regulator. The dc output voltages from the power supply are +30 vdc, ± 6 vdc, and ± 5 vdc.

Three-Phase Regulator

The 3-phase regulator receives 208 vac from the power control panel and changes the voltage to a regulated, 32 vac output for use in the A supply, B supply, and the BC power supply.

MAINTENANCE SYSTEM

The maintenance system aids in rapid system setup, testing, and fault isolation. The system can be used to monitor voltages and signals within the reader and BC. Fault indicators are provided to indicate both controlware and hardware faults. Controlware and system diagnostics supplement the maintenance features.

A preventive maintenance index, preventive maintenance procedures, corrective maintenance procedures, and troubleshooting procedures are in section 6.

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SECTION 6

MAINTENANCE

GENERAL

The reader is designed to provide continuous performance for a period of 15,000 hours before refurbishment if a conscientious program of preventive and corrective maintenance is followed. Accurate records of all maintenance must be kept if the maintenance program is to be effective. The reader requires a minimum of preventive maintenance; therefore, unscheduled maintenance should not be performed if the reader is operating satisfactorily.

This section contains information on special tools and test equipment for the reader. A preventive maintenance schedule, troubleshooting procedures, repair and replacement procedures, and alignment and calibration procedures are also contained in this section. Schematic diagrams, which can be used as reference material when performing the troubleshooting procedures, are presented in volume 2.

ON-LINE CHARACTER CORRECTION UNIT (OLCC)

Maintenance information, servicing instructions, and adjustment procedures for the display monitor are contained in this manual and in the Tektronix 603/604 Monitor Instruction Manual supplied with the OLCC. The display monitor is warranted against defective materials and workmanship for 15 months. Any maintenance required during this warranty period should be performed by the nearest Tektronix representative. Arrangements may be made with Tektronix for repairs after the warranty expires.

No preventive maintenance is required for the OLCC. Adjustments and unscheduled maintenance are required only when necessary (see tables 6-53 through 6-55).

SPECIAL TOOLS

Special tools needed to maintain the reader are listed in Table 6-1 and those for the buffer controllers are listed in tables 6-2 and 6-3.

TEST EQUIPMENT

The following test equipments, or equivalents, are used to maintain the reader:

Digital Voltmeter	-	Fairchild 7050, (CDC Part No. 18697518)
Maintenance Console, Buffer Controller	-	TF201 or TF204
Oscilloscope	-	Tektronix 543 with dual-trace preampli- fier, or Hewlett-Packard 180
Volt-Ohmmeter	-	Simpson 260, Series 5 Not to be used for measurements above 1000 vdc.
Diagnostic Tape	-	BC mirror engineering diagnostic punched paper tape and program listing or SMM17 diagnostic tape
	-	955 transport engineering diagnostic punched paper tape and program listing
Steel Rule	-	12-inch with 0.01-inch graduations

TABLE 6-1. SPECIAL TOOLS FOR READER

Part No.	Description	Quantity	Part No.	Description	Quantity
12210436	SOLDER SUCKER	1	12259135	COMPARATOR W/O RETICLE	0
12210851†	GUN, WIRE WRAP, MANUAL	1	12259136*	RETICLE, OCR SIZE I	0
12212196	EXTRACTOR AND TEST PROBE,		12259137 †	RETICLE, OCR SIZE IV	0
12212885	INTEGRATED CIRCUIT TIP, SCOPE PROBE, FLEX LEAD	2 3	12259138 †	RETICLE, MULTIPLE REGIS- TRATION	0
12212886 12218402 [†]	TIP, SCOPE PROBE, GROUND BIT, WIRE WRAP, 30 GAUGE	, 3 1	20258200	INTEGRATED CIRCUIT DESOLDERING TIP	1
12218402 12218403†		1	48385300	EXTENDER, PC CARD, 80 PIN	2
12259183	UNWRAP TOOL, LH AND RH	- 1	48446100 †	WIRE STRIPPER W/26, 28 AND 30 GAUGE HEAD	1
12218462 12218463	TISSUES, LINT FREE (500) SWABS, LINT FREE (500)	1	48446200*	WIRE STRIPPER HEAD, 30 GAUGE ONLY	1
12218477	PLUG, INTEGRATED CIRCUIT ADAPTOR/EXTENDER	3	48777400	EXTENDER, MIRROR AND XPORT. ELECTRONICS	1
12254026	TIP, SCOPE PROBE	3	86386900	HAND WIRE WRAP TOOL, 30	
12259111 [†]	GUN, WIRE WRAP, BATTERY POWERED	0		GAUGE	1

TABLE 6-2. SPECIAL TOOLS FOR BUFFER CONTROLLER (CJ122 MODELS C, D, F, AND J)

Part No.	Description	Quantity	Part No.	Description	Quantity
12206342	BACK PANEL WIRE SPREADER	1	12218452	SOLDERING IRON, 6W	1
12210275	TWEEZER, FINE POINT	1	12218453	SOLDERING IRON TIP	1
12210781†	CRIMPING TOOL (BUCHANAN)	0	18072300	EXTENDER, CORDWOOD	
12210897†	INSERT POSITIONER	0		MODULE	2
12210988	PIN REMOVAL TOOL (61 PIN)	1	10247400	EXTENDER, CARD, 50 PAK	2
12211810	WIRE CADDY, W/O WIRE	1	18672000	ADAPTER, SCOPE PROBE, 50 PAK	3
12213235	INSERTION TOOL, GROUND PIN	1	18934700	EXTRACTION TOOL (RECEP-	
12213236	PUNCH, GROUND PIN	1		TACLE)	1
12213237	INSERTION TOOL, WIRE SIDE OF PLATE	1	20258200	INTEGRATED CIRCUIT DESOLDERING TIP	1

* NOT SUPPLIED WITH INITIAL SPARE PARTS. MUST BE ORDERED SEPARATELY, AS REQUIRED.

TABLE 6-3. SPECIAL TOOLS FOR BUFFER CONTROLLER (CJ122 MODELS E, G, H, AND K)

Part No.	Description	Quantity	Part No.	Description	Quantity
12218402*	WIRE WRAP BIT, 30 GAUGE	0	48446200*	WIRE STRIPPER HEAD, 26-30	
12218403:*	WIRE WRAP SLEEVE, 28-30 GAUGE	0		GAUGE	0
12259111 *	WIRE WRAP GUN, BATTERY POWERED	0	53093400	PIN REMOVAL TOOL, PLASTIC BLOCK	1
12259183 *	WIRE UNWRAP TOOL, 28-30		53561800	SOLDER REMOVAL TOOL	1
	GAUGE, L/R	0	53665802	EXTENDER BOARD, 62 Pin, TTL	1
18668500 48446100 †	CONNECTOR, PUSH-ON WIRE STRIPPER, (IDEAL), 26-30	10	59309500 †	MAINTENANCE CONSOLE CONVERSION KIT, TTL	0
10110100	GAUGE	0			
NOT SUPPLIED WITH INITIAL SPARE PARTS. MUST BE ORDERED SEPARATELY, AS REQUIRED.					

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PREVENTIVE MAINTENANCE

The required preventive maintenance schedule is listed in table 6-4. The schedule is based on a calendar period or operating hours (whichever comes first). A reader ELAPSED TIME meter is located on the front of the Power Input Control module and indicates the total time that the READER POWER ON switch is activated.

The Preventive Maintenance Index (PMI), table 6-4, is divided into four columns. The Page column indicates the page on which the preventive maintenance procedure (PMP) is found. The PMP column indicates the level of maintenance by the first digit. The second digit is the number assigned to the procedure. The Title of Procedure column indicates the specific procedure to be performed.

Inspection Procedures

Visually inspect the reader as follows:

- 1. Inspect console for scratches, dents, cracks, or other damage.
- 2. Inspect all mounted parts for tightness. Retighten any loose screws or parts or replace as required.
- 3. Inspect wiring and cabling for broken strands and wires, cracked or brittle insulation and illegible or incomplete markers. Replace or correct discrepancies.
- 4. Inspect electrical components for cracks, charred or burned parts, corrosion, or other damages. Replace damaged components.

Cleaning Procedures

WARNING

There must be no smoking or open flames within the area in which solvents are used for cleaning purposes. Prolonged breathing of vapors should be avoided.

To clean the reader, proceed as follows:

- 1. Clean exposed surfaces and recessed areas.
- 2. Using a lint-free cloth dipped in solvent (trichlorethylene or isopropyl alcohol), wipe all interior and exterior surfaces to remove any accumulated deposits of dust, corrosion, or contaminants.

NOTE

The following PMI lists the recommended frequency of performing preventive maintenance on the reader. Scheduling of the preventive maintenance is a site responsibility. Scheduling may include variations in the recommended frequency due to individual site conditions (e.g., usage, environment, time, etc.).

TABLE 6-4. PREVENTIVE MAINTENANCE INDEX

	Level 2 Level 3 Level 4	A One week or 110 hours [†] 2 One month or 440 hours [†] 3 Quarterly or 1320 hours [†] 4 Semiannually or 2640 hours [†] 5 Annually or 5280 hours [†]
Page	PMP	Title of Procedure
6-5	1.1	Vacuum Reader
6-7	1.2	Clean Feed and Dedoubler Rollers
6-9	1.3	Clean Takeaway Area
6-11	1.4	Clean Paper Advance Belts
6-13	1.5	Clean Air Filters
6-15	1.6	Check Vacuum Levels
6-17	1.7	RX-1 System Test
6-19	1.8	Transport Control Test
6-21	1.9	Line Scanning System Mirror Control System Alignment Test
6-23	1.10	Six Lines Per Inch System Test
6-41	1.11	Clean Optics
6-43	2.1	Check Feed, Dedoubler, and Pre-Feed Rollers
6-45	2.2	Replace Sun Gun Lamp
6-47	2.3	Check PM Head and Optics
6-52A	2. 3A	Check Video Quantize Level (CJ122 Models E, F, G, H, J, and K)
6-53	2.4	Check for Loose Setscrews
6-55	2.5	Check Pre-Feed Roller
6-57	2.6	Rotate Mirror Drive Motor (S/N 100 and Up)
6-61	2.7	Check Vacuum Motor Brushes
6-63	2.8	Read Zone Sensor Alignment Test
6-65	2.9	RX-3 System Test
6-67	2.10	RX-4 System Test
6-69	2.11	BC2 Buffer Controller Test
6-71	3.1	Check Mirror Alignment
6-73	3.2	Check Constant Current, LEMAL, Lower A/D Converter, and Character Quantizer Reference Voltage
6-75	3.3	Clean Vacuum Holes
6-77	3.4	Check Belt Tensions
6-79	4.1	Check Power Supply Voltages (CJ122 Models C,
		D, F, and J)
6-83	4.2	Check Power Supply Voltages (CJ122 Models E, G, H, and K)
†Total	hours as	indicated by maintenance meter.

1.1 Vacuum Reader

1. Deenergize reader.

- 2. Remove front and rear panels on reader and buffer controller.
- 3. Vacuum interior, including timing belts.
- 4. Vacuum fan above read area.
- 5. Vacuum surface of feedup table, edger, and conveyor.

CAUTION

Use extreme care when cleaning the optics area. Do not touch mirrors or lens with vacuum attachment as scratches on the optics will impair character recognition.

6. Vacuum optics area.

6-5/6-6

1.2 Clean Feed and Dedoubler Rollers

- 1. Energize reader and load controlware.
- 2. Remove feeder cover.
- 3. Dampen cheese cloth slightly with isopropyl alcohol.

WARNING

Be careful that cloth does not become wrapped around roller or shaft, or fingers may be pulled into roller.

4. Hold cloth against rollers and press LOAD pushbutton indicator on control panel.



1.3 Clean Takeaway Area

1. Deenergize reader.

2. Turn off takeaway motor circuit breaker on POWER CONTROL panel.

3. Open left panel door and stacker panel door.

CAUTION

The turnaround guide assembly will spring back (under spring tension) when the knob is loosened.

4. Loosen knob under takeaway area and allow turnaround guide assembly to slide away from drum.

5. Dampen cheese cloth slightly with trichloroethane or isopropyl alcohol.

6. Remove dirt from drum, turnaround guide and belt, belt rollers, and takeaway vacuum belt.

6-9/6-10

1.4 Clean Vacuum Belts

1. Deenergize reader.

2. Ensure that takeaway area is in same condition as in PMP 1.3.

3. Dampen cheese cloth with trichloroethane or isopropyl alcohol.

4. Remove dirt from all vacuum belts.



1.5 Clean Air Filters

To filter the cooling air, three filters are provided - one below the buffer controller power supply and regulator, one below the buffer controller, and one below the high voltage power supply.

- 1. Deenergize reader.
- 2. Remove rear panels.
- 3. Slide out filters.
- 4. If filter is not extremely dirty, clean with a vacuum cleaner. Otherwise, wash gently in a detergent-water solution. Hold filter vertically to prevent damaging it. Do not use a high-pressure spray.
- 5. Coat filter with filter fluid (CDC Part No. 12210958).
- 6. Reinstall filter and check all cooling fans for normal operation.

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1.6 Check Vacuum Levels

Vacuum pressure gauges are located at the rear of the reader under the recognition rack. One gauge should indicate 1.5 to 2.0 inches of vacuum and the other gauge should indicate 8 inches of vacuum unloaded. Load document reading on gauge should stay within tolerance. Refer to table 6-41, Vacuum Level Calibration Procedure, if indicators are not correct.

3

2/

6 - 15/6 - 16

1.7 RX-1 System Test

The RX-1 system test is the primary preventive maintenance test used to determine system operability. The following equipment is used in running RX-1:

1700 Computer or SC1700 System Controller with at least 8K memory 608 or 609 Magnetic Tape Transport 1711 or 1713 Teletypewriter (TTY)

RX-1 interfaces with the 1700 System Maintenance Monitor (SMM17) only for the purpose of loading RX-1. Once loaded, the RX-1 monitor assumes complete control. Refer to SMM17 System Maintenance Monitor, Pub. No. 60182000, for loading and operation.

Run selected test documents to verify reading reliability of all available fonts while varying QL (quantize level) from 50 to D0. The lower quantize level will check for weak lightpipes or photomultipliers. If errors occur, refer to table 6-16.

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1.8 Transport Control Test

NOTE

This PMP must be performed with transport stopped.

- 1. Connect DVM to TP-W of the transport control electronic board. Verify the DVM reading is between ±50 mv.
- 2. Connect DVM to TP-D. Verify that velocity command is between ±50 mv.
- 3. Connect DVM to summing amplifier section TP-J. Verify that output is 0 vdc.
- 4. Disconnect DVM and proceed to table 6-51 if readings are incorrect.

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6-19/6-20

1.9 Line Scanning System/Mirror Control System Alignment Check

- 1. Force MNZV to logic 0 by grounding TP-A on mirror electronics board.
- 2. Connect DVM to power amplifier TP-B, and verify reading is 0 ± 50 mv (with MNZV =0, the power amplifier output voltage can easily drift ± 0.5 V in a relatively short time). The output voltage will vary randomly, but this is normal. If reading is outside this range, adjust offset potentiometer R 37 on mirror electronics board.
- 3. Remove ground from TP-A. Adjust R07 on the power amplifier and R37 on the mirror electronics board for 0V±50 mv at TP-B on the power amplifier.
- 4. Proceed to table 6-52 if 0 vdc cannot be obtained in steps 2 and 3.



1.10 Six-Lines-Per-Inch System Test

NOTE

Steps 1 through 6 should be used for new installations only; otherwise, proceed to step 7.

PRELIMINARY CHECKS

- 1. Check mating of all cables on logic doors 1 and 2 for tightness and proper connections.
- 2. Check all ground and power connections on both doors and all logic panels for proper hardware and tightness.
- 3. On the 6-inch panel, check with a VOM for shorts between +5 vdc, -15 vdc, and -12 vdc, also for shorts to either frame or ground.
- 4. Reset all circuit breakers after connecting main power to cord to proper supply. Power up the BC and reader.
- 5. Verify all voltages on the logic doors at proper levels. Verify $-12 \text{ vdc } \pm 0.6 \text{ V}$ on the zener circuit of board 0.
- 6. Record all logic voltages on proper forms for future reference.
- 7. Load RX3 (refer to SMM17 reference manual, Pub. No. 60182000).
- 8. Mount SMM17 auxiliary tape on tape unit 1.
- 9. Select Module 1 by making the following entries at the teletype (* =Buffer Controller equipment code):

SM* = 1	(Select Module 1)
AP*	(Automatic Parameters)
AL* = H	(Load Module 1)

10. Perform quick look of 6/inch fonts as follows (refer to SMM17 reference manual, test RX3, for description of 6/inch fonts):

RE* = 200	(Repetitions = 200)
QL* = UP1 - BOTLESS	(Font Select)

11. If error printouts occur, proceed to step 12; otherwise, test is complete.

1.10 Six-Lines-Per-Inch System Test (Cont'd)

INTERFACE CHECKOUT

12. The following boards must be checked for the proper signals between the basic reader logic doors and the option panel. No program is necessary for this; simply verify that the signal is present at both points.

4A 28-06	2E19-05	Load Register Transfer
4D12-13	0 + F18 - 06	V53
4E12-10	0 + F18 - 11	V58
4E12-12	0 [,] C08-09	V59
4E12-08	0 D11-08	V57
4E12-06	0 C08-03	V56
4D03-01	0 + 16 - 08	V09
4E12-04	0D12-02	V55
4E12-02	0D12-04	V54
4D12-02	0D14-03	V00
4D12-04	0D14-01	<u>V01</u>
4C15-03	0D12-06	TO
4C15-06	0D13-12	T1
4C16-02	0D13-10	Τ2
4C16-06	0D13-13	Τ3
4C17-02	0D13-06	Τ4
4C17-06	0D13-04	Т5
4C18-02	0D13-02	Т6
4C18-06	0D12-12	Τ7

Vertical Column Counter

4E22-02	2S04-44	<u>VC25</u>
$4 \pm 22 - 01$	0F09-02	$\overline{\mathrm{V}\mathrm{C}2^5}$
	0F20-02	
	0F25-04	
4E22-04	2S04-42	VC24
, -	0B16-09	
	0B17-09	
4E22-06	2S04-37	$VC2^3$
	0B16-10	
	0B17-10	
4E22-08	2S04 - 27	$\rm VC2^2$
	0B16-11	
	0B17-11	
4E22 - 10	2S04-55	$VC2^{1}$
	0B16-12	
	0B17-12	
4E22-12	2S04-53	$VC2^{0}$
	0B16-13	
	0B17-13	

VERTICAL COUNT DECODES

- 13. Connect oscilloscope probe to board 4E08 pin 08 (sync negative) and verify ($\overline{V22}$).
- 14. Move oscilloscope to board 2A28-8 and verify $(\overline{V25})$, and compare all waveforms with figure 6-1.
- 15. Verify that both pulses in steps 13 and 14 are of the same width and occur only once per column.
- 16. Verify that the same signals are present at the following locations:

Board 2A27 pin 08	Board 0E27 pin 01 (S/N 116 and 118 only)
Board 2A28 pin 08	Board 0E27 pin 03

17. With the Journal Tape option also installed, the following pair of points will toggle to a logic 1 when JOURNAL TAPE switch is pressed on operator's control panel. With the option not installed the signal will remain a logic 0.

	Board 3D24 pin 11	Board 0F18 pin	12
--	-------------------	----------------	----

18. Load RX3 Module 4 (mirror test) with the following parameters and execute (any coordinates may be used).

SM* =4	(Select Module 4)
AP*	(Automatic Parameters)
AL* =H	(Load Module 4)
SD*	(Suppress Data)

The following points will toggle to a logical 0 on each forward scan of the mirror.

Board 0F22 pin 04 Board 0F23 pin 10

19. Load RX3 Module 1 (electronic read test). Define data as follows:

SM* =1	(Select Module 1)
AP*	(Automatic Parameters
AL* = H	(Load Module)
DF* =ANSI MEDIUM	(Define Font)
DD* =E, E, , , ,	(Define Data)
SD*	(Suppress Data)

20. With oscilloscope verify that the following points have the same signal:

Board	Pin	Board	Pin	Function
4D24	03	0D16	12	White-to-black transition
5A12	11	0D11	01	Read
4C30	09	0C08	01	Read reset
2B07	06	4A11	09	Scrub count
2A07	06	4A23	02	Serial data

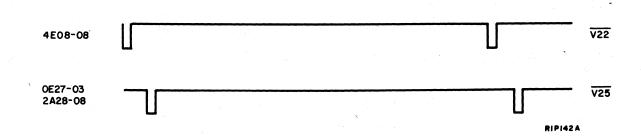


Figure 6-1. Vertical Count Decode Waveforms

SCAN 2 SELECT

21. Load the following into the BC and run:

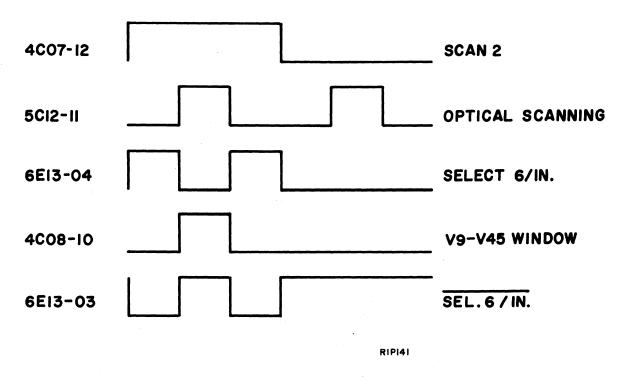
P	INST	$\mathbf{x}_{i} = \left\{ \mathbf{x}_{i} \in \mathbf{X} : i \in [1, \dots, n] \right\}$
0000	0A5F	Set Scan 2
0001	0A57	Set Optical Scaling
0003	0B5F	Clear Scan 2
0004	0A57	Set Optical Scaling
0005	0 B57	Clear Optical Scaling
0006	BF06	Jump Back 6

Scan 2 from BC will select six-lines-per-inch window unless optical scaling is also selected. If this situation occurs, window will be from V09 to V45 and not a tracking window as is 6/inch.

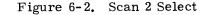
- 22. Synchronize oscilloscope (+) and connect probe to board 4C07-12 and verify proper waveform (see figure 6-2). Move probe to remaining test points to verify proper operation.
- 23. Verify with oscilloscope that the following locations have the signals indicated:

Select Six Lines per Inch 6E13-04 2A06-01 2E20-10 0F14-04 Select Six Lines per Inch 6E13-03 2A06-04 2E20-13 0F14-03

24. Synchronize oscilloscope as required to verify the proper waveform, as shown on figure 6-3 for clock driver network (see sheet 4 of logic diagrams, Pub. No. 48430045).



1.10 Six-Lines-Per-Inch System Test (Cont'd)



25. Enter parameters as follows:

RP* CHAR PITCH =7 FONT ENABLE = ANSI MEDIUM FONT ENABLE = ANSI =0123456F CHAR PEAK =12 IP* =C DD* =E, E, , , , SD*

- 26. Synchronize oscilloscope channel 1 (+), set at TIME BASE B and connect on V00 board 0D12 pin 10.
- 27. Synchronize oscilloscope channel 2 (+), set at TIME BASE A and connect on read board 0D11 pin 2.
- 28. Couple TIME BASE B into input of TIME BASE A. Blank video with probe connected to board 0C08 pin 11.

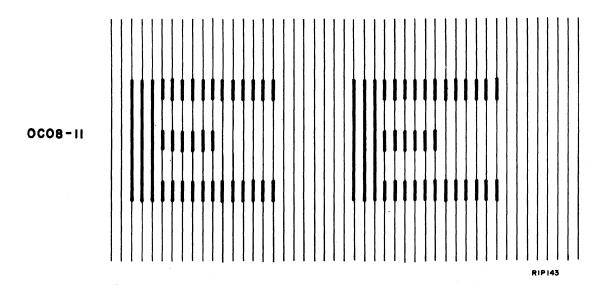
48430080 C

6 - 27

0F13-05	η	V54
0F13-01	Ω	V58
0F13-06	Г	V54.T6
0F13-03		V58.T6
0F13-08 0F11-01		
0F12-02		TI
0F11-02		T5
0D07-06 0D07-08		PROFILE AND BUFFER CLOCK 56 POSITIVE PULSES 500NS. DURATION TI TO T5 TIME

Figure 6-3. Clock Driver Network Waveforms

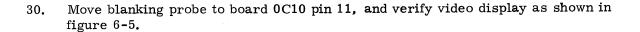
48430080 C



1.10 Six-Lines-Per-Inch System Test (Cont'd)

Adjust oscilloscope controls as required for video display as shown on figure 6-4.

Figure 6-4. Serial Data Input Six-Lines-Per-Inch Logic



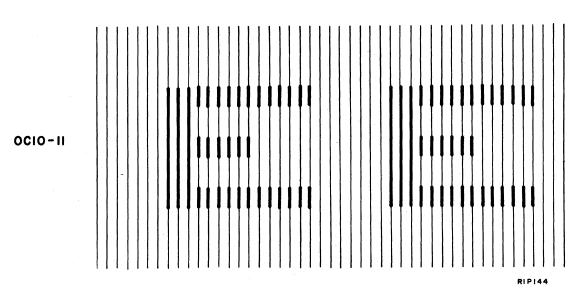


Figure 6-5. Serial Data Out of 5-Column Accumulator

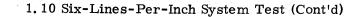
48430080 C

5.

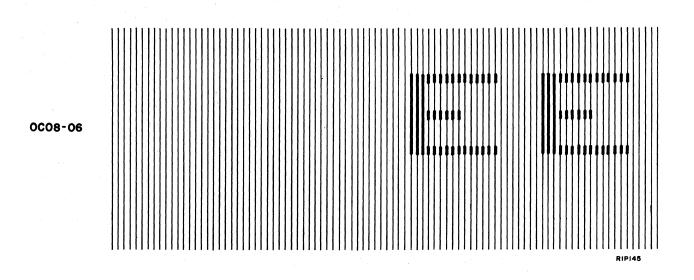
A Contraction

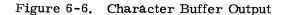
29.

.



31. Move blanking probe to board 0C08 pin 06, and verify video display as shown in figure 6-6.





32. Move blanking probe to board 0F14 pin 06, and verify video display as shown in figure 6-7.

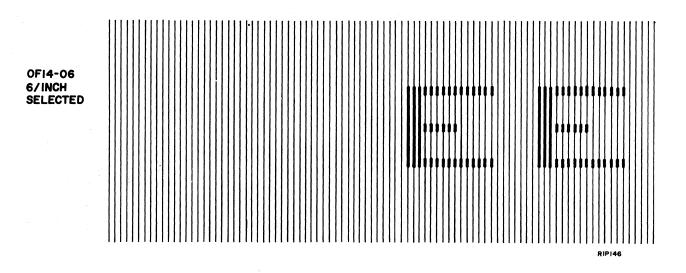


Figure 6-7. Scan 2/3 Video Test Point

1.10 Six-Lines-Per-Inch System Test (Cont'd)

33. If no printout occurs, the unit is basically reading. If printout occurs, manually interrupt the TTY and perform the following:

Enter parameter SD*

CAUTION

Do not type ET* (error total request) while operating in suppressed mode (SD*). Destruction of RX3 (1700 Resident) will result.

- 34. You may now trouble shoot serial data flow if any of the waveforms in figures 6-1 through 6-7 were in error. (The windowing of board 0F14, pin 6 is of no concern at this time.)
- 35. Manually interrupt RX3 and enter parameters as follows:

IP^{*}	=C
DF*	=ANSI MEDIUM
DD*	=E, E, , , ,
SD*	

36. Move oscilloscope blanking probe to board 0A06, pin 06 (filtered data).

NOTE

The data will appear slightly rounded on the corners as compared to data from board 0C10, pin 11. This is due to the dirt algorithm and is normal.

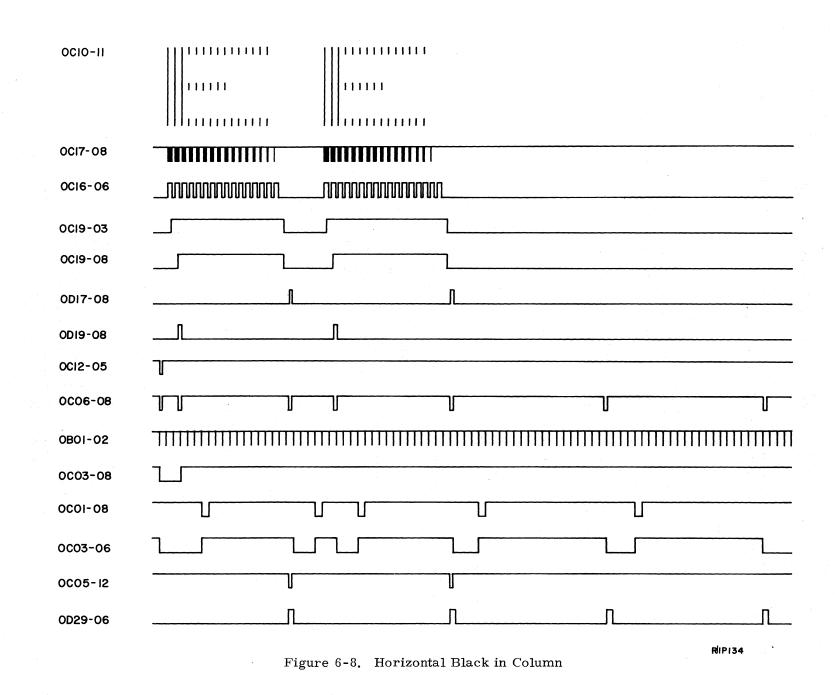
- 37. Refer to sheet 9 of logic diagrams and figure 6-8 to verify that all timing is correct.
- 38. To observe the profile with respect to the video, add a test chip type 74 (SN7400J) or equivalent Part No. 94918809) to an unused 14-pin IC socket.
- 39. Add the following test jumpers and blank the scope with pin 6:

0B21-09 to pin 1 0C04-08 to pin 2 pin 3 to pin 5

NOTE

Verify appearance of a thin vertical line one column thick after the character. This line must be as high as the highest and lowest points of the character. Any other full height characters may be used (except field marks) simply by defining them on TTY.

48430080 C



6-32

48430080 C

5.2

8 9

S. 9

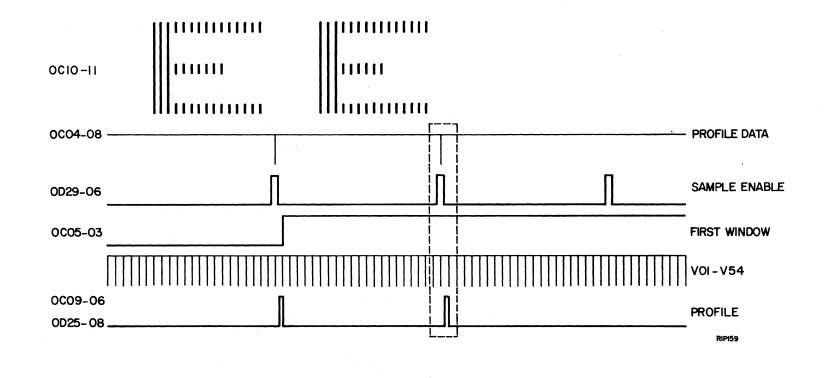
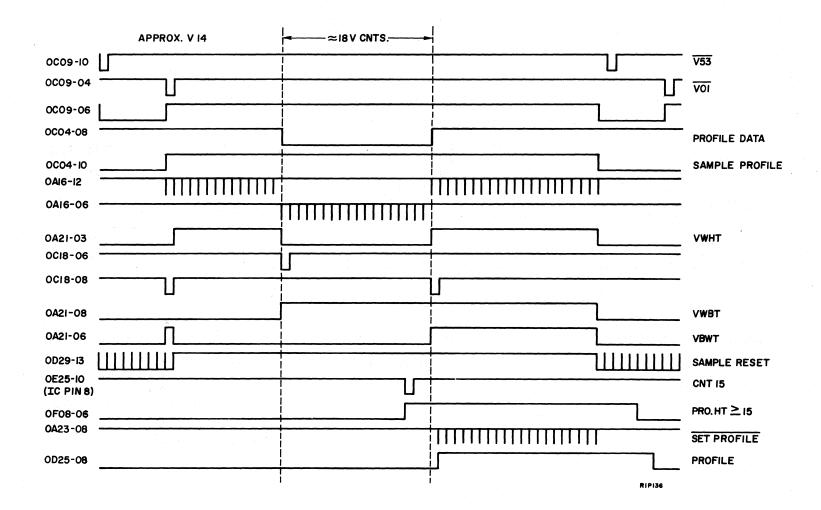
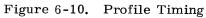


Figure 6-9. Profile Timing





1. 10 Six-Lines-Per-Inch System Test (Cont'd)

- 40. Remove all jumpers and test chip added in steps 38 and 39.
- 41. Define data as E, E, Space, Space, Space, and suppress data (only if you changed it). Refer to logic diagrams sheets 13 through 17 and figures 6-9 and 6-10 to verify proper operation. Figure 6-10 is an expanded view of figure 6-9.
- 42. Manually interrupt RX3. Load and execute UP1 font as follows:

DF* =UP1 LF* SD*

- 43. Verify waveforms shown in figure 6-11.
- 44. Manually interrupt RX3. Load and execute WAVE font as follows:

DF* =WAVE LF* SD*

This font causes the test image to shift up and down as a test of window tracking.

- 45. Use figures 6-12 through 6-14 with the above data pattern. Examine the window logic on sheets 19 and 21 of logic diagrams for proper operation.
- 46. Verify the windowed video tracks the entire line of data and does not chop any of it off.

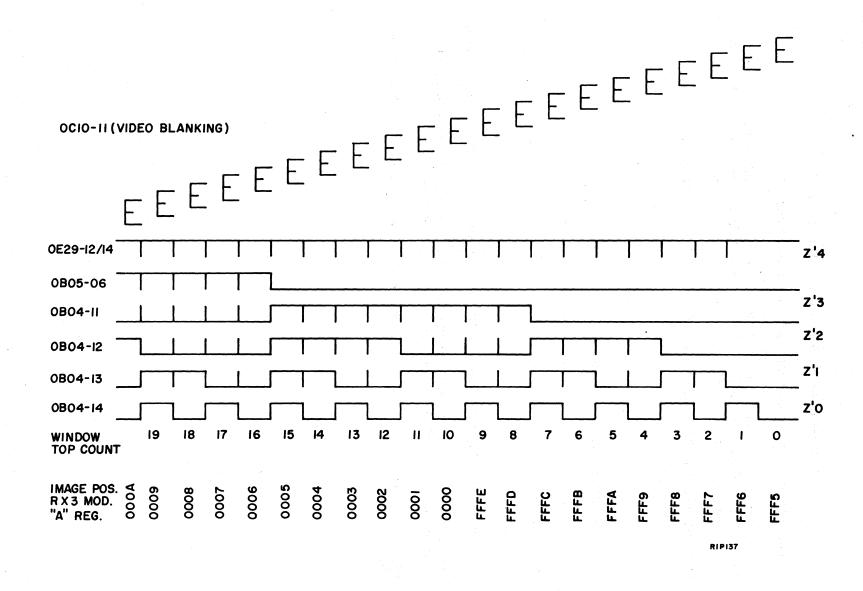


Figure 6-11. Top Window Counter Waveforms

48430080 C

6-36

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1.00

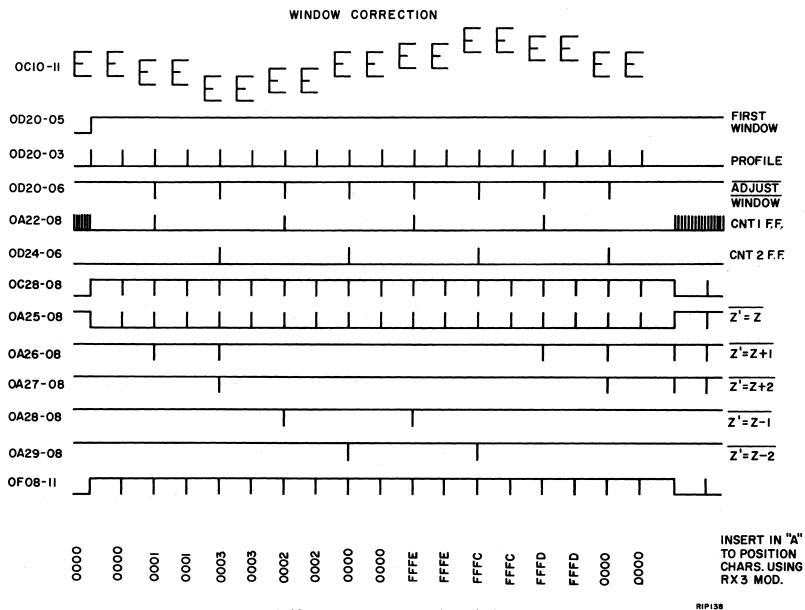
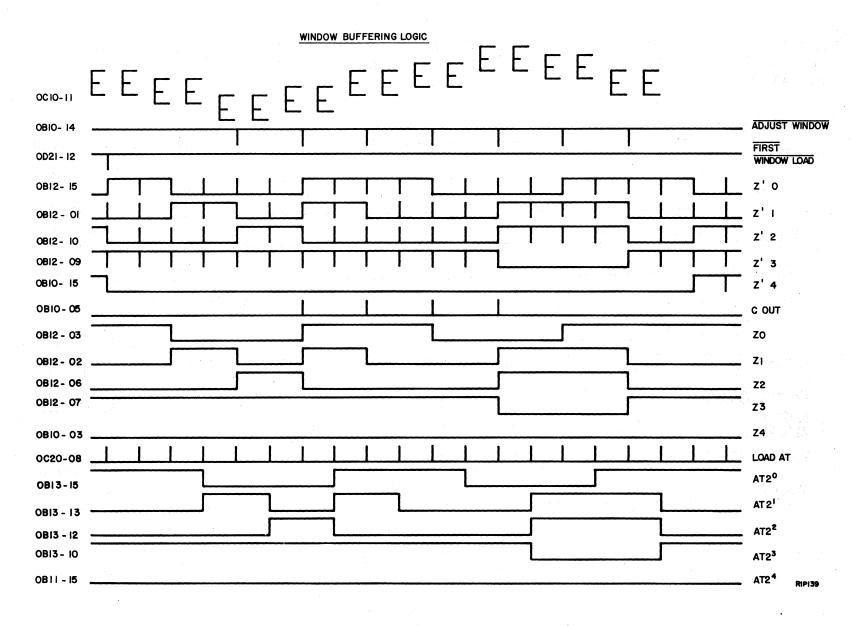


Figure 6-12. Window Correction Timing Diagram

6-37





6-38

48430080 C

·····EEEEEEEEEEEEEEEEEEE SAMPLE WINDOW RESET LOGIC 0F12-04 READ 0F12-08 **BUFFER CLEAR** READ RESET 0E17-01 Z CNT 20 OEI9 - 03 Z CNT 2 OE19 - 02 Z CNT 22 **OEI9 - 06** Z CNT 23 OE19-07 Z CNT 24 0E20-03 RIPI40

48430080 C



Figure 6-14. Sample Window Reset Logic Waveforms

S.



1.11 Clean Optics

1. Deenergize reader.

- 2. Lift left and center hoods.
- 3. Brush dust off lens, scanning mirror, and sun gun reflector using camel's hair brush.
- 4.

CAUTION

Do not touch quartz surface of sun gun lamp with bare fingers or lamp may fail prematurely due to contamination.

If dirt or smudges are on lens, mirror, or sun gun reflector, wipe clean with Texwipe lens cleaning paper dampened slightly with Kodak lens cleaner.

2.1 Check Feed, Dedoubler, and Pre-feed Rollers

- 1. Visually inspect the feed and dedoubler rollers for abrasion, rounding of edges and other signs of wear, figure 6-15. Refer to table 6-26 for feed roller replacement or to table 6-27 for dedoubler roller replacement.
- 2. Check that the dedoubler rollers are above the stationary ramp, but below the spring fingers.

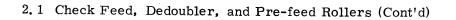
NOTE

The document must contact the feed rollers before contacting the dedoubler rollers for proper dedoubling action. If the dedoubler rollers are set below the stationary ramp (less than 0.000 inch) the documents will crease.

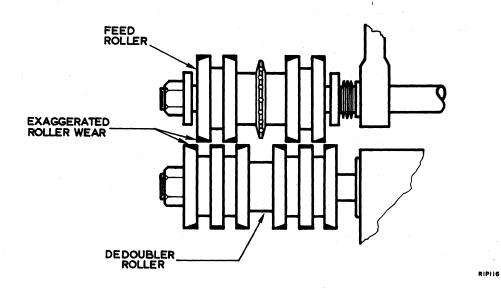
If the dedoubler roller adjustment is not as described above, perform stationary ramp adjustment procedures in table 6-39.

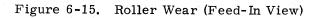
- 3. Check the parallelism between the feed and dedoubler rollers as follows:
 - a. Insert narrow piece (above 2 inches) of paper between feed and dedoubler rollers on one side of sprocket. Press spring fingers to keep paper from touching fingers.
 - b. Note feel of snugness.
 - c. Repeat 'a' and 'b' for other side of sprocket.
 - d. Relative degree of snugness should be the same for each pair of rollers. If not, perform procedures in table 6-38.
- 4. Rotate feed and dedoubler rollers 90 degrees and repeat steps 3a through 3c to check roundness of rollers. Rotate feed and dedoubler rollers another 90 degrees and repeat roundness test. If rollers are out-of-round, refer to table 6-26 to replace feed rollers and table 6-27 to replace dedoubler rollers.

6-43



1





2.2 Replace Sun Gun Lamp

1. Deenergize reader.

2,

3.

WARNING

Allow sun lamp to cool before removing to prevent burns.

Remove sun lamp by pulling it straight out of socket.

CAUTION

Do not touch quartz surface of new sun lamp with bare fingers or lamp may fail prematurely due to contamination.

Install new sun gun lamp in socket.

4. Adjust sun gun lamp per PMP 2.3, step 5.

2.3 Check PM Head and Optics

This procedure checks light source, lens, lightpipes, PM tubes, and servo boards. Proper setup of the PM head and optics will ensure optimum reading performance.

Typical problems are sagging sun gun filaments, faulty servo boards, low or high gain PM tubes, and defective lightpipes.

NOTE

The PM head must have been operational for 1 hour before attempting the following checks and adjustments. Operational means full or half sun gun brilliance to the PM tubes.

- 1. Clean lens and reflectors. Use lint-free tissue and/or swabs for cleaning.
- 2. Place a white piece of paper in read area and position scanning mirror at center of paper. Paper must be clean and void of any dark spots or marks.
- 3. Bring up reader. Sun gun lamp should go to full brilliance. Set high voltage to -1550 vdc, using a voltmeter of at least 10 megohm impedence. Do not use voltmeter on high voltage power supply panel.
- 4. Adjust sun gun lamp voltage to a nominal value as follows:

NOTE

If the handprint option is installed, a dc voltage is applied to the sun gun lamp. All other machines will have ac applied to lamp.

- a. For ac lamps connect voltmeter to yellow test jacks on 'A' power supply. For dc lamps connect voltmeter to plus and minus terminals of lamp dc power supply terminal strip. The dc power supply is accessible by removing cover at left front of machine.
- b. Turn LAMP ADJUST potentiometer until nominal sun gun lamp is as follows:

650 watt lamp

600 watt lamp

80-90V (brown PM tubes 85-95V (red PM tubes) 90-100V (orange PM tubes) 85-95V (brown PM tubes) 90-100V (red PM tubes) 95-105V (orange PM tubes)

- 5. Adjust sun gun lamp angle as follows:
 - a. Remove cover from photomultiplier assembly at rear of reader.

%

2.3 Check PM Head and Optics (Cont'd)

5. (Continued)

NOTE

A seating screw is used to hold the PM box firmly in position. This screw is located underneath the PM box at the rear center of the bottom plate. If the seating screw is too tight it will cause the PM box to distort and degrade the reading ability of the reader.

It is recommended that if correct PM head voltages can be obtained without use of the seating screw that the screw be left out. If correct voltages cannot be obtained without use of the seating screw, ensure that the screw is not so tight as to cause distortion.

b. Connect voltmeter (this is a high-voltage measurement) to test point C of servo board (XA20) for lightpipe 20. (See sheet 30 in logic diagrams manual.)

NOTE

Use only digital voltmeter.

- c. Initially position lamp housing 1/4 inch from deflector. Manually move mirror across paper in read station. Adjust lamp assembly to give lowest reading across width of paper on XA20.
- d. Repeat step 5c monitoring lightpipe 40 (TP-C, XA40). This will ensure optimum positioning.
- 6. Check HV with DVM or VOM.
- 7. Check and record each PM servo board HV output as follows:

NOTE

Ensure that light is being reflected from unblemished center of paper at read position.

- a. Connect voltmeter to HV output of servo board for lightpipe 2. This would be TP-C of XV2 (located at top right) in Row A. Record HV reading.
- b. Repeat step 7a for lightpipes 3 through 55 (TP-C for even-numbered lightpipes and TP-D for odd-numbered lightpipes). Refer to table 6-5.
- c. If the majority of HV outputs are greater than -250 volts, adjust the lamp voltage to bring outputs below -250 volts. Lamp voltage is not to be adjusted below 70 volts or above 100 volts.

2.3 Check PM Head and Optics (Cont'd)

7. (Continued)

- d. If any or all HV outputs are still greater than -250 volts, or less than -75 volts, refer to troubleshooting chart (table 6-10).
- e. The servo board HV reading must not be more than -250 volts nor less than -75 volts.
- 8. Check each PM servo board video signal output as follows:
 - a. Connect oscilloscope test probe to applicable PM head or logic rack test point for lightpipe 2. Refer to table 6-5.

If reader contains the handprint option, prepare a test document by making several vertical marks on a blank piece of paper with a No. 2 pencil. Use medium pressure. Register this document at read station with vertical marks in read zone.

If reader does not have handprint option register a 14-mil test document at the read station with a line of print in the read zone.

b. Scan test document and observe white-to-black transitions of video signal.
White levels should be stable and clear at -14V for PM heads with SB-3 servo boards, or -11V for PM heads with SB-4, SB-5, or SB-6 servo boards. Black level should rise to -0. 4V (TP-A for even-numbered lightpipes and TP-F for odd).

Failure to meet these specifications usually indicates a bad servo board.

- c. Continue to scan read zone and repeat steps 7a and 7c for lightpipes 3 through 55.
- 9. Adjust sun gun lamp voltage to nominal voltage listed in step 4. Remove test document from read area.

NOTE

If size 'C' is installed, the size 'C' lightpipes must be checked holding the same specifications.

Bow	Photomultiplier			HV	Video Signal Test Points	
Row	Lightpipe	Socket	Board	Test Point	SV Board	Logic Rack
Α	$2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10$	XV2 XV3 XV4 XV5 XV6 XV7 XV8 XV7 XV8 XV9 XV10 XV11 XV12 XV13 XV14 XV15 XV16 XV17	XA 2 XA 3 XA 4 XA 5 XA 6 XA 7 XA 8 XA 9 XA 10 XA 11 XA 12 XA 13 XA 14 XA 15 XA 16 XA 17	C D C D C D C D C D C D C D C D C D C D	A F A F A F A F A F A F A F	2B08 pin 5 2A08 pin 2 2A08 pin 5 2B09 pin 2 2B09 pin 5 2A09 pin 5 2A09 pin 5 2B10 pin 5 2B10 pin 5 2A10 pin 5 2B11 pin 5 2B11 pin 5 2A11 pin 5 2B12 pin 2
a B B A B	$ \begin{array}{r} 18\\ 19\\ 20\\ 21\\ 22\\ 23\\ 24\\ 25\\ 26\\ 27\\ 28\\ 29\\ 30\\ 31\\ 32\\ 33\\ 34\\ 35\\ 36\\ 37\\ \end{array} $	XV18 XV19 XV20 XV21 XV22 XV23 XV24 XV25 XV26 XV27 XV28 XV29 XV30 XV31 XV32 XV33 XV34 XV35 XV36 XV37	XA 18 XA 19 XA 20 XA 21 XA 22 XA 23 XA 24 XA 25 XA 26 XA 25 XA 26 XA 27 XA 28 XA 29 XA 30 XA 31 XA 32 XA 33 XA 34 XA 35 XA 36 XA 37	C D C D C D C D C D C D C D C D C D C D	A F A F A F A F A F A F A F A F A F A F	2B12 pin 5 2A12 pin 2 2B13 pin 2 2B13 pin 2 2B13 pin 5 2A13 pin 5 2A13 pin 5 2A13 pin 5 2B14 pin 2 2B14 pin 5 2B14 pin 2 2B15 pin 2 2B15 pin 5 2A15 pin 5 2A15 pin 5 2B16 pin 5 2B16 pin 5 2A16 pin 5 2B17 pin 2

2.3 Check PM Head and Optics (Cont'd) TABLE 6-5. PM HEAD AND OPTICS LIGHTPIPE TEST POINTS

48430080 C

Row	Photomultiplier			HV	Video Signal Test Points	
	Lightpipe	Socket	Board	Test Point	SV Board	Logic Rack
С	38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55	XV38 XV39 XV40 XV41 XV42 XV43 XV44 XV45 XV46 XV45 XV46 XV47 XV48 XV49 XV50 XV51 XV52 XV53 XV54 XV55	XA 38 XA 39 XA 40 XA 41 XA 42 XA 43 XA 44 XA 45 XA 45 XA 46 XA 47 XA 46 XA 47 XA 48 XA 49 XA 50 XA 51 XA 52 XA 53 XA 54 XA 55	C D C D C D C D C D C D C D C D C D C D	A F A F A F A F A F A F A F A F A F A F	2B17 pin 5 2A17 pin 2 2A17 pin 2 2A17 pin 5 2B18 pin 2 2B18 pin 2 2A18 pin 5 2A18 pin 5 2B19 pin 2 2B19 pin 5 2A19 pin 5 2A19 pin 5 2B20 pin 2 2B20 pin 5 2A20 pin 5 2B21 pin 2 2B21 pin 5 2A21 pin 5 2A21 pin 5

2.3 Check PM Head and Optics (Cont'd)

TABLE 6-5. PM HEAD AND OPTICS LIGHTPIPE TEST POINTS (CONT'D)

48430080 C

6-51/6-52

2. 3A Check Video Quantize Level

Enable maximum quantizing level by either of the following methods:

1. Using RX-1 diagnostic, set quantize level to FF by pressing MANUAL INTERRUPT at the teletype and entering C, OCR(QL) = FF.

2.

a. Insert the following program into the 1700:

P =0000;	X = C000 0100 6807 E000 0509 0B00 03FE 0DFE C400 0100 0B00	D8FC C8FB 9000 0110 0101 18F6 0DF8 0A01 03FE 0000	P =0100;	X =0A3F 0A6F 0A6E 0A6D 0A6C 0A6B 0A6A 0A69 0A68 B800
	$0\mathrm{B00}$ $03\mathrm{FE}$			

- b. MASTER CLEAR the 1700 and set in run mode. This will set READY on the 955/959 and will set QL = FF.
- c. Measure the -15 vdc in the photohead and insure that it reads exactly 15.0 vdc.
- d. Using digital voltmeter, test the voltage on 2C23-02 and adjust pot on 2C23 to read -4.1 ±.02 vdc.

2.4 Check for Loose Setscrews

1. Deenergize reader.

2. Check all accessible gears, pulley, and couplings for loose setscrews and clamps. Remove any loose setscrews and re-insert after application of Loctite or equivalent grade C sealant.



2.5 Check Feed and Pre-feed Rollers

1. Energize reader.

- 2. Check feed and pre-feed roller surfaces for evidence of glazing (shiny and hard).
- 3. If glaze is apparent, hold sheet of 400 grit emery cloth lightly against roller and press LOAD pushbutton indicator on operator's control panel.
- 4. Stop sanding when roller surface becomes dull.
- 5. Wipe roller with cheese cloth slightly dampened with isopropyl alcohol.

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2.6 Rotate Mirror Drive Motor

The mirror dc servo motor normally drives the mirror shaft through an angle of only 45.9 degrees covering 12.240 inches $(00_{16} \text{ to FF}_{16} \text{ mirror shaft position count})$ in the document plane. The motor commutator will wear unevenly if the rotation of the motor frame remains fixed, resulting in a depression in the commutator over the limits of the scanning angle under each of the four brushes. To help even distribution of commutator wear, rotate the motor frame monthly as follows:

CAUTION

Do not alter or disassembly mirror drive motor.

1. Locate slot in motor flange as shown in figure 6-16.

NOTE

If this is first performance of procedure, slot should be aligned with hole in mirror drive base. If this is not first performance, proceed to step 3.

2. Using felt tip marking pen, mark reference lines every 10 degrees on both the motor flange and mirror drive base for 90 degrees to the left and right of slot as shown in figure 6-16.

3.

CAUTION

Do not rotate motor frame beyond ± 90 degree positions to avoid damage to motor cable.

Loosen four motor clamps and rotate motor frame one reference mark (10 degrees) from previous position in the following direction. Direction of rotation is determined from record of previous motor position. The motor frame is turned clockwise to the +10 degree reference mark the first time this procedure is performed, then clockwise in increments of 10 degrees each time thereafter until the +90 degree reference mark is reached. Once the +90 degree position is reached, the motor frame is turned counterclockwise in increments of 10 degree position is reached, the motor reaches the -90 degree position. Once the -90 degree position is reached, the 180 degree rotation is repeated in monthly increments of 10 degrees.

- 4. After motor frame is rotated to new position, tighten four motor clamps.
- 5. Enter date and initials beside corresponding motor position in record provided in table 6-6.

2.6 Rotate Mirror Drive Motor (Cont'd)

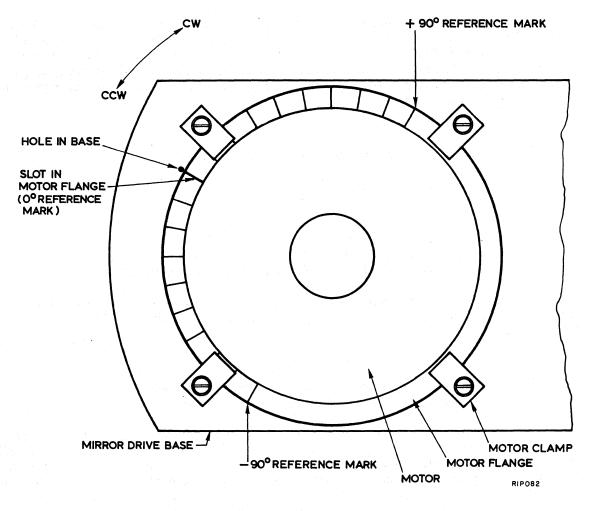


Figure 6-16. Mirror Drive Motor Rotation

2.6 Rotate Mirror Drive Motor (Cont'd)

Date and Initials	Position (Degrees)						
	+10		-10		+10		-10
	+20		- 20		+20		- 20
	+30		-30		+30		- 30
	+40		- 40		.+40		- 40
	+50		-50		+50		-50
	+60		- 60		+60		- 60
	+70		-70		+70		-70
	+80		-8 0		+80		-80
	+90		-90		+90		- 90
	+80		-80		+80		-80
	+70		-70		+70		-70
	+60	-	- 60		+60		- 60
	+50		-50		+50		-50
	+40		-40		+40		- 40
	+30		-30		+30		- 30
	+20		- 20		+20		- 20
	+10		-10		+10		- 10
	0		0		0		0

TABLE 6-6. MOTOR POSITION RECORD

48430080 C

2.7 Check Vacuum Motor Brushes

1. Deenergize reader.

2. Remove brush enclosure caps.

3. Remove retaining clips from brush housing.

4. If brush is less than 1/2 inch long, replace brush (Part No. 94901503).

2.8 Read Zone Sensor Alignment Test

The purpose of this test is to check the Document Ready position of the reader. Document Ready position means that the read zone centerline is 0.200 inch from the leading edge of the document. This position can be modified by using the DPA (Document Page Advance) parameter in RX1. Document Ready position is advanced down the page by 0.008 inch for each count in the DPA parameter.

NOTE

The following patch must be loaded in the BC prior to running this test:

LOC		\underline{INST}
0BDD	=	0800
0BDE	=	C800

- 1. Measure from top edge of standard test document to center of first line, subtract 0.200 and divide by 0.008 to determine DPA setting.
- 2. Load RX1 and select the following parameters:

DPA	=	(as determined in step 1)
LCT	=	1
ADV		0
RSC		0
EOL	=	0
ESP	=	2
TMC	=	40
CMP	=	A

- 3. Load standard ANSI document 14/0/3, to the read zone and ready reader.
- 4. Initiate reader in servo data mode OCR (SDM) TTY. This will read 14/0/3 in upper left hand corner of document and print SERVO DATA below it.
- 5. Load another document and repeat several times in order to establish an average location where the documents are stopping in the read zone.
- 6. A servo zone printout of 18 ± 3 (15 to 21) indicates the characters are centered in the read zone and document ready is set correctly.

If the line falls high in the read window the position of the read zone sensor must be moved toward the feedup table; if the line is low in the window the read zone sensor must be moved away from the feedup table. If adjustment is required, load the next document after the adjustment is made.

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2.8 Read Zone Sensor Alignment Test (Cont'd)

- 7. Adjust the read zone sensor to achieve a servo data reading of 18 ± 3 while maintaining a ± 15 V reading on the output of the read zone sensor. It may be necessary to adjust the light source in order to maintain a minimum reading of ± 15 V on the read zone sensor (test point B).
- 8. Final check once adjustment is correct. Scan 25 documents; servo zone line for all documents should be 18 ±3.

2.9 RX-3 System Test

The RX-3 system test is a preventive maintenance test used to determine system operability. The following equipment is used in running RX-3:

1700 Computer or SC1700 System Controller with at least 8K memory 608 or 609 Magnetic Tape Transport 1711 or 1713 Teletypewriter (TTY)

RX-3 interfaces with the 1700 System Maintenance Monitor (SMM17) only for the purpose of loading RX-3. Once loaded, the RX-3 monitor assumes complete control. Refer to SMM 17 System Maintenance Monitor, Pub. No. 6018200, for loading and operation.

All applicable modules and subtest should be run, with the exception of module 2, subtests 6 and 7; a more accurate test of transport operation and document handling is obtained from RX4, module 1, subtest 1 (see PMP 2.10).

When running module 4, set up mirror coordinates and dwell times as follows:

- 1. IMC (Initial Mirror Coordinate) =10₁₀, TMC (Terminal Mirror Coordinate) =250₁₀; run at dwell =1₁₀ and again at dwell =200₁₀.
- 2. IMC = 10_{10} , TMC = 100_{10} ; dwell times same as above.
- 3. IMC =100₁₀, TMC =150₁₀; dwell times same as above.
- 4. IMC =150₁₀, TMC =250₁₀; dwell times same as above.

If errors occur during RX3, refer to the troubleshooting sources or procedures listed below:

Module 1:	See CJ122 logic diagrams, Pub. No. 48430081, vol. 2, part 1A (Mods. C
	and D) or Pub. No. 48948100, vol. 2, part 1 (Mods. E, F, G, H, J, and K).
Module 2:	Subtests 1 - 3: see tables 6-8, 6-9, and PMP 2.8.
	Subtests 4 and 5: see table 6-51, table 6-17.
Module 3:	See logic diagrams (refer to module 1 above).
Module 4:	See logic diagrams (refer to module 1 above); see table 6-49, table 6-52.
Ъ <i>Т</i> - Л	Car have deviced large discreasing Date No. 49142091 (CW126 Mode A E) on

Module 5: See handprint logic diagrams, Pub. No. 48143981 (CW126 Mods. A-E) or Pub. No. 48911900 (CW126 Mod. F, CW207 Mod. A); see table 6-15.

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2.10 RX-4 System Test

The RX-4 system test is a preventive maintenance test used to determine system operability. The following equipment is used in running RX-4:

1700 Computer or SC1700 System Controller with at least 8K memory 608 or 609 Magnetic Tape Transport 1711 or 1713 Teletypewriter (TTY)

RX-4 interfaces to the 1700 System Maintenance Monitor (SMM17) only for the purpose of loading RX-4. Once loaded, the RX-4 monitor assumes complete control. Refer to SMM17 System Maintenance Monitor, Pub. No. 60182000 for loading and operation.

Run module 1, subtest 1 to verify stepping accuracy. If errors occur, refer to table 6-51.

2.11 BC2 Buffer Controller Test

The BC2 buffer controller test is used to determine whether the buffer is operating properly.

The following equipment is used in running BC2:

1700 Computer or SC1700 System Controller with at least 8K memory 608 or 609 Magnetic Tape Transport CDC 1711 or 1713 Teletypewriter (TTY) Maintenance Console

Refer to SMM17 System Maintenance Monitor, Pub. No. 60182000, for loading and operation.

If errors occur, see BC2 troubleshooting procedures, page 6-104.



3.1 Check Mirror Alignment

Mirror alignment ensures that the mirror encoder is properly aligned on the scanning shaft and that documents fed to the read station are centered below the scanning mirror.

- 1. Mark a vertical black line through the middle of a test document and place document in feeder.
- 2. Adjust paper guides such that the middle of the document falls on center of transport belt.
- 3. Using RX-1 diagnostic, feed document up to read area. Check that middle of document is still aligned with center of transport belt. If not, perform procedures in table 6-43 to adjust edger.
- 4. Using RX-1 diagnostic and CJ122 test document, perform a stationary read using the following coordinates:

ADV	=0
IMC	=2C
TMC	=37
POS	=1C
DPA.	=2E ? U
LCT	=0

5. Repeat this procedure, changing the following coordinates:

ADV	=2
LCT	=20

6. Check printout. The only characters read should be 'A' through 'E', inclusive. If printout differs from 'A' through 'E', inclusive, perform mirror calibration adjustment procedures in table 6-49.

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3.2 Check Constant Current, LEMAL, Lower A/D Converter, Character Quantizer Reference Voltages

Reference voltages are checked to ensure optimum character correlation.

- 1. Perform procedures in table 6-47 to check LEMAL and lower A/D converter reference voltage adjustment.
- 2. Perform procedures in table 6-46 to check constant current adjustment.
- 3. Perform procedures in table 6-48 to check character quantizer reference voltage adjustment.

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3.3 Clean Vacuum Holes

1. Deenergize reader.

2. Check vacuum holes for accumulated dirt. Clean as required.

3. Dampen cheese cloth slightly with trichloroethane or isopropyl alcohol.

4. Clean surface around vacuum holes.

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3.4 Check Timing and Vacuum Belt Tensions

1. Deenergize reader.

2. Check timing belts by applying a 1- to 2-pound force at center of belt.

a. All timing belts, except feeder drive belt, should deflect from 1/16 to 1/8 inch.b. Feeder drive belt should deflect 3/16 inch.

3. Refer to table 6-37 for adjustment procedure if required.

4. Measure length of springs on edger tension bracket. Spring should be elongated 5/16 inch $\pm 1/32$ inch from unstretched length.

5. Refer to step 11, table 6-30 for tension adjustment, if required.

- 6. Measure length of spring on conveyor tension lever. Spring should be approximately 4.5 inches from end to end.
- 7. Refer to step 11, table 6-29 for tension adjustment, if required.



4.1 Check Power Supply Voltages (CJ122 Mods. C, D, F, and J)

1. Energize reader.

2. Remove three front lower panels, front BC panel, and center front panel.

NOTE

In the following steps, if indicated voltage is not obtained, refer to table 6-14 for trouble shooting.

3. Measure following voltages at controller power supply panel:

Voltage

Test Jack

dc common	DC COMMON, black (TP02)
- 2 ±0.3V	- 2 vdc, blue (TP06)
- 6 +0.9V	- 6 vdc, blue (TP04)
+ 6 ±0.9V	+ 6 vdc, red (TP05)
+ 8 ±1.2V	+ 8 vdc, red (TP01)
$+16 \pm 2.4 V$	+16 vdc, red (TP03)

NOTE

If necessary, adjust out of tolerance vdc level at appropriate adjustment screw on 3-phase regulator.

4. Measure following voltages at the A SUPPLY panel.

Voltage	Test Jack
dc common	COMMON, black (TP06)
+ 5 ±0.1V	+ 5 vdc, red (TP01)
+15 ±0.3V	+15 vdc, red (TP02)
-15 ±0.3V	-15 vdc, blue (TP03)
$+12 \pm 0.24$ V	+12 vdc, red (TP04)
+10 ±0.2V	+10 vdc, red (TP05)

NOTE

Mods. F and J only: Adjust out of tolerance +15 vdc or -15 vdc at appropriate adjustment screw on panel; adjust out of tolerance +5 vdc by removing bottom panel of power supply and adjusting large tapped resistor (see figure 2-10B).

- 4.1 Check Power Supply Voltages (CJ122 Mods. C, D, F, and J) (Cont'd)
- 5. At LAMP TEST yellow test jacks (TP07 and TP08) on A SUPPLY panel, measure . nominal sun gun voltages as follows:

650 Watt Lamp

600 Watt Lamp

80-90V (brown PM tubes) 85-95V (red PM tubes) 90-100V (orange PM tubes) 85-95V (brown PM tubes) 90-100V (red PM tubes) 95-105V (orange PM tubes)

NOTE

If journal tape option is installed, add 10 vac to indicated voltages. If necessary, adjust vac level at LAMP ADJUST potentiometer on A SUPPLY panel. If handprint option is installed, the lamp voltages listed above are dc and are measured at the lamp supply rectifier/filter at left front corner of reader.

6. Measure following voltages at B SUPPLY panel:

Voltage

Test Jack

dc common	COMM, black (TP02)
+20 ±0.6V	+20 vdc, red (TP01)
$-20 \pm 0.6 V$	-20 vdc, blue (TP03)

7. Measure following voltages at TRANSPORT SERVO SUPPLY panel:

Voltage

Test Jack

de common	COM, black (TP03)
+45V	+45 vdc, red (TP02)
-45V	-45 vdc, blue (TP04)

8. Remove attaching screws from POWER CONTROL UNIT front panel. Pull out power control unit and lower front panel until terminal board TB01 on interlock power supply is accessible. Remove terminal board protector as shown in figure 6-17. Measure following voltages at TB01:

Voltage	Test Point
dc common	TB01-5
+6 ±0.15V	TB01-4
+5 ±0.15V	TB01-3

Reinstall terminal board protector and front panel.

9. Insert a piece of unmarked white paper in hopper and load to read zone. Check HV with DVM or VOM and verify that reading is approximately -1550V. The exact value is recorded on the reader's checkoff list.

NOTE

If necessary, adjust high voltage at VOLTAGE ADJUST potentiometer on high voltage power supply.

10. Reinstall three front lower panels, front BC panel, and center front panel.

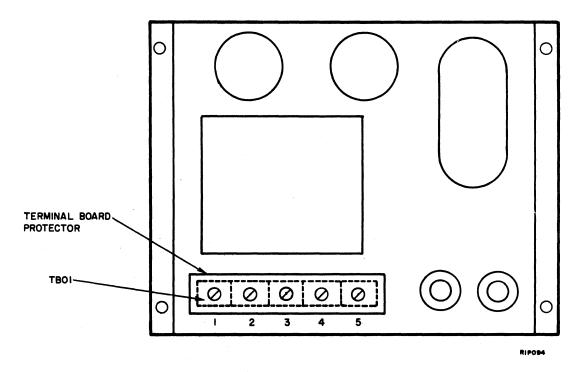


Figure 6-17. Interlock Power Supply



4.2 Check Power Supply Voltages (CJ122 Mods. E, G, H, and K)

1. Energize reader.

2. Remove three front lower panels, front BC panel, and center front panel.

NOTE

In the following steps, if indicated voltage is not obtained, refer to table 6-14 for troubleshooting.

3. Measure following voltages at controller power supply panel:

Voltage

Test Jack

dc common	COM, black (TP06)
+ 5 ±0.15V	+ 5 vdc, red (TP01)
- 5 ±0.15V	- 5 vdc, blue (TP02)
+30 ±0.5V	+30 vdc, red (TP03)
- 6 ±0.2V	- 6 vdc, blue (TP04)
$+ 6 \pm 0.2 V$	+ 6 vdc, red (TP05)

NOTE

If necessary, adjust out of tolerance +5 vdc or -5 vdc level at appropriate adjustment screw on controller power supply.

4. Measure following voltages at the A SUPPLY panel.

Voltage	Test Jack	
dc common	COMMON, black (TP06)	
+ 5 ±0.1V	+ 5 vdc, red (TP01)	
+15 ±0.25V	+15 vdc, red (TP02)	
$-15 \pm 0.25 V$	-15 vdc, blue (TP03)	
+12 ±1. 2V	+12 vdc, red (TP04)	
+10 ±1.0V	+10 vdc, red (TP05)	

NOTE

If necessary, adjust out of tolerance +15 vdc or -15 vdc at appropriate adjustment screw on panel; adjust out of tolerance +5 vdc by removing bottom panel of power supply and adjusting large tapped resistor (see figure 2-10B).

5. At LAMP TEST yellow test jacks (TP07 and TP08) on A SUPPLY panel, measure:

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4.2 Check Power Supply Voltages (CJ122 Mods. E, G, H, and K) (Cont'd)

90 vac ±2 percent if reader has orange photomultiplier tubes.
85 vac ±2 percent if reader has red photomultiplier tubes.
80 vac ±2 percent if reader has brown photomultiplier tubes

NOTE

If journal tape option is installed, add 10 vac to indicated voltages. If necessary, adjust vac level at LAMP ADJUST potentiometer on A SUPPLY panel. If handprint option is installed, the lamp voltages listed above are dc and are measured at the lamp supply rectifier/filter at left front corner of reader.

6. Measure following voltages at B SUPPLY panel:

Voltage

** 1/

Test Jack

COMM, black (TP02)

dc common +20 ±0.6V -20 ±0.6V

+20 vdc, red (TP01) -20 vdc, blue (TP03)

7. Measure following voltages at TRANSPORT SERVO SUPPLY panel:

Voltage	Test Jack	
dc common	COM, black (TP03)	
+45V +5.0 -1.0V	+45 vdc, red (TP02)	
-45V +5.0 -1.0V	-45 vdc, blue (TP04)	

8. Remove attaching screws from POWER CONTROL UNIT front panel. Pull out power control unit and lower front panel until terminal board TB01 on interlock power supply is accessible. Remove terminal board protector as shown in figure 6-17. Measure following voltages at TB01:

Voltage	Test Point
dc common	TB01-5
+6 ±0.15V	TB01-4
+5 ±0.15V	TB01-3

Reinstall terminal board protector and front panel.

 Insert a piece of unmarked white paper in hopper and load to read zone. Check HV with DVM or equivalent having at least 10 megohms input impedance; verify that reading is -1550V. The exact value is recorded on the reader's checkoff list.

NOTE

If necessary, adjust high voltage at VOLTAGE AD-JUST potentiometer on high voltage power supply.

10. Reinstall three front lower panels, front BC panel, and center front panel.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures are given in logical order. The actions performed for each step must be performed in the order given; any deviation in the order of action may result in an incorrect indication of the fault.

The procedures are not all-inclusive. The tests are intended only to direct the technician to the stage or stages requiring repair or calibration. Obvious checks, such as for blown fuses, etc., are not included.

NOTE

When performing resistance checks, examine the schematic diagrams to become aware of parallel resistance paths which will affect the meter indication.

The troubleshooting tables contain procedures to assist the technician in locating faulty parts within the units. The Symptom column lists those indications that may occur and subsequent columns provide procedures which will isolate the trouble to the faulty part. Settings for switches are not given in the tables unless they differ from the settings used during the check and alignment.

WARNING

Lethal voltages may be present within a repairable unit. Discharge all capacitors prior to performing troubleshooting or replacement procedures.

CAUTION

Do not remove or insert any of the solenoid driver PC boards when the 955 is in a POWER ON condition. Damage to the boards will result if this precaution is not observed.

NOTE

Tag all wires as to destination and size before removal or replacement.

After locating the cause of the trouble, the technician should refer to the appropriate unit schematic and parts location diagram to aid in identifying the defective part or unit for replacement. When the trouble is apparently corrected, repeat all steps in the PMP's up to the point where the malfunction indication was first discovered to be certain that no other malfunction has been caused by the replacement.

CAUTION

Use low-wattage soldering iron (25 watts max.) when soldering connections or semiconductors. Connect a heatsink to leads on semiconductor before applying soldering iron.

NOTE

Failure is often caused by marginal performance of a part which is not obviously defective itself. When troubleshooting, consider what circumstances could have caused the failure, then critically examine those parts likely to be at fault.

Video Display Setup Procedure

The video display setup procedure listed in table 6-7 pertains to CJ122 Mods. C and D, and enables the video image of scanned characters to be displayed on an oscilloscope. Each column of character data is sampled at the output of the reader image register. For CJ122 Mods. E, F, G, H, J and K, character video can be viewed directly at the COL GEN test point on the maintenance panel.

When using the oscilloscope for troubleshooting or display on the CJ122, ground the oscilloscope using the ground leads that attach to the scope probe(s). If both probes are to be utilized, connect ground leads from both probes. Ground leads are to be connected to a ground point as near to the signal being monitored as possible.

This grounding procedure provides a shield for the scope probe cables which results in a cleaner and more stable oscilloscope picture.

When this grounding procedure is being used, <u>do not</u> use a ground connection from the oscilloscope chassis to the CJ122.

On any CJ122 utilizing the FF104 or FR113 it may be desirable to look at some circuit, line, or register at a particular time in the Buffer Controller program. A sync for the oscilloscope is available on the FF104 at location B01, Test Point AW, and on the FR113 at location A11, Test Point 5. This signal comes up any time the 'S' register matches the breakpoint switches on the maintenance console.

TABLE 6-7. VIDEO DISPLAY SETUP PROCEDURE (CJ122 MODS. C AND D)

Step	Procedure
1	Sync positive on READ test jack on maintenance panel.
2	Connect CHANNEL 1 test probe to sawtooth (COL GEN) test jack on maintenance panel.
3	Connect CHANNEL 2 test probe to last stage output of image register at recogni- tion rack location C22, TP-U (Mod. C) or to location A10, TP-N (Mod. D).
4	Set MODE select switch on scope preamplifier to ADD.
5	Adjust VERTICAL GAIN on both channels until characters displayed on scope are proportional.

Step	Trouble Symptom	Possible Cause	Corrective Action
1	No change in sensor out- put voltage when infrared path is broken	Infrared light path out of alignment	Align infrared light source and sensor unit per steps 1 and 2 of table 6-44.
		Power inputs incorrect or not present	Check power inputs to infrared light source and sensor unit.
		No infrared light	Replace infrared light source.
		Faulty comparator ampli- fier in sensor unit	Replace sensor unit.
		Sensor unit output clamped by excessive load	Check for loading in logic area.
2	No change in sensor unit photocell output voltage	Infrared light path out of alignment	Align infrared light source and sensor unit per steps 1 and 2 of table 6-44.
		Power inputs incorrect or not present	Check power inputs to infrared light source and sensor unit.
		No infrared light	Replace infrared light source.
		Faulty photocell in sen- sor unit	Replace sensor unit.

TABLE 6-8. DOCUMENT SENSOR CIRCUIT TROUBLESHOOTING PROCEDURE

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Step	Trouble Symptom	Possible Cause	Corrective Action
1	Incorrect response or no response from DOUBLES INDICATOR on document adjustment panel	Doubles remote circuit out of adjustment	Adjust doubles remote cir- cuit per steps 6 through 9 of table 6-45.
		Power inputs incorrect or not present	Check power inputs to doubles remote circuit.
		Faulty voltage compara- tor or output transistor in doubles remote circuit	Replace doubles remote circuit.
		Faulty indicator	Replace light-emitting- diode on document adjust- ment panel.
2	No output or excessively low output from doubles sensor	Infrared light path out of alignment	Align doubles sensor per steps 6-9 of table 6-45.
		Power inputs incorrect or not present	Check power inputs to doubles sensor and infra- red light source.
		No infrared light	Replace infrared light source.
		Faulty amplifier or photocell in doubles sensor	Replace doubles sensor.

TABLE 6-9. DOUBLES SENSOR TROUBLESHOOTING PROCEDURE

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Step	Trouble Symptom	Possible Cause	Corrective Action
1	1 All PM servo boards have HV outputs greater than -250 volts	Low light emission from sun gun lamp	
		a. Incorrect power input	Adjust sun gun lamp vol- tage.
		b. Defective sun gun lamp	Replace lamp.
		High voltage power supply output high	Reduce until outputs are in range.
		Electromechanical lens shutter hung	Ensure that lens shutter is open for Size I or Size IV and is free to move.
2	Any one PM servo board HV output greater than	Faulty PM servo board	Replace servo board.
	-250 volts	Low gain PM tube	Replace PM tube.
		Weak or no light from lightpipe	
		a. Due to variations in acceptable lightpipes, a particular lightpipe may transmit less light than others	Switch PM tubes. Another PM tube with higher gain will compensate for marginal lightpipe.
		b. Lightpipe improperly installed. Could be recessed.	Check lightpipe installa- tion, per procedures in table 6-33.
		c. End of lightpipe covered. Could be piece of rubber from holder.	Remove obstruction.
		d. Lightpipe cracked	Replace lightpipe per table 6-33.

TABLE 6-10. PM HEAD AND OPTICS TROUBLESHOOTING PROCEDURE

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Step	Trouble Symptom	Possible Cause	Corrective Action
3	All PM servo board HV outputs less than -75 volts	High light emission from sun gun lamp	Adjust sun gun lamp vol- tage.
		High voltage power sup- ply output low	Increase until outputs are in range.
		PM box not seated pro- perly	Ensure bolt in bottom of PM box is tight.
		Size IV shutter hung allowing light to both sets of lightpipes	Unhang. (See table 6-34, step 12.)
4	Any one PM servo board output less than -75	Faulty PM servo board	Replace servo board.
	volts	High gain PM tube	Replace PM tube.
		Due to variations in acceptable lightpipes a particular lightpipe may	Switch PM tubes. Another PM tube with lower gain will compensate for light-
		transmit more light than others.	pipes with high light transmission.

TABLE 6-10. PM HEAD AND OPTICS TROUBLESHOOTING PROCEDURE (CONT'D)

Step	Trouble Symptom	Possible Cause	Corrective Action
1	Document jams at feeder and dedoubler rollers.		
2	Documents hang up on stationary ramp.	Sensor flag improperly set	Perform steps 1, 2, and 3 of table 6-40.
3	Gap between documents becomes too great.	Feed roller slick	Perform procedures in PMP 2.5,
		Documents binding	Set guide walls to 1/16 inch by turning PAPER WIDTH ADJUST switch.
		Weight on feeder impro- perly set	Perform steps 4 to 7 of table 6-40.
		Dedoubler set wrong	Adjust dedoubler.
4	Document becomes skewed after it leaves edger.	Doubles sensor too close to conveyor vacuum belt	Measure from trailing edge of sensor shield to con- veyor belt. Should be 0.040 to 0.060 inch.
			Adjust height by moving doubles sensor bracket in slotted mounting holes.
			Check for doubles. Refer to table 2-17.
		Dirt on conveyor trough	Clean trough using cheese- cloth dampened with tri- chloroethane or isopropyl alcohol.
		Document sensor too close to vacuum belt	Adjust cover assembly to remove interference.
		Plastic trough section above level of vacuum belt	Remove shims (C washers).
		Vacuum at edger belt too high	Lower vacuum level.

TABLE 6-11. DOCUMENT FEED TROUBLESHOOTING PROCEDURE

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TABLE 6-12. JOURNAL TAPE (OPTION) TROUBLESHOOTING PROCEDURE

CAUTION

The journal tape takeup spool is driven by a pic-belt. If the spooler is running free it should not be stalled or stopped abruptly as damage to the pic-belt will result.

Step	Trouble Symptom	Possible Cause	Corrective Action
1	Tape buckles in read area	Spliced tapes not parallel to each other	Correct splicing. Raise input roller arm by turning roller arm adjustment screw.
2	Tape slips over con- veyor belt towards takeup assembly	Takeup motor set too high	Adjust motor setting at journal tape control panel.
3	Tape does not roll on takeup spindle	Takeup motor set too low	Adjust motor setting at journal tape control panel.
4	Conveyor will not feed tape through read area	Conveyor vacuum pres- sure too low	Refer to table 6-41.

TIMING FAULT DETECTION

The procedures for detecting timing faults in the oscillator, phase generator, and vertical shift counter and decoder are contained in table 6-13. Once the incorrect timing signal is detected, isolate the fault by tracing back to the defective component. Refer to CJ122 Reader Logic Rack Diagrams, Dwg. No. 48950000, sheets 24 and 25, Pub. No. 48430081, or Dwg. No. 48950100, sheets 24 and 25, Pub. No. 48948100.

Step	Procedure
1	Check 7.8546 MHz crystal oscillator output with oscilloscope as follows:
	 a. Sync positive on 4503/57 pin 56/2. b. Ground 4A12-10 and 4B10, pin 2 (CJ122 Mod. C01) or 4B14-3 (CJ122 Mods. C02, D, E, F, G, H, J, and K). c. Set oscilloscope TIME/CM to 100 nanoseconds/division. d. Connect oscilloscope probe to points shown in figure 6-18 and compare waveforms.
2	Check four-phase generator as follows:
	 a. Sync positive on PHASE GEN test point on maintenance panel. b. Set TIME/CM to 100 nanosecond/division scale. c. Connect oscilloscope test probes to designated locations and observe four-phase generator timing diagrams as shown in figure 6-19.
3	Check eight-phase generator as follows:
	 a. Sync positive on PHASE GEN test point on maintenance panel. b. Set oscilloscope TIME/CM to 100 nanosecond/division scale. c. Connect oscilloscope test probes to designated locations and observe eight-phase generator timing diagrams as shown in figure 6-20.
4	Check vertical shift counter and decoder as follows:
	 a. Sync negative on 4D18, pin 5. b. Set oscilloscope TIME/CM to 10 microsecond/division scale. c. Connect oscilloscope test probes to designated locations and observe vertical shift counter timing diagrams as shown in figure 6-21. d. Syncing on the same location (4D18, pin 5), connect oscilloscope CHANNEL 1 test probe to 4D19, pin 2. e. Connect CHANNEL 2 test probe to designated locations and observe vertical shift counter decoder timing diagrams as shown in figure 6-22. f. Disconnect oscilloscope.

TABLE 6-13. TIMING FAULT DETECTION

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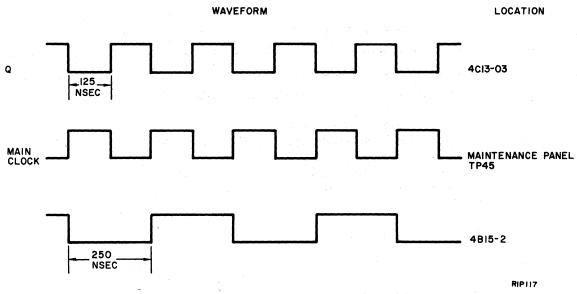
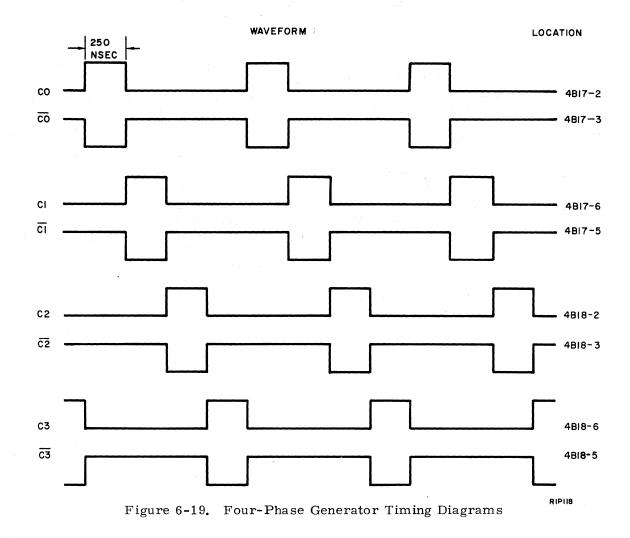


Figure 6-18. Oscillator Timing Diagrams



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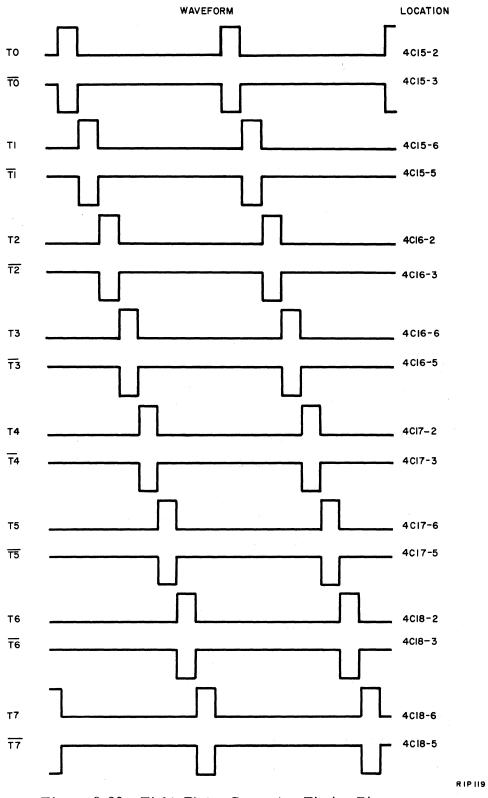


Figure 6-20. Eight-Phase Generator Timing Diagrams

 $\sum_{i=1}^{n}$

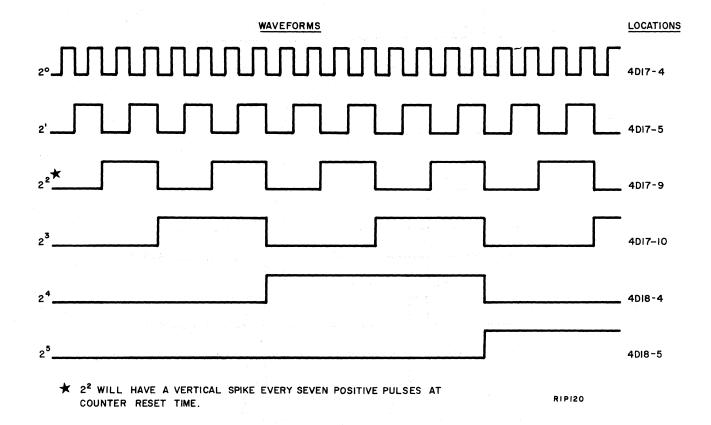


Figure 6-21. Vertical Shift Counter Timing Diagrams

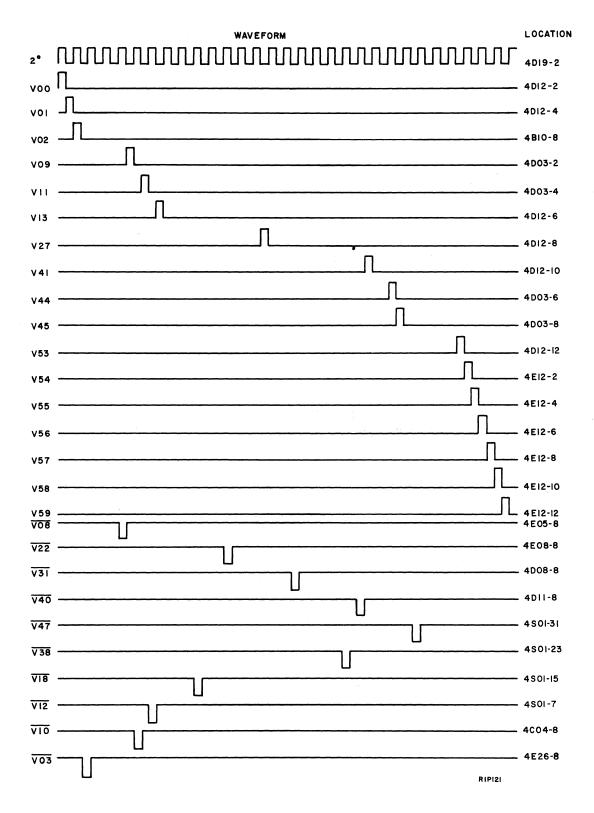


Figure 6-22. Vertical Shift Counter Decoder Timing Diagrams

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Step	Trouble Symptom	Corrective Action
1	The dc voltages measured at buffer con- troller power supply are out of tolerance.	Replace either the 3-phase regulator or the buffer controller power supply.
2	One or more dc voltages at A supply are out of tolerance.	Replace A supply.
3	The 90 or 85 vac power for sun gun lamp is out of tolerance.	Check variac in A supply and regulator in power controller A13.
		Replace defective component.
		NOTE
		If H. P. option is installed there is a dc rectifier/filter that could cause sun gun problems. See page 7-78 of Pub. No. 48991800 (Dwg. No. 48200000).
4	± 20 V levels are out of tolerance.	Replace B supply.
5	± 45 V levels are out of tolerance.	Re p lace transport servo supply.
6	Either +6.0V or +5.0V levels are out of tolerance.	Replace interlock power supply in power control unit.
7	Nominal -1550V is not obtained.	Replace high voltage power supply.

TABLE 6-14. POWER TROUBLESHOOTING PROCEDURE

TABLE 6-15. HANDPRINT (OPTION) TROUBLESHOOTING PROCEDURE

Step	Procedure							
	Normal ANSI Reading							
	NOTE							
	The 73ZPR is a tri-level voltage source (see figure 6-23) used to control the SB5 or SB6 servo board. The voltage out (TP-A) is controlled by one of three input conditions. See Pub. No. 48430045, Dwg. No. 48860300.							
1	Check that TP-C (white clamp) and TP-A (zapper) are at logic 1.							
3	Connect oscilloscope to TP-A and check voltage. This voltage should be less than (more negative than) -15 vdc.							

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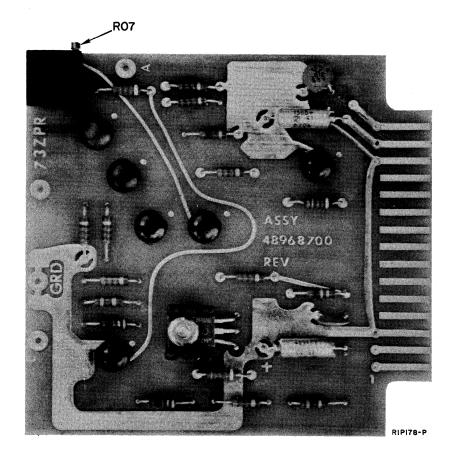


Figure 6-23. 73ZPR PC Board Parts Location Diagram

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TABLE 6-15. HANDPRINT (OPTION) TROUBLESHOOTING PROCEDURE (CONT'D)

Step	Procedure
3	If -15 vdc is not available, replace PC board and repeat steps 1 through 3.
	Size IV Reading
4	Connect oscilloscope to TP-A.
5	Momentarily connect ground to TP-B. The voltage at TP-A should swing from -15 vdc to approximately -4.1 vdc ± 0.7 V.
6	If the voltage does not swing as stipulated in step 5 disconnect oscilloscope, replace PC board, and repeat steps 4 through 6.
	Handprint Reading
7	Measure and record -15 vdc supply voltage at card pin 2.
8	Mark a test document with a No. 1 pencil, using heavy horizontal strokes. Completely fill one line with glossy pencil marks.
9	Mount SMM17 test tape and load RX-3, Module 4 (see PMP 2.9). Enable handprint and continuous rescan of the test line.
10	Connect oscilloscope to TP-A and check voltage. This voltage should nominally be -11.75 vdc $\pm 0.1V$ when white clamp (TP-C) is at logical 0 (handprint enabled).
	NOTE
	The voltage at TP-A is related to the level of the -15 vdc supply. The correct value for TP-A is found as follows:
	a. Algebraically add -15.7V to the measurement taken in step 7. The answer can be either negative or positive.
	b. Algebraically add the result to -11.75V.
11	Adjust resistor R07 to obtain the correct voltage if reading obtained in step 10 is not correct.
12	Check TP-B for logical 1.
13	If voltage is not obtainable after performing step 11, disconnect oscilloscope, replace PC board, and repeat steps 7 through 13.

SYSTEM TEST TROUBLESHOOTING

The following programs have been developed for maintaining the reader system:

- 1. RX-1 System Test Used as the primary check during preventive maintenance to determine system operability. Also used to test the system using the controlware and the customer parameters as a first step in isolating a problem.
- 2. BC2 Buffer Controller Test Used periodically as a preventive maintenance test to ensure coupler communications reliability. BC2 contains interface, memory, and command tests for testing the BC.
- 3. RX-3 Module Tests Used for testing the following, when any of these is the suspected problem area:
 - a. reading ability
 - b. document handling
 - c. mirror control and accuracy
 - d. operator panel

If the system is operational, no testing other than RX-1 and BC2 is necessary. When a problem is suspected, do not reload the buffer controller as a first measure. Run RX-1 system test. If RX-1 runs successfully, run BC2 to check that communications and interrupts are operating properly. If RX-1 fails, examine all status and other errors to determine the next course of action.

RX-1 SYSTEM TEST TROUBLESHOOTING

Table 6-16 lists alphabetically some troubleshooting procedures emanating from RX-1 error messages.

References in table 6-16 to CJ122 Logic Rack Diagrams are abbreviated to save space. The full reference depends on the model of the machine under consideration, as follows:

CJ122 Mods. C and D

CJ122 Mods. E, F, G, H, J, and K

Pub. No. 48430081 Dwg. No. 48950000

TABLE 6-16. RX-1 SYSTEM TEST TROUBLESHOOTING PROCEDURE

Step	RX-1 Error Message	Possible Cause	Corrective Action	
1	BC CHECKSUM ERROR	Buffer controller impro- perly loaded	Reload buffer controller. If error persists, run BC2.	
2	BC FAILED TO RESPOND	Wrong equipment code	Check buffer controller equipment code.	
		Power failure	Ensure buffer controller is energized.	

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Pub. No. 48948100 Dwg. No. 48950100

TABLE 6-16. RX-1 SYSTEM TEST TROUBLESHOOTING PROCEDURE (CONT'D)

Step	RX-1 Error Message	Possible Cause	Corrective Action
2			
cont'd		Interrupt channel mal- function	Check that interrupt chan- nel is properly connected.
3	BLANK LINE		Check video display (see table 6-7). Video data should go all the way through the image register.
			Check that Character Data Ready signal is sent to the buffer controller. Refer to CJ122 Reader Logic Rack Diagram, sheet 59.
4	BUSY FROM START	Coupler malfunction	Run BC2.
		Last function not com- pleted in specified time	
5	DELETE LINE	Delete line read when none exists	Check video display (see table 6-7.) Look for solid horizontal line through entire video display. Refer to CJ122 Reader Logic Rack Diagrams, sheet 58.
		May be generating im- proper code in buffer controller	Run RX-3, Electronic Read and Verify Test.
6	DOCUMENT NO SORT	Stepping off page	Change line count to cor- rect number.
		Overlapping documents	Perform RX-3, Document Handling Test.
7	EXTERNAL REJECT		Reload buffer controller. Run BC2 if error persists.
8	FF104 NOT READY	Document no loaded and ready	Check power.
9	ILLEGAL ENTRY	Parameter error	Retyp e parameter.

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TABLE 6-16. RX-1 SYSTEM TEST TROUBLESHOOTING PROCEDURE (CONT'D)

Step	RX-1 Error Message	Possible Cause	Corrective Action
10	LINE LOCATE AND DATA SKEW		
			Check video display (see table 6-7).
			Check topless/bottomless logic circuit. Refer to CJ122 Reader Logic Rack Diagrams, sheet 53.
11	LOST DATA	Lost data on line just read	Check Character Dat a communications logic. Refer to CJ122 Reader Logic Rack Diagrams, sheet 59.
12	MEMORY PARITY ERROR AT LOCATION \$xxxx		Run SMM17 Test 2, Mem- ory Test.
13	MT CHECKSUM ERROR FILE NO. xx		Retry read or write oper- ation
			Recopy tape.
			Run SMM17 tape test.
14	MT DOES NOT RESPOND	Tape transport not ready	Run BC2. Ready tape transport. If another unit
		Tape transport controller unit select card in error	responds, check unit select card.
			If no unit responds, check magnetic tape controller for malfunction.
15	PROGRAM PROTECT FAULT AT LOCATION \$xxxx		Run SMM17 Test 9, Pro- tect Test or Command Test.
16	TRANSPORT FAULT OCCURRED THIS LINE	A mechanical fault other than mirror fa u lt	Perform RX -3, Transport Test.

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Step	RX-1 Error Message	Possible Cause	Corrective Action		
17	UNDEF INED ALARM STATUS		Run BC2. NOTE		
			There are times when this error message occurs, yet nothing is wrong with BC, e.g., topless/ bottomless.		
18	955 STATUS=xxxx				
	Bits 15, 14, 13, 12 7 → 0	Mirror fault	Perform RX-3, Mirror Test.		
	Bit 11	Parameter error	If parameters correct, run BC2.		
	Bit 10	Document length fault from overlapping docu- ments or improper sensing	Perform RX-3, Document Handling Test.		
19	CHECK FF104 CONV, AND EQUIPMENT NUMBER	Improper parameter entry	Re-enter parameters.		
20	FF104 PROGRAM PROTECT SWITCH IS NOT SET		Set switch.		
21	BLK CH FAIL, RUN BC2	Noise spike during data transfer.	Reload BC firmware.		
22	PRINTER ALARM		Check line printer.		
23	AUTOLOAD REQUIRED		Reload BC firmware.		

TABLE 6-16. RX-1 SYSTEM TEST TROUBLESHOOTING PROCEDURE (CONT'D)

BC2 BUFFER CONTROLLER TEST TROUBLESHOOTING

When errors occur during running of BC2, the customer engineer must begin by tracing the error stop location in the listing of the Command 2 Test, thus locating the faulty instruction loop. He may then use the instruction timing tables (see following) for the FR-101 controller (CJ122 Mods. C, D, F, and J), the TTL input/output channel test point tables (see following) for the FR-113 Controller (CJ122 Mods. E, G, H, and K), and the BC logic diagrams to isolate the problem.

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Assume that failure occurred during a subtract operation, with A=FEFE and the contents of a memory location (M)=EFEF. The correct answer is 0F0F, but the actual answer is CF0F.

When the BC halts, the following register values may be displayed.

- P = 46F
- B1 = 46D (Absolute buffer controller return address)
- B2 = 0F0F (Correct answer)
- A = CF0F (Actual answer)

Looking up the B1 address in the Command 2 listing (see legend 5 of figure 6-24) shows that the test loop is in absolute buffer controller locations 466 through 46E. At location 466, A is set to FEFE and a subtract is performed, using a memory location containing EFEF. Location 46D indicates that an overflow should have occurred. A halt at location 46E would indicate no overflow, which is in error for these operands.

Instruction Timing Table for FR-101 Buffer Controller

The instruction timing information (see Pub. No. 60278300) provides a comprehensive troubleshooting analysis for the BC2 Command 2 Test. The timing tables cite each instruction and detail the actions that should occur at each point during the instruction cycle. The instruction sequence data is valid for both the FR-101 and FR-113 controllers. However, the controlling terms, board locations, and test points listed are unique to the FR-101.

TTL Input/Output Channel Test Point Tables for FR-113 Controller

These tables list test points for input and output channel data and channel select terms. They are useful in isolating a fault to one modular logic block, which is replaceable as a unit.

BC Logic Diagrams

See Pub. No. 60278300 for the FR-101 controller; see Pub. No. 60334500 for the FR-113 controller.

RX-3 MODULE TESTS TROUBLESHOOTING

The RX-3 module tests are used to isolate faults when certain errors are detected during the RX-1 system test, PMP 1. 7, or when operation errors are suspected to be in circuitry tested by the diagnostic. The diagnostic consists of six distinct modules. Five modules are in a selected buffer controller and the other module is a 1700 computer program which loads the buffer controller programs and communicates normal and error messages with the operator.

Descriptions of the five RX-3 module tests are contained in the following paragraphs.

Module 1 - Electronic Read and Verify Test Description

The electronic read and verify tests checks the reader recognition logic electronics as shown in figure 6-25. The program sends the character images to the reader load register

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4510 4511 4512	P0C42 P0C43 P0C44 P0C45 P0C46	1101 0820 06 0 0	NUM NUM NUM	\$40B1 \$1101 \$0820 \$0600 \$40B2	455 456 457		LDD SBN Tov TA1 LDD	C0000 1 0 CFFFF	INPUT 0000 -	0001 0001			BC245090 BC245100 BC245110 BC245110 BC245120 BC245130
4514 4515 4516 4517 4518	P0C47 PnC48 PnC49 P0C4A P0C4B	0700 1802 8882 E802 0000	NUM NUM NUM NUM	\$0700 \$1802 \$8882 \$E802 \$0000	459 45A 45B 45C 45D		TA2 EAR UJR FJR SLS	0 \$+2 CKADR \$+2 0		OVERFLOW		EEEE	BC245140 BC245150 BC245160 BC245160 BC245170 BC245180
4520 4521 4522 4523	PnC4C PnC4D PnC4E PnC4F PnC50 PnC51	1001 0820 C302 0000	NUM NUM NUM NUM	\$4082 \$1001 \$0820 \$C302 \$0000 \$E302	45F 460 461 462		LDD ADN TOV ZJR SLS TJR	CFFFF 1 0 \$+2 0 \$+2		FFF + 1 = 0	D	EEEE	BC245190 BC245200 BC245210 BC245220 BC245220 BC245230 BC245240
4525 4526 4527 4528 4529	P0C52 P0C53 P0C54 P0C55 P0C55 P0C56 P0C57	0000 43EA 6BA6 0820 0600	NUM NUM NUM NUM	\$0000 \$43EA \$6BA6 \$0820 \$0600 \$439F	464 465 466 467 468		SLS LDR SBR TOV TA1 LDR	0 CFEFE CEFEF 0 0 CC0F0F		VERFLOW NO. II-24 EFEF	(9		BC245250 BC245260 BC245270 BC245280 BC245290 BC245290 BC245300
4531 4532 4533 4534 4535	P0C58 P0C59 P0C59 P0C58 P0C58 P0C50 P0C50	0700 1802 88A1 E302 0000	NUM NUM NUM NUM	\$0700 \$1802 \$8841 \$E302 \$0000 \$43CA	46A 46B 46C 46D 46E		TA2 EAR UJR TJR SLS LDR	0 \$+2 CKADR \$+2 0 C6666		VERFLOW			BC245310 BC245320 BC245330 BC245330 BC245340 BC245350 BC245360
4537	POCSE POCSE POCSF	60B0	NUM	\$60B0 \$0820	470		ADD	C5555 0	6666 + 		(3	BC245370 BC245380
Leger		card num	nber			1700 Asse		Language	7	Remarks	-	RIPI05A	an An An Angalan An
	f comp	ister addı outer 7 contents			5 /			controller	8	EEEEE in stop Instruction			
\sim	nis loca			(6 I	Buffer co	ntrolle	r instructio		sample add			.1.

Figure 6-24. BC2 Command 2 Listing (Example)

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N. 2 - N. 2 - N. 2

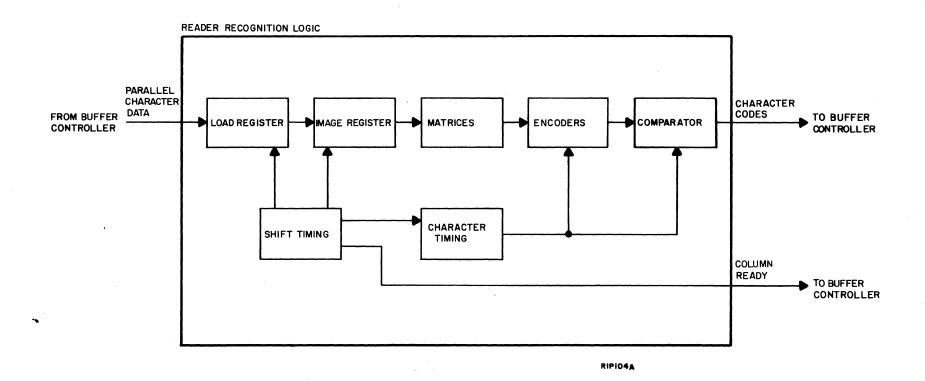


Figure 6-25. RX-3 Electronic Read and Verify Test Data Flow

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via the BC channel 7 and tests for proper recognition by examing the character codes sent out by the reader character encoders.

The BC program is initialized with a group of character images prior to execute time. Each image requires 30 words of core storage in the BC. The set of ASCII character codes representing the images are also sent by the computer program to the BC program.

At execution time the BC begins to output the images by performing a series of 4-word outputs to the BC channel 7. Each 4-word output simulates one vertical column of character data to the reader. Each column of character data contains 56 bits (four 14-bit words). When the simulated image is centered in the reader shift register, the BC checks for a data ready signal from the reader. If the data ready signal is present, the program inputs the status of the reader encoder, inputs the character voltage, and performs various housekeeping functions. If the data ready signal is not present, additional 4-word outputs of either character data or space data are sent while testing for data ready and errors. When all the images have been sent to the reader, the program compares the character codes generated by the reader encoder with the reference ASCII codes sent to the BC from the computer. The program increments the total images read counter by the number of images read and updates the reject or error counters if errors are detected. If no errors are detected, the program tests for end of test; if the test if not yet complete, the program will return to read the same set of images. If either an error or a reject has been detected, the program checks the mode of operation.

The test is run on-line when the computer is available for message processing. The test is run off-line when the BC maintenance console is used for control and display. If the program is running in the on-line mode, the following information is sent to the computer and displayed on the teletype output:

Characters read totals Characters misread (error) totals Reject totals Reference line Error line Voltage line

If the program is running in the off-line mode, the program will come to a halt if the SELSTOP switch on the maintenance console is set to ON. The definition of each error halt, the expected ASCII code, and the code received from the reader encoder is displayed in the maintenance console A Register.

Module 1 also checks the operation of topless/bottomless logic, read window servoing, operation of reader load and shift registers, and OLCC capture and display capability.

Module 2 - Page and Document Handling Test Description

The page and document test checks the document transport mechanics and electronics. The test consists of seven subtests as follows:

Subtest 1 - Light Sensor Test Subtest 2 - Dark Sensor Test (Sort to Pocket 1) Subtest 3 - Dark Sensor Test (Sort to Pocket 2) Subtest 4 - Transport Speed Test (Check Points RZ and SST1) Subtest 5 - Transport Speed Test (Check Points RZ and SST2) Subtest 6 - Document Slippage Test Subtest 7 - Reader Feed and Sort Exerciser

Subtest 1 tests all of the document path sensors for a light condition (not covered). The BC program will indicate to the computer program the status of any sensor in an incorrect state.

During subtest 2, one document is fed and sorted to pocket 1. As the document moves through the transport system, the sensors are monitored for a light-to-dark transition. After the document is sorted to pocket 1, the sensors are tested for a light condition. Sensors not demonstrating a light-to-dark transition are reported to the operator through the computer program.

Subtest 3 operates the same as subtest 2, except that the document is sorted to pocket 2.

During subtest 4, the program feeds one document and waits for the read zone sensor to cover. Using the document length information specified by the feed parameters, the program calculates the document velocity. A velocity error message is reported to the operator if the velocity is not within four percent of the expected speed. The program now waits for sort station 1 to cover. Using again the document length information specified by the feed parameters, the program calculates the document velocity. A velocity error message is reported to the operator if the operator if the velocity is not within ten percent of the expected 70 inches per second.

Subtest 5 operates the same as subtest 4 with the following exception. The document is sorted in the secondary hopper in order to check document velocity at sort station 2.

During subtest 6, the program feeds documents at the specified speed and as each document covers and uncovers the read zone sensor, the transport motion is brought to a halt. From the time the document uncovered the read zone sensor and the stop command was given, the program will record the number of conveyor counts required for the document to come to a complete stop. If no document slippage occurred, moving the document backward to the read zone sensor should cover the sensor with the same number of conveyor counts which were required to bring the document to a halt. The BC program will notify the computer program of the direction and number of conveyor counts whenever document slippage is detected.

Subtest 7 is a general feed/sort routine. The feed rate and sort sequence are specified by the operator during initialization. After the test is executed from the TTY, the BC program will initiate document feeding when the READY pushbutton is pressed at the reader operator control panel. As the documents are moving through the transport system, the BC performs the following checks. The program monitors the document gap at the read zone sensor. A gap error is recorded if the gap becomes less than 1/4 inch or greater than 2 inches.

The program constantly monitors the document throughput rate by counting the documents fed and using the reader real time clock pulses to update a minute and a second clock. All jams, doubles, and no feeds are counted by the program and sent to the computer as they are detected. In the event of a jam, the BC program will turn off the reader transport power and the takeaway motor in the sort area. To restart, the operator must clear the jam conditions and press READY. The operator may define the throughput rate at any time by using the FP* manual parameter.

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Module 3 - Operator Panel Test Description

The operator panel test checks the reader operator control panel indicators and switches. After the test is executed at the TTY, the BC program causes the reader operator control panel indicators to sequentially flash from left to right, top to bottom. Indicators not operating properly will remain extinguished. The program will terminate the indicator test and begin the switch test when the operator presses the END OF FILE pushbutton. The program initiates the switch test by flashing the first switch indicator to be tested. If operating properly, the pushbutton indicator lights when pressed and remains lit until the pushbutton is released. Upon release, the program begins to flash the next switch to be tested. When all switches have been tested, the program will repeat the entire test.

Module 4 - Mirror Test Description

The mirror test checks the reader mirror drive electronics. After the test is executed at the TTY, the BC program waits for the operator to press READY to begin the test. After READY is pressed, the program executes a stop mirror command and monitors MNZV (mirror near zero velocity). If the program does not receive the MNZV signal within 10 milliseconds, the program will notify the computer program to report the failure to the operator. If the signal is received, the program checks the mirror status by monitoring for a mirror count or mirror velocity fault. Either fault will be reported to the operator.

The program will now execute a zero mirror command and wait for the mirror to go out of the scan gate. As soon as the mirror is out of the scan gate, the program drops the zero mirror command and executes a stop mirror command. The encoder count is checked at this time and the operator is informed if the count is not zero. The program will now terminate the stop mirror command and execute a scan forward command. As the mirror scans forward, the program frequently monitors the encoder. If, at any time, the program detects that the encoder has moved more than 1 coordinate, the operator is informed and the test is restarted. If reverse pulses are received from the encoder as the mirror is scanning forward, an appropriate message is sent to the operator and the test is restarted.

Following the scan forward command, the program waits for the mirror to reach the speed of 75 inches per second. As soon as the mirror reaches the speed of 75 inches per second, the program, using the reader real time clock, will record the time until the mirror reaches the forward coordinate specified by the operator. Upon reaching the forward coordinate, the program terminates the scan forward command and executes a stop command. As the program waits for the MNZV signal, it records the number of coordinates the mirror moves. Upon receiving the signal, the program starts the dwell timer and waits for the timer to time out. If the mirror moves, the program records the number of coordinates. The program now checks the calculated mirror speed and reports the actual mirror speed to the operator if the mirror speed is not within one percent of the expected 75 inches per second. The program checks also the number of mirror coordinates the mirror moved after the stop mirror command was executed until after the dwell time.

The operator is informed if the mirror moved more than three coordinates. The test is repeated if a zero mirror command must be executed at this time. If the program contains a reverse mirror coordinate parameter, the program computes the midpoint coordinate between the forward and reverse coordinate. The stop mirror command is now terminated and the accelerate reverse command is executed. The program frequently monitors the encoder as it waits for the mirror to reach the midpoint coordinate. The operator is informed if the encoder decrements by more than one count or generates forward pulses. As the

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mirror reaches the midpoint coordinate, the program will terminate the accelerate reverse command and continue to monitor the encoder until the mirror reaches the reverse coordinate. Upon reaching the reverse coordinate, the program executes a stop mirror command and waits for the MNZV signal. The number of coordinates which the mirror might move at this time are recorded. Upon receiving the MNZV signal, the program starts the dwell timer and waits for the timer to time out. If the mirror moves, the program records the number of coordinates. If the mirror moved more than three coordinates after the stop mirror command was executed until after the dwell time, the operator is informed before the next scan forward command is executed.

MODULE 5 - HANDPRINT ELECTRONIC READ AND VERIFY

This module checks the recognition logic of the handprint option. Simulated handprint character images and character codes are transferred from the 1700 computer via the BC to the reader, just as described for module 1. However, the reader recognition logic is disabled when handprint recognition is enabled. Six columns of data at a time are transferred from the reader image register to the handprint unit input register. The handprint unit analyzes each character image for significant features and outputs a character code to the BC, which transfers it to the 1700. After all the images have been processed by the handprint unit, the 1700 compares the received character codes with the character codes sent to the BC. If the program is running on-line, the 1700 enables a summary printout at the teletype, containing the following data:

Characters read (total) Errors (total) Substitutions (total) Rejections (total) Reference line Numerics (total) Alphas (total) Symbols (total)

Transport Power Amplifier Troubleshooting Procedure

The transport power amplifier assembly is spared or replaced as an assembly. However, problems with the amplifier assembly often can be isolated and the defective component replaced.

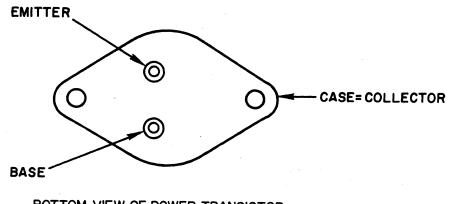
The most common failure in the amplifier assembly is the occurrence of shorts or opens in the power transistors. Q1 through Q6 are used for forward motion and Q7 through Q11 are used for reverse motion. If sufficient spares are available, all six (forward) and five (reverse) transistors should be replaced when any one transistor fails. (Type 2N3773 transistors are to be replaced upon failure with type 2N6259.)

These power transistors are difficult to meter and determine good/bad, but the procedure in table 6-17 will usually identify a defective transistor. Transistor balancing after replacement should be done according to table 6-50; then check transport speed accuracy by running RX-3, module 2, subtests 4 and 5 (PMP 2.9).

TABLE 6-17.TRANSPORT POWER AMPLIFIERTRANSISTOR TROUBLESHOOTING PROCEDURE

Step	Procedure	Indication				
1 1	Using Simpson 260 multimeter or equivalent, set on 10K-ohm scale and -dc.					
2	Connect common lead of multimeter to emitter lead of transistor being tested (see figure 6-26).					
8	Connect positive lead of multimeter to base lead of transistor.	Open or shorted condition indicates bad transistor; remove and replace (see table 6-35).				
4	Move positive lead of multimeter to collector (case) of transistor.	Open or shorted condition indicates bad transistor meter.				
5	Connect common lead of multimeter to collector (case) of transistor.					
6	Connect positive lead of multimeter to base lead of transistor.	There should be no meter deflection. If there is, replace transistor (see table 6-35).				
7	Move positive lead of multimeter to emitter lead of transistor.	There should be no meter deflection. If there is, replace transistor (see table 6-35).				
		NOTE This procedure checks only for open or shorted transistors.				
		When any transistor is replaced as a result of this procedure, all other transistors with trans- port power amplifier should also				
		be replaced (see table 6-35). After replacing transistors, proceed to table 6-50 and run RX3, module 2, subtests 4 and 5.				

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BOTTOM VIEW OF POWER TRANSISTOR

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Figure 6-26. Transistor Connections

TABLE 6-18. BC INPUT/OUTPUT CHANNEL CHECKS

Step	Procedure
	Input Signals
· · ·	NOTE
	These checks require the use of a BC maintenance console.
1	Enter the following instructions via the maintenance console:
	P Register
	Address Instruction
	0000 0CX0 0001 B800
	where X = input channel.
2	Select the A register. The high bits of the selected input channel will be displayed (illuminated) on the A register.
3	Enter the instruction above with $X = 3$. Ground each of the following points in turn and observe that the corresponding bit position is illuminated at the A register.

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Step	Proc	edure		
3	Signal	Location	Bit	
cont'd	500HZ Clock	6B29 - 11	0	
	Sort Pocket 2 Full	5C18-9	7	
	Sort Entry Photocell	6E30-13	8	
	Sort Pocket 1 Full	5C18-3	9	
	Sort Station 2 Photocell	6D30-13	10	
	Sort Station 2 Photocell	6D30-13	10	
		6C30-11		
	Read Zone Photocell		12	
	Doubles Sensor	6C30-5	13	
	Xport and Mirror Fault	5D19-11	14	
	Reader Ready	5D23-13	15	
4	Enter the instruction above with X =4. R following list:	epeat the proce	dure in step	3, using the
	Signal	Location	Bit	
	<u>Bighar</u>	LICATION		
	Scan Gate	6B24-5	1	
	Mirror Near 0 Velocity	6B22-9	2	
	Page Adv. Near 0 Vel.		4	(1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,
		6B30-13		
	Page Adv. Count $2/2$	6D29-9	5	
	Page Adv. Count $2/1$	6D29-11	6	
	Page Adv. Count $2/0$	6D29-13	7	
	Mirror Count 2/7	6A30-9	8	
	Mirror Count 2/6	6A30-5	9	
	Mirror Count 2/5	6A30-3	10	
	Mirror Count 2/4	6A30-1	11	
	Mirror Count 2/3	6A23-13	12	
	Mirror Count 2/2	6A23-11	13	
	Mirror Count 2/1	6B24 - 11	14	
	Mirror Count 2/0	6A24-11	15	
5	Enter the instruction in step 1 with X =5. following list (without handprint):	Repeat the pro	ocedure in s	tep 3, using the
	Signal	Location	Bit	
	Late Character Data	5B07-1	0	
$(1,1) \in \mathbb{R}^{d}$	Servo Data Ready	4B07-1	1	
	Servo Data 2/5	4A07-13	$\frac{1}{2}$	
	Servo Data 2/3 Servo Data 2/4	4A07-12	3	
an in s	Servo Data 2/4 Servo Data 2/3	4A07-12 4A07-9	3 4	
	Servo Data 2/3 Servo Data 2/2	4A07-9 4A07-5	4 5	
s de la constitución de la constitu Constitución de la constitución de la				
	Servo Data 2/1	4A07-2	6	
	Servo Data 2/0	4A07-1	7	

TABLE 6-18. BC INPUT/OUTPUT CHANNEL CHECKS (Cont'd)

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TABLE 6-18. BC INPUT/OUTPUT CHANNEL CHECKS (CONT'D)

Step	Proc	edure		/
5 cont'd	Signal	Location	Bit	
Joint d	Character Data Ready	5B07-2	8	
	Character Data 2/6	5B07-5	9	
	Character Data 2/5	5B08-13	10	
	Character Data 2/4	5B08-12	11	
	Character Data 2/3	5B08-9	12	
	Character Data $2/2$	5B08-5	13	
	Character Data 2/1	5B08-2	14	
	Character Data 2/0	5B08-1	15	
6	If handprint option is installed, enter the procedure in step 3, using the following h		tep 1 with X = <u>Bit</u>	=5. Repeat th
	Handprint Data Boady	3B27-13	1	
	Handprint Data Ready			
	Handprint Clear	3A26-1	2	
1	High	3A25-13	3	
	Error	3A24-1	4	
	Low	3A24-3	5	
	Numeric 2/3	3A25-11	6	
	Numeric 2/2	3A25-9	7	
	Numeric 2/1	3A25-5	<u>, 19</u>	
	Numeric 2/0	3A25-3	9	
	Alpha 2/2	3A25-1	10	
	Alpha 2/1	3A26-13	11	
	Alpha 2/0	3A26-11	12	
	Symbol 2/2	3A26-9	13	
	Symbol 2/1	3A26-5	14	
	Symbol 2/0	3A26-3	15	
7	Enter the instruction in step 1 with X =6. following list:	Repeat the pro	ocedure in ste	ep 3 using the
	Signal	Location	Bit	
	Column Ready (Image Reg)	2C12-9	0	
	Topless Data	4B07-3	2	
[Bottomless Data	4B07-5	3	
	Character Voltage 2/3	4B03-9	4	
	Character Voltage $2/2$	4B03-5	5	
	Character Voltage 2/2 Character Voltage 2/1	4B03-5 4B03-3	5 6	

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catility:

Step		Pr	ocedure		· · · · · · · · · · · · · · · · · · ·
7 ont'd		Signal	Location	Bit	
mu		Journal Tape Sw.	4B28-1	9	
		Parameter Entry Sw.	5B20-1	10	`
		End of File Switch	5E29-9	12	
		Load Switch	5E29-3	13	
		Stop Switch	5E29-1	14	
		Ready Switch	5E29-5	15	
8	Enter the ir following li	estruction in step 1 with X st:	=7. Repeat the pro	cedure in ster	3 using the
		Signal	Location	Bit	
		I.R. Input Bit 13	2E08-12	0	· · · ·
		I.R. Input Bit 12	2E08-1	1	
		I.R. Input Bit 11	2E09-1	2	
		I.R. Input Bit 10	2E09-5	3	
		I.R. Input Bit 9	2E09-9	4	
		I.R. Input Bit 8	2E09-12	5	
		I.R. Input Bit 7	2E10-1	6	
		I.R. Input Bit 6	2E10-4	7	
		I.R. Input Bit 5	2E10-9	8	
		I.R. Input Bit 4	2E10-12	9	
		I.R. Input Bit 3	2E11-1	10	
		I.R. Input Bit 2	2E11-5	11	
		I.R. Input Bit 1	2E11-12	12	
		I.R. Input Bit 0	2E11-12	13	
		I.R. Control Bit $2/1$	2E08-5	14	
		I.R. Control Bit 2/0	2E08-9	15	
	Output Sign	als			
0	······································		following programme		
9		he maintenance console the	ionowing program:		
	<u>P</u>	INST			
	0000		C = CHANNEL		
	- 1		X = BIT		
	2	8809	TO BE TESTED		
	3	C802			
	4	0BXY			
	5		GRAM WILL SET A		
	6		AL PERIODS OF T		
	7		ANNEL AND BIT T	HE OPERATO	DR
	8	B800 SELECTS			
	9	0000			
		0000			
		loscope, check for toggling			

TABLE 6-18. BC INPUT/OUTPUT CHANNEL CHECKS (CONT'D)

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ALC: NO

TABLE 6-19. OUTPUT SIGNALS

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Channel	D:4	Trad	Cimiel Deservicien	Test	Point
Channel	Bit	Ind.	Signal Description	Board	Pin
_					
3	2		GEN. SYNC. 2	5D23	4
3	3		GEN. SYNC. 1	5D23	6
3	0		CONTROLLER RUNNING	5D24	11
3	1		INHIB. READER TIMING	4A23	4
3	4		RECIRCULATE IMAGE	$4\mathrm{E}28$	2
3	5		JOURNAL TAPE READY	$4\mathrm{E}26$	1
3	6	YES	PARAMETER ENTRY	6505	15/8
3	7	YES	SORT HOPPER FULL	5A21	12
3	8	YES	SORT CHECK	5A21	8
3	9	YES	MIRROR CHECK	6505	54/5
3	10	YES	XPORT CHECK	6505	58/1
3	11	YES	DOUBLES CHECK	6505	65/2
3	12	YES	END OF FILE	6505	3/12
3	13	YES	LOAD IND.	5A21	6
3	14	YES	STOP IND.	5A21	2
3	15	YES	READY IND.	6505	61/6
4	0		READ	5B12	2
4	1		SCAN MIRROR FWD	6C22	1
4	2		ACCELERATE REV.	6C22	9
4	3		ZERO MIRROR	6C22	4
4	4		STOP MIRROR	6C22	12
4	5		SCAN LEFT TO RIGHT	6A24	12
4	6		REV. SHIFT	4E29	4
4	7		UPSIDE DOWN	2B24	11
4	8		CLEAR CHAR. DATA	5C04	6
4	9		CL. SERVO DATA	5C12	6
4	10		SORT GATE CONTROL	6C30	2
4	11		TRANSPORT COMMAND -5 IPS	6E09	8
4	12		TRANSPORT COMMAND 40 IPS	6E29	12
4	13		TRANSPORT COMMAND 20 IPS	6E29	8
4	14		TRANSPORT COMMAND 12.5 IPS	6E29	5
4	15		TRANSPORT COMMAND 5 IPS	6E29	1
5	0		USASI MARK SENSE	6D06	2
5	1		USASI NUMERIC	6D06	4
5	2		USASI CONTROL	6D06	6
5	3		USASI ALPHA "5"	6D06	8
5	4		USASI ALPHA "21"	6D06	10
5	5		USASI PUNCT. 1	6D06	10
5	6		USASI PUNCT. 2	6E06	$\frac{12}{2}$
5	7		OPTICAL SCALING	5C12	10
5	8		ALT. FONT LINE 1	5C12 6E06	· · · · · · · · · · · · · · · · · · ·
5	9		ALT. FONT LINE 2	6E06	4
5 5			ALT. FONT LINE 2 ALT. FONT LINE 3		6 8
Э	10		ALI. FUNI LINE 3	6E06	Ő

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TABLE 6-19. OUTPUT SIGNALS (CONT'D)

Sector of the sector	Channel	Bit	Ind.	Signal Description	Test I	Points '
	Chaimer		ma.	biginal Description	Board	Pin
5 13HANDPRINT ENABLE SUPERFILL (GOTHIC HANDPRINT) $3B23$ 5 5 14SUPERFILL (GOTHIC HANDPRINT) $3B23$ 5 6 0HORIZ, LINE TH. $4C07$ 12 6 0HORIZ, LINE TH. $4B25$ 4 6 1BLACK FILL ENABLE $3A24$ 12 6 2ACCUM CNT 2^5 $2B22$ 6 6 3ACCUM CNT 2^5 $2B22$ 10 6 4ACCUM CNT 2^3 $2B22$ 12 6 6ACCUM CNT 2^2 $2B23$ 2 6 7ACCUM CNT 2^0 $2B23$ 4 6 8QUANTIZE 2^7 $2B23$ 6 6 9QUANTIZE 2^6 $2B23$ 8 6 10QUANTIZE 2^5 $2B23$ 10 6 11QUANTIZE 2^4 $2B24$ 2 6 13QUANTIZE 2^1 $2B24$ 4 6 14QUANTIZE 2^1 $2B24$ 6 6 15QUANTIZE 2^0 $2B24$ 8 7 011R. OUTPUT BIT 1 $2E16$ 7 31R. OUTPUT BIT 3 $2E16$ 12 7 51R. OUTPUT BIT 5 $2E17$ 4 7 61R. OUTPUT BIT 11 $2E16$ 12 7 71R. OUTPUT BIT 11 $2E16$ 2 7 71R. OUTPUT BIT 11 $2E16$ 12 7 9	5	11		PITCH 7/INCH	6E06	10
514SUPERFILL (GOTHIC HANDPRINT)3B235515 $4/IN$ SCAN HEIGHT $4C07$ 1260HORIZ, LINE TH, $4B25$ 461BLACK FILL ENABLE $3A24$ 1262ACCUM CNT 2 ⁵ 2B22663ACCUM CNT 2 ⁵ 2B221065ACCUM CNT 2 ³ 2B221065ACCUM CNT 2 ³ 2B221066ACCUM CNT 2 ¹ 2B23266ACCUM CNT 2 ¹ 2B23267ACCUM CNT 2 ⁰ 2B23468QUANTIZE 2 ⁷ 2B23669QUANTIZE 2 ⁵ 2B2310611QUANTIZE 2 ⁵ 2B2310611QUANTIZE 2 ³ 2B242613QUANTIZE 2 ³ 2B242614QUANTIZE 2 ¹ 2B24670I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16872I. R. OUTPUT BIT 32E161273I. R. OUTPUT BIT 62E17274I. R. OUTPUT BIT 72E17877I. R. OUTPUT BIT 102E182714I. R. OUTPUT BIT 112E184715I. R. OUTPUT BIT 122E18716I. R. OUTPUT BIT 132E18717 <td< td=""><td>5</td><td>12</td><td></td><td>PITCH 8/INCH</td><td>6E06</td><td>12</td></td<>	5	12		PITCH 8/INCH	6E06	12
5154/IN SCAN HEIGHT4C071260HORIZ, LINE TH.4B25461BLACK FILL ENABLE3A241262ACCUM CNT 2^5 2B22663ACCUM CNT 2^5 2B221065ACCUM CNT 2^3 2B221065ACCUM CNT 2^3 2B2212666ACCUM CNT 2^1 2B23266ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^5 2B2310611QUANTIZE 2^5 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B246614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 32E161273I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 62E171677I.R. OUTPUT BIT 62E171677I.R. OUTPUT BIT 102E182710I.R. OUTPUT BIT 112E184711I.R. OUTPUT BIT 112E162710I.R. OUTPUT BIT 122E162710I.R. OUTPUT BIT 122E1627	5	13			3A24	5
5154/IN SCAN HEIGHT4C071260HORIZ, LINE TH.4B25461BLACK FILL ENABLE3A241262ACCUM CNT 2^5 2B22663ACCUM CNT 2^5 2B221065ACCUM CNT 2^3 2B221065ACCUM CNT 2^3 2B2212666ACCUM CNT 2^1 2B23266ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^5 2B2310611QUANTIZE 2^5 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B246614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 32E161273I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 62E171677I.R. OUTPUT BIT 62E171677I.R. OUTPUT BIT 102E182710I.R. OUTPUT BIT 112E184711I.R. OUTPUT BIT 112E162710I.R. OUTPUT BIT 122E162710I.R. OUTPUT BIT 122E1627	5	14		SUPERFILL (GOTHIC HANDPRINT)	3B23	5
61BLACK FILL ENABLE $3A24$ 1262ACCUM CNT 2^5 $2B22$ 663ACCUM CNT 2^4 $2B22$ 864ACCUM CNT 2^3 $2B22$ 1065ACCUM CNT 2^2 $2B22$ 12666ACCUM CNT 2^2 $2B23$ 267ACCUM CNT 2^0 $2B23$ 468QUANTIZE 2^7 $2B23$ 669QUANTIZE 2^5 $2B23$ 10611QUANTIZE 2^5 $2B23$ 12612QUANTIZE 2^4 $2B23$ 12612QUANTIZE 2^3 $2B24$ 2613QUANTIZE 2^1 $2B24$ 4614QUANTIZE 2^1 $2B24$ 870I.R. OUTPUT BIT 0 $2E16$ 671I.R. OUTPUT BIT 2 $2E16$ 1073I.R. OUTPUT BIT 3 $2E16$ 1274I.R. OUTPUT BIT 5 $2E17$ 476I.R. OUTPUT BIT 6 $2E17$ 677I.R. OUTPUT BIT 1 $2E18$ 2710I.R. OUTPUT BIT 18 $2E16$ 12710I.R. OUTPUT BIT 13 $2E16$ 2713I.R. OUTPUT BIT 13 $2E16$ 2714I.R. CONTROL BIT 21 $2E16$ 4715I.R. CONTROL BIT 21 $2E16$ 4714I.R.	5	15			4C07	12
61BLACK FILL ENABLE $3A24$ 1262ACCUM CNT 2^5 2B22663ACCUM CNT 2^4 2B22864ACCUM CNT 2^3 2B221065ACCUM CNT 2^2 2B23266ACCUM CNT 2^1 2B232667ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^5 2B2310611QUANTIZE 2^5 2B2312612QUANTIZE 2^5 2B2312613QUANTIZE 2^3 2B242613QUANTIZE 2^1 2B246615QUANTIZE 2^1 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 32E161273I.R. OUTPUT BIT 52E17476I.R. OUTPUT BIT 62E17677I.R. OUTPUT BIT 72E171079I.R. OUTPUT BIT 112E182710I.R. OUTPUT BIT 182E171079I.R. OUTPUT BIT 132E162713I.R. OUTPUT BIT 132E162714I.R. CONTROL BIT 212E164715I.R. CONTROL BIT 212E162<	6	0		HORIZ, LINE TH.	4B25	4
6 2 ACCUM CNT 2^5 2B22 6 6 3 ACCUM CNT 2^4 2B22 8 6 4 ACCUM CNT 2^2 2B22 10 6 5 ACCUM CNT 2^2 2B22 12 6 6 ACCUM CNT 2^1 2B23 2 6 7 ACCUM CNT 2^0 2B23 4 6 8 QUANTIZE 2^7 2B23 8 6 10 QUANTIZE 2^5 2B23 10 6 11 QUANTIZE 2^4 2B23 12 6 12 QUANTIZE 2^4 2B23 12 6 13 QUANTIZE 2^1 2B24 2 6 14 QUANTIZE 2^0 2B24 2 6 13 QUANTIZE 2^0 2B24 8 7 0 I.R. OUTPUT BIT 0 2E16 10 7 1 I.R. OUTPUT BIT 1 2E16 10 7 3 I.R. OUTPUT BIT 5 2E17 4 7 4 I.R. OUTPUT BIT 1 <td< td=""><td>6</td><td>1</td><td></td><td></td><td></td><td>12</td></td<>	6	1				12
63ACCUM CNT 2^4 2B22864ACCUM CNT 2^3 2B221065ACCUM CNT 2^2 2B221266ACCUM CNT 2^1 2B23267ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^7 2B2310611QUANTIZE 2^5 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B246614QUANTIZE 2^0 2B24670I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 32E161073I.R. OUTPUT BIT 42E17275I.R. OUTPUT BIT 52E17476I.R. OUTPUT BIT 62E17677I.R. OUTPUT BIT 72E17879I.R. OUTPUT BIT 102E182711I.R. OUTPUT BIT 122E184712I.R. OUTPUT BIT 132E184713I.R. OUTPUT BIT 132E184714I.R. CONTROL BIT 2^0 2E164715I.R. OUTPUT BIT 122E162715I.R. OUTPUT BIT 122E1627 <td>6</td> <td>2</td> <td></td> <td>ACCUM CNT 2⁵</td> <td></td> <td></td>	6	2		ACCUM CNT 2 ⁵		
64ACCUM CNT 2^3 2B221065ACCUM CNT 2^2 2B221266ACCUM CNT 2^1 2B23267ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^6 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^4 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B242613QUANTIZE 2^1 2B246614QUANTIZE 2^0 2B24870I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16870I. R. OUTPUT BIT 32E161273I. R. OUTPUT BIT 32E161274I. R. OUTPUT BIT 52E17275I. R. OUTPUT BIT 62E17677I. R. OUTPUT BIT 72E17878I. R. OUTPUT BIT 102E182710I. R. OUTPUT BIT 132E184712I. R. OUTPUT BIT 132E184712I. R. OUTPUT BIT 132E186713I. R. CONTROL BIT 2^0 2E164715I. R. CONTROL BIT 2^0 2E164715I. R. CONTROL BIT 2^0 2E16		3		ACCUM CNT 24		
65ACCUM CNT 2^2 2B221266ACCUM CNT 2^1 2B23267ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^5 2B2310611QUANTIZE 2^5 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^3 2B242613QUANTIZE 2^1 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^1 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 22E161073I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 32E161275I.R. OUTPUT BIT 62E17476I.R. OUTPUT BIT 72E17878I.R. OUTPUT BIT 102E182710I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E162713I.R. CONTROL BIT 2^1 2E162714I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^1 2E164714I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^1 2E162 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						
66ACCUM CNT 2^1 2B23267ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^6 2B238610QUANTIZE 2^5 2B2310611QUANTIZE 2^3 2B242612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B244614QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 22E161073I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 52E17275I.R. OUTPUT BIT 62E17476I.R. OUTPUT BIT 72E17877I.R. OUTPUT BIT 102E171079I.R. OUTPUT BIT 102E182710I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E186713I.R. OUTPUT BIT 122E164714I.R. CONTROL BIT 2^0 2E164715I.R. CONTROL BIT 2^0 2E164715I.R. CONTROL BIT 2^0 2E164715I.R. CONTROL BIT 2^0 2E164<		-				
67ACCUM CNT 2^0 2B23468QUANTIZE 2^7 2B23669QUANTIZE 2^6 2B2310610QUANTIZE 2^5 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^1 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 22E161073I.R. OUTPUT BIT 32E161073I.R. OUTPUT BIT 42E17275I.R. OUTPUT BIT 62E17677I.R. OUTPUT BIT 72E17878I.R. OUTPUT BIT 72E17879I.R. OUTPUT BIT 102E171079I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E186713I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^2 2E164214CHAR. PEAK REF. 2^2 6B12 </td <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td>		-				
68QUANTIZE 2^7 2B23669QUANTIZE 2^6 2B238610QUANTIZE 2^5 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^4 2B2312613QUANTIZE 2^3 2B242613QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16872I. R. OUTPUT BIT 22E161073I. R. OUTPUT BIT 32E161274I. R. OUTPUT BIT 42E17275I. R. OUTPUT BIT 52E17476I. R. OUTPUT BIT 62E17677I. R. OUTPUT BIT 72E17878I. R. OUTPUT BIT 82E171079I. R. OUTPUT BIT 92E1712710I. R. OUTPUT BIT 102E182711I. R. OUTPUT BIT 132E186713I. R. OUTPUT BIT 132E186714I. R. CONTROL BIT 2^0 2E164214MARKING PEN6E126212CHAR. PEAK REF. 2^3 6B124214CHAR. PEAK REF. 2^1 6B126			}			
69QUANTIZE 2^6 2B238610QUANTIZE 2^5 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^4 2B242613QUANTIZE 2^2 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16672I. R. OUTPUT BIT 22E161073I. R. OUTPUT BIT 32E161274I. R. OUTPUT BIT 52E17275I. R. OUTPUT BIT 62E17276I. R. OUTPUT BIT 72E17878I. R. OUTPUT BIT 82E171079I. R. OUTPUT BIT 92E1712710I. R. OUTPUT BIT 102E182711I. R. OUTPUT BIT 112E184712I. R. OUTPUT BIT 132E184713I. R. OUTPUT BIT 132E186714I. R. CONTROL BIT 2^0 2E164214CHAR. PEAK REF. 2^3 6B122213CHAR. PEAK REF. 2^1 6B126						
610QUANTIZE 2^5 2B2310611QUANTIZE 2^4 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E161073I.R. OUTPUT BIT 32E161073I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 52E17275I.R. OUTPUT BIT 62E17276I.R. OUTPUT BIT 72E17878I.R. OUTPUT BIT 82E171079I.R. OUTPUT BIT 102E182710I.R. OUTPUT BIT 102E182711I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E186713I.R. OUTPUT BIT 132E186714I.R. CONTROL BIT 2^0 2E164214MARKING PEN6E126212CHAR. PEAK REF. 2^3 6B122213CHAR. PEAK REF. 2^1 6B126		1	1			
611QUANTIZE 2^4 2B2312612QUANTIZE 2^3 2B242613QUANTIZE 2^2 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 22E161073I.R. OUTPUT BIT 32E161073I.R. OUTPUT BIT 52E17275I.R. OUTPUT BIT 52E17476I.R. OUTPUT BIT 62E17677I.R. OUTPUT BIT 72E17878I.R. OUTPUT BIT 82E171079I.R. OUTPUT BIT 102E182711I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E186713I.R. OUTPUT BIT 132E188714I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^0 2E164214CHAR. PEAK REF. 2^3 6B122213CHAR. PEAK REF. 2^1 6B126		1		•		
612QUANTIZE 2^3 QUANTIZE 2^2 QUANTIZE 2^2 QUANTIZE 2^1 QUANTIZE 2^0 QUANTIZE 2^0 Product 2^0 Prod						
613QUANTIZE 2^2 2B244614QUANTIZE 2^1 2B246615QUANTIZE 2^0 2B24870I.R. OUTPUT BIT 02E16671I.R. OUTPUT BIT 12E16872I.R. OUTPUT BIT 22E161073I.R. OUTPUT BIT 32E161274I.R. OUTPUT BIT 52E17275I.R. OUTPUT BIT 62E17276I.R. OUTPUT BIT 62E17677I.R. OUTPUT BIT 72E17878I.R. OUTPUT BIT 92E171079I.R. OUTPUT BIT 92E1712710I.R. OUTPUT BIT 102E182711I.R. OUTPUT BIT 112E184712I.R. OUTPUT BIT 122E182713I.R. OUTPUT BIT 132E184712I.R. OUTPUT BIT 132E184712I.R. CONTROL BIT 2^1 2E162715I.R. CONTROL BIT 2^0 2E164211MARKING PEN6E126212CHAR. PEAK REF. 2^3 6B122213CHAR. PEAK REF. 2^1 6B126						
6 14QUANTIZE 2^1 $2B24$ 6 6 15QUANTIZE 2^0 $2B24$ 8 7 0I. R. OUTPUT BIT 0 $2E16$ 6 7 1I. R. OUTPUT BIT 1 $2E16$ 8 7 2I. R. OUTPUT BIT 2 $2E16$ 10 7 3I. R. OUTPUT BIT 3 $2E16$ 12 7 4I. R. OUTPUT BIT 5 $2E17$ 2 7 5I. R. OUTPUT BIT 5 $2E17$ 4 7 6I. R. OUTPUT BIT 6 $2E17$ 6 7 7I. R. OUTPUT BIT 7 $2E17$ 8 7 8I. R. OUTPUT BIT 8 $2E17$ 10 7 9I. R. OUTPUT BIT 9 $2E17$ 12 7 10I. R. OUTPUT BIT 10 $2E18$ 2 7 11I. R. OUTPUT BIT 12 $2E18$ 4 7 12I. R. OUTPUT BIT 13 $2E18$ 8 7 13I. R. OUTPUT BIT 21 $2E16$ 2 7 14I. R. CONTROL BIT 2^0 $2E16$ 4 2 11MARKING PEN $6E12$ 6 2 12CHAR. PEAK REF. 2^3 $6B12$ 2 2 13CHAR. PEAK REF. 2^1 $6B12$ 6						
615QUANTIZE 2^0 2B24870I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16872I. R. OUTPUT BIT 22E161073I. R. OUTPUT BIT 32E161274I. R. OUTPUT BIT 42E17275I. R. OUTPUT BIT 52E17476I. R. OUTPUT BIT 62E17677I. R. OUTPUT BIT 72E17878I. R. OUTPUT BIT 82E171079I. R. OUTPUT BIT 92E1712710I. R. OUTPUT BIT 102E182711I. R. OUTPUT BIT 112E184712I. R. OUTPUT BIT 122E162713I. R. OUTPUT BIT 132E188714I. R. CONTROL BIT 212E162715I. R. CONTROL BIT 202E164214CHAR. PEAK REF. 2 ³ 6B122213CHAR. PEAK REF. 2 ¹ 6B126		3				
70I. R. OUTPUT BIT 02E16671I. R. OUTPUT BIT 12E16872I. R. OUTPUT BIT 22E161073I. R. OUTPUT BIT 32E161274I. R. OUTPUT BIT 42E17275I. R. OUTPUT BIT 52E17476I. R. OUTPUT BIT 62E17677I. R. OUTPUT BIT 72E17878I. R. OUTPUT BIT 82E171079I. R. OUTPUT BIT 82E1710710I. R. OUTPUT BIT 102E182711I. R. OUTPUT BIT 112E184712I. R. OUTPUT BIT 122E186713I. R. OUTPUT BIT 122E162715I. R. CONTROL BIT 212E162715I. R. CONTROL BIT 202E164214CHAR. PEAK REF. 2^3 6B122213CHAR. PEAK REF. 2^1 6B126						
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[†]CJ122 Mods. G and H

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Channal	774	Trad	Simol Description	Test Points	
Channel	Bit	Ind.	Signal Description	Board	Pin
2	0		TRANSPORT CHECK	6E12	13
2	1		TRANSPORT DROP POWER	6D23	11
2	8		HP HORIZONTAL PITCH 2 ⁰	3B24	1
2	9		HP HORIZONTAL PITCH 2 ¹	3B24	3

TABLE 6-19. OUTPUT SIGNALS (CONT'D)

REPAIR AND REPLACEMENT

Procedures for the removal and replacement of component parts of the reader and OLCC are contained in tables 6-20 through 6-36. Removal and replacement of component parts of the reader and OLCC are limited to those functional parts that are found to be faulty in performing the PMP's or the troubleshooting procedures.

NOTE

Tag all wires as to destination and size before removal or replacement.

After locating the cause of the trouble, the technician should refer to the appropriate unit schematic and parts location diagrams to aid in identifying the defective part or unit for replacement. When the trouble is apparently corrected, repeat all steps in the PMP's up to the point where the malfunction indication was first discovered to be certain that no other malfunction has been caused by the replacement.

CAUTION

Use low-wattage soldering iron (25 watts max.) when soldering connections or semiconductors. Connect a heatsink to leads on semiconductor before applying soldering iron.

NOTE

Failure is often caused by marginal performance of a part which is not obviously defective itself. When troubleshooting, consider what circumstances could have caused the failure, then critically examine those parts likely to be at fault.

Extreme caution should be exercised when working in the area of the transport encoder.

The transport encoder is very shock-sensitive. If any hammering or shaft-moving type maintenance is to be performed in the vicinity of the encoder, remove the encoder and replace it after maintenance has been completed.

Step	Procedure
1	Ensure that tape ends to be spliced are square and both tapes are same size (see figure 6-27).
2	Ensure that left and right edges of spliced tapes are parallel. Maximum skew of 2 degrees acceptable.
3	Use a nonbleed, clear transparent tape on nonread side.
4	Ensure that read fields are a minimum of $1/2$ inch from either side of splice.
5	Splices may be either butt or overlapped. Overlapped splices shall have an over- lap of less than 1/8 inch and trailing edge of leading tape shall be under leading edge of trailing tape.

TABLE 6-20. JOURNAL TAPE (OPTION) SPLICING

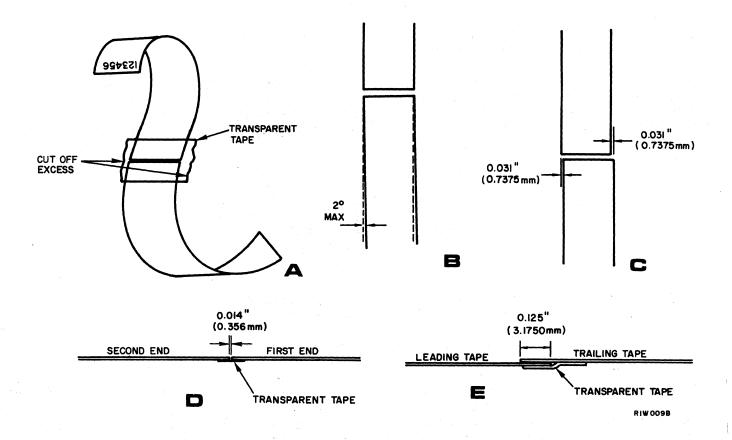


Figure 6-27. Journal Tape (Option) Splicing Restrictions

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DOCUMENT TRANSPORT SYSTEM

The document transport system consists of the feedup table, feeder, edger, conveyor, takeaway, and sort pockets.

CAUTION

To prevent inadvertant breaking or damaging of the Transport Encoder when any maintenance or disassembly is performed along the Encoder Driveshaft Assembly, the following procedure should be followed: Refer to figure 6-28.

- 1. Loosen split coupling and pillow block mounting hardware.
- 2. Slide Encoder Driveshaft so that .06 to .12 inches gap exists between Driveshaft and Encoder Shaft.
- 3. Tighten split coupling hardware <u>first</u>; then tighten pillow block hardware (<u>after</u> coupling is tightened).
- 4. Remove Encoder Drive flexible coupling and remount encoder. Check alignment of Encoder Driveshaft and Encoder Shaft.
- 5. If shafts do not align properly visually (i. e., approximately within .01 to .02 inches of each other) from all angles, the following steps (6 through 8) must be worked. If alignment seems visually acceptable, reassembly starting at step 8.
- 6. Remove encoder mounting plate and open the three mounting hole to . 312 diameter (from . 213 diameter).
- 7. Reassembly finger tight and adjust encoder until the two shafts are visually aligned. If they will not visually align properly, this will show that the self-aligning pillow block is frozen and must be broken free. (This may be accomplished by removing the pillow block and shaft from the machine and working the pillow block in a vise (with grease) until it pivots under a torque of no more than 50 inch pounds.)
- 8. Remove Encoder and Mounting Plate together and slip on the flexible coupling.
- 9. Leave the three mounting plate screws finger tight and adjust the encoder plate assembly until the flexible coupling slides <u>easily</u> back and forth along the encoder and encoder driveshaft. When the encoder is in this position of the coupling (being able to slide easily), tighten the three mounting screws. Check the sliding of the coupling after the mounting screws are tightened to ensure against slippage during tightening.

10. Tighten the coupling set screws.

Timing Belts Replacement

The intermediate timing belt shown in figure 6-40 is replaced by performing the procedures in table 6-21. The other timing belts shown in figure 6-40 can be removed by relieving the tension on affected shafts. After replacing belts, perform Timing Belt Adjustment Procedure in table 6-37.

* THESE TWO SHAFTS SHOULD VISUALLY BE ALIGNED (i.e: CENTERLINES WITHIN .0I TO .02 TO EACH OTHER)



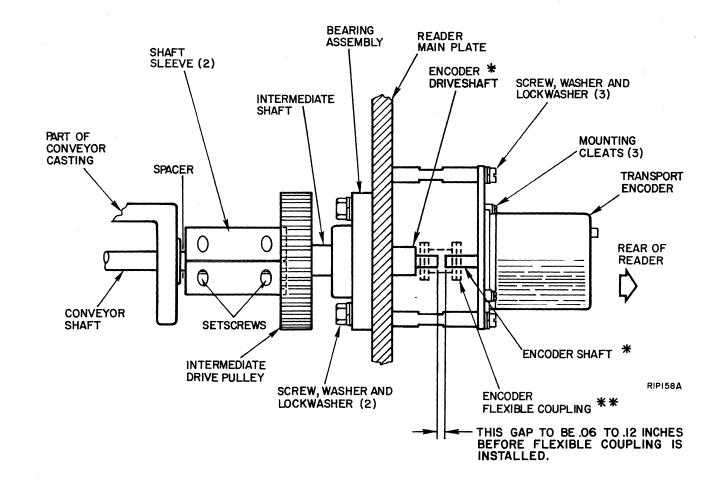


Figure 6-28. Transport Encoder Disassembly

6-122

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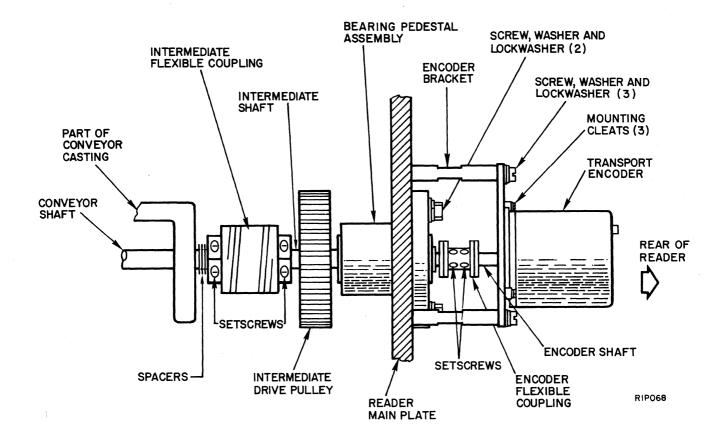
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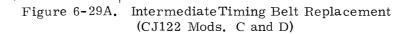
Step	Procedure
1	Deenergize reader.
2	Remove rear vertical and center front panels.
3	Swing out logic rack.
4	Loosen setscrews in encoder flexible coupling which secure encoder shaft as shown in figures 6-29A (CJ122 Mods. C and D) and 6-29B (CJ122 Mods. E, F, G, H, J, and K).
5	Loosen mounting cleats securing transport encoder and turn cleats 180 degrees. Remove transport encoder.
6	Loosen setscrews on intermediate coupling.
7	Loosen setscrew on intermediate drive pulley.
8	Remove feeder drive timing belt by relieving tension on feeder idler pulley shown in figure 6-40.
9	Loosen mounting screws on drive pulley assembly.
10	Remove bearing pedestal assembly mounting screws, lock washers, and washers.
11	NOTE
	Intermediate drive pulley contains a key which may fall when shaft is removed.
	Pull bearing pedestal assembly back away from mainplate until intermediate drive pulley is released from the intermediate shaft.
12	Remove intermediate timing belt.
13	Install new intermediate timing belt over drive pulley assembly and on intermedi- ate drive pulley.
14	Position pulley next to intermediate flexible coupling (CJ122 Mods. C and D) or shaft sleeve (CJ122 Mods. E, F, G, H, J, and K). Place key in shaft keyway and and push bearing pedestal assembly towards mainplate, ensuring that shaft goes into pulley and key is inserted into pulley keyway. Ensure that shaft goes into intermediate flexible coupling or shaft sleeve.
15	Tighten setscrew in intermediate drive pulley.
16	Secure bearing pedestal assembly with washers, lock washers, and mounting screws.

TABLE 6-21. INTERMEDIATE TIMING BELT REPLACEMENT PROCEDURE

TABLE 6-21. INTERMEDIATE TIMING BELT REPLACEMENT PROCEDURE (CONT'D)

Step	Procedure
17	Tighten setscrews in intermediate coupling or shaft sleeve, ensuring that set- screws are seated on flats on the shaft.
18	Adjust tension on intermediate timing belt. (Refer to table 6-37.) Check tension on main drive timing belt on opposite side of mainplate. Adjust if necessary. (Refer to table 6-37.)
19	Replace feeder drive timing belt and adjust tension. (Refer to table 6-37.)
20	Replace transport encoder, ensuring that shaft is in encoder flexible coupling and aligned with intermediate shaft.
	Replace mounting cleats.
21	Swing logic rack back into reader.
22	Replace panels.





6-123

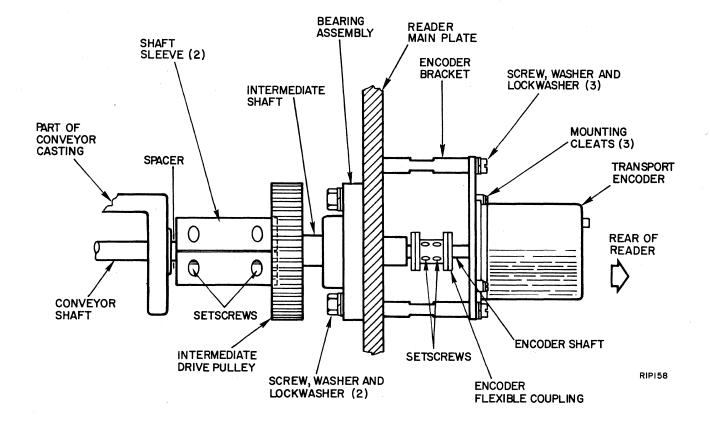


Figure 6-29B. Intermediate Timing Belt Replacement (CJ122 Mods. E, F, G, H, J, and K)

Feedup Table

Clutch Replacement

The feedup clutch is a replaceable unit located at the rear of the feedup table. Table 6-22 lists the replacement procedures.

TABLE 6-22. FEEDUP CLUTCH REPLACEMENT PROCEDURE

Step	Procedure
1	Deenergize reader.
2	Remove right side, buffer controller front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Remove front housing of feedup table by pulling housing straight out from table.
5	CAUTION
	DO NOT move edging walls on feedup table or edger when side guide drive chains are removed.
	Loosen nut holding chain idler sprocket, figure 6-30, to relieve chain tension.
	Remove side guide drive chain.
6	Remove leveling pad mounting screws (2 each pad) from under buffer controller frame.
7	Slide feedup table to rear until clutch bracket mounting screws are clear of controller frame.
8	Loosen coupling setscrews on clutch shaft shown in figure 6-30.
9	Disconnect wire leads of clutch from terminal block.
10	Remove clutch assembly from feedup table by removing screws (4) from under feedup table pan.
11	Remove takeup bracket from clutch assembly.
12	Mount takeup bracket to new clutch assembly.
13	Install new clutch assembly in reverse order of removal (steps 10 through 2).

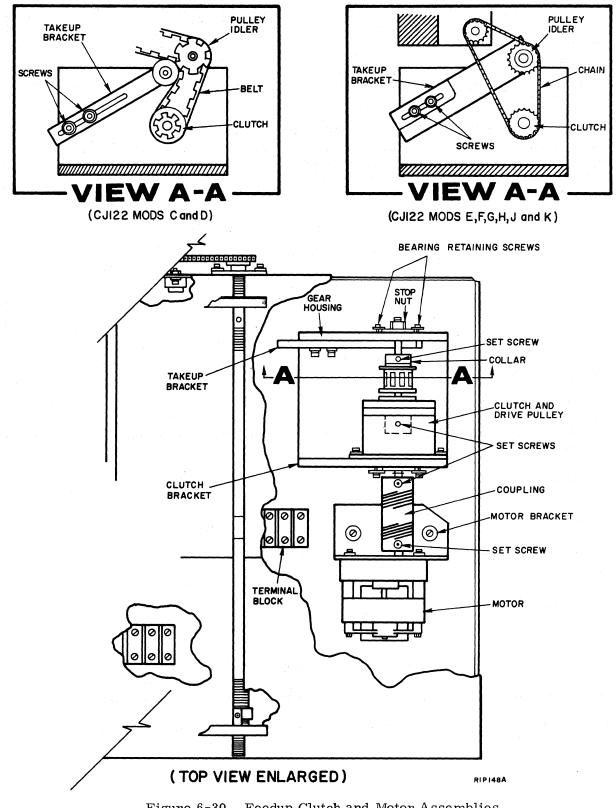


Figure 6-30. Feedup Clutch and Motor Assemblies

Step	Procedure
1	Deenergize reader.
2	Remove right side, BC front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Loosen coupling setscrew, then coupling, shown in figure 6-30.
5	Disconnect wires from motor to terminal block.
6	Remove motor mounting bracket from feedup table.
7	Remove four screws holding motor to bracket.
8	Install new motor in reverse order of removal (steps 7 through 2).

TABLE 6-23. FEEDUP MOTOR REPLACEMENT PROCEDURE

TABLE 6-24. FEEDUP TABLE TIMING BELT REPLACEMENT PROCEDURE

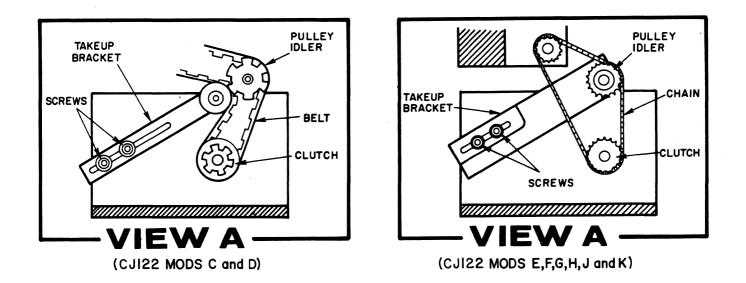
Step	Procedure
1	Deenergize reader.
2	Remove right side, BC front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Loosen two screws on takeup bracket shown in figure 6-30.
5	Remove stopnut and washer from end of clutch shaft.
6	Remove bearing retaining screws and slide bearing out of clutch bracket.
7	Remove timing belt by sliding belt along clutch shaft and through bearing slot.
8	Install new timing belt in reverse order of removal (steps 7 through 2).

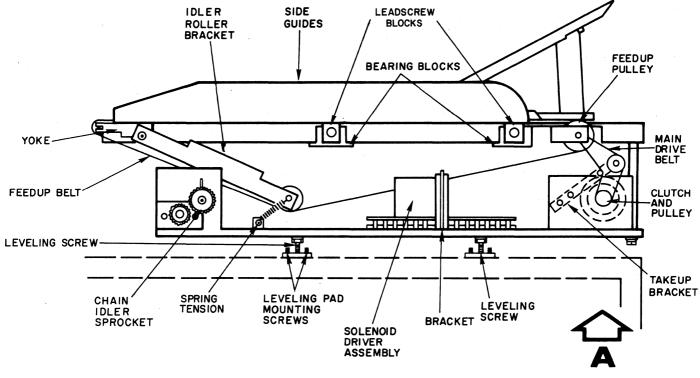
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Step	Procedure
1	Deenergize reader.
2	Remove right side, BC front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Remove front housing of feedup table by pulling housing straight out from feedup table. Remove nearside side guide from the leadscrew blocks.
5	CAUTION
	DO NOT move edging walls on feedup table or edger when side guide drive chains are removed.
	Loosen nut holding chain idler sprocket shown in figure 6-31. Remove side guide drive chain.
6	Remove eight screws (two each pad) from leveling pads. Slide feedup table to rear until clear of feeder assembly.
7	Release tension spring from idler roller bracket.
8	Slide feedup belt off rollers.
9	NOTE
	The feedup belt has been spliced. Install new belt with printed matter on inside and with splice positioned as shown in figure 6-32.
10	Install new feedup belt in reverse order of removal (steps 8 through 2).

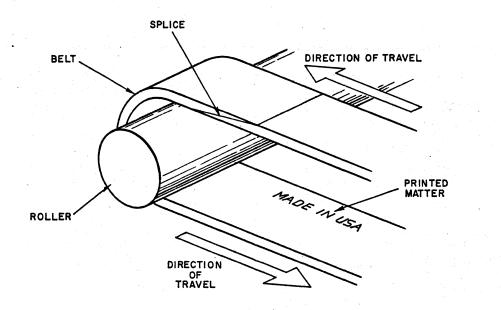
TABLE 6-25. FEEDUP BELT REPLACEMENT PROCEDURE





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Figure 6-31. Feedup Table



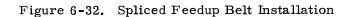


TABLE 6-26. FEED ROLLER REPLACEMENT PROCEDURE

Step	Procedure
1 1	Deenergize reader.
2	Remove right side, buffer controller front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Grasp feed roller shaft at the flat securely using wrench or vise grips.
5	Remove stop nut at the end of the shaft.
6	Slide entire yoke assembly off shaft, being careful not to lose small steel bushings between shaft and bronze bushings in yoke.
7	Replace feed rollers between yoke arms and slide yoke assembly onto feed roller shaft. Rotate feed rollers until D-hole in roller is aligned with shaft.
8	NOTE
	The Belleville spring washers and stop nut position the feed rollers and also provide clamping action needed to hold sprocket to feed rollers.
	Tighten stop nut until grooves in feed rollers are centered with lands on brushback rollers.

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Step	Procedure
1	Deenergize reader.
2	Remove right side, BC front, and center front panels.
3	Remove baffle plate in front of feedup table.
4	Turn DOCUMENT THICKNESS ADJUST knob on document adjustment panel to lower dedoubler rollers.
	NOTE
	The dedoubler coupling setscrews are difficult to get at; the best way is to remove the front portion of the feedup assembly and, using a 0.050 hex-screwdriver (P/N 12210905), reach in between the feedup belt. The transport drive can be rotated to gain access to all four setscrews.
5	Remove stop nut shown in figure 6-33.
	a. If dedoubler roller shaft has a slot in the end, hold shaft with narrow screw- driver while removing stop nut.
	b. If there is no slot in the end of the shaft, slide the feedup table away from the feeder assembly by performing Steps 2 through 6 of table 6-22 until the double universal joint is exposed.
	CAUTION
	Do not put stress on double universal joint when removing stop nut.
	Using vise grips, grasp the dedoubler shaft between the bearing block and the double universal joint shown on figure 6-33 and remove the stop nut and lock - washer.
6	Slide dedoubler roller off shaft and replace with new roller.
7	Replace lockwasher and stop nut.
8	Adjust dedoubler roller by performing procedures in table 6-38.
9	Reinstall feedup table by performing step 5b.
10	Readjust document height setting by performing steps 1 through 3 in table 6-40.
11	Readjust document thickness setting by performing step 7 of table 2-17, section 2.

TABLE 6-27. DEDOUBLER ROLLER REPLACEMENT PROCEDURE

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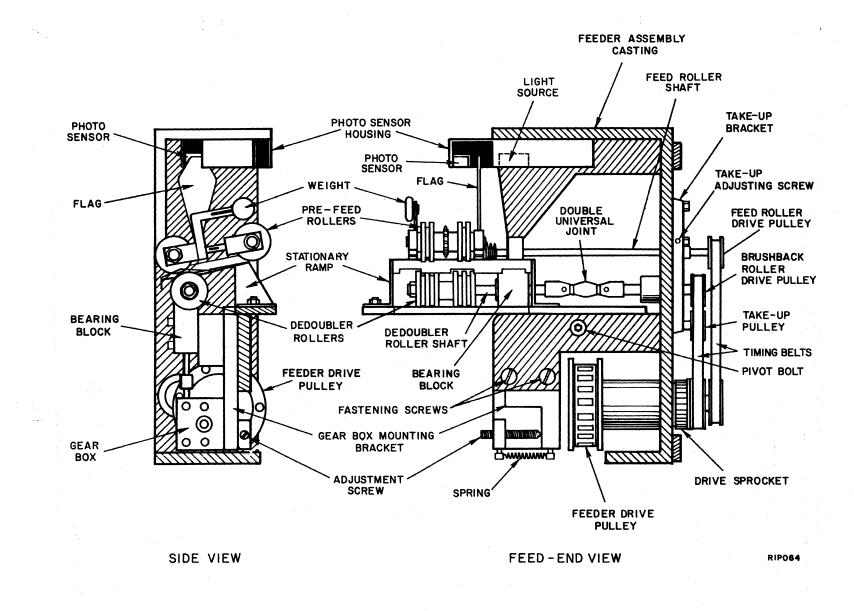


Figure 6-33. Feeder Assembly

6-132

Step	Procedure
1	Deenergize reader.
2	Remove feeder cover.
3	Remove retaining ring from one end of pre-feed roller shaft.
4	Push shaft through pre-feed yoke until pre-feed roller drops free.
5	Place chain around new pre-feed roller and place roller between yokes.
6	Insert shaft through yoke arms and roller.
7	Replace retaining ring.
8	Readjust document height, if necessary, by performing steps 1 through 3 in table 6-40.

TABLE 6-28. PRE-FEED ROLLER REPLACEMENT PROCEDURE

TABLE 6-29. CONVEYOR VACUUM BELT REPLACEMENT PROCEDURE

Step	Procedure
1	Deenergize reader.
2	Open stacker panel door and remove center front panel.
3	Remove hold-down bar located on conveyor at read station.
4	Loosen lock nut, then loosen tension adjustment screw until spring goes slack.
5	Slip conveyor vacuum belt out of guide rollers.
6	Remove edger timing belt by removing screws on intermediate pulley flange, then removing belt.
7	Remove plastic cable ties and disconnect any cables that trap belt.
8	Remove conveyor vacuum belt by sliding belt out over rollers.
	Raise edging wall slightly and slide belt under wall.
9	Install new conveyor belt in reverse order of removal (steps 8 through 2).
10	CAUTION
	Conveyor vacuum belt must not be pinched be- tween rollers.
	Turn adjustment screw in eccentric adjustment block (see inset, figure 6-34) so that spacing between main drive roller and takeup roller is 0.40 to 0.50 inch.
11	Turn tension adjustment screw against tension lever until spring is 4.75 inches long from end to end, then tighten locknut.
12	Check alignment of read zone light source.

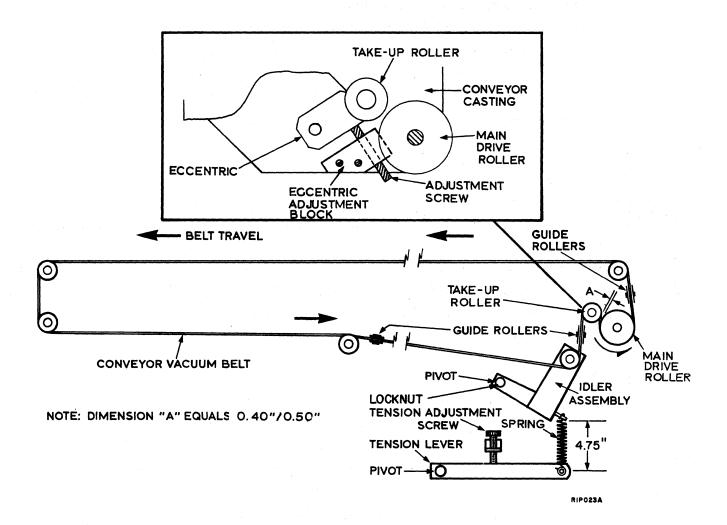


Figure 6-34. Conveyor Vacuum Belt

Step	Procedure
1	Deenergize reader.
2	Remove center front and front buffer controller panels.
3	Remove edger timing belt by loosening screws on edger timing drive pulley bracket, thus relieving tension on belt.
4	Remove side guide drive chain to feedup table by loosening nut holding chain idler sprocket, figure 6-31, thus relieving chain tension.
5	Turn tension screw counterclockwise to relieve tension on tension idler arm assembly.
6	Remove belt from guide rollers.
7	Slip belt off tension idler arm roller.
8	Raise edging wall slightly at conveyor and slide belt under wall.
9	Remove vacuum belt from edger.
10	Install new vacuum belt in reverse order of removal (steps 9 through 2).
11	Adjust vacuum belt tension to 8 pounds by extending springs 0.31 inch to 2.06 inches. (See figure 6-35.)
12	Readjust tension on edger timing belt by performing procedures in table 6-37.

TABLE 6-30. EDGER VACUUM BELT REPLACEMENT PROCEDURE

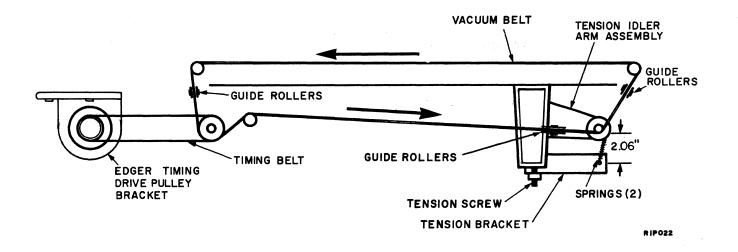


Figure 6-35. Edger Vacuum Belt Replacement

Takeaway System

The takeaway system, shown in figure 6-36, is comprised of a turnaround assembly, a turnaround guide assembly, and a takeaway vacuum belt. The turnaround assembly consists of a drum, guide roller, and a paper guide - all of which have a fixed position.

A screw on the bottom of the turnaround guide assembly is inserted into a long, slotted hole in the mounting bracket and secured by a large knob. The slotted hole allows the turnaround guide assembly to slide away from the turnaround assembly for ease in belt replacement or removing a possible paper jam.

The procedures for replacing the turnaround guide belt are listed in table 6-31, the procedures for replacing the takeaway vacuum belt are listed in table 6-32.

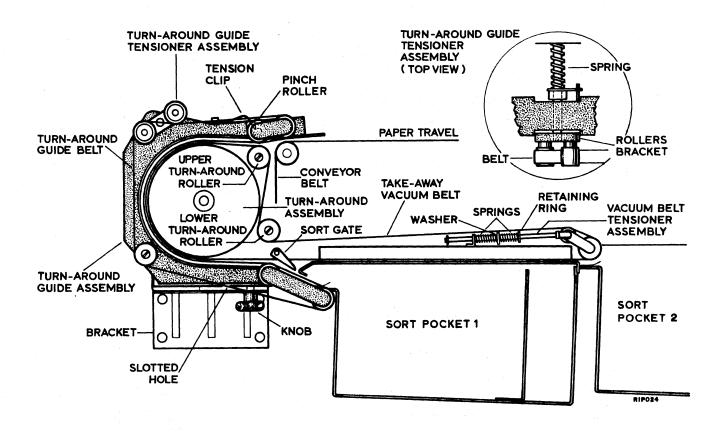


Figure 6-36. Takeaway System

TABLE 6-31. TURNAROUND GUIDE BELT REPLACEMENT PROCEDURE

Step	Procedure
1	Deenergize reader.
2	Open end panel and stacker panel doors.
3	Loosen knob and slide turnaround guide assembly out until it stops.
4	Remove worn turnaround guide belt.
5	NOTE
	Turnaround guide belt has been spliced. Install new belt with printed matter on inside and with splice positioned as shown in figure 6-32.
	Thread new turnaround guide belt around all rollers except turnaround guide tensioner assembly rollers and drum.
6	Set tensioner assembly turning rollers bracket 1 turn counterclockwise (looking at machine from front).
7	Holding bracket, thread belt on turnaround guide tensioner assembly rollers as shown in figure 6-36. Release bracket slowly.
8	CAUTION
	Do not push turnaround guide assembly in hard or microswitch may be damaged.
	Push turnaround guide assembly slowly towards drum until assembly stops. Tighten knob.

1

TABLE 6-32, TAKEAWAY VACUUM BELT REPLACEMENT PROCEDURE

Step	Procedure
1	Deenergize reader.
2	Open end panel and stacker panel doors.
3	CAUTION
	Turnaround guide assembly will spring out (under spring tension) when knob is removed. Do not drop.
	Remove knob and remove turnaround guide assembly from reader.
4	Press vacuum belt tensioner assembly down to relieve tension on belt. Remove old belt.
5	NOTE
	Takeaway vacuum belt has been spliced. Install new belt with printed matter on inside and with splice positioned as shown in figure 6-32.
	Install new belt by threading around upper turnaround roller, vacuum tensioner assembly roller, and drum as shown in figure 6-36.
	n en
6	Compress springs on vacuum belt tensioner assembly and stretch belt under lower turnaround roller.
7	CAUTION
	Turnaround guide assembly will spring out (under spring tension) when knob is removed. Do not drop.
	Replace turnaround guide assembly and tighten knob.

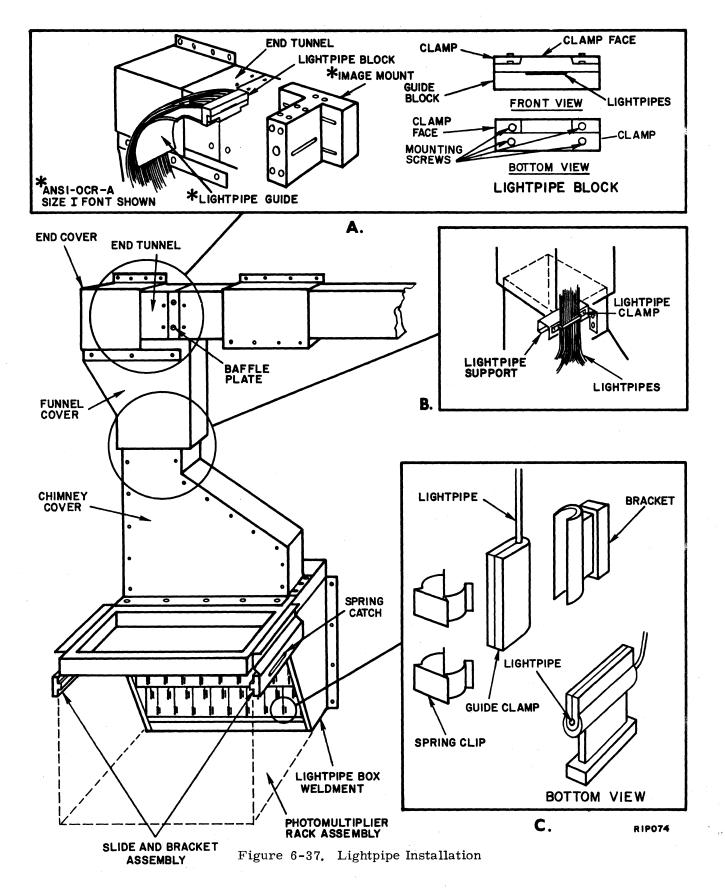
Step	Procedure
1	Deenergize reader.
2	Remove rear vertical panel.
3	Swing out logic rack.
4	CAUTION
	Remove J5 and J6 connectors at bottom rear of photo- multiplier rack assembly before removing rack, and J01, J02, and J03 on right side.
	Press spring latch on side of each slide and bracket assembly and carefully slide photomultiplier rack out of reader.
5	Visually ensure that lightpipe brackets shown in figure 6-37A are vertically aligned. Check that ends of lightpipes, guide clamps, and brackets are flush.
6	CAUTION
	Use extreme care when removing covers, etc., as lightpipes are very fragile.
	Remove following in listed sequence by removing attaching screws:
	 a. end cover b. funnel cover c. chimney cover d. baffle plate e. end tunnel
7	Remove spring clamps and guide clamp holding defective lightpipe from bracket.
8	Remove lightpipe from guide clamp.
9	Loosen screw on end of lightpipe clamp closest to defective lightpipe, figure 6-37B, approximately 1/4 turn.
10	Pull defective lightpipe up through clamp.
11	Loosen two screws attaching lightpipe block to image mount and pull block back away from image mount.
12	Loosen, 1/8 turn, two clamp face mounting screws in lightpipe block, figure 6-37A.

TABLE 6-33. LIGHTPIPE REPLACEMENT PROCEDURE

2

TABLE 6-33. LIGHTPIPE REPLACEMENT PROCEDURE (CONT'D)

Step	Procedure
13	Carefully pull defective lightpipe out of lightpipe block.
14	CAUTION
	Do not touch ends of new lightpipe. Do not bend lightpipe in a radius less than 4 inches or lightpipe may break.
	Place one end of new lightpipe in bracket at photomultiplier rack, figure 6-37C. Feed lightpipe up through lightpipe clamp in lightpipe chimney.
	CAUTION
	Ensure that lightpipe does not cross over other lightpipes as lightpipe is threaded through foam.
	Thread lightpipe through foam into empty slot in lightpipe block until end extends 1/4 inch out other side.
	Press lightpipe back into block with back of thumbnail until lightpipe end is flush with block and clamp face.
15	Ensure that other lightpipes are in their proper positions.
16	CAUTION
	Do not over-tighten screws in clamp face. Light- pipes could be damaged.
	Tighten clamp face screws approximately 1/8 turn or until snug.
17	Replace lightpipe block in image mount and tighten mounting screws.
18	Insert bottom end of lightpipe into guide clamp ensuring that end of lightpipe is flush with end of clamp.
19	Insert guide clamp into bracket, ensuring that bottom ends of clamp and bracket are flush.
20	Visually ensure that lightpipe brackets shown in figure 6-37A are vertically aligned. Check that ends of lightpipes, guide clamps, and brackets are flush.
21	Reassemble in reverse order of removal (steps 6 through 1).
22	Perform procedures in PMP 2.3 to ensure optics assembly is operational.

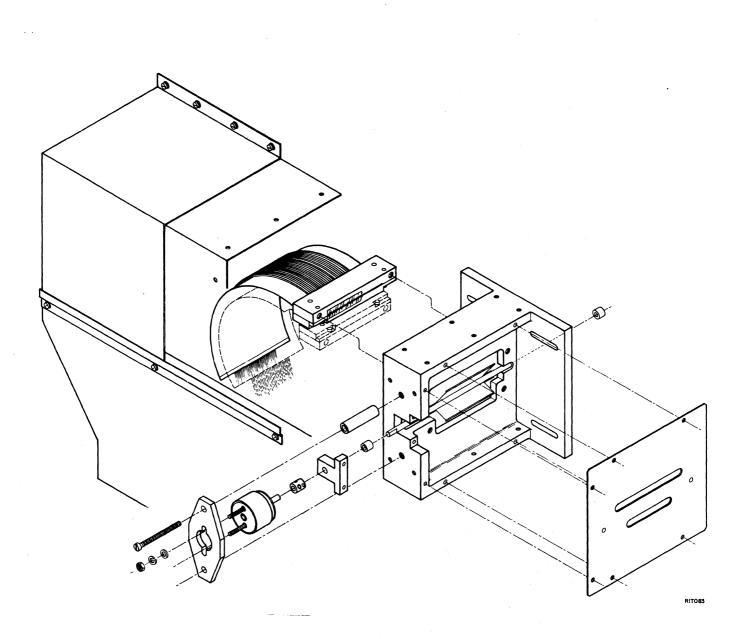


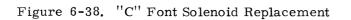
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Step	Procedure
1	Deenergize reader.
2	Remove rear vertical panel.
3	Swing out logic rack.
4	Disconnect leads to solenoid.
5	Loosen two setscrews that attach coupling (see figure 6-38).
6	Remove two screws that hold solenoid mount to image mount. Solenoid, solenoid mount, and spacers will come free.
7	Remove solenoid from mount.
8	Attach new solenoid to mount.
9	Check setscrew that holds coupling to shutter to ensure that it is tight.
10	Reattach solenoid mount and spacers.
11	Connect leads to solenoid.
	CAUTION
· · · · · · · · · · · · · · · · · · ·	If the shutter is not positioned as described above, it will not operate correctly and/or the solenoid life will be shortened considerably.
12	Solenoid should be attached to coupling as follows:
	a. Turn'shutter to extreme clockwise position (from rear of machine); shutter will rest lightly on foam bumper; it should not be pressed into bumper during this procedure.
	b. Position shutter such that it strikes the image mount toward the front of the machine. Back off 0.010 to 0.015 inch.
	c. Hold solenoid by hand in actuated position (extreme clockwise).
	d. Tighten setscrews that attach coupling to solenoid.
	e. Actuate and release solenoid slowly by hand. Check that there is no binding (shutter against image mount) and that the solenoid reaches the end of its clockwise stroke without meeting resistance from the shutter hitting the bumper.

TABLE 6-34. "C" FONT SOLENOID REPLACEMENT PROCEDURE





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TRANSISTOR REPLACEMENT

Some models of the transport power amplifier assembly use a long threaded bolt for mounting the power transistors, and a resistor is mounted on the excess length of the bolt. When necessary to replace the power transistor on this model, reverse the bolt when reassembling so that the nut is against the transistor case.

TABLE 6-35. TRANSISTOR REPLACEMENT PROCEDURE

Step	Procedure
1	Remove retaining bolts and remove transistor.
2	Clean area where transistor is to be mounted (heat sink).
3	Coat the bottom of the new transistor with silicone grease (Dow Corning 4 Com- pound) prior to mounting.
4	Mount and solder leads of new transistor.
5	Perform steps of tables 6-50 and 6-51.

REPLACEMENT OF DEFECTIVE OCER CARDS

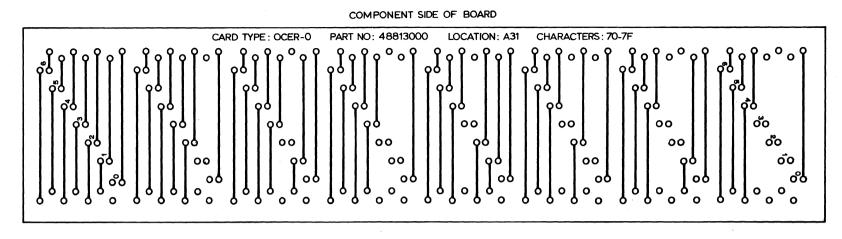
Beginning with CJ122 Serial Number 120 (CJ122 Mods. C02 and above), only one OCER card is supplied for spares. This one OCER card can be modified for use in any of the OCER locations.

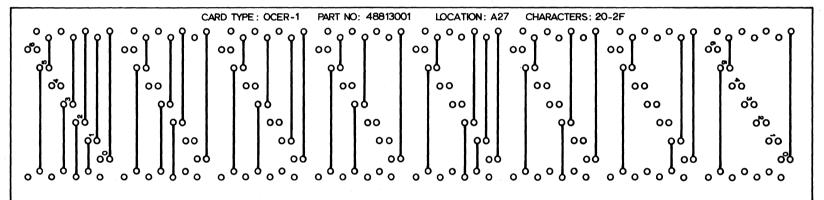
OCER card, Part No. 48813000, is supplied as a spare. Should it be necessary to replace any of the OCER cards, use the procedure in table 6-36.

TABLE 6-36.	DEFECTIVE	OCER	CARD	REPLACEMENT	PROCEDURE
		00110	C		

Step	Procedure
1	Determine which of the wiring configurations shown in figure 6-39 applies to the card to be replaced.
2	Remove wires (4, 5, or 6) from OCER card, CDC P/N 48813000, so that the wiring configuration agrees with the OCER card that is to be replaced.
	NOTE
	Wires 0, 1, 2, and 3 are of the same configuration for all OCER cards.
3	Identify this card with the part number of the OCER card that it is replacing.

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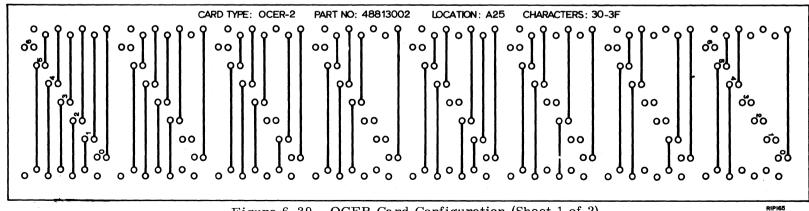


Figure 6-39. OCER Card Configuration (Sheet 1 of 2)

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COMPONENT SIDE OF BOARD

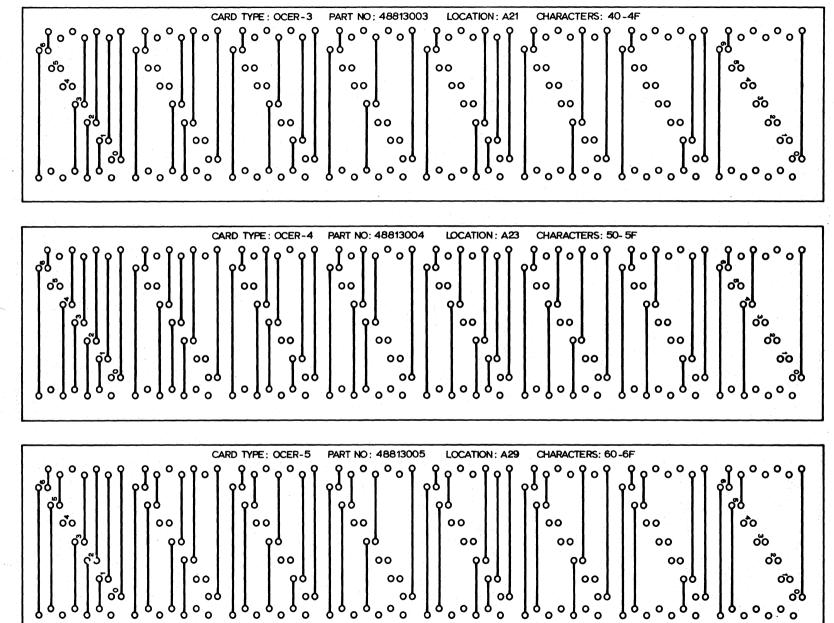


Figure 6-39. OCER Card Configuration (Sheet 2 of 2)

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REPLACEMENT OF TRANSPORT DRIVE MOTOR

Should it be necessary to replace a transport drive motor, do not replace only the motor itself; replace at the next higher assembly. The transport motor plate assembly includes the motor.

CALIBRATION AND ALIGNMENT PROCEDURE

Tables 6-37 through 6-55 provide procedures for checking individual units of the CJ122 Reader. Tests of individual units should be performed every 6 months or whenever the individual unit has undergone extensive repair. The steps must be performed in the sequence presented, since each step depends upon proper operation of components tested by previous steps.

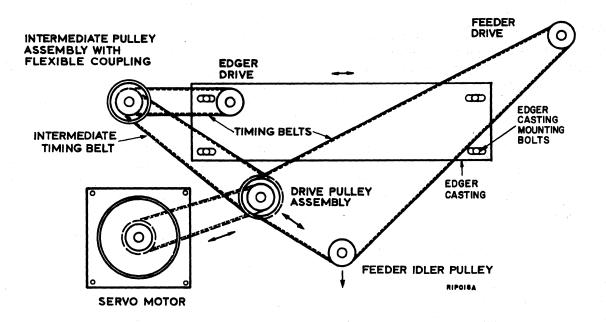
If the normal indication is not obtained for a particular step, refer to the instructions in the Procedure column. These instructions will be either to check specific components or to refer to a troubleshooting table. If the instructions are to check a specific component, check all wiring associated with the component to isolate the fault to the specific component or the associated wiring. Whenever a fault has been detected and repaired, repeat the check and alignment procedure to make sure that all normal indications are obtained. If reference is made to a troubleshooting table, proceed to the step and action in the troubleshooting table referenced, find the applicable symptom, isolate and repair the fault, and repeat the check and alignment procedures.

TIMING BELTS ADJUSTMENT

The transport system drive is applied from the servo motor to the main drive pulley assembly. The feeder and edger assemblies are driven by the main pulley. An intermediate pulley assembly with a flexible coupling (to compensate for the slight angle of the edger rollers and belt) transfers the drive from the main pulley to the edger. Timing belt adjustment procedures are listed in table 6-37 and shown in figure 6-40.

Step	Procedure
1	Apply a 1- to 2-pound force at the center of the belt. Short belts should deflect from $1/16$ to $1/8$ inch; feeder drive belt should deflect $3/16$ inch.
2	Adjust edger drive belt by loosening four edger casting mounting bolts and moving edger casting in direction of arrows.
3	Adjust intermediate timing belt tension by moving drive pulley assembly in direction of arrows.
4	Adjust feeder drive belt tension by moving feeder idler pulley in direction of arrow.
5	Adjust servo motor belt by moving servo motor in direction of arrows.
	NOTE
	Check tension on corresponding belts when adjust- ing tension on any timing belts. Belt tension is interrelated due to common pulley shafts or ad- justment points.

TABLE 6-37. TIMING BELT ADJUSTMENT PROCEDURE



NOTE : -- BELT TENSIONING ADJUSTMENT DIRECTION

Figure 6-40. Timing Belts Tension Adjustments

TABLE	6-38.	DEDOUBLER	ROLLER	PARALLEL
	A	DJUSTMENT F	ROCEDU	RE

Step	Procedure
1	Deenergize reader.
0	
2	Remove right side, BC front and center front panels.
3	Remove baffle plate in front of feedup table.
4	Remove front of feedup table to provide access to adjusting and fastening screws of feeder assembly shown in figure 6-33.
5	Loosen fastening screws.
6	Adjust dedoubler roller by turning adjustment screw at bottom of assembly. Repeat step 3 in PMP 2.1.
7	If rollers become too tight, readjust document thickness setting by performing procedures in table 2-17, section 2.

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TABLE 6-38. DEDOUBLER ROLLER PARALLEL ADJUSTMENT PROCEDURE (CONT'D)

Step	Procedure
8	Repeat step 3 in PMP 2.1.
9	When rollers are parallel, tighten fastening screws.
10	Repeat step 3 in PMP 2.1.
11	Check that grooves in feed rollers are centered with lands on dedoubler rollers. If not, adjust by loosening or tightening stopnut on feed roller shaft shown in figure 6-41A.
12	Repeat step 3 in PMP 2.1.
13	Replace front of feedup table.

TABLE 6-39. STATIONARY RAMP ADJUSTMENT PROCEDURE

Step	Procedure
1	Move feedup table away from f eeder assembly by performing steps 1 through 7 in table 6-22.
2	Check that ramp mounting bracket is properly secured to feeder casting.
3	Loosen screws securing stationary ramp to mounting bracket.
	NOTE
	If adjustments in steps 4, 5, and 6 cannot be made using stationary ramp slots, loosen ramp mounting bracket screws and make necessary adjustments.
4	Slide ramp on slotted holes until dedoubler roller extends above ramp approxi- mately 0.005 inch.
	NOTE
	If 0.005 inch cannot be obtained by moving ramp, add or remove shims between ramp and mounting bracket as required.
5	Check that stationary ramp is centered on dedoubler roller. If not, readjust ramp.
6	Check that stationary ramp is parallel to edger plate as shown in figure 6-41D. If not readjust ramp.

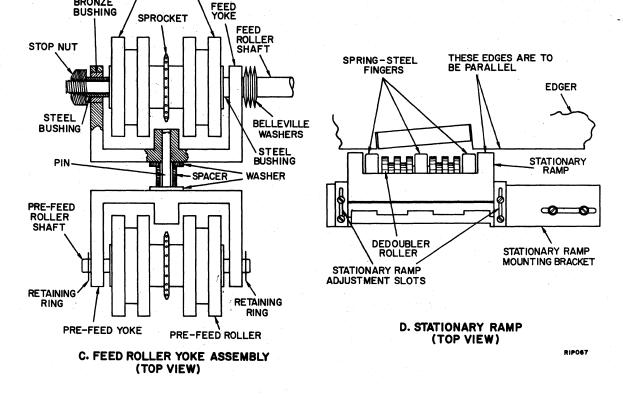


Figure 6-41. Feeder Adjustments

A. ROLLER WEAR (FEED-IN VIEW)

BRONZE

FEED ROLLERS

B. CRITICAL FEEDER SETUP DIMENSIONS (SIDE VIEW)

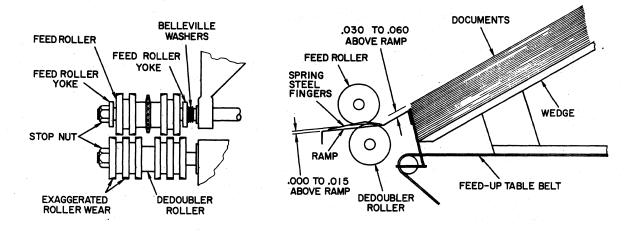


TABLE 6-39. STATIONARY RAMP ADJUSTMENT PROCEDURE (CONT'D)

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Step	Procedure		
7	Tighten all screws and recheck dimension obtained in step 4.		
8	Check flag position. Refer to steps 1 through 3 in table 6-40.		
9	Move feedup table into mounting position on buffer controller and check that feedup belt is positioned inside stationary ramp so that rubber strips on belt are centered in slots in ramp and do not bind on ramp. If necessary, adjust ramp by moving in slots (see figure 6-41D).		
	Move feedup table into mounting position and adjust leveling pads. (Feedup table will be 0.060 to 0.090 inch above edger.)		

TABLE 6-40. GENERAL FEEDER ADJUSTMENT PROCEDURE

Step	Procedure
	Document Height Adjustment
1	Place documents on feedup table at same angle as wedge. Document height above stationary ramp should be between 0.030 to 0.060 inch as shown in figure 6-41B.
2	Slightly loosen two screws attaching flag to feed yoke.
3	If too many documents are being fe d into feed and dedoubler rollers, move flag towards edger.
	If too few documents are being fed into feed and dedoubler rollers, move flag towards feedup table.
	NOTE
	If there is not enough play in flag mounting holes, move sensor towards feedup table if too many documents are fed and towards edger if too few documents are fed.
	Pre-feed Rate Adjustment
4	Turn weight on bracket of feed yoke to loosen weight.
5	If document gap is greater than 15 percent of document length, move towards feedup table.

TABLE 6-40. GENERAL FEEDER ADJUSTMENT PROCEDURE (CONT'D)

Step	Procedure
	CAUTION
	Do not use the DOCUMENT THICKNESS ADJUST knob on document adjust panel for adjusting docu- ment gap.
6	Load documents onto feedup table and run.
	Readjust weight if required.

CONVEYOR VACUUM BELT

For vacuum belt tension adjustment see figure 6-34 and table 6-29.

The conveyor vacuum belt tension must be set so that the belt lies flat and snug on the vacuum chamber. Too much tension causes the sides of the belt to curl as it passes underneath the conveyor. Not enough tension causes belt to lift, and when transport direction is changed there is no movement. Curling may cause excessive wear on the belt, requiring premature replacements. Refer to table 6-29 for replacement procedures.

VACUUM LEVEL CALIBRATION

The reader vacuum pressure is supplied by a low level, high volume system. The system supplies vacuum of 1.5 to 2.0 and 8 inches of water at nominal flow rate of 6 cubic feet per minute. One and one-half to 2.0 inches of vacuum is supplied to the edger; 8 inches of vacuum is supplied to the conveyor vacuum belt and stacker vaccum belts and is used for cooling by drawing air through the main drive motor.

Two vacuum blowers are housed in an enclosure located under the recognition rack. The enclosure is divided into two chambers - one for the 1.5- to 2.0-inch level and one for the 8-inch level. A damper between the two chambers and a relief valve on each chamber serve as individual adjustments and regulators for each level as shown in figure 6-42. Vacuum level calibration procedures are in table 6-41.

TABLE 6-41. VACUUM LEVEL CALIBRATION PROCEDURE	TABLE 6-41.	VACUUM LE	EVEL CALIBRA	TION PROCEDURE
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Step	Procedure
1	Check that fan is rotating in both vacuum pump motors to ensure that motors are running.
2	Check that all vacuum hoses are connected (figure 6-43) and connections are tight.
3	When either (but not both) of the two gauges indicates a variation in the vacuum level, adjust relief valve on chamber (see figure 6-42). If pressure in the other chamber is affected during this adjustment, readjust relief valve on other chamber.
4	If vacuum pressure in each chamber cannot be adjusted to proper level by adjusting relief valves, adjust vacuum gate between chambers (figure 6-42).

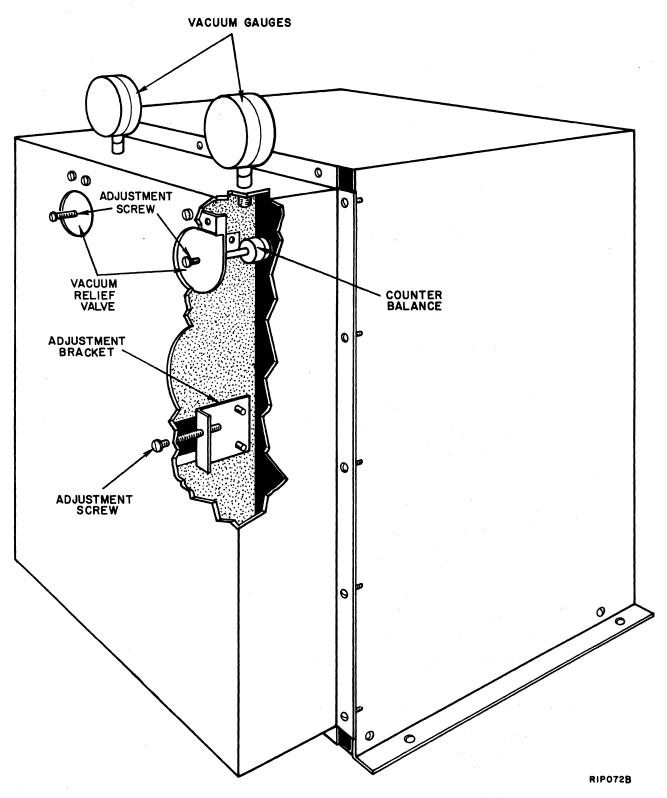


Figure 6-42. Vacuum Assembly Adjustments

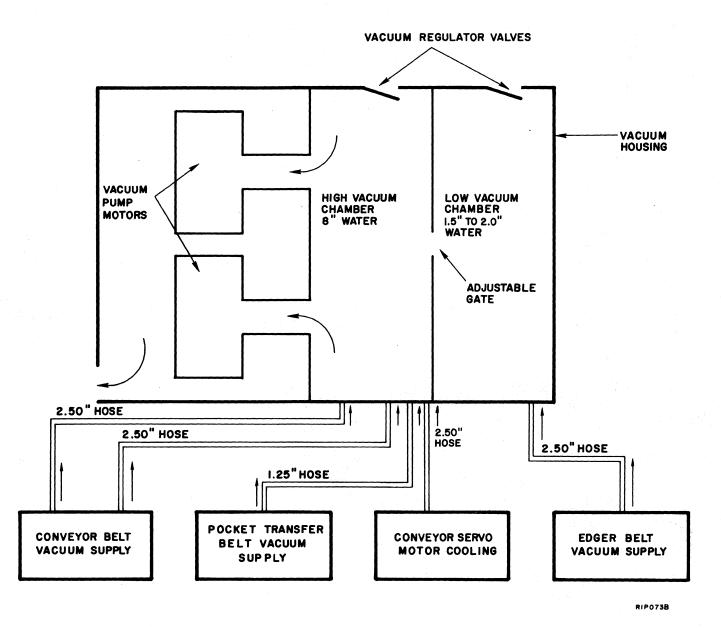


Figure 6-43. Vacuum Supply Connections

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MARKING PEN ALIGNMENT PROCEDURES

The marking pen alignment procedures are contained in table 6-42.

The marking pen is designed to be retracted away from the trough when not in use. There is a tab on the bracket on which the marking pen solenoid is mounted that prevents the bracket from revolving and interfering with the scanning mirror.

When the marking pen is raised away from the trough it is possible to raise the pen so far that the stop tab will not prevent the bracket from revolving and striking the scanning mirror. The pen should not be raised so far that the stop tab is ineffective.

Step	Procedure			
1	Deenergize reader.			
2	Lift left hood.			
3	Rotate mounting clamp until marking pen is in appropriate location on document (see figure 6-44).			
	NOTE			
	Mounting clamp is held by spring tension so that rotational adjustments can be done without loosen- ing adjustment screws each time.			
	NOTE			
4	For on-line marking during page and document reading, the marking pen should be set as far to right on mounting clamp arm as possible.			
	If necessary, loosen horizontal adjustment screw and slide clamp bracket to right until it stops.			
	Tighten horizontal adjustment screw.			
	NOTE			
	For marking journal tape, the marking pen should be downstream of read area. Distance is deter- mined by program parameters.			
	Loosen horizontal adjustment screw and slide clamp bracket required distance to left.			
	Tighten horizontal adjustment screw.			
5	CAUTION			
	Marking pen must not be raised to extent that marker guide bracket clears the clamp bracket.			
	If necessary, loosen vertical adjustment screw and move marker guide bracket up or down until top of ink holder assembly is 5/64 inch above surface of conveyor trough.			

TABLE 6-42.	MARKING	PEN.	ALIGNMENT	PROCEDURE
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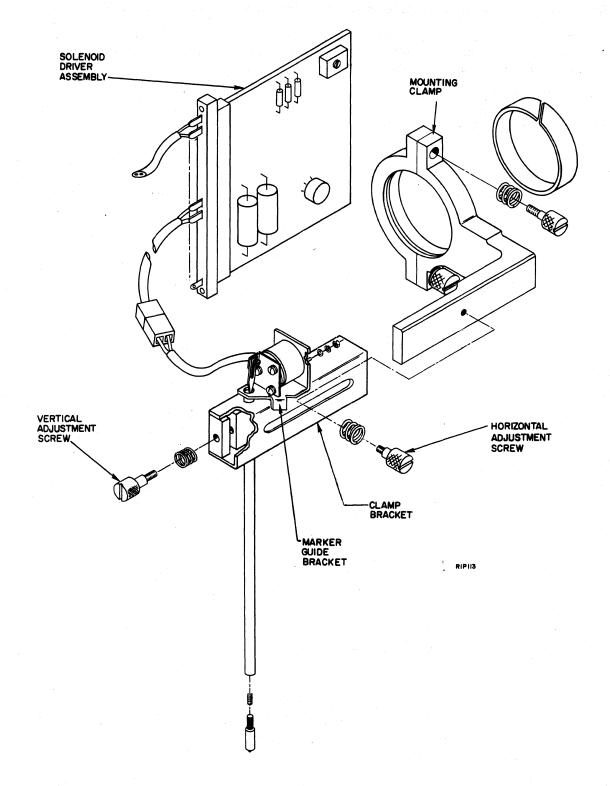


Figure 6-44. Marking Pen Option

Step	Procedure
1	Remove side guide drive chain from edger by loosening nut holding chain idler sprocket, figure 6-31 on feedup table.
2	Draw a line down the center of a document (any size within specified range).
3	Place document against edging wall of edger.
4	Adjust edger until line is aligned with center row of vacuum holes in conveyor trough.
5	Adjust paper guides on feedup table until outside guide is aligned to 3/16 inch inside of edging wall.
6	Adjust inside guide on feedup table so that test document fits inside the two guides (approximately 1/16 inch between document edges and guides).
7	Ensure that paper guides on feedup table are parallel with each other.
8	Replace side guide drive chain on edger.
9	Energize reader.
10	Place document (used in step 2) on feedup table.
	Adjust paper guides to 1/16 inch of document edges on feedup table by manipulating PAPER WIDTH ADJ. switch on document adjustment panel.
11	Press ENABLE FEED UP pushbutton switch.
	When LOAD pushbutton indicator lamp lights, press LOAD.
	Note that line on document is centered on conveyor as document travels to read area.
	If document is not centered, repeat alignment procedure.

TABLE 6-43. EDGER ALIGNMENT PROCEDURE

DOCUMENT SENSOR ALIGNMENT PROCEDURE

The procedure in table 6-44 is used to align the following document sensor circuits:

Feedup Sort entry Sort station 1 Sort pocket 1 full Sort station 2 Sort pocket 2 full

The sensor locations are shown in figure 6-45.

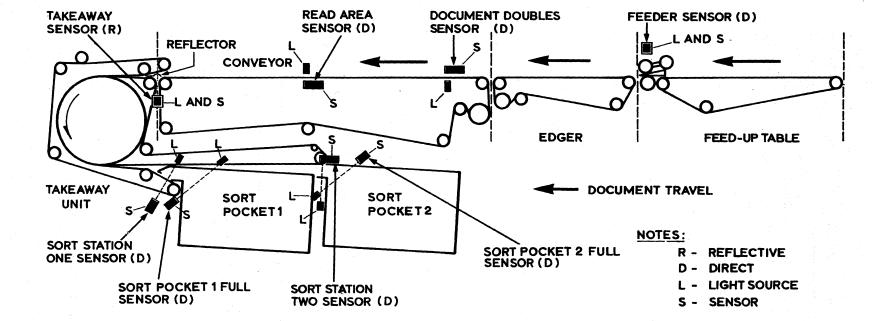


Figure 6-45. Locations of Document Sensors

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TABLE 6-44. DOCUMENT SENSOR ALIGNMENT PROCEDURE

Step	Procedure		
1	Connect digital voltmeter to TP-B on sensor unit as shown in figure 6-46.		
2	sensor unit and infrared ligh	oosening mounting screws and alternately adjusting t source until voltage appears maximum on TP-B no voltage change occurs refer to step 2, table 6-8.	
3	After maximizing voltage at TP-B cover the photocell with a single sheet of paper (use test document number 48705201) and monitor the level that TP-B drops to.		
4		adjust the potentiometer screw (see figure 6-46) until ay between the voltages read in steps 2 and 3. The roper operation.	
5	Connect test probe to the appropriate sensor unit output as follows:		
	Sensor	Output Check Location	
	Feedup Sort entry Sort station 1 Sort pocket 1 full Sort station 2 Sort pocket 2 full	5A 20-13 6E30-5 6D30-3 5C18-1 6D30-5 5C18-5	
6	sensor unit. Breaking the in	eak the infrared path between the light source and afrared path should cause the output voltage to change $+0.1V$. If this voltage change does not occur, refer	

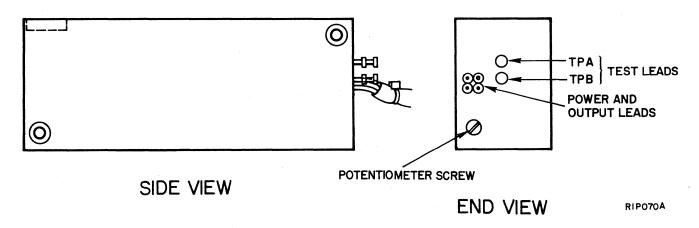


Figure 6-46. Document Sensor Connections

DOUBLES SENSOR ALIGNMENT PROCEDURE

To align the doubles sensor circuit consisting of an infrared light source, a doubles sensor, and a doubles remote circuit, perform procedures listed in table 6-45.

TABLE 6-45. DOUBLES SENSOR ALIGNMENT PROCEDURE

Step	Procedure
1	Verify that all required voltages are present on the sensor, remote sensor, and the source.
2	Connect the positive lead of the DVM to TP-C (figure 6-47, bottom of R4) of the remote sensor PC board (see figure 6-47). The remote sensor PC board is mounted on rear of document adjustment panel.
3	Ground negative lead of DVM.
4	Ground TP-A of doubles sensor.
5	Adjust R01 on doubles sensor for a reading of zero volts on the DVM and remove ground.
6	At the document adjust panel, set DOUBLES ADJUST Control to mid-range (6).
7	Loosen screws holding the doubles sensor and reposition until DOUBLES INDICATOR lamp at document adjust panel lights. If this indicator will not light, see table 6-9.
8	Insert one sheet of paper (normal weight as used in customer installation) under the doubles sensor. Adjust doubles sensor position until DOUBLES INDICATOR lamp goes out. Tighten doubles sensor screws.
9	Insert two sheets of paper under doubles sensor. Verify that DOUBLES INDICATOR lamp lights.

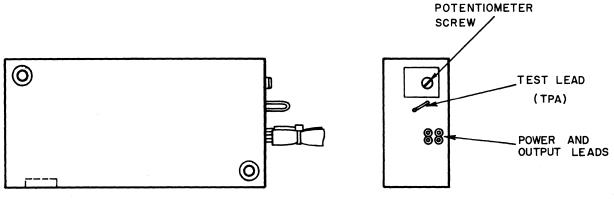
CONSTANT CURRENT CALIBRATION

The procedures for calibrating the constant current used to drive the common emitters are contained in table 6-46. The constant current is adjusted so that a common emitter transistor will turn on when its character matrix is nearest 0 vdc.

NOTE

Adjust LEMAL voltage according to table 6-47 before performing this procedure.

DOUBLES SENSOR



SIDE VIEW

END VIEW

DOUBLES REMOTE CIRCUIT

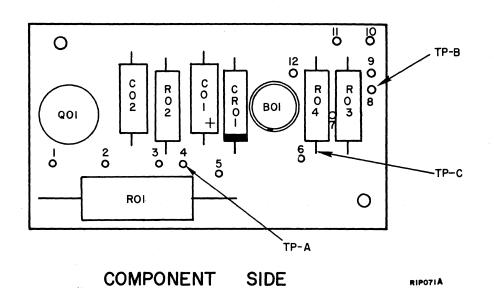


Figure 6-47. Doubles Sensor Connections

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TABLE 6-46. CONSTANT CURRENT CALIBRATION PROCEDURE

Step			Procedure		
1	Remove the font inhibit card (OFIR) from location A26 [†] or A51 [‡] .				
2	Ground A22 Pin 8^{\dagger} or B28 pin $8^{\dagger\dagger}$ (OCMR).				
3	Connect oscilloscope 10X test probe or DVM to A22 pin 4 [†] , or B28 pin 4 ^{††} (OCMR).				
4					
4	All recognition racks except CW167W04, CW209, CW210: adjust R17 on the character quantizer-constant current OCIR card (see figure 6-48) located at A20 ⁺ or on the 1CIR card, located at A 43 ⁺⁺ (see figure 6-49) until the signal changes from some negative voltage (-6 vdc maximum) to 0 \pm 0.02 vdc. CW167W04, CW209, CW210: adjust R17 on 1CIR card until voltage changes from some negative value to +0.65 \pm 0.12 vdc.				
5		/M lead on each of the orresponding pin, and	-		able below,
		DVM Monitor Pin	Ground Pin	Voltage	
		4	8		
		3	7		
		12	16		
		18	22		
		24	28		
		30	34		
		Sum of Volta	ages		
		Mean Val	ue		
6	Determine a	nd record the sum of	voltages measure	d at each pin.	
7	Divide the su	um of the voltages obt	ained in step 6 by	6 and record.	
8	By inspection of voltages recorded, determine which value is closest to mean value determined in step 8 and record in table				
9	Place the DVM lead on that pin determined in step 8.				
10	Ground the corresponding pin called out in the table.				
11	Adjust R17 on OCIR or 1CIR card so that the DVM indicates 0.0 \pm 0.02 volts.				
12	Connect the DVM monitor lead to pin No. 4 on the OCMR Card at A22 [†] or B28 ^{††} .				
**CJ	122 Mods. C01 122 Mods. D,	l and C02. E, F, G, H, I, J, an	d K.		· · · · · · · · · · · · · · · · · · ·

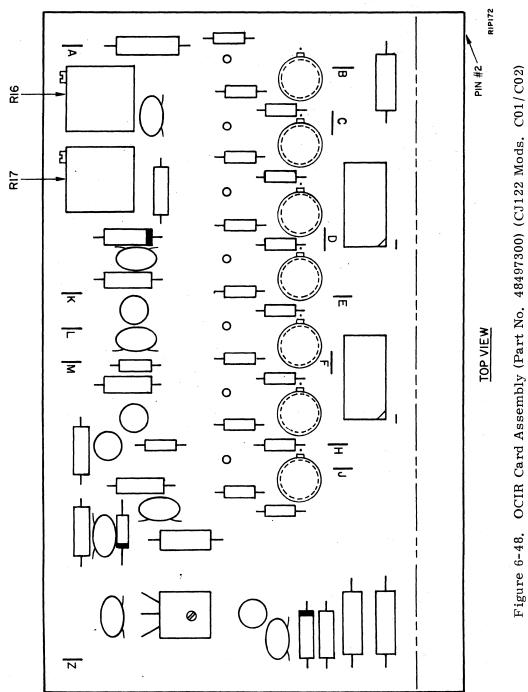


TABLE 6-46. CONSTANT CURRENT CALIBRATION PROCEDURE (CONT'D)

Step	Procedure
13	Ground pins 7 and 8 of the OCMR card (A22 ^{\dagger} or B28 ^{$\dagger\dagger$}).
14	Observe DVM reading. The value should be within -4.5 to -1.5 vdc.
15	Connect DVM to pin 3 of OCMR card.
16	Observe DVM reading. The value should be within -4.5 to 1.5 vdc.
17	Disconnect all DVM and ground connections.
18	Proceed to table 6-47.
[†] CJ	122 Mods. C01 and C02. 122 Mods. D, E, F, G, H, I, J, and K.

TABLE 6-47. LEMAL CALIBRATION PROCEDURE

Step	Procedure
1	Connect 10X oscilloscope probe or DVM to TP-2 of the constant current card OCIR at location A20 [†] or to TP-r on 1CIR located at A43 ^{††} .
2	All recognition racks except CW167W04, CW209, CW210: adjust R21 on the OCIR or 1CIR board for $+2.3 \pm 0.3$ vdc (the lower the voltage nearer ground the better the character match must be to be read out), minimum setting $+2.0$ vdc; maximum $+3.0$ vdc. (See figure 6-48 or 6-49.) Recognition racks CW167W04, CW209, CW210: adjust R21 on the 1CIR card for $+3.15 \pm 0.35$ vdc, maximum $+3.5$ vdc, minimum $+2.8$ vdc.
3	Disconnect oscilloscope or DVM.
4	Proceed to table 6-48.
	122 Mods. C01 and C02. 122 Mods. D, E, F, G, H, J, and K.

CHARACTER QUANTIZER REFERENCE VOLTAGE CALIBRATION

The procedures for calibrating the character quantizer reference voltage level are contained in table 6-48.

TABLE 6-48.	CHARACTER QUANTIZER REFERENCE VOLTAGE
	CALIBRATION PROCEDURE

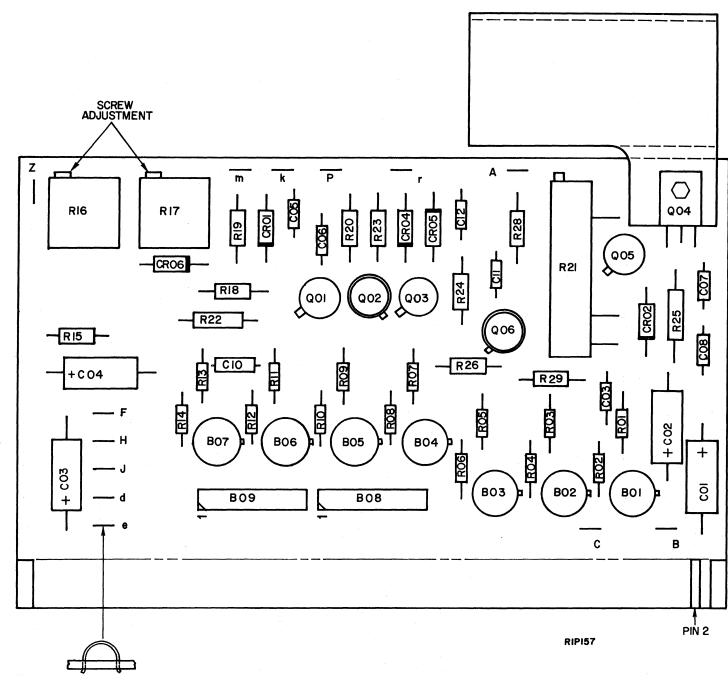
Step	Procedure		
1	Remove character quantizer-constant current card OCIR located at recognition rack location A20 [†] or 1CIR located at A43 ^{††} and insert extender card between location and card (see figure 6-48 or figure 6-49.		
2	Connect oscilloscope 10X test probe to junction R15 and R16 on character quantizer- constant current card.		
3	Adjust R16 until observed voltage is -3 ± 0.01 vdc.		
4	Disconnect oscilloscope.		
5	Remove extender card and reinsert character quantizer-constant current card at recognition rack location.		
6	Reinsert font inhibit card (OFIR) removed in table 6-46, step 1.		
	[†] CJ122 Mods. C01 and C02. [♥] CJ122 Mods. D, E, F, G, H, J, and K.		

MIRROR ENCODER CALIBRATION

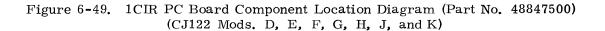
Procedures for calibrating the mirror encoder are contained in table 6-49. Ensure that test document is centered in read area and that specified mirror coordinates are correct before calibrating encoder.

TABLE 6-49. MIRROR ENCODER CALIBRATION PROCEDURE

Step	Procedure
1	CAUTION
	Do not remove encoder cover.
	Loosen four mounting screws on mirror encoder.
2	Perform PMP 3.1.
	NOTE
	The mirror encoder adjustment is very sensitive and requires little movement of the mirror encoder in either direction.
	If the "A" in PMP 3.1 is being cut off or the "F" is being read, rotate the mirror encoder counterclockwise (CCW, facing the lead side of the encoder) until the "A" through "E", inclusively, is read.
	If the "E" is being cut off, rotate the mirror encoder clockwise (CW, facing the lead side of the encoder) until the "A" through "E", inclusively, is read.



TEST POINTS



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TRANSPORT CONTROL SYSTEM CALIBRATION

Procedures for calibrating the transport control system are contained in table 6-50 and table 6-51. Table 6-51 adjusts transport speeds and servoing. Table 6-50 checks the transport power amplifier for branch current balance. The procedures in table 6-50 should be followed whenever the transport power amplifier has been repaired; the procedure in table 6-51 should be followed if errors have been printed out during RX-3, Module 2, or RX-4.

TABLE 6-50. TRANSPORT POWER AMPLIFIER CURRENT BALANCING PROCEDURE

Step	Procedure
1	With reader powered up, force transport to +20 ips by grounding 6E29-10 or by entering the following instructions into the BC via the maintenance console:
	0A4D B800
	Allow to run for at least 2 minutes before proceeding.
2	Using a DVM, measure and record the voltage drop across the common forward resistor (R02 on the chassis). If voltage fluctuates, record mean value. Divide this value by 5 to determine mean branch voltage. Then multiply the result by +20 percent and -20 percent to determine upper and lower branch voltage limits.
	NOTE
	Do not ground DVM.
3	Measure and record the voltage drop across each of the forward emitter resistors (R02-R06) except R01. If voltage fluctuates, record mean value. Each value should be within the upper and lower limits found in step 2. If any value is outside these limits, replace the corresponding transistor and repeat steps 1 through 3.
4	Stop transport by removing ground installed in step 1.
5	Force transport to run at -5 ips by grounding $6E09-10$ or by entering the following instruction into the BC:
	0A43 B800
	Allow to run at least 2 minutes before proceeding.
6	Using a DVM, measure and record the voltage drop across the common reverse resistor (R03 on the chassis). If voltage fluctuates, record mean value. Divide this value by 5 to determine mean branch voltage. Then multiply the result by +20 percent and -20 percent to determine upper and lower branch voltage limits.
	NOTE
	Do not ground DVM.
7	Measure and record the voltage drop across each of the reverse emitter resistors (R08-R12) except R07. If voltage fluctuates, record mean value. Each value should be within the upper and lower limits found in step 2. If any value is outside these limits, replace the corresponding transistor and repeat steps 5 through 7.

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Step	Procedure
8	Stop transport by removing ground installed in step 1.
	NOTE
	An alternate method of current bal- ancing is given in steps 9 through 22.
9	Force transport to run at $+20$ ips by grounding 6E29-10 or by entering the following instructions into the BC:
	0A4D B800
	Allow to run at least 2 minutes before proceeding.
10	Compute adjusted voltage drop across R02 as follows:
	a. Find current through R01 by measuring voltage drop E01 and dividing by $10\Omega \left(I01 = \frac{E01}{R01} \right)$.
	 b. Find voltage drop across R02 contributed by I01 by multiplying I01 by R02 (E02* = I01 X R02).
	c. Subtract voltage drop contributed by I01 from E02 (E02-E02* = E02a).
11	Determine status of reader as one of the following:
	 a. Machine below S/N151 b. Machine above S/N151 without ECO 5087 c. Machine above S/N151 with ECO 5087 d. Machine above S/N176 or refurbished unit
12	Multiply the voltage found in step 10 by one of the following values, according to machine status (step 11). This is the lower limit of acceptable emitter voltage.
	$\frac{A/B/C}{0.16} \frac{D}{0.32}$
13	Repeat step 12, using one of the following values, according to machine status. This is the upper limit of acceptable emitter voltage.
	$\frac{A/B/C}{0.24} \qquad \frac{D}{0.48}$
14	Measure and record the voltage drop across each of the forward emitter resistors (R02-R06) except R01. Compare each voltage obtained with the upper and lower limits obtained in steps 12 and 13. If any of the voltages are outside these limits, proceed to step 21.
15	Remove feeder drive timing belt. Force transport to run at -5 ips by grounding 6E09-10, or by entering the following instructions into the BC:
	0A43 B800

TABLE 6-50. TRANSPORT POWER AMPLIFIER CURRENT BALANCING PROCEDURE (CONT'D)

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Step	Procedure			
15	Run at least 2 minutes before proceeding.			
(Cont'd)	NOTE			
	Watch transport vacuum belts closely for tracking irregularities.			
16	Compute adjusted voltage drop across R03 as follows:			
	a. Find current through R07 by measuring voltage drop E07 and dividing by $10\Omega \left(I07 = \frac{E07}{R07} \right)$.			
	 b. Find voltage drop across R03 contributed by I07 by multiplying I07 by R03 (E03* = I07 X R03). 			
	c. Subtract voltage drop contributed by I07 from E03 (E03-E03* = E03a).			
17	Multiply the voltage obtained in step 16 by one of the values below, according to machine status (step 11). This is the lower limit of acceptable emitter voltage.			
	$\begin{array}{ccc} \underline{A} & \underline{B/C} & \underline{D} \\ 0.20 & 0.16 & 0.32 \end{array}$			
	0.20 0.16 0.32			
18	Multiply the voltage obtained in step 16 by one of the following values, according to machine status. This is the upper limit of acceptable emitter voltage.			
	$\underline{A} \underline{B/C} \underline{D}$			
	$\frac{A}{0.30} \frac{B/C}{0.24} \frac{D}{0.48}$			
19	Measure and record the voltage drop across each of the reverse drive emitter resistors (R06-R12) except R07. If voltage fluctuates, record mean value, compare each voltage obtained with the limits obtained in steps 17 and 18. If any of the emitter voltages are outside this limit, proceed to step 21.			
20	Stop transport by removing ground installed in step 15. Replace feeder timing belt.			
21	Examine the emitter voltages falling outside the upper or lower limit. If the voltage is more than the acceptable upper limit, the corresponding transistor is drawing too much current. Try replacing with another of the same Vbe rating (color code). If this does not correct the problem, try another transistor of a higher Vbe rating.			
	If the voltage across the emitter resistor is less than the acceptable lower limit, the corresponding transistor is not drawing enough current. Try replacing with another transistor of the same Vbe rating. If this does not correct the problem, try another transistor of a lower Vbe rating.			
22	After replacing transistors, return to step 9 and re-run test procedure to verify current balance.			

TABLE 6-50. TRANSPORT POWER AMPLIFIER CURRENTBALANCING PROCEDURE (CONT'D)

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TABLE 6-51. TRANSPORT CONTROL SYSTEM CALIBRATION PROCEDURE

	· ·	Procedure	
		NOTE	
	wise not	age measurements are made to ted. All measurements made or d to local signal ground on that b	n a given board should be
	(CJ122)	o schematics numbers 48554900, Mods. C and D) or 48914200, 48 0 (CJ122 Mods. E, F, G, H, J	5555700, 48896100, and
	Use the	PC extender board as required.	
	standar	are the transport system is mee d belt tensions, good conveyor b pressures, no loose setscrews,	elt tracking, proper
	board (4	current limit pots, R16 and R1 8555800), for maximum curren ck CW 1/16 turn. (See figure 6-	t (full CCW). Then turn
	measure transpo	ect A48-P06, P11, and P12 and e the resistance across each dio rt control electronics board (fig be 400 ohms forward bias, 1.5M	de CR01 and CR02 on the ure 6-50). Readings
1		oort boards, reconnect A48-P06, SERVO circuit breaker off.	, P11, and P12 and power up the
2	at logical "1".	TP-V, TP-U, TP-T, TP-S, ar	sport control electronics board are nd TP-R. Check for the presence conics board, referenced to TP-X:
2	at logical "1".	TP-V, TP-U, TP-T, TP-S, ar	nd TP-R. Check for the presence
2	at logical "1". of the following	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H,
2	at logical "1". of the following Voltage	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D)	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K)
2	at logical "1". of the following Voltage +15 vdc	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28
2	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc -6 vdc	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59 Pin 3	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30 Pin 2
2	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30
2	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc -6 vdc -15 vdc Connect the DV	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59 Pin 3 Pin 5	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30 Pin 2 Pin 3 rt control electronic board. Adjust
	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc -6 vdc -15 vdc Connect the DV R63 (see figure Load the follow	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59 Pin 3 Pin 5 M to test point W of the transport 6-51) on the board until the DVI	nd TP-R. Check for the presence conics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30 Pin 2 Pin 3 rt control electronic board. Adjust
3	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc -6 vdc -15 vdc Connect the DV R63 (see figure Load the follow	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59 Pin 3 Pin 5 M to test point W of the transport 6-51) on the board until the DVI ing into the Maintenance Console lable, proceed to step 5.	tonics board, referenced to TP-X: Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30 Pin 2 Pin 3 rt control electronic board. Adjust M reads 0 ±10 mv.
3	at logical "1". of the following Voltage +15 vdc +12 vdc +5 vdc -6 vdc -15 vdc Connect the DV R63 (see figure Load the follow	TP-V, TP-U, TP-T, TP-S, ar voltages at the transport electr Location (CJ122 Mods. C and D) Pin 55 Pin 57 Pin 59 Pin 3 Pin 5 M to test point W of the transport 6-51) on the board until the DVI ing into the Maintenance Console lable, proceed to step 5.	nd TP-R. Check for the presence conics board, referenced to TP-X Location (CJ122 Mods. E, F, G, H, J, and K) Pin 28 Pin 29 Pin 30 Pin 2 Pin 3 rt control electronic board. Adju M reads 0 ±10 mv. e "A" Register. If no maintenance

Step	Procedure	
4 cont'd	Set the following bits for the desired speed. To change speeds, depress "A" register clear and select new speed.	
	Bit Speed	
	11 -5 ips	
	12 +40 ips	
	13 +20 ips	
	14 +12.5 ips 15 +5 ips	
5	Load the following program into the 1700 or SC1700 via the operator control panel on the front of the computer. Load at 0100 (autoload routine).	
	P = 0100 - C000 XX08 - C400 XX10 - 010	1
	1 - XXXX (FWA) 9 - XXXX (FWA) 11 - 18F	
	2 - 6807 A - 0800 $12 - 0$ DF	
	3 - E000 B - 03FE 13 - 0A0	
	4 - 0509 C - D8FC 14 - 03F 5 - 0800 D - C8FB 15 - 000	
	5 - 0800 D - C8FB $15 - 00006 - 03FE E - 9000$	0
	7 - 0 DFE F - XXXX (LWA)	
6	Load the program to be autoloaded in the BC in locations 0000 to 00FF in the computer (1700 or SC1700). Also be sure this program is in the BC format. example: To run the transport at 5 ips you would load the following program:	For
	P INST	
	0000 0000	
	0A4X where $X = F = 5$ ips	
	$096E \qquad \text{where } X = E = 12.5 \text{ ips}$	
	$EF01 \qquad \text{where } X = D = 20 \text{ips}$	
	$\begin{array}{ccc} 0B4X & \text{where } X = C = 40 & \text{ips} \\ 00CD & \text{where } X = D = 5 & \text{ipg} (Berr) \end{array}$	
·	096D where X = B = -5 ips (Rev.) EF01	
	BF06	
	MASTER CLEAR the computer and run from 0100 (initial location of the autolo routine). This will load the BC with the above program and execute it. Push READY switch on the control panel and this will gate the command into the log To stop the command press the STOP switch; to restart the command press the LOAD switch.	the ic.

TABLE 6-51.TRANSPORT CONTROL SYSTEMCALIBRATION PROCEDURE (CONT'D)

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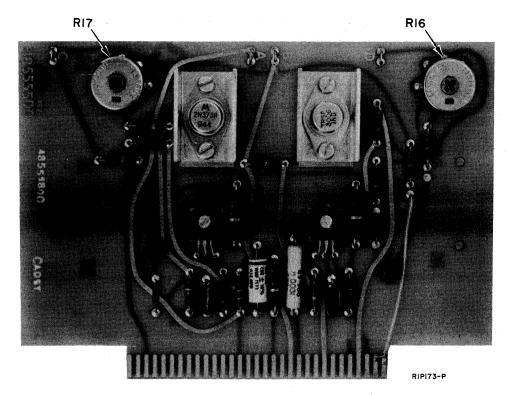


Figure 6-50. Transport Power Preamplifier Assembly (Part No. 48555800)

TABLE 6-51.TRANSPORT CONTROL SYSTEMCALIBRATION PROCEDURE (CONT'D)

Step	Procedure
7	Load the proper command into the program for 5 ips and repeat step 6. Adjust R50 on the transport control board (see figure 6-51) to obtain +0.850V at test point L. Return the 5 ips command to logical 1 by pressing the STOP switch.
8	Load the proper command into the program for 12.5 inches/second and repeat step 5. Adjust R53 (see figure 6-51) to obtain +2.13V at test point M. Return 12.5 ips command to logical 1 by pressing the STOP switch.
9	Load the proper command into the program for 20 ips and repeat step 5. Adjust R56 (see figure 6-51) to obtain +3.40V at test point N. Return 20 ips command to logical 1 by pressing the STOP switch.
10	Load the proper command into the program for 40 inches/second and repeat step 5. Adjust R59 (see figure 6-51) to obtain +6.80V at test point P. Return 40 ips command to logical 1 by depressing the STOP switch.

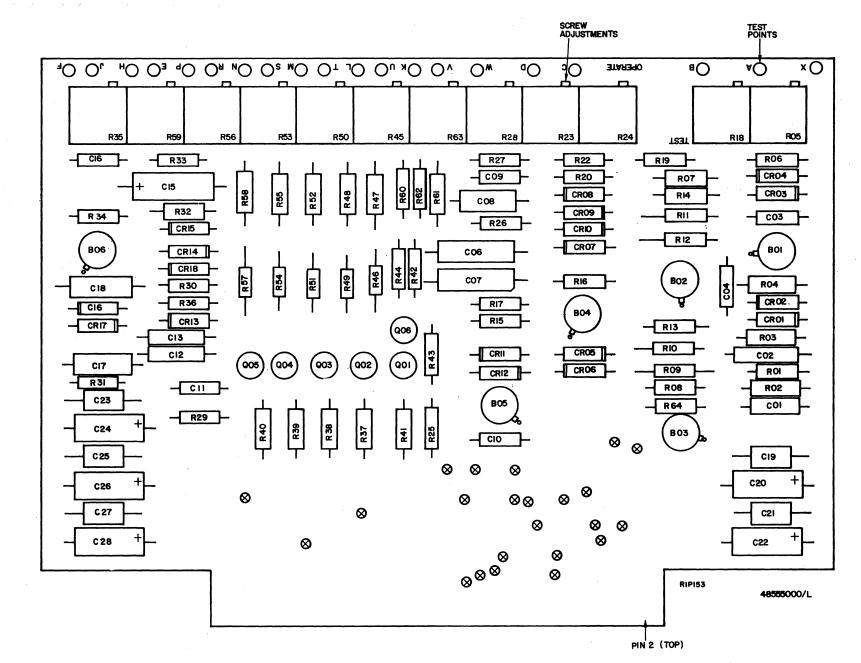


Figure 6-51. Transport Control Electronics Assembly (Part No. 48555000) (CJ122 Mods. C and D) and 72TCR Card Assembly (Part No. 48914300) (CJ122 Mods. E, F, G, H, J, and K)

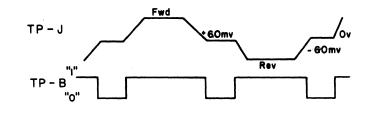
48430080 C

2.2

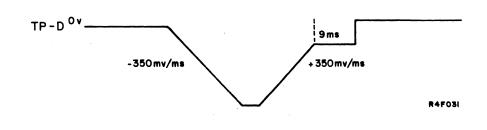
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TABLE 6-51.TRANSPORT CONTROL SYSTEMCALIBRATION PROCEDURE (CONT'D)

Step	Procedure										
11	Load the proper command into the program for -5 ips and repeat step 5. Adjust R45 (see figure 6-51) to obtain -0.850V at test point K. Return -5 command to logical 1 by pressing the STOP switch.										
12	Repeat step 3.										
13	Connect DVM to TP-D. All commands should be logical 1 (transport stopped). Adjust R24 for zero switch point.										
14	Set SERVO circuit breaker on. Connect the DVM to summing amplifier section TP-J. Adjust pot R35 (10K) for zero switching point. If reading will not zero, connect DVM to TP-B on power pre-amp and adjust R63 for 0 vdc. Then recheck TP-J and readjust R35 as necessary.										
15	Set R18 and R23 to center or mid-range.										
16	Load the proper command into the program for 20 ips command and repeat step 5.										
17	Measure the voltage at TP-N with the DVM. Now connect the DVM to TP-D of the board. Adjust R28 (5K) on the board for a DVM reading equal to and opposite that just measured at TP-N. Remove the DVM. Set 20 ips command to logical 1 by pressing the STOP switch.										
18	Ground TP-W on transport electronics board and connect DVM to TP-B on power preamplifier (figure 6-50). Set SERVO circuit breaker at ON and adjust R24 (10K) on the transport electronics board to obtain zero volts at the output lead. Remove the ground jumper and adjust R63 (2K) on the board to zero the DVM. Disconnect the DVM.										
19	Set R05 to its mid-point. Load the following program into the BC via the main- tenance console or autoload routine and run. Press the READY switch on CJ122 control panel; the transport should step forward at 5 ips, dwell, and then step reverse at 5 ips, continuing this cycle indefinitely. Display output of summing amplifier TP-J and NZV signal TP-B. Check that NZV is being generated in both directions at TP-B when TP-J equals ± 60 mv. Adjust R05 (if necessary) for this condition (see figure 6-52A).										
	\underline{P} <u>INST</u> \underline{P} <u>INST</u> \underline{P} <u>INST</u>										
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$										
	1 - A821 B - A824 14 - 0B4B 2 - 0A4F C - 8824 15 - A825										
	3 - 8820 D - CF01 16 - 8825										
	4 - CF01 E - 0A4B 17 - CF01										



A. SUMMING AMPLIFIER/NZV, ±5ips stepping



B. VELOCITY COMMAND, 20 ips stepping

Figure 6-52. Transport Alignment Waveforms

200

 $\sum_{i=1}^{n}$

	CALIBRATION PROCEDURE (CONT'D)									
Step	Procedure									
19 cont'd	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$									
20	9 - A822 Run test RX4 (see PMP 2.10), Module 1, subtest 3. No coordinate changes are necessary. After loading, enter EX* at teletype and press READY switch at operator's panel. The transport will now step forward at 20 ips, stop and dwell, and step forward again.									
	Connect oscilloscope to TP-D and observe waveform (see figure 6-52B, velocity command waveform). Potentiometer R23 adjusts both the accelerate (negative going) slope and the decelerate (positive going) slope of the command waveform. Potentiometer R18 adjusts the accelerate slope only. Starting with R23, in the middle of its range, adjust both potentiometers to obtain:									
	Accelerate Slope = -350 mv/ms Decelerate Slopes = +350 mv/ms Back Porch (5 inches/second) time duration = 9 msec If this cannot be achieved, R23 and R18 will have to be changed again, but the accelerate slope of -350V/second must be preserved. When the 9 msec back porch									
21	has been achieved, record the value of the decelerate slope. Observe the voltage waveform across R1 (0.1 ohm) at the rear of the heat sink. Adjust each current limit potentiometer (R16 and R17) on the power pre-amp board clockwise until current limiting occurs, then back off above the settings where current limiting occurs (voltage waveform clips) so that there is no current limiting.									
22	Stop the program (all input commands = logical 0); connect the DVM to the power amplifier output lead (to the motor) on the heat sink assembly. Adjust R63 on the pulse processor board to zero the DVM. Remove DVM.									
23	Now load RX-3 Module 2 and run subtest 4 and select all 4 speeds consecutively and run. This will check the speeds of the transport. If there are any error printouts on the speed, adjust the corresponding command potentiometer for the speed you are running until there are no error messages. Repeat this process, running subtest 5.									
	If any change is made in speed potentiometers, repeat steps 4, 13, and 14.									

TABLE 6-51.TRANSPORT CONTROL SYSTEMCALIBRATION PROCEDURE (CONT'D)

Step	Procedure										
	NOTE										
	See schematics 48854500 (CJ122 Mods. C and D) or 48914500 (CJ122 Mods. E, F, G, H, and K).										
1	Check all power supply voltage inputs.										
2	Press 955 READY switch. MASTER CLEAR BC. The following interface logic levels should exist on the mirror drive board.										
	$TP-A, \underline{NMZV} = logical 1$ $TP-B, \overline{Flyback Enable} = logical 1$ $TP-C, Flyback decelerate = logical 0$ $TP-D, \underline{Flyback accelerate} = logical 0$ $TP-F, Sweep Forward = logical 1$ $TP-E, 24 Velocity Correction Bit = logical 1$ $TP-H, 2^{3} Velocity Correction Bit = logical 0$ $TP-J, 2^{2} Velocity Correction Bit = logical 0$ $TP-K, 2^{1} Velocity Correction Bit = logical 0$ $TP-L, 2^{0} Velocity Correction Bit = logical 0$ $TP-R, RMV = logical 0$ $TP-S, M. O. V. Rev. = logical 0$ $TP-T, M. O. V. Fwd. = logical 0$										
3	 Check for following voltages, using DVM (see figures 6-53 and 6-54): (1) Mirror electronics: a. cathode of zener diode CR03 should be +5.1 vdc ±6 percent (o. 3V) b. anode of zener diode CR02 should be -5.1 vdc ±6 percent (0. 3V) c. voltage across R06 (2.7 ohms) should be 7.8 mv ±10 percent (CJ122 models C and D only). d. TP-Y =0 vdc ±12 mv. e. TP-U =0 vdc ±40 mv. (2) Servo amplifier output: TP-B=0 ±20 mv. (Use R07 to adjust amplifier offset voltage.) 										
4	Force MNZV to logical 0 by grounding TP-A on mirror drive board. Adjust R37 for power amplifier output voltage at TP-B of 0 vdc ± 50 mv. (With MNZV =0, the power amplifier output voltage can easily drift $\pm 0.5V$ in a relatively short time. The output voltage will vary randomly, but this is normal.)										

TABLE 6-52. LINE SCANNING SYSTEM, MIRROR CONTROL SYSTEM ALIGNMENT PROCEDURE

* Manually grounded.

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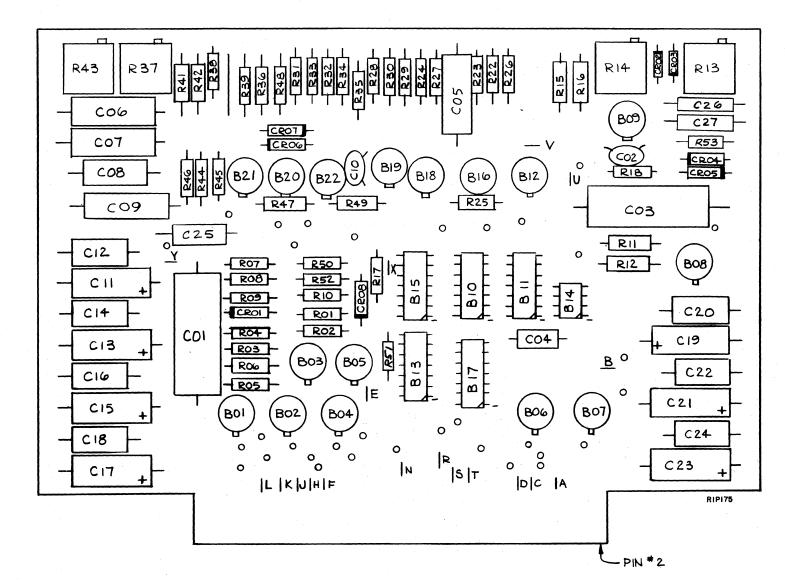


Figure 6-53. Mirror Drive Electronics Assembly (Part No. 48854700) (CJ122 Mods. C and D) and 72MER Assembly (Part No. 48914400) (CJ122 Mods. E, F, G, H, J, and K)

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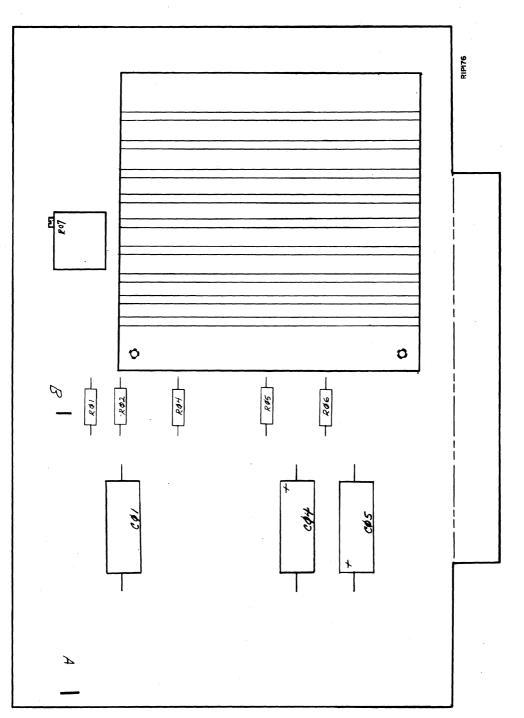


Figure 6-54. Mirror Servo Amplifier Assembly

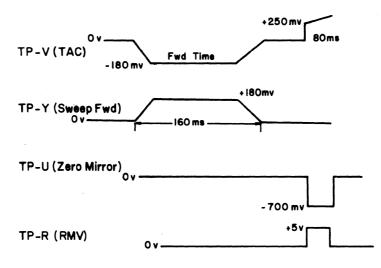
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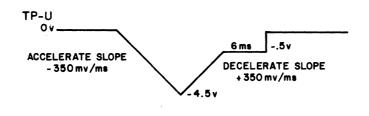
TABLE 6-52.LINE SCANNING SYSTEM, MIRROR CONTROL SYSTEMALIGNMENT PROCEDURE (CONT'D)

Step	Procedure									
5	After returning MNZV to logical 1, repeat step $3(2)$ and 4 until both the offset is 0 to ± 50 mv. and mirror motion is stopped.									
6	Set the Sweep Forward command by grounding TP-F and TP-A on mirror drive board. Check the following voltages:									
e L	TP-Y =180 mv. ±10 percent (18 mv) Remove GND from TP-F.									
7	Load RX-3 Module 4. The coordinates are as follows:									
	FWD: 246 REV: (CR) DWELL = 50									
	Be sure to suppress printout (S0*).									
	Enter 001 ₍₁₆₎ into BC A register.									
	Press the 955 READY switch.									
	Press the BC GO button.									
	The mirror should repetitively scan forward and zero mirror with a 50-msec dwell at the end of each forward and reverse motion.									
8	Use the scope for the following voltage measurements (see figure 6-55):									
	 a. during Sweep Forward, TP-Y = 180 mv. ±10 percent b. during Zero Mirror, TP-U = -700 mv. ±20 percent c. TP-V (tachometer voltage) = -180 mv. ±10 percent during sweep forward and = +230 mv. ±20 percent during zero mirror. d. TP-R should be a logical 1 during Zero Mirror Time. 									
	Observe TP-Y and TP-V simultaneously during sweep forward time (trigger scope negative going on TP-F). The two signals should be very nearly equal in amplitude and the time lag of the tachometer waveform relative to the command waveform during sweep start-up should be no greater than 2 msec.									
	Observe TP-U and TP-V simultaneously during zero mirror time. The zero mirror voltage at TP-U should be very close to 3 times the voltage at TP-V and the lag of the tachometer waveform relative to integrator (TP-U) waveform during zero mirror start-up should be no greater than 2.5 msec. For this time delay measure- ment, trigger the scope on TP-D positive going and adjust the channel gains so that both waveforms are the same height on the scope face.									

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A. MIRROR FORWARD and STOP WAVEFORMS



B. FLYBACK COMMAND

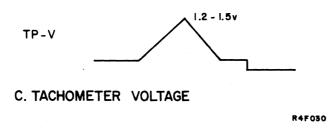


Figure 6-55. Mirror Control Alignment Waveforms

Step	Procedure					
9	Make the reverse coordinate equal to 0016 and execute ($EX*$).					
	The mirror should repetitively scan forward and fly back with a 50-msec dwell at the end of each forward and reverse motion.					
	 a. Observe TP-U on the scope. Adjust R13 to obtain a flyback accelerate slope of -350 mv/msec. (Trigger the scope positive going on TP-D.) Adjust R14 to obtain a flyback decelerate slope of +350 mv/msec. (Trigger on TP-D, negative going.) 					
	The range of slope control for both R13 and R14 should be approximately $275V/sec.$ to $750V/sec.$					
	The mirror is now flying back from mirror coordinates $F6_{(16)}$, $246_{(10)}$ to mirror coordinate $10_{(16)}$, $16_{(10)}$.					
	b. Adjust R14 to obtain an integration "backporch" (just prior to stopping) of 5 to 6 msec duration.					
	The peak integration flyback voltage, TP-U, should be approximately $-4.5V$.					
	The peak tachometer flyback voltage, $TP-V$, should be approximately +1.5V.					
10	Change mirr o r coordinates as follows:					
	FWD:250 (10)REV:001 (10)DWELL:1					
	Be sure the output to teletype or printer is enabled. Run test for 5 minutes; if no error messages occur, the mirror may be considered to be properly aligned.					

TABLE 6-52. LINE SCANNING SYSTEM, MIRROR CONTROL SYSTEM ALIGNMENT PROCEDURE (CONT'D)

ON-LINE CHARACTER CORRECTION UNIT (OLCC)

Adjustment procedures for the +5V, -5V, and -12V power supplies are contained in table 6-53. Horizontal and vertical gain adjustment procedures for the display monitor are contained in table 6-54. The adjustment procedure for the display monitor Z-axis gain is contained in table 6-55.

Step	Procedure								
	NOTE								
1	See figure 1-3 for location of power supplies.								
1	Remove top cover from OLCC.								
2	Turn on power at control panel.								
3	Measure $+5V$ output of PS01 at OUT terminal for $+5 \pm 0.1V$.								
	If necessary, adjust R9 potentiometer on PS01 for correct output voltage.								
4	Connect oscilloscope to +5V output of PS01 and observe noise level. Noise level should be less than 10 millivolts peak to peak. If noise level is greater than 20 millivolts peak to peak, replace power supply.								
5	Measure -5V output of PS02 at OUT terminal for -5 ± 0.1 V.								
	If necessary, adjust R9 potentiometer on PS02 for correct output voltage.								
6	Connect oscilloscope to -5V output of PS02 and observe noise level. Noise level should be less than 10 millivolts peak to peak. If noise level is greater than 20 millivolts peak to peak, replace power supply.								
7	Measure -12V output of PS03 at OUT terminal for -12 +0. 25V.								
	If necessary, adjust R8 potentiometer on PS03 for correct output voltage.								
8	Connect oscilloscope to -12V output of PS03 and observe noise level. Noise level should be less than 10 millivolts peak to peak. If noise level is greater than 20 millivolts to peak, replace power supply.								
9	Turn off power at control panel.								
10	Reinstall top cover on OLCC.								

TABLE 6-53. OLCC POWER SUPPLY ADJUSTMENT PROCEDURES

TABLE 6-54. HORIZONTAL (X) AND VERTICAL (Y) GAIN ADJUSTMENT PROCEDURES

Step	Procedure						
1	Lift OLCC off system teletypewriter mounting brackets or cradle and set unit on stand or table.						
2	Remove top cover from OLCC.						
3	Switch beam intensity $(-Z)$ input and grounding cap $(+Z)$ at rear of display monitor. Reversing inputs will cause character images to be dark and background to be intensified on display screen.						
4	Energize reader on OLCC.						
5	Read document that will cause reader to generate a character reject. Character images will be displayed on display monitor with rejected character centered and underlined.						

TABLE 6-54. HORIZONTAL (X) AND VERTICAL (Y) GAIN ADJUSTMENT PROCEDURES (CONT'D)

Step	Procedure
6	Adjust intensity control knob at OLCC control panel for normal display brightness.
7	Adjust horizontal position control knob at control panel until illuminated area is centered horizontally.
8	Adjust display monitor X gain (R325 on A1 deflection amplifier circuit board) until illuminated area is approximately 1/8 inch from left and right edges of display screen. Refer to display monitor instruction manual, figure 4-2, for location of R325 potentiometer. Repeat step 7, if necessary.
9	Adjust vertical position control knob at control panel until illuminated area is centered vertically.
10	Adjust display monitor Y gain (R125 on A1 deflection amplifier circuit board) until illuminated area is approximately 1/8 inch from top and bottom edges of display screen. Refer to display monitor instruction manual, figure 4-2 for location of R125 potentiometer. Repeat step 9, if necessary.
11	Adjust TRACE ROTATION potentiometer at rear of display monitor until display perimeter is symmetrical with edges of display screen.
12	Switch beam intensity input and grounding cap at rear of display monitor back to normal. Beam intensity input should normally be connected to $-Z$ input, and grounding cap should be connected to $+Z$ input.
13	Adjust INTENSITY and FOCUS control knobs at control panel for normal display brightness and sharpness. If display is unsatisfactory, perform Z gain adjustment procedure in table 6-55.
14	Turn off power at control panel.
15	Reinstall top cover on OLCC.
16	Mount OLCC on system TTY mounting brackets or cradle.

TABLE 6-55. Z-AXIS GAIN ADJUSTMENT PROCEDURE

Step	Procedure					
1	Lift OLCC off system TTY mounting brackets or cradle and set unit on stand or table.					
2	Remove top cover from OLCC.					
3	Energize reader and OLCC.					
4	Read document that will cause reader to generate a character reject. Character images will be displayed on display monitor with rejected character centered and underlined.					

TABLE 6-55. Z-AXIS GAIN ADJUSTMENT PROCEDURE (CONT'D)

Step	Procedure
5	Turn INTENSITY and FOCUS control knobs at control panel OLCC control panel to center position.
6	Adjust display monitor Z gain (R512 on A2 Z-axis circuit board) for proper con- trast of character images. Refer to display monitor instruction manual, figure 4-5, for location of R512 potentiometer. Character images should be intensified with background blanked.
7	Adjust INTENSITY and FOCUS control knobs at control panel for normal bright- ness and maximum sharpness.
8	Turn off power at control panel.
9	Reinstall top cover on OLCC.

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SECTION 7

MAINTENANCE AIDS

A definition of the type of integrated circuit (IC) logic used in the reader, along with a detailed description of the function, power supply requirements, loading capabilities, and circuit operation of each IC element used are presented in this section. Table 7-1 provides a cross reference of CDC part numbers to interchangeable IC's from various vendors. The table is arranged by coded component type, as found at the end of each logic element tagging line in the logic diagrams (vol. 2, part 1). For clarity, all logic element codes are included in the table, although some do not represent IC's.

Integration of circuit functions instead of discrete components is classified as conventional or small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI). SSI employs IC packages having normally up to 30 internal gates, and one level of interconnection (function). MSI elements contain up to 80 gates and are characterized by two levels of interconnection. LSI packages contain a significant increase over MSI packages in number of gates, pins, and levels of interconnection.

The reader employs MSI adder, counter, and register circuits. Hybrid chips provide digital-to-analog (D/A) conversion. The D/A converter used occupies the space of four conventional elements. LSI shift registers are used in the image register section of the reader.

INTEGRATED CIRCUIT LOGIC

IC's used in the reader employ diode transistor logic (DTL), transistor transistor logic (TTL) and metal-oxide semiconductor transistor logic (MOS). DTL and TTL circuits are logically and electronically compatible. Most MOS circuits used are LSI shift register circuits which function as serial memories. MOS level changers and analog switches are also used.

DTL circuits use diodes, transistors, and resistors as circuit components. Input diodes provide isolation of source and load, perform logic operations and, in multivibrators, provide input steering. Transistors used in DTL circuits perform amplification, switching, and inverting function; input diodes in DTL circuits provide isolation that promotes noise immunity. Moderate speed, typically 30 nanoseconds for gates, is characteristic of DTL circuits used.

TTL circuits are composed of transistors and resistors. Transistors achieve all logic operations and provide source and load isolation, amplification, switching, and inversion. A multiple-emitter transistor replaces input diodes common to DTL and input resistors common to RTL (resistor transistor logic) circuits. The input transistor constitutes an active-component input circuit which is considerably faster than passive-component circuits common to DTL, RTL, and other logic types. Further enhancement of speed in TTL circuits is obtained via active output (Pull-up) transistors.

The low capacitance input of a TTL circuit subjects driving circuits to very little loading. Very high speed, typically 10 nanoseconds, and power handling capability, nominally 10 milliwatts per gate, are the most desirable performance characteristics of TTL circuits used in the reader. MOS circuits operate on the principle of the insulated-gate, field-effect transistors (FET). An MOS circuit consumes less power and is smaller than an equivalent circuit constructed with bipolar transistors. The high input impedance of each MOS input gate provides a high fan-in capability. The FET transistors used in MOS circuits are voltage controlled and act almost as ideal switches because signal flow from input (source) to output (drain) is gated. So long as the gate voltage equals the source voltage no current flow occurs. When the gate potential exceeds a threshold voltage the FET turns on and current flows. MOS register circuits are used in the image register section of the reader.

POWER SUPPLY REQUIREMENTS

Operating power for most IC elements is $+5.0 \pm 0.25$ V. Following is a list of IC elements having unique ground and/or power supply pins; all other IC elements have +5 V applied to pin 14 and ground applied to pin 7.

Coded Type	Chip Type	Voltage/Pin No.	Ground Pin No.
02	N5710/MA710	+12/11, -6/6	2
12	SN7494	+5/5	12
26	UD4181	+5/4	11
28	N8T18	+20/13, +5/14	7
39	SN7483A	+5/5	12
42	SN74H106	+5/5	13
44	845-U5	+15/24, -15/9	7
45	MA741	+15/11, -15/6	· · · · ·
58	LM311	+15/11, -15/6	-
62	K-1035	+5/1	2
63	SN7490A	+5/5	10
64	SN7482	+5/4	11
69	9322	+5/16	8
71	K -10 35	+5/1	2
72	9312	+5/16	8
78	SN74123	+5/16	8
80	K-1035	+5/1	2
90	SL-7-2050	+5/11, -12/12	3
95	MK1002	+5/5, -12/11	6
96	SL-7-4032	+5/1, -12/2	4
97	9316	+5/16	8
98	9304	+5/16	8
99	9314	+5/16	8
100	SN74191	+5/16	8
101	9324	+5/16	8
103	9024	+5/16	8

INTEGRATED CIRCUIT DESCRIPTIONS

IC elements described in the following paragraphs are classified according to logic function performed (i.e., NAND, OR, FLIP-FLOP, etc.). Under each major classification a general description of the function is presented, along with typical schematic and logic diagrams, logic equation, or truth table; specific types of IC elements that perform the described function can be found in table 7-1.

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Coded Texas Instruments Signetics National Other CDC Fairchild Function Type Motorola DM949J 50252300 MC849L U6A994959X SN15849J Quad 2-input NAND 1 SN52710J **MA710**F LM710J 51715100 Differential ampli-2 MC1710L U6A7710312 fier 3 MC3000L 9H00DC SN74H00J 8H80F 36188700 Quad 2-input NAND 36187801 Dual AND-OR 4 MC7451L 9N51DC SN7451J N7451F DM7451J inverter MC853LU6A909359X SN158093J DM9093J 52339301 Dual J-K flip-flop 5 52335600 6 MC3008L 9H04DC SN74H04J N74H04F Hex inverter U6A994659X SN15846J DM946J 51577900 7 MC846L Quad 2-input NAND N74H30F DM74H30J 51801400 8 MC3016L 9H30DC SN74H30J 8-input NAND 48418602 Discrete component 9 chip DM937J 51767700 MC837L U6A993759X SN15837J Hex inverter 10 36186700 MC1814L Quad latch 11 94913200 4-bit parallel-in, 12SN7494L 7494DC SN7494J N7494F serial-out shift register SN74107J N74107F DM74107J 15105000 Dual J-K flip-flop MC74107L 74107DC 13 DM932J Dual 4-input SN15832J 51577600 14 MC832L U6A993259X expandable NAND Not used 1536189200 Dual J-K flip-flop 1674H108DC SN74H108J N74108F DM962J 51578100 Triple 3-input 17MC862L U6A996259X SN15862J NAND 94903704 Hex inverter 18 MC834L SN15834J

TABLE 7-1. CROSS REFERENCE OF INTERCHANGEABLE IC ELEMENTS

Part number (CDC or vendor) specifying plastic chip-ceramic replacement preferred.

CDC	Function	Coded Type	Motorola	Fairchild	Texas Instruments	Signetics	National	Other
51577500	Dual 4-input expandable NAND	19	MC830L	U6A99 305 9X	SN15830J		DM930J	
	Not used	20						
36186200	Quad 2-input NAND	21	MC857L		SN15857J		DM957J	
51577700	Dual 4-input expander	22	MC833L	U6A993359X	SN15833J		DM933J	
51654400	Hex inverter	23	MC836L		SN15836J		DM936J	
15104600	Triple 3-input NAND	24	MC3005L	74H10DC	SN74H10J	N74H10F		
	Not used	25						
94912403†	Power driver	26						UD4181 [†] (Sprague)
52339200	R-S flip-flop	27	MC845L	U6A994559X	SN15845J			
94912401	Dual 2-input NAND	28				N8T18A [†]		
36186300	Quad 2-input NAND power gate	29	MC858L		SN15858J		DM958J	
94903703 [†]	Triple 3-input NAND	30	MC863L	U6A996359X	SN15863J		DM963J	
36188500	Monostable multi- vibrator	31		74121DC	SN74121J	N74121F	DM74121J	
94916105 [†]	4-bit up/down counter	32				N8284A [†]		
36186600	Quad exclusive OR	33	MC1812L		SN151812J	N7495F		
52335500	4-bit right-left shift register	34	SN7495L	7495DC	SN7495AJ	N7495F	DM7495J	
52335700	Dual 4-input NAND	35	MC3010L	74H20DC	SN74H20J	N74H20F	DM74H20N [†]	
[†] Part numb	[†] Part number (CDC or vendor) specifying plastic chip-ceramic replacement preferred.							

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CDC	Function	Coded Type	Motorola	Fairchild	Tex a s Instruments	Signetics	National	Other
94915210 [†]	Divide-by-16 counter	36	MC839L					
94916107*	Quad dual input NAND	37				N8T80A. [†]		
15104800	Dual clocked type flip-flop	38		7474DC	SN7474J	N7424F	DM7474J	
36188100	4-bit adder	39	SN7483L	7483DC	SN7483AJ	N7483E	DM7483J	
48418621	Discrete component chip	40	•					
48418623	Discrete component chip	41						
39389400	Du a l J-K flip-flop	42		74H106DC	SN74H106J	$N74106B^{\dagger}$		
94916110	Quad AND/OR inverter	43	MC7454L	7454DC	SN7454J	N7454F	DM7454J	
94915801	Digital-to-analog converter	44						845-U5 (Beckman)
94913001	Operational ampli- fier	45	MC1741CL	U6A7741393	SN72741J	N5741A [†]	LM741CJ	
94915208 [†]	Single 8-input expandable NAND	46	MC1803L		SN151803J			
94929100	Discrete component chip	47						
48418601	Discrete component chip	48					-	
48418622	Discrete component chip	49						
48325500	AKLDG element	50						

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CDC	Function	Coded Type	Motorola	Fairchild	Texas Instruments	Signetics	National	Other
48418624	Discrete component chip	51						
48418605	Discrete component chip	52						
48418606	Discrete component chip	53						
48418607	Discrete component chip	54						
48418608	Discrete component chip	55						
48418609	Discrete component chip	56						
48418610	Discrete component chip	57						
94917501	Voltage comparator	58			SN72311J	LM311F	LM311J	
48418612	Discrete component chip	59						
94918808 [†]	2-wide, 4-input AND/OR inverter, expandable	60	MC3034L	74H55DC	SN74H55J	N74H55F	DM74H55N [†]	
48418613	Discrete component chip	61						
94917800	Oscill a tor, 7. 83461 MHz	62	K1035A		х.			
84748800	Decade counter	63	MC7490L	7490DC	SN7490AJ	N7490F	DM7490J	
94914802 [†]	2-bit binary full adder	64	MC17482L	7482DC	SN7482J			

[†]Part number (CDC or vendor) specifying plastic chip-ceramic replacement preferred.

		Coded			Texas			
CDC	Function	Туре	Motorola	Fairchild	Instruments	Signetics	National	Other
48418614	Discrete component chip	65			· ·			
48418615	Discrete component chip	66						
48418616	Discrete component chip	67						
48418617	Discrete component chip	68						
51784000	Quad 2-input multi- plexer	69		9322DC	SN74157J	N74157B [†]	DM74157N [†]	
17184600	Hex inverter	70	MC7405L .	7405DC	SN7405J	N7405F	DM7405J	
94917805	Oscill a tor, 5. 9944 MHz	71	K1035A					
50252200	8-input multiplexer	72	MC8312L	9312DC	SN29312J	N8230F		
36187500	Dual power driver	73	MC7440L	7440DC	SN7440J	N7440F	DM7440J	
36186800	Quad 2-input NAND	74	MC7400L	7400DC	SN7400J	N7400F	DM7400J	
36181700	Hex inverter	75	MC7404L	7404DC	SN7404J	N7404F	DM7404J	
48418619	Discrete component chip	76						
48418620	Discrete component chip	77						
50254300	Du al retriggera ble one-shot	78			SN74123J	N74123F	DM74123N [†]	
48418618	Discrete component chip	79						
94917801	Oscillator, 5.4001 MHz	80	K1035A					
[†] Part num	ber (CDC or vendor) s	specifyi	ng plastic chi	p-ceramic re	placement pre	ferred.		

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CDC	Function	Coded Type	Motorola	Fairchild	Texas Instruments	Signetics	National	Other
48418625	Discrete component chip	81	· · · · · · · · · · · · · · · · · · ·					
48418626	Discrete component chip	82					ч.	
48418627	Discrete component chip	83						
48418628	Discrete component chip	84						
	Not used	85						
	Not used	86						
	Not used	87						
	Not used	88						
	Not used	89						
15104900	Dual 50-bit static shift register	90						SL-7-2050 (General
		a an		1.4				Instruments
94903720 [†]	8-bit serial-in parallel-out shift register	91		74164DC	SN74164J	N74164F	DM8570J	
36187400	Single 8-input NAND	92	MC7430L	7430DC	SN7430J	N7430F	DM7430J	
50250700	Triple 3-input NAND	9 3	MC7410L	7410DC	SN7410J	N7410F	DM7410J	
36187300	Du a l 4-input NAND	94	MC7420L	7420DC	SN7420J	N7420F	DM7420J	
15 110300[†]	Dual 128-bit static shift register	95	MK1002L		$ ext{TMS3114J}$			MEM3128 (General Instruments

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TABLE 7-1. CROSS REFERENCE OF INTERCHANGEABLE IC ELEMENTS (CONT'D)

CDC	Function	Coded Type	Motorola	Fairchild	Tex a s Instruments	Signetics	National	Other
94916115	Quad 32-bit static shift register	96						S1-7-4032 (General Instruments)
51761500	4-bit synchronous counter	97		9316DC	SN74161J	N74161F		
39126600	Du a l full a dder	98		9304DC				
15107300	Quad latch	99		9314DC				
52342700	4-bit synchronous up down counter	100		74191DC	SN74191J			
51783500	5-bit comparator	101		9324DC				
36188800	Dual 4-input NAND buffer	102	MC3024L	74H40DC	SN74H40J	N74H40F		
51786700	Dual J-K flip-flop	103		9024DC	SN74109J	N74109F		
15107000	Quad 2-input Power NAND	104		7437DC	SN7437J	N7437A [†]		
94959101	Terminating register network	105						899-5- R2201330
94959003 94959004	Oscillator, 5.4001 MHz	106	K1091A					(Beckman)
94959004	Oscill a tor, 5.9944 MHz	107	K1091A					
94959005	Oscillator, 7.8546 MHz	108	K1091A					
52341200	Retriggerable monostable multivibrator	109	MC8601L	U6A960159X	SN74122J	N74122F	DM8601J	
48418629	Discrete component chip	110						

Differences among the various types of IC elements performing a logical function occur generally in number of circuits per element, number of inputs per circuit, and input and output loading factors.

With the exception of shift registers, positive logic is used in all IC elements in the reader; specifically, a logical "1" is +2.8 to +5V and a logical "0" is 0 to +0.4V.

GATE FUNCTIONS

Positive logic NAND gates and inverters comprise the basic DTL and TTL gates used. These gates and inverters are configured to perform the NAND, AND, NOR, and OR logic operations. High-current inverters, or inverters connected in parallel, are used to achieve high fan-out.

NAND Gates

NAND signifies NOT AND. NAND gates perform as two circuits: and AND gate and an inverter. Typical schematics for DTL and TTL NAND gates are shown in figure 7-1. Also shown in this figure are the logic symbols and equations for the NAND gate. The dashed line in figure 7-1 is applicable only to the expandable gate and shows the connection made when an expander circuit is used. (See expander description in this section.) All expandable gates used in the reader are DTL elements.

The output of a NAND gate is "1" if any input is "0". The output is "0" only when all inputs are "1". In figure 7-1, output D for a nonexpandable gate will be "1" if A or B or C is "0", and will be "0" only when A and B and C are all "1".

An expandable NAND gate output is "1" if any input to the gate or expander is "0". To obtain a "0" output for the expandable gate, all inputs to the gate and expander must be "1". Inputs A, B, and C and all inputs to the expander [E] must be "1" before output D is "0". If the input to A, B, or C or any input to the expander is "0", the output D will be "1".

The [E] symbol in the logic equation denotes that the expander input to the NAND gate is the result of an AND function performed within the expander and not within the NAND gate. NAND gates used in the reader are listed below.

Type	Type	Type
1	21	46
3	24	74
7	28	92
8	29	93
14	30	94
17	35	102
19	37	104

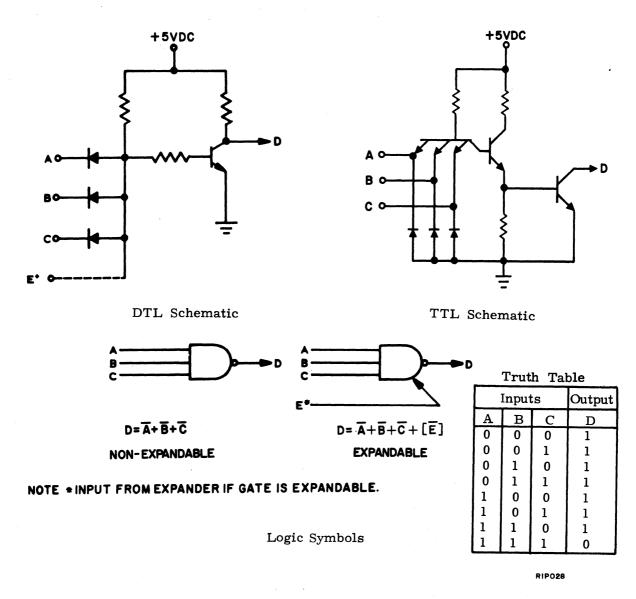
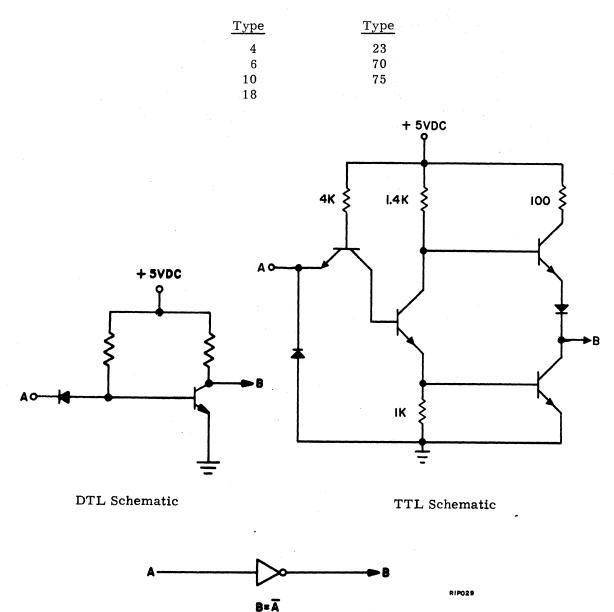


Figure 7-1. NAND Gates

Inverters

Inverter circuits provide binary complementing ("1" to "0"; "0" to "1") from input to output. Typical inverter schematics, logic symbol, and logic equation are shown in figure 7-2. Inverter circuits act as common-emitter amplifiers of unity gain.

All inverter elements used have six circuits per element, each circuit having one input and one output. Differences among the inverter elements used exist in the input and output loading factors, presence or absence of input diodes, and presence or absence of output pull-up transistors and resistors. The inverter output is "1" when the input is "0" and vice-versa.



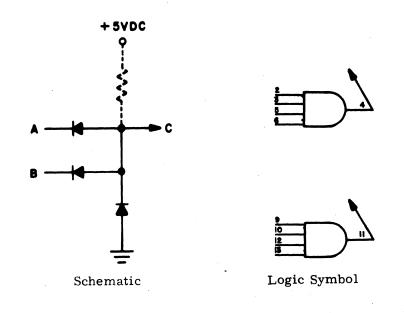
Inverters used in the reader are listed below.



Figure 7-2. Inverter

Expander

An expander increases the number of inputs to a gate and consequently increases the number of signals processed by one gate. The expander can only be used with an expandable gate. The type 22 expander circuit is shown in figure 7-3. When the output of the expander is connected to a NAND gate input, as illustrated in figure 7-1, the expander will operate as an AND gate and inputs A and B must be "1" in order for output C to be "1". If either input is "0", C will likewise be "0". The dashed part of figure 7-3 depicts the connection made within a NAND gate. With this connection the logic equation is $C = A \bullet B$.



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Figure 7-3. Expander

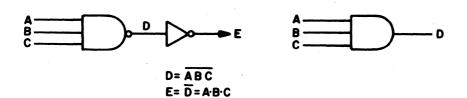
AND, OR, NOR Gates

NAND gates and inverters can be connected to provide AND, OR, and NOR logic functions. Figure 7-4 shows the NAND gate and the inverter connections necessary to obtain the AND, OR, and NOR functions.

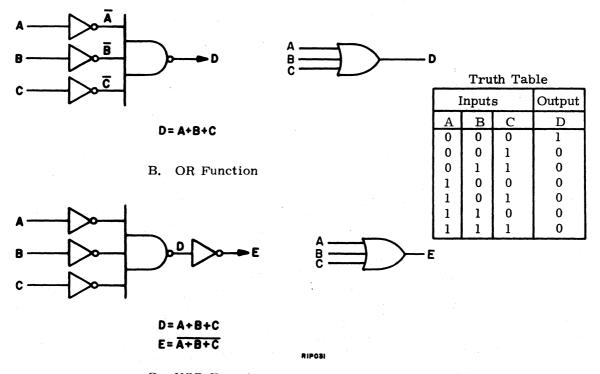
The AND function requires that the output be "0" if any one input is "0", and that the output be "1" when, and only when, all inputs are "1". The AND function is obtained by connecting an inverter circuit to the NAND gate output. The resulting logic symbol and equation are shown in figure 7-4A. If A or B or C is "0" at the NAND input, the NAND output will be "1". This "1" is then inverted to "0" by the inverter. When A, B, and C are all "1", the NAND gate output is "0" and the inverter output is "1". Thus, the inverter output with reference to the NAND gate input conforms to the logic operation required of an AND gate.

Implementation of the OR function requires that the output be "1" if any input is "1", and that the output be "0" when, and only when, all inputs are "0". To obtain the OR function, inverters are connected to each NAND gate input as shown in figure 7-4B. Thus, all inputs

are inverted before application to the NAND gate. If A, B, and C are "1", "0", and "0" respectively, the inverter output for A, B, and C is "0", "1", and "1", respectively. Within the NAND gate the "0", "1", and "1" are ANDed to "0" and inverted to a "1" output. When A, B, and C inputs are all "0", the inverter circuit outputs are "1". The three "1" inputs to the NAND gate are then ANDed to "1", which is then inverted to a "0" output. Thus, the inverter inputs with respect to the NAND gate output conforms to the logic operation of an OR gate. NOR operation is the inverse of an OR operation. Therefore, by connecting an inverter at the output of the OR circuit, shown in figure 7-4B, the NOR function is obtained as shown in figure 7-4C. Thus, the output of the OR circuit is inverted and the OR-invert combination satisfies the requirements of a NOR gate.



A. AND Function

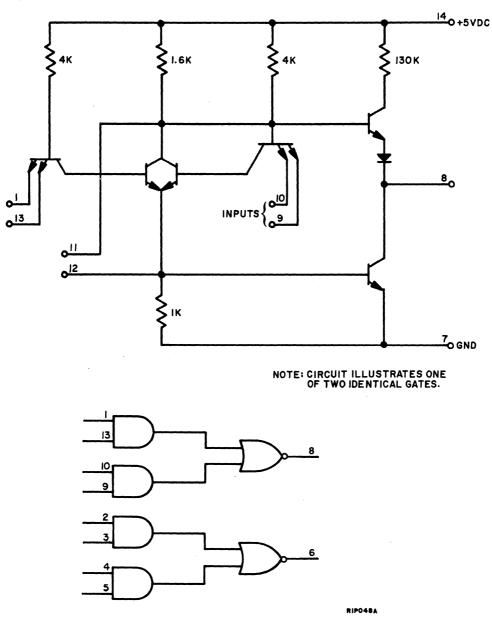


C. NOR Function

Figure 7-4. Implementation of AND, OR, and NOR from Basic NAND Logic

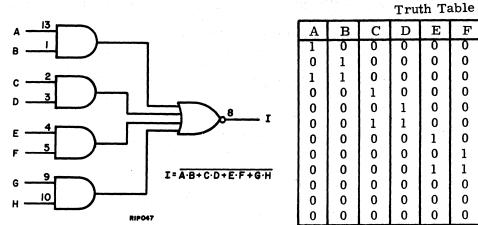
AND-OR-Invert Gates

The types of AND-OR-Invert gates used in the reader are type 4, shown in figure 7-5, type 43, shown in figure 7-6, and type 60, shown in figure 7-7. The NOR gate functions as an inverter for any of the AND gate outputs; the chips thus function like two (or four) NAND gates tied in parallel.

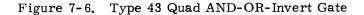


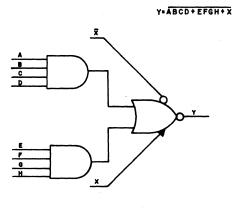
Logic Symbol

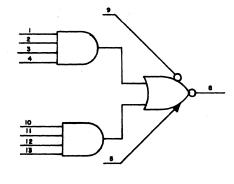
Figure 7-5. Type 4 Dual AND-OR-Invert Gate



	1.1.1							
Α	B	С	D	Е	F	G	H	Ι
1	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0
1 0	0	1	0	0	0	0	0	1
0	0	0	1	0	0	0	0	1
0	0	1	1	0	0	0	0	0
0	0	0	0	1	0	. 0	0	1
0	0	0	0	0	1	0	0	1
0	0	0	0	1	1	0	0	0
0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	1	0







LOGIC SYMBOL

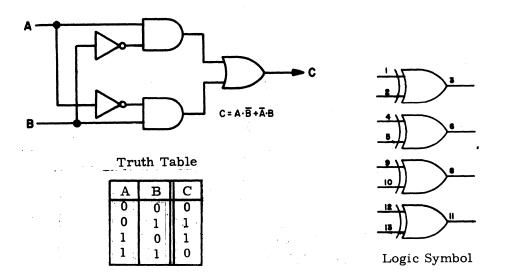
R4F005

Figure 7-7. Type 60 AND-OR Inverter

Exclusive OR Gate

FUNCTIONAL LOGIC

The exclusive OR gate (type 33) performs an "either but not both" function. Output C, as shown in figure 7-8, is "1" only when inputs A and B are complementary. If A and B are the same logic level, output C is "0".



RIPO38A

Figure 7-8. Type 33 Exclusive OR

MONOSTABLE MULTIVIBRATORS

The monostable multivibrator (one-shots) used in the page and document reader are types 31, 109, and 78. The logic symbols and truth tables for these multivibrators are shown in figures 7-9 and 7-10.

The type 31 chip consists of a one-shot flip-flop with gated trigger inputs. Triggering is controlled by ANDing a dual negative-transition trigger input (A1 and A2) with a positivetransition trigger input (B); the B input can also be used as an inhibit line. Triggering occurs either when B is held high and one or both of the A inputs decrease, or when one A input is held low and the B input increases. Triggering occurs at a particular voltage level and is not related to pulse transition time. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components.

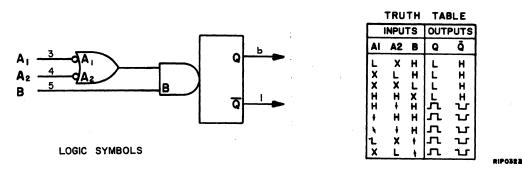
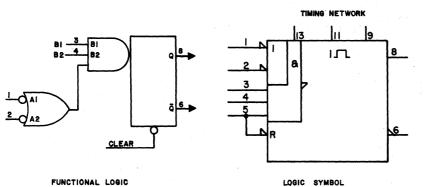


Figure 7-9. Type 31 Monostable Multivibrator

The types 109 and 78 are similar to the type 31, with the addition of master clear inputs and retrigger capability. When the clear input is "0", the flip-flop is reset and further change of state is inhibited. The clear input can terminate the output pulse at any point, or can function as a high-level trigger when A is low and B is high. The retrigger

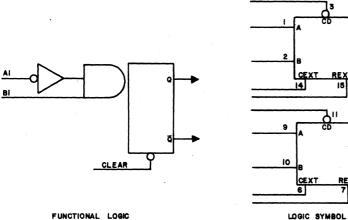
48430080 C



	ŤF	NUT	H .	TAB	LE	
	INF	UTS	1		OUT	PUTS
CLEAR	AI	A2	BI	82	Q	ą
	XHXXLLLXXXN++	X N X X X X X L L L + + N		***	יייייללילללל	לללל *לל ****
+	L X	X L	H	H	Л	꾼

FUNCTIONAL LOGIC

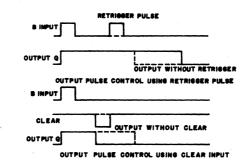
A. TYPE 109 Monostable Multivibrator



TRUTH TABLE								
INPUTS OUTPUTS								
CLEAR	A		Q	ð				
L	x	X	L	н				
x	н	X	L	н				
x	×	L	L	н				
н	L	+	л	പ				
н	н	л	ഹ					
1 4 -	L	н	л	ប				

FUNCTIONAL LOGIC (ONE FLIP-FLOP)

B. TYPE 78 Dual Monostable Multivibrator



REXT

15

11

C. RETRIGGER/CLEAR PULSE CONTROL

R4F004

Figure 7-10. Retriggerable Monostable Multivibrators

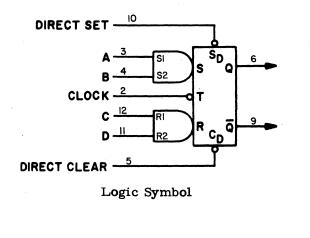
capability allows the flip-flop to be retriggered at the B (high-level) input before the output pulse terminates, allowing the generation of a long-duration output pulse. The combination of clear and retrigger provides an infinitely variable output pulse width. The type 78 differs from the 109 in having only one each A and B input, and in having two independent multivibrators rather than one.

BISTABLE MULTIVIBRATORS

Bistable multivibrators (flip-flops) used in the reader are of the R-S (reset-set), D (delay) and J-K types.

R-S Flip-Flops

The R-S (reset-set) flip-flop (type 27) is a binary flip-flop distinguished by individual set and reset inputs. The Q output of the clocked R-S flip-flop shown in figure 7-11 can only be set to "1" when the A and B inputs are both "1" or when a direct set (S_D) input is applied. Q can only be set to "0" by both C and D inputs being "1" or by the application of a direct clear (C_D) input. The outputs Q and Q can only change state with the falling edge of the clock pulse. Should all inputs, A, B, C, and D be "1", the Q and Q outputs of R-S flipflops are indeterminate. This is depicted in the truth table of figure 7-11. In this table, "Qn" denotes the last state of the flip-flop previous to any input and "U" signifies that the output is indeterminate.



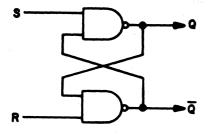
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				Outputs				
0 0 0 1 1 0 1 0 0 1 1 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 0 1 0 0 0 0 1 0	s _D	C _D	Α	в	С	D	ୡ	ାଦ
	0 0 0 0 0 1	0 0 0 0 0	0 0 1 0 1 0	0 0 1 0 0 1 0	0 1 0 1 0 0 0 0	1 0 0 1 0 0 0 0	Q _n Q _n Q 1 1 0	1 0 0 1

Truth Table

Figure 7-11. R-S Flip-Flop

Two NAND gates can be connected to function as an R-S flip-flop having one set and one reset input. The circuit, shown in figure 7-12 along with the associated truth table, is commonly referred to as a latch, and is used extensively in reader logic circuits. $"Q_n"$ in the truth table denotes the output logic state present prior to the inputs and "U" indicates that the output is indeterminate.

7-19



Logic Symbol

Truth Table

Ing	outs	Outputs				
S	R	Q	Q			
0	0	Q n 0	\overline{Q}_{n}			
1	0	0	1			
0	1	1	0			
1	1	U	U			

RIP034

Figure 7-12. NAND Latch

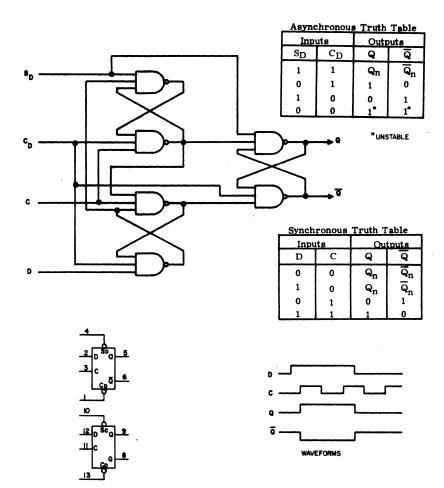
Type D Flip-Flop

The type D flip-flop (type 38) is used in applications requiring temporary information storage; it is basically an R-S flip-flop with only one data line (D). An enable or clock signal applied to the C input transfers data on the D line to the output Q as shown in figure 7-13. When the C input changes to "1", the Q output will assume the same state ("1" or "0") as the input at D. When the C input goes to "0", the Q output remains fixed at the last D input present prior to the C input becoming "0". During the time the C input is "0", the Q output cannot be changed. A "0" applied to the direct preset (S_D) input sets the Q output to the "1" state. A "0" applied to the direct clear (C_D) input sets the Q output to the "0" state. The S_D and C_D functions are independent of the D and C inputs, and must both be high ("1") for the flip-flop to follow the D input. The Q output is the "not" (inverted) function of the Q output. The truth table for a type D flip-flop is presented in figure 7-13. Q_n represents the output logic state established prior to the present inputs.

J-K Flip-Flops

R-S flip-flop and NAND latch outputs are ambiguous when simultaneous "1's" are applied to the R and S inputs. In applications requiring the elimination of this output ambiguity, J-K flip-flops are used. J-K flip-flops use AND gate inputs to the set and clear sections of the flip-flop as shown in figure 7-14. By connecting one side of the J input AND gate to the \overline{Q} output and one side of the K input AND gate to the Q output, a complementing circuit is obtained which causes the Q and \overline{Q} outputs to toggle with the clock when both inputs are "1" (type 103 is a J-K flip-flop; the outputs toggle when J is "1" and \overline{K} is "0"). The flip-flop is set with the clock if only the J input is "1"; the flip-flop is cleared with the clock if only the K input is "1" (\overline{K} is "0"). Direct set and clear inputs override the J, K, and clock inputs.

The J-K flip-flops used in the CJ122 reader are types 5, 13, 16, 42, and 103. Figure 7-14 shows functional logic and waveforms typical of J-K flip-flops; figure 7-15 shows specific logic symbols and truth tables associated with the five types used in the CJ122.



Logic Symbol



R28033A

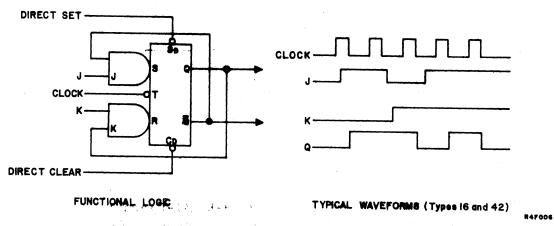
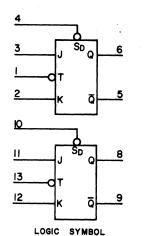


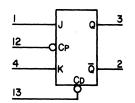
Figure 7-14. J-K Flip-Flop Characteristics

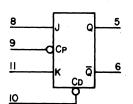
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	TRUTH T	ABL	E		
PRESET	CLOCK	J	К	ଦ	ାଦ
L	X	Х	х	Н	L
Н	<u>л</u>	L	L	Qn	$\overline{Q_n}$
Н	Л	н	L	H	L
Н	Л	L	н	L	н
Н	Л.,	н	н	тос	GLE

A. TYPE 5 FLIP - FLOP





LOGIC SYMBOL

Sn

SD

LOGIC SYMBOL

2

6

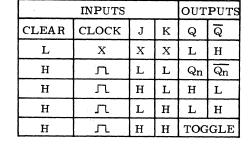
13

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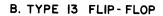
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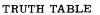
12

8



TRUTH TABLE

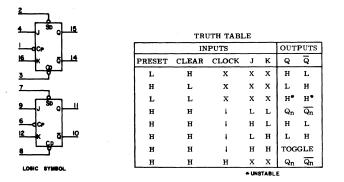


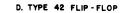


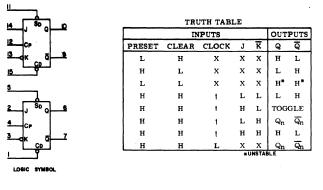
		INF	UTS			OUT	PUTS
	PRESET	CLEAR	CLOCK	J	к	Q	Q
	L	Н	X	х	x	H	L
	Н	L	Х	х	x	L	Н
-	L	L	X	х	х	н*	н*
	н	H	Ļ	L	L	Qn	\overline{Q}_n
	н	Н		H	L	H	L
	H	Н	ţ	L	H	L	Н
	H.	H	4	H	H	TOG	GLE
	н	Н	н	x	х	Q_0	\overline{Q}_0
· · · ·			*UN	ISTA	BLI	2 R41	017
C. TYPE 16 FLI	P - FLOP						

Figure 7-15. J-K Flip-Flops, Truth Tables and Logic Symbols (1 of 2)

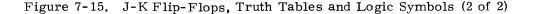
7-22











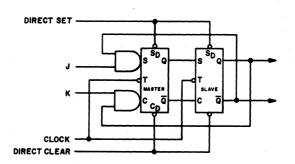
MASTER-SLAVE FLIP-FLOPS

Three of the flip-flops used in the reader (types 5, 13, and 27) operate on the master-slave principle; that is, input information is stored in an input flip-flop (master) at the leading edge of the positive clock pulse and is transferred to an output flip-flop (slave) at the trailing edge of the positive clock pulse.

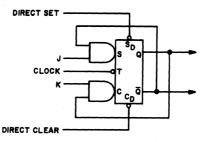
A J-K master-slave flip-flop configuration is shown in figure 7-16A. The master and slave flip-flops are directly coupled. Outputs Q and \overline{Q} of the slave are connected to the K- and J-AND-gate inputs respectively, to provide complementing. Complementing ensures that the Q and \overline{Q} outputs change state when the J and K inputs are both "1" prior to the trailing edge of the positive clock pulse.

The master-slave flip-flop logic symbol is shown in figure 7-16B. Note that, in figure 7-16B, although only one flip-flop symbol is used, a master and slave (two flip-flops) exist within each such symbol.

A general rule for flip-flops operated on the master-slave principle is: If one or more inputs that affect the master flip-flop are present at the leading edge of the positive clock pulse, the flip-flop will respond only to the last input present prior to the trailing edge of the clock pulse.



A. Master and Slave J-K Flip-Flop Functional Logic



B. Logic Symbol for J-K Master-Slave Flip-Flop

RIPO37

Figure 7-16. J-K Master-Slave Flip-Flop

Latches

The following components are used for temporary storage of four bits. Each latch consists of four type D flip-flops. The type 11 latch operates synchronously with the clock input; the type 99 latch operates without a clock input and is controlled by the master reset and enable lines.

Type 11 Latch

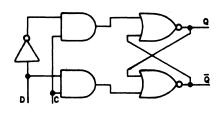
This latch (figure 7-17) assumes the state of the D input lines when the clock (enable) input goes high. The output state will remain at its last level while the clock is low, and is only affected by the D input when the clock again goes high. No master set or clear is provided. Two of the flip-flops have complementary outputs (Q and \overline{Q}), and two have only Q outputs.

Type 99 Latch

In this latch (figure 7-18), the output line of each flip-flop (Q) follows the input line (D) only if the following conditions are present:

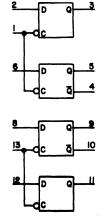
- 1. Master reset (MR) is high.
- 2. Enable (E) is low.
- 3. Set (S) for that flip-flop is low.

All flip-flops are reset when \overline{MR} goes low; the outputs of all flip-flops are fixed when \overline{E} goes high. The output of any individual flip-flop is fixed when both the D line and the S line go high.



FUNCTIONAL LOGIC

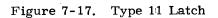
 $\begin{array}{c|cccc} D & C & Q & \overline{Q} \\ H & H & H & L \\ L & H & L & H \\ X & L & Q_n & \overline{Q_n} \end{array}$

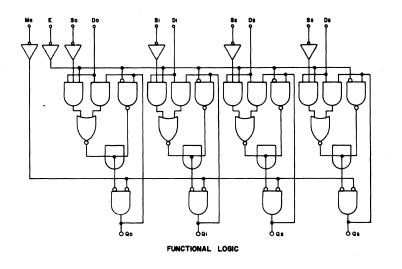


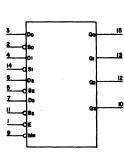


R4F014

TRUTH TABLE (EACH FLIP-FLOP)







LOGIC SYMBOL

84F018

MR	Е	D	s	Q
н	L	L	L	L
Н	L	H	L	н
H	L	L	н	L
H	L	н	н	Q _N
Н	н	х	x	Q _N
L	x	x	x	L

TRUTH TABLE (EACH FLIP-FLOP)

Figure 7-18. Type 99 Latch

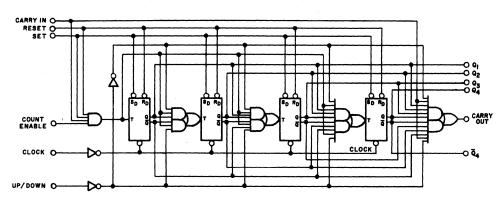
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7-25

COUNTERS

4-Bit Up/Down Counter

The 4-bit up/down counter (type 32), shown in figure 7-19 is a divide-by-10 (decade) or divide-by-16 (hexadecimal) counter. The circuit counts synchronously with the negative transition of the positive clock pulse input. The count direction is controlled from a single line (UP/DOWN input), where a "0" causes a down count and a "1" causes an up count. SET and RESET provide asynchronous entry to the counter and clear the counter for an output of all 0's or all 1's. The CARRY IN input increments the counter asynchronously. The output of the counter is the binary-coded-decimal (BCD) 8421 code at Q_1 through Q_4 , respectively. The complement of the highest order bit (\overline{Q}_4) is also provided at the output in addition to a carry output.

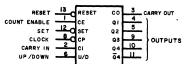


Functional Logic

		Asynch	ronous 1	ruth Tab	le
		Carry	Count	Up/	
Set	Reset	In	Enable	Down	Function
1	0	Х	Х	Х	"0"(0000)
0	1	х	Х	X	''15''(1111)

Synchronous Truth Table

		Carry	Count	Up/						
Set	Reset	In	Enable	Down	Function*					
1	1	0	X	Х	Hold					
1	1	Х	0	Х	Hold					
1	1	1	1	0	"Down"Count					
1	1 1 1 1 "Up" Count									
			s ync hr o n f clock p		negative-					



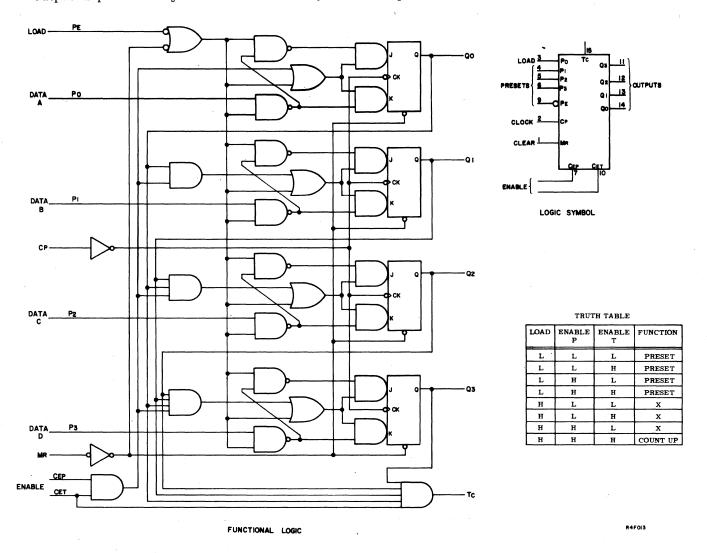
Logic Symbol

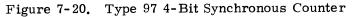
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Figure 7-19. Type 32 4-Bit Up/Down Counter

4-Bit Synchronous Counter

The CJ122 reader uses a 4-bit count-up synchronous binary counter (type 97), as shown in figure 7-20. The counter increments synchronously with the positive edge of the clock input when both enable inputs and load are high (1). The counter outputs can be preset to either high or low via the data lines; the presetting is synchronous with the next positive-going clock transition when the load input is low. The clear input is asynchronous and clears the counter when low, regardless of the clock state. When the counter is full (1111), a carry output is produced synchronous with the Q0 (LSB) output.





4-Bit Synchronous Up/Down Counter

The type 100 counter (figure 7-21) is a synchronous, reversible 4-bit binary counter. The four flip-flops are all triggered simultaneously by the low-to-high clock transition, provided the enable input is low. A high on the enable input inhibits the counter. The direction of

the count is determined by the state of the down/up input; when this input is low, the counter counts up, and when it is high, the counter counts down. The counter outputs may be preset to any level by placing a low on the load input and entering the desired level at the data inputs. The outputs will then change to agree with the data inputs independently of the clock, and will begin counting from this point on the next positive clock transition. The ripple clock and maximum/minimum outputs produce pulses when an overflow or underflow condition occurs. The ripple clock is a negative pulse equal in duration to one clock pulse (one-half clock cycle); the maximum/minimum output is equal in duration to one full clock cycle.

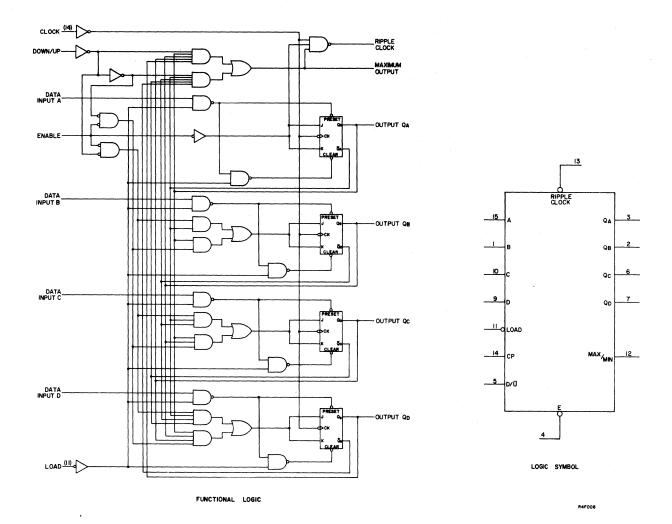
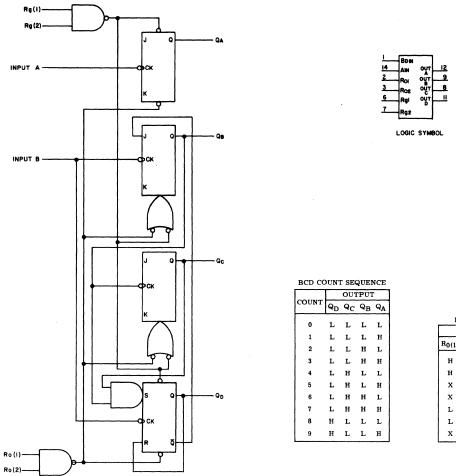


Figure 7-21. Type 100 4-Bit Synchronous Up/Down Counter

Decade Counter

The type 63 chip (figure 7-22) counts asynchronously from 0 to 9 BCD. The QA output must be connected to the B input to achieve this count length. The counter has gated reset inputs (Ro) and a gated set-to-nine input (Rg) for use in nines' complement counting.



F	RESET INPUTS					PUT		
R ₀₍₁₎	R ₀₍₂₎	R _{g(1)}	$R_{g(2)}$	Q_D	QC	$Q_{\mathbf{B}}$	QA	
н	н	L	х	L	L	L	L	
н	н	х	Ĺ	L	L	L	L	
х	х	н	н	н	L	L	H	
х	L	х	L	COUNT				
L	х	L	х	COUNT				
L	х	х	L	COUNT				
х	L	L	х		со	UNT		

R4F021

Figure 7-22. Type 63 Decade Counter

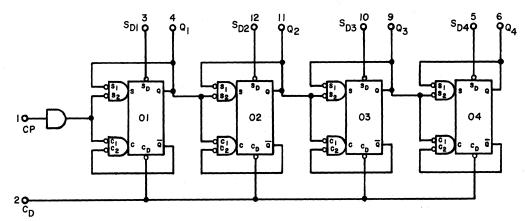
Divide-by-16 Counter

The divide-by-16 counter (type 36) is an asynchronous (ripple) counter that operates at frequencies up to 20 MHz. The outputs Q1 through Q4 correspond to the 8421 BCD code with individual direct sets (S_{D1} through S_{D4}) and a common direct clear (C_D). The counter sequence, the counter logic, and schematic circuits are shown in figure 7-23.

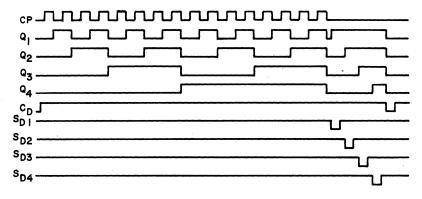
REGISTERS

4-Bit Parallel-In, Serial-Out Register

The 4-bit parallel-in, serial-out register (type 12) shown in figure 7-24 is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these circuits provide a register which performs either as a



Functional Logic



Counter Sequence

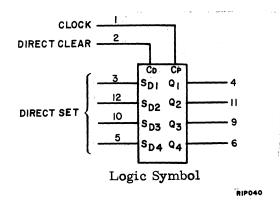


Figure 7-23. Type 36 Divide-by-16 Counter

serial-in, serial-out register or as a dual source parallel-to-serial converter. All flipflops are simultaneously set to "0" by applying a "1" to the Clear input. The Clear input will override the clock pulses but not the Preset inputs. The Preset inputs override both the Clock and Clear inputs.

The register is used in the reader as a dual source parallel-to-serial converter. Four bits of parallel data may be applied to the four register stages either by way of inputs 1A through 1D or by way of inputs 2A through 2D, depending on the logic states of the Preset 1 and Preset 2 inputs. The Preset 1 and 2 inputs enable one of the two parallel input paths. When a "1" is applied to Preset 1 with Preset 2 at "0", inputs 1A through 1D are enabled. When a "1" is applied to Preset 2 with Preset 1 at "0", inputs 2A through 2D are enabled.

Data transfer to the output occurs each time the clock input goes to "1". This transfer is from left to right with each flip-flop receiving the Q or \overline{Q} output of the preceding flip-flop at each positive clock pulse input. The Clear, Preset 1, and Preset 2 inputs must all be "0" when clocking occurs.

8-Bit Shift Register

The type 91 chip (figure 7-25) is a gated, clocked, 8-bit serial-to-parallel converter. Serial data received at either A or B is passed to the register only when the other input (A or B) is high. Data that passes the input AND gate is shifted down the register with each positive clock transition. If either input (A or B) goes low, the first flip-flop will be reset and further input of data at the other input will be inhibited; data in the register at this time will continue to be shifted down the register.

Dual 128-Bit Shift Register

The type 95 (figure 7-26) chip consists of two independent 128-bit MOS static shift registers, independently clocked. Each shift register has a recirculate input (RIN) and a recirculation control input (RC). Recirculation is enabled when RC is low. Data entered at DIN is shifted (stored) when the clock is high. When data is entered at RIN, "1" is stored when the clock is low, "0" is stored when the clock is high.

Quad 32-Bit Shift Register

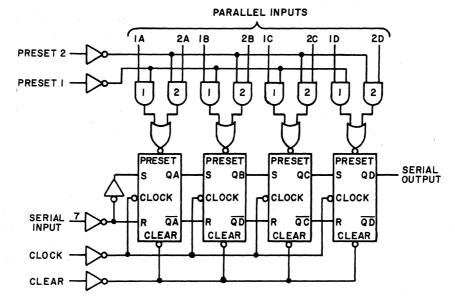
The type 96 chip (figure 7-27) contains four 32-bit static shift registers. Each register has a separate data input and output; a common clock input shifts all four registers. Data is read into the register when the clock is low and is shifted down the register on each positive clock transition. Data can be stored indefinitely in the register if the clock is stopped.

Dual 50-Bit Shift Register

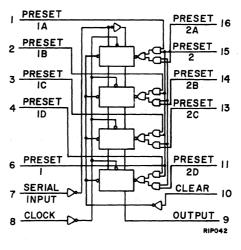
The type 90 chip (figure 7-28) contains two 50-bit static shift registers. Operation is similar to the SL-7-4032.

4-Bit, Right-Left Shift Register

The 4-bit, right-left shift register, (type 34) shown in figure 7-29, consists of four R-S master-slave flip-flops, four AND-OR-Invert gates, one AND-OR gate, and six inverterdrivers. Register shift direction, right or left, is dependent upon the logical input level to the mode control.

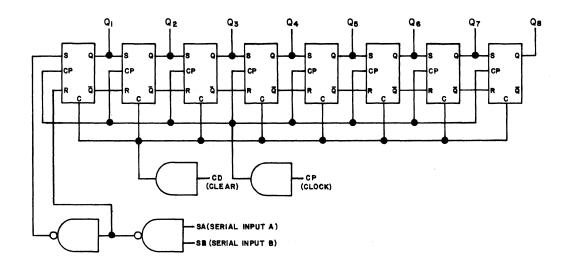


Functional Logic

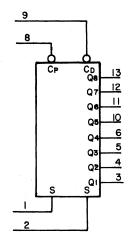


Logic Symbol

Figure 7-24. Type 12 4-Bit Parallel-In, Serial-Out Register







LOGIC SYMBOL

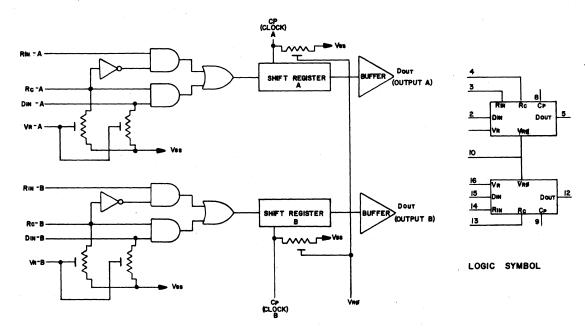
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Figure 7-25. Type 91 Shift Register

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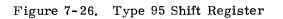
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7-33



FUNCTIONAL LOGIC

R4FOII



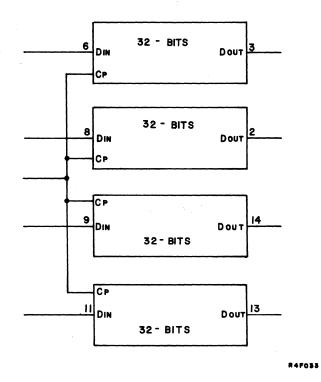


Figure 7-27. Type 96 Shift Register, Logic Symbol

48430080 C

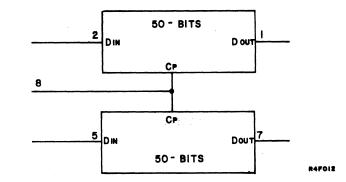


Figure 7-28. Type 90 Shift Register, Logic Symbol

When a "0" is applied to the mode control input, the #1 AND gates are enabled, the #2 AND gates are inhibited, and a right-shift mode of operation is enabled. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop, and the right-shift operation is initiated by the Clock 1 Right-Shift input. In the right-shift mode, serial data is entered at the serial (SI) input. The Clock 2 Left-Shift and parallel inputs I_1 through I_4 are inhibited by the #2 AND gates.

When a "1" is applied to the mode control input, the "1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the #2 AND gates are enabled to allow a left-shift of data entered via parallel inputs I_1 through I_4 . Shift-left operation requires external connection of each flip-flop output to the parallel input of the previous flip-flop. Data is then shifted left by the Clock 2 Left-Shift input.

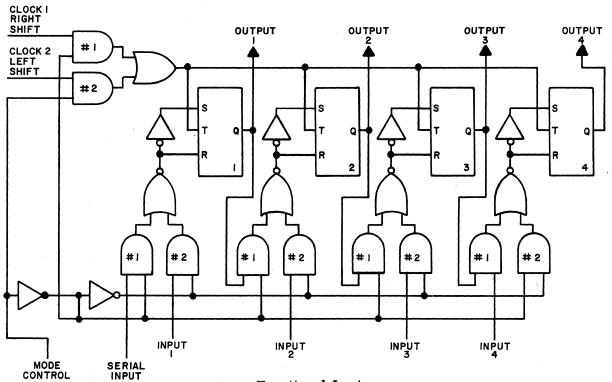
FULL ADDERS

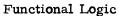
The full adders (types 39, 64, and 98) shown in figures 7-30 and 7-31, add binary numbers. The types 64 and 98 add two 2-bit binary numbers and the type 39 adds two 4-bit binary numbers. The type 98, which consists of two 1-bit adders, has provision in one of them for normal or inverted inputs, allowing it to be used for binary subtraction as well as addition. All the adders produce a sum output for each bit position and a carry output derived from the most significant bit. All the adders have a carry input to be used when paralleling with other adders.

DIGITAL/ANALOG CONVERTER

The D/A converter, (type 44), shown in figure 7-32, is an MSI, hybrid element that will accept a parallel, 8-bit, binary word at standard DTL logic levels and output a ± 15 volt analog value representing the input binary word. This converter has an enable input. A "1" on the Enable input allows manual converter operation which may be accomplished by logic input command or by permanently connecting pin 1 to pin 25. A "0" on the Enable input causes the converter output to remain at the negative 15V limit.

The D/A converter uses a resistive voltage divider network (called a ladder network) to convert digital input signals to output analog voltages. The resistors of the ladder network are weighted so that each bit contributes to the analog output according to bit value, with the most significant bit having the highest analog output and the least significant bit having the lowest. The input digital signal determines the analog output voltage by switching precise analog switches which are connected between the ladder network and a precision reference voltage. The ladder switches are either open or closed depending on the input binary code. The output analog range of the D/A converter is from -15V to +15V.





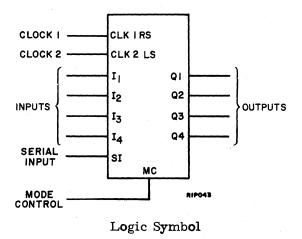
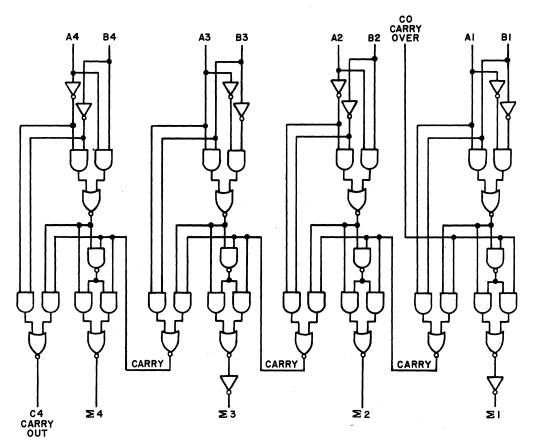


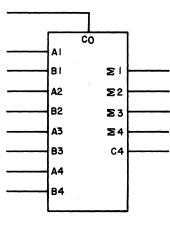
Figure 7-29. Type 34 4-Bit Right-Left Shift Register

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Functional Logic



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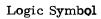
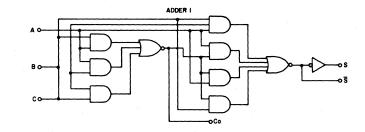


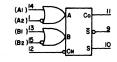
Figure 7-30. Type 39 4-Bit Binary Full Adder

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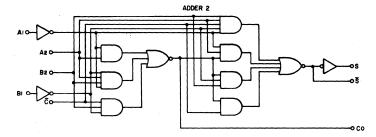
7-37



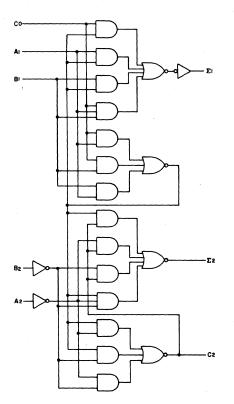




LOGIC SYMBOL



FUNCTIONAL LOGIC





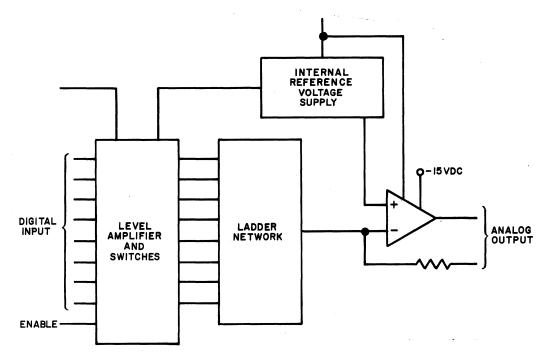
LOGIC SYMBOL

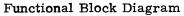
	INP	UTS			OUTPUTS				
				WHI	EN CO	= L	WH	EN CO) = H
A1	B1	A 2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
L	L	L	L	L	L	L	н	L	L
н	L	L	L	н	L	L	L	н	L
L	н	L	L	н	L	L	L	н	Ĺ
н	н	L	L	L	н	L	н	н	L
L	L	н	L	L	н	L	н	н	L
Н	L	н	L	н	н	L	L	L	н
L	н	н	L	н	н	L	L	L	н
н	н	н	L	L	L	н	н	L	н
L	L	L	н	L	н	L	н	н	L
н	L	L	н	н	н	L	Ľ	L	н
L	н	L	н	н	н	L	L	L	н
Н	н	L	н	L	L	н	н	L	H
L	L	н	н	L	L	н	н	L	н
H	L	н	н	н	L	н	L	н	н
L	н	н	н	н	L	н	L	н	н
н	н	н	н	L	н	н	н	н	н

FUNCTIONAL LOGIC

Figure 7-31. Type 64 2-Bit Binary Full Adders

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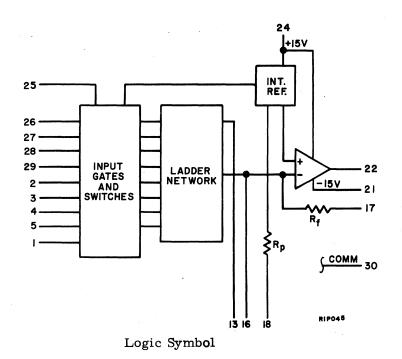


Figure 7-32. Type 44 8-Bit D/A Converter

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7-39

MULTIPLEXERS

Quad 2-to-1 Multiplexer

The type 69 chip (figure 7-33) selects one of two 4-bit inputs and transfers it to the output lines. Data selection is controlled by the Select input line (pin 1). When this input is low, data on the A (0) lines are selected for output; when Select is high, data on the B (1) lines are selected for output. The strobe (clock) input must be low for the Select line to have effect.

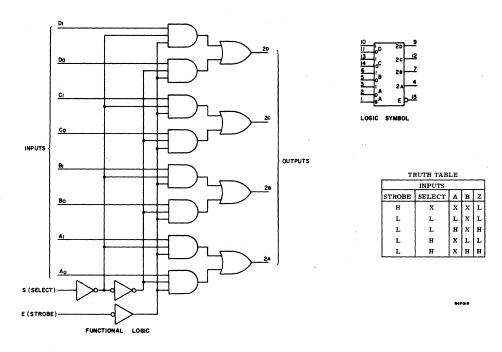


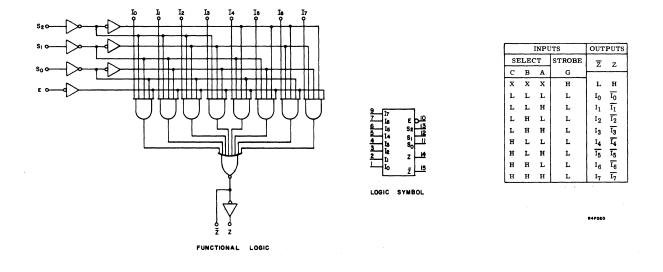
Figure 7-33. Type 69 Quad 2-to-1 Data Selector/Multiplexer

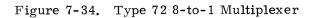
8-to-1 Multiplexer

The type 72 multiplexer, shown in figure 7-34, decodes a 3-bit data select code (000 to 111) to select one of eight data inputs for transfer to the output. The complement of the data selected is also output via a parallel inverter. When the strobe input is high, the Z output is forced high and the \overline{Z} output is forced low.

5-BIT COMPARATOR

The type 101 comparator (figure 7-35) compares two 5-bit binary words and generates a status bit on one of three output lines indicating "A greater than B", "A equal to B", or "A less than B". The output is gated out only when the enable line (\overline{E}) is low. Two comparators can be paralleled for use in comparing words longer than five bits by tying the A>B output from one comparator to an A input of the second comparator, and the A < B output to the corresponding B input.





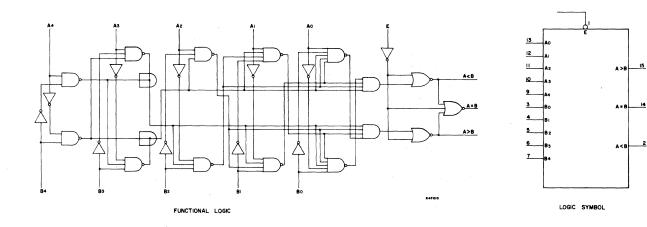


Figure 7-35. Type 101 5-Bit Comparator

POWER DRIVER

In the type 26 power driver (figure 7-36), the four 2-input NAND gates each drive highcurrent switching transistors.

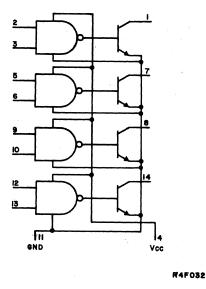


Figure 7-36. Type 26 Power Driver, Logic Symbol

VOLTAGE COMPARATOR

The type 58 differential voltage comparator (figure 7-37) compares two differential input voltages. When their algebraic sum is zero or negative, the voltage comparator conducts. When their algebraic sum is positive, the voltage comparator cuts off. When the strobe input is low, the voltage comparator is forced into a cutoff state. The output amplifier provides high output current and voltage capability.

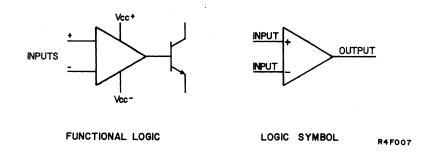
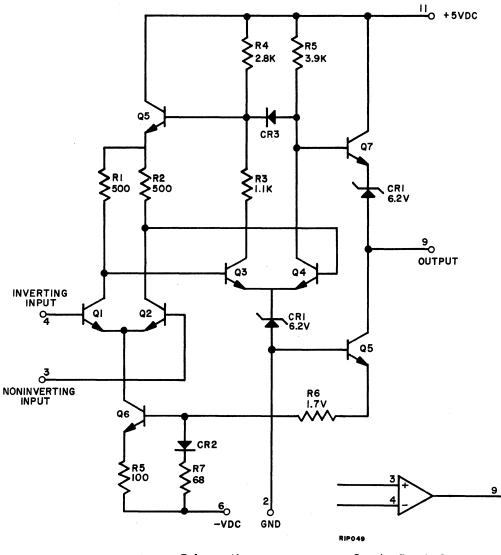


Figure 7-37. Type 58 Voltage Comparator

DIFFERENTIAL AMPLIFIER

The logic symbol and circuit for the differential amplifier (type 2) are shown in figure 7-38. This component acts similarly to the voltage comparator, except that the absence of an

output amplifier limits the output current; the output voltage swing is correspondingly limited to approximately 4V.



Schematic

Logic Symbol

Figure 7-38. Type 2 Differential Amplifier

OPERATIONAL AMPLIFIER

The logic symbol for the operational amplifier (type 45) is shown in figure 7-39. This component is designed for high stability and constant gain characteristics. Construction is similar to a differential amplifier; in operation the output is tied to the inverting input to provide negative feedback.

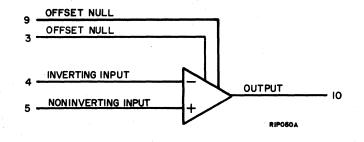


Figure 7-39. Operational Amplifier

DISCRETE COMPONENT ELEMENTS

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Discrete component elements constructed according to CDC specifications are shown on the functional integrated circuit charts in the CJ122 Logic Rack Diagrams, Drawing No. 48950000 or 48950100. The diagrams are contained in volume 2.

COMMENT SHEET

MANUAL TITLE	CJ122	Models	С,	D,	Е,	F,	G,	Н,	_J,	and	Κ	Page	and	Docum	lent

Reader Volume 1 Hardware Maintenance Manual

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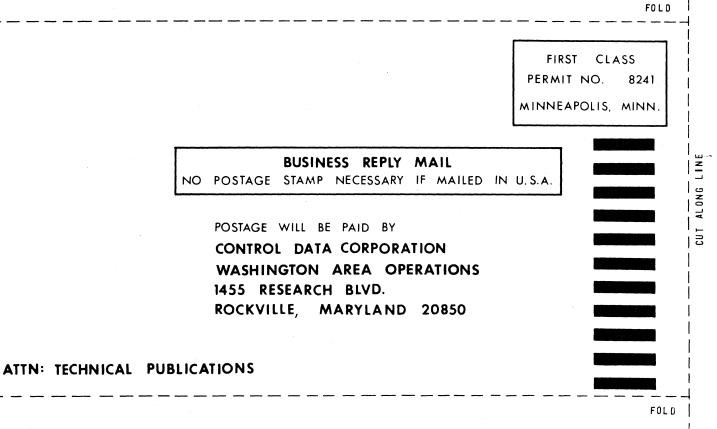
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