Printed Circuit Manual

VOLUME 1

CONTROL DATA

CORPORATION

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

REVISION RECORD

REVISION	DESCRIPTION
A	Corrections.
B	1604 Inverter Ground Rules and Hammer Storage Card 91 pages added.
C	Long Line Driver and Receiver Cards CA98 and HA26 pages added.
D	Corrections to card type C64 and C65.
E	Add index tabs, chapter headings, new Table of Contents addition to Appendix, type "E" and 1604 cards; and Delay Card P13A.
F	Replace the following pages 3-HA18-1 and 2; 4-C62 and C-61-5 and 6; Appendix pages 5 through 10. Add pages 4-60, 60A, 62 and 67-1 through 3; 4-79A-1, 5-97-1 and 2, 5-E10-1. Replace page 4-E12-1.
G	6600 information and circuit module schematics added as volume 3.
H	Volume 1, addition of revised record of revisions volume 2, addition of record of revisions. Replace the following revised pages; chapter 4 contents page, 4-C62 and C61-1, 4-C62 and C61-2, 4-C62 and C61-3, 4-C62 and C61-5, 4-C62 and C61-6, 4-C62 and C61-7, 4-P14A and P16A-3, 5-C94-3.
J	Volume 1, page 2-3600 inv-3 revised. Volume 2, chapter 5, second page of contents revised, removes pages 5-PED-1 through 5-PED-22. Chapter 6 added and Appendix 1, pages 16, 17, and 18 removed and new pages added.
K	Publication Change Order 11170. Record of Revisions for volumes 1 and 2 revised. Removed pages 15 through 31 of volume 2, Appendix 1 and replaced with revised pages.
L (10-5-65)	Change Orders 10344 and 10708. Pages v, vi, vii, viii of volume 1 revised. Chapter 4 contents page, 4-HA19-3, 4-HA37 and HA43-10, 4-P14C and P16A-1, 4-P14C and P16-2, 4-P14C and P16-A-3, chapter 5 contents pages, 5-C84-1, 5-C84-2, 5-C84-3 (new pages), 3, 4, 7, and 8 (appendix) revised. Pages 5-C60-1, 5-C60-2, 5-C60-3, 5-C97-1, 5-C97-2, and 5-C97-3 added. Pages 5-HA27 and 5-HA28-1 and 5-HA27 and 5-HA28-2 revised.
M (12-13-65)	Change Order 12131. Appendix 1; pages 16 through 31 revised and pages 32 through 47 added.
N (5-13-66)	Publication Change Order 12940. New peripheral equipment cards added to chapter 6; ADH, ITA/ITB/ITC, ITD, TYA, OJB, OYA, and UJB. Revised text for page; 6-OHA-1. Revised schematic for page 6-IAA, IAB-2. Appendix 1 revised. This revision obsoletes all editions of pin assignments- 1604 and 3600. Printed circuit cards, publication number 60106200, which is now included in this revision.
P (5-13-66)	Publication Change Order 13632. Pages 6-ISC-1 of chapter 6 is revised. The following new cards are added to chapter 6; ALA, AMF, AMG, AMH, AMI, ANB, ANC, AND, AUA, EUA, EUC, EVB, FCA, FCB, FDA, FGA, FHA, FIA, FJA, FKA, FLA, FLB, FMA, FNA, FPA, FRA, FSA, FTA, FUA, FVA, FWA, FYA, JBA, JCA, JDA, and OTA.
R (2-13-67)	Publications Change Order 15800. The following new cards added to chapter 6; AIB, AKA, AOA, ATA, ATB, AVA, AYA, BAA, BAB, BBA, BCA, EEG, EEH, EWA, EWB, EZA, FAB, FOA, FOB,

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REVISION RECORD (CONT'D)

REVISION	DESCRIPTION
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(Cont'd)	JEB, JEC, ONA, OUA, OVA, UEA, UHB, UIA, UJC, UKA, and UKB.
S	Publications Change Order 16541. The following new cards are added; AHC, AMJ, AMK, AMI, AVB,
(6-23-67)	AVC, AVD, AYB, BCB, BDA, BFA, BGA, BHA, BHB, BIA, BJA, EEK, EEL, EEM, EEO, EUD,
	EWC, FCC, FCD, FCE, FGB, FGC, FOC, FOD, FOE, FOF, FOG, FOH, FVB, FXC, GAB, GAC,
	GDA, GEA, GFA, GFB, GFC, GGA, HAA, IOE, IOF, ISH, JAD, JAE, JAF, JAG, OSC, OVB, TAA,
	ULA.
T	Engineering Change Order 20995, publications change only. The following new cards are added;
(11-22-68)	Card type 144, CC10, ADG, AMM, AMN, AMO, AMP, AMQ, AUB, AUC, AZA, BEA/B, BMA,
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	JAH, JAI, JED, JEE, JFA, JHB, JJA, JLA, JOA, JPA, OGD, OWB, PJA, PJB, UPA, URA, USA.
	The documentation for the following cards is affected by either revisions or page number changes;
	Card type 54, 74; HA18; C07C; HA20; HA27; HA28; HA35; AMF through AML; AUA, AVA, through
	AVD; FCA through FCE; FGA through FGC; FMA; FOA through FOH; FXB, FXC, FYA, HAA, IOB
	through IOF; JAD through JAG; UAA, UAB, UHB, ULA, pages 5, 20, and 21 under appendix 1.
	The following miscellaneous changes are being made: expansion from two to three volumes, re-
	labeling of chapter 6 tabs, and appendix 1 tab repositioned.
U	Engineering Change Order 28728, publications change only. Incorporates publications change
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	are revised: 3-HA14-3, V5-E08-2, 5-97-1, 5-97-2, 5-HA20-1, appendix 1 page 15.
V	Engineering Change Order 36403, publications change only. No effect on this publication.
(6-10-75)	
W	Manual revised; includes Engineering Change Order 37817, publications change only. Page
(2-23-77)	3-HA14-3 is revised.

PREFACE

This manual is for use by design engineers, maintenance personnel, and others who need detailed characteristics of CONTROL DATA* Printed Circuit Cards. A separate manual is available for those interested in schematics only. THE SCHEMATICS INCLUDED IN THIS MANUAL DO NOT NECESSARILY REFLECT THE LATEST REVISIONS.

The descriptions and schematics presented in chapters 2 through 5 are representative of the various types of circuits. Any user who desires more information about a given circuit may order a print of the schematic drawing from the cognizant division, using the drawing number from one of the tables in the appendix section. The schematic drawing bears the name of the designer, who may be contacted for first-hand information.

The appendix section of this manual contains tables listing all printed circuit cards produced by Control Data Corporation. Further up-to-date listings may be obtained by ordering the Standard Printed Circuit Card Index, available from Engineering Services, Computer Division.

Page numbering system used in this manual provides modularity so that additional circuit descriptions may be inserted without affecting the sequential order of page numbers. Additional descriptions may be obtained from the Technical Publications Department as they become available.

Every effort will be made to keep this manual current. Users are requested to notify the Technical Publications Department of any errors or suggestions for improvement.

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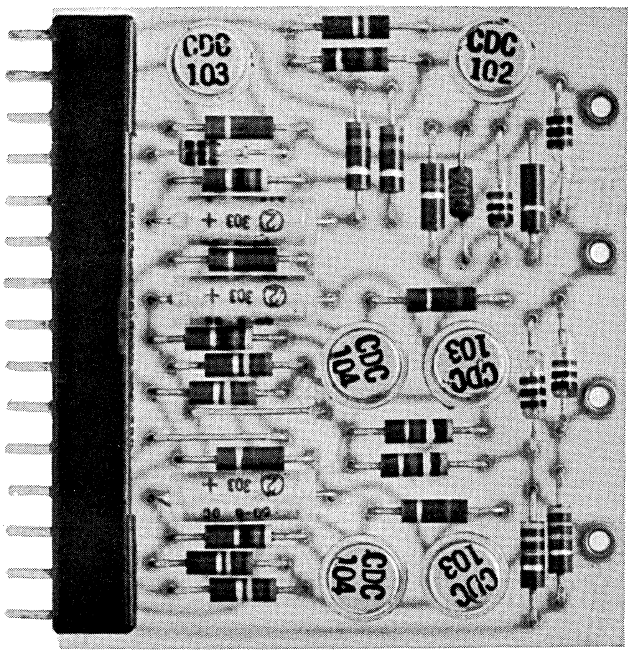
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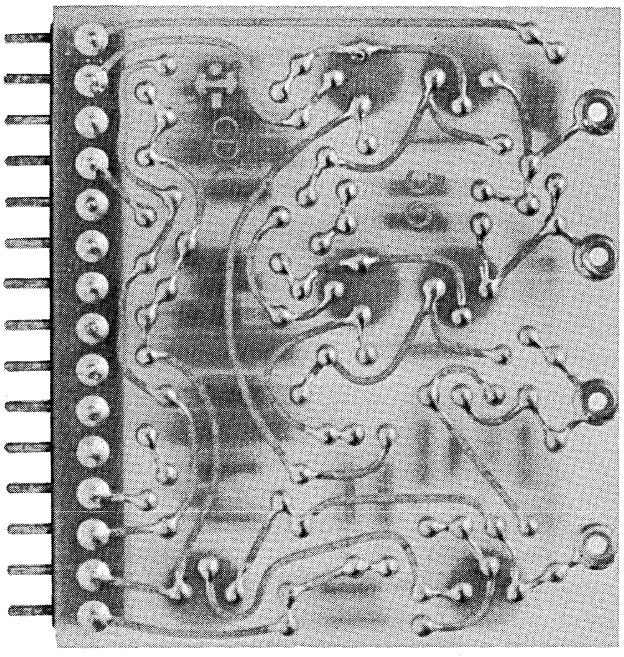


CONTENTS

A Contents page is included (where appropriate) at the beginning of each chapter and indicates the card types within that chapter.

CHAPTER 1. ELEMENTS OF CONTROL DATA LOGIC

The basic logic element in Control Data computers and peripheral devices is a transistor inverter circuit. A flip-flop (FF) is a combination of two inverters; a control delay is three inverters with clocked inputs. The major portion of a digital computer is built by interconnecting these circuits. Connections of inverters, flip-flops, and control delays form the various units of a digital computer, e. g., registers, counters, adders, complementers, and comparators. To facilitate the diagrammatic representation of these circuits the logic diagram technique is used. This technique emphasizes the functional aspect of a digital computer rather than the electronic aspect.

As a general rule, a digital computer has four main sections: Control, Arithmetic, Storage, and Input/Output. The Control and Arithmetic sections can be grouped under Logic section. Accordingly, the descriptions of the circuits in this manual are presented in four groups: Logic, Storage, Input/Output, and Special Purpose, (Chapters 2, 3, 4, and 5).

PRINTED CIRCUIT CARDS

Control Data electronic circuits are mounted on printed circuit cards (frontispiece). Each card is equipped with a 15 pin male connector for plugging into the equipment chassis. The printed circuit card technique has the advantages of ease of design and maintenance, use of solid state components, greater reliability, and modular construction.

INVERTER

The basic logic building block is an inverter circuit, represented by a rectangle as shown in figure 1-1. This circuit employs a 180^{o} electrical phase shift to produce an inversion; a "1" input results in a "0" output, and vice versa. In addition to use as an inverter, combinations of this basic logic element form bi-stable flip-flops and control delays.

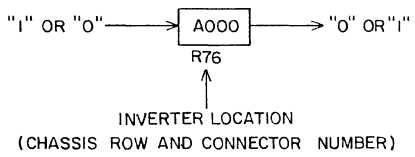


Figure 1-1. Conventional Inverter Symbol

FLIP-FLOP (FF)

A FF is two inverter circuits interconnected as shown in figure 1-2. Each rectangle represents a single inverter. One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a "1" signal on the set input. Conversely, it is placed in the "0" (cleared) state by a "1" signal on the clear input.

The storage capability of a FF means that the FF remains in the state in which it was placed by the last "1" input. Specifically, if a "1" signal is present at the set input, then the output of inverter K000 (figure 1-2) becomes "0". This output is applied as an input to K001 and its output then becomes "1". The output of K001 is fed back to K000. Thus, when the set input drops to "0", the feedback connection between K000 and K001 permits the storage of the state to which the "1" signal on the set input forced the FF. Should the clear input later receive a "1" signal the output of K001 becomes "0", and the feedback input to K000 is "0". Consequently, K000 furnishes a "1" output which is returned to K001 and replaces the "1" signal at the clear input.

When the FF is set, K001 has a "1" output and K000 has a "0" output. Conversely, when the FF is cleared, K001 has a "0" output, and K000 has a "1" output.

The conventional square or box symbol for a FF is used in figure 1-2 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

CONTROL DELAY

The function of the control delay is to synchronize a sequence of logic operations within the computer with the two-phase master clock. Logical "1" inputs are received during one phase time, either odd or even, and "1" outputs are provided during the next phase time, either even or odd. The phase time of the output is opposite the phase time of the input.

DEFINITION OF A CLOCK PHASE TIME

A clock phase time is the time during which an inverter driven by that phase has a "1" output. The input to the inverter is the raw clock signal received directly from the clock card. Thus during a clock phase time, the raw clock signal from that phase is a logical "0".

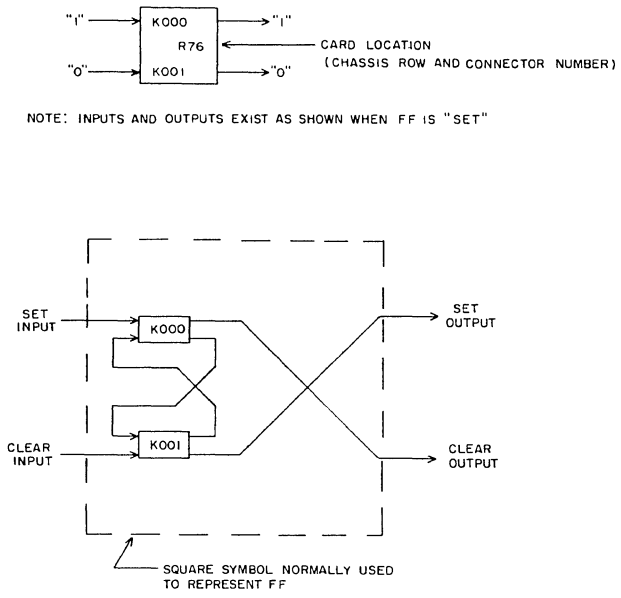


Figure 1-2. Conventional Flip-Flop Symbol

The response time of the inverter is approximately 1/4 to 1/2 a phase time. Thus the clock phase time always lags behind the raw clock signal, due to the delay of the inverter. However, this delay is not shown in the timing diagram of figure 1-4.

DESCRIPTION

The control delay consists of a FF having its feedback ANDed with a raw clock signal, and one or more inverters with two OR inputs each, which are driven by the A section of the FF and by a raw clock signal. The raw clock signal which enables the FF feedback is the phase opposite that which drives the inverter or inverters.

A diagram of a control delay symbol and the circuits encompassed by it is shown in figure 1-3. Figure 1-4 shows the timing of its operation.

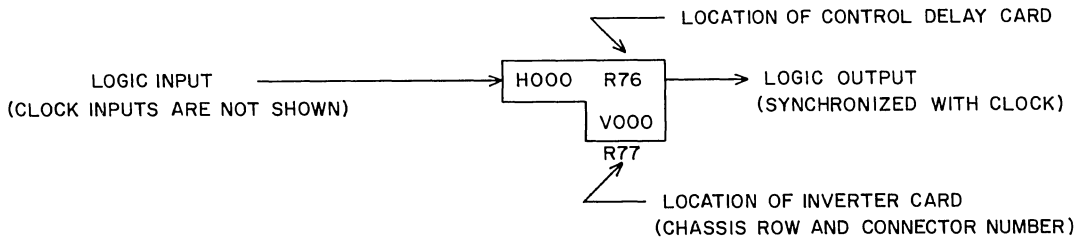
The clock inputs to a control delay are ordinarily not shown on a drawing. It is understood that the output occurs during the odd or even phase time, while the corresponding raw clock signal is a "0", depending upon whether the third superscript digit is odd or even. For example, control delay H100/V100 would have its output during an even clock phase time, while H101/V101 would have its output during an odd clock phase time.

The logic input to a control delay is gated by the external circuitry. Normally, the input drops to "0" shortly after the output appears, and is not repeated. If the input does not drop, then the output of the control delay is a series of pulses from the inverter, since it is driven by the raw clock signal.

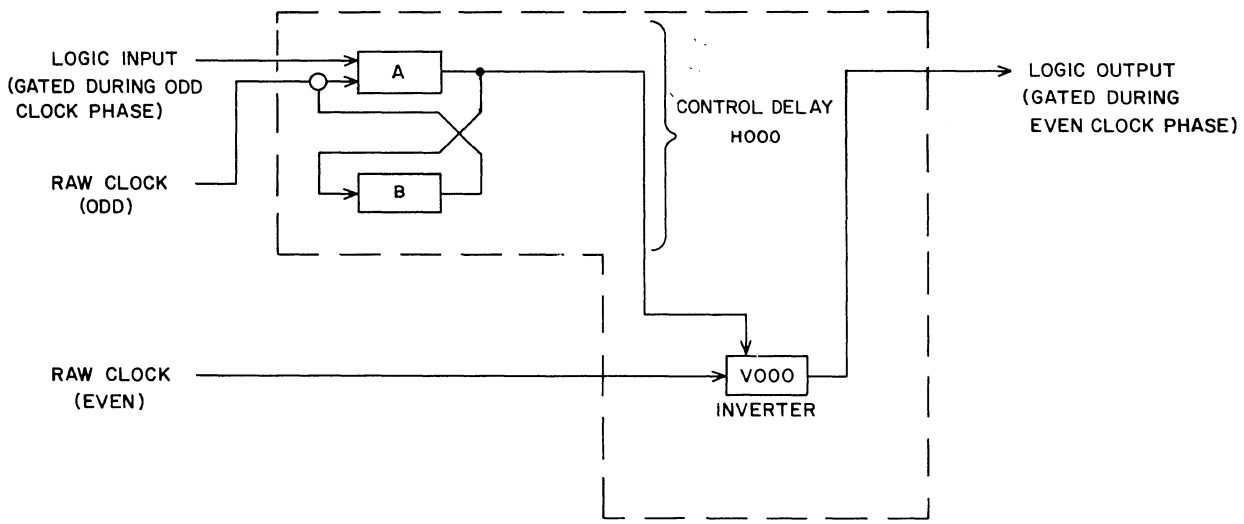
CIRCUIT OPERATION

Figure 1-3 shows that the gated logic input goes directly into the A section of H000. This forces the output of A to "0", resulting in a "1" output from B. The input to A is gated during the odd clock phase time; thus during this time, the odd raw clock signal is "0". When the odd raw clock signal becomes "1", the logic input to A drops, but the feedback path from B to A is enabled so that A continues to have a "0" output until the next odd clock phase time.

Inverter V000 is gated both by the output of A and by the even raw clock signal. With a "0" input from A, inverter V000 provides a "1" output during the even clock phase time, since the even raw clock signal is a "0". The "1" output from V000 continues until the next odd clock phase time disables the FF feedback, and the control delay returns to initial conditions.



NOTE:
INVERTER MAY BE REPRESENTED BY EITHER V---, N---, OR Y---.



NOTE:
LOGIC INPUT IS GATED INTO CONTROL DELAY WHILE ODD CLOCK PHASE IS "1". THE INPUT DROPS WHEN ODD PHASE BECOMES "0" AND IS NOT REPEATED.

Figure 1-3. Conventional Control Delay Symbol

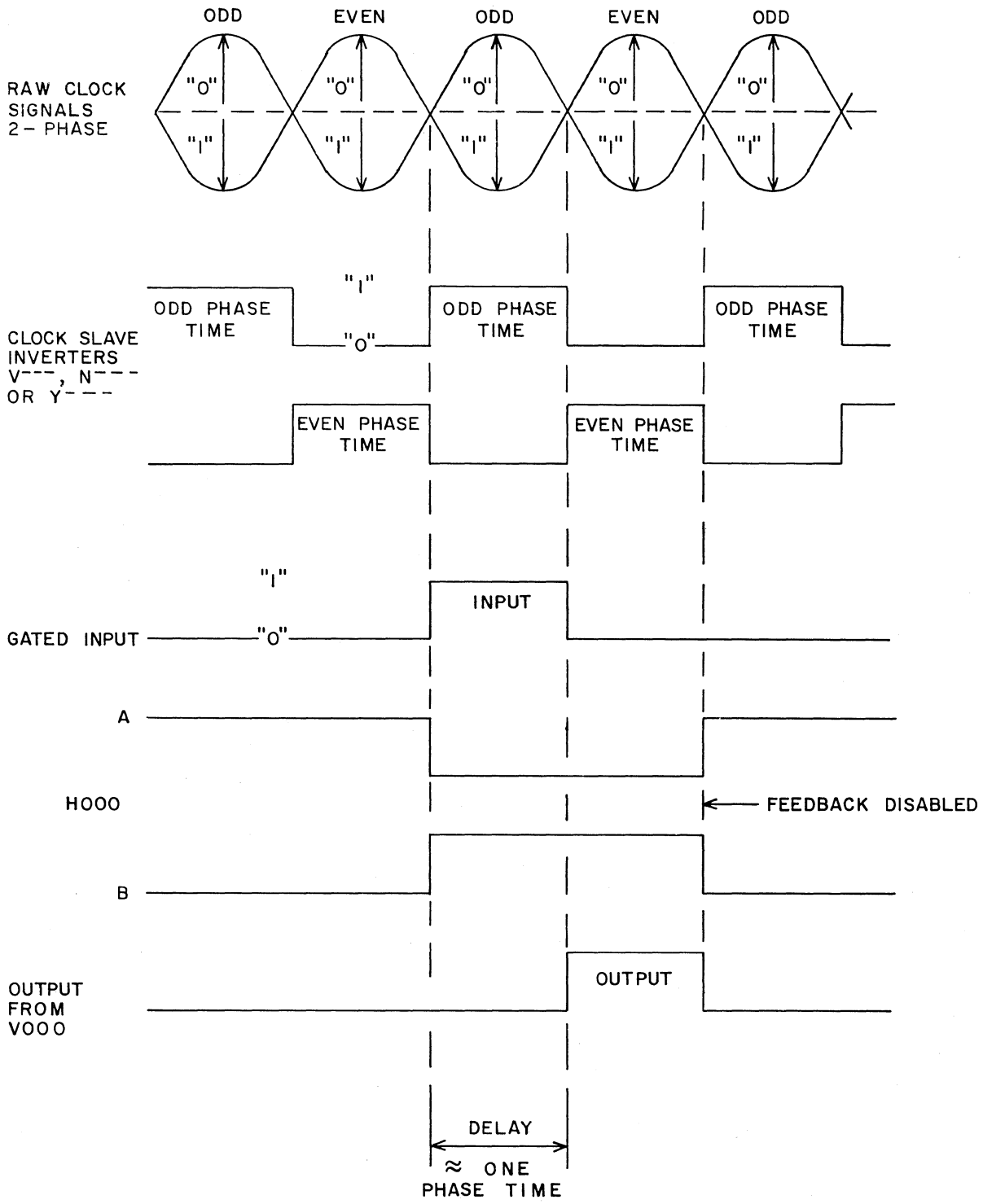


Figure 1-4. Control Delay Timing Diagram

LOGICAL EQUATIONS OF A CONTROL DELAY

A control delay may be represented by a minimum of two logical equations: one equation for the H--- term, and one equation for each V---, N---, or Y--- term. The symbol on the left of the equal sign is the subject term, and the expression on the right describes the configuration of its inputs.

All raw clock and gated logic inputs to a control delay are represented in its equations. The H--- term requires a logic input gated during a clock phase, and a raw clock signal which gates the FF feedback. The V--- term requires a raw clock signal to gate its output, and a logic input from the H--- term. These conditions are covered by the following basic rules:

1. Every input term of an H--- equation must contain one, and only one, clocked symbol such as V---, N---, or Y---.
2. The last term of an H--- equation must be a C--- (raw clock).
3. At least one input term of a V---, N---, or Y--- equation must contain an H--- symbol.
4. The last term of a V---, N---, or Y--- equation must be a C--- (raw clock) symbol.

A set of equations for control delay which would have an output during an even phase time could be written as follows:

H000 = Z024 W005 N001 + C001

V000 = H000 + C000

The symbols in the above equations refer to the following:

H000	A circuit on a control delay card which receives its input during an odd phase time, since the third superscript digit is even.
Z024	A logic input.
W005	A logic input.
N001	A clock slave inverter which provides a "1" input enabling the 3-way AND during an odd clock phase time.
C001	A raw clock signal which is a "0" during odd clock phase times; it is received at the control delay card and gates the FF feedback.
V000	The inverter portion of the control delay which provides a "1" output during an even clock phase time only.
C000	A raw clock signal which is "0" during even clock phase times and drives the control delay inverter.

LOGICAL "AND"

A three-input AND circuit is shown in figure 1-5. The small circle and connections used to represent this circuit on a logic diagram are also shown.

The AND gate requires that all inputs must be a "1" simultaneously. If any one of the AND inputs is a "0", then a "1" on another input is not sensed.

Thus, if the transistors A, B, and C are not conducting, their output diodes are biased in the reverse direction, and the resulting output signals are at the logical "1" level. This condition allows the -20v through the AND resistor to place a negative voltage on the base of transistor D, so that it conducts.

However, if any one of transistors A, B, or C is conducting, its collector goes to approximately ground potential. Its output diode is biased in the forward direction from the -20v through the AND resistor. This prevents the -20v source from applying drive current to transistor D, and transistor D is held in the non-conducting state.

LOGICAL "OR"

A three-input OR circuit is shown in figure 1-6 (the conventional logic diagram representation is also shown). An OR gate allows a "1" signal on any input to be sensed, although a "0" signal may simultaneously appear on another input.

Figure 1-6 shows three single-input ANDs connected to produce three logical OR inputs to transistor D. The input lines are separated by diodes, so that a "1" signal is not nullified by a "0" signal on another input line. Thus, if any one of transistors A, B. or C is not conducting so that it has a "1" output, the -20v through the respective AND resistor applies a negative voltage to the base of transistor D, causing it to conduct.

BASIC THREE-STAGE COUNTER

A counter is essentially a double rank register which increases or decreases the quantity stored, an increment at a time. The three-stage counter circuit shown in figure 1-7 is additive from binary 000 through 111.

A count is stored in two steps:

1. A "1" input on the Advance line sets a FF in rank 1. This occurs in consecutive order and when all three are set, the next

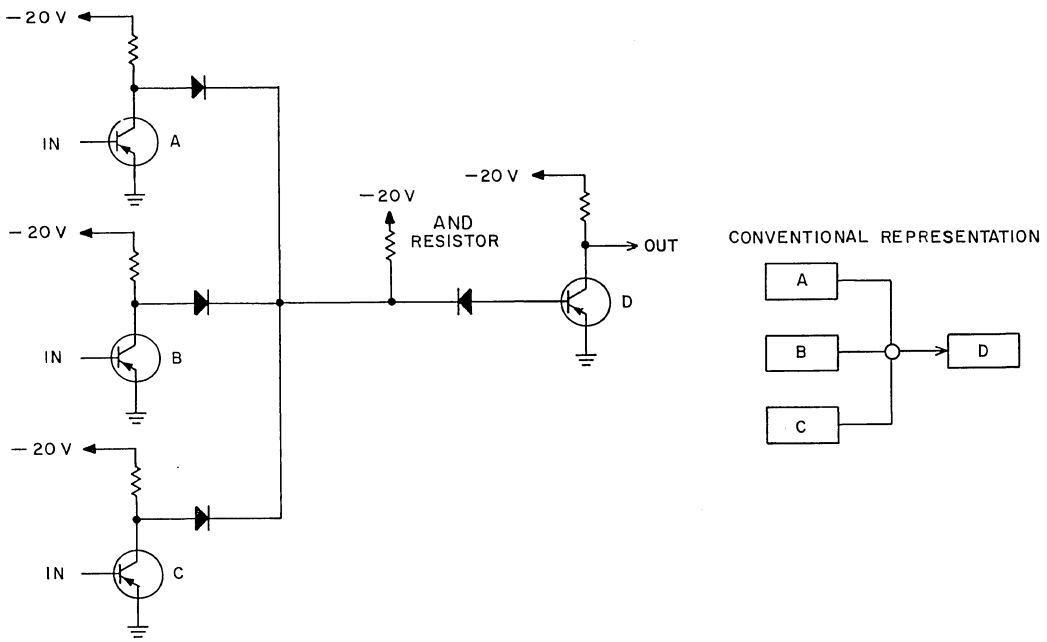


Figure 1-5. Logical AND

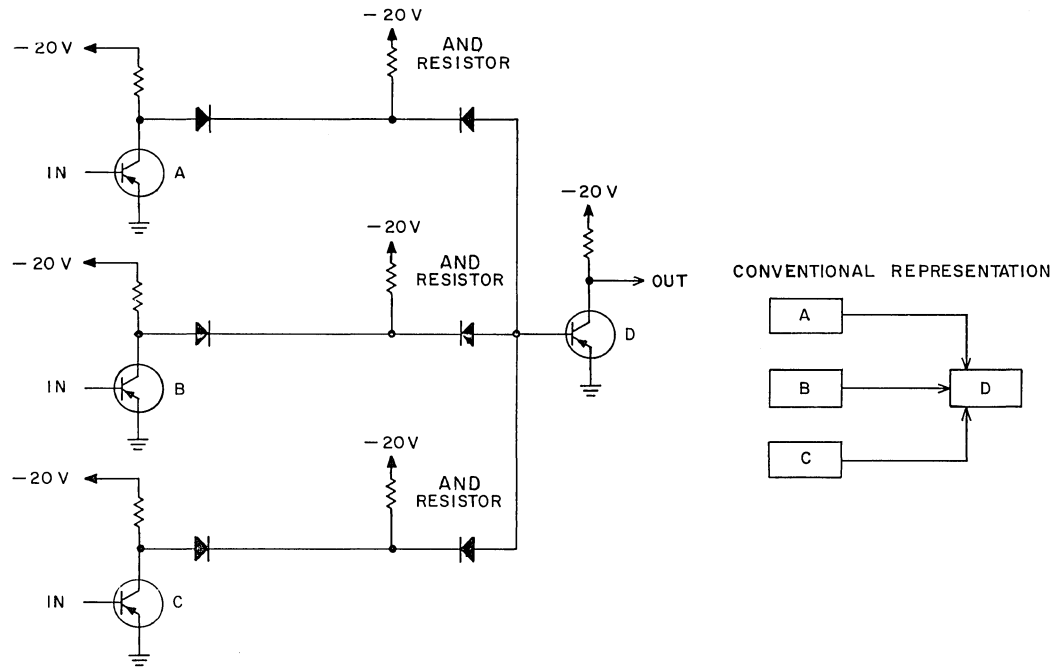


Figure 1-6. Logical OR

input clears them.

2. A "1" input on the Transfer line causes the FFs in rank two to assume the identical states as their corresponding FFs in rank 1.

To analyze the operation of the counter, assume that both ranks are initially cleared, so the count stored is zero. The first Advance command finds the AND gate to K000 enabled and therefore enters the count 001 (octal 1) into rank 1. This partially enables the AND gate to K002 so that the Transfer command enters the count 001 into rank two. The next Advance command finds the AND gate to K001 and K010 enabled and thus enters the count 010 (octal 2) into rank 1. The operation continues in this manner as shown in table 1-1 until the count reaches 111 (octal 7), which is the highest possible count in a three-stage counter. This is followed by a command sequence which returns both ranks to the count 000.

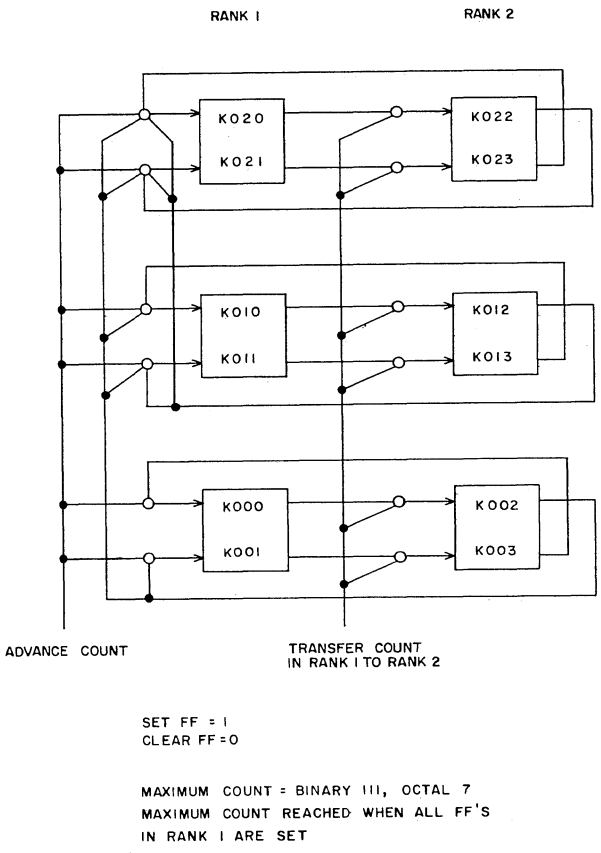


Figure 1-7. Basic Three-Stage Counter

TABLE 1-1. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

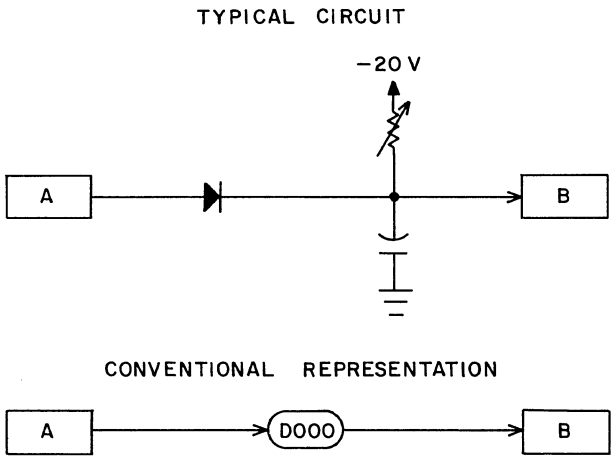
Command	Quantity Stored (Octal)	Rank 1			Rank 2		
		K02-	K01-	K00-	K02-	K01-	K00-
Initial conditions	0	0	0	0	0	0	0
Advance	1	0	0	1	0	0	0
Transfer		0	0	1	0	0	1
Advance	2	0	1	0	0	0	1
Transfer		0	1	0	0	1	0
Advance	3	0	1	1	0	1	0
Transfer		0	1	1	0	1	1
Advance	4	1	0	0	0	1	1
Transfer		1	0	0	1	0	0
Advance	5	1	0	1	1	0	0
Transfer		1	0	1	1	0	1
Advance	6	1	1	0	1	0	1
Transfer		1	1	0	1	1	0
Advance	7	1	1	1	1	1	0
Transfer		1	1	1	1	1	1
Advance	0(or8)	0	0	0	1	1	1
Transfer		0	0	0	0	0	0

CAPACITIVE DELAY

Capacitive delay circuits are constructed by placing a capacitor from the signal line to ground. The delay time is the time required to charge the capacitor when a "1" signal appears on the line. A "0" signal is delayed approximately one tenth as long as a "1". The method of connecting a delay between two logic cards, and the symbols used to represent this connection on a logic diagram are shown in figure 1-8.

Figure 1-8 shows that when the transistor on card A is conducting, its collector is almost at ground potential. Hence, the voltage across the delay capacitor is quite low and it contains very little charge. However, when the output of card A switches to "1" and its transistor stops conducting, the circuitry attempts to bias the input line at the "1" level. Initially this voltage is absorbed by the uncharged delay capacitor, which gradually obtains a charge as shown in figure 1-9.

Two factors govern the delay time: the size of the capacitor and the rate at which it receives charging current. Generally, the larger the capacitor, the longer the delay time. The delay time may be adjusted by varying the resistance in series with the capacitor. Increasing the resistance decreases current flow to the capacitor, increasing the delay time.



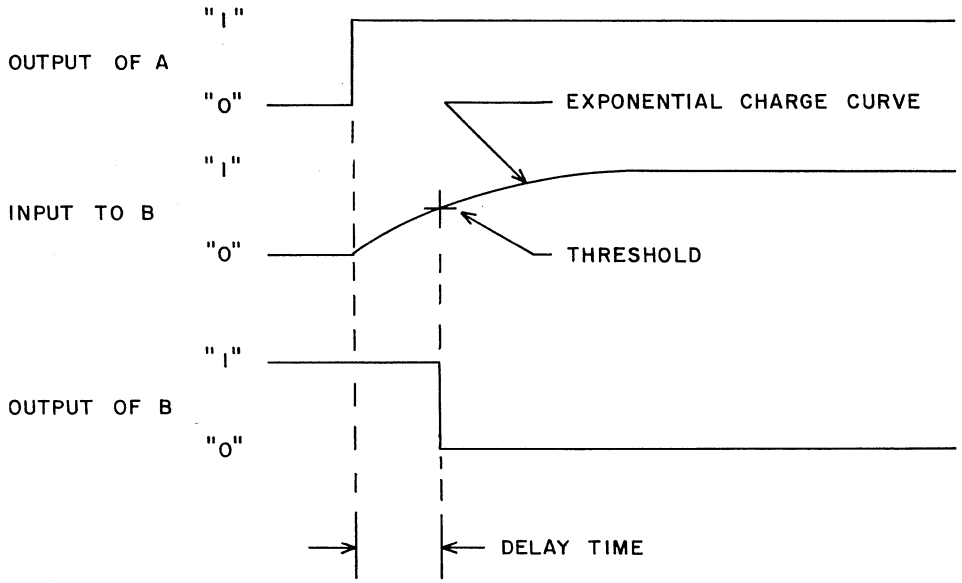
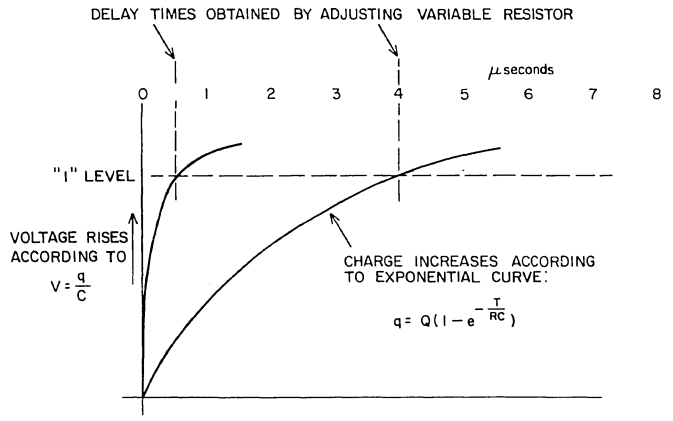


Figure 1-8. Capacitive Delay



NOTE:

SYMBOL	REFERS TO:	UNITS
T	TIME	SECONDS
q	PARTIAL CAPACITOR CHARGE	COULOMBS
Q	FINAL CAPACITOR CHARGE	COULOMBS
R	SERIES RESISTANCE	OHMS
C	CAPACITANCE	FARADS
V	APPLIED POTENTIAL	VOLTS
e	NATURAL LOGARITHM BASE	PURE NUMBER 2.718, APPROX.

Figure 1-9. Capacitor Charge Curve

PULSE FORMING NETWORKS

Many circuits contain pulse forming networks, consisting of two inverters and a capacitive delay, for the purpose of reshaping a steady "1" signal into a short "1" pulse. There are two types: those which produce a pulse upon receipt of a "1" signal and those which produce a pulse when the "1" signal ends. These types are known respectively as "leading edge" and "trailing edge" networks, and are presented in figure 1-10.

When a "1" input is received by a leading edge network, an immediate double inversion occurs, producing a "1" output. However, as soon as the capacitor is sufficiently charged, a "1" is sent directly into A001, and the output of inverter A001 switches to "0".

In the case of a trailing edge network, the steady input signal is fed directly into both inverters. Thus, when this signal goes to "0", the output of both inverters switches to "1". However, the "1" output of A000 does not reach A001 until the capacitor has charged sufficiently; at that time the output of A001 switches to "0".

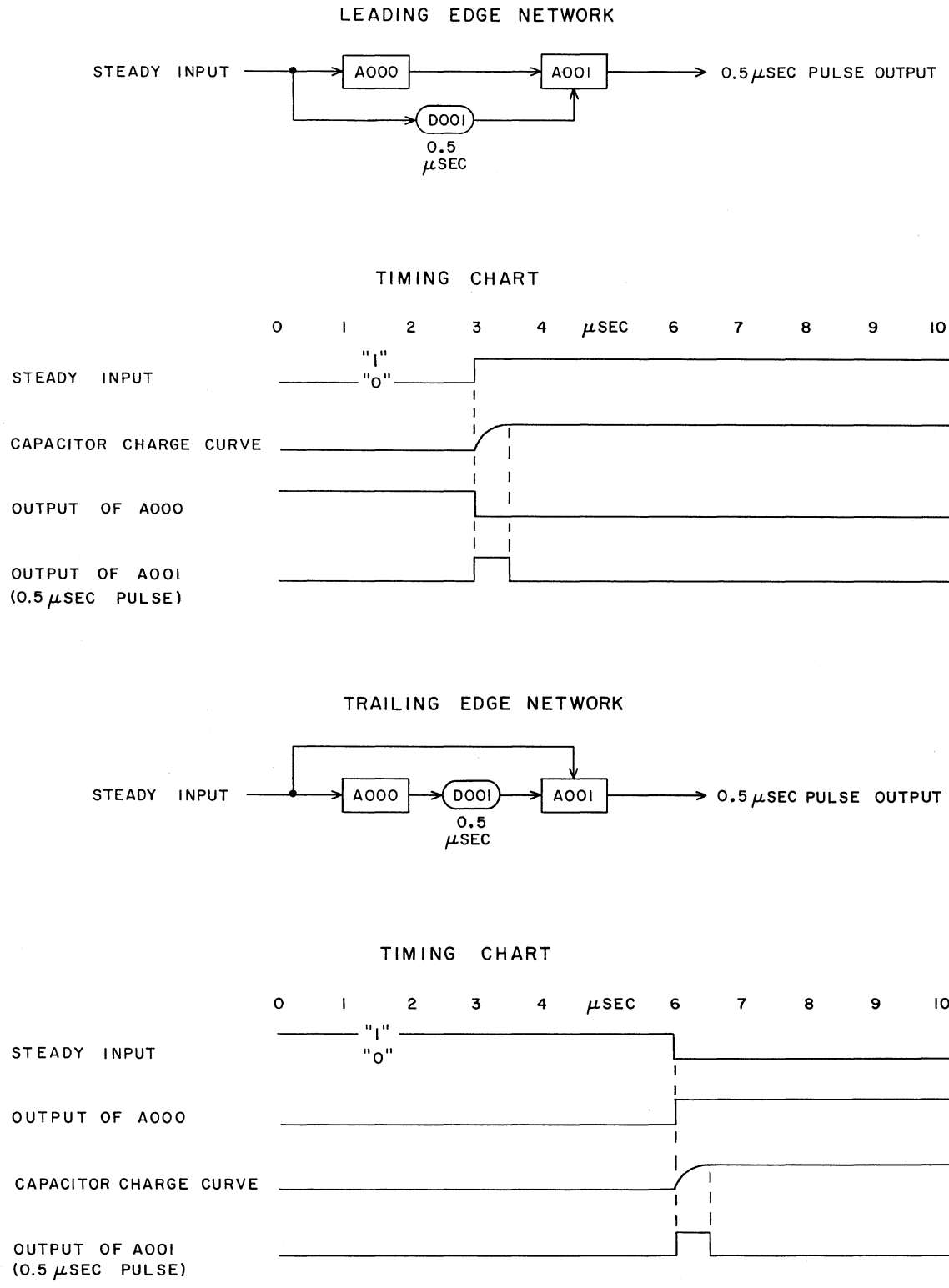


Figure 1-10. Pulse Forming Networks

TIMING CHAIN PULSE GENERATOR

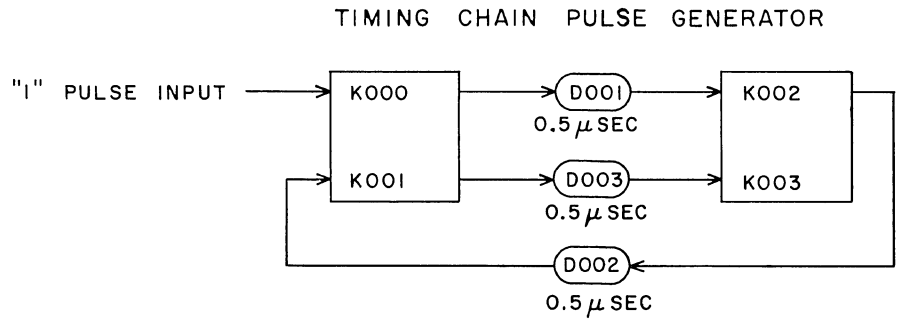
A convenient method of obtaining a series of sequential pulses using flip-flops and delays is shown in figure 1-11.

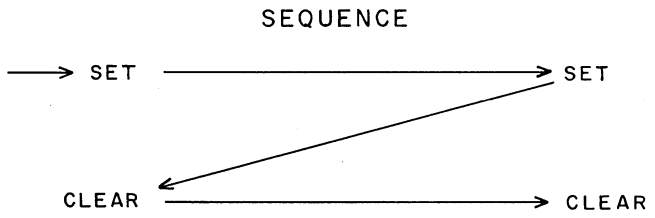
The two FFs exhibit four distinct sets of conditions at successive time intervals. Initially both are in the clear state. A "1" pulse input to K000 sets K000/001, so that K001 has a "1" output. After a brief delay, this signal sets K002/003. K003 then sends a "1" through a delay to K001, so that K000/001 is cleared. This causes K000 to send a "1" through the third delay to K003, so that K002/003 is also cleared and initial conditions prevail.

These four conditions and the times at which they occur are as follows:

	K000/K001	K002/K003
Time 0	Clear	Clear
Time 1	Set	Clear
Time 2	Set	Set
Time 3	Clear	Set
Time 0 (or 4)	Clear	Clear

The lengths of these time intervals are dependent upon the value of the capacitive delays. In the example shown, all of the times are 0.5 us. However, these may be varied in any manner desired.





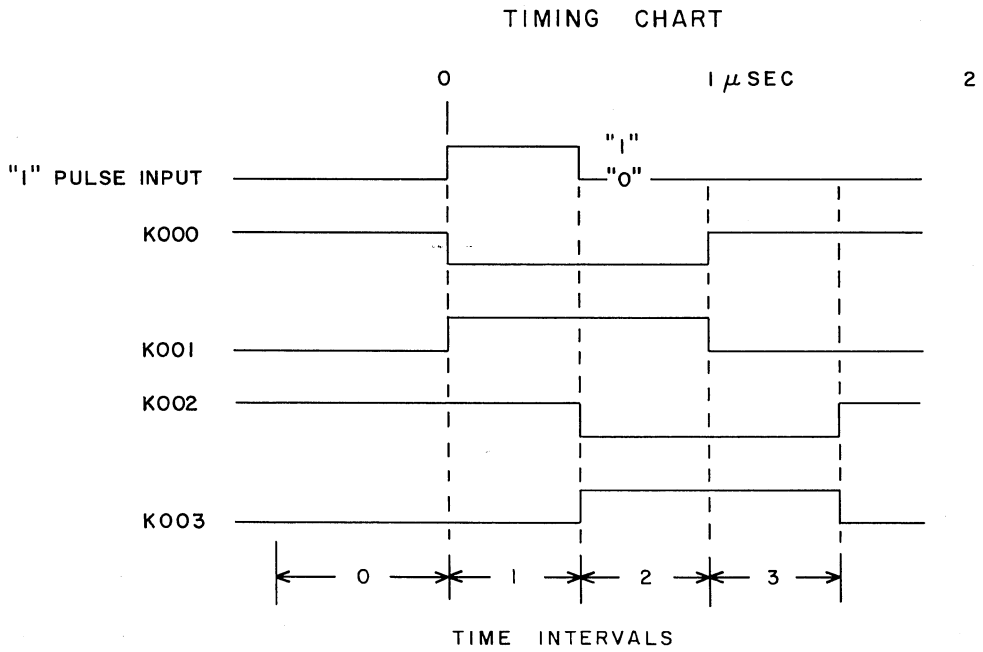


Figure 1-11. Timing Chain

CHAPTER 2. LOGIC CARDS

1604 Inverter Circuit and Ground Rules

3600 Inverter Circuit and Ground Rules

INVERTER CIRCUIT
1604 TYPE

The two signal levels in 1604 type logic are: -3.0v, logical "1", and -0.5v, logical "0". The single inverter inverts these signal levels: a -3.0v input becomes a -0.5v output, and vice versa.

In the standard inverter circuit shown, transistor Q01 is connected as an emitter-follower; Q02, as an amplifier. The collector circuits of the transistors have two feedback loops which prevent the transistors from being driven to cutoff or saturation. As a result, switching from one state to the other is accomplished in from 50 to 100 nanoseconds.

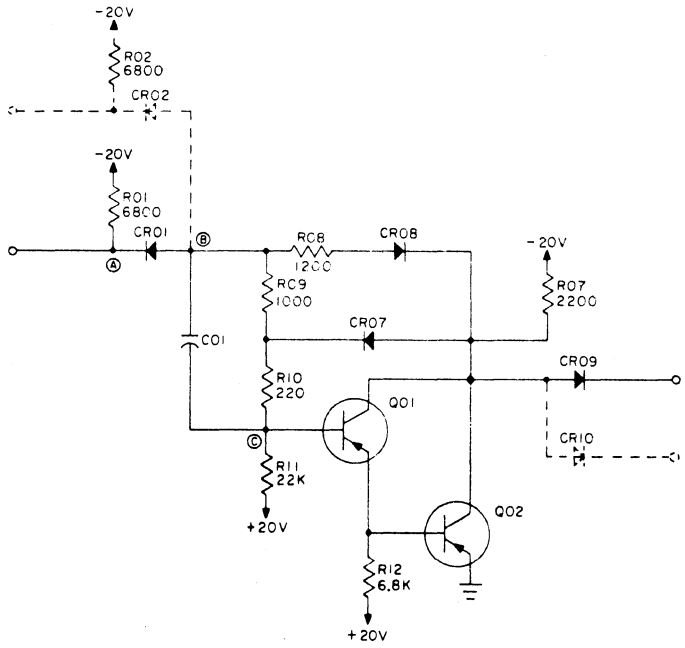
An input signal is applied via isolation diodes CR01 or CR02 to a voltage divider network composed of resistors R07, R08, R09, R10 and R11. An input signal of -0.5v (point A) results in -1.5v at point B and 0.8v at the base of Q01 (point C). CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

Transistors Q01 and Q02 each provide beta* current gains of approximately 100; loop gain of the two transistors is in the order of 10^4. The collector current of Q01 and Q02 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output line connected to CR10.

Diodes CR07 and CR08 form the feedback loops which prevent transistors Q01 and Q02 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors. When the transistors approach cutoff, their collectors approach -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R09 and R10. As a consequence the base of Q01 always is held at a sufficiently negative voltage to permit some minimum conduction of Q01 and thus Q02.

*The beta current gain is the ratio of collector current to base current.

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.



Schematic Diagram of 1604 Type Inverter Circuit

GROUND RULES

The following ground rules for usage of the basic 1604 inverter circuit are intended as guidelines in obtaining optimum performance. They are not intended to be excessively restrictive, because it is often found that a circuit will operate satisfactorily in a configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic and timing considerations, and are the responsibility of the designer.

1) A maximum of eight outputs may be taken from a single inverter.

2) An inverter will drive a maximum of six simultaneously gated AND loads.

3) The total number of inputs and outputs of a single inverter must not exceed 12.

4) The number of OR inputs to an inverter is limited to a maximum of six.

5) For high speed operation, the number of AND connections which can be made to a single OR input should be limited to four. If timing is not critical, the maximum number of AND connections can be increased to six.

6) All unused input pins must be grounded.

7) The minimum switching time for a mesa transistor inverter driving one load is approximately 30 nanoseconds. This will increase to about 75 nanoseconds as additional loads are added.

8) The minimum switching time for a drift transistor inverter driving one load is approximately 50 nanoseconds. This will increase to about 100 nanoseconds as additional loads are added.

9) An inverter will drive a load having 0.015 uf of capacitance. This may be increased at the discretion of the designer; however, long capacitive delays (greater than 10 usec) should be constructed using card type 97.

10) A capacitive delay should not be driven directly by a flip-flop, especially a flip-flop using mesa transistors, unless the discharge time of the capacitance is appreciably shorter than the duration of the input to the flip-flop.

3600 INVERTER CIRCUIT

NOTE

Type CA cards having OR inputs have been discontinued and should not be used for new design.

AVAILABLE CARD TYPES

Three series of printed circuit cards have been produced during development of the 3600 family of computing systems. The initial prototype series was designated Type C. Later, after the design had been approved, the physical size of the phenolic board was increased slightly and the cards went into production as the Type CA series. Except for the addition of more test points, there was no change in the circuit.

As shown in figure 1, logical OR inputs on Type CA inverters consist of only the OR diode without any connection to -20 volts. This was intended to eliminate the requirement for grounding unused OR inputs, since an open OR input will not drive the circuit output to "0". In actual practice, however, it was found that the distributed capacitance of large numbers of open OR inputs could result in a delay in switching time. In addition, since OR inputs did not provide the clamping action of AND inputs, the circuits tended to respond excessively to transients on the signal line. These conditions brought about the development of two new series of cards, called Type HA and Type K. Both of these have the same basic inverter circuit as the Type CA inverter, but the inputs are modified. The logical AND and OR input configuration of a Type K card is identical to the corresponding Type CA number, but all OR's have been converted to single-way AND's including the feedback of flip-flops. Cards in the Type HA series are built with a limited number of inputs, e. g., an HA 07 card contains two inverters with each having only one single-way AND input. Type CA cards have since been discontinued and should not be used in new design.

BASIC INVERTER CIRCUIT

The basic inverter circuit consists of two transistor stages, as shown in figures 1 and 2. Transistor Q01 is a grounded emitter stage which supplies AND current to the load, and transistor Q02 is an emitter follower stage which supplies OR current to the load.

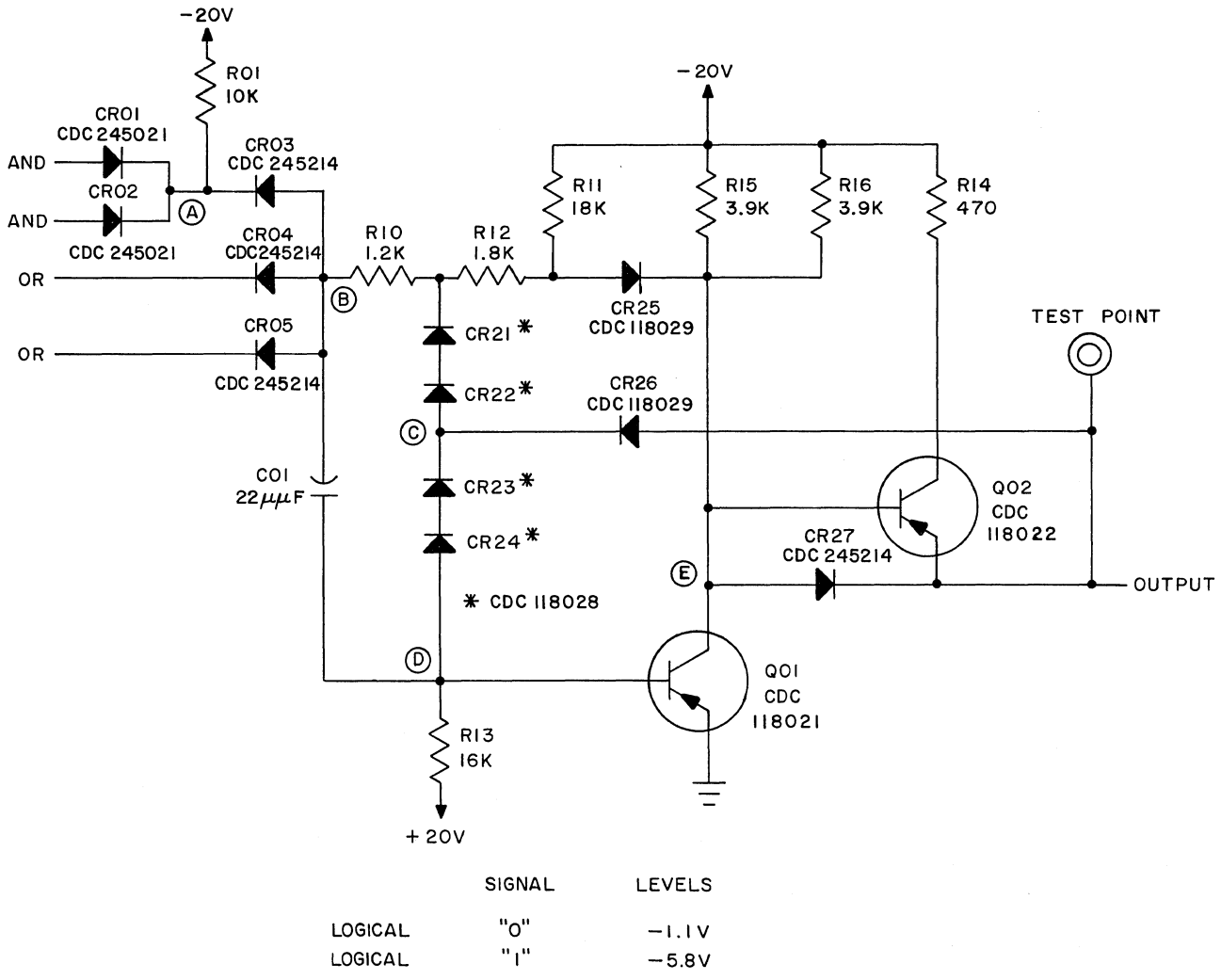


Figure 1. Schematic Diagram Type CA Inverter Circuit
(Not to be used for new design)

The input to the circuit consists of two levels of diode logic. The maximum number of inputs is limited by the number of available input pins on a circuit card; however, the maximum number of individual inputs to any single AND cannot exceed 6.

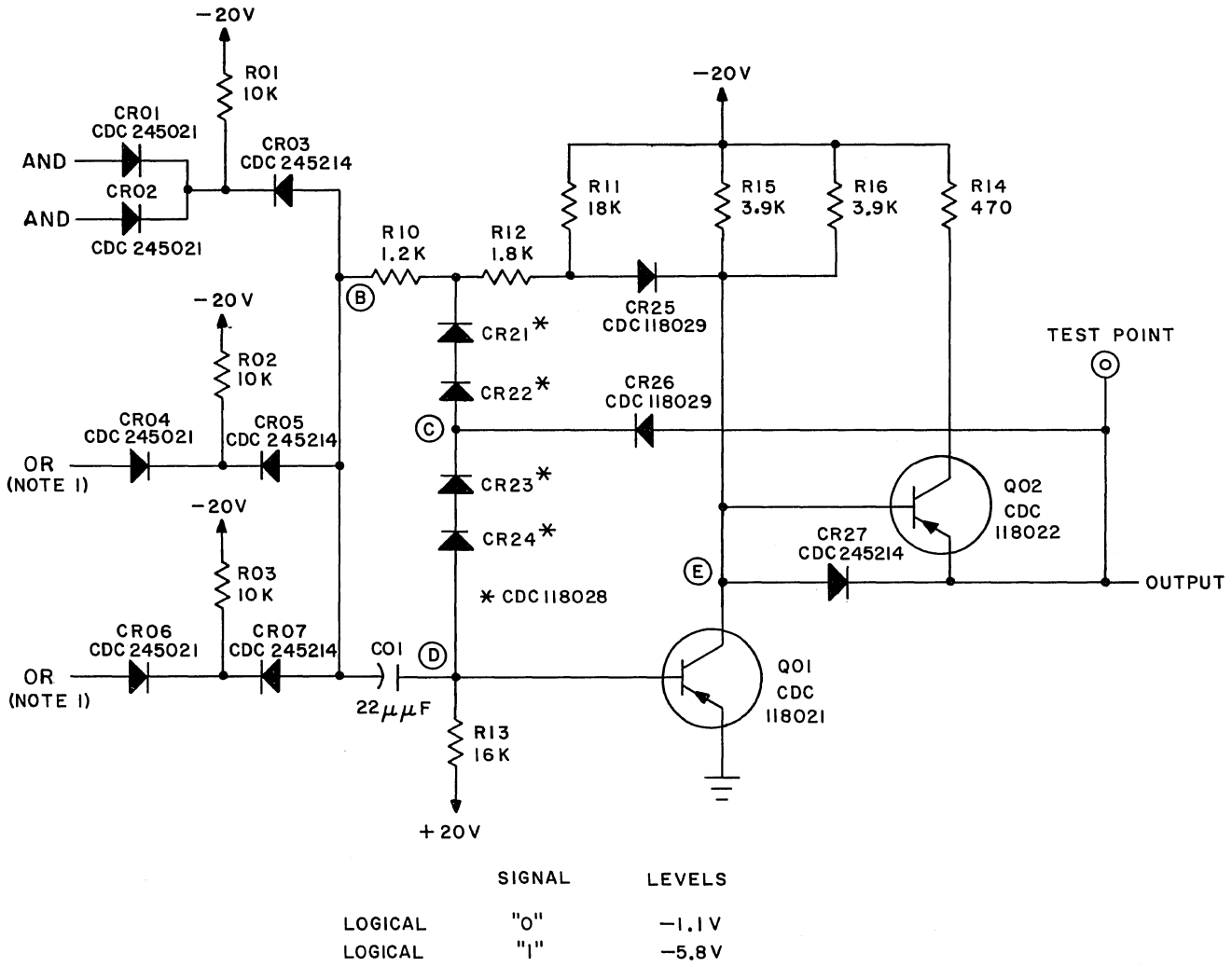


Figure 2. Schematic Diagram of Type K and Type HA Inverter Circuit

The input logic diodes are medium speed germanium devices. Initially, Hughes HD2969 diodes were used, and a set of graphs is included in this report which show the comparative recovery time of these diodes.

The response of an AND input is a function of the time constant of the AND resistor R01, shunt circuit capacitance at point (A) and the recovery speed of the input diodes. Because additional AND diode inputs increase the shunt capacitance, it is necessary to decrease the size of the AND resistor a proportionate amount as the number of inputs to the AND increases beyond 3.

The transition speed of the AND circuit varies inversely with the recovery speed of the AND diodes. Slow diodes allow additional recovery current to be drawn. This, in effect, allows a larger turn-on current in the first transistor stage.

The input resistor and diode network of transistor Q01 establishes the clamping levels for the output signal. This network also provides feedback to the base of Q01 which stabilizes the two quiescent values of the output voltage.

The input network establishes an input threshold level of approximately -3 volts. Thus, the input signal must be more negative than -3 volts before transistor Q01 turn-on current is allowed to flow. Silicon forward drop diodes CR21 through CR24 are used in the input network to obtain a constant d-c level for signal threshold. These diodes also have a low dynamic impedance which causes little attenuation of the input signal current.

The 22 uuf speed-up capacitor C01 on the input of the first stage bypasses the 1.2 k resistor R10 and the diode network during the initial rise or fall of the input signal. This provides additional drive to the base of Q01 during the input signal transition, thereby speeding the switching of this stage.

Feedback is accomplished through two high speed silicon diodes, CR25 and CR26, which have very low stored charge characteristics. If these diodes were capable of storing excessive charge, there would be additional delay in switching. By using diodes with very low storage, the initial switching speed is greatly improved.

When the grounded emitter stage Q01 is turned on, collector current flows out of the circuit through the series diode CR27. In this state, Q01 can supply current to 8 AND loads. Transistor Q01 is clamped out of saturation by the silicon feedback diode CR26, and the output voltage settles at a nominal value of -1.1 volt. The voltage drop across diode CR27 insures a back bias being applied to the base-emitter junction of Q02, thereby keeping this stage turned off.

When Q01 turns off, the collector voltage starts to rise toward -20 volts. Since the voltage across the load cannot change as quickly as the collector voltage of Q01, the series output diode CR27 is back biased and the output emitter follower stage Q02 is turned on.

The turn-on current is applied to the base of Q02 at the rate at which Q01 turns off. The turn-on current is the current that is drawn through the first stage collector resistors R15 and R16. This current is available to turn on the output stage only as fast as it is turned off in the first stage.

Transistor Q02 in the on state proceeds to drive the output voltage negative. At about -5.8 volts, the output is fed back to the input of the first stage by diode CR25 to start the clamping action. Since this process has delay associated with it, the output signal overshoots the -5.8 volt mark and may carry as far as -8 volts. The circuit then settles the voltage back to the -5.8 volt level. In this state, transistor Q02 provides a low impedance path to the -20 volt supply.

GROUND RULES

(Effective November 21, 1963)

The following ground rules for usage of the basic 3600 inverter circuit are the result of tests performed by the Special Projects Department, Government Systems Division of Control Data Corporation. Inquiries concerning these ground rules should be addressed to the above department.

The ground rules are intended as guidelines in obtaining optimum circuit performance. They should not be considered as being excessively restrictive, because it is often found that a circuit will operate satisfactorily in a less than optimum configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic considerations, and are the responsibility of the designer.

Definition: Minimum Usage Inverter

The minimum usage inverter referred to in the following rules is defined to be an inverter driving one load and having one input. The inverter which drives the minimum usage inverter must drive no other loads. All wire lengths are kept as short as possible, voltages are adjusted to proper levels, and temperatures are allowed to stabilize.

LOADING

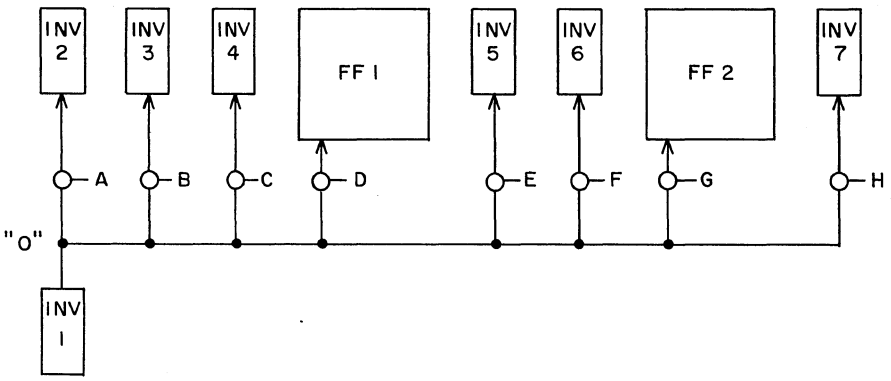
Any single input to a recipient inverter, regardless of whether it is a part of a 1, 2, 3, 4, 5, or 6 input AND or an OR input, is considered to be one load.

1) An inverter may simultaneously drive eight AND loads, eight OR loads, or any combination up to eight loads total.

2) A flip-flop or a control delay may drive only seven loads, because it is required to provide its own feedback which constitutes one load.

Exception to Rule

Inverter 1 is normally capable of maintaining a logical "0" on eight input AND gates. However, there is one exception when all the points, A through H, are driven to a "1" simultaneously. The current demand on inverter 1 is of such magnitude that the "0" condition is lost momentarily, allowing runt pulses to occasionally set a flip-flop or be amplified through an inverter. This condition can be avoided by limiting the inverter to a total of six loads as opposed to the usual eight loads.



UNUSED INPUTS

3) In case an entire AND input group is unused, at least one of the inputs must be grounded.

4) All unused OR inputs must be grounded, if using type C or CA cards.

5) All unused single-way AND inputs must be grounded.

NOISE SUPPRESSION

6) When a noise condition cannot be alleviated by the following suggestions or if an interconnecting lead is over 80 inches in length use logic level clamp card CA02.

   a) Maintain wire runs as short as possible.

   b) When possible, drive heavily loaded inverters from a lightly loaded source.

   c) When possible, use cards with 1, 2, 3, or 4 input AND gates as opposed to 5 and 6 input AND gates.

   d) Avoid using OR inputs unless the OR is a single-way AND.

7) All drive lines from H--- terms to N---, V---, and Y--- terms must be clamped, regardless of length, and must enter the recipient N---, V---, and Y--- terms through AND inputs.

8) N---, V---, and Y--- terms having a clock signal on an AND input must use one of the special card types numbered K72, CA73, K74, K92, K93, and HA06.

The clock input must be on the following pins:

Card Type	Inverter A	Inverter B
CA72	5 or 6	13 or 14
K72	2, 5, or 6	10, 13, or 14
CA73	2 or 3	10 or 11
CA74	5 or 6	13 or 14
K74	5 or 6	13 or 14
K92	2	
K93	2 or 3	
HA06	5 or 6	13 or 14

Exception to Rule

a) A clock input must come in on an AND; if the listed pins do not lend themselves to conditions, another AND input can be used.

b) The restriction of using only the above card types may be violated in applications where the logic circuits are heavily loaded.

PROPAGATION DELAYS AND TIMING ALLOWANCES

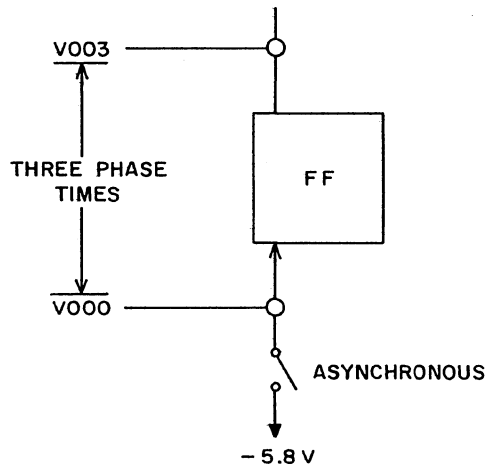
9)	Allow 17×10^{-9} seconds	To switch from "0" to "1" any minimum usage inverter using any type input.
10)	Allow 11×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverter using a 1, 2, 3, or 4-way AND input.
11)	Allow 8×10^{-9} seconds	To switch from "1" to "0" minimum usage inverters where equal numbers of AND and OR inputs are involved in a string of inverters.
12)	Allow 6×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverters using a 5 or 6-way AND input.
13)	Allow 5×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverters using OR inputs.
14)	Allow 2×10^{-9} seconds per foot	For propagation time from point to point through all lengths of wire.
15)	Add 1×10^{-9} seconds	To each inverter switching time for each additional load beyond one.
16)	Add 2×10^{-9} seconds	To each inverter switching time for each foot of wire attached to the output.

17) The transition times from -1.1v "0" to -5.8v "1" and from -5.8v "1" to -1.1v "0" range from 20×10^{-9} to 50×10^{-9} seconds and 15×10^{-9} to 35×10^{-9} seconds, respectively. These times are highly influenced by loading effects.

18) If two inverters are cross coupled to perform as a flip-flop and the load on either side of the flip-flop is two loads or less, the cross-coupling must come into AND inputs.

19) The length of cross-coupling leads of inverters to be used as a flip-flop must not exceed six inches.

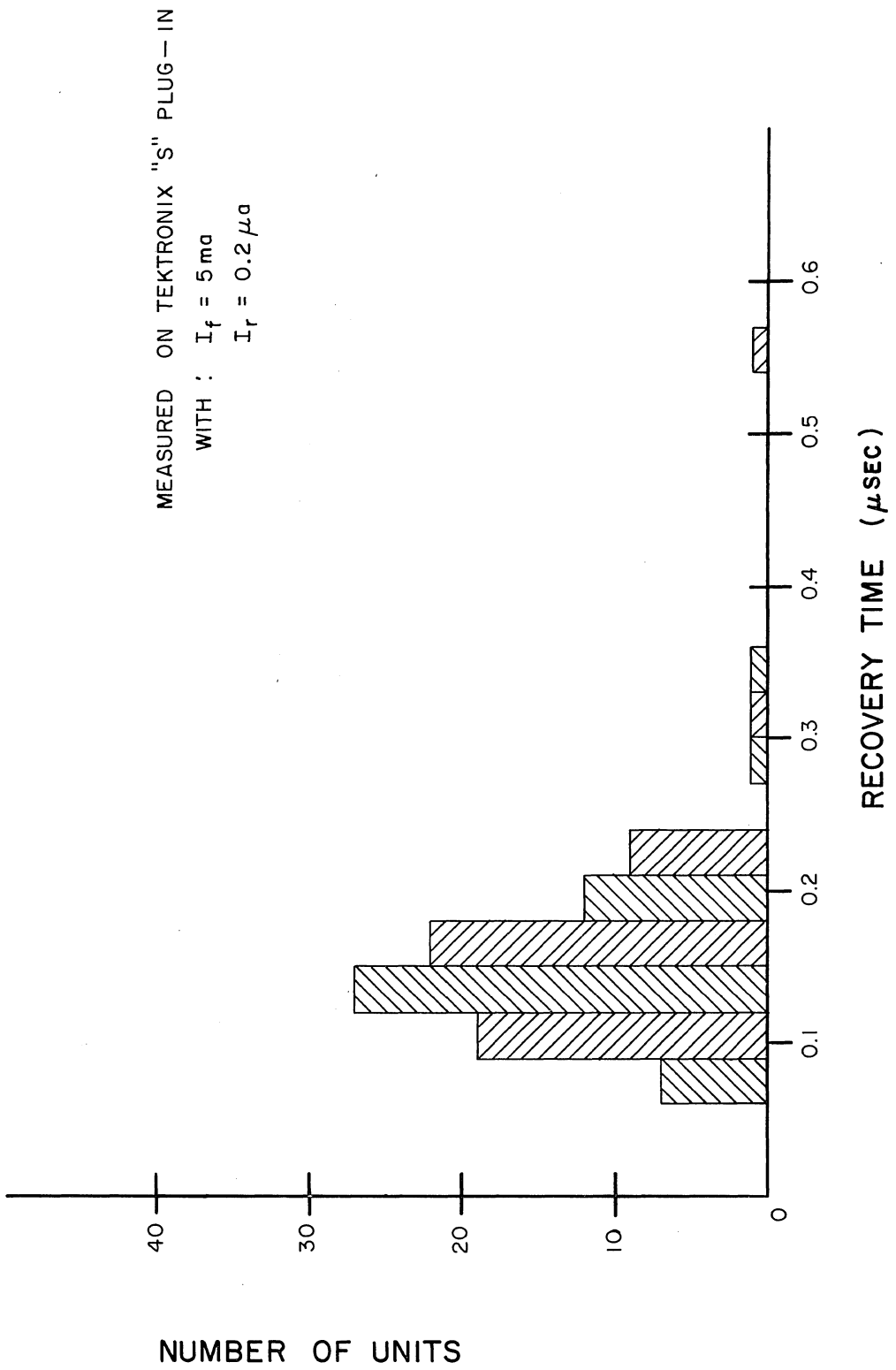
20) In applications where an asynchronous signal forms an AND gate with an N---, V---, or Y--- term, allow a minimum of three clock-phase times (187.5×10^{-9} sec) before probing the flip-flop output for reliable information.



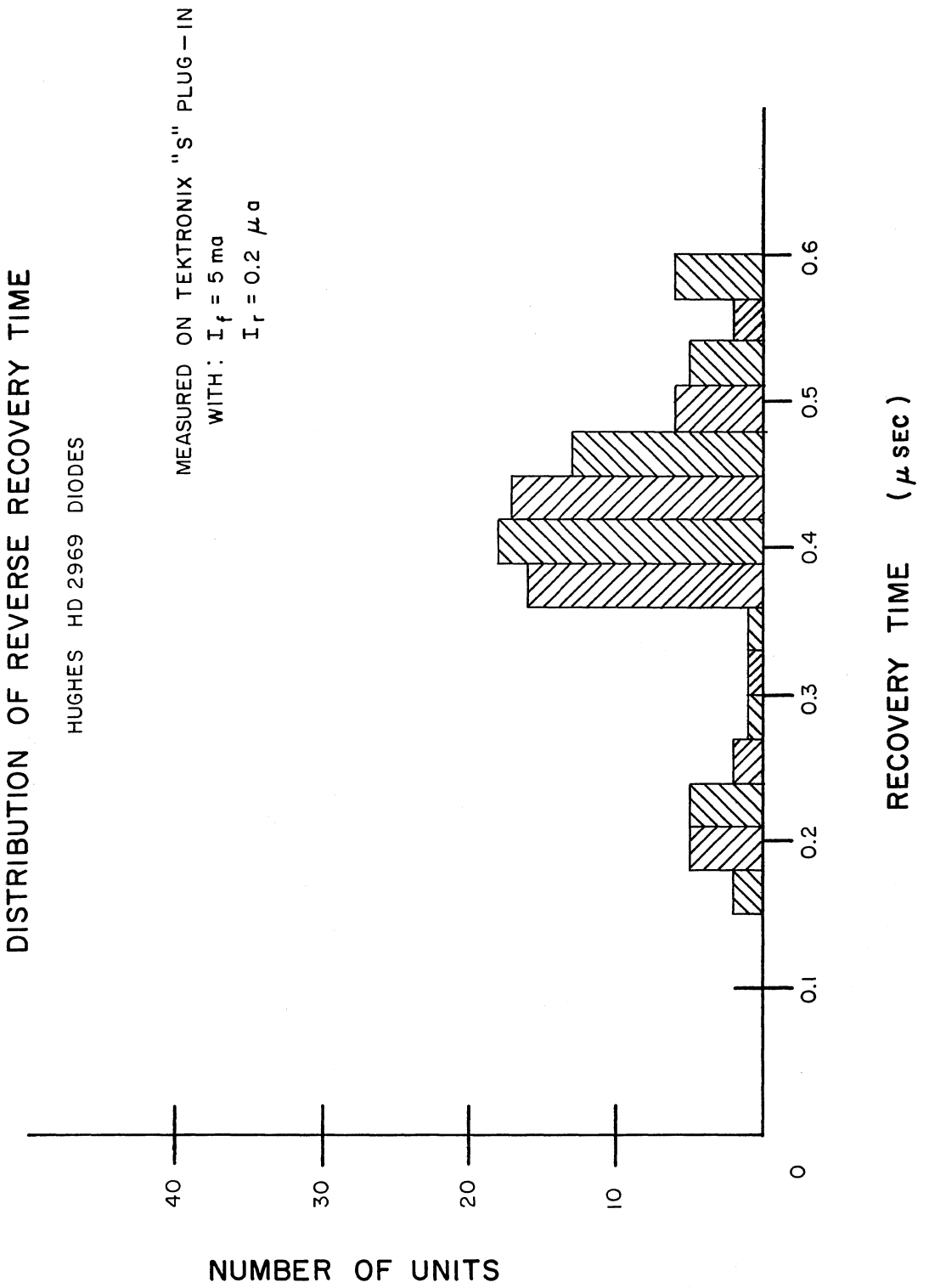
TEST RESULTS

The following pages contain graphs showing the comparative recovery time of the logic diodes and the margins over which the +20v and -20v supplies may vary.

The voltage margin tests were made by varying the supply voltage of an entire chassis until failure occurred. The final version of the inverter circuit was tested in a chassis composed of 1170 cards which contained 2046 inverters.



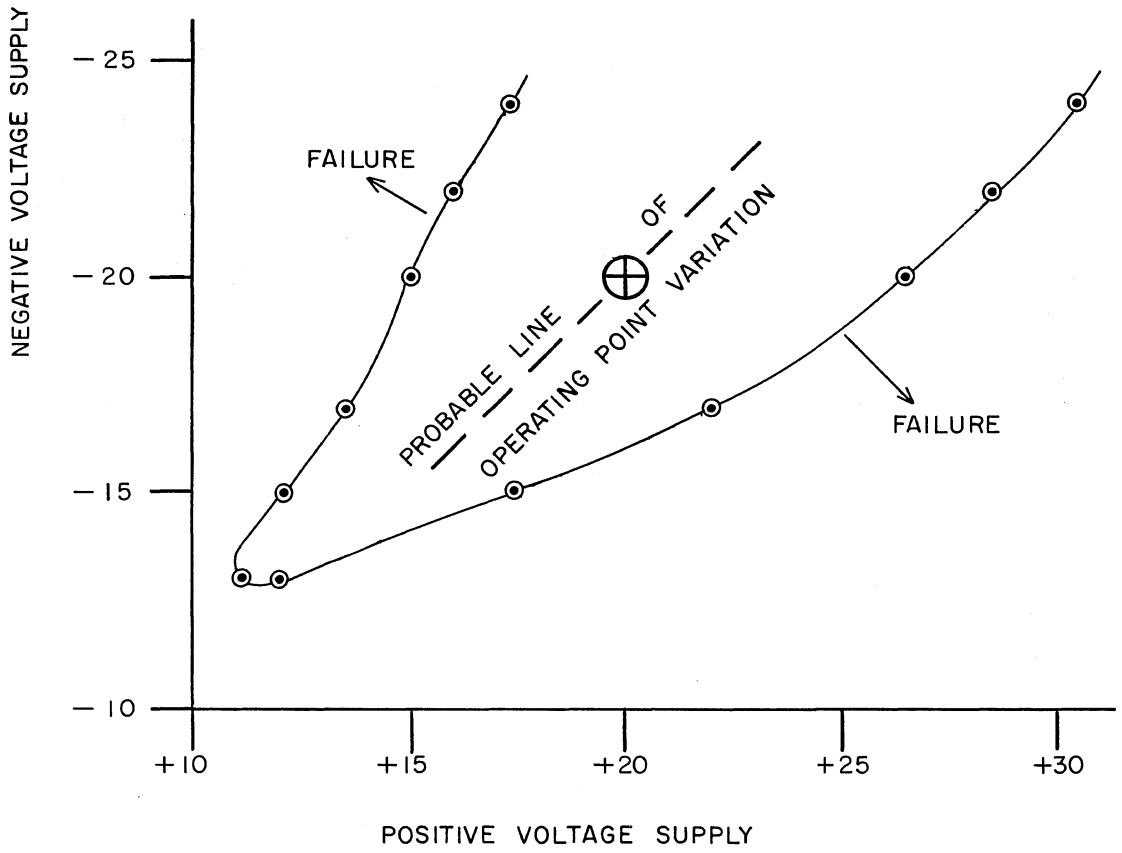
Clevite CGD 899 Diodes
Distribution of Reverse Recovery Time



Hughes HD 2969 Diodes
Distribution of Reverse Recovery Time

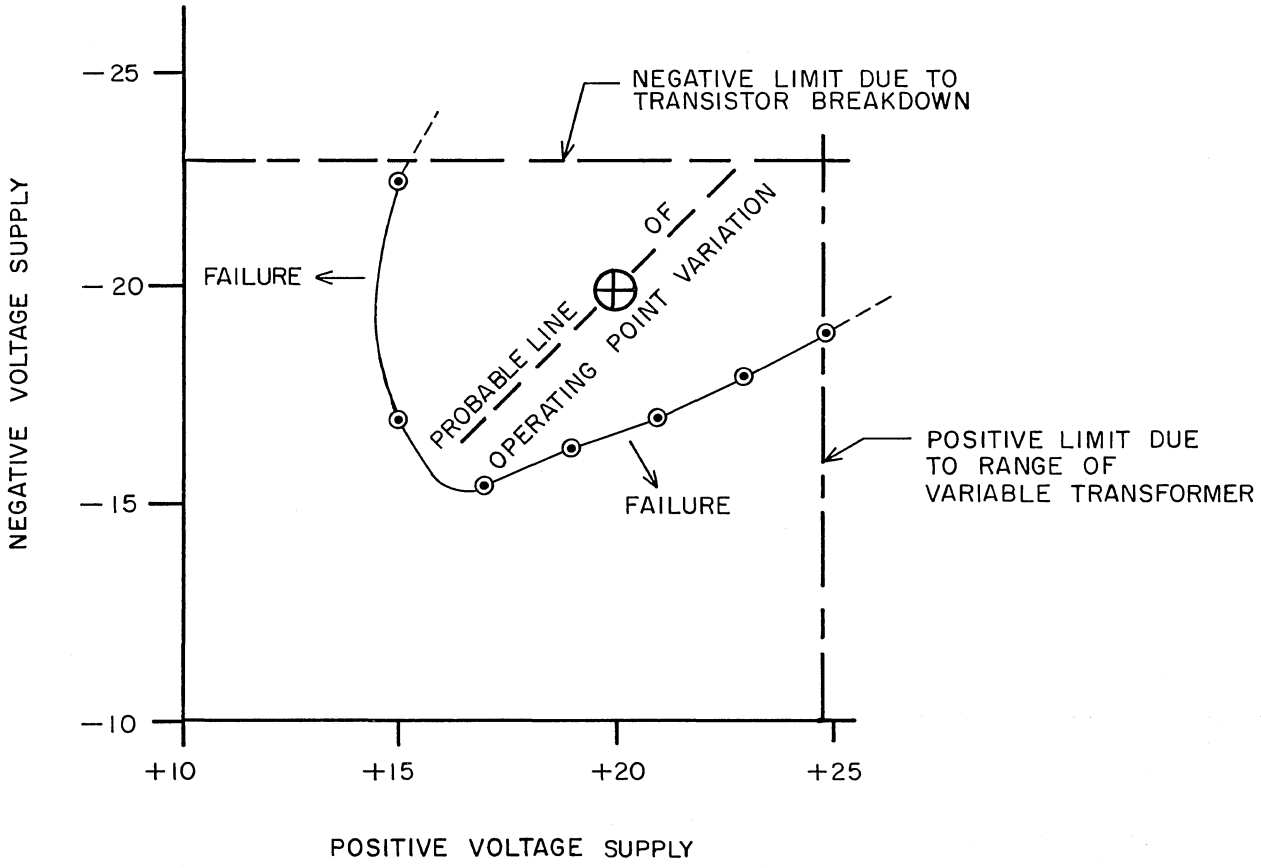
VOLTAGE MARGINS

8 mc "P" COUNTER CONTAINING 43 CARDS
LOGIC DIODES HD 1804



Voltage Margins

TEST CHASSIS CONTAINING 1170 CARDS (2046 INVERTERS)
FINAL VERSION OF CIRCUIT AS SHOWN IN 2-3600 INV-2



Voltage Margins

CHAPTER 3. STORAGE CARDS

Drive Generator	51, 51A
Diverter	52, 52A
Selector	53
Current Source	54, 74
Inhibit Generator	55, 55A, 58, 58A, 59, 59A
Sense Amplifier	56
Sense Amplifier	57
Even Plane Inhibit Driver	C00
Line Driver	C03
Odd Plane Inhibit Driver	C04
Gate	C05
Sense Amplifier	C06
Inhibit Compensator	C09
Drive Line Transformer	C10
I/O Sense Amplifier	C86
I/O Memory Driver	C87
I/O Memory Diverter	C88
I/O Emitter Follower	C90
Digit Driver	H14
Digit Compensator	H15
Sense Amplifier	H16
Sense Amplifier	H18
Memory Driver	P51
Memory Diverter	P52
Sense Amplifier	P56

DRIVE GENERATOR
Card Types 51 and 51A

The driver generator (page 3-51-2) develops the R/W current which is applied to the memory drive lines selected (designated H and V in the 1604 computer). Two identical channels feed opposite ends of the primary winding of transformer T01. Each channel consists of transistor Q01, connected as an emitter-follower, and transistors Q02 and Q03, connected in parallel as amplifiers. The input signal is an AND combination of two selector (card type 53) outputs. A -1v input results in approximately 0v at the base of Q01. The emitter of Q01 is clamped to ground by CR03, so neither Q02 nor Q03 conducts. Consequently, no current flows in the primary of T01.

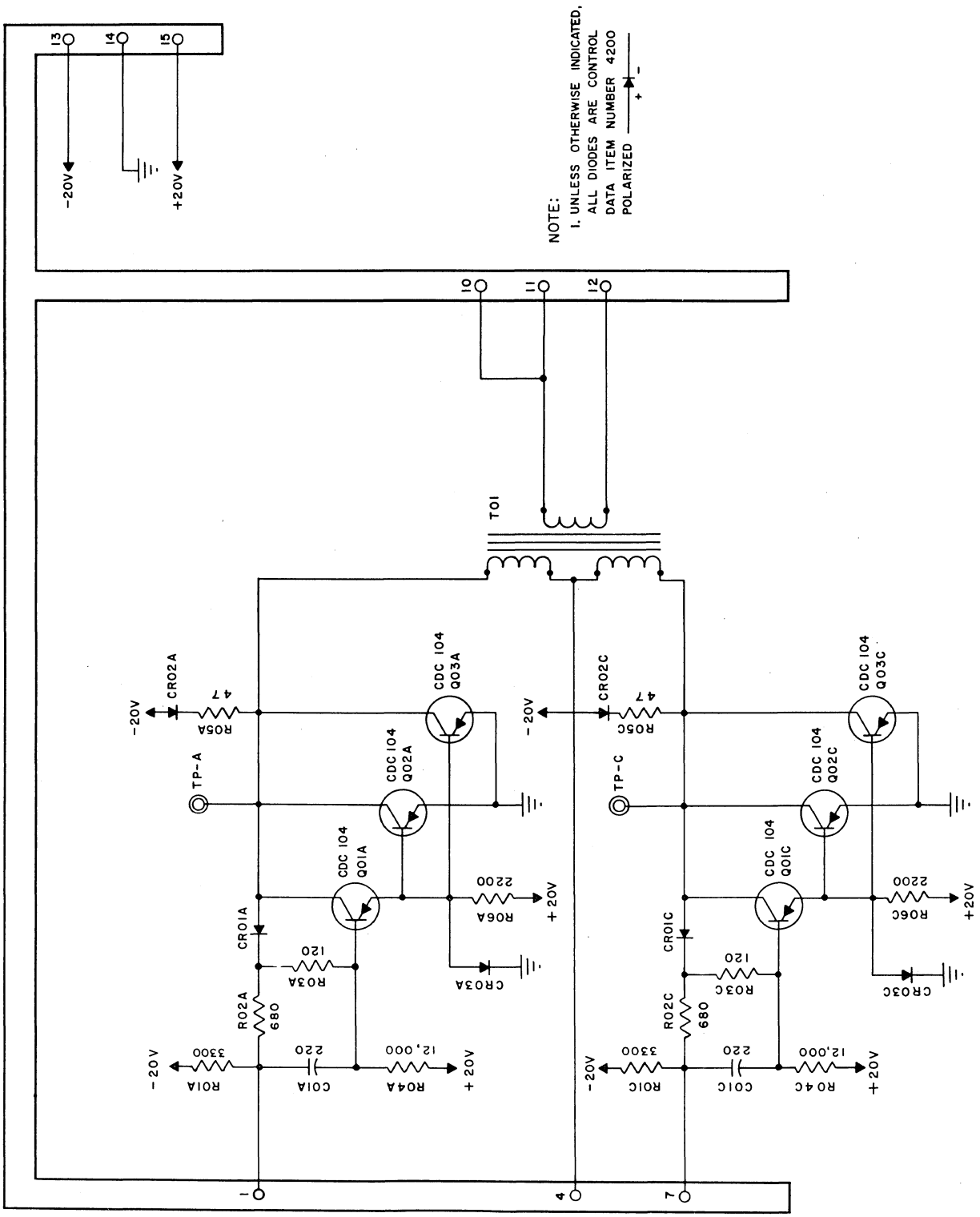
Note: Transistor Q03 is not used on card type 51A.

A -12v input signal causes Q01 to conduct; however, the conduction is held below saturation by feedback diode CR01. The negative voltage developed across R06 is applied to the bases of Q02 and Q03, causing these transistors to conduct. Current flows from the current sources through the emitters of Q02 and Q03 to the collectors, through the primary of T01, to the current sources. The current pulse from the secondary of T01, amplified by the step-down action of T01, is applied to the drive line of the memory plane assembly. It then flows through the selected diverter and back to the secondary of T01.

The polarity of the output current from T01 is determined by the direction of the current flow in the primary. The direction of current flow, in turn, is determined by the selected channel. For example, if channel A receives a -12v input, a read pulse is generated; a channel B input generates a write pulse. Acceptable switching times are as follows:

Negative to positive $\leq$ 0.15usec

Positive to negative $\leq$ 0.2 usec



Drive Generator 51

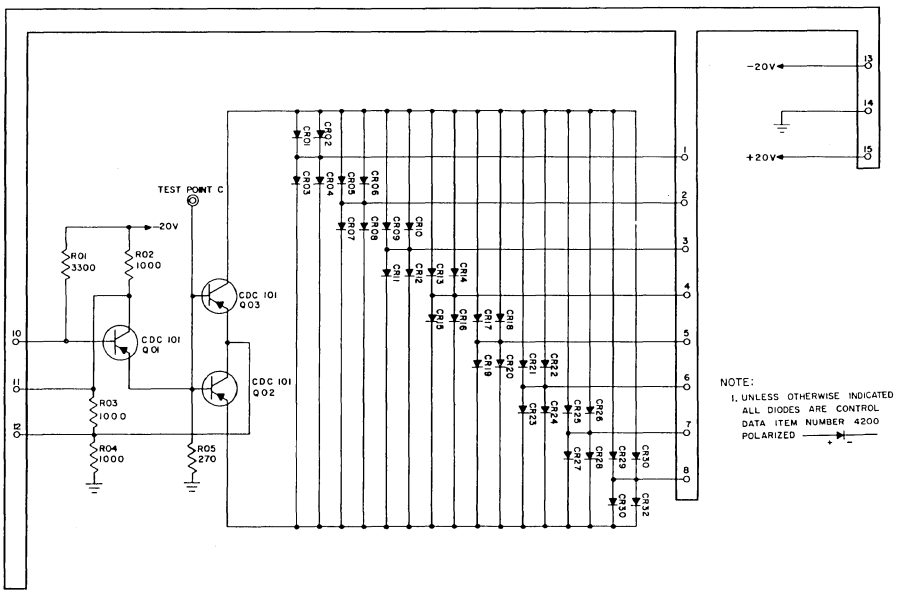
DIVERTER

Card Types 52 and 52A

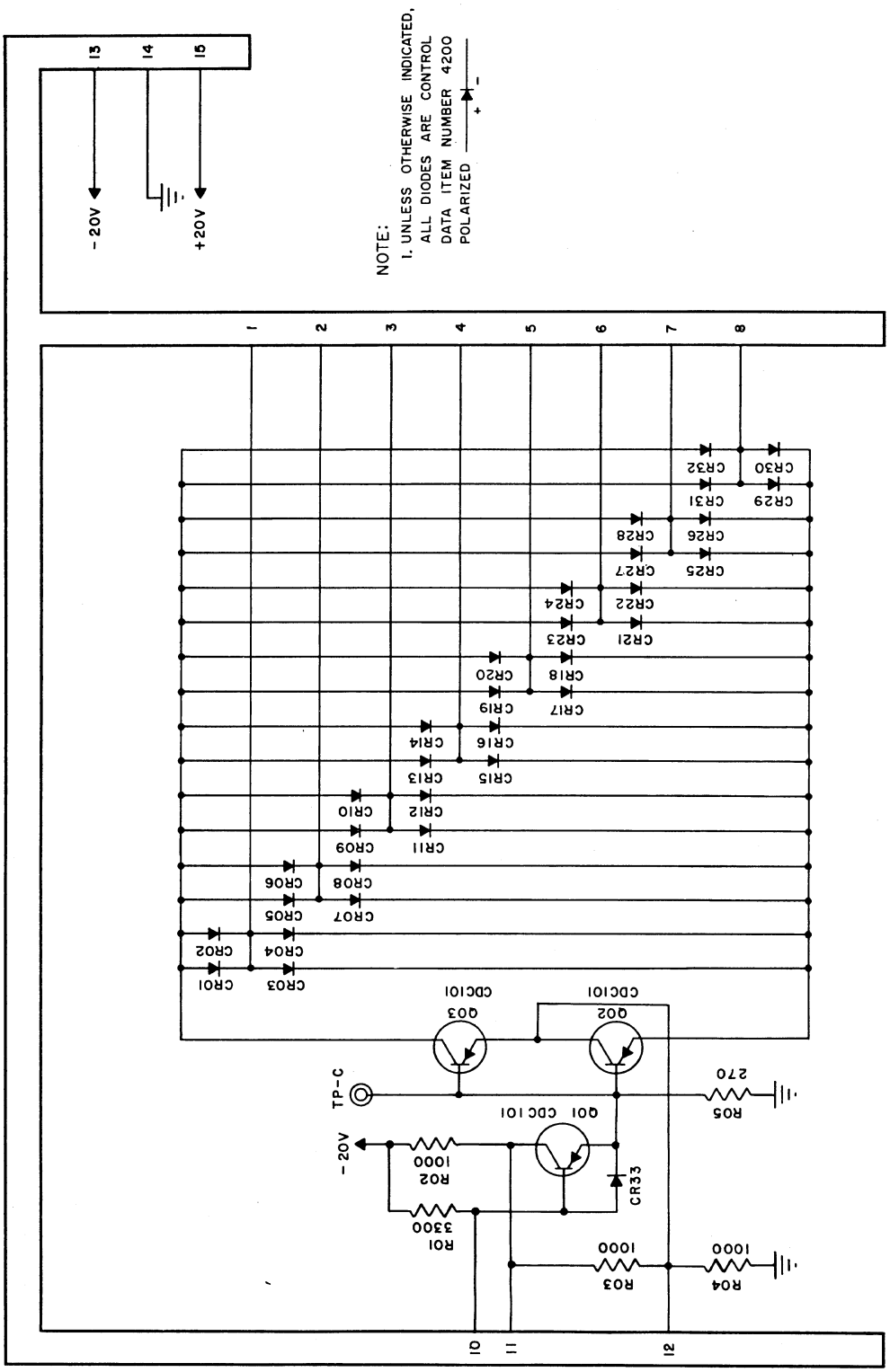
DIVERTER (Type 52)

The diverter circuit serves as an electronic switch in series with a drive line of the memory plane assembly. Transistor Q01 is connected as an emitter follower, and transistors Q02 and Q03 as switches. A -3v input causes Q01 to conduct; the negative signal from Q01 enables Q02 and Q03. One or the other transistor passes the current pulse on the drive line to which the diverter is connected.

A positive pulse passes one of the pairs of diodes CR03/CR04, CR07/CR08, CR11/CR12, etc., depending upon the driver selection, and passes Q02. A negative pulse passes one of the pairs of diodes CR01/CR02, CR05/CR06, etc., and passes Q03. In either case, the current pulse is returned to the R/W driver. The bleeder networks of all diverters are connected in parallel via terminals 11 and 12 to equalize the current flow through the bleeders and reduce heating.



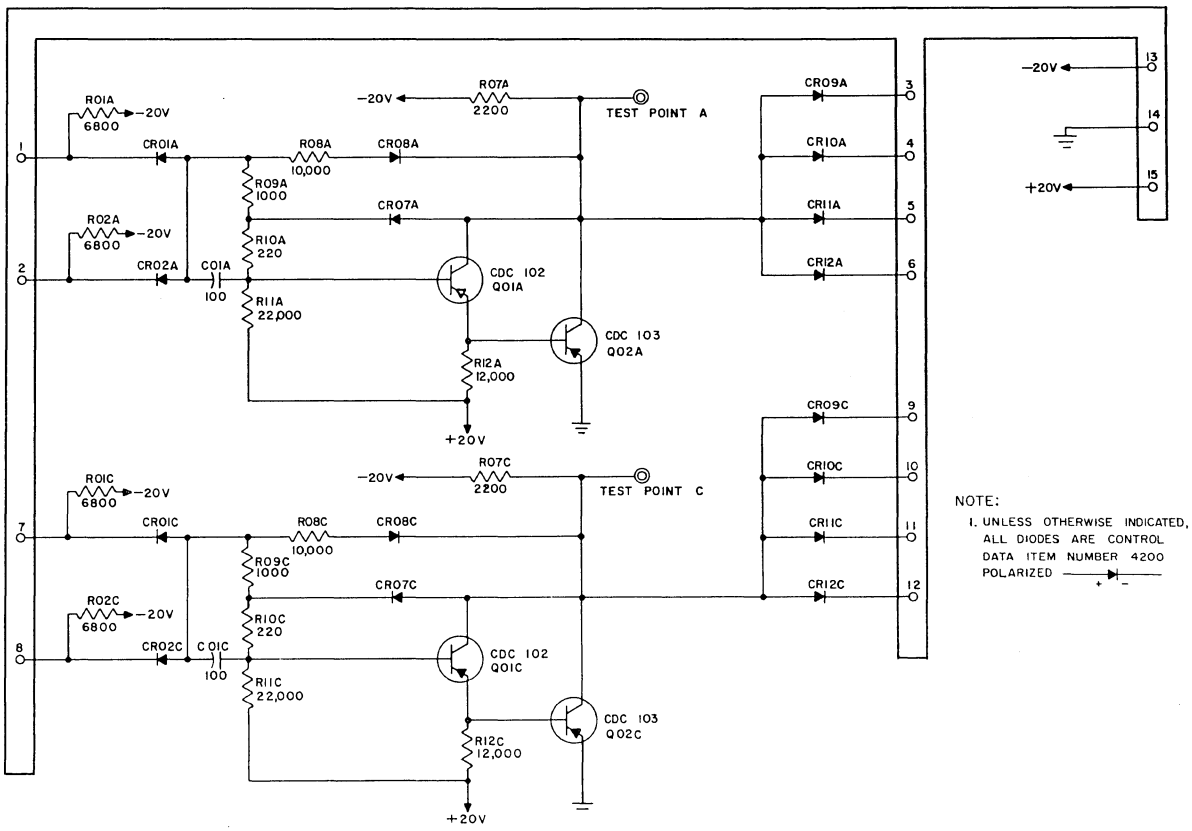
Diverter 52



Diverter 52A

SELECTOR
Card Type 53

Each selector card consists of two identical circuits designed to feed a drive generator circuit. A selector circuit is similar to the 1604 type inverter except that the resistance results in output signal levels of -1v and -12v. Each selector circuit has two input diodes CR01/CR02 and four output diodes CR09/CR10/CR11/CR12.



Selector 53

CURRENT SOURCE
Card Types 54 and 74

A current source card consists of banks of parallel resistors, each of which connects an output pin and the -20v supply. The function of this card is to provide the resistances needed to hold memory drive and inhibit currents to the desired amplitude.

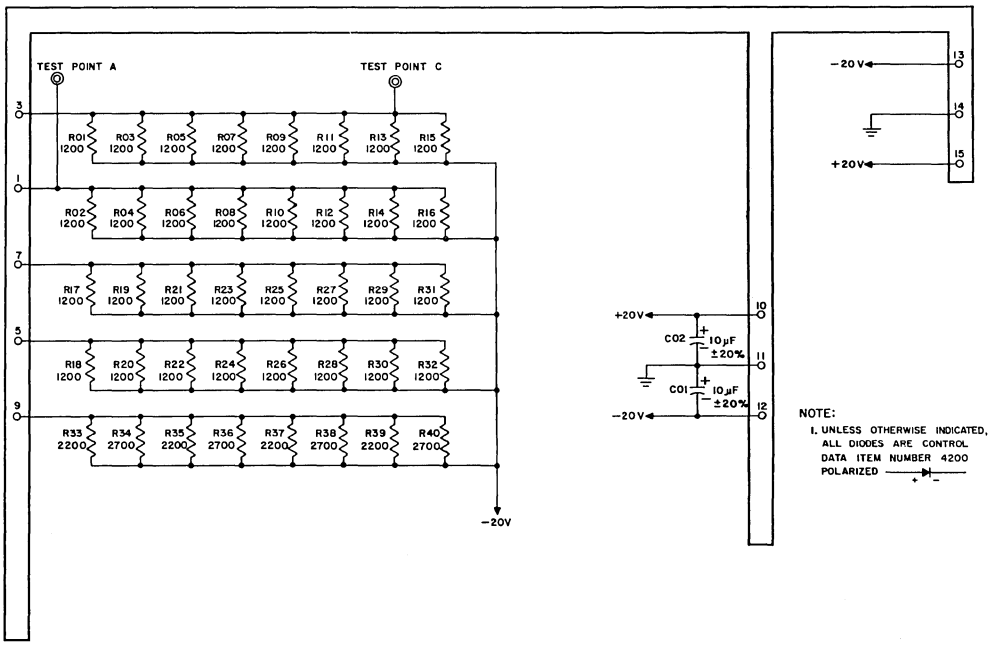
The available resistances are as follows:

Card Type 54

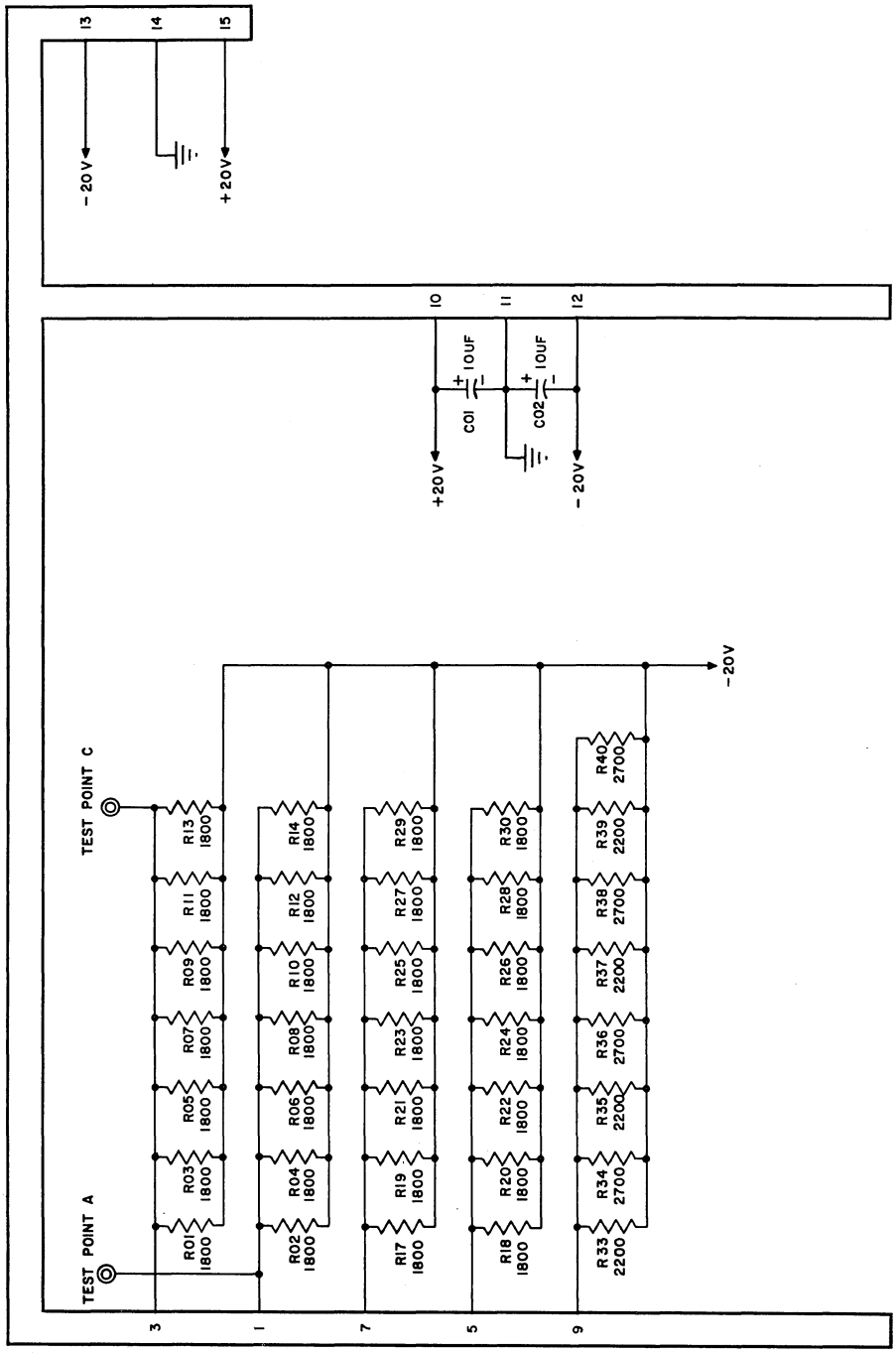
pins 1, 3, 5, 7	150 ohms
pin 9	303 ohms

Card Type 74

pins 1, 3, 5, 7	257 ohms
pin 9	303 ohms



Current Source 54



Tape Current Source 74

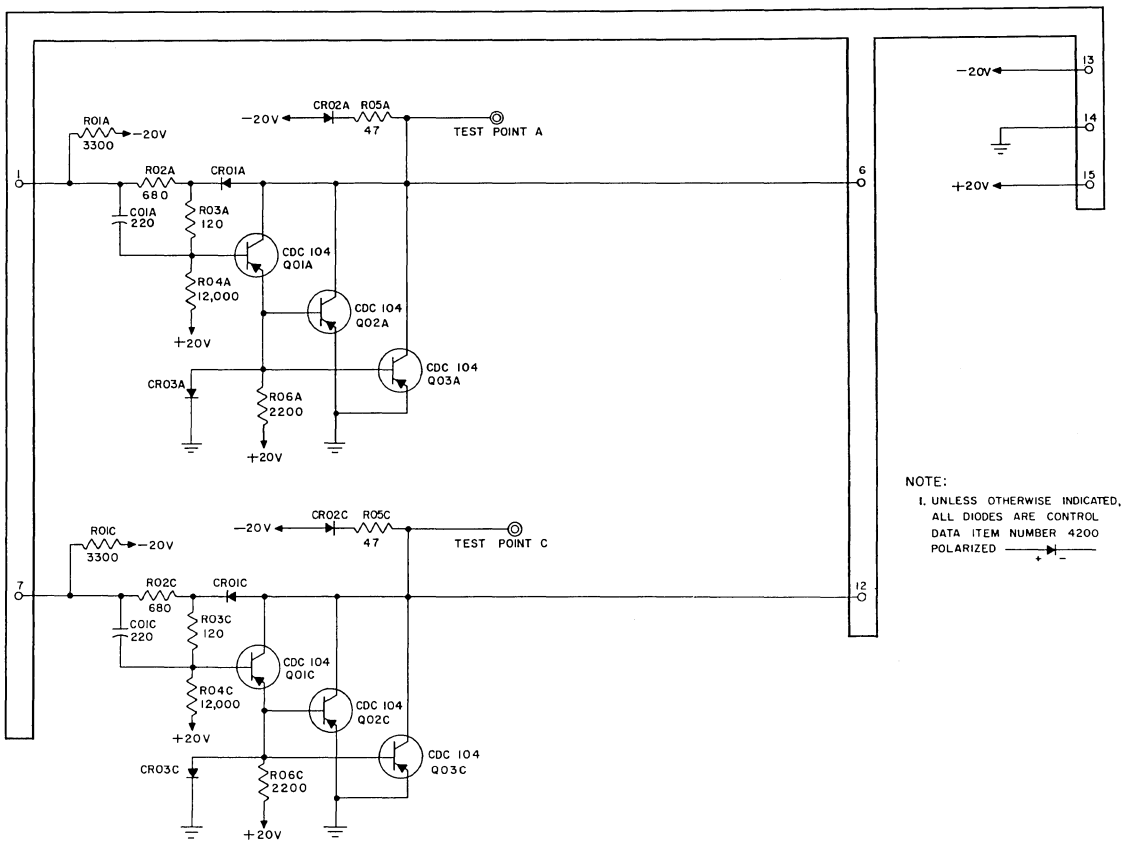
INHIBIT GENERATOR

Card Types 55, 55A, 58, 58A, 59, 59A

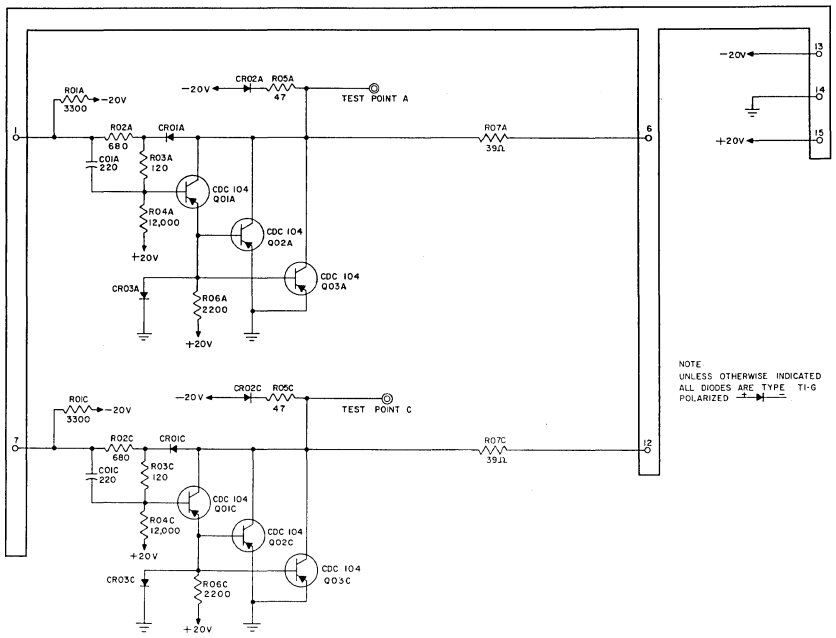
Note: Transistor Q03 is not used on card types 55A, 58A, and 59A.

Each inhibit generator card has two generator circuits which are similar to the type 51 drive generator channels except for the absence of an output transformer. The output of each channel is independently connected to a terminal of the card.

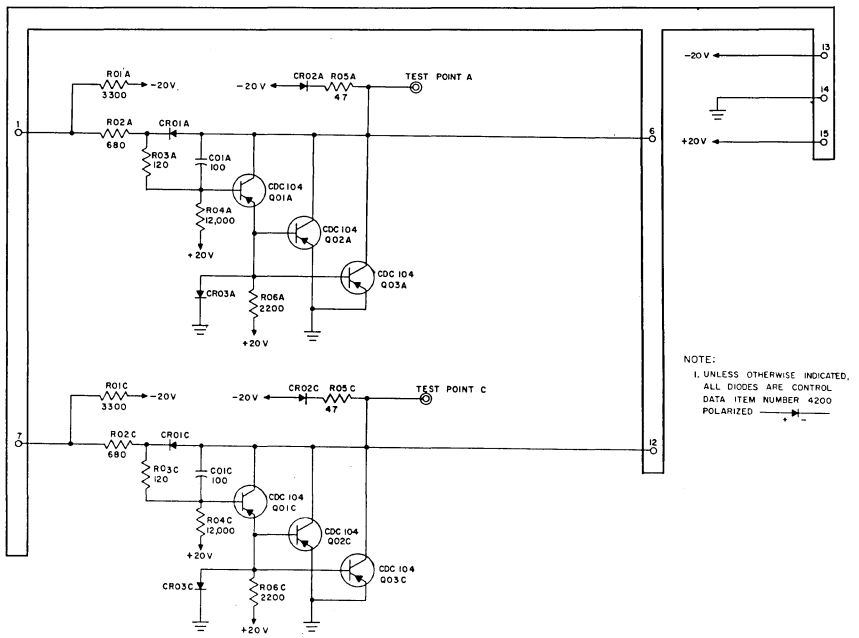
A -12v input signal to either generator of a type 58 card causes Q01 to conduct and thus enable Q02 and Q03. Current from the external source connects to the generator via terminal 6 or 12 and passes through Q02 and Q03 to ground.



Inhibit Generator 55



Inhibit Generator 58



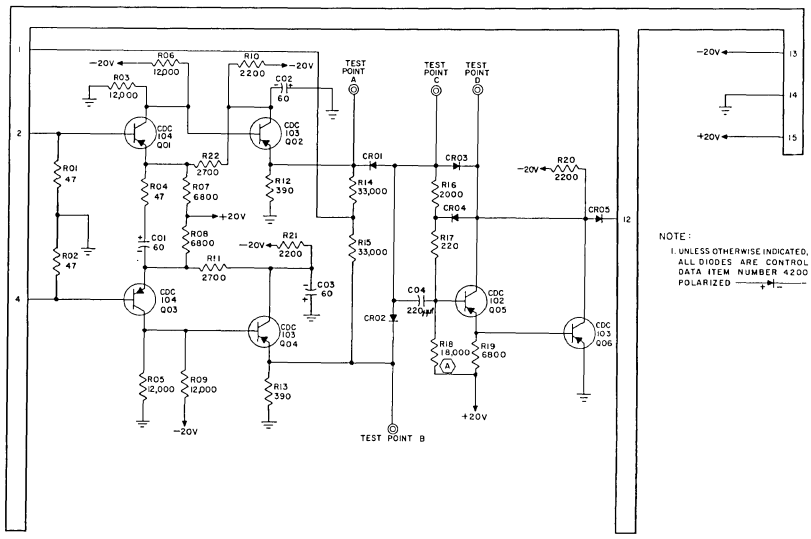
Inhibit Generator 59

SENSE AMPLIFIER

Type 56

The 56 card amplifies the signals from a memory plane as the result of a read pulse, and produces a "0" output when a core switches. Transistors Q01 to Q04 are connected in a differential amplifier circuit. The signals from either end of the sense windings are applied to Q01 and Q03. The emitters are held at the difference voltage by a difference network composed of R04 and C01; noise voltages on the sense line are cancelled.

Capacitors C02 and C03, in the collector circuits of Q02 and Q04, provide d-c stabilization. Diodes CR01 and CR02 pass the negative-going components of the signals from Q02 and Q04, and serve as clippers. The bias across these diodes, and thus the clipping level, is adjustable by the Margin Switch on the operator's console. When the switch is up, +20v is applied to the junction of R14 and R15 raising the reference voltage across the input diodes to the last stage. When the switch is down, -20v is applied to R14 and R15 making the circuit more sensitive to the signal from the sense line which tends to make spurious pulses look like "1's". Transistors Q05 and Q06 are connected in an amplifier-inverter circuit. The output, a signal from CR05, as a result of a "1" signal from the sense wire, is -0.5v.



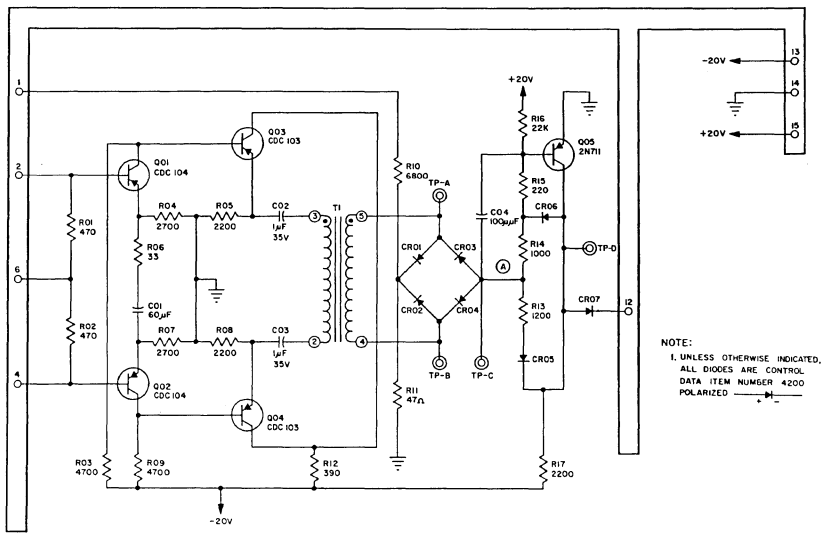
Sense Amplifier 56

SENSE AMPLIFIER

Type 57

The sense amplifier below amplifies the signal from a memory plane (pins 2 and 4) as the result of a read pulse, and produces a "0" output when a core switches. Transistors Q01, Q02, Q03, and Q04 form a differential amplifier which feeds T1 through coupling capacitors C02 and C03. The secondary of T1 is connected to a bridge detector so that the signal polarity at (A) is always the same. The Q05 network is a standard inverter circuit providing normal output logic levels of -3.0v and -0.5v.

Gain from the differential amplifier for the common mode component of the input signal is about 2; for the differential mode component, across R06 - C01, gain is about 100. Detector bias is determined by the Margin switch on the console. With the switch at HI, the +20v applied to pin 1 raises the reference level of the detector making it less sensitive; weak signals tend to be dropped. With the switch at LO, -20v appears at pin 1 and the detector is more sensitive to spurious pulses. No connection to pin 1 is made when the switch is in the normal, center position. Pin 6 is connected to the diverter bus (-7.0v) to provide bias for input transistors Q01, Q02. The output from Q05, as the result of a "1" signal on the sense lines, is -0.5v.



Sense Amplifier 57

EVEN PLANE
INHIBIT DRIVER
Card Type C00

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from the +40v source at pin 6 to the inhibit winding at pin 1 or pin 15. This occurs whenever all inputs to the respective circuit are at the logical "1" level of -5.8v. The inhibit circuit contains a series 120-ohm resistor so that the resulting current is approximately 340 ma.

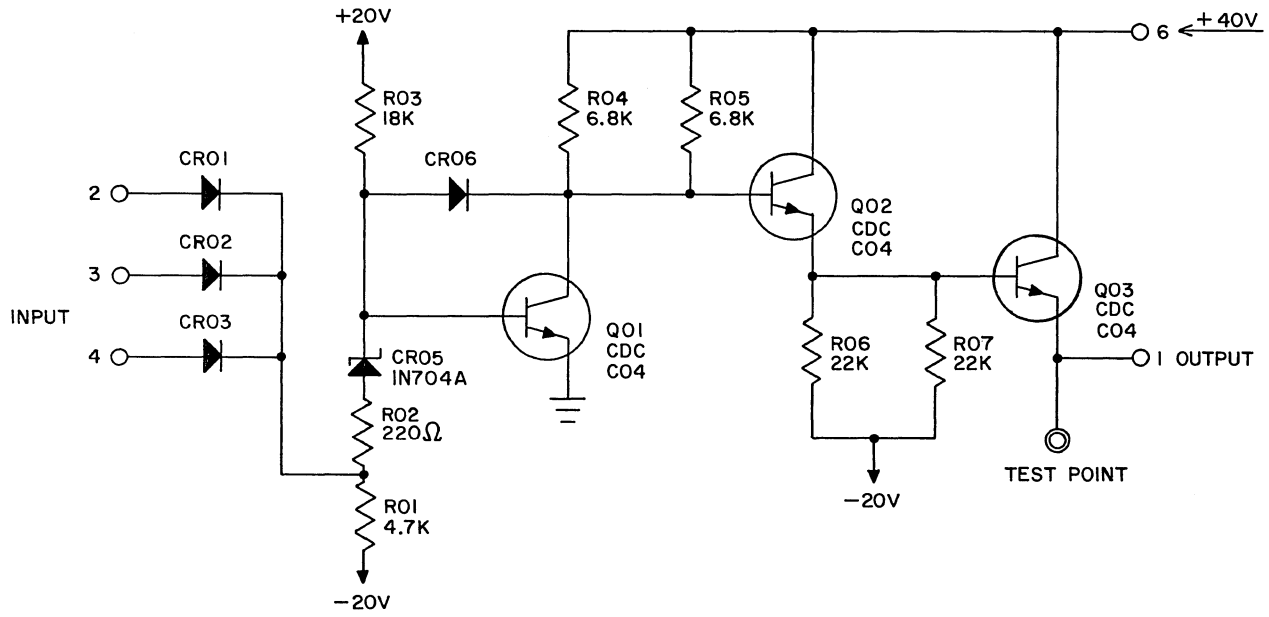
OPERATION

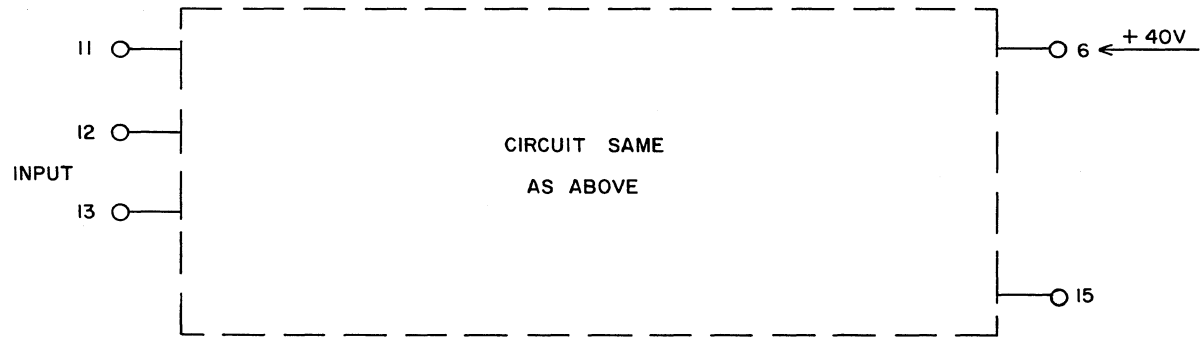
Each circuit has a three-way logical AND input, meaning that all inputs must be at the -5.8v "1" level in order for an input to be sensed. A -1.1v "0" signal on any input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

A level-shifting action is provided to the base of Q01 by resistors R01, R02, R03, and the 4.1v zener diode CR05. The zener diode CR05 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When a -1.1v "0" signal appears at an input, the zener diode CR05 places a forward bias on the base of Q01. Transistor Q01 then switches to a state of heavy conduction. It is held out of saturation by the feedback diode CR06 and its collector voltage is approximately +0.4v. The low collector voltage of Q01 is also the base voltage of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is equal to its +0.4v base voltage minus its base-emitter junction drop, and is approximately -0.3v. This provides sufficient forward bias so that a minimum conduction is maintained through Q02. Transistor Q03 is connected as an emitter follower with the inhibit winding load in series with the emitter. The emitter of Q03 is connected to ground through the inhibit line. The base-emitter junction is therefore reverse biased by the -0.3v input, so that Q03 is cut off. This disables the current path from the +40v supply to the inhibit winding.

With the AND input satisfied by -5.8v "1" signals, the base of Q01 is biased at approximately -1.5v and Q01 is cut off. The collector voltage of Q01 rises to approximately +38.5v (40v minus the IR drop across R03 and R04). This provides drive to the





NOTES:

1. EACH CIRCUIT HAS THREE "AND" INPUTS.
2. TRANSISTORS Q02 & Q03 CONDUCT WHEN ALL INPUTS ARE -5.8V "1".
3. ALL DIODES ARE HD2969 UNLESS OTHERWISE INDICATED.

EVEN PLANE

Inhibit Driver C00

base-emitter junction of Q02. Transistor Q02 is connected as an emitter follower; thus its emitter voltage becomes approximately +38v. This provides a strong forward bias to the base of Q03, causing Q03 to conduct heavily. The voltage applied to the inhibit line is the emitter voltage of Q03 and is approximately +37.5v. The 340 ma inhibit current is also the emitter current of Q03, and is allowed to flow when Q03 switches to the conduction state.

LINE DRIVER

Card Type C03

FUNCTION

The function of the circuits on this card is to enable 450 ma of positive current to flow from the output pins 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. Pins 1 and 15 connect to the two ends of the primary windings of eight memory driver transformers. During the memory cycle, one transformer will be center-tapped to +20v; thus current flow in either direction may be obtained by selecting one of the circuits on the C03 card.

The output pins 1 and 15 are connected as shown on page 3-C03-2 by capacitor C03 and resistor R06, which form a series differentiating network. This connection transmits only those signals having a high rate of change, such as a sharp noise spike, and blocks entirely a steady d-c voltage. Thus, a noise spike appearing at pin 1 also appears at pin 15, and their total effect is to cancel each other. However, the d-c levels of pins 1 and 15 are completely separated if either circuit switches to the conduction state while the other remains cut off.

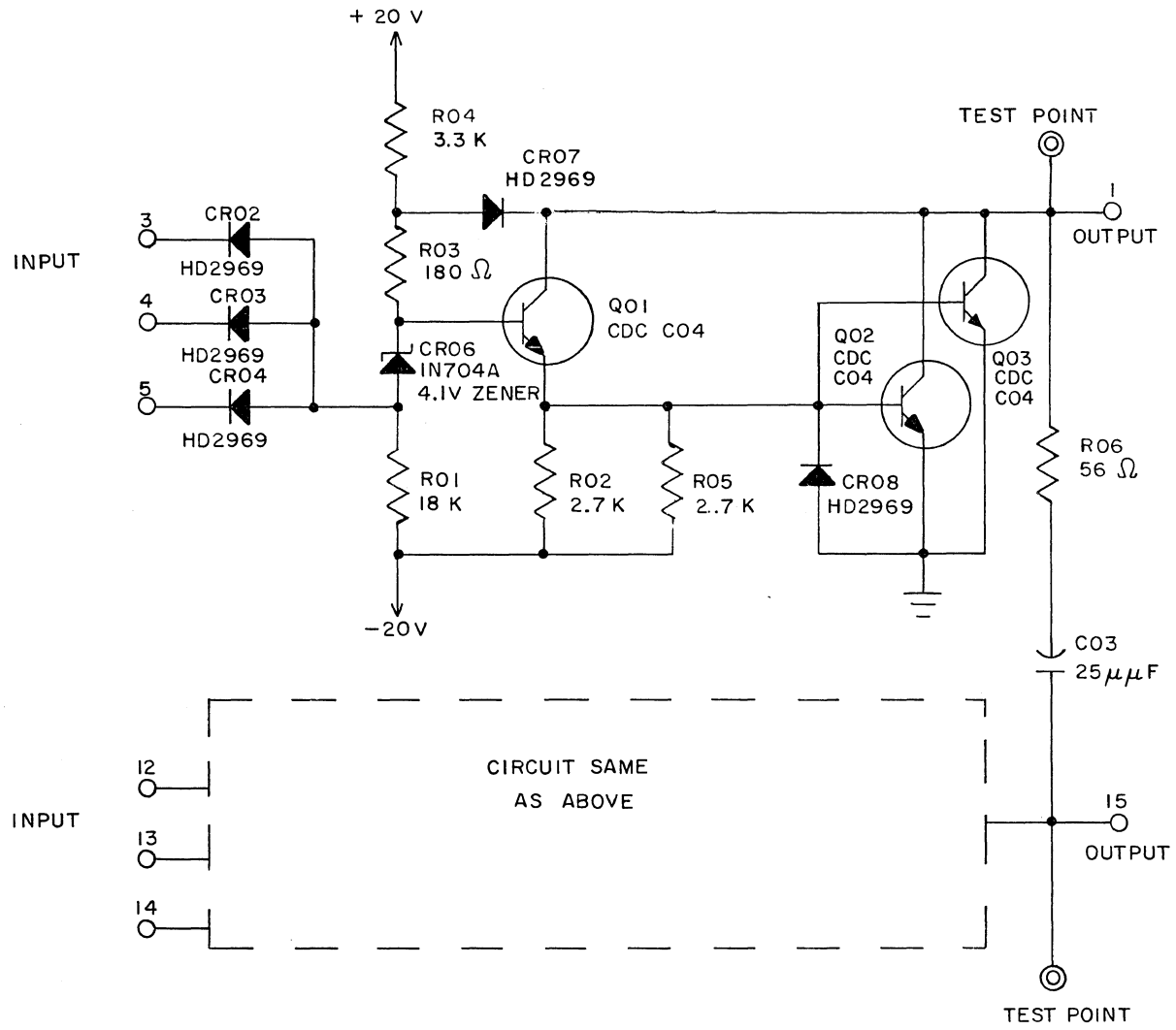
OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit; however, the component numbers mentioned are those appearing in circuit A.

A level shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and it is cut off. The bases of Q02 and Q03 are held at approximately -0.3v by the forward drop of diode CR08, and they are likewise cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing



NOTES:

1. EACH CIRCUIT HAS 3 "OR" INPUTS.
2. TRANSISTORS SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

Line Driver C03

through the transformer primary into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a positive voltage. This forward bias is sufficient so that Q01 conducts heavily, but it is held out of deep saturation by diode CR07 and resistor R03. Transistor Q01 in its conduction state allows the +20v source, which connects to pin 1 through the transformer primary, to bias the bases of Q02 and Q03 at a positive potential. Thus they also conduct heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of approximately 1v across Q02 and Q03.

Transistors Q02 and Q03 are grounded emitter stages driven by the emitter follower stage Q01. Their base drive is taken directly from the emitter of Q01; thus the input to Q02 and Q03 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the bases of Q02 and Q03 well into the positive voltage domain, so that they also switch on and conduct heavily. Likewise, when Q01 switches off, Q02 and Q03 also switch off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junctions of Q02 and Q03 so that they are well into the cut off region.

ODD PLANE
INHIBIT DRIVER
Card Type C04

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from pin 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. The inhibit wires are energized by a source of +40v, and each inhibit circuit contains a series 120-ohm resistor so the resulting current is approximately 340 ma. The odd plane inhibit wires terminate at either pin 1 or pin 15 of a C04 card, and the path is completed to ground allowing current to flow, if the respective inhibit generator circuit switches to its conduction state.

OPERATION

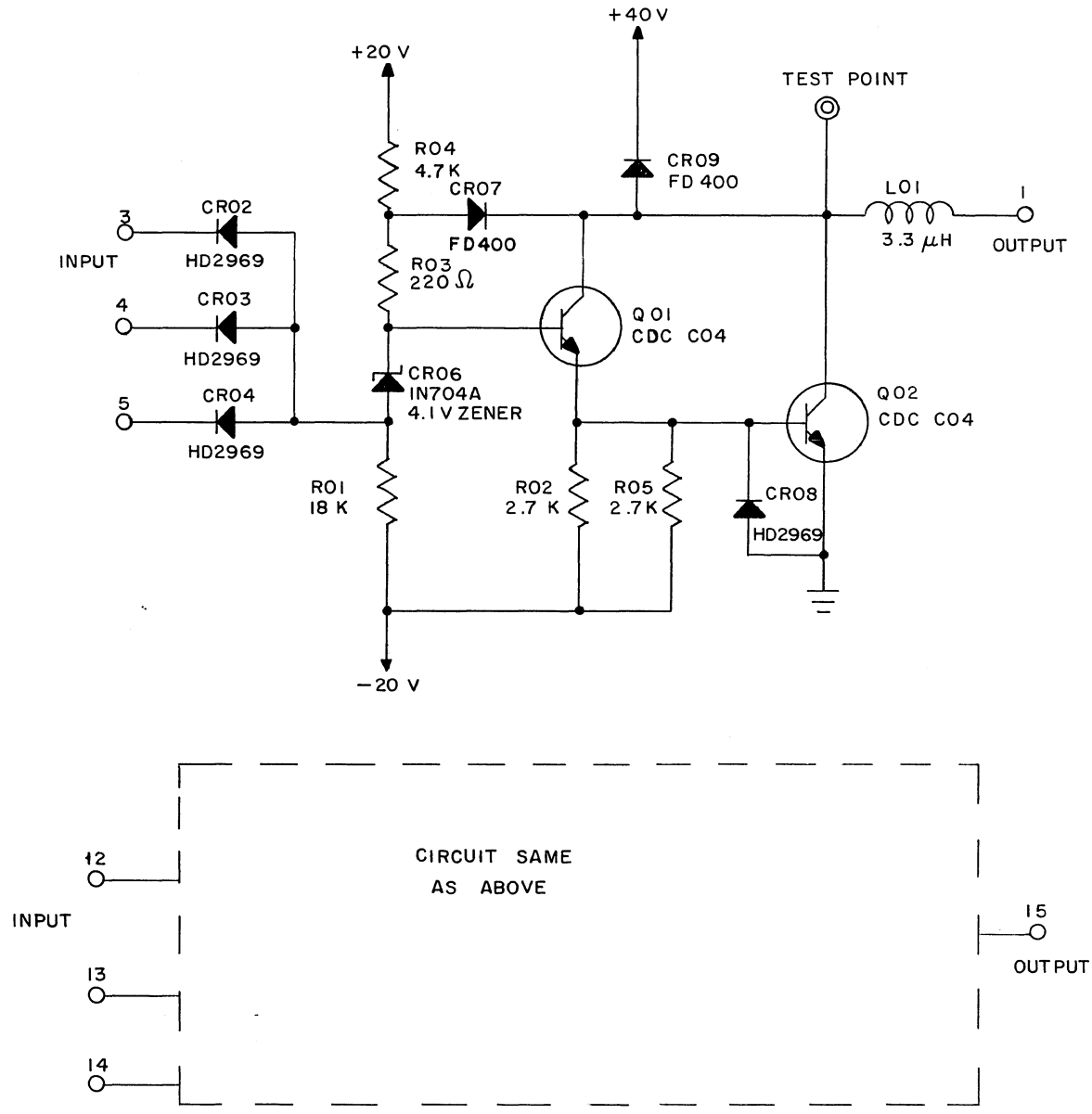
The two circuits contained on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit but the component numbers mentioned are those appearing in circuit A.

A level-shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and Q01 is cut off. The base of Q02 is held at approximately -0.3v by the forward drop of diode CR08, and Q02 is also cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing through the inhibit wire into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a sufficiently positive voltage so Q01 conducts heavily. In this state, diode



NOTES:

1. EACH CIRCUIT HAS THREE "OR" INPUTS.
2. A CIRCUIT WILL SWITCH TO ITS CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

ODD PLANE

Inhibit Driver C04

CR07 holds Q01 out of saturation. Transistor Q01 in its conduction state allows the +40v source, which connects through the inhibit wire to pin 1, to bias the base of Q02 at a positive level. Thus transistor Q02 also conducts heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of 1v across Q02.

Transistor Q02 is a grounded emitter stage driven by the emitter follower stage Q01. The base drive for Q02 is taken directly from the emitter of Q01; thus the input to Q02 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the positive voltage domain, so Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junction of Q02 so it is well into the cut off region.

The connection of diode CR07 and the +40v source provides a clamp for the collector voltage of the transistors. When the transistors switch to the non-conducting state, the inductance of the inhibit wire tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode.

The 3.3 uh inductor in series with the output pin is for reducing ringing on the inhibit wire. The inductor increases the current rise time and hence reduces the overshoot.

GATE
Card Type C05

FUNCTION

The function of the Gate circuit is to enable a current path from a +20v source through which current of the order of 900 ma flows to the primary windings of two memory driver transformers. Pin 4 connects to +20v and pins 1, 2, and 3 provide the output. The path from pin 4 to the output is enabled only when all inputs to the Gate circuit are at the logical "0" level of -1.1v.

The function of the Discharger circuit is to ground the primary windings of the two memory driver transformers previously energized. This removes stored charge from the windings and neutralizes the transformers. The Discharger circuit is enabled by a -1.1v "0" input.

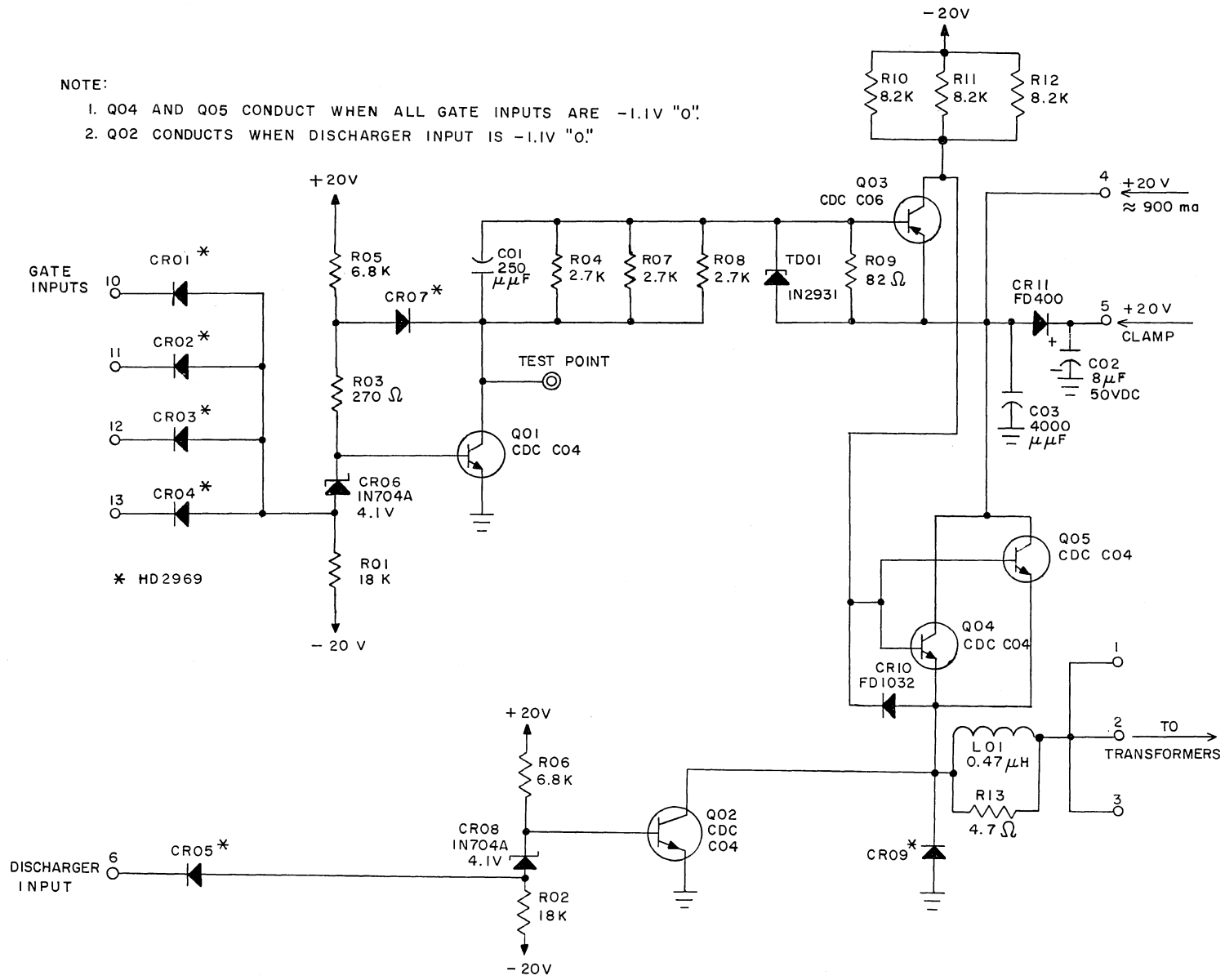
OPERATION

Pins 10 through 13 provide four logical OR inputs to the Gate circuit, and pin 6 provides an OR input to the Discharger. An unused input is interpreted as a steady "0", regardless whether it is grounded or left open.

A level-shifting action for the Gate inputs is performed by resistors R01, R03, R05, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations. Resistors R02, R06, and zener diode CR08 perform the level-shifting action for the Discharger.

With open circuits or logical "0" signals on all Gate inputs, the base of Q01 is at an approximate potential of +0.7v. It is prevented from going more positive by the low forward base-emitter impedance of Q01. During this time, Q01 is in the conduction state. However, if any input receives a -5.8v "1", the zener diode CR06 holds the base of Q01 at approximately -1.7v and Q01 is cut off.

During the time that Q01 is cut off by a "1" signal, its collector potential is raised to a high positive value by the +20v source attached to pin 4. Since no appreciable current now flows through the 82-ohm resistor and tunnel diode between base and emitter of Q03, it is also essentially cut off.


NOTE:
1. Q04 AND Q05 CONDUCT WHEN ALL GATE INPUTS ARE -1.1V "0".
2. Q02 CONDUCTS WHEN DISCHARGER INPUT IS -1.1V "0."
-20V
R10 8.2K
R11 8.2K
R12 8.2K
+20V
Q03 CDC C06
4 +20V ≈ 900 ma
GATE INPUTS
10
11
12
13
CR01 *
CR02 *
CR03 *
CR04 *
R05 6.8K
CR07 *
C01 250 μμF
R04 2.7K
R07 2.7K
R08 2.7K
TD01 IN2931
R09 82 Ω
CR11 FD400
5 +20V CLAMP
C02 8μF 50VDC
C03 4000 μμF
TEST POINT
R03 270 Ω
Q01 CDC C04
CR06 IN704A 4.1V
R01 18 K
* HD2969
-20 V
Q05 CDC C04
Q04 CDC C04
CR10 FD1032
1
2 TO TRANSFORMERS
3
L01 0.47μH
R13 4.7 Ω
CR09 *
+20V
R06 6.8K
CR08 IN704A 4.1V
Q02 CDC C04
DISCHARGER INPUT
6
CR05 *
R02 18K
-20V

When Q01 switches to its conducting state, current is allowed to flow from the +20v source at pin 4 through the tunnel diode and 82-ohm resistor between emitter and base of Q03, through the three parallel 2.7k resistors, and through Q01 to ground. A threshold level is provided by the tunnel diode, since in its low-voltage state, it does not allow Q03 to conduct. However, when current through the tunnel diode increases to 10 ma, it switches to its high-voltage state. This places approximately 0.8v forward potential on the base of Q03 causing it to switch to its conduction state. This enables the series circuit from +20v at pin 4 through Q03 and through the three parallel 2.7k resistors to -20v. The base drive for Q04 and Q05 is taken from the collector of Q03, and when Q03 conducts, turn-on current is provided for Q04 and Q05 so that they switch to the conduction state. Thus the circuit is completed, allowing positive current to flow from pin 4 to the output. When Q03 switches off, the voltage drop across diode CR10 applies a reverse bias of approximately 0.6v to the base-emitter junctions of Q04 and Q05, cutting them off.

Transistors Q04 and Q05 control a current of the order of 900 ma flowing in a highly inductive load. Diode CR09 is therefore provided so that when Q04 and Q05 interrupt the current, the induced high-voltage transient is dissipated with no effect on other transistors.

Diode CR11 acts as a clamp against positive voltage surges at the collectors of Q04 and Q05 when current is interrupted. Pin 5 connects to a separate +20v bus and prevents pin 4 from becoming more positive than +20.6v, taking into account the 0.6v drop across the silicon diode.

Capacitors C02 and C03 provide a smoothing filter for spikes and ripple in the +20v sources at pins 4 and 5. The 8 microfarad capacitor C02 is sufficient for ripple and low frequency fluctuations; however, it exhibits a certain amount of inductive reactance due to its large area. For this reason, it is necessary to include C03 which has negligible inductive reactance and is therefore effective in filtering high frequency spikes.

The Discharger circuit is enabled by a -1.1v "0" input on pin 6. This causes zener diode CR08 to apply sufficient forward bias to the base of Q02 so that Q02 switches to its maximum conduction state. Transistor Q02 thus provides a low impedance path to ground for any stored charge remaining in the primary windings of the two memory driver transformers.

SENSE AMPLIFIER
Card Type C06

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "0" output on pin 15.

The circuit may be conveniently divided into two sections: a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -13.6v. The output of -13.6v represents a logical "1" which changes to a logical "0" when a memory core switches its magnetic state. The following logic card interprets any signal more positive than -3v as a logical "0", however the discriminator output approaches -1.6v when a core switches.

AMPLIFIER

The differential voltage amplifier is the symmetrical portion of the circuit to the left of the diode bridge, as shown in the accompanying diagram. Input signals from the sense winding are received on pins 4 and 5. The ends of the sense winding are connected to these two pins, forming a series loop which threads all memory cores in a plane quadrant. The only ground reference to this loop is through the 1000-ohm resistor R02, thus the nominal 30 mv potential induced in the sense winding by the switching of a core is applied equally and oppositely to both input pins. This is amplified into a 3v signal which appears across the diode bridge.

The amplifier circuit is sensitive only to the difference in potential between pins 4 and 5, which is produced by the application of a double-ended signal from the sense winding. A simultaneous shift of the d-c reference level of both input pins produces only a negligible effect. It is possible for both inputs to fluctuate simultaneously by as much as 2v without producing more than 0.2v fluctuations at the diode bridge.

"Common mode rejection ratio" refers to the number used to represent the degree of sensitivity exhibited by a differential amplifier to potential differences between its inputs and simultaneous shifts of both inputs in the common mode. The number for this circuit is of the order of 40,000.

Resistors R01 and R03 are connected in series across the two inputs as shown. This relatively low resistance is in parallel with the input impedance of the amplifier, so that the total terminating impedance across the sense line is reduced. This has the effect of making the amplifier less sensitive to noise induced by the flow of inhibit current.

The 3.3 uh inductors in the emitter circuits of Q02 and Q03 determine the high frequency roll-off of the amplifier. This inductance reduces the gain at high frequencies and prevents the amplifier from responding to noise spikes.

The signals produced by the memory cores are received and amplified in the double-ended fashion. As an example of operation, assume that the 30 mv potential from the memory core is in a direction so that pin 4 shifts negative 15 mv and pin 5 shifts positive 15 mv from the rest state. These potentials are applied to the bases of Q02 and Q03, causing Q02 to conduct more heavily while conduction through Q03 decreases. This action is further regulated by the constant-current source through Q01, so an emitter current increase in Q02 must be accompanied by a decrease in Q03.

Due to the action described above the collector of Q02 becomes more positive and the collector of Q03 becomes more negative. This, in turn, causes transistors Q04 and Q06 to conduct less heavily while conduction through Q05 and Q07 increases. The collectors of Q04 and Q06 therefore shift approximately 1.5v in the negative direction and the collectors of Q05 and Q07 shift a similar amount in the positive direction. A potential difference of 3v then exists across the diode bridge.

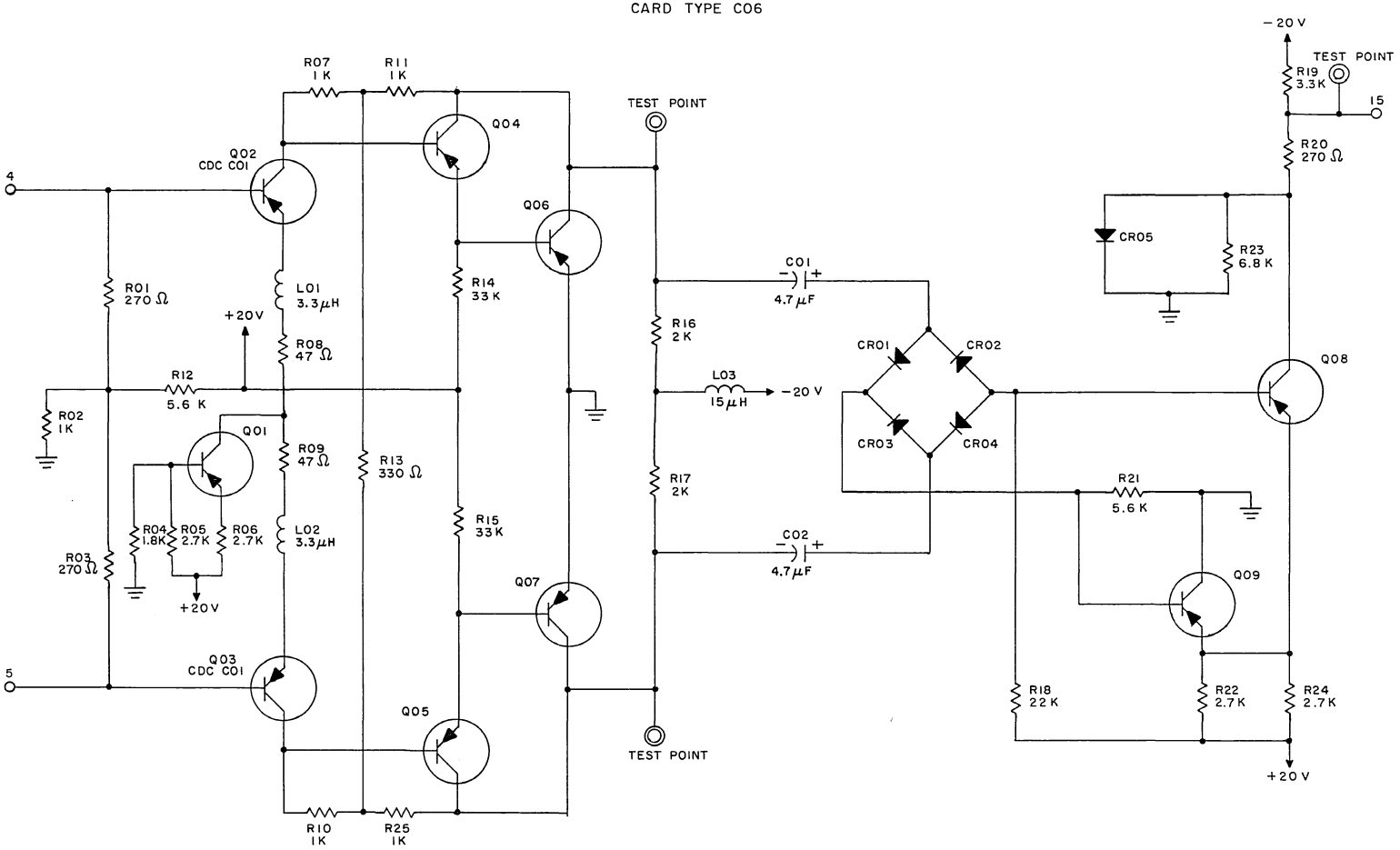
The signals from the collectors of Q02 and Q03 are amplified by a factor of 100 by Q04 and Q06, and by Q05 and Q07, respectively, which are connected as an emitter follower and a grounded emitter amplifier. Depending upon their particular characteristics, the two transistors are capable of providing a maximum available gain of the order of 1000. To insure stable operation, this is reduced to around 30 by the negative feedback connection of the two 1000-ohm resistors from collector to base. A portion of this negative feedback, however, is nullified by the 330-ohm resistor connecting the two feedback lines, so the over-all voltage gain of each of the stages is approximately 100.

DISCRIMINATOR

The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The

SENSE AMPLIFIER

CARD TYPE C06



NOTE :

1. ALL DIODES FD 1032.
2. ALL TRANSISTORS CDC C02, UNLESS OTHERWISE INDICATED.

output of the discriminator is from pin 15 and is approximately -13.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -1.6v which is interpreted as a logical "0".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q08 is held at around 1.2v higher positive potential than the base of Q09. Transistor Q09 thus conducts quite heavily while Q08 conducts very little. Under these conditions the output at pin 15 is around -13.6v, due to the voltage dividing action of R19, R20, and R23. Transistor Q09 provides a low impedance path to ground, so the emitter of Q08 cannot rise to a high positive potential when it is in a state of low conduction.

The diode bridge rectifies the potential across it, so an input of either polarity results in a negative input to the base of Q08 and a positive input to the base of Q09. This has the effect of causing Q08 to conduct heavily while Q09, in turn, conducts very little. Transistor Q08 thus enables a low impedance path from +20v to ground through diode CR05, which is a silicon diode having a forward drop of approximately 0.6v. The anode of CR05 is therefore at approximately +0.6v, so that pin 15 is biased at approximately -1.6v by resistors R20, R19, and the -20v source. This output voltage level is interpreted as a logical "0"

INHIBIT COMPENSATOR
Card Type C09

FUNCTION

The function of the circuits on this card is to enable a 340 ma current to flow from pin 1 or 15 to ground, whenever at least one input to the respective circuit is a -1.1v "0". The inhibit compensator circuits are energized by a +40v supply. Each circuit contains a series 133-ohm resistor external to the circuit on the card. Each inhibit compensator circuit terminates at either pin 1 or pin 15 of a C09 card, and the path is completed to ground allowing current to flow if the respective circuit attached to that pin switches to its conduction state.

OPERATION

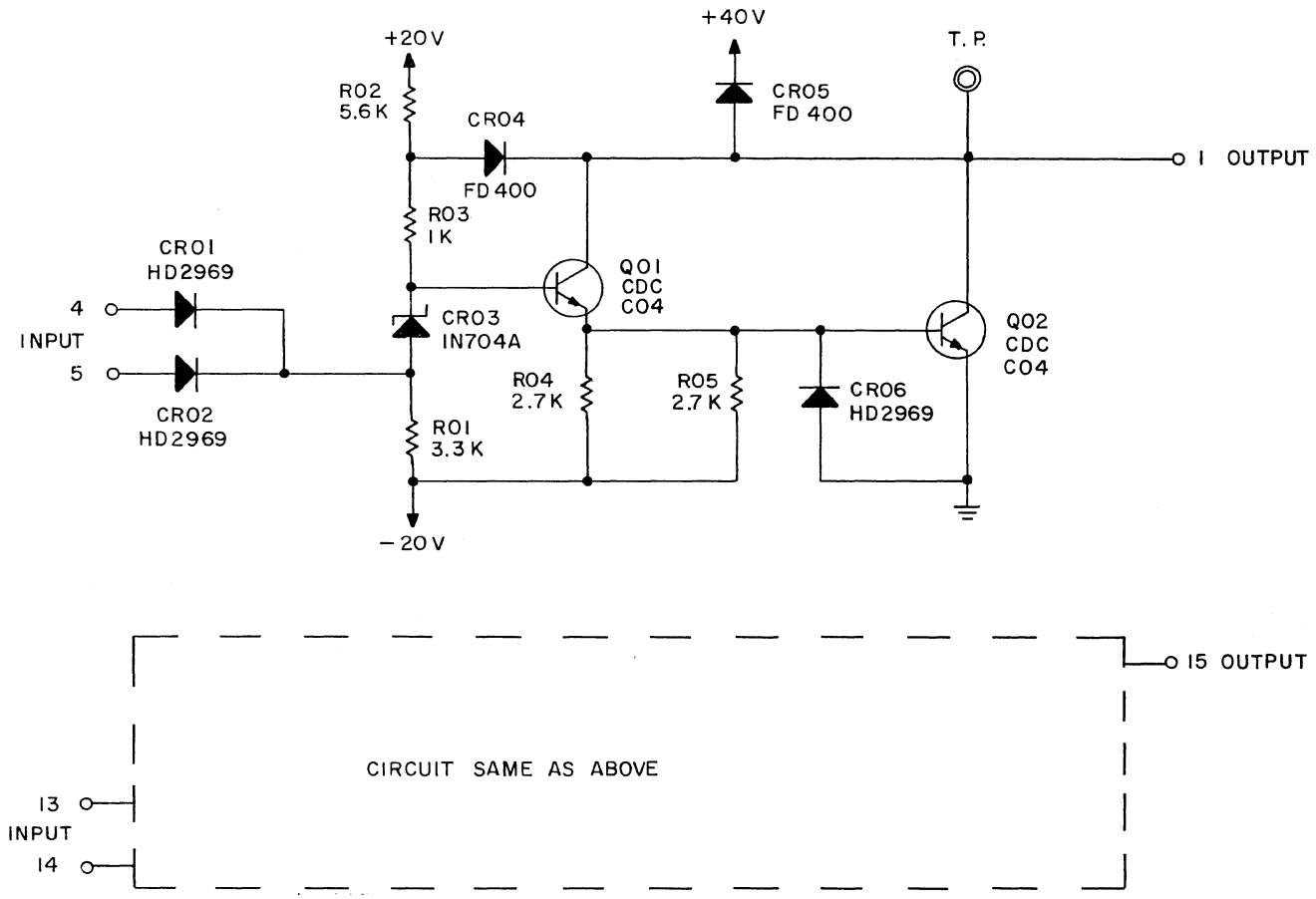
Each circuit has a two-way logical AND input, meaning that both inputs must be at the -5.8v "1" level for an input to be sensed. A -1.1v "0" signal on either input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

The transistors are disabled if the AND is satisfied by two -5.8v "1" inputs, preventing current from flowing. If either input receives a -1.1v "0", the transistors switch to the conduction state and current is allowed to flow from the output pin to ground.

A level-shifting action is provided by the 4.1v zener diode CR03. This diode is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When the AND is satisfied by -5.8v "1" inputs, this voltage level plus the forward drop of diodes CR01 and CR02 holds the anode of CR03 at approximately -6.1v. The base of Q01 is therefore at approximately -2v. The emitter of Q01 is held at approximately -0.3v by the forward drop of CR06. This places a reverse bias of 1.7v across the base-emitter junction of Q01, so it is well into the cut off region. In addition, the 0.3v drop of CR06 reverse biases the base-emitter junction of Q02, so that it is also cut off. Thus, except for negligible leakage effects, the output pin is completely isolated from ground.

When either input receives a -1.1v "0", the anode of CR03 is held at approximately -1.4v. The 4.1v voltage differential across the zener diode CR03 attempts to hold the



NOTES:

1. EACH CIRCUIT HAS A TWO-WAY "AND" INPUT.
2. A -1.1V "0" ON EITHER INPUT ENABLES CIRCUIT TO CONDUCT.
3. -5.8V "1's" ON BOTH INPUTS PREVENT CIRCUIT FROM CONDUCTING.

Inhibit Compensator C09

base of Q01 at approximately +2.7v. This causes Q01 to switch on and conduct heavily, but it is clamped out of saturation by CR04. The emitter voltage of Q01 rises to approximately +2.2v, providing drive to the base of Q02. Transistor Q02 thus switches to the conduction state, allowing current to flow from the output pin to ground.

The connection of diode CR05 and the +40v supply provides a clamp for the collector voltage of the transistors. When the transistors switch to the nonconducting state, the inductance of the load tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode CR05.

DRIVE LINE TRANSFORMER
Card Type C10

FUNCTION

The function of this card is to provide half-currents of 340 ma at approximately 44v to the memory stack when supplied with primary power at the +20v level. The card contains four 3:4 voltage step-up transformers, each having two secondary windings of 32 turns and a center-tapped primary of 48 turns. The transformers are connected so that two operate simultaneously with their primary windings energized in parallel from +20v and their secondaries connected in series. The output voltages are therefore additive, resulting in levels of approximately 44v.

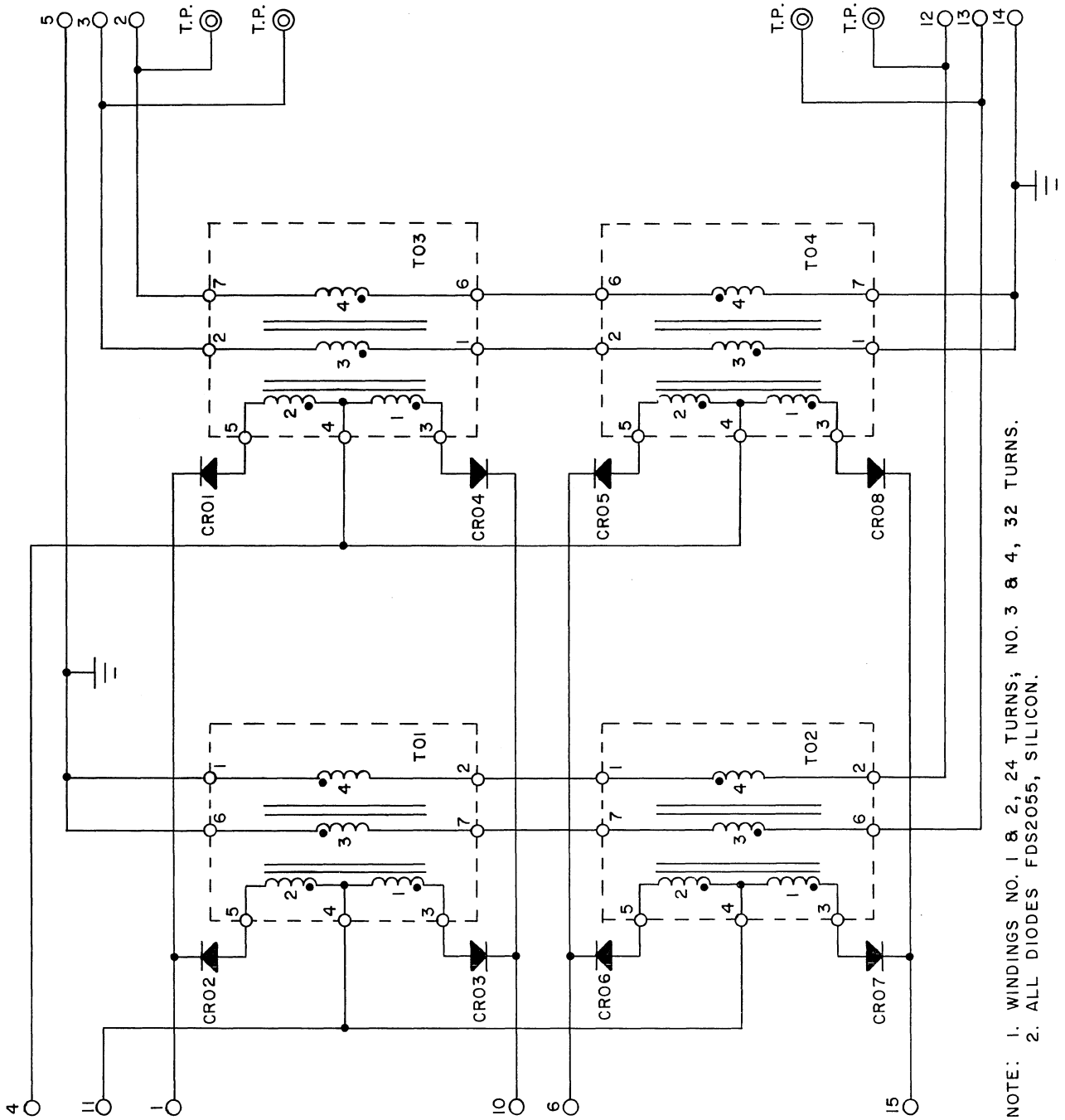
This card operates in conjunction with three other cards; a gate card which switches a source of +20v into the center taps of the transformer primaries, and with two transformer driver cards which allow current to flow from one of the primary windings to ground.

OPERATION

A schematic of the circuit contained on card type C10 is presented in the accompanying diagram, with the transformers indicated by dashed outlines. The transformers are identical, each having four windings and seven connecting pins as shown. Silicon diodes at transformer pins 3 and 5 provide isolation so current cannot flow through a primary winding in the wrong direction and prevent interaction between transformers.

The dots on the transformer windings indicate polarities according to the usual convention. For example, if current flows into the dotted end of the primary winding, current must flow out of the dotted end of the secondary winding. If a voltage is impressed across the primary winding so that the dotted end is positive, the dotted end of the secondary will also be positive.

As an example of operation, assume that card pin 11 is energized from a source of +20v. This is fed to the center tap of the primary windings of transformers T01 and T02. Then, by connecting card pins 1 or 10, and 6 or 15 to ground, it is possible to produce either +44v or -44v at either pin 12 or pin 13 while the other pin remains at essentially zero potential. The positive and negative potentials correspond to the memory cycle, in which a current of one polarity is used to read and the other to write.



Memory Drive Line Transformer C10

REV. A

To produce +44v at pin 12, the external circuitry would connect card pins 10 and 15 to ground, allowing 450 ma to flow through windings # 1 of T01 and T02. The primary voltage is of the order of +18v, due to the drop across the silicon diode and external circuitry; however, the 3:4 transformer step-up produces a secondary voltage of approximately +22v.

It is seen that windings # 4 of T01 and T02 are connected in series so the voltages are additive, resulting in +44v at pin 12. It is further seen that windings # 3 are connected oppositely, so the voltages cancel and only a negligible effect is produced at pin 13. However, +44v appears at pin 13 with negligible voltage at pin 12 if the external circuitry grounds pin 6 instead of pin 15.

If it is desired to produce -44v at pin 12, then pins 1 and 6 are grounded; and if the -44v is to appear at pin 13, pins 1 and 15 are grounded.

Under the preceding sets of conditions, the voltages appearing on pins 12 and 13 appear on pins 2 and 3, if the source of +20v is gated into pin 4 instead of pin 11.

The various outputs available at pins 2, 3, 12, and 13 and the conditions necessary to produce them, are listed below. Pin 5 provides a common return for pins 12 and 13, and pin 14 provides a common return for pins 2 and 3.

Gate +20v into:	Enable Ground Connection From:	Resulting Voltages at: Pin 2	Pin 3	Pin 12	Pin 13
Pin 4	Pins 6 and 10	+44v			
Pin 4	Pins 1 and 15	-44v			
Pin 4	Pins 10 and 15		+44v		
Pin 4	Pins 1 and 6		-44v		
Pin 11	Pins 10 and 15			+44v	
Pin 11	Pins 1 and 6			-44v	
Pin 11	Pins 6 and 10				+44v
Pin 11	Pins 1 and 15				-44v

I/O SENSE AMPLIFIER
Card Type C86

FUNCTION

The function of the circuits on this card is to detect, amplify, and shape the pulse induced in the sense winding when a magnetic memory core switches state during the Read phase of the memory cycle. The pulse produced during the Write portion of the cycle is not detected.

During the rest state, the circuit output is a logical "1" of approximately -5.7v. When a core is read, the output switches to a logical "0" of approximately -0.5v.

The circuits are restricted to driving AND loads only.

OPERATION

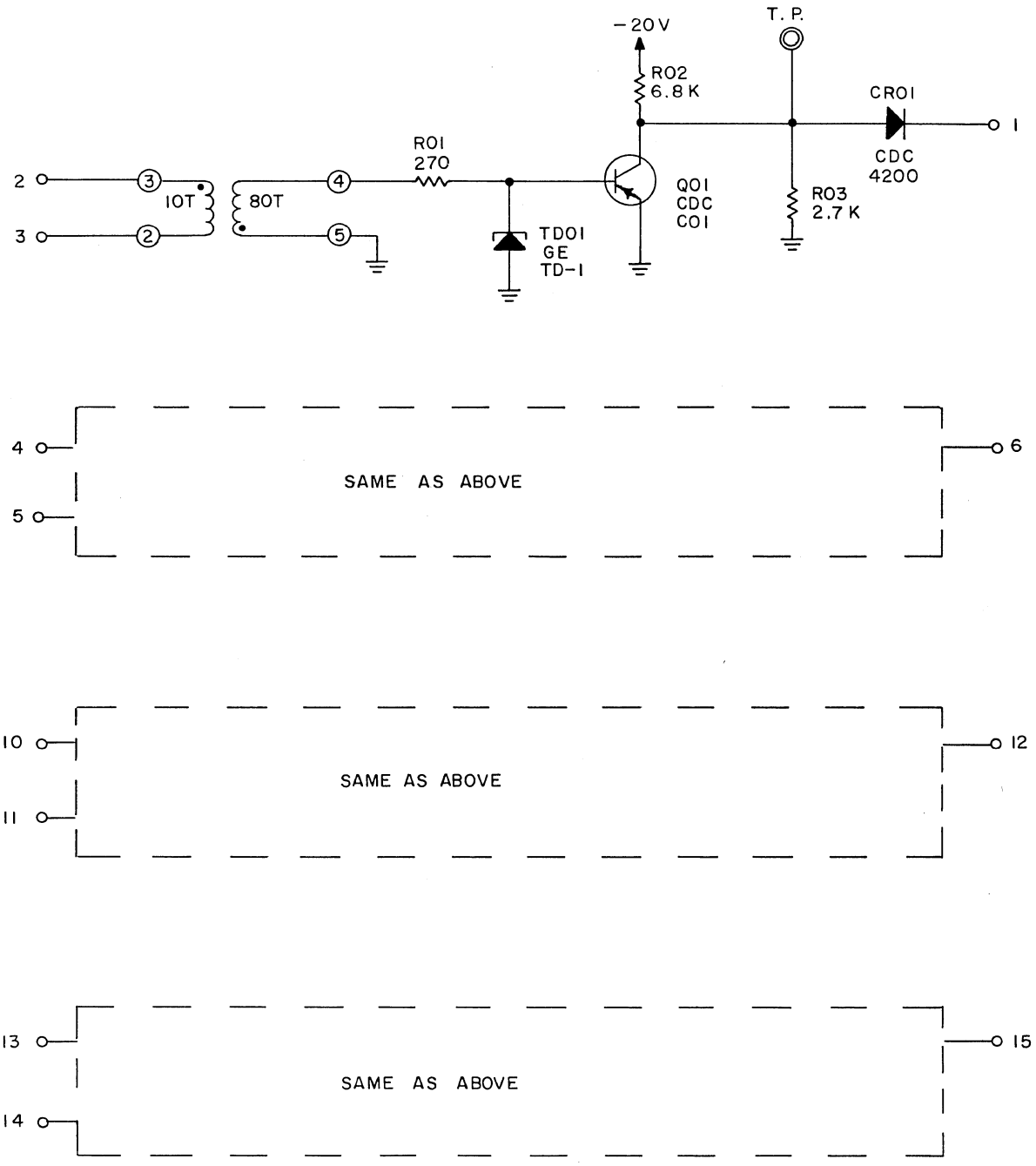
The Sense Amplifier circuit consists of a grounded emitter PNP transistor with a tunnel diode between base and ground. The tunnel diode provides a noise threshold rejection level and results in an essentially square output from the circuit.

In its low-voltage state, the tunnel diode holds transistor Q01 cut off. The circuit output is then produced by the voltage-dividing action of R02 and R03 and stabilizes at approximately -5.7v. The effect of the load is negligible, since the circuit is restricted to driving AND loads only.

The tunnel diode in its high-voltage state places a forward bias of approximately 0.5v across the base-emitter junction of Q01, causing Q01 to switch on and conduct heavily. The output voltage becomes equal to the collector voltage of Q01 plus the drop across diode CR01 and is approximately -0.5v.

The output produced when a memory core switches state is approximately 47 mv. During the Read phase, the core outputs are of a polarity such that pin 4 of the input transformer goes negative. The 47 mv input is increased by the 1 : 8 voltage step-up of the input transformer.

Initially, the tunnel diode is in its low-voltage state and the circuit is providing a "1" output. The tunnel diode remains in its low-voltage state as current through it increases, until it reaches the peak of its characteristic curve where I and V are approximately 1 ma and 65 mv, respectively. A slight increase in current puts the tunnel diode in the regenerative region and the voltage increases almost instantaneously to



NOTE:

A SENSE AMPLIFIER IS RESTRICTED TO DRIVING "AND" LOADS, ONLY.

I/O Sense Amplifier C86

500 mv. This causes Q01 to conduct and the circuit output switches to "0". The tunnel diode remains in the high-voltage state until current through it decreases to approximately 0. 12 ma. This is the characteristic curve valley, and at this point, the voltage drops almost instantaneously to approximately zero. This cuts off transistor Q01 and the circuit output returns to "1".

I/O MEMORY DRIVER
Card Type C87

FUNCTION

The function of this circuit is to provide drive current to a memory unit upon receipt of a -5.8v "1" input. The output may be either a half-current of approximately 200 ma, or a full current of up to 800 ma. In order to obtain a maximum current from pin 14 pin 10 must be grounded.

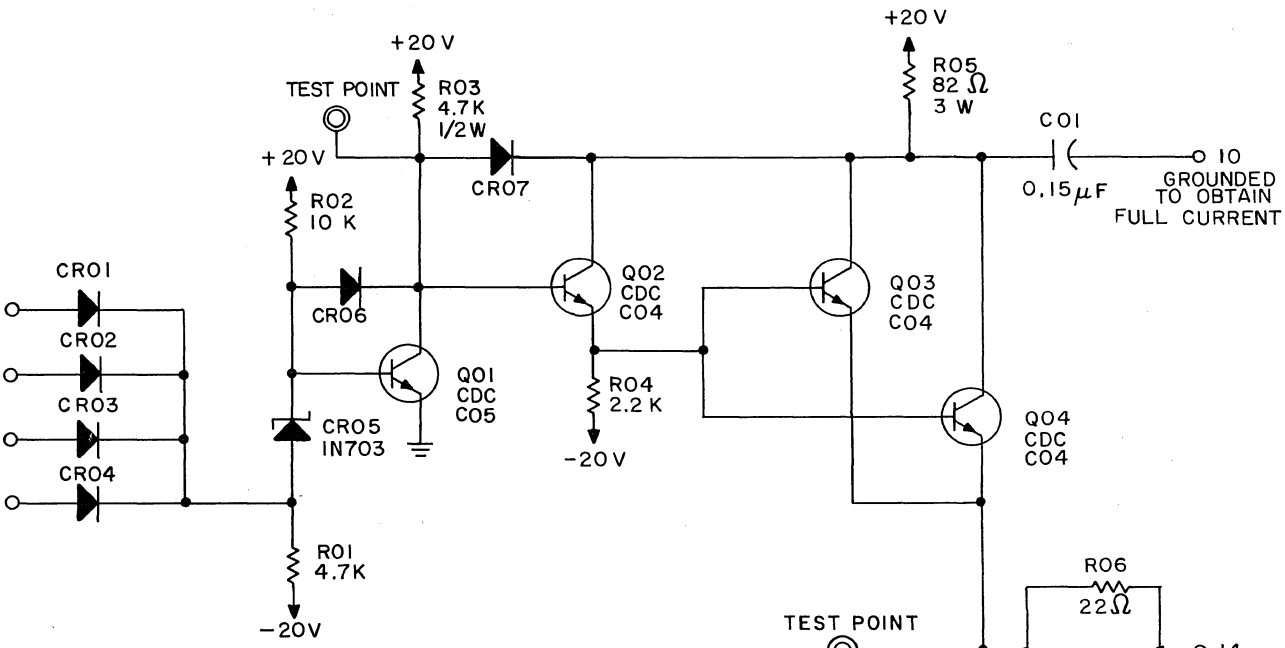
OPERATION

The circuit has a four-way logical AND input, meaning all inputs must be at the -5.8v "1" level in order for an input to be sensed. A 1.1v "0" on any input will disable the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 3.5v zener diode CR05. The zener diode CR05 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 3.5v positive with respect to the anode regardless of current fluctuations.

With -1.1v "0" inputs, zener diode CR05 holds the base of Q01 sufficiently positive so that it conducts heavily. Transistor Q01 is held out of deep saturation by CR06, and its collector voltage is approximately +0.5v. The collector voltage of Q01 is applied to the base of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is therefore equal to its base voltage less the base-emitter junction drop, and is approximately -0.1v. The emitter voltage of Q02 is applied to the bases of Q03 and Q04, which are also connected as emitter followers. The emitter circuits of Q03 and Q04 thread the memory plane and terminate at a Diverter circuit; thus the emitter voltage of Q03 and Q04 is approximately +0.9v. The -0.1v input from Q02 therefore back biases the base-emitter junctions of Q03 and Q04, cutting them off.

A -5.8v "1" input results in approximately -2.3v at the base of Q01, so Q01 is cut off. If the circuit is providing a half-current, pin 10 is not grounded and resistors R05 and R08 limit the current to approximately 200 ma. In addition, the voltage drop across R05 holds the collector voltage of the transistors at a relatively low level. The collector of Q01 rises to approximately +3.5v, providing drive to Q02. The emitter voltage of Q02 becomes approximately +2.9v, causing Q03 and Q04 to switch to the conduction state. Transistor Q02 is held out of deep saturation by CR07. Q03 and Q04 are held out



NOTES :

1. ALL DIODES CDC 4200, UNLESS NOTED.
2. CIRCUIT HAS A FOUR—WAY "AND" INPUT.
3. −5.8V "1's" ON ALL INPUTS CAUSE Q03 AND Q04 TO CONDUCT.

I/O Memory Driver C87

of deep saturation by the voltage drop across Q02. The emitter voltage of Q03 and Q04 is applied to the drive lines and is approximately +2.2v. The emitter currents of Q03 and Q04 combine to provide the memory drive current.

In order to obtain a peak value of full current from the circuit, pin 10 must be grounded. This allows capacitor C01 to become charged while the circuit is not providing drive current. When transistors Q03 and Q04 switch on, C01 discharges into the drive line, providing an initial high current surge. With Q01 cut off, its collector voltage rises to approximately +19v, providing drive to Q02. The emitter voltage of Q02 rises to approximately +18.4v, causing Q03 and Q04 to switch on and conduct heavily. The voltage applied to the drive lines is the emitter voltage of Q03 and Q04, and is approximately +17.8v during the initial high current surge. As capacitor C01 becomes discharged, the voltage levels within the circuit decrease toward the values given in the preceding paragraph.

I/O MEMORY DIVERTER
Card Type C88

FUNCTION

The function of this circuit is to enable memory drive current to flow from one of the output pins to ground, whenever all inputs are at the logical "0" level of -1.1v. The drive lines are energized with half-currents of 200 ma or full currents of up to 800 ma peak by the circuit contained on a Driver card C87. Each drive line terminates at one of the output pins of a Diverter card, and the circuit is completed to ground allowing current to flow when transistors Q02 and Q03 switch to the conduction state.

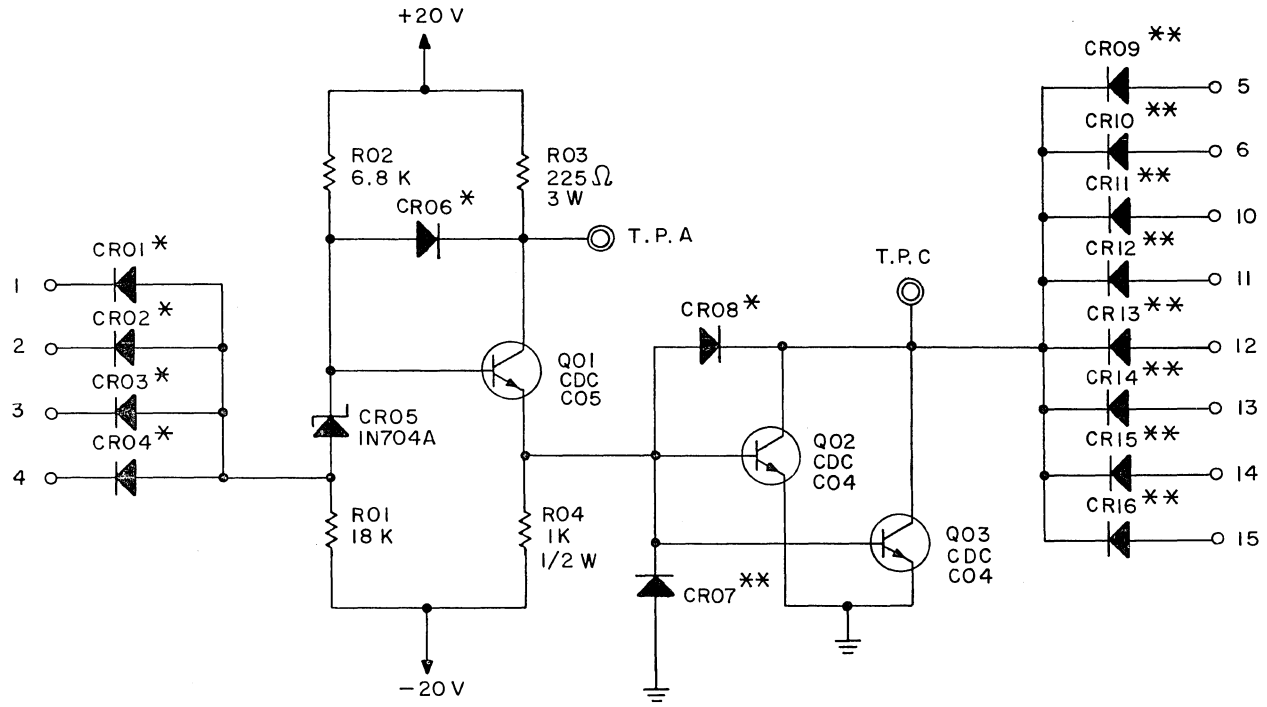
OPERATION

The circuit has four logical OR inputs, and transistors Q02 and Q03 switch to the conduction state only when all inputs are -1.1v "0". A -5.8v "1" on any input holds Q02 and Q03 in the cut off state.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 4.1v zener diode CR05. The zener diode CR05 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

A -5.8v "1" input results in approximately -1.5v at the base of Q01. This cuts off Q01, since its emitter is clamped at approximately -0.6v by diode CR07. The bases of Q02 and Q03 are also clamped at approximately -0.6v by diode CR07, and since their emitters are grounded, they are cut off.

If all inputs are at the -1.1v "0" level, zener diode CR05 holds the base of Q01 at approximately +1.4v. This causes Q01 to switch to a state of heavy conduction, but it is held out of deep saturation by diode CR06. Transistor Q01 is connected as an emitter follower; thus its emitter voltage rises to approximately +0.7v, providing drive for Q02 and Q03. The +0.7v input from Q01 causes Q02 and Q03 to switch on and conduct heavily, but they are held out of deep saturation by diode CR08.



* CDC 4200 (HD 2969)

** CDC 4211 (FD 400)

NOTES :

1. CIRCUIT HAS FOUR "OR" INPUTS.
2. TRANSISTORS Q02 AND Q03 SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE −1.1V "0".

I/O EMITTER FOLLOWER
Card Type C90

FUNCTION

The function of the circuits on this card is to convert the outputs from the brushes of a punched card reader into memory drive currents of approximately 200 ma. The circuit output is in series with a memory drive line, which connects to a -20v supply. The circuit input is driven by one of the brushes at a card reading station. When the brush senses a hole in the card, transistor Q01 conducts heavily, enabling memory drive current to flow.

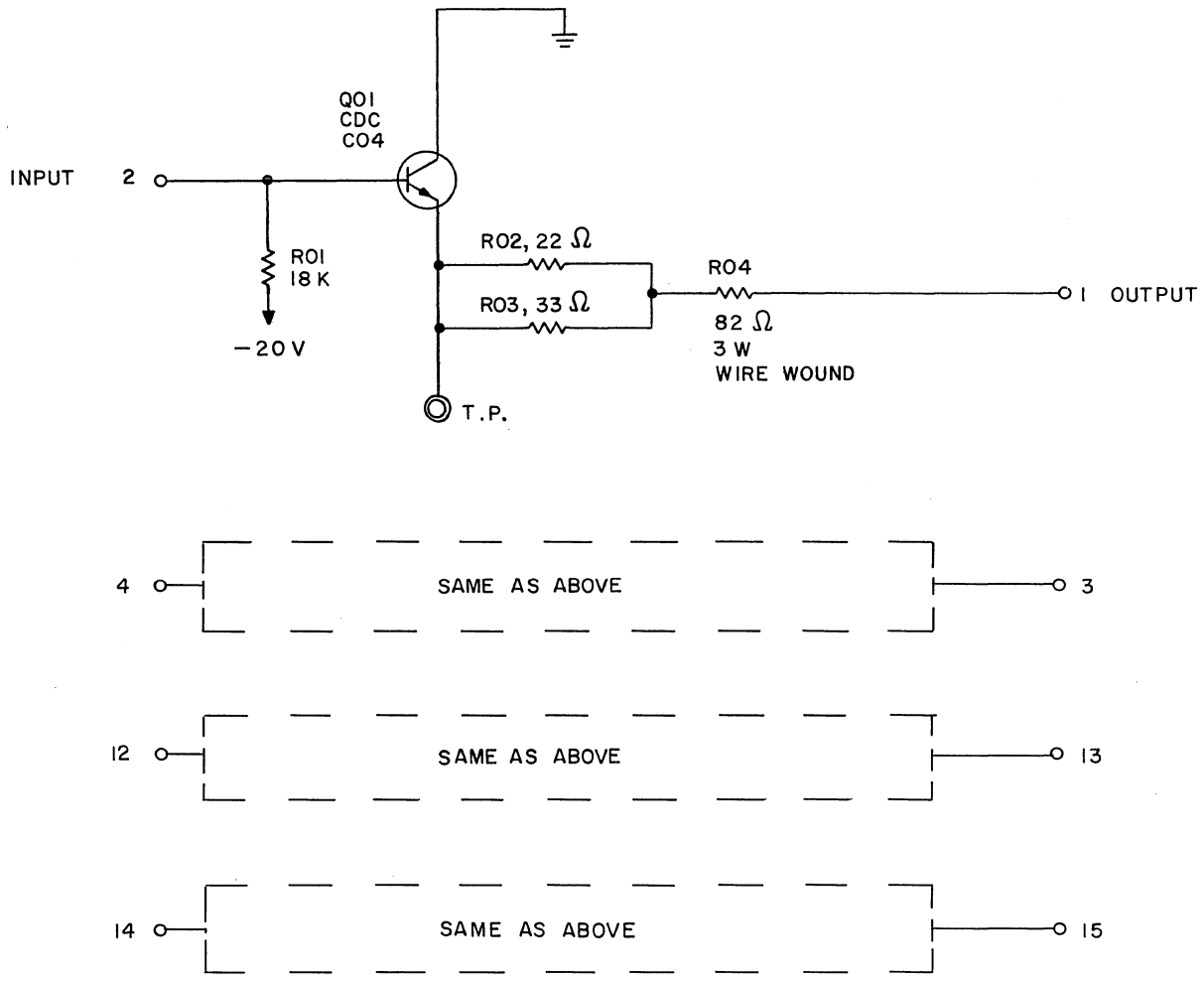
OPERATION

Inputs to the circuit are provided by a brush at the card reading station, and the signal levels are open circuit and approximately ground. The ground signal results when a hole in the punched card allows the brush to touch a metallic roller which is at approximately ground potential. If a hole is not present, the insulating effect of the card produces an open circuit.

The metallic roller at the reading station is held at approximately ground potential by a Relay Driver card type C84. The roller is thus at a potential equal to the saturation voltage of the Relay Driver transistor which is approximately -0.6v.

An open circuit input allows the base voltage of Q01 to rise toward -20v. The emitter of Q01 is also at -20v, since it connects through the memory drive line to a -20v supply. This puts Q01 in the cut off condition, and memory drive current is prevented from flowing.

An input of approximately ground allows Q01 to switch on and conduct heavily. The voltage applied to the drive line is -20v, less the drop across the Relay Driver transistor and the base-emitter voltage of Q01, and is approximately -18.5v. The memory drive current is also the emitter current of Q01 and is limited by resistors R02, R03, and R04 to approximately 200 ma. The base current of Q01 is equal to the 200 ma emitter current divided by h_{FE} and is approximately 8.5 ma. The brush at the reading station is therefore required to carry the base current of Q01 plus enough additional current so that the voltage drop across R01 is approximately 19.4v; a total of approximately 9.5 ma.



NOTES:

1. INPUT SIGNAL LEVELS ARE:
   A. OPEN CIRCUIT, Q01 CUTS OFF.
   B. ≈ GROUND, Q01 CONDUCTS HEAVILY.

I/O Emitter Follower C90

DIGIT DRIVER
Card Type HA14

FUNCTION

The function of this circuit is to provide bi-directional 400 ma drive currents through a digit winding in a word organized memory. The two ends of the winding connect to pins 14 and 15. Pin 13 connects through a power resistor to +20 v.

The circuits are activated by -1.1v "0" inputs. Each circuit has a 2-way AND input and pin 12 acts as a gate. The receipt of -1.1 v "0" inputs at pins 10 and 12 will cause pin 15 to go positive and 14 to go negative; with "0" inputs at pins 11 and 12, pin 14 will go positive and 15 will go negative.

OPERATION

The filter network consisting of L01, L02, and C04-C08 performs a decoupling function. The current carried by pins 14 and 15 is of the order of 400 ma. The decoupling network prevents voltage surges and fluctuations on the circuit input which could result from heavy current switching at the output.

The two input circuits are identical, as shown in the accompanying diagram. The components mentioned here are those associated with test point A.

The input of each circuit is a 2-way AND, and -1.1 v "0" inputs allow transistor Q01 to conduct. A level-shifting action is provided by the 4.1 v zener diode CR05. A -5.8 v "1" input at either pin 10 or 12 will result in approximately -1.2 v at the base of Q01, so that Q01 is cut off. With both inputs at the -1.1 v "0" level, zener diode CR05 will bias the base of Q01 well into the conduction region.

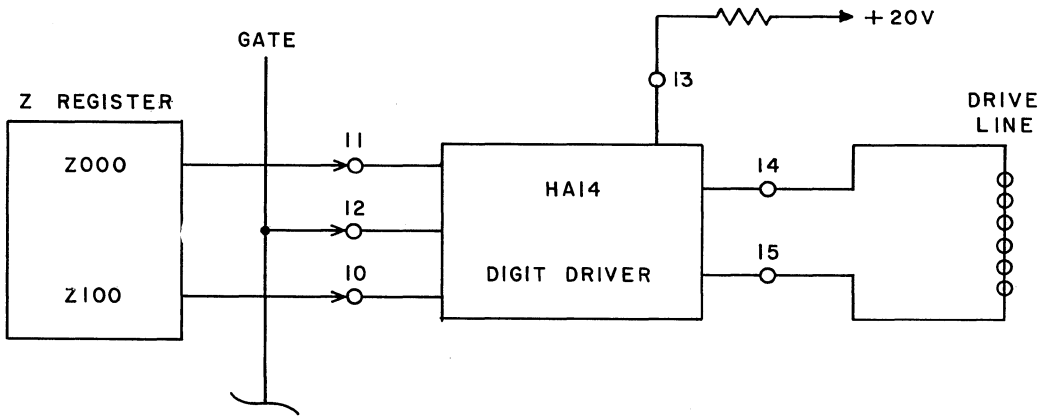
Transistor Q01 in its conduction state allows current flow to increase through the primary winding of transformer T1. In this state, current through the 16-turn primary of T1 will be approximately 2 ma. This results in about 8 ma in each of the 4-turn secondaries and provides forward drive current for Q03 and Q06, causing them to switch.

Transistors Q03 and Q06 in their conduction state cause pin 15 to go positive and 14 to go negative. The 100-ohm resistor R15 provides a blocking action, causing practically all of the current from Q03 to flow out of pin 15, through the 2-ohm drive line resistance, back into pin 14, and through Q06 to -20 v.

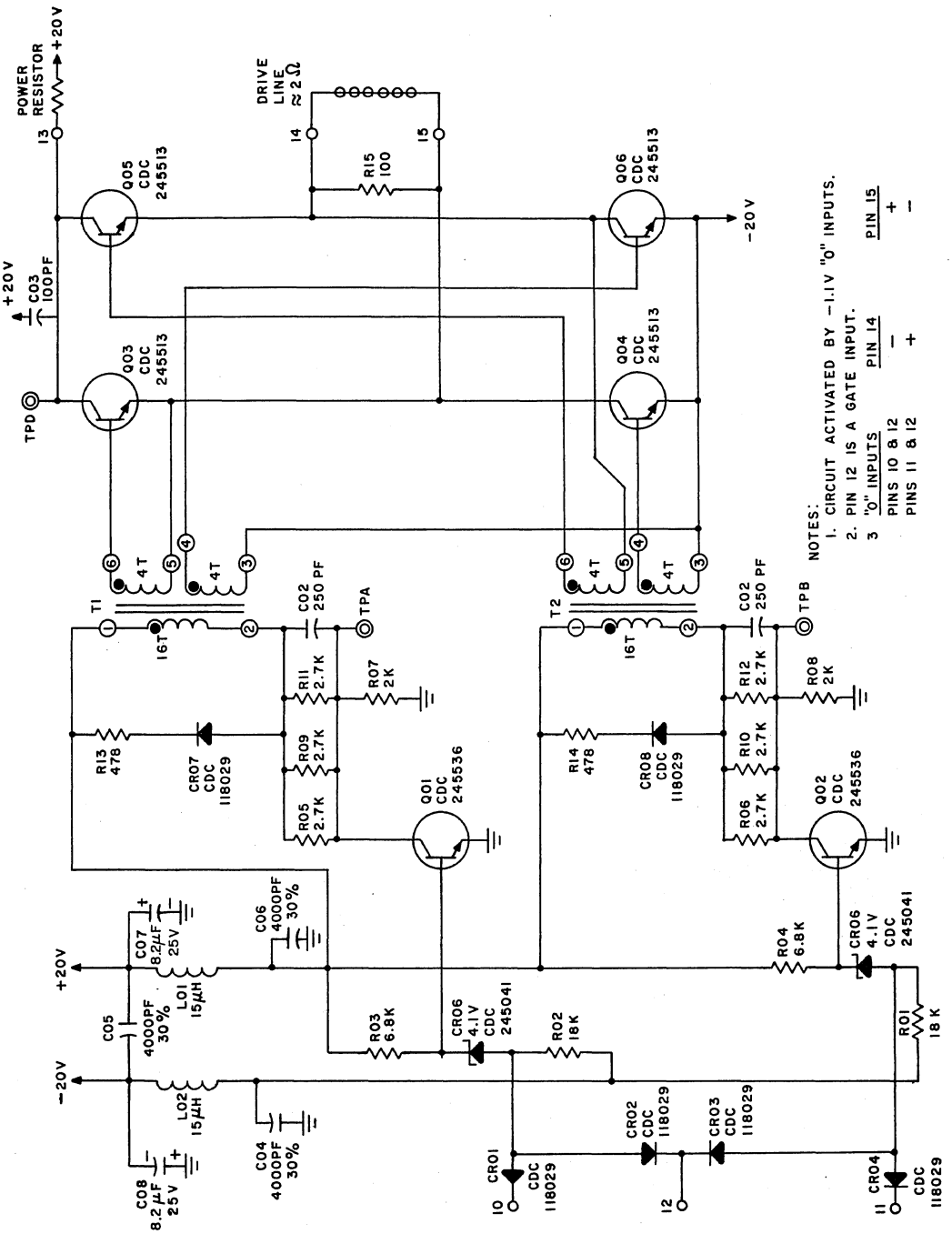
(Note that with "0" inputs at pins 11 and 12, transistors Q04 and Q05 will conduct producing an output current of the opposite polarity.)

Capacitor C03 performs a speed-up function, providing an initial surge of high current when the transistors switch on. This gives a sharper leading edge to the output waveform.

The connection of R13 and CR07 provides a clamp for the transformer primary. This dissipates any inductive transient which could result when Q01 switches off.



TYPICAL APPLICATION



Digit Driver HA14

DIGIT COMPENSATOR
Card Type HA15

FUNCTION

This circuit operates in conjunction with the drive hardware of a word-organized memory. Its purpose is to provide a constant load for the -20v power supply by driving a 400 ma current through a load resistor during times when no drive lines are energized.

The load resistors are external to the circuits on the card and are connected in series from pins 1 and 15 to -20v. Current is allowed to flow whenever at least one of the inputs to the respective circuit is a -5.8v "1".

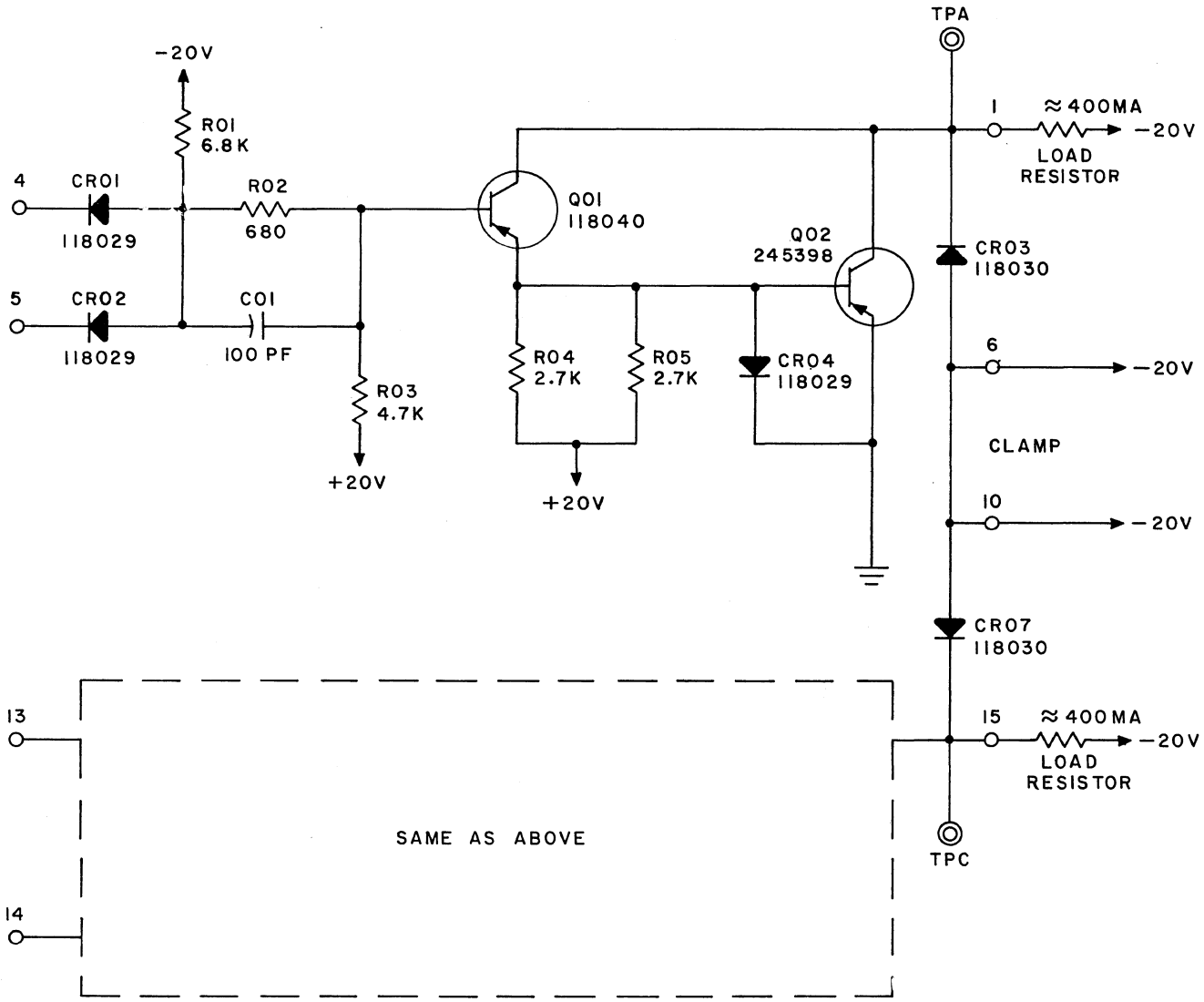
OPERATION

Each circuit has two OR inputs, and a -5.8v "1" on either input will cause the circuit to conduct. If both inputs are left open, the base of Q01 will rise toward approximately +4.5v and the circuit will be cut off.

A -1.1v "0" on both input will hold the circuit in the OFF state. This results in approximately +2v at the base of Q01. The emitter of Q01 and the base of Q02 are held at +0.5v by the forward drop across CR04, so that both transistors are cut off.

A -5.8v "1" on either input holds the base of Q01 at approximately -2v. The base drive for Q02 is taken from the emitter of Q01. A negative-going input to Q01 causes it emitter current to increase. Initially, this current is supplied from the +20v source through R04 and R05. However, the voltage drop across R04 and R05 is clamped at about 0.3v by the base-emitter junction drop of Q02. Resistors R04 and R05 are therefore able to supply only about 0.22 ma, and a further increase in the emitter current of Q01 will draw drive current through Q02, causing it to switch to its conduction state.

Diodes CR03 and CR07 provide clamps for the collector voltage of the transistors. This clamp connection should be used when driving an inductive load.



NOTES: 1. EACH CIRCUIT HAS TWO "OR" INPUTS.
2. TRANSISTORS CONDUCT WHEN EITHER INPUT RECEIVES A −5.8V "1".

SENSE AMPLIFIER
Card Type HA16

FUNCTION

This card is designed for use as a sense amplifier in a word-organized memory. It consists of a differential amplifier driving a discriminator with a strobe input. Pins 4 and 5 connect to the two ends of the sense line, pin 15 provides the output, and pin 12 is the input for the -1.1v "0" strobe pulse. In the quiescent state, the output at pin 15 is about +0.3v which is interpreted as a logical "0".

The polarity of the differential 0.1 v input signal determines whether the output at pin 15 will be "1" or "0". If pin 4 goes positive with respect to pin 5, the strobed output at pin 15 will be a "1" of approximately -5.8 v. If pin 4 goes negative with respect to pin 5, the output at pin 15 remains at a +0.3 v."0".

The strobe input at pin 12 is a -1.1 v "0" pulse. This input must be present in order to allow the circuit to produce a -5.8 v "1" output. If pin 12 is held at -5.8 v "1", the output at pin 15 will be held at +0.3 v "0".

OPERATION

Since this circuit is a direct coupled amplifier, regulated voltages must be used. A connection to -18 volts is made at pin 2 and a connection to -6.8 v is made at pin 13. The -18 v may be obtained from an 18-volt zener diode and a 4.5-ohm resistor in series to -20 v, and the -6.8 v may be obtained using a 6.8-volt zener diode and a 30-ohm resistor in series to -20 v.

The 200-ohm resistors R01 and R04 terminate the sense line, while R02 and R03 provide bias for Q01 and Q02. The 100 mh inductor in the emitter circuit of Q01 and Q02 greatly increases the emitter impedance and improves the common mode characteristics.

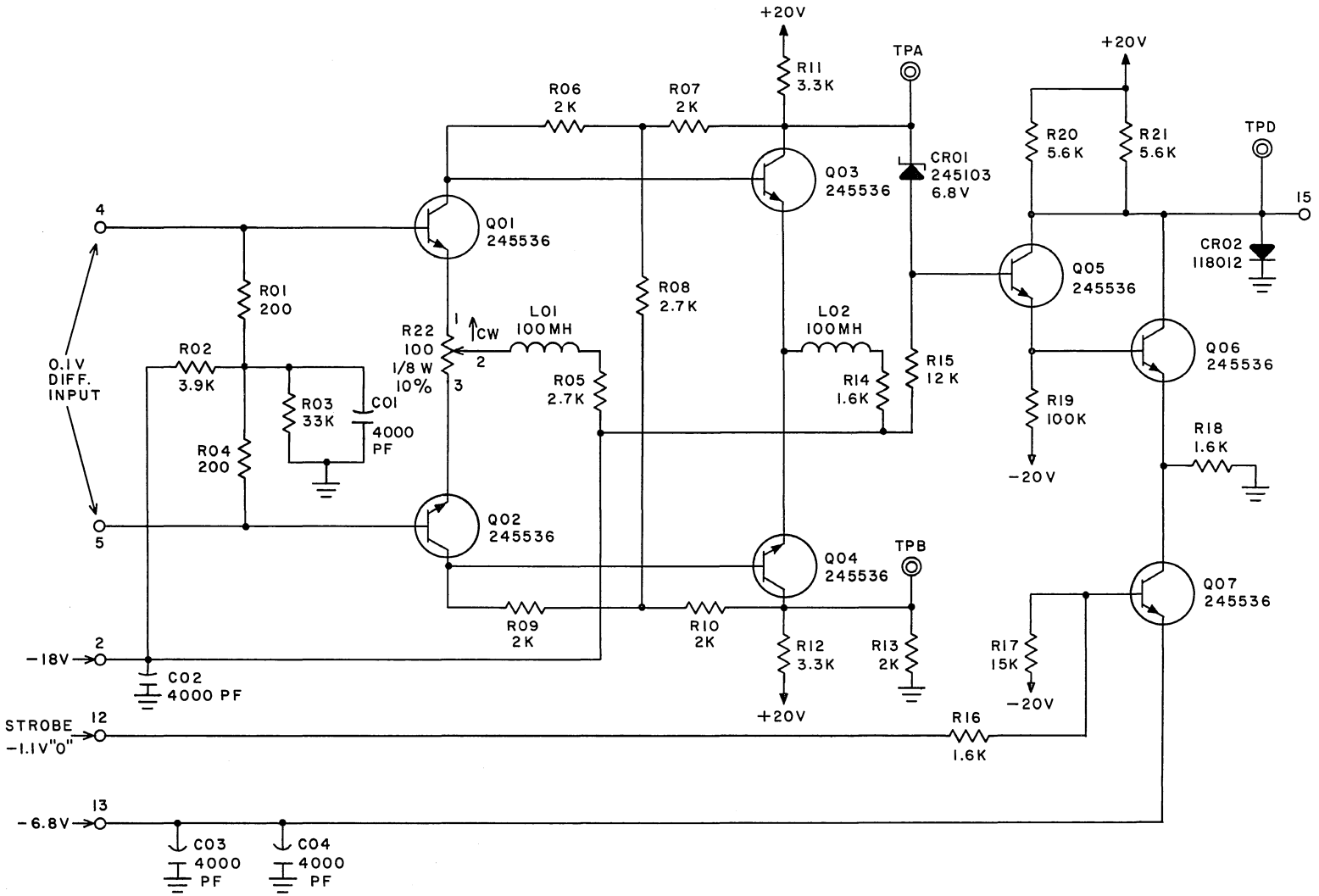
The 2K resistors in the collector circuits of the amplifier provide negative feedback. A portion of this is nullified by the positive feedback connection of R08.

The load resistances of Q01 and Q02 consist of the two 2K resistors plus the 3.3 K resistor. The load of Q03 is the 3.3 K resistor in parallel with the output circuit, while the load of Q04 is the 3.3 K resistor and the 2 K resistor in parallel.

Level translation is performed by the 6.8v zener diode CR01, which drives the input of the Darlington amplifier consisting of Q05 and Q06.

Transistors Q06 and Q07 perform an AND function. If both conduct at the same time, the -6.8v at pin 13 will produce approximately -5.8v at pin 15, allowing for voltage drop across the transistors. Transistor Q06 is driven to its conduction state by a differential input which causes pin 4 to become positive with respect to pin 5. Transistor Q07 is driven to conduction by a -1.1v "0" strobe pulse at pin 13.

If the AND condition of simultaneous conduction by Q06 and Q07 is not met, the voltage at pin 15 will be a logical "0" at approximately +0.3v. This is produced by the forward drop across CR02.



NOTE:

THE POLARITY OF THE DIFFERENTIAL INPUT DETERMINES WHETHER THE STROBED OUTPUT AT PIN 15 IS "1" OR "0", AS FOLLOWS.

PIN 4	PIN 5	PIN 15
+	−	"1", −5.8V
−	+	"0", +0.3V

SENSE AMPLIFIER
Card Type HA18

FUNCTION

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "1" output at pin 15.

The circuit may be conveniently divided into two sections; a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -1.6v. The output of -1.6v represents a logical "0" which changes to a logical "1" when a core switches. The following logic card interprets any signal more negative than -3v as a logical "1", however the circuit output approaches -14.6v when a core switches.

AMPLIFIER

The differential voltage amplifier portion of the circuit is similar to card type C06, which is discussed elsewhere. However, the overall gain is approximately 100 so that the nominal 30 mv induced in the sense winding by the switching of a core results in approximately 3v at the diode bridge.

DISCRIMINATOR

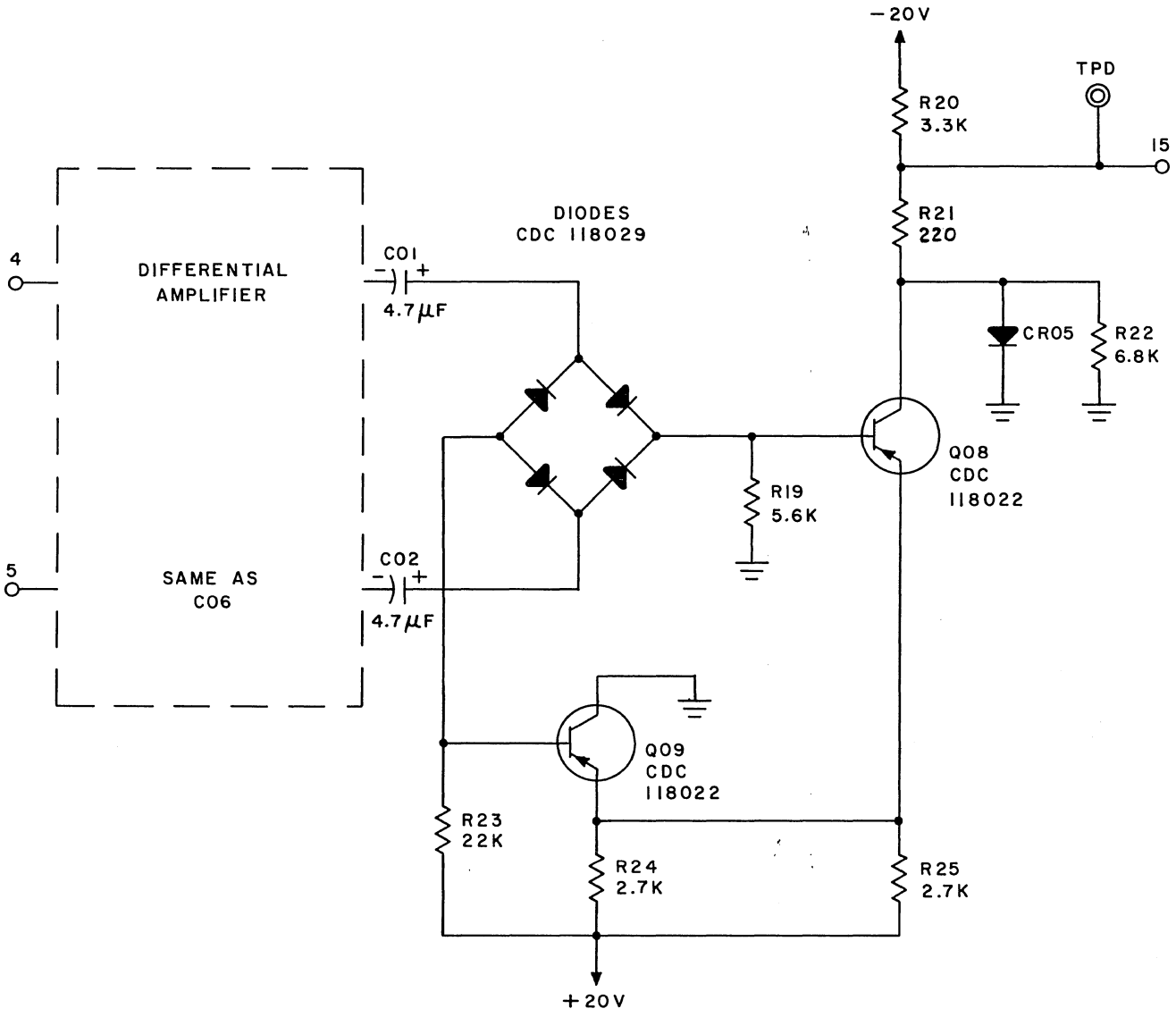
The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The output of the discriminator is from pin 15 and is approximately -1.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -14.6v which is interpreted as a logical "1".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state, a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q09 is held at around 1.2v higher positive potential than the base of Q08. Transistor Q08 thus conducts quite heavily while Q09

conducts very little. Under these conditions the output at pin 15 is around -1.6 v, due to the voltage dividing action of R20, R21, and the -20 v source. Diode CR05 is in a state of heavy forward conduction, being forward-biased by the +20 v source through R25 and Q08. In this state, the anode of CR05 is at approximately +0.6 v.

The diode bridge rectifies the potential across it, so an input of either polarity results in a positive input to the base of Q08 and a negative input to the base of Q09. This has the effect of causing Q09 to conduct heavily while Q08, in turn, conducts very little.

The output of -14.6 v is established by the voltage-divider action of R20, R21, and R22. Transistor Q09 provides a low impedance path to ground, so that the emitter of Q08 cannot rise to a high positive potential.



NOTE: PRODUCES "1" OUTPUT WHEN CORE SWITCHES.

Sense Amplifier HA18

MEMORY DRIVER

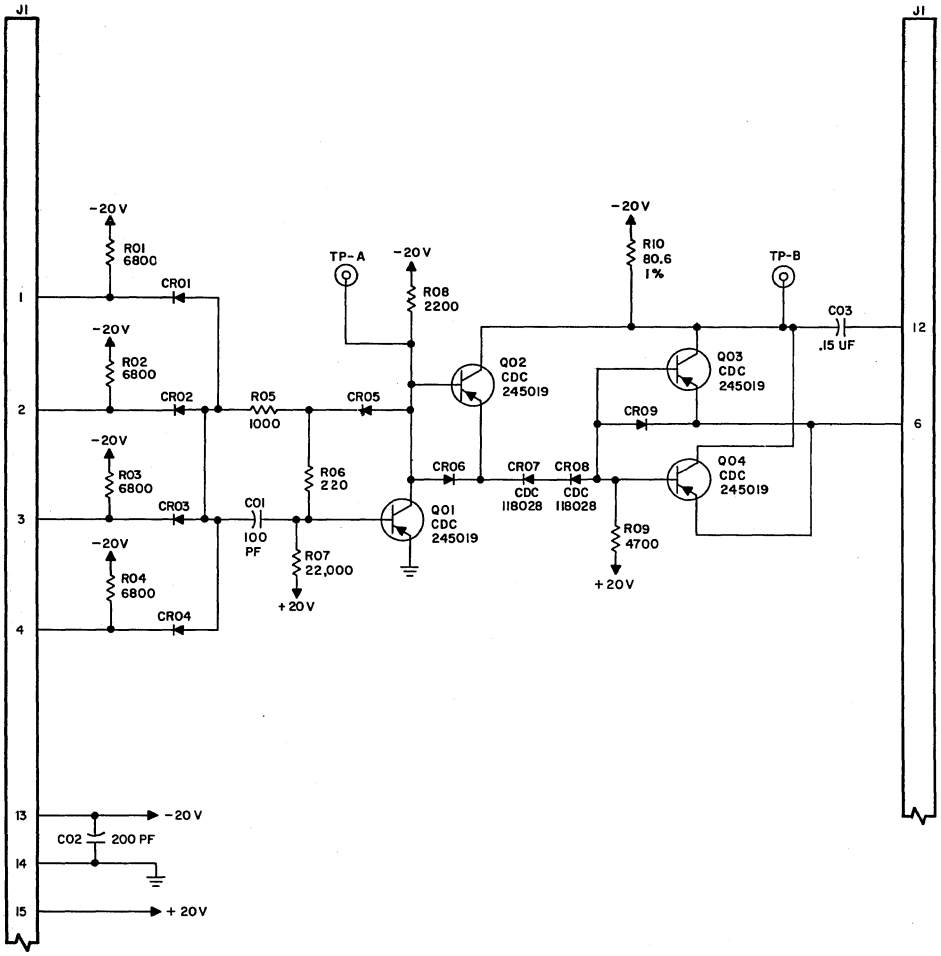
Card Type P51

Card P51 provides either 200 ma half-current or 400 ma full-current (with pin 12 grounded) pulses to the wires threading the magnetic cores in the memory unit by enabling transistors Q03 and Q04, so positive current may flow from pin 6 to -20v.

This card is controlled by logic inputs on pins 1, 2, 3, and 4. Inputs are either -3v, logical "1", or -0.5v, logical "0". Transistors Q03 and Q04 are cut off if any of the card inputs receives a logical "1" and conduct only if all inputs are a logical "0".

Assume that input pins 2, 3, and 4 are grounded ("0") and that a -3v signal appears on the collector of the transistor on the preceding logic card, which is connected to input pin 1 of the P51 card. This level is sufficiently negative to cause the output diode on the logic card to cut off and permit the input diode on pin 1 of the P51 card to conduct. This biases the emitter-base junction of Q01 in the forward direction. With Q01 in a conduction state, its collector goes to approximately ground potential and Q02 cuts off. The base potential of Q03 and Q04 is then raised toward +20v so that they are also cut off.

If the collector on the preceding logic card were at -0.5v, its output diode would conduct and hold the input of the P51 card at about -1.0v. This is sufficiently positive to bias the emitter-base junction of Q01 in the reverse direction. Q01 would then cease to conduct and its collector would go negative, causing Q02 to conduct. This places a negative potential on the bases of Q03 and Q04, causing them to conduct, and permitting current to flow from pin 6 to -20v. Pin 12 is grounded when the card is used as a read driver, so that capacitor C03 can supply an initial surge of current.



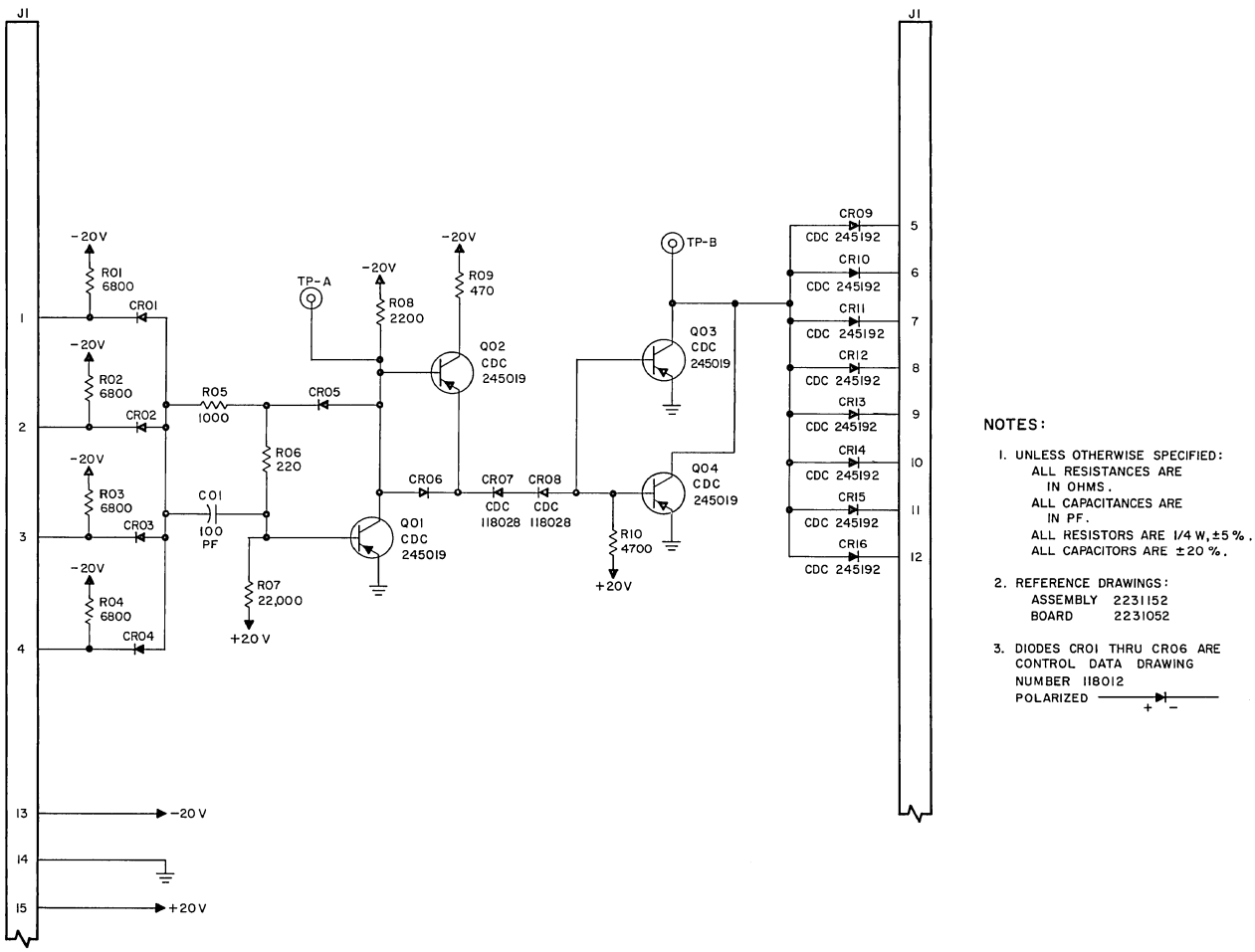
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231151
   BOARD 2231051
3. DIODES CR01 THRU CR06 AND CR09 ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED

Memory Driver P51A

MEMORY DIVERTER
Card Type P52

Card P52 simultaneously grounds eight of the wires threading the magnetic cores in the memory unit to provide complete circuit paths for the read and half-write current. Transistors Q03 and Q04 conduct when all inputs are "0".



NOTES:

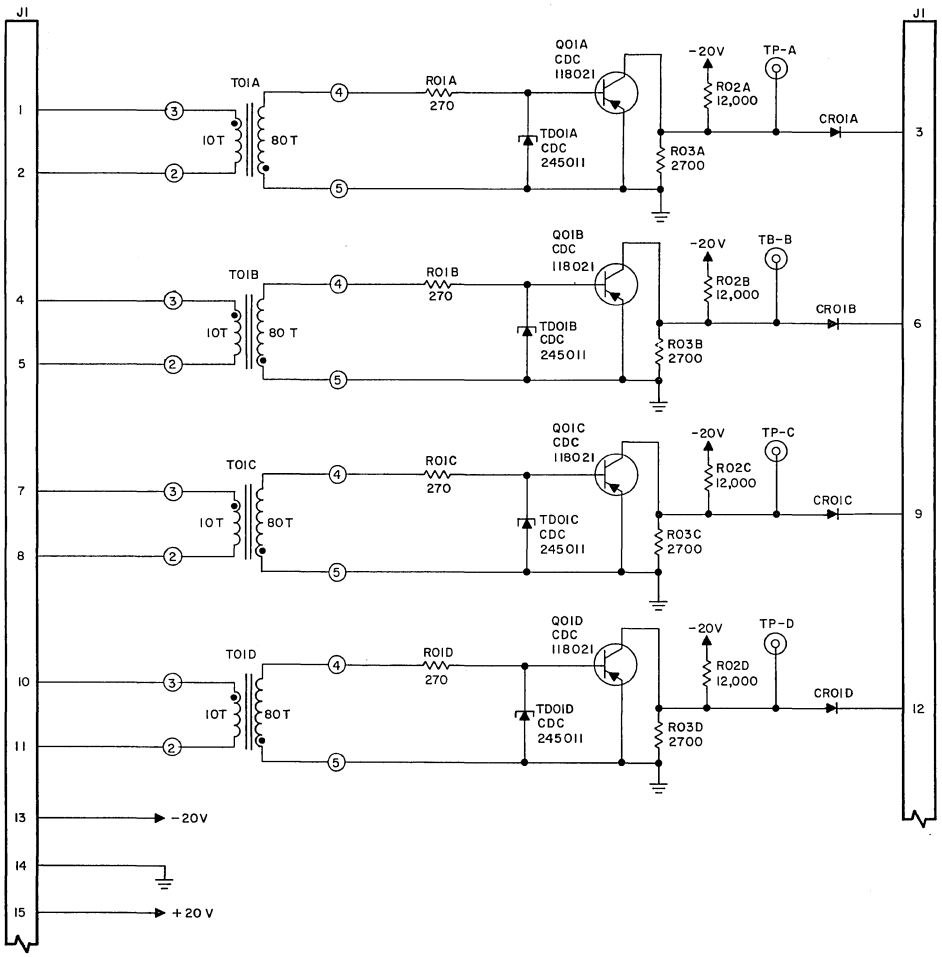
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231152
   BOARD 2231052
3. DIODES CR01 THRU CR06 ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED + –

Memory Diverter P52

SENSE AMPLIFIER
Card Type P56

Card P56 detects, amplifies, and shapes the pulses induced in a sense winding when the state of a magnetic core is changed by a read current pulse. The card contains four identical amplifiers, A, B, C, and D. Each amplifier consists of a grounded emitter PNP transistor with a tunnel diode connected from the base to ground, to reject noise below a predetermined threshold and square the pulse. The base of the transistor is driven by a 1 : 8 step-up transformer in which the primary winding is connected in series with the sense wire threading one of the rows of magnetic memory cores.

Example: Assume that an input is being received and terminal 4 of the transformer is starting to go negative. This causes current to flow through the 270 ohm resistor R01 and through the tunnel diode TD01 to ground. Initially the card has a -3v output, since the tunnel diode in its low voltage state does not permit transistor Q01 to conduct. When tunnel diode current has increased to 1 ma, it switches to its high voltage state. Q01 conducts and the card output goes to -0.5v, where it remains as long as TD01 is in its high voltage state. When the input current decreases to 0.1 ma, the tunnel diode switches back to its low voltage state, Q01 is cut off, and the card output returns to -3v. In this manner, a square wave output is produced and noise signals insufficient to switch the tunnel diode are rejected.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 2231156
   BOARD 2231056

3. DIODES CR01A THRU CR01D ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED

CHAPTER 4. I/O CARDS

Output Cards (L)	60, 60A, 62, 67
Input Cards (M)	61, 87
Output	79A
Transmitter and Receiver	C62B, C61
Modified M--- Input	C75, C75B
Modified L--- Output	C76, C76A
Long Line Driver and Receiver	C98, H26
Line Driver	E12
Line Receiver	E13
Line Driver	E15
Line Receiver	E61A
Line Driver	E62B, E67A
Receiver	H11A
Transmitter	H19
Level Translator	H31
Line Driver	H32A
Transmitter (1000-foot)	H37, H43
Transmitter and Receiver	P14C, P16A

OUTPUT CARDS (L)

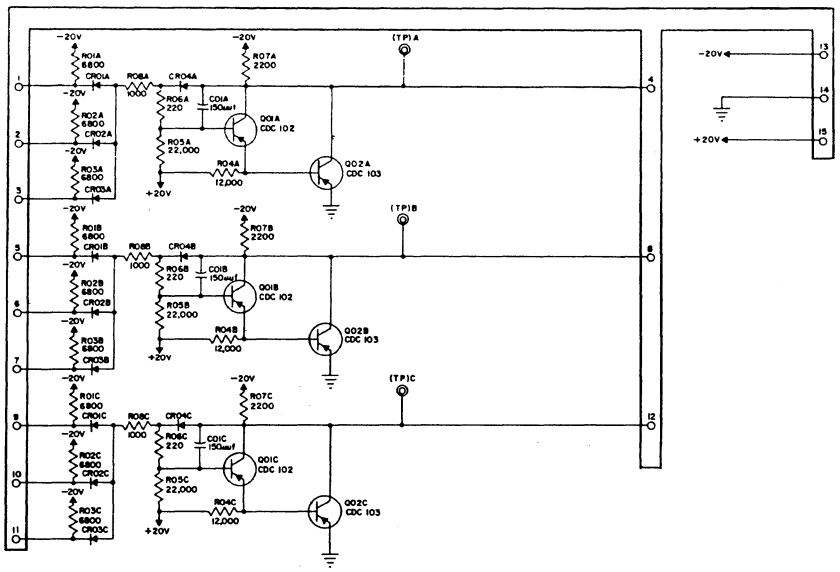
Card Types 60, 60A, 62 and 67

The circuits contained on these cards adapt the relatively low level 1604 logic voltages to the relatively high level voltages necessary for transmission over a 1604-type I/O cable. Each card contains three separate circuits designated A, B, and C.

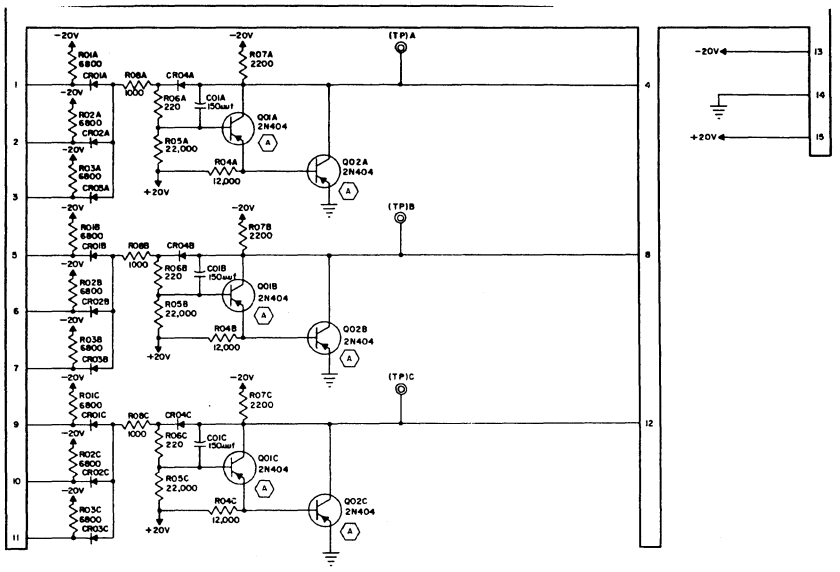
These circuits are similar to 1604-type inverters, in that they contain a common emitter transistor circuit producing a 180^{o} electrical phase shift

The switching speed of the circuit is limited by the 150 uuf of Miller feedback capacitance, and the feedback network allows a -0.5v "0" input to drive the circuit to cutoff. Input and output levels are as follows:

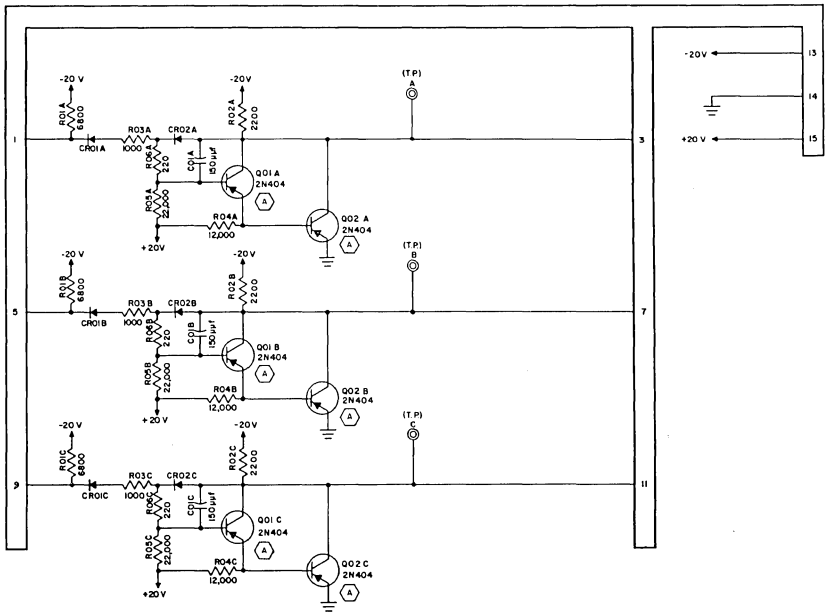
Input	Output
-3v "1"	-0.5v
-0.5v "0"	-18v



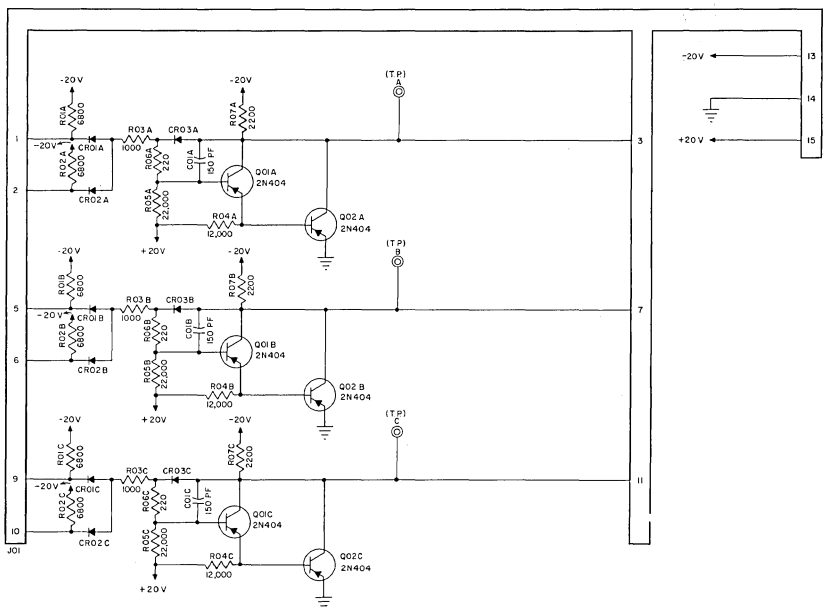
Output 60



Output 60A


-20 V
R01A 6800
CR01A
R03A 1000
CR02A
R02A 2200
C01A 150 µµf
R06A 220
R05A 22,000
+20V
R04A 12,000
Q01A 2N404
Q02A 2N404
(T.P.) A
R01B 6800
CR01B
R03B 1000
CR02B
R02B 2200
C01B 150 µµf
R06B 220
R05B 22,000
R04B 12,000
Q01B 2N404
Q02B 2N404
(T.P.) B
R01C 6800
CR01C
R03C 1000
CR02C
R02C 2200
C01C 150 µµf
R06C 220
R05C 22,000
R04C 12,000
Q01C 2N404
Q02C 2N404
(T.P.) C
-20V
+20V
1
3
5
7
9
11
13
14
15

62


R01A 6800
-20V
CR01A
R02A 6800
CR02A
R03A 1000
R07A 2200
C01A 150 PF
R06A 220
R05A 22,000
+20V
R04A 12,000
Q01A 2N404
Q02A 2N404
(T.P.) A
R01B 6800
CR01B
R02B 6800
CR02B
R03B 1000
R07B 2200
C01B 150 PF
R06B 220
R05B 22,000
R04B 12,000
Q01B 2N404
Q02B 2N404
(T.P.) B
R01C 6800
CR01C
R02C 6800
CR02C
R03C 1000
R07C 2200
C01C 150 PF
R06C 220
R05C 22,000
R04C 12,000
Q01C 2N404
Q02C 2N404
(T.P.) C
J01
1
2
3
5
6
7
9
10
11
13
14
15

Output 67

INPUT CARDS (M)

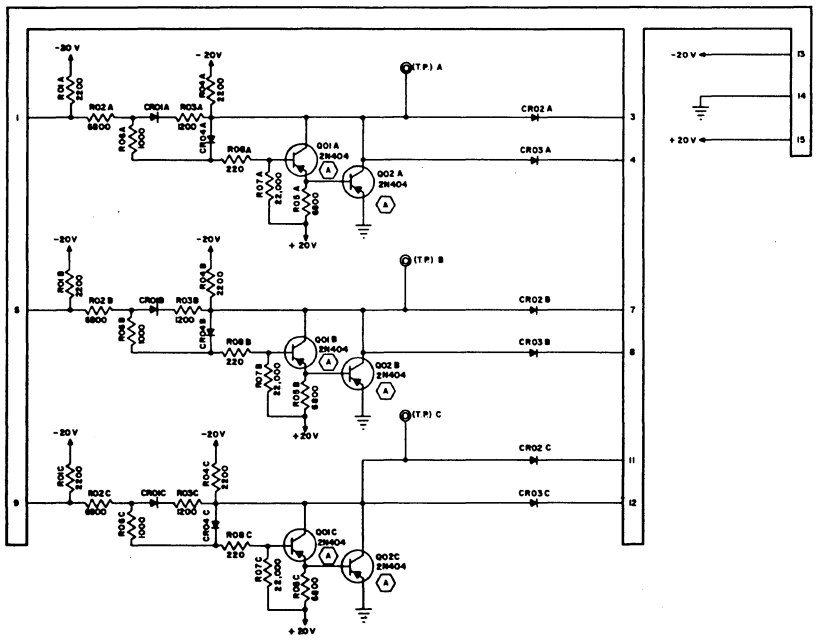
Card Types 61 and 87

The circuits contained on these cards adapt relatively high line voltage used for 1604-type cable transmission to the relatively low level voltage used for logical functions. Each card contains three separate circuits designated A, B, and C.

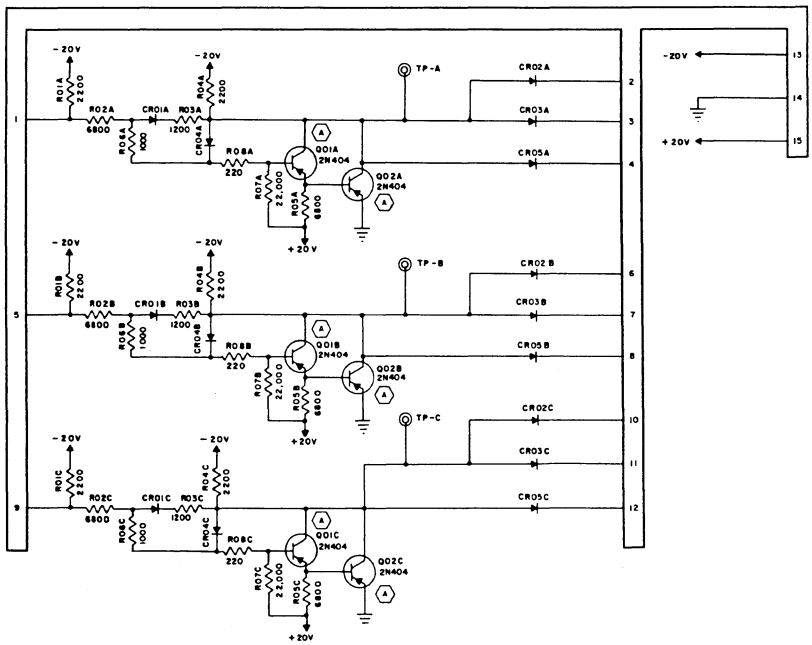
These circuits are similar to the 1604-type inverter, except that the modified input allows the circuit to accept higher voltage signals.

Inputs and outputs are as follows:

Input	Output
-0.5v (or ground)	-3v "1"
-18v (or open)	-0.5v "0"



Input 61

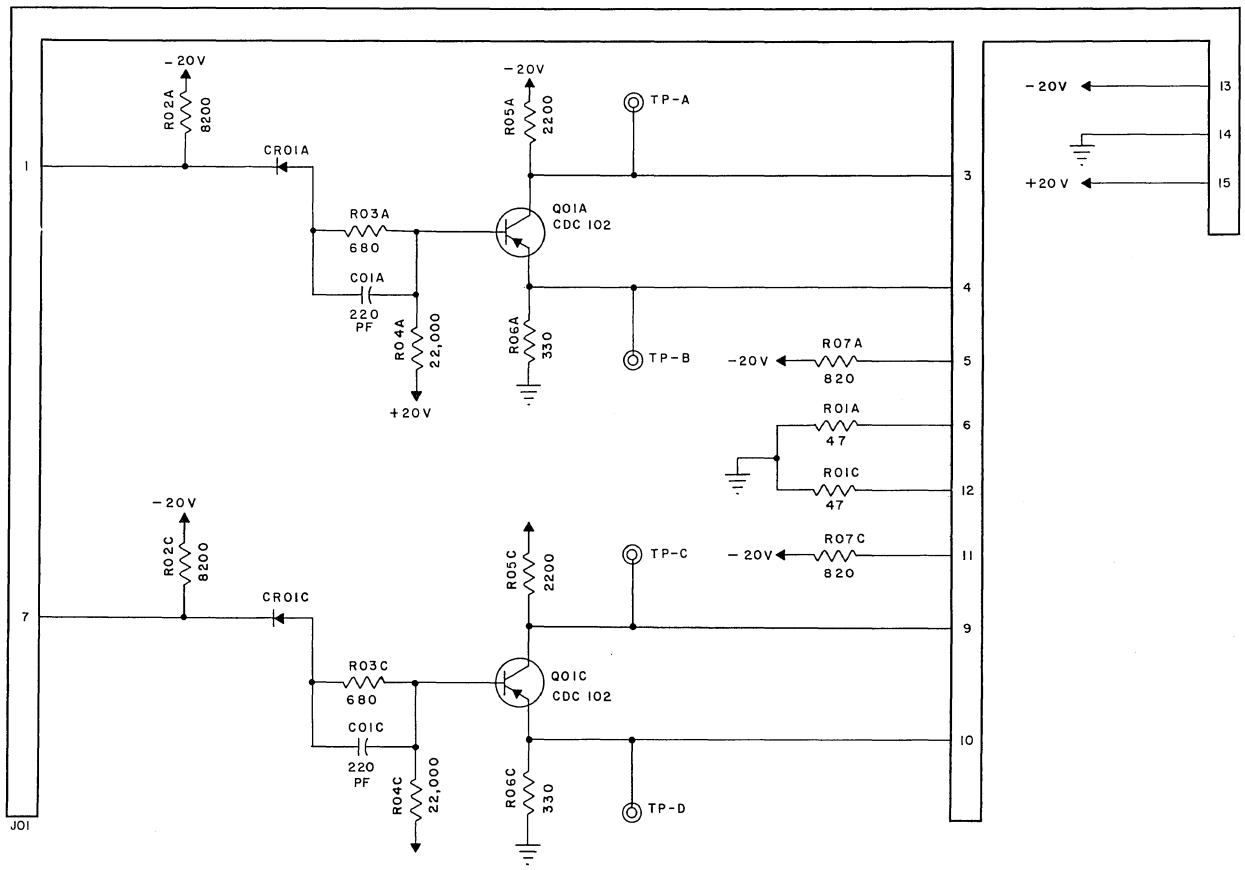


Input 87

OUTPUT

Card Type 79A

The function of the circuits on this card is to enable 1604-type logic to interface with IBM equipment. The card contains a biasing network, and both "P" and "N" signal levels may be produced as shown in the accompanying diagram.



Output 79A

TRANSMITTER AND RECEIVER
Card Types C62B and C61

GENERAL

The circuit configuration shown on page 4-C62-3 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v, respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter satisfactorily drives 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v line-to-line, and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

When the 3-way AND input to the transmitter is disabled by a "0", transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03. With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction to the 5 ma bias current; thus the net current flow is 5 ma in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

TRANSMITTER, Card Type C62

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown on page 4-C62-3.

The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction of Q01 to be forward biased, fully turning on Q01. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the AND input is satisfied, the base of Q01 is held at approximately -5 volts. This reverse biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

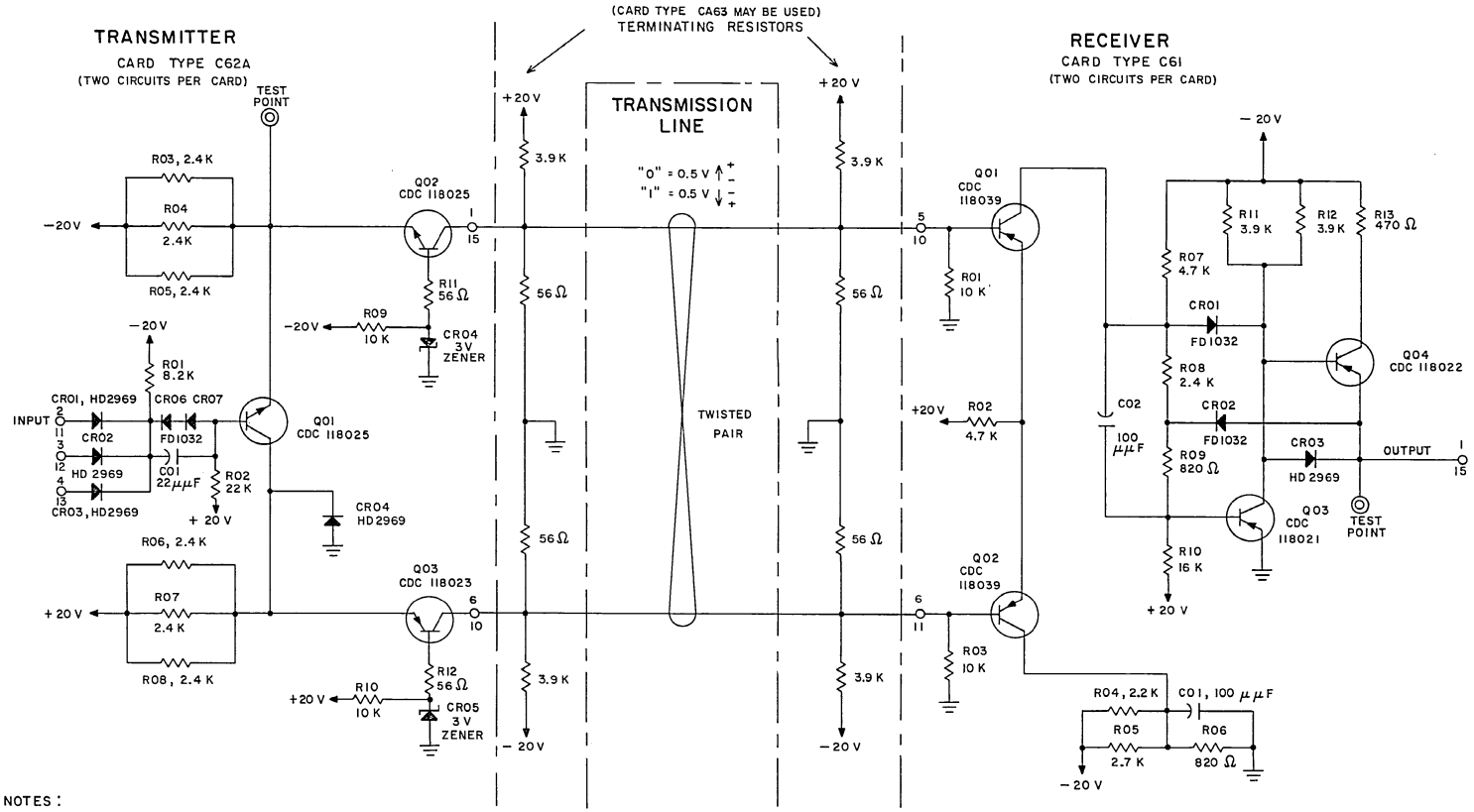
The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage is allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter operates satisfactorily with up to 3 volts of random noise on the transmission line.

The transmitter must be connected to the line in only one polarity, as shown on page 4-C62-3. This is necessary to provide current through the terminating resistors in a direction opposite the bias current.

TRANSMISSION LINE

A terminated balanced twisted-pair transmission line carries digital information from the transmitter to the receiver. This information is in the form of line-to-line

Transmitter and Receiver C62 and C61



NOTES:

1. THE CONNECTION SHOWN DOES NOT PROVIDE A LOGICAL INVERSION; A "1" INPUT RESULTS IN A "1" OUTPUT.
2. TO PRODUCE AN OVER-ALL LOGICAL INVERSION, THE TRANSMISSION LINE CONNECTION AT THE RECEIVER WOULD BE REVERSED.
3. THE TRANSMISSION LINE CONNECTION AT THE TRANSMITTER CAN NOT BE REVERSED, BECAUSE OF VOLTAGE POLARITIES.

differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

The line is biased at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v line-to-line.

The length of a transmission line may be up to 200 feet, with as many as 20 transmitters and 20 receivers placed in parallel along its length.

Bit rates of 8 mc or greater are possible on a 200 foot line. Low bit rates over longer distances are limited by the d-c line losses; however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50 percent to 60 percent of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

RECEIVER, Card Type C61

The printed circuit card contains two identical receiver circuits designated A and B. A Typical example is presented on page 4-C62-3. This portion of the circuit connected to the collector of Q01 is similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input conducts more heavily while the one receiving the positive input conducts less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output is a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown on page 4-C62-3 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

GROUND RULES

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.
4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter can not be reversed, due to the polarity of the line bias voltage.

9. Up to 20 transmitters and 20 receivers may be connected along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.
12. No more than 8 transmitters should be driven by an inverter and no more than 7 should be driven by a flip-flop.

MODIFIED M^{---} INPUT
Card Types C75* and C75B

FUNCTION

This card contains two identical circuits. Its function is to enable the 3600 computer system to receive information from a 1604 type input/output cable. This is done by converting the "1" and "0" signal levels from -0.7v and -18v to -5.8v and -1.1v, respectively.

OPERATION

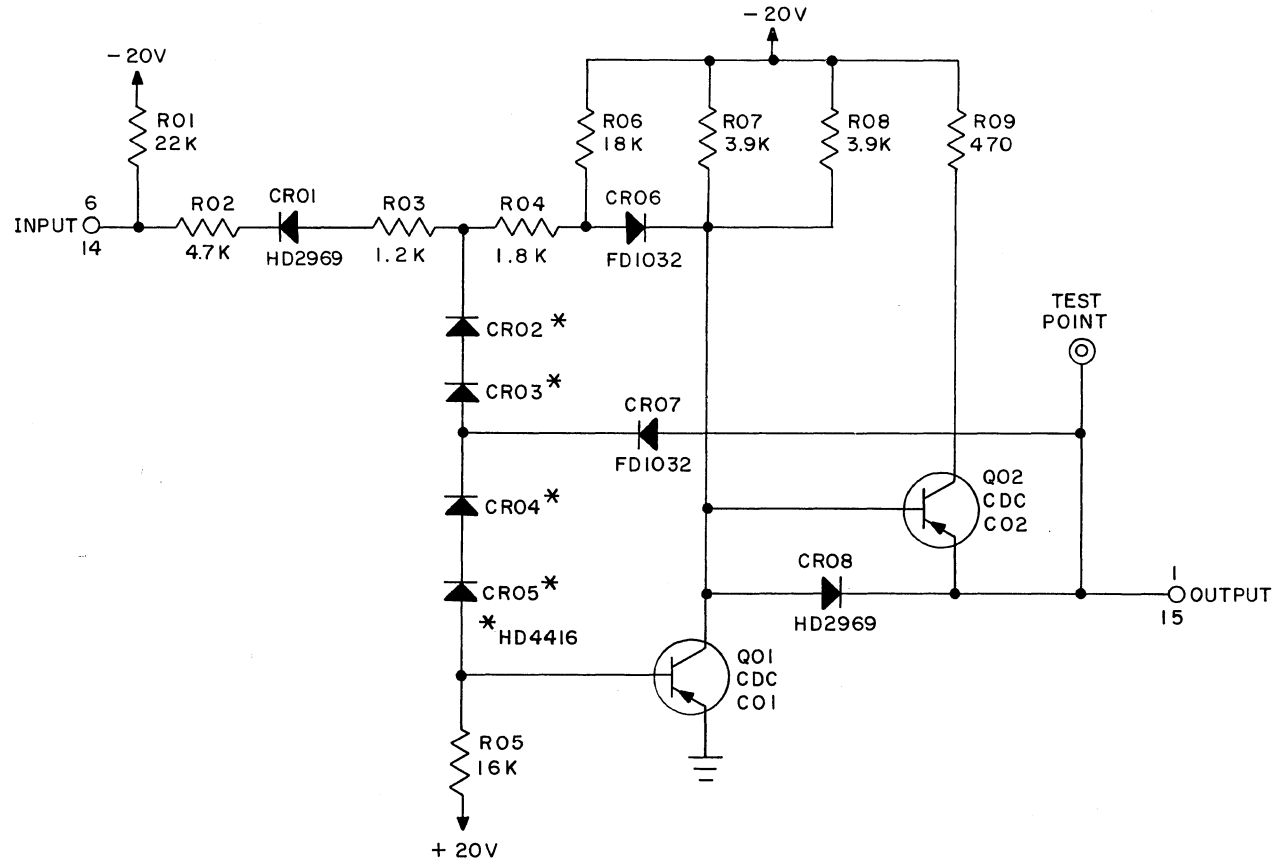
This circuit is essentially a single inverter having one OR input which has been modified by the deletion of the input coupling capacitor and the addition of resistors R01 and R02. These provide a voltage dividing effect, so a -18v input results in approximately -6v at the cathode of CR01. Similarly, a -0.7v input results in -0.7v at that point.

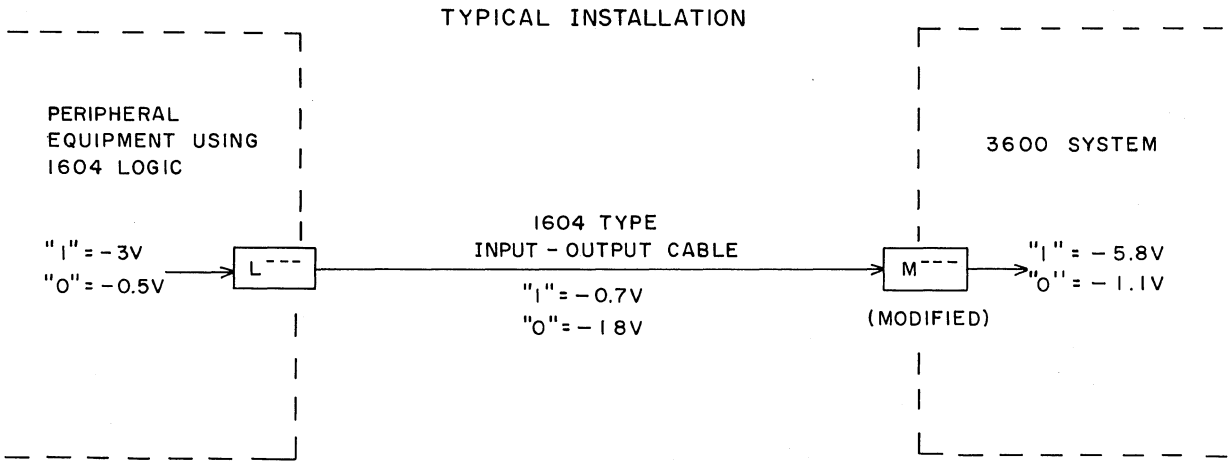
The remainder of the circuit is identical to a single inverter, which is discussed elsewhere.

The C75B is capable of driving 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.

The C75 is capable of driving 3 OR loads, 8 AND loads, or any combination resulting in 8 loads total, but not to exceed a total of 3 OR loads.

*All future cards of this type are C75B.





Modified M--- Input C75
(Two circuits per card)

MODIFIED L--- OUTPUT
Card Types C76* and C76A

GENERAL

This card contains two identical circuits. Its function is to enable the 3600 computer system to transmit information to peripheral equipment containing 1604 type logic. This is done by converting "1" and "0" levels from -5.8v and -1.1v to approximately -0.7v and -18v, which are the signal levels transmitted over a 1604 input/output cable. An M--- card in the peripheral equipment converts these signals to -3v and -0.5v, which respectively represent "1" and "0" in the 1604 type logic.

MODIFICATIONS

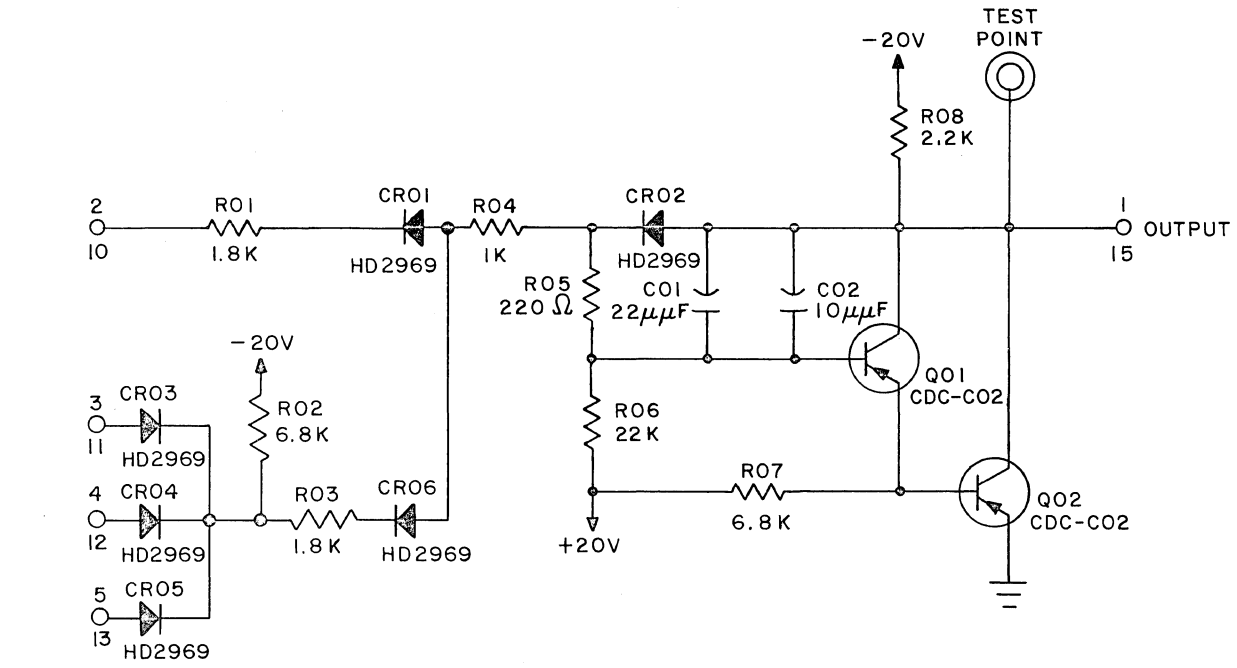
The modified L--- circuit shown on page 4-C76-2 is similar to one of the circuits contained on the 1604 card type 62. It has been modified through the use of CDC C02 transistors, reduction of the Miller feedback capacitance to 32 uuf, and the addition of 1.8 k resistors in the input networks. This enables the circuit to accept 3600 logic level inputs, and results in a switching time of approximately 0.8 usec.

OPERATION

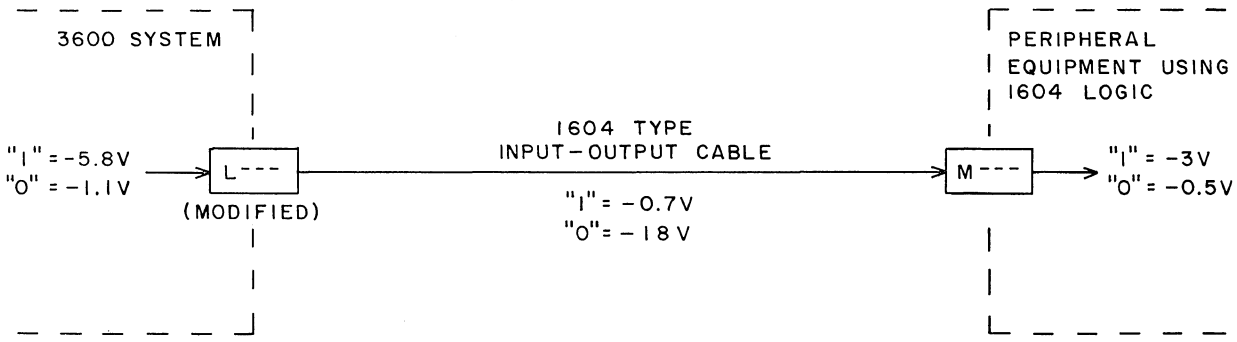
The circuit inputs are a three-way AND and an OR. The threshold level at the cathodes of CR01 and CR06 is approximately -1.5v. Thus as the circuit input becomes more negative, conduction increases from the +20v source through the resistor network. When the circuit input reaches the -3v level, the resulting voltage drop at the base of Q01 provides sufficient forward bias to the base-emitter junction of transistor Q01, so that it starts to switch to its conduction state.

The voltage at the base of Q01 is clamped at the sum of the base-emitter junction drops of Q01 and Q02, which is approximately -0.6v. Thus, as the input goes negative, the voltage across R06 is clamped at approximately 20.6v so that the current through it does not increase beyond approximately 0.9 ma. Therefore, as the input becomes more negative, turn-on current is drawn through transistors Q01 and Q02. This action begins when the input reaches approximately -3v, and as the input continues moving negative to the -5.8v "1" level, Q01 and Q02 switch to a state of heavy conduction.

*All future cards of this type are C76A.



TYPICAL INSTALLATION



Modified L--- Output C76
(Two circuits per card)

Transistor Q01 is connected as an emitter follower and Q02 as a grounded emitter stage. Thus when Q01 switches on, Q02 conducts heavily, providing a low impedance path from ground to the circuit output. The transistors are clamped out of saturation by diode CR02, but their collector potential is approximately -0.7v when both are in the conduction state.

A positive-going input causes transistor drive current to decrease, and when the input becomes more positive than -3v, transistor Q02 switches off, and the circuit output approaches -18v.

The switching time of the circuit is approximately 0.8 usec. The limiting factor is the 32 uuf of Miller feedback capacitance, which effectively slows the response of Q01.

LONG LINE DRIVER AND RECEIVER
Card Types CA98 and HA26

GENERAL

This circuit configuration performs high-speed transmission of digital information from one module to another over distances to 1000 feet. The driver card converts system logic levels into voltages suitable for output over an unbalanced transmission line. The receiver card converts the transmission line voltages into system logic levels capable of operating subsequent logical stages.

Transmitted carrier levels are -0.15v for a logic "1" and -2.1v for a logic "0". These levels are established by current flow through the termination networks. When the transmitter is turned off, the terminating network biases the line at 2.1v while turning on the long line driver forces the line to the -0.15v level.

LONG LINE DRIVER, Card Type CA98

The printed circuit card shown in the illustration contains two identical transmitter circuits which are designated A and B.

The logic input circuitry consists of a 3-way AND and an OR input. A -1.1v logic "0" results in the application of a positive potential to the base of Q01. Consequent emitter follower action causes a positive voltage to be coupled to the base of Q02. The resultant reverse bias condition at the emitter/base junction turns off Q02.

When Q02 is turned off, the transmission line will be biased at -2.1v. A -5.8v logic "1" signal causes a negative potential to be applied to the base of Q01. The resultant current increase in Q01 allows the base current of Q02 to increase to the saturation level. The saturation of Q02 forces the transmission line to the -0.15v level.

TRANSMISSION LINE

A terminated unbalanced transmission line conveys digital information between the driver and receiver cards. A -2.1v input to the receiver card signifies a logic "0" while a -0.15v level signifies a logic "1".

The line is terminated at each end in approximately 110 ohms. A normal -2.1v line level is established by the terminating network, while turning on the driver forces the line to -0.15v.

Separate power supplies may be used with each terminating network. The two power supplies are interconnected by means of the illustrated diode network. This arrangement gives either or both power supplies the ability to bias the line.

The transmission line, which is limited to 1000 feet, can service combinations of up to eight long line drivers and eight long line receivers.

Two electrically paralleled connectors connect a given piece of equipment to the transmission line. Equipment located at the extremities of the line must have one of its connectors directed to a termination network.

The velocity of signal propagation along the line is approximately 50 to 60 percent of the velocity of light. The resultant time delay per foot is of the order of 1.6 to 2.0 nanoseconds.

The long line driver/receiver will tolerate typical noise levels to 0.75v.

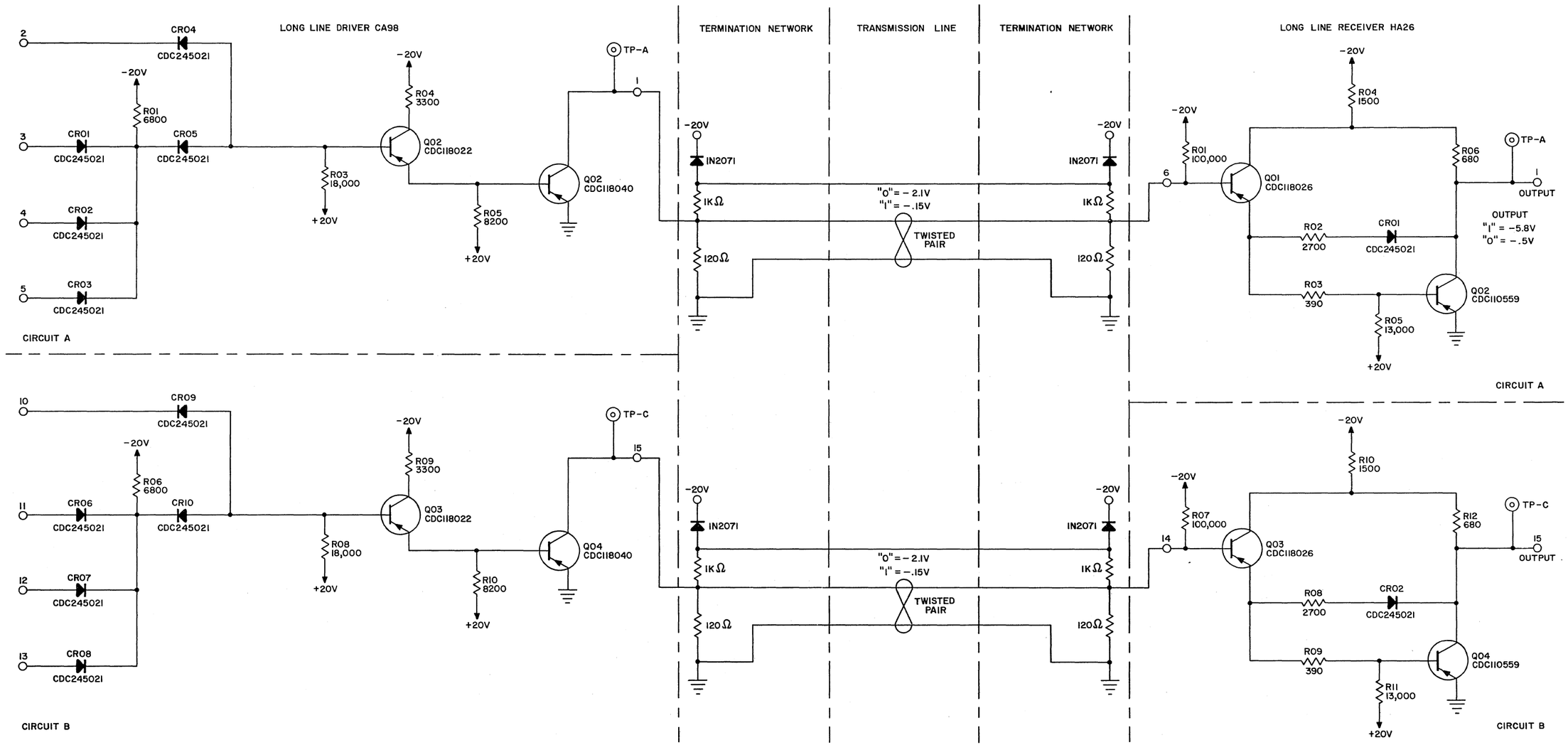
LONG LINE RECEIVER, Card Type HA26

This card contains two identical long line receiver circuits designated A and B. The receiver card responds to transmission line inputs of -2.1v and -0.15v which signify logic "0" and logic "1" inputs respectively. A -2.1v signal at the receiver input is applied to the base of Q01. The resultant forward bias condition allows conduction through Q01. Emitter follower action forward biases Q02. The resultant saturation of Q02 forces the collector potential to 0.2v.

A -0.15 signal at the receiver input turns Q01 off. This allows diode CR01 to become forward biased permitting feedback between the base and collector. This feedback stabilizes the collector voltage at -5.8v.

GROUND RULES

1) The output of a logic card constitutes a proper input to a long line driver.
2) The output of a long line receiver constitutes a proper input to a logic card.
3) A long line receiver may drive up to eight "AND" loads or up to three "OR" loads.
4) The transmission line may be of any length to 1000 feet. Transmission lines over 500 feet in length use 20-gauge wire, whereas lines less than 500 feet may use 24-gauge wire.
5) Any combination of up to eight long line drivers and eight long line receivers may be connected to one transmission line.



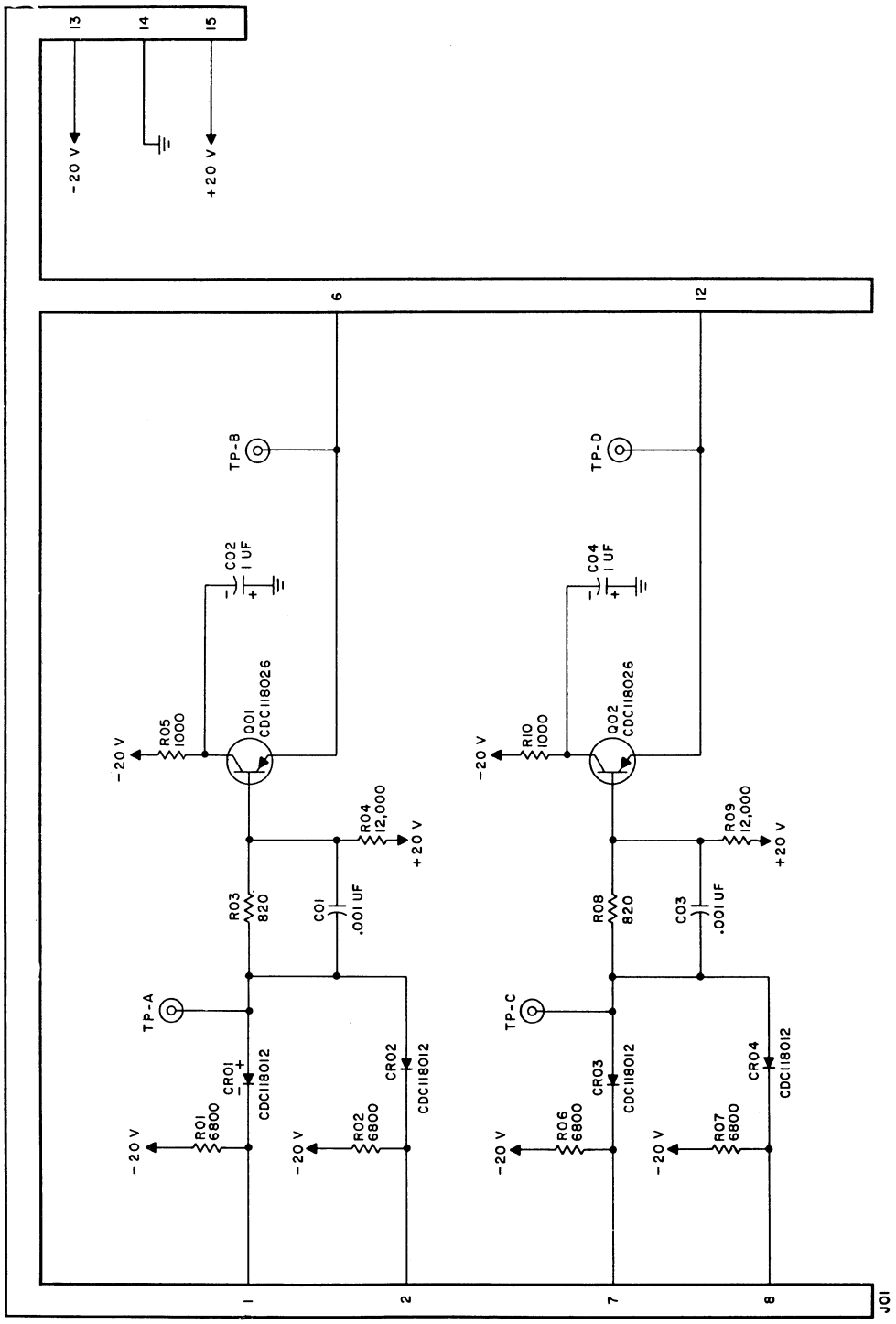
Long Line Driver CA98 Transmission Line and Long Line Receiver HA26

LINE DRIVER

Card Type E12

Card Type E12 is a ±1.0v (C Type, IBM) Line Driver. This card can be used to interface Control Data equipment using 1604-type logic with IBM equipment which uses C-line voltage levels. The card has two inputs and one output. An output of ±1.0v is obtained when a -3v "1" or -0.5v "0" is applied at the input.

The card has two identical emitter follower circuits. Since transistor Q01 is connected in an emitter-follower configuration, there is no phase reversal between the input and output. As the input signal becomes less negative, -0.5v, the forward bias is reduced and the output is +1v. When the input signal is -3.v, the forward bias is increased and the output is -1v.



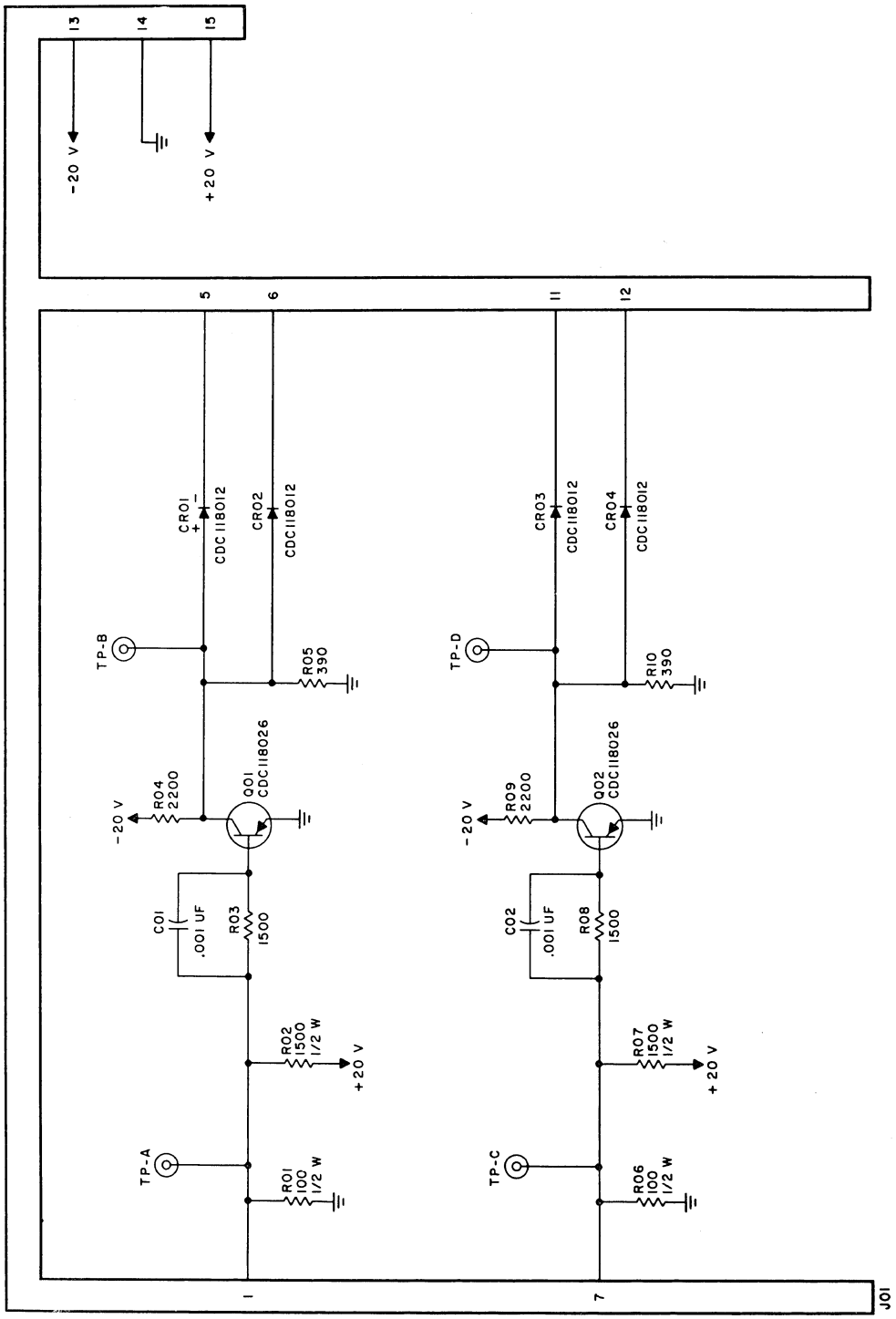
Line Driver E12

LINE RECEIVER

Card Type E13

Card type E13 is a ±1.0v (C-type), IBM Line Receiver and is a counterpart of E12. The card enables 1604-type logic to receive signals from IBM equipment which uses C-line logic levels.

The card has two identical common inverter circuits Pins 1 and 7 are used as input pins; and pins 5, 6, 11, and 12 as output pins. An input of -1.0v gives an output of -0.5v "0". An input of +1.0v gives an output of -3.0v "1". Resistors R01, R02, and R05 are voltage dividers and C01 is a by-pass capacitor.



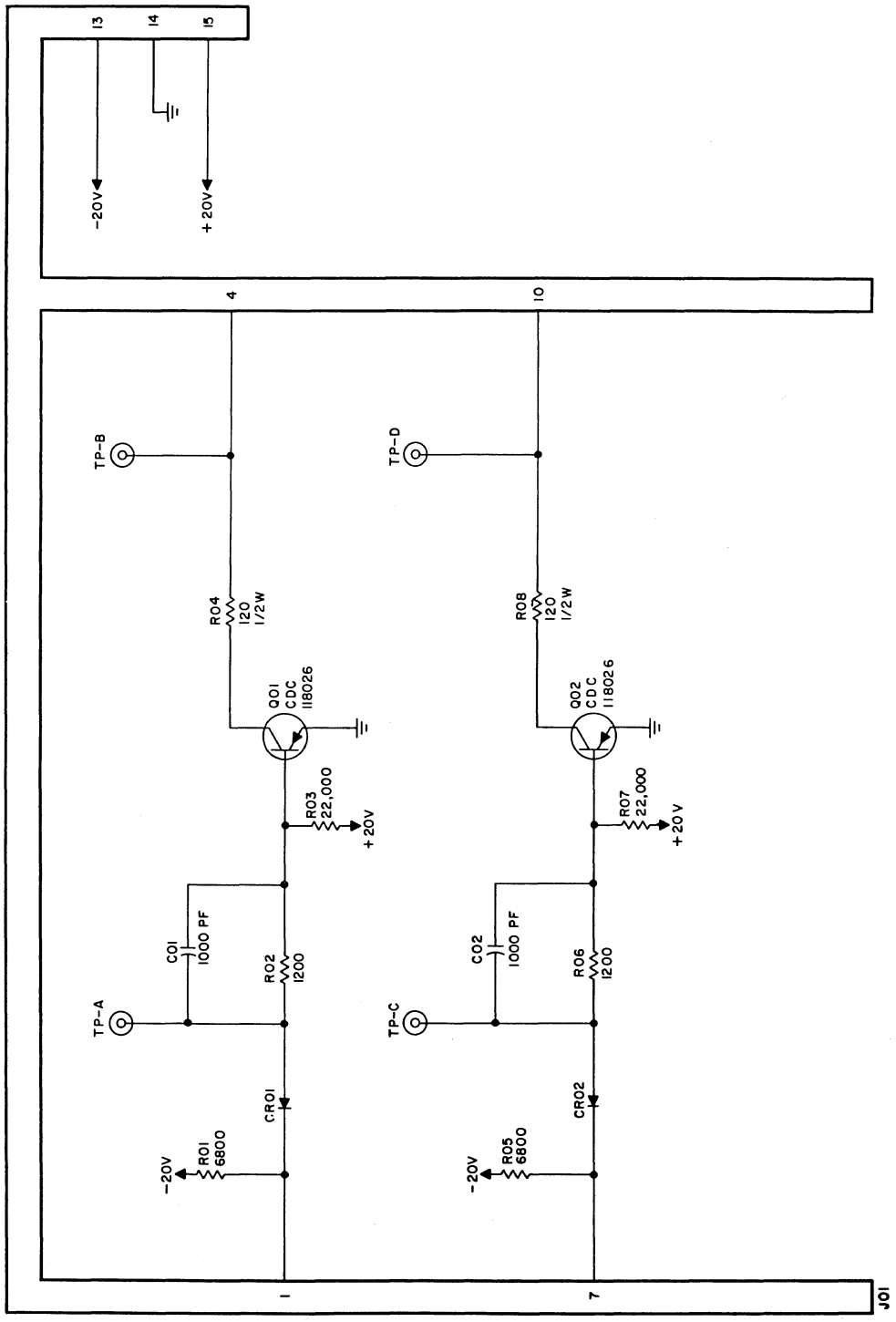
Line Receiver E13

LINE DRIVER

Card Type E15

Card E15 has been designed to convert 1604-type logic levels to IBM P-line logic levels (-6 ± 1v).

The card has two identical circuits, each having one input and one output. The circuit consists of a single stage simple inverter (common-emitter). Capacitor C01 is a bypass capacitor. An output of -6 ± 1v is obtained when a -3.0v "1" or -0.5v "0" is fed as an input.



Line Driver E15

LINE RECEIVER

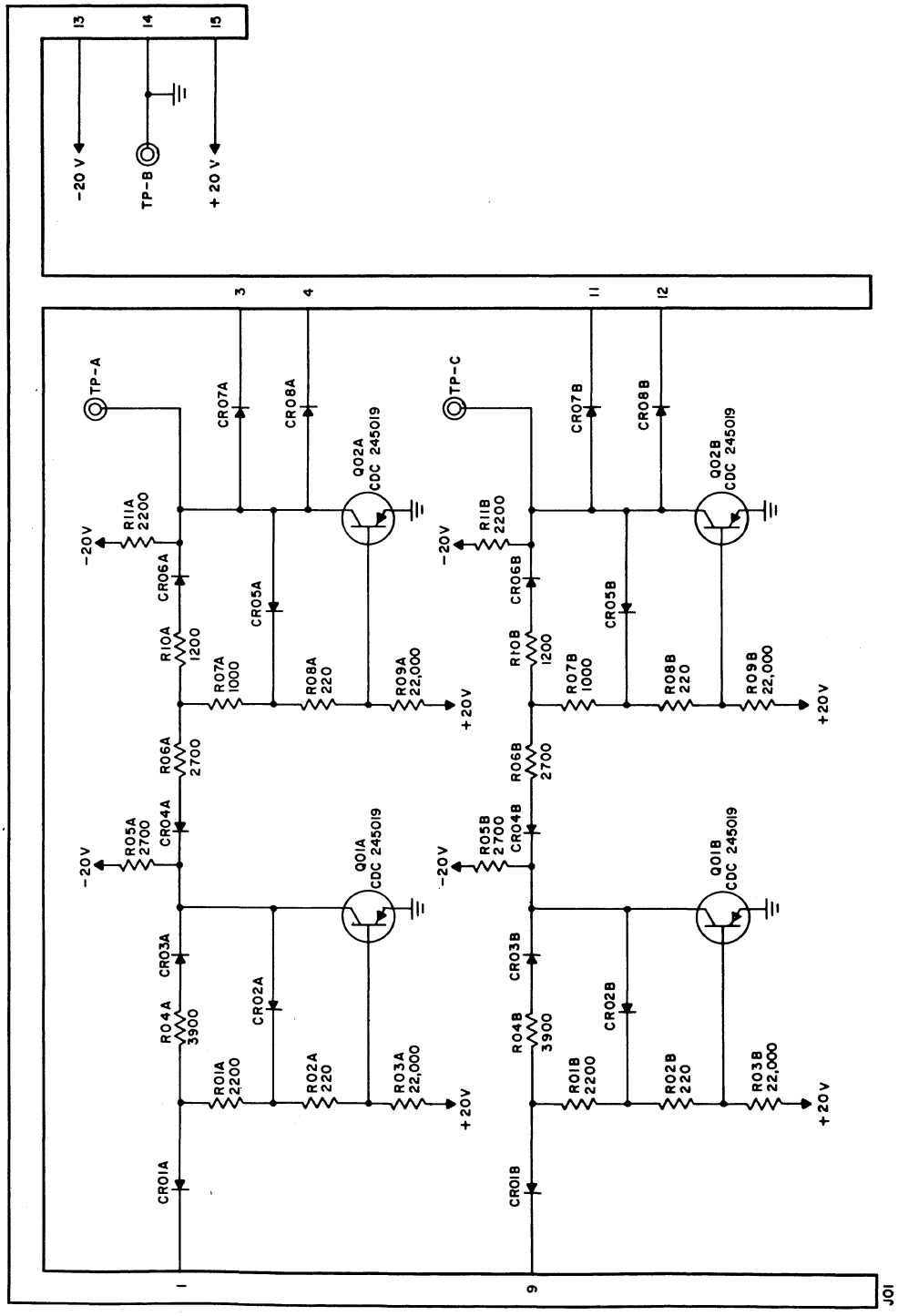
Card Type E61-A

Card type E61A is a receiver card which converts a -6v input to -3v "1" output and a 0v input to a -0.5v "0" output.

The card has two identical circuits, each containing one input and providing two outputs. A circuit consists of two common emitter inverter sections. The component values of the two circuits are such that an input of approximately 0 volts causes Q01 to approach cutoff and Q02 to approach saturation. When Q02 is near saturation, output diodes CR07 and CR08 provide a -0.5v output. An input of -6v causes Q01 to approach saturation and Q02 to approach cutoff. When Q02 is near cutoff, output diodes CR07 and CR08 provide a -3.0v output.

Feedback diodes CR02, CR03, CR04, CR05, and CR06 speed the switching time of the transistors by preventing complete cutoff or saturation.

Line driver counterparts of the E61A receiver are E62B and E67A.



Line Receiver E61A

LINE DRIVER

Card Types E62B and E67A

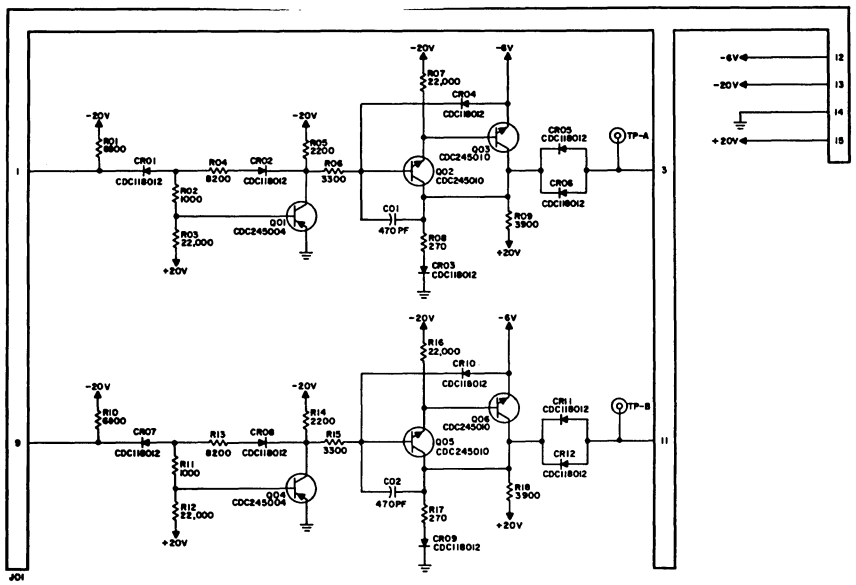
Card types E62B and E67A provide a 0v output for a -0.5v "0" input and a -6v output for a -3v "1" input. The only difference between the two cards is that E67A has an additional OR input.

Card circuits have three sections: input, amplifier, and output. The input section consists of a PNP transistor inverter. The amplifier section consists of two NPN transistor amplifiers. The output section consists of two parallel isolating diodes.

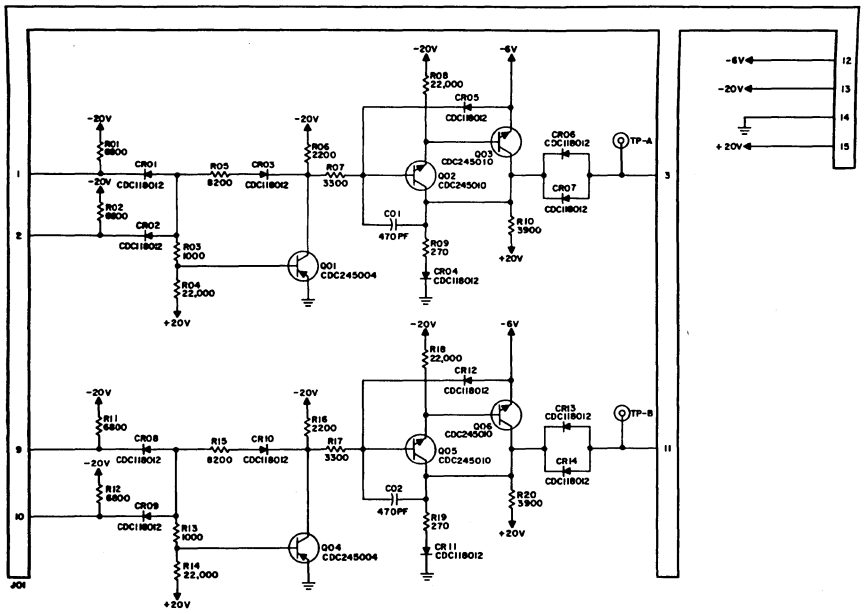
An input of logical "0" (-0.5v) at pin 1 (pin 2 for E67A) places a small positive voltage (approximately .8v) on the base of transistor Q01, causing it to approach cutoff. When Q01 is near cutoff, its collector is at approximately -10v, and the base of Q02 approaches -6v as C01 charges through R06, causing transistors Q02 and Q03 to approach cutoff. When Q03 is near cutoff, diodes CR05 and CR06 are reverse biased and have a small positive voltage (effectively 0v).

An input of "1" (-3.0v) at pin 1 (pin 2 of E67A) places a negative voltage of approximately -0.5v on the base of transistor Q01, causing it to approach saturation. When Q01 is near saturation, the voltage on its collector approaches 0v, and the base of Q02 becomes more positive as C01 discharges through R06. As the base of Q02 becomes more positive, conduction increases, and Q02 approaches saturation. As the conduction of Q02 increases, the base of Q03 becomes more positive, and it approaches saturation. When Q03 is near saturation, the -6v supply is impressed across the output diodes CR05 and CR06.

The switching time of the Q02-Q03 amplifier circuit is dependent upon the charge-discharge time of C01 through R06. In order to speed the switching time of the transistors, feedback is provided through CR02 and CR04 to prevent the transistors from being driven to complete saturation.



Line Driver E62B



Line Driver E67A

4-E62B & E67A-2

Rev. E

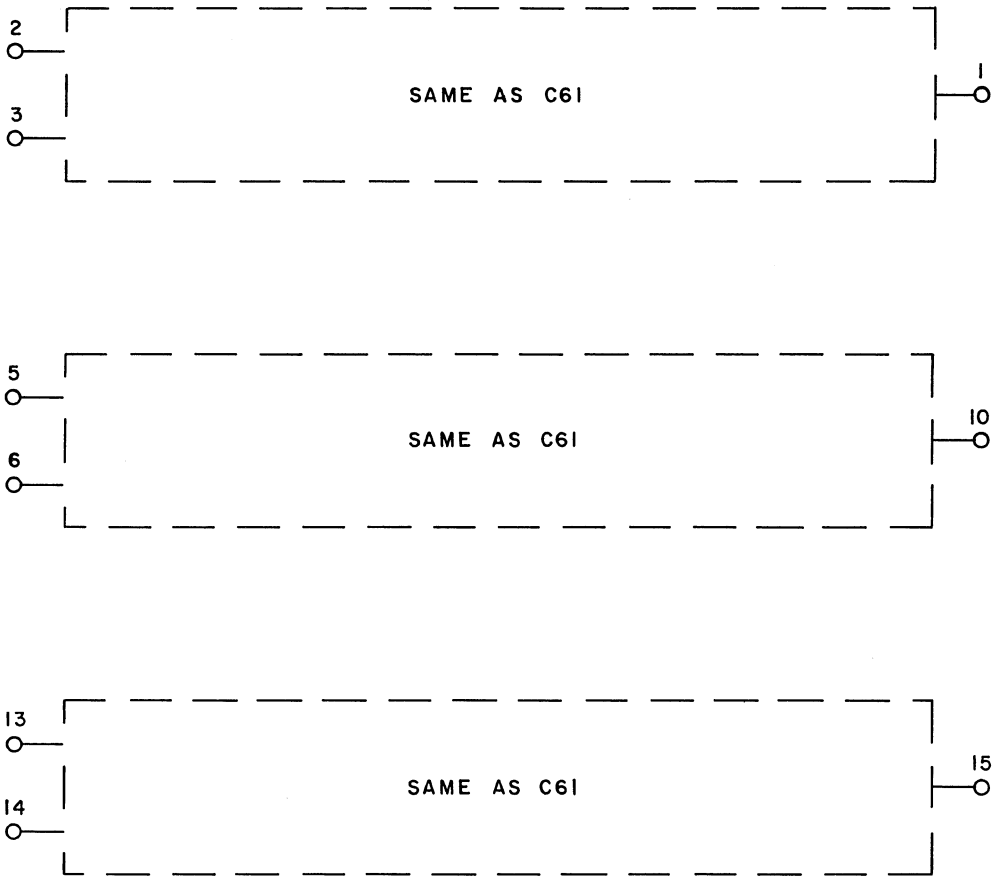
RECEIVER
Card Type HA11A

This card contains three receiver circuits, having the pin connections shown in the accompanying diagram. The circuits operate the same as card type C61, which is discussed elsewhere.

The circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either a -5.8 v "1" or a -1.1 v "0", according to the polarity of the differential 0.5 v signal which the two input terminals receive from the transmission line.

The transmission line is balanced, terminated, twisted-pair, and the signals are centered about ground. As an example, if pin 2 goes to +0.25 v and pin 3 goes to -0.25 v, pin 1 will go to -1.1 v "0". If the inputs are reversed, the output will be -5.8 v "1".

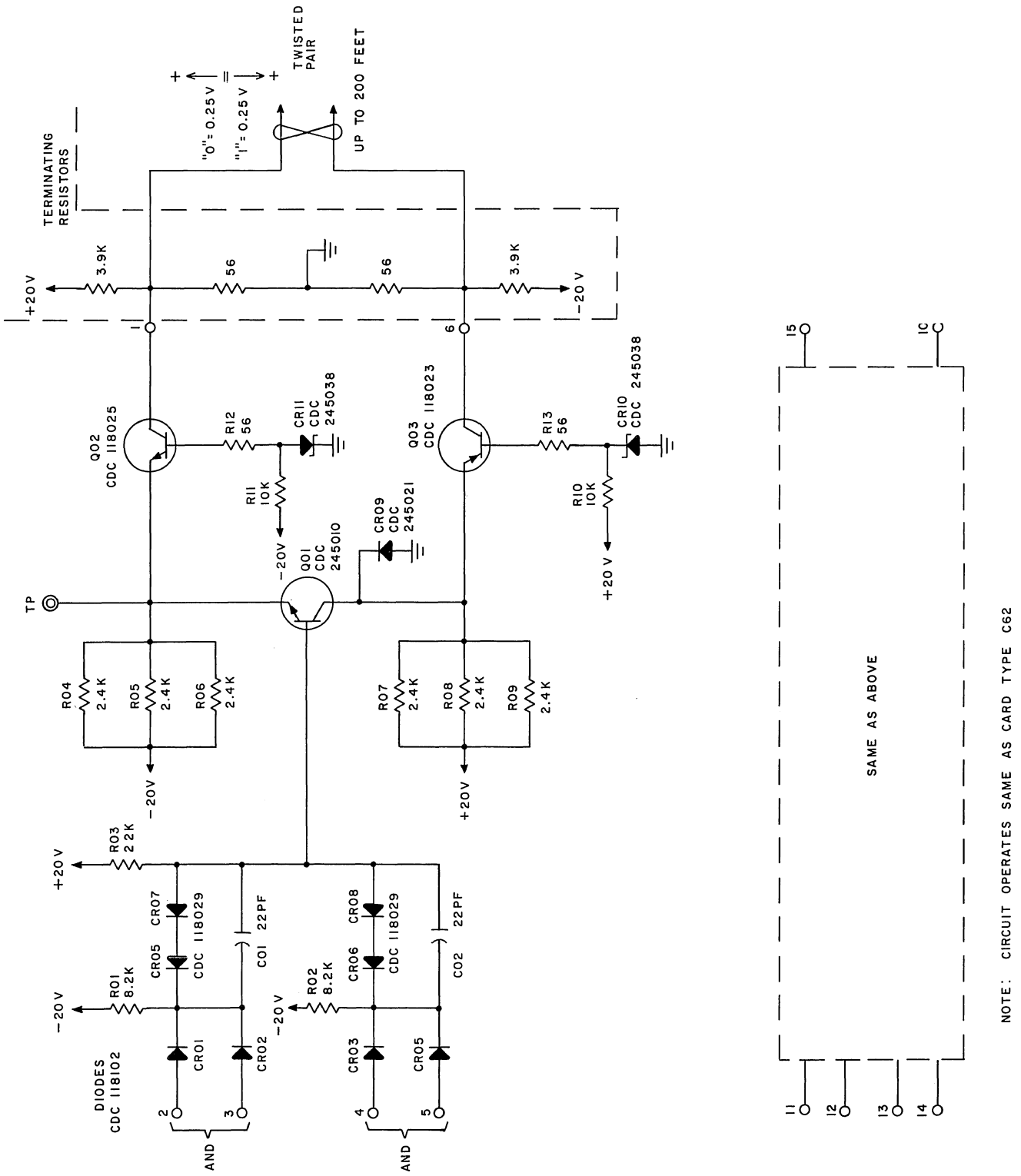
The receiver circuit will drive 8 loads, and the ground rules are the same as for card type C61.



NOTES: 1. CIRCUITS OPERATE SAME AS C61.
2. 3 RECEIVER CIRCUITS PER CARD.

TRANSMITTER
Card Type HA19

The function of the circuits on this card is to convert logic signals into outputs suitable for transmission over a balanced, terminated, twisted-pair transmission line up to 200 feet in length. Each circuit has two 2-way AND inputs. The remainder of the circuit is identical to card type C62 and the same ground rules apply.



Transmitter HA19

LEVEL TRANSLATOR
Card Type HA31

FUNCTION

The function of the circuits on this card is to perform a level-shifting action so that a 3600 receiver circuit can receive inputs from a 75-ohm coaxial line. A typical application is shown in the accompanying diagram.

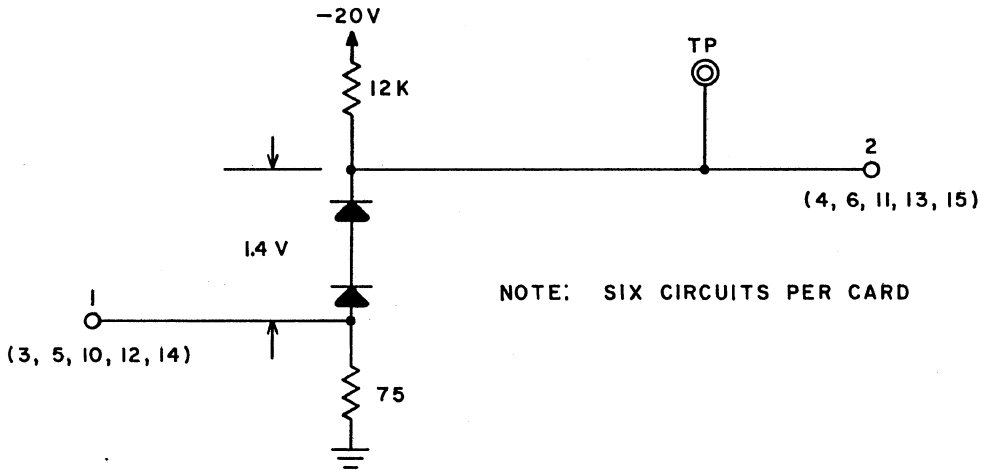
OPERATION

The card contains six identical circuits, as shown. The output of each circuit is held approximately 1.4 v negative with respect to the input.

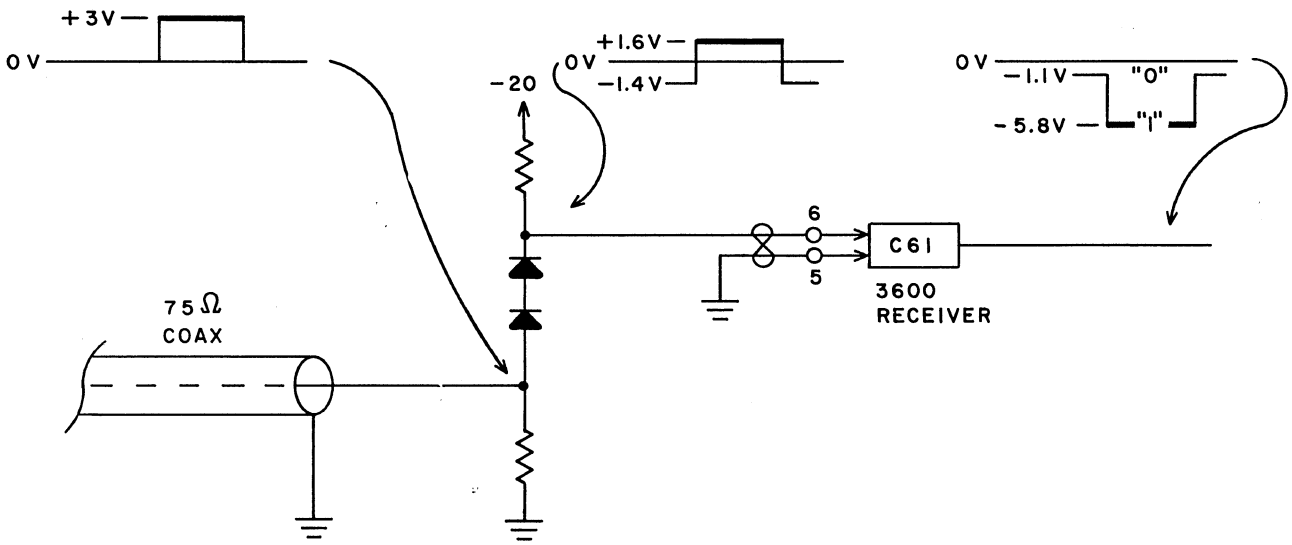
The level-shifting action is performed by two silicon diodes, each having a forward drop of approximately 0.7 v. These diodes also have a low dynamic impedance which will cause little attenuation of input signal current.

The purpose of the 75-ohm resistor is to provide impedance matching for the 75-ohm coaxial cable input.

SCHEMATIC



TYPICAL APPLICATION



Level Translator HA31

LINE DRIVER
Card Type HA32A

FUNCTION

The function of this card is to enable 3600 logic to interface with a disc file, as described in specification 118086. The circuit is designed so that, in the quiescent state with -1.1 v "0" inputs, all transistors are cut off and the circuit draws very little power. Upon receipt of a -5.8 v "1" input, all transistors switch to their conduction state and the circuit produces a positive going output.

The circuit will drive a signal a distance of 50 feet. The output from pin 2 can feed either a twisted pair with one line grounded or a 75-ohm coaxial line. By jumpering pins 1 and 2, approximately 70 ma of current may be provided for activating a reed relay.

OPERATION

The logic input to the circuit consists of two 4-way ANDs and two single-way ANDs. The circuit will be turned off only when all AND groups receive -1.1 v "0" inputs or are grounded. An open AND group or a -5.8 v "1" which satisfies the AND will activate the circuit.

Diodes CR16 and CR17 are silicon forward-drop devices, each of which has a constant forward drop of 0.7 v. They have a low dynamic impedance and are used to obtain an input level shift for transistor Q01.

A -1.1 v "0" input on each AND group results in all transistors being cut off. The level-shifting action of CR16 and CR17 attempts to bias Q01 well into the cut off region, however, the base of Q01 is clamped at about +0.7 v by diode CR18.

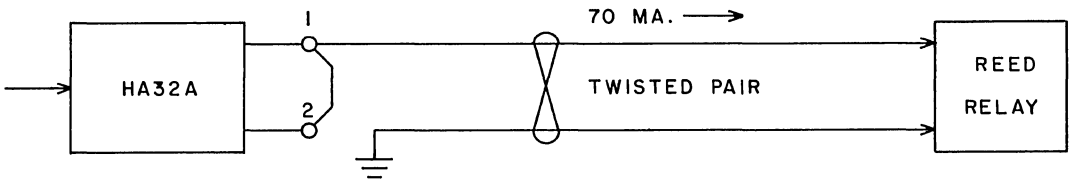
The collector voltage of Q01 rises to approximately -5.4 v, due to the voltage-divider action of R08, R09, R10, R11, and R12. The input at the base of Q02 will be about -3.4 v so that it is well into the cut off region. The input at the base of Q03 rises toward +20 v, however, its emitter is held at +19.3 v by the forward drop across CR20 so that Q03 is also cut off. In this state, the output impedance of the circuit is approximately 5,000 ohms, established by R17 and the output resistors.

A -5.8 v "1" input which satisfy one of the AND groups will cause all of the transistors to switch to their conduction state. This input voltage causes diodes CR16 and CR17 to place a strong forward bias on the base of Q01, causing it to conduct heavily. However, Q01 is held out of saturation by diode CR15 and its collector voltage stabilizes near -0.7 v.

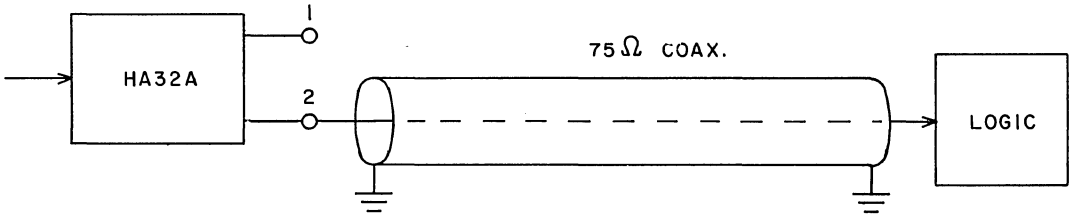
The voltage-dividing action of R09, R11, and R12 provides forward drive for Q02. It is prevented from saturating by CR19. Transistor Q02 in its conduction state causes current flow through R16 to increase. The voltage drop across R16 is limited by the sum of the drops across CR20 and the emitter-base junction drop of Q03. A further increase in the collector current of Q02 will draw turn-on current through Q03, causing it to switch on and conduct heavily. This allows the -20 v source through CR20 and Q03 to produce an output at pins 1 and 2.

The 1000-ohm resistor R25 will prevent damage to Q03 and CR20 if the circuit test point is accidentally grounded.

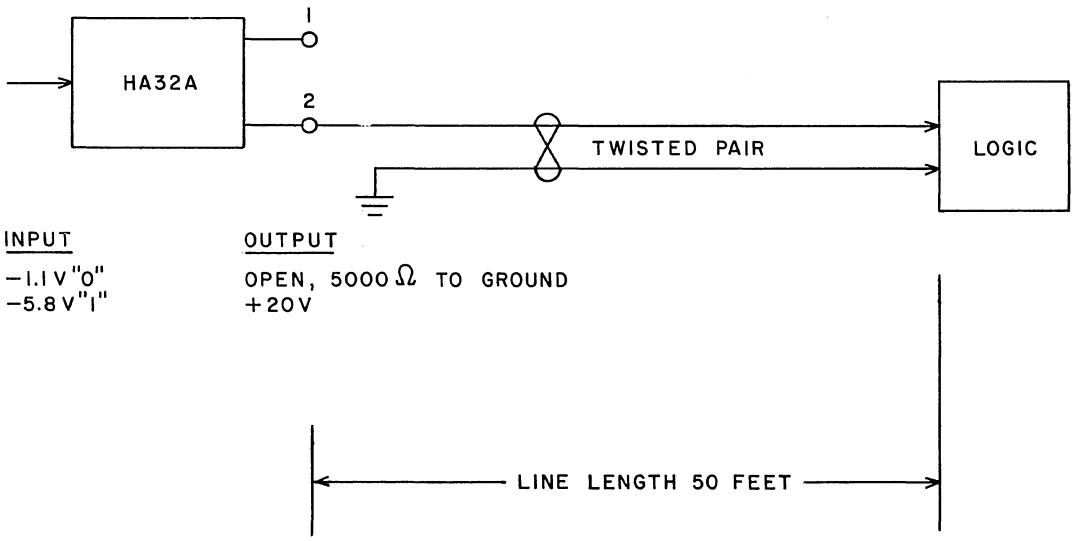
TYPICAL APPLICATIONS



INPUT	OUTPUT
−1.1 V "0"	OPEN, 5000 Ω TO GROUND
−5.8 V "1"	70 MA. ≈ +9V

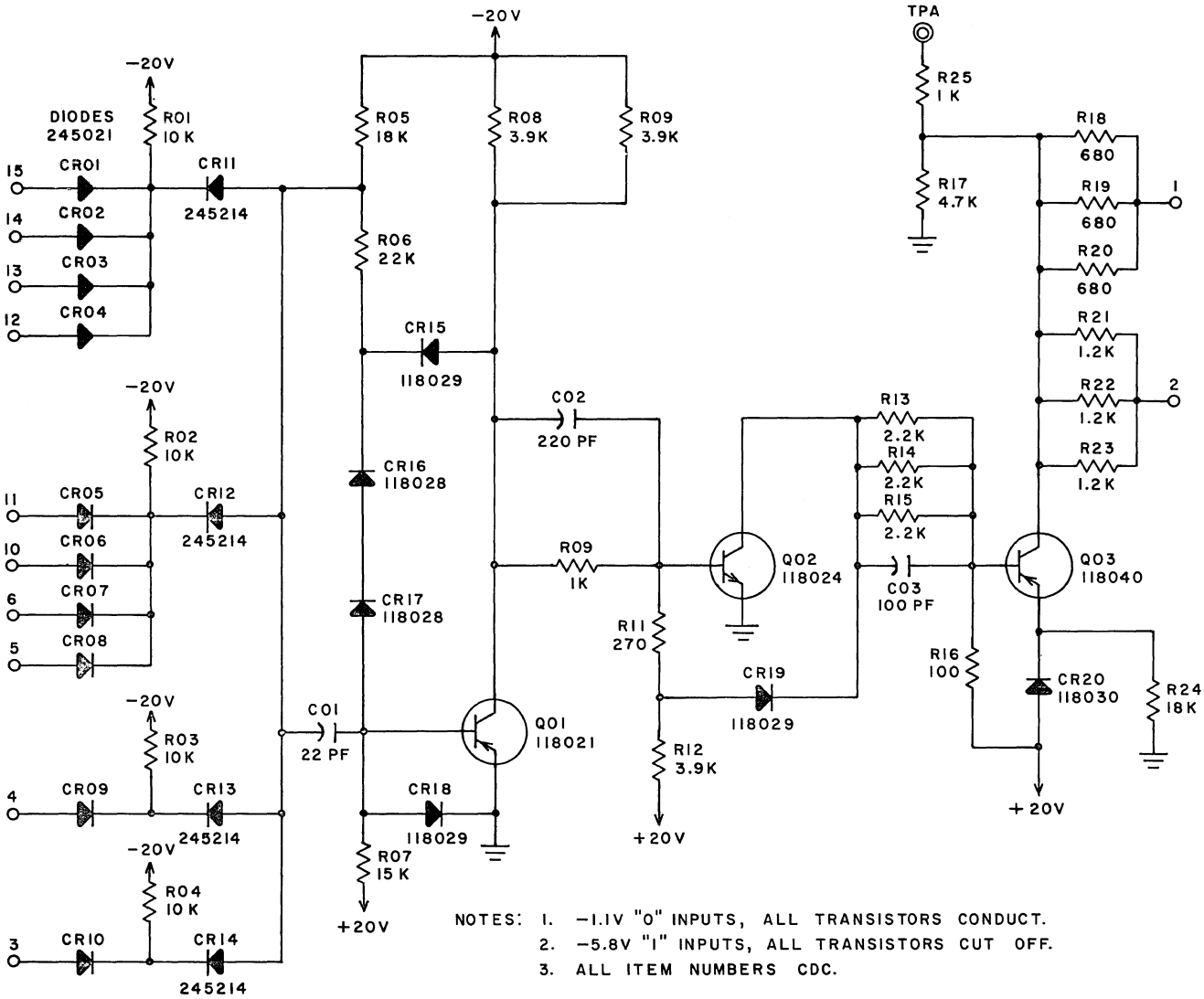


INPUT	OUTPUT
−1.1 V "0"	OPEN, 5000 Ω TO GROUND
−5.8 V "1"	+20 V



INPUT	OUTPUT
−1.1 V "0"	OPEN, 5000 Ω TO GROUND
−5.8 V "1"	+20V

Typical Applications



Line Driver HA32A

TRANSMITTER
(1000-foot line)
Card Types HA37 and HA43

GENERAL

The purpose of the long-line transmitter circuits is to increase the distance over which signals may be sent on a 3600-type transmission line. The standard transmitter cards (C62 and HA19) are restricted to driving 200-foot lines; by substituting card types HA37 and HA43, the line length may be increased to 1000 feet. This feature will allow peripheral equipment to be installed in locations remote from the computer system.

The circuits on card types HA37 and HA43 are identical; the difference lies in their input configurations. The circuits on card type HA37 each have a 3-way AND input, the same as card type C62. The circuits on card type HA43 each have two 2-way AND inputs, the same as card type HA19.

The long-line system is d-c coupled, similar to the standard system. A limit of 1000 feet has been placed on the system to minimize changes required in standard hardware and because of limitations due to data transmission characteristics.

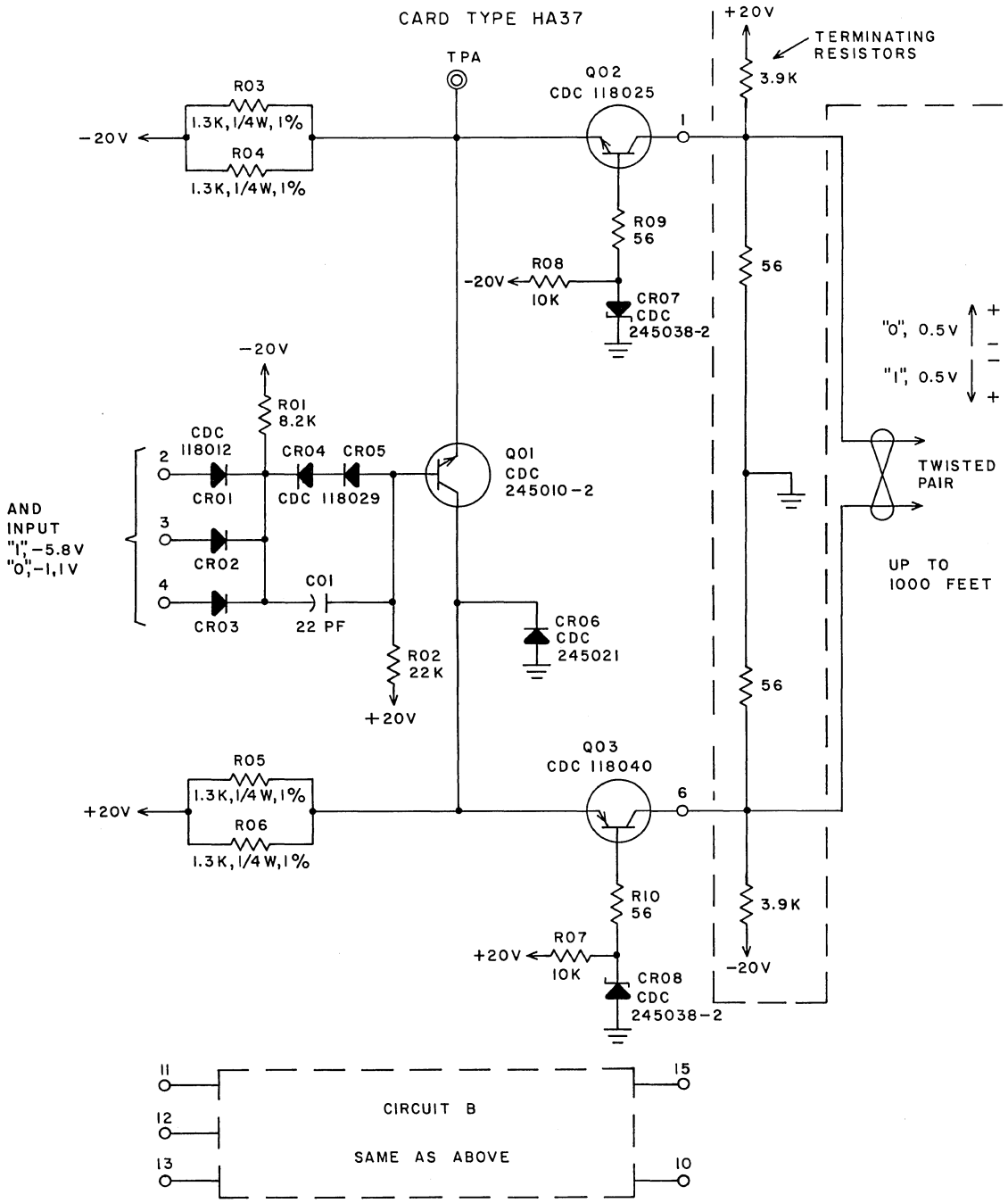
OPERATION

The long line transmitter circuit is identical in operation to the standard 3600-type transmitter. The major differences in the two circuits are the higher power capability of the HA37 and HA43 cards, and changes in specifications of some of the components.

Each circuit card contains two circuits designated A and B, as shown in the accompanying diagram. The input consists of a 3-way AND on HA37 cards, and two 2-way AND's on HA43 cards. The output of a standard logic logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction to Q01 to be forward biased, turning Q01 fully on. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the "AND" input is satisifed, the base of Q01 will be held at approximately -5 volts. This reverse-biases the emitter-base junction by approximately 3 volts and causes Q01

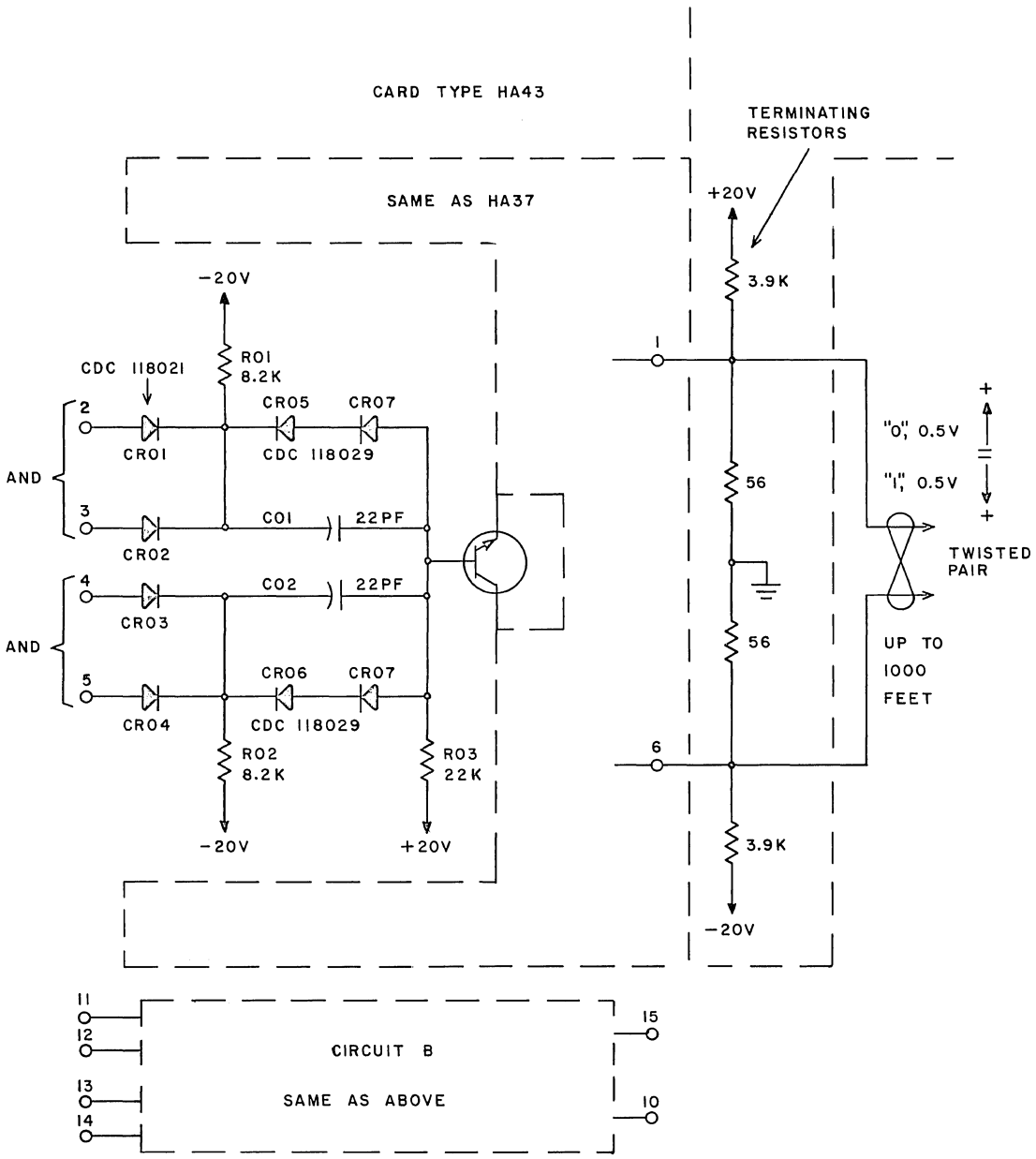


NOTE: THIS CARD MAY BE SUBSTITUTED FOR THE C62 CARD, TO DRIVE LINES UP TO 1000 FEET.

Transmitter HA37

4-HA37 & HA43-2

Rev. E



NOTE: THIS CARD MAY BE SUBSTITUTED FOR THE HA19 CARD TO DRIVE LINES UP TO 1000 FEET.

Transmitter HA43

to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 26 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contains a 3.45v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 will reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage will be allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3.28 volts, since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter will operate satisfactorily with more than 3 volts of random noise on the transmission line.

RECEIVER CIRCUIT

The receiver is the standard type C61 or HA11, which are described elsewhere in this manual.

CABLE

The signal cable is standard 3600-type, containing 29 twisted-pair transmission lines. Each transmission line consists of two 24-gauge conductors. If required, a cable with a protective copper braid shield may be used to protect against extreme electrical noise and other environmental hazards.

LINE TERMINATIONS

Line terminations are standard 3600-type signal cable terminators.

GROUND RULES

1. Installation:
   a. To convert an interface from a 200-foot cable length limitation to 1000-foot capability, all CA62B cards must be replaced with HA37 cards and all HA19 cards must be replaced with HA43 cards.
   b. Receiver cards remain unchanged.
   c. Transmission line terminations remain unchanged.

2. Each long line transmitter card requires approximately 1/3 watt more power than a standard transmitter card. The additional power is divided equally between the +20v and -20v supplies.

3. A maximum of 16 long line transmitters and 16 standard receivers may be distributed along a 1000-foot transmission line.

4. At a distance of 1000 feet, the output waveform of the receiver will be symmetrical for switching rates up to 500 kc. Switching rates in excess of 500 kc will result in degradation of symmetry. For distances of less than 200 feet, switching rates are similar to a standard transmitter-receiver system.

5. The balanced system using differential receiving techniques allows a difference in noise levels of up to 3 volts between the transmitter ground reference and the receiver ground reference. To avoid problems of noise pickup, it is recommended that the terminators on all remote equipments be energized from the common 40v supply, with an earth ground reference level. Decisions regarding the possible use of other terminator power and ground connections are the responsibility of the design engineer.

6. When driving signals through a 1000-foot cable, total delay time between input to the transmitter and output from the receiver will be approximately 2 micro-sec.

7. A signal de-skewing delay of 300 nanoseconds must be allowed for parallel transmission of 12 data bits over distances from 600 to 1000 feet.

DELAY AND SKEW ON A 1000-FOOT CABLE

When changing from a line driver system with a maximum distance of 200 feet to a system with a maximum distance of 1000 feet, the following changes must be made and new characteristics observed:

1. For distances from 600 to 1000 feet, the control signal (Data Signal, Reply, etc.) deskewing delay must be increased from 100 to 200 nanoseconds.

   Data Channel - Peripheral Device Delays

   Normal Operation

   The data channel allows 100 nanoseconds for Data Signal deskewing. This is active during both Read and Write operations. During a Write operation, the peripheral device must allow Data Signal delay for parity checking.

During a Read operation, the peripheral device delays the Reply for 200 nanoseconds to allow for signal deskewing and data channel parity checking.

Recommended Modifications for 200 Nanosecond Deskewing Delay

Modification should be done at the peripheral device, which would normally be the remote site. During a Write operation, the Data Signal should be delayed 100 nanoseconds at the peripheral device in addition to the parity checking delay. During a Read operation, the Reply delay should be increased by 100 nanoseconds to 300 nanoseconds to allow for signal deskewing and data channel parity checking.

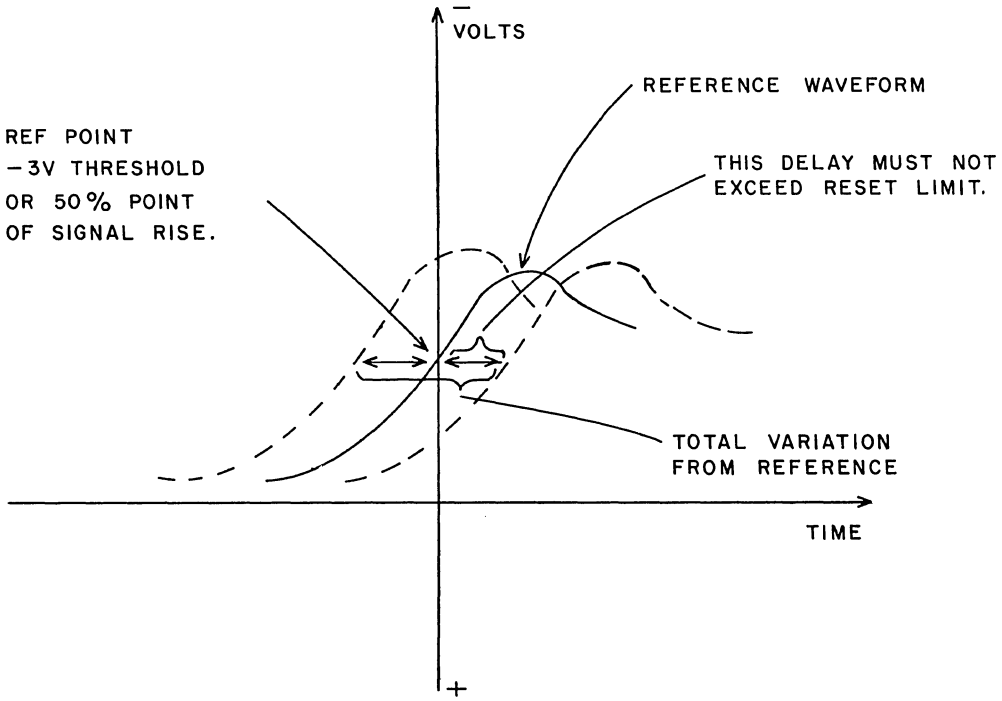
No attempt will be made to specify how the added delay should be inserted. The delay may be added in a manner most feasible for the device involved.

2. If normal operation does not occur, the following tests should be conducted:

   A. Check for required signal outputs from the transmitters (H37 card output) and receiver circuits (C61 card output). If no signal is received, check transmitter and receiver circuits; check line termination and voltages. If no problem appears to exist at this point, proceed to step B.

   B. From information on the logic of the connected equipment, find cases where the data or signal code lines are sampled within a certain period after the control signal is received. If the delay is preset, for example, at 100 nanoseconds, test if the delay period is at least 100 nanoseconds. Preset delay shall not be less than 100 nanoseconds. Synchronize an oscilloscope on the output of the control line receiver and observe the variation of the receiver outputs of the data or code lines with respect to the control line reference. The reference point may be considered as the -3 volt threshold point or 50% of the risetime point of 3600 logic.

In pictorial form, risetime variation may be sketched as follows:



The delay of the signal risetime of any data or code line must not exceed the preset 100 or 200 nanoseconds, whichever the case may be. Where required, fall time going from a "1" to a "0" signal may be tested in a similar manner. If the delay does not fall within the preset time, check for: (1) bad receiver card, bad components, etc. (2) bad wiring connection (3) improper line termination or termination voltages.

C. Check the system logic for Data Signal-Reply operation. The propagation time becomes an important factor in this situation. For example, assume device A has a Data Signal up and the remote site responds with a Reply. Device A drops the Data Signal in response to the Reply. The Reply is dropped at the remote site. Device A cannot bring up the next Data Signal until the dropping of the Reply at the remote site is recognized at Device A. Otherwise, Device A may accept the Reply from the previous word transfer and the information will be lost.

D. Connect and Disconnect Delay. For a system in which a data channel is communicating with peripheral equipments via 1000 feet of cable, the equipments must be modified so that the selected equipment will not return a Reply earlier than 3 usec after receiving the Connect signal.

TIME VARIATIONS DUE TO CABLE DELAY

A significant amount of time is lost in transmission of signals through cables. The following is an itemized list of approximate time lag in a 3600 system over a 1000-foot cable.

1.	Transmit Data Signal and data from data channel to peripheral device plus Data Signal delay	2,100 nano.
2.	Response time of peripheral device, i.e., examine parity, bring up Reply, and control signal delay	400 nano.
3.	Send Reply to data channel	2,000 nano.
4.	From dropping of Data Signal until data channel senses dropping of Reply.	4,000 nano.
5.	Memory reference time between 48-bit words	1,500 nano.
		10,000 nano.

$$\frac{1.0}{10.0 \times 10^{-6}} = .100 \times 10^{6}$$

100 KC word rate

200 KC character rate

worst case with 60 usec. memory reference time

$$\begin{array}{r} 8.5 \text{ usec.} \\ +\ 60 \text{ usec.} \\ \hline 68.5 \text{ usec.} \end{array}$$

$$\frac{1.00}{68.5 \times 10^{-6}} = .0146 \times 10^{6}$$

14.6 KC word rate

29.9 KC character rate

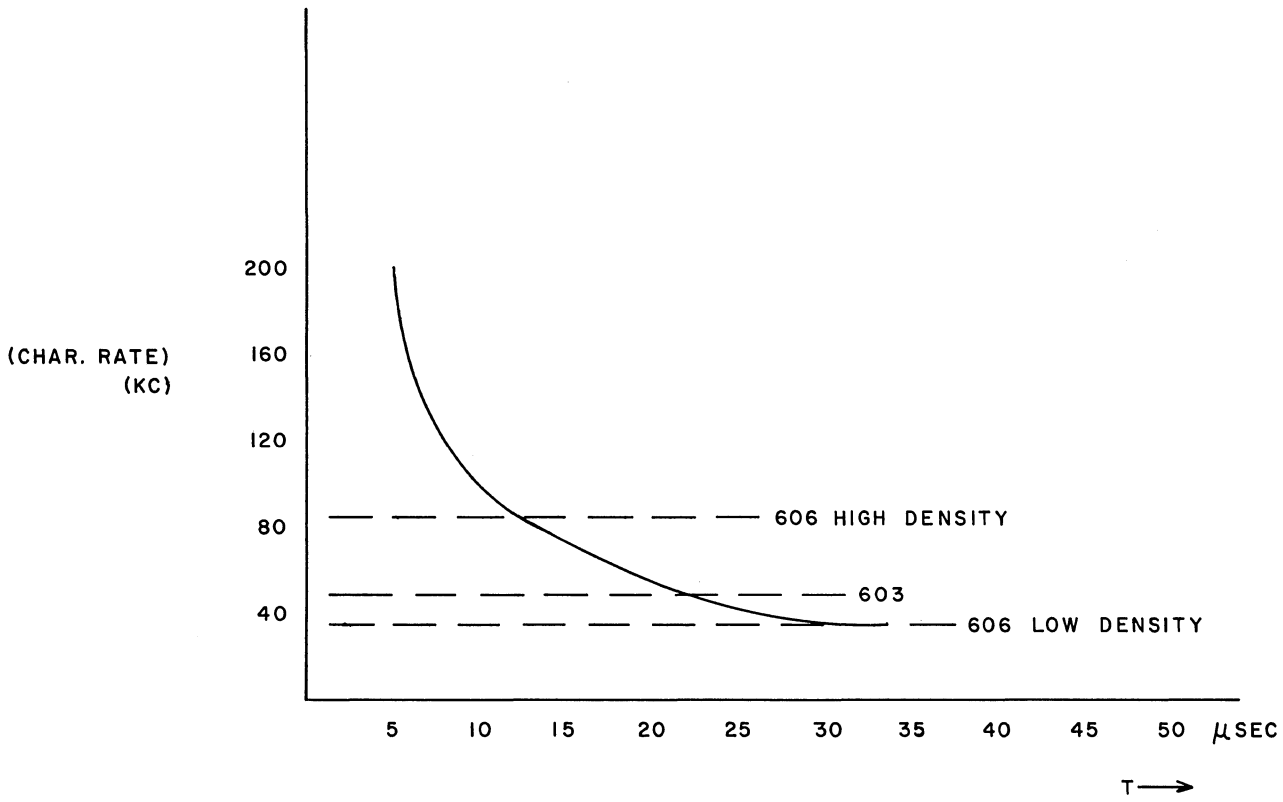
Read Delay (See accompanying diagram)

1. Same as for write (1).
2. This time is dependent on peripheral device speed.
3. 200 nanoseconds required with 200 to 1000 foot cable.
4. 100 nanoseconds for parity generation and checking.
5. Same as (1).

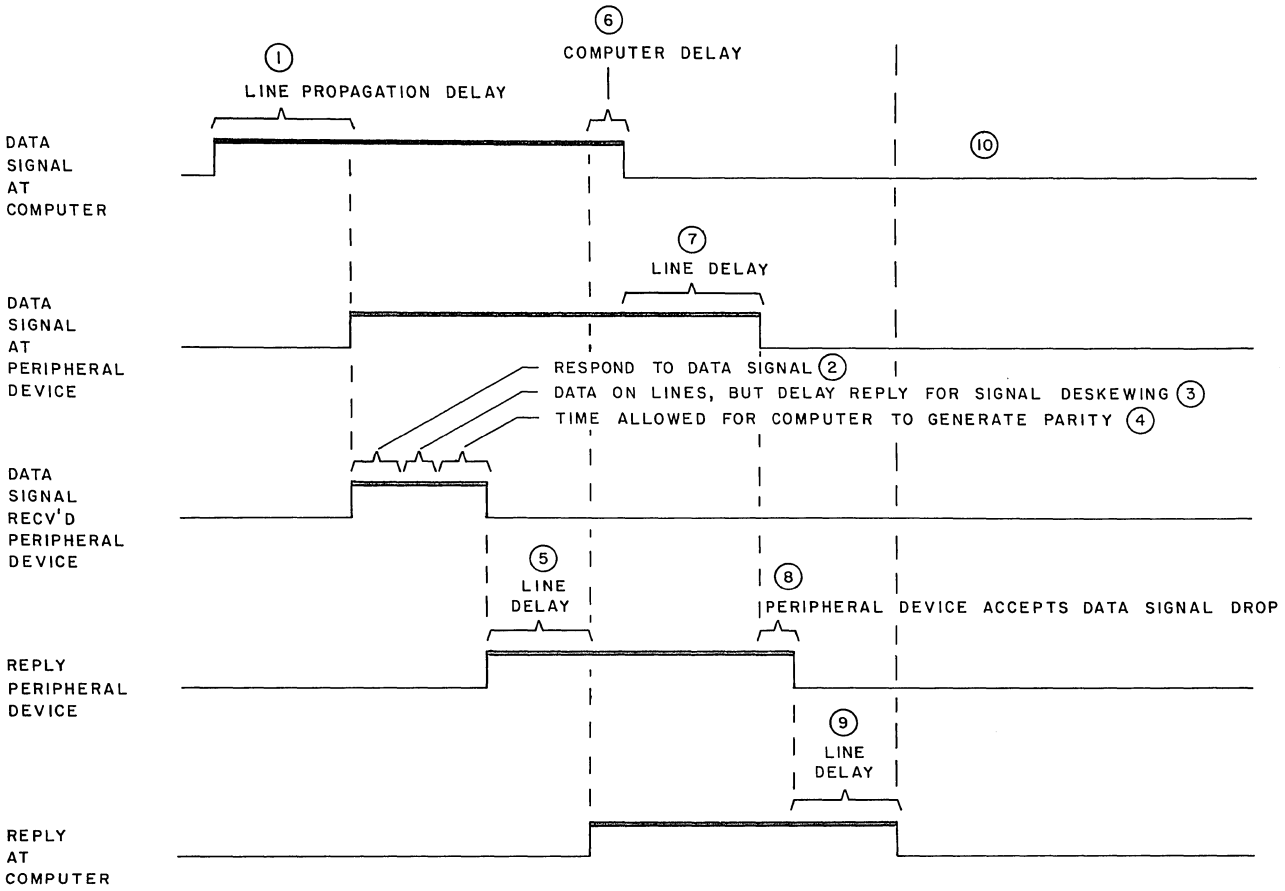
6. Computer responds to Reply, samples lines and drops Data Signal, (100 nanoseconds for 3606 data channel).
7. Same as (1).
8. Peripheral device responds to Data Signal drop and drops Reply.
9. Same as (1).
10. The next Data Signal can be transmitted and the computer can accept a Reply/ Reject signal only after time (9) is completed.

Write Delay (See accompanying diagram)

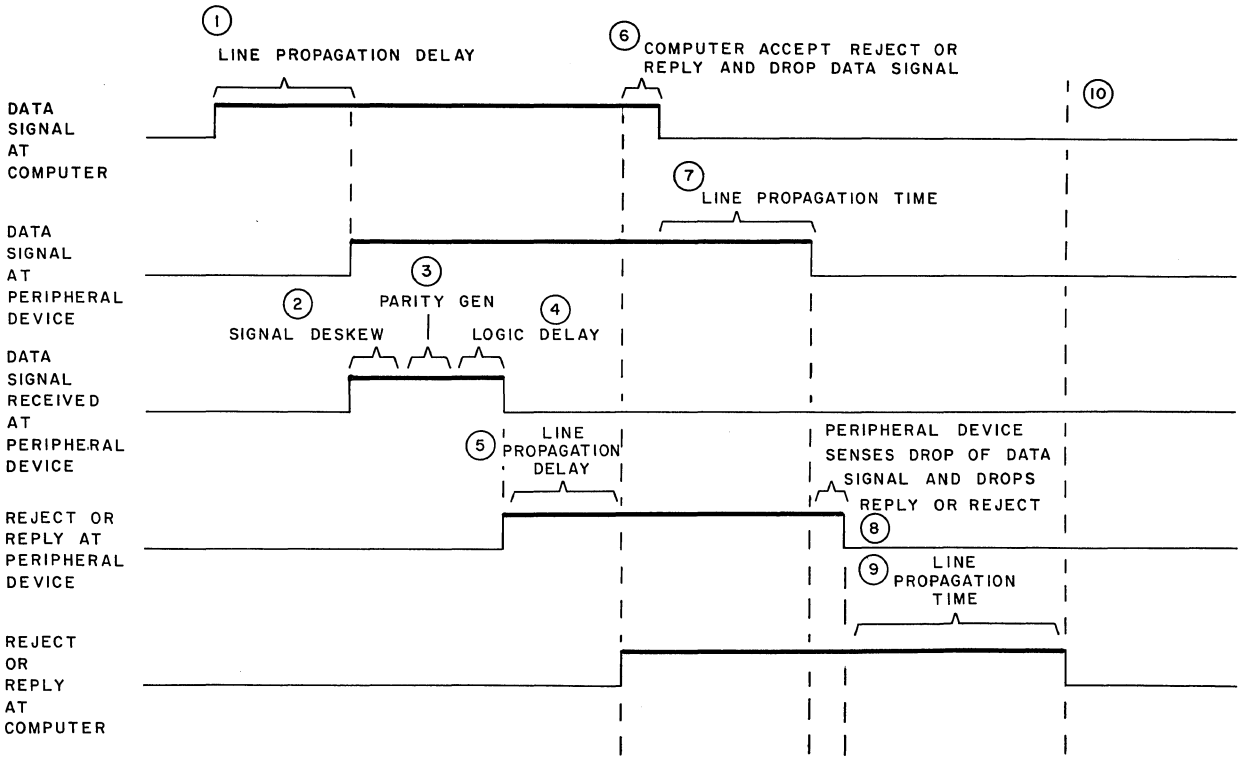
1. Line, transmitter and receiver card delay (approx. 2 usec. per 1000 feet).
2. Signal deskew allows the data lines to stabilize prior to sampling. (200 nanoseconds required for 1000 feet). The 3606 data channel inserts 100 nanoseconds of the required 200 nanoseconds.
3. Parity generated from data and checked against received parity bit.
4. Logic delay for decision making -- such as examine data and send Reply or Reject. This delay must be 3 usec. on a Connect operation to allow all peripheral devices to disconnect if the connect code does not pertain to that device.
5. Same as 1.
6. Computer accepts Reject or Reply and drops Data Signal. (The 3606 data channel allows 100 nanoseconds).
7. Same as 1.
8. Dependent on peripheral device.
9. Same as 1.
10. The next Data Signal can be transmitted and the computer can accept a Reject or Reply signal only after time (9) is completed.



APPROXIMATE CHARACTER SPEED FOR
3600 COMPUTER I/O OPERATIONS



DELAYS DURING READ OPERATION



DELAY DURING WRITE OPERATION

TRANSMITTER AND RECEIVER
Card Types P14C and P16A

FUNCTION

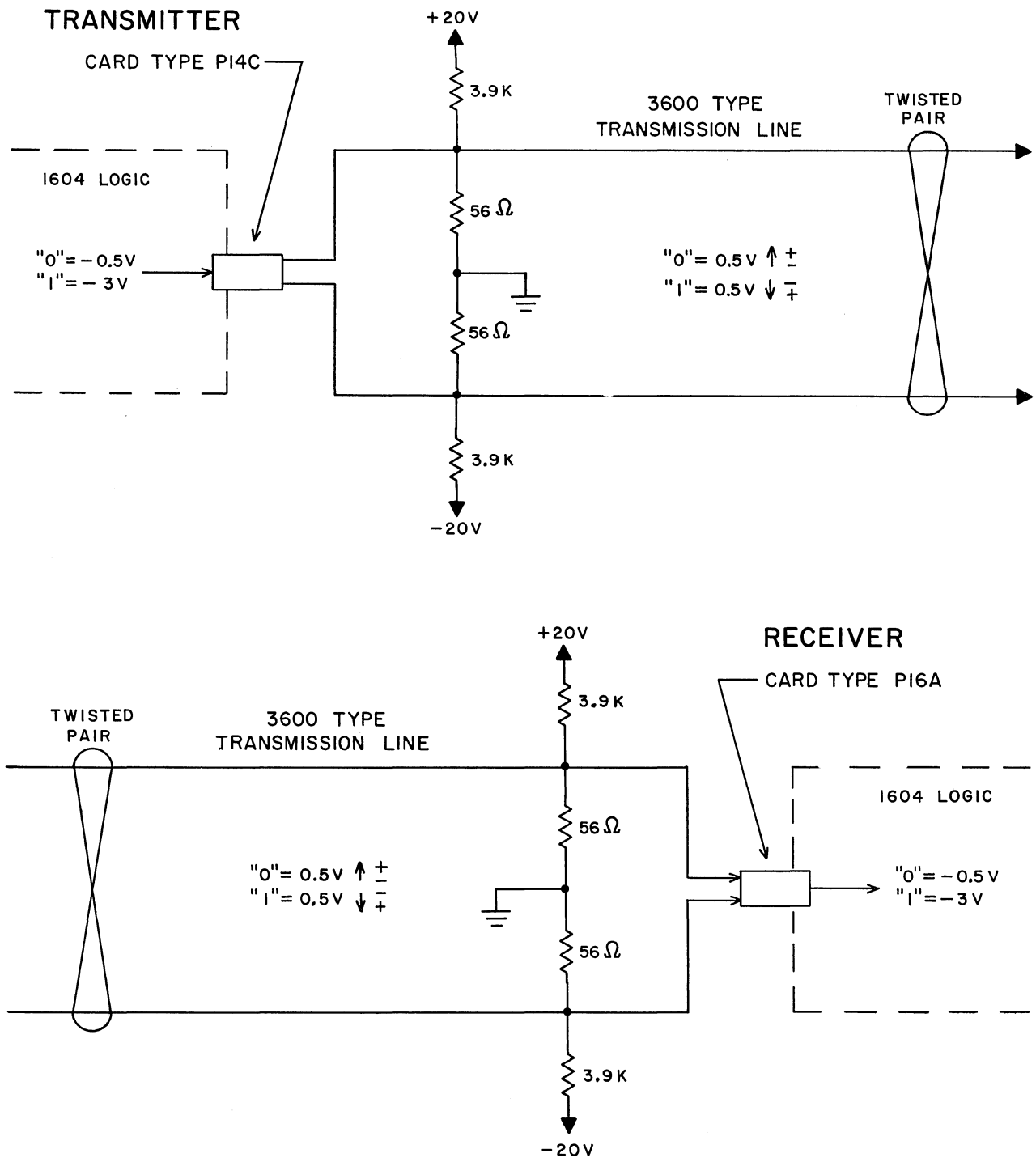
These circuits enable equipment containing 1604 logic to receive and transmit via a 3600 type I/O cable. This is accomplished by converting the 3600 transmission line signal levels of 0.5v line-to-line to the 1604 logic levels of "1" = -3v and "0" = -0.5v. Card types P14C and P16A have the same capabilities and impedance characteristics as 3600 type transmitters and receivers. Both types of transmitters and receivers may use the same transmission line.

OPERATION

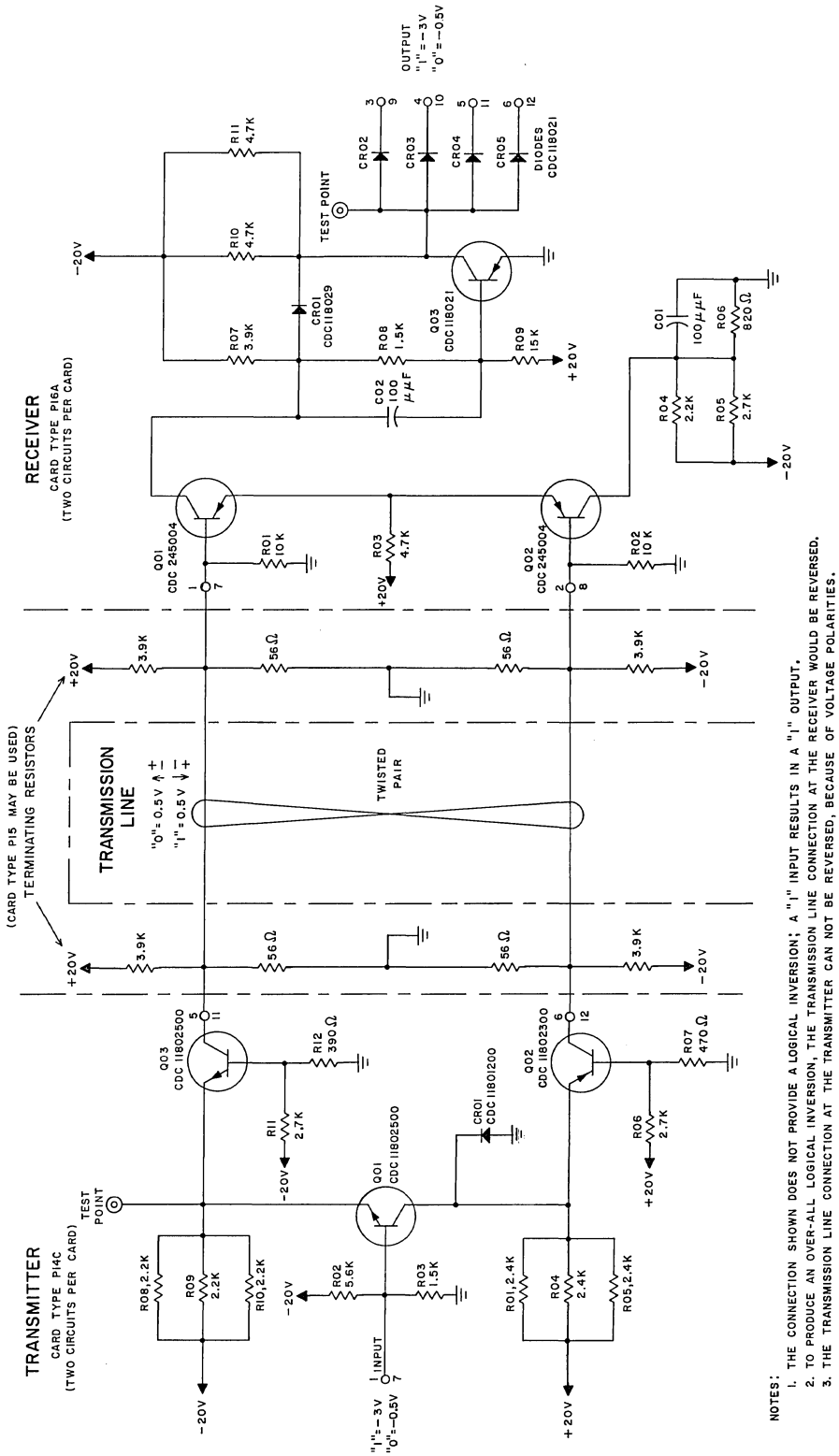
The transmitter, card type P14C, is similar to the C62A, which is discussed elsewhere. It converts single-ended inputs into double-ended outputs suitable for driving a balanced, terminated, twisted-pair transmission line. A -3v "1" input to transistor Q01 causes Q02 and Q03 to inject a current of about 20 ma into the transmission line. This results in a full line-to-line voltage reversal.

The "0" line signal level is established by the flow of bias current through the terminating resistors. In order to obtain proper voltage polarities, the transmitter must be connected to the line as shown.

The receiver, card type P16A, is similar to the C61B, which is discussed elsewhere. It functions both as a differential amplifier and as a discriminator, providing logic outputs of -3v "1" or -0.5v "0" according to the polarity of the 0.5v signal received from the transmission line. The transmitter and receiver combination can be made to provide a logical inversion by reversing the transmission line connections at the receiver.



Transmitter P14C and
Receiver P16A

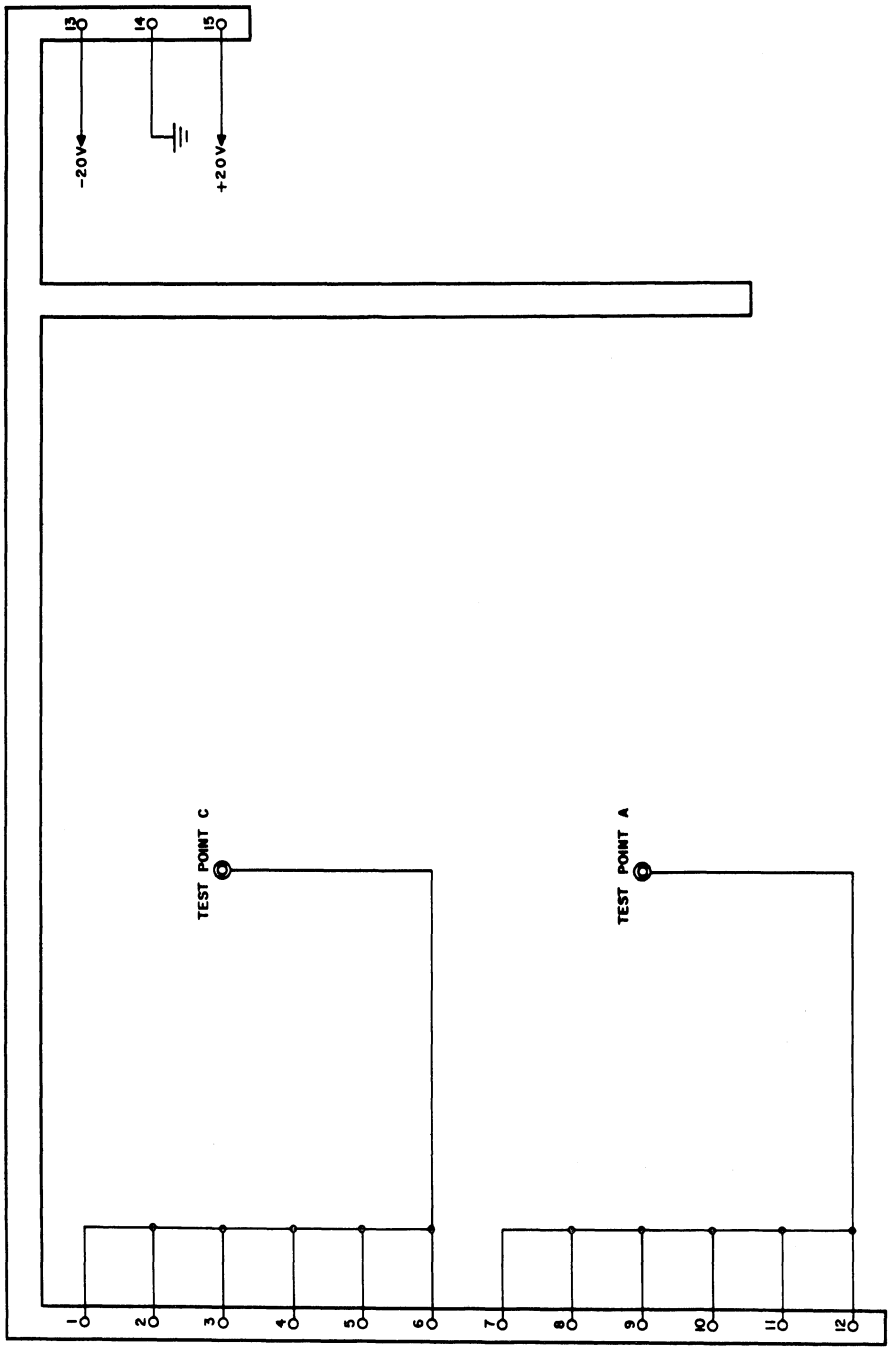


Transmitter P14C
Transmission Line and Receiver P16A

CLOCK DISCONNECT

Card Type 00

The clock disconnect is a jumper type card which synchronizes pulses from three 1604-type clock cards by connecting their tanks in parallel. It has no active components. This card should be removed when clock cards are being tested in order that they may be tested individually.



Clock Disconnect 00

CHAPTER 5. SPECIAL PURPOSE CARDS

Clock Disconnect	00
Oscillator	01, 01A, 02A
Oscillator Amplifier	06
Capacitor	50
Speaker Driver	65
Punch Puller	66
Read Amplifier	70B
Delay Capacitors	73, 73A, 77, 82
Reader Level Amplifier	75, 75A
Reader Brake-Clutch Driver	76A
Punch Puller	86
Hammer Storage	91
Delay	97A,
Hammer Driver One-Shot	144
Clock Oscillator-Amplifier	C01
Clamp	C02
Emitter Follower	C07C
Delay Line Driver	C08
Switch	C60A
Resync Circuit	C64A, C65A, C66A
Capacitive Delay	C67, K67, C68, C69, C70C, C71, K71
Priority Circuit	C77, C78B, C79A
Delay Line, 1 usec	C80
Crystal Oscillator	C81, C82, C83
Relay Driver	C84
Strobe Shaper	C85
Amplifier-Shaper	C89
Reader Level Amplifier	C91
Overload Protector	C94
Channel Disable	C97
Relay Card	CC10
Jumper	E00
Crosspoint Module	E01A, E02A
Crosspoint Crosspoint Module	E03A, E04A

Decoder	E05
Terminator	E06, E07
Single Pulser	E08
Integrator	E10
Delay	E11
Variable Clock	E14
Terminator	E19
Resistor Assembly	E20
Console Interface	H10A
Delay Line Amplifier	H12
Filter	H17
Light Driver	H20
Keyboard Translator	H27, H28
Delay Line, 0.1 usec	H35
Diode	H38
Line Terminator	H39
Delay, Inductive, 0.15 usec	P13A
Power Supply Filter & Jumper	P54
Power Supply Filter & Jumper	P55
Hammer Driver	P91, P92
Pulse Shaper	P93
Ribbon Advance	P94
Brake-Clutch One-Shot	P95, P99
Ribbon Drive and Hold	P96
Hammer Driver One-Shot	P97

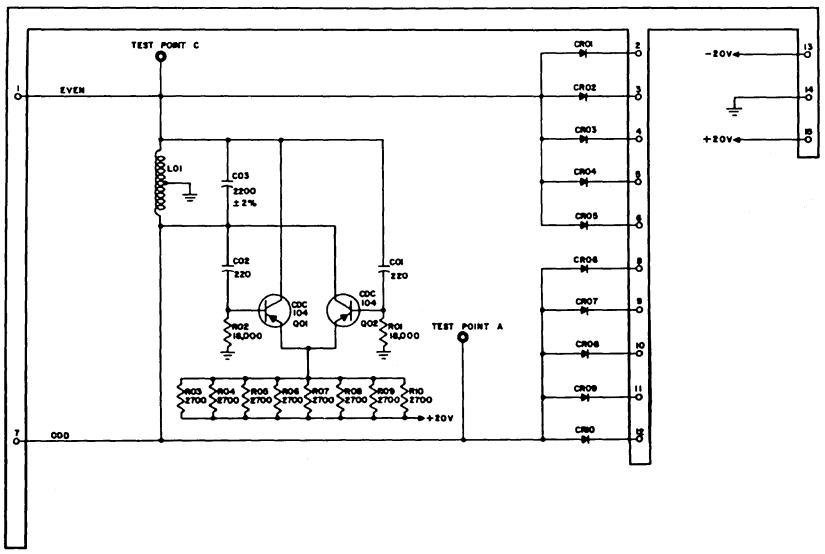
OSCILLATOR

Card Types 01, 01A, and 02A

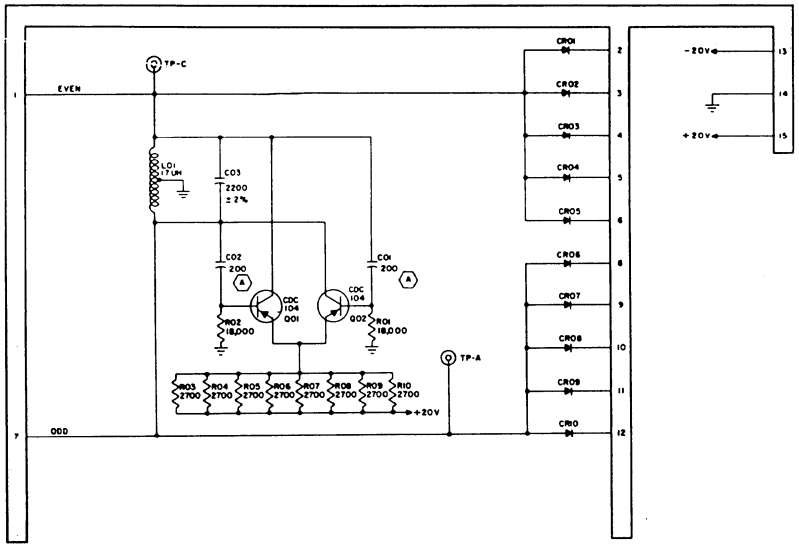
Oscillator cards provide odd and even clock pulses, which provide timing for certain operations, at a nominal frequency of 2.5 megacycles. The circuits of the three cards are similar.

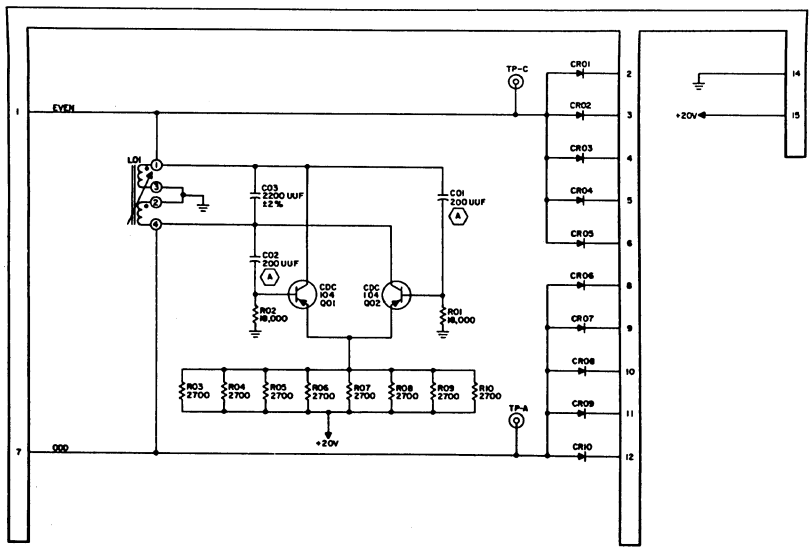
These oscillator cards contain a tank circuit which feeds the multivibrator, consisting of transistors Q01 and Q02. To provide odd and even pulses, the collector of one transistor is tied to the base of the other. When transistor Q01 is conducting, transistor Q02 is cut off; and when Q02 is conducting, Q01 is cut off.

02A differs slightly from 01 and 01A in that it has an adjustable inductor (L01).



Oscillator 01





Oscillator 02A

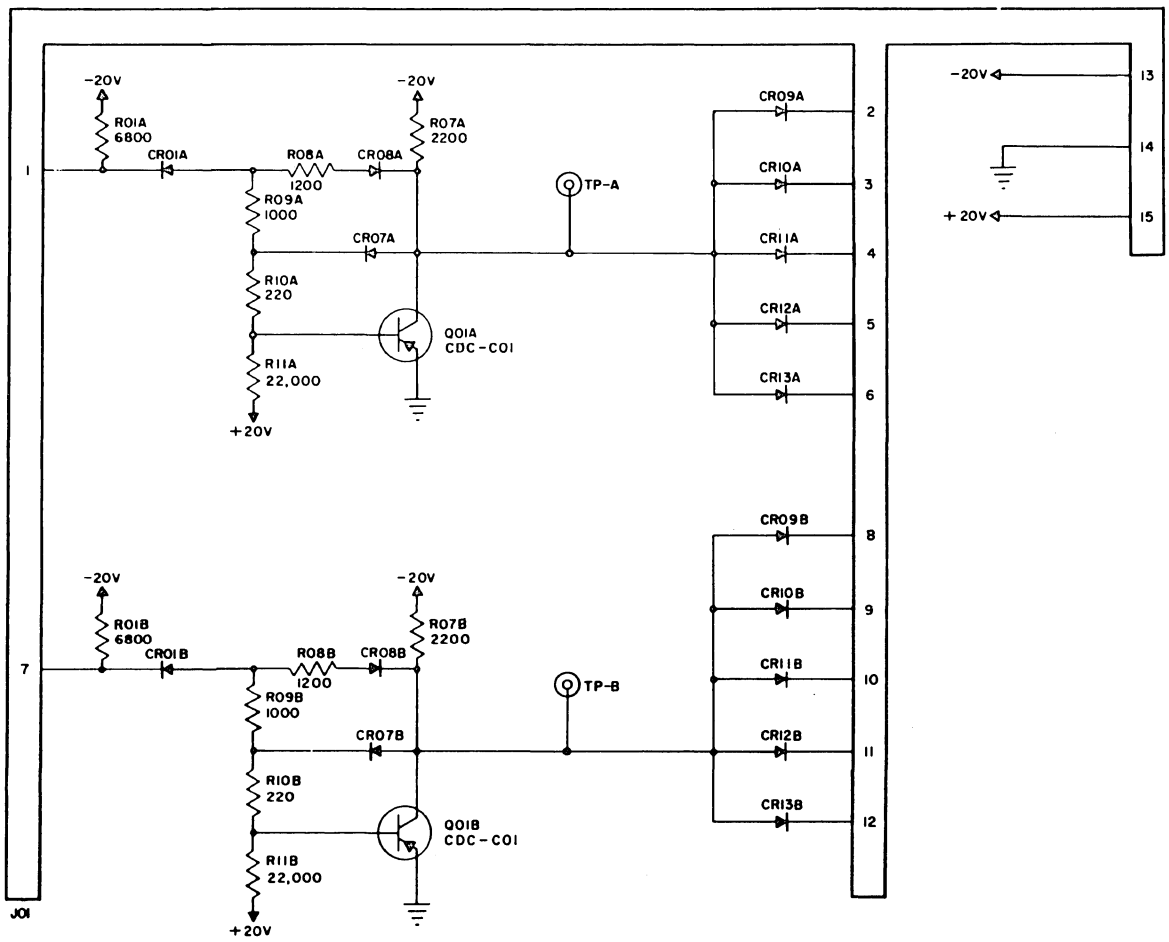
5-01, 01A, 02A-2

Rev. E

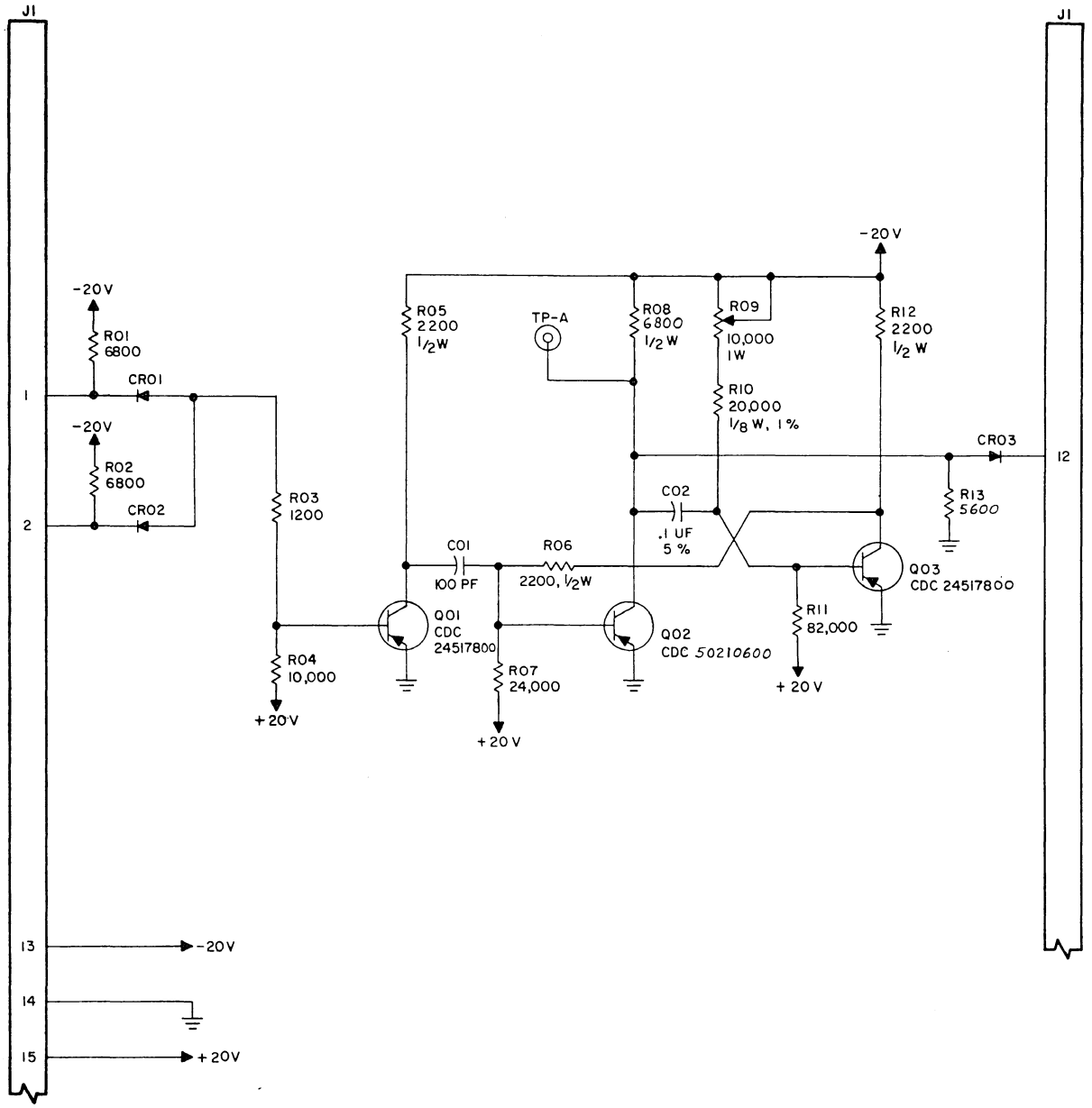
OSCILLATOR AMPLIFIER

Card Type 06

An oscillator amplifier consists of two 1604-type inverter circuits. Except for the type of transistors, it is identical to card type 21A.



Oscillator Amplifier 06



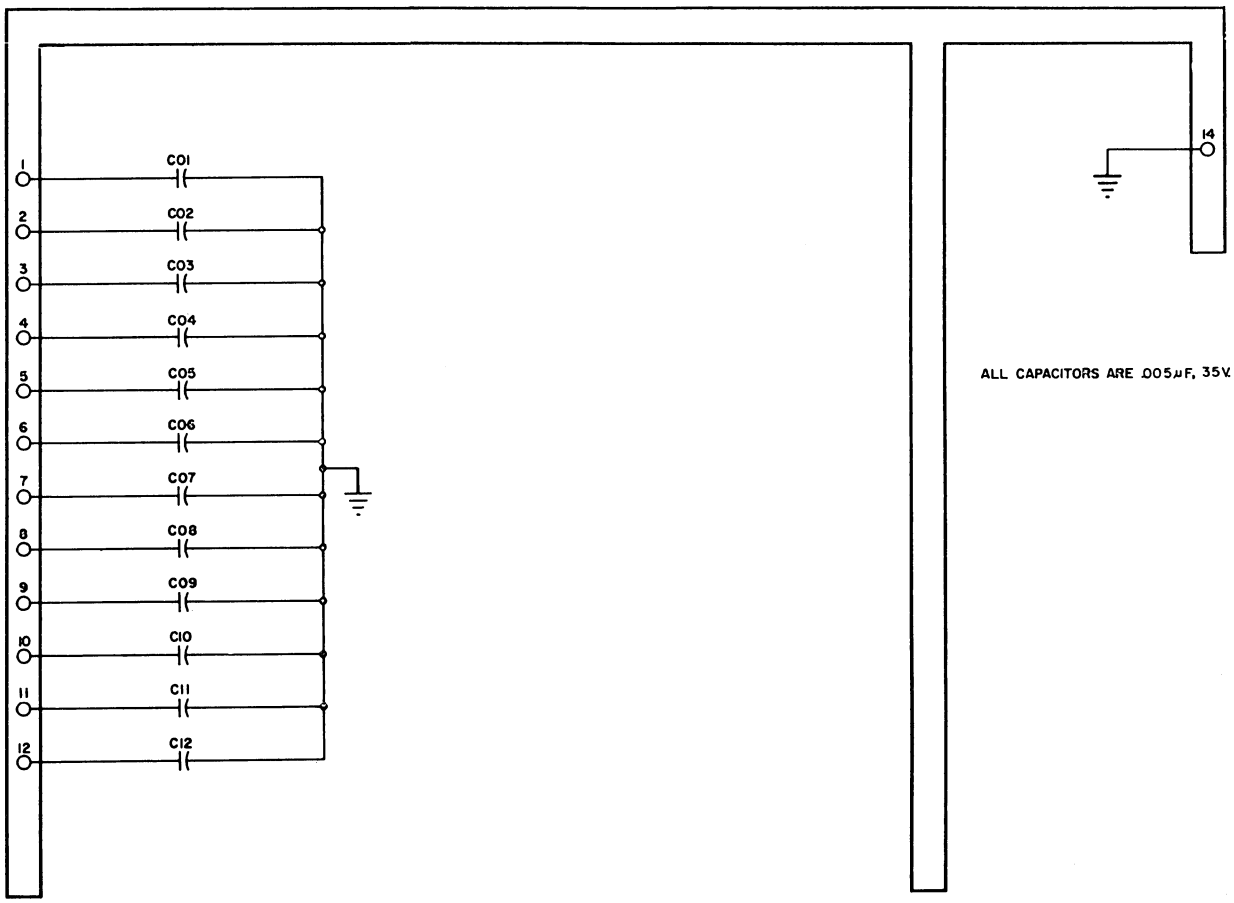
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 1825 4000
   BOARD 1825 4100
3. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES ARE CONTROL DATA DRAWING NUMBER 11801200
   POLARIZED

CAPACITOR

Card Type 50

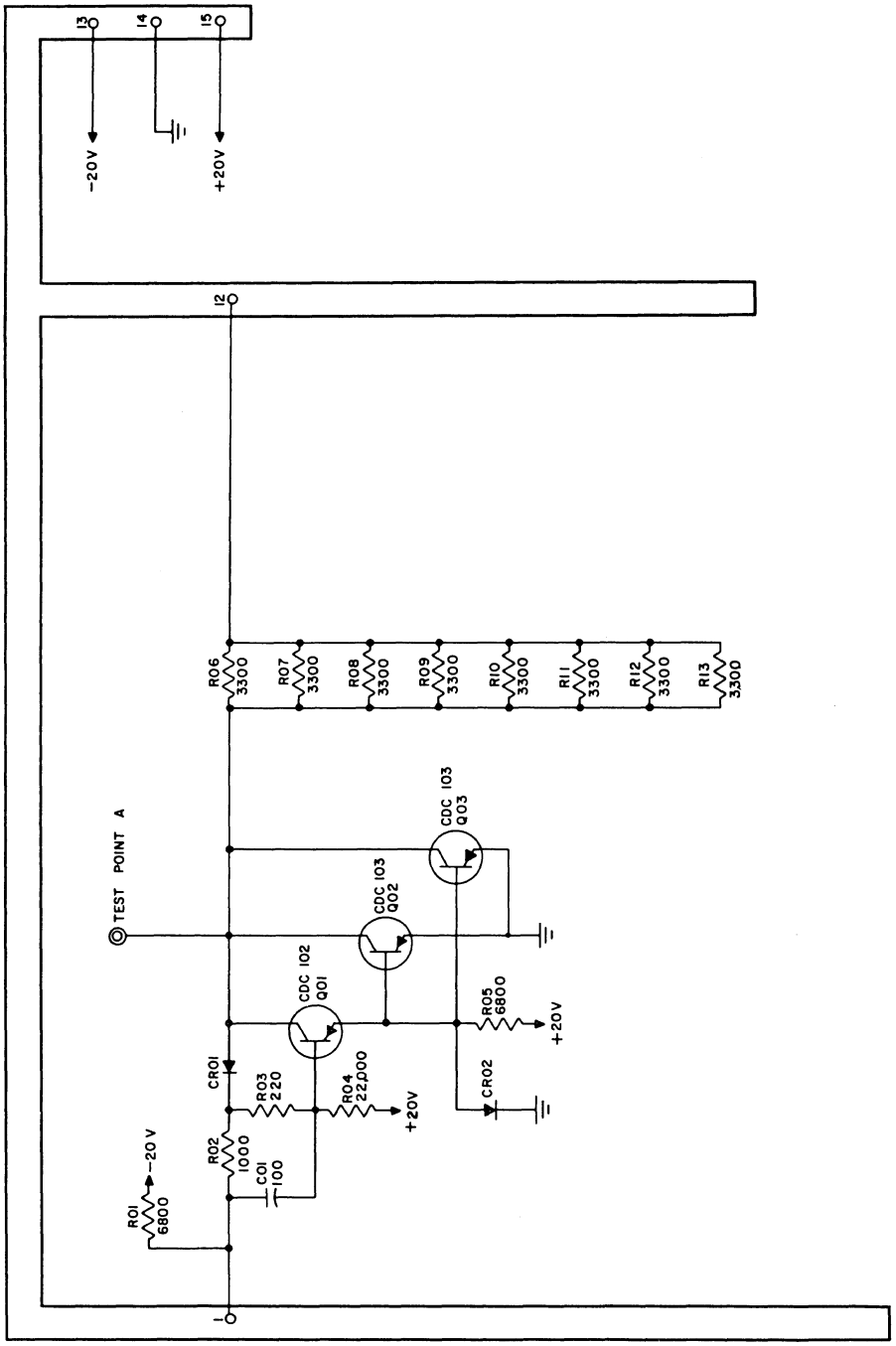
This card contains twelve 0.005 uf, 35v capacitors. It may be used as a delay or as a filter.



SPEAKER DRIVER
Card Type 65

Card type 65 is used to drive a speaker with a low-impedance coil.

The speaker driver has a two stage circuit, input and output. The input stage consists of an inverter which feeds the output stage. The output stage consists of two transistors (Q02 and Q03) which are operated in parallel to protect the transistors and minimize power dissipation. The resultant resistance of the input of the speaker and the resistor bank (consisting of R06, R07, R08, R09, R10, R11, R12, R13) is approximately 400 to 500 ohms. An input of -3v "1" at pin 1 causes sufficient current generation to activate the speaker.



Speaker Driver 65

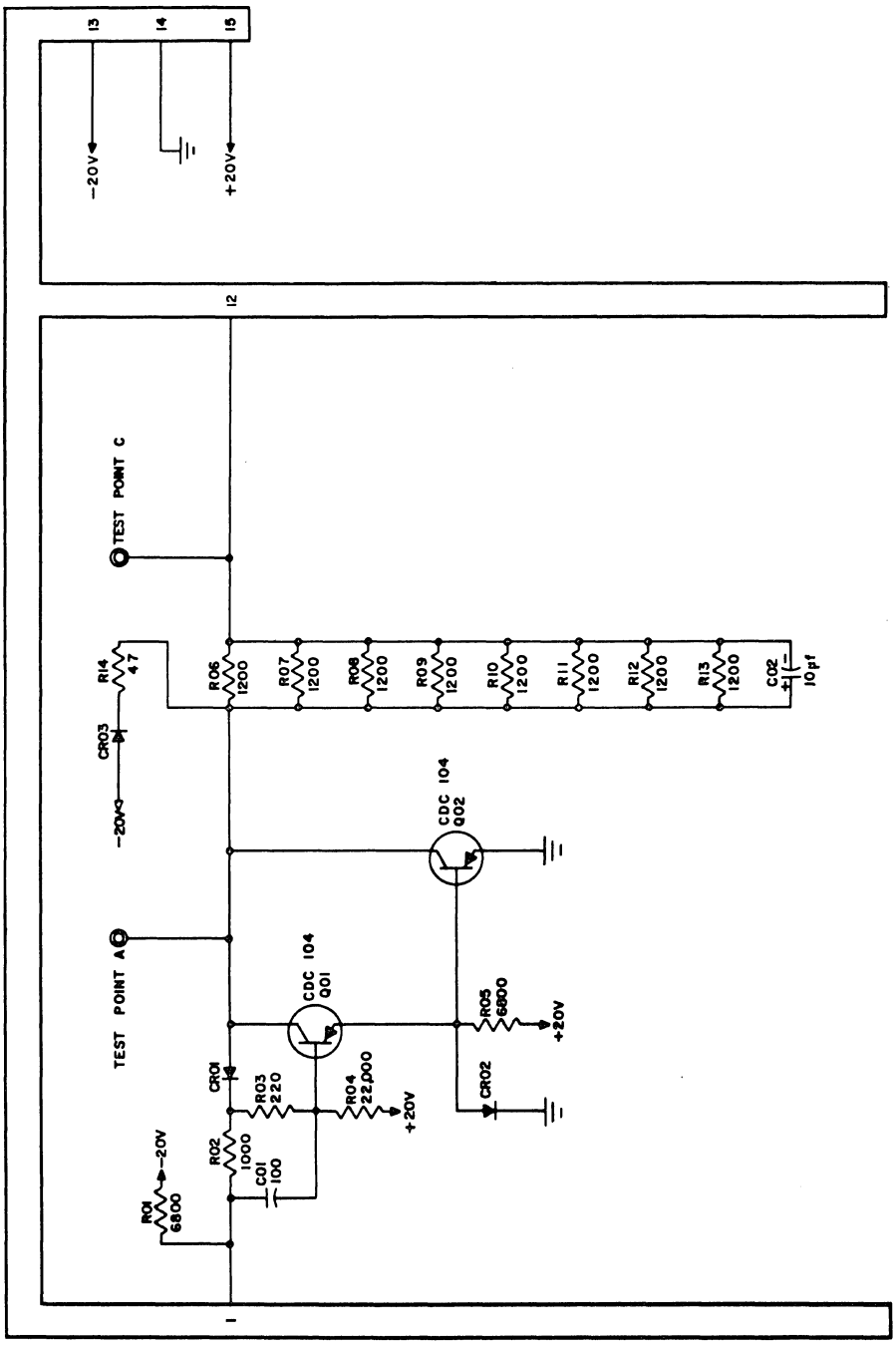
PUNCH PULLER

Card Type 66

This card is designed to handle a current of the order of 100 ma in an inductive load. The circuit is similar to an L^{---} card.

The circuit consists of an emitter follower driving a grounded emitter amplifier. A -0.5v "0" (or ground) input raises the emitter of Q01 to a sufficiently positive potential so that the forward drop across CR02 will cause Q02 to be cut off. A -3.v "1" (or open) input will cause both transistors to conduct heavily, and if pin 12 is fed from -20v, current flow through the resistor network will be about 130 ma.

The connection of diode CR03 clamps the collectors at approximately -20.3v when the circuit switches off.



Punch Puller 66

READ AMPLIFIER

Card Type 70B

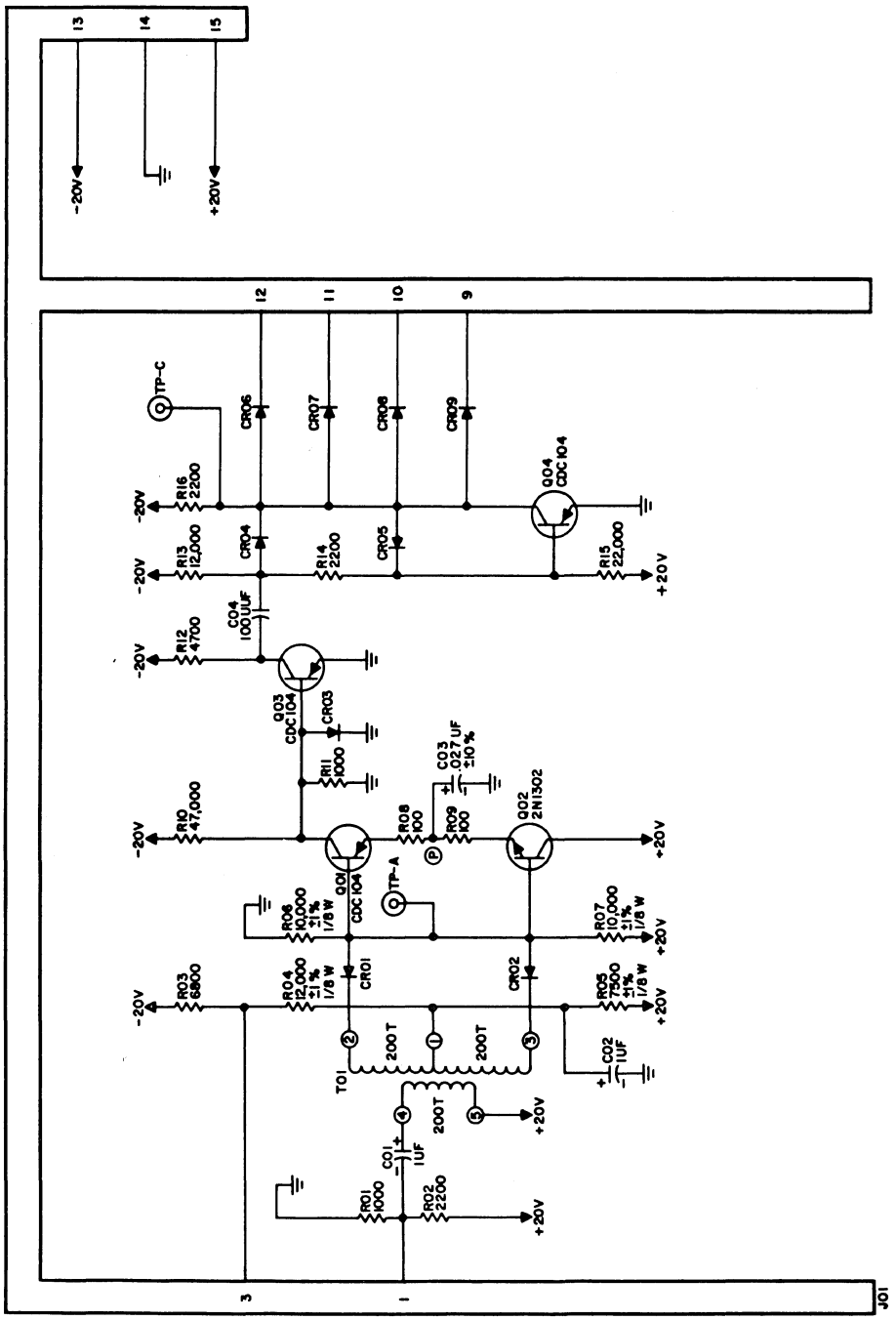
The 70B card detects sinusoidal signals and provides outputs of -3v "1". The input at pin 1 ranges from 6-8 volts (peak to peak) during a read-write mode and from 4-8 volts (peak to peak) during a normal read mode. To insure writing during a read-write mode, the write pulse should be fed to pin 3.

This circuit consists of three stages: the threshold detecting stage, the peak detecting stage, and the output stage. Essentially, the peak detecting stage and the output stage are a standard type of inverter; the only difference is that they are a-c coupled by the capacitor C04.

In the quiescent state, transistors Q01 and Q02 are cut off. As the input signal goes negative, Q01 starts to conduct, drawing its current from the charge on C03 since Q02 is still cut off. The point common to resistors R08 and R09 (point P) follows the negative signal by 2 usec. When the voltage at point P is equal to the input voltage, Q01 is cut off. As the input voltage goes positive, Q02 starts to conduct; it conducts until the input and output voltages at point P are equal. Thus transistors Q01 and Q02 provide pulses of negative polarity from either input polarity which are of greater magnitude than the bias supply voltage which acts as a threshold of detection level.

The peak detecting stage is a common emitter amplifier. When Q03 is cut off, a sharp negative transient is produced across R12. A small capacitor (C04) and a diode couple the peak detector stage and the output stage. The diode clips any positive signals and passes any negative signals. The time constant of C04 and the backward resistance of the diode are chosen to provide a negative spike for approximately 2 usec. This spike turns on transistor Q04, providing an output of "1" for a duration of 2 usec.

The voltages for an input of 4.0 volts (peak to peak) 30 KC should be about -2.0 v/cm and 0.5 v/cm at test points A and C.



Read Amplifier 70B

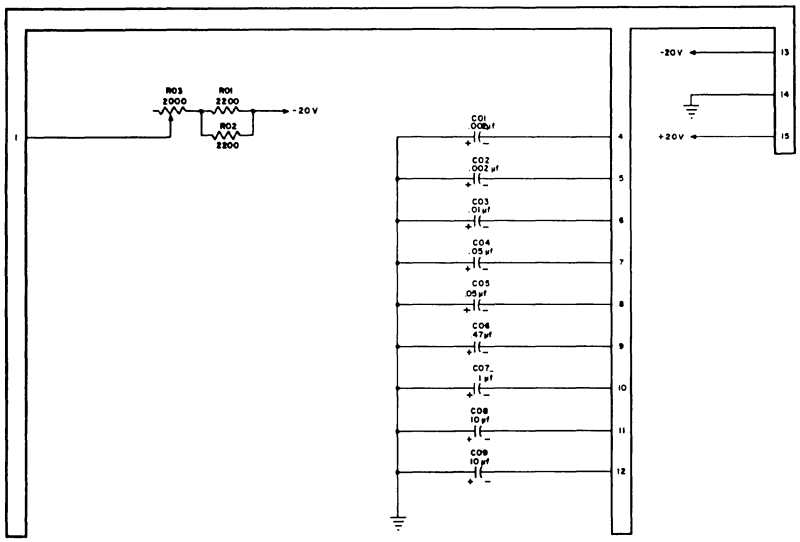
DELAY CAPACITORS

Card Types 73, 73A, 77, 82

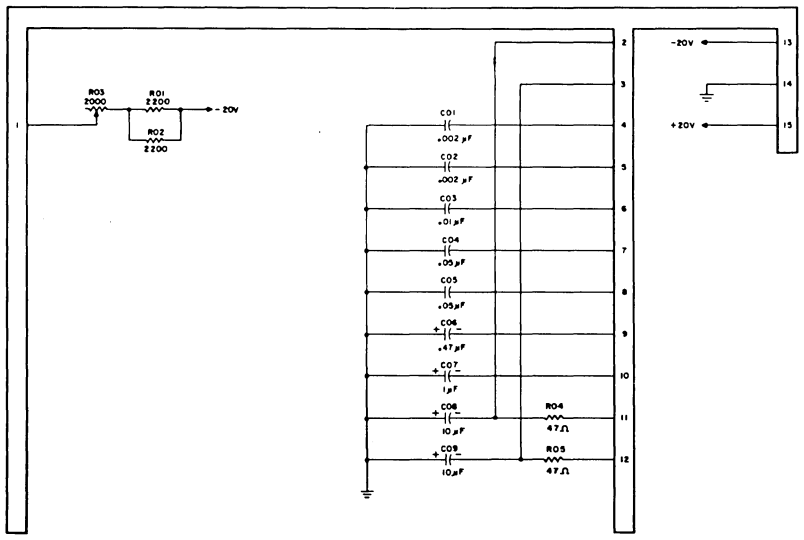
The purpose of a delay circuit is to provide an interval of time between successive logical operations. This is achieved by connecting a capacitor from the signal line to ground. The time elapsing between the input and output of a pulse, the time required to charge the capacitor, is known as delay time. The delay time is a function of the size of the capacitor and the rate at which it receives current. Other things being equal, the larger the capacitor, the longer the delay time; the smaller the capacitor, the shorter the delay time.

In the adjustable delay circuit, the delay time can be altered by varying the resistance in series with the capacitor. Varying the resistance increases or decreases the current flow to the capacitor, thereby increasing or decreasing the delay time. In the non-adjustable delay circuit, the delay time is fixed; it is a function of the size of the capacitor only.

The circuits contained on these cards may be used alone to provide short delays. To obtain long delays (greater than 10 usec) with greater stability, they may be used in conjunction with card type 97.



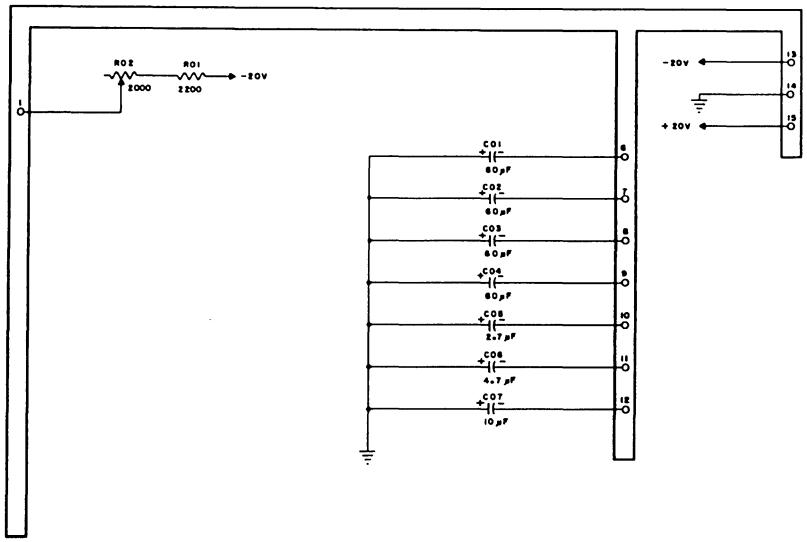
Delay 73

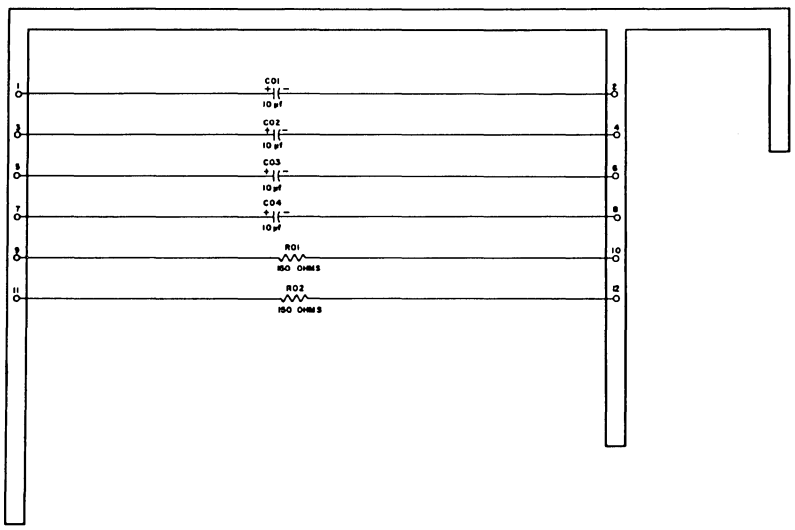


Delay 73A

5-73, 77, 82-2

Rev. E





Delay 82

5-73, 77, 82-3

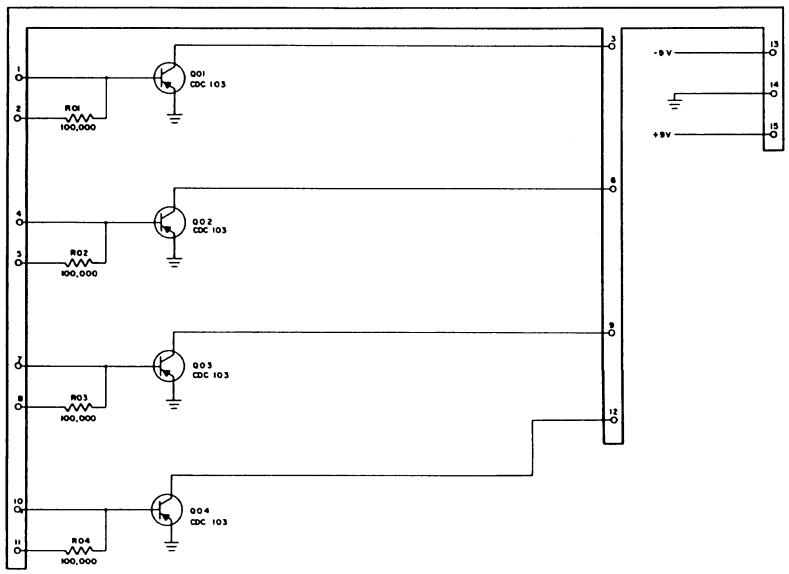
Rev. E

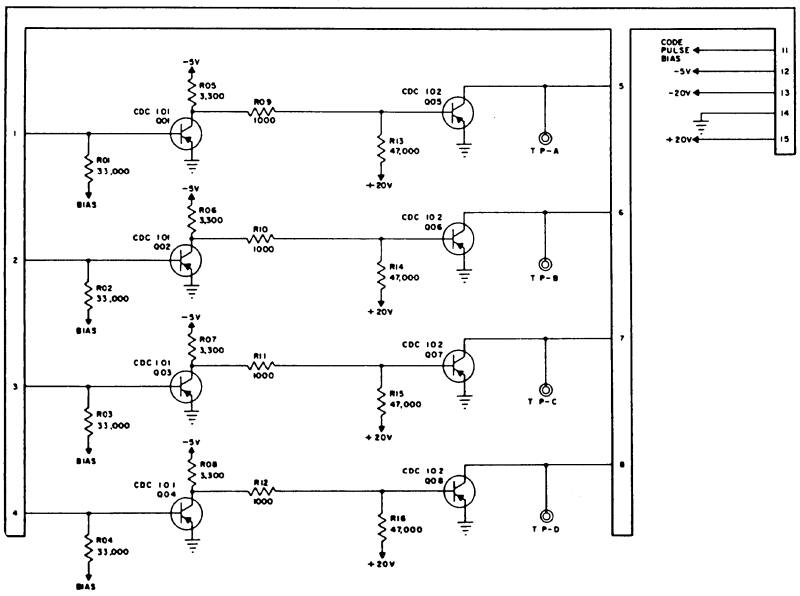
READER LEVEL AMPLIFIER

Card Types 75 & 75A

The circuits on card type 75 each consist of a single transistor connected as a grounded-emitter amplifier. A positive-going input causes the transistor to be cut off, while a negative-going input causes it to conduct. The transistor has a biasing resistor connected to its base, so that the sensitivity of the amplifier may be adjusted.

Card type 75A is designed to convert solar cell outputs from a paper tape reader into -0.5v outputs, representing a "0" in 1604-type logic. If no hole is sensed, the output transistor will be cut off. When light strikes the solar cell, the circuit input will be approximately +0.4v. This causes the input transistor to cut off and the output transistor to conduct. At other times, the input will be approximately an open circuit and the bias must be such that the input transistor is in its conduction state.





Reader Level Amplifier 75A

5-75 & 75A-2

Rev. E

READER BRAKE-CLUTCH DRIVER

Card Type 76A

FUNCTION

This card controls the starting and stopping of tape in a paper tape reader by alternately energizing the clutch and brake coils.

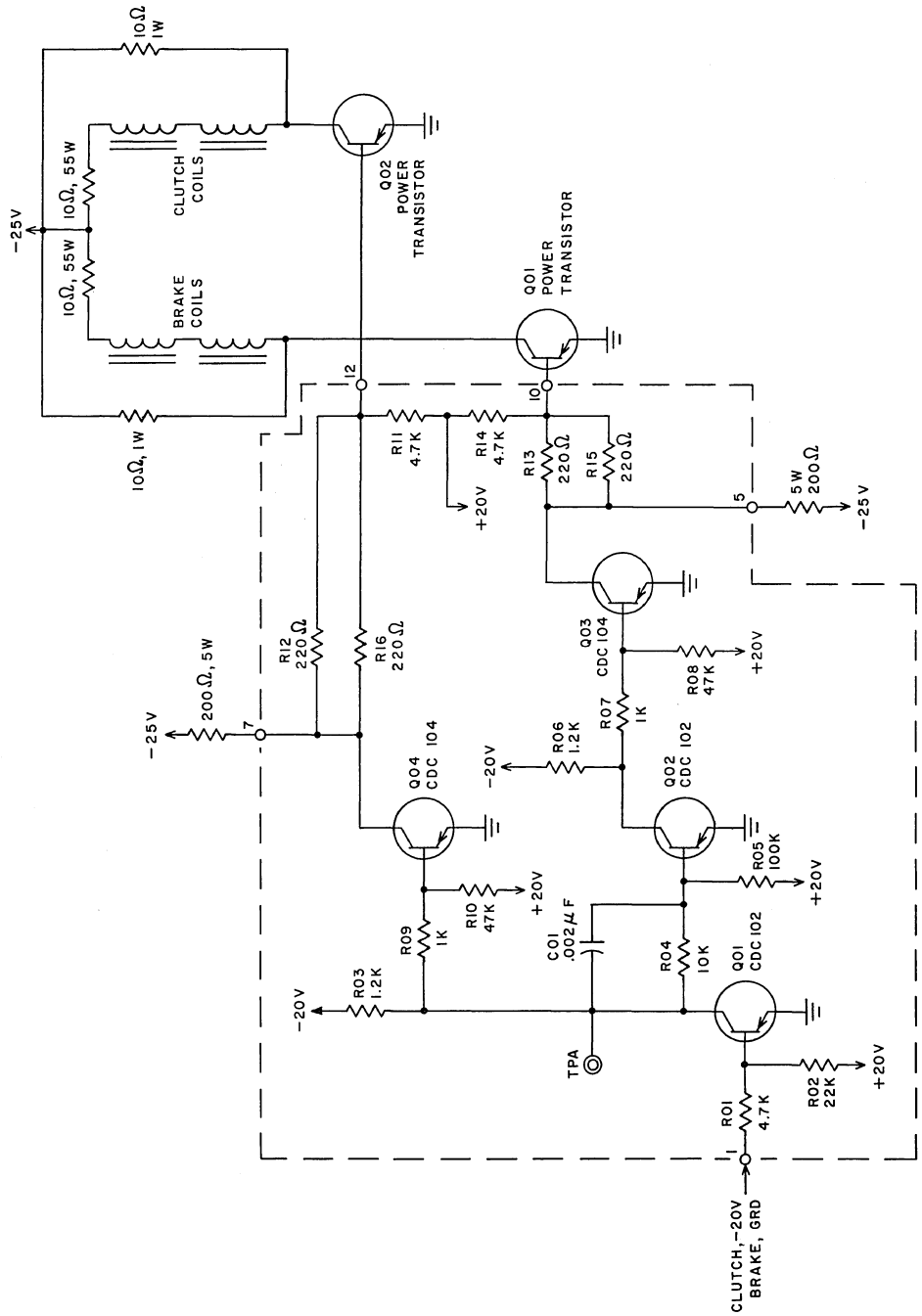
OPERATION

The clutch signal, a -20 volt potential applied to the base of Q01, energizes the clutch coils and starts the tape. The bias is determined by the voltage dividing network. The collector of Q01 drives transistors Q02 and Q04 to cut off. This forces the base of Q03 negative and Q03 conducts. A voltage dividing network supplies a positive base drive to power transistor Q01 and a negative base drive to power transistor Q02. The clutch coils are energized and the tape is advanced.

When the external equipment drops the clutch signal to ground, the brake coil is energized and the tape stops. Q02 and Q04 conduct because Q01 is cut off. The base of Q03 goes positive and power transistor Q01 receives the negative base drive necessary to energize the brake coils.

Diodes are used in conjunction with the brake and clutch coils. These diodes prevent back EMF induced by the coils when the transistors switch off from driving the collectors of the power transistors too far above the supply voltage.

The two brake electromagnets are identical coils connected in series. The clutch electromagnets are connected in similar fashion.



Reader Brake-Clutch Driver 76A

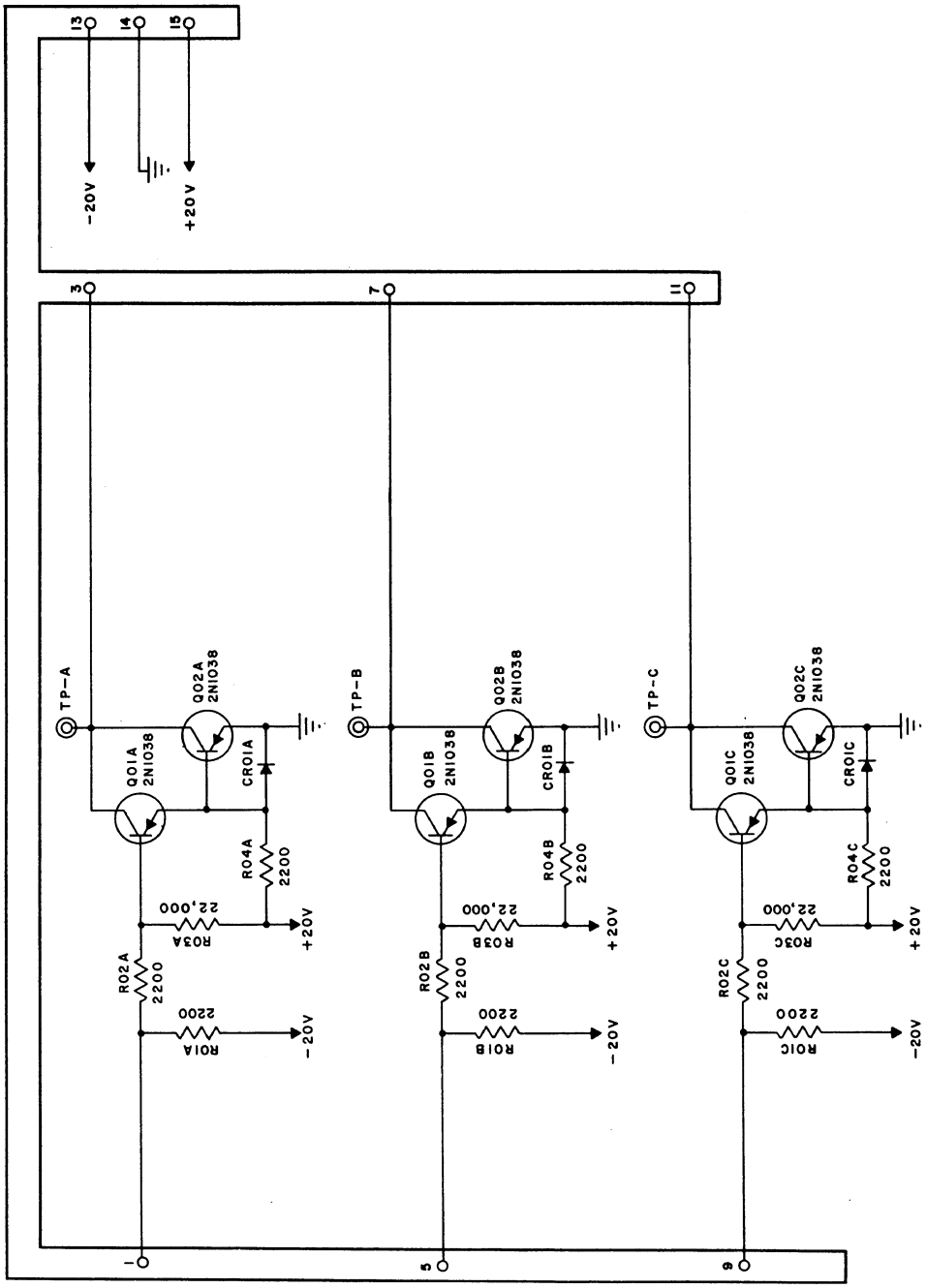
PUNCH PULLER

Card Type 86

(Note: Card Type 86A is identical except different transistors)

This circuit is designed to activate the magnets in a paper tape punch. It can switch a current of the order of 1.25 amperes at - 28V.

The circuit is driven by an L--- card. A - 18V input causes both transistors to switch to the conduction state. A - 0.5V input causes conduction through Q01 to decrease and the forward drop across CR01 cuts off Q02.



Punch Puller 86

HAMMER STORAGE
CARD TYPE 91

The design of the 91 card combines a binary storage location with an inverter of high current-switching ability.

SWITCH

The inverter-switch portion of the 91 card is capable of conducting 400 milliamperes continuously. A "1" input to Q03 from Q02 causes conduction. Output diode CR18 allows the card to drive one standard inverter or flip-flop. Another 91 card in the "0" state, connected to pin 10, acts as a block and prevents Q04 from conducting.

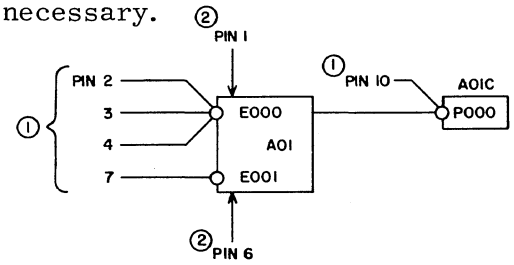
STORAGE

The storage flip-flop, a simplified version of the 1604 flip-flop series, contains two transistors, Q01 and Q02. A "1" input to Q01 (pins 1-4) sets the flip-flop and causes Q04 to conduct if a "1" is present at pin 10. A "1" input to Q02 (pins 6-7) clears the flip-flop.

The 1604 series of inverters and flip-flops used by Control Data have isolation diodes placed at their output and none at their input. A 1604 card may therefore drive only as many cards as it has output diodes (a maximum of eight). The 91 card, which has three isolation diodes on the set side of its input and one on the clear side, may be driven directly by Q04 of other 91 cards. Because of the high switching current property of Q04, it is possible to drive up to 120 91 cards with only one 91 driver. The result is elimination of the slave inverter pyramid usually required to drive so many cards. In addition to the isolated inputs, the 91 card has a standard input on the set and on the clear side for inputs from the 1604 series of logic cards. The isolated and non-isolated inputs are ANDed together within the 91 card.

SYMBOL

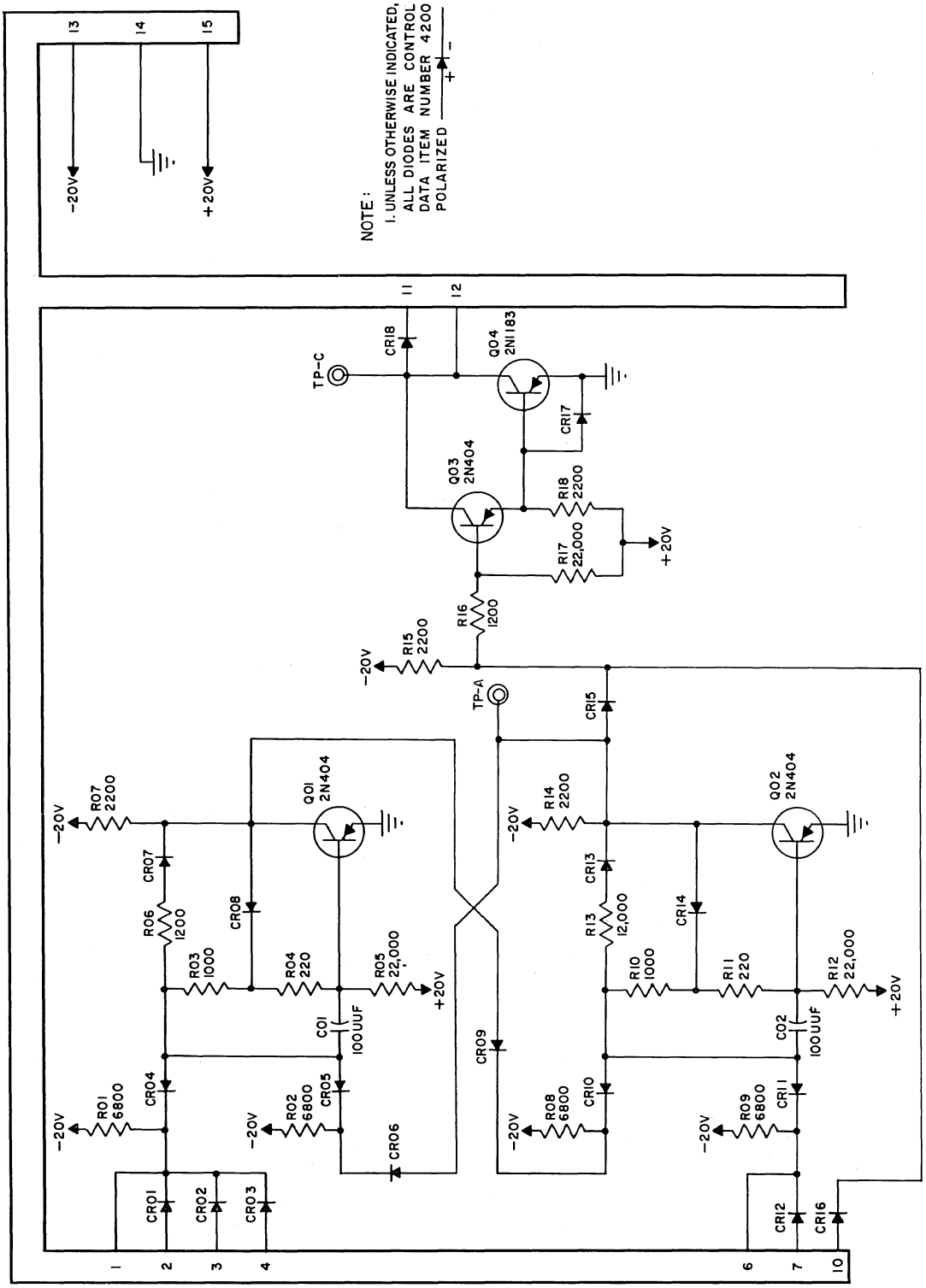
The combination of isolated and non-isolated inputs on the 91 card made a new logic symbol necessary.



Notes:

1. Feed from pin 12 of other 91 cards.
2. Treat as standard 1604 input.

Logic Symbol, Card Type 91



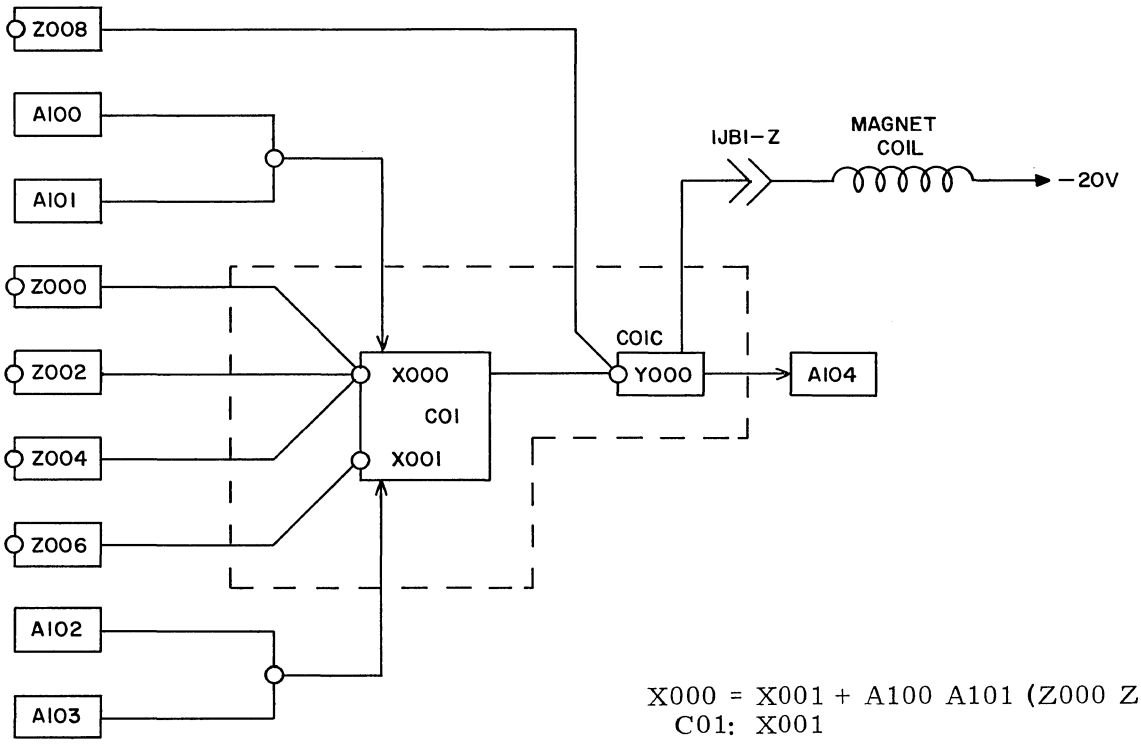
Schematic Diagram, Card Type 91

TESTPOINTS

There are two testpoints located on the 91 card, TP-A and TP-C. TP-A registers a "1" when the flip-flop is set. TP-C registers a "0" when the inverter-switch is conducting.

EQUATIONS

91 card equations are similar to those for standard 1604 logic cards. An exception is the use of parenthesis around terms connected to isolated inputs. A sample circuit and its associated equations is shown below.



X000 = X001 + A100 A101 (Z000 Z002 Z004)
C01: X001

X001 = X000 + A102 A103 (Z006)
C01A: X000: Y000

Y000 = X001 (Z008)
C01C: A104: 1JB1-Z

Sample Logic Diagram With Equations

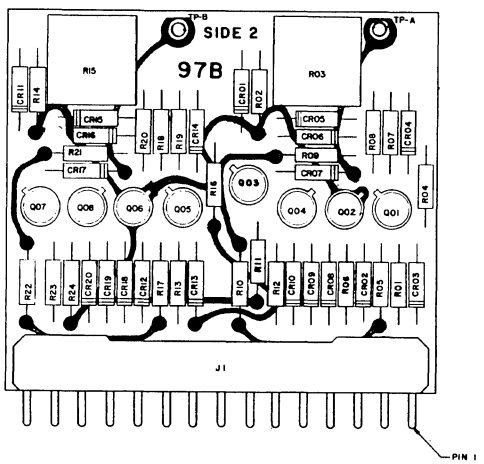
DELAY

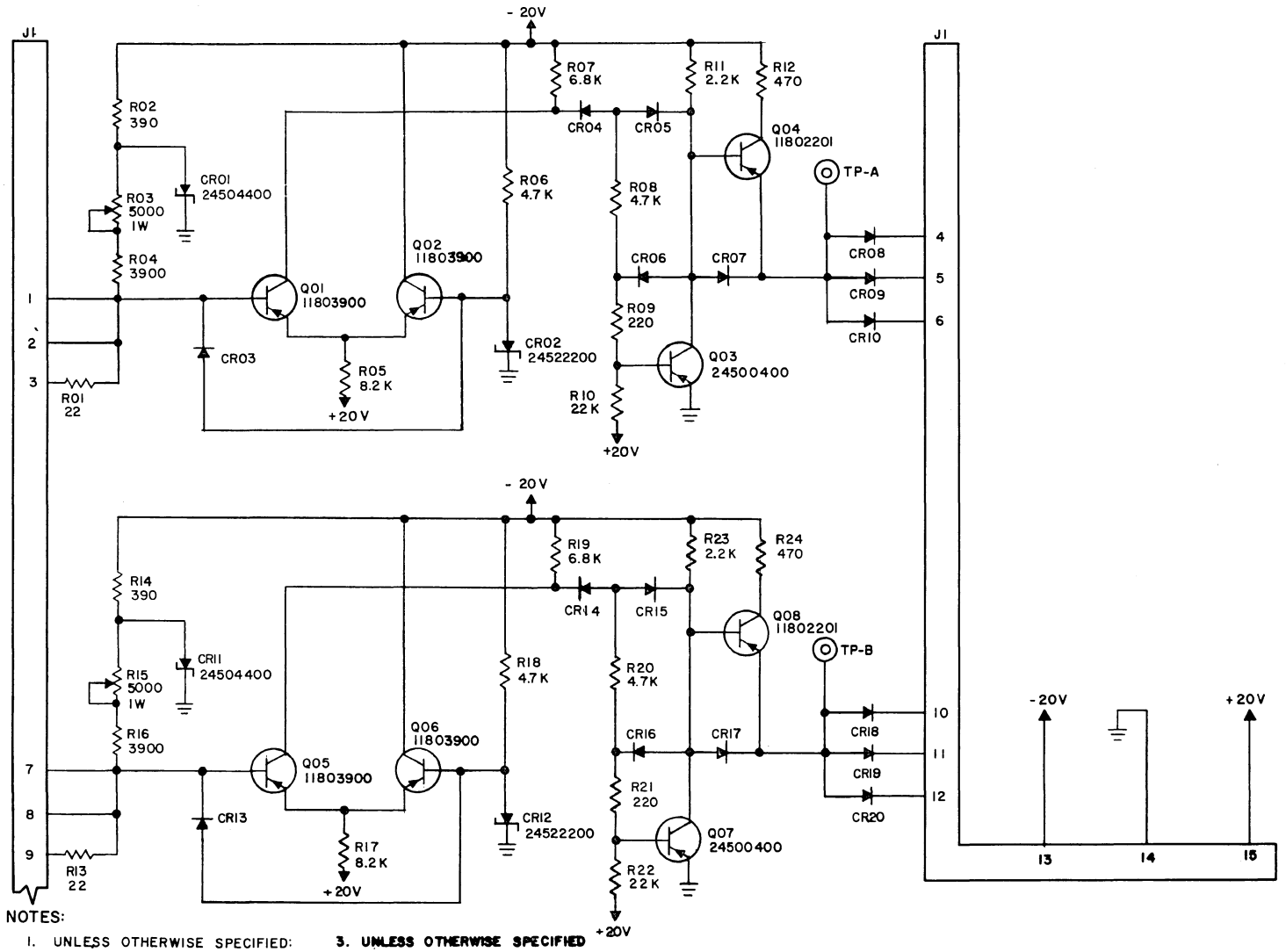
Card Type 97 B

This circuit is designed to provide stable delay times of relatively long duration in 1604-type logic. It consists of a double inverting network such that the circuit does not produce an overall logical inversion. The input to the circuit must be connected to an external capacitor. The delay time obtained can be adjusted approximately + 15% by means of the variable resistor R03.

The circuit consists of a zener controlled capacitor charging network (R03, R04), a differential comparator with a threshold of -2.6v and a compatible inverter with 3 output logic diodes for forming AND logic.

The external delay capacitor can be connected to either pin 2 or pin 3. Pin 3 contains a series 22-ohm resistor to protect against damage from peak currents when using large capacitors.





NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ± 5%.
   ALL CAPACITORS ARE ± 20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 24406901
   BOARD 24406600
3. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE CONTROL DATA CORP. DWG. NO. 1101200. POLARIZED

Delay 97B

5-97-2

Rev U

CLOCK OSCILLATOR-AMPLIFIER
Card Type C01

GENERAL

The clock oscillator-amplifier shown on page 5-C01-2 is essentially a tank circuit which may be tuned through a small range around 8 megacycles, with drive provided to the tank by two transistor amplifiers. The transistors are connected in a push-pull configuration, with the two circuit inputs directly connected to their bases. When the transistor inputs are provided with cross-coupled feedback from the oscillator transformer secondary, a continuous self-oscillation is maintained.

The circuit is designed so that, if external drive is provided to the inputs, the two transistors will operate as sine wave amplifiers, providing a two-phase output at the tank frequency.

PYRAMID CONNECTION

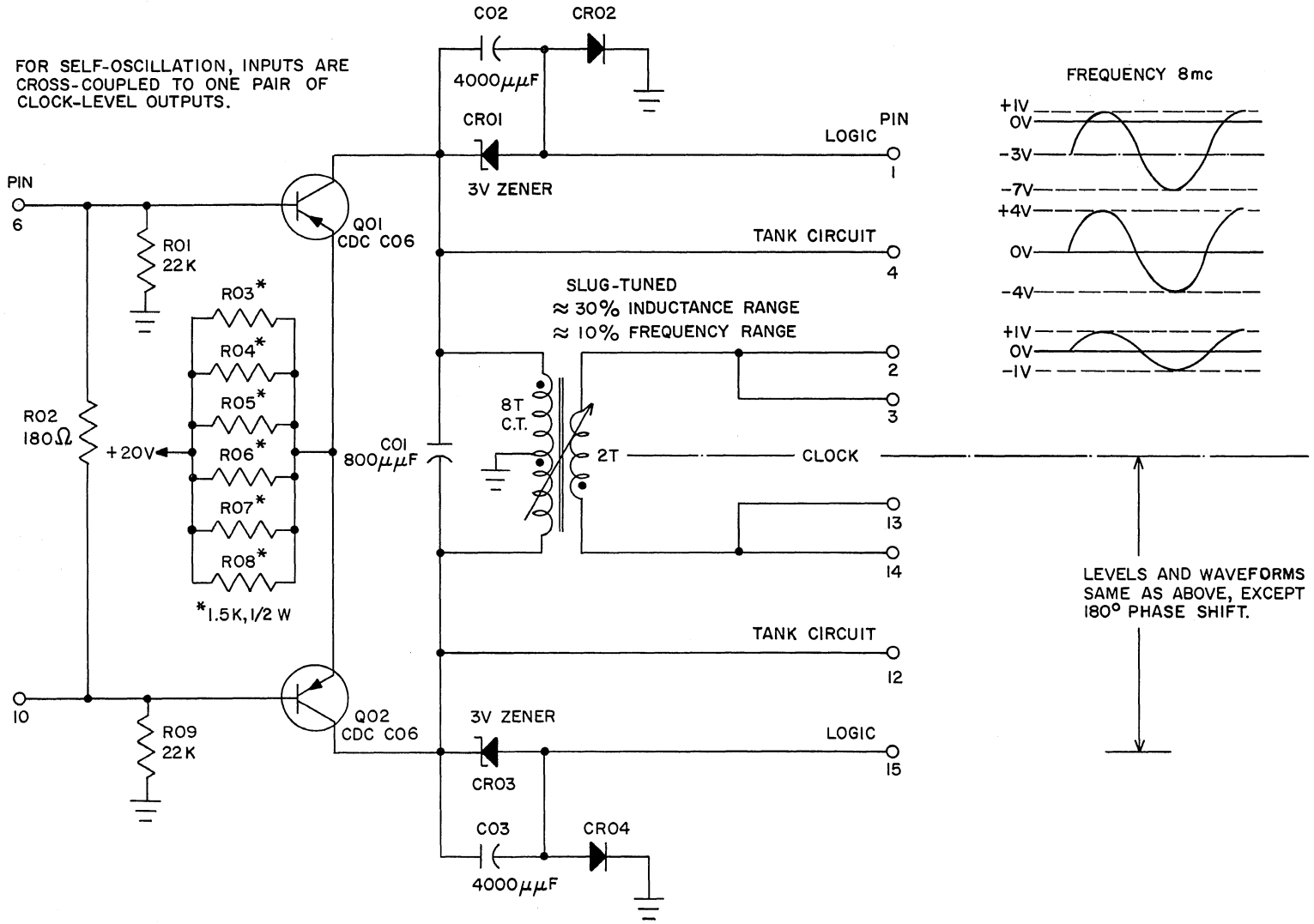
The computer timing configuration for which this circuit is designed is an oscillator-amplifier pyramid, as shown on page 5-C01-3. The master oscillator is a clock circuit connected as a feedback oscillator. To avoid undue loading effects, the master oscillator is permitted to drive only 2 amplifiers.

The ranks of amplifiers are clock circuits which receive external inputs and function as push-pull sine wave amplifiers. Each amplifier is capable of driving 4 others; thus, the pyramid effect is produced. Each amplifier in a rank must be in phase with every other amplifier in that same rank, although it is not necessary for the ranks to be in phase with each other or with the master oscillator. Outputs to the logic are taken only from the final rank of amplifiers.

CIRCUIT OPERATION

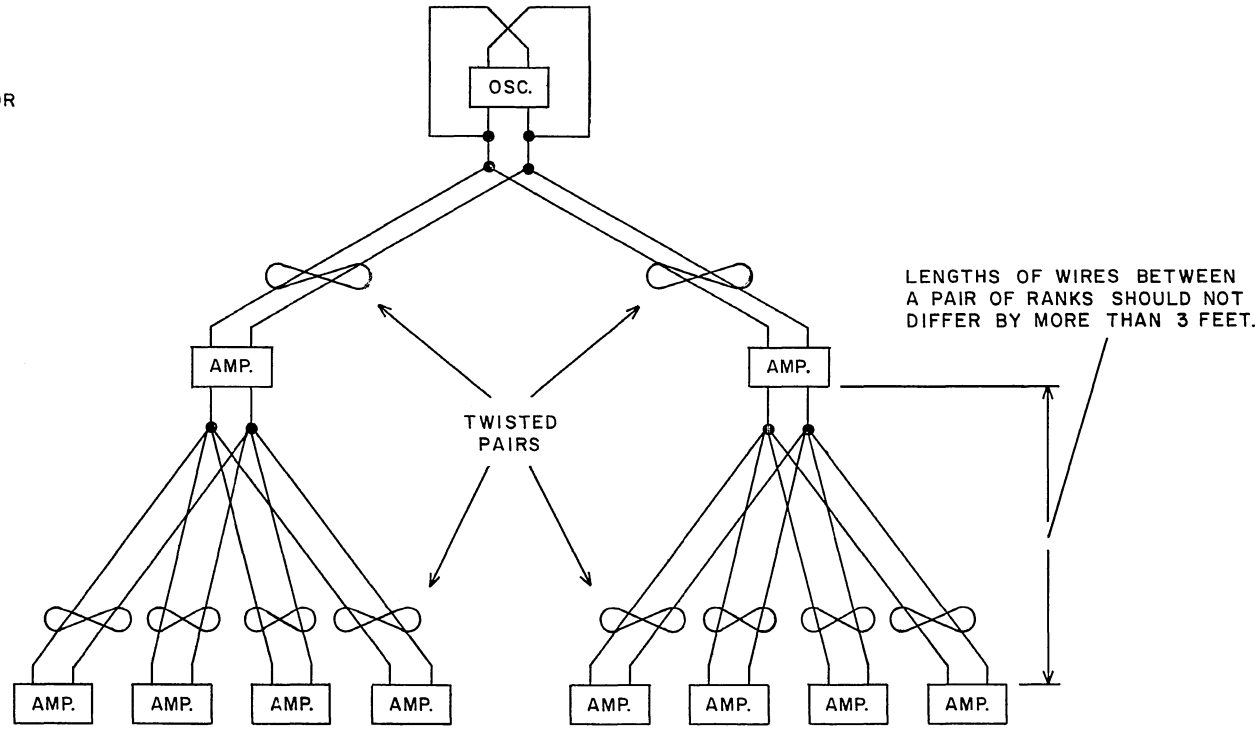
The driving transistors Q01 and Q02 are CDC C06's and are connected in a push-pull configuration. Only one transistor is necessary to sustain oscillation; however, two transistors greatly increase the ability of the circuit to drive an unsymmetrical load.

Clock amplifier logic outputs are restricted to driving AND loads only. Through jumpered connections, an amplifier may drive up to 10 loads. Ideally, this is distributed



Clock Oscillator-Amplifier C01

Clock Pyramid C01



NOTE:

1. MASTER OSCILLATOR MAY DRIVE 2 AMPLIFIERS.
2. EACH AMPLIFIER MAY DRIVE 4 FOLLOWING AMPLIFIERS.
3. ALL AMPLIFIERS IN THF SAME RANK ARE IN PHASE WITH EACH OTHER, BUT NOT NECESSARILY IN PHASE WITH ANY OTHER RANK OR WITH THE MASTER OSCILLATOR.

with 5 loads on each output phase; however, the loading may be unbalanced to 8 and 2, if necessary.

The characteristics of transistors Q01 and Q02 are such that they have a power handling capability of 150 mw at 25°C ambient. The average transistor dissipation in an oscillator circuit is of the order of 60 mw.

An 800 uuf silver-mica capacitor C01 having a low temperature coefficient and good stability is used in the tank circuit to resonate with the transformer inductance at a center frequency of 8 megacycles. The transformer inductance may be tuned through a range of approximately 30 percent by means of a low permeability ferrite slug. This has the effect of shifting the tank frequency through a range of approximately 10 percent.

The peak-to-peak signal develped across the tank is restricted to approximately 8v by the clamp diodes CR01 and CR04. The printed circuit card provides outputs at pins 4 and 12 at which this sine wave appears. If necessary, all tanks in a rank of amplifiers may be locked in phase with one another by connecting these outputs in parallel.

A logic-level signal is a sine wave about -3v, with peaks at +1v and -7v. It is produced by using a zener diode to shift the d-c reference level of the tank output. Logic-level outputs are taken only from the last rank of the clock pyramid and are available at pins 1 and 15.

The circuit on page 5-C01-2 provides a clock-level output at pins 2, 3, 13, and 14, which is taken from the secondary of the tank transformer. The secondary winding consists of 2 turns, while the primary winding is 8 turns, center-tapped; therefore the clock-level output is a sine wave about ground with a peak-to-peak amplitude of approximately 2v.

The clock-level signals are used as drive signals throughout the clock pyramid, as shown on page 5-C01-3. All wires used to transmit clock-level signals must be twisted pair, and the distance over which the signal is transmitted should be less than 15 feet. In addition, there should be less than a 3 foot variation in the lengths of wire used to transmit drive signals between a given pair of ranks.

PROCEDURE FOR TUNING A CLOCK PYRAMID

A scope equipped with a differential or dual-trace preamplifier, such as a Tektronix type CA, may be used for tuning the pyramid. The probe leads should be equal in length and must be grounded at the cards. The scope should be externally synchronized during step 3. Use the master oscillator for this.

Step 1.

Adjust the transformer of the master oscillator to the correct computer frequency. This may be done by setting the horizontal sweep at 0.1 usec/cm and adjusting until 8 peaks are seen across the 10 cm scope grid, if the desired frequency is 8 megacycles.

Step 2.

With the scope on a sensitive range, adjust one of the amplifiers in Rank 1 for maximum amplitude.

Step 3.

Using external sync, adjust the remaining amplifiers in Rank 1 to be in phase with the reference amplifier tuned in step 2. This may be done with a differential preamplifier, by inverting one signal and adding algebraically, and adjusting for minimum deflection with the scope on a sensitive range.

Other ranks are tuned according to steps 2 and 3.

GROUND RULES

A. Clock-level outputs.

1. The oscillator may drive 2 amplifiers in addition to providing its own feedback.
2. Each amplifier may drive 4 other amplifiers.
3. Interconnecting wires between ranks of amplifiers and from the master oscillator to rank 1 must be twisted pair.
4. Signals may be transmitted up to 15 feet.
5. There should be no more than a 3-foot difference in the lengths of interconnecting wires between a given pair of ranks.

B. Tank circuit output.

1. This is used only to phase-lock the tanks within a single rank of amplifiers, if necessary.

C. Logic-level outputs.

1. Clock outputs must always connect to logic card AND inputs.
2. A maximum of 10 loads may be driven.
3. A maximum of 8 loads may be driven by any single output; with 8 loads on one output, the opposite-phase output of that amplifier may drive only 2 loads, so that the total number does not exceed 10.

CLAMP

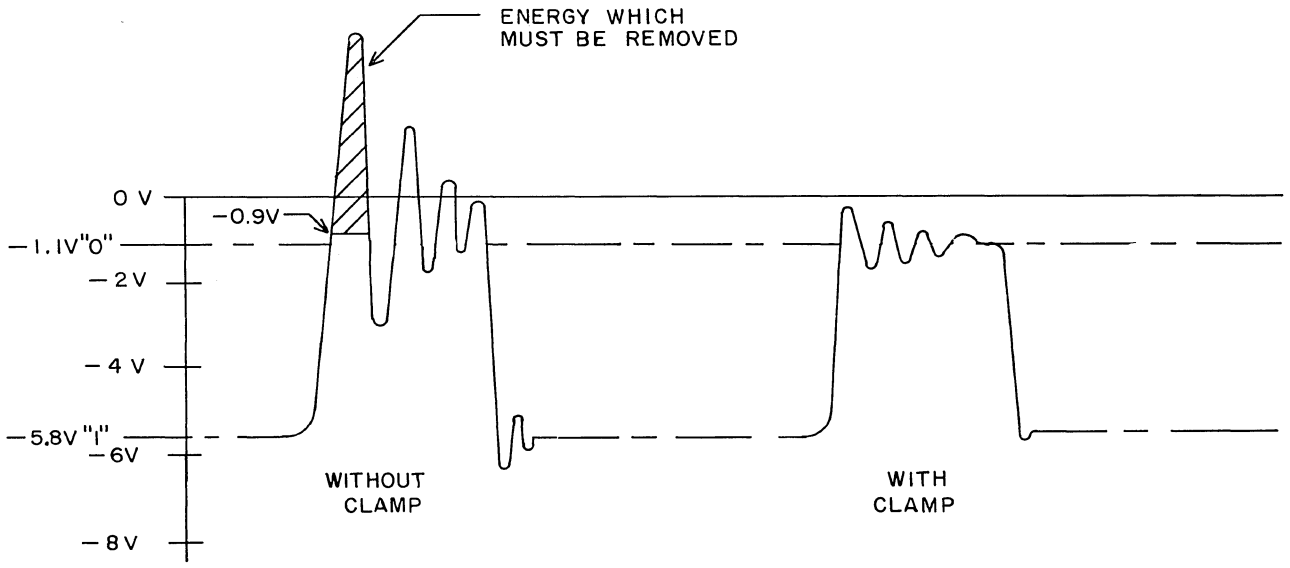
Card Type C02

This circuit provides a clamp for logic circuit connecting lines, so that ringing is minimized. If sufficient energy is removed from the first overshoot, the remainder of the ringing has an amplitude less than the logic circuit threshold. A schematic of the clamp circuit is presented on page 5-C02-2, with typical waveforms showing its effect on a line having excessive ringing.

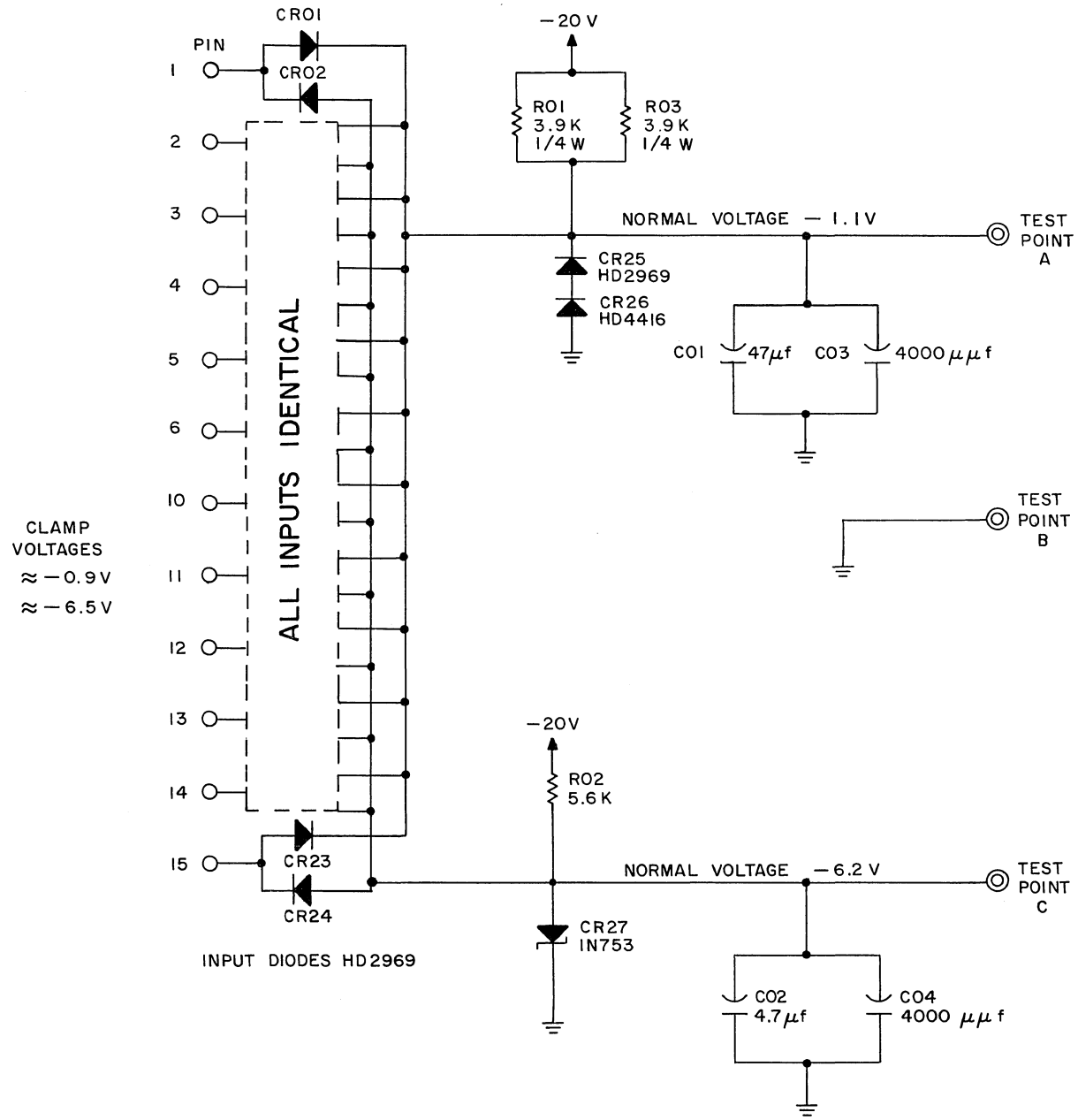
The clamp voltage in the positive direction is the sum of the forward drops across diodes CR25 and CR26, less the drop across the input diodes. It is approximately -0.9v.

The clamp voltage in the negative direction is the sum of the drop across zener diode CR27 plus the drop across the input diodes. It is approximately -6.5v.

Filtering is provided by capacitors C01, C02, C03, and C04. Due to their large area C01 and C02 present an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitors C03 and C04 in order to filter out high-frequency spikes.



Typical Logic Line Voltage, 3600


CR01
PIN
1
CR02
2
3
4
5
6
10
11
12
13
14
15
ALL INPUTS IDENTICAL
CR23
CR24
INPUT DIODES HD2969
CLAMP VOLTAGES
≈ −0.9 V
≈ −6.5 V
−20 V
R01 3.9K 1/4 W
R03 3.9K 1/4 W
NORMAL VOLTAGE — 1.1V
TEST POINT A
CR25 HD2969
CR26 HD4416
C01 47μf
C03 4000μμf
TEST POINT B
−20V
R02 5.6K
NORMAL VOLTAGE −6.2 V
TEST POINT C
CR27 IN753
C02 4.7μf
C04 4000 μμf

Clamp C02

EMITTER FOLLOWER
Card Type C07C

FUNCTION

The function of this circuit is to convert inputs received from a terminated 200-ohm delay line into outputs suitable for driving a logic card load. This circuit provides a high impedance load for the delay line, avoiding excessive current drain which affects its operating characteristics.

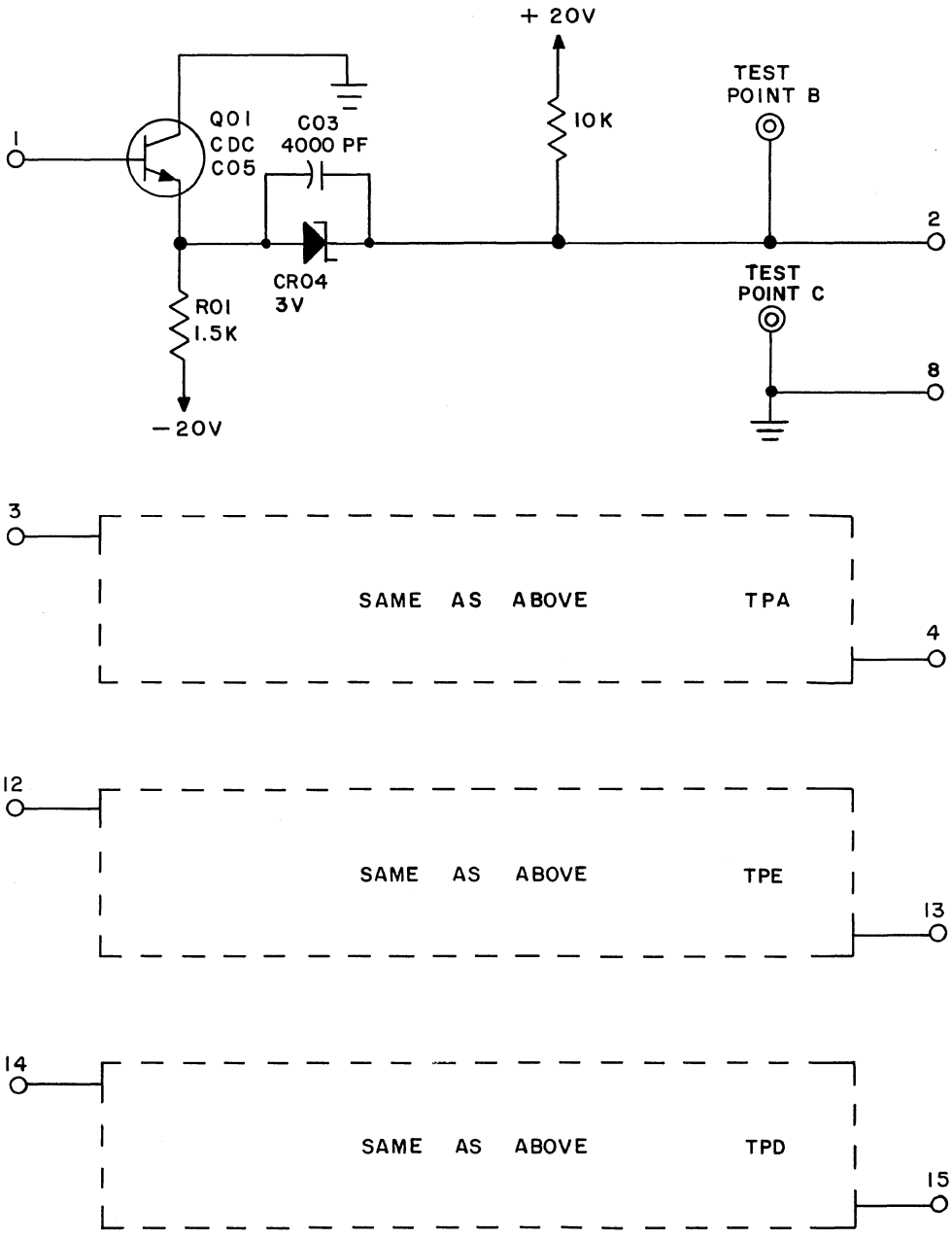
OPERATION

The delay line is driven by the circuit on card type C08; thus its input signal levels are approximately -0. 3v and -10v. However, due to integrating characteristics and attenuation, the peak voltage levels tend to diminish slightly as the signal travels down the delay line. The input signal levels of the emitter follower circuit are therefore of the order of -0. 3v and -10v, depending upon the point of the delay line from which the signal is taken.

A -0. 3v input results in an output near ground which is interpreted as a logical "0". A -10v input results in an output of approximately -9. 3v which is interpreted as a logical "1".

Transistor Q01 is an NPN silicon type CDC C05. It is connected as an emitter follower; thus its emitter voltage is always approximately 0. 7v more negative than the circuit input.

CR04 is a zener diode having a voltage drop of approximately 3v. This holds the circuit output 3v more positive than the emitter of Q01.



Emitter Follower C07C

DELAY LINE DRIVER
Card Type C08

FUNCTION

The function of this circuit is to provide an output suitable for driving a terminated 200-ohm delay line. With a 200-ohm load at pin 1 and the circuit in its quiescent state, the output voltage level is approximately -10v. Upon receipt of a -5.8v "1" input, both transistors switch to a state of heavy conduction and the output voltage becomes approximately -0.3v.

OPERATION

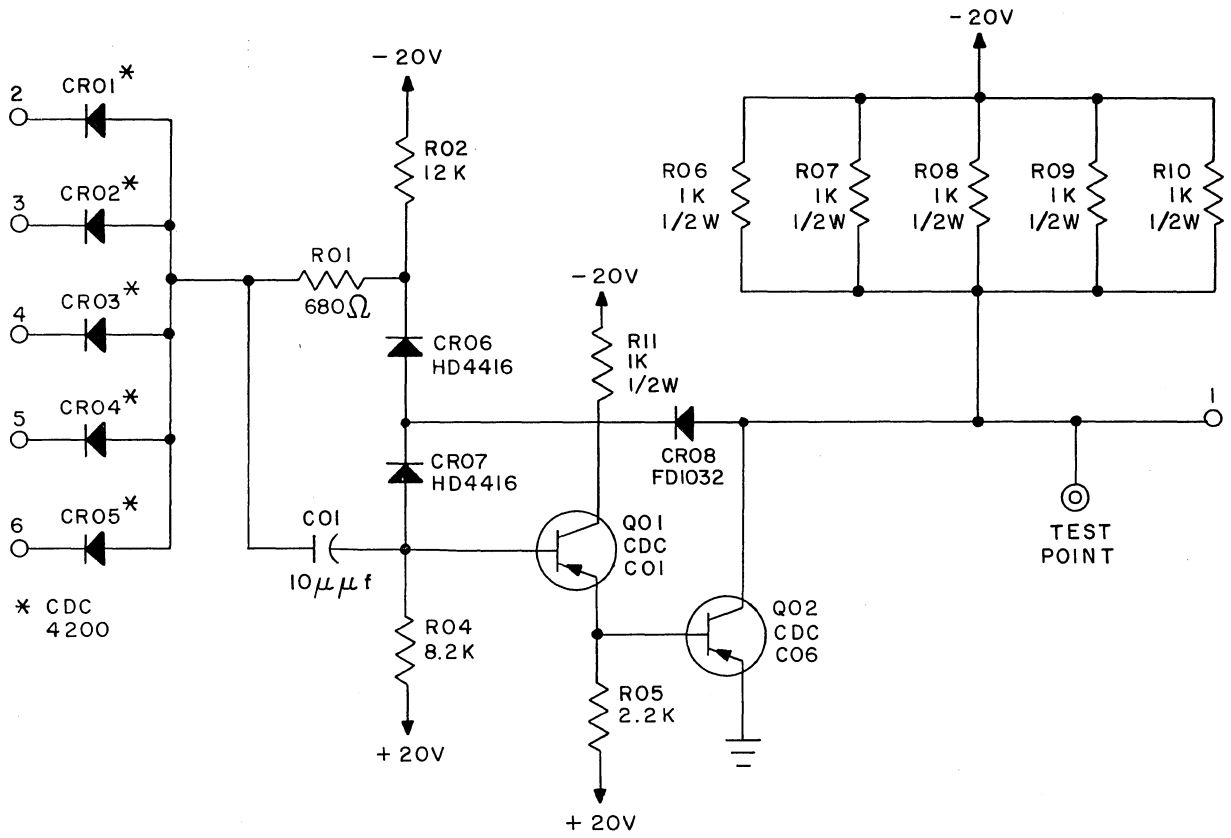
The circuit has 5 logical OR inputs; thus a -5.8v "1" on any input activates the circuit. An unused input is effectively a steady "0", regardless whether it is grounded or left open.

An input level-shifting action is provided by the two forward-drop diodes CR06 and CR07. These are silicon diodes having a forward voltage drop of approximately 0.7v. The two diodes in series provide a voltage shift of +1.4v from the cathode of CR06 to the anode of CR07.

With -1.1v "0" inputs, the base of Q01 is held at approximately +1.3v by the level-shifting diodes. Transistor Q01 is connected as an emitter follower; thus its emitter voltage is equal to the base voltage plus the base-emitter junction drop, and is approximately +1.6v. This provides sufficient forward bias so that minimum conduction is maintained through Q01. The emitter voltage of Q01 drives the base of Q02, which is a grounded emitter stage. The base-emitter junction of Q02 is therefore back-biased by the +1.6v input, and Q02 is cut off.

A -5.8v "1" input holds the base of Q01 at approximately -0.6v causing Q01 to conduct heavily. The emitter voltage of Q01 goes to approximately -0.3v, which causes Q02 to switch on and conduct heavily. In this state, the circuit output is clamped at approximately -0.6v by CR08.

With Q02 in the cut off state, its collector voltage tends to rise toward -20v. However, the 200-ohm load acts as a voltage divider with the equivalent 200-ohm resistance of the five 1000-ohm resistors, and the output stabilizes at -10v.



NOTES:

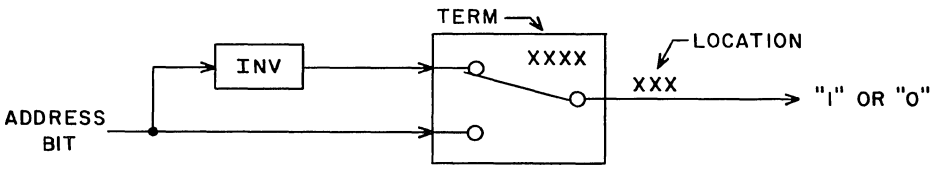
1. CIRCUIT HAS 5 "OR" INPUTS.
2. A -5.8V "1" INPUT CAUSES TRANSISTORS TO CONDUCT.

Delay Line Driver C08

COMPUTER DIVISION
PRINTED CIRCUIT DESCRIPTION
SWITCH
Card Type CA60A

FUNCTION AND OPERATION

This card contains four single-pole, double-throw toggle switches. The card was originally disigned as a memory selection switch to translate four bits of a storage address. The two positions of each switch correspond to the "1" and "0" values of the address bit.

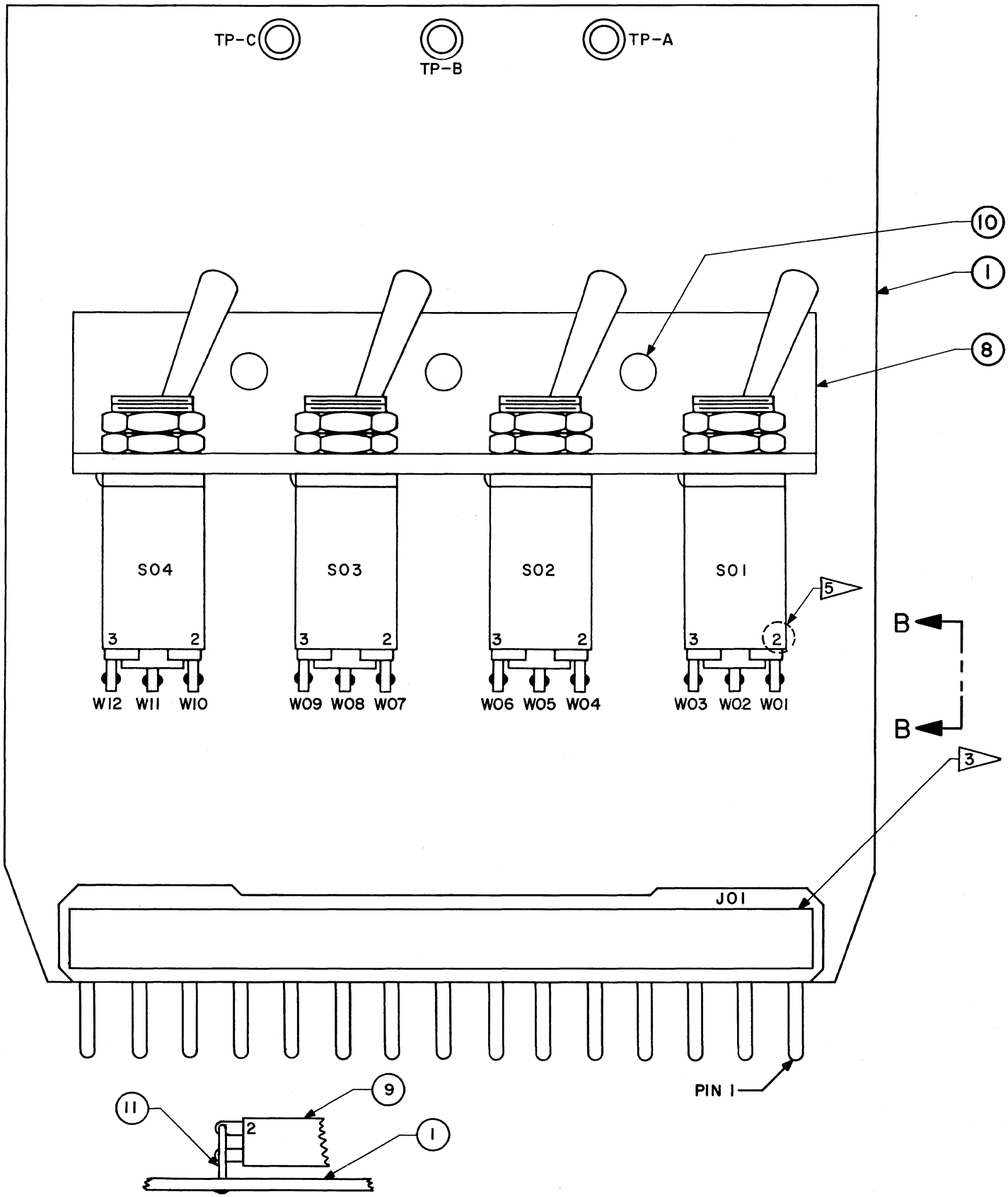


LOGIC DIAGRAM SYMBOL

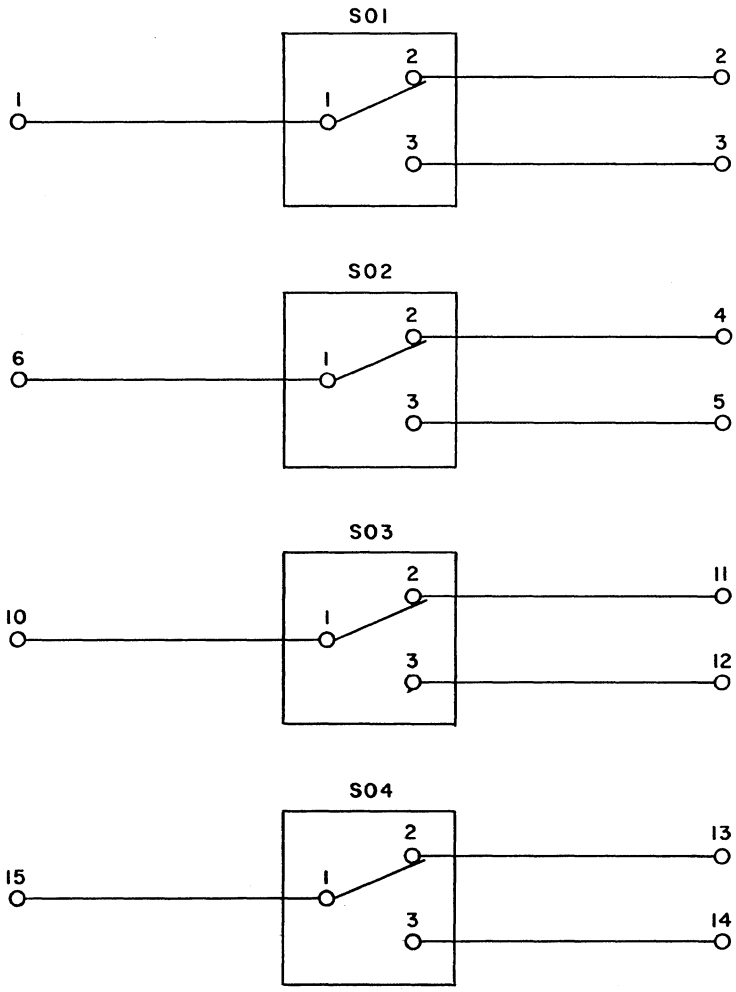
RELATED DOCUMENTS	NUMBER
Parts List	30923800
Assembly Drawing	30923800
Schematic Drawing	30923900
Engineering Specification	None

GROUND RULES

1. Because of the size of the size of the switches, the card location adjacent to the component side of the CA60A card cannot be used.



VIEW B-B COMPONENT LAYOUT



Switch CA60A

RESYNC CIRCUIT
Card Types C64A, C65A, C66A

GENERAL

The resync circuit shown on page 5-C64-3, is contained on three printed circuit cards, the type numbers being C64, C65, and C66. The logical operation of this circuit is presented on page 5-C64-2, and a timing diagram is shown on page 5-C64-5.

The function of a resync circuit is to synchronize an asynchronous signal of random length with the computer clock. Upon receipt of a logical "1" input signal, the resync circuit produces a "1" output during a clock phase. This output is 62.5 nanoseconds long and is not repeated, regardless of the duration of the input.

The delay time through the resync circuit is approximately 40 nanoseconds. The clock which drives the resync circuit must be phase-shifted so that the resync output coincides with the computer clock.

The average time required for resynchronization is 2 clock phase times, taking into account the 40-nanosecond circuit delay. It is possible, however, for this to occur during 1 phase time, and it never requires more than 3. A simplified timing diagram of the resync circuit is shown on page 5-C64-5. The best case and worst case conditions refer to the length of time required for synchronization.

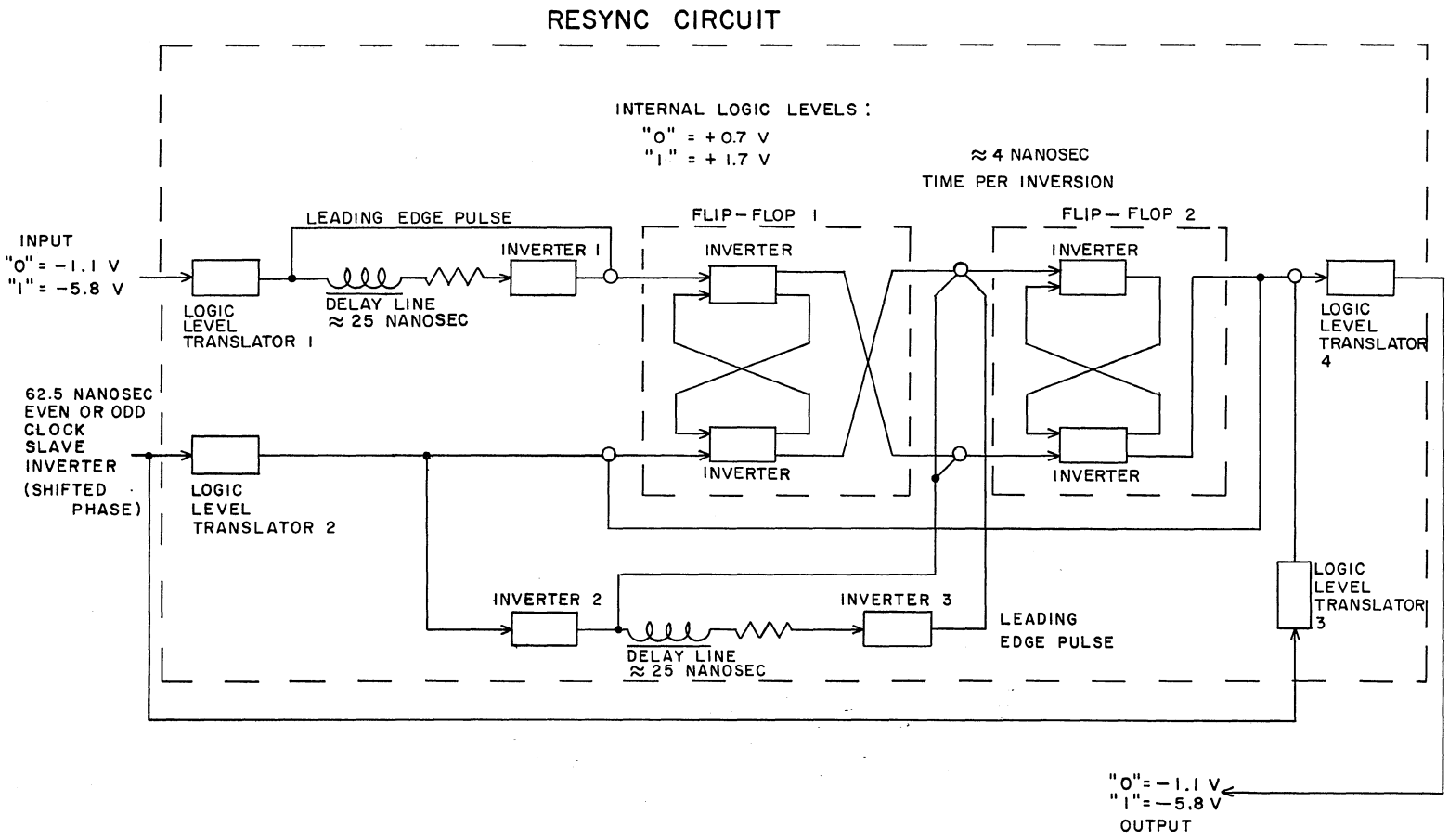
Logic levels within the resync circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v.

LOGICAL FUNCTIONING

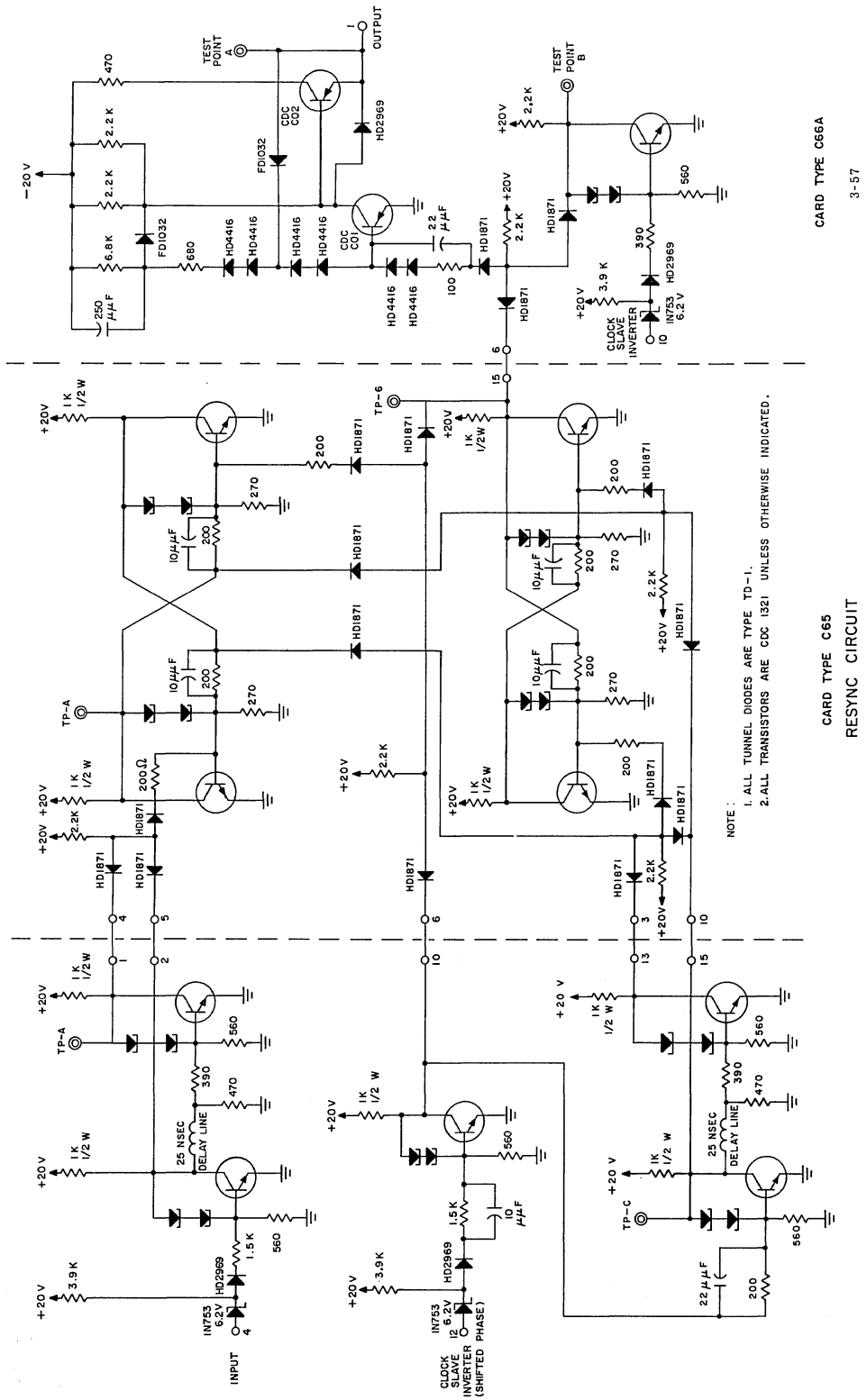
With initial conditions prevailing, the input to the circuit is a steady "0" and the output of inverter 1 is a steady "1". When a "1" input is received by the circuit, the delay line allows the output of inverter 1 to remain a "1" for approximately 25 nanoseconds. During this time FF 1 is set.

Next, FF 2 is set by the ANDed outputs of inverters 2 and 3. When the clock input goes to "0", the output of inverter 2 goes to "1". The delay line allows the output of inverter 3 to remain a "1" for 25 nanoseconds, setting FF 2.

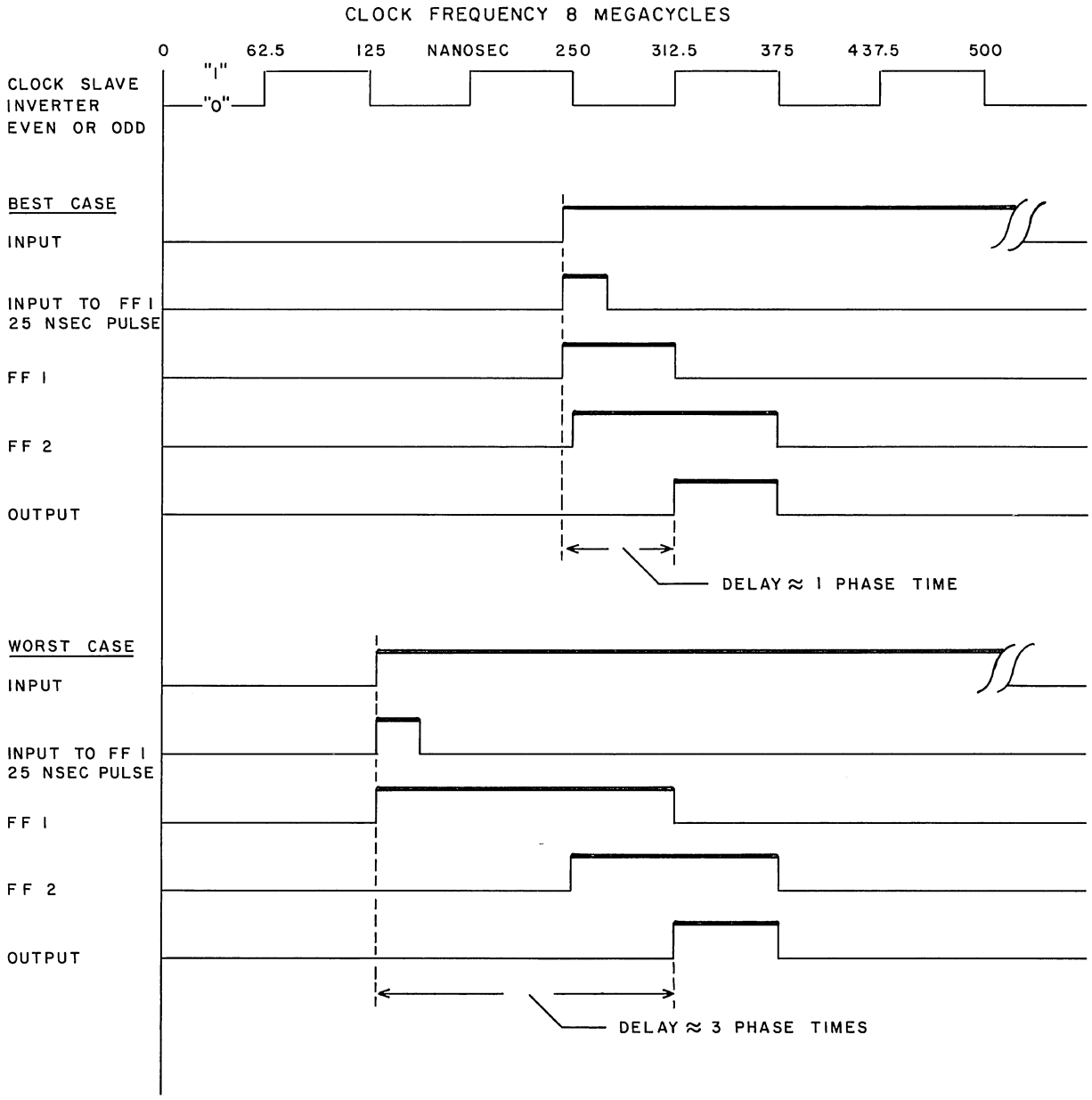
With FF 2 set, the "1" is gated out of the circuit by a full 62.5 nanosecond clock phase, which also clears FF 1. Following this, the clock input clears FF 2, and initial conditions prevail.



Resync Circuit
5-C64, C65 and C66-2



Resync Circuit C64A, C65A, and C66A



NOTES:

1. BEST CASE — INPUT RECEIVED JUST BEFORE CLOCK PHASE GOES TO "0."
2. WORST CASE — INPUT RECEIVED JUST AFTER CLOCK PHASE GOES TO "0."

Resync Circuit Timing Diagram

5-C64, C65 and C66-5

REV. D

CIRCUIT OPERATION

As shown on page 5-C64-3, except for the transistors in the output logic level translator, all of the resync circuit transistors are CDC 1321. This is a high speed silicon NPN type, having a gain-bandwidth of 1 kmc, which provides a time per inversion of approximately 4 nanoseconds, as used in this circuit. All of the CDC 1321 transistors have a base-to-collector tunnel diode network. This network establishes an input threshold level and holds the output voltage at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes are type TD-1. This is an axial tunnel diode having an I_p = 1 ma and a V_{fp} = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite V_{fp} = 1v. Due to slight individual differences, no two tunnel diodes switch at exactly the same point, but the difference is negligible in this high speed circuit.

Logic level translators 1, 2, and 3 perform the function of changing a -5.8v "1" to a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, upon receipt of a -5.8v "1" input, the 6.2v drop across the zener diode causes tunnel diode current to increase to approximately 1.2 ma, so they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The inverter circuits change a +1.7v "1" input to a +0.7v "0" output, and vice versa. Again, the output levels are taken from the collector, and the collector potential is equal to the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

As shown on page 5-C64-3, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bistable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is discussed elsewhere. This circuit converts a +0.7v "0" into a -1.1v "0", and a

+1.7v "1" into a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The input to this translator consists of the set output of FF 2, ANDed with the output of logic level translator 3. This produces an output pulse width of 62.5 nanoseconds, since the input from the clock slave inverter is a -5.8v "1" for this length of time. There is a delay of approximately 40 nanoseconds from this input to the resync circuit output.

The grounded emitter transistor is a PNP type CDC C01. The base bias is such that a +0.7v "0" allows it to switch on, producing a -1.1v "0" output, while a +1.7v "1" input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The clock slave inverter input to pin 12 of the C64 card and pin 10 of the C66 card should be phaseshifted so that the resync output coincides with the computer clock.
2. There is a delay of approximately 40 nanoseconds from the clock slave inverter input at pin 10 of the C66 card to the resync circuit output.
3. The resync circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

CAPACITIVE DELAY

Card Types C67, K67, C68, C69, C70, C71, K71

FUNCTION

The function of a capacitive delay is to provide an interval of time delay between successive logical operations. This is done by regulating the length of time required for a logical "1" to pass through the delay circuit. The delay time for a logical "0" is approximately one-tenth of the delay time for a logical "1".

The circuits contained on card types C67, C68, C69, C70, and C71 provide delay times ranging from 20 nanoseconds to 40 ms, and are shown on pages 5-C67-5 through 5-C67-10. In addition, the delays on card types C68 and C69 may be varied through a range of approximately ±15 percent by means of the variable resistor R02.

OPERATION, Card Types C67, C71, and K71

A delay circuit configuration is shown on page 5-C67-5, with typical waveforms. It consists of a capacitor from the signal line to ground, having a source of charging current through a series resistance with the voltage regulated by a 15v zener diode. The delay time from A to B is the time required to charge the capacitor to the input threshold level of inverter B when the output of inverter A switches to a -5.8v "1".

The charging voltage is stabilized at a constant 15 volts by a zener diode. The delay time is therefore proportional only to the RC time constant of the series resistance and the capacitance, and is not affected by small line voltage variations. On card types K67, C68, and C69, the series resistance is variable by means of a 2k potentiometer. This provides a close adjustment of the delay times through a range of approximately ±15%.

The AND input contains FD 1032 silicon diodes having a voltage drop of approximately 0.6v; thus point (1) on page 5-C67-5 is always 0.6v more negative than the logic-level input. The voltage across the capacitor is controlled by the level of the input signal. With a -1.1v "0" input, this voltage is approximately -1.7v. When the input from A switches to a -5.8v "1", the voltage at point (1) approaches -6.4v in an exponential curve according to the rate at which charging current flows into the capacitor. At the threshold level of approximately -3v, inverter B switches state.

OPERATION, Card Types K67, C68, and C69

The circuit contained on these cards is designed to provide stable delay times of relatively long duration. It consists of a capacitive delay followed by a double inverting network such that the circuit does not produce an over-all logical inversion.

The circuit output characteristics are similar to those of a logic card, and it drives a maximum of 8 logic card loads. These may be 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

As discussed in the previous section, the delay time is the time required to charge the capacitor to the threshold level of the following inverter when the circuit input switches to the -5.8v "1" level. The threshold level at which the inverter switches state is approximately -3v, but often varies slightly from card to card. From an examination of the exponential charge curve of the capacitor, it is seen that a small variation of the threshold level makes an appreciable difference in the delay time. This variation can be eliminated by always using the same inverter with a given capacitive delay. Mounting the inverter on the same card ensures that the capacitive delay always drives the same inverter and the threshold remains essentially constant.

As discussed previously, the input logic diodes are high speed devices having a voltage drop of approximately 0.6v. This holds the anode of zener diode CR05 at a potential 0.6v more negative than the logic-level input.

Zener diode CR05 functions as a threshold-setting device. The breakdown voltage of CR05 is approximately 4.9v; thus with its anode held at -6.4v by "1" inputs, CR05 applies approximately 1.3v of forward drive to the base of Q01. As the circuit input goes negative, conduction increases through CR05 and resistor R05. When current flow through R05 reaches approximately 0.36 ma, the negative-going input starts to draw turn-on current from transistor Q01. The input continues moving negative to the -5.8v "1" level, causing Q01 to conduct heavily.

A -1.1v "0" input holds the anode of CR05 at approximately -1.7v. In this state, CR05 does not have sufficient bias to hold it in the zener breakdown region. The base of Q01 is therefore held at a low positive voltage by resistors R05 and R06, and Q01 is cut off.

Base drive for transistor Q02 is taken from the collector of Q01. When -5.8v "1" inputs cause Q01 to conduct heavily, its collector holds the base of Q02 at approximately -0.5v, so that Q02 is in a state of minimum conduction. The collector voltage of Q02 is clamped

at approximately -6v by resistors R07, R08, and diode CR06.

The -6v level is applied to the base of Q03 and its emitter is isolated by CR07. Transistor Q03 is connected as an emitter follower, and in this state, it can supply OR current for 8 logic card loads.

A -1.1v "0" input causes Q01 to cut off and its collector voltage rises toward -20v, causing transistor Q02 to conduct heavily. The collector voltage of Q02 approaches -0.5v, and the circuit output becomes a logical "0". In this state, transistor Q03 is cut off and Q02 can supply AND current for 8 logic card loads.

Positive feedback is provided from the collector of Q02 to the base of Q01 by resistors R05, R06, and capacitor C09. This produces a regenerative effect which speeds the switching action.

OPERATION, Card Type C70C

This circuit is designed to provide an approximate linear delay, requiring 120 to 150 nanoseconds for the output to change from "0" to "1", and requiring 60 to 75 nanoseconds to change from "0" to the -3v threshold. The delay time from "1" to "0" is approximately one-tenth as long, or 10 to 15 nanoseconds.

With a -1.1v "0" input, the cathode of CR01 is near -1.3v. The two forward-drop diodes CR02 and CR04 hold the base of Q03 near ground. Transistor Q03 is connected as an emitter follower; thus the circuit output is equal to the base voltage less the base-emitter junction drop and in this state is approximately -0.8v.

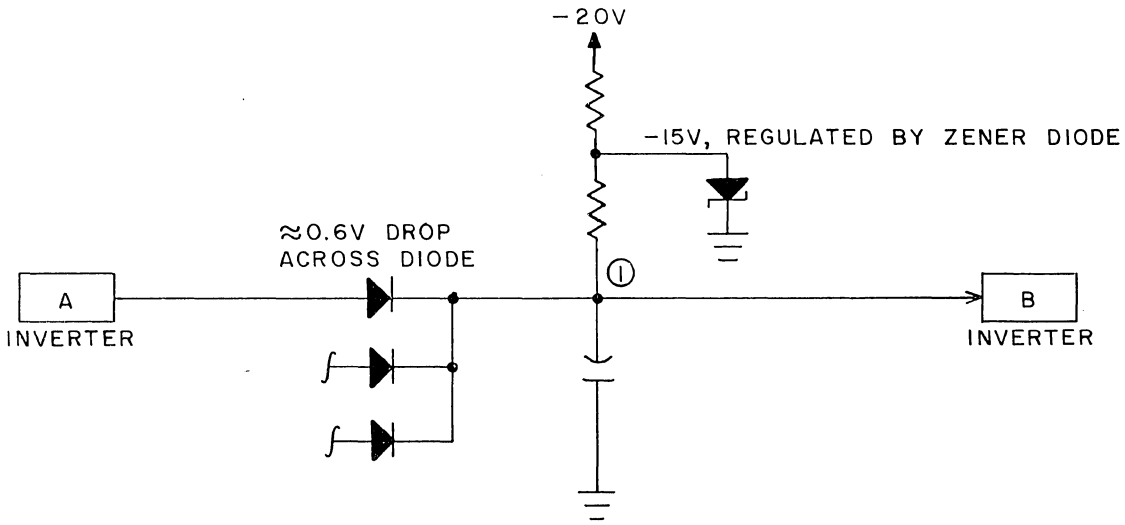
When the input switches to a -5.8v "1", capacitor C01 begins charging toward -6v. This causes conduction through Q01 to decrease so that the circuit output moves negative. However, the negative-going output is coupled back by the "bootstrap" connection of CR03, which is a 3v zener diode. This results in a nearly constant current of about 3.5 ma through resistor R02. Capacitor C03 is therefore charged at a nearly constant rate, resulting in a highly linear output.

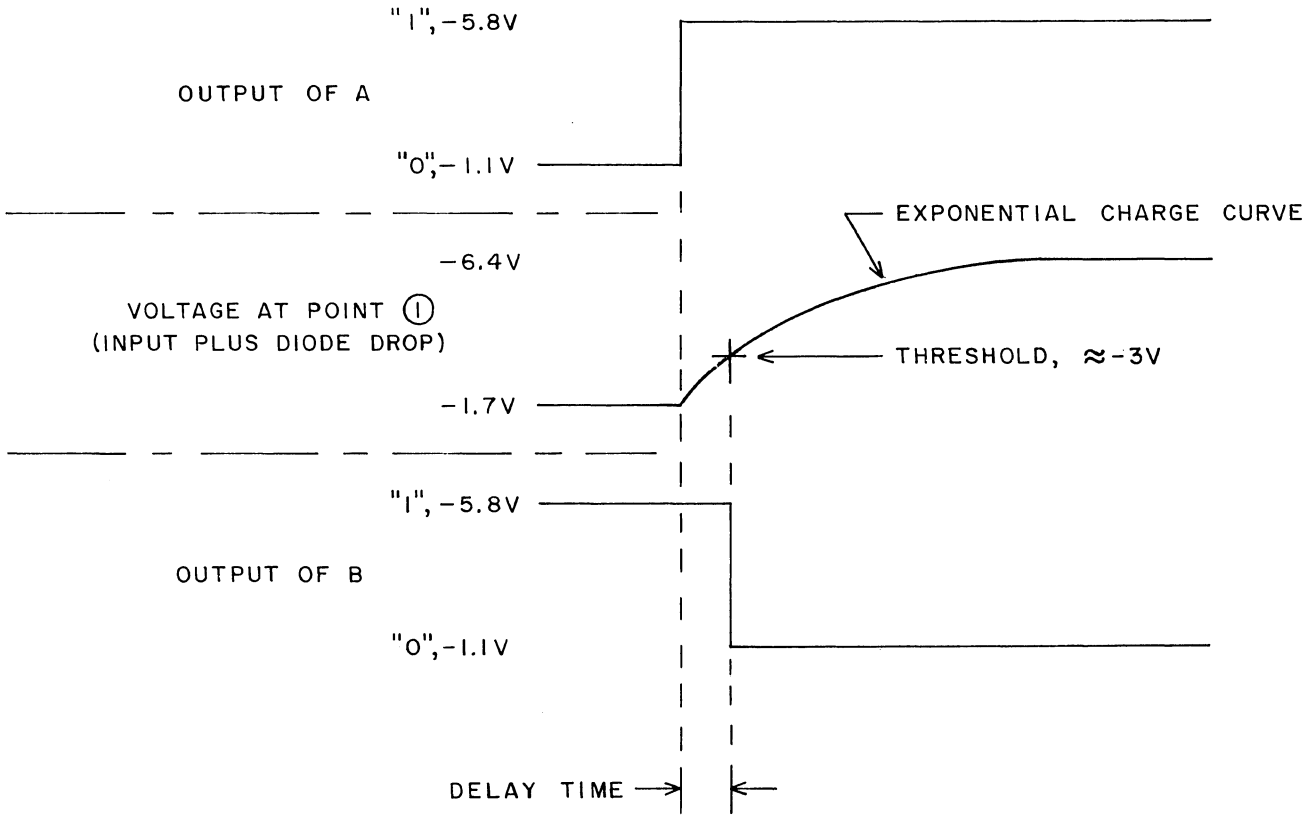
GROUND RULES

1. Each delay circuit contained on card types C67 and C71 may drive only one logic circuit.
2. The outputs of delay circuits contained on card types C67 and C71 must always connect to logic circuit OR inputs, while the circuit on Card Type K71

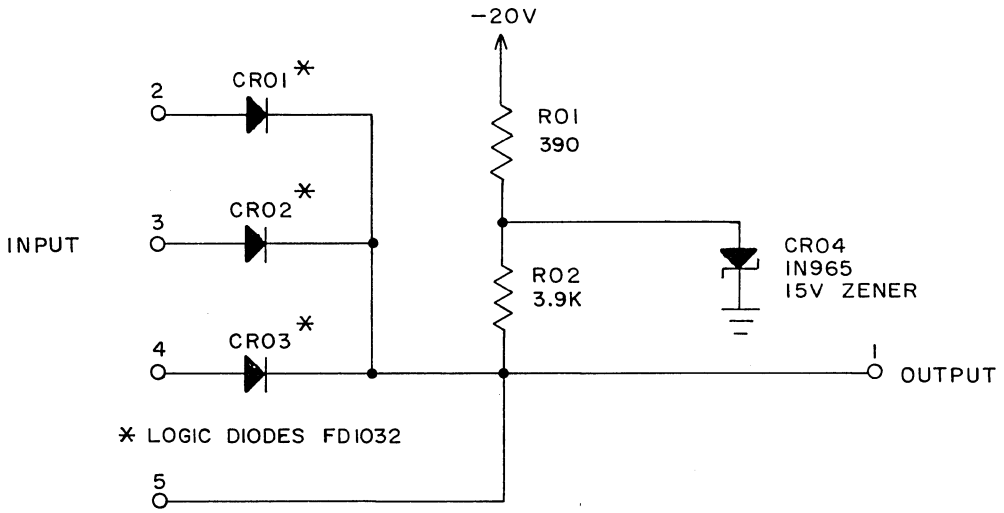
must drive AND inputs.

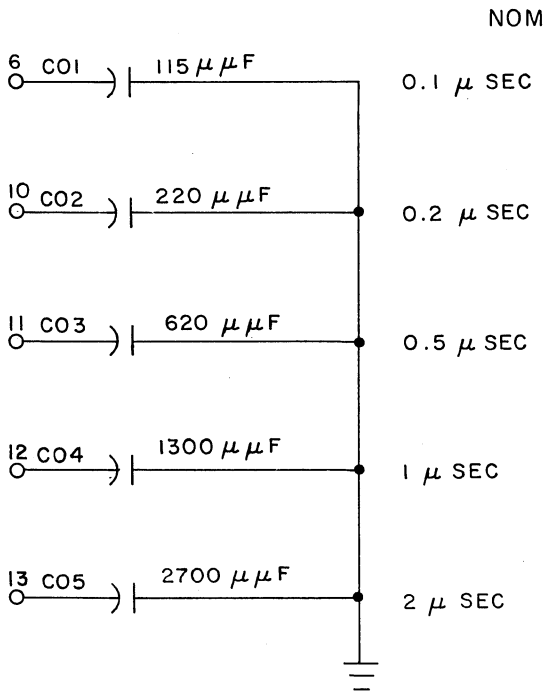
3. The delay circuits contained on card types K67, C68, and C69 may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
4. The nominal delay times pertain to a logical "1".
5. The delay time for a logical "0" is approximately one-tenth of the corresponding delay time for a logical "1".





Typical Circuit Configuration

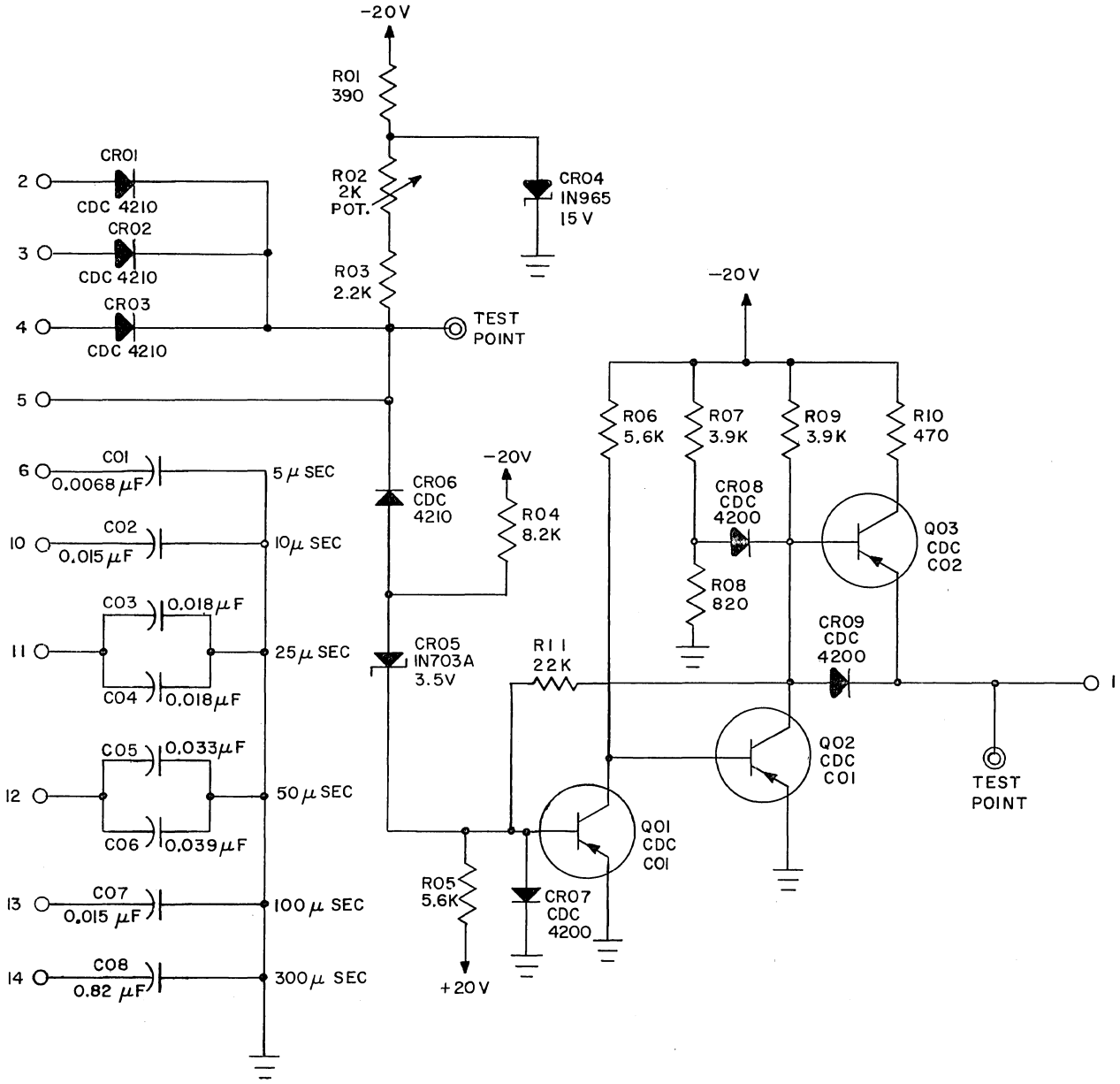




NOTE:

1. AN EXTERNAL JUMPER CONNECTS PIN 5 TO THE DESIRED DELAY.
2. CARD TYPE K67 GIVES SAME DELAY TIMES, BUT CIRCUIT IS SIMILAR TO C68 AND C69.

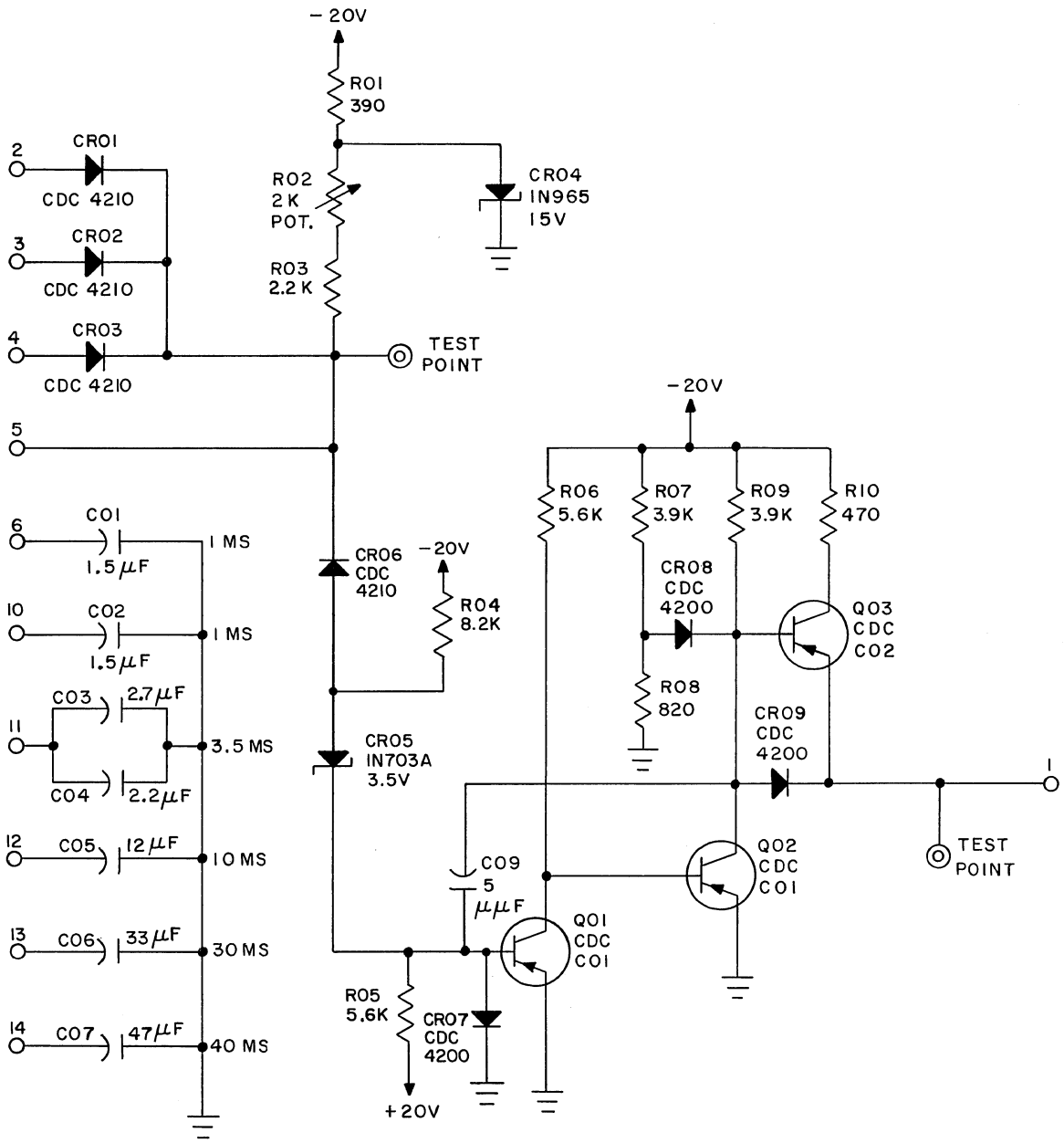
Capacitive Delay, Fixed C67



NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15% BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

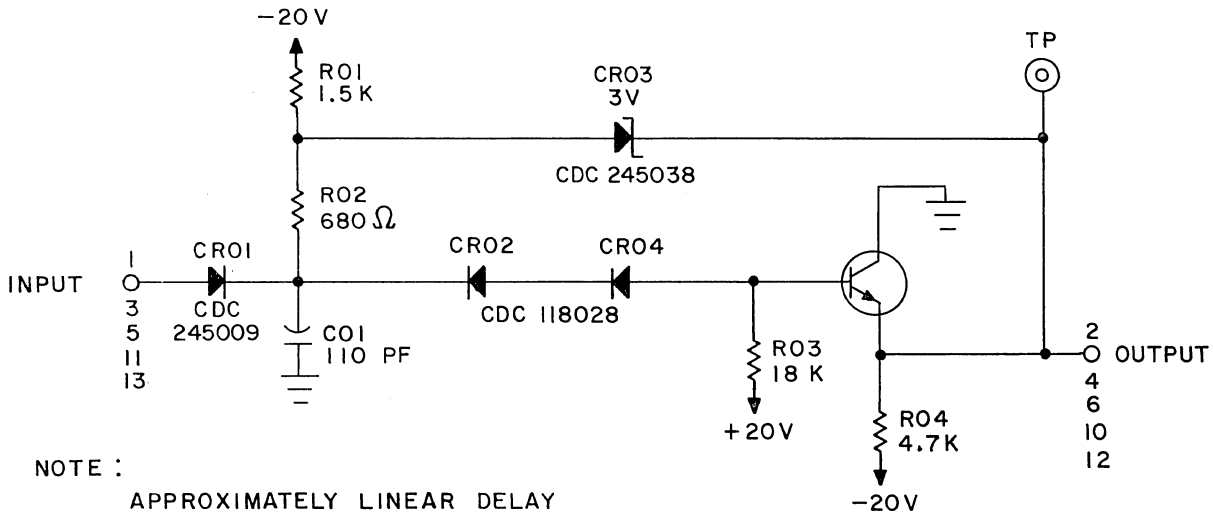
Capacitive Delay, Variable C68

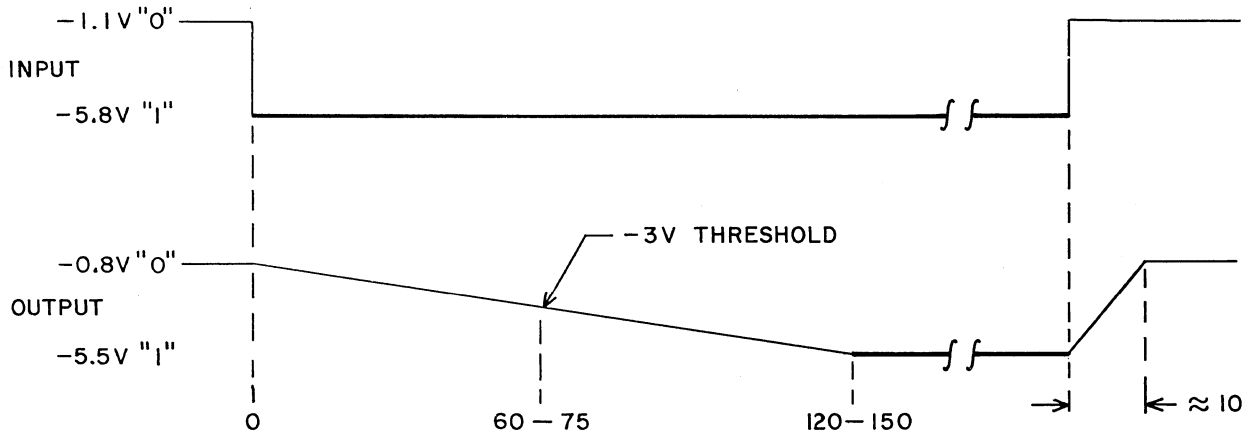


NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15 % BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

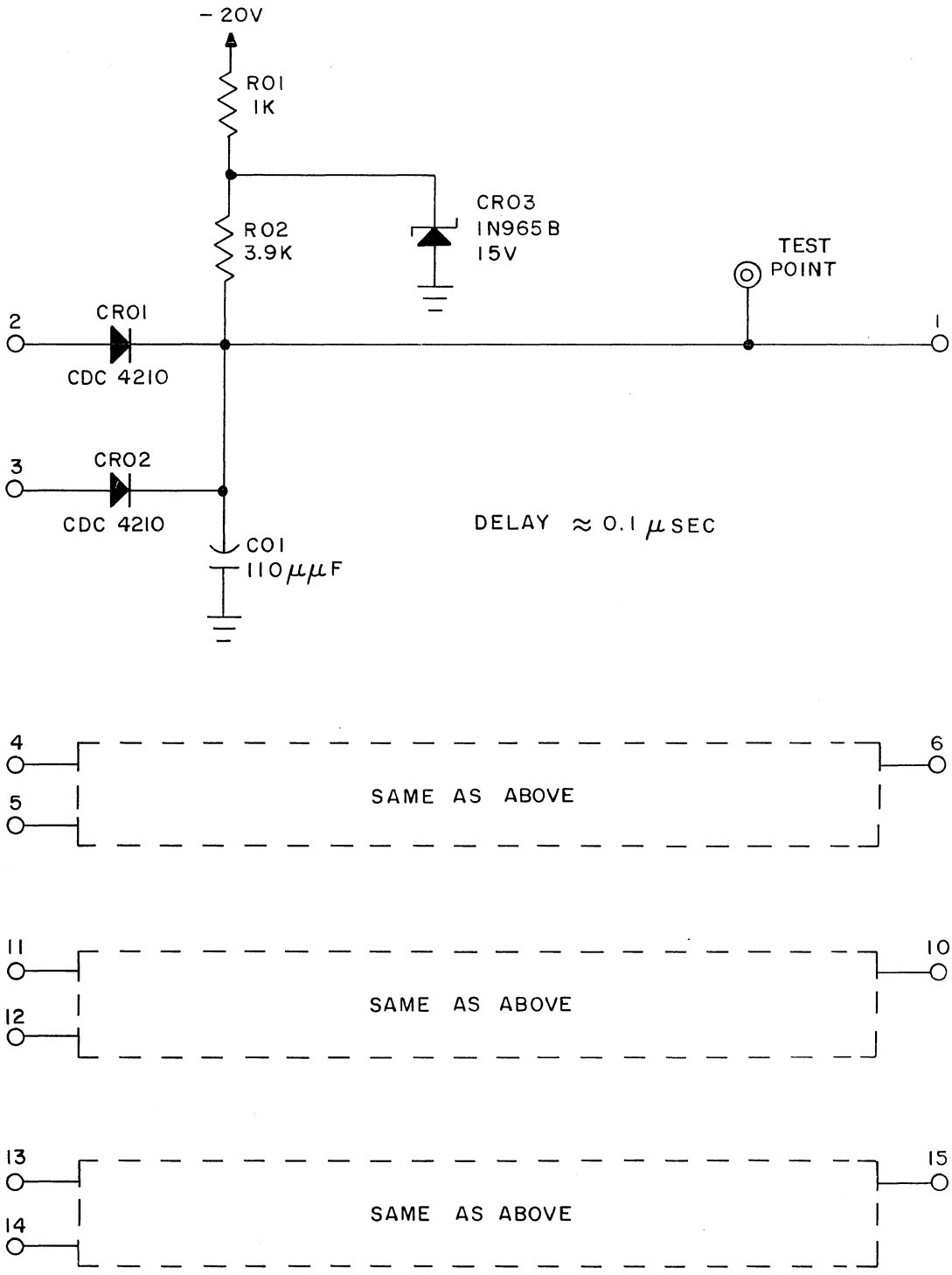
Capacitive Delay, Variable C69





NOTE :

ALL TIMES ARE IN NANOSECONDS.



Capacitive Delay, 0.1 usec C71

PRIORITY CIRCUIT

Card Types C77, C78B, C79A

(See Pub No. 60042000 3609 Diagrams, drawing number 311518)

GENERAL

The priority circuit shown on page 5-C77-3 is contained on three printed circuit cards, the type numbers being C77, C78, and C79. The logical operation of this circuit is presented on page 5-C77-2, and a timing diagram is shown on page 5-C77-5.

The function of the priority circuit is to enable a storage module to honor its five access channels on a first-come, first-serve basis, without interference from any other access channel. Priority circuits are contained in the input logic of each of the five access channels, and when one of them receives a "1" input, it disables the priority circuits in the remaining four channels. Thus a request on any of the remaining channels is not honored until the first channel is released.

The priority circuits differentiate between access channel requests spaced down to approximately 7 to 8 nanoseconds. Requests arriving more closely than this are considered to have arrived simultaneously, and factors such as supply voltage and wire length determine which channel is honored. If two requests arrive simultaneously and all other factors are equal, then neither is honored.

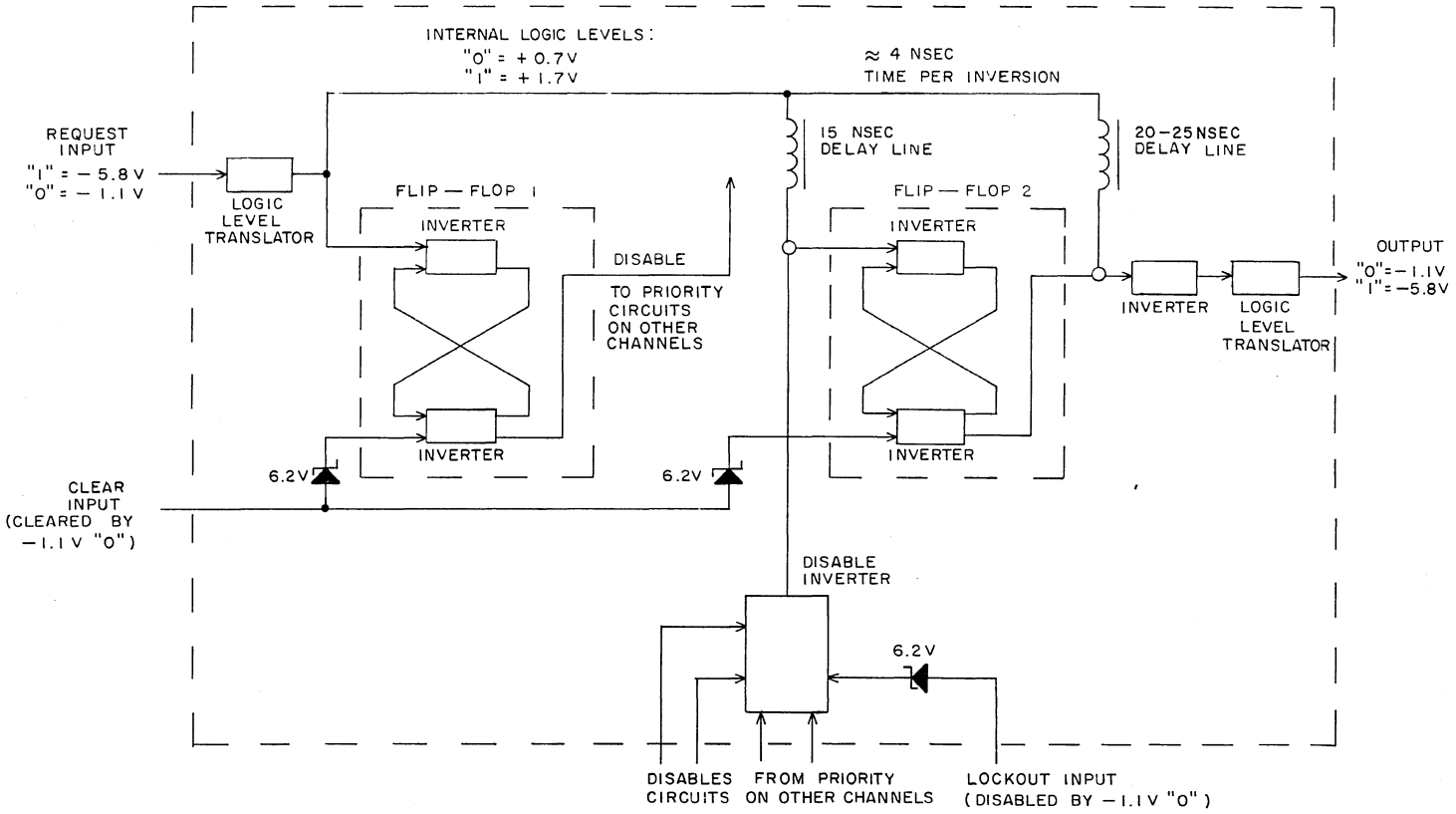
With card type C79A, the delay time through a priority circuit is 30 to 40 nanoseconds. The 20-nanosecond delay line accounts for the majority of this, since the transistor and tunnel diode logic provides a time per inversion of approximately 3 to 4 nanoseconds. A priority circuit timing diagram is presented on page 5-C77, C78 and C79-5.

Logic levels within the priority circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v. The disable signal sent from one priority circuit to the other four is the set output of FF1, and is a +1.7v "1".

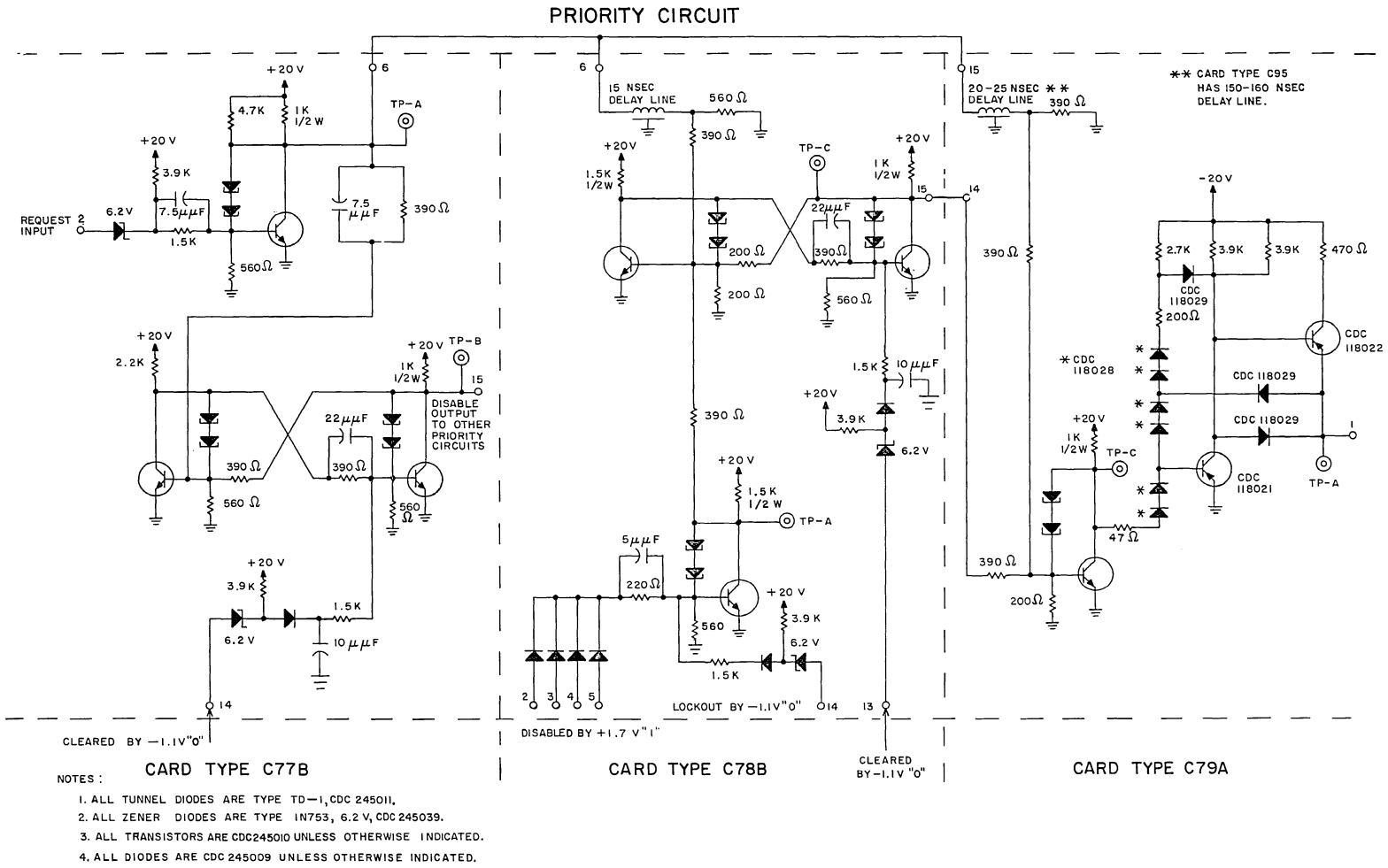
NOTE

Card type C95 is similar to C79A, except that the delay line is 150-160 nanoseconds.

Priority Circuit



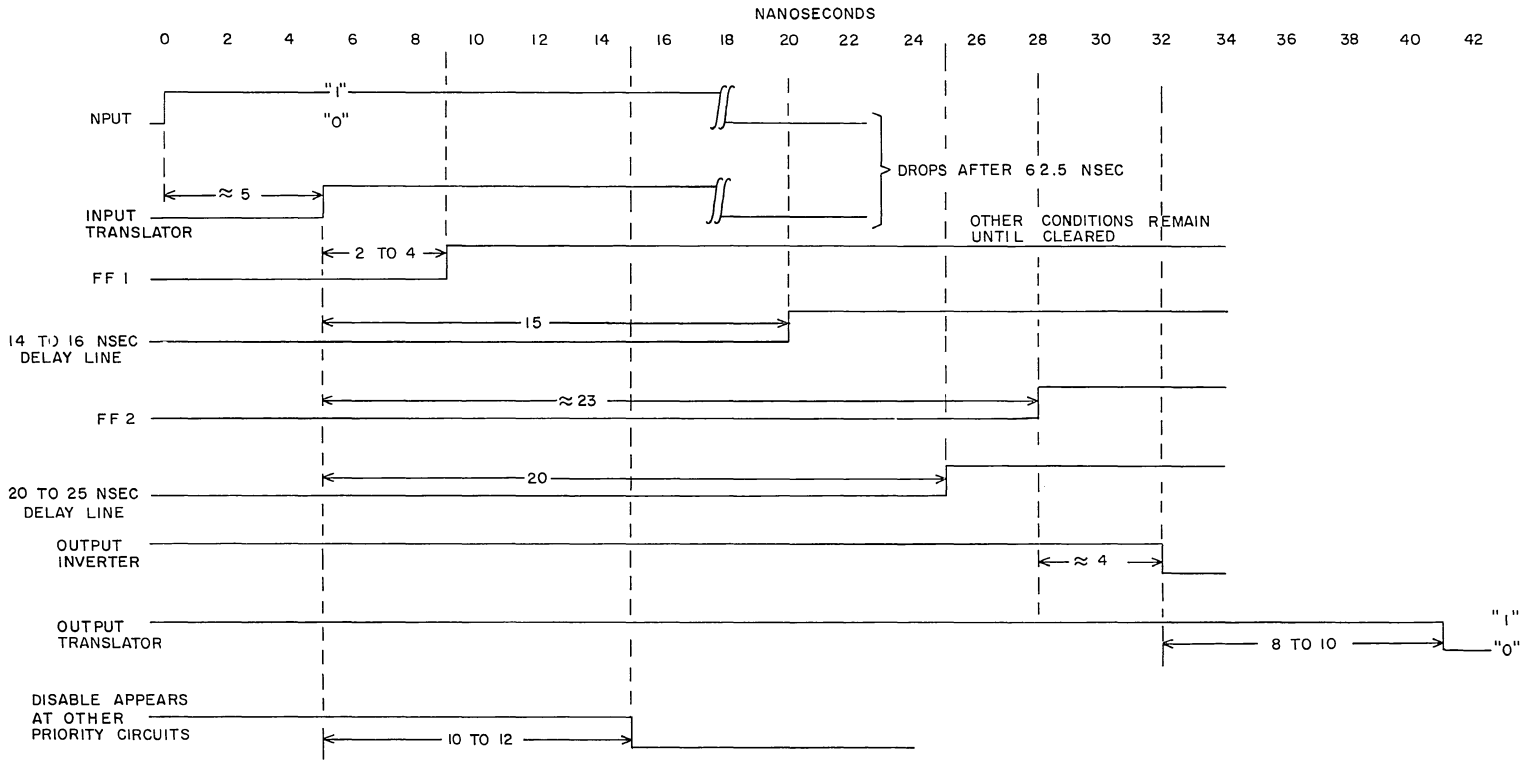
NOTE:
CIRCUIT PRODUCES A LOGICAL INVERSION BETWEEN INPUT AND OUTPUT.



NOTES :

1. ALL TUNNEL DIODES ARE TYPE TD−1, CDC 245011.
2. ALL ZENER DIODES ARE TYPE 1N753, 6.2 V, CDC 245039.
3. ALL TRANSISTORS ARE CDC245010 UNLESS OTHERWISE INDICATED.
4. ALL DIODES ARE CDC 245009 UNLESS OTHERWISE INDICATED.

PRIORITY CIRCUIT TIMING DIAGRAM



NOTE: OVER—ALL INVERSION BETWEEN INPUT AND OUTPUT

LOGICAL FUNCTIONING

As shown on page 5-C77-2, the portions of the priority circuit are: an input logic level translator; flip-flop 1 which produces the signal disabling the other priority circuits; an inverter which disables flip-flop 2 if another access channel has priority; flip-flop 2; an output inverter; and an output logic level translator.

In addition, the priority circuit contains four 6.2v zener diodes, three of which function both as logic level translators and inverters. A -5.8v "1" input to a zener diode becomes a +0.4v output, and a -1.1v "0" input becomes a +5.1v output. These outputs act as "0" and "1", respectively, in the priority circuit logic. The remaining zener diode performs a level-shifting action in the input logic level translator.

A Request signal on an access channel results in a -5.8v "1" input, which is converted by the input logic level translator to a +1.7v "1". This sets FF1, which, in turn, disables the other priority circuits.

After a delay of 15 nanoseconds, the "1" reaches the AND into FF2. If a disable input is not being received, the output of the disable inverter is also a "1", so that FF2 is set. Then, after an additional 5-nanosecond delay, the "1" is ANDed with the set output of FF2 into the output inverter, where it becomes a +0.7v "0". This is converted by the output logic level translator to a -1.1v "0". The priority circuit therefore produces a logical inversion between input and output.

As soon as the access channel has been honored, the priority circuit is cleared by a -1.1v "0" input, which is converted by zener diodes to +5.1v, and is applied to the clear inputs of FF1 and FF2. This removes the disable from the other priority circuits so that a request on another channel may be honored.

CIRCUIT OPERATION

As shown on page 5-C77-3, except for the transistors in the output logic level translator, all of the priority circuit transistors are CDC 245010. This is a high speed silicon NPN type, having a typical gain bandwidth of 1 kmc, which provides a time per inversion of approximately 2 to 4 nanoseconds, depending upon the loading.

All of the CDC 245010 transistors have a base-to-collector tunnel diode network. This establishes an input current threshold level and holds the output voltages at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes used are CDC 245011. This is an axial tunnel diode having an I_p =1 ma and a V_{fp} = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite V_{fp} =1v. Due to slight individual differences, no two tunnel diodes ever switch at exactly the same point, but the difference is negligible in this high speed circuit.

The input logic level translator performs the function of changing a -5.8v "1" into a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, a -5.8v "1" input causes tunnel diode current to increase to a value in excess of 1 ma, so that they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The disable inverter and the output inverter circuits are for changing a +1.7v "1" to a +0.7v "0", and vice versa. In addition, the disable inverter also changes the +5.1v signal received through the zener diode to a +0.7v "0". Again, the output levels are taken from the collector, and the collector potential equals the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

The amount of speed-up capacitance used on inverters of this type is dependent upon the particular input. A single OR input may have a fairly large speed-up capacitor; however, the speed-up capacitance on the OR inputs to the disable inverter must be kept small. This is because FF 1 on each priority circuit must drive four disable inverter inputs and is loaded too heavily if too much speed-up capacitance is used. Also, the speed-up capacitance on AND inputs must be small in order to prevent runt pulses and partial enables from satisfying the AND.

As shown on page 5-C77-3, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bi-stable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is

discussed elsewhere. This circuit converts a +0.7v "0" to a -1.1v "0", and a +1.7v "1" to a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The grounded emitter transistor is a PNP type CDC118021.The base bias is such that a +0.7v input allows it to switch on, producing a -1.1v "0" output, while a +1.7v input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The priority circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
2. Lead length from FF 1 to the disable inverters on the other priority circuits must be less than 5 inches.
3. Only one priority circuit may be cleared by any one inverter, because a priority circuit requires approximately 15 ma of current for clearing.
4. One inverter may drive the lockout inputs of 4 priority circuits, because a lockout input requires approximately 4 ma.

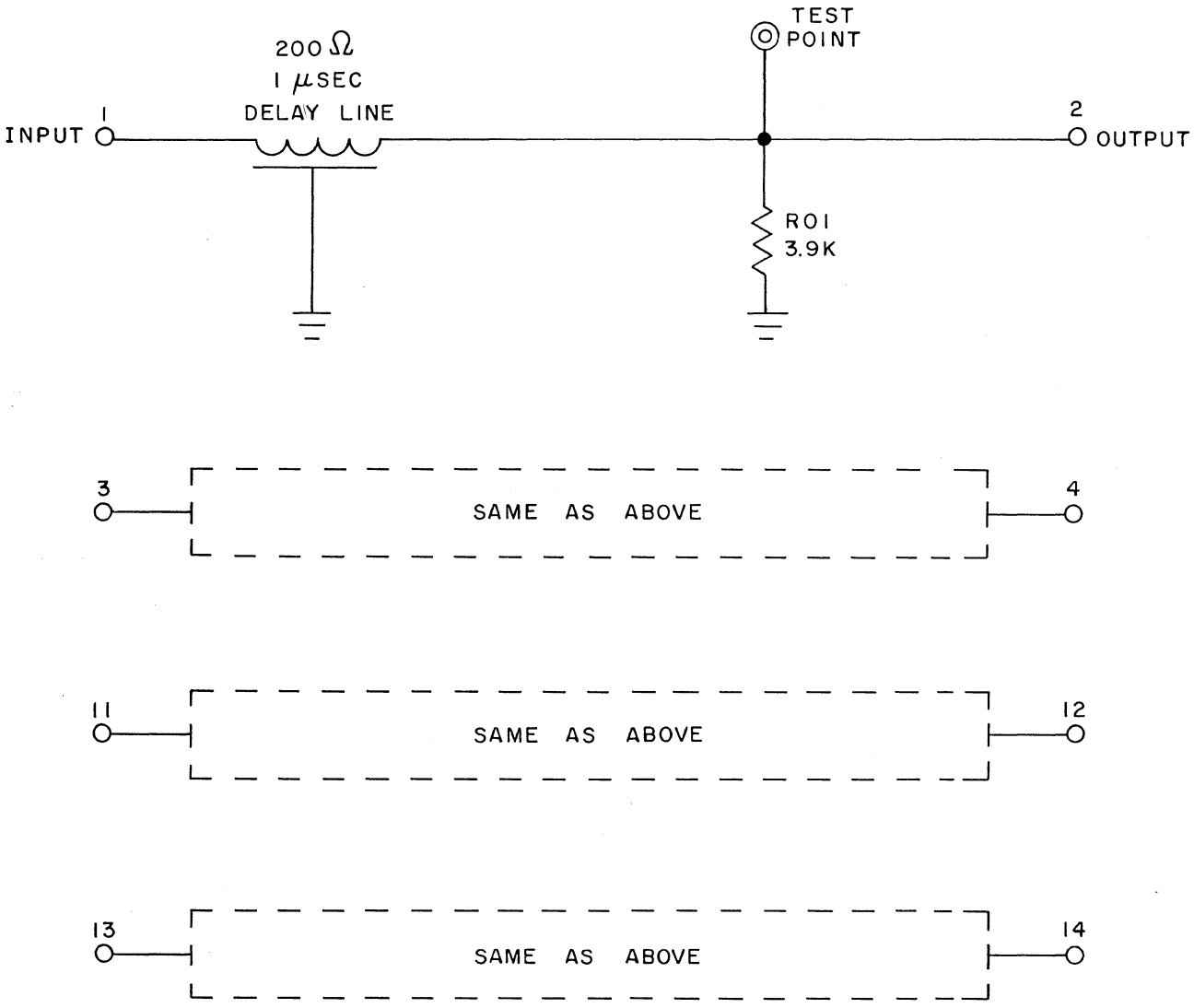
DELAY LINE, 1 USEC

Card Type C80

The function of this circuit is to provide an interval of time delay between successive logical operations. It is designed for use in applications requiring greater stability than may be obtained from capacitive delays.

The nominal 1 usec delay time applies to both "1's" and "0's", and the delay may be used to drive either an AND or an OR input. Attenuation through the delay line is negligible.

The characteristic impedance of the delay line is 200 ohms. The purpose of resistor R01 is to provide better impedance matching between the logic circuit input and the delay line output.



NOTE:

1. EACH DELAY MAY DRIVE ONE LOGIC CIRCUIT USING EITHER AN "AND" OR AN "OR" INPUT.

Delay Line, 1 usec C80

CRYSTAL OSCILLATOR

Card Type C81, 30 kc
Card Type C82, 83.4 kc
Card Type C83, 120 kc

FUNCTION

The function of these circuits is to produce accurately timed signals for controlling the Write operation in magnetic tape equipment. Information may be written on tape at rates of either 30,000, 83,400, or 120,000 frames per second. A single-phase sine wave output is taken from the oscillator tank and is converted by the circuit contained on card type C89 into a chain of square pulses at logic voltage levels.

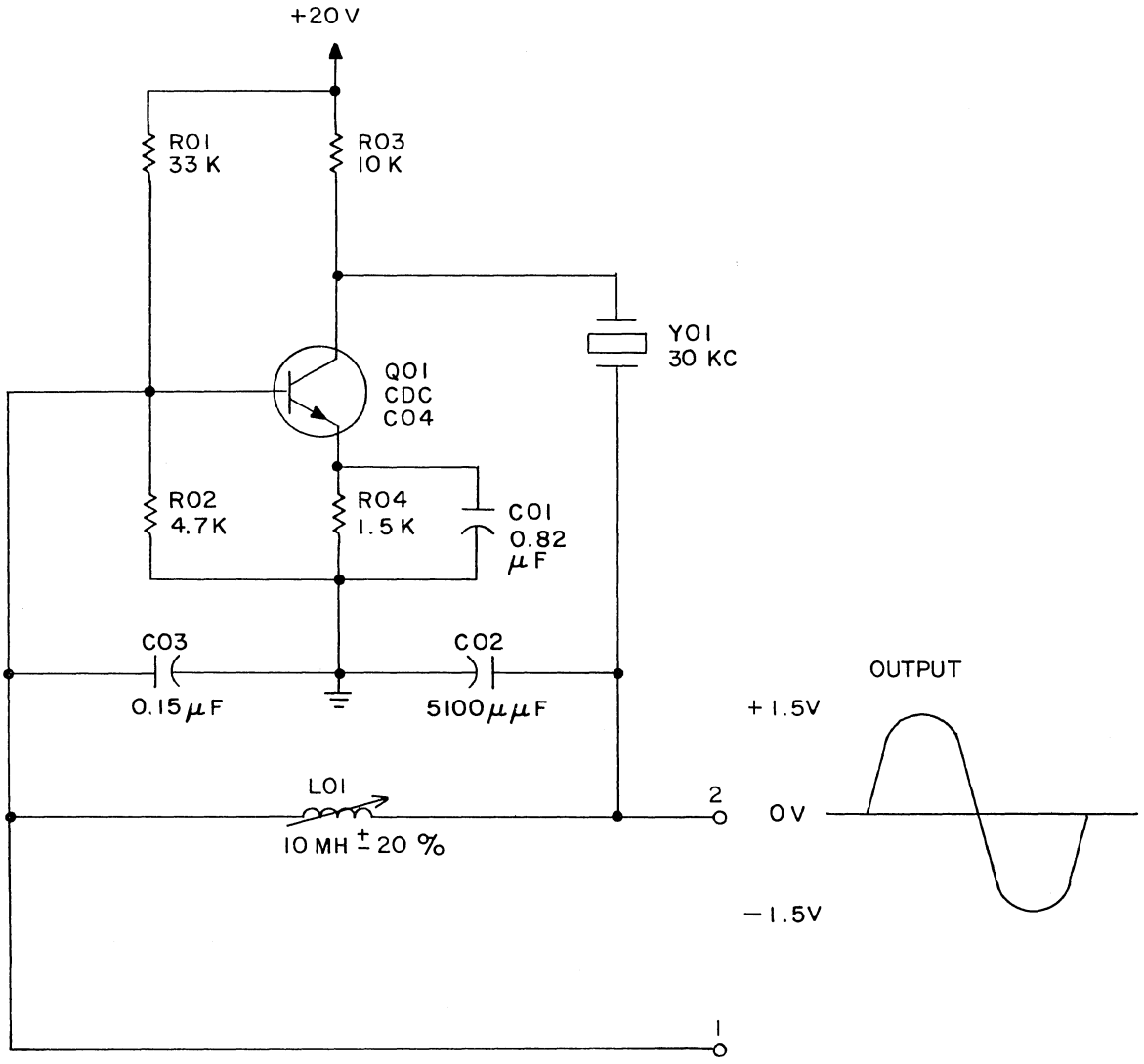
OPERATION

The circuit is essentially a Colpitts oscillator having a crystal filtered power amplifier. Opposite-phase outputs are taken from the oscillator tank and are available at pins 1 and 2 of the printed circuit card. Each output is a sine wave about ground; however, the peak-to-peak amplitude of the output at pin 2 is approximately 3 volts while that at pin 1 is approximately 0.5v.

Sufficient gain to maintain oscillation is provided by transistor Q01, which is connected as a Class C power amplifier. Q01 is an NPN silicon transistor capable of providing a current gain greater than 25 with a collector current of 400 ma. Transistor Q01 is driven both into saturation and cut off, so that its collector voltage is approximately a square wave.

The square wave signal from the collector of Q01 is filtered by the crystal filter Y01 into a sine wave at the fundamental frequency. Y01 is a high impedance quartz crystal having a Q value of the order of 10^5. It exhibits a frequency stability of 0.005 percent over the range $25^{\circ}C \pm 35^{\circ}C$, and a long-term stability with time of 1 ppm per week.

The oscillator tank consists of capacitors C02, C03, and the inductance L01. The values of these components are shown in the accompanying diagrams. Inductance L01 is adjustable through a range of approximately ± 20 percent, so that the tank may be tuned to the center frequency of the crystal.

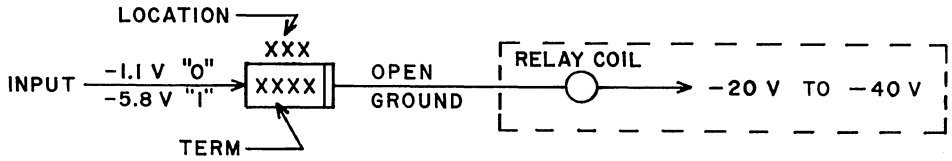


Crystal Oscillator, 30KC C81
(Others are similar)

COMPUTER DIVISION
PRINTED CIRCUIT DESCRIPTION
RELAY DRIVER
Card Type CA84A

FUNCTION

The function of this circuit is to enable a low impedance path from ground to the circuit output, upon receipt of a -5.8v "1" input. The circuit is designed to switch a current of the order of 1 ampere flowing in a highly inductive load such as a relay coil. A diode clamp connection is provided at the collector of Q02, so that a high-voltage inductive transient induced when current is interrupted does not damage the transistor.



LOGIC DIAGRAM SYMBOL

RELATED DOCUMENTS	NUMBER
Parts List	30933400
Assembly Drawing	30933400
Schematic Drawing	30933500
Engineering Specification	None

OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion applies to either circuit, but the component numbers mentioned are those appearing in circuit A.

The circuit has one logical OR input, and a 3-way AND. An unused OR input has no effect on the circuit, while an unused AND input, if left open, acts as a steady "1." Thus if the entire AND group is unused, at least one pin must be grounded.

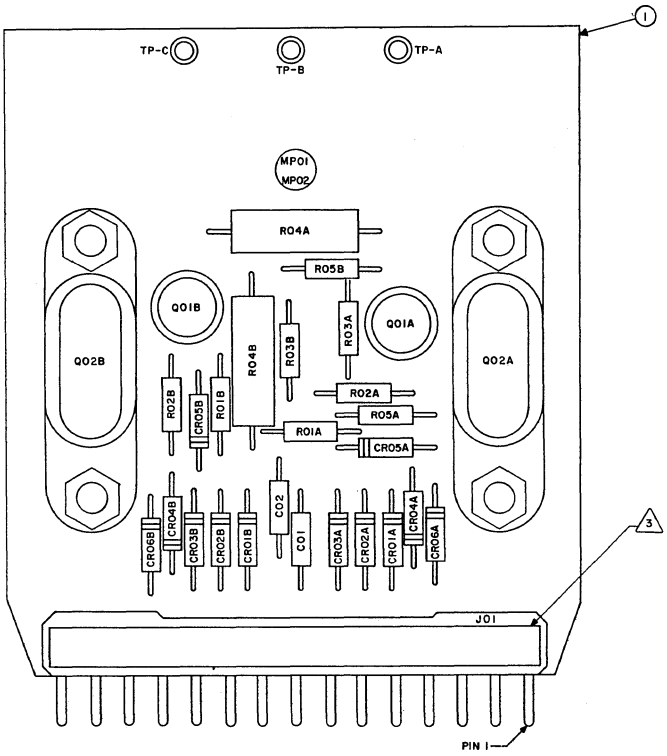
A -1.1v "0" input holds the base of Q01 at a low negative voltage with respect to the emitter, so that Q01 conducts relatively little. However, a -5.8v "1" input

results in a base current sufficiently large so that Q01 conducts heavily.

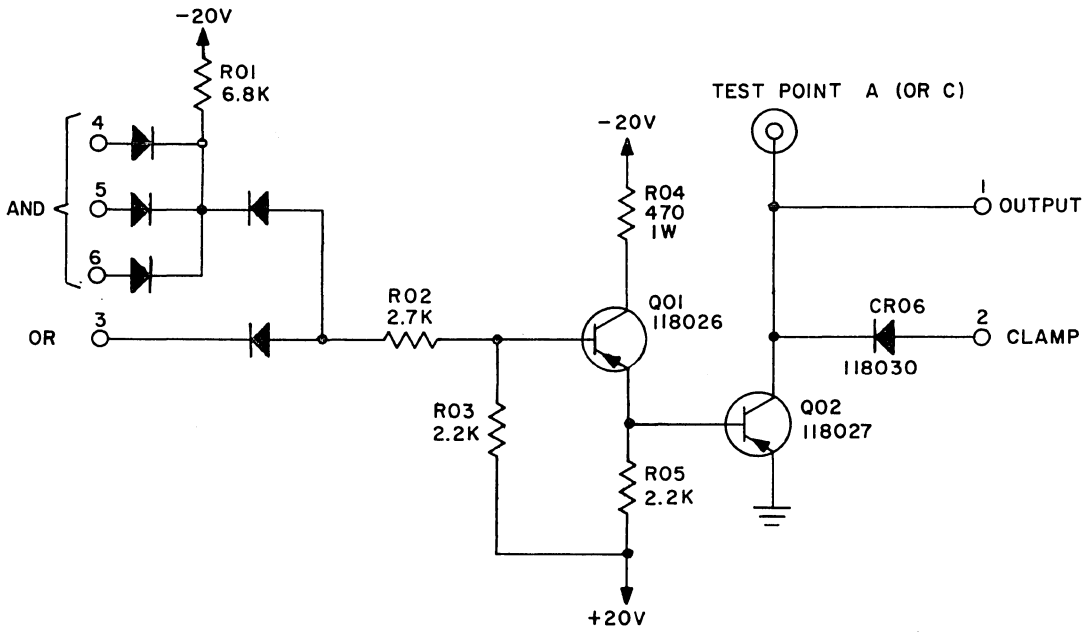
Transistor Q02 is a grounded emitter stage driven by the emitter follower Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the negative voltage region, so that Q02 also switches on the conducts heavily. Likewise, when Q01 switches off, Q02 switches off and the positive voltage source applies a reverse bias to the base-emitter junction of Q02 so that it is well into the cut off region.

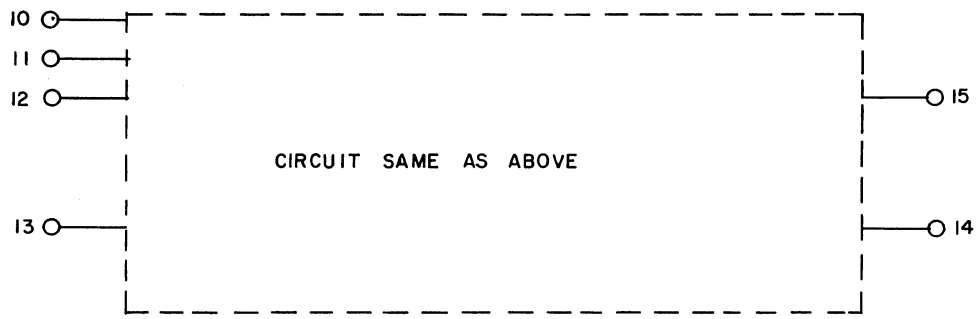
GROUND RULES

1. Any inductive load must be by-passed by the clamp diode.
2. The power supply voltage which drives the load must not exceed 40 volts.
3. With a 40v supply, load current cannot exceed 0.5 ampere; with a 20v supply, load current cannot exceed 1 ampere.
4. In case an entire AND group is unused, at least one of the inputs must be grounded.



COMPONENT LAYOUT





NOTE:
1. A -5.8V "1" INPUT CAUSES TRANSISTORS TO SWITCH TO CONDUCTION STATE.
2. LOGIC DIODES ARE 245021.

Relay Driver C84

STROBE SHAPER
Card Type C85

FUNCTION

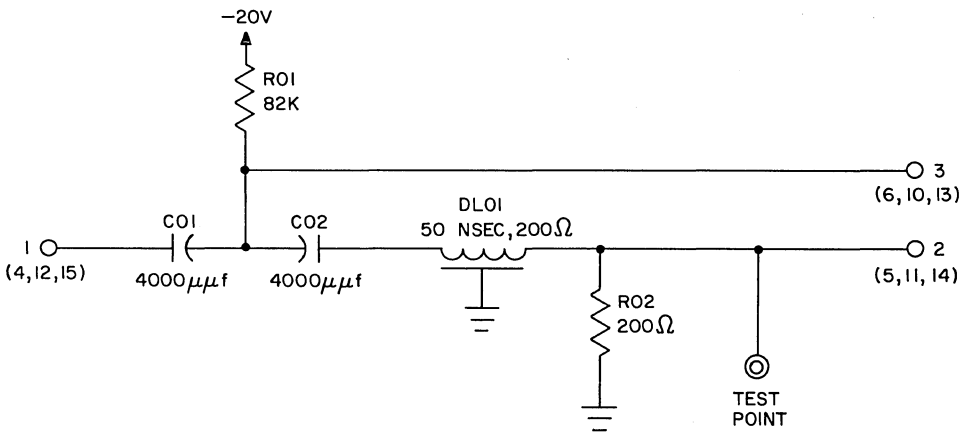
This circuit operates with a Receiver circuit contained on card type C61. Their function is to convert a delay line output (received via an Emitter Follower circuit on card type C07) into a -1.1v "0" pulse 50 nanoseconds in length.

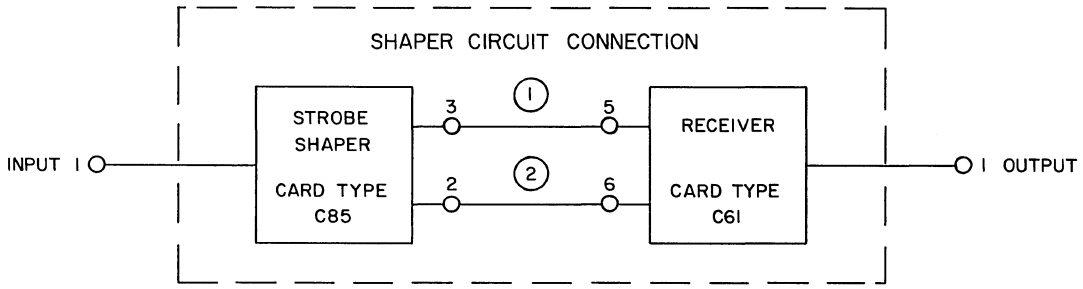
OPERATION

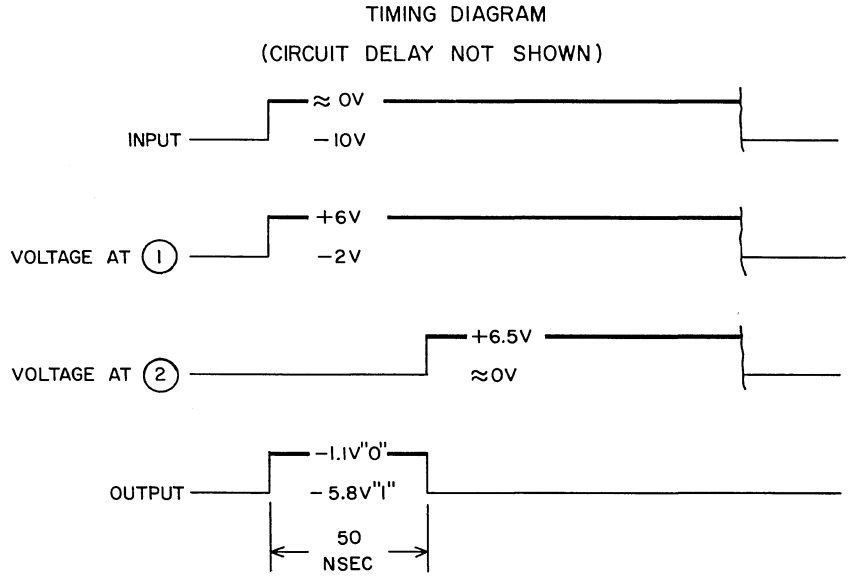
As shown on the accompanying diagram, the input from the Emitter Follower circuit is a positive-going pulse with a swing from -10v to ground, approximately. This input is received by the Strobe Shaper circuit and immediately appears on one of the outputs, causing the Receiver output to switch to -1.1v "0". After a delay of 50 nanoseconds, the input signal appears on the other output, causing the Receiver output to return to -5.8v "1". When the input signal drops, the bias from -20v through R01 holds the Receiver output at -5.8v "1".

Capacitors C01 and C02 isolate the input and the delay line output from the -20v bias voltage. The d-c levels of the input and output are approximately the values shown in the timing diagram.

The delay line is 50 nanoseconds, with a 200-ohm characteristic impedance. The 200 ohm resistor R02 provides impedance matching between the delay line and the Receiver input.







Strobe Shaper C85
(Four Circuits per card)

AMPLIFIER - SHAPER

Card Type C89

FUNCTION

The function of this circuit is to convert the sine wave output of a crystal oscillator into a chain of -5.8v "1" pulses of approximately 0.2 us duration. The input is a sine wave about ground with a peak-to-peak amplitude of approximately 3v. The -5.8v "1" pulse output is produced immediately after the input crosses the zero axis in the positive-going direction.

OPERATION

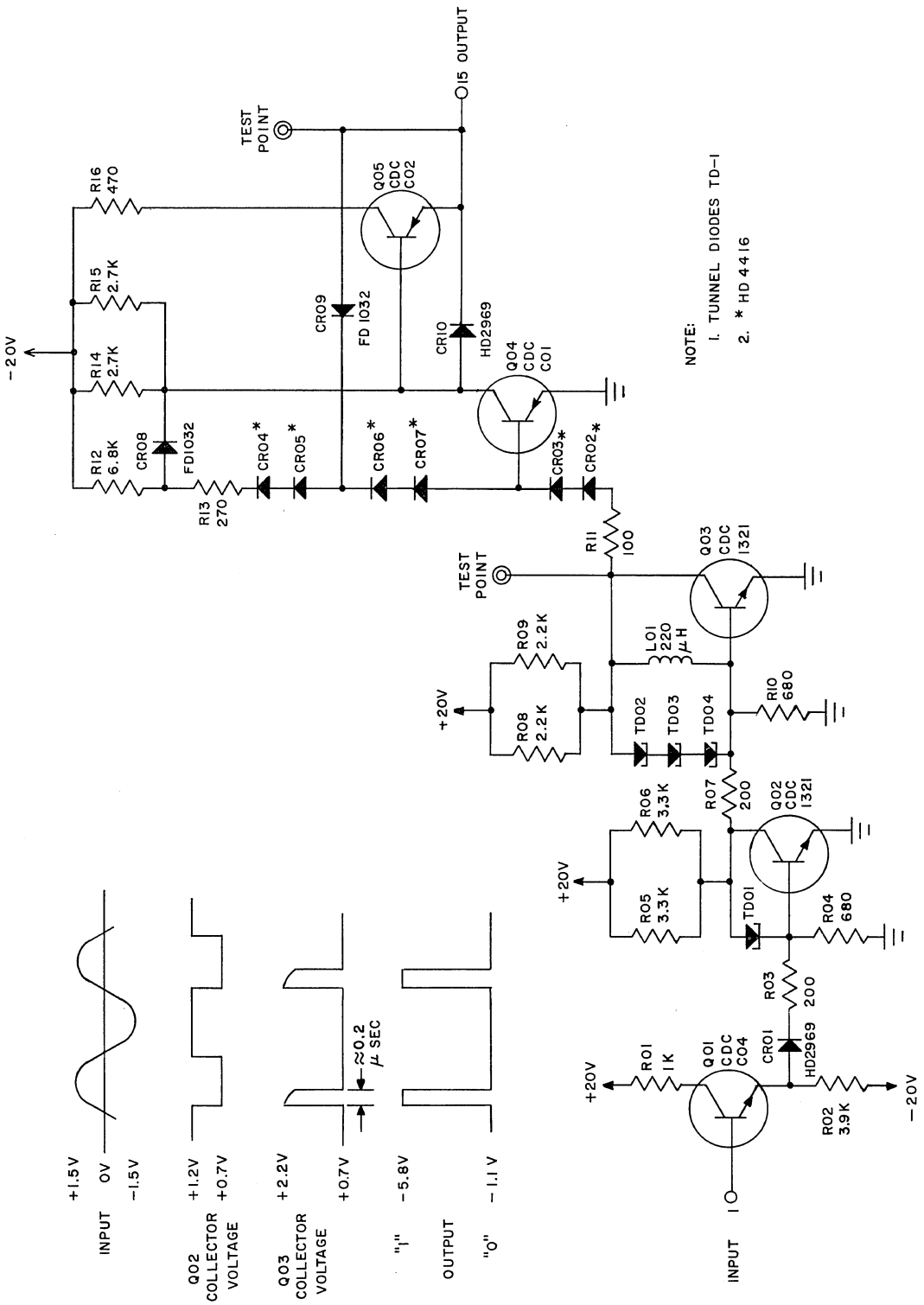
The width of the output pulse is approximately 0.2 us and is determined by the 200 uh inductance L01. The repetition rate of the output is determined by the frequency of the input signal.

The input signal is applied to the base of transistor Q01, which is an NPN silicon type CDC C04. In this application, it is used as an emitter follower current amplifier providing drive current for transistor Q02.

Transistors Q02 and Q03 are CDC 1321, which is a high speed NPN silicon type having a gain-bandwidth of 1 kmc. Each of these transistors has a base to collector tunnel diode network which produces an essentially square waveform and establishes its voltage level.

The tunnel diodes used are type TD-1. This is an axial tunnel diode having an I_p = 1 ma and a V_{fp} = 500 mv. Assuming an ideal case, the three tunnel diodes connected to Q03 would switch at 1 ma with a composite V_{fp} = 1.5v. Due to slight individual differences, no two tunnel diodes ever switch at exactly the same point, but the difference is negligible in this high speed application.

As shown in the accompanying diagram, a positive-going input results in a -5.8v "1" output of approximately 0.2 us duration. As the input goes positive, Q01 provides drive current to Q02 so that it switches to a state of heavy conduction. This results in minimum current flow through TD01 so that it switches to its low voltage state. The collector voltage of Q02 is therefore approximately equal to its base-emitter junction drop of +0.7v, being a grounded emitter silicon transistor. Transistor Q02 in its conduction state allows current flow to increase through TD02, TD03, and TD04, so that they switch to their high voltage states. This causes conduction through Q03 to



Amplifier Shaper C89

decrease, and its collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter junction drop, a total of +2.2v. This voltage level causes Q04 to switch to a state of minimum conduction and the circuit output becomes a -5.8v "1".

The length of the -5.8v "1" output pulse is determined by the 220 uh inductance L01. The tunnel diodes are able to switch state almost instantaneously while current through the inductance increases exponentially. After a time of approximately 0.2 us, current through the inductance has increased to the point that the tunnel diodes are effectively by-passed and they return to their low voltage states. This reduces the collector voltage of Q03 to approximately +0.7v, which causes Q04 to conduct heavily and returns the circuit output to a -1.1v "0".

A negative-going circuit input prevents Q01 from providing drive current to Q02. This allows current through TD01 to increase, causing it to switch to its high voltage state. Conduction through Q02 decreases and its collector voltage becomes equal to the sum of the tunnel diode voltage and the base-emitter junction drop, a total of +1.2v. This provides forward drive to the base of Q03, holding the circuit in the quiescent state.

The portion of the circuit consisting of Q04, Q05, and their associated biasing network is similar to a logical inverter, which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.

READER LEVEL AMPLIFIER
Card Type C91

FUNCTION

This card contains two identical circuits, the function of which is to convert solar cell outputs from a punched card reader into logical "0" signals of -1.1v. The circuit input is driven by one of the solar cells at a card reading station. When the solar cell senses a hole in the card, the circuit output switches to a -1.1v "0". If no hole is sensed, the output remains a -5.8v "1".

OPERATION

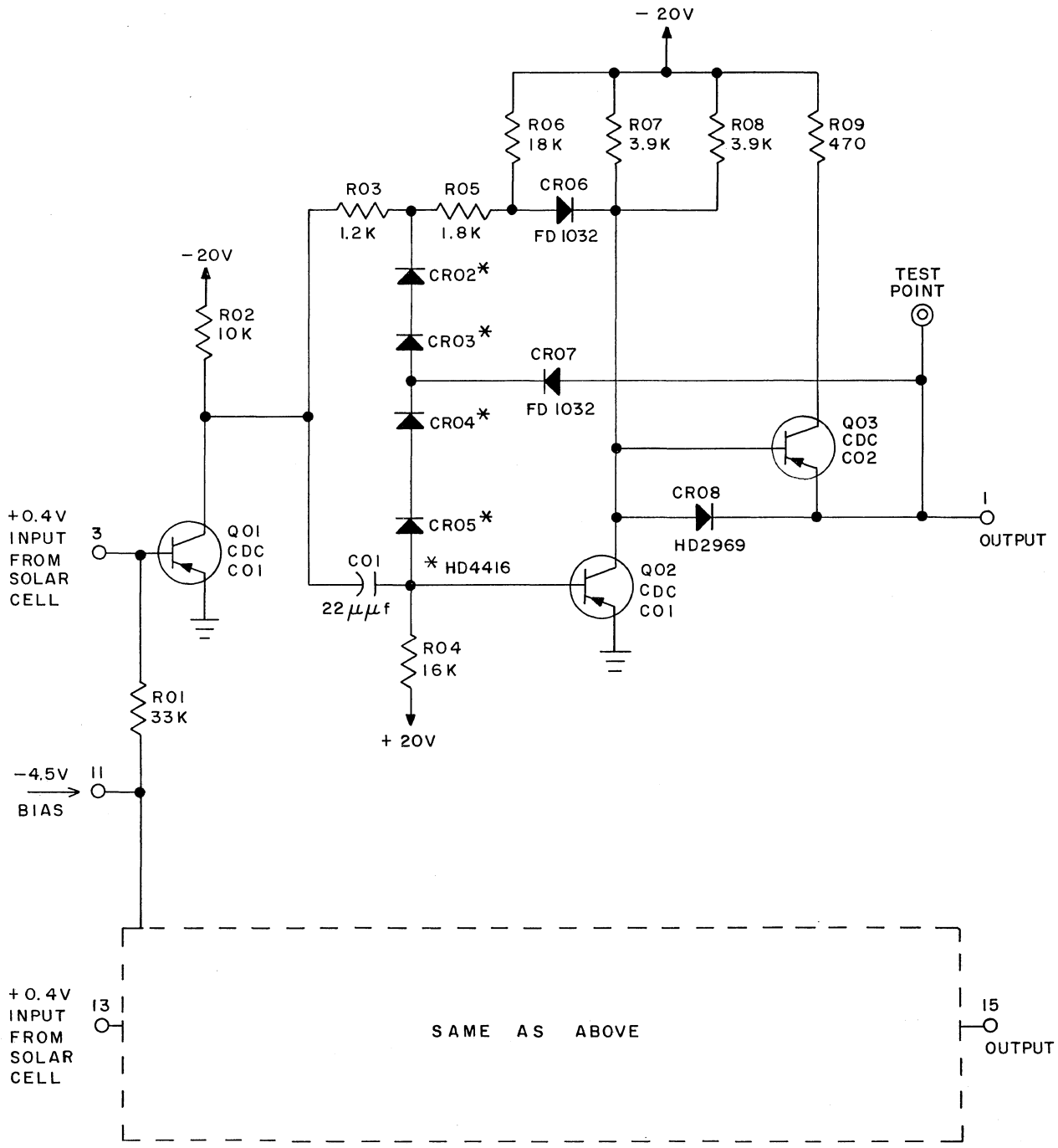
Inputs to the circuit are provided by a solar cell at the card reading station, and the signal levels are +0.4v and open circuit. The +0.4v signal results when light shining through a hole in the punched card activates the solar cell. If a hole is not present, light is prevented from striking the solar cell and its high impedance produces essentially an open circuit. Any leakage current is not more than a few ua.

The two circuits on this card are single inverters having one OR input which is fed by the network consisting of resistors R01, R02, and transistor Q01. In both circuits, the base of transistor Q01 is biased through resistor R01 to the -4.5v supply at pin 11.

An open circuit input allows the -4.5v supply at pin 11 to apply a strong forward bias to the base of Q01. This causes Q01 to conduct heavily and its collector potential becomes approximately -0.5v. The low collector voltage of Q01 is applied to the cathode of input diode CR01 and causes the inverter to provide a -5.8v "1" output.

A +0.4v input reverse biases the base-emitter junction of Q01 so that Q01 is cut off. Its collector potential rises toward -20v, but is clamped at approximately -6v by the input impedance of the inverter and the drop across R02. The -6v collector potential of Q01 is applied as an input to the inverter and causes its output to switch to a -1.1v "0".

The remainder of the circuit is identical to a logical inverter which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.



Reader Level Amplifier C91

OVERLOAD PROTECTOR
Card Type C94

FUNCTION

This circuit provides protection from excessive current flow in the memory drive lines (labeled X and Y in the 3600 system). In addition, it monitors the drive and inhibit voltages and disables the logic if any of these voltages fall below operating level. As shown in the accompanying diagram, the circuit contained on card type C94 operates in conjunction with other power supply components which are mounted elsewhere. The memory drive power supply system is disconnected if the type C94 card is removed from its connector.

Typical external connections to a C94 card are shown on page 5-C94-3. For the actual wiring of the Overload Protector circuit in the 3609 Storage Module, see the 3609 Diagrams manual, Pub. No. 60042000.

OPERATION, Over-Current Protectors

The card contains two identical circuits for dropping power if a current overload occurs in the X or Y drive scheme. This is shown with the principal current paths indicated by heavy lines. Normal current flow to the X or Y gate circuits is of the order of 900 ma. If this should increase to approximately 1.4 amperes, the voltage drop across the 18-ohm resistor causes the transistor to switch to its conduction state, firing the silicon controlled rectifier.

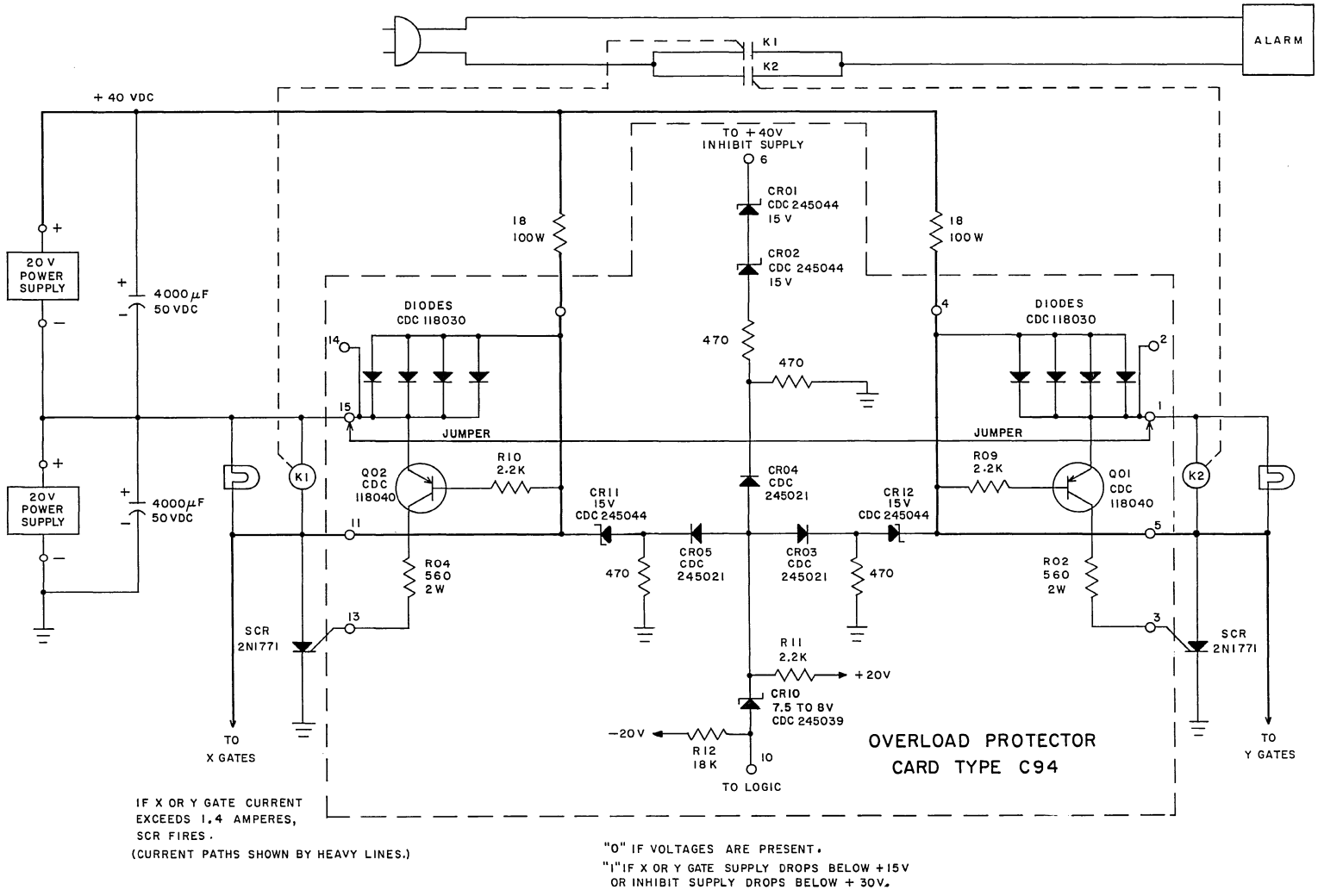
During normal operation, the rank of four CDC 118030 diodes are in a state of heavy forward conduction and the drop across the 18-ohm resistor is very close to 19.3v. The output supplied to the gate circuits is the voltage at the anodes of the diodes and is around 20.7 volts (20v plus 0.7v forward diode drop). A heavier output current results in a greater drop across the 18-ohm resistor, and when the current reaches approximately 1.4 amperes, the diodes cut off. A further increase in current draws turn-on current through the transistor causing it to switch on, which fires the silicon controlled rectifier (SCR).

As shown in the diagram, the SCR in its high conduction state grounds the output to the gate circuits, lights an indicator, and closes a relay to sound an alarm. The SCR may be returned to its OFF state by lowering the power supply voltages to zero.

OPERATION, Voltage Monitor

This portion of the circuit monitors the +20v gate supplies and the +40v inhibit supply. If these three voltages are present, a "0" output of approximately -0.7v appears at pin 10. If the inhibit supply falls below +30v, or if either gate supply falls below +15v, this output switches to a "1" of approximately -6.5v, disabling the operation of the memory logic.

A 3-way AND connection is provided by diodes CR03, CR04, and CR05, so that a low input voltage to any diode results in a "1" output. A level-shifting action is provided by the zener diode CR10. This diode is back biased sufficiently so that the voltage across it is a constant 7.5 to 8v.


ALARM
K1
K2
+ 40 VDC
TO +40V
INHIBIT SUPPLY
6
CR01
CDC 245044
15 V
CR02
CDC 245044
15 V
18
100W
18
100W
20 V
POWER
SUPPLY
4000μF
50 VDC
DIODES
CDC 118030
470
470
4
DIODES
CDC 118030
14
2
15
1
JUMPER
JUMPER
20 V
POWER
SUPPLY
4000μF
50 VDC
K1
Q02
CDC
118040
R10
2.2K
CR11
15V
CDC 245044
CR04
CDC
245021
CR12
15V
CDC 245044
R09
2.2K
Q01
CDC
118040
K2
11
5
CR05
CDC
245021
CR03
CDC
245021
470
470
R04
560
2W
R02
560
2W
13
3
SCR
2N1771
SCR
2N1771
R11
2.2K
+20V
CR10
7.5 TO 8V
CDC 245039
-20V
R12
18K
10
TO LOGIC
TO
X GATES
TO
Y GATES
OVERLOAD PROTECTOR
CARD TYPE C94
IF X OR Y GATE CURRENT
EXCEEDS 1.4 AMPERES,
SCR FIRES.
(CURRENT PATHS SHOWN BY HEAVY LINES.)
"0" IF VOLTAGES ARE PRESENT.
"1" IF X OR Y GATE SUPPLY DROPS BELOW +15V
OR INHIBIT SUPPLY DROPS BELOW + 30V.

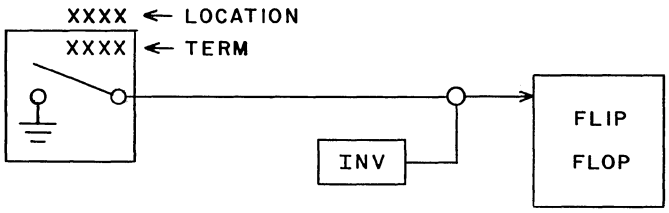
COMPUTER DIVISION

PRINTED CIRCUIT DESCRIPTION

CHANNEL DISABLE
Card Type CA97

FUNCTION AND OPERATION

This card contains a single-pole, double-throw toggle switch and a biasing network by which the output pins may be held at either -6.8 volts or ground, representing a logical "1" or "0". The card is designed to be used as a controlling input to an AND gate, providing a means of manually disabling the input.

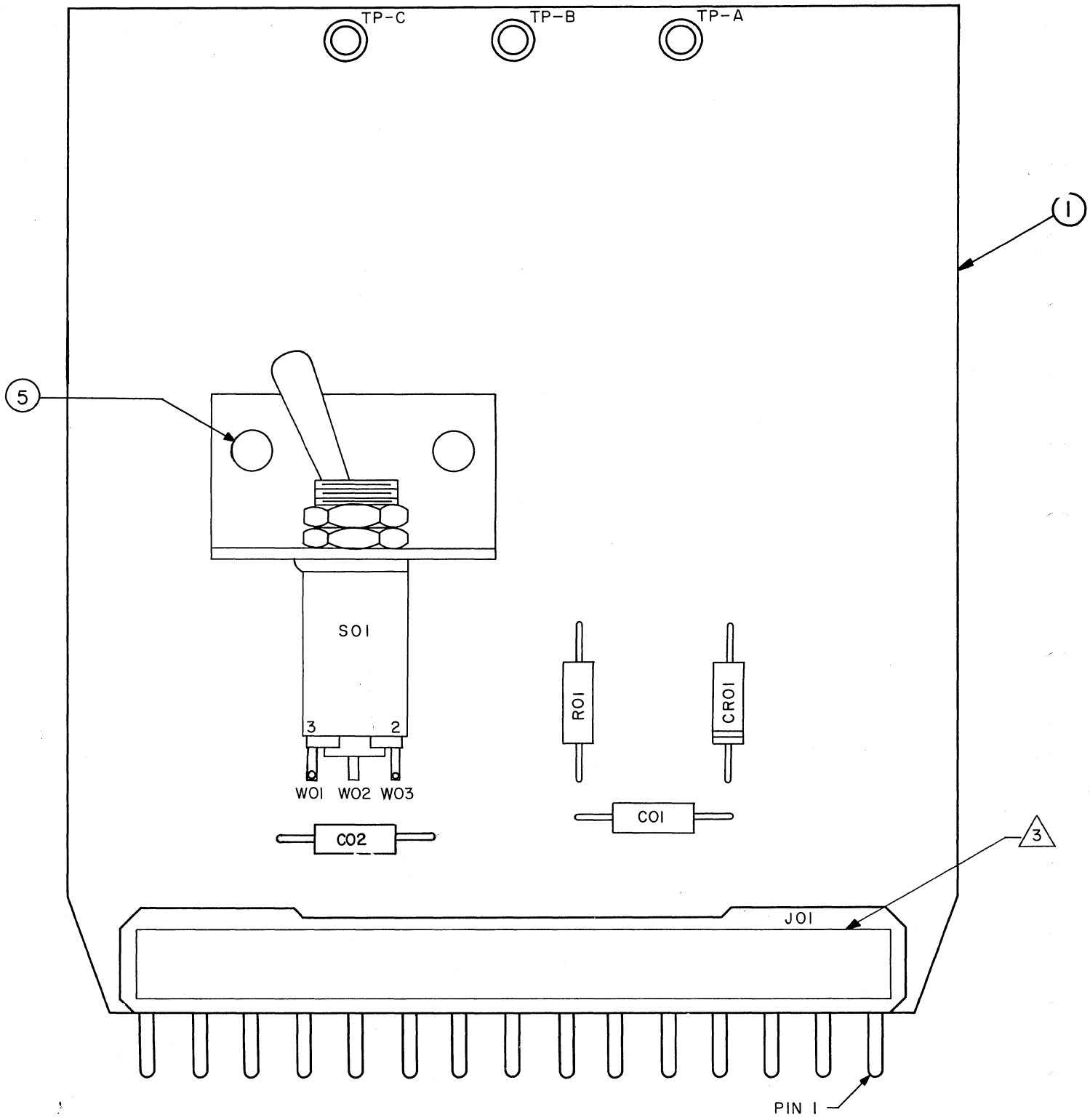


LOGIC DIAGRAM SYMBOL

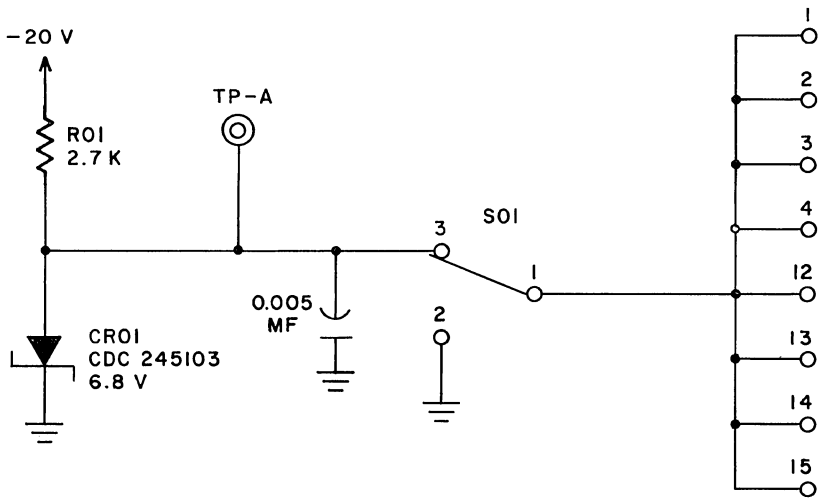
RELATED DOCUMENTS	NUMBER
Parts List	30938600
Assembly Drawing	30938600
Schematic Drawing	30938700
Engineering Specification	None

GROUND RULES

1. Each output can control 12 AND gates.
2. Because of the size of the switch, the card location adjacent to the component side of the CA97 card cannot be used.



COMPONENT LAYOUT

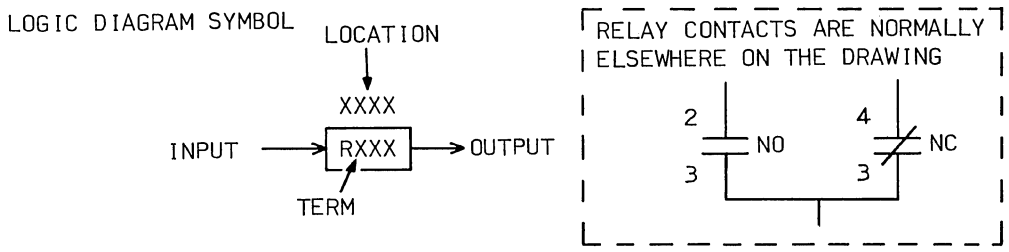


Channel Disable CA97

RELAY CARD
Card Type CC10

FUNCTION

This card, containing two relays, provides isolated, form D (make-before-break), relay contacts.



RELATED DOCUMENTS	NUMBER
Parts List (Bill of Materials)	A65172100
Card Assembly Drawing	C65172100
Schematic Drawing	B65172400
Specification	None

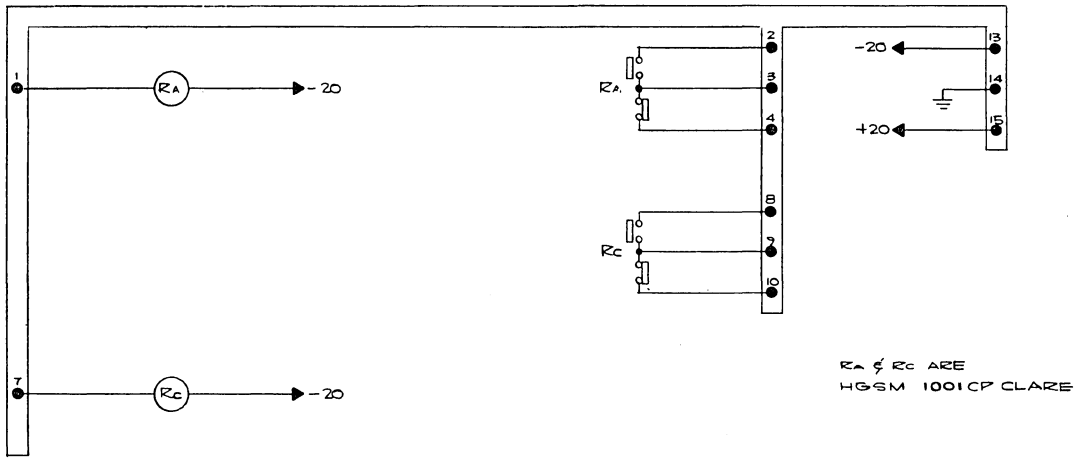
OPERATION

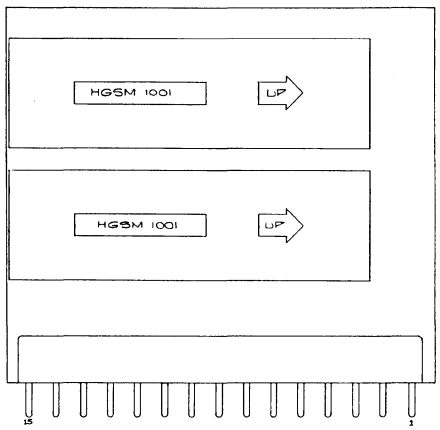
The two relays, with mercury-wetted contacts, are mounted on a standard printed circuit card which requires the mounting space of two logic cards because of the thickness of the relays. They are driven by standard logic driver cards. The relays are fast-operating, reliable, and without any contact bounce.

With -20 vdc on the input line to circuit RA (identical to circuit RC in operation), the relay contacts are in the quiescent condition as shown on the schematic drawing. After the relay driver card forces RA to zero volts, a drop of -20 vdc across RA allows the relay to energize and, in turn, change the contacts to a configuration opposite of that in the schematic drawing.

GROUND RULES

1. The individual relay input requires a drive current of a least 17 ma at -20 vdc.
2. Contact current must not exceed 2 amp.
3. Power requirements: -20 vdc ± 10% at 34 ma (pin 13)
   +20 vdc (Pin 15 not used)
   Ground (Pin 14)


1
RA
-20
RA
2
3
4
-20
13
14
+20
15
8
RC
7
16
7
RC
-20
RA & RC ARE
HGSM 1001 CP CLARE


HGSM 1001
UP
HGSM 1001
UP
15
1

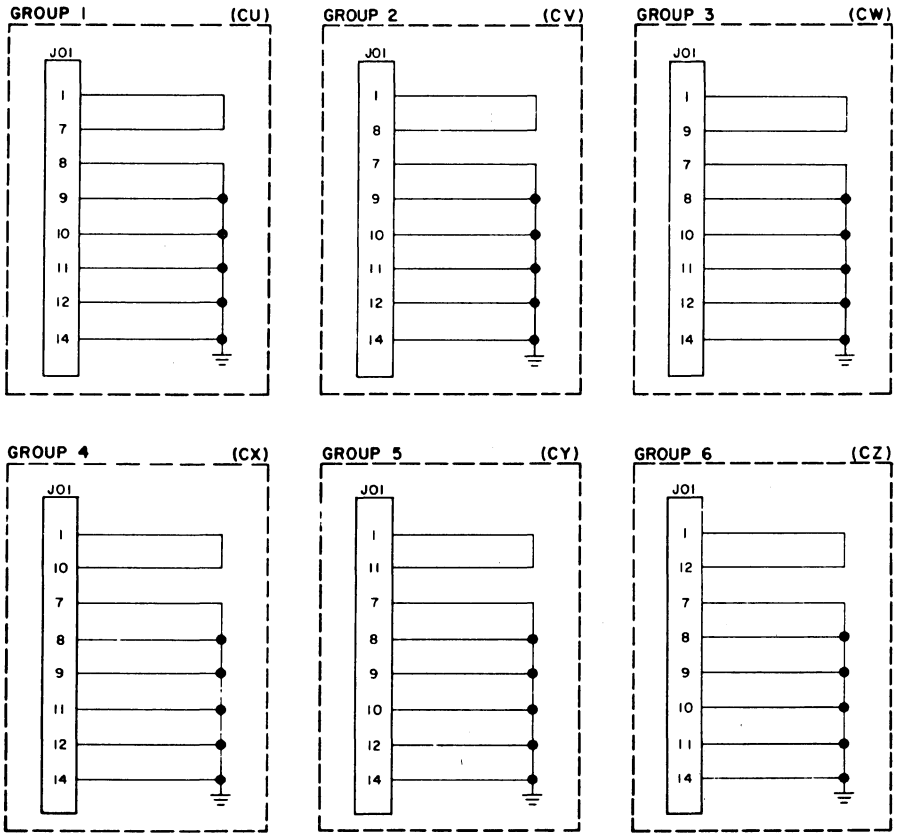
JUMPER
Card Type E00

E00 cards were developed by OPCONCTR for use in select identify circuits. These circuits enable each 160-A computer to identify itself, via program control, with respect to other 160-A computers in the system. Each of the six groups of jumper cards is wired to transmit one specific output pulse. Depending upon the bit location of the logical "1" in a Select Identify EXF code (1100), a particular jumper card will receive a pulse and transmit the pulse to its computer. Jumper cards have no active components.

E00 does not use pins 2, 3, 4, 5, 6, 13 and 15. Pin 14 is grounded. Pin 1 is the only input pin used. Pins 7, 8, 9, 10, 11 and 12 are output pins. The output of the card is dependent upon which output pin is connected to pin 1; the remaining pins are grounded. A logical "1" input to pin 1 from the set side of the select identify flip-flop produces a "1" on the output pin that is connected to pin 1. The logical "1" is fed through an L card to a 160-A computer.

"1" bit locations and the unit symbols of the computers they select:

Group 1 - CU - bit 6	Group 2 - CV - bit 7	Group 3 - CW - bit 8
Group 4 - CX - bit 9	Group 5 - CY - bit 10	Group 6 - CZ - bit 11


GROUP 1
(CU)
J01
1
7
8
9
10
11
12
14
GROUP 2
(CV)
J01
1
8
7
9
10
11
12
14
GROUP 3
(CW)
J01
1
9
7
8
10
11
12
14
GROUP 4
(CX)
J01
1
10
7
8
9
11
12
14
GROUP 5
(CY)
J01
1
11
7
8
9
10
12
14
GROUP 6
(CZ)
J01
1
12
7
8
9
10
11
14

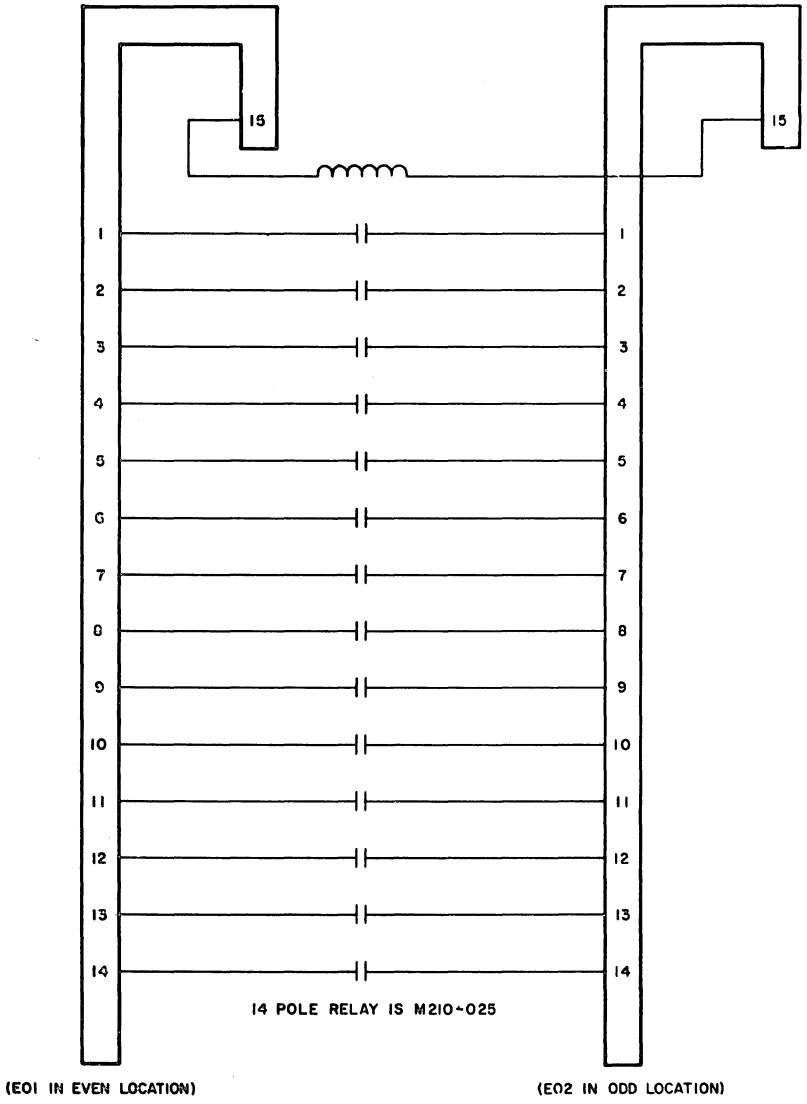
Jumper E00

CROSSPOINT MODULE
Card Types E01A and E02A

Crosspoint Module (CM) is an assembly of a 14-pole relay. The 14-pole relay, encapsulated and enclosed in an aluminum box, is between two printed circuit cards, E01A and E02A. The module has a 30 pin connector.

The relay consists of 14 miniature dry-reed switches. The simultaneous opening and closing of the 14 switch contacts is controlled by a single d-c operating coil. The coil-resistance is about 250 ohms and dissipates about 16 watts when energized with 20 volts, giving an operating current of about 80 ma. The operating and release time is about 5 usec. The life expectancy of a single reed is about 100,000 cycles.

Each reed switch is hermetically sealed in a glass capsule containing approximately one atmosphere of nitrogen. The switch consists of two nickel-iron alloy reed elements with contacts of diffused gold. The reed switch contacts are Form A, normally open. They close when a magnetic field of the required strength is applied.



Crosspoint Module E01A & E02A

CROSSPOINT CONTROL MODULE
Card Type E03A and E04A

The Crosspoint Control module consists of selection and latching relays and an Override switch. The two relays, (housed in separate cans), the override switch, and two diodes are mounted between two printed circuit cards E03A and E04A. The module has a 20 pin connector. The two diodes are used for inductive suppression. All the odd numbered pins are on E03A;, even numbered pins on E04A. Of 30 pins, only pin numbers 4, 6, 8, 12, 14, 16, 26, 28, and 30 are used; the remainder are open.

SELECTION RELAY

The selection relay consists of a Form A type reed switch and two magnetic coils excited separately. In order to close the reed switch in the relay, both coils must be energized simultaneously. However, to keep the switch closed only one coil need be energized. Since the coils are slow to magnetize, they are slow to damp out after the excitation pulse has been removed. This limits the rate at which the relay can be selected. A rate of 400 cycles per second is normal.

LATCHING RELAY

The latching relay is a Form C bi-stable device with two coils of reversible polarity. It switches the relay from one state to the other. The coil operates at a power of 300 mw with an operate time of 3 ms. A supply of 20v is needed to energize the relay.

The form C dry-reed switch has 3 contacts. The center contact (or movable reed) is located between the other two contacts. Biasing is accomplished by positioning permanent magnets adjacent to the reed leads. One reed is induced with the "N" polarity and the other with the "S" polarity.

If the release coil is excited, the center reed switches to the normally closed (NC) reed. If the operate coil is excited, the center reed switches to the normally open (NO) reed. If both coils are energized at the same time, the latching relay does not change its state.

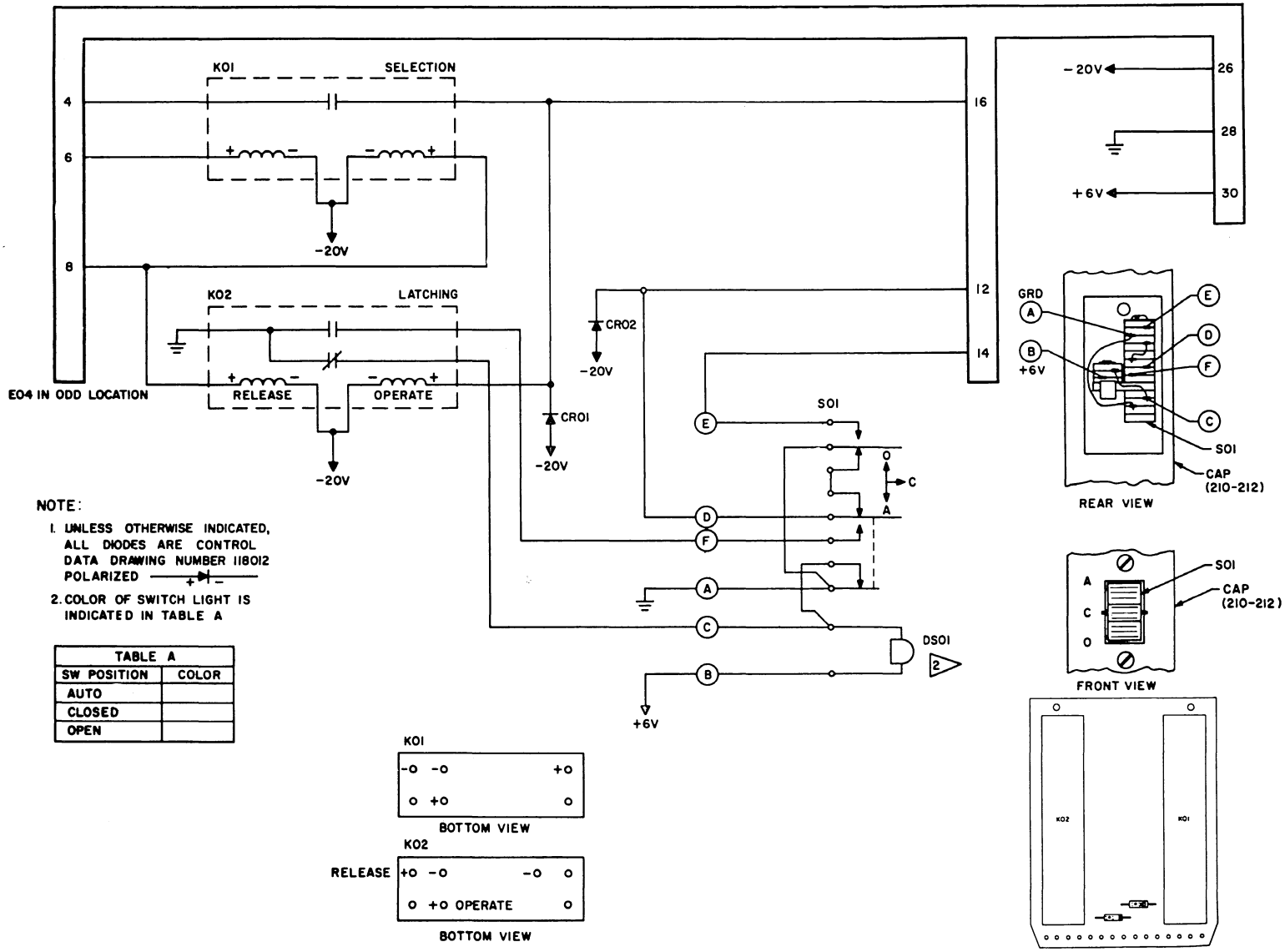
OVERRIDE SWITCH

The Override switch has three positions: Automatic (A); Closed (C), and Open (O). Each position of the Override switch is indicated by a lighted colored background.

In the A position, the circuit to the 14-pole relay coils may be either Open or Closed. In the A position, the selection or deselection of a crosspoint is automatic. The amber light is off if the latch relay is closed to the 14-pole relay (crosspoint made). The light is on if the contact is open.

In the C position, the circuit to the 14-pole relay coils is always closed.

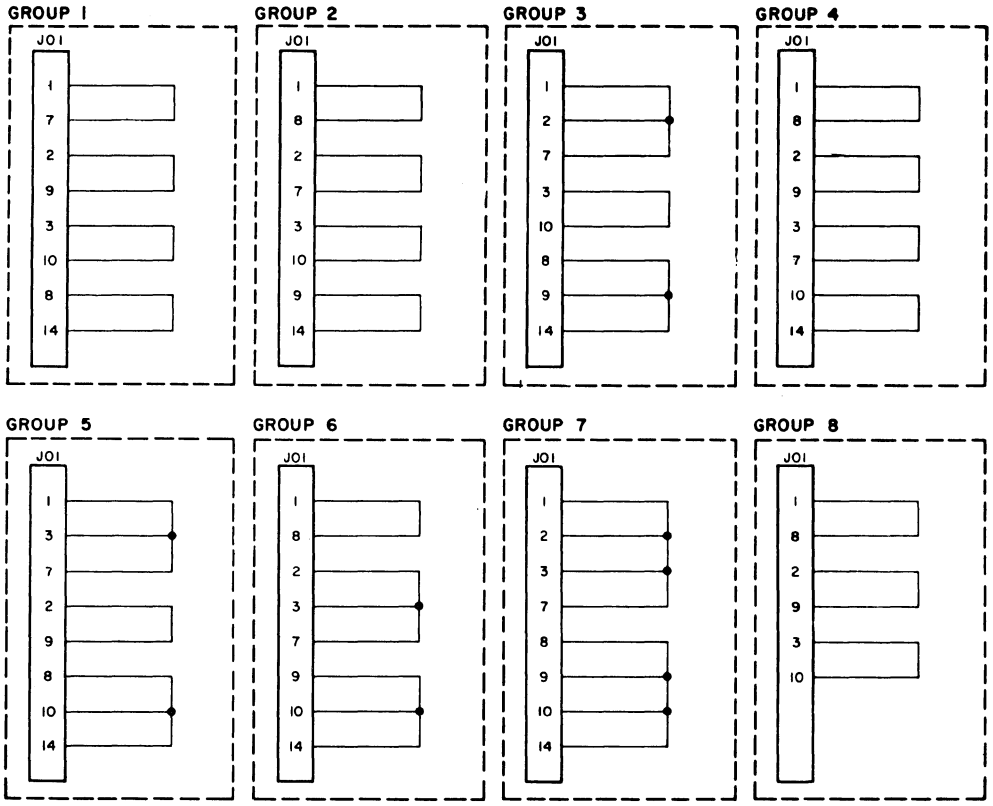
In the O position, the circuit to the 14-pole relay coils is always open.


K01
SELECTION
4
6
8
-20V
K02
LATCHING
RELEASE
OPERATE
E04 IN ODD LOCATION
CR02
CR01
16
12
14
-20V
-20V
-20V
SOI
E
D
F
A
C
B
+6V
DSOI
2
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED
2. COLOR OF SWITCH LIGHT IS INDICATED IN TABLE A
TABLE A
SW POSITION
COLOR
AUTO
CLOSED
OPEN
K01
BOTTOM VIEW
K02
RELEASE
OPERATE
BOTTOM VIEW
-20V
+6V
26
28
30
GRD
REAR VIEW
CAP (210-212)
FRONT VIEW
K02
K01

DECODER
Card Type E05

Function decoders are primarily used in the selection of equipment and peripheral device controllers. The cards receive function codes from computers and decode them, providing proper address bits for the selection of devices. The decoder cards are similar to other printed circuit cards in appearance, but have no active components. If the required pins are connected, the cards can decode any octal digit (0-7). Groups 1-7 decode octal digits 1-7 respectively; group 8 decodes 0.

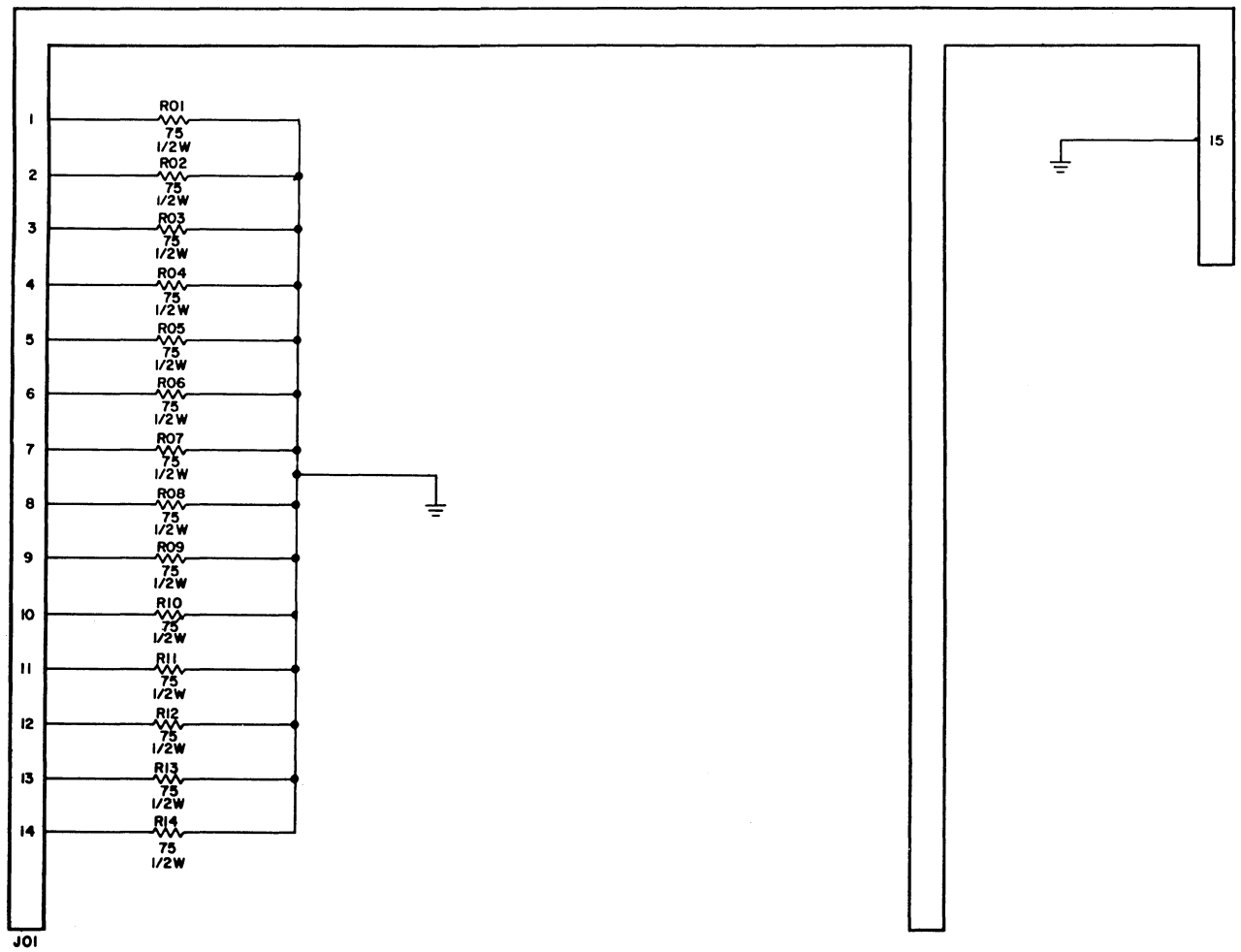
Card E05 does not use pins 4, 5, 6, 11, 12, 13 and 15. Pin 14 is grounded. The outputs from function translators are fed to pins 1, 2 and 3. Decoding is accomplished by interconnecting various combinations of pins 1, 2 and 3 with pin 7. Logical "1" inputs ANDed with pin 7 produce logical "1" outputs. Logical "0" outputs are produced by ANDing inputs with some pin other than pin 7. Logical "0" outputs are fed through an inverter to a gate where they are ANDed with the "1" output from pin 7.


GROUP 1
J01
1
7
2
9
3
10
8
14
GROUP 2
J01
1
8
2
7
3
10
9
14
GROUP 3
J01
1
2
7
3
10
8
9
14
GROUP 4
J01
1
8
2
9
3
7
10
14
GROUP 5
J01
1
3
7
2
9
8
10
14
GROUP 6
J01
1
8
2
3
7
9
10
14
GROUP 7
J01
1
2
3
7
8
9
10
14
GROUP 8
J01
1
8
2
9
3
10

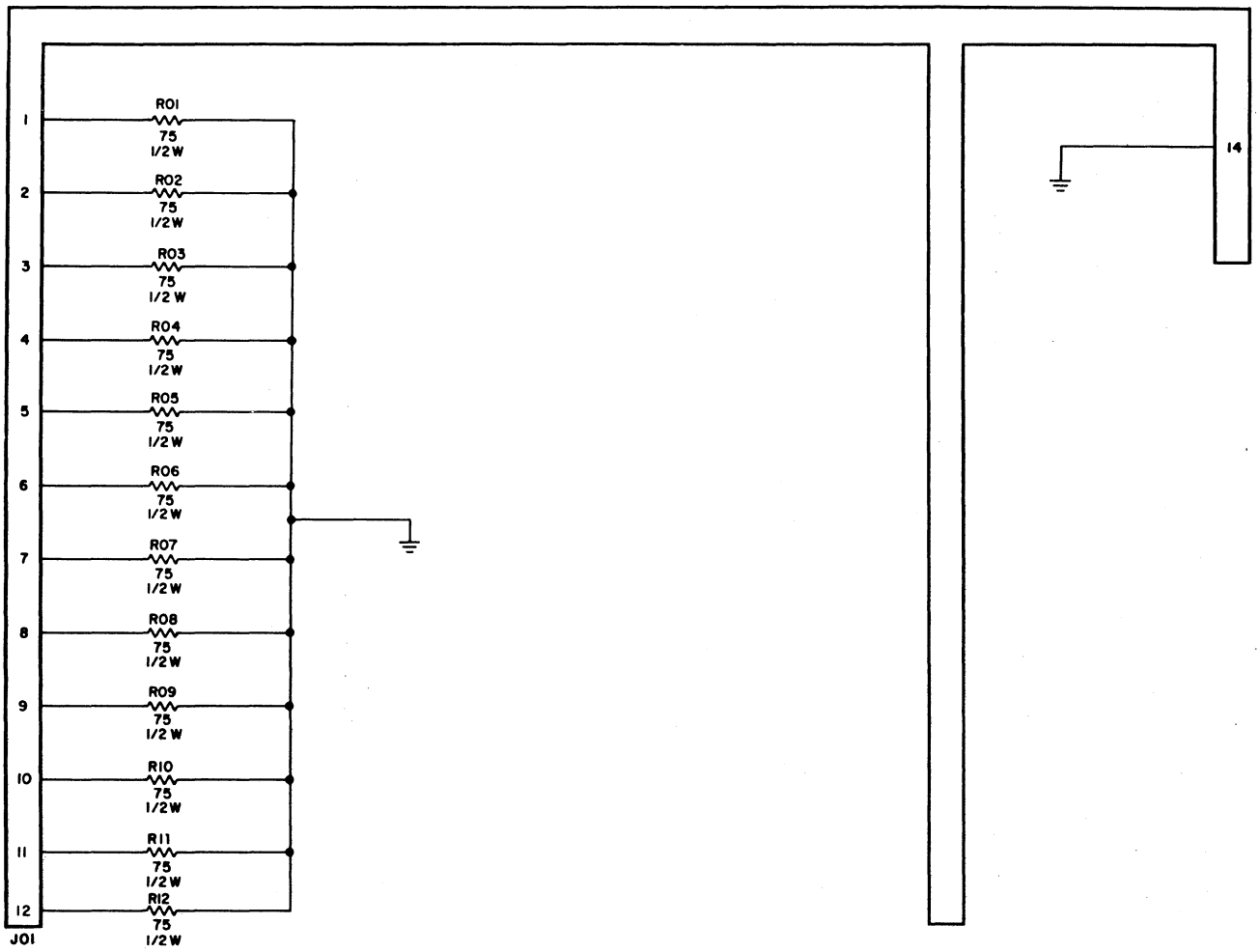
TERMINATOR

Card Types E06 and E07

Card types E06 and E07, which are used for impedance matching on inter-device cables, contain 75-ohm, 1/2-watt resistors. E06 is a 14 resistor assembly; E07 is a 12 resistor assembly.



Terminator E06

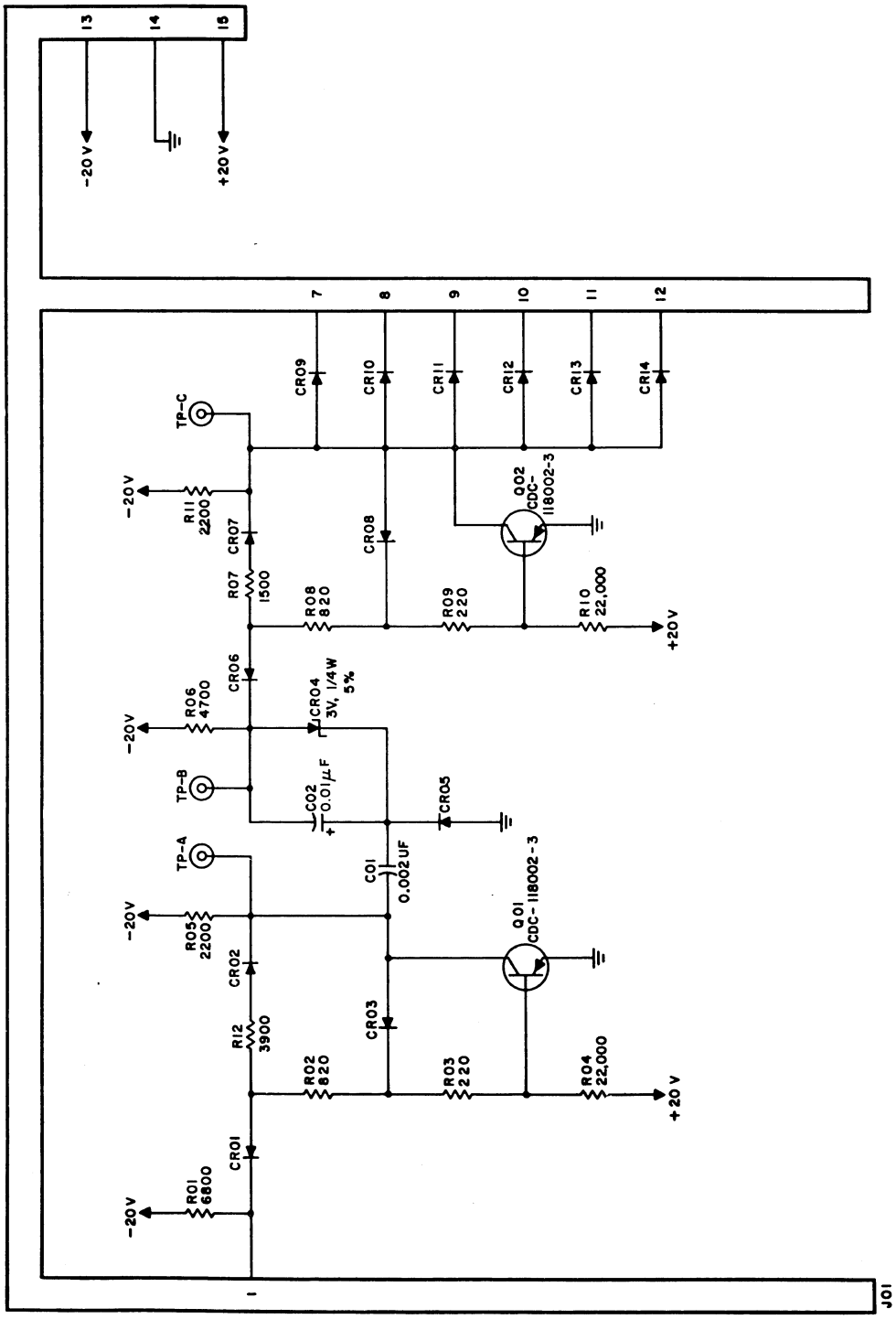


Terminator E07

SINGLE PULSER
Card Type E08

Card type E08 consists of two common-emitter inverters. The card has one input and six outputs. The main function of the card is to provide 6 outputs for one input of the same voltage level and phase.

An input of -0.5v "0" at pin 1 provides 3.0v across diode CR04. This 3.0v fed through the inverter, consisting of transistor Q03, gives an output of -0.5v "0" at pins 7-12. Similarly, an input of a -3v "1" at pin 1 provides an output of -3.v "1" at pins 7-12. An input of -3v "1" at pin 1 grounds capacitor C01 and provides +1.0v as an input to the second stage of the circuit. This will decay to -3.0v as C01 discharges. Capacitor C01 cannot recharge until the input to pin 1 again returns to 0.5v "0".

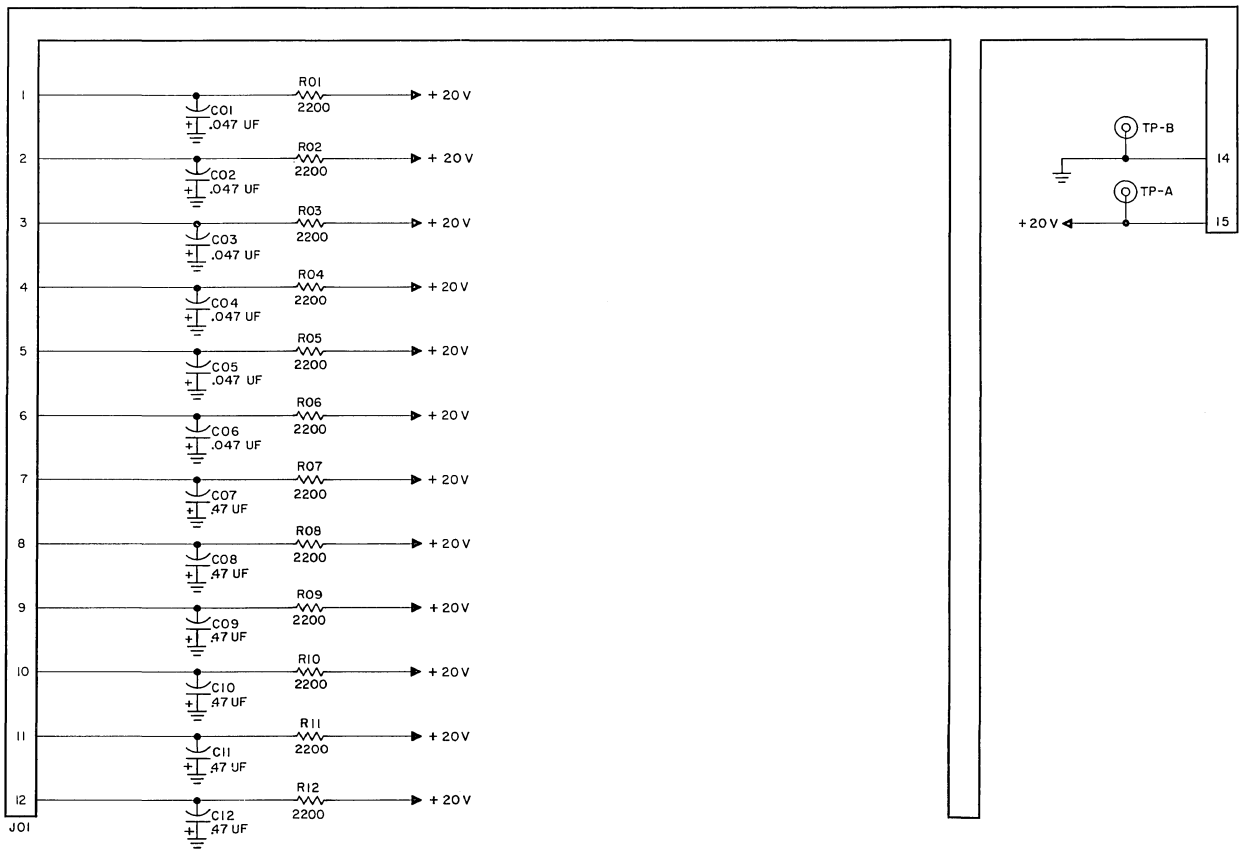


Single Pulser E08

INTEGRATOR

Card Type E10

Card Type E10 is a simple filter to remove unwanted signals or noises from the mechanical devices (e.g., a card reader or card punch). Card E10 can also be used as a delay.

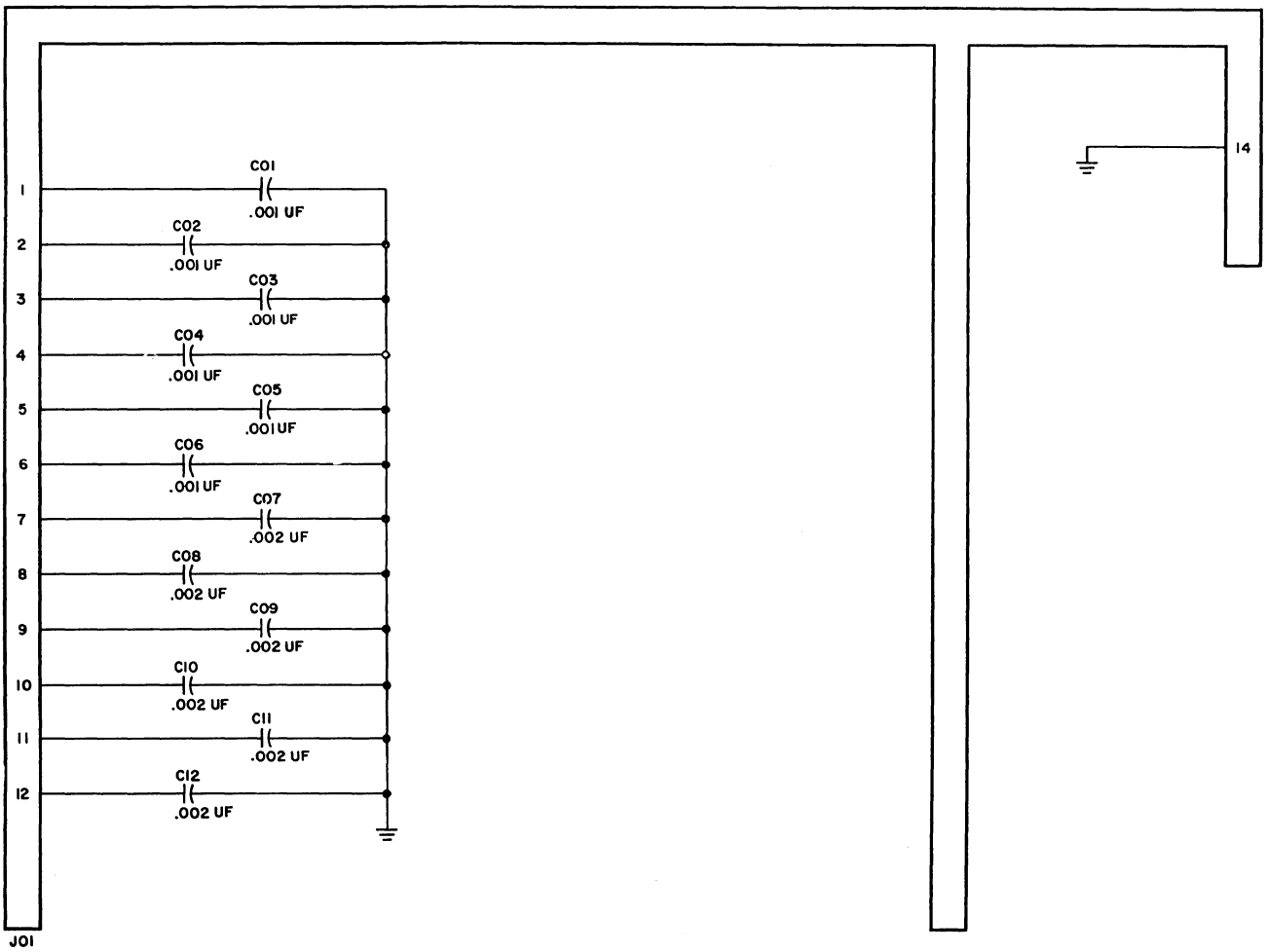


Integrator E10

DELAY

Card Type E11

Card type E11 is a bank of two types of capacitive delays: .001 uf and .002 uf. A .001 uf capacitor causes a delay in 1604-type logic of half a usec, and a .002 uf capacitor causes a delay of 1 usec to the incoming signal. .001 capacitors are connected to pins 1-6; .002 capacitors are connected to pins 7-12. Pin 14 is grounded, and pins 13 and 15 are not used.



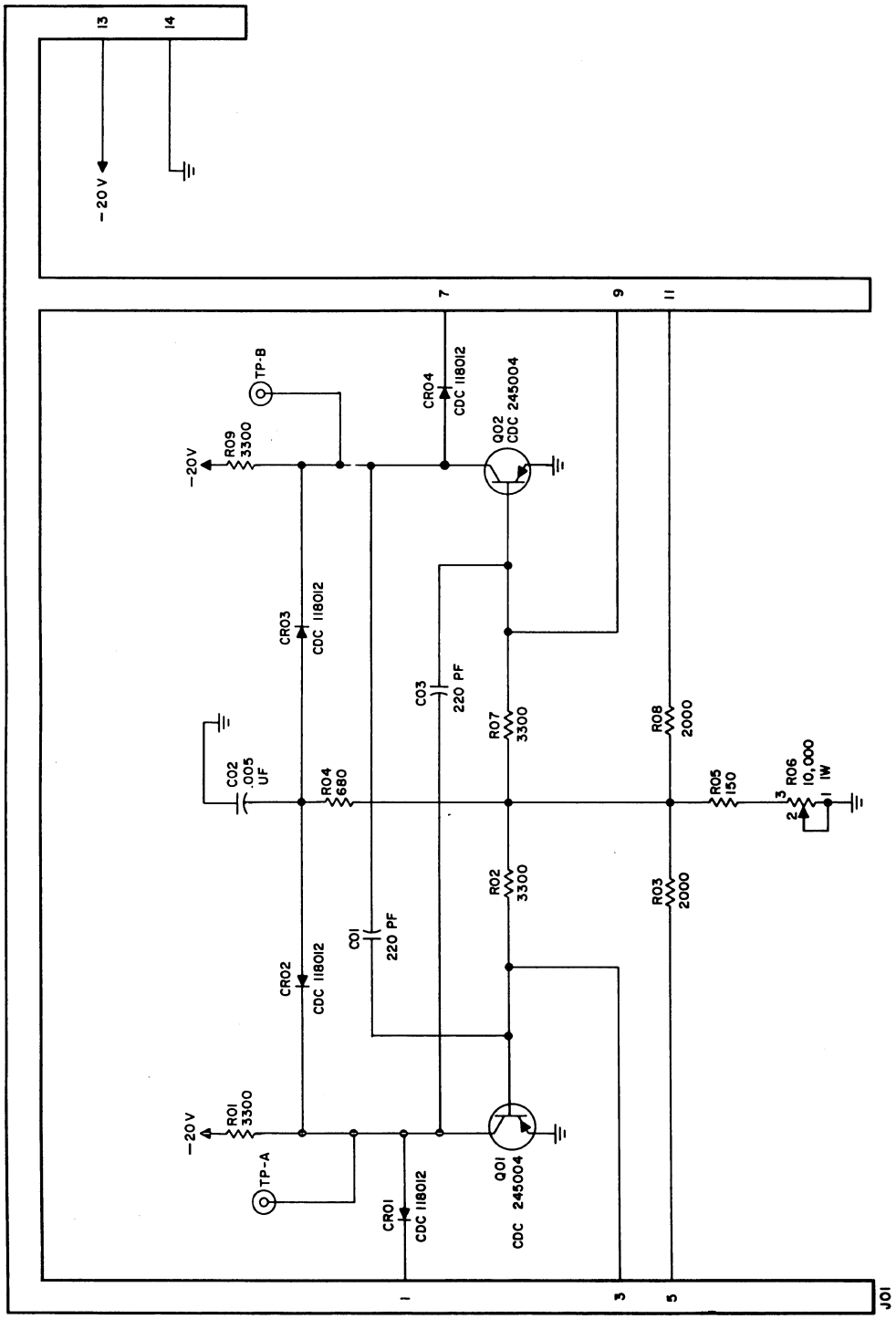
Delay E11

VARIABLE CLOCK
Card Type E14

Card type E14 is a variable clock or a free-running multivibrator with a frequency range of 4kc to 1.5 megacycles. The frequency is changed by varying the time-constant of the circuits, i.e., by jumper pins 3 and 5 or by the variable resistance R06.

The charge on a capacitor and the voltage across its plates cannot change instantly; these factors affect operation. Capacitor C01 connects the base of transistor Q01 with the collector of Q02, and capacitor C03 connects the base of Q02 with the collector of Q01. When supply voltage (-20v) is initially applied, currents flow in the various circuit branches and the capacitor builds up charge. Because the two halves of the circuit are alike, currents are alike at first, but even the slightest imbalance results in a cumulative difference in the two collector currents, saturating one of the transistors and cutting off the other. Outputs are obtained from pins 1 and 7. Diodes CR02 and CR03 switch the two transistors from one state to the other.

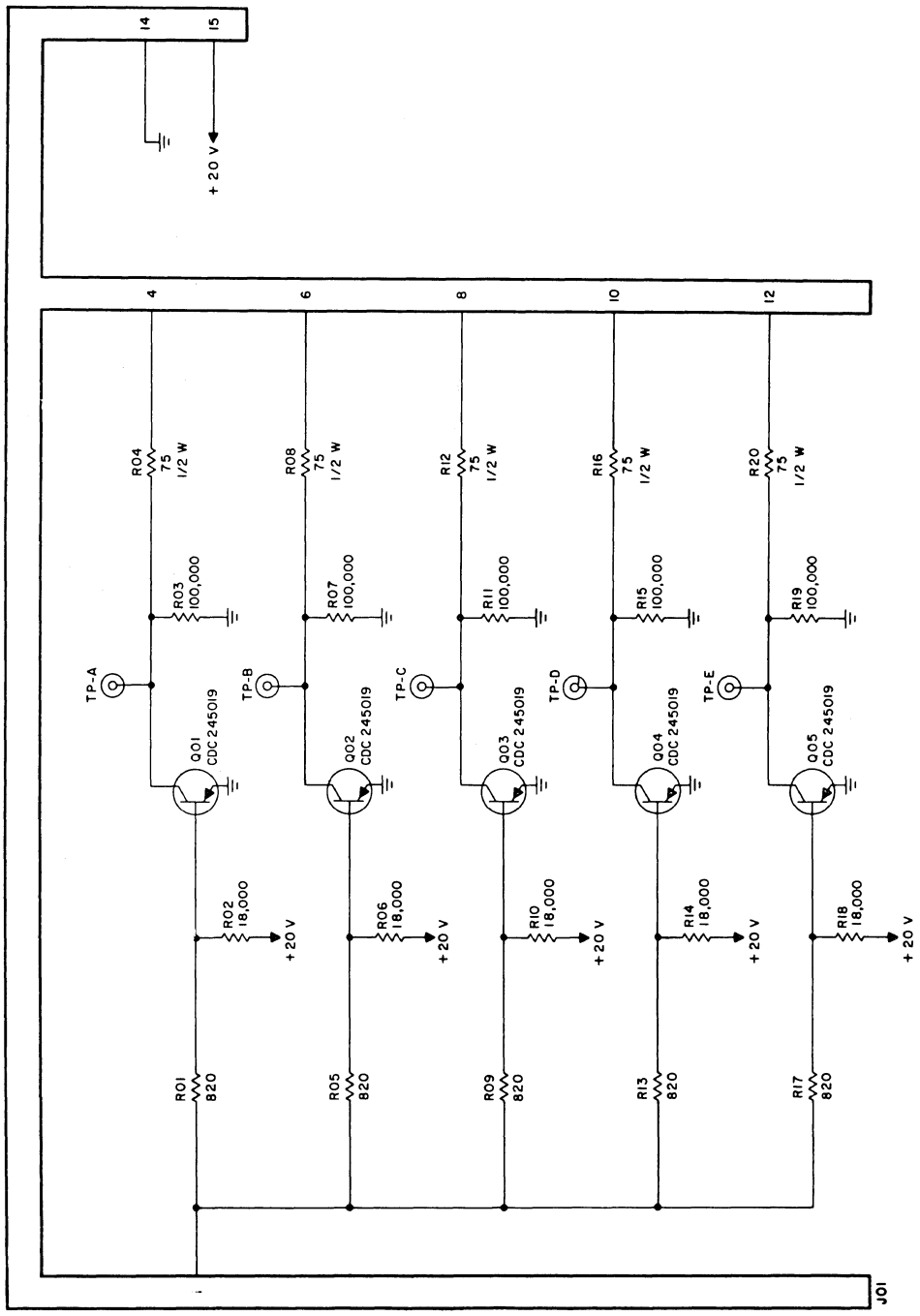
Once the circuit is triggered, it continues to provide an output at the desired frequency, as long as the supply voltage is maintained.



Variable Clock E14

TERMINATOR
Card Type E19

Card type E19 contains five terminator circuits that are switched by transistors. When the transistors are conducting, the circuits serve as impedance matchers; when the transistors are not conducting, the circuits serve as bleeders. E19 has a single input at pin one and outputs at pins 4, 6, 8, 10 and 12. When the voltage level at pin 1 is at or near -6v potential, the transistors conduct, providing 75 ohms resistance from the output pins to ground. An input of 0 volts at pin 1 cuts off the transistors, providing 100K ohms resistance from the output pins to ground.

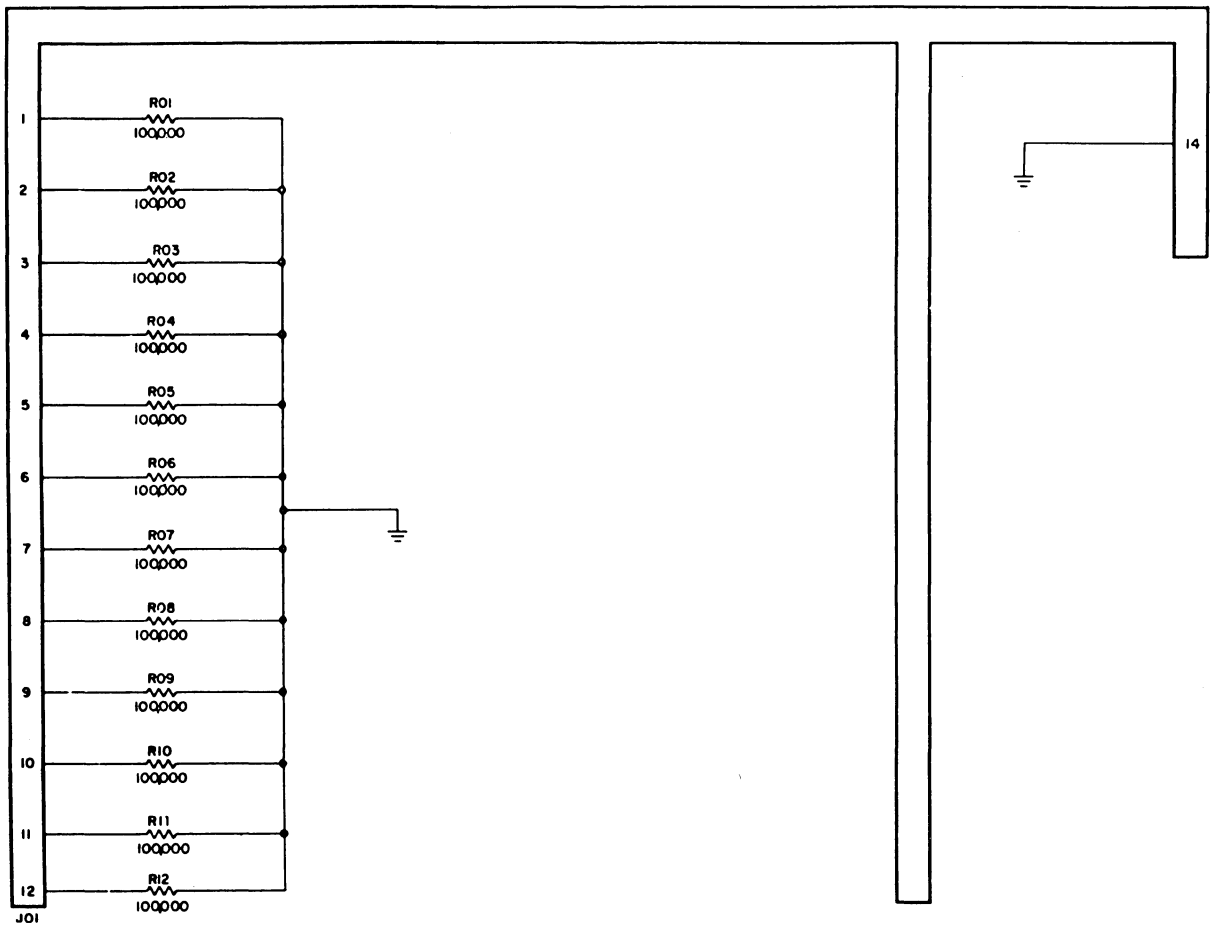


Terminator E19

RESISTOR ASSEMBLY

Card Type E20

Card type E20 contains twelve 100K, 1/2 watt resistors. It is designed to be used in a bleeder network.



Resistor Assembly E20

CONSOLE INTERFACE

Card Type HA10A

FUNCTION

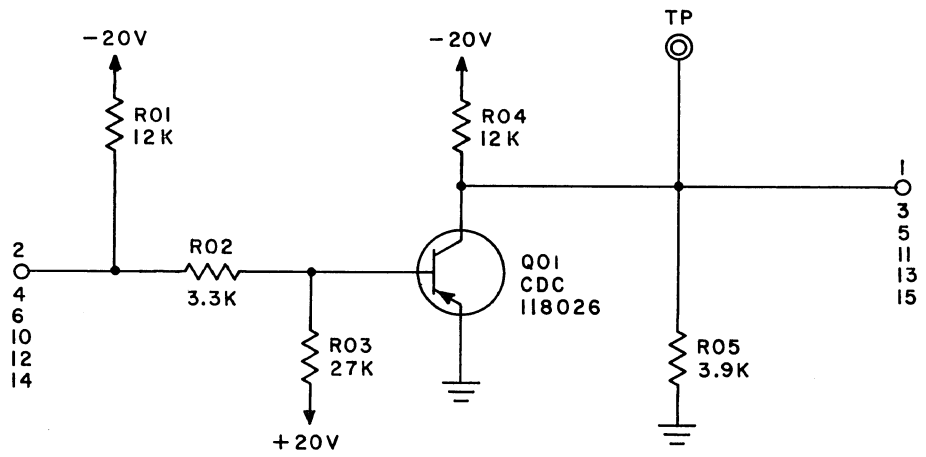
This circuit converts the signals received from either logical inverters or manual switches into outputs suitable for driving a high-current load such as a 5v light. This circuit can also function as a logical inverter since its output voltages are approximately those required for "1's" and "0's".

OPERATION

Transistor Q01 is capable of handling a current of the order of 200 ma. A -5.8 v "1" (or open) input causes Q01 to conduct, while a -1.1 v "0" (or ground) input causes Q01 to cut off.

A -1.1 v "0" or ground input allows the +20 v through resistor R03 to reverse-bias the emitter-base junction of Q01, so that Q01 is cut off. In this state, the test point voltage will be approximately -5.6 v. This is produced by the voltage divider action of R04 and R05.

A -5.8 v "1" or an open input will cause Q01 to switch on and conduct heavily. A negative-going input causes current flow to increase through R02. Initially this current is supplied by the +20 v source through R03, however the voltage drop across R03 is limited by the base-emitter junction drop of Q01. A further increase in current flow will draw turn-on current through Q01, causing it to switch to its conduction state.



NOTE: SIX CIRCUITS PER CARD.

DELAY LINE AMPLIFIER
Card Type HA12

FUNCTION

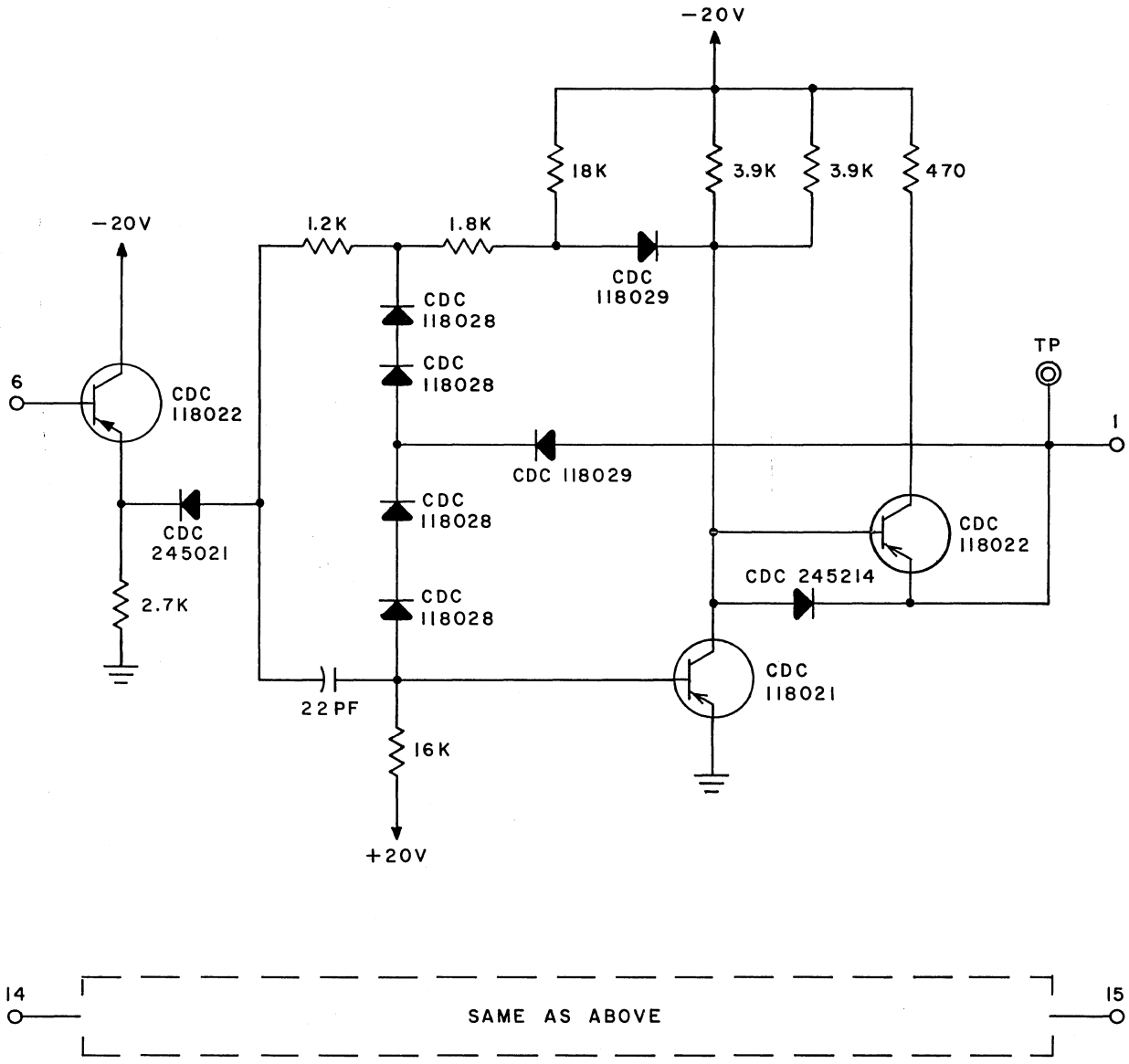
The function of this circuit is to convert inputs received from a terminated, 200-ohm delay line into logic outputs. The circuit provides a high-impedance load for the delay line, avoiding excessive current drain. The circuit output is a -1.1 v "0" which goes to -5.8 v "1" upon receipt of a positive-going pulse from the delay line. It is capable of driving eight loads, and its output characteristics are identical to a logical inverter.

OPERATION

The circuit consists of an emitter follower feeding an inverter through an OR diode. Inputs are received by tapping from the delay line. The quiescent value of the input signal is about -10 v, with pulses going to ground.

The input transistor is an emitter follower current amplifier, which provides a high impedance load with little current drain for the delay line. It is coupled directly into the inverter by means of an OR diode. With a -10 v input, the emitter of the input transistor is held at approximately -9.3 v. This holds the output of the inverter at -1.1 v "0". A positive-going input is effectively the same as a logical "0" and will cause the inverter to have a -5.8 v "1" output.

The inverter portion of the circuit is similar to a logical inverter, which is discussed elsewhere.

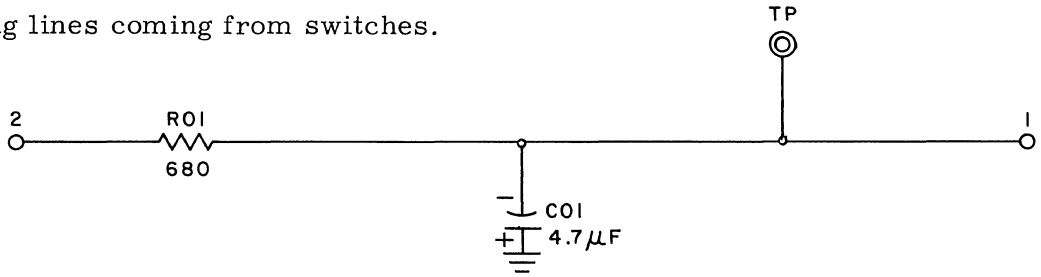


Delay Line Amplifier HA12

FILTER

Card Type HA17

This card contains six identical RC filters, each consisting of a series resistor followed by a capacitor to ground, as shown on the accompanying diagram. It is designed to be used in conjunction with card type HA10 on long lines coming from switches.



NOTE: ALL CIRCUITS IDENTICAL

LIGHT DRIVER

Card Type HA20

FUNCTION

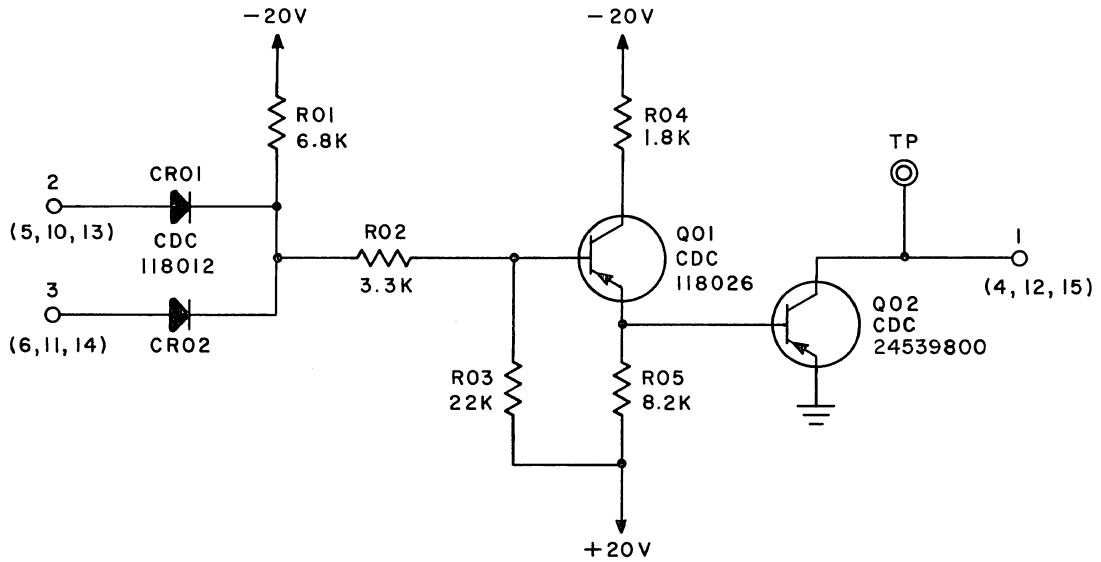
This card contains four identical circuits, the function of which is to provide a low impedance path from ground to the circuit output upon receipt of a -5.8v "1" input. The output transistor can handle a collector current of 500 ma at -18v, and is therefore well suited for driving an indicator light.

OPERATION

Transistor Q01 operates as an emitter follower and Q02 as a grounded emitter amplifier. The input to Q02 therefore follows the input to Q01 and is increased by the gain of Q01.

Each circuit has a 2-way AND input. Open inputs have the same effect as -5.8v "1's". If both inputs are open, the -20v through R01 will switch the transistors to the conduction state.

The base of Q02 is held approximately 0.5v more positive than the base of Q01 by the base-emitter junction drop of Q01. If the circuit inputs are -5.8v "1", the input to Q01 will be approximately -3.4v. This puts a strong forward bias on the base of Q02, enabling it to conduct. A -1.1v "0" circuit input holds the base of Q01 at about +2.7v. This applies a reverse bias of around +3v to Q02 so that it is cut off.



NOTE: 4 CIRCUITS PER CARD

5-HA20-1

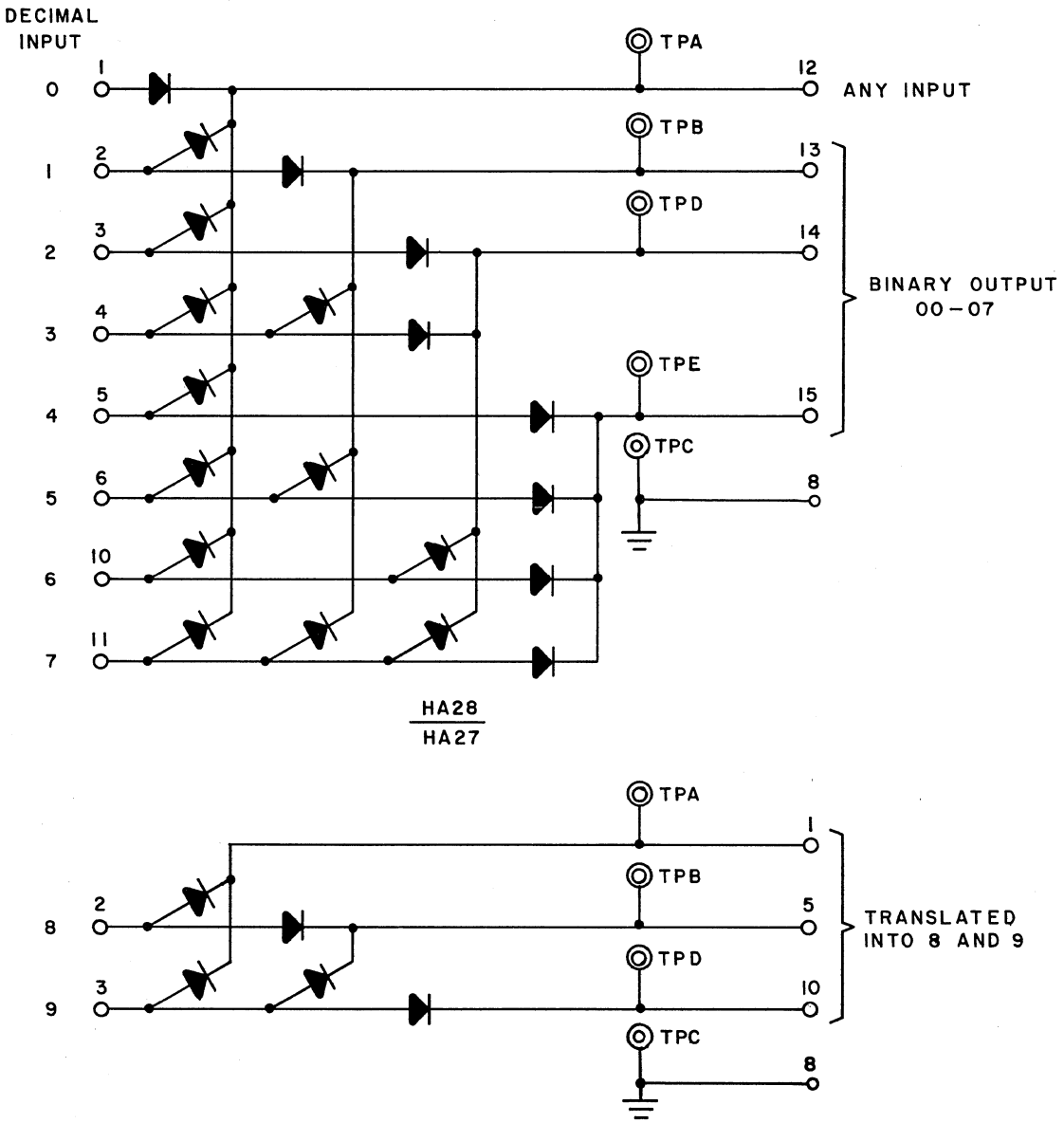
Rev. U

KEYBOARD TRANSLATOR
Card Types HA27 and HA28

The function of these cards is to perform a decimal to binary conversion. Card type HA28 converts the numbers 0 through 7 and HA27 converts 8 and 9.

The circuits consist of AND diodes, and when one of the input pins is grounded, the output pins at which the ground appears will represent a binary number. The input pins are connected to a set of decimal push-buttons on a keyboard. As the buttons are pressed, the diode translator network converts the number to binary.

Note that pin 12 on card type HA28 will be at ground if any input pin is grounded. Similarly, pins 1 and 5 on card type HA27 will indicate a ground at either input.



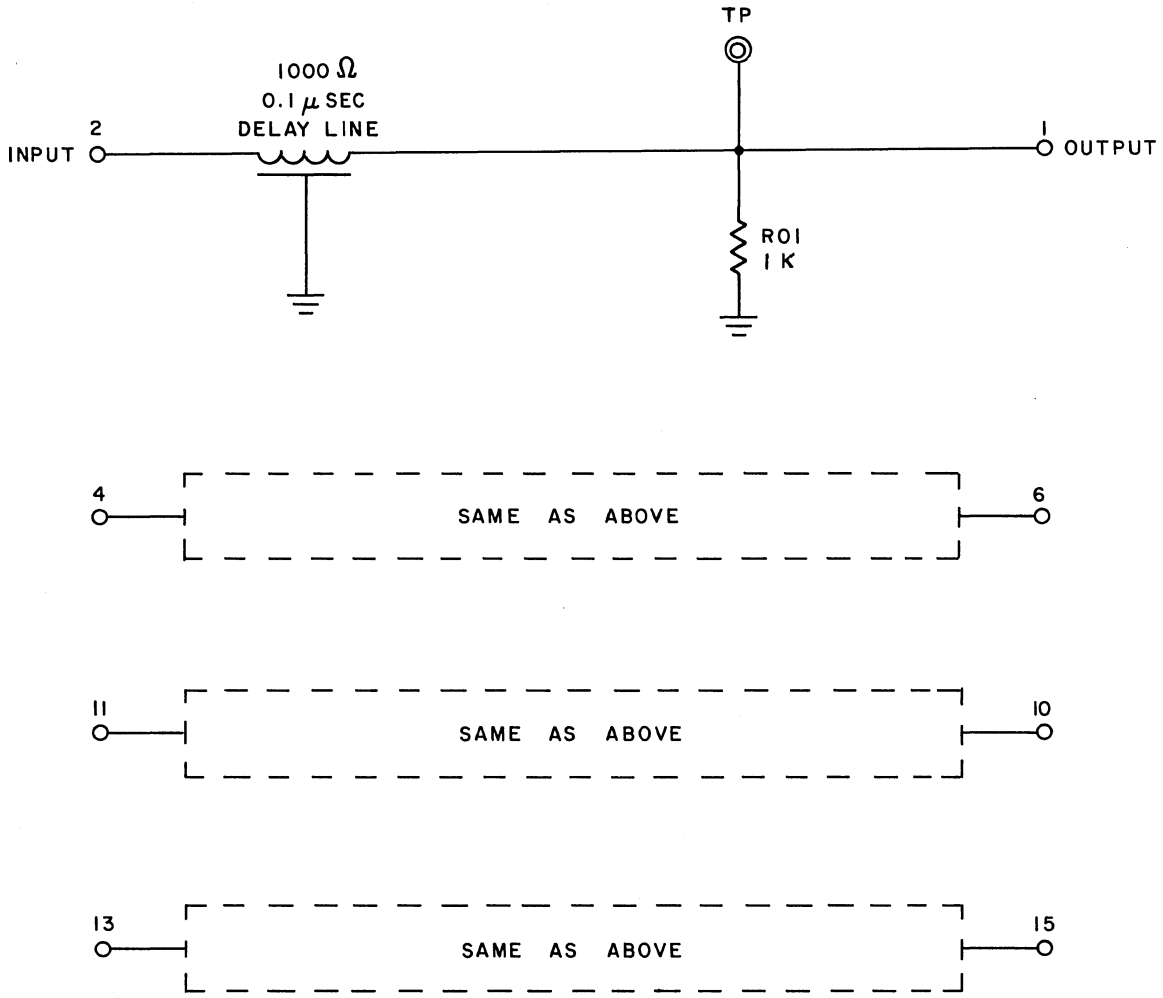
Keyboard Translator HA27 & HA28

DELAY LINE, 0.1 USEC
Card Type HA35

The function of this circuit is to provide an interval of time delay between successive logical operations. It is designed for use in applications requiring greater stability than may be obtained from capacitive delays.

The nominal 0.1 usec delay time applies to both "1's" and "0's", and the delay may be used to drive either an AND or an OR input. Attenuation through the delay line is negligible.

The characteristic impedance of the delay line is 1000 ohms. The purpose of resistor R01 is to provide better impedance matching between the logic circuit input and the delay line output.



NOTE:

1. EACH DELAY MAY DRIVE ONE LOGIC CIRCUIT USING EITHER AN "AND" OR AN "OR" INPUT.

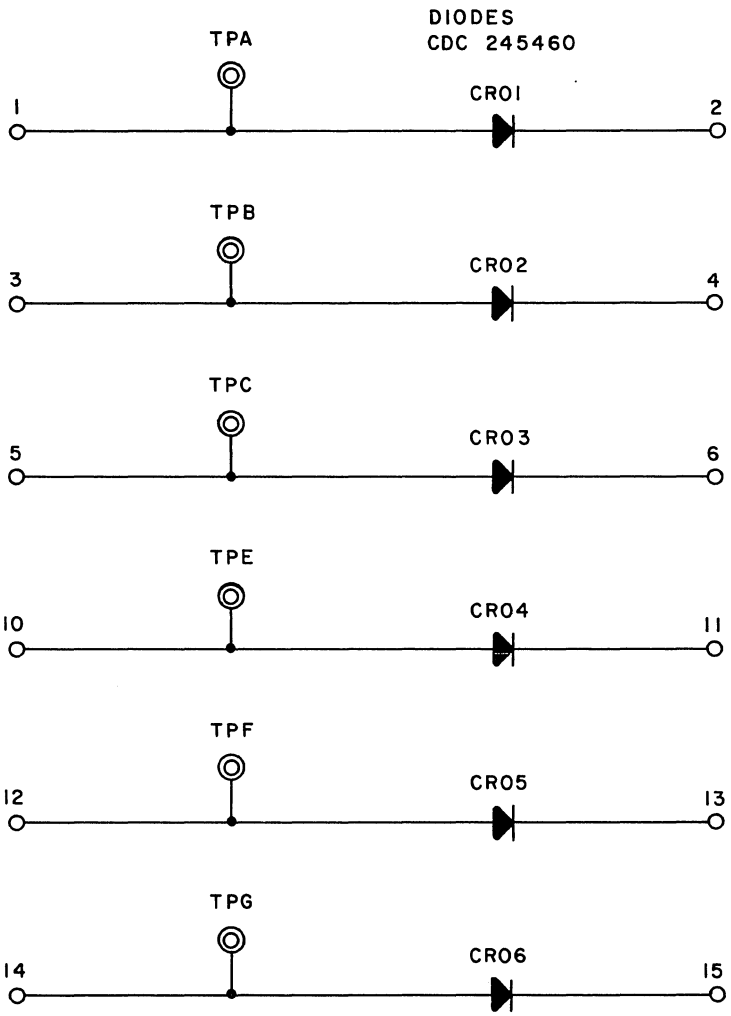
Delay Line, 0.1 usec HA35

DIODE

Card Type HA38

This card contains six diodes, as shown in the accompanying diagram. These diodes are high-current silicon devices, and a summary of their characteristics is as follows:

A. Average rectified forward current, 25°C; 750 ma.
B. Peak forward current; 6 amperes.
C. Peak reverse voltage; 600 volts.



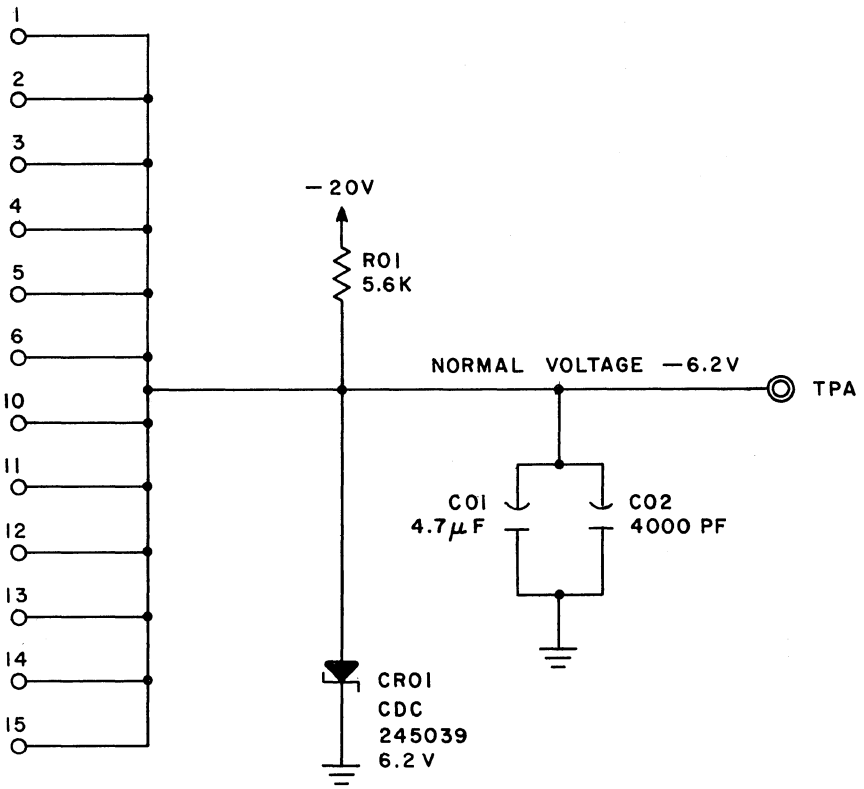
NOTE: DIODES RATED 750 MA.

LINE TERMINATOR

Card Type HA39

This circuit provides a clamp for logic lines, so that ringing is minimized. Any negative-going overshoot will be clamped at approximately -6.2 v. As shown in the accompanying diagram, the clamp voltage is the drop across the 6.2 v zener diode CR01.

Filtering is provided by capacitors C01 and C02. Due to its large area, C01 presents an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitor C02 to filter out high-frequency spikes.



DELAY
(Inductive, 0.15 usec)
Card Type P13A

FUNCTION

The function of this circuit is to provide an interval of time delay between successive inversions in 1604-type logic. It is designed for use in application requiring greater stability than may be obtained with capacitive delays.

The normal 0.15 usec delay time applies to both "1's" and "0's". The delay will drive one load, which may be either an AND or an OR.

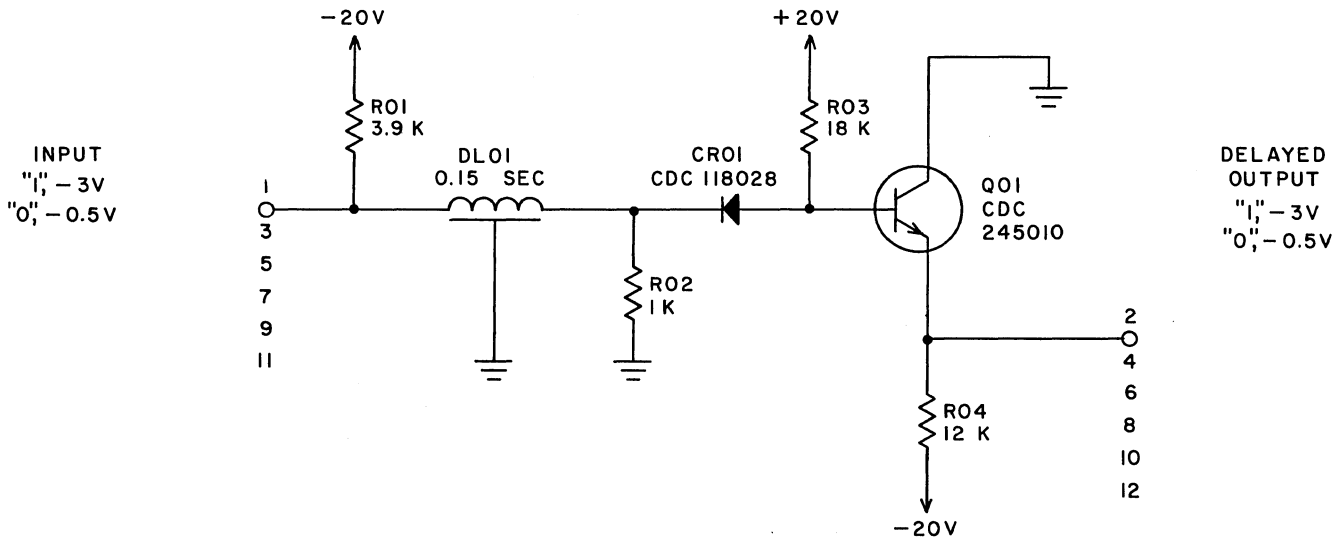
OPERATION

The delaying action is performed by the 0.15 usec inductive delay line DL01. The characteristic impedance of DL01 is about 1000 ohms. Resistor R02 provides impedance matching for the delay line output. Transistor Q01 operates as an emitter-follower current amplifier.

Resistors R02, R03, and diode CR01 perform a level-shifting function between the delay line and the base of Q01. CR01 is a silicon forward-drop diode having a differential of 0.7v between anode and cathode.

A -0.5v "0" input results in about +0.2v at the base of Q01. The output voltage is equal to the base voltage of Q01, less the base-emitter junction drop and is approximately -0.5v.

A -3v "1" input holds the base of Q01 at about -2.3v. However, the base-emitter junction drop of Q01 is approximately equal and opposite to the drop across CR01, so that the circuit output is about -3v.



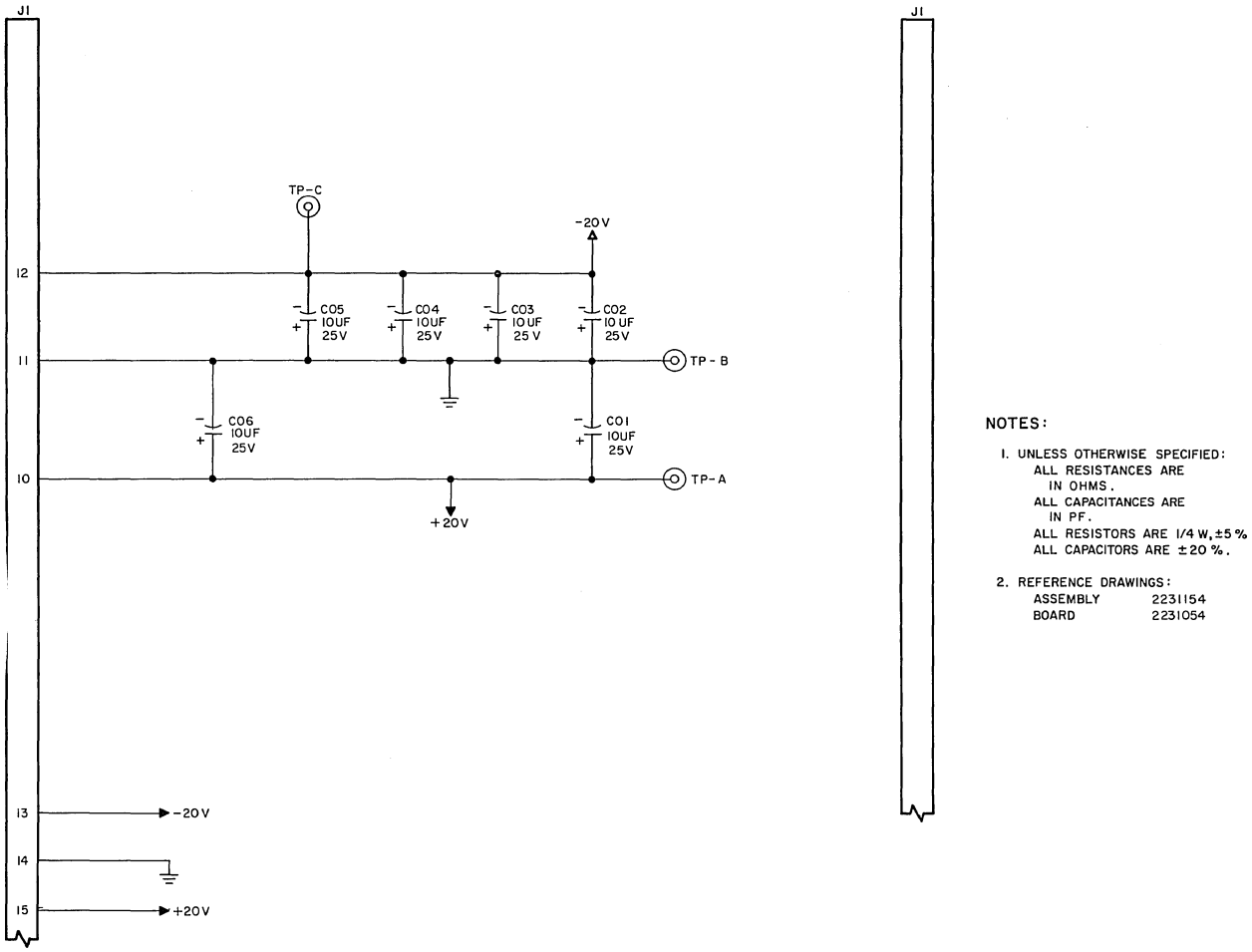
NOTES:

1. 6 CIRCUITS PER CARD.
2. APPROXIMATELY EQUAL DELAY FOR "1" AND "0".

POWER SUPPLY FILTER AND JUMPER
Card Type P54

Card P54 provides multiple connections to -20v, ground, and +20v. Pins 13, 14, and 15 are connected in the usual sequence to -20v, ground, and +20v. So that other connections can be taken from this card, pin 12 is held at -20v, pin 11 is held at ground, and pin 10 is held at +20v.

P54 also contains six filter capacitors rated uf at 25v. Four are connected between -20v and ground and two are connected between +20v and ground, to diminish any ripple in the supply voltage.



NOTES:

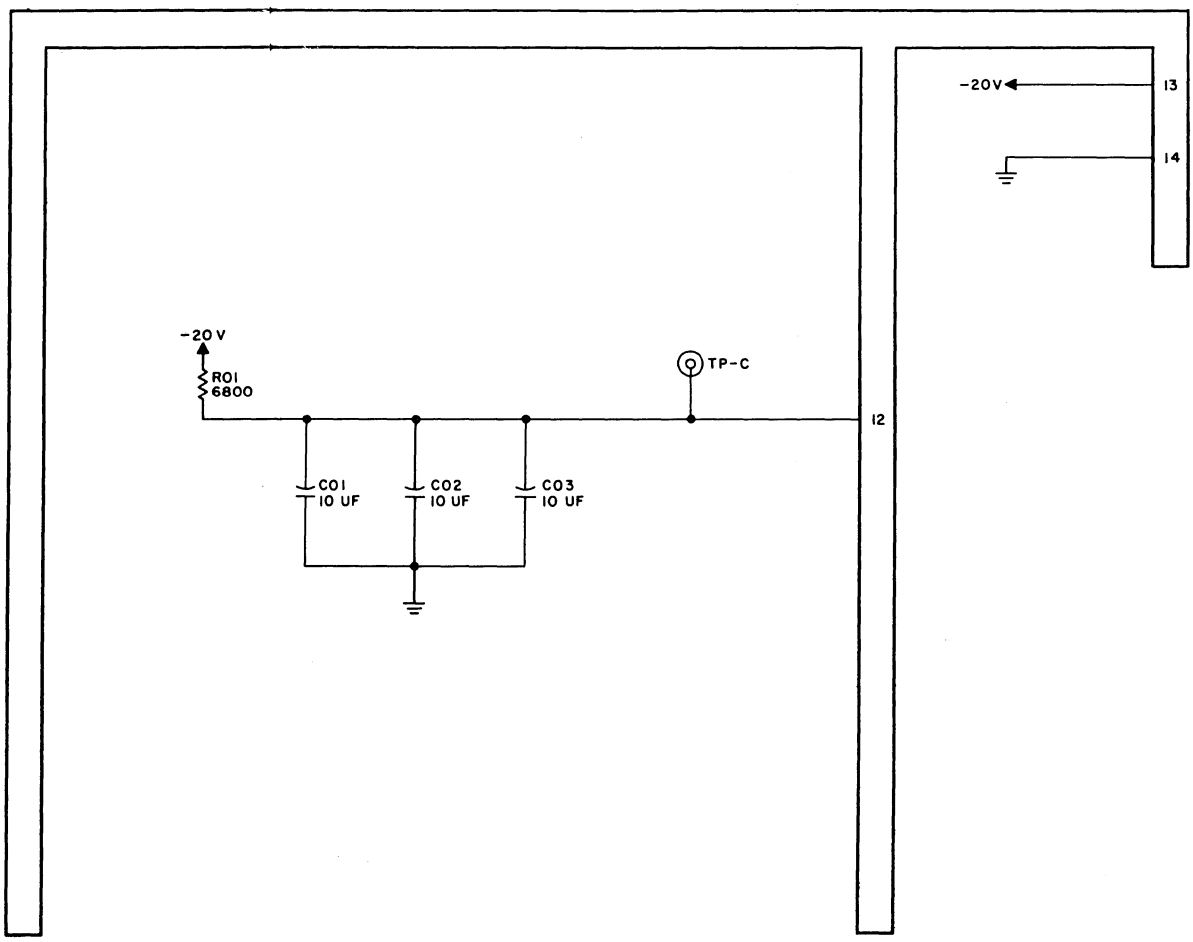
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231154
   BOARD 2231054

Power Supply Filter and Jumper P54

POWER SUPPLY FILTER & JUMPER

Card Type P55

This card contains a total of 30 uf of capacitance to ground, with a source of charging current through a 6800-ohm resistor to -20v, as shown on the accompanying diagram. The circuit may be used in various ways, such is to produce a power-on Master Clear pulse by connecting pin 12 to the input of an M^{---} card. When power is first applied, the uncharged capacitors on the P55 card will cause the M^{---} card to have a "1" output which may be used to drive the Master Clear inputs. When the capacitors obtain sufficient negative charge, the output of the M^{---} card will go to "0".



Power Supply Filter & Jumper P55

HAMMER DRIVER
Card Types P91 and P92

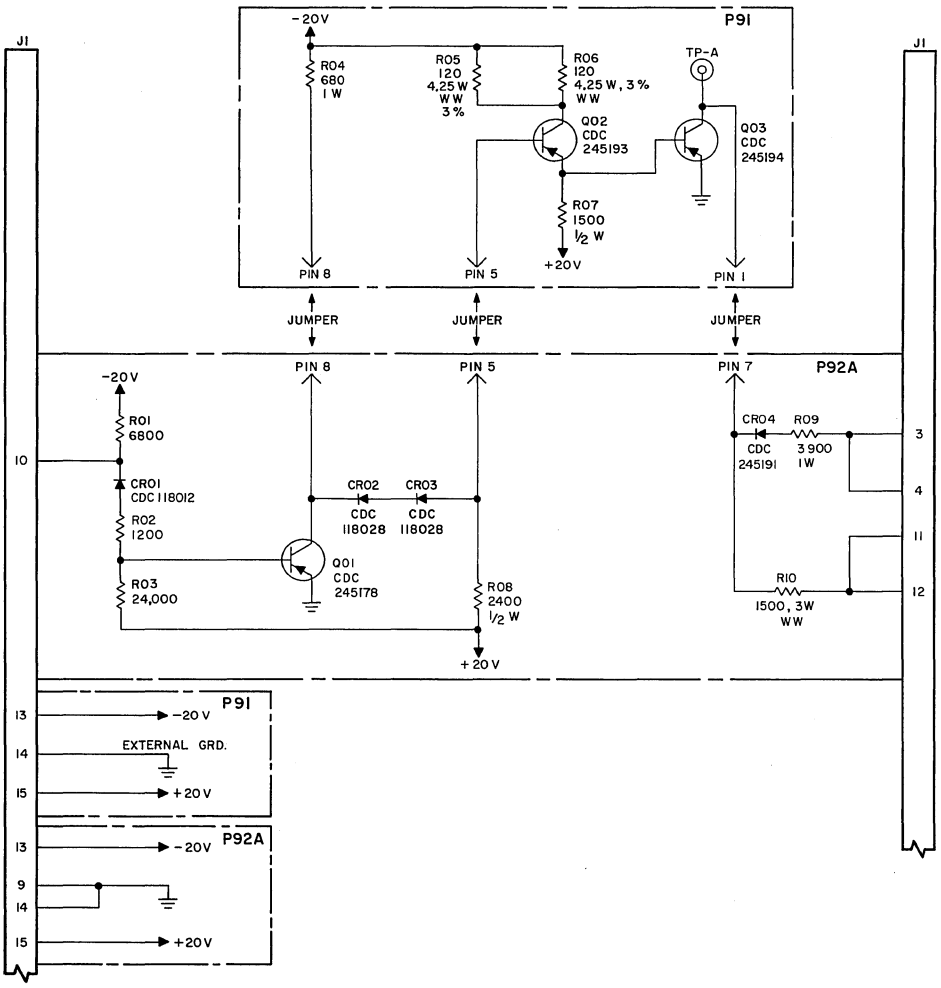
(Normal Test Point Voltages: -36v, or ground)
Card types P91 - P92 share circuitry. The 30-pin connector into which they are inserted is wired so the complete circuit is as shown.

The circuit is designed to switch a current of 7 amp from a -36v source. It is used as a hammer driver in which it provides 1.3 ms pulses to the hammer solenoids, and in the paper feed circuit, where it provides 4 ms starting pulses to the clutch and brake coils.

The circuit receives logic inputs from One-Shot card P95 or P97. These cards provide logical "0" input pulses of 4 ms and 1.3 ms.

Upon receipt of a "0" input (-0.5v), the base of Q01 is at a positive potential and it is cut off. The base of Q02 is biased somewhat negative and conducts. Transistor Q03 also conducts being connected to Q02 as an emitter follower, and the circuit is completed from pins 11 and 12 to ground. Upon receipt of a logical "1" (-3v) this circuit is cut off.

Provision is made to handle the high-voltage transient induced in the inductive coil when Q03 is cut off, by use of the diode CR04 and the connection at pins 3 and 4. A series circuit is provided through the diode with the coil as a source of EMF, so that the transient is dissipated harmlessly.



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   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 2231191, 2231192
   BOARD 2231091, 2231092
   FINAL ASSEMBLY 2231402

Hammer Driver P91 and P92

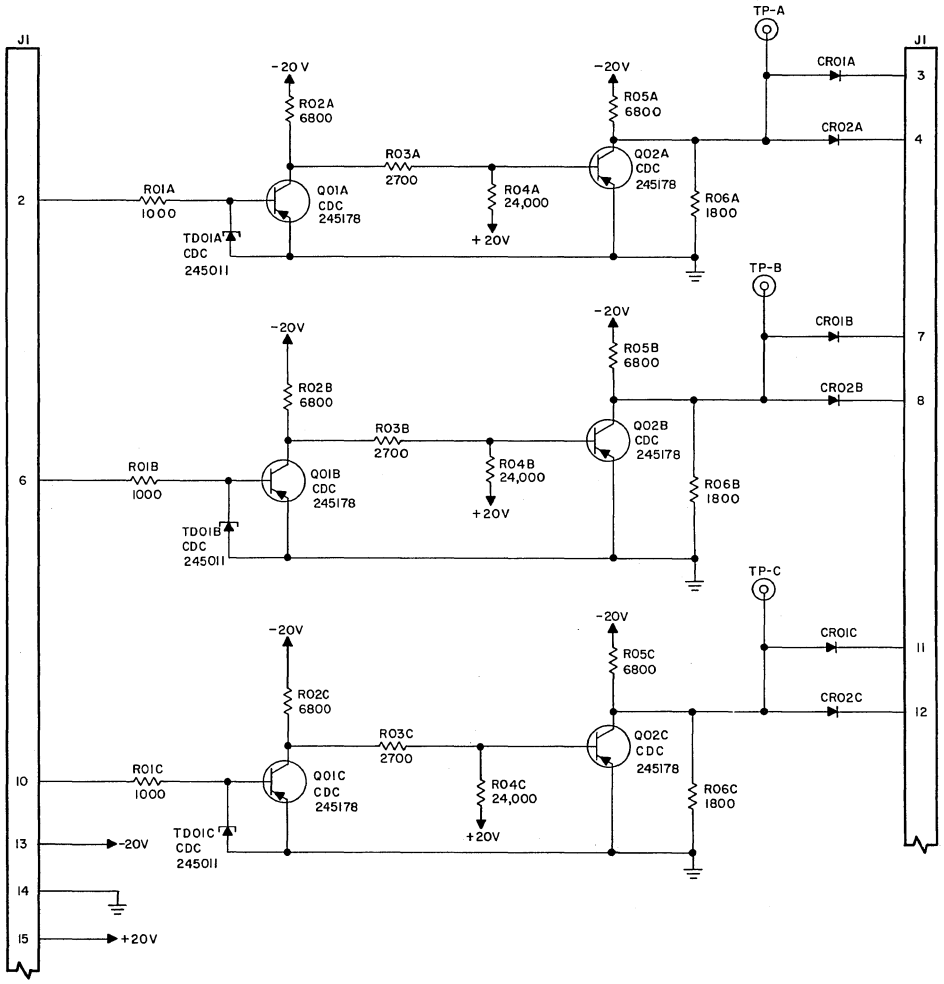
PULSE SHAPER
Card Type P93

(Normal Test Point Voltage: -4v, or ground)
Card type P93 contains three identical circuits, the function of which is to convert the irregular character, index, and paper strobe pulses into square wave, logic level outputs. Thus, a negative pulse is converted to a logical "1" (-3v), and a positive pulse is converted to a logical "0" (-0.5v).

A threshold level of discrimination is provided by the tunnel diode connected between base and emitter of transistor Q01 on each of the circuits. The tunnel diode exhibits two stable states. The voltage across it is quite low or relatively high, and it switches from one state to the other almost instantaneously.

As an example of card operation, assume that one of the circuits is receiving a positive-going input. This cuts off Q01. The base of Q02 is biased negative, and it conducts providing a steady -0.5v "0" output during the time that the circuit receives a positive input.

A low negative voltage also results in a zero output, if tunnel diode current is not sufficient to make it switch to its high voltage state. As the input signal approaches -2.7v, so that tunnel diode current is approximately 1 ma, the tunnel diode switches to its high voltage state and Q01 conducts. This causes Q02 to be cut off, so that the circuit output is held at -3v.



NOTES:

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   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 2231193
   BOARD 2231093

3. UNLESS OTHERWISE SPECIFIED
   ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED

Pulse Shaper P93

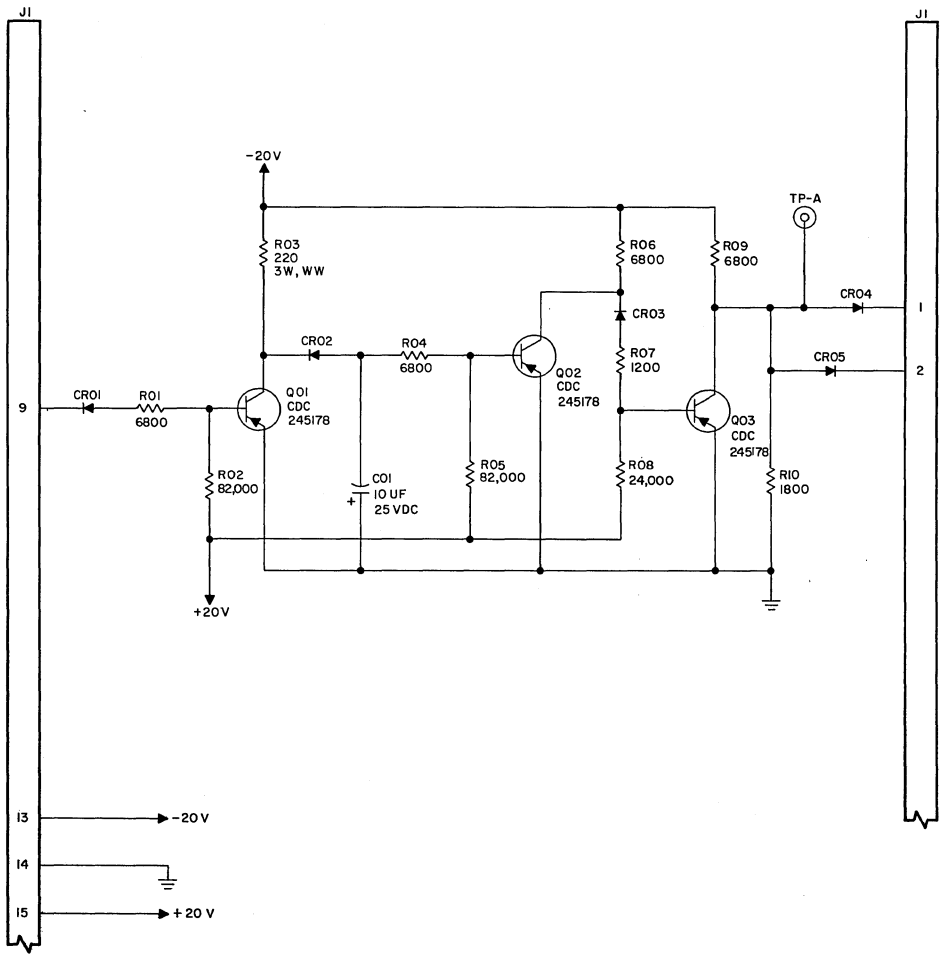
RIBBON ADVANCE
Card Type P94

(Normal Test Point Voltage: -4v, or ground)
P94 enables the ribbon motion to continue for approximately 250 ms after paper motion has stopped. Inputs are received from pin 2 of the P96 card in the paper clutch circuit. The input levels are -0.5v and -36v, and the corresponding card outputs are -3v and -0.5v. Upon receipt of the -36v input, the -3v "1" output continues for approximately 250 ms before switching to the -0.5v "0" level.

As an example of card operation, assume that a -0.5v "0" input signal is being received on pin 9. The base of Q01 is at a positive voltage and is cut off. The base of Q02 is at a negative potential and conducts cutting off Q03, so that the output is a -3v "1". During the time that Q01 is cut off, the anode of CR02 is at approximately -15v, so that capacitor C01 obtains a negative charge.

A -36v signal causes Q01 to conduct; its collector goes to approximately ground potential. CR02 forces the charge on C01 to decay through R04 and R05. Q02 remains in its previous conduction state and the -3v output continues. When the negative charge on C01 has decayed sufficiently, Q02 is cut off. A negative potential then appears on the base of Q03, causing it to conduct, and the card output drops to -0.5v, which is a logical "0".

The time during which the charge on C01 causes Q02 to remain in its conducting state is not critical; it is designed to be approximately 250 ms.



NOTES:

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   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231194
   BOARD 2231094
3. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012, POLARIZED

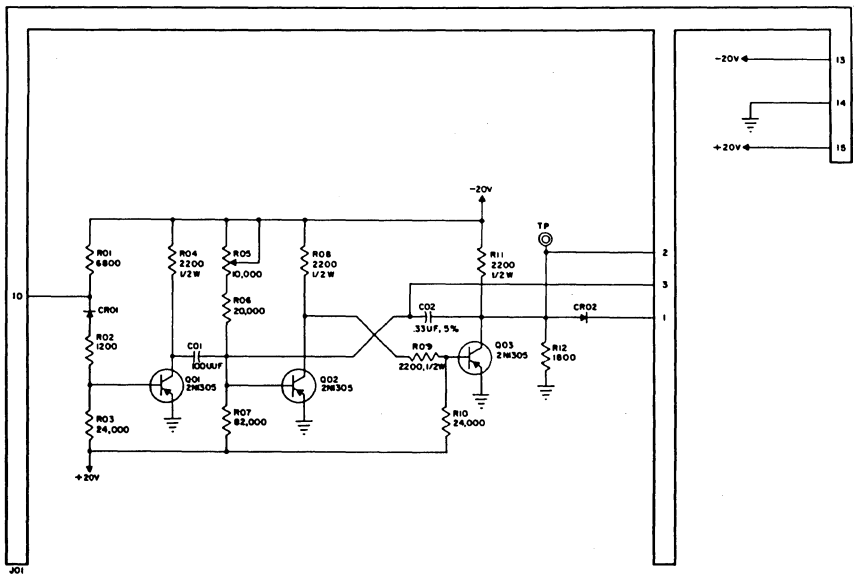
Ribbon Advance P94

BRAKE-CLUTCH ONE-SHOT
Card Types P95 and P99

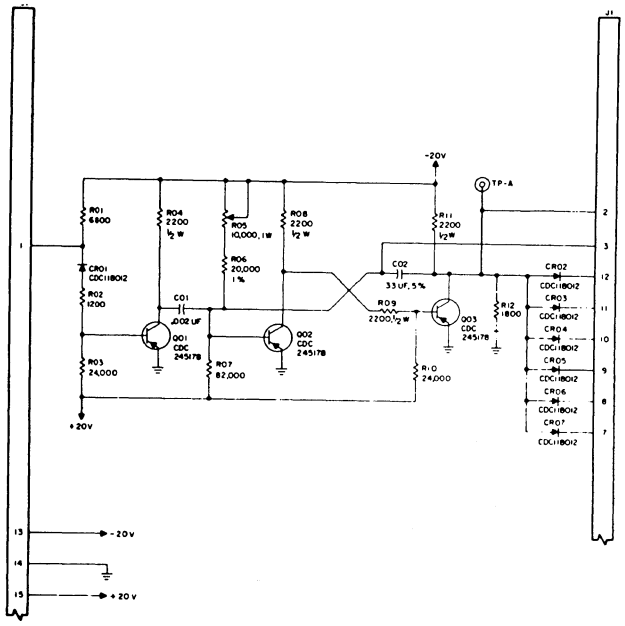
(Normal test point voltages: -9v, or ground)
These cards provide -0.5v "0" pulses of exactly 4 ms duration to the paper feed brake and clutch circuitry. For the major portion of its duty cycle, the card receives a "0" input and provides a steady "1" output. Upon receipt of a "1" input, the card output switches to "0" where it remains for 4 ms and then returns to a steady "1".

Assume that a "0" input is being received on pin 10. This puts a positive potential on the base of Q01 so that it is cut off. Due to the voltage-dividing action of R05, R06, and R07, the base of Q02 is at a negative potential and conducts. Q03 is therefore cut off, and the card output is a steady "1". The potential across capacitor C02 is approximately zero and the capacitor is uncharged.

A "1" signal causes Q01 to conduct; Q02 is cut off, and Q03 conducts. The card output goes to "0". The potential across C02 is no longer zero; it obtains a charge at a rate determined by the setting of R05. Thus, after a time of 4 ms, C02 has obtained a sufficiently negative charge so that Q02 conducts, Q03 is cut off, and the card output returns to a steady "1".



Brake-Clutch One-Shot P95



Brake-Clutch One-Shot P99

RIBBON DRIVE AND HOLD

Card Type P96

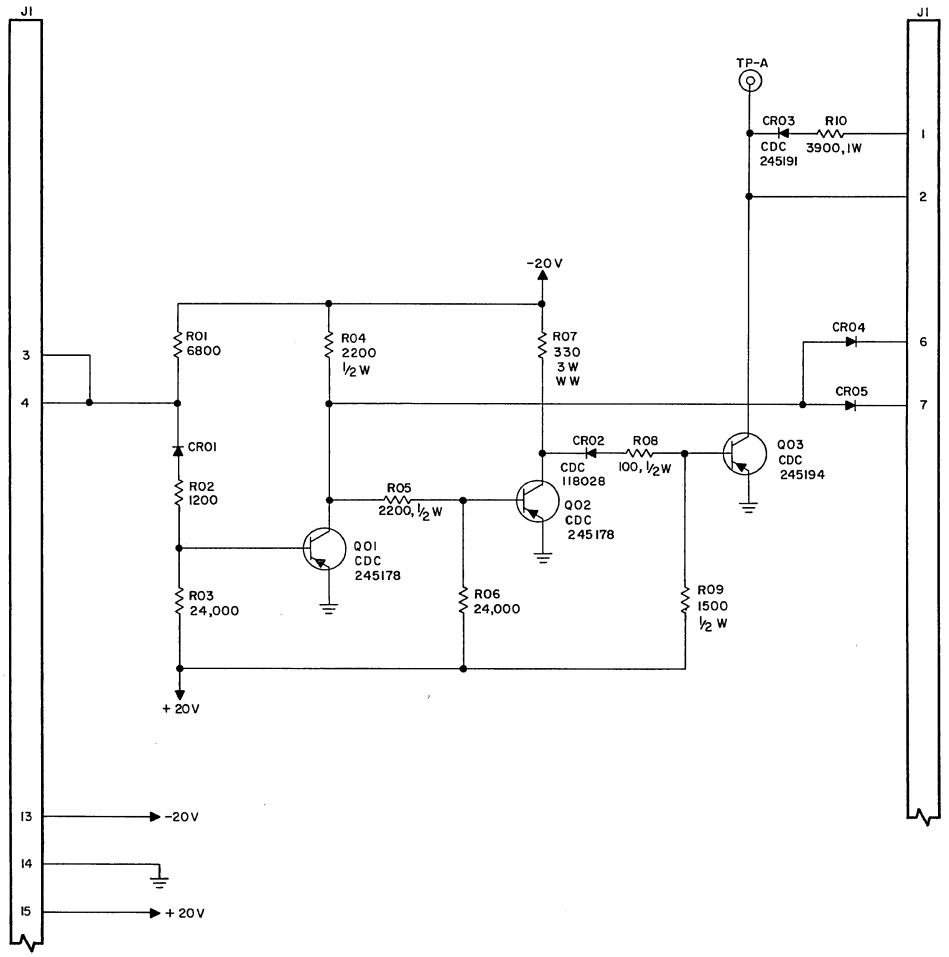
(Normal Test Point Voltages: -36v, or ground)
Card type P96 functions: as a logical inverter, in providing interlock signals to paper and ribbon feed circuitry; and as a switch, controlling the 200 ma ribbon drive current and the hold current of the paper clutch and brake.

The card receives logic inputs on pins 3 and 4. A logical "1" (-3v) input results in a logical "0" (-0.5v) output from pins 6 and 7, and enables Q03 so that 200 ma of negative current flows from pin 2 to ground. Upon receipt of a logical "0" input, the output from pins 6 and 7 changes to a "1" and the circuit from pin 2 to ground is opened.

As an example of card operation, assume that a -3v "1" signal is received on pins 3 and 4. This results in a potential of about -1v on the base of Q01, so that it conducts. The collector of Q01 therefore goes to approximately ground potential, placing a logical "0" signal on pins 6 and 7, and placing a positive voltage on the base of Q02. Thus Q02 is cut off, which places a negative voltage on the base of Q03 and causes it to conduct, closing the circuit from pin 2 to ground.

Similarly, upon receipt of a "0" input signal, Q01 is cut off and a "1" appears on pins 6 and 7. Q02 conducts, cutting off Q03, so that the circuit is broken from pin 2 to ground.

The connection at pin 1 and the diode CR03 provide a means of dissipating the high-voltage transient induced when the 200 ma of current flowing through the inductive coil is switched off. A connection is made at pin 1, producing a series circuit with the coil as the source of EMF. This prevents the inductive transient from damaging Q03 when the transistor is cut off.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231196
   BOARD 2231096
3. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED

Ribbon Drive and Hold P96

HAMMER DRIVER ONE-SHOT
Card Type P97

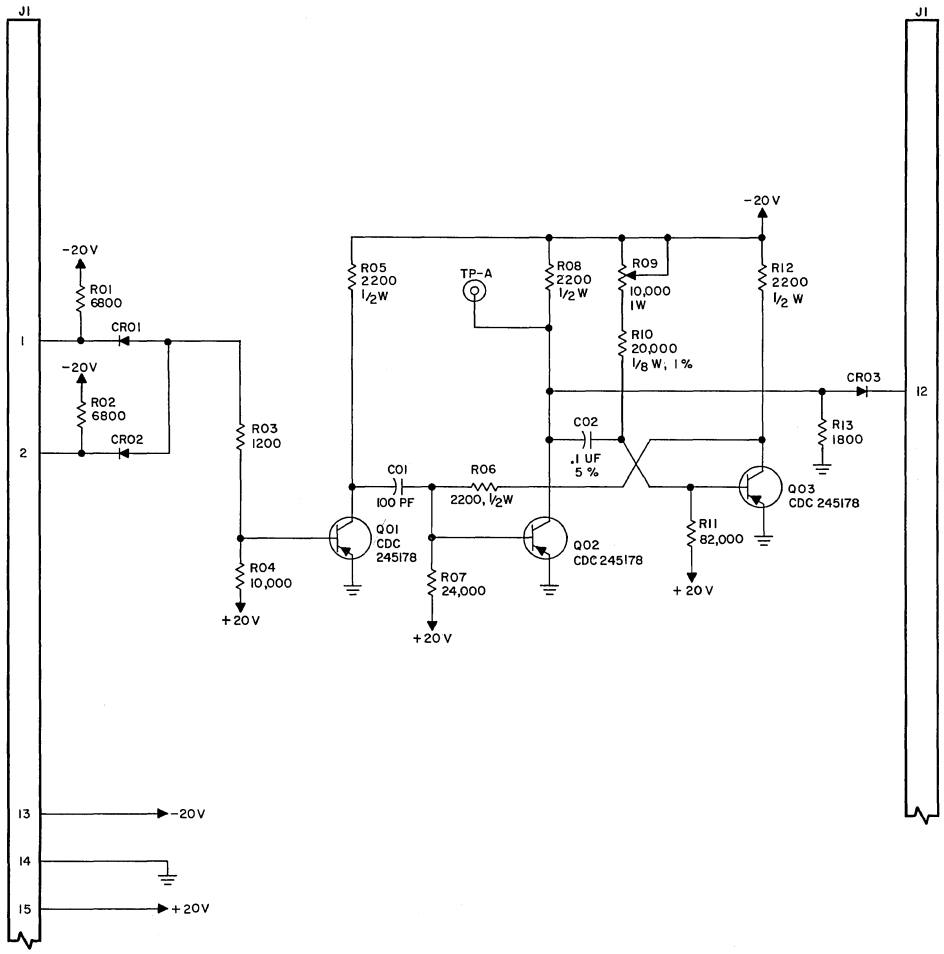
(Normal Test Point Voltage: -9v, or ground)
Card type P97 provides a 0.5v "0" pulse of 1.3 ms duration to a print hammer driving circuit, upon receipt of a "0" pulse. This "0" input is received from a sense amplifying circuit, and is caused by a memory core switching during the read operation.

During the major portion of its duty cycle, this card produces a steady "1" output. A "0" input switches the output to "0" where it remains for 1.3 ms, and then automatically returns to a steady "1".

There are two OR inputs to the circuit used to gate the action, since both of these inputs must simultaneously be at -0.5v ("0") for the circuit to produce a "0" output pulse. If either input is at -3v ("1"), a "0" on the other input is not sensed, and the circuit produces a steady "1" output.

As an example of card operation, assume that a "1" input is being received. Thus, transistor Q01 has a base potential sufficiently negative for conduction, while Q02 has a positive base voltage and is cut off. This biases CR04 in the reverse direction, so that the output is sensed as a logical "1", and also applies a negative voltage to the base of Q03 causing it to conduct. Since Q02 is not conducting and the base of Q03 is at a small negative voltage during this time, there is a potential difference across C02 and it obtains a charge.

If the circuit receives a "0" input, Q01 is cut off and Q02 conducts, providing a "0" output signal and cutting off Q03. The potential of approximately -8v across C02 discharges at a rate set by R12 and R13. The value of R12 is adjusted so that, after 1.3 ms, C02 has gained a sufficient negative charge to cause Q03 to conduct. This places a positive voltage on the base of Q02, cutting it off, and the circuit output returns to a steady "1".



NOTES:

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   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231197
   BOARD 2231097
3. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED +

Hammer Driver One-Shot P97

COMMENT SHEET

MANUAL TITLE CDC Printed Circuit Manual Volume 1

PUBLICATION NO. 60042900 REVISION W

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