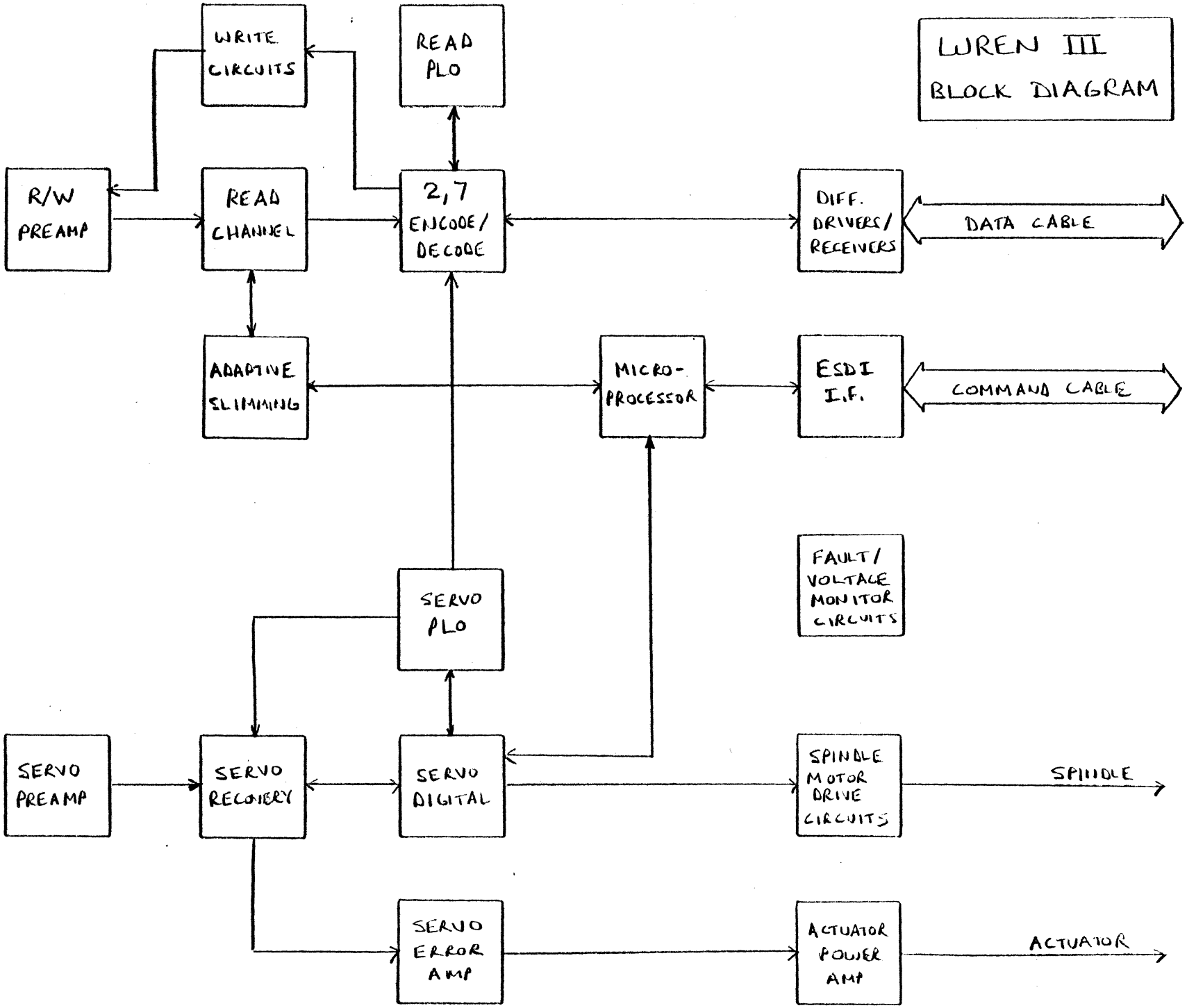

WREN III
BLOCK DIAGRAM
WRITE CIRCUITS
READ PLO
R/W PREAMP
READ CHANNEL
2,7 ENCODE/ DECODE
DIFF. DRIVERS/ RECEIVERS
DATA CABLE
ADAPTIVE SLIMMING
MICRO-PROCESSOR
ESDI I.F.
COMMAND CABLE
FAULT/ VOLTAGE MONITOR CIRCUITS
SERVO PLO
SERVO PREAMP
SERVO RECOVERY
SERVO DIGITAL
SPINDLE MOTOR DRIVE CIRCUITS
SPINDLE
SERVO ERROR AMP
ACTUATOR POWER AMP
ACTUATOR

WREN III ELECTRICAL CONCEPTS

ADDRESSING PREVIOUS AREAS OF CONCERN

- ACCESS TIME
  - NEW ACTUATOR MAGNETICS DESIGN
  - NEW SERVO CIRCUITS ALLOW HIGHER MAXIMUM VELOCITY
- SERVO DEFECT SENSITIVITY
  - NEW TRI-PHASE SERVO RECOVERY USES TRUE SAMPLE AND HOLD CIRCUITS.
  - SELF SYNCHING
  - TRACK CROSSING AND SAMPLE SWITCHING DETERMINED DIFFERENTIALLY.
  - HIGHER SAMPLE RATE REDUCES NOISE. WIDER HEADS GIVE MORE OUTPUT.
- SERVO-WRITER SENSITIVITY
  - RTZ WRITING REDUCES PHASE-COHERENCE SENSITIVITY
- HEAD/MEDIA PARAMETER SENSITIVITY
  - ADAPTIVE SLIMMING AUTOMATICALLY ADAPTS R/W CIRCUITS TO VARYING PARAMETERS.
- FIRMWARE CHANGES
  - EXTERNAL MEMORY DESIGN ALLOWS FLEXIBILITY OF EPROM AND MASK ROM.
  - 4K MEMORY SPACE WITH 8051 MICROPROCESSOR
- CIRCUIT STABILITY
  - ALL KNOWN FIXES FOR WREN I/WREN II CIRCUIT STABILITY PROBLEMS ARE INCORPORATED IN INITIAL LAYOUTS.
- ESDI TESTABILITY
  - NUMBER OF INTERFACE OPTIONS ON WREN II HAS BEEN REDUCED FOR EASIER MANUFACTURING TEST.
  - DRIVE DIAGNOSTIC STATUS AVAILABLE
- WATCH DOG TIMER
  - WATCH DOG TIMER INCORPORATED IN LSI. NO EXTERNAL CAPACITORS.

WREN-III SERVO ERROR BUDGET GOALS

THERMAL (10° TO 60°C)		MICROINCHES
1. SPINDLE TILT	=	20
2. ACTUATOR TILT	=	30
3. SERVO DISK SHIFT	=	30
4. R/W FLEX BIAS	=	10
5. HEAD SCATTER	=	60
6. CIRCUITS	=	20

OTHERS

7. NON-REPETITIVE SPINDLE RUNOUT	=	20	
8. HEAD GIMBAL HYSTERESIS	=	10	
TOTAL SHIFT	=	200	
8. VELOCITY NOISE	=	25	
10. SERVO LOOP SETTLING	=	50	
11. WRITE CURRENT NOISE	=	10	
12. BEARING FRICTION	=	8	
13. ACTUATOR UNBALANCE	=	2	
14. BASEPLATE VIBRATION	=	30	
15. SPINDLE VIBRATION	=	20	
16. ROTARY ARM VIBRATION	=	25	
17. STW VIBRATION	=	30	
RMS OF 9 TO 17	=	78	MICROINCHES
TOTAL PEAK TO PEAK OFFSET	=	278	MICROINCHES
TRACK TO TRACK SPACING (1/TPI)	=	1041	MICROINCHES
% OFF-TRACK ERROR PP	=	26.7	

DCP

2/13/85

ADVANTAGES OF WREN III
TRI-PHASE SERVO PATTERN

- SERVO TRACK WRITING TIME REDUCED NEARLY 50% DUE TO ONLY ONE SERVO TRACK PER DATA TRACK.

- SAMPLE RATE 214% HIGHER THAN WREN II.

- SERVO SIGNAL AMPLITUDE IS 43% HIGHER DUE TO WIDER SERVO HEAD.

- MORE DATA TRACK AREA BECAUSE A DEDICATED SYNC ZONE IS NOT REQUIRED.

- VARIOUS CODES CAN DEFINE SPECIAL FUNCTIONS SUCH AS INDEX, TRACK 0, ETC.

- A SPIRAL DC ERASE CAN BE DONE BEFORE SERVO TRACK WRITING DURING A BURNISH CYCLE.

- IMPROVED LINEAR SERVO DATA RANGE.

- MORE UNLIKELY TO FALL OFF CYLINDER BECAUSE A LESS TIME CRITICAL SELF SYNC PATTERN ALLOWS RECOVERY FROM FAULTY SYNC BITS WITHOUT EXCESSIVE OFF-TRACK ERROR AND FAST RECOVERY FROM BAD SERVO DATA.

1/18/85

ADVANTAGES OF WREN III
TRI-PHASE SERVO PATTERN

- BETTER TRACK CROSSING DETECTION BY USING HIGHER SAMPLING RATE AND DIFFERENCE COMPARISON OF ERROR SIGNALS.

- REDUCED AMPLITUDE MODULATION BY USE OF ERROR PATTERN SIGNALS FOR AGC INSTEAD OF MISALIGNED SYNC BITS.

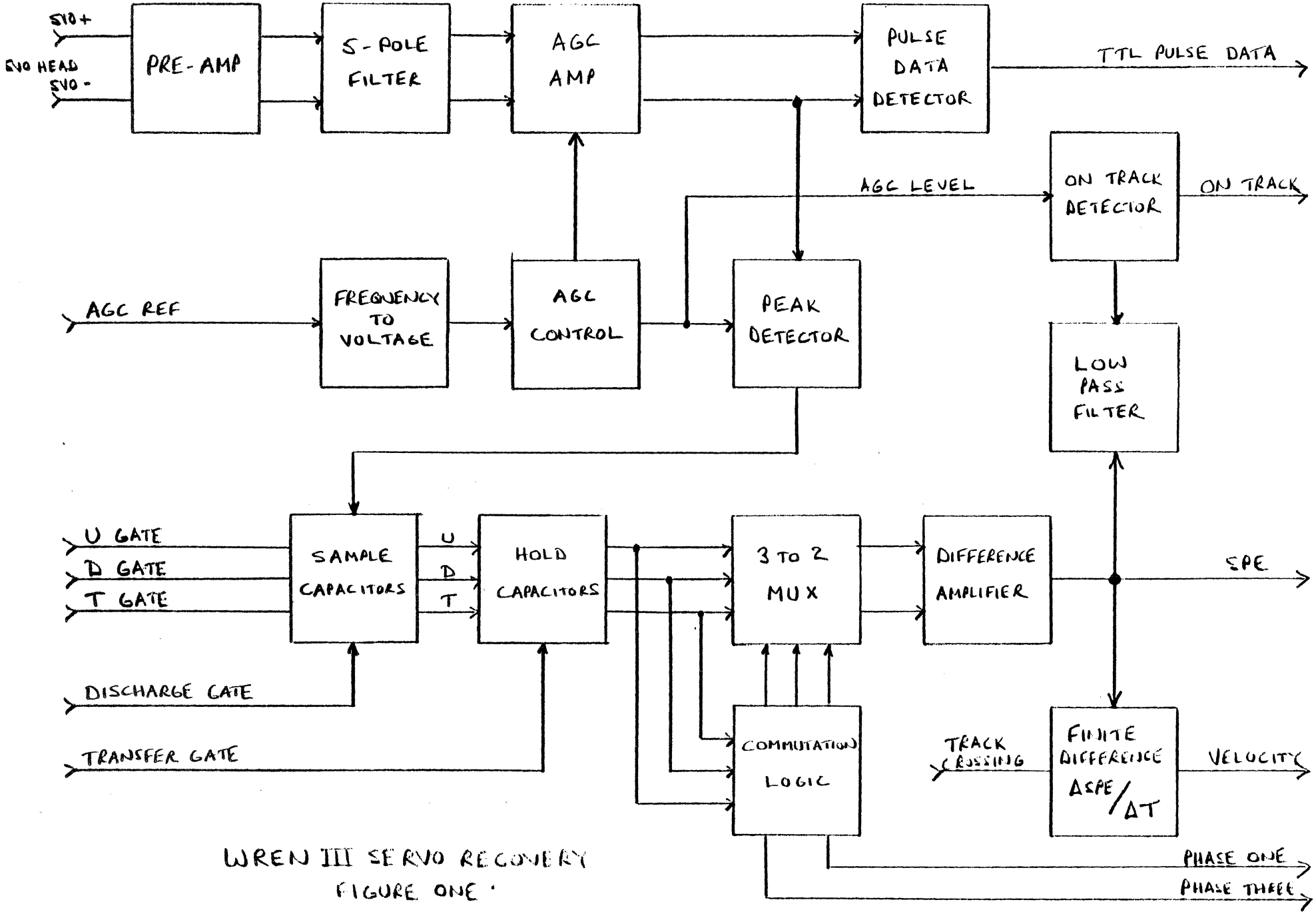
SERVO RECOVERY THEORY

In the following discussion please refer to the block diagram in figure one. The first stage amplifies the signal 300 to 500 times. This increases the level from the microvolt range into millivolt range. The signal is next filtered by a five pole filter with a roll-off at about 10 MHZ. The filter is followed by a automatic gain control stage (AGC). The output of the AGC will be a fixed level of about one volt peak.

At this point we have finished conditioning the signal and are now ready to begin to process the signal's information. The first information we will extract is the timing of the dibits and the presence or absence of the code dibit. The timing will be used to lock a phase locked loop (PLL) which will be used to create qualifying gates. The code dibit is used to encode index, track zero, etc. This is done by the pulse data detector (see figure one). The pulse data detector is a fast comparator with hysteresis. The comparators output goes high when the signal goes below the negative threshold and low when the signal becomes positive. This output is buffered by a TTL buffer and sent to the servo LSI.

The actual position information is extracted by the peak detector and the sample capacitors. There are three sample capacitors and three analog switches. Each capacitor is switched in when the dibit it is sampling is present. When all three sample capacitors have been charged, three additional switches are closed and the three hold capacitors are charged to that level. The sample capacitors are then discharged so that they are ready for the next frame. The control signals are supplied by the servo LSI. The hold capacitors allow the sample capacitors to be discharged each frame and therefore no frame can effect any other frame. This minimizes the effect of bad data. They also allow all position information to be in phase.

At this point we have the amplitude of the three dibits and we would like to take the differance of two of them for our servo position error (SPE). The commutation logic takes a look at the amplitude of the dibits and determines which two should be used. The amplitude of one dibit as the head crosses tracks is shown in figure two. The amplitude pattern for the other two is the same but they are one third track out of phase. In figure three all three dibits are shown, you will note that there are six points where two of the dibit are equal. These are the three track centers and the track boundaries. The lower three waveforms in figure four show the results of comparing three sets of two dibits. The upper waveforms are the result of a logical "and" of one of the lower waveforms and the inverse of one of the lower waveforms. The net result is three non-overlapping signals that define the three track types or phases. Two of these phases are buffered sent and to the servo LSI which uses them to generate a pulse at each track crossing.



WREN III SERVO RECOVERY
FIGURE ONE

The phases are now used to control six analog switches which select two of the three dibits for the differance amplifier. At this point we have the SPE signal available at the output of an op-amp. Note that SPE is not switched. This is because the input is switched. The microprocessor does not have to keep track of which track the drive is on; as a matter of fact, this circuit can tell it which track it's on (to within three).

The velocity is generated from the rate of change of SPE. This is done by subtracting the SPE value in the last frame from the present value. By adding the right amount of gain a correctly scaled velocity signal is obtained, with one small problem. When the SPE is switched it starts track position over, going from a large voltage to a small voltage or the reverse. This causes a discontinuity which would cause an error in the velocity. To prevent this from happening the track crossing signal ,generated by the servo LSI, is used to hold the velocity for a short time.

The peak detector has a second output (AGC level) which represents the level of a full amplitude dibit. The on track detector compares filtered SPE to the AGC level and sets the "on track" signal when the drive is within five percent of track center. The AGC level is also used to close the AGC loop. The microprocess outputs a PWM signal called "AGC REF" and the AGC control circuit compares this with the AGC level to set the gain of the AGC amplifier. Changing the "AGC REF" level changes the overall system gain, and is used to accomplish the "auto velocity adjust" function.

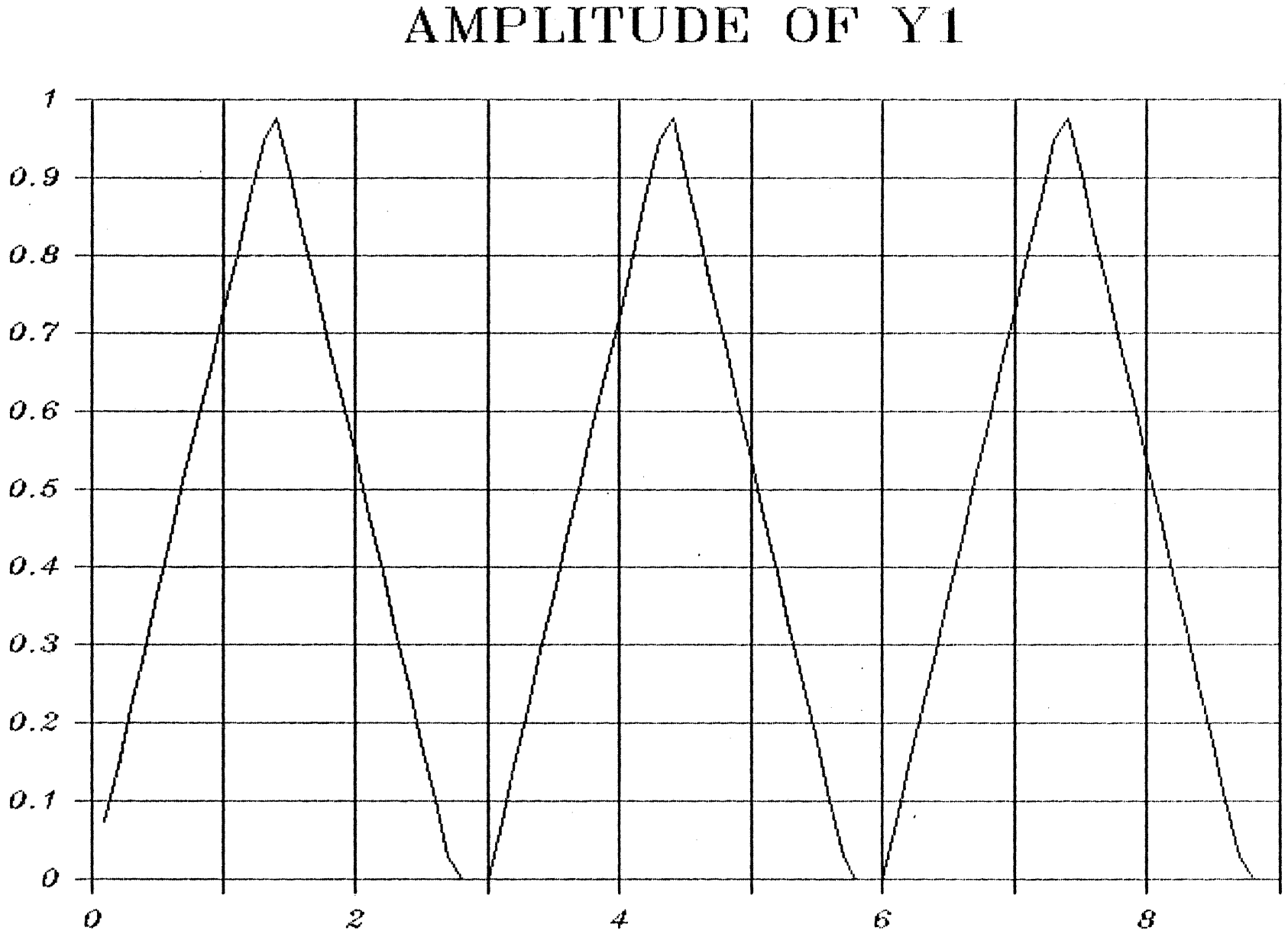


FIGURE TWO

AMPLITUDE OF Y1, Y2 AND Y3

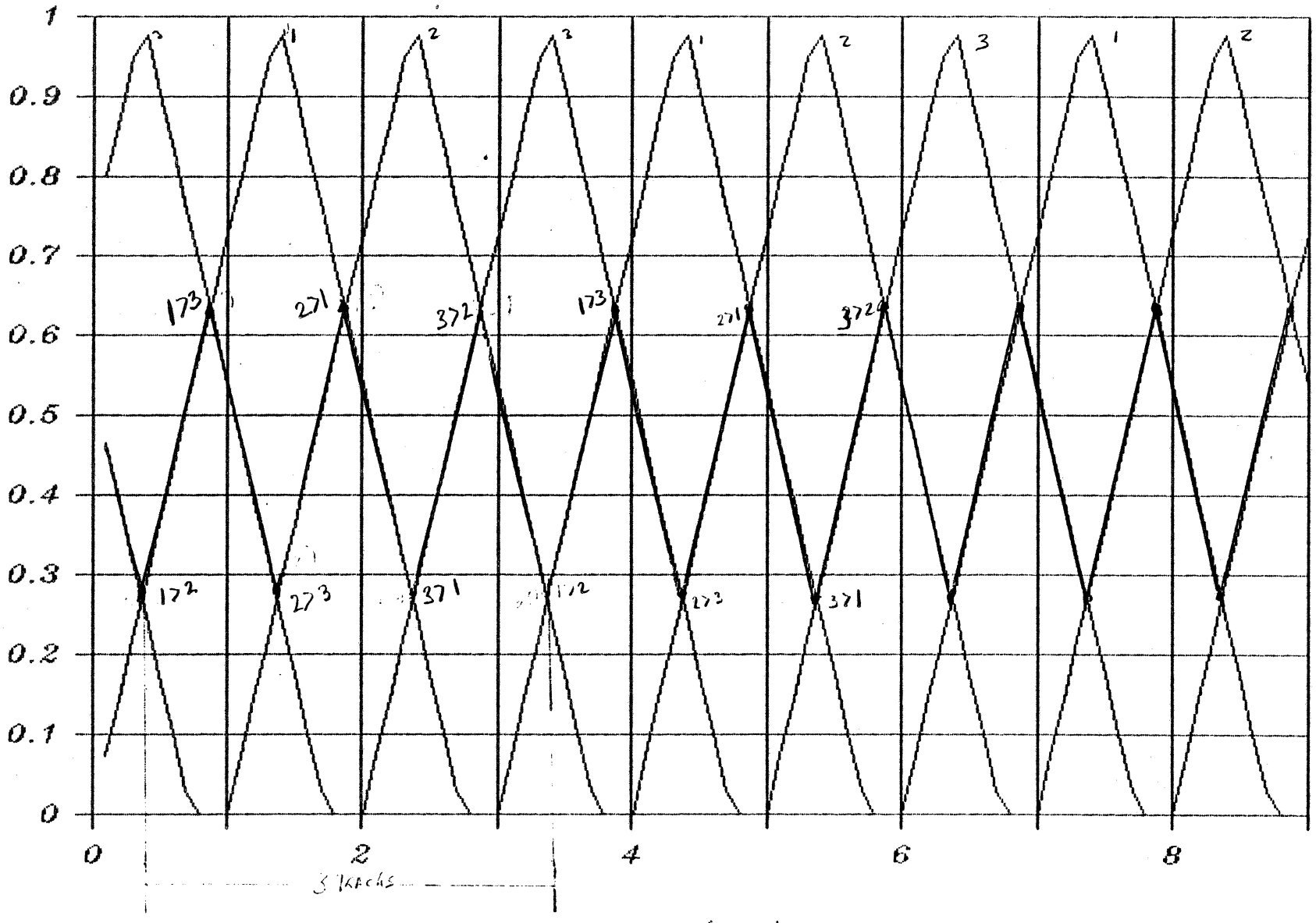


FIGURE THREE

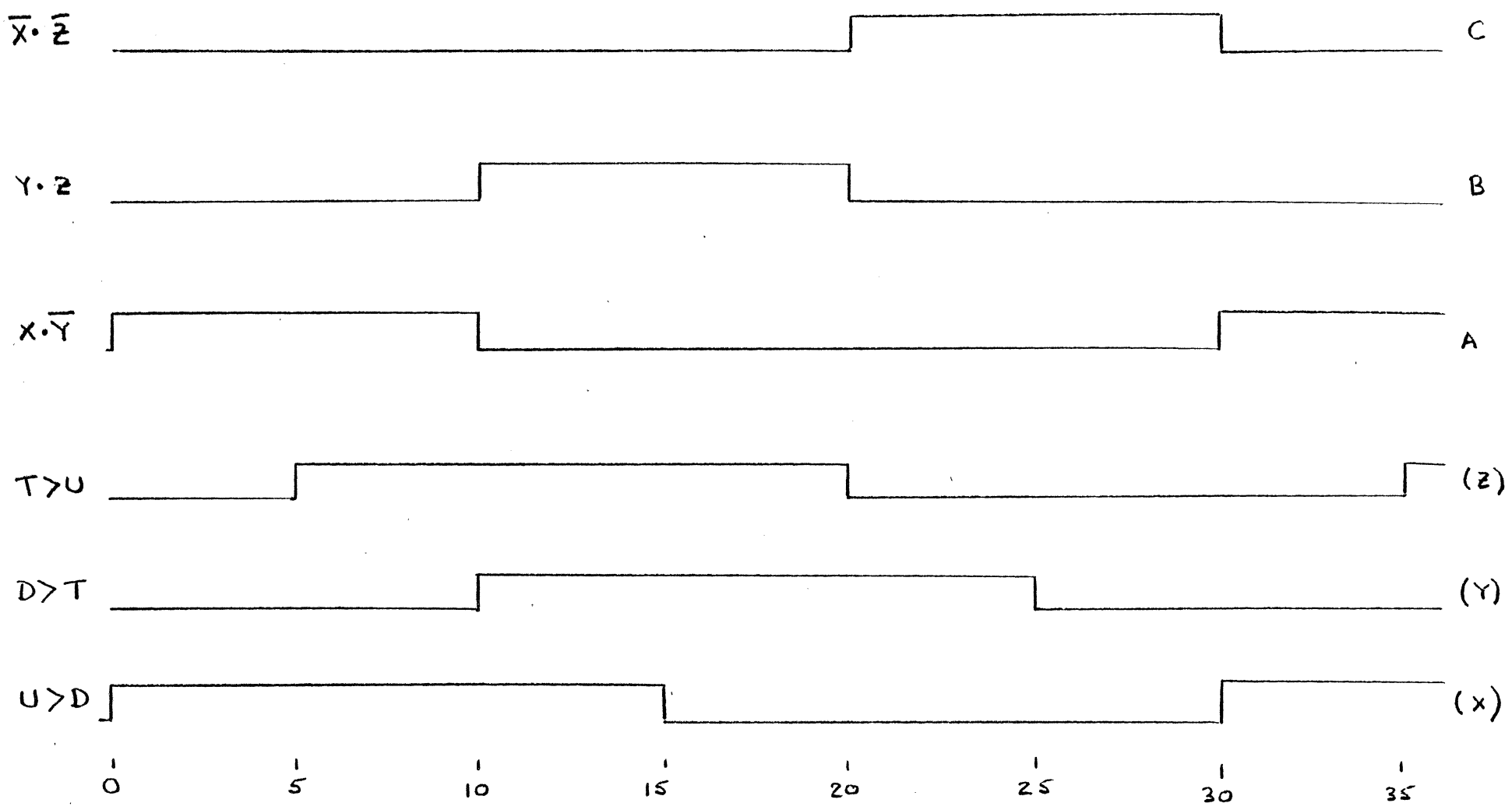

$\overline{X} \cdot \overline{Z}$
C
$Y \cdot Z$
B
$X \cdot \overline{Y}$
A
T>U
(Z)
D>T
(Y)
U>D
(X)
0
5
10
15
20
25
30
35

FIGURE FOUR

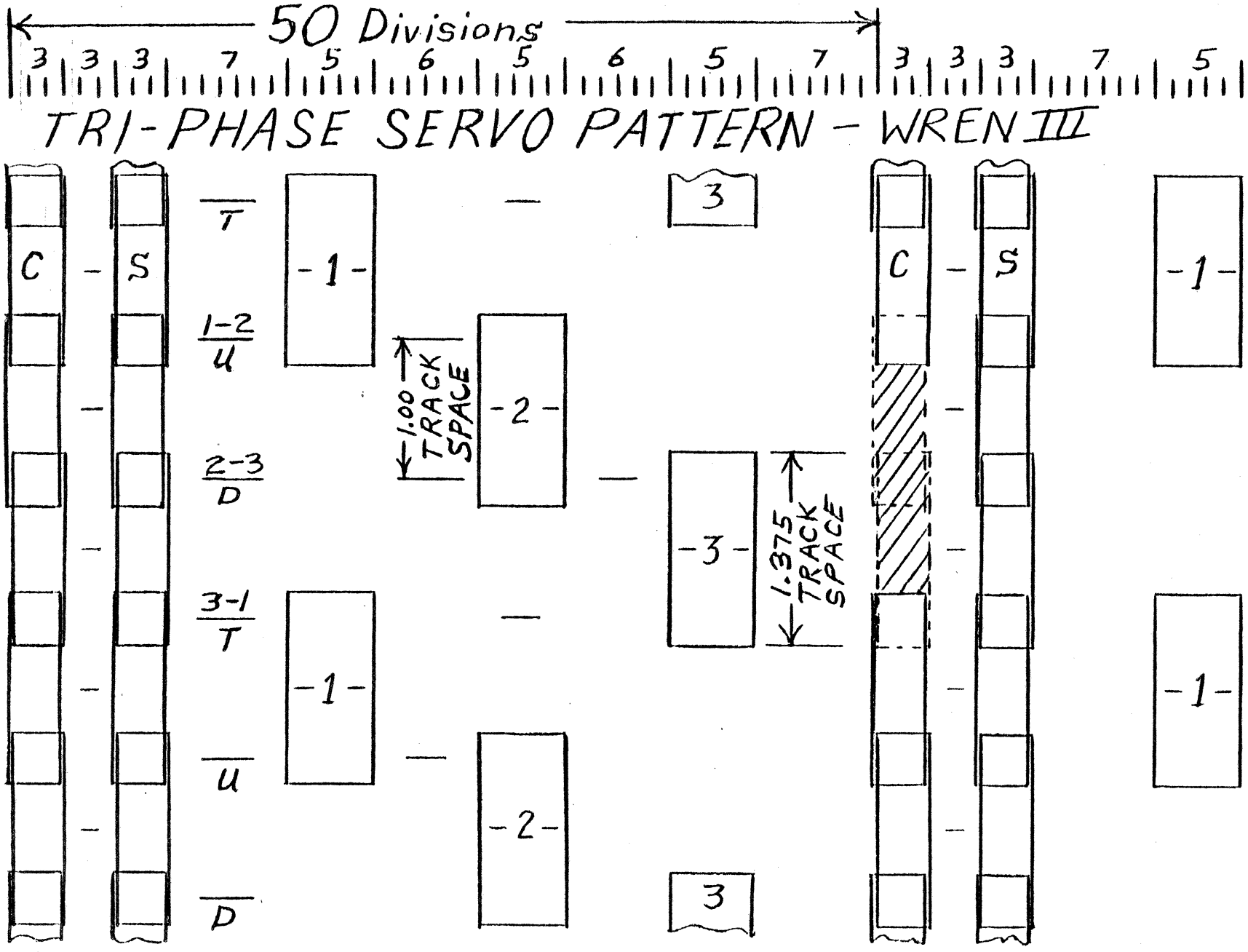
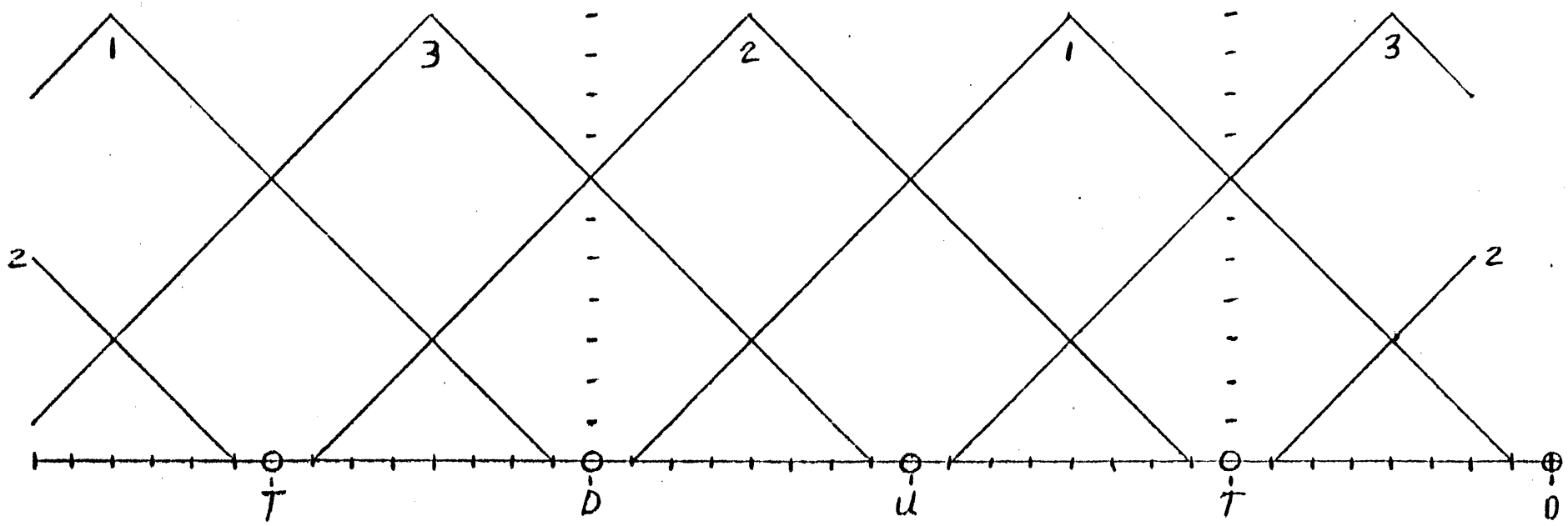


FIG. 1A

Donald W. Janz
Sept 25, 1984



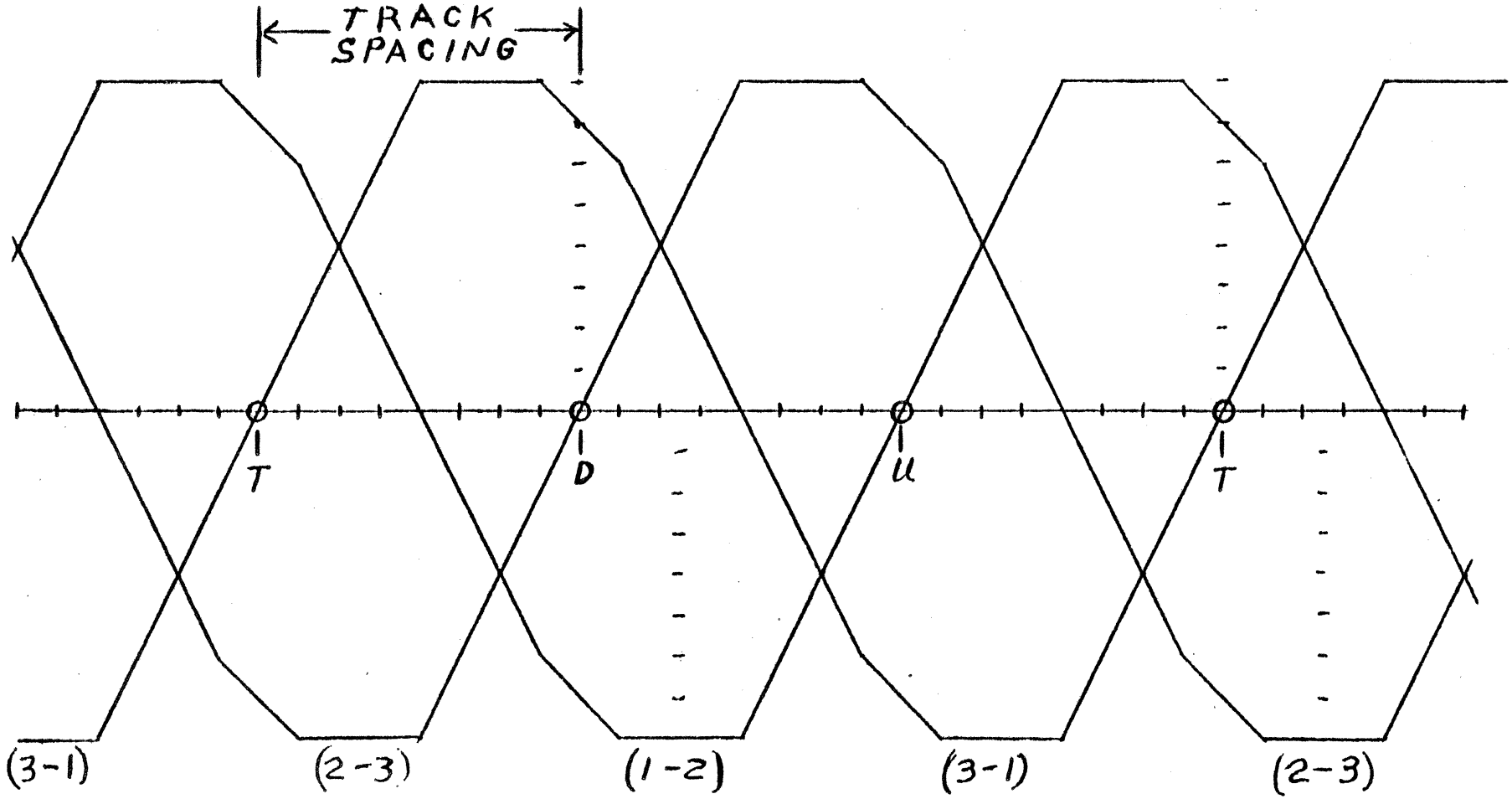
TRI-PHASE SERVO SIGNALS

FOR HEAD WIDTH = 1.375 TRACK SPACE

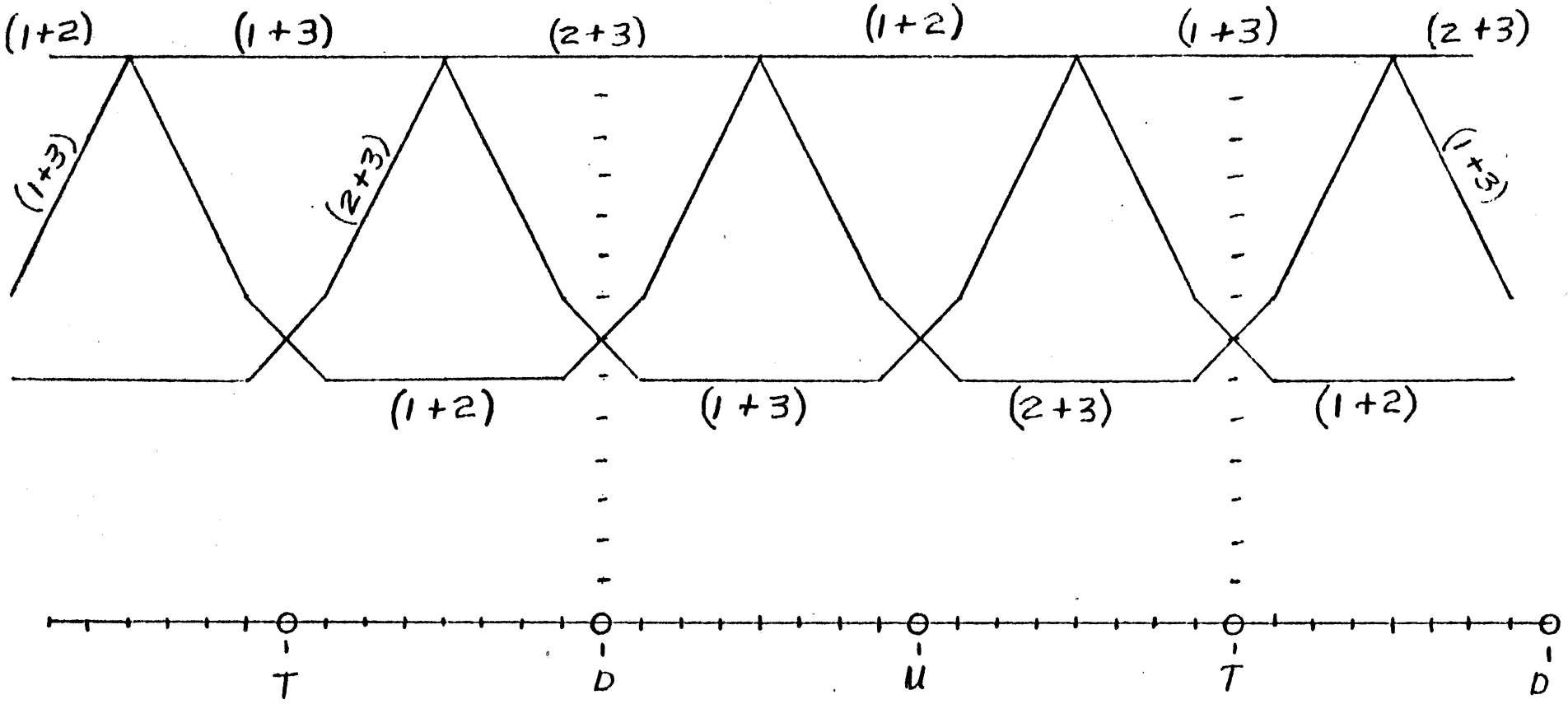
G W. Janz Sept 4, 1984

TRI-PHASE SERVO ERROR SIGNALS

FOR HEAD WIDTH = 1.375 TRACK SPACE



D W Jantz Sept 4, 1984



TRI-PHASE SERVO AGC SIGNALS

FOR HEAD WIDTH = 1.375 TRACK SPACE

D W Jarz
Sept 4, 1984

ANY STEP DISCONTINUITY IN DATA BYTE RATE AT THE END OF ONE REVOLUTION OF THE DISK AND THE BEGINNING OF THE NEXT IS MINIMIZED BY PLACING AN INTEGER NUMBER OF DATA BYTES PER DISK REVOLUTION. LIKEWISE, ANY STEP DISCONTINUITY IN SERVO SYNC SIGNALS CAN ALSO BE REDUCED BY PLACING AN INTEGER NUMBER OF SERVO FRAMES, EACH CONTAINING A SINGLE SERVO SYNC SIGNAL, PER DISK REVOLUTION. IT IS ADVANTAGEOUS FOR A DISK DRIVE SYSTEM THAT BOTH OF THE ABOVE CONDITIONS BE MET. TABLE 1 SHOWS THREE SETS OF PARAMETERS THAT MEET THESE CONDITIONS. COLUMN I IS THE SET CHOSEN FOR WREN III OVER ANOTHER CONSIDERED IN COLUMN II BECAUSE OF ITS HIGHER DATA BYTE COUNT PER REVOLUTION. COLUMN III REPRESENTS A SET WITH THE SMD DATA RATE AND THE SAME SERVO FRAME COUNT AS IN COLUMN I.

	UNITS	I	II	III
D	DIVISIONS / FRAME	50.	50.	50.
K	DIVISIONS / SVO. BIT	2.	2.	2.
DC / KB	DATA BITS / FRAME	29.0	28.0	28.0
M	DATA BYTES / REV.	20,880. $(2^4 \times 3^2 \times 5 \times 29)$	20,832. $(2^5 \times 3 \times 7 \times 31)$	20,160. $(2^6 \times 3^2 \times 5 \times 7)$
F	FRAMES / REV.	5760. $(2^7 \times 3^2 \times 5.)$	5952. $(2^6 \times 3 \times 31.)$	5760. $(2^7 \times 3^2 \times 5)$
DF	DIVISIONS / REV.	288,000.	297,600.	288,000.
C	DATA BITS / SECOND	10.000×10^6 $(2^7 \times 5^7)$	10.000×10^6 $(2^7 \times 5^7)$	9.67680×10^6 $(2^{11} \times 3^3 \times 5^2 \times 7)$
C / BM	REV. / SECOND	59.8659004	60.00384025	60.0000
FC / BM	FRAMES / SECOND	344,827.58	357,142.857	345,600.
P	SECONDS / FRAME	$2.9000 \times 10.^{-6}$	2.8000×10^{-6}	$2.8935185 \times 10.^{-6}$
B ≡ (CDF / BMK)	SVO. BITS / SECOND	$8.620689655 \times 10.^6$ $(2^7 \times 5^9)/29.$	$8.9285714 \times 10.^6$ $(2^5 \times 5^9)/7.$	8.6400×10^6 $(2^9 \times 3^3 \times 5^4)$
KB	DIVISIONS / SECOND	$17.241379 \times 10.^6$	$17.857143 \times 10.^6$	$17.2800 \times 10.^6$
1 / KB	SECONDS / DIVISION	58.000×10^{-9}	$56.000 \times 10.^{-9}$	$57.870371 \times 10.^{-9}$
RPM	REV. / MINUTE	3591.954023	3600.230415	3600.000

DESIGN STATUS

First prototype complete.

Tested prototype with emulator.

- Emulated seeks at up to 100 KTPS.
- SPE and TRACK PHASE valid to 100 KTPS.
- Velocity valid to 50-70 KTPS.

Wren III servo pattern has not been written yet.

Over all outlook at this point:

- chances of improving performance are very good.
- chances of additional circuit changes still high.

AREAS OF CONCERN

RISK	ACTION
Cannot write return to zero servo pattern.	improve STW circuits
Sink-code pair to fast to be written consistently	possibly slow spindle at STW.
High sink dibit modulation	add circuit to AGC on sum of the dibits
Servo pattern is non-linear	add feed-foreword circuit
Lower operating voltages will cause off-set problems	add auto-zero circuit

WREN III SERVO LSI DESIGN GOALS

- TO FIT IN A 40 PIN PLASTIC DIP PACKAGE.
- TO FIT IN A 2200 GATE ARRAY USING A 3 MICRON STANDARD CELL CMOS TECHNOLOGY.
- TO PROVIDE CONTROLLABILITY THROUGH A 5 BIT 8051 COMPATIBLE MICRO-CONTROLLER INTERFACE.
- TO BE ABLE TO SUPPORT BOTH 10 MHZ AND 15 MHZ DATA RATES.

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SERVO GATE TIMING

- GATE CLOCK IS SELECTED AS EITHER A DIVIDE BY TWO OR A DIVIDE BY THREE OF THE PLO CLOCK INPUT.

- EACH SERVO FRAME IS DEFINED BY 5 STATES WHICH ARE GENERATED BY THE DIVIDE BY 5 STATE COUNTER.

- THE DIVIDE BY 6 JOHNSON COUNTER PROVIDES TIMING WITHIN STATES AND CLOCKS THE DIVIDE BY 5 STATE COUNTER.

- THE DIVIDE BY 5 STATE COUNTER IS USED TO PROVIDE EXTERNAL GATES AND ADDITIONAL DECODE USING THE DIVIDE BY 6 JOHNSON COUNTER PROVIDES INTERNAL SERVO TIMING.

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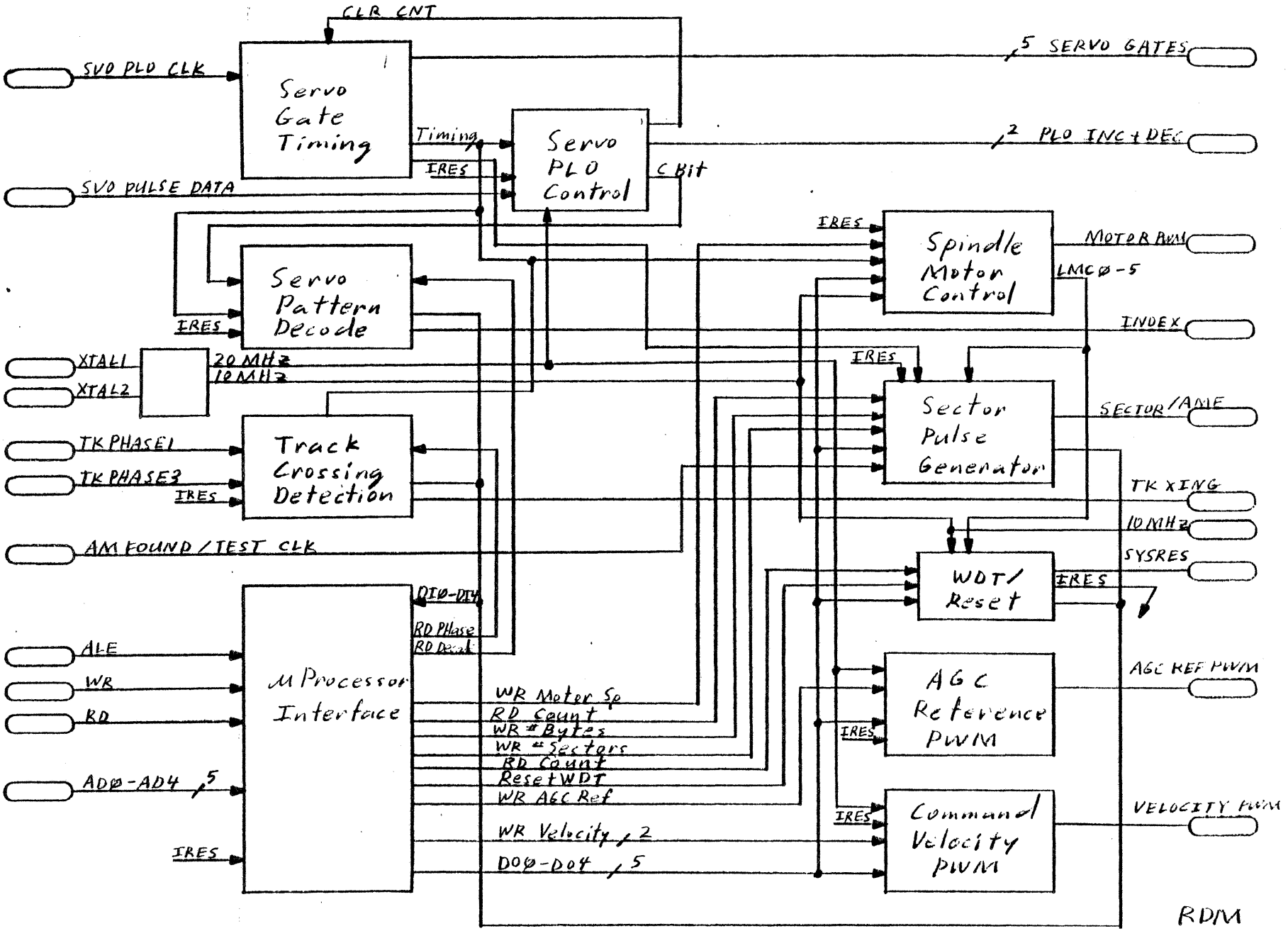
SERVO LSI



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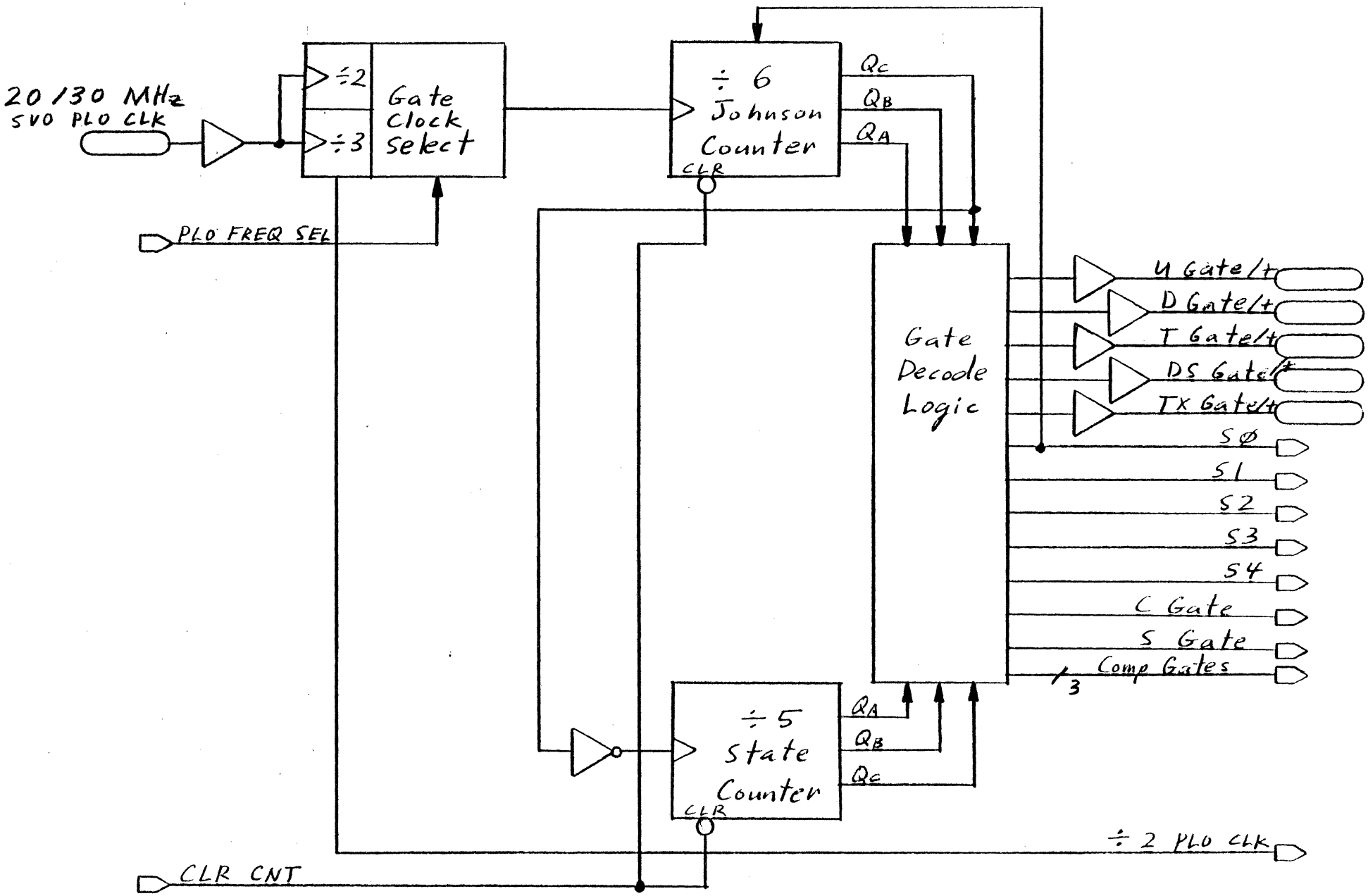
Servo Gate Timing



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SERVO PLO CONTROL

I. PLO NOT LOCKED

- THE PLO IS PUMPED DOWN ON RESET SO THAT ACQUISITION IS PERFORMED FROM BELOW FREQUENCY.
- THE DIVIDE BY 9 COUNTER IS USED TO DETECT CODE-SYNC PAIRS.
- ONCE A CODE-SYNC PAIR IS DETECTED, CLR CNT IS RELEASED TO ENABLE SERVO GATE TIMING.
- THE PLO FINC AND FDEC ARE BASED ON THE ERRORS BETWEEN THE NEXT CODE-SYNC PAIR AND SØ.
- A FAULTY FDEC DUE TO A MISSING CODE-SYNC PAIR IS COMPENSATED FOR WITH AN EQUIVALENT FINC.
- AFTER EACH PLO ADJUSTMENT, CLR CNT IS ACTIVATED TO DISABLE SERVO GATE TIMING TILL THE NEXT CODE-SYNC PAIR IS DETECTED.
- THE TRANSITION TO LOCK IS MADE AFTER 128 CONSECUTIVE SERVO PULSES WITHIN THE SYNC GATE ARE DETECTED.

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SERVO PLO CONTROL

II. PLO LOCKED

- PLO FINC AND FDEC ARE LIMITED BY SYNC GATE.
- ANY FDEC WHICH IS OUT OF RANGE OF SYNC GATE IS CONSIDERED FAULTY AND IS COMPENSATED FOR. WHEN THIS OCCURS TX GATE IS DIABLED FOR THE NEXT SERVO FRAME.
- CLR CNT IS HELD ACTIVE. PHASE ERRORS ARE CUMMULATIVE.
- THE TRANSITION OUT OF LOCK IS PERFORMED WHEN 8 CONSECUTIVE PULSES WITHIN SYNC GATE ARE MISSING.

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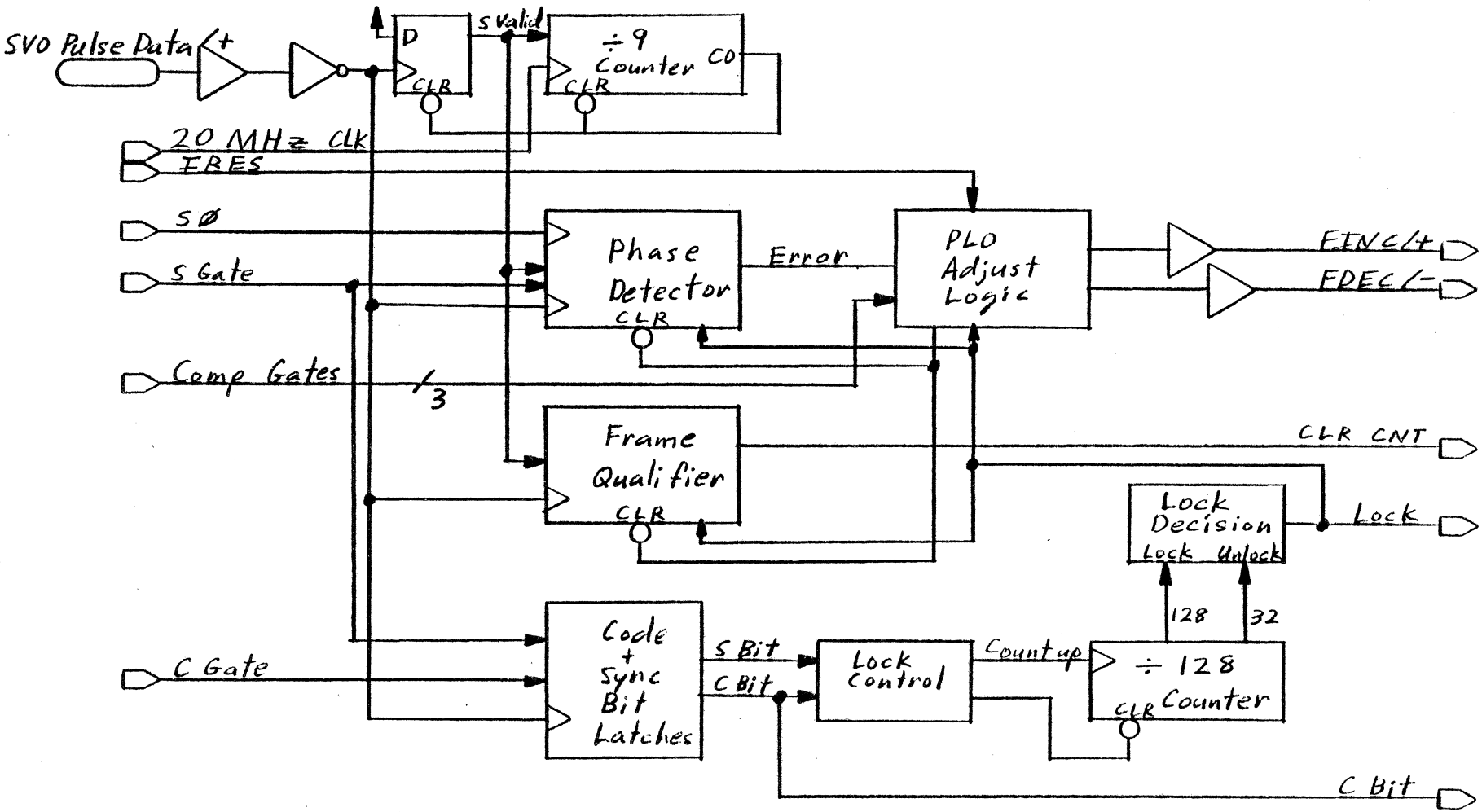
Servo PLO Control



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SERVO PATTERN DECODE

- THE 7 BIT SHIFT REGISTER HOLDS THE CURRENT PATTERN WINDOW.
- THE PATTERN DECODE LOGIC DECODES THE PRE-DEFINED 7 BIT CODE PATTERNS.
- THE DECODED PATTERNS ARE GATED WITH EACH OTHER TO GUARANTEE UNIQUENESS AND THEN LATCHED. AN ADDITIONAL LATCH IS USED BY THE PROCESSOR TO INDICATE A PREVIOUS GUARD BAND DETECTION.
- THE INDEX LOGIC SYNCHRONIZES INDEX AND SETS THE DUTY CYCLE.

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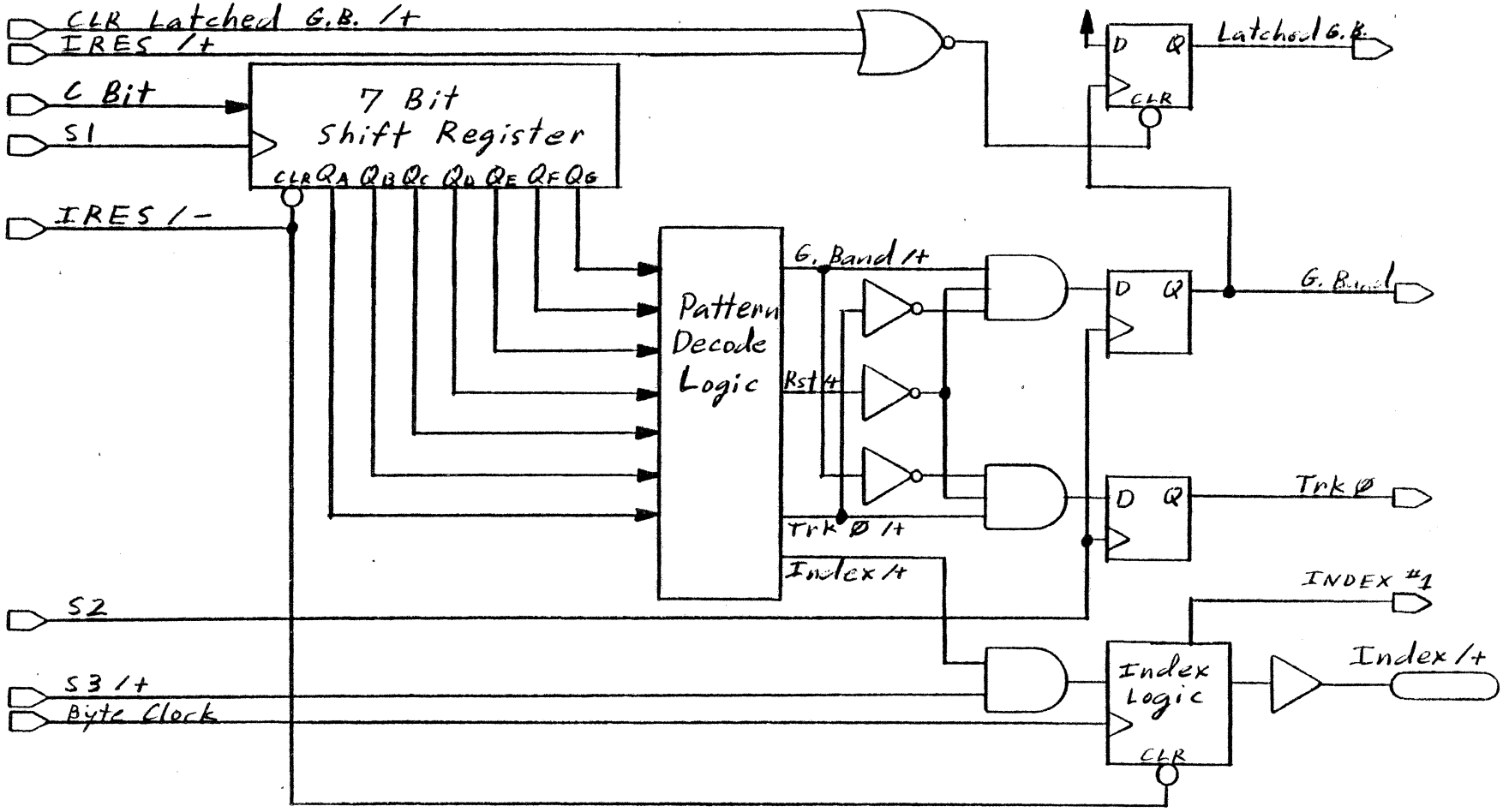
Servo Pattern Decode



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SPINDLE MOTOR CONTROL

- A MOTOR SPEED VALUE IS WRITTEN TO THE 9 BIT DATA LATCH USING THE MICROPROCESSOR.

- THE MOTOR SPEED VALUE IS USED IN THE DIVIDE BY 512 LOADABLE COUNTER TO GENERATE A REFERENCE.

- THE VALUE OF THE REFERENCE AT THE END OF THE DIVIDE BY 16 FRAME COUNT IS USED TO INCREMENT OR DECREMENT THE DIVIDE BY 16 SELECT COUNTER.

- THE PWM DUTY CYCLES ARE DECODED FROM THE DIVIDE BY 16 FRAME COUNTER.

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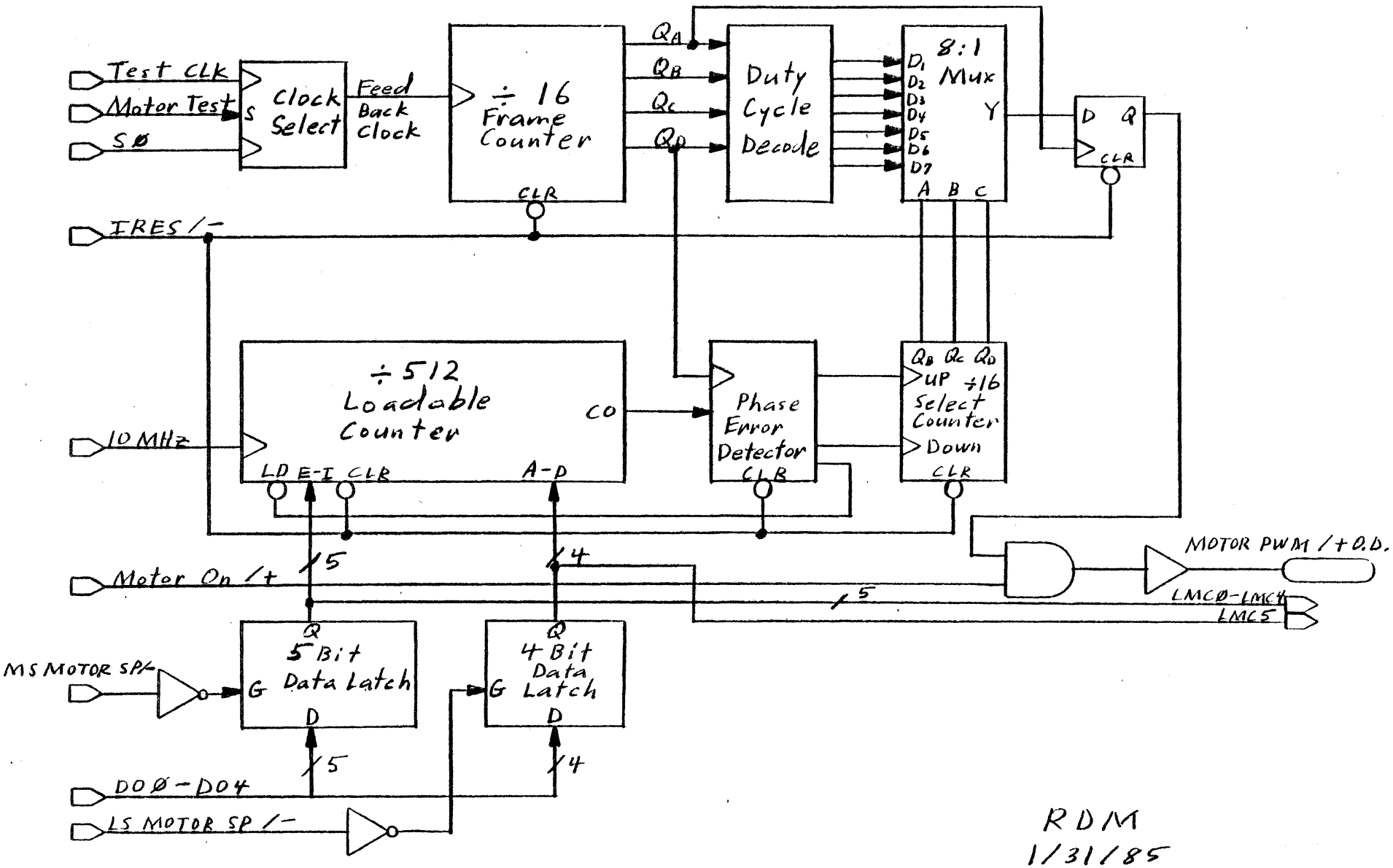
Spindle Motor Control



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TRACK CROSSING DETECTOR

- TRACK PHASE 1 IS ALSO USED TO GENERATE TRACK PHASE 2.

- THE TRACK PHASE QUALIFIER LOGIC LIMITS THE NEXT POSSIBLE PHASE BASED ON PRESENT PHASE AND DIRECTION OF VELOCITY.

- THE PHASE LATCHES DETECT A QUALIFIED CHANGE OF PHASE AND HOLD THE VALUE FOR USE BY THE PHASE QUALIFIER LOGIC.

- THE TK XING LATCHES ALONG WITH THE DIVIDE BY 2 COUNTER DETECT AND GENERATE A TK XING PULSE AT LEAST ONE SERVO FRAME WIDE.

- THE MICROPROCESSOR INTERFACE SETS RD PHASE TO READ THE TRACK PHASES AND RESET THE PHASE LATCHES.

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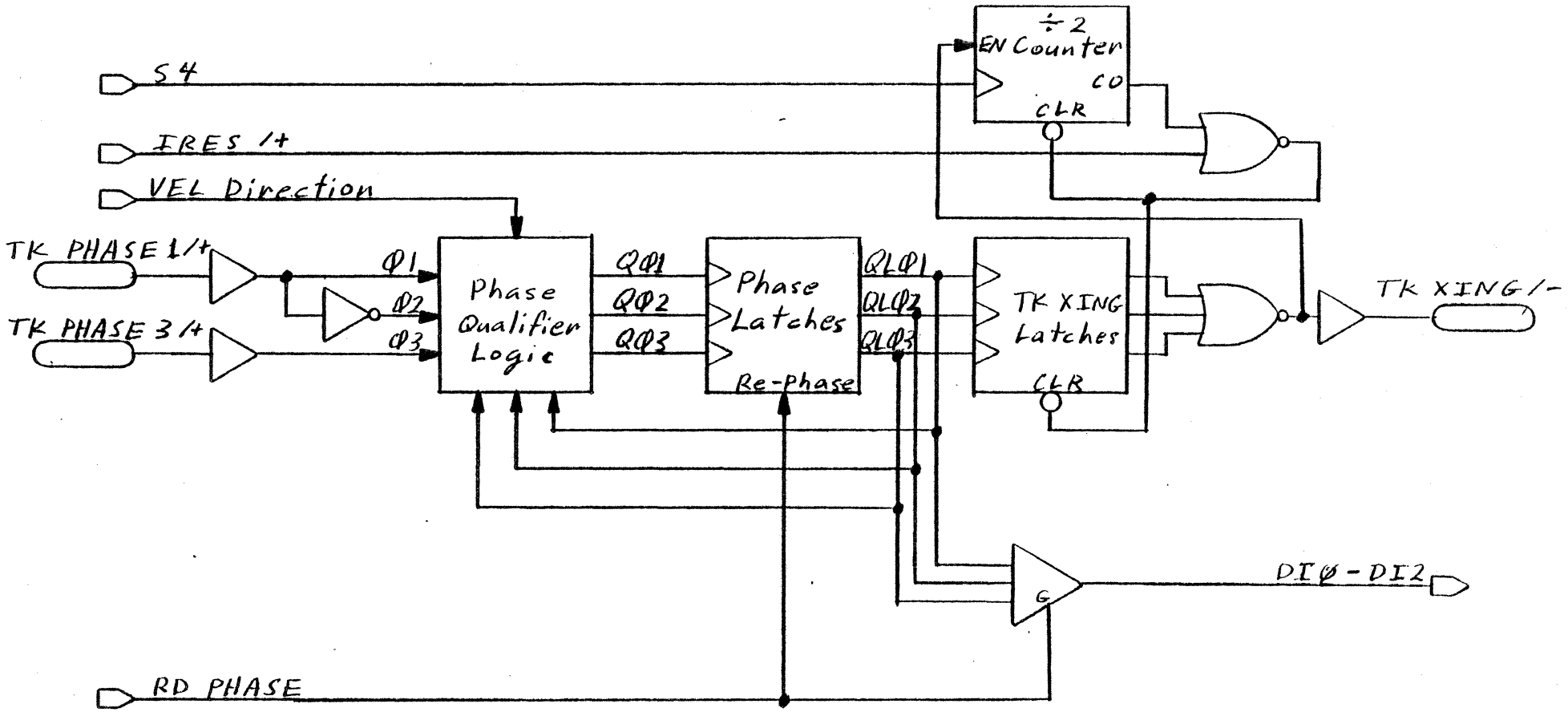
Track Crossing Detector



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AGC REFERENCE PWM

- AN AGC DUTY CYCLE VALUE IS LOADED INTO THE 5 BIT DATA LATCH USING THE MICROPROCESSOR INTERFACE.

- WHEN THE DUTY CYCLE VALUE IS EQUAL TO THE 6 BIT COUNTER VALUE THE J-K FLIP-FLOP SETS AGC REF ACTIVE STARTING ON THE NEXT CLOCK EDGE.

- A ZERO COUNT DECODE SETS AGC REF INACTIVE ON THE NEXT CLOCK EDGE.

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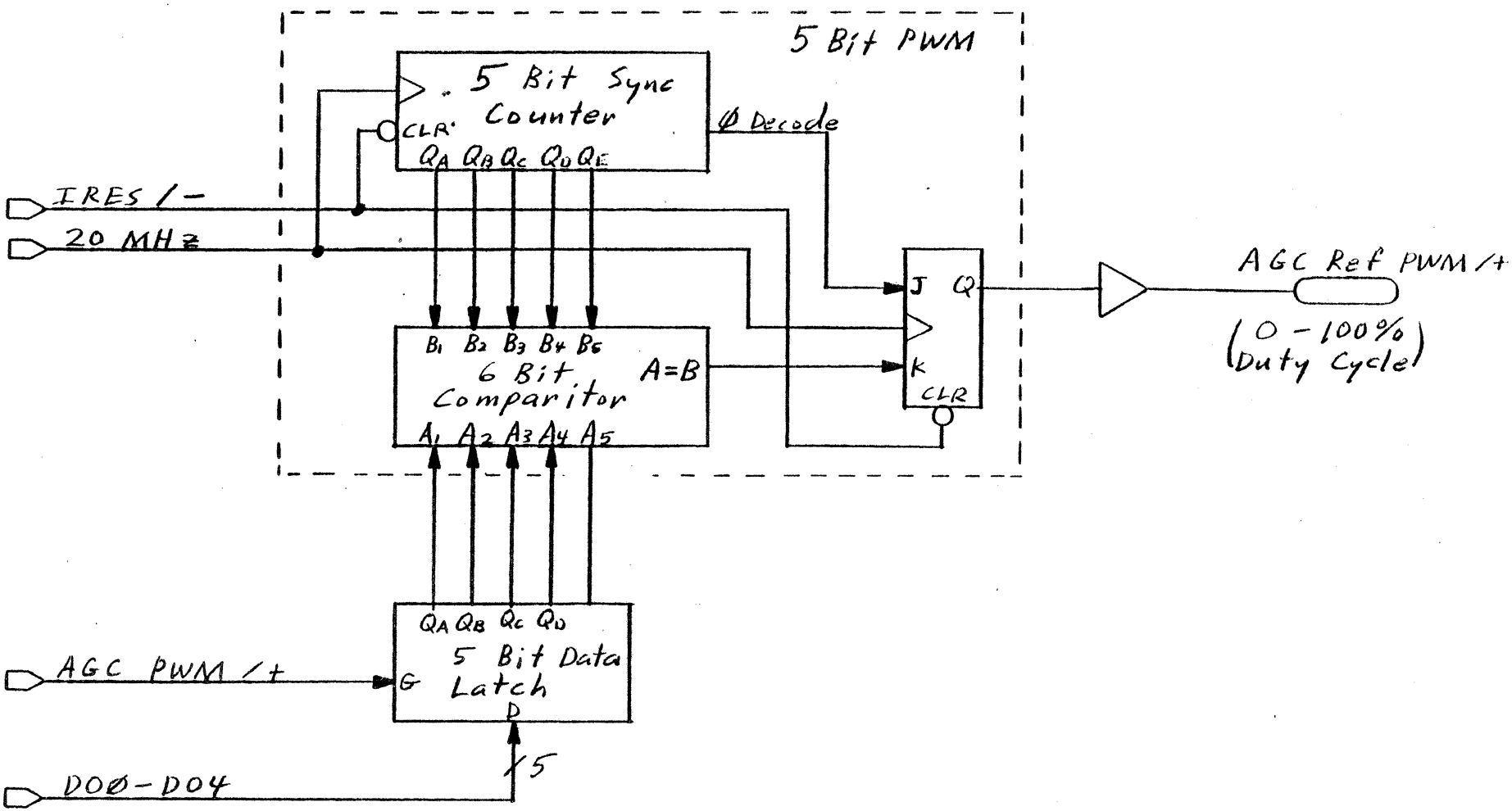
AGC Reference PWM



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MICROPROCESSOR INTERFACE

- THE 5 BIT ADDRESS LATCH USES ALE TO HOLD THE CURRENT ADDRESS.

- THE WRITE ADDRESS DECODE LOGIC DECODES THE LATCHED ADDRESS (00-0FH) AND SELECTS THE CORRESPONDING LATCH ENABLE WHEN WR IS ACTIVE.

- THE READ ADDRESS DECODE LOGIC DECODES THE LATCHED ADDRESS (00-0FH) AND SELECTS THE CORRESPONDING OUTPUT ENABLE WHEN RD IS ACTIVE. A BLOCK DECODE IS USED TO ENABLE OUTPUT TO THE EXTERNAL BUS. OUTPUT TO THE EXTERNAL BUS IS NOT ENABLED WHEN RD1 IS ACTIVE.

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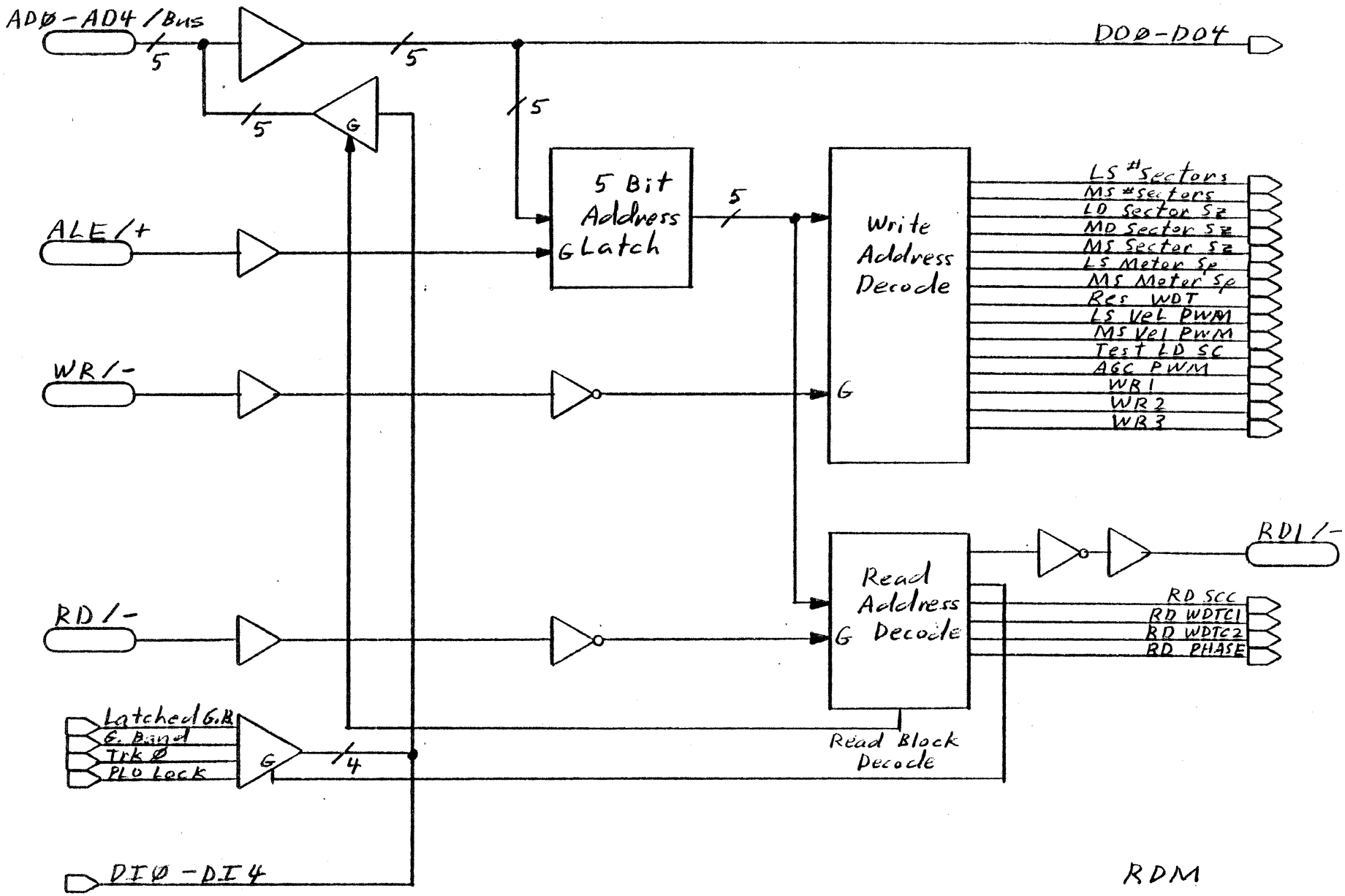
μProcessor Interface



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SECTOR PULSE GENERATOR

- THE SECTOR COUNT AND NUMBER OF SECTORS IS LOADED INTO THE FIVE - 4 BIT DATA LATCHES USING THE MICROPROCESSOR INTERFACE.

- THE COMPLIMENT OF THE LATCHED SECTOR COUNT AND NUMBER OF SECTORS IS LOADED INTO THE FIVE - 4 BIT COUNTERS DURING THE FIRST BYTE OF INDEX.

- THE CARRY FROM THE LEAST SIGNIFICANT 3 COUNTERS IS USED TO GENERATE THE SECTOR PULSE. THESE COUNTERS ARE RELOADED AT THE END OF EACH SECTOR.

- THE MOST SIGNIFICANT 2 COUNTERS ARE USED TO COUNT THE NUMBER OF SECTORS SINCE INDEX. A CARRY FROM THESE COUNTERS HOLDS THE BYTE COUNTERS IN THE LOAD STATE UNTIL THE NEXT INDEX. THIS IS DONE TO INHIBIT SHORT SECTORS PRIOR TO INDEX.

- THE COUNTER CLOCK SELECT ALONG WITH THE AM FOUND/TEST CLOCK INPUT ARE INCORPORATED FOR EASE OF TESTABILITY OF THE COUNTER SECTION.

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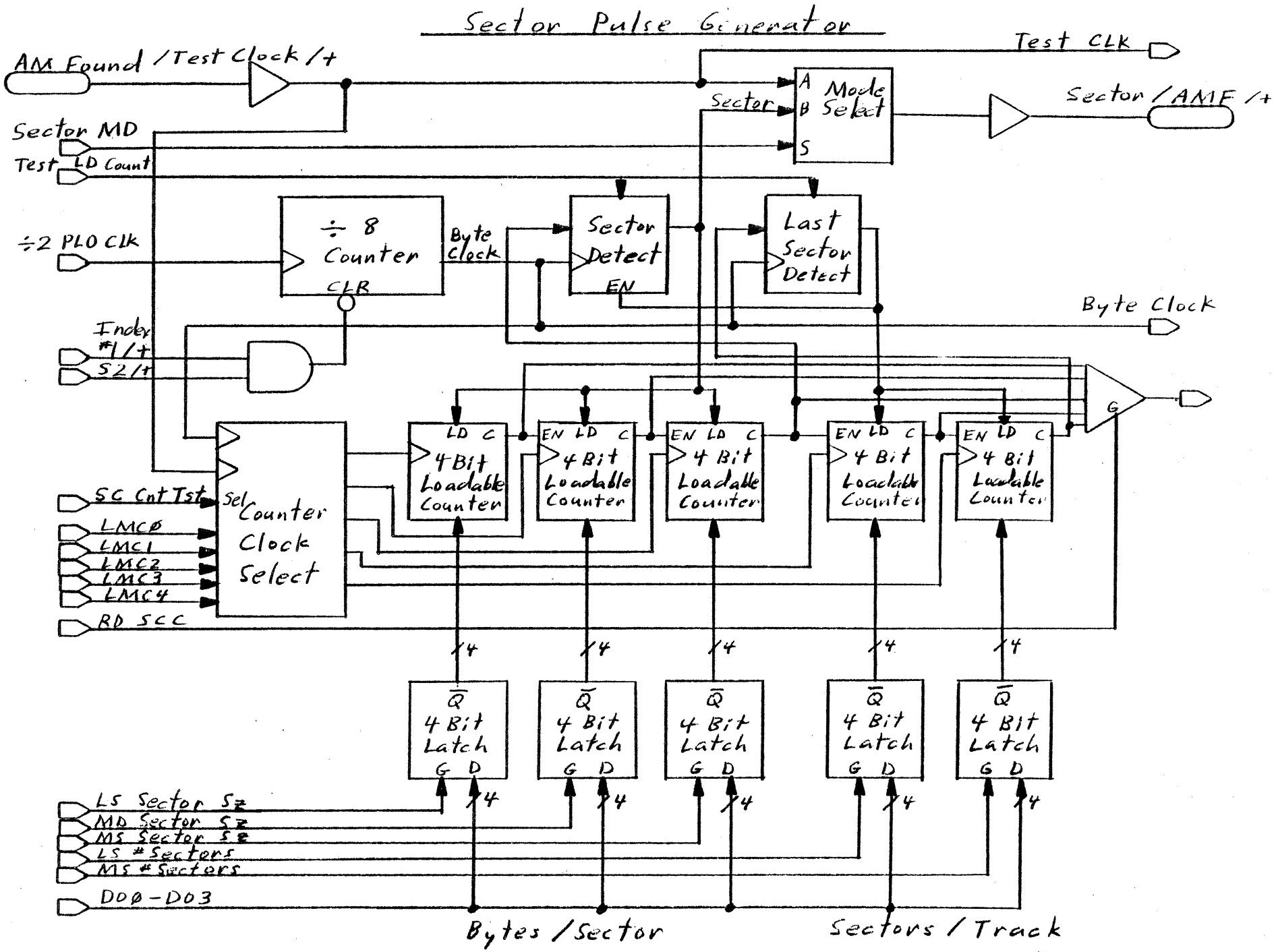
Sector Pulse Generator



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COMMAND VELOCITY PWM

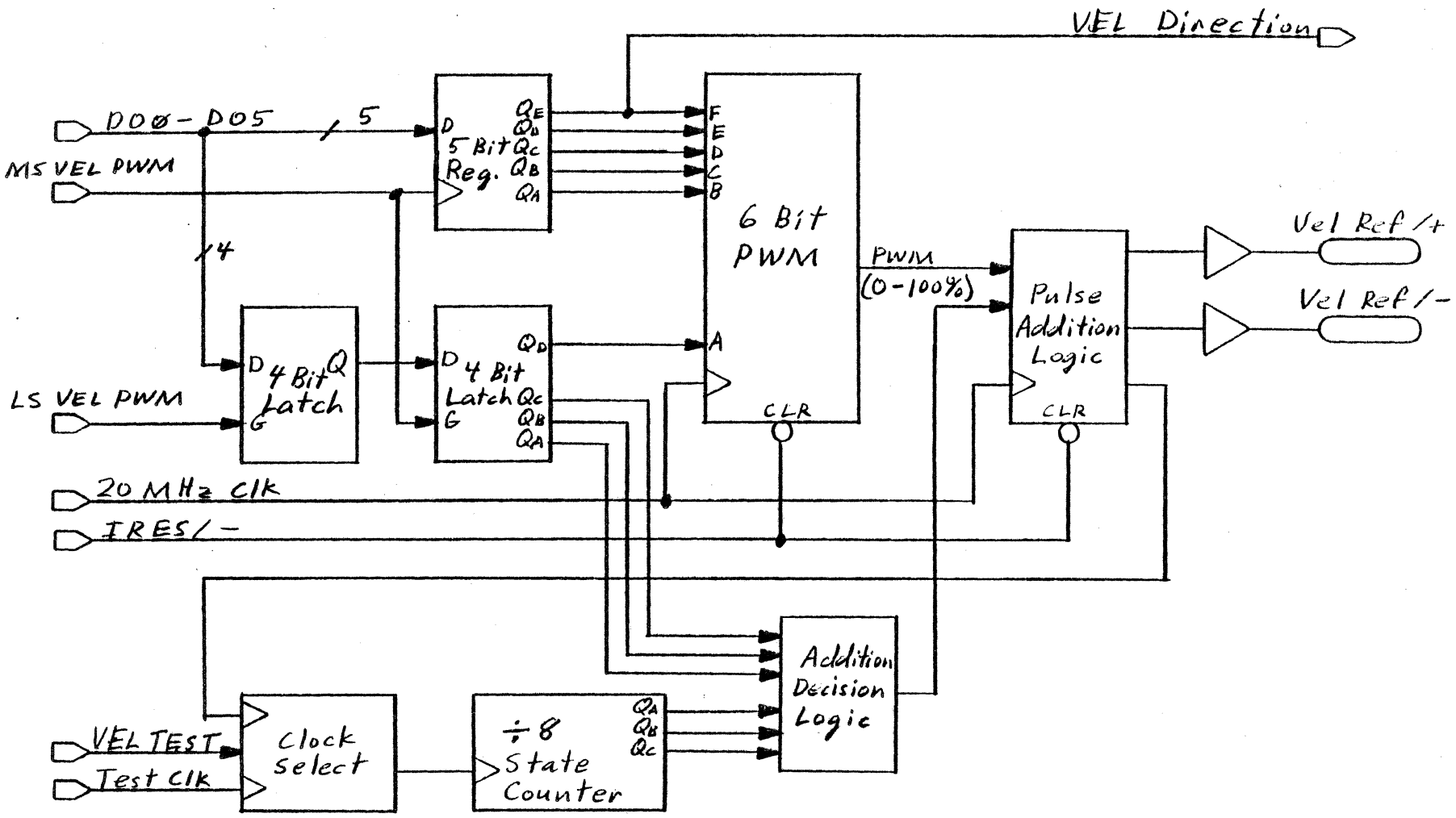
- THE VELOCITY PWM DUTY CYCLE VALUE IS LOADED USING THE MICROPROCESSOR INTERFACE. THE LOW ORDER 4 BITS ARE DOUBLE BUFFERED TO GUARANTEE A CLEAN CHANGE OF VELOCITY.

- THE LOW ORDER 3 BITS AND THE DIVIDE BY 8 STATE COUNTER ARE USED TO DEFINE WHICH PERIODS SHOULD HAVE AN ADDITIONAL CLOCK OF ON TIME.

- THE PWM USED IS A 6 BIT VERSION OF THE ONE USED FOR AGC.

RDM
1/31/85

Command Velocity PWM



RDM
1/31/85

WATCH DOG TIMER/RESET LOGIC

- AN ACTIVE RESET WILL SET SYSRES AND IRES ALONG WITH CLEARING THE 6 STATE RIPPLE COUNTER.

- UPON RELEASE OF RESET THE SYSRES OUTPUT WILL REMAIN ACTIVE UNTIL THE 6 STAGE COUNTER REACHES A COUNT OF 128 AT WHICH POINT SYSRES IS CLEARED.

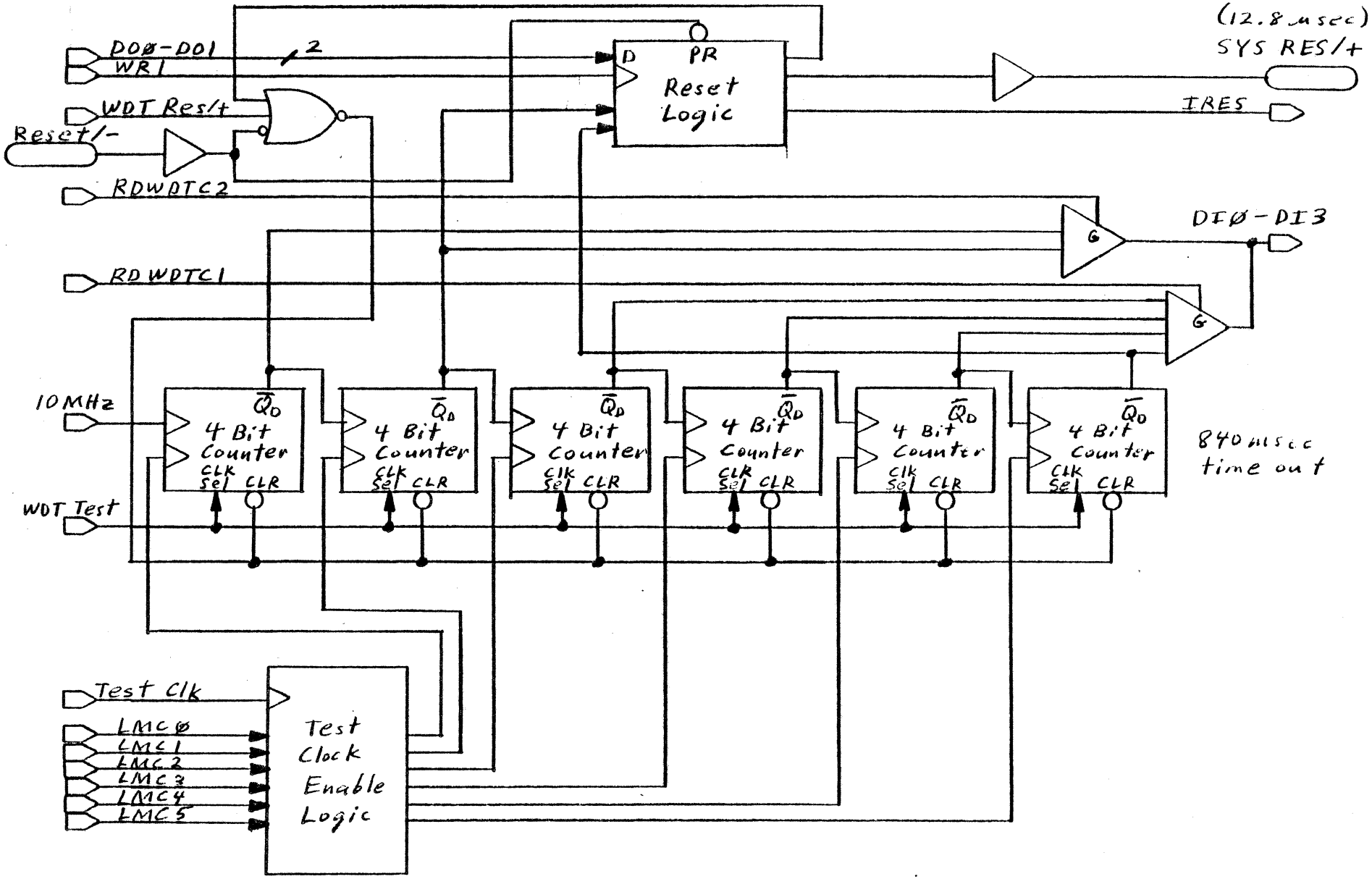
- WHEN THE 6 STAGE COUNTER REACHES A COUNT OF 800000H (840 MSEC) AND THE WDT IS ENABLED, SYSRES WILL BE ACTIVATED.

- THE MICROPROCESSOR INTERFACE CAN CLEAR THE 6 STAGE COUNTER USING WDT RES AND CAN INDEPENDENTLY SET IRES AND DISABLE THE SYSRES LOGIC.

- THE TEST CLOCK ENABLE LOGIC ALONG WITH TEST CLOCK IS INCORPORATED FOR EASE OF TESTABILITY OF THE 6 STAGE COUNTER SECTION.

RDM
1/31/85

Watch Dog Timer / Reset Logic



RDM
1/31/85

RISKS & ALTERNATIVES

- PLO CONTROL USING THE CODE-SYNC PAIR DETECTION CONCEPT IS NEW AND HAS ONLY BEEN PROVEN ON THE SERVO DI-BIT GENERATOR.

  SOME ADDITIONAL LOGIC IN THE PLO CONTROL SECTION MAY BE REQUIRED.

- THE SERVO DECODE PATTERNS ARE NEW AND HAVE NOT BEEN TESTED ON A WORKING DRIVE.

  DECODE PATTERNS MAY HAVE TO BE RE-DEFINED.

- THE 3 MICRON SERIES GATE ARRAY MAY NOT BE FAST ENOUGH TO SUPPORT THE 20 MHZ PULSE WIDTH MODULATORS AND THE 15 MHZ DATA RATE OPTION.

  MAY HAVE TO GO TO A FASTER PWM WITH A LARGER GATE COUNT AND/OR GO TO A 2 MICRON SERIES GATE ARRAY.

RDM
1/31/85

SERVO LSI STATUS

BREADBOARD * (FUNCTIONS 1-5)	% COMPLETE
DESIGN	100
BREADBOARD	100
DEBUG/TEST	100
EMULATOR	
DESIGN	100
LAYOUT PWB	20
DEBUG/TEST	0
INTEGRATE	0
LSI	
DESIGN/CONVERT	100
SIMULATE	0
INTEGRATE	0

*FUNCTIONS 1 - SERVO GATE TIMING
2 - SERVO PLO CONTROL
3 - TRACK CROSSING DETECTOR
4 - AGC REFERENCE PWM
5 - COMMAND VELOCITY PWM

RDM
1/31/85

SERVO POSITIONING

FEATURES

- USES ONLY POSITIVE SUPPLIES - +12V, +10V REF AND +5V REF.

- PULSE WIDTH MODULATOR/DEMOD ELIMINATES NEED FOR DAC AND ASSOCIATED CIRCUITRY. MOD/DEMOD IS MULTIPURPOSE - USED FOR DEMAND VELOCITY GENERATION, DATA RECOVERY OFFSET AND WRITE COMPENSATION MODES (THIS IS POSSIBLE SINCE THE THREE MODES ARE MUTUALLY EXCLUSIVE). COMPLEX LOGIC FOR PWM MECHANIZATION IS IMPLEMENTED IN LSI.

- WITH EXCEPTION OF PWM AND SPE/VELOCITY FRONT END, SERVO ARCHITECTURE IS IDENTICAL TO WREN II, THEREBY MINIMIZING IMPLEMENTATION RISKS.

OLF
1/18/85

RISKS & CONCERNS

- OFFSET SENSITIVITY OF PWM DUE TO TEMPERATURE VARIATION.

- QUALITY/RELIABILITY OF NEWLY RELEASED HIGH SPEED ANALOG SWITCH USED IN PWM DEMOD.

- EFFECT OF +5V REF STABILITY ON SERVO PERFORMANCE.

OLF
1/18/85

ALTERNATIVES

- THE ALTERNATIVE TO A PWM PROBLEM IS TO REPLACE IT WITH A DAC WHICH WILL OPERATE WITH POSITIVE SUPPLY ONLY AND ADDITION OF APPROPRIATE LOGIC INTERFACE WITH LSI OUTPUTS.

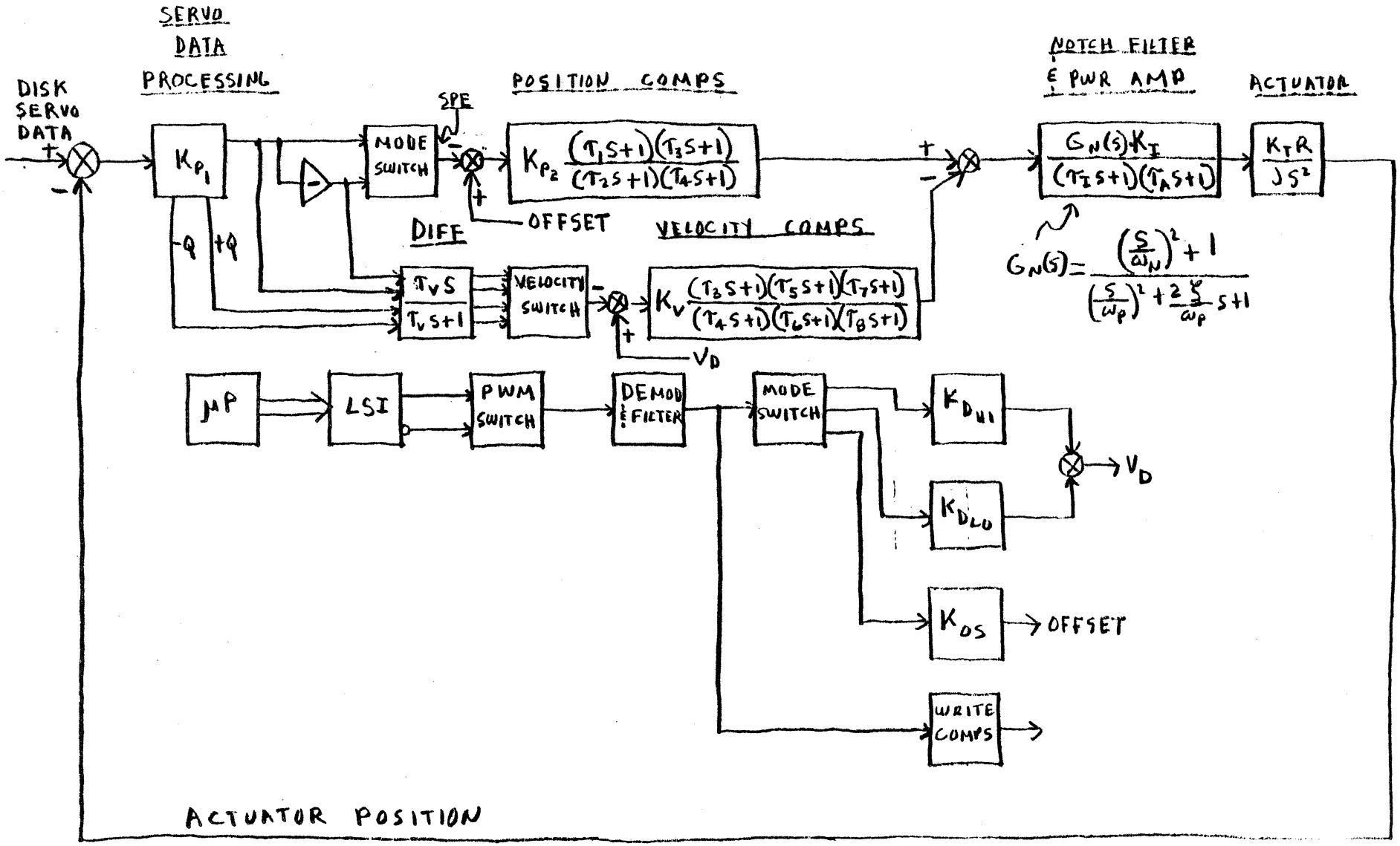
- A +5V REF STABILITY PROBLEM CAN BE SOLVED BY 1) INCREASING LOAD CURRENT CAPABILITY AND 2) SELECTION OF HIGHER GRADE COMPONENTS.

TEST RESULTS

- BENCH TESTS ON THE PWM INDICATE

  A) VOLTS /BIT + 11 MV/BIT (512 BIT RANGE)
  B) VOLTS/BIT = 22 MV/BIT (256 BIT RANGE)
  C) NON-LINEARITY 1% (BOTH RANGES)
  D) MAX RIPPLE = 100 MVPP @ 312.5 KHZ (BOTH RANGES)

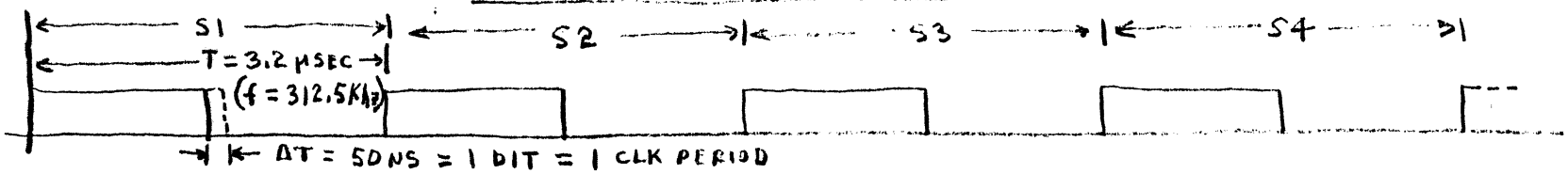
OLF
1/18/85



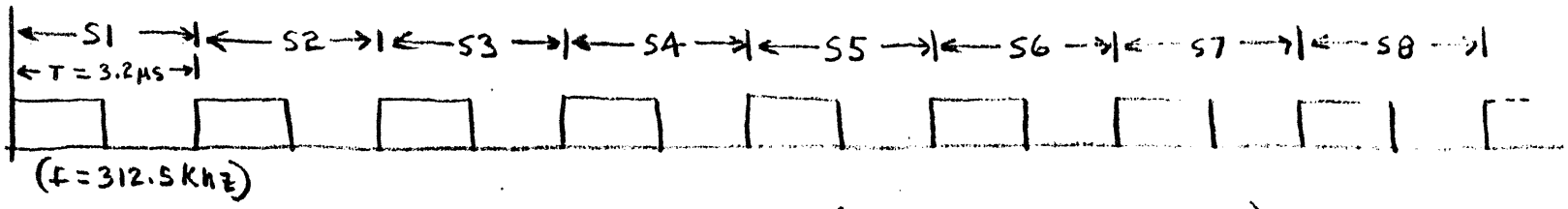
WREN III POSITIONING SERVO 1-18-85

017

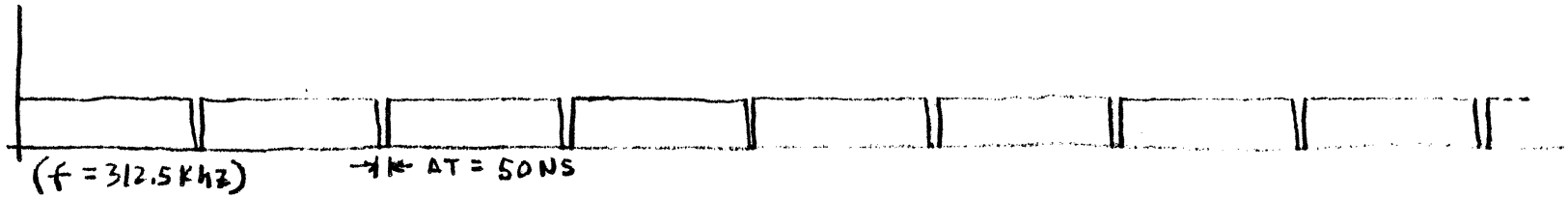
256 BIT SEGMENTATION (4 SEGMENTS)



512 BIT SEGMENTATION (8 SEGMENTS)



50% D.C. — OUTPUT = +5V (0 VELOCITY REFERENCE) — 256 BITS



98.4375% D.C. — MAX OUTPUT = +7.90625V — 504 BITS

1.5625% D.C. — MIN OUTUT = +2.09375V — 8 BITS

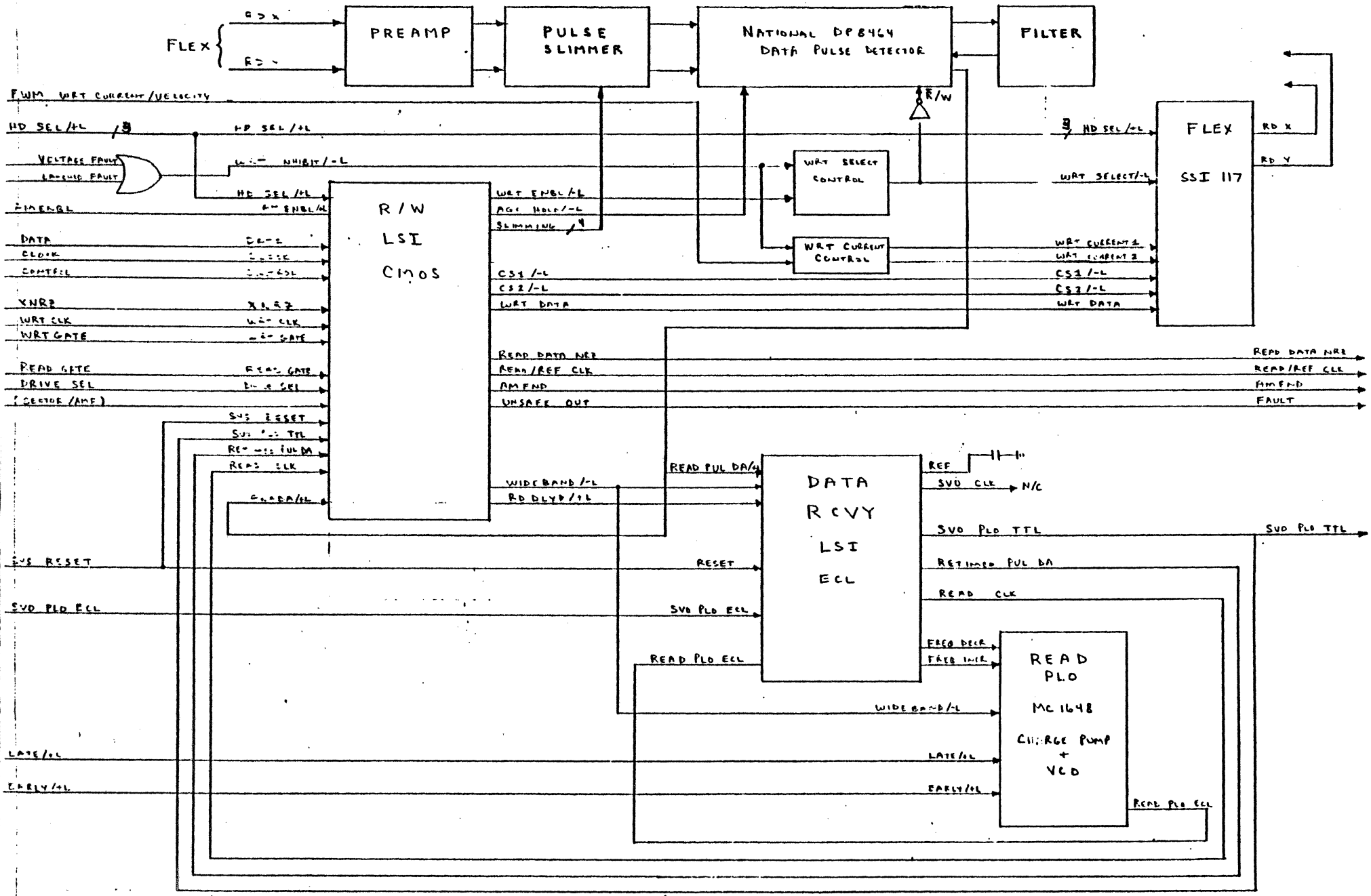
VOLTS/BIT RESOLUTION = 11.71875 MV/BIT. — NON-LINEARITY < 1% — MAX RIPPLE < 100 MV PP

PWM MECHANIZATION — 1-21-85 d/f

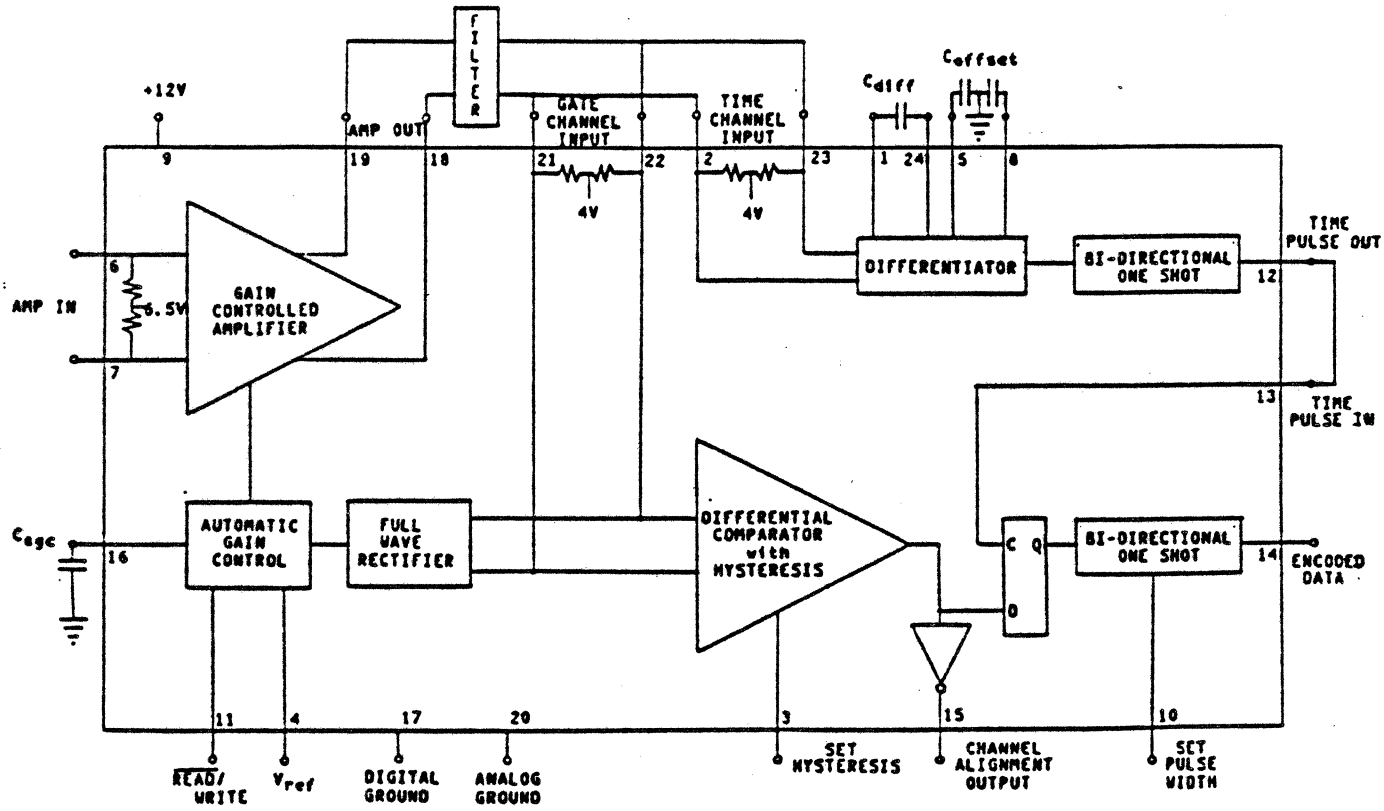
DESIGN GOALS

R. Cronch

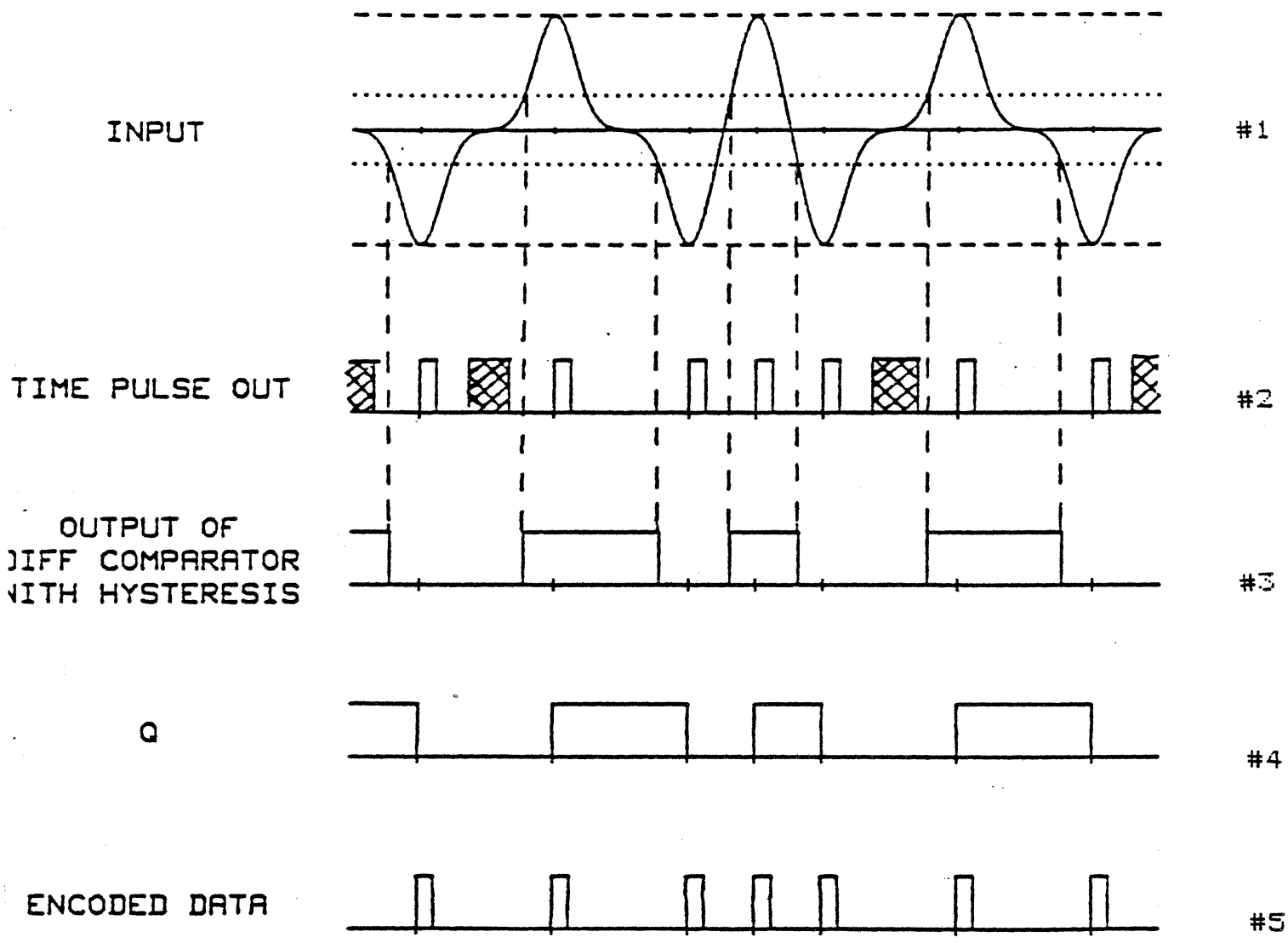
- Develop read/write circuitry that would work with twice the BPI of the present Wren II product
- Minimize circuitry and board area
  - Common read/write design for Wren III and Wren III slimline
- Minimize cost
- Utilize common industry parts where possible
- Maintain the same or added functionality with proven Wren and Lark designs
- Provide maximum head/media flexibility
- Improve vendor adaptability
- All positive supply, +12 or +5 VDC operation



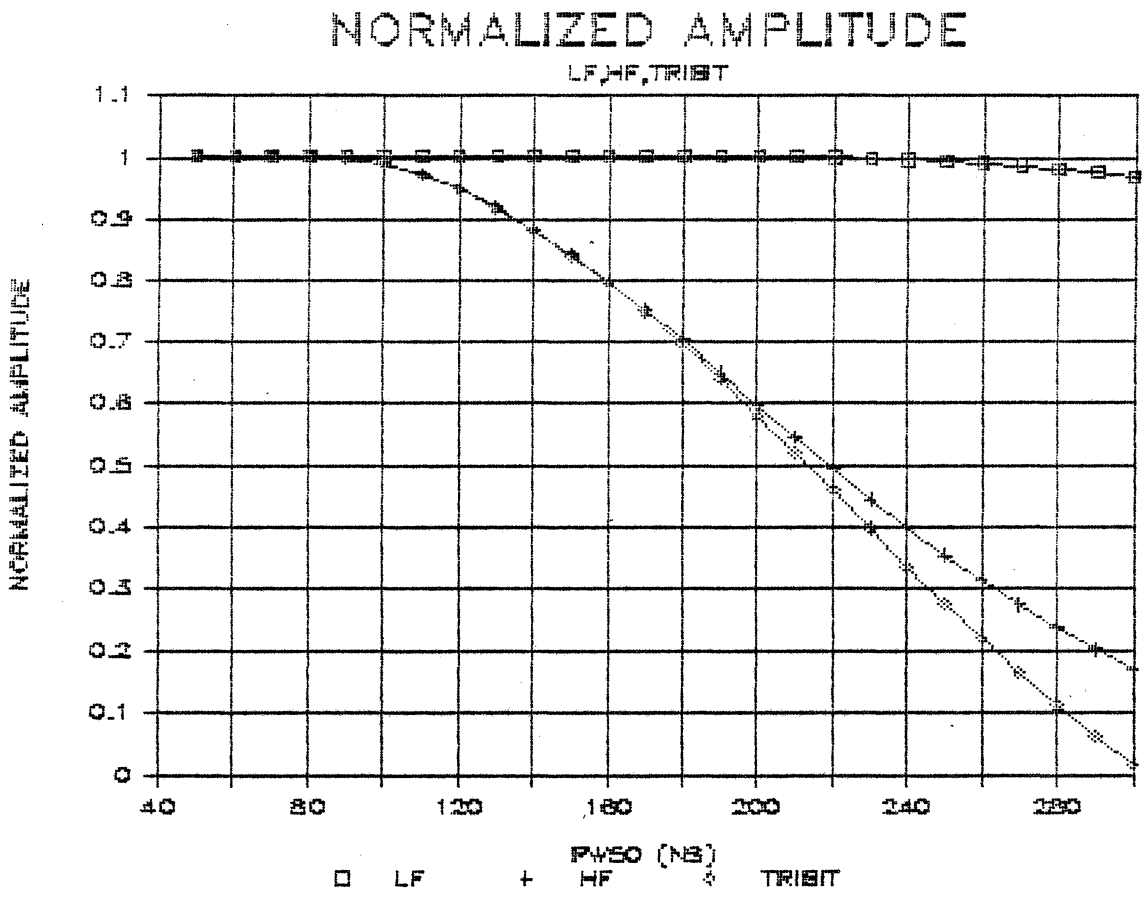
WREN III R/W BLOCK DIAGRAM



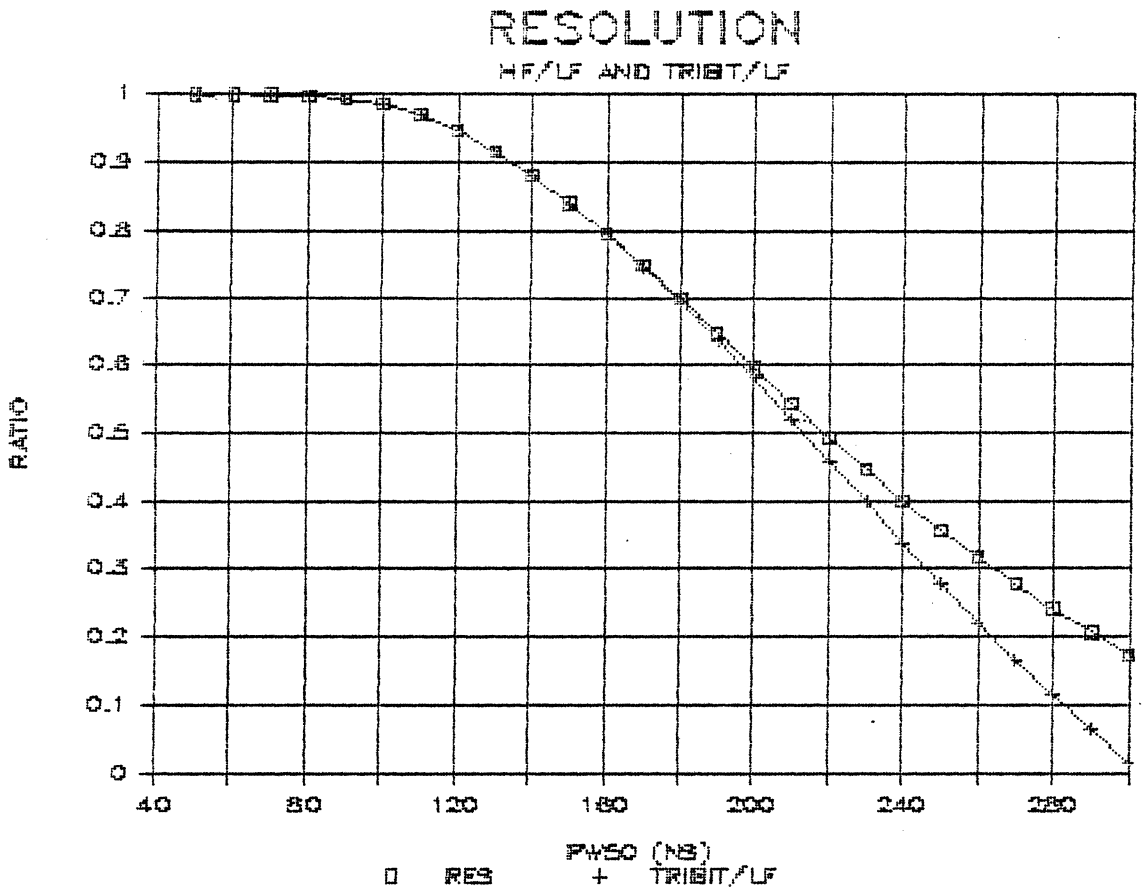
DP8464 DATA PULSE DETECTOR
BLOCK DIAGRAM



DP8464 TIMING DIAGRAM



NORMALIZED AMPLITUDE FOR LOW FREQUENCY (1.25 MHZ), HIGH FREQUENCY (3.33 MHZ) AND TRIBIT PATTERN AS A FUNCTION OF ISOLATED PULSE WIDTH



RESOLUTION (HF AMPL/LF AMPL) AND RATIO OF TRIBIT AMPLITUDE TO LF AMPLITUDE AS A FUNCTION OF ISOLATED PULSE WIDTH

MAJOR DESIGN FEATURES

- 2,7 ENCODING/DECODING
- SSI 117 PREAMP
- FIXED ADJUSTABLE PREAMP
- ADAPTIVE SLIMMING
- NATIONAL DP 8464

2,7 ENCODING/DECODING

ADVANTAGES:

- Reduces Flux Reversals Per Inch from 19,202 F.R.I. to 12,801 F.R.I. (Equivalent to 6.65 MHZ MFM)
- Industry Standard
- Better Error Propagation than Lark 2/9 Code (K + 3 bits)
- Implementable in Standard CMOS

RISKS:

- More Complex R/W LSI

ALTERNATIVES:

- Parts from National (DP 8462) and Adapter (AIC 270) Available this Year (T-TL Compatible)
- FSD ECL Encoder/Decoder Chip

SSI 117 PREAMP

ADVANTAGES:

- 6 Channel
- Low Cost of PLCC Quadpack Package
- +12, +5 V Operation
- Separate Write Data Input/Read Data Output
  - Better for write to read recovery
- Internal Write Data Flip Flop
  - Eliminates External Circuitry
- Internal Write Current Source
  - Eliminates External Circuitry
- High Gain

RISKS:

- Presently single sourced, although Cherry, Microcircuits, and Fairchild all have programs underway to second source this part
- Longer switching times than SSI 115
- Requires external damping resistors making flex layout difficult
- Limited functional tests have begun

ALTERNATIVES:

- Use SSI 115
- Use Flat Pack in Place of PLCC
- Other Flex Layouts Feasible

FIXED ADJUSTABLE PREAMP

ADVANTAGES:

- Allows Centering of AGC Range to Expected Head/Media Amplitudes

- Provides Output Drive for Slimming Circuitry

RISKS:

- None

DP 8464

ADVANTAGES:

- o Availability
  - Currently only real choice of read channel chip for this application
- o Standard Part
  - Projected less cost than custom LSI development
- o Flexible Architecture
  - Adaptable with the addition of more circuitry to a number of different architectures
- o Reduced Board Area
  - 300 mil narrow 24-pin dual-in-line package
- o Preliminary Tested Performance at 5 MHz

RISKS:

- o Single Source
- o Overall timing accuracy may not be sufficient for a 10 MHz transfer rate
- o Initial Cost

ALTERNATIVES:

- o Components can be added to improve performance
- o SSI plans a functionally equivalent part but not pin for pin compatible
- o Low cost Wren II design could be adapted with amplitude qualification

WREN III CHIPS OVERVIEW

DATA ENCODING/DECODING

NATIONAL 8462	2/7 ENDEC AVAILABLE 4TH QTR
ADAPTEC 270	2/7 ENDEC
FAIRCHILD uA2490	2/7 ENDEC/PLL AVAILABLE 4TH QTR

R/W PREAMP

SSI 117	FERRITE
SSI 5XX	TFH
FAIRCHILD uA248	FERRITE JULY 84

DATA PULSE DETECTION

MPI	
NATIONAL 8464	
SSI 540	NO AGC, NO AMPL QUALIFICATION
SSI 541	SAMPLES 4QTR 84

READ PHASE LOCK LOOP

MC1648	PRESENTLY USED
NATIONAL 8460	NO PROVISION FOR EARLY/LATE STROBE
OMTI 5070	DESIGNED FOR MFM
NATIONAL 8462	RLL VERSION OF 8460, UNANNOUNCED
MC1658	ALTERNATIVE TO MC1648, ELIMINATES VARACTORS

WREN III READ PLO

DESIGN GOALS

- TO BE ABLE TO LOCK TO CORRECT FREQUENCY (40 MHZ) WITHIN TIME ALLOWED DURING THE PLO SYNC FIELD ($\approx$ 5 μS).

- ONCE LOCKED THE READ CLOCK SHOULD HAVE 2 NS OR LESS JITTER AT THE PHASE DETECTOR.

JRV
1/18/85

WREN III READ PLO

THEORY OF OPERATION

THE "HEART" OF THE WREN III READ PLO IS THE MC1648, A VOLTAGE CONTROLLED OSCILLATOR. A TANK CIRCUIT SETS THE OPERATING FREQUENCY OF THE MC1648. THE TANK CIRCUIT CONTAINS 2 VOLTAGE VARIABLE CAPACITORS (VARACTOR DIODES), BY VARYING THE VOLTAGE ON THESE YOU VARY THE FREQUENCY OF THE MC1648. THE CONTROL VOLTAGE OF THE TANK CIRCUIT IS SET UP BY THE CHARGE PUMP WORKING WITH THE LOOP FILTER. THE AMOUNT OF CURRENT DELIVERED TO THE LOOP FILTER IS DETERMINED BY THE WIDE BAND ENABLE LINE, IF THE WIDE ENABLE IS ACTIVE THE CHARGE PUMP WILL DELIVER MORE CURRENT TO THE LOOP FILTER. THE LOOP FILTER IS THE VARIABLE COMPONENT IN THE PLO. THE TIME CONSTANTS OF THE PLO ARE DETERMINED BY THE COMPONENTS AND CONFIGURATION OF THE LOOP FILTER. THESE TIME CONSTANTS DETERMINE THE LOCK-UP TIME OF THE PLO AS WELL AS THE STABILITY OF THE PLO.

THE EARLY STROBE AND THE LATE STROBE ARE IMPLEMENTED IN THE CHARGE PUMP ALSO. THESE TWO SIGNALS EFFECTIVELY DELAY OR ADVANCE THE EDGES OF THE VCO OUTPUT. THE OUTPUT OF THE VCO OR READ CLOCK FOR WREN III IS 40 MHZ. THIS 40 MHZ READ CLOCK IS DIVIDED BY 2 AND THEN PHASE COMPARED WITH THE READ DATA, WHICH IS THE FUNCTION OF THE PHASE DETECTOR. THE PHASE DETECTOR'S OUTPUT IS EITHER A FREQUENCY INCREMENT OR DECREMENT PULSE. THESE TWO SEPARATE LINES GO TO THE CHARGE PUMP AND CONTROL ITS CURRENT SWITCHING FUNCTION.

JRV
1/18/85

WREN III READ PLO

REASONS FOR DECISIONS/RISKS AND ALTERNATIVES

THE REASON FOR CHOOSING THE CONFIGURATION PROPOSED FOR THE WREN III, PRIMARILY, IS THAT WE HAVE PREVIOUS EXPERIENCE WITH THE CIRCUIT. OTHER THAN A FEW COMPONENT VALUE CHANGES THE CIRCUIT IS IDENTICAL TO THE PLO USED ON THE WREN II ESDI.

THE MC1648 HAS 2 SOURCES, ALTHOUGH, ONE DOES NOT PRODUCE AS GOOD A PRODUCT AS THE OTHER, BOTH SOURCES ARE USABLE. ANOTHER VCO COULD BE USED, THE MC1658, BUT BOTH THE CHARGE PUMP AND LOOP FILTERS WOULD HAVE TO BE CHANGED. THESE CHANGES WOULD TAKE A LOT OF DEVELOPMENT TIME TO GET TO A FUNCTIONAL CIRCUIT.

JRV
1/18/85

WREN III READ PLO

CURRENT STATUS

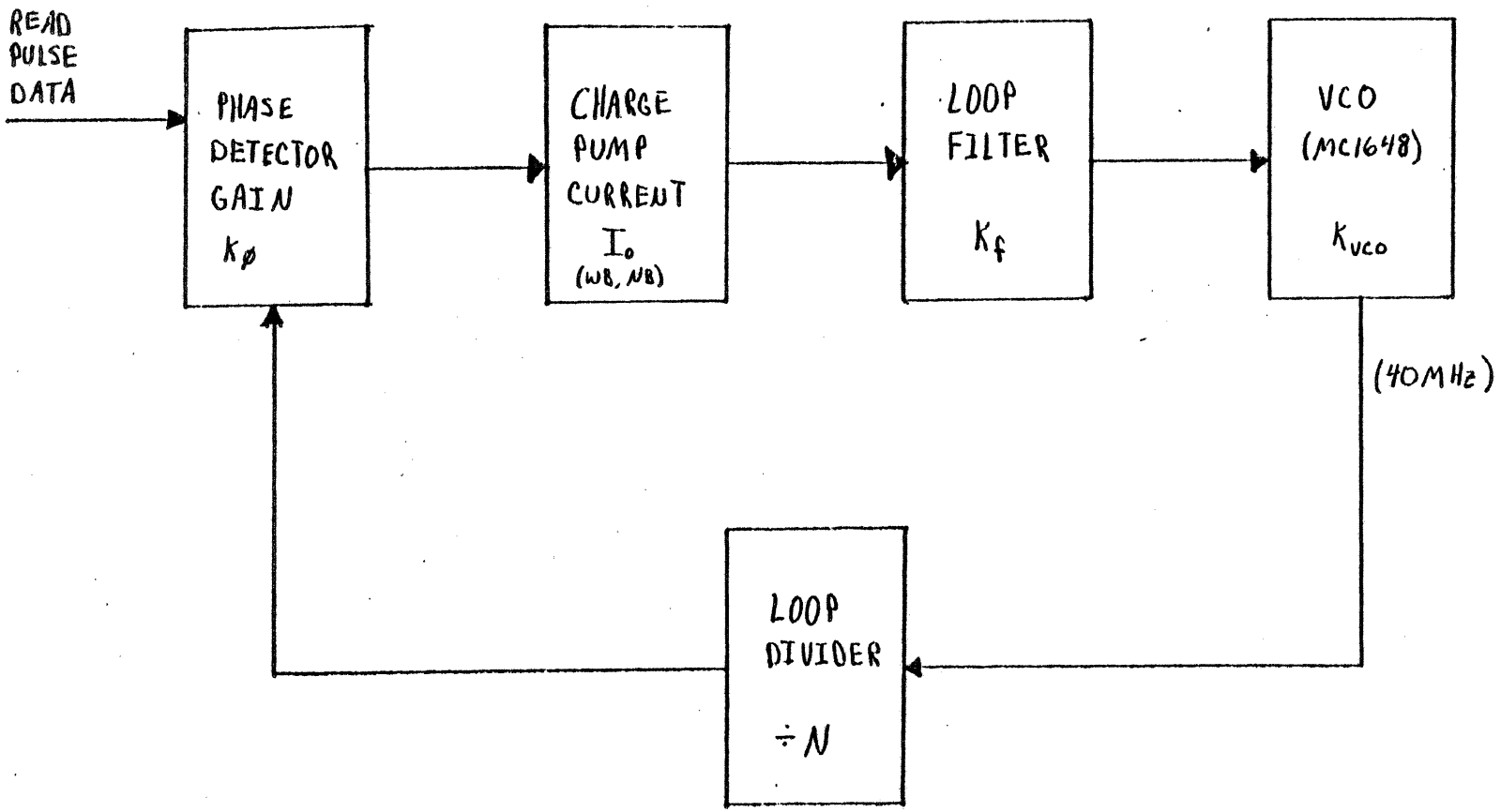
- WREN II ESDI MODIFIED TO RUN WITH MC1648 GOING 40 MHZ. IT EASILY READS ALL PATTERNS. AND, CLOCK JITTER AT THE PHASE DETECTOR IS NOT MEASURABLE WITH AN OSCILLOSCOPE (LESS THAN 2 NS OF JITTER).

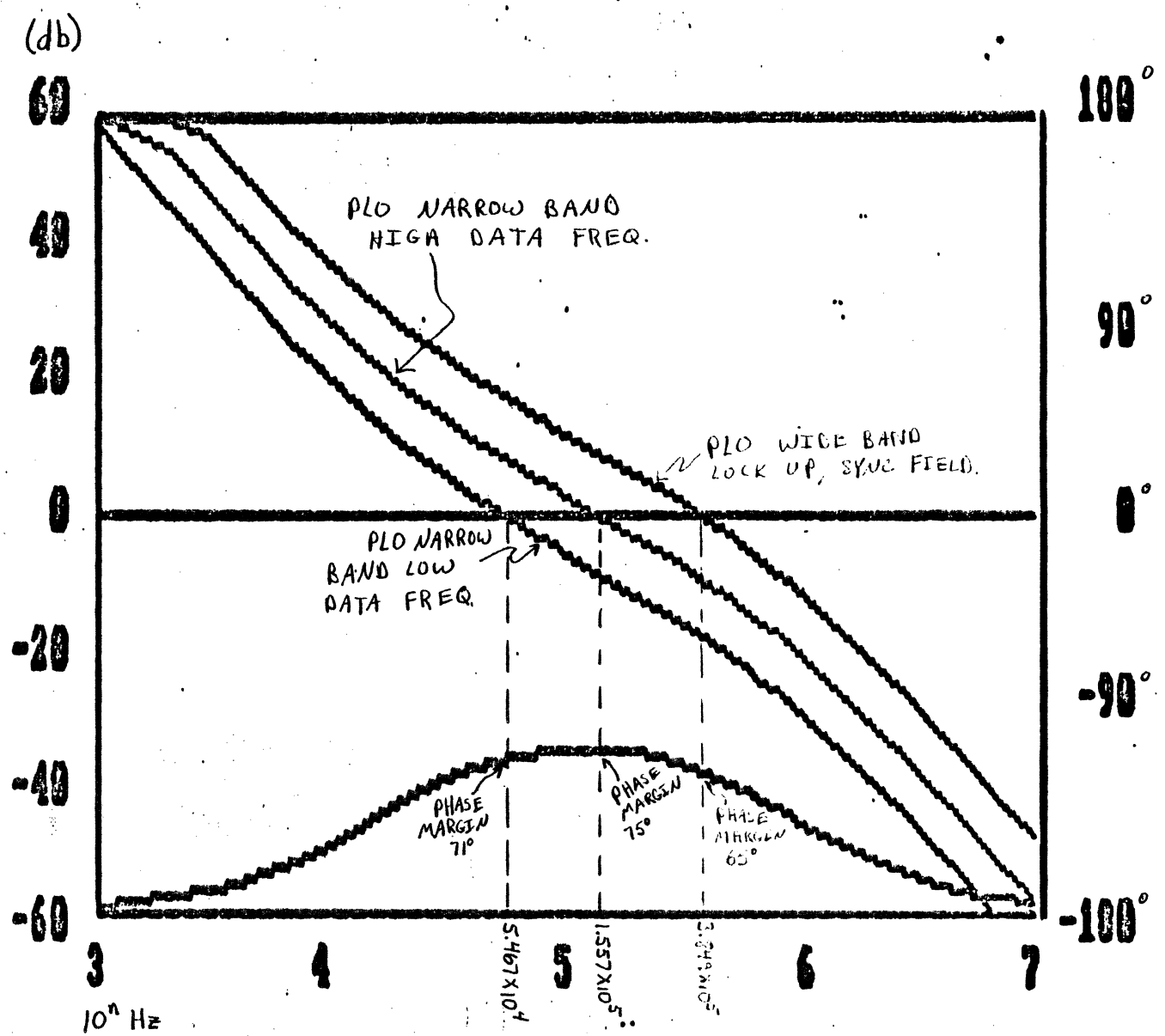
- SCHEMATICS HAVE BEEN INPUT, READY FOR PROTOTYPE CIRCUITS TO BE BUILT, (WHEN PROTOTYPE DATA BOARDS ARE BUILT).

JRV
1/18/85

WREN III READ PLO BLOCK DIAGRAM.

JRU(01/18/85)





WREN III READ PLO OPEN LOOP GAIN/PHASE PLOTS

JRV(01/18/85)

WREN III Read PLO open Loop Gain/Phase values

Narrow Band

2.5 MHz (L.F.)

T1 = 3.3E-08
T2 = .0000101
T3 = 1.69E-07
VCO GAIN CONSTANT = 2.5E+07
PHASE DET. GAIN = 8.557E-05
LOOP DIVIDER = 2
0 db FREQUENCY = 54670
PHASE MARGIN @ 0 db FREQUENCY = 71

FREQUENCY	GAIN(db)	PHASE	NOISE RESPONSE(db)
1000	58.3046	-176.4297	-58.29407
2000	46.31534	-172.8884	-46.27358
3000	39.35689	-169.4035	-39.26447
4000	34.47587	-166.0002	-34.31529
5000	30.74484	-162.6999	-30.5011
6000	27.7489	-159.5201	-27.40986
7000	25.26514	-156.4741	-24.82181
8000	23.15915	-153.5707	-22.60568
9000	21.34316	-150.8151	-20.67675
10000	19.75637	-148.2091	-18.97712
20000	10.41186	-129.4511	-8.91029
30000	5.848525	-119.5359	-4.641045
40000	2.914706	-113.934	-2.604459
50000	.7568148	-110.5318	-1.538311
60000	-.9537583	-108.3609	-.9284151
70000	-2.37402	-106.9375	-.5521685
80000	-3.590532	-105.9987	-.3055012
90000	-4.656019	-105.3902	-.1357677
100000	-5.604992	-105.0163	-1.437038E-02
200000	-11.84813	-106.4949	.3612457
300000	-15.61304	-110.6765	.4074929
400000	-18.4176	-115.269	.4002332
500000	-20.7164	-119.7703	.3761339
600000	-22.70244	-124.0063	.3460119
700000	-24.47289	-127.913	.3145234
800000	-26.08233	-131.4759	.2839801
900000	-27.56419	-134.7046	.2555246
1000000	-28.94053	-137.6212	.2296461
2000000	-39.0948	-155.237	8.788412E-02
3000000	-45.67705	-162.8731	4.327513E-02
4000000	-50.50078	-166.9775	2.529682E-02
5000000	-54.29431	-169.5139	1.648834E-02
6000000	-57.41587	-171.2303	1.156592E-02
7000000	-60.06595	-172.4667	8.550455E-03
8000000	-62.36751	-173.399	6.572084E-03
9000000	-64.40113	-174.1267	5.207714E-03
1E+07	-66.22249	-174.7103	4.226244E-03

WREN III Read PLO open Loop
Gain/Phase values

Narrow Band

6.67 MHz (H.F.)

T1 = 3.3E-08
T2 = .0000101
T3 = 1.69E-07
VCO GAIN CONSTANT = 2.5E+07
PHASE DET. GAIN = 2.2833E-04
LOOP DIVIDER = 2
0 db FREQUENCY = 155700
PHASE MARGIN @ 0 db FREQUENCY = 75

FREQUENCY	GAIN(db)	PHASE	NOISE RESPONSE(db)
1000	66.82944	-176.4297	-66.82549
2000	54.84017	-172.8884	-54.82455
3000	47.88172	-169.4035	-47.8472
4000	43.0007	-166.0002	-42.94085
5000	39.26967	-162.6999	-39.17904
6000	36.27374	-159.5201	-36.148
7000	33.78997	-156.4741	-33.62594
8000	31.68398	-153.5707	-31.47958
9000	29.86799	-150.8151	-29.62216
10000	28.2812	-148.2091	-27.9938
20000	18.93669	-129.4511	-18.32759
30000	14.37335	-119.5359	-13.65776
40000	11.43953	-113.934	-10.75613
50000	9.281645	-110.5318	-8.711853
60000	7.57107	-108.3609	-7.168339
70000	6.150808	-106.9375	-5.953669
80000	4.934296	-105.9987	-4.971982
90000	3.868811	-105.3902	-4.163947
100000	2.919839	-105.0163	-3.489934
200000	-3.3233	-106.4949	-.3258158
300000	-7.088211	-110.6765	.5391018
400000	-9.892772	-115.269	.8135611
500000	-12.19157	-119.7703	.8811168
600000	-14.17761	-124.0063	.8642483
700000	-15.94806	-127.913	.8119369
800000	-17.5575	-131.4759	.7464928
900000	-19.03936	-134.7046	.6786518
1000000	-20.4157	-137.6212	.6135493
2000000	-30.56997	-155.237	.2360661
3000000	-37.15222	-162.8731	.1159097
4000000	-41.97595	-166.9775	6.765435E-02
5000000	-45.76948	-169.5139	4.406282E-02
6000000	-48.89104	-171.2303	3.089532E-02
7000000	-51.54112	-172.4667	2.283184E-02
8000000	-53.84268	-173.399	1.754769E-02
9000000	-55.87631	-174.1267	1.390099E-02
1E+07	-57.69766	-174.7103	1.128171E-02

WREN III Read PLO open Loop Gain/Phase values

Wide Band 6.67 MHz (PLL sync field)

T1 = 3.3E-08
T2 = .0000101
T3 = 1.69E-07
VCO GAIN CONSTANT = 2.5E+07
PHASE DET. GAIN = 6.7437E-04
LOOP DIVIDER = 2
0 db FREQUENCY = 384900
PHASE MARGIN @ 0 db FREQUENCY = 65

FREQUENCY	GAIN(db)	PHASE	NOISE RESPONSE(db)
1000	76.23614	-176.4297	-76.2348
2000	64.24688	-172.8884	-64.24159
3000	57.28842	-169.4035	-57.27675
4000	52.4074	-166.0002	-52.38718
5000	48.67638	-162.6999	-48.64579
6000	45.68044	-159.5201	-45.63804
7000	43.19668	-156.4741	-43.14141
8000	41.09068	-153.5707	-41.02188
9000	39.27469	-150.8151	-39.19199
10000	37.68791	-148.2091	-37.59123
20000	28.3434	-129.4511	-28.13357
30000	23.78006	-119.5359	-23.51311
40000	20.84624	-113.934	-20.55261
50000	18.68835	-110.5318	-18.38226
60000	16.97778	-108.3609	-16.66651
70000	15.55751	-106.9375	-15.24534
80000	14.341	-105.9987	-14.03075
90000	13.27552	-105.3902	-12.96931
100000	12.32655	-105.0163	-12.02613
200000	6.083407	-106.4949	-5.92655
300000	2.318494	-110.6765	-2.512143
400000	-.4860669	-115.269	-.3616569
500000	-2.784867	-119.7703	.9367254
600000	-4.770909	-124.0063	1.627087
700000	-6.541351	-127.913	1.917602
800000	-8.150793	-131.4759	1.973493
900000	-9.63266	-134.7046	1.90639
1000000	-11.00899	-137.6212	1.782843
2000000	-21.16327	-155.237	.7119224
3000000	-27.74552	-162.8731	.3464404
4000000	-32.56925	-166.9775	.2012721
5000000	-36.36277	-169.5139	.130772
6000000	-39.48433	-171.2303	9.156383E-02
7000000	-42.13442	-172.4667	6.760735E-02
8000000	-44.43597	-173.399	5.192822E-02
9000000	-46.4696	-174.1267	4.112091E-02
1E+07	-48.29096	-174.7103	3.336066E-02

2,7 ENCODER/DECODER

L DESIGN GOALS

A. LOWEST POSSIBLE RISK FOR FIRST TIME IMPLEMENTATION OF 2,7.

B. TAKE ADVANTAGE OF PREVIOUS LARK & CMD DESIGNS WITH 2,9 CODE AND 10 MHZ TRANSFER RATE. (ESPECIALLY ON SUBTILITIES OF PLO CONTROL)

C. IMPLEMENT HIGH SPEED SYNCHRONOUS LOGIC CAPABLE OF 15 MHZ TRANSFER (TO GIVE ADDITIONAL CONFIDENCE OF WORSE CASE OPERATION AT 10 MHZ DESPITE UNFORESEEN PLO PROBLEMS).

D. NOTE: REASONS FOR 2,7 OVER 2,9:

LOWER PLO AND FILTER DRIFT TIME, LOWER ERROR PROPAGATION, SLIGHTLY LESS LOGIC.

RISKS

- BREADBOARD CIRCUITS NOT YET TESTED IN A DRIVE.
- LSI SCHEDULE - AVAILABILITY OF PROTOTYPES.

ALTERNATIVES

- NATIONAL 2,7 ENCODE/DECODE CHIP

  REQUIRES CONSIDERABLE EXTERNAL LOGIC FOR ADAPTIVE SLIMMING CONTROL.

  SAMPLES NOT YET AVAILABLE.

STATUS

I. BREADBOARD AND DEBUGGER COMPLETE. ENCODER SEEMS FULLY FUNCTIONAL. DECODER NOT TESTED.

II. SCHEMATICS FOR LSI HAVE BEEN COMPLETED AND MOSTLY ENTERED AS GATE ARRAY NET LISTS. SIMULATION CAN BEGIN SOON.

SH
2/6/85

ADDRESS MARK DETECTION

A. AN ADDRESS MARK WILL APPEAR AS 27 BITS OF NO FLUX REVERSALS (COUNT = 26.5 NOMINAL) DURING READBACK.

B. THE BEGINNING OF THE A.M. VARIES ± 2 BITS DUE TO PHASE OF LAST 2,7 FR DURING WRITING. DURING READBACK, IT MAY ALSO BE LENGTHENED BY A DROPOUT OR SHORTENED BY A DROP-IN (ALLOW ANOTHER +3/-2 BITS).

C. THE END OF THE A.M. VARIES DUE TO DROP-INS/DROP-OUTS DURING READ-BACK (ALLOW ANOTHER +3/-2).

D. SENSITIVITY TO DROP-INS IS REDUCED AFTER THE A.M. IS VALID (NO F.R. FOR 6 BITS). AGC IS ALSO DISABLED THEN.

2,7 ENCODER: THEORY OF OPERATION

I. DATA RETIMER - (SAME AS LARK, WREN II)

CAREFULLY RETIMES DATA TO WRITE CLOCK THEN SERVO CLOCK.

II. NRZ SHIFT REGISTER - HOLDS 5 BITS (Q_A TO Q_E) FROM ABOVE.

III. ENCODER - COMBINATIONAL LOGIC TO GENERATE 2,7 CODE BASED ON ABOVE 5 NRZ BITS AND TIME REFERENCE FROM 2 BIT COUNTER. (NOTE: ENCODE IS TIMED WITH QC).

A. ENCODE TABLE FOR EVEN (FIRST) FLUX REVERSAL SITE:

NRZ →	REVERSAL	(QA – QE)	COUNTER	PR	REDUCE LOGIC
00	10 00	(X00XX)	0	0	
101	10 0X 00	(101XX)	0	0	
100	00 10 00	(X001X)	1	0	
1101	00 10 0X 00	(1011X)	1	0	
1100	00 00 10 00	(X0011)	2	0	
PREAMBLE	10 0X 00	(—)	0	1	

B. ENCODE TABLE FOR ODD (DELAYED) FLUX REVERSAL SITE:

NRZ →	REVERSAL	(QA-QE)	COUNTER	PR	REDUCE LOGIC
01	01 00	(X10XX)	0	0	
101	X0 01 00	(X101X)	1	X	
111	00 01 00	(X111X)	1	X	
1101	00 X0 01 00	(X1011)	0 OR 2	0	
PREAMBLE	X0 01 00	(—)	1	1	

C. END OF FRAME (USED FOR COUNTER SYNCHRONOUS RESET):

NRZ	(QA — QE)	COUNTER	PR
00 , 01	(XXX0X)	1 (OR 3)	0
100 , 101	(XXX01)	2 (OR 3)	X
111	(XX111)	2 (OR 3)	X
PREAMBLE	(—)	2 (OR 3)	1

IV. FINAL RETIMER - PUTS 2 FLUX REVERSAL SITES OUT AT PROPER TIMES

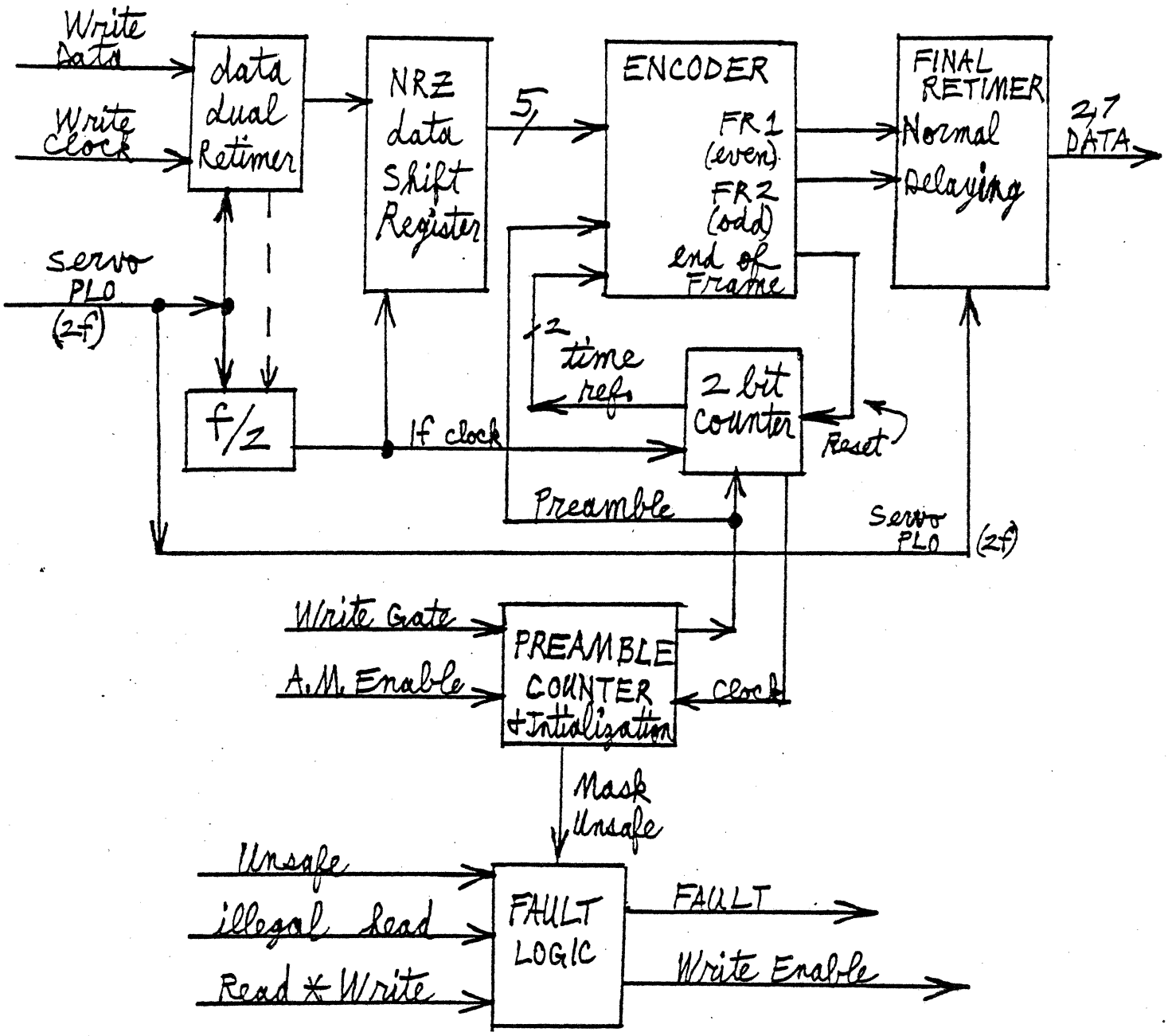
V. PREAMBLE COUNTER/INITIALIZATION CONTROL - LOCKED TO BIT COUNTER TO GENERATE ALMOST 8 BYTES OF HIGHEST FREQUENCY FLUX REVERSALS FOR MORE RELIABLE PLO SYNC.

VI. WRITE FAULT LOGIC:

A. UNSAFE GENERATES A WRITE FAULT IF PRESENT ANYTIME AFTER 8 BYTES OF WRITING.

B. ALSO GENERATES WRITE FAULT WITH AN ILLEGAL HEAD OR READ-GATE WHILE WRITING.

ENCODER BLOCK DIAGRAM



2,7 DECODER: THEORY OF OPERATION

I. PLO CONTROL/RETIMED PULSE DATA - STILL DONE IN AN ECL CHIP TO MAINTAIN SUB-NANOSECOND RESOLUTION ERRORS ON INCOMING PULSES (EVEN MORE CRITICAL AT 10 MHZ THAN 5).

II. DATA SHIFT REGISTER - SHIFTS 4 EARLY AND 4 LATE FLUX REVERSALS AT EACH NEW BIT DECODE TIME.

III. DECODER - COMBINATIONAL LOGIC TO DECODE 2,7 FLUX REVERSALS.

$\overline{\text{NRZ DATA}} = S_6 + S_{7A} + S_{7B}$

$S_{7B} = (Qe + Qf + Qg + Qh)*Qc$

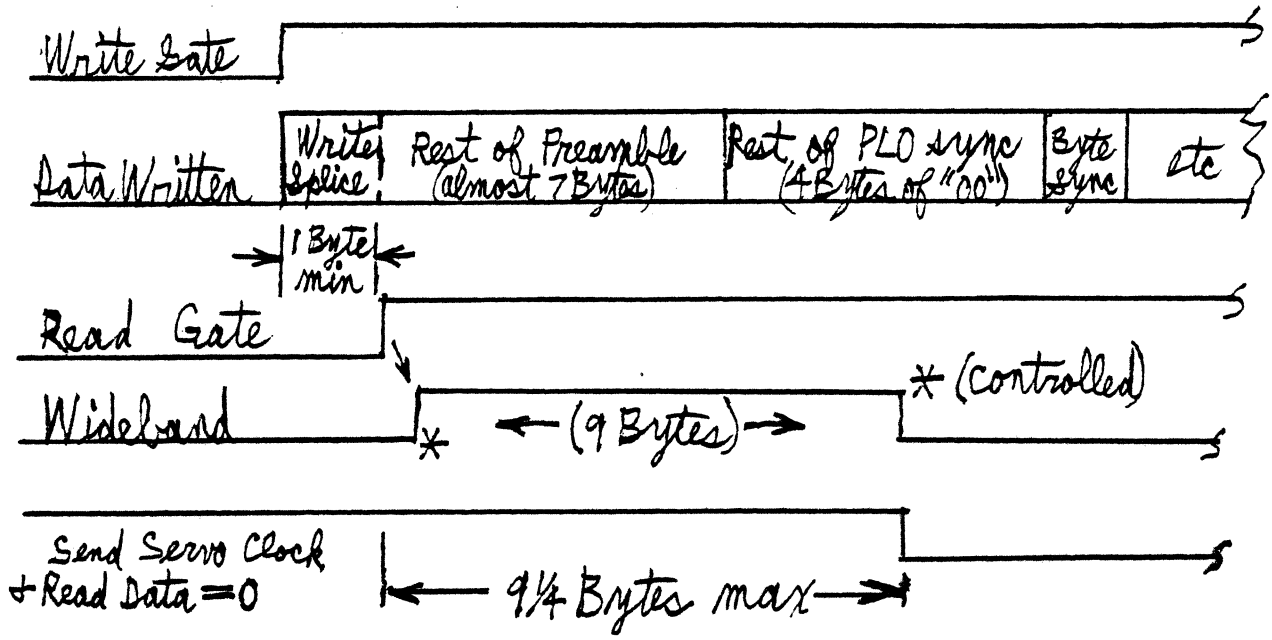
DECODER	Qa	Qb	Qc	Qd	Qe	Qf	Qg	Qh
S_6	0	0	0	1				
S_{7A}			0	0	0	1		
S_{7B}			1		Z	Z	Z	Z
	—	—	—	—	—	—	—	—
BAD SYNC	1	0		0	1	0		0

"BAD SYNC" CAUSES DECODE TIME OF PLO/2 TO SHIFT ONE FR SITE LATER. (ONLY DURING PLO SYNC FIELD - TO GET PROPER DECODE OF CUSTOMER'S ALL "00").

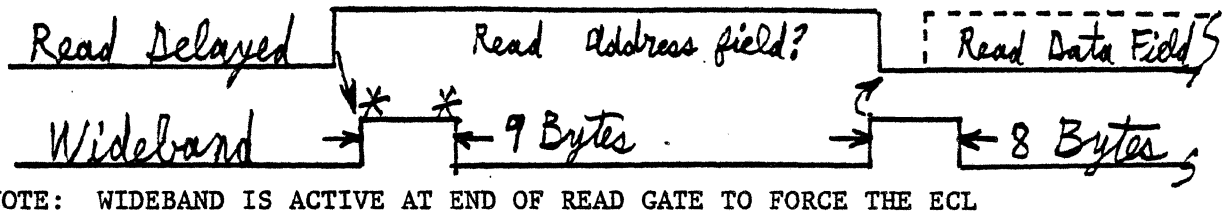
IV. INITIALIZER/TIMER

A. GENERATES PLO SYNC TIMING PER BELOW:

(WRITING OF ENCODER PREAMBLE IS FOR INFO. ONLY).



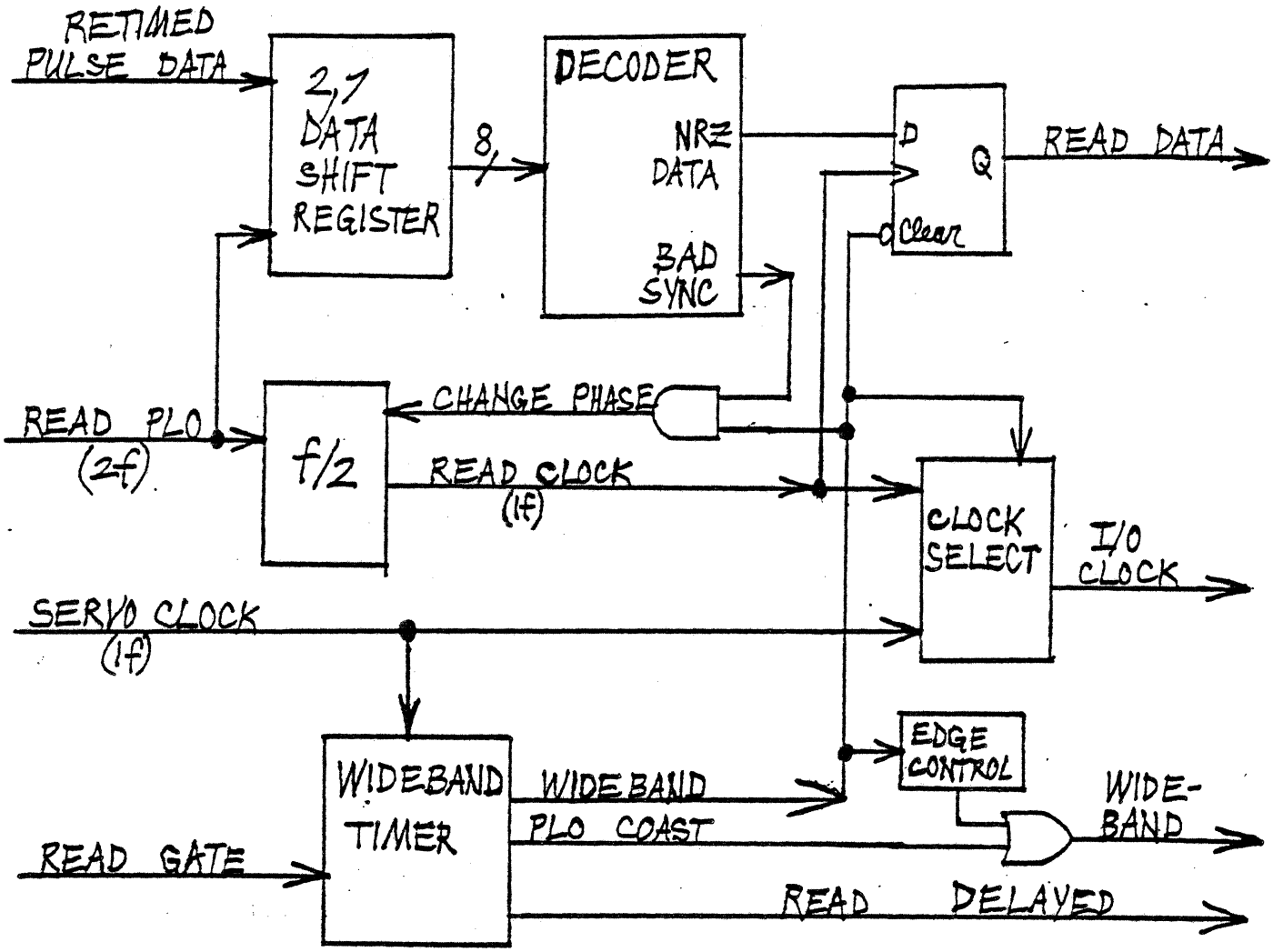
B. TIMING OF "READ DELAYED" FOR PLO CONTROL



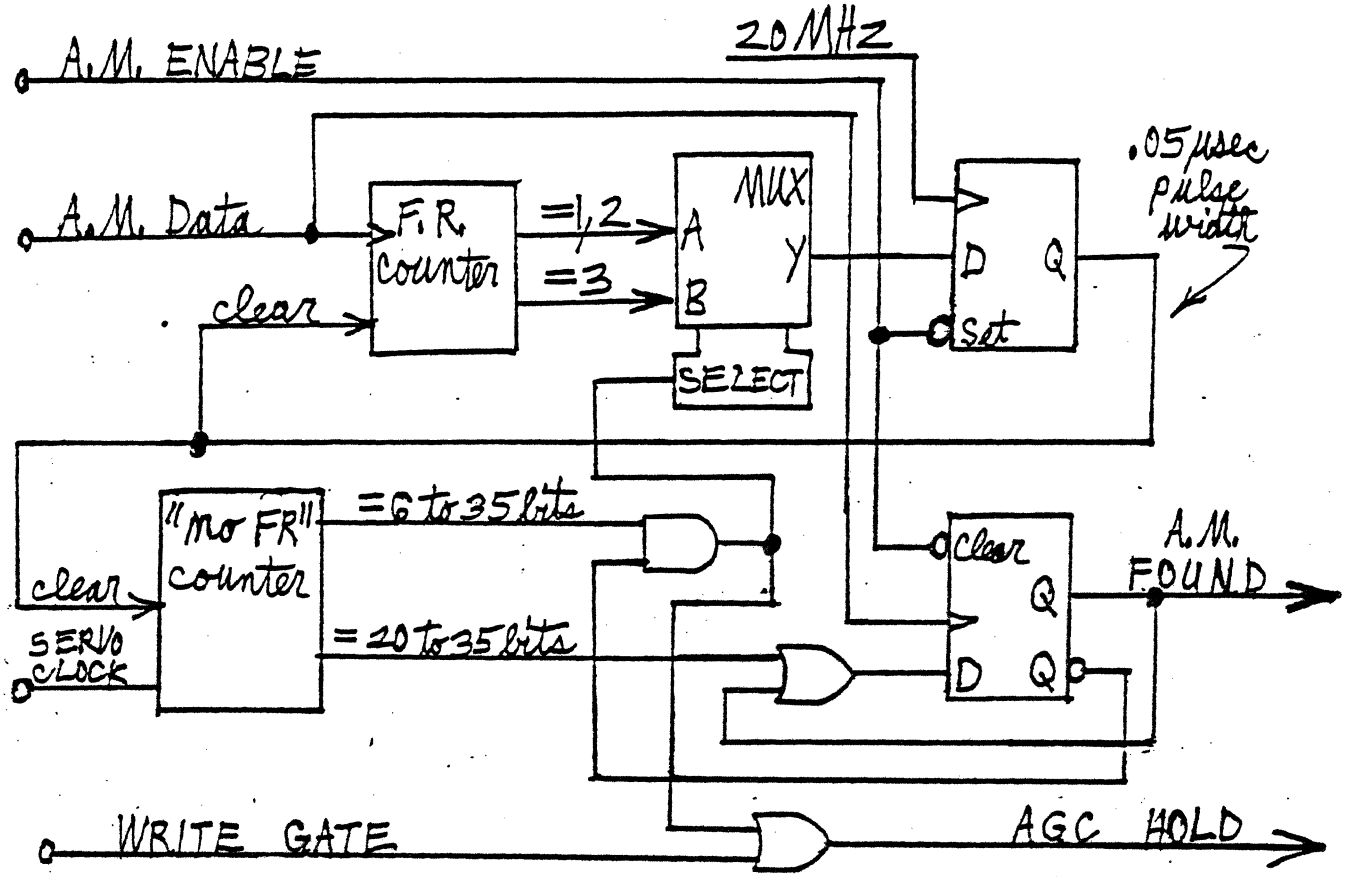
NOTE: WIDEBAND IS ACTIVE AT END OF READ GATE TO FORCE THE ECL CHIP TO COAST (NO FREQ "UP" OR "DOWN" TO THE READ PLO). THIS IS A "COVER UP" FOR AN UNLOCK PROBLEM IN THE SYSTEM THAT LOCKS THE READ PLO TO THE SERVO PLO. THIS WILL NOT COVER THE "PROBLEM" FOR CUSTOMERS THAT RE-ACTIVATE READ GATE ABOUT 9 TO 10 BYTES LATER (AS IN READING A DATA FIELD AFTER AN ADDRESS FIELD.)

SH
2/6/85

DECODER BLOCK DIAGRAM



ADDRESS MARK DETECTION



WREN III FLEX CIRCUIT

OVERVIEW

- USE SSI117-6 FOR DATA TRANSFER
- USE TI592B FOR SERVO READ
- USE SAME HARDWARE AS WREN II
- DATA CHIP AS CLOSE TO HEADS AS POSSIBLE FOR NOISE IMMUNITY.
- MAYBE USED AS A THREE DISK SINGLE CHIP FLEX

PRESENT STATUS

- LAYOUT OF ARTWORK IN DRAFTING
- ALL COMPONENTS FOR IN-HOUSE PROTOTYPES HAVE BEEN RECEIVED. (I.E. 117'S 750Ω CHIP RES., 110Ω CHIP, 10KΩ & .01UF).
- 117 CHIPS HAVE BEEN USED FOR RIGID DISK DATA TRANSFER.

1/18/85

WREN III FLEX CIRCUIT

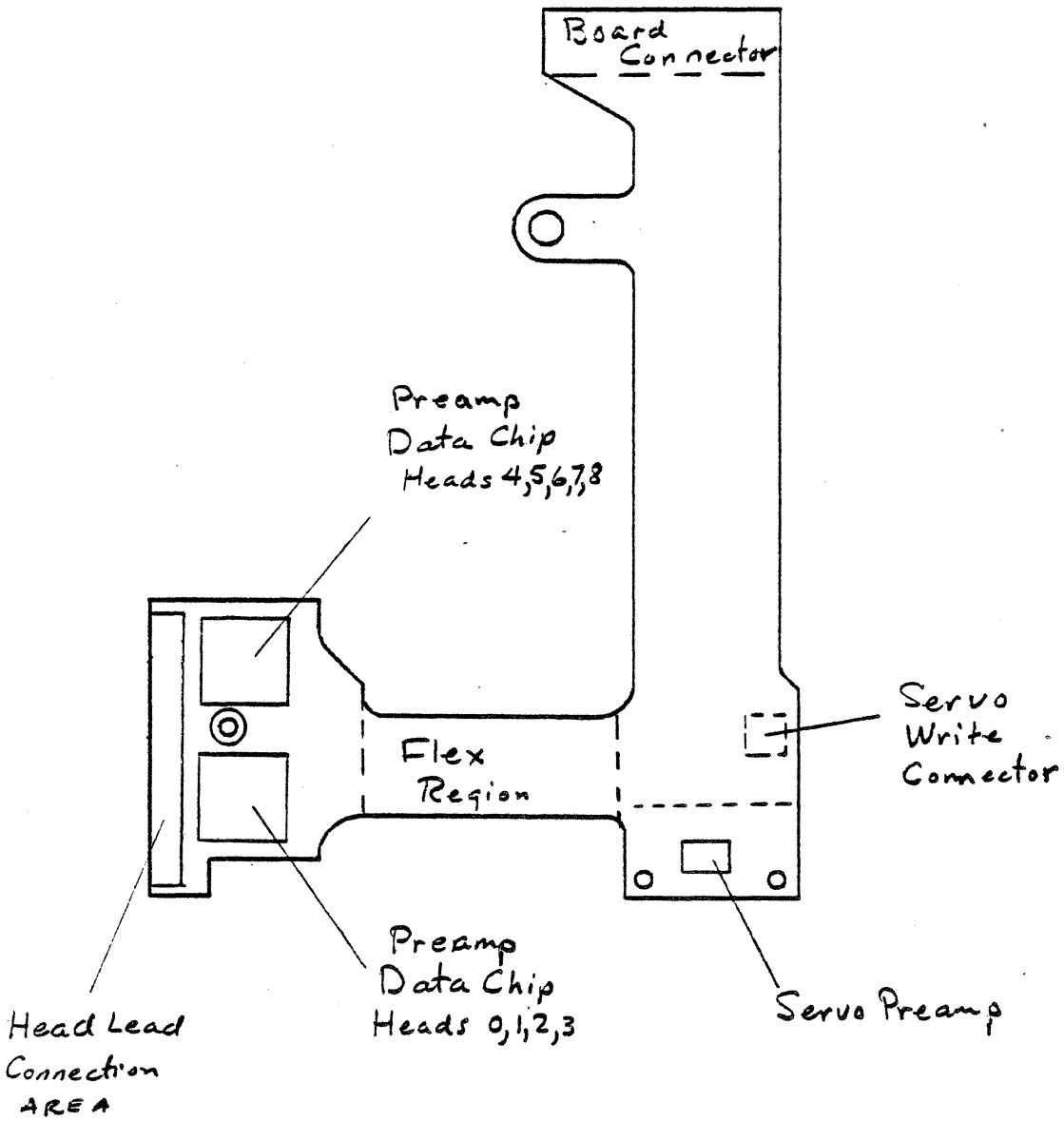
RISK & CONCERNS

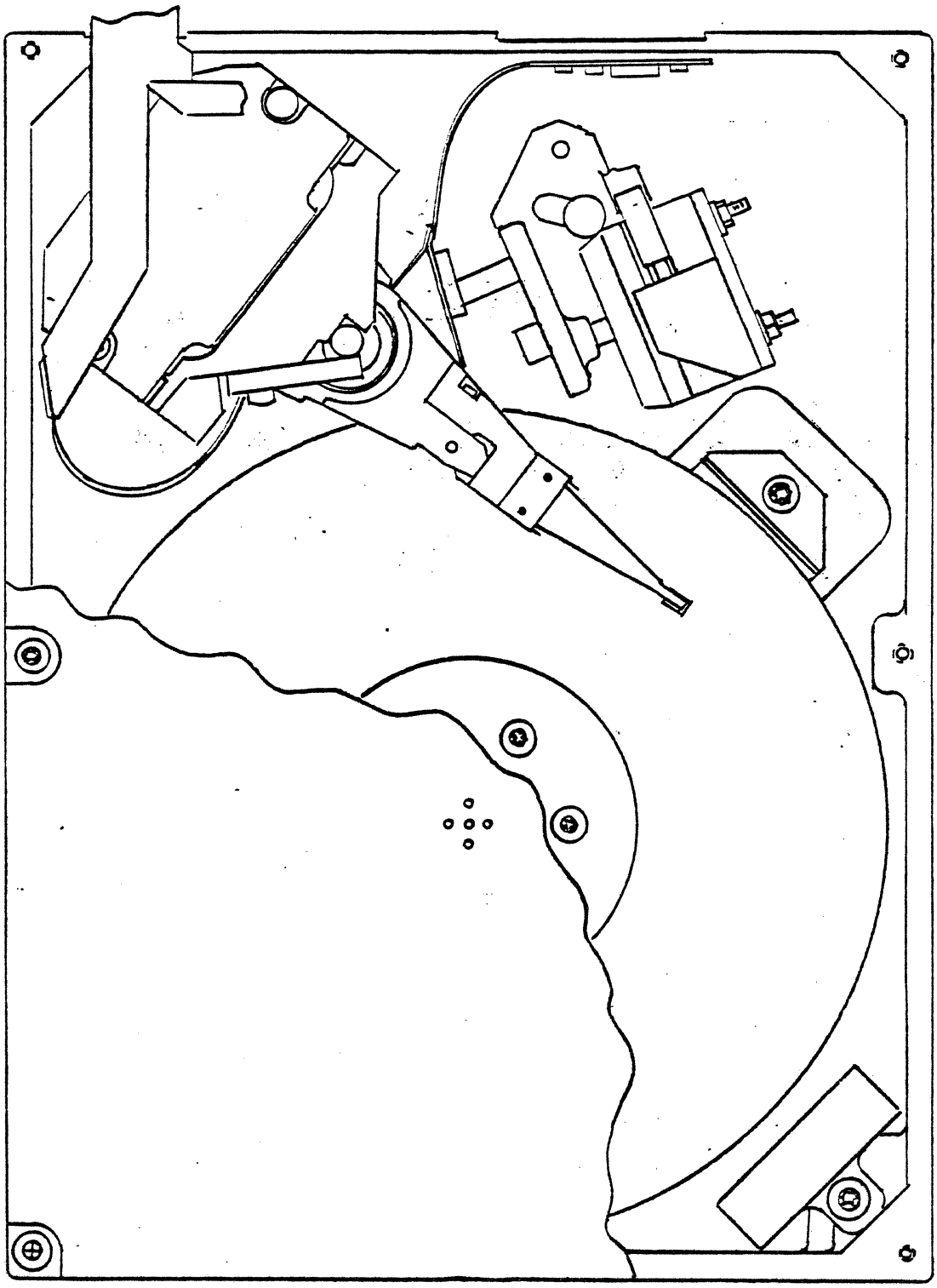
- RESISTORS MOUNTED ON HEAD LEADS
- STIFFENER ON ROTARY IS LARGER AND ANGLED FOR CLEARANCE
- MAY HAVE HIGH BIAS FORCE
- OSCILLATION MAY BE PROBLEM
- 117 CHIPS HAVE TWO DIFFERENT ORIENTATIONS
- NON-USED PINS AND RUNS INSULATED ONLY BY COVER FILM
- SSI SOLE SUPPLIER AT PRESENT
  (CHERRY, FAIRCHILD, MICROCIRCUITS NATIONAL TO SOON HAVE CHIPS AVAILABLE).

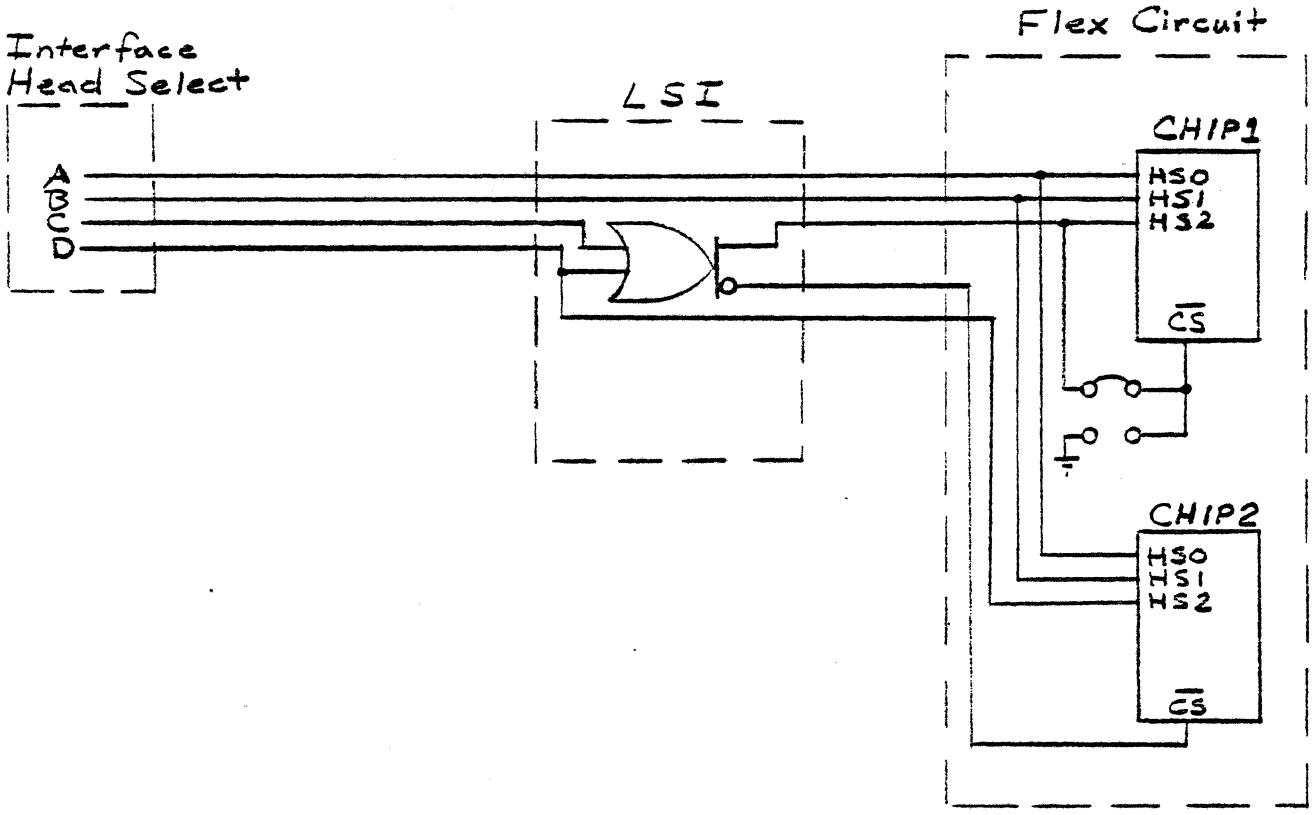
POSSIBLE REDUCTIONS OF RISK

- HYBRID WITH RESISTORS IN CHIP FROM MICROCIRCUITS AND SSI (POSSIBLY).
- IMPROVED PINOUT FROM SSI
- NEW LAYOUT OF FLEX WITH DATA CHIPS NOT ON THE ROTARY ARM.
- NEW LAYOUT OF FLEX WITH DATA AND SERVO CHIPS ON ROTARY ARM WITH FOLDED FLEX.

1/18/85


Board Connector
Preamp Data Chip Heads 4,5,6,7,8
Flex Region
Servo Write Connector
Preamp Data Chip Heads 0,1,2,3
Servo Preamp
Head Lead Connection AREA





Head Selected	Interface A	B	C	D	CHIP 1 HS0	HS1	HS2	CS	CHIP 2 HS0	HS1	HS2	CS
0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	0	1	0	0	1
2	0	1	0	0	0	1	0	0	0	1	0	1
3	1	1	0	0	1	1	0	0	1	1	0	1
4	0	0	1	0	0	0	1	1	0	0	0	0
5	1	0	1	0	1	0	1	1	1	0	0	0
6	0	1	1	0	0	1	1	1	0	1	0	0
7	1	1	1	0	1	1	1	1	1	1	0	0
8	0	0	0	1	0	0	1	1	0	0	1	0

WREN III ARCHITECTURE

DESIGN GOALS

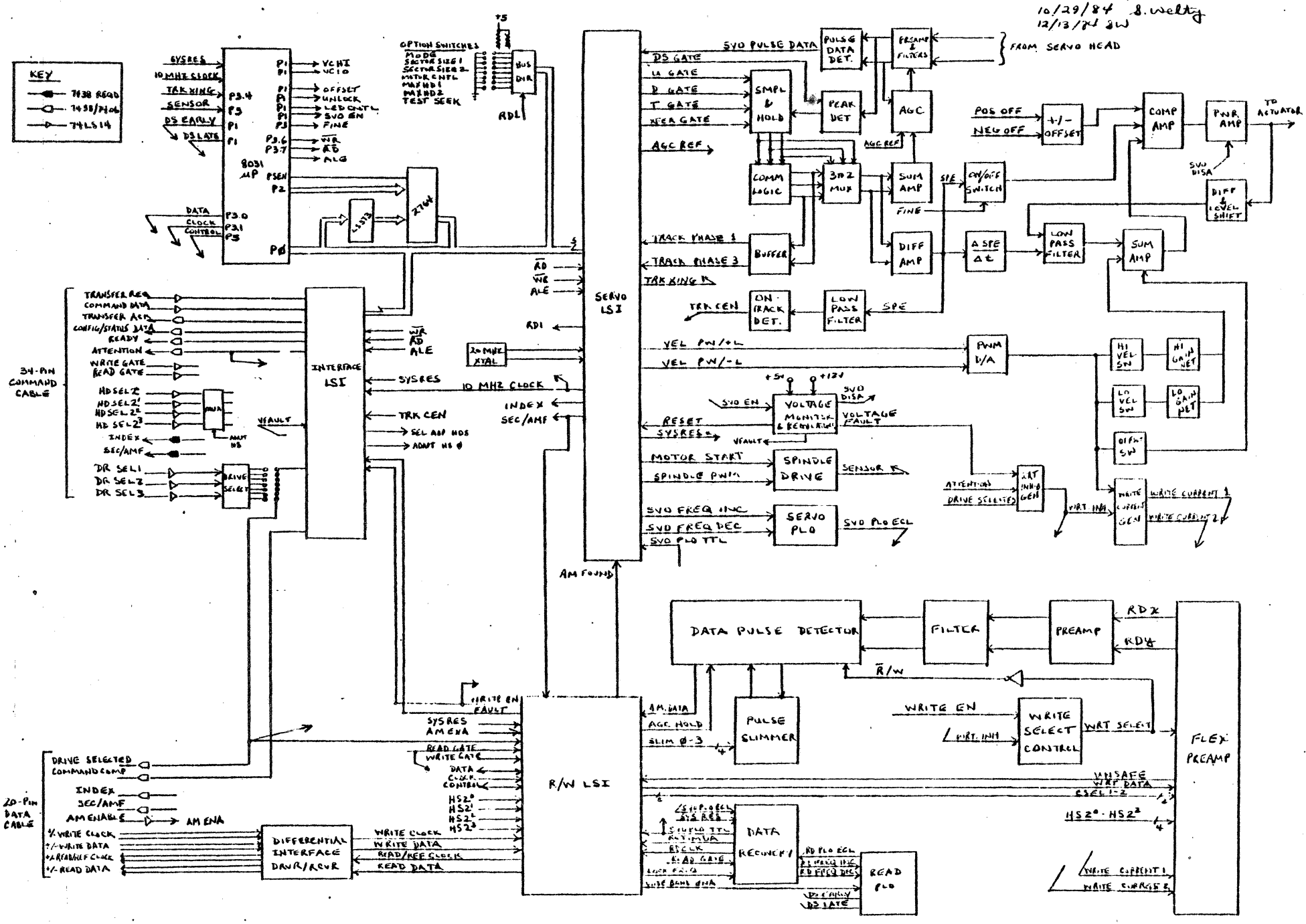
- HAVE THE DRIVE UPROC "READ" DATA WRITTEN ON THE DRIVE DURING MANUFACTURING AND USE THIS DATA TO CALCULATE OPTIMUM SLIMMING VALUES.
- DECREASE AVERAGE ACCESS TIME.
- DECREASE PWB AREA WITHOUT LOSS OF FUNCTIONALITY.
- ALLOW FOR FLEXIBILITY IN FIRMWARE UPDATES.
- PLACE AS MANY FUNCTIONS AS POSSIBLE IN LSI WHILE MINIMIZING COST.

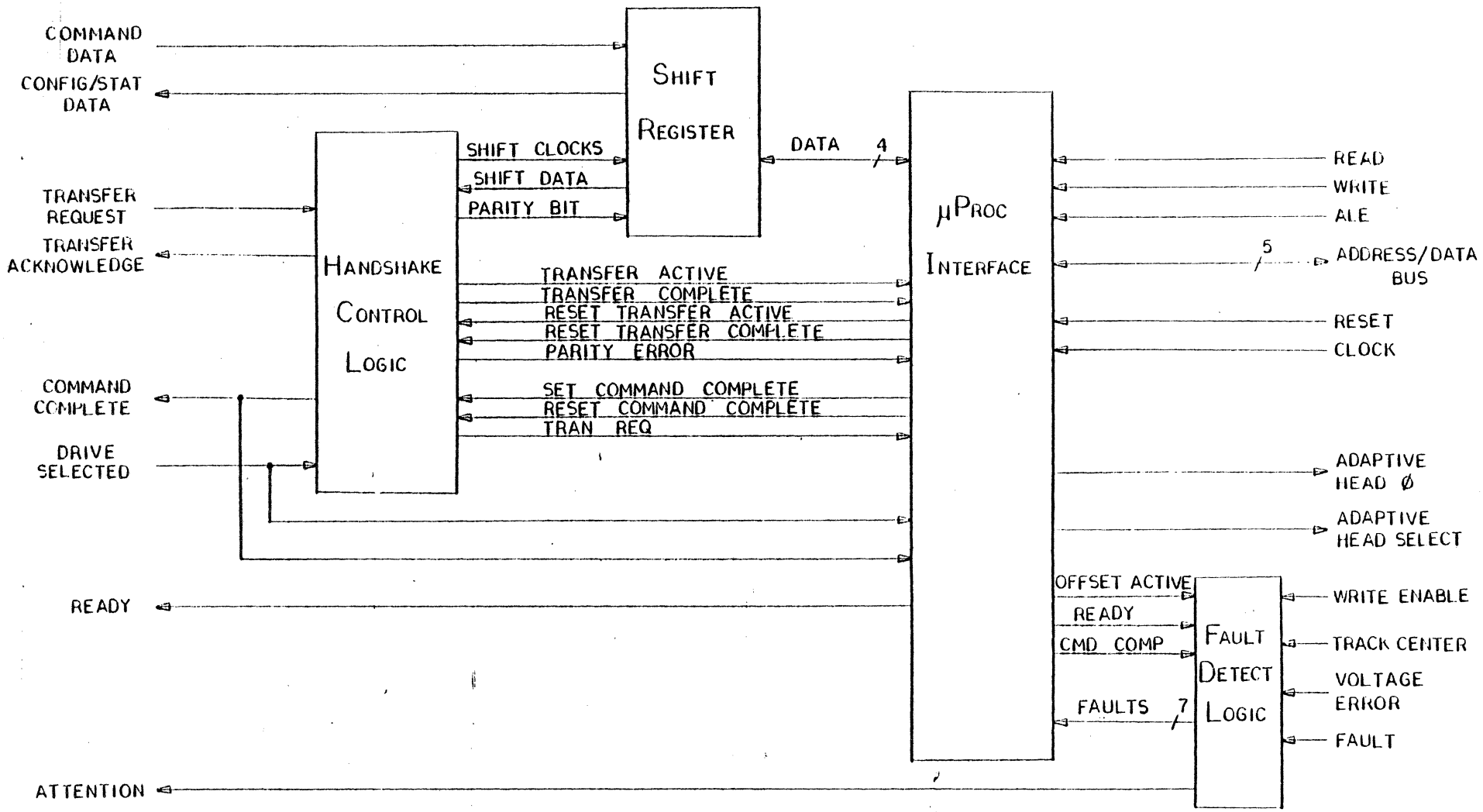
IMPLEMENTED THROUGH

- SERIAL COMMUNICATIONS LINK BETWEEN UPROC AND RW LSI.
- ESDI COMMAND AND CONFIG/STATUS DATA TRANSFERS CONTROLLED BY HARDWARE.
- A) MOVE WATCH DOG TIMER INTO LSI
  B) VELOCITY, WRITE CURRENT, AND TRACK OFFSET GENERATOR USE SAME HARDWARE AND PWM TECHNIQUE.
  C) MOVE DIGITAL WRITE FAULT LOGIC INTO LSI.
  D) MOVE INTERFACE SIGNALS GATED WITH DRIVE SELECTED INTO LSI.
- EXTERNAL PROGRAM MEMORY CAPABILITY
- 8031 UPROC WITH BUS COMMUNICATION TO SERVO AND I/O LSI, SERIAL COMMUNICATION TO R/W LSI, AND INDIVIDUAL PORTS.

MI
1/18/85

WREN-III
DETAILED BLOCK DIAGRAM
10/29/84 S. Welty
12/13/84 SW





I/O LSI BLOCK DIAGRAM

1-30-85
M J IRWIN

WREN III ESDI I/O LSI

THEORY OF OPERATION

THE I/O LSI WAS DESIGNED TO DECREASE THE TIME THE UPROC SPENT RECEIVING COMMAND DATA AND SENDING CONFIG/STATUS DATA. THE I/O LSI CAN RECEIVE (OR TRANSMIT) ONE 17-BIT WORD IN UNDER 25 USEC ($\approx$ 1.5 USEC/BIT). IF THE HOST CONTROLLER WERE TO IMPLEMENT ITS END OF THE HANDSHAKE PROTOCOL IN HARDWARE ALSO, THE ENTIRE COMMAND DATA TRANSFER WOULD TAKE LESS THAN 50 USEC AND HAVE NEGLIGIBLE IMPACT ON SEEK TIME. AS A COMPARISON, A CONTROLLER AND A DRIVE BOTH IMPLEMENTING THE COMMAND TRANSFER IN FIRMWARE WOULD ADD 1.5 USEC TO THE SEEK TIME JUST TO TRANSFER THE COMMAND.

THE I/O LSI CAN RECEIVE THE ENTIRE 17 BITS OF COMMAND DATA FROM THE HOST WITHOUT INTERVENTION FROM THE DRIVE PROCESSOR. THE LSI WILL DEACTIVATE THE COMMAND COMPLETE SIGNAL WHEN THE FIRST TRANSFER REQ IS RECEIVED. THE TRANSFER ACTIVE FLAG IS SET EACH TIME A TRANSFER REQ IS RECEIVED AND CAN ONLY BE RESET BY THE UPROC. THIS ALLOWS THE UPROC TO MEASURE THE TIME BETWEEN TRANSFER REQ'S TO DETERMINE IF AN INTERFACE FAULT HAS OCCURRED. (THIS FUNCTION WOULD TAKE A PROHIBITIVELY LARGE NUMBER OF GATES TO IMPLEMENT IN THE LSI.) THE LSI WILL ACTIVATE THE TRANSFER COMPLETE FLAG AFTER THE 17 BITS OF COMMAND DATA HAVE BEEN RECEIVED. THE LSI HAS BEEN CALCULATING THE PARITY OF THE COMMAND DATA AS EACH BIT IS SHIFTED INTO THE SHIFT REGISTER AND THE PARITY ERROR FLAG WILL BE ACTIVE AT THIS TIME IF INCORRECT PARITY OCCURRED.

THE UPROC WILL BE ABLE TO READ THE COMMAND DATA FROM THE SHIFT REGISTER IN FOUR 4-BIT NIBBLES. THE UPROC DECODES THE COMMAND DATA AND EXECUTES THE COMMAND. WHEN THE COMMAND IS COMPLETED, THE UPROC WILL SET COMMAND COMPLETE TO ALLOW A NEW COMMAND TO BE SENT. SETTING COMMAND COMPLETE CAUSES TRANSFER COMPLETE TO BE RESET.

2 - THEORY OF OPERATION

IF COMMAND EXECUTION REQUIRES THAT CONFIG/STATUS DATA BE SENT TO THE HOST CONTROLLER, THE UPROC WILL LOAD THE SHIFT REGISTER WITH FOUR 4-BIT NIBBLES AND THEN RESET TRANSFER COMPLETE. THE CONFIG/STATUS DATA IS SENT TO THE HOST CONTROLLER AUTOMATICALLY. THE PARITY BIT IS CALCULATED AS THE DATA IS SHIFTED OUT AND IS PLACED ONTO THE CONFIG/STATUS DATA SIGNAL LINE IN THE 17TH BIT POSITION. THE UPROC MAY AGAIN MONITOR THE TRANSFER ACTIVE FLAG FOR INTERFACE ERRORS AS THE DATA IS SHIFTED OUT. THE TRANSFER COMPLETE FLAG WILL BE ACTIVATED AFTER THE 17TH BIT HAS BEEN SENT. THE UPROC WILL THEN SET COMMAND COMPLETE (WHICH RESETS TRANSFER COMPLETE) TO INDICATE THAT THE DRIVE IS READY TO RECEIVE THE NEXT COMMAND.

THE UPROC INTERFACE PORTION OF THE I/O LSI CONSISTS OF REGISTERS WHICH THE PROCESSOR CAN WRITE TO AND BUFFERS TO READ FROM. THE MEMORY SPACE IS FIXED (BETWEEN 0010H AND 0017H) AND IS DECODED INSIDE THE LSI.

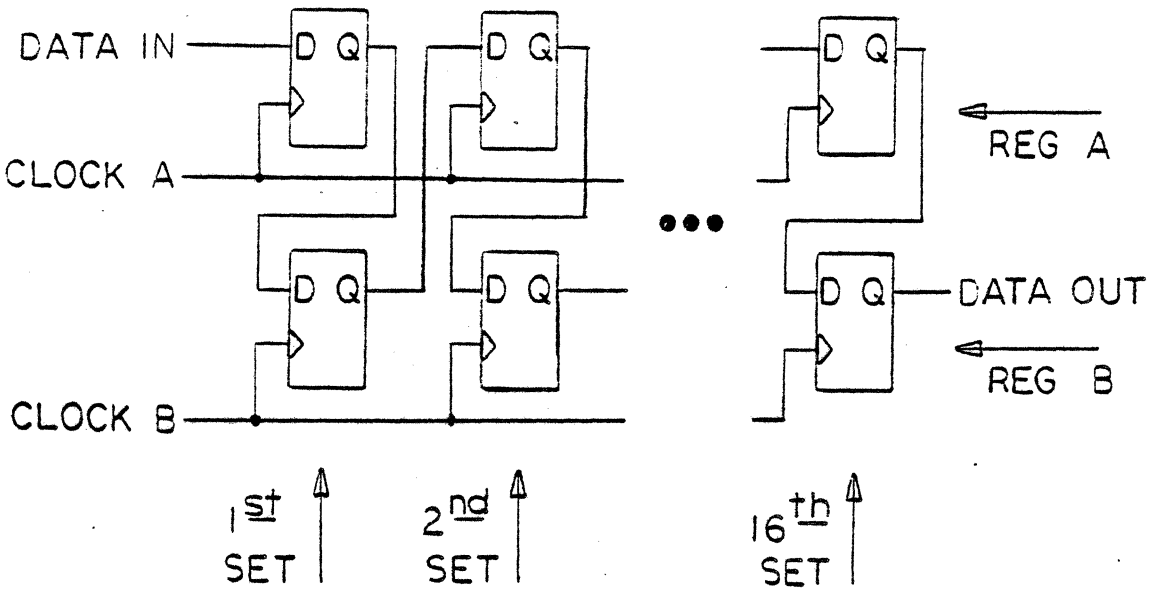
FOUR WRITE ADDRESSES ARE USED TO LOAD THE SHIFT REGISTERS WITH CONFIG/STATUS DATA. THREE ADDRESSES ALLOW THE PROCESSOR TO WRITE TO CONTROL BITS WHICH SET/RESET THE FAULT LATCH, RESET TRANSFER COMPLETE, ETC. WRITING TO THE EIGHTH ADDRESS GENERATES A PULSE WHICH SETS COMMAND COMPLETE.

FOUR READ ADDRESSES ARE USED TO ACCESS THE COMMAND DATA IN THE SHIFT REGISTER. THREE ADDRESSES ALLOW THE PROCESSOR TO READ STATUS BITS SUCH AS TRANSFER ACTIVE, TRANSFER COMPLETE, AND PARITY ERROR. THE EIGHTH ADDRESS IS NOT USED.

THE SHIFT REGISTER IS COMPOSED OF TWO SETS OF D FLIP-FLOPS. TWO CLOCKS ARE APPLIED TO THE SHIFT REGISTER EACH TIME A BIT IS SHIFTED INTO (OUT OF) THE REGISTER. EACH DATA BIT IS SHIFTED FROM THE NTH FLIP-FLIP IN THE A REGISTER TO THE N + 1TH FLIP-FLOP IN THE B REGISTER ON THE FIRST CLOCK. THE SECOND CLOCK SHIFTS

3 - THEORY OF OPERATION

THE DATA FROM THE N + 1TH FLIP-FLOP IN THE B REGISTER TO THE N + 1TH FLIP-FLOP IN THE A REGISTER. THIS ENSURES THAT DATA HOLD AND SET-UP TIMES FOR THE FLIP-FLOPS IN THE SHIFT REGISTERS ARE MET AND PREVENTS LOSS OF DATA.



THE FAULT DETECTION LOGIC CONSISTS OF A GROUP OF FLIP-FLOPS WHICH ARE SET INDIVIDUALLY WHEN A SPECIFIC TYPE OF FAULT IS DETECTED AND A COMMON FLIP-FLOP WHICH IS SET WHEN ANY FAULT IS DETECTED. THE PROCESSOR IS ABLE TO READ THE OUTPUTS OF ALL THE LATCHES TO DETERMINE WHICH FAULT CONDITION CAUSED THE ATTENTION LINE (THE COMMON FLIP-FLOP) TO BE SET. THE PROCESSOR CAN SET THE COMMON LATCH AND RESET ALL LATCHES. IF A FAULT CONDITION PERSISTS WHILE/AFTER THE PROCESSOR RESETS THE LATCH, THE FAULT LATCH WILL REMAIN SET.

WREN III I/O LSI

RISKS & ALTERNATIVES

- USE OF RCA AS VENDOR FOR I/O LSI.
- NO TIME SCHEDULED FOR A SECOND PASS ON THE LSI.

LSI LOGIC CORPORATION MAKES A 5000 SERIES PART WHICH IS PURPORTED TO BE EQUIVALENT TO RCA'S PART.

CURRENT STATUS

1-21-85 CONVERSION OF TTL EMULATOR SCHEMATICS IS COMPLETE. NET LIST WILL BE BUILT AND SIMULATION WILL BE UNDER WAY BY FEBRUARY 5 & 6.

MI
1/18/85

WREN II/WREN III/ESDI COMPATIBILITY

- WREN III IS A FULLY COMPATIBLE IMPLEMENTATION OF THE INDUSTRY STANDARD ESDI INTERFACE.

	WREN II	WREN III
INTERFACE MODES	STEP/SERIAL	SERIAL ONLY
ADDRESSING MODES	BYTE CLOCK/SECTOR/ ADDRESS MARK	SECTOR ONLY*
TRANSFER RATE	5 MHZ	10 MHZ
INTERFACE HANDSHAKING	FIRMWARE	HARDWARE
DIAGNOSTICS	LIMITED - ERROR STATUS	SAME AS WREN II

* ADDRESS MARK WILL BE SUPPORTED IF REQUIRED.

DCP
2/13/85

WREN II/WREN III POWER COMPATIBILITY

	WREN II	WREN III
5V SUPPLY	± 5%	± 5%
12V SUPPLY -STARTUP	±10%	± 10%
OPERATION	± 5%	± 5%
TYPICAL POWER DISSIPATION	25W	25W

- RIPPLE AND NOISE SENSITIVITY SPECIFICATIONS SAME AS WREN II.

DCP
2/13/85

ESTIMATED MECHANICAL DESIGN CHANGES

ACTUATOR & ASSEMBLY

PARTS	CHANGES
LOWER HOUSING	ONE PIECE
UPPER HOUSING	
CENTER POLE	NOT REQUIRED
MAGNETS	NEODYMIUM
COIL	PANCAKE
ROTARY ARM	COIL ATTACHMENT
BASEPLATE M/C	ACTUATOR MOUNTING

HUMIDITY CONTROL SYSTEM

CAPILLARY TUBE	NEW PART
DESICCANT & CONTAINER	NEW PART
TOP COVER	NEW PART
GASKET	NEW PART
BASEPLATE M/C	NEW PART
BREATHER FILTER	NEW PART

OTHER PARTS

R/W FLEX CIRCUIT	PACKAGING OF 117 DATA CHIPS
FLEX MOUNT BRACKET	
SOLENOID LOCK	INCREASED TRACKS

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2/14/85

WREN III SINGLE SOURCE ITEMS

- NATIONAL DP8464 READ CHANNEL I.C.
- TL026 AGC AMPLIFIER

CURRENTLY SINGLE SOURCED-SECOND SOURCE BEING WORKED

- SERVO LSI
- I/O LSI
- R/W LSI
- 117 R/W PREAMP
- CA3127 TRANSISTOR ARRAY

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2/13/85

UNIQUE PARTS TO WREN III

- NATIONAL DP8464 READ CHANNEL I.C.
- 117 R/W PREAMP I.C.
- LSI - SERVO 2200 GATE ARRAY
  R/W 1400 GATE ARRAY
  I/O 850 GATE ARRAY
- 74 HC 4066 HIGH SPEED ANALOG SWITCH
- MC1658 VCO
- 74F14 "FAST" TTL INVERTER
- TL026 AGC AMPLIFIER
- 20 MHZ CRYSTAL

DCP
2/13/85

WREN III DESIGN REQUIREMENTS SUMMARY

FORM FACTOR	5 1/4" FULL HEIGHT (5 3/4" X 3 1/4" X 8")
HEADS	90° ROTATED SMALL CATI SLIDER
MEDIA	75 MIL PLATED (130 MM O.D., 40 MM I.D.)
TYPE	FIXED MEDIA
MOUNTING	HORIZONTAL AND VERTICAL
USEFUL LIFE	5 YRS OR 30,000 HRS
MTBF	SUPERIOR - 18,000 HRS
	TARGET - 15,000 HRS
WEIGHT	LESS THAN 8 LBS
INTERFACE	ESDI (SERIAL MODE ONLY)
	(SECTOR OPTION ONLY)
PARTS GOALS	
PREFERRED	90% (AT BLUE LINE RELEASE)
EXISTING	80%
TYPES	425
TOTAL PARTS	1,000
MLB - SUPERIOR	$780
TARGET	$810
THRESHOLD	$835
BASED ON HEADS	$25
MEDIA	$27.22
START-UP COSTS	$3,000,000

NO OPERATOR CONTROLS - POWER UP WITH USER SYSTEM POWER
NO PREVENTIVE MAINTENANCE
LIMITED DIAGNOSTIC CAPABILITY FOR FIELD SERVICE
DEPOT OR FACTORY SERVICING ONLY

DCP
2/13/85

PERFORMANCE

UNFORMATTED CAPACITY	182 MB
NO. OF DATA SURFACES	9
NO. OF SERVO SURFACES	1
TPI	960
CYLINDERS	969
BPI	19,058
BYTES/TRACK	20,880
INTERFACE TRANSFER RATE	10 MHZ NRZ
RECORDING CODE	2,7
POSITIONING TIMES (WORST CASE)	
SINGLE TRACK	8 MS
AVERAGE	25 MS
MAXIMUM	65 MS
SPINDLE SPEED	3600 RPM
POWER REQUIREMENTS	12V $\pm$ 5%
	+ 5V $\pm$ 5%
	30 W TYPICAL
READ ERROR RATE	
RECOVERABLE	$<$ 1 IN 10^{10}
NON-RECOVERABLE	$<$ 1 IN 10^{12}
SEEK ERROR RATE	$<$ 1 IN 10^{6}

DCP
2/13/85

ENVIRONMENT

TEMPERATURE	
OPERATING	10°C TO 46°C
BASEDECK	57°C MAXIMUM
GRADIENT	12°C/HR
TRANSIT	-40°C TO 60°C
GRADIENT	20°C/HR
STORAGE	-10°C TO 50°C
GRADIENT	15°C/HR
HUMIDITY (W/O CONDENSATION)	
TRANSIT	5% TO 95%
STORAGE	10% TO 90%
ALTITUDE	
OPERATING	-1,000 TO 10,000 FT.
OPERATING & STORAGE	-1,000 TO 10,000 FT.
TRANSIT	-1,000 TO 10,000 FT.
SHOCK	
TRANSIT	40G
VIBRATION	
OPERATING	5 - 22 HZ .01 IN. DISPLACEMENT
	22 - 500 HZ .25 G's

DESIGNED TO MEET UL, CSA AND VDE REQUIREMENTS

FCC	CLASS B IN A TYPICAL CABINET
EMC	MEASUREMENT ONLY
ACOUSTIC	MEASUREMENT ONLY
	PERFORMANCE EQUAL TO WREN II

DCP
2/13/85

D.R. VS ENGINEERING SPEC

CAPACITY - TARGET	182 MB	182 MB
SUPERIOR	-	192 MB
TRACKS/SURFACE - TARGET	969	969
SUPERIOR	-	1024
BPI, MAX.	19,058	19,209
AVG. ACCESS - TARGET(WORST CASE)	25 ms	25 ms
SUPERIOR (TYPICAL)	-	20 MS
MTBF - TARGET	15,000 POH	15,000 POH
SUPERIOR	18,000 POH	-
POWER SUPPLY REQMTS.(TYPICAL)	30W	25W
TEMPERATURE - OPERATING	10° to 46°C	5.5° TO 50°C
TRANSIT	-40° TO 60°C	-40° TO 70°C
STORAGE	-10° TO 50°C	-14 TO 54°C
HUMIDITY - OPERATING	20% TO 80%	15% TO 85%
TRANSIT	5% TO 95%	5% TO 95%
STORAGE	10% TO 90%	5% TO 95%
ALTITUDE - OPERATING	-1,000 TO 10,000	-1,000 TO 10,000 FT.
TRANSIT	-1,000 TO 10,000 FT.	-1,000 TO 12,000 FT.
STORAGE	-1,000 TO 10,000 FT.	-1,000 TO 10,000 FT.
OPERATING VIBRATION - TARGET	.25 G'S	.25 G'S
SUPERIOR	-	.5 G'S
SHOCK - TRANSIT	40 G'S	50 G'S

DCP
2/13/85

HIGH RISK AREA EVALUATION

BEARING LIFE

THERMAL PERFORMANCE

ACOUSTIC NOISE LEVEL

RESONANCES RELATED TO HEADS, ROTARY ARM, SPINDLE ASSEMBLIES

R/W FLEX CABLE PACKAGING

NEW SERVO CONCEPT (TRI PHASE PATTERN)

NEW R/W CONCEPT (ADAPTIVE SLIMMING/NATIONAL READ CHAIN CHIP)

LSI DEVELOPMENT (SCHEDULE CONCERN FOR THREE NEW LSI)

AVAILABILITY OF HEAD/MEDIA WITH PROVEN INTERFACE AND PARAMETRICS

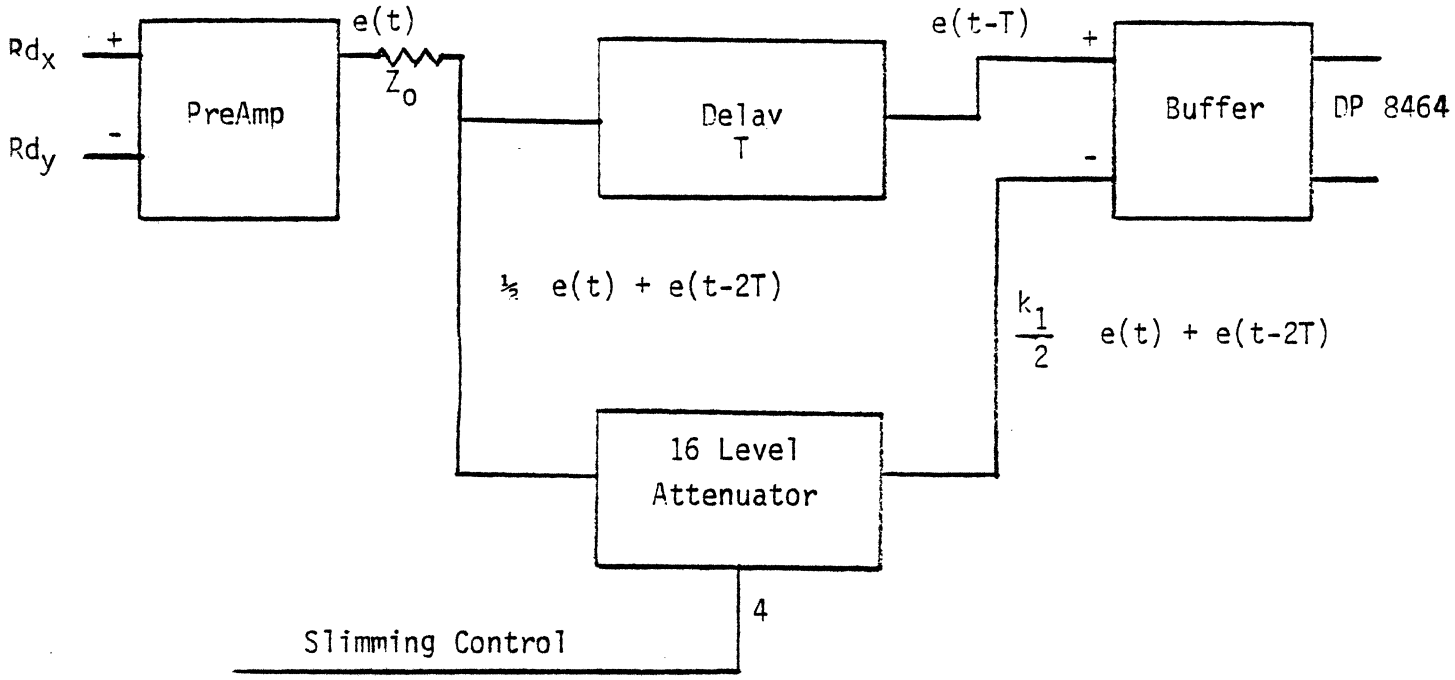
CIRCUIT STABILITY

DCP
2/13/85

WREN III SCHEDULE

DESIGN REQUIREMENTS	COMPLETE
ENGINEERING SPECIFICATION	COMPLETE
CONCEPT DESIGN REVIEW	2/85
ENGINEERING MODELS COMPLETE	7/85
PROTOTYPE DESIGN REVIEW	9/85
PRODUCT ANNOUNCEMENT	10/85
DVT START	10/85
DVT COMPLETE	1/86
CEU START	10/85
FCC TESTING COMPLETE	11/85
UL/CSA APPROVAL	12/85
PREPRODUCTION START	12/85
CLASS B RELEASE	1/86
PVT START	1/86
PVT COMPLETE	5/86

DCP
2/14/85



$$e_o = e_{in} - k\, e_{in}(t+T) - k\, e_{in}(t-T)$$

$$G(s) = 1 - k\, e^{Ts} - k\, e^{-Ts}$$

$$G(w) = 1 - 2k \cos(wT)$$

Adaptive Slimming Network

THEORY OF OPERATION
Adaptive Slimming

The output of the fixed gain flex circuit read/write amplifier (SSI 117 or equivalent) is AC coupled to an adjustable gain preamplifier. The adjustment of this preamplifier will be set to center the nominal system gain based on current broad based head/media performance into the center of the dynamic range of latter automatic gain control circuitry. The preamplifier serves also to boost signal levels in order to improve the noise immunity of single ended analog circuitry associated with the adaptive slimming network.

The adaptive slimming network consists of a passive delay line, a digitally controlled attenuator network, and an output buffer with relatively high input impedance. The slimming network is a modification of the cosine equalizer circuitry first developed for the Lark program and subsequently used on both Wren I and Wren II. The adaptive slimming concept represents a major advancement toward improving head/media vendor adaptation. The full impact of this design feature has been parlayed for reduced board area.

The operation of the adaptive slimming system is based on obtaining current information on the amount of slimming that is necessary for each head/disk combination. Data is then recorded at the outer guard band data track which represents the optimal slimming necessary for that head/disk combination. Under firmware control, this information is then read off of the disk and is used to load data registers contained in the read/write LSI during track to track seeks. Head select lines input to the read/write LSI are used to decode which of the registers are output to the slimming control lines. The present implementation provides for sixteen levels of slimming. The present digitally controlled attenuator circuitry used in the analog portion of the adaptive slimming circuitry has a limited range and resolution (linearity) and has been optimized for board space and cost.

The function of the cosine equalizer is to reduce intersymbol interference which gives rise to peak shift and amplitude modulation. The compensated signal at the output of the buffer is then AC coupled into the read channel chip. The amplifier and AGC will accept input signals from approximately 20 mV P-P differential to 600 mV P-P differential and amplify them to 4 V P-P differential. The amplifier's output voltage is fed back via an external filter to an internal full wave rectifier and compared against the external voltage on the V_{ref} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the gate channel input four times the DC voltage on V_{ref}.

The peak detection is performed by feeding the filtered output of the amplifier to the differentiator. The differentiator

output changes state when the input pulse changes direction. Generally this will be at the peaks. However, if the signal exhibits shouldering, the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised of a differential comparator with hysteresis and a D-flip-flop. The hysteresis or amplitude qualification level for this comparator is externally set via the set hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level and hence be amplitude qualified. The peak of the input signal will generate a pulse out of the differentiator and bidirectional one shot. This in turn clocks the D-flip-flop and prevents baseline noise from affecting the encoded data output. The encoded data output represents an ALS TTl compatible read pulse data output with the rising edge indicating the occurrence of a flux reversal.

The read pulse data output is then buffered, converted to level shifted ECL and input to the custom ECL data recovery LSI. This part (used on Wren II ESDI) includes both a frequency and phase detector used in the read PLO, as well as data separation circuitry. Both retimed pulse data and its associated clock appear at its output along with increment and decrement pulses used to drive an external PLO charge pump. This charge pump has the ability to offset the PLO phase and shift the timing of the incoming read pulse data with respect to the 40 MHz PLO clock. This provides both early and late strobe capability. The read/write LSI receives retimed pulse data and decodes this from the 2/7 encoding scheme to NRZ data.

The selection of the SSI 117 flex preamp and elimination of write preamp has allowed all write functions except the write current control circuitry to be incorporated within the read/write LSI. The provision for write current adjustments on a track to track basis has been provided with minimal circuitry.

PRESENT STATUS

- Early tests of National PLO exhibited lock-up and stability problems

- Performed early tests of attenuator/adaptive slimming on Wren II-5 with good results. Was able to modify peak shift. Elimination of write precompensation has also been shown to be feasible on Wren II.

- Calculated and measured filter responses with several different bandwidths.

- Test PWB was constructed and a Wren III system built from Wren II ESDI and FSD ECL 2/7 encoder/decoder. Using switch selectable slimming, have debugged 10 MHz Field Test Unit and am able to write/read worst case patterns with error rates > 1×10^{9}. Initial testing with one head has been done on Level 6 doing write/reads with random seeks over inner tracks, 462-924. Error rates greater than 1 in 10^{10} with random and worst case patterns have been demonstrated.

ADAPTIVE SLIMMING

RONALD METZNER

JANUARY 18, 1984

ADAPTIVE SLIMMING

Adaptive slimming allows the drive to adapt to the particular Heads/Media in that drive. During production, tests are made on the drive to determine its slimming requirements. The slimming information obtained from the tests will be written on Track -1 (Guard Band) on a data surface. Upon Power-up, the microprocessor will read the slimming information and determine the amount of slimming required.

I. DESIGN GOALS

A. Read slimming information from the disk and send it to the microprocessor through the microprocessor's serial interface.

B. Receive and store slimming control nibbles, R/W LSI configuration nibble, maximum head nibble, and diagnostic nibble from the microprocessor.

C. Send status bytes to the microprocessor. The status bytes include the slimming control nibbles, R/W LSI configuration nibble, maximum head nibble, and diagnostic nibble.

II. BENEFITS

A. Automatically shifts slimming for Head/Media changes without stopping production for board changes or use of engineering time.

B. Allows 10 to 15% wider isolated pulse widths for lower head costs. (This may be the critical factor in not needing thin film heads with adequate margins.

C. Allows automatic switchover for multiple Head/Media combinations of vendors.

III. REQUIREMENTS

A. Pushing R/W LSI by adding more lines.

B. Adds more gates to LSI.

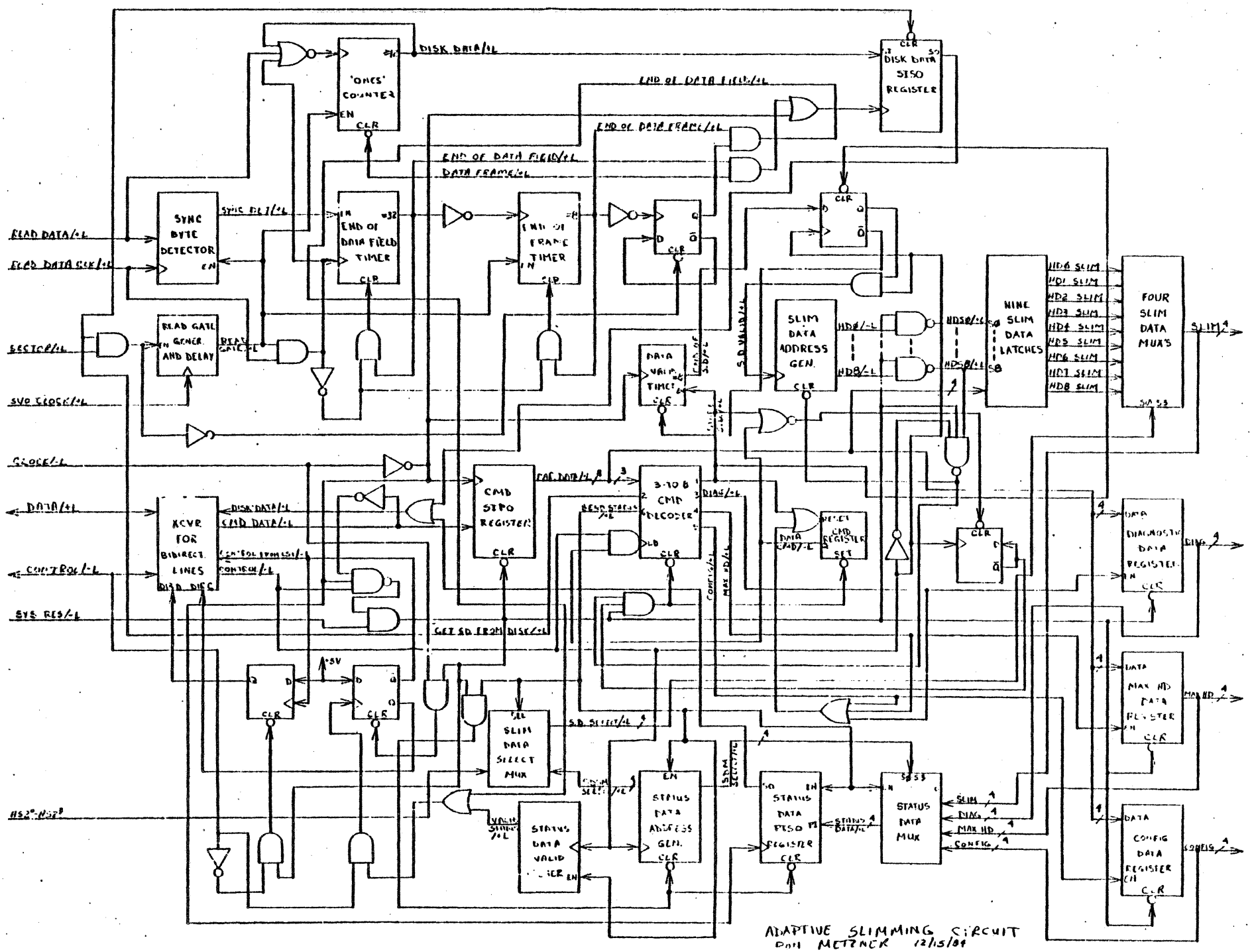
IV. RISKS

A. Increases cost of R/W LSI.

B. Trying out a new concept. It is not known how much adaptive slimming will improve drive performance.

V. ALTERNATIVES

A. Use non-adaptive slimming instead of adaptive slimming.



ADAPTIVE SLIMMING CIRCUIT
DAN METZNER 12/15/84

PROCESS DEFINITION

The slimming information will be written during production on Track -1 (Guard Band) using the Disk Data Format defined below.

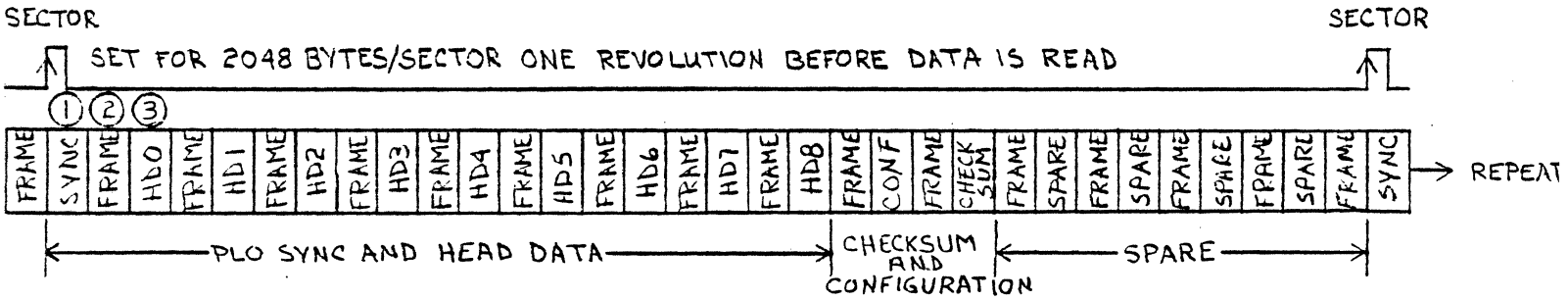
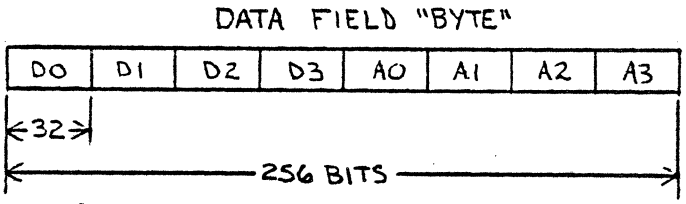


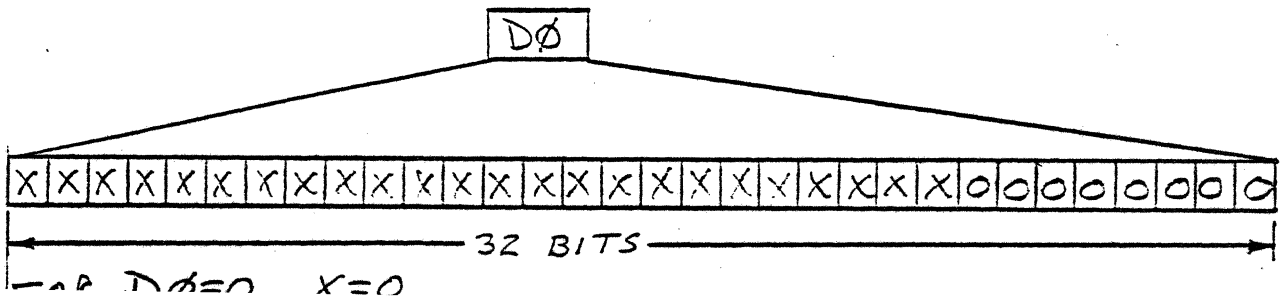
Fig. 1. Disk Data Format For 25.6 us Data Field and Input Times.

1. The "Sync" frame consists of 31 bytes of zeros followed by F7H. The F7H is used to synchronize the adaptive slimming circuit to the information on the disk.

2. Each frame is 32 bytes long to allow processor time to serially input data with plenty of time tolerance before shift register control is switched to next data field. Frame data is all "Zeros" for PLO lock.

3. Each "Bit" of all data fields is 32 bits long to reduce sensitivity to disk defects and allow the processor time to process information. "Zero" data is recorded as 32 zeros. "One" data is 24 ones followed by 8 zeros to allow for errors in sector decode timing. A count of over 12 ones is interpreted as "one" data. Each data "Byte" being 8 "Bits" long is recorded LSB first for the data "Nibble" and then the Address "Nibble". Address "Nibbles" are verified by the processor as incrementing to prevent loss of a "Nibble". The Check Sum "Byte" is also checked. A pictorial of the data field is given below.





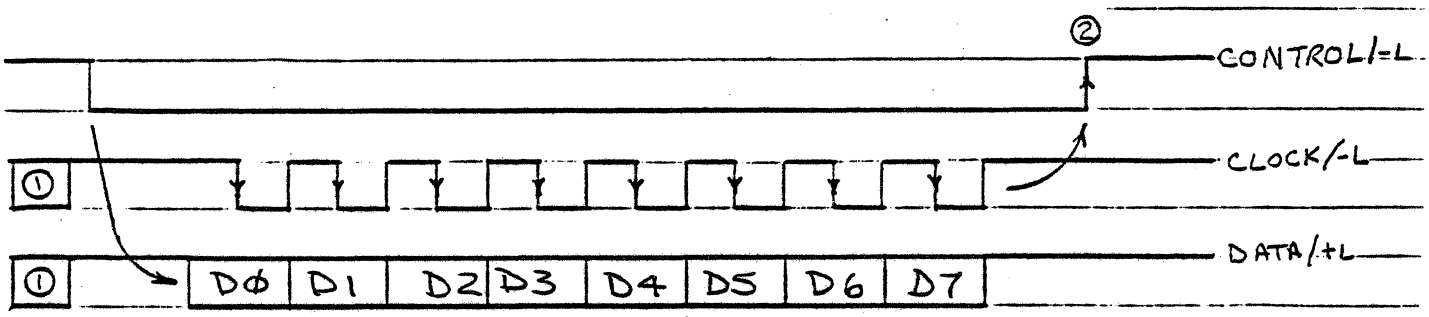


Fig. 2. Serial Transfer From Processor To LSI

1. An illegal condition of "Clock" and "Data" low with "Control" high (inactive) from processor will always reset entire serial logic for new command. Use only for malfunction.

2. LSI will take data shifted in as a command on the trailing edge of "control" line.

Head information for slimming should be requested on Power Up, any head unload, or any other time that the integrity of the processor registers is doubted due to possible "Electrostatic Discharge".

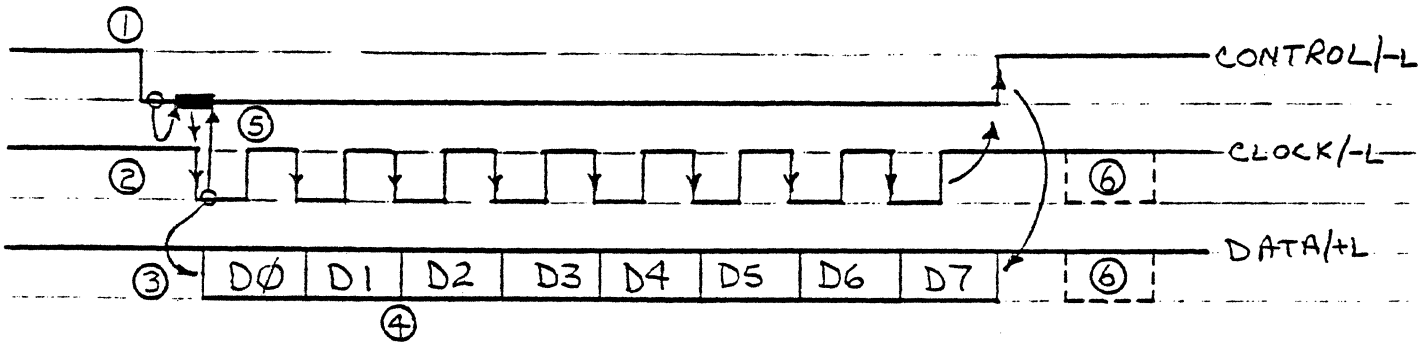


Fig. 3. Serial Transfer Of Disk Data To Processor

1. LSI informs processor that data is ready by setting "control" line low.

2. Processor responds when ready by activating "control" line and then the "clock" line. The heavy black line shows the "control" line being held low by both the LSI and the processor.

3. LSI responds to "clock" line low by releasing its control of the "control" line and outputing the first disk data bit.

4. LSI continues to output each data bit as clocked from the processor until the "control" line is set inactive by the processor. LSI Data output is then tristated while the LSI searches for the next data byte from the disk surface. Once data has been found, go to step 1.

5. The processor inputs data.

6. The processor can terminate this process at any point by leaving the "control" line high with the "clock" and "data" lines both low. At this point, all LSI Disk Data logic and serial transfer logic will be reset. The "control" and "data" lines will be tristated for the next command.

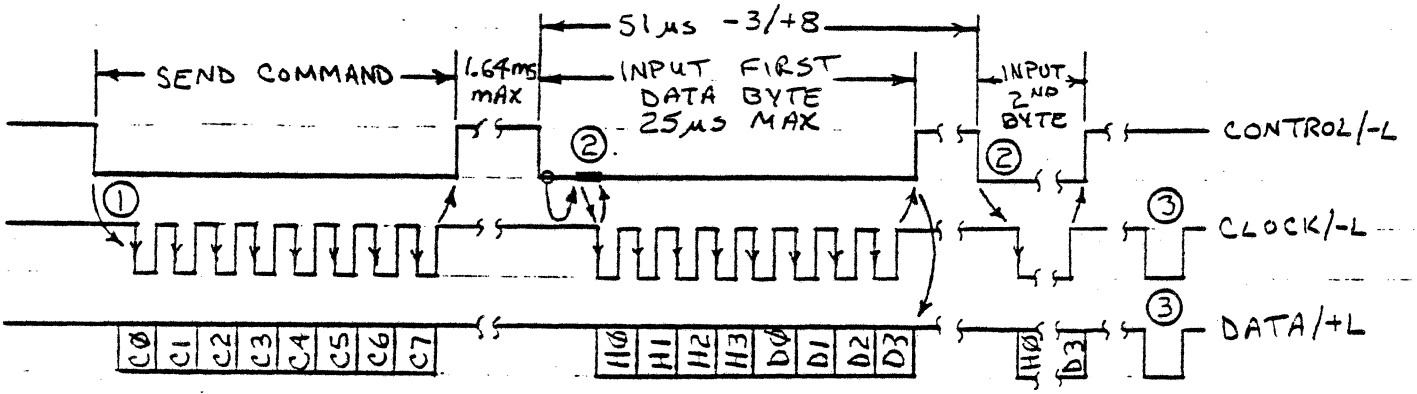


Fig. 4. Transfer Of Disk Data From LSI To Processor

1. Processor begins process by setting the "control" lines low and writing command byte to serial port. The serial port automatically clocks data to the LSI.

2. The LSI sets the "control" line low when a data byte is found and continues to do so until the "clock" line goes low. The processor must also set the "control" line low and then output clock pulses to allow the LSI to shift data out using a 12 us serial input instruction. Data will be taken in by the processor near rising clock edges. the first byte input may be for any Head, therefore, the processor must ignore all data until "Head 0" data is received.

3. The processor can terminate the data input mode after the last byte by leaving the "control" line high with the "clock" and "data" lines both low. The last bytes read should be the system configuration and checksum bytes.

CURRENT STATUS

The adaptive slimming circuit is now in the breadboard stage. A test circuit has been designed to simulate the slimming information being read from the disk. The adaptive slimming circuit has been debugged to the point where it reads the slimming information and sends it to the microprocessor. The serial interface between the adaptive slimming circuit and the microprocessor has also been debugged. The process of sending the status bytes to the microprocessor is being debugged at the time of this writing.

ADAPTIVE SLIMMING TESTER

The adaptive slimming tester will consist of a margin code tester, HP9816, and drive control electronics. The margin code tester will generate the margin codes that the HP9816 will use to determine the slimming information to be written on the disk. The margin code tester has been built and is working. The software required to determine the slimming information will be written once the adaptive slimming circuit has been debugged. The drive control electronics will be designed upon completion of the adaptive slimming circuit.