CONTROL DATA

Student Training Manual for

Cyber 170 ECL Logic

An Individualized Course

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or use Comment Sheet in the
back of this manual.

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INTRODUCTION

CYBER 170 Logic is an introductory course that gives you the capability to read and analyze CYBER 170 logic diagrams. In addition, you learn the physical characteristics of the CYBER 170 logic modules and integrated circuit chips.

At the completion of the course you will not be qualified to perform maintenance on any specific piece of equipment. However, you must know the information in this course to learn how to maintain the various sections of the CYBER 170 mainframe.

This course is designed specifically for persons who are planning to maintain a CYBER 17X mainframe. Although it will not make you a design engineer, the material has sufficient depth to enable you to maintain the logic of a CYBER 170 system.

This course is an individualized, self-study package that allows you to learn at your own pace. The multi-media lessons, using audio, microfiche and text readings, not only reduce boredom, but also provide you with the most effective learning experiences possible.

If this is your first experience with a self-study course you may want to read through appendix A, "Using Individualized Instruction," before you begin the course. Appendix B explains the correct procedure for signing on to the PLATO terminal. Appendix C gives an explanation of how to use microfiche.

You may now begin the course by starting Module 1.

MODULE 1
PHYSICAL CHARACTERISTICS

During this module of instruction you learn the physical characteristics of CYBER 170 logic. Module 1 covers the following topics:

- Logic Pack Characteristics
- Integrated Circuit Chip Characteristics
- Module-Handling Procedures

PRETEST

To start this module, sign on the PLATO® terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

If you have access to a spare CYBER 170 logic module from your site, get it before starting this module of instruction. The module does not have to be any specific type, because you will be learning the general characteristics of logic modules. Having a module helps you understand some of the items more easily, but a module is not required equipment.

LEARNING ACTIVITIES

In the assigned column below, put a check mark by each activity assigned to you by PLATO Learning Management (PLM). Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	1-A	Audio/Microfiche: Logic Pack Characteristics. During this activity you learn how a CYBER 170 module is constructed. You also learn how to locate various components on a logic module.	1-3

Assigned	Completed	Activity	Description	Page
_____	_____	1-B	Text Reading: ECL, TTL, and MOS Chip Characteristics. During this activity you learn some of the physical characteristics and requirements of various logic chips used in a CYBER 170.	1-6
_____	_____	1-C	Text Reading: Module Handling Procedures. During this activity you learn the proper handling procedures for different types of CYBER 170 logic modules.	1-11

LEARNING ACTIVITY 1-A. AUDIO/MICROFICHE: LOGIC PACK CHARACTERISTICS

During this activity you learn how a CYBER 170 logic module is constructed. You also learn how to locate various components on a logic module.

OBJECTIVE

- You will be able to identify the physical characteristics of a CYBER 170 logic module.

While you are viewing the microfiche, refer to figures 1-1, 1-2, and 1-3 on the following pages for some of the material in the lesson. Make notes on the figures if you wish.

At this time, load the microfiche labeled "Logic Pack Characteristics," P/N 75444756, into your projector and the corresponding audiotape, P/N 75444756, into your cassette player and proceed with the activity.

STUDENT NOTES

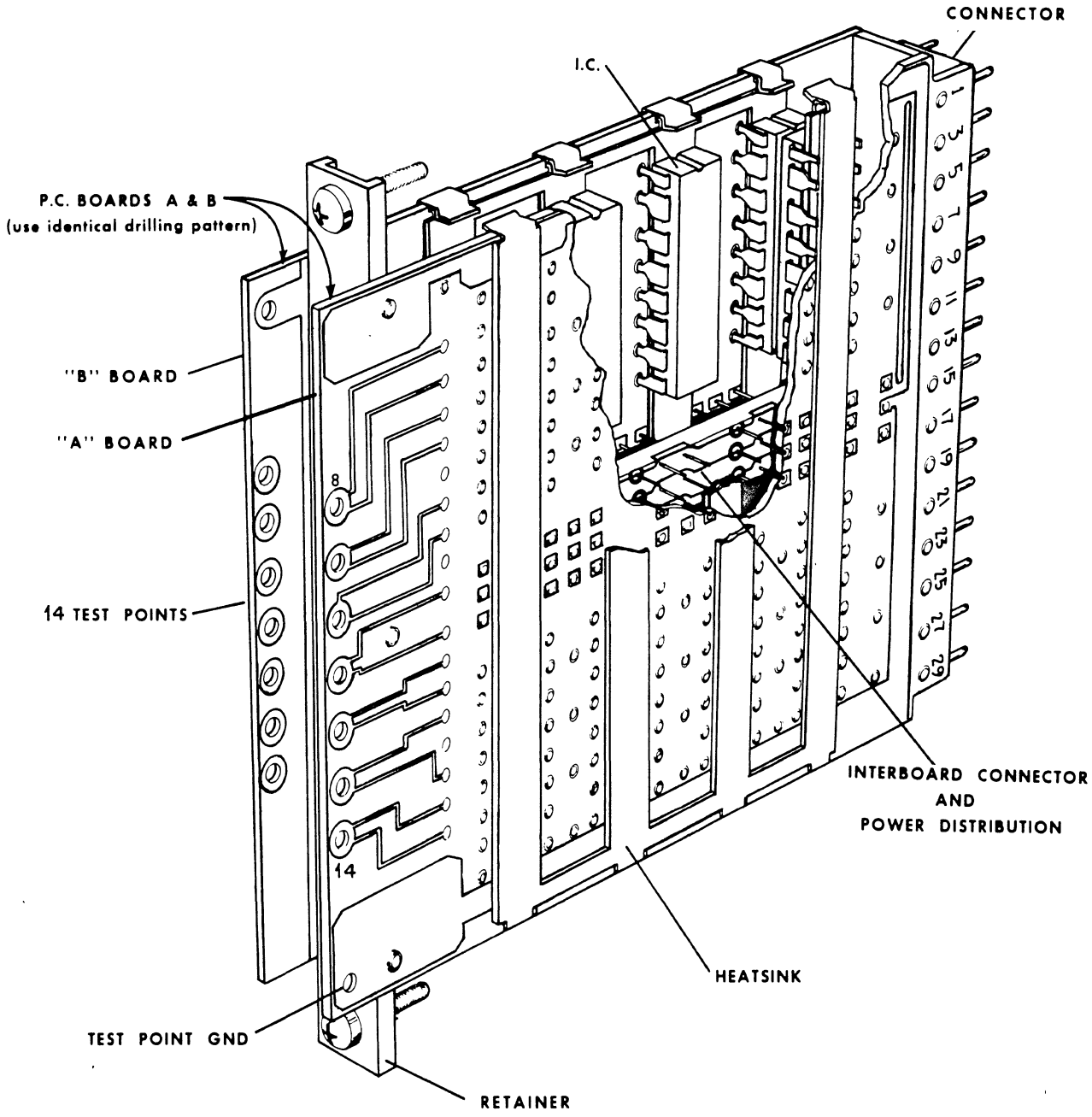


Figure 1-1. CYBER 170 Logic Module

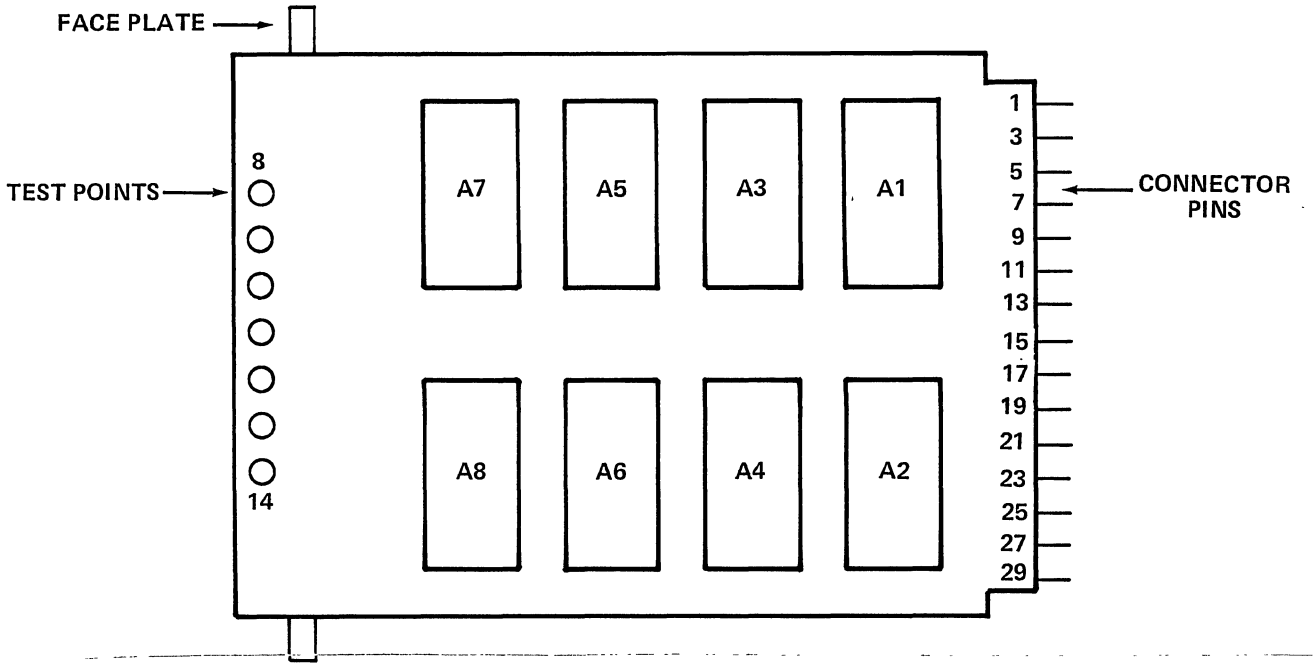


Figure 1-2. 170 Logic Module - A Board Chip Locations

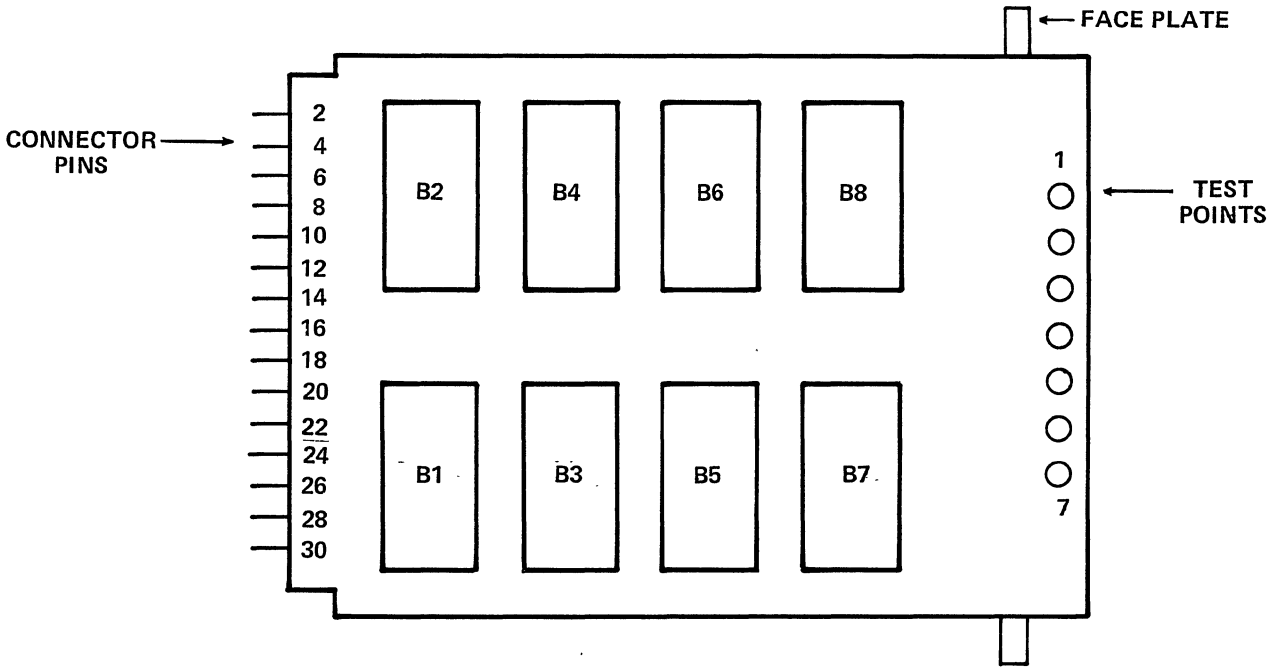


Figure 1-3. 170 Logic Module - B Board Chip Locations

LEARNING ACTIVITY 1-B. TEXT READING: ECL, TTL, AND MOS CHIP CHARACTERISTICS

During this activity you learn some of the physical characteristics and requirements of various logic chips used in a CYBER 170. The activity covers the following topics:

- Pin Numbering
- Voltage Requirements
- Logic Levels

OBJECTIVE

- You will be able to identify the physical characteristics and functions of the IC chips used in the CYBER 170 logic modules.

First of all, note how the pins are numbered. Figure 1-4 shows the pin numbering for chips with 16 pins. Almost all ECL chips and all of the TTL chips in the CYBER 170 have 16 pins. One end of the chip in the figure has a notch in it. This notch is always at the end of the chip where pin number 1 is located. Pin 1 is always in the same relationship to the notch as it appears in figure 1-4.

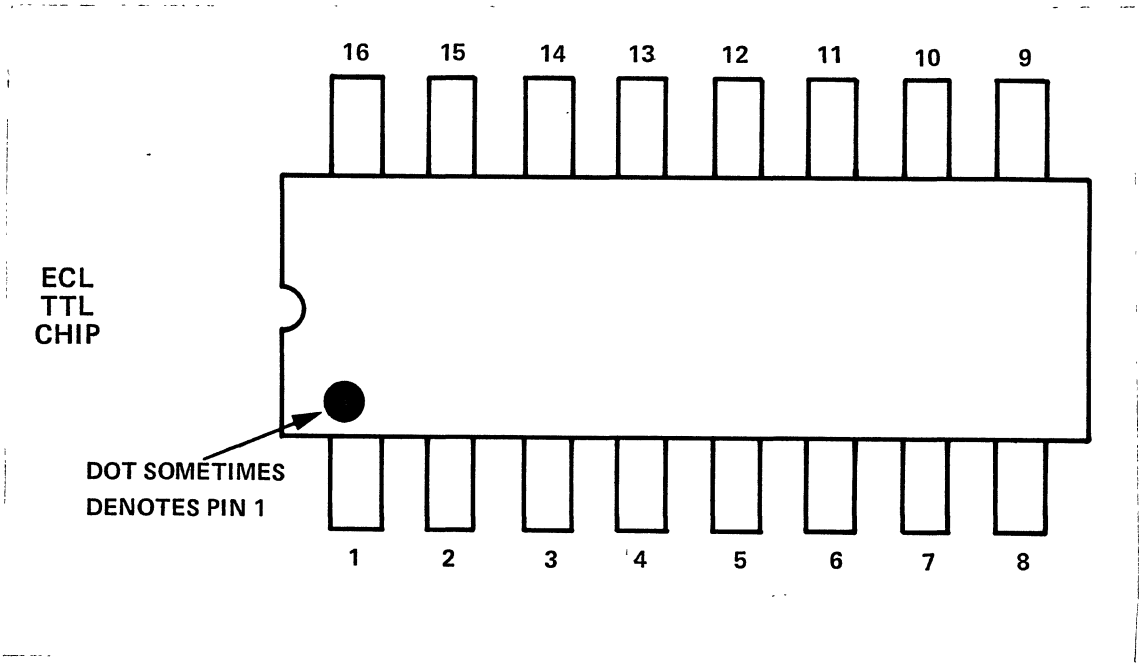


Figure 1-4. Chip Pin Layout - 16-Pin Chips

Some chips do not have a notch in one end. If you see a chip without a notch, then pin 1 is marked by a white dot on the top of the chip. In some cases, a chip has both a notch and a dot. Then, you should have no trouble at all finding pin 1 of the chip.

The last thing you should observe about the chip is that the pins are numbered counterclockwise around the chip from pin 1 when you are looking at the top of the chip. Thus, if you look at the chip from the bottom (which you usually will do when it is in the module), the pins are numbered clockwise from pin 1.

Figure 1-5 shows a 24-pin chip. Only one chip type in the CYBER 170 has 24 pins. It is an ECL arithmetic logic unit chip. The only difference between this chip and the 16-pin chips is that it has 12 pins on each side. Otherwise, it has the same pin-numbering scheme as 16-pin chips.

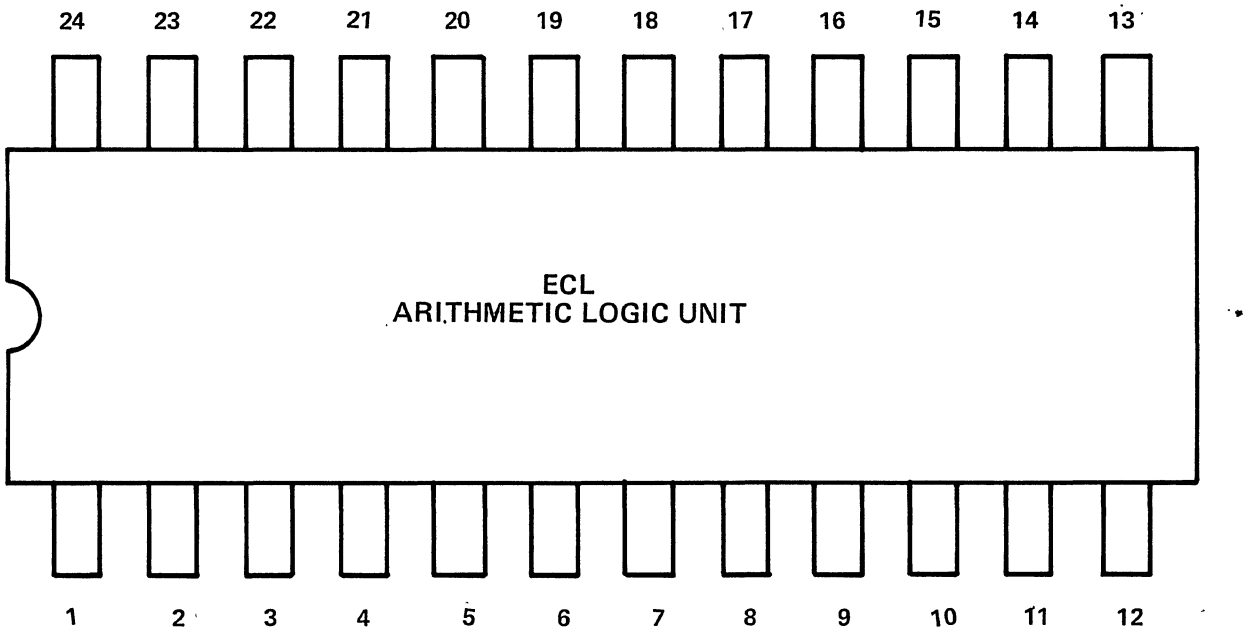


Figure 1-5. Chip Pin Layout - 24-Pin Chip

Figure 1-6 shows the pin numbering for an MOS memory chip. Its numbering is like the others, except that it has 18 pins.

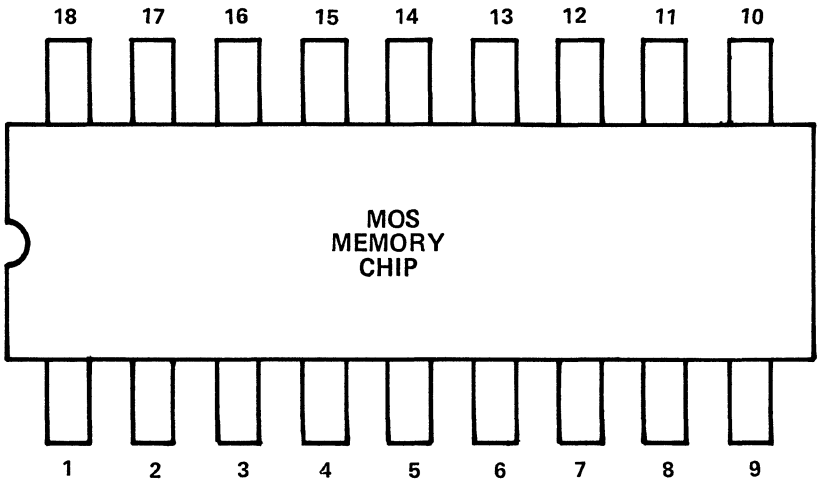


Figure 1-6. Chip Pin Layout - 18-Pin Chips

Now let us examine the voltages necessary to run the various logic types in the CYBER 170. The table in figure 1-7 shows the voltages that each logic type requires. Power supplies located in each logic chasis of the mainframe generate these voltages. In a future course you will learn how the power supplies operate.

ECL	GROUND, -2.2V AND -5.2 VOLTS
TTL	GROUND AND +5 VOLTS
MEMORY	GROUND, +8V, +20V AND +22.5V

Figure 1-7. ECL, TTL, and MOS Power Supply Requirements

Finally, you need to know the signal logic levels for each logic type. Figure 1-8 shows the logic levels for the ECL, TTL, and MOS types of logic. Note that the ECL is negative logic; that is, a logical 1 is the most negative signal or a low, and a logical zero is a high. Conversely, the TTL and MOS types use positive logic; in these types, a logical 1 is a high, and a zero is a low.

Because most of the logic in a CYBER 170 is ECL, the logic diagrams are drawn in the negative logic convention. When a diagram has TTL or MOS logic on it, there will be a note to that effect.

The drawing in figure 1-9 shows how voltages are connected to each logic module through the logic chassis back-plane wiring pins. Note that Logic Paks are the black faceplate modules; Driver Paks are the blue faceplate modules; and Memory Paks are the red faceplate modules.

This concludes the lesson on chip characteristics and logic levels. The information will be useful to you when you have to do any scoping in the logic or when installing FCOs.

LOGIC TYPE	HIGH	LOW
ECL	-0.8V(LOGICAL 0)	-1.6V(LOGICAL 1)
TTL	+3.6V(LOGICAL 1)	+0.8V(LOGICAL 0)
MOS	+20.0V(LOGICAL 1)	GROUND(LOGICAL 0)

Figure 1-8. ECL, TTL, and MOS Logic Levels

ECL CYBER170 MODULE POWER PIN DESIGNATIONS

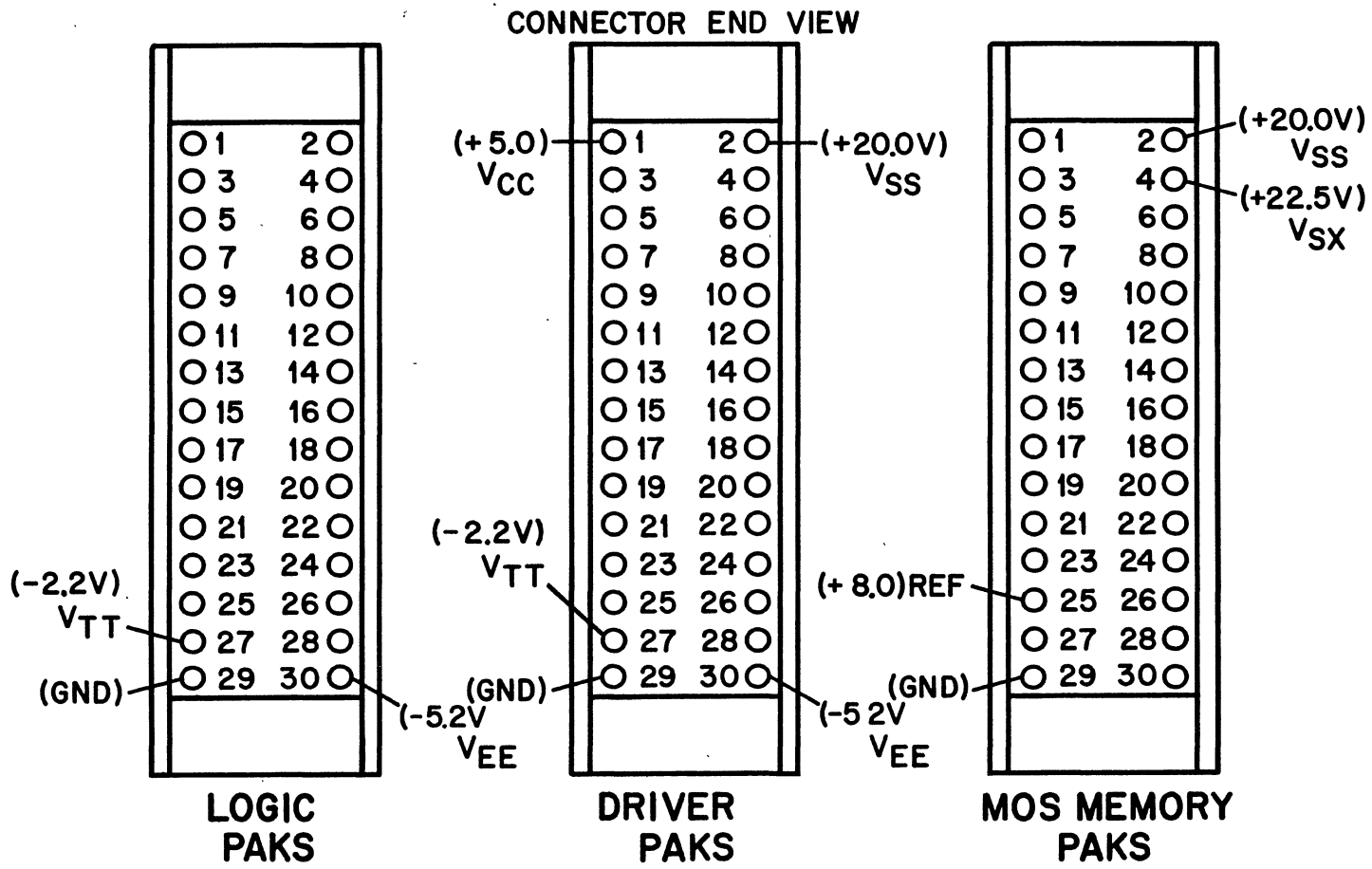


Figure 1-9. Power Pin Designators

LEARNING ACTIVITY 1-C. TEXT READING: MODULE HANDLING PROCEDURES

During this activity you learn the proper handling procedures for different types of CYBER 170 logic modules.

OBJECTIVE

- You will be able to describe the proper handling procedures for the logic modules.

Earlier in the module you learned that the logic modules have three different colors on their faceplates. A red faceplate indicates that the module contains MOS memory logic. A blue faceplate indicates that the module has TTL memory-drive logic. A black faceplate indicates that the module has ECL logic.

Because of the physical characteristics of the various types of logic, you need different guidelines for handling each type of module.

First of all, let us discuss handling of black faceplate modules. These modules require less care in handling than the other types. You may hold them in any manner without fear of damaging the logic. When you replace a black faceplate module in a logic chassis, you do not need to drop power to the chassis to replace it. Take care, however, when inserting a module into the logic chassis to be sure it is put in upright. If you insert a module upside down, you may damage the logic on the module. Otherwise, there are no special procedures for black-faced modules.

When working with blue-faced modules, you must be more careful. You need not be concerned with damaging the module by touching it, because TTL logic is fairly solid and reliable. The point at which caution is important in handling a blue-faced module is when replacing it in a logic chassis. When replacing a blue-faced module, you must power off the chassis before removing or inserting the module. If you fail to do so, you very likely will damage some portion of the logic in the chassis. You may not damage the module, but some other logic such as the memory or other driver cards. In summary, if you remember to power the chassis down before replacing a blue faceplate module, you should have no problems.

Red-faced modules require the most care. Because of the way MOS memory chips are constructed, they are very sensitive to static electricity. Therefore, you must not touch the pins of the memory chips or the pins of the module itself. When handling a red module, you should hold it by the faceplate. Then, you will not have to worry about damaging the module.

CYBER 170 ECL Logic
Learning Activity 1-C

When red-faced modules are shipped or stored, they are kept in a black bag that is made of an antistatic material. This protects the logic from being damaged when it is not in the machine. You should not remove the module from the bag until you are ready to put it into the logic chassis. The module that you remove from the chassis should be placed in the bag to protect it, also.

Like the blue-faced modules, the red-faced modules require that you turn off the power of the chassis before replacing a module in the machine.

All CYBER 170 logic modules are shipped individually in cardboard boxes designed especially for them. One end of the box has a cellophane window through which you can determine the type of module. Leave the modules in their boxes while storing them! This helps to prevent accidental damage to the modules.

If you follow the guidelines that you have learned during this activity, you should have few problems with damaged modules caused by mishandling.

POST TEST

When you have completed the learning activities assigned for Module 1, sign on to the PLATO terminal and take the Module 1 test.

Depending on the results of the test you will be told either to review some of the previous activities, or to go on to the Module 2 Pretest.

MODULE 2
ECL LOGIC SYMBOLOGY AND DIAGRAMS

During this module you learn the standard logic symbology and the functions of the various types of ECL logic circuits used in the CYBER 170. You also apply this knowledge to read logic diagrams. The diagrams you study are actual CYBER 170 logic diagrams taken from the CYBER 170 system manuals.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

The main objective of this module is to learn how to read logic diagrams. However, you also learn some concepts of the CYBER 170 operation. These concepts may help you during the CYBER 170 Maintenance course.

LEARNING ACTIVITIES

In the assigned column below, put a check mark by each activity assigned to you by PLATO Learning Management (PLM). Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	2-A	Audio/Microfiche: Key to Logic Symbols. During this activity you learn the standard symbology used in the CYBER 170 logic diagrams.	2-4
_____	_____	2-B	Exercise: ECL Logic Circuits - ANDs and ORs. During this activity you learn the functions of the various ECL AND gates and OR gates used in the CYBER 170 system.	2-9

LEARNING ACTIVITY 2-A. AUDIO/MICROFICHE: KEY TO LOGIC SYMBOLS

During this activity you learn the standard symbology used in CYBER 170 logic diagrams. During the remaining activities in this module you learn the functions of the ECL chips used in the CYBER 170. Each of the chips uses some of the symbols that are the topics of study in this activity.

OBJECTIVE

- You will be able to identify logic level symbols and tagging information for the ECL chips used in the CYBER 170.

Figures 2-1 through 2-3 show the symbols and give a brief definition of the function of each symbol.

The information in this activity is taken from the Engineering Standard for Logic Symbols. The manual for this standard is available through LDS. If you wish to know more about standard symbology, order the standard under the number, CDC-STD 1.41.104.

At this time load the microfiche labeled "Key to Logic Symbols," P/N 75444757, into your projector and the corresponding audiotape, P/N 75444754, into your cassette player and proceed with the activity.

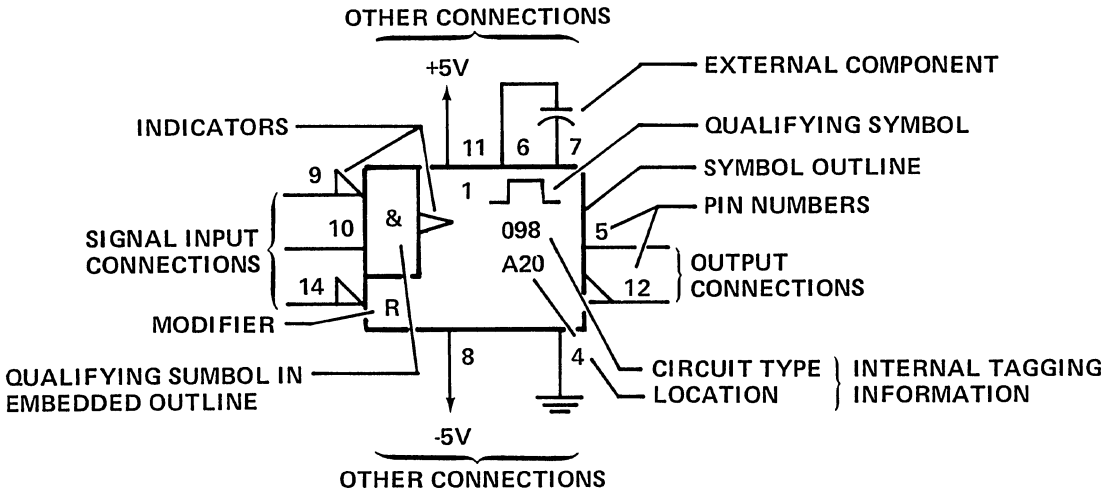


Figure 2-1. Example of Logic Symbol

SYMBOL	DEFINITION
&	AND - The output will assume its active state IFF (if and only if) all of the inputs assume their their active states.
& ◊	WIRED AND - Same as above except the AND function is accomplished by wiring outputs together rather than by using gates involving other active or inactive components. The output of a Wired And cannot be an input to a Wired Or.
1	OR - The output will assume its active state IFF one of more of the input(s) assume their active states.
1 ◊	WIRED OR - Same as above except the OR function is accomplished by wiring outputs together rather than using gates involving other active or inactive components. The output of a Wired Or cannot be the input of a Wired And.
= 1	EXCLUSIVE OR - The output will assume its active state IFF one (no more, no less) of the two inputs assumes its active state.
=	LOGIC IDENTITY - The output will assume its active state IFF all of the inputs assume their active state or if all of the inputs assume their inactive states.
2K + 1	ODD AND ONLY ODD - The output will assume its active state IFF an odd number (1,3,5....) of the inputs assume an active state. K represents any integer (0,1,2,3,....).
ALU	ARITHMETIC AND LOGIC UNIT (either or both) – A function performing arithmetic and/or logic functions, usually on group(s) of input(s) and providing output(s) according to functions defined internally in the symbol outline or in separate external tables.
MUX	MULTIPLEXER - A function or an array of functions in which control lines determine which one of several inputs is selectively routed to the output.
X→Y CODER	CODER (CONVERTER, TRANSLATOR) - A combinational logic function with multiple inputs and multiple outputs, in which the relationship between a particular set of input values and the resultant outputs is described by an appropriate weighting technique of modifiers or a reference table. Use of the functional name CODER is optional in places other than the neck of a common control block.
X MAX→Y CODER	PRIORITY CODER - A combinational logic function with multiple inputs and multiple outputs in which the resultant outputs are a representation of the active input with the greatest consecutive number modifier regardless of any other active inputs with weighting modifiers.

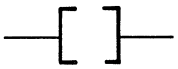
Figure 2-2. Key to Logic Symbols, Symbol Qualifiers (Sheet 1 of 2)

SYMBOL	DEFINITION
X/Y	SIGNAL LEVEL CONVERTER - A device that converts logic signals having a certain pair of physical states to corresponding logic signals having a different pair of physical states. It may be used to indicate a line driving or receiving function which does not change either of the two physical states such as voltage.
	REGISTER - An array of flip-flops having common input connections, such as reset, clock, or other gating functions.
	SHIFT REGISTER - m arrays of flip-flops, each comprised of m' bits. The shift register shall have at least one input that is used to transfer information in a specified direction from each bit position to another bit position. The direction of shifting data and the number of bit positions shifted by each successive shift signal are indicated by the input modifier which activates the shifting.
	COUNTER - An array of flip-flops in which the active and inactive states of the flip-flops represent a number, which may be either increased and/or decreased by certain inputs (designated +m, or -m), as the input(s) assume their active state(s). The sign and number used in the associated input modifier indicates whether the number stored is either incremental or decremental and by what amount when the input is active. The modulus of the counter is indicated by the number used to replace m.
	MEMORY - An addressable array of flip-flops in which input(s) and output(s) of data are multiplexed to and from selected bit positions. The number of addresses at which bits are located is indicated by the address (A) modifier suffixes in the common control block. The number of bits at each address is indicated by the number of flip-flops abutted vertically to the common control block.
	DELAY ELEMENT - The output will assume its active state only after a specific period of time m following the transition to the active state at the input. The output reverts to its inactive state only after a specific period of time m following the transition of the input to its inactive state. Where there are tapped delays and the delay time is equal in both directions, the appropriate unit of time shall replace m in the qualifying symbol, and the corresponding numerical value of delay used as a modifier with each output.
TERM	TERMINATOR - Used to terminate signals between one circuit and another.
DRVR	DRIVER (TRANSMITTER) - Twisted pair driver circuit. Places a differential voltage on a pair of transmission lines. The voltage relationship of the lines is determined by the state of input to the circuit.
RCVR	RECEIVER - Receives the twisted pair differential transmission signal and converts it to logic levels.
TR00	TRANSFORMER - Used when transmitting and receiving signals on a coaxial cable (single line transmission).
(No Qualifying Symbol)	FLIP-FLOP - A binary sequential logic element with two stable states. One of these is called the set state (or active state); the other is called the reset state (or inactive state). The active states of outputs correspond to the set state of the flip-flop. The inactive states of the outputs correspond to the reset state of the flip-flop. In most cases, flip-flops can be identified by one or more of the following input signal modifiers that are associated with flip-flops: C, D, J, K, R, S, or T. In a few exceptional cases where flip-flops are part of an array, such as some shift registers, these signal modifiers do not appear. However, in these situations it is obvious from the nature of the array that individual states are flip-flops.

Figure 2-2. Key to Logic Symbols, Symbol Qualifiers (Sheet 2 of 2)

SYMBOL	DEFINITION
D	Data Modifier - This is a data input that is always gated by a control (C) affecting input. The active state of the D input will cause the bi-stable element to take on its set (active) state and the inactive state will cause the bi-stable element to take on its reset (inactive) state.
R	Reset Input Modifier - A binary input that causes a flip-flop element to assume its reset condition when the R input is active. The return of the R input to its inactive state produces no action.
S	Set Input Modifier - A binary input that causes a flip-flop element to assume its set condition when the S input is active. The return of the S input to its inactive state produces no action.
+m	Incrementing Input Modifier - A binary input that causes the states of an array of flip-flops serving as a counter to change the binary number by +m each time the +m input is active. The return of the +m input to the inactive state produces no action. The counter is assumed to be cyclic such that the minimum value is the next number higher than its maximum value. The m is replaced by the appropriate integer, commonly 1.
-m	Decrementing Input Modifier - A binary input analogous to the +m input except that it causes the binary number to change by -m each time the -m input is active. The counter is assumed to be cyclic, and therefore, the maximum value is the next number lower than its minimum value.
→m	Shift Down (Right) Input Modifier - A binary input that causes the contents of an array of flip-flops to which it is connected to form a shift register, to shift m positions down (or right) each time the →m input is active. The return of the →m input to its inactive state causes no action. The m is to be replaced by an integer. The integer may be omitted if it is 1.
←m	Shift Up (left) Input Modifier - A binary input analogous to the →m modifier except that it causes the contents to shift m positions up (or left) each time the ←m input is active.
G	AND Dependency Modifier (Gate). A binary affecting input with an AND relationship to those inputs that are labeled with the same identifier. NOTE In inputs affected by both a G and C input, such as a data (D modifier) input, it is important to note that the And relationship is between G and the active state of the signal in. G does not affect control (C modifier) input(s).
C	Control Dependency Modifier (Clock)- A binary affecting input where more than a simple AND relationship is implied to those inputs or outputs that are labeled with the same identifier. In sequential binary functions, the C input is an affecting input to be used exclusively for data entry (D Modifiers) into bi-stable elements(s). The data entry is subject to the C input being active and the absence of other active inputs having an overriding and contradicting effect. When the C input is inactive, the outputs of the bi-stable element will be determined by conditions other than the state of the input(s) affected by the C input.
	Inhibit Input Modifier - A binary input that inhibits the active state of a logic function when the inhibit input is active regardless of the states of the other inputs. The inhibit input has no effect when it is inactive.

Figure 2-3. Key to Logic Symbols, Modifiers



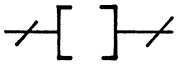
Implied Indicator - In polarity convention, the absence of the polarity indicator (▷) implies a static HI.

Polarity Indicator - In polarity convention, the polarity indicator indicates the active state is a static LO. It is not used for indicating negation between horizontally abutted symbols, or between an embedded symbol and the symbol it is embedded within.

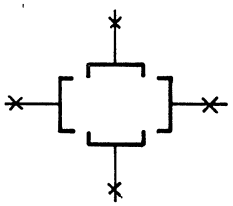
NOTE

When the polarity indicator is combined with the inhibit modifier, its position is as shown as follows:

Dynamic Active State Indicator - The active state is the transition from the inactive static state to the active static state (not merely the presence of the active static state). The transition from the active static state to the inactive static state has no effect.



Non-standard Binary Logic Level Indicator - Line carrying binary level or levels that differ from those defined as standard. All nonstandard levels used in an equipment are to be appropriately identified and defined on each and every sheet on which they appear.



Non-Binary and Non-Analog Indicator - Connection Line not carrying binary or analog information when necessary to distinquish it from other lines, and when no other indicators apply. This symbol is used for MOS levels in the CYBER 170.

Grouping Bracket - Two or more grouped lines, such as a differential pair, carrying only one bit of binary information and representing a single input. Lines within a group are required to maintain a fixed relation in state to each other (all lines active or all lines inactive according to applicable polarity indicators). The use of the grouping bracket on outputs is disapproved.

LO Output Only Indicator - The minus sign denotes that an element output is capable of supplying LOs only. A HI output must come from some other source.

HI Output Only Indicator - The plus sign denotes that an element output is capable of supplying HIs only. A LO output must come from some other source.

Figure 2-4. Key to Logic Symbols, Indicators

LEARNING ACTIVITY 2-B. EXERCISE: ECL LOGIC CIRCUITS—ANDS AND ORS

During this activity you learn the functions of the various ECL AND gates and OR gates used in the CYBER 170 system.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the ECL chips used as AND/OR gates in the CYBER 170.

Refer to page 10101 of the manual titled, ECL 10,000 Series Microcircuits, publication number 60417700, which is part of your course materials.

Note that the manual does not use a regular page numbering system. Instead, each page number is the actual vendor cross-reference number of the chip.

There is at least one page in the manual for each type of chip. Using page 10101 as an example, you find that the symbol for the circuit is drawn in both the negative and positive logic convention. Because the CYBER 170 diagrams are drawn in the negative logic convention, only those symbols will be referenced throughout this module.

Directly below the symbol is a mechanical drawing and vendor cross-reference block. The mechanical drawing is not very useful to anyone but a design engineer. To the right of the drawing is the Motorola number for the chip; directly below it is the CDC part number. While, in most cases, you will not be replacing chips on a module, these part numbers may be useful if you do need to order an individual chip.

In the left center of the sheet, you see the operational description block. This is useful when you are learning the basic functions of a symbol. As you become more capable of reading logic diagrams, you probably will not need to refer to the description as often.

To the right of the operational description is the function table or truth table of the circuit. This table tells you what the outputs of the circuit will be with given input conditions.

On the bottom of the page is the schematic diagram of the chip. You will seldom need to use it unless you want to redesign the machine.

One last note about the page. In the title block you will find the name of the circuit. (For example, the 10101 circuit is called a Quad Gate.)

CYBER 170 ECL Logic
Learning Activity 2-B

You will be using the ECL 10,000 Series Microcircuits manual throughout the remaining exercises in this module. During this exercise you will be studying the AND gates and OR gates used in the CYBER 170 system. Not all circuits are covered; only the circuits that are used in the CYBER 170 are topics for study in this exercise.

The format of this exercise consists of studying a particular circuit and then answering questions about the circuit. After you have answered the questions, check your answers with those at the end of this activity before going on to the next circuit.

If, at any time, you need to review a logic symbol, refer to the key to logic symbols (figures 2-1 through 2-4) in Learning Activity 2-A.

Exercise 2B-1: 10101 Circuit

Directions: Study the description of the 10101 chip in your manual, and then answer the following questions about the circuit. Remember that all questions refer to negative logic.

1. The 10101 chip has 4 AND gates.
2. Each gate has 2 inputs.
3. Pin number 12 is common to all gates of the 10101 chip.
4. If pin 10 and pin 12 are both LO, what will be the state of pin 11? low Pin 14? high
5. If pin 12 is HI, what will be the state of pin 3? low

Exercise 2B-2: 10102 Circuit

Directions: Study the description of the 10102 chip in your manual, and then answer the following questions.

1. A 10102 chip contains 4 gates.
2. Each gate has 2 inputs.
3. If the output of pin 9 is used, the function of its gate is a (an) and (AND/NAND).
4. If pin 6 is LO and pin 7 is open, what will be the state of pin 3? low
5. What is the CDC part number of a 10102 chip? 15112000

Exercise 2B-3: 10105 Circuit

Directions: Study the description of the 10105 chip in your manual, and then answer the following questions.

1. Each gate of the 10105 chip functions as an AND / NAND gate.
2. If pin 2 is LO, what is the state of pin 3? Hi
3. What does the + (plus sign) next to each output pin mean? the output only
4. If pins 9, 10, and 11 are all LO, pin 6 will be Hi.

Exercise 2B-4: 10107 Circuit

Directions: Study the description of the 10107 chip in your manual, and then answer the following questions.

NOTE

When the qualifying symbol is an =1 the function of the gate is an exclusive OR. When the symbol is just an = it is an exclusive NOR or equivalence circuit.

1. How many gates are in a 10107 chip? 3
2. Pin 4 is LO and pin 5 is HI. What is the state of pin 2? [illegible]
3. Pins 14 and 15 are both HI. What is the state of pin 13? Low
4. Pin 7 is grounded and pin 9 is open. What is the state of output pin 11? [illegible]

Exercise 2B-5: 10109 Circuit

Directions: Study the description of the 10109 chip in your manual, and then answer the following questions.

1. How many gates are on a 10109 chip? 2

2. What kind of gates are they? and

3. Pin 14 is LO if any input is HI. (True/false)

Exercise 2B-6: 10117 Circuit

Directions: Study the description of the 10117 chip in your manual. Note that there is a logic diagram that may help you understand its operation. When you have studied the description, answer the following questions.

NOTE

The 10117 is a multifunction gate. In negative logic, it performs an AND/OR function of the input.

1. How many OR gates are on one 10117 chip? 2

2. How many AND gates? 2

3. Which pin is common to two AND gates? 9

4. What is the equation for output pin 2 = LO?
(Pin 4. Pin 5)+(Pin 6. Pin 7. Pin 9)

NOTE

Sometimes a 10117 chip will be used to form a latch type of circuit. Refer to figure 2-5. Let us call the AND gate (made of pins 9, 10, and 11) the set gate and the AND gate (for pins 14 and 15) the clear gate. By connecting pin 15 to pin 13 you can make a holding path for the latch (providing that pin 12 is a LO level) until you want to clear the latch. To set the latch you must have pins 9, 10, and 11 LO. This makes pin 15 LO. With pin 15 LO AND pin 13 LO (clear), the bottom AND gate is made, and the output on pin 15 is HELD LO. Now the inputs on pins 9, 10, and 11 can go to any state with no change in he output. In other words, you have latched up the gate. This condition remains until pin 13 goes HI. At that time, the bottom gate is broken and the output at pin 15 goes HI.

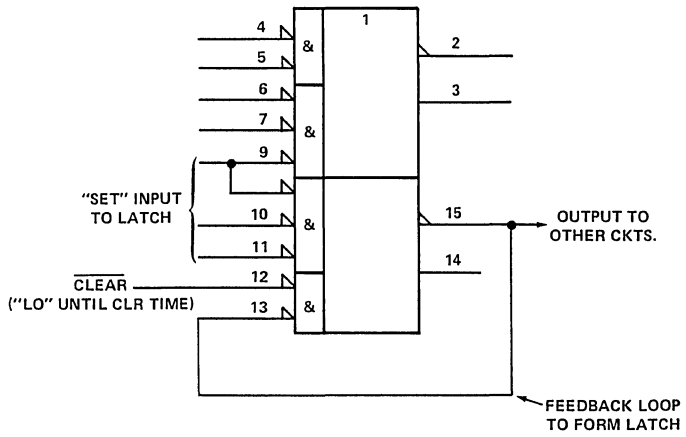


Figure 2-5. 10117 Chip Used as a Latch

Exercise 2B-7: 10121 Circuit

Directions: Study the description of the 10121 chip in your manual, and then answer the following questions.

1. What is the difference between a 10121 circuit and a 10117 chip?
4 and gates feeding 1 or gate 2 and gates feeding 1 or gate 2 separate sections

2. Write the equation that would produce a LO on output pin 2.
4·5·6 + 7·9·10 + 11·12·13 + 13·14·15

3. Could a 10121 be used as a latch? If so, how? Yes
pin 2 to any input pin

This concludes the exercise on ECL AND gates and OR gates. The circuits you have learned appear throughout the CYBER 170 logic diagrams. In addition, the concepts of these gates are used in the circuits that you learn about in the next activities in this module.

ANSWERS FOR LEARNING ACTIVITY 2-B

EXERCISE 2B-1

1. 4

2. 2

3. Pin 12

4. Pin 11 = LO.
   Pin 14 = HI.

5. LO; the gate is not made, so pin 6 = HI and pin 3 = LO.

EXERCISE 2B-2

1. 4

2. 2

3. AND

4. HI; remember an open is equal to a one or a LO.

5. 15118000

EXERCISE 2B-3

1. AND/NAND

2. HI; it is always the complement of other output from the gate.

3. The output is capable of supplying HIs only. A LO output comes from some other source (usually the input of the next circuit).

EXERCISE 2B-4

1. 3

2. LO; unlike inputs make pin 2 LO.

3. LO; like inputs make it so.

4. LO; remember: open pin = LO = 1; grounded pin = HI = 0.

EXERCISE 2B-5

1. 2

2. AND/NAND

3. True; any HI input breaks the gate.

EXERCISE 2B-6

1. 2

2. 4

3. Pin 9

4. (Pin 4 Pin 5)+(Pin 6 Pin 7 Pin 9); either AND gate being made will give a LO on pin 2.

EXERCISE 2B-7

1. The 10121 chip has four AND gates feeding one OR gate. The 10117 has two sections; each section has two AND gates feeding one OR gate.

2. (Pins 4·5·6)+(Pins 7·9·10)+(Pins 10·11·12)+(Pins 13·14·15).

3. Yes; connect output pin 2 to one of the input gates. The latch would have three set input gates.

LEARNING ACTIVITY 2-C. EXERCISE: ECL LOGIC CIRCUITS—FLIP-FLOPS AND REGISTERS

During this activity you learn the functions of ECL flip-flops and register circuits.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the ECL chips used as flip flops and registers in the CYBER 170.

The format of this exercise is the same as in the previous activity. Use the ECL 10,000 Series Microcircuits manual, publication number 60417700, as a reference. After studying a circuit, answer the questions. Check your answers with those at the end of this activity before going on to the next circuit.

NOTE

Remember to refer to the negative logic symbol in the manual.

Exercise 2C-1: 10130 Circuit

Directions: Study the two-page description of the 10130 chip in the ECL 10,000 Series Microcircuits manual. This circuit is rather complex, but the questions and answers will guide you through the description. After you have read the description, answer the following questions.

1. What type of circuit is found in a 10130 chip? D type F F

2. What does the CD by pins 7 and 10 mean? Clocked data

3. Using the function table for reference, list the function of each of the following pins for a 10130 chip.

   a. Pin 6 - Clock enable

   b. Pin 9 - Common clock

   c. Pin 5 - Reset

   d. Pin 4 - Set

   e. Pin 7 - Data

f. Pin 2 - output

g. Pin 3 - output

4. In order for the top latch to be clocked, pins 6 and 9 both must be LO.

5. If both clock signals are LO, and if the D input is LO, what will be the state of pin 2? low

6. The output is latched on the (positive/negative) transition of the clock. This is the (leading/trailing) edge of the clock.

7. If pin 4 is HI, what happens to the flip-flop? force set

8. A LO on pin 12 would have what effect on the flip-flop? force reset

NOTE

Because the circuit timing diagram in the ECL 10,000 Series Microcircuits manual may require some explanation, figure 2-6 shows the same diagram with notes attached.

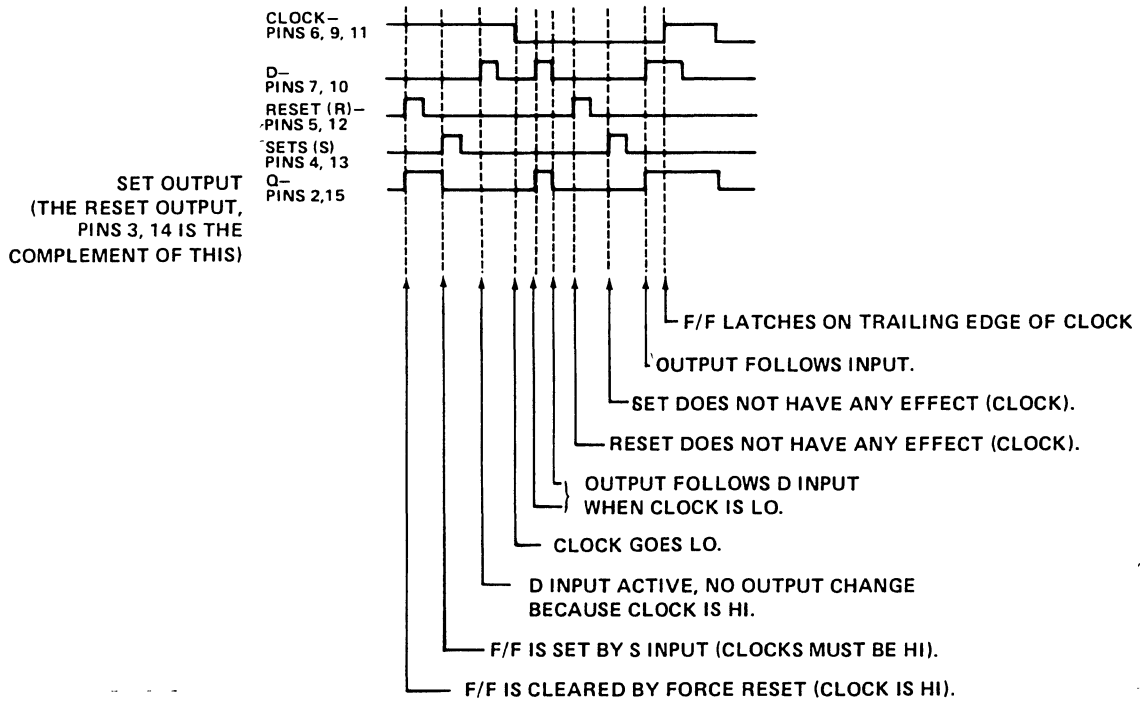


Figure 2-6. 10130 Chip Timing Diagram

Exercise 2C-2: 10131 Circuit

Although the 10131 and 10130 chips have some similarities, there are also differences between the two. Read the two-page description of the 10131 circuit in the ECL 10,000 Series Microcircuits manual. See if you can detect some of the differences. Then answer the following questions.

1. Are there any differences in pin assignments between a 10131 and a 10130 chip? If so, what differences? no differences in pin assignment

2. What is the meaning of the horizontal triangle (]>C) by the clock input? Clock on clock switch only

3. The set and reset inputs of a 10131 chip will override the clock inputs. (True) false)

4. The output states of the flip-flop change on the positive transition of the clock.

NOTE

Figure 2-7 is the circuit timing diagram from the manual with some explanations of the signals.

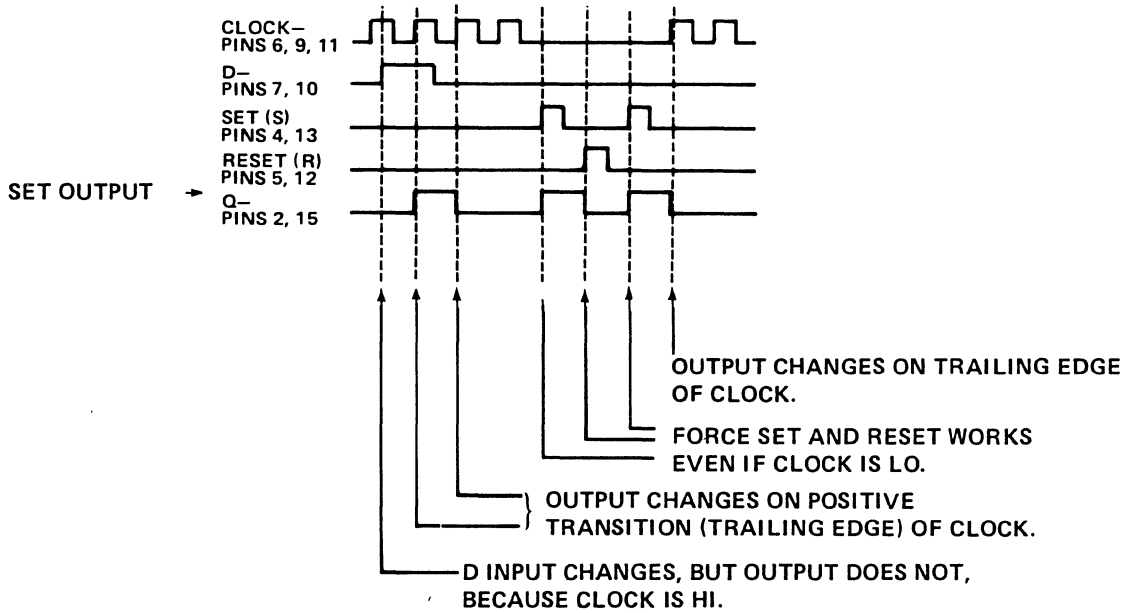


Figure 2-7. 10131 Circuit Timing Diagram

NOTE

Figure 2-8 shows the way the 10131 circuit most often appears in the CYBER 170 logic diagrams. It still works the same way except that pin 9, which is common to both F/Fs, is connected to the common control block.

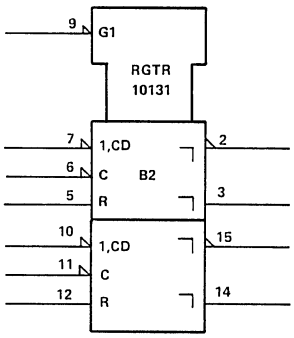


Figure 2-8. 10131 Symbol

Exercise 2C-3: 10133 Circuit

Directions: Study the description of the 10133 chip in your manual. Then answer the following questions.

1. A 10133 circuit contains 4 latches.

2. The D inputs on pins 3 and 7 are controlled by the clock on pins 4 and 13.

3. The outputs on pins 11 and 15 are controlled by the G term on pin 10.

4. The latches store data on the negative edge of the clock.

5. The outputs are not available until the G terms are low (HI/LO).

6. As long as the G terms are HI the latch outputs are low (HI/LO).

NOTE

Figure 2-9 shows the circuit timing diagram of a 10133 chip with some explanatory notes.

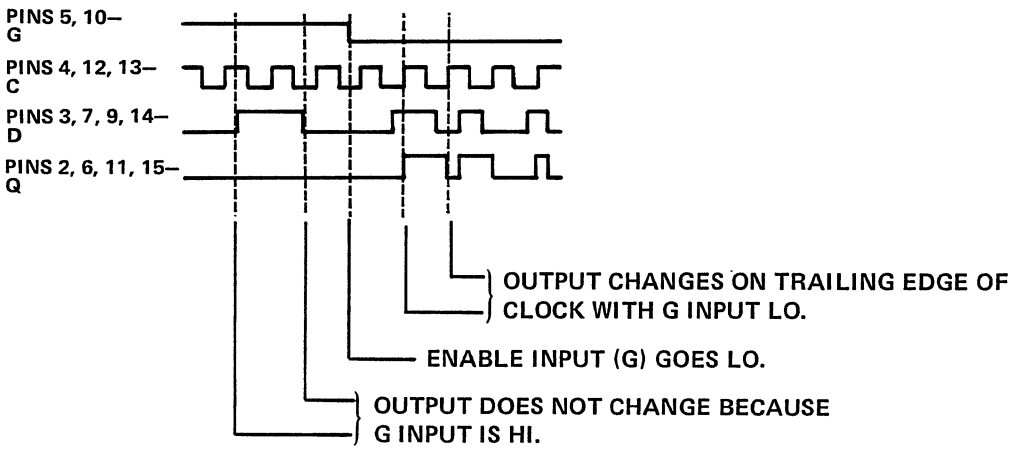


Figure 2-9. 10133 Circuit Timing Diagram

This concludes the exercise on ECL flip-flops and registers. You were not required to study the J-K type of flip-flops because they are not used in the CYBER 170 system. You may read their descriptions, however, if you wish.

ANSWERS FOR LEARNING ACTIVITY 2-C

EXERCISE 2C-1

1. Two clocked, type D, latching flip-flops.

2. The D means that it is the data input to the flip-flop; the C means that the data is clocked by the C input.

3. a. Pin 6 - Clock enable or gate.

   b. Pin 9 - Common clock.

   c. Pin 5 - Force reset input.

   d. Pin 4 - Force set input.

   e. Pin 7 - Clocked data input.

   f. Pin 2 - Set output = LO when F/F is set.

   g. Pin 3 - Reset output = HI when F/F is set; reset output = LO when F/F is reset.

4. 6, 9

5. Pin 2 will be LO. Remember that the output follows the input when clock is LO.

6. Positive, trailing; do not forget that this is negative logic (LO=1).

7. The F/F is forced set, providing that both clock pins (6, 9) are not LO.

8. No effect; a HI state is required to force reset to F/F. (Note that there is no triangle on the line.)

EXERCISE 2C-2

1. No differences in pin assignment functions.

2. It means that no gating takes place except on the transition of the clock.

3. True; this is different from the 10130 chip.

4. Positive transition (trailing edge).

EXERCISE 2C-3

1. 4

2. 4, 13; the C2 by pins 4 and 13 correspond to the C2 in the top two latches.

3. 10; the 3 by pins 11 and 15 correspond to the G3 by pin 10.

4. Trailing edge; the trailing edge is the falling edge in negative logic.

5. LO

6. LO

LEARNING ACTIVITY 2-D. EXERCISE: ECL LOGIC CIRCUITS—COUNTERS AND SHIFT REGISTERS

During this activity you learn how the ECL logic counter and shift register work.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the ECL chips used as counters and shift registers in the CYBER 170.

A description of these circuits appears in the ECL 10,000 Series Microcircuits manual, publication number 60417700.

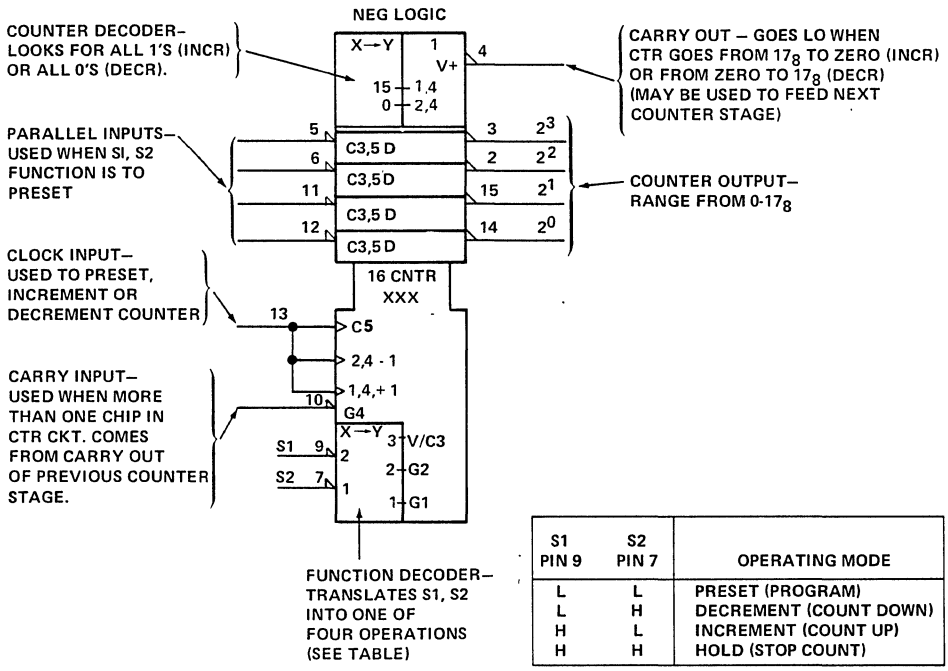
This exercise has the same format as the two previous activities. After you have studied a circuit, answer the questions about the circuit. Check your answers with those at the end of this activity before going on to the next circuit.

Exercise 2D-1: 10136 Circuit

Directions: Study the description of the 10136 chip in the ECL 10,000 Series Microcircuits manual. Refer to figure 2-10 for an explanation of the purpose of various parts of the circuit. Then answer the questions about the circuit.

NOTE

Be sure to look at the signal relationships on sheet 2 of the description.



S1 PIN 9	S2 PIN 7	OPERATING MODE
L	L	PRESET (PROGRAM)
L	H	DECREMENT (COUNT DOWN)
H	L	INCREMENT (COUNT UP)
H	H	HOLD (STOP COUNT)

Figure 2-10. 10136 Universal Hexadecimal Counter Circuit

1. What does the 16 CNTR symbol mean? 4 bit counter

2. In order to preset the counter, the S1 and S2 terms must be in what states?

   a. S1 = LO

   b. S2 = LO

3. The counter changes state on the positive transition of the clock.

4. The carry out of pin 4 goes LO only when incrementing from all ones to all zeros. (True/false)

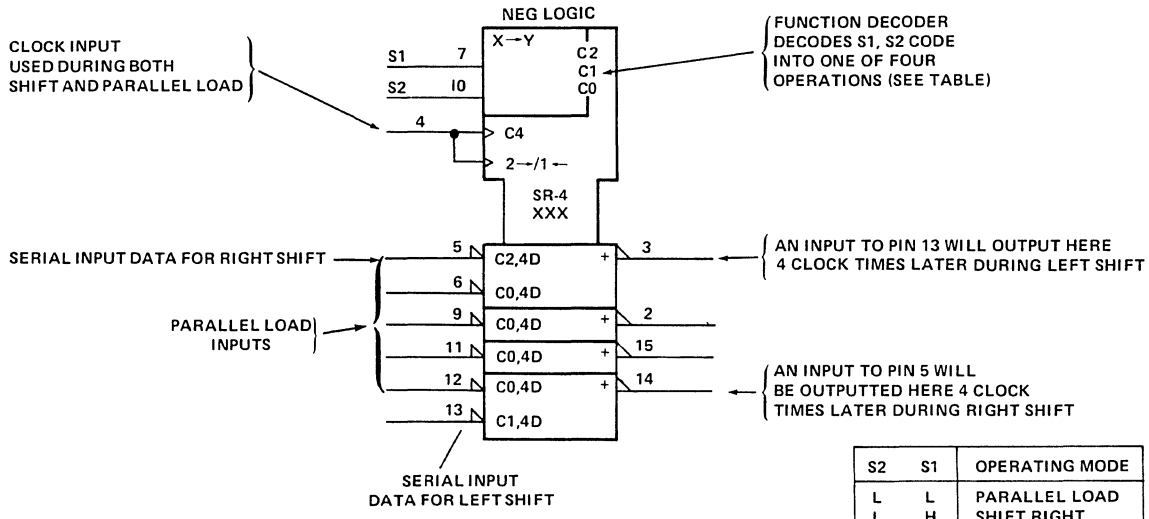
5. Each flip-flop in the counter symbol has the term, C3, 5D. What does the term mean? C3 preset data and clock apply to the D latch

6. Which output pin is the output of the most significant bit of the counter? Pin 3

7. Pin 7 is HI; pin 9 is LO; pin 4 is LO. What is the state of the counter? Counter is decrementing from 0000 to 1111

Exercise 2D-2: 10141 Circuit

Directions: Study the description of the 10141 chip in your manual. (Figure 2-11 may help you understand the purpose of the various sections of the circuit.) Then answer the questions about the circuit.



S2	S1	OPERATING MODE
L	L	PARALLEL LOAD
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	HOLD

Figure 2-11. 10141 4-Bit Left/Right Shifter Circuit

CYBER 170 ECL Logic
Learning Activity 2-D

1. Data appears at the outputs of the circuit after the positive transition of the clock pulse.

2. During a right shift, how many clock times after data is input to pin 5 will it appear at outpin 15? 3 clock times

3. Pin 7 is LO, pin 10 is HI. What is the function of the circuit? shift left

4. What function select code is necessary to make use of pin 11 of the circuit?

   S1 = LO

   S2 = LO

NOTE

Be sure to look at the circuit timing diagram for the 10141 chip.

This concludes the activity on the ECL counter and shift register. Because of the multiple functions that each is capable of doing, there is only one of each kind in the ECL 10,000 series logic.

ANSWERS FOR LEARNING ACTIVITY 2-D

EXERCISE 2D-1

1. The CNTR means that the circuit is a counter and the modulus of the counter is 16_{10} (4 places).

2. a. LO

   b. LO

3. Positive (trailing edge)

4. False; also during decrementing from 0000 to 1111 and during preset.

5. The D latches are affected by a select code of 3 (preset); the 5 is from the C5 by pin 13 (clock).

6. Pin 3 = 2^3bit.

7. The counter is decrementing and is going from 0000_2 to 1111_2.

EXERCISE 2D-2

1. Positive

2. 3

3. Left shift

4. LO

   LO

   (Pin 11 is only used during a parallel load.)

LEARNING ACTIVITY 2-E. EXERCISE: ECL LOGIC CIRCUITS—CODERS AND MULTIPLEXERS

During this activity you learn the functions of the various ECL circuits that can perform encoding, decoding, and multiplexing operations.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the ECL chips used as coders and multiplexers in the CYBER 170.

The circuits are described in the ECL 10,000 Series Microcircuits manual, publication number 60417700.

The format of this lesson is the same as in the previous activities. When you have answered the questions about a circuit, check them with the answers at the end of this activity before going on to the next circuit.

Exercise 2E-1: 10160 Circuit

Directions: Study the description of the 10160 chip in the ECL 10,000 Series Microcircuits manual. This chip is used in all parity generation and checking circuits in the CYBER 170 system. The symbol that is used is the negative logic one with a 2K+1 qualifying symbol. After you have studied the circuit, answer the following questions.

1. The size of the input word to the 10160 chip is 12 bits.

2. Unused inputs to the circuit should be uncommitted.

3. The input word is 1257_8. What is the state of pin 2? High

Exercise 2E-2: 10161 Circuit

Directions: Study the description of the 10161 chip in the ECL 10,000 Series Microcircuits manual. This circuit is used mainly as a decoder in the CYBER 170 system. Most instruction translation circuits have several of these chips to decode the instruction that is to be executed. After studying the circuit, answer the following questions.

1. What is the meaning of the symbol on the lines to pins 2 and 15? inhibit input

2. Pin 14 is LO, pin 9 is HI, and pin 7 is LO. Which output pin is active? 4

3. The input to the circuit is a code of 2_8. Which output pin will be active? 12

4. Pin 14 is open; pin 9 is LO; pin 7 is HI; pin 2 is HI. Which output pin is active? none

5. Pin 6 is LO. What is the input code? 111

Exercise 2E-3: 10164 Circuit

Directions: Study the description of the 10164 chip in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

1. What is the function of pins 7, 9, and 10 in the circuit? select output

2. Which input pin will be gated through to the output if the code on pins 7, 9, and 10 is equal to 5_8? 4

3. Pin 13 input is to be gated to the output. What are the states of pins 7, 9, and 10?

   Pin 7 = LO

   Pin 9 = HI

   Pin 10 = HI

Exercise 2E-4: 10165 Circuit

Directions: Study the description of the 10165 circuit in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

1. The input to pin 10 is HI; the other seven inputs are LO. What is the state of the output pins?

   Pin 15 = LO

   Pin 2 = HI

Pin 3 = HI

Pin 14 = HI

2. With all inputs LO, what is the state pin 14? LO

3. Pins 10, 11, 12, and 13 are all HI. What is the binary output code? 5₈

NOTE

An application of the 10165 priority encoder is in the central memory control section of the CYBER 170 system. You should recall that CMC handles requests to use central memory from the other sections of the mainframe on a priority basis. The requests go to a 10165 chip in CMC. CMC looks at pin 14 to see if a request is already present. If there is a request present, it blocks additional requests. When a new request is accepted, CMC allows the circuit to function. At that time the highest order request will be encoded and placed in the chips output latches. Then, CMC can look at the code and determine where the request came from. This code becomes the tag code that you learned about in the Overview course.

Exercise 2E-5: 10173 Circuit

Directions: Study the description of 10173 chip in the ECL 10,000 Series Microcircuit manual. Then answer the following questions.

1. How many latches are on a 10173 chip? 4

2. Each latch has 2 inputs.

3. Which pin determines which input to the latches is to be used? 9

4. The output of the latches follows the inputs when the clock is LO.

5. Pins 4, 6, 11, and 13 are used as the input. Pin 9 must be HI (HI/LO).

This concludes the exercise on ECL coders and multiplexers. As you continue this course, you will come to some applications for these circuits.

ANSWERS FOR LEARNING ACTIVITY 2-E

EXERCISE 2E-1

1. 12

2. Left open (open = 1).

3. HI; there already is an odd number of one bits in the word (1257_8 = 001 010 101 111_2).

EXERCISE 2E-2

1. Inhibit input. The inputs must be LO to allow the circuit to operate.

2. Pin 4 - the input code = 5_8.

3. Pin 12

4. None; because pin 2 is HI, which inhibits the circuit.

5. 7_8 = 111_2 = pins 14, 9, and 7, all LO.

EXERCISE 2E-3

1. They select which input line data will be gated to the output of the chip.

2. Pin 4

3. Pin 7 = LO

   Pin 9 = HI Select code = 001

   Pin 10 = HI

CYBER 170 ECL Logic
Learning Activity 2-E

EXERCISE 2E-4

1. Pin 15 = LO
   Pin 2 = HI
   Pin 3 = HI
   Pin 14 = HI

   Code = 4_8

2. LO

3. 5_8; pin 13 is highest order HI input.

EXERCISE 2E-5

1. 4

2. 2

3. Pin 9

4. LO

5. HI

LEARNING ACTIVITY 2-F. EXERCISE: ECL LOGIC CIRCUITS ARITHMETIC LOGIC UNIT

During this activity you learn the various functions of the ECL Arithmetic and Logic Unit (ALU) circuits. There is one type of ALU chip used throughout the CYBER 170 system. Any time that you see an adder, it will be using this type of ALU circuit.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the ECL chips used as arithmetic logic units in the CYBER 170.

The format of this lesson is the same as in previous activities. The descriptions of the circuits are locted in the ECL 10,000 Series Microcircuits manual, publication number 60417700. After reading the description, answer the questions about the circuit. Check your answers with those at the end of the activity before going on to the next circuit.

Exercise 2F-1: 10181 Circuit

Directions: Study the description of the 10181 ALU chip in the ECL 10,000 Series Microcircuits manual. Figure 2-12 in your student manual may help you understand the purpose of the various sections of the circuit. Then answer the questions about the ALU.

NOTE

Be sure to look at the notes below the active low inputs function table.

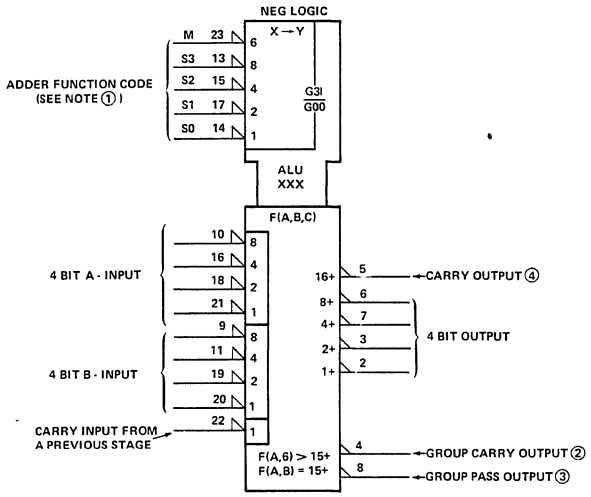


Figure 2-12. 10181 Arithmetic Logic Unit Circuit

COMMENTS

① The code on S0, S1, S2, and S3 inputs determines the function that the ALU is to perform. The M input is the 2^4 bit of the code. It determines if the function is a logical operation (M = HI) or an arithmetic operation (M = LO).

Example: An ALU function code of 11_8 (01001_2) tells the circuit to do an exclusive OR of the A and B inputs.

② The group carry is generated if there is a carry generated within the group and it is not satisfied within the group. The carry in to pin 22 is not included in the function.

Example:
1010_2 = A input
0111_2 = B input
Carry Out $\overline{0001}$ = Sum

The carry generated in this stage is not satisfied within the group.

(3) The group pass is generated if all stages within the group are enable (pass) stages. In effect, it says that the two inputs are the complement of each other.

```
Example:        1010 = A input
                0101 = B input
  Group pass    1111 = Sum
  Output
```

All stages are passes (unlike).

(4) Pin 5 is a carry output that includes the carry in on pin 22. It will be active in the same conditions as those described in comment (2). It will also be active if there is a carry in on pin 22, and if there are all passes within the group.

NOTE

There are 32 different functions that the ALU is capable of performing. However, in the CYBER 170 system, adders only use 10 of the functions. The codes that are used are listed in figure 2-13.

CODE	SYMBOL	DEFINITION
00_8	F = A	A input straight through to output
01_8	F = A+B	Inclusive OR of A and B inputs
04_8	F = A·B	AND (Logical Product) of A and B
05_8	F = B	B input straight through to output
10_8	F = A·$\overline{B}$	AND of A and the complement of B
11_8	F = A⊕B	Exclusive OR of A and B
12_8	F = $\overline{B}$	Complement of B input to the output
14_8	F = 00	Output of ALU is forced to zeros
26_8	F=A-B-1	Subtract A minus B
31_8	F=AplusB	ADD - Output = sum of A plus B

Figure 2-13. ALU Functions Used in the CYBER 170

CYBER 170 ECL Logic
Learning Activity 2-F

1. The 10181 ALU chip can perform operations on two 4 -bit numbers.

2. If the A input is 1001_2 and the B input is 0101, what are the states of pin 4 and pin 8? The adder code = 31_8.

   Pin 4 = H1

   Pin 8 = H1

3. What is the function of pin 22? Carry in

4. If the ALU function code is 31_8, what operation is being performed? G3

5. The A input is 0100_2, the B input is 0111_2, and the ALU function code is 00_8. What is the output of the chip? 0100

6. What ALU function code causes the circuit to pass the complement of A straight through the adder? 1111

7. The A input is 0000_2; the B input is 1111_2; the ALU function code is 11_8; what is the output of the circuit? 1111

Exercise 2F-2: 10179 Circuit

The symbol for the 10179 Carry Look-Ahead circuit in the ECL 10,000 Series Microcircuits manual is confusing because it is drawn differently from the drawing in the CYBER 170 logic diagrams. The symbol in figure 2-14 is the way the circuit is drawn in the CYBER 170 logic.

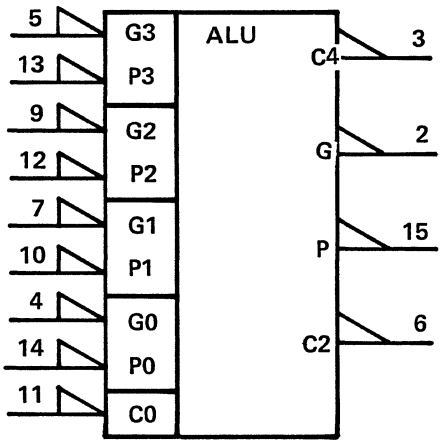


Figure 2-14. 10179 Carry Look-Ahead Circuit Symbol

The 10179 chip is used with the 10181 ALU circuit when a large adder is made. As you recall from the previous exercise, the ALU outputs a group carry and/or group pass for the four bits in its group. Those two signals are the inputs to the 10179 chip. By grouping the groups, the adder can quickly determine where carries and passes are. Consequently, the result of the arithmetic operation is achieved faster. Figure 2-15 gives you an idea of how the 10179 is used in conjunction with the 10181 ALU circuits.

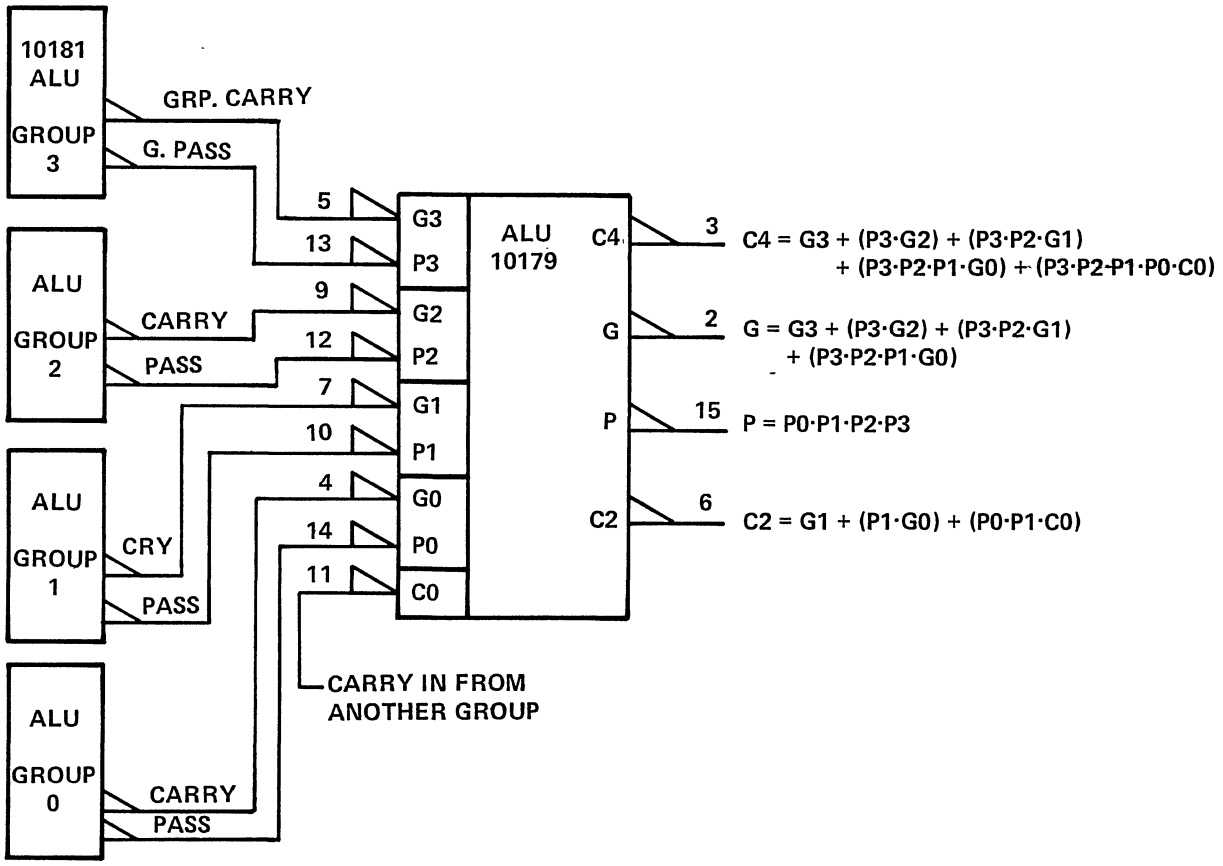


Figure 2-15. 10179 Circuit with Equations

Directions: Study the operational description, and look at the function table for the 10179 chip in the ECL 10,000 Series Microcircuits manual. You should be able to correlate the equations in figure 2-15 with the function tables. Then answer the following questions.

1. The 10179 circuit is always used in conjunction with 10181 circuit.

2. Pins 13, 12, 10, and 14 of the 10179 chip are all LO. Which output pin is active? 6

3. What is the difference in output of pin 3 (C4) and the output of pin 2 (G)? P0, P1, P2, P3, C0
same result as C4 includes above

4. Each G and P input to the 10179 circuit is a group signal. How many bits are in each group? 4

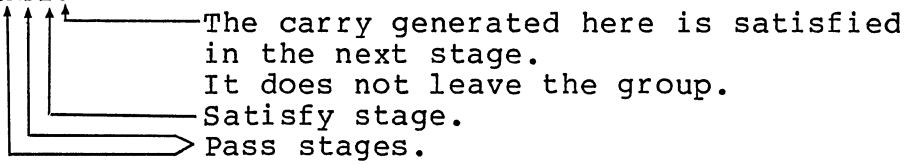
This concludes the activity on the ECL Arithmetic and Logic Unit circuits. You will see these circuits in a logic diagram application in a future learning activity.

ANSWERS FOR LEARNING ACTIVITY 2-F

EXERCISE 2F-1

1. 4

2. Pin 4 = HI A = 1001
   Pin 8 = HI B = 0101
   SUM = 1110



3. Carry input from another group.

4. An ADD function (sum of A plus B).

5. 0100_2; A function of 00_8 says the output is the A input.

6. 17_8; M = HI, S0, S1, S2, and S3 = LO.

7. 1111_2; an 11_8 code is an exclusive OR of A and B. (Unlike stages output a 1.)

EXERCISE 2F-2

1. 10181 ALU

2. Pin 15; the p output is active if all groups contain passes.

3. C4 says a carry was generated within the groups and not satisfied in the groups. It also is active when all groups contain passes and there is a carry in (CO) from another group. G means the same as C4 except it does include the CO and all passes condition.

4. 4 bits; each ALU handles two 4-bit numbers.

LEARNING ACTIVITY 2-G. EXERCISE: ECL LOGIC CIRCUITS—MISCELLANEOUS

During this activity you learn the functions of some ECL circuits that do not perform logical functions, but are necessary to support the basic ECL logic circuits.

OBJECTIVE

- You will be able to identify the symbols used and list the functions of the remaining ECL chips used in the CYBER 170.

These circuits are described in the ECL 10,000 Series Microcircuits manual, publication number 60417700.

The format of this exercise is the same as in the previous activities. After studying a circuit, answer questions about its operation. Then check your answers with those at the end of the activity before going on to the next circuit.

Exercise 2G-1: 10124 Circuit

The 10124 circuit is a level converter. It converts TTL logic levels to ECL levels. These circuits are used in the CYBER 170 to interface the TTL memory drivers with the ECL logic sections of the system.

Directions: Study the description of the 10124 circuit in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

NOTE

The negative logic symbol is on the right hand side.

1. What does the slash (/) symbol on the input lines indicate? ~~Inverted Signal~~

2. Which pin is common to all four sections of the circuit? 6

3. In TTL logic a HI is equal to +1.8 - 5.0 volts and a LO is equal to +1.1 volts.

4. If pin 11 is LO, what are the states of pins 14 and 13?

   Pin 14 = LO

   Pin 13 = HI

Exercise 2G-2: 10125 Circuit

The 10125 circuit is an ECL to TTL converter. It is used in the CYBER 170 system to convert ECL signals to TTL levels for the TTL memory driver circuits.

Directions: Study the description of the 10125 chip in the ECL 10,000 Series Microcircuits manual. (The right hand symbol is for negative logic.) Then answer the following questions.

NOTE

Pin 1 (-1.29 Voltage Regulator) is usually tied to input pins 2, 6, 10, and 14. This provides the bias voltage to the grouped input of each section of the circuit.

1. What does the bracket by each set of input pins mean?
   a differential receiver

2. If pin 3 is an ECL one, what is the state of pin 4?
   LO = 0 TTL

3. If pin 11 is open, what is the state of pin 12?
   LO = 0 TTL

CYBER 170 ECL Logic
Learning Activity 2-G

Exercise 2G-3: 10114 Circuit

The 10114 circuit is a long line receiver. It is most commonly used as a receiver when transmitting signals from one chassis to another.

Directions: Study the description of the 10114 circuit in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

1. What does the (∪) symbol on pin 11 indicate? Ref. voltage output

2. If pin 5 is LO and pin 4 is HI, what are the states of pins 2 and 3?

   Pin 2 = L

   Pin 3 = HI

Exercise 2G-4: 10192 Circuit

The 10182 circuit is an ECL Driver. It supplies a differential output that is used as a transmitter when sending signals from one chassis to another.

Directions: Study the description of the 10192 circuit in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

1. What does the arrow (↕ P) symbol on the output lines indicate? twisted pair

2. Which input pins are used to produce an output on pins 14 and 15? 9, 10

Exercise 2G-5: TR00 Circuit

The TR00 circuit is a pulse transformer. These circuits are primarily used to transmit and receive over coaxial cables because of the length of the cables.

Directions: Study the description of the TR00 circuit in the ECL 10,000 Series Microcircuit manual. Then answer the following question.

1. What conditions are necessary to transmit a signal?

   Pin 1 = Ground

   Pin 8 = open

   Pin 9 = open

   Pin 16 = Ground

Exercise 2G-6: DL17 Circuit

The DL17 circuit is a tapped delay line. It is most commonly used to form one-shot pulses in conjunction with other logic circuits. It also delays timing pulses in special timing operations.

Directions: Study the description of the DL17 circuit in the ECL 10,000 Series Microcircuits manual (near the back of the manual). Then answer the following questions.

1. The maximum delay available through a DL17 circuit is 17.5 NS. nanoseconds.

2. What is delay time from input pin 2 to output pin 5? 11.5 NS

3. A 50-nanosecond pulse on input pin 7 would result in a 41-nanosecond pulse at output pin 4. (True/false) FALSE

Exercise 2G-7: Resistor Circuits

There are two types of resistor chips used in the CYBER 170. They are called the R100 Terminator Module and the R500 Pull-Down Resistor Module.

All signals between logic modules must be terminated at the receiving end. Consequently, most modules have some of these circuits on them. In a future activity you learn when each of the two resistor chips is used.

CYBER 170 ECL Logic
Learning Activity 2-G

Directions: Study the descriptions of the R100 and R500 circuits in the ECL 10,000 Series Microcircuits manual. Then answer the following questions.

1. What is the symbol for the R500 circuit? Term

2. An R100 circuit has 12 resistors; each has a resistance of 100 ohms.

3. What is the size of the resistors in an R500 circuit? How many are there? 500 ohms 14

4. What is the supply voltage for the R100 circuit? -2.2

5. The R500 circuit uses 5.2 volts.

This concludes the activity on miscellaneous ECL circuits. You will see these circuits in a logic diagram application in a future learning activity.

ANSWERS FOR LEARNING ACTIVITY 2-G

EXERCISE 2G-1

1. The slash (/) symbol indicates that the logic level is non-standard for the machine. In this case it means TTL. In the logic diagram there will be a footnote that identifies which logic level is non-standard.

2. Pin 6; it is usually tied to a +5vdc in the machine.

3. +3.6v to +5 volts; 0v to +.8v.

4. Pin 14 = LO (ECL Logical 1).

   Pin 13 = HI (ECL Logical 0).

EXERCISE 2G-2

1. The bracket indicates that the circuit is a differential (twisted pair) receiver.

2. Pin 4 is a TTL zero (TTL-LO = zero).

3. Pin 12 = LO (OPEN INPUT = LO).

EXERCISE 2G-3

1. It is the symbol for a reference voltage. Pin 11 has a stable reference voltage of -1.29v.

2. Pin 2 = HI

   Pin 3 = LO

EXERCISE 2G-4

1. The arrow (↕P) symbol indicates that the outputs are paired; the difference of current between the two pins is the signal being transmitted.

2. Pin 10 and pin 9 (F1).

EXERCISE 2G-5

1. Pin 1 = ground

   Pin 8 = open

   Pin 9 = open

   Pin 16 = ground

EXERCISE 2G-6

1. 17.5

2. 11.5 nanoseconds

3. False. The pulse duration does not change because the DL17 delays both ones and zeros. The pulse would be delayed by 9.0 nanoseconds but not shortened in width.

EXERCISE 2G-7

1. TERM

2. 12; 100

3. 500 ohms; 14

4. -2.2vdc at pin 1

5. -5.2vdc

LEARNING ACTIVITY 2-H. TEXT READING: BASIC LOGIC DIAGRAM LAYOUT

During this activity you learn some of the ways to read a CYBER 170 logic diagram. Most of the logic diagrams have a basic format. During this lesson you learn what the various parts of the logic diagram are and how to use them.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

Figure 2-16 is a typical logic diagram from the CYBER 170. The logic on the diagram is very simple in operation and will be described later in this lesson.

Each unique aspect of the drawing in figure 2-16 has a circled number pointing to it. A description of each identified item follows the drawing.

At this time use the descriptions and the logic diagram to study the basic parts of the diagram. When you finish, read the circuit description of the logic on the module which follows the notes about the diagram.

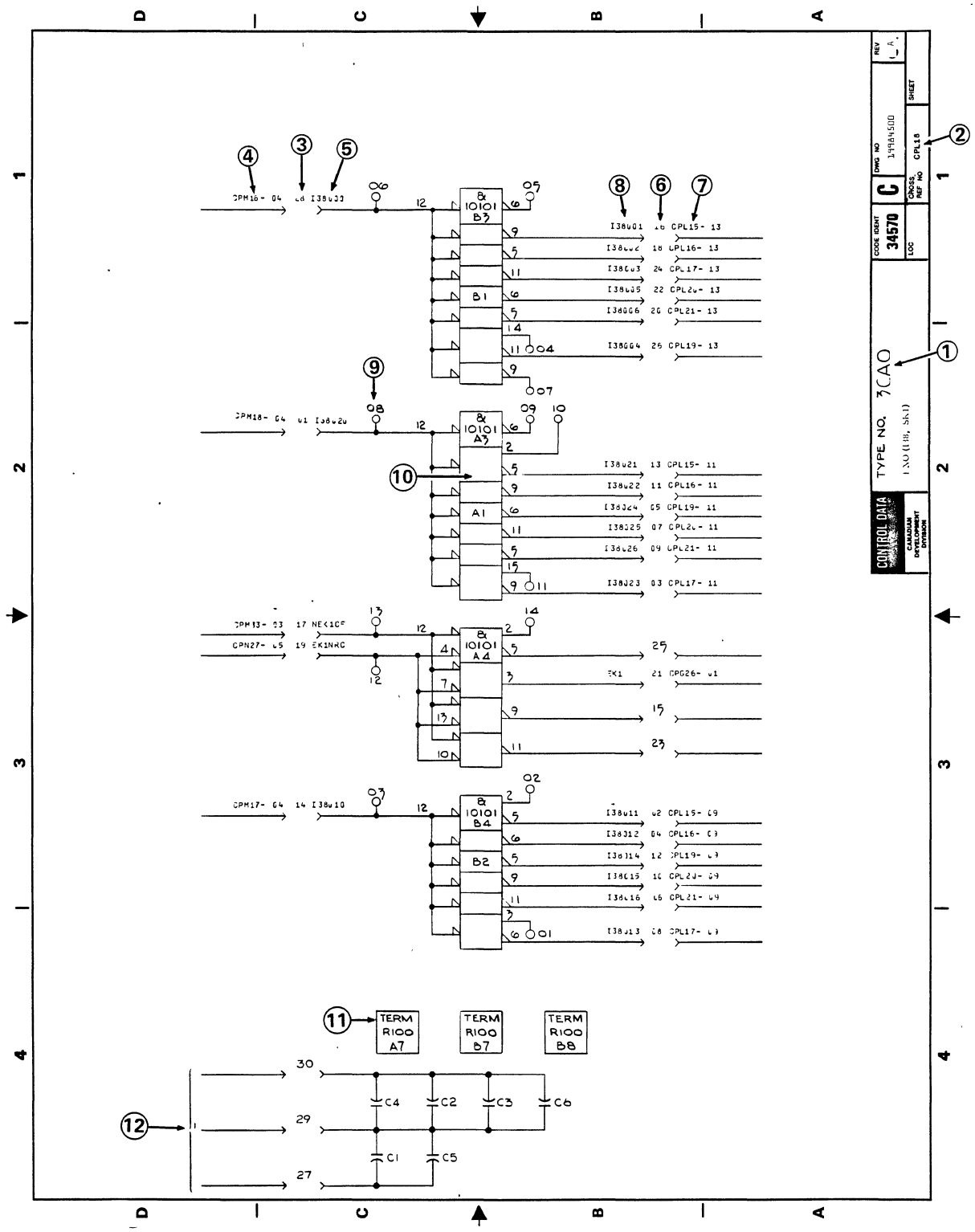


Figure 2-16. Typical CYBER 170 Logic Diagram

These notes correspond to the numbered circles in figure 2-16.

(1) MODULE TYPE - The module type is a four-digit number that has the following format:

```
3CA0
|||└ Manufacturing Division Code
||└  0 = Toronto
||   7 = Arden Hills
|└ Module type - corresponds to type on module
|                faceplate.
└ Design year - a type of revision level. The 3
                means the circuit was designed in
                1973.
```

(2) MODULE POSITION - The position is a five-character code using the following format:

```
CPL18
|||└┴ The position of the module in the logic row
|||    (42 positions available)
||└ The logic row in the chassis (A through R)
|└ The chassis the module is in:
|    CP = Central processor unit (chassis 1)
|    PP = Peripheral processor subsystem (chassis 2)
|    CS = Central storage unit (chassis 3)
|    CM = Central memory control (chassis 4)
```

(3) INPUT PIN NUMBER - The pin number of the module where the signal enters. Input pins are always on the left side of the logic diagram.

(4) INPUT SIGNAL ORIGIN - The module location and pin number where the signal originated. In this example the signal comes from the CPU chassis, location M16, and pin 4 of the module in that location.

(5) INPUT SIGNAL NAME - The input signal name is usually a six-character mnemonic code that defines the function of the signal. As you learn the various sections of the mainframe, the meaning of the signal name becomes very useful in reading logic diagram.

(6) OUTPUT PIN NUMBER - The pin number of the module where the signal leaves it. The output pins are always on the right side of the logic diagram.

⑦ OUTPUT SIGNAL DESTINATION - The location and pin number of the module where the signal is going. This signal is going to pin 13 of the module at location L15 in the CPU chassis.

⑧ OUTPUT SIGNAL NAME - The output signal name is usually a six-character mnemomic code that identifies something about the function of the signal.

⑨ TEST POINT - This is the standard symbol for a test point. Each module has a maximum of 14 test points connected to selected signals (input or output) on the module.

⑩ ABUTTED SYMBOLS - There are two separate 10101 circuits represented by this one symbol. The top three gates are in location A3 of the module, and the bottom four gates are in location A1. This convention is used frequently in the logic diagrams to save space and to combine signals with similar functions.

⑪ TERMINATORS - The terminator circuits that are found on most modules usually will not have any lines into or out of them. They are being used, but for the sake of readability of the diagrams, the lines are not drawn to them.

⑫ POWER INPUT AND FILTER CIRCUIT - Each module has a filter circuit for the power that it uses in its logic circuits. The pin assignments for ECL modules (black faceplates) are: pin 29 = ground, pin 27 = -2.2vdc, and pin 30 = -5.2vdc.

The items that have been described here are found on almost every module diagram in the CYBER 170 system. When you study other diagrams, you will see different conventions that are used for specific applications. These will be described as you see them.

The following is a description of the logic circuits of the 3CA0 module.

The logic on a CA module is very simple in operation. The basic function of the circuit is to fan-out signals that drive many load circuits.

Look at the top circuit first. The circuits in locations B3 and B1 of the module are 10101 chips. A 10101 chip is a quad two-input AND gate. Pin 12 is common to all four gates of the circuit. In this example, pin 12 is the only input pin used by the two circuts. The other input pins are left open and are not even shown on the diagram. Remember, an open input is the same as a LO signal. Therefore, whenever the signal I38000 (the input signal to pin 12 of the chip) is active (LO), the outputs of the eight gates at B1 and B3 will be

active. There is no change to the function of the signal. The only thing that was accomplished was to get several outputs from one input.

The circuits at A3 and A1 function exactly the same way, except that they have a different input signal (I38020). So do the circuits at B4 and B2.

The circuit at A4 works a little differently. In this chip we are using both inputs of the AND gates. The signal, "NEK1CF," feeds pin 12 of the chip, and the signal, "EK1NRC," feeds each gate at pins 4, 7, 13, and 10. When both input signals are active (LO), the output on pin 3 goes HI (no triangle on pin 3). The name of the output signal is EK1, and it is connected to pin 21 of the module.

At the same time, the outputs on pins 5, 9, and 11 are LO. There are no output signal names for these pins, because they are not used in the machine. However, they are available if they are needed.

This concludes the lesson on basic logic diagram layout. The information you have learned in this activity will be used in the next few exercises on logic diagrams.

LEARNING ACTIVITY 2-I. EXERCISE: FAN OUT AND CONTROL DIAGRAMS

During this activity you have an opportunity to practice reading CYBER 170 logic diagrams. The diagrams in this lesson are fairly simple to analyze because they do not have much complex logic.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

After you study a logic diagram, answer the questions about it. Check your answers with those at the end of the activity before going on to the next diagram. You may use your Key to Logic Symbols and your ECL 10,000 Series Logic manual whenever you need to know the type of circuit.

NOTE

> The signal names on the diagrams are simply letter codes rather than the mnemonic codes that are used in the CYBER 170 manuals. The main objective of the lesson is to learn to read logic, not to decode signal names.

Exercise 2I-1: Fanout Circuit

Directions: Study the logic diagram in figure 2-17. Then answer the following questions about it.

1. What is the module type? 3FX0
2. Where is the module located? CPF12
3. How many terminator circuits are on the module? 4
4. What is the location on the module of the circuit that is connected to output pin 25? A3
5. If you looked at TP-08 with an oscilloscope, what signal would you be looking at? B

6. Write the logic equation for each of the following pins.

a. A1-6 = $A \cdot B$

b. A4-5 = $A \cdot B$

c. B3-5 = $A \cdot C$

d. B6-11 = AC

e. B1-5 = C

f. TP-03 = $\overline{A \cdot C}$

g. TP-10 = $\overline{AB}$

h. TP-04 = C

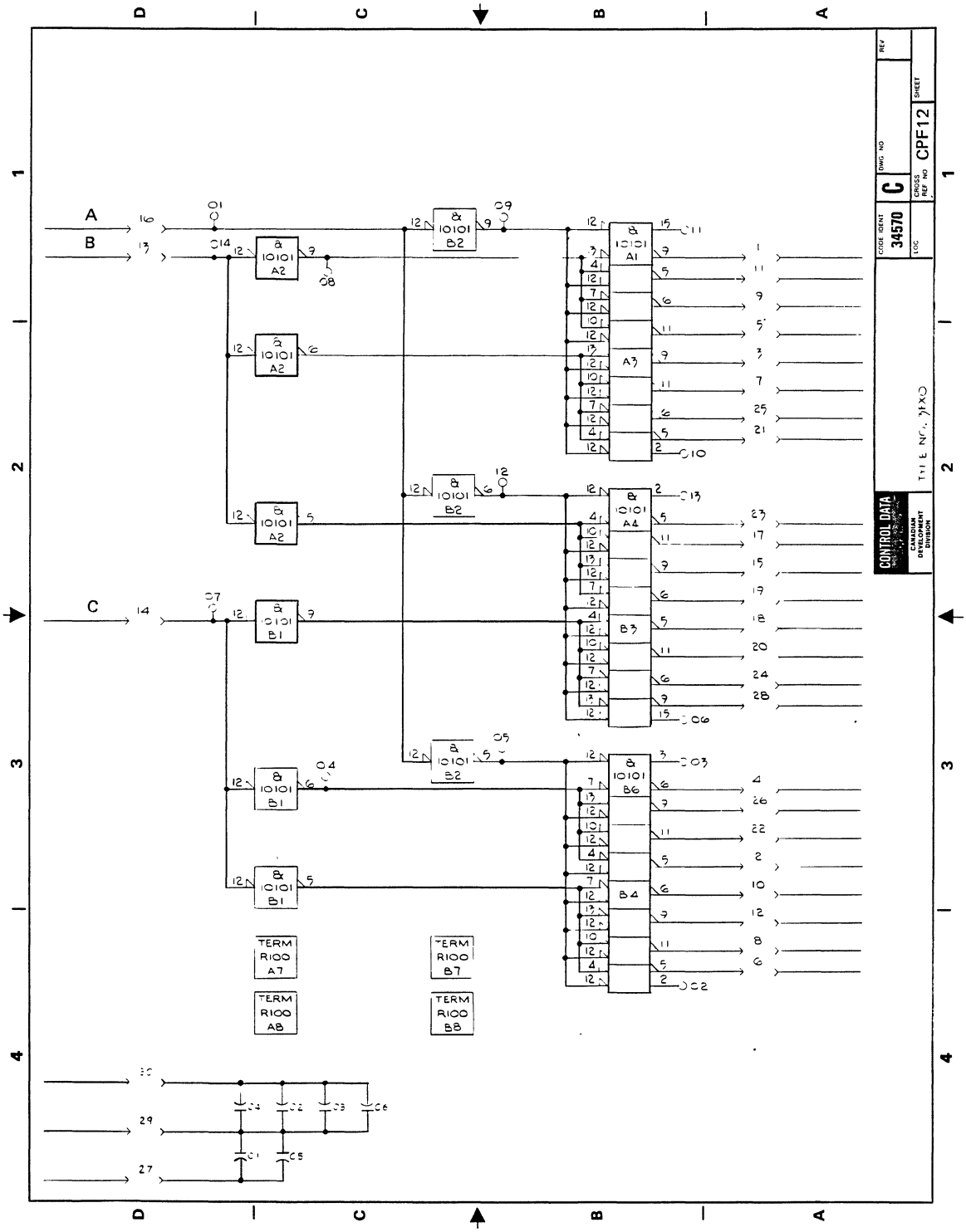


Figure 2-17. Fanout Logic Diagram

Exercise 2I-2: Control Logical Diagram

Directions: The logic diagram that is used in this exercise is taken from a control section of the CYBER 170 system. Study the logic in figure 2-18. Then answer the following questions about its functions.

1. What is the pack type in figure 2-18? 3GC0
2. What logic row is it in? PP R01
3. What is always connected to pin 29? GROUND
4. How many chips are on the module? 7
5. What is the signal on TP-06? S
6. Write the equation for each of the following pins or test points.
   a. A2-2 = $\overline{ABCD}$
   b. PPR01-04 = $\overline{U \cdot W X}$
   c. B1-2 = KLMN
   d. TP-10 = PRST
   e. TP-03 = EFGHJ
   f. A1-3 = $\overline{ABCD}$ $\overline{EFGHJ}$
   g. TP-11 = ABCDEFGHJKLMNPRST

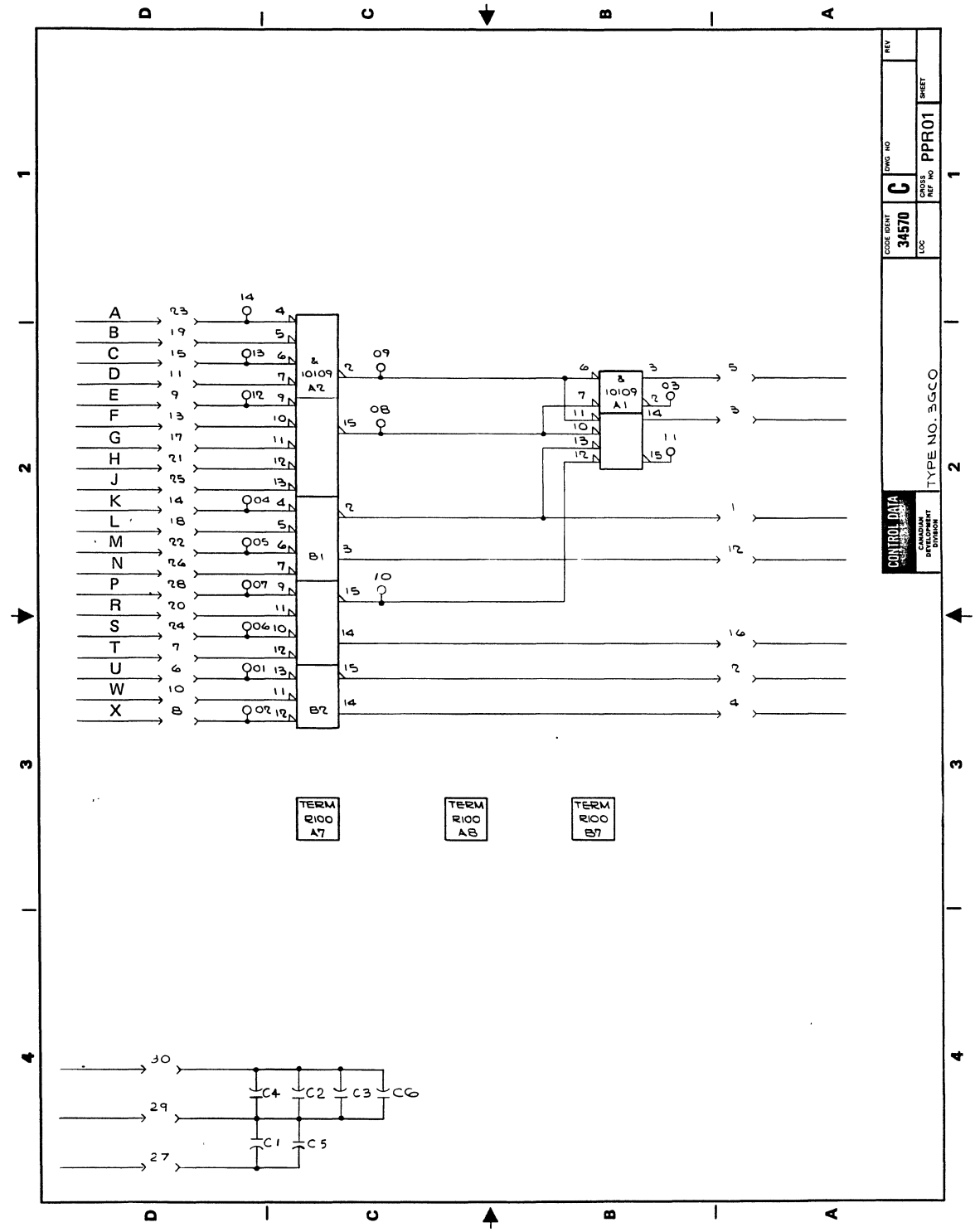


Figure 2-18. Control Logic Diagram

Exercise 2I-3: Control Logic Diagram

Directions: Figure 2-19 has some different logic circuits on it. Study it, then answer the following questions.

1. What is the module type? 4BFO

2. Write the equation for each of the following pin numbers or test points:

   a. TP-11 = $\overline{E}$

   b. A2-2 = $A\overline{E} + BC\overline{E} + BD$

   c. A5-2 = $A\overline{E} + BC\overline{E} + BD$

   d. B5-15 = $FG + H$

   e. B3-3 = $\overline{FG + H}$

   f. B2-2 = $XY + Z$

   g. CPG03-08 = $\overline{Z}$

   h. CPG03-07 = $XY\overline{Z}$

This concludes the activity on fanout and control diagrams.

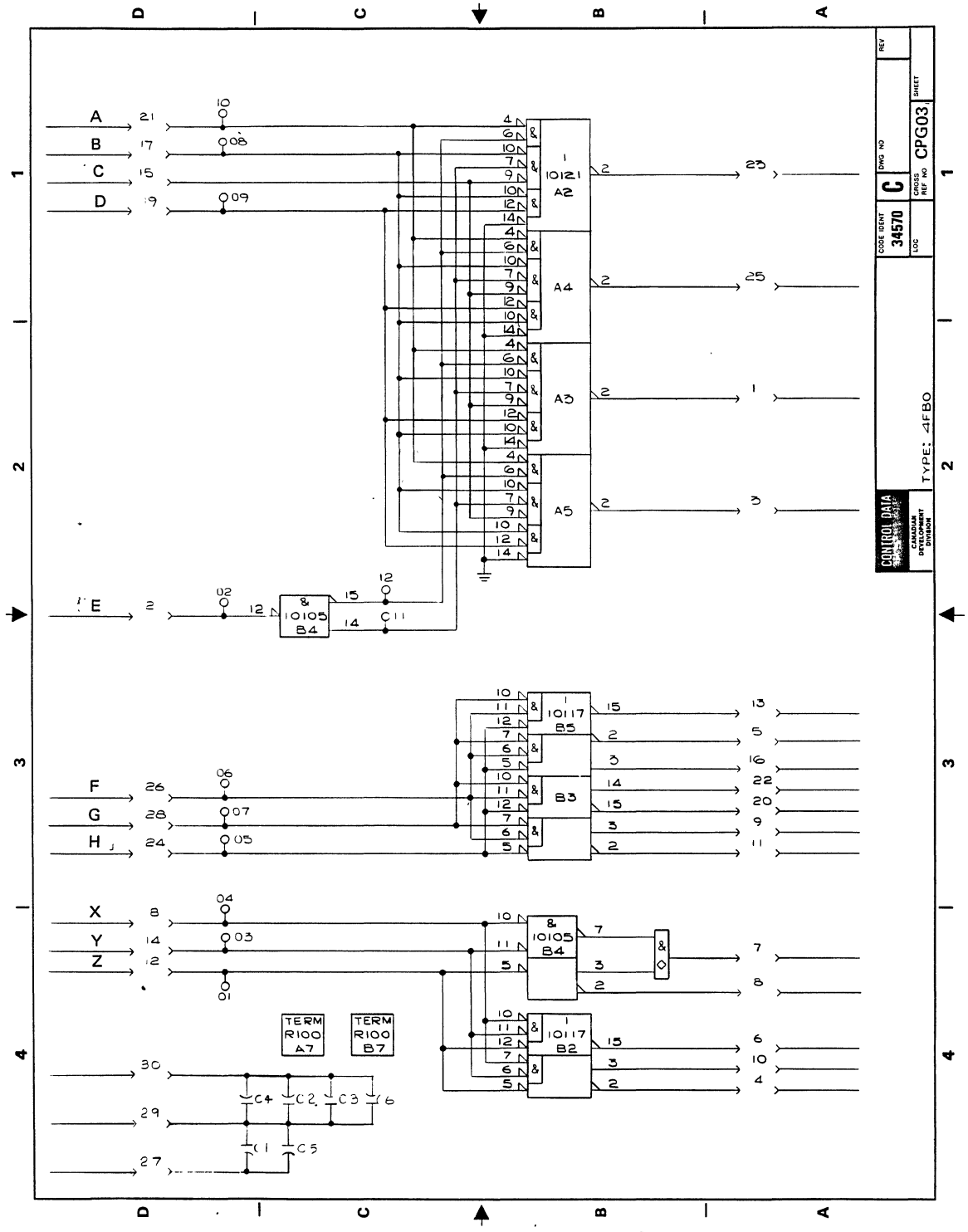


Figure 2-19. Control Logic Diagram

ANSWERS FOR LEARNING ACTIVITY 2-I

EXERCISE 2I-1

1. 3FX0 or FX
2. CPF12 - location F12 in the CPU chassis.
3. 4
4. A3
5. B
6. a. A1-6 = $A \cdot B$
   b. A4-5 = $A \cdot B$
   c. B3-5 = $A \cdot C$
   d. B6-11 = $A \cdot C$
   e. B1-5 = C
   f. TP-03 = $\overline{AC} = \bar{A}+\bar{C}$
   g. TP-10 = $\overline{AB} = \bar{A}+\bar{B}$
   h. TP-04 = C

EXERCISE 2I-2

1. 3GC0 or GC
2. Row R
3. Ground
4. 7 - A1, A2, B1, B2, A7, A8, and B7.
5. S
6. a. A2-2 = $A \cdot B \cdot C \cdot D$ or ABCD
   b. PPR01 - 4 = $\overline{U \cdot W \cdot X}$ or $\bar{U}+\bar{W}+\bar{X}$ (Output pin 4 from module).
   c. B1-2 = $K \cdot L \cdot M \cdot N$

d. TP-10 = $P \cdot R \cdot S \cdot T$

e. TP-03 = ABCDEFGHJ or $(ABCD) \cdot (EFGHJ)$

f. A1-3 = $\overline{ABCDEFGHJ}$

g. TP-11 = ABCDEFGHJKLMNPRST

EXERCISE 2I-3

1. 4FB0 or FB

2. a. TP-11 = $\bar{E}$

b. A2-2 = $(A \cdot E) + (B \cdot C \cdot \bar{E}) + (B \cdot D)$

NOTE

Pin 14 is grounded; consequently, that section of each 10121 chip is disabled.

c. A5-2 = $(A \cdot E) + (B \cdot C \cdot \bar{E}) + (B \cdot D)$ (Same as A2-2).

d. B5-15 = $(F \cdot G) + H$

e. B3-3 = $\overline{(F \cdot G) + H}$

f. B2-2 = $(X \cdot Y) + Z$

g. CPG03-08 = Z

h. CPG03-07 = $[(X \cdot Y) \cdot \bar{Z}]$; - That is a <u>wired</u> AND gate.

LEARNING ACTIVITY 2-J. EXERCISE: DECODER DIAGRAMS

During this activity you learn how logic can be used to decode the contents of a register and generate control signals based on those contents.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

The format for this exercise is the same as in the previous activity. After studying a logic diagram, answer questions about its operation. Check your answers with those at the end of the activity before going on to the next diagram.

Exercise 2J-1: PPU Instruction Decoder

Figure 2-20 is the logic diagram for one of the modules used to decode instructions in the CYBER 170 PPS. You should recall that the PPU register that holds instructions is the K register. The K register is 9 bits long. The upper 6 bits (2^3 - 2^8) are the instruction, and the lower 3 bits (2^0 - 2^2) are the trip count.

Certain actions must occur during the execution of an instruction. The BL module decodes the contents of the K register and generates the necessary control signals to enable the correct actions to occur.

There is a convention used on the BL diagram that you have not yet seen called Signal Bundling. When a logic diagram has many signal lines on it, the signal bundling technique is used to make it easier to read the logic. On the BL module the heavy line running through the middle is the bundle. Any line that touches it at an angle is going into or out of the bundle. The angle of the line touching the bundle indicates the direction to look for its exit. Of course, in order to find both ends of a signal line, the inputs and outputs of the bundle must be labeled.

Here is an example:

1. Find A6-pin 3 (in the lower left). The output of A6-3 is labeled XX4.

2. XX4 enters the signal bundle at an up angle. This means that the output of the bundle is somewhere higher on the page.

3. The first place that XX4 goes when it leaves the bundle is to the B5-pin 4. The angle of that line is downward, which means it came from lower on the page.

4. XX4 also feeds A5-pin 15 and A5-pin 12.

A line that touches the bundle at both an up and down angle indicates that the signal goes in both directions. Finally, it a line crosses the bundle at right angles, it means that signal does not use the bundle.

Here is an example of how the module works to detect a shift instruction.

1. The PPU code for a shift instruction is $=10_8$. Because the shift instruction requires only one memory cycle to execute, the trip count has no significance to it.

2. Locate pin 08 of the module (lower right). It is labeled shift. Pin 08 comes from B6-2. It is a two-input AND gate.

3. The input to B6-4 is 1XX, which comes from the 10161 circuit at B2-11. B2 is decoding the upper 3 bits of K, which holds the upper bits of the instruction.

4. The input to B6-5 is X0X, which comes from A2-10. A2 decodes bits 2^3-2^5 of K, which are the lower 3 bits of a 6-bit PPU instruction code.

5. The output of B6, then is (1XX·X0X), which, if put in simpler form, is 10X. The 10 means shift, and the X means the decode does not care what it is.

Directions: Answer the following questions, then check your answers with those at the end of this activity.

1. What is the code on pin 9 of A3? Where does that signal come from?

   A3-9 = X3X

   Originating pin = A2-13

2. When is the signal "Q to B" generated? 2XX

3. For what instructions is the signal WRITE (pin 11) generated?

   624 637

4. When will the signal "PINC" be generated? (Output pin 10)

   612·FLAG 711

5. For what instructions will the signal "DCOM" occur? (Output pin 13) 03X 04X 05X 06X 07X
2XX+3XX·36X·37X

6. What is necessary to generate the signal "F to B?" (Output pin 24) 2XX + 3XX·36X+3YY·37X

7. What is the difference between "D to B" and "F to B?" 1XX + 2XX + 3XX·36X + 3XX·37X

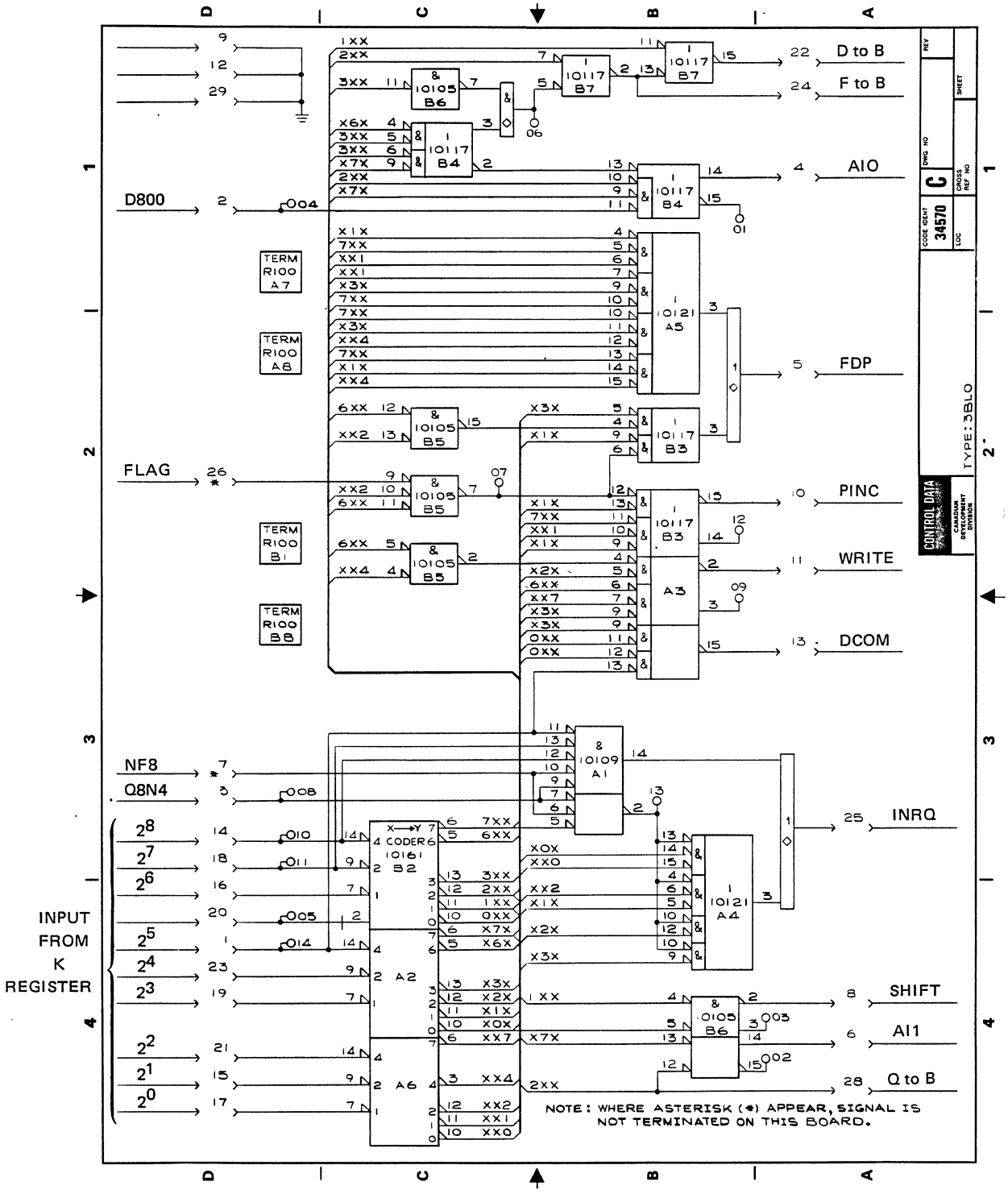
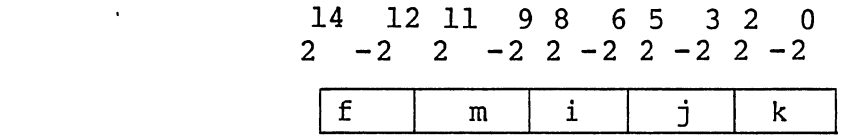


Figure 2-20. PPU Instruction Coder

Exercise 2J-2: CPU Instruction Decoder

Figure 2-21 is the logic diagram of a 6FK0 module. It is used to decode instructions in the CPU section of the CYBER 170.

Here is a quick review of the instruction format in the CPU. The basic instruction designators are f, m, i, j, and k in this configuration.



Each designator is 3 bits. The f and m portions or f, m, and i portions tell the CPU what to do. The j and k portions are operand registers, and the i portion designates the result register, in most cases. There are times when the i portion is part of the instruction itself if it is not needed to designate a result register.

Directions: The FK module decodes the f, m, and i portions of the instruction for the CPU. Study the logic on the module and then answer the following questions.

1. When will output pin 5 of the module be active? F=7

2. For each of the following pin numbers, write the CPU instruction that causes it to be active.
   a. B3-2 = 36-37
   b. B5-7 = 010
   c. B6-2 = 00
   d. B6-7 = 031
   e. A4-7 = 014-015-016-017
   f. A2-7 = 42 43
   g. B5-2 = 46

3. When is the output of A3-15 active? I=6 07

This concludes the lesson on decoder logic diagrams. During the activity you have seen how logic can be used to decode the contents of a register and generate control signals based on those contents.

You may go on to Learning Activity 2-K.

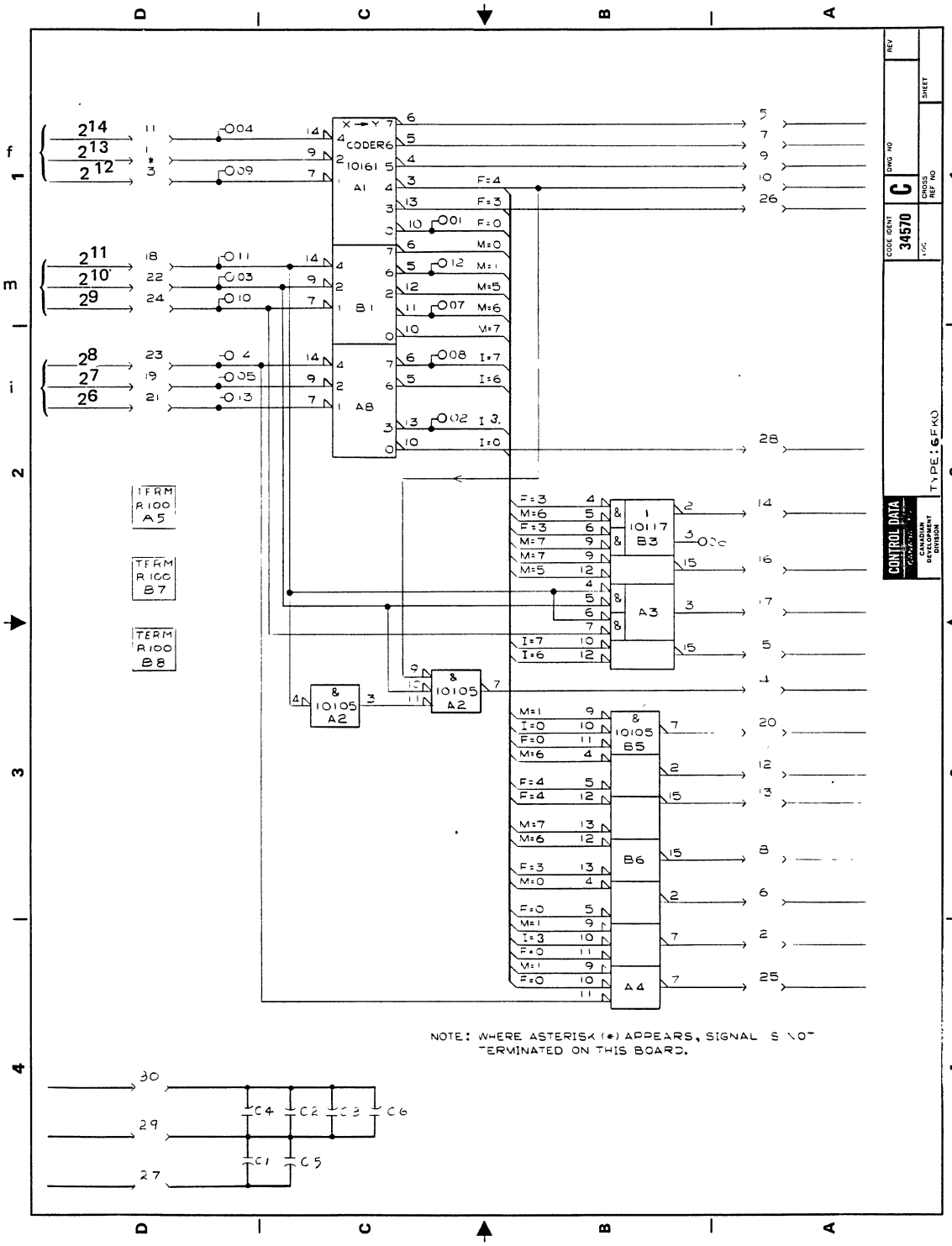


Figure 2-21. CPU Instruction Decoder

ANSWERS FOR LEARNING ACTIVITY 2-J

EXERCISE 2J-1

1. A3-9 = X3X

   Originating pin = A2-13

2. Any 2XX instruction (20 through 27)

3. 624 (6XX·XX4·X2X)

   637 (6XX·X3X ·XX7)

4. 612·FLAG OR 711

   (612 = (6XX·XX2)·X1X) (711 = 7XX·XX1·X1X)

5. 03X and 04X through 07X. This one is tricky. A3-pin 13 is bit 2^5 of K, and it is the only bit of the 2^3, 2^4, and 2^5 group that is checked by A3. So, if that portion of the instruction is X4X, X5X, X6X, or X7X the condition is satisfied, because bit 2^5 will be a "one" in all four cases.

6. $(2XX)+(3XX\cdot\overline{36+37})$. If the 3XX instruction is a 36 or 37, B4-3 will be HI and the wired AND will be broken.

7. "D to B" is generated any time "F to B" occurs, but also if a "1XX" (10-17) is in the K register.

EXERCISE 2J-2

1. If the "f" portion of the instruction is equal to 7_8.

2. a. B3-2 - fm = 36+37

   b. B5-7 - fmi = 010

   c. B6-2 - fm = 00

   d. B6-7 - fmi = 013

   e. A4-7 - fmi = 014, 015, 016, or 017

   f. A2-7 - fm = 42+43 (A2-3 is inverting the upper bit of "m".)

   g. B5-2 - fm = 46

3. Whenever "i" is equal to a 6_8 or 7_8. (It is used for the increment write instructions.)

LEARNING ACTIVITY 2-K. EXERCISE: SHIFT REGISTERS AND COUNTERS DIAGRAMS

During this activity you see some applications of shift register circuits and counter circuits.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

The format of this activity is the same as in previous activities. Study the logic diagram from the CYBER 170 prints, then answer the questions about its operation. Check your answers with the answers at the end of this activity before going on to the next diagram.

Exercise 2K-1: Shift Register Diagram

Figure 2-22 is a diagram of the 4AJ0 module from the CYBER 170 PPS chassis. This module is used in the PPU barrel registers.

As you recall, the PPU "slot" is where all arithmetic operations occur. While a PPU is making its next memory reference, the contents of the operating registers are shifted through the barrel. Each output of the barrel is synchronized with the output of a PPU memory so that both enter the "slot" at the same time.

The AJ module handles 2 bits of a barrel register. In order to make up the full barrel of the 18-bit "A" register, the PPS chassis has 9-AJ modules. If the register contains 12 bits, then its barrel has 6-AJ modules.

Directions: Study the logic for the AJ module, and then answer the following questions.

1. What are the logic states of pins 7 and 10 of chips A2, B1, A6, and B5?

   Pin 7 = H/1

   Pin 10 = LO

2. With the logic states that you used in question 1, what function are the 10141 circuits performing? Right shift

3. What determines when the shifting in the 10141 chips takes place?
Clock

4. If the clock occurs every 50 nanoseconds, how long after a data bit enters A2-5 will it be output from A6-14? ____
400 N.S.

5. What is the relationship of the output of B5-15 to B5-14?
One Clock Time Period

6. What is the output equation for B3-6? ____
A · B

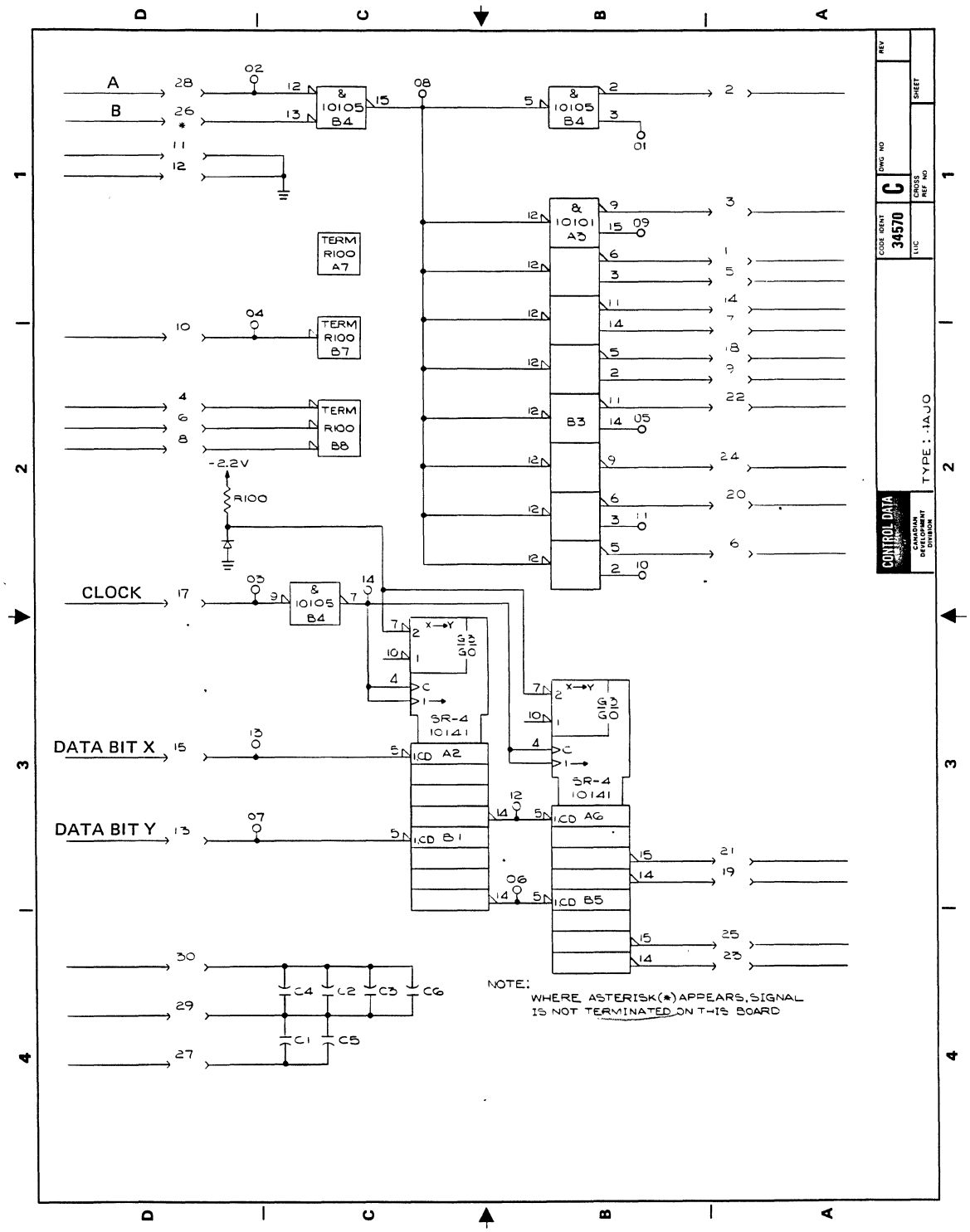


Figure 2-22. PPS Barrel Register

Exercise 2K-2: Counter Logic

Figure 2-23 is a diagram of the 4CL0-type module. It contains two counter circuits.

Directions: Study the logic on the diagram, and then answer the following questions.

NOTE

There are two counter circuits on the ~~A1~~ module. Each counter consists of 5 bits (modules = 32_{10}). The 10131 flip-flop fed by the carry-out signal from each 10136 counter is the 2^4 bit of the respective counters.

1. What is the logic level at pins 5, 6, 11, and 12 of the counter chips? Hi

2. What function will the counters perform for the following conditions?

   a. Count enable (pin 23) = LO - count at clock rate

   b. Count enable = HI - Reset to all zeros parallel inputs Hi

3. What happens to the flip-flop at A2(TP-13) every time it is clocked (pin 6)? toggles Q

4. When is pin A6-4 active? when Count goes from 1111 to zero

5. If the clock signal (TP14) occurs at a 1 microsecond rate, how often will A4-15 go LO? 32 μsec rate

6. What conditions will cause the counter circuit at B6 to be advanced? / count enable & clock every 32 microsec. when A4-14 goes hi

7. The outputs at module pins 25, 6, 4, 2, and 8 will be all zeros (HIs) every _____ microseconds.
32 X 32 = 1024 usec

This concludes the lesson on shift register and counter diagrams.

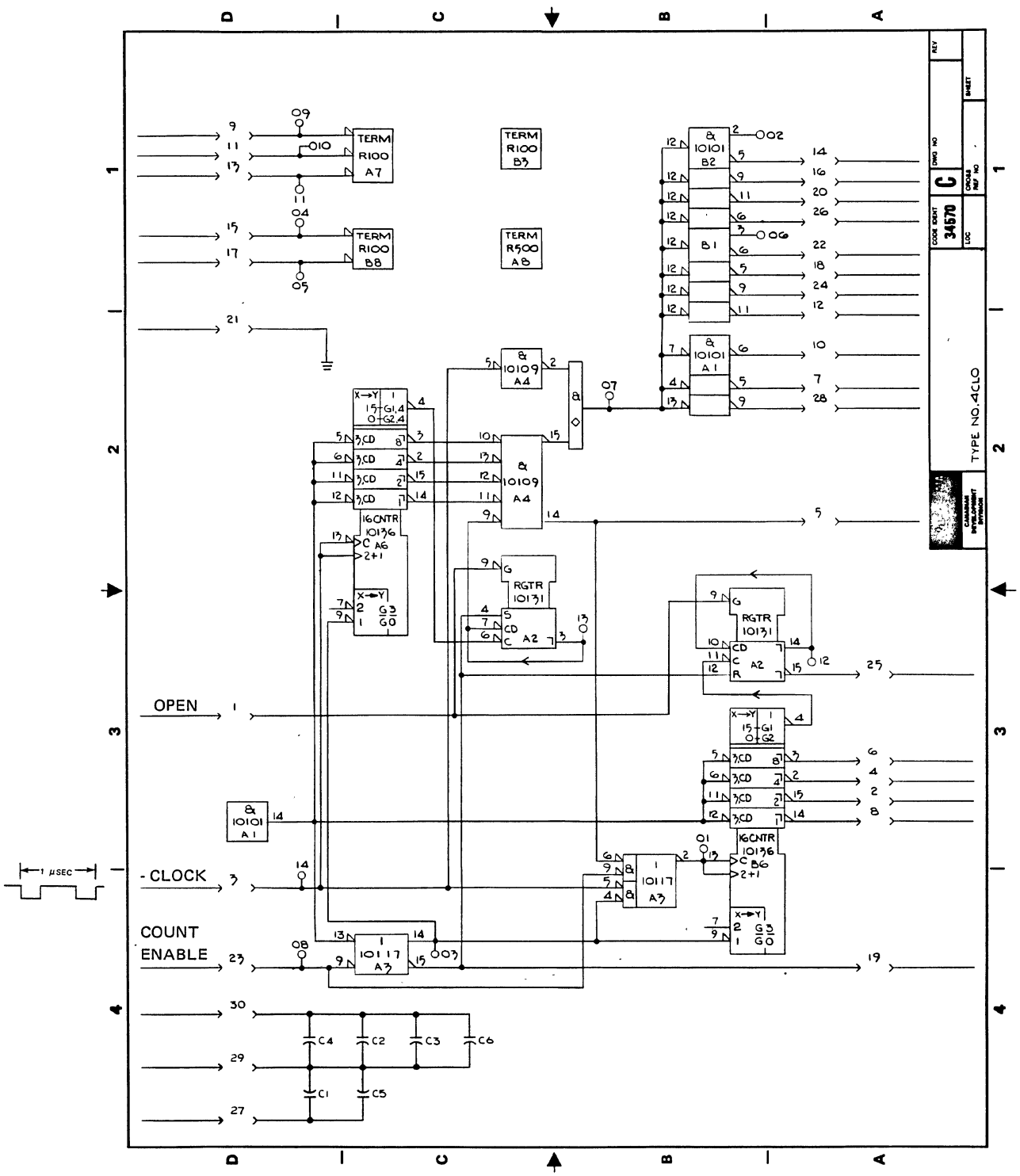


Figure 2-23. Counter Logic Diagram

ANSWERS FOR LEARNING ACTIVITY 2-K

EXERCISE 2K-1

1. Pin 7 = HI; it is connected to ground.

   Pin 10 = LO; it is open.

2. A right shift or shift down; reference the 10141 circuit in the ECL manual.

3. Whenever the clock signal at pin 4 goes HI.

4. 400 nanoseconds - there are a total of 8 stages in the two chips (8 x 50 nsecs = 400 nsecs).

5. B5-15 outputs one clock time earlier than B5-14.

6. A·B - The top part of the AJ diagram is fanout logic. It has no direct relationship to the shifters.

EXERCISE 2K-2

1. All HIs - A1-14 is always HI because its inputs are open (LOs).

2. a. Count enable = LO - Counter increments at clock rate. (See ECL manual.) Pin 7 = OPEN = LO; pin 9 = HI from A3-14.

   b. Count enable = HI - Counter is preset (cleared) to all zeros (pin 7 and 9 both = LO). It is cleared because the parallel inputs are always HI.

3. It changes to the state opposite of the one it was. The reset output (pin 3) is the D input (pin 7). If it is reset and clock occurs, it will be set. Conversely, if it gets clocked when set, it will go the reset state.

4. Whenever the counter reaches all ones (1111_2) and then rolls over to all zeros.

5. Every 32 microseconds; the counter at A6 must be all ones and A2-3 must be LO (reset). Because the A2 flip-flop toggles whenever the counter carry-out (A6-4) occurs, the A4 AND gate is made on every other count of 16 in the counter circuit.

6. 1) Clock·$\overline{\text{Count Enable}}$; this will clear the counter.

   2) Every 32 microseconds, because that is when A4-14 goes HI and breaks the AND gate into A3 and causes the clock to B6(TP-01) to go HI.

7. 1024 microseconds; the modules of the B6 counter is 32, and it is advanced by one every 32 microseconds (answer to question 6). Therefore, 32 microseconds x 32 = 1024 microseconds.

LEARNING ACTIVITY 2-L. EXERCISE: ARITHMETIC LOGIC UNIT DIAGRAM

In this activity you study the application of an ALU chip in a logic diagram.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

Figure 2-24 is the logic diagram of a 3AH0 module. It is the standard adder module is the CYBER 170 PPS. All the arithmetic sections in the PPS slot use this module. This includes the A, Q, K, and P registers.

Directions: Study the logic on the AH module, then answer the following questions. Check your answers with the answers on the last page of this activity.

1. What is the purpose of the signals M, S3, S2, S1, and S0 that are inputs to the module? function inputs

2. When are input signals B0, B1, B2, and B3 available at the B input of the ALU chip? [illegible]

3. If the adder function code (S0-S3 and M) is 04_8, what operation will the ALU perform? (Hint: refer to figure 2-13 for codes.) [illegible]

4. If the BYPASS signal is HI, what is output of the module at pins 24, 22, 26, and 28? [illegible]

5. Given: ALU function code = 31_8

ALU function code = 31_8

A0-A3 input = 1010

B0-B3 input = 0101

Carry input = HI

What are the states of the following ALU pins?

a. A4-2 = LO

b. A4-3 = LO

c. A4-7 = LO

d. A4-6 = LO

e. A4-4 = HI

f. A4-8 = LO

g. A4-5 = HI

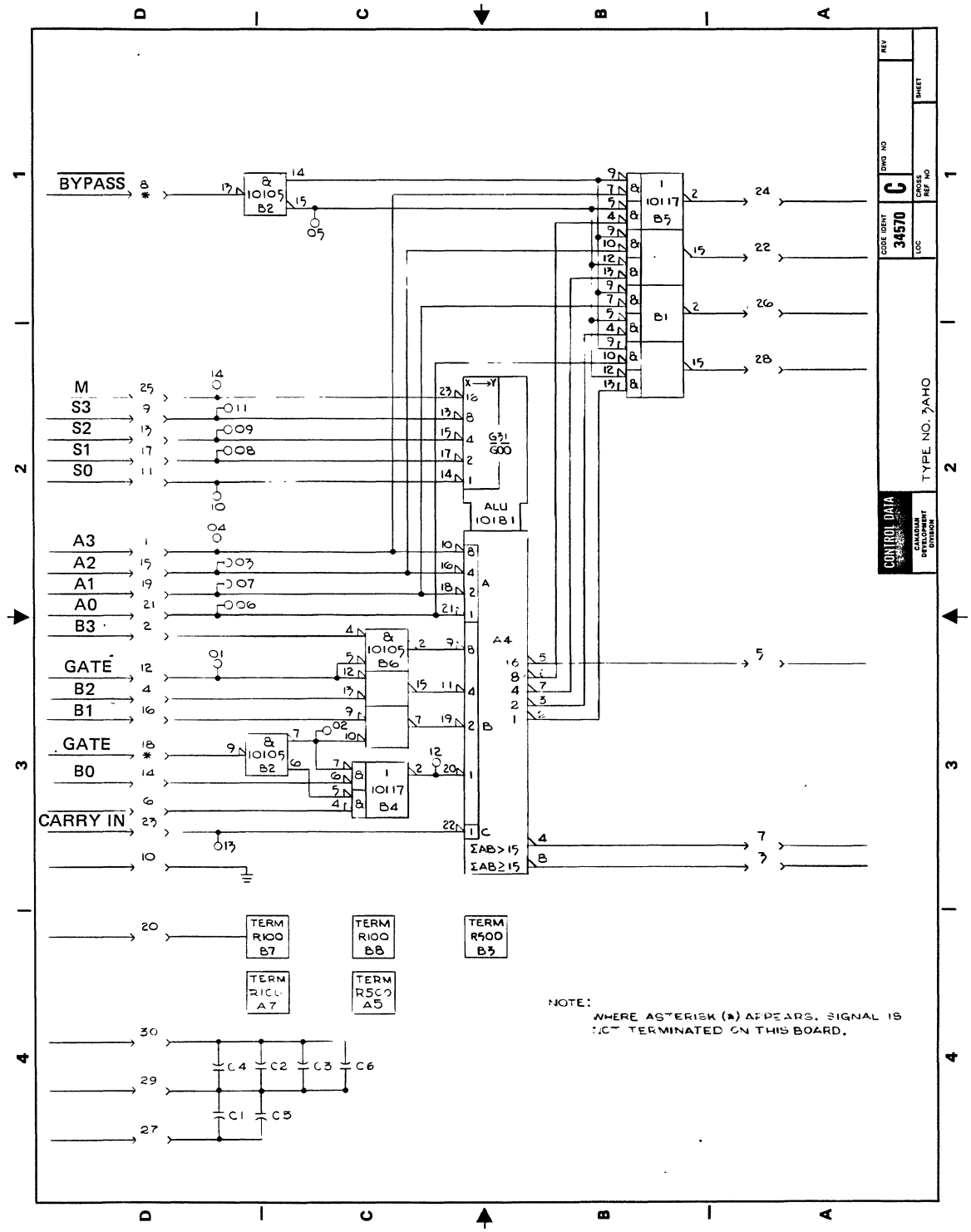


Figure 2-24. ALU Logic Diagram

6. If the GATE signals (pins 12 and 18) are HI, what is the value of the B inputs to the ALU? (Module pin 6 is open.)

   a. A4-9 = HI

   b. A4-11 = HI

   c. A4-19 = HI

   d. A4-20 = LO

This concludes the lesson on ALU applications. At this time you may proceed to the optional activity in Learning Activity 2-M or sign on the terminal and take the Module 2 test.

NOTE

You will need your student manual to take the Module 2 test.

ANSWERS FOR LEARNING ACTIVITY 2-L

1. They are the ALU function codes that determine which operation the circuit is to perform.

2. When the GATE signals at pins 12 and 18 are LO.

3. A logical AND of the A and B inputs (Logical Product).

4. What is input to the module at A0-A3. There are situations in the PPS when the output of an adder cannot be used, so the ALU is bypassed at those times. The PPS control logic determines when to bypass and when not to bypass.

5. a. A4-2 = LO
   b. A4-3 = LO
   c. A4-7 = LO
   d. A4-6 = LO

   } The sum is 1111_2.

   e. A4-4 = HI; no carry is generated.

   f. A4-8 = LO; all stages are enables (passes).

   g. A4-5 = HI; no carry-in or carry generates.

6. a. A4-9 = HI

   b. A4-11 = HI

   c. A4-19 = HI

   d. A4-20 = LO

   The default input (no gate signal) to the ALU is 0001_2 if module pin 6 is open. If pin 6 is grounded, then the input is 0000_2. The PPS control logic will sometimes need a code of 0001_8 at the input to an adder. By using the GATE and module pin 6 the code can be formed.

LEARNING ACTIVITY 2-M. EXERCISE (OPTIONAL): LOGIC DIAGRAM ANALYSIS

This optional activity includes two logic diagrams from the CYBER 170 manuals. If you need practice in analyzing logic diagrams, or if you want to learn more about logic, do the exercises. If you prefer, you may now take the Module 2 test.

OBJECTIVE

- You will be able to analyze and trace logic symbols on an annotated logic diagram (level 4).

The format of this exercise is the same as in the previous activities in the module. Study the logic diagram, then answer the questions about its operation. Check your answers with those at the end of the activity before going to the next exercise.

Exercise 2M-1: Parity Generator/Checker Diagram

Figure 2-25 is the logic diagram of the 3BF0 module. The main function of the circuit is to generate or check PPU memory parity. It is used both on PPU memory input data as a generator and on the PPU memory output as a parity checker.

Directions: Study the logic of the BF module. Then answer the following questions.

1. What is the logic level at TP-12 if the data word is 6300_8? LO

6 2. If the data word is 0000_8 and the parity bit = LO (one), what is the level of A2-12? HI

3. If module output pin 2 is HI, does a parity error exist? (Odd Parity.) NO

4. What is the equation for A1-15? Clock • X

5. What is the equation for A1-2? Clock • ABCD

6. How long will A1-2 be LO? 12.5 NS

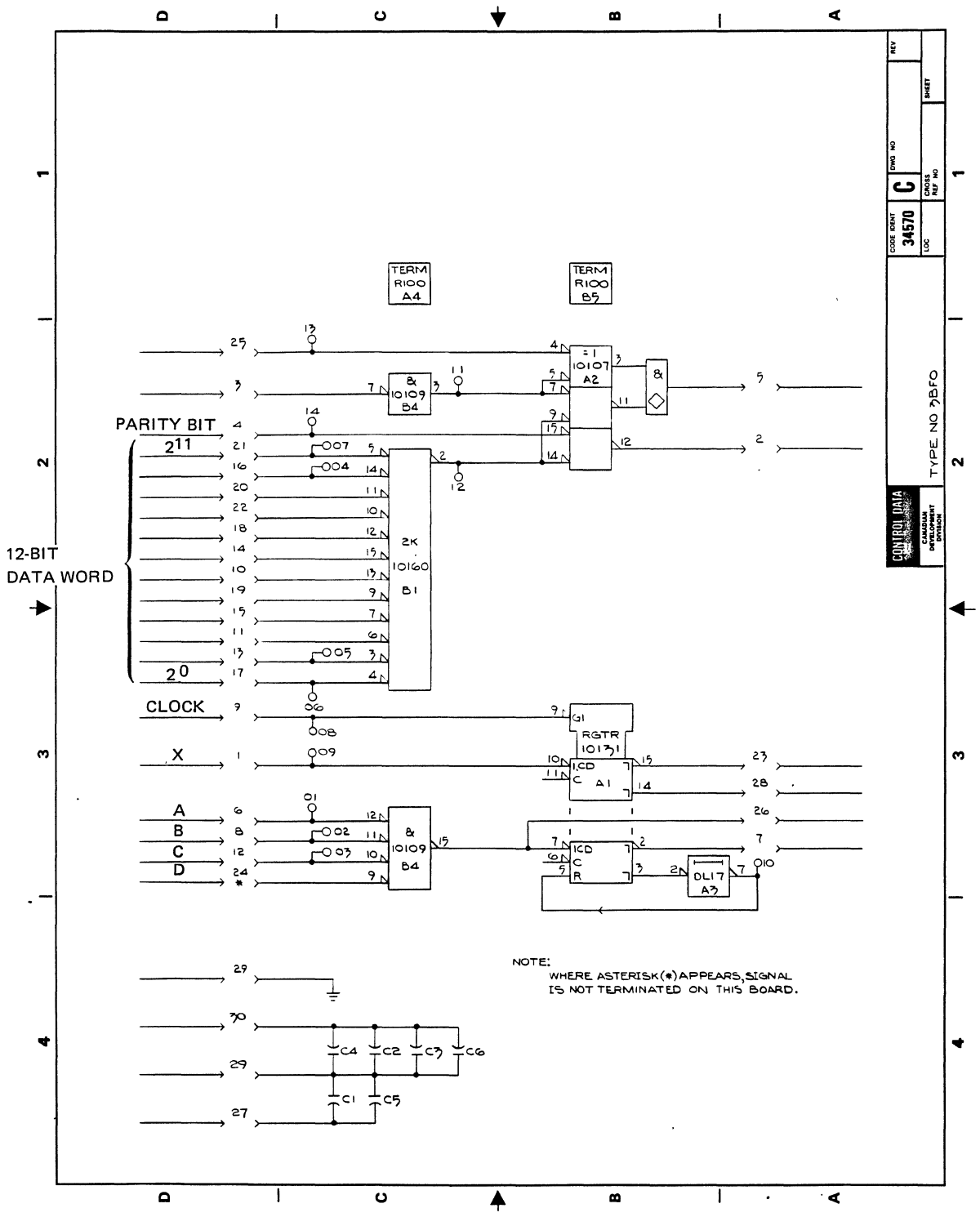


Figure 2-25. Parity Check Logic

Exercise 2M-2: Timing Chain Logic

Figure 2-26 is the logic diagram of a 4GD0 module. It contains a timing chain made up of 10130 and 10131 flip-flop circuits. It also has some control logic to determine if certain conditions exist during the running of the timing chain.

Figure 2-27 is a timing diagram for the flip-flops in the timing chain.

Directions: Study the timing diagram to make sure you understand how the timing chain works. Then come back to this page for the remainder of the exercise.

The note on the timing diagram about pin B8-15 states that it will be LO at T214 if B1-3 is LO. B1-3 is LO if the wired AND gate output is HI. If the output of A6, B5, or A7 is HI, then the wired AND gate is broken and its output goes HI.

Note that there are many conditions that may cause the output of the wired AND gate to go HI. Which condition is used is determined by the code of the ABC input and the KLM input. If the condition is met, then the flip-flop at B8-15 is set. If not, then the flip-flop is reset.

Directions: Answer the questions about the logic on the GD module. As you check your answers, you should get a good idea of how the circuit works.

1. Module output pin 18 is HI at T214 if the condition met flip is set. (True/false) FALSE

2. Output pin 17 is active at T 114 and T 214.

3. What is the equation for B5-6? $\overline{T114} \cdot \overline{T214} \cdot$ Conditions met

4. Given: ABC code = 2_8.

   What condition is necessary to set the "condition met" flip-flop? _____

5. For each of the following ABC codes, write the equation for the condition that will allow the "condition met" flip-flop to be set.

   a. ABC code = 4. Condition = $ABC=4 \cdot J$

   b. ABC code = 5. Condition = $ABC=5 \cdot \overline{J}$

   c. ABC code = 6. Condition = $ABC=6 \cdot E \cdot F=G+\overline{F} \cdot E \neq G$

   d. ABC code = 7. Condition = $ABC=7 \cdot G \cdot E=G+F \cdot E \neq G$

6. Given: ABC code = 3

   KLM code = 6

   What condition is necessary to set the "condition met" flip-flop? _____

7. Given: ABC code = 3

   KLM code = 1

   What condition is necessary? $\overline{V} \cdot \overline{W}$

This concludes the optional exercise. If you understand the logic on the GD module, you should have few problems reading most CYBER 170 logic diagrams. If you had trouble with it, realize you are not alone. As you get more practice in future courses, you will be able to read the diagrams more easily.

NOTE

You will need your student manual while taking the Module 2 test.

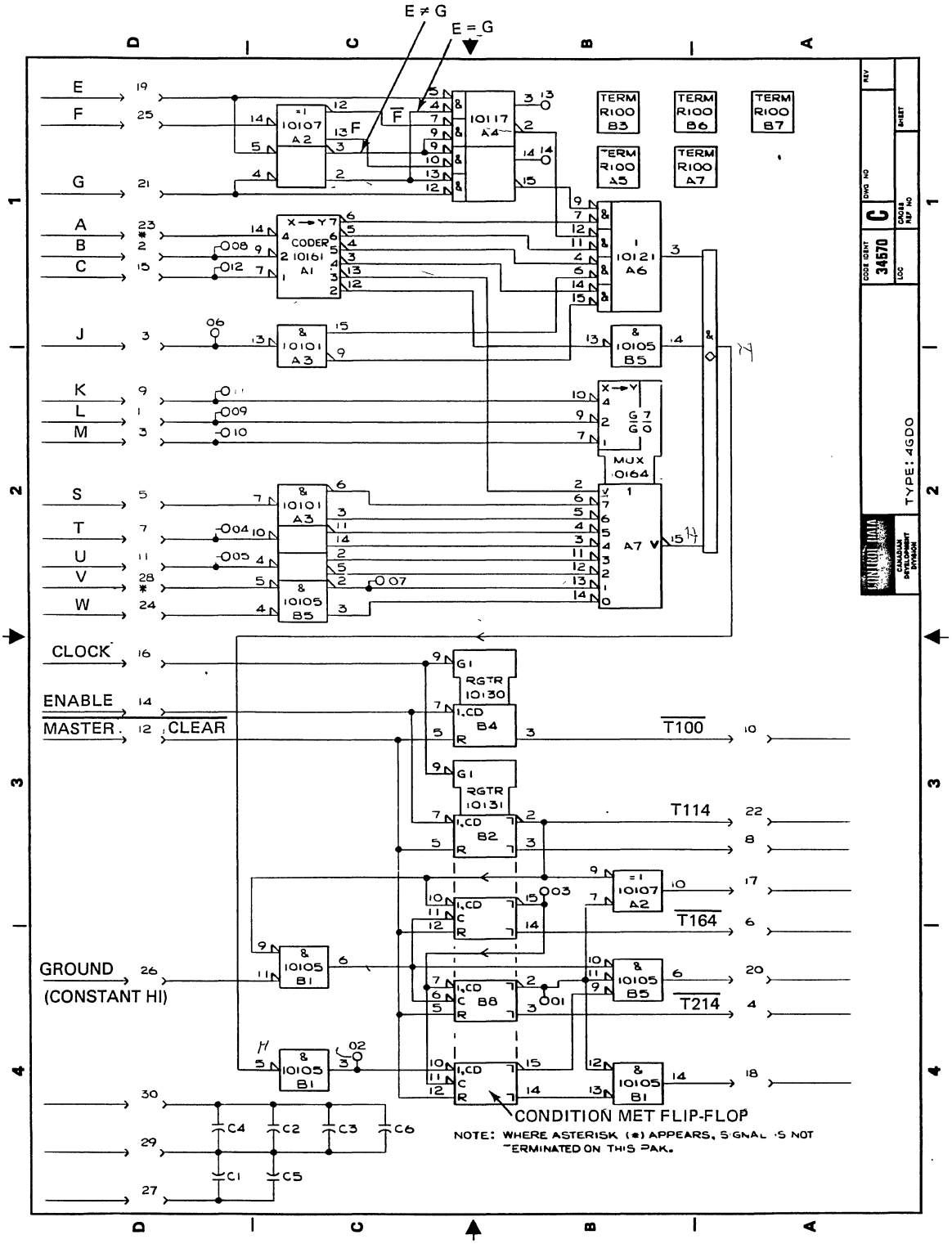


Figure 2-26. Timing Chain Logic Diagram

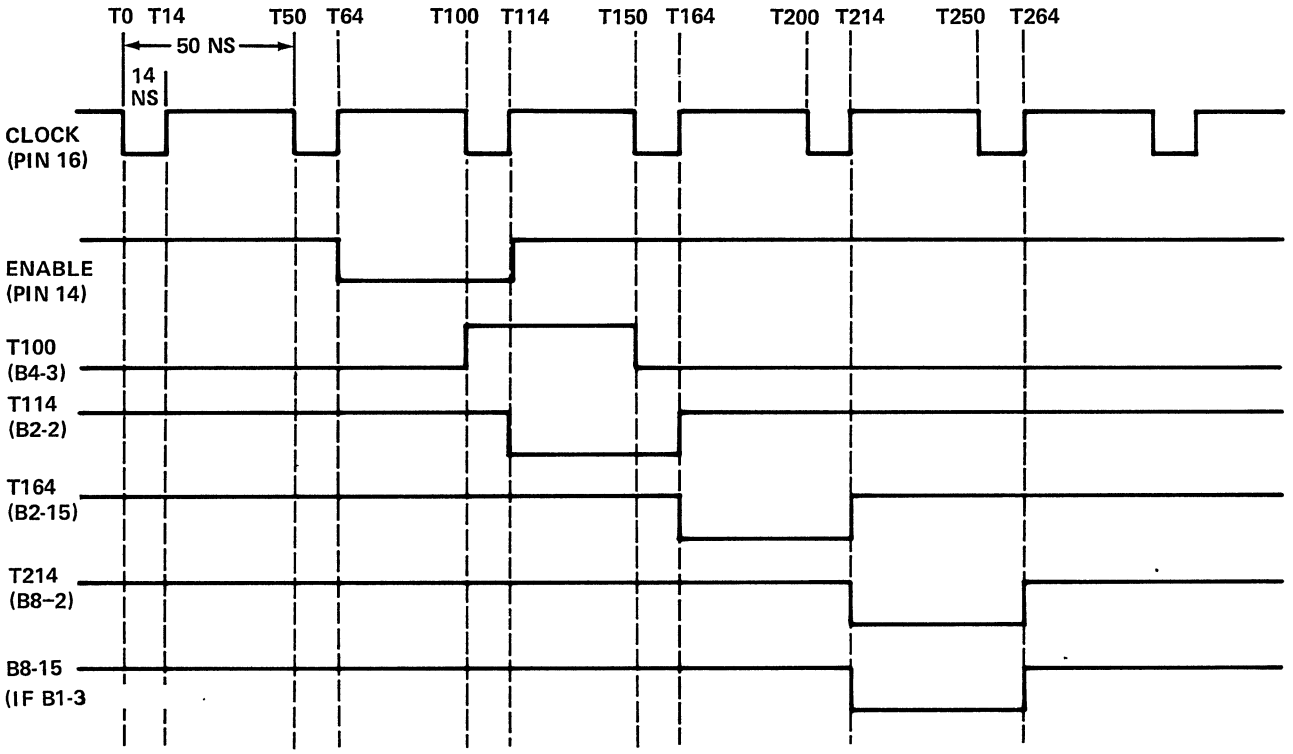


Figure 2-27. GD Module Timing Diagram

ANSWERS FOR LEARNING ACTIVITY 2-M

EXERCISE 2M-1

1. TP-12 = LO - 6300_8 = 110 011 000 000_2 = even number of bits.

2. A2-12 = HI; all zero input is an even number of bits. Therefore, B1-2 (TP-12) is LO. Two LOs into a 10107 cause pin 12 to go HI.

3. No; a LO indicates a parity error. (Refer to question 2 in which no parity error existed and A2-12 = HI.)

4. CLOCK·X

5. CLOCK (A·B·C·D)

6. 17.5 nsecs. When A1-2 goes LO, A1-3 goes HI. After the delay in A3, the HI from A1-3 will be at A1-5, and it force resets the flip-flop. It is a one-shot type of circuit.

EXERCISE 2M-2

1. False; condition met FF must be reset (B8-14 = LO).

2. T114 and T214

3. $\overline{(T114 \cdot T214 \cdot \text{CONDITION MET})}$

4. Only the ABC code = 2 is needed to satisfy the condition. (A1-2 goes LO, B5-14 goes HI, B1-3 goes LO, and the B8-FF sets at T214.)

5. ABC = 4. Condition = J

   ABC = 5. Condition = $\overline{J}$

   ABC = 6. Condition = $(E \cdot E = G) + (\overline{F} \cdot E \neq G)$

   ABC = 7. Condition = $(F \cdot E \neq G) + (G \cdot E = G)$

6. S - 1) ABC = 3 enables the MUX chip

   2) KLM = 6 enables A7-5 to A7-15

   3) S = LO makes A3-3 HI which passed through A7 breaking the wired AND gate.

7. $\overline{V \cdot W}$ $(\overline{V}+\overline{W})$ satisfies the condition. It causes B5-2 to go HI.

POST TEST

When you have completed the learning activities assigned for Module 2, sign on the PLATO terminal and take the Module 2 test.

Depending on the results of the test you will be told either to review some of the previous activities, or to go on to the Module 3 Pretest.

NOTE

You will need the diagrams included in the Appendix D for the Module 2 test.

MODULE 3
MEMORIES

During this module you learn the concepts of MOS memory circuits as they are used in the CYBER 170 PPS and CSU chassis.

There are several types of MOS memory circuits in the CYBER 170 mainframes. The type of circuit in a mainframe is dependent on the model of the machine. The circuits you will see in this module are:

- 6002 circuit - used in CYBER 170, models A and B
- 2102 circuit - used in CYBER 170, model C
- 4044 circuit - used in CYBER 170, model D

The types of circuits have many similarities in their operations. At the completion of this module you will be able to analyze a logic diagram of MOS memory chips, have an understanding of the internal operations of a memory circuit, and know the differences between 6002, 2102, and 4044 circuits.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column below, put a check mark by each activity assigned to you by PLATO Learning Management (PLM). Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	3-A	Audio/Microfiche: 6002 Memory Theory. During this activity you learn the basic concepts of the 6002 MOS memory circuit.	3-3

Assigned	Completed	Activity	Description	Page
_____	_____	3-B	Text Reading: 6002 Memory Circuits. During this activity you learn the symbol for a 6002 memory chip. You also learn how to read a memory module logic diagram.	3-4
_____	_____	3-C	Text Reading: 2102 Memory Theory. During this activity you learn the basic concepts of the 2102 MOS memory circuit.	3-9
_____	_____	3-D	Text Reading: 2102 Memory Circuits. During this activity you learn the logic symbol of a 2102 memory circuit and the basic paths used to access a 2102-type memory. You also see the logic diagram of a 2102-type memory module.	3-11
_____	_____	3-E	Audio/Microfiche: 4044 Memory Theory. During this activity you learn the basic concepts of the 4044 MOS memory circuit.	3-17
_____	_____	3-F	Text Reading: 4044 Memory Circuits. During this activity you also learn how to read a memory module logic diagram.	3-18
_____	_____	3-G	Text Reading: RAM Memories. During this activity you learn the symbol for the 10145 RAM memory chip. You also learn how to read a logic diagram containing a RAM memory.	3-22

LEARNING ACTIVITY 3-A. AUDIO/MICROFICHE: 6002 MEMORY THEORY

During this activity you learn the basic concepts of the 6002 MOS memory circuit.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 6002 MOS memory chip.

When maintaining a CYBER 170 memory circuit the greatest depth of maintenance you preform is to swap modules until you find the failure. The concepts you learn in this module are probably not necessary to be able to perform maintenance to that level. However, they help you understand the purpose of some of the memory dirvertype circuits that you will see during the maintenance courses.

At this time load the microfiche labeled "6002 Memory Theory," P/N 75444758, into your projector and the corresponding audiotape, P/N 75444758 into your cassette player and proceed with the activity.

STUDENT NOTES

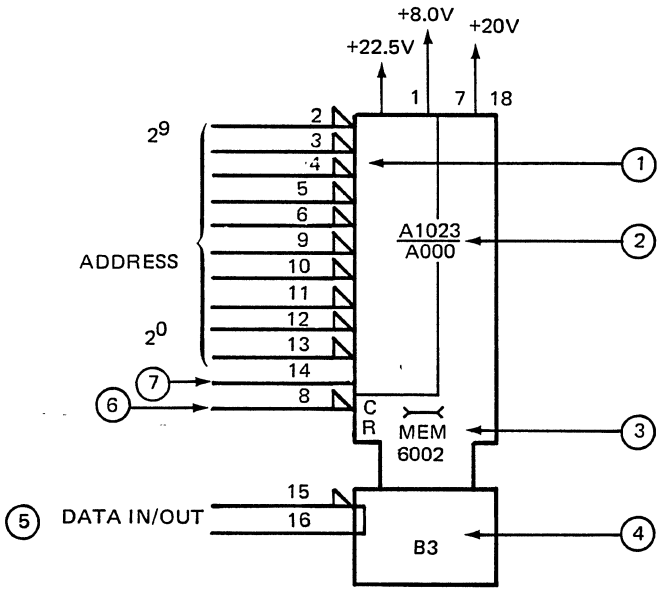
LEARNING ACTIVITY 3-B. TEXT READING: 6002 MEMORY CIRCUITS

During this activity you learn the symbol for a 6002 memory chip. You also learn how to read a memory module logic diagram.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 6002 MOS memory chip.

Figure 3-1 is the symbol for the 6002 memory circuit. Study it and read the notes.

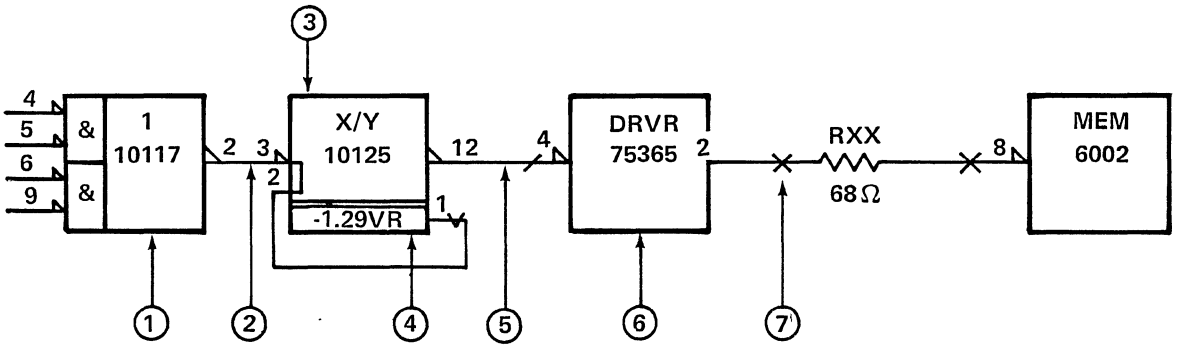


Notes:

① This X/Y section is the address decoder portion.
② Symbolizes the range of the addresses (000 to 1023_{10}).
③ Qualifying symbol for memory circuit. The ⋊ means that it's a read/write memory.
④ This portion of the symbol is the actual memory array itself.
⑤ Data path for both read and write data.
⑥ Reset input - a timing pulse that precharges the chip at the beginning of the memory cycle.
⑦ Clock input - occurs after the address has been decoded. It is during "clock" that data is stored or read.

Figure 3-1. 6002 Memory Logic Symbol

The signal levels used to drive the 6002 memory chip are non-standard MOS levels. ECL logic is not capable of directly driving an MOS circuit. In order to drive the memory, TTL logic is used. This means we must convert ECL logic levels to TTL levels and then use the TTL levels to run the memory drivers. Figure 3-2 is a drawing of a typical memory driver circuit from an ECL input to the memory chip itself. Note that the type of circuits shown in figure 3-2 are used for the address, clock, and reset lines to the MOS chip. The circuits for data are slightly different, as you will see later in this activity.



Notes:

① ECL circuit
② ECL Logic Levels
③ ECL to TTL converter
④ This -1.29V voltage regulator is internal to 10125 chip. It provides a reference bias voltage for the input. (See description in ECL manual.)
⑤ TTL logic levels. The ⟋ symbol indicates this.
⑥ TTL driver of MOS circuits
⑦ MOS levels - the ✕ indicates this.

Figure 3-2. Typical Memory Driver Circuit

The driver circuits are found in the blue faceplate modules in a CYBER 170 chassis. Sometimes they will be all one module, and sometimes they will be on two modules.

Remember, the circuit in figure 3-2 is a typical circuit. The actual circuits may vary slightly. You will learn more about them in the PPS and CSU maintenance courses.

Now let us see how to get data to and from a 6002 memory chip. Figure 3-3 shows a typical data path circuit. It shows the path for write data and read data.

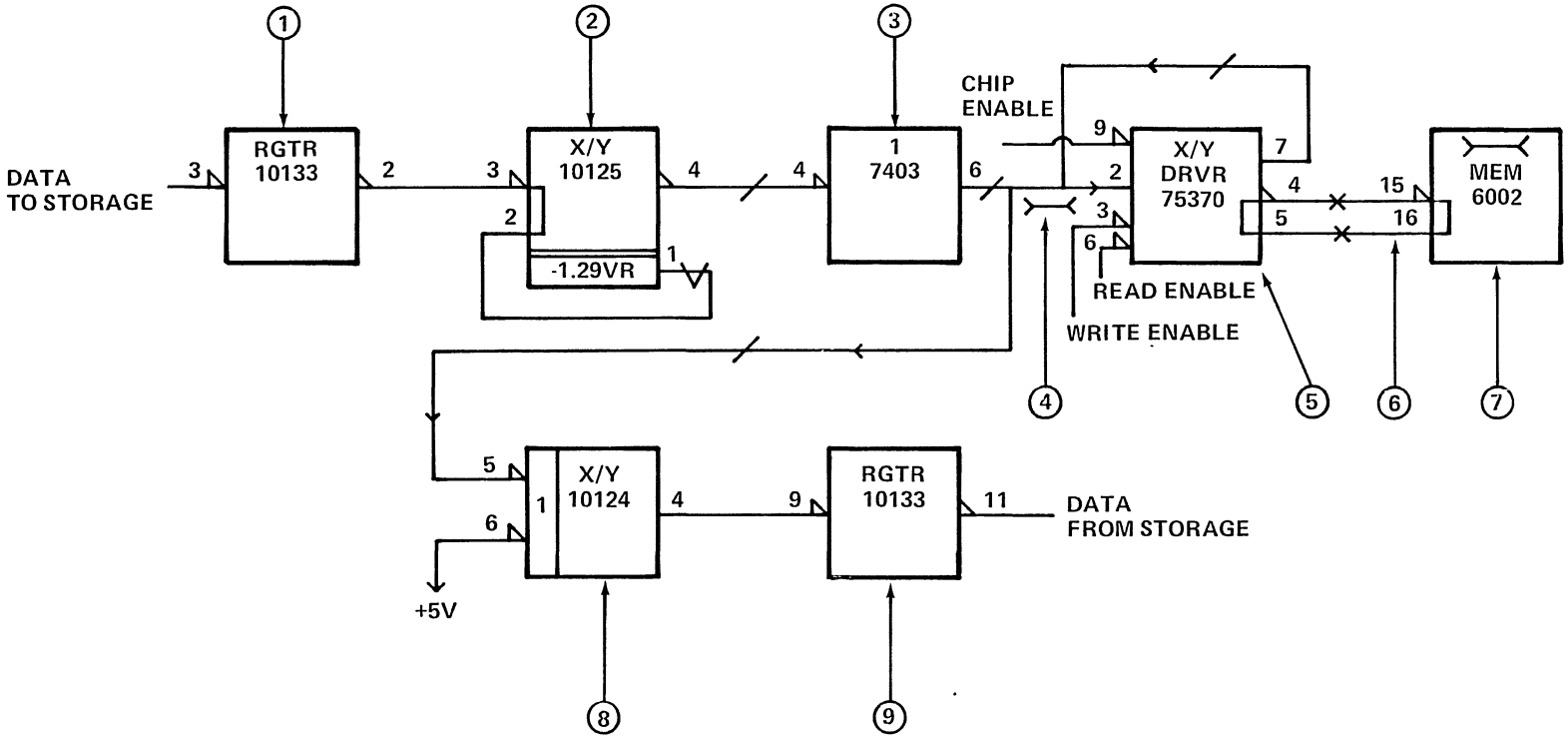
Note the bidirectional lines used in this circuit. They are possible because in the MOS memory only a read or a write can be performed during any given memory cycle. Consequently, there should be no conflicts on these lines.

The logic for the circuits shown in figure 3-3 is located on two modules. The memory circuit and the 75370 TTL driver are on a red faceplate module. The remaining circuits are on a blue faceplate module.

The final item of study in this activity is the logic diagram of a CU-type module. It is on figure 3-4. This shows you how the memory chips are laid out to form a 4K by 4-bit circuit on one module. Study the diagram and its notes; then return to this page.

This concludes your activity on MOS memory circuits. During this lesson you have learned the symbol for an MOS memory chip and the circuits required to drive an MOS memory. Finally, you have studied the logic diagram of a CYBER 170 memory module.

At this time you may review the material in this activity if you wish. Then go on to the next assigned activity.



① ECL Logic - Memory Data In Holding Register
② ECL to TTL Converter
③ TTL Driver Circuit
④ Bidirectional line
⑤ Memory data path driver (Read and Write)
⑥ MOS levels on memory input/output data
⑦ MOS Memory circuit
⑧ TTL to ECL converter
⑨ ECL Logic - Memory Data Out holding register

Figure 3-3. 6002 MOS Memory Data In/Out Paths

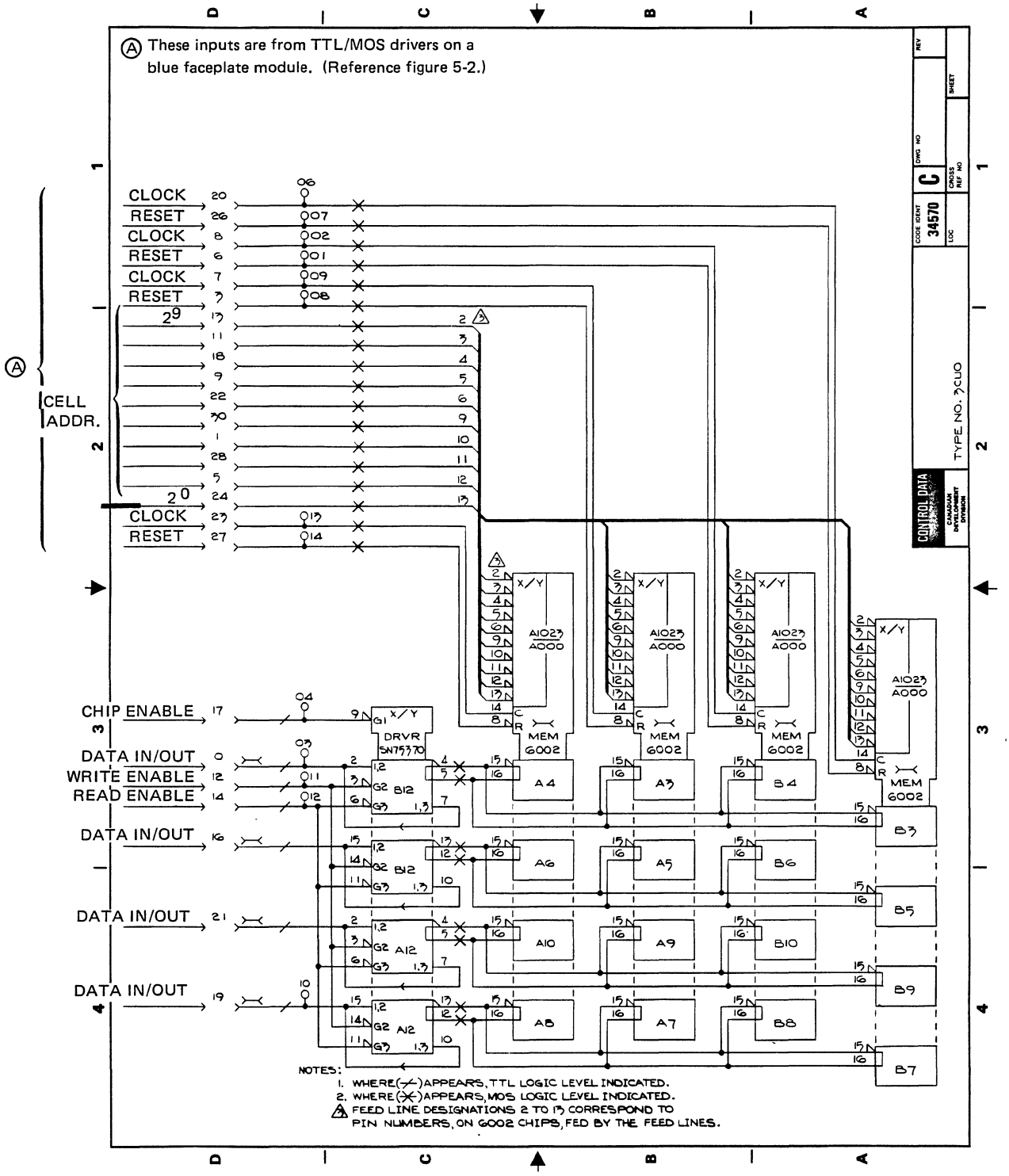


Figure 3-4. CU Module Logic Diagram

LEARNING ACTIVITY 3-C. TEXT READING: 2102 MEMORY THEORY

During this activity you learn the basic concepts of a 2102 MOS memory circuit.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 2102 MOS memory chip.

In Learning Activity 3-A you learned the concepts of the 6002 memory circuit. The 2102 chip has many similarities to the 6002 chip. It is an MOS type of memory. Each chip has a storage capacity of 1024_{10} locations, which means it requires 10 address bits to access a cell in the 32 by 32 array of the chip.

There are some differences in a 2102 chip, however. First of all, each cell is a true bistable multivibrator or flip-flop. Once the cell is set to a state, it holds that state as long as the chip has power applied to it. It does not depend on the inherent capacitance of the MOS transistors to hold a state. This means that the 2102 chip does not require refreshing.

Another difference in the 2102 circuit is that it requires only a +5 volt power source. You recall that the 6002 chip requires +8, +20, and +22.5 volts for its operation. the system power scheme with a 2102 type memory is thus significantly simpler than in the model A and B systems which have the 6002 type memory.

Because the 2102 uses the same +5 volts that is used for the TTL logic, there is less TTL driver logic required to run the memory itself. You will see this in the next learning activity.

Figure 3-5 is a block diagram of the internal functions of a 2102 circuit. Note that there is only one gating signal (chip select) and a write enable signal feeding the circuit. If the chip select signal is present but no write enable, then the operation is a read from memory. You should also note that there is an input data line and a separate output data line. This differs from the 6002 circuit.

The address decode works in a similar way to the 6002 chip. It decodes five of the address bits to select one of 32 row (word) drivers; the other five address bits are decoded to select one of the 32 sense (read) lines or write lines.

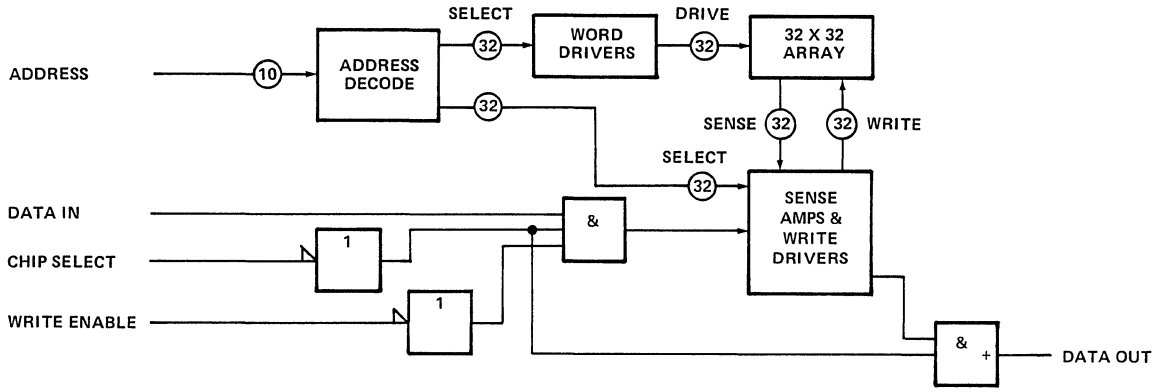


Figure 3-5. 2102 Memory Circuit Block Diagram

The physical layout of 2102 memory circuits in a module is the same as the 6002-type circuit; the memory modules have red faceplates, and each module has either 4K of 4 bits or 4K of 5 bits. To distinguish a module with 2102 circuits on it, the first letter of the module type is a Q rather than the C used for 6002-type modules. Therefore, a QU-type module contains 4K of 4 bits, and a QS module contains 4K of 5 bits. A PPU memory, then, is made up of two QU modules and one QS module for a total size of 4K of 13 bits.

As in models A and B, the CYBER 170 model C (2102 memories) has blue faceplate modules that contain the TTL driver logic for the memory circuits.

This concludes the activity on 2102 memory theory. If you wish, you may review this material.

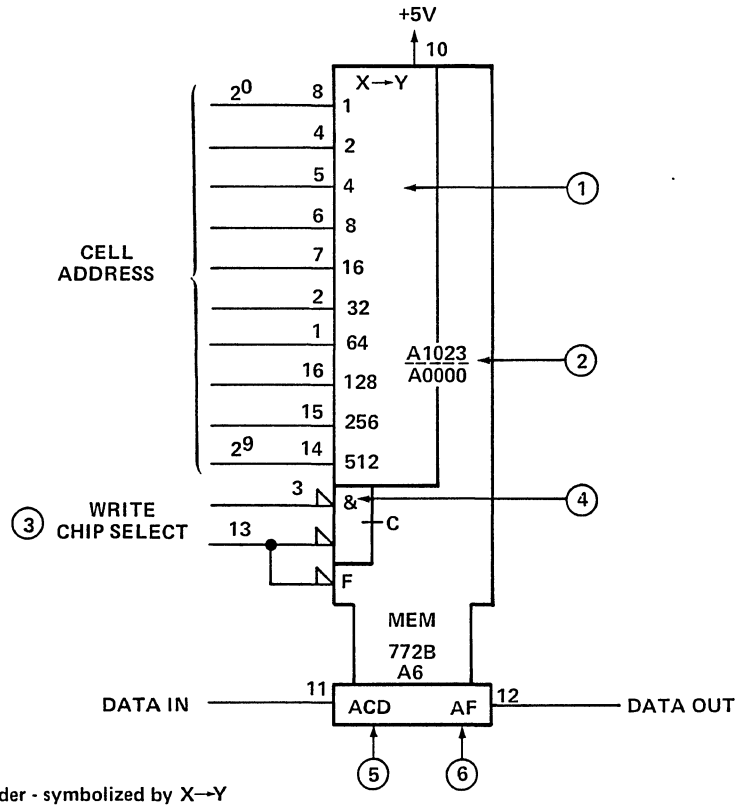
LEARNING ACTIVITY 3-D. TEXT READING: 2102 MEMORY CIRCUITS

During this activity you learn the logic symbol of a 2102 memory circuit and the basic paths used to access a 2102 type memory. You also see the logic diagram of a 2102-type memory module.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 2102 MOS memory chip.

Figure 3-6 is the symbol for a 2102-type memory circuit. Study it, and be sure to read the notes.

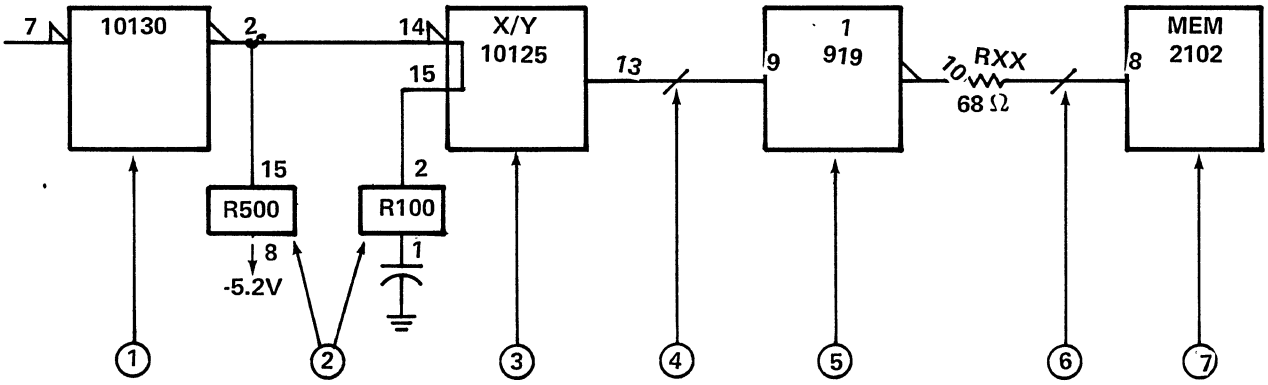


Notes:

1. Address decoder - symbolized by X→Y
2. Range of addresses - 0000 to 1023_{10}
3. Chip Select is the gating signal that gates data in or out of the cell after the address has been decoded.
4. C = Chip Select · Write
5. Write data in - Requires Address (A), Clock (C) and Data (D)
6. Read data out - Requires only Address (A) and Chip Select (F)

Figure 3-6. Memory Circuit Symbol

All input and output signals of the 2102 memory circuit are TTL levels. In order to be compatible with the ECL logic they must go through some conversion circuits. Figure 3-7 is a typical circuit used to get the address and control signals to a 2102 memory circuit.

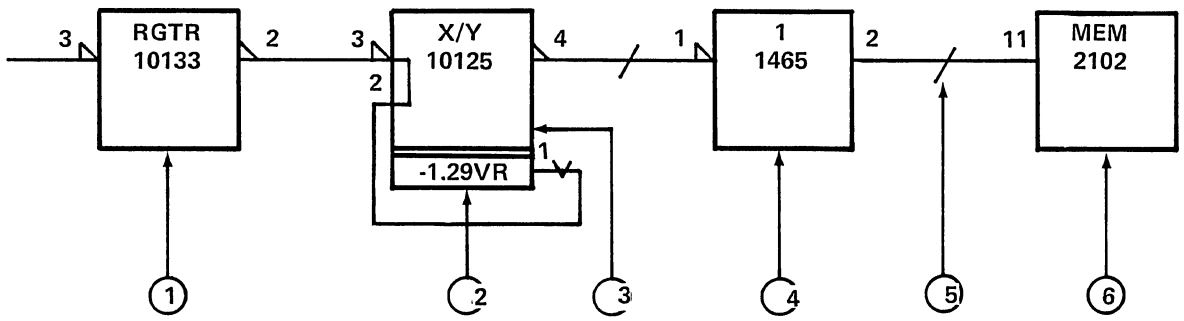


Notes:

① ECL Holding Register Flip-Flop
② Provide reference bias voltage for 10125 circuit
③ ECL to TTL converter
④ TTL level as symbolized by ⫽
⑤ TTL memory driver circuit
⑥ TTL level
⑦ MOS memory driver by TTL levels

Figure 3-7. Typical TTL Driver Circuit

The input data path to a 2102 memory circuit is very straightforward. Figure 3-8 shows a typical path.

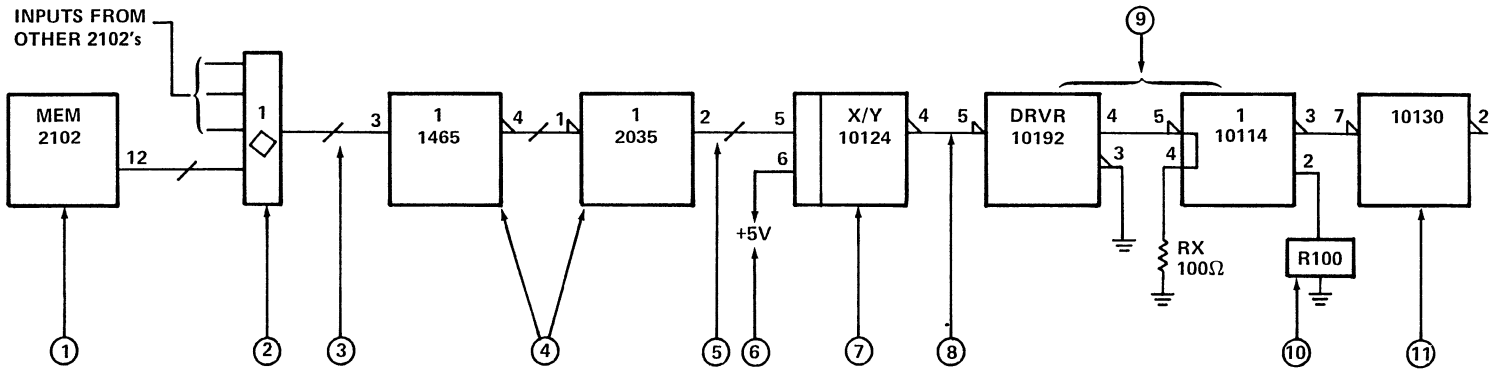


Notes:

① ECL Logic - Data In Holding Register
② Provides Reference Bias Voltage for 10125 chip
③ ECL to TTL converter
④ TTL fan-out circuit
⑤ TTL logic level
⑥ MOS Memory using TTL input levels

Figure 3-8. Typical Data-In Path

The data-out path used when reading from the memory is a more complex circuit because it is also used to reduce noise interference on the data lines. Figure 3-9 is a diagram of a typical data-out path for 1 bit of a memory word. Study it, and read the notes explaining the purpose of each circuit.



Notes:

(1) MOS Memory with TTL output levels
(2) Wired OR gate - Fan-in from other 2102 chips
(3) TTL level as symbolized by +
(4) TTL inverters - provide isolation between memory and ECL circuits
(5) Still TTL levels
(6) Unused input must be tied to +5V
(7) TTL to ECL converter
(8) ECL logic levels
(9) A twisted pair differential transmission driver and receiver using only one line. The other line is terminated at both ends. This scheme provides current transmission rather than voltage and it is much more immune to noise interference.
(10) Unused output is terminated to eliminate noise.
(11) ECL data out holding register

Figure 3-9. Typical 2102 Data Out Path

The last item in this activity is the logic diagram of a 2102-type memory module. It is shown in figure 3-10. The diagram is the logic for a QU module. It contains 4K of 4 bits of storage. A QS module is identical in operation to a QU, except that it has 4K of 5 bits on it. Both the QU and QS modules have red faceplates.

Study the diagram in the figure. You may wish to refer to figures 3-6 through 3-9 to relate where the inputs and outputs of the module are connected. When you are finished studying the diagram, return to this text.

This concludes the activity on 2102 memory circuits. If you wish, you may review the material in this lesson and the previous lessons in this module.

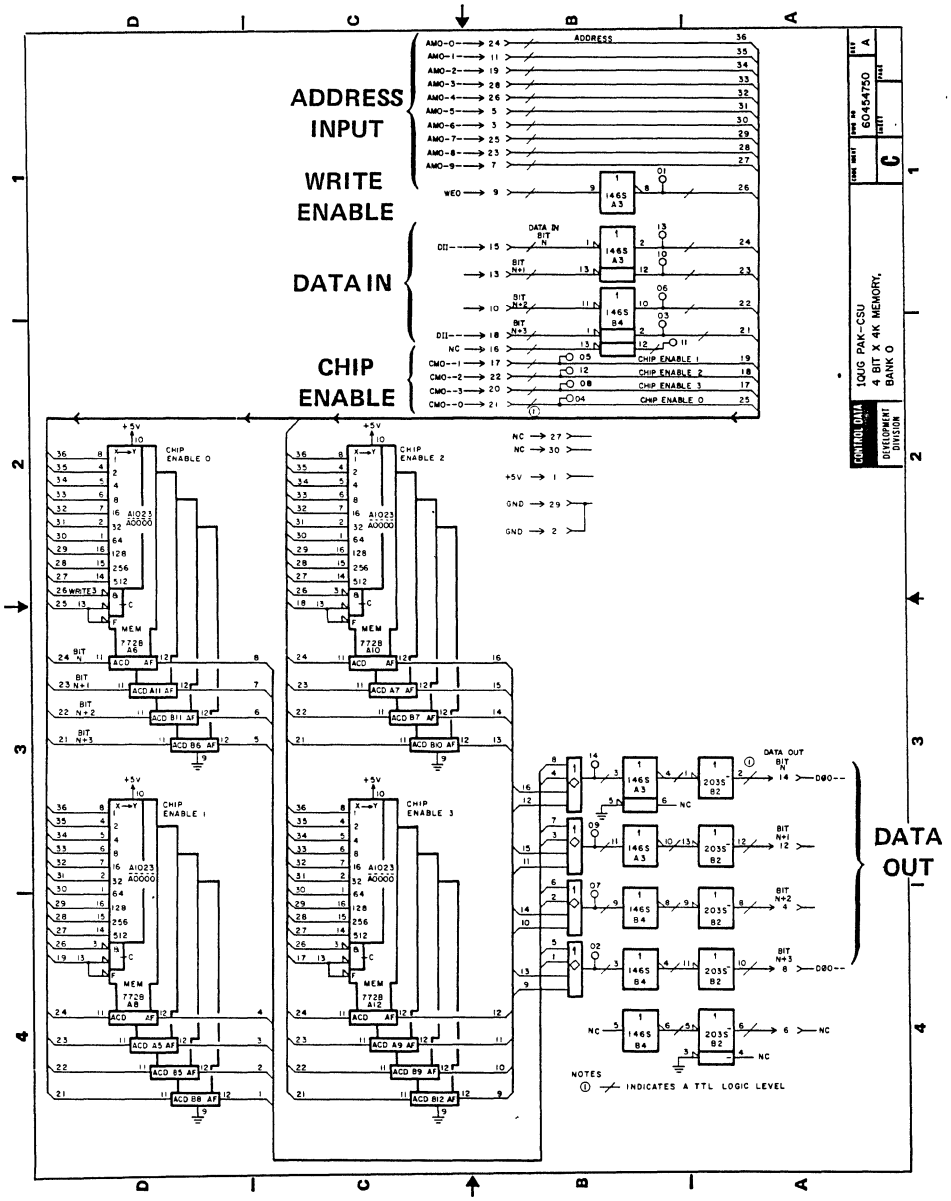


Figure 3-10. QU Module Logic Diagram

LEARNING ACTIVITY 3-E. AUDIO/MICROFICHE: 4044 MEMORY THEORY

During this activity you learn the basic concepts of the 4044 MOS memory circuit.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 4044 MOS memory chip.

When maintaining a CYBER 170 memory circuit the greatest depth of maintenance you perform is to swap modules until you find the failure. The concepts you learn in this module are probably not necessary to be able to perform maintenance to that level. However, they help you understand the purpose of some of the memory drivertype circuits that you still see during the maintenance courses.

At this time load the microfiche labeled "4044 Memory Theory," P/N 75445247, into your projector and the corresponding audiotape, P/N 75445247, into your cassette player and proceed with the activity.

STUDENT NOTES

LEARNING ACTIVITY 3-F. TEXT READING: 4404 MEMORY CIRCUITS

During this activity you learn the logic symbol of a 4044 memory circuit and the basic paths used to access a 4044-type memory. You also see the logic diagram of a 4044-type memory module.

OBJECTIVE

- You will be able to identify the characteristics and functions of the 4044 MOS memory chip.

Figure 3-11 is the symbol for a 4044-type memory circuit. Study it, and read the notes.

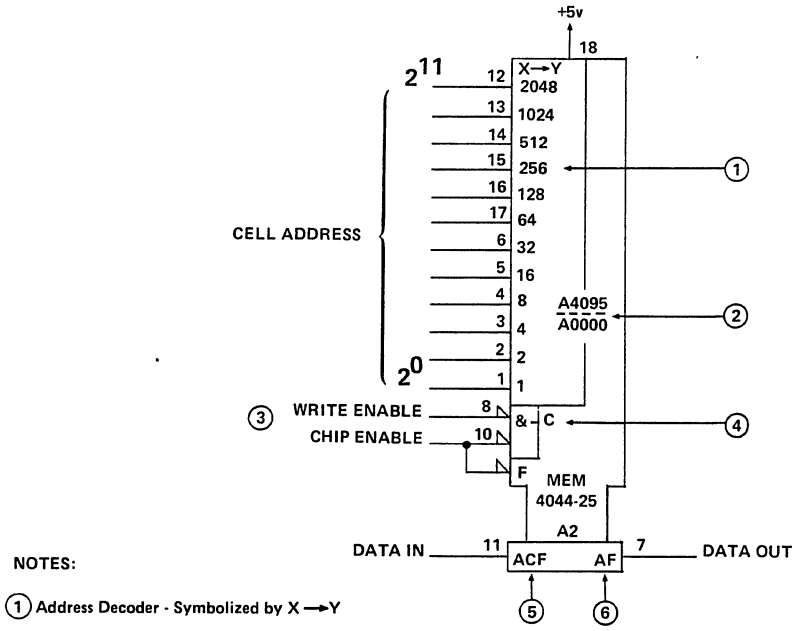


Figure 3-11. 4044 Memory Logic Symbol

All input and output signals of the 4044 memory circuit are TTL levels as on the 2102 memory. Consequently, the circuits used are the same. If you want to review them, you can turn back to Learning Activity 3-D, and where the 2102 memory chip is shown, change it to a 4044 or 2147 memory chip.

The last item in this activity is the logic diagrams for the 4044 and 2147-type memory modules. Figure 3-12 is the diagram of a WC type module. It is used for the PP memories and contains 4K of 13 bits of storage or one complete PP memory. The WC module uses the 2147 memory chip, which is the faster of the 2 chips used in the D model machines. Figure 3-13 is the diagram of the RJ type module. It is used in the CSU and contains 8K of 4 bits of storage. This module uses the 4044 memory chip and is used in conjunction with the QK module (8K of 5 bits of storage) to form the CSU in the CYBER 720, 730 and 750 machines. There are also RS (8K by 5 bits) and RU (8K by 4 bits) modules, which contain the faster 2147 chip and are used in the CYBER 760 machine. These modules all operate like the RJ module shown.

This concludes the activity on the 4044/2147 memory circuits. If you wish you may review the material in this lesson.

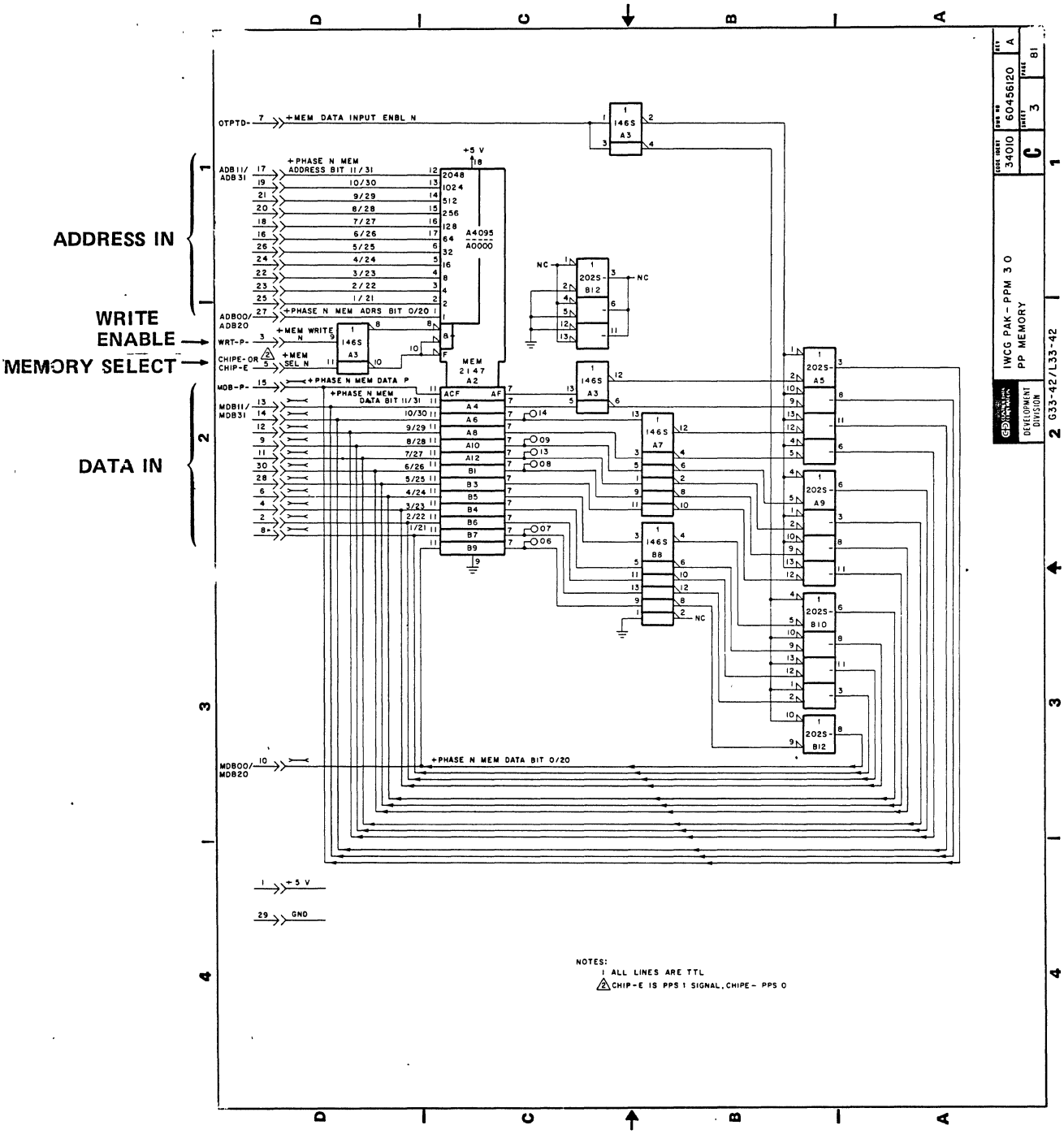


Figure 3-12. WC Module Logic Diagram

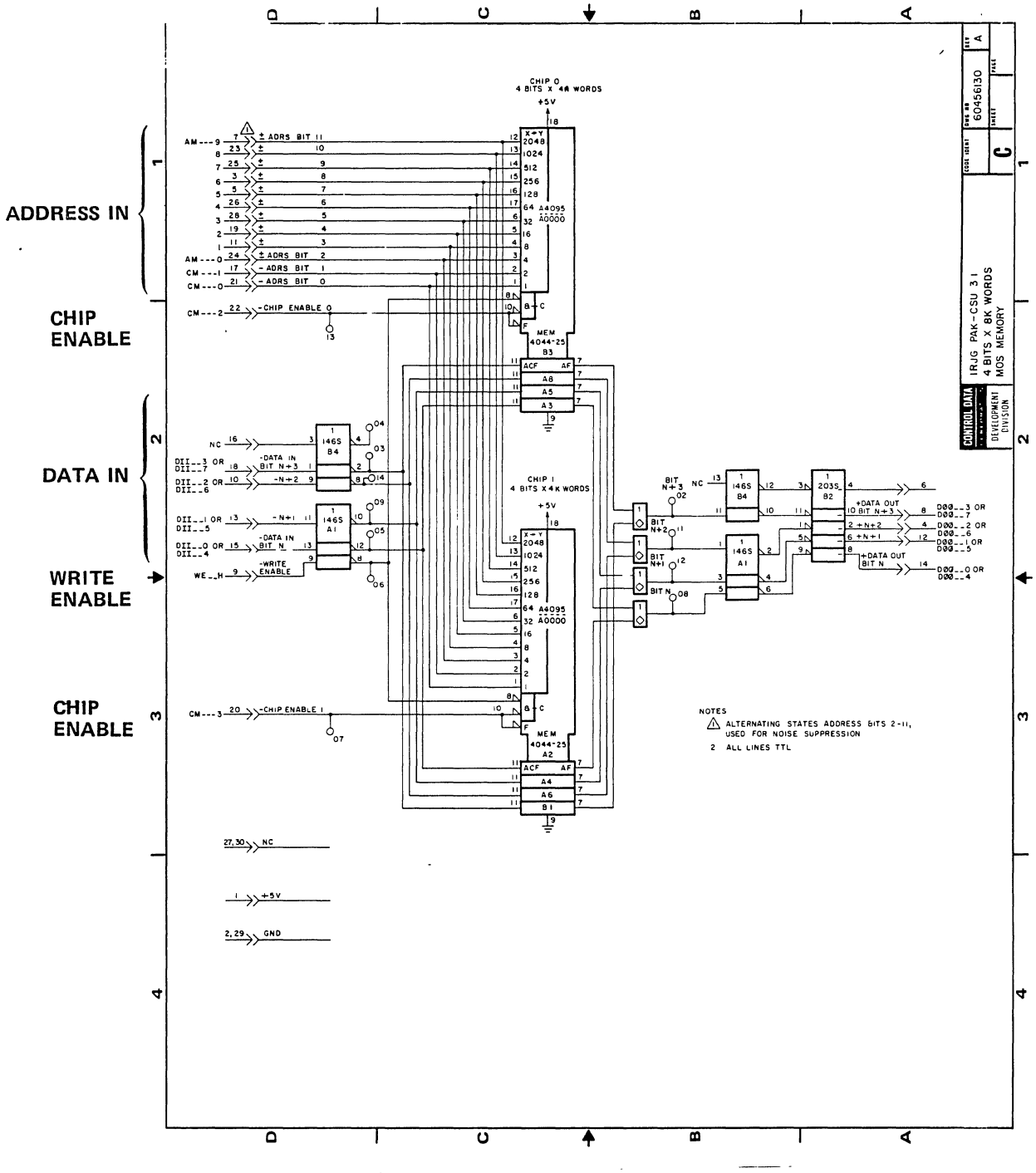


Figure 3-13. RJ Module Logic Diagram

LEARNING ACTIVITY 3-G. TEXT READING: RAM MEMORIES

During this activity you learn the basic concepts of a RAM memory.

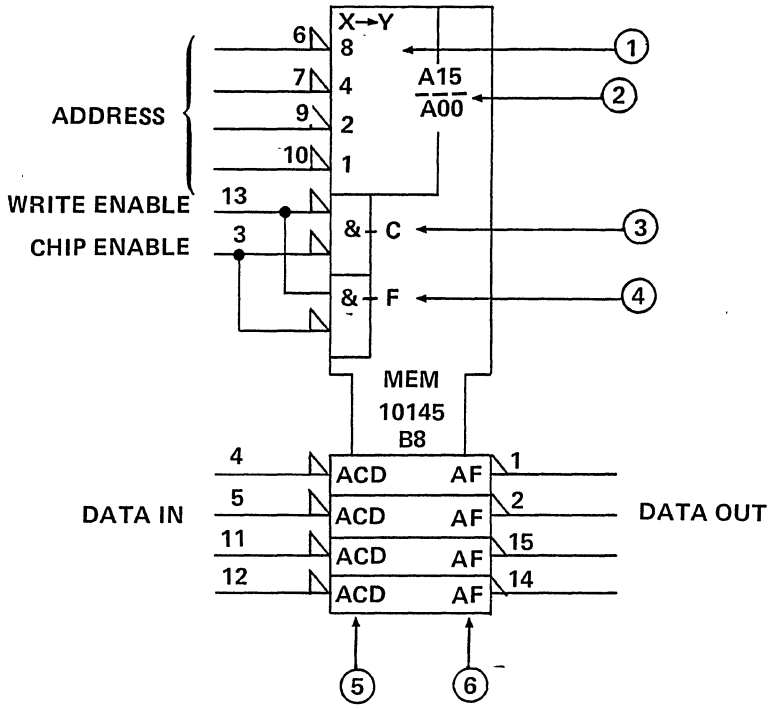
OBJECTIVE

- You will be able to identify the characteristics and functions of the RAM memory chips used in the CYBER 170.

The RAM or Random Access Memory is a small memory chip that is used in the CYBER 170 D model machines PPUs. It is used in the central memory interface or read/write pyramids as they were referred to in earlier machines. In this area they are used to speed up and simplify the assembly and disassembly of data going to or coming from central memory. The RAM chips are also used to form the barrel in the D model PPUs.

The RAM chip used in these areas is the 10145 chip. It is a standard ECL chip so it does not need any special chips or drivers to interface with the other logic in the PP chassis. The 10145 chip holds 16 locations of 4 bits of data. It has write enable and chip enable signals similar to those used in the 2102, 4044 and 2147 MOS type memory chips. The 10145 chip functions very similarly to these MOS chips, in that once a location is addressed, it is necessary to have both the write enable and chip enable signals present to store data. Similarly, to read data from the RAM after it has been addressed, the chip enable signal and absence of the write enable signal are required.

The logic symbol for the 10145 RAM is shown in figure 3-14. Study it and read the notes.



NOTES:

(1) Address Decoder - Symbolized by X Y

(2) Range of Addresses - $0\text{-}15_{10}$

(3) C = Chip Enable Write Enable

(4) F = Chip Enable Write Enable

(5) Write data in - Requires Address (A), Clock (C) and Data (D)

(6) Read data out - Requires Address (A) and (Chip Enable • $\overline{\text{Write Enable}}$) (F)

Figure 3-14. 10145 RAM Logic Symbol

Figure 3-15 is a logic diagram of an ST module which contains the 10145 RAM memory. This module contains RAM chips to hold 16 locations of 8 bits; however, it only uses 8 locations of 8 bits. This module is used in the Barrel/Slot area of the PPS chassis, the 10145 RAM memory chip is also used on many other board types in different areas of the machine.

This concludes the activity on the RAM memories.

If you wish you may review the material in this lesson or any of the previous lessons in this module.

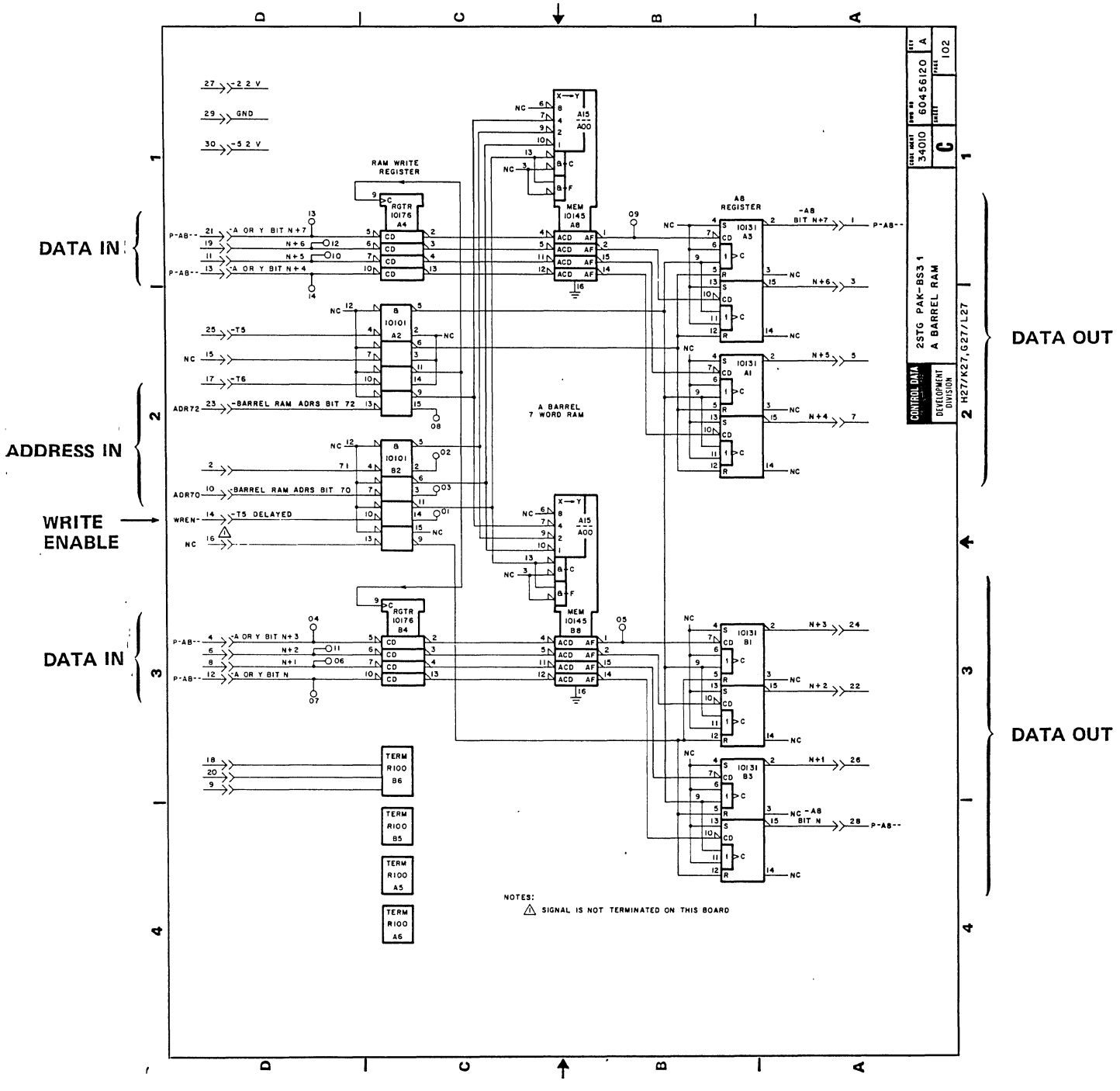


Figure 3-15. ST Module Logic Diagram

POST TEST

When you have completed the learning activities assigned for Module 3, sign on to the PLATO terminal and take the Module 3 test.

Depending on the results of the test you will be told either to review some of the previous activities, or to go on to the Module 4 Pretest.

MODULE 4
DATA TRANSMISSION AND WIRE LISTS

In Module 4 you learn how data moves from one location to another in the CYBER 170 system. Topics covered include:

- Inter-Module Transmission
- Inter-Chassis Transmission
- Data Channel Transmission

You will also learn how to trace these signals, using the wire lists. Topics covered include:

- Multi-Level Diagram Usage
- Chassis Wire Lists
- Cable Wire Lists

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column below, put a check mark by each activity assigned to you by PLATO Learning Management (PLM). Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	4-A	Text Reading: Inter-Module Transmission. During this activity you learn how data is transmitted between modules within a CYBER 170 logic chassis.	4-3

LEARNING ACTIVITY 4-A. TEXT READING: INTER-MODULE TRANSMISSION

During this activity you learn how data is transmitted between modules within a CYBER 170 logic chassis.

OBJECTIVE

- You will be able to state the types of data transmission used and identify the types of logic circuits used in the CYBER 170.

When transmitting a signal between one ECL 10,000 series circuit and another, there must be some type of termination of the signal line. As a minimum, each circuit uses a 500-ohm emitter pull-down resistor (Rp) or a 100-ohm line terminator (Rt).

The required 500-ohm and 100-ohm resistors are found in the R500 and R100 chips that you learned about in Module 2 of this course.

Rp is usually connected to ECL 10K circuits, as shown in figure 4-1.

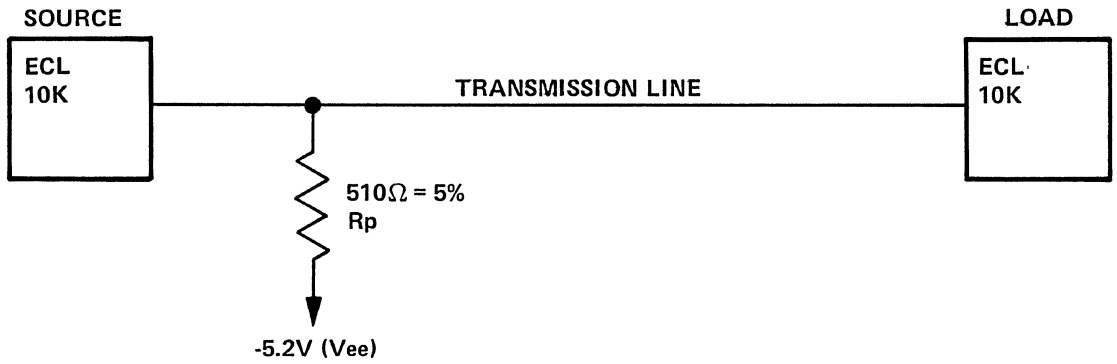


Figure 4-1. Placement of Rp on an ECL Line

Rt is connected to ECL 10K circuits, as shown in figure 4-2.

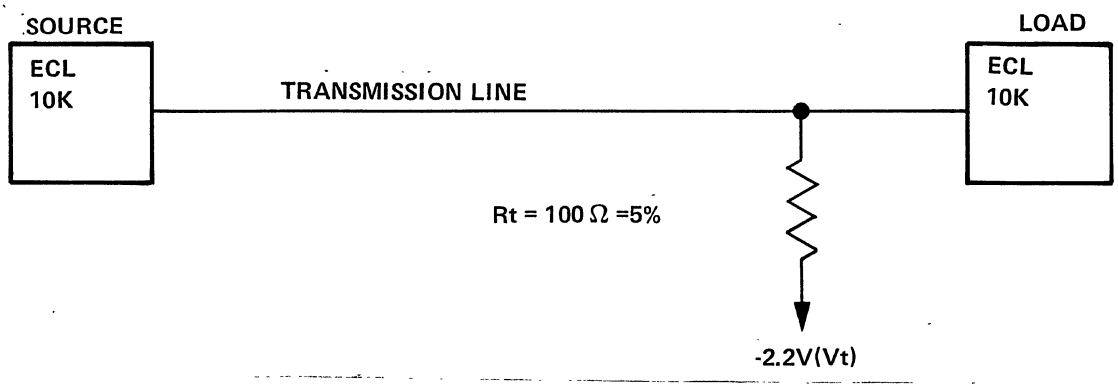


Figure 4-2. Placement of Rt on an ECL Line

In some conditions, either Rt or Rp may be used. However, there are times when one or the other is specifically required. Use the following rules when transmitting signals from one circuit to another on the module.

1. Rt is not required if there is an Rp on the line, and the line is less than 12 inches long, and the maximum number of loads is 4.

2. Rt must be connected if the line length exceeds 12 inches, or if the loading exceeds 4 gates. Rp is required for a line length of 48 inches or more, with distributed loads. If the loading exists only at the end of the line, Rp is not required.

When transmitting signals from one module to another, these are the rules that the designer uses:

1. Rp is not required for any output leaving a module, unless it is driving stub lines to other modules.

2. For every input to a module, there must be an Rt connected except for:

   a. Stub lines, as shown in figure 4-3.

   b. Daisy chaining, as shown in figure 4-4.

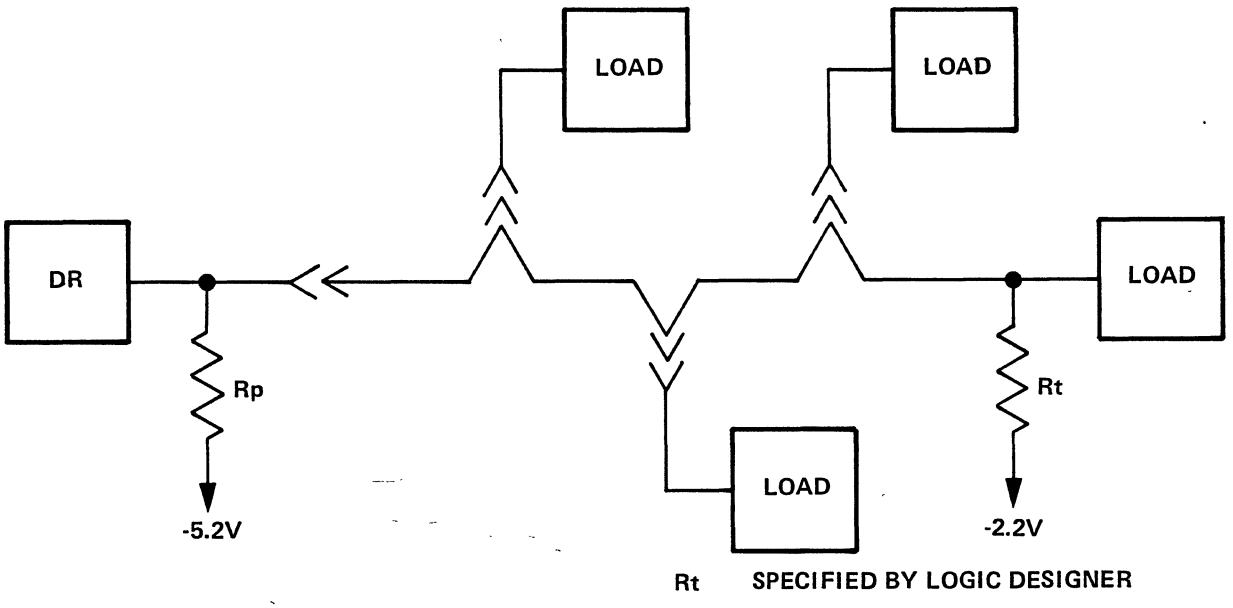


Figure 4-3. Stub Line

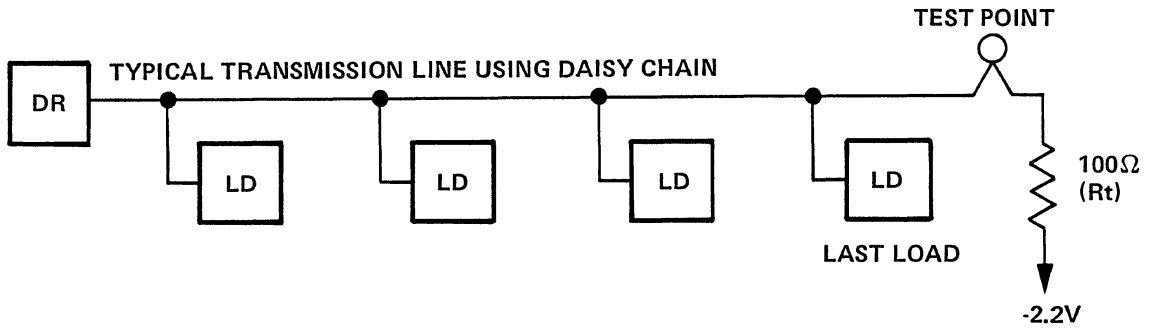


Figure 4-4. Daisy Chain

Figure 4-4 also shows where a test point is located on a terminated line. Note that a test point is always between the last gate load and the terminator. This permits a continuity check of the line and measurement of pulse timing at the load point.

Now let us see how the signal lines are connected to the modules. Between the connector pins of two modules which are wired together, you will find two wires. One is black; the other is white. These two wires are twisted together. The white wire carries the signal. The black wire is connected to ground at both ends.

Each connector pin location has two wire pins (see figure 4-5). One of the pins is connected to ground and the other is connected to the module. The purpose of the ground wire is to prevent signal distortion between modules. Study figure 4-5, which shows a typical signal path from the output of an ECL 10K circuit on one module to the input of the load circuit on another module.

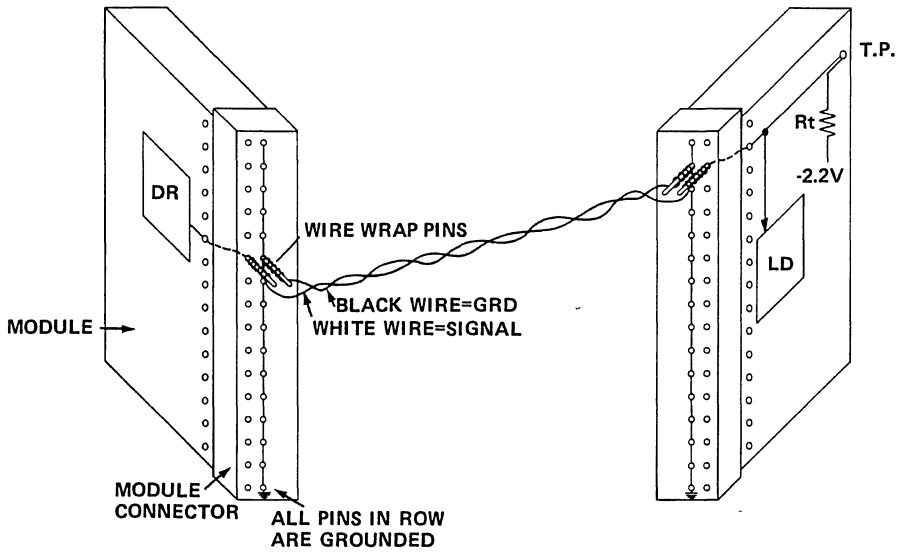


Figure 4-5. Inter-Module Wiring

CYBER 170 ECL Logic
Learning Activity 4-A

During this activity you learned the basic rules that designers must follow when creating logic circuits using ECL 10K circuits. This activity is not intended to enable you to design circuits but to understand better why some things are done the way they are in the CYBER 170 logic chassis.

LEARNING ACTIVITY 4-B. REFERENCE READING: DATA TRANSMISSION LOGIC CIRCUITS

During this activity you learn the logic circuits used by the CYBER 170 to transmit and receive signals. The circuits are used in both inter-chassis and data channel transmissions, which will be discussed in Learning Activities 4-C and 4-D.

OBJECTIVE

- You will be able to state the types of data transmission used and identify the types of logic circuits used in the CYBER 170.

Review the description of the following circuits in your ECL 10,000 Series Microcircuits manual, publication number 60417700.

10192 - Quad ECL Driver
10114 - Triple Line Receiver
TR00 - Pulse Transformer Module (last page of manual)

When you are ready to see applications of these circuits, go on to Learning Activity 4-C.

LEARNING ACTIVITY 4-C. TEXT READING: INTER-CHASSIS TRANSMISSION

During this activity you learn how data is transmitted between circuits from one CYBER 170 chassis to another.

OBJECTIVE

- You will be able to state the types of data transmission used and identify the types of logic circuits used in the CYBER 170.

Inter-chassis transmission uses a concept called "Twisted Pair Differential Transmission". This means that a signal is sent over two lines, and the difference in potential of the two lines determines what the output of the receiver will be.

In Learning Activity 4-A you learned that inter-module transmission uses two lines. However, one of the lines is always grounded. In differential transmission, both lines have a voltage potential. It is the difference in this potential that the receiver circuit uses to determine what its output state would be.

Refer to figure 4-6. It shows a typical differential transmission circuit. The 10192 driver circuit converts the ECL logic level input to a differential output. If the input signal (pin 5) is LO (Logical 1) and the enable (pin 7) is LO, then current will flow through output pin 3. There will be no current on output pin 4. The 10114 receiver circuit detects the difference in the two lines; because it has current on input pin 5, it will output a LO on pin 3 and a HI on pin 2.

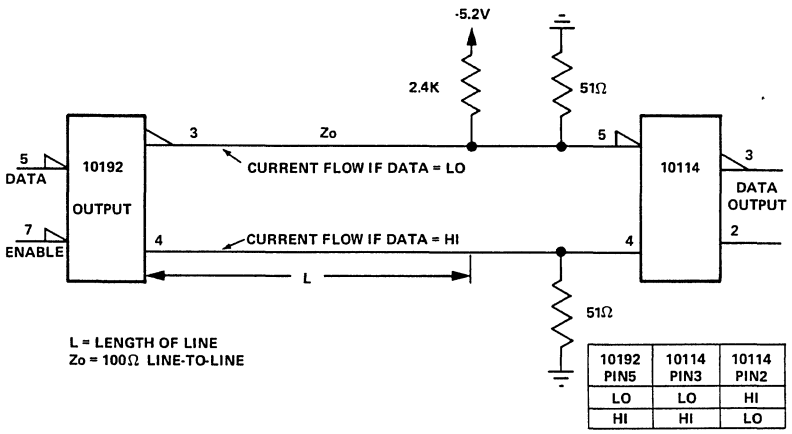


Figure 4-6. Differential Transmission

Conversely, if the level at pin 5 of the 10192 is HI (logical 0), current flow out of pin 4 occurs. This is felt at pin 4 of the 10114 receiver and causes a HI on its pin 3 and LO on pin 2.

This concept of differential transmission is used between chassis because of the distance the signal must travel. The 10114 is very sensitive to the amount of its input current. Because only one input line will have current at any given time, it can reliably output the correct logic level even with a high degree of signal degradation.

Figure 4-7 and 4-8 are logic diagrams of the KT-type and KR-type modules. They are used to transmit and receive data between CYBER 170 chassis.

Look at the KT module first. The logic is fairly simple to follow. Each KT module can transmit 8 bits of data simultaneously. The module contains a register of flip-flops and then a 10192 driver circuit for each data bit.

Now, look at the KR logic diagram to see what happens when the data comes into the chassis. Be sure to read the notes at the bottom of the diagram. The KR module can receive 8 data bits and hold them in a flip-flop register. Note that the 10114 receivers have no clocking term. They just sense the differential input and convert it to a logical level, which is then stored in the register. The register is often called a catching register. The last item to note on the KR module is the 10160 chip in the lower right. It generates a parity bit for the 8 data bits on the pak. This parity bit along with the parity bits from other KR modules will be used to check parity on the data word received by the chassis.

This concludes the activity on inter-chassis transmission. If you wish you may review the material.

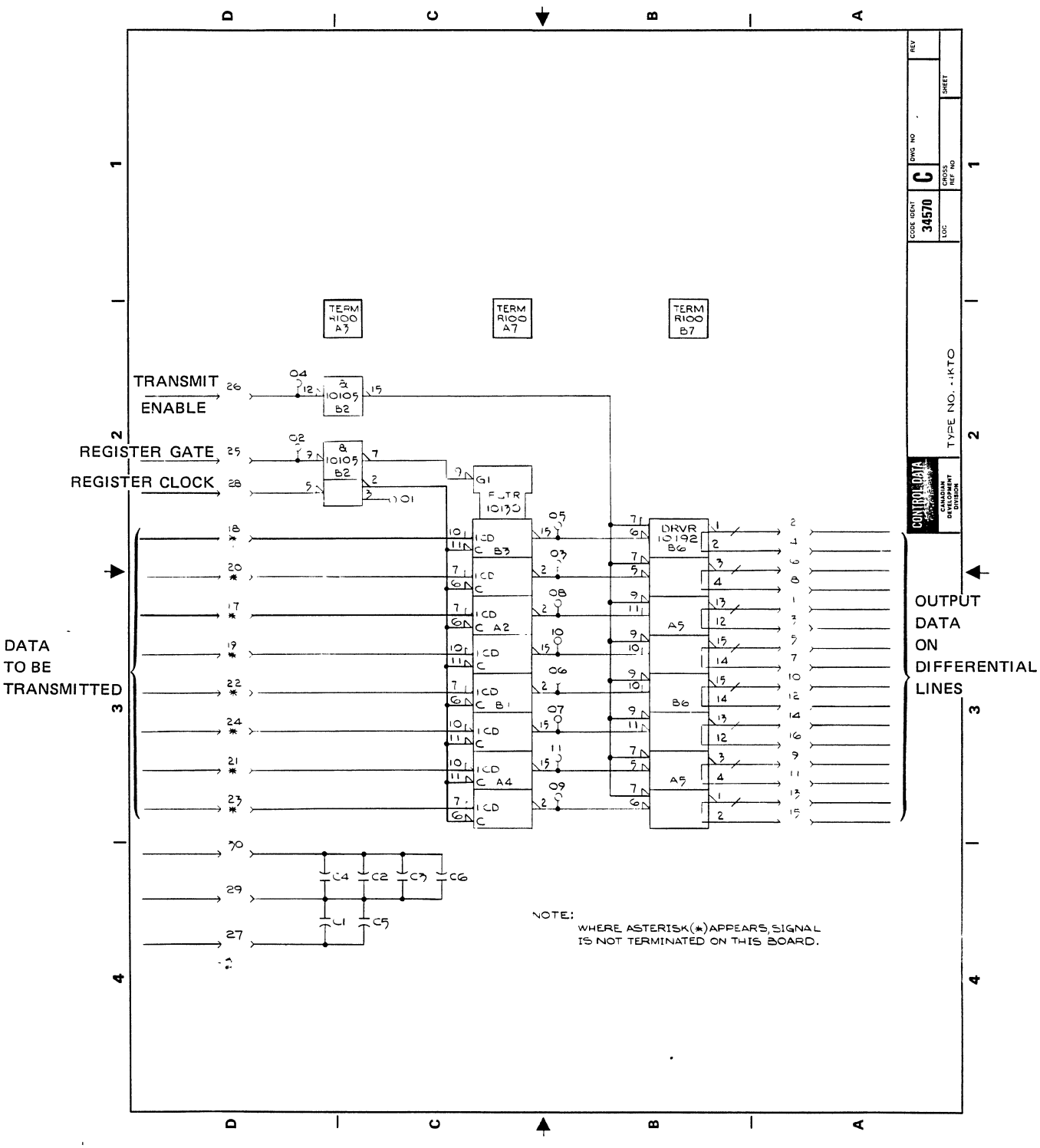


Figure 4-7. Typical 2102 Data Out Path

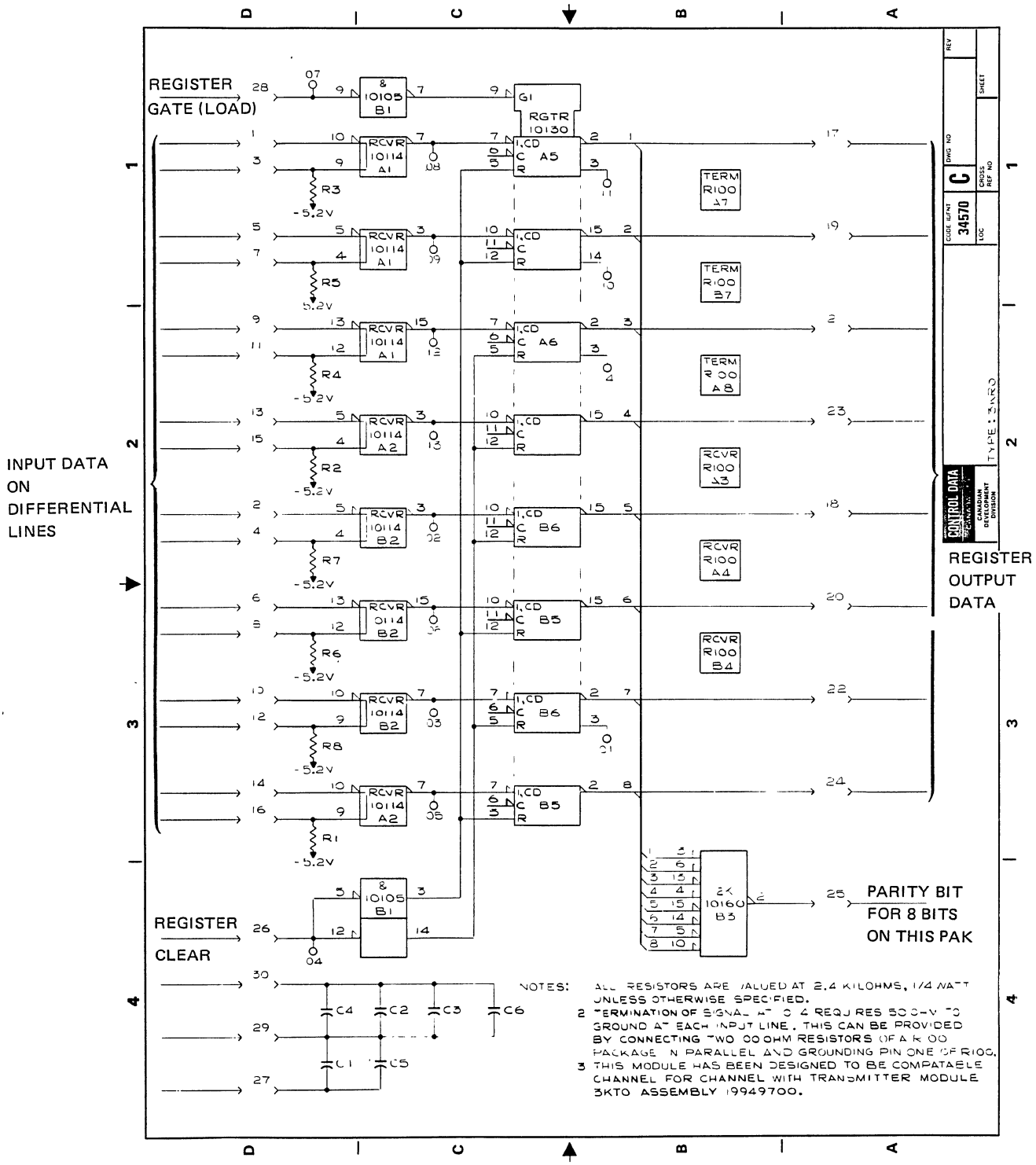


Figure 4-8. KR Receiver Module

LEARNING ACTIVITY 4-D. TEXT READING: COAXIAL CABLE TRANSMISSION

During this activity you learn how signals are transmitted on coaxial cable.

OBJECTIVE

- You will be able to state the types of data transmission used and identify the types of logic circuits used in the CYBER 170.

This type of transmission is used on the CYBER 170 data channel cables and, also, on the fanouts of the CYBER 170 master clock to each chassis in the mainframe.

Coaxial transmission is a pulse-type signal on a single wire. This single wire runs through a grounded shield. By using this system, the signal on the wire has almost no interference from external sources. Figure 4-9 shows the basic construction of a coaxial cable.

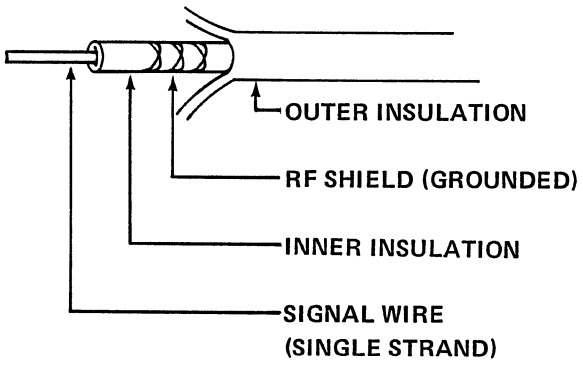


Figure 4-9. Coaxial Cable Construction

A simplified circuit using coaxial transmission is shown in figure 4-10. The transmitter circuit requires a data input and a clock. Data is transmitted at clock time. The output of the transmitter circuit drives a center-tapped transformer unit. The output of the transformer is tied to the coaxial cable.

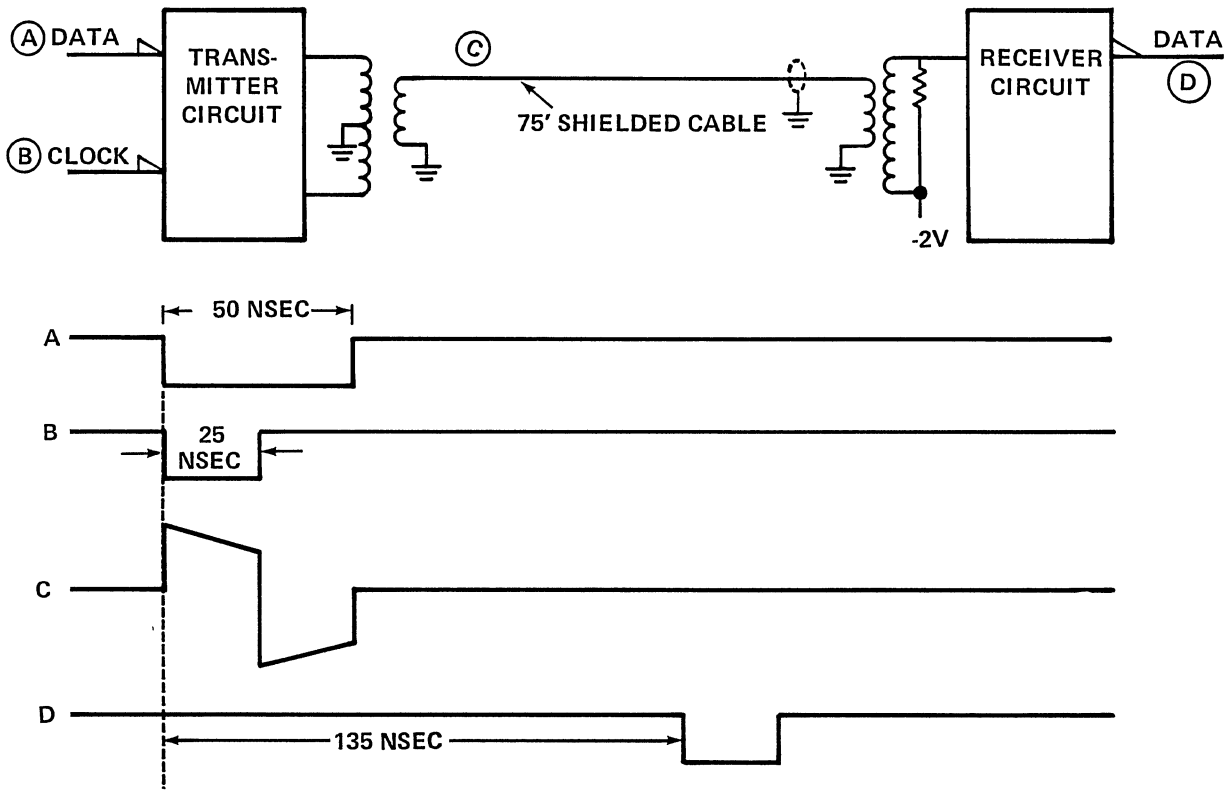


Figure 4-10. Coaxial Transmission

The signal on the cable is as shown on the figure. It is positive for the same duration that both inputs are LO. It is negative when only the data input is LO. You should note that only logical ones (LOs) are transmitted as pulses on coaxial cable. If the data input is a logical zero (HI) at clock time, there will be no pulse on the cable.

On the receiver side of the circuit you also see a transformer unit that matches the impedance of the line to the receiver. The receiver output is LO for the duration of the positive portion of the pulse. During the negative portion of the pulse, the receiver output is HI. The output of the receiver feeds some type of catching register that can hold the information received. The receiver itself cannot hold data; therefore, the register is needed for that purpose.

The 75-foot cable is the standard length in the CYBER 170 system data channels. All cables must be exactly the same length in order for the data to be synchronized with the control signals that are used in the data channels. As shown in the figure, 75 feet of cable, plus the switching times of the circuits, yields a total transmission time of 135 nanoseconds.

Figure 4-11 shows how the transmitter section is formed using ECL logic circuits. There are two 10192 circuits and on TR-00 circuit in each transmitter. When they are connected as shown, the output of the TR-00 circuit will be the pulse on the coaxial cable.

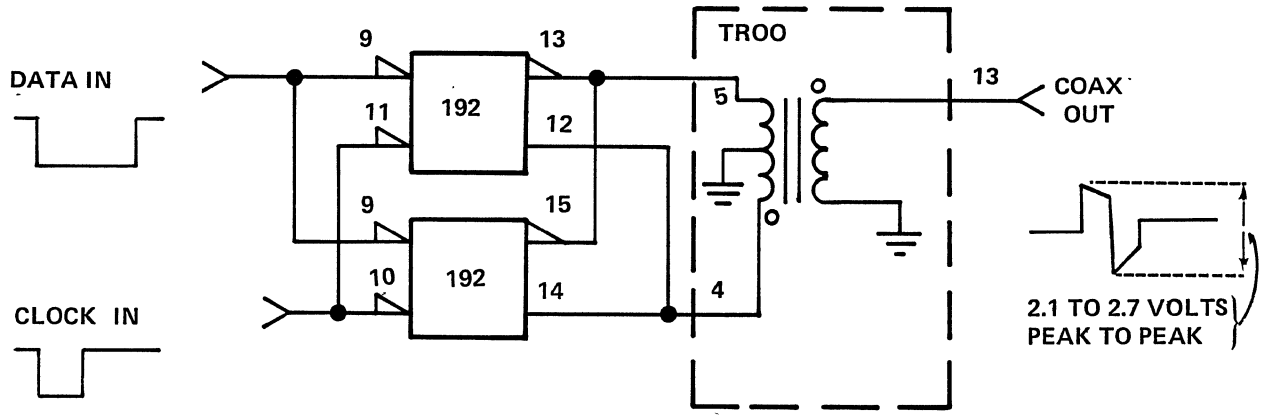


Figure 4-11. ECL Coaxial Transmission

Figure 4-12 shows a typical ECL receiver circuit for coaxial cable. It requires one TR-00 transformer circuit and one 10114 receiver circuit. When the circuits are connected as shown they will convert the coaxial pulse input to a logic pulse input to a logic output.

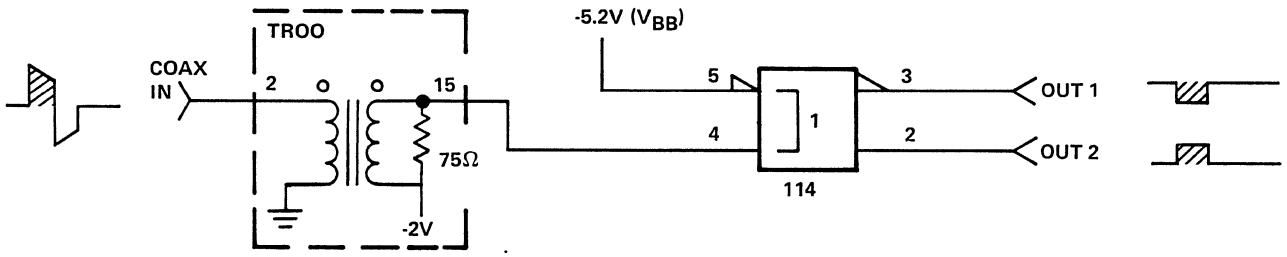


Figure 4-12. ECL Coaxial Receiver

This concludes the activity on coaxial cable transmission. During this activity you have learned the purpose of coaxial transmission and the circuits needed to transmit and receive signals on coaxial cable.

LEARNING ACTIVITY 4-E. EXERCISE: DATA CHANNEL LOGIC DIAGRAM

During this activity you learn how the CYBER 170 data channels function.

OBJECTIVE

- You will be able to state the types of data transmission used and identify the types of logic circuits used in the CYBER 170.

The data channels are bidirectional devices. They can transmit or receive data from PPU memories and peripheral equipment. As you recall from the overview course, each CYBER data channel can be accessed by any one of the PPUs in the mainframe.

Each data channel contains one 12-bit data register. This register is bidirectional. All input data to the PPUs and output data to the peripherals go through the channel data register. Also, if two PPUs communicate over a data channel, they send data through the channel register to each other.

Figure 4-13 shows how all this is done on a block diagram. Study the diagram before continuing this activity.

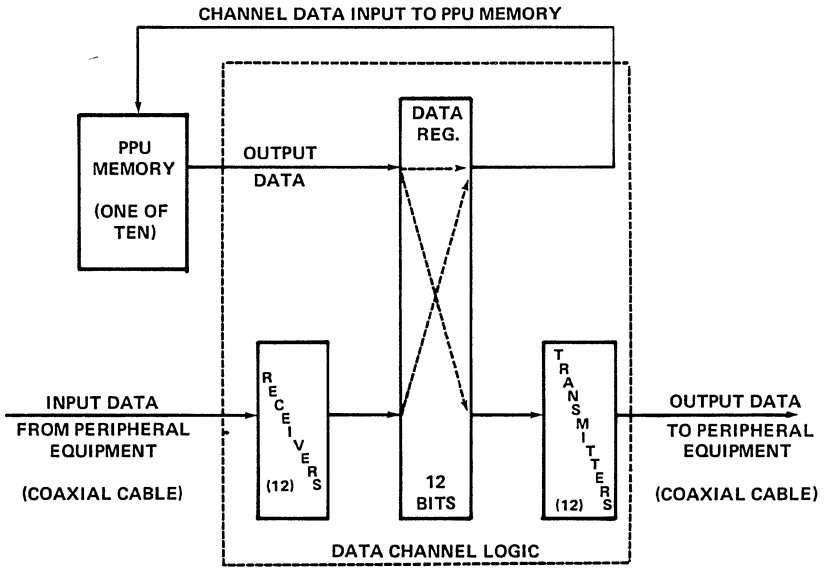


Figure 4-13. CYBER 170 Data Channel

CYBER 170 ECL Logic
Learning Activity 4-E

Figure 4-14 is the logic diagram of an AP module. It contains four bits of the data channel.

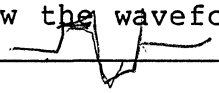
Directions: Study the circuit, then answer the following questions about its operation. Check your answers with those at the end of the activity to be sure that you understand the operation of the circuit.

1. What are the locations of the four channel data register bits? A4, A2, A6, A8,

2. How is each channel data register bit able to hold data? Pin 2 ⇒ 15 latch

3. How many AP modules are needed to make an entire data channel? 3

4. Draw the waveform of a one on module pin 16.



5. Which module input pin must be LO to gate input channel data into the channel data register? Pin 25

6. A PPU memory is inputting from the channel. What is the path for bit 20 through the AP module? List module pins and circuits.

module pin 22 → B5 → A2 → A0-4 module pin 3

7. A PPU memory is outputting to the channel and another PPU is inputting from the same channel. List the path through the AP module used by bit 2^2. Pin 17 A2-9 Pin 7

8. What type of cable will be connected to module pin 4? Co-Axial

9. A PPU memory is outputting data to a peripheral equipment. List the path through the AP module used by bit 21. Pin 21 - A6=9 A5-4 B4-9 B2-4 Pin 4

10. What happens when module pin 6 goes LO? B6-14 goes hi breaking data holding latch clearing register

11. What is the purpose of the CLOCK signal on module pin 5? transmit data out

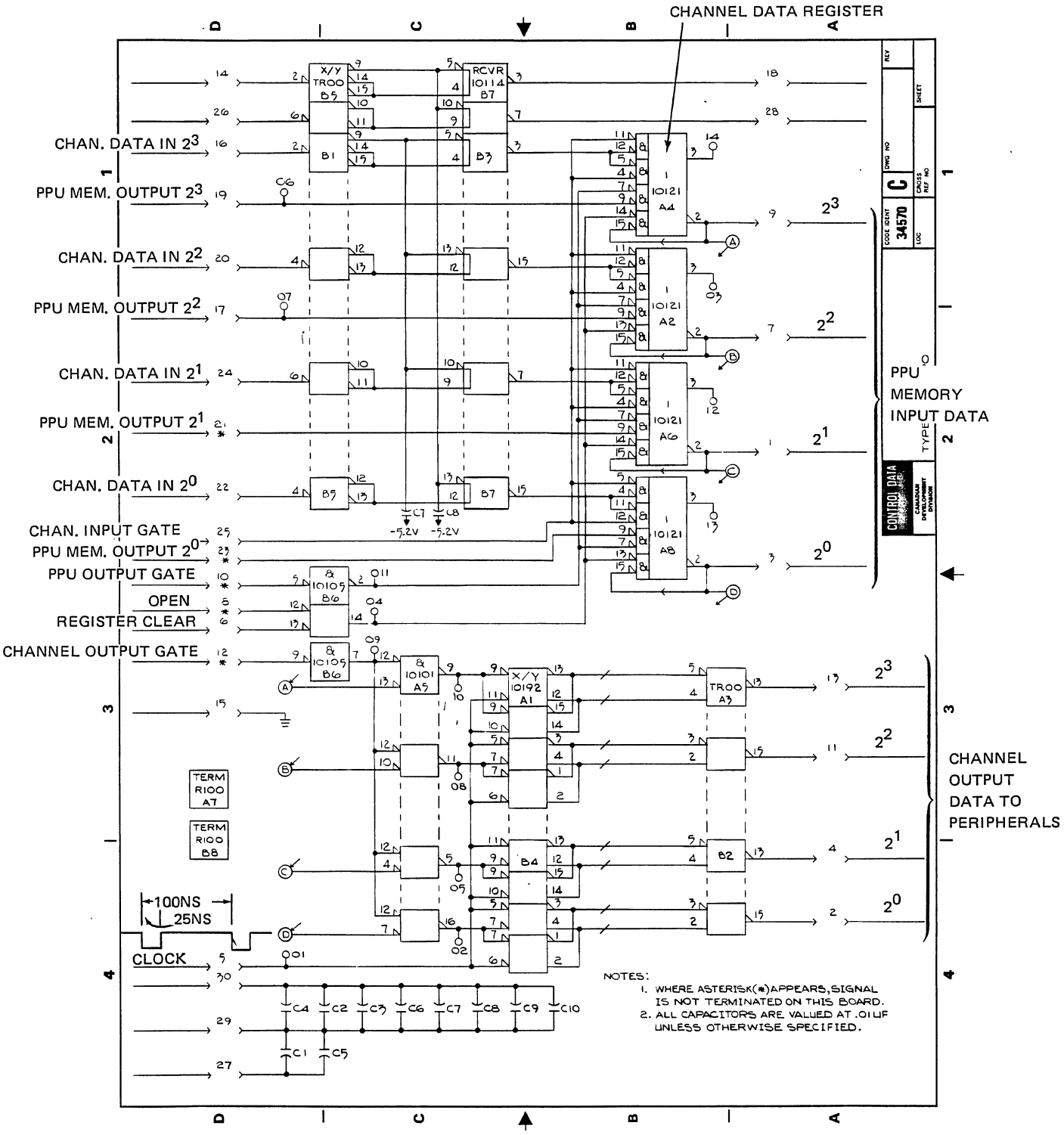


Figure 4-14. 4AP0 Logic Diagram

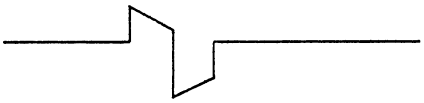
This concludes the exercise on the data channel logic diagram. During this activity you have seen an application of coaxial cable receivers and transmitters. You also have seen how the CYBER 170 data channel is a bidirectional circuit allowing inputs and outputs to occur while using only one register.

ANSWERS FOR LEARNING ACTIVITY 4-E

1. A4, A2, A6, and A8.

2. It is wired into latch. The LO output is wired back to one of the input AND gates. (Refer to Learning Activity 2-B, Exercises 2B-6 and 2B-7 to review this concept.)

3. 3 modules; each contains 4 bits of the 12-bit data channel.

4.  The input from the channel is on coaxial cable.

5. Module pin 25, channel input gate.

6. Module pin 22 ⟶ B5-4 ⟶ B7-12 ⟶ A8-4, 11 ⟶ module pin 3.

NOTE

Two sections of A8 have the same inputs. This is because one of them is not needed and it was easier to wire in the signals than to disable the gate.

7. Module pin 17 ⟶ A2-9 ⟶ module pin 7.

NOTE

When PPU memories communicate, they do not use the transmitters and receivers.

8. Coaxial cable

9. Module pin 21 ⟶ A6-9 ⟶ A5-4 ⟶ B4-9 ⟶ B2-4, 5 ⟶ module pin 4.

10. B6-14 goes HI which breaks the latching inputs to the channel data register, thus clearing the register.

11. It is used to form the coaxial pulses at the appropriate time when outputting data to the peripherals.

LEARNING ACTIVITY 4-F. TEXT READING: MULTI-LEVEL DIAGRAM USAGE

During this activity you learn how to use the multi-level diagrams that are in each CYBER 170 Hardware Maintenance manual.

OBJECTIVE

- You will be able to identify the different diagrams used on the CYBER 170.

Each chassis of the CYBER 170 mainframe has its own diagrams manual. In these manuals you find four levels of diagrams. The four levels and their titles are:

- Level 1 - Primary Block Diagram
- Level 2 - Secondary Block Diagrams
- Level 3 - Detailed-Pak Diagrams
- Level 4 - Logic Diagrams

At different times while learning and maintaining the CYBER 170 system, you are required to use each of these levels of diagrams.

To show you what is on each type of diagram we will use examples from the CYBER 170 Peripheral Processor Subsystem (PPS) Diagrams manual.

First of all, figure 4-15 is the primary block diagram of the PPS. Note that the sheet number in the lower right corner is 1.0. That indicates it is a level 1 diagram. The primary block diagram contains everything included in a chassis on large scale blocks. All the registers, memories, adders, and so forth that are in the chassis are shown. The diagram also shows how they are interconnected. Although only limited maintenance can be performed using a primary block diagram, it is extremely useful when learning the equipment, especially in finding the more detailed logic for a particular section of the chassis. Basically, it helps you keep a "big picture" of what is happening in a chassis.

During this activity we follow the logic for the A adder logic through the various levels of diagrams. On the primary block diagram, the A adder is in the upper right at coordinates 3D.

The secondary block diagram for the A adder is shown in figure 4-16. Note that this diagram only has blocks for the A register slot and barrel. Its sheet number is 2.0. In the PPS diagrams there are a total of 12 level 2 diagrams, numbered from 2.0 through 2.11.

Secondary block diagrams show all the logic modules used by a particular section of the chassis. Each module type and its location are shown. There is little information about control signals on level 2 diagrams. The most important purpose of these diagrams is to follow data paths. Then they become useful because you can see a fairly long string of data path modules without having to turn a number of pages in the manual. In effect, you will probably use these diagrams after learning the basics of the chassis operation as a quick reference for module locations while troubleshooting the system.

The logic for the A adder is in the lower right of the 2.0 diagram at sheet coordinate B1. Each of the module types is AH, and their locations are at F38, G38, H38, I38, and J38. Each block also shows which bits are at each location. For example: bits 4-7 are at location I38. If you are mainly concerned with finding where certain bits are located, then you will find the level 2 diagrams very useful.

If, however, you need to know what control signals are on a module, then you may need to use the level 3 Detailed Pak Diagrams (DPD) to find them. Figure 4-17 is a DPD for the A adder. Note that its sheet number is 3.0. The PPS chassis has 21 level 3 diagrams numbered from 3.0 through 3.20. The DPDs show all the modules in a chassis, including their types and locations. However, they show in greater detail what is happening on each module. Items such as equations, gating signals, translations, and so forth appear in these diagrams.

The DPDs are very useful for both learning and maintaining the system. On the facing pages of the DPDs, you often will find test point charts for the key signals on the sheet. Therefore, you can do a significant amount of troubleshooting, either by module swapping or with the oscilloscope, using these diagrams.

The logic for the A adder is on the right center of the sheet at coordinate 2C. As you can see, it has more detail than the level 2 diagram has.

About the only times you will have to go beyond the level 3 diagram are to find a module pin number, a test point not listed in the test point chart, or to verify the operation of a circuit if you have doubts about the way it works.

Figure 4-18 is the level 4 logic diagram of an AH module. you should be familiar with these diagrams already, as they are what you have studied in modules 2 and 3 of this course. You studied the AH module in Module 2, Learning Activity 2-L.

The logic diagrams do not have sheet numbers. They are found in the diagrams manual after the last 3.X diagram and placed in alphabetic order by module type: AA, AB, AC,..., AZ, BA,..., BZ, and so forth.

Because there is more than one AH module in the PPS chassis, you will not find a complete set of input and output signal names. Instead, there are abbreviated names to show you approximately where the signal is located. For example, in figure 4-18, module input pin 21 has the letter N on its line, which means bit N of the input data. The N could be bit 0, bit 4, bit 8, bit 12, or bit 16 of the adder, depending on what the location of the module in the chassis.

To determine the exact signal name for each module pin in the chassis, you need to use the wire lists for that chassis. You learn how to read wire lists in the next learning activity.

This concludes the activity on multi-level diagrams. You have seen that there are four levels of diagrams for each CYBER 170 chassis and you have learned the basic purpose of each. At this time you may review the material of this lesson if you wish.

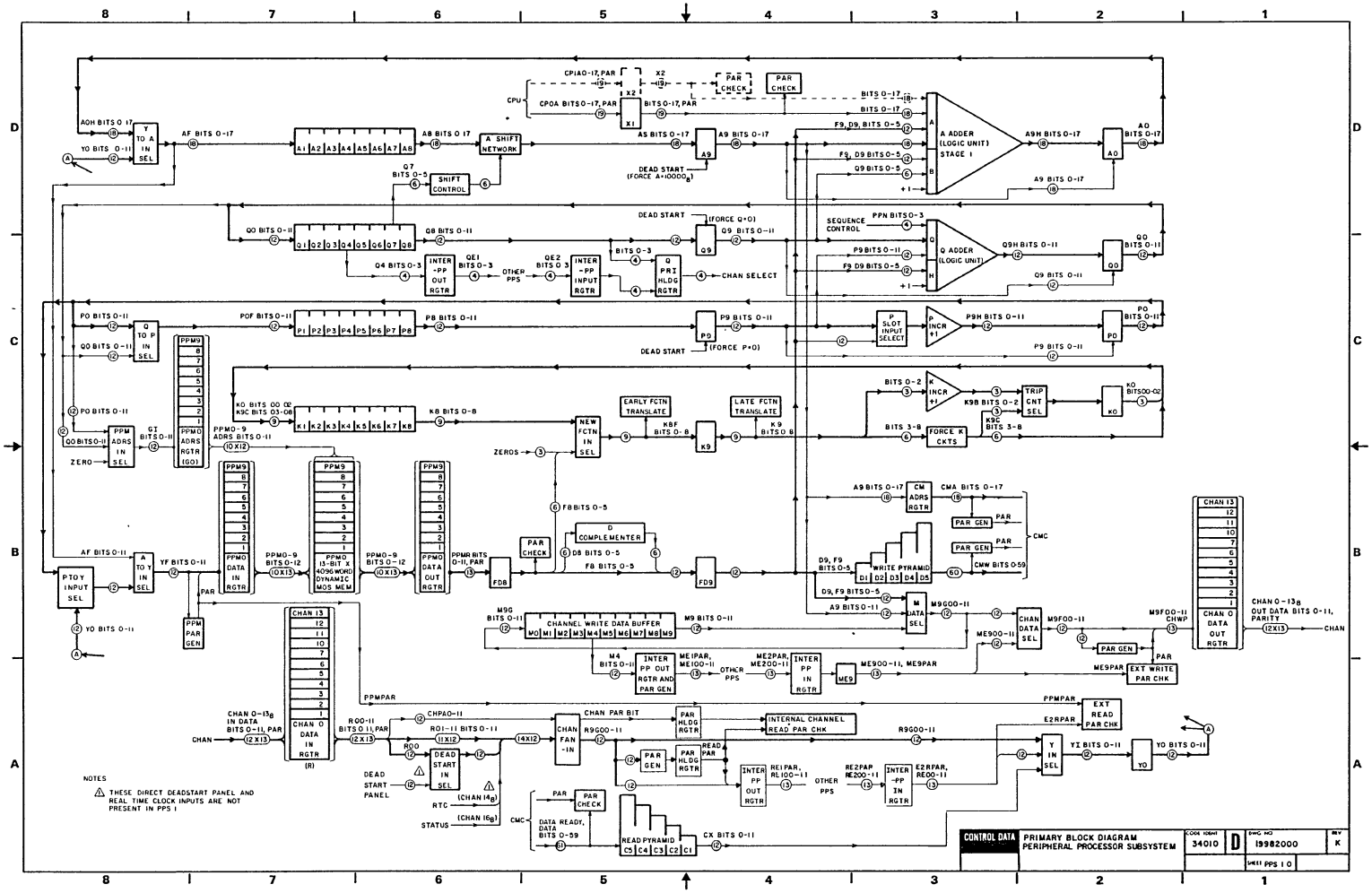


Figure 4-15. Level 1 - Primary Block Diagram

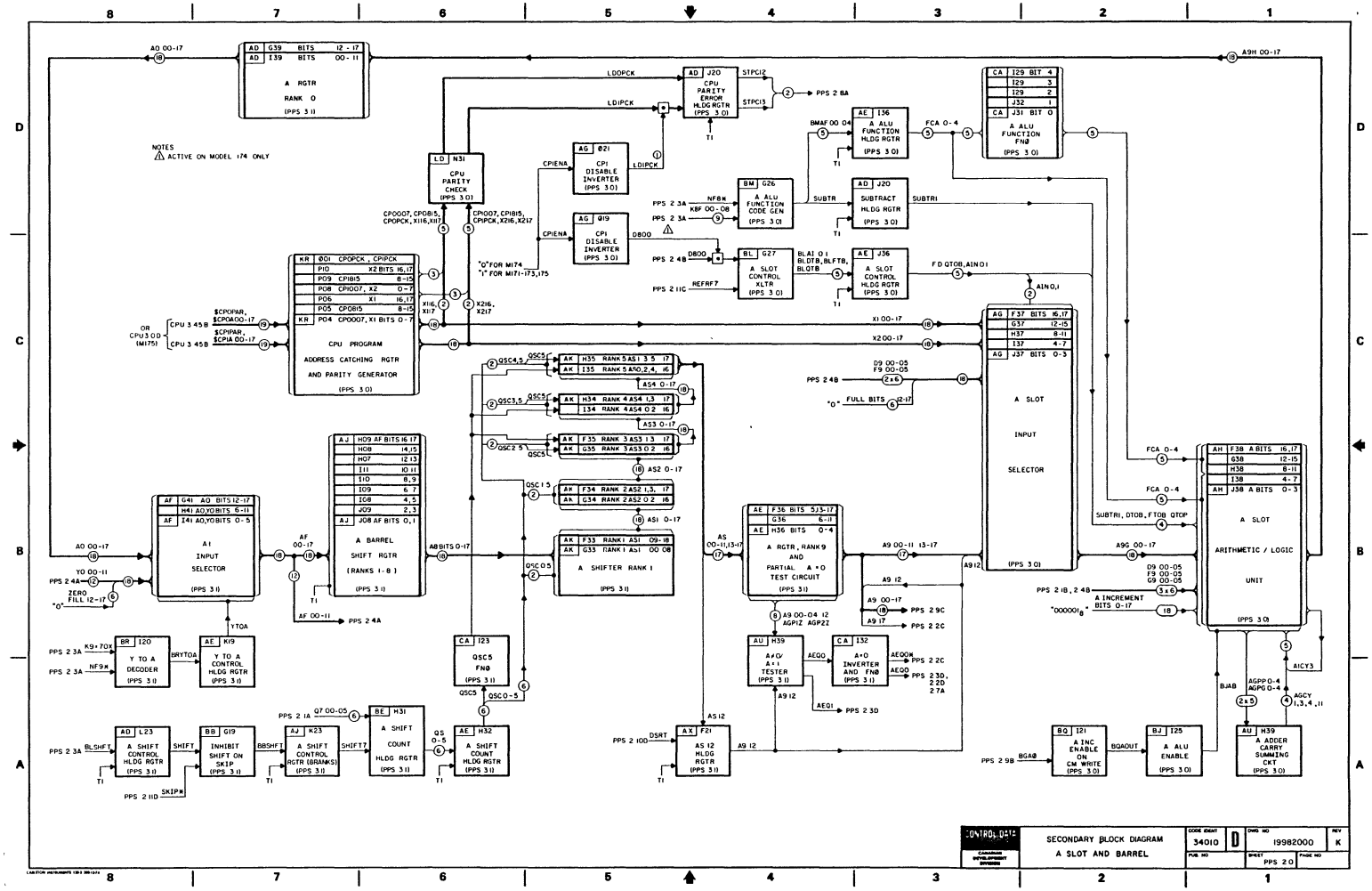


Figure 4-16. Level 2 - Secondary Block Diagram

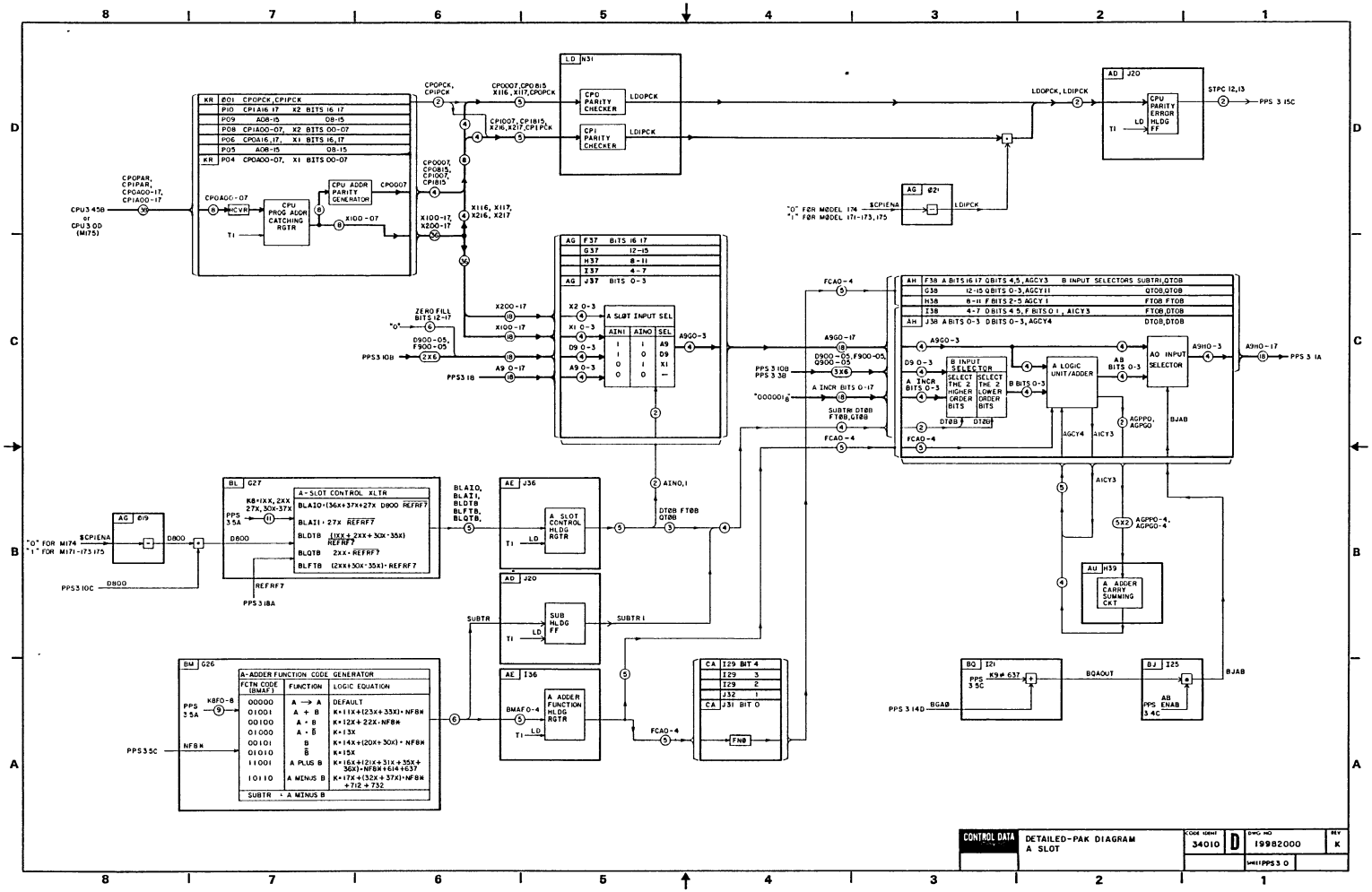


Figure 4-17. Level 3 - Detailed Pak Diagram

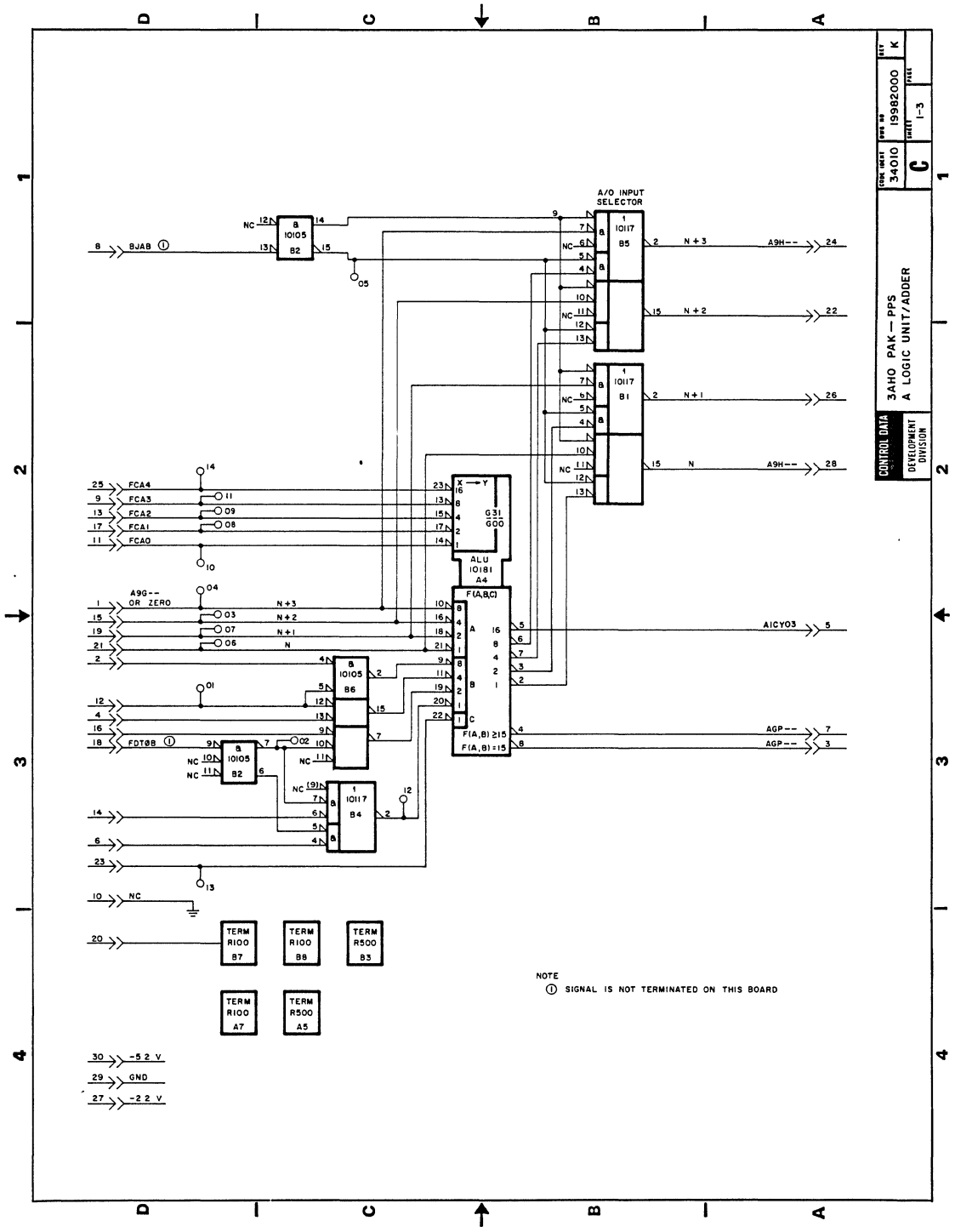


Figure 4-18. Level 4 - Logic Diagram

LEARNING ACTIVITY 4-G. TEXT READING: WIRE LISTS

During this activity you learn how to read CYBER 170 chassis wire lists.

OBJECTIVES

- You will be able to trace and analyze signal paths in a set of wire lists.

As you learned in the previous learning activity, at times you need to use wire lists to find out which signal wire is connected to a module wire-wrap pin. You also need to use the wire list to follow the path of a signal wire if it is daisy-chained to several module locations.

In the wire list manuals, there is one page for each module location. The module locations are arranged in sequence by chassis location (A01 through R42); locations not used are omitted from the listings.

The following information appears on each page of the wire lists. Refer to figure 4-19, Sample Wire List, as you read the list.

- Pak: chassis location.
- Pins: connector pin numbers (01 through 30) on the backpanel.
- Signal name: name assigned to the wire connected to the pin. (This name also appears on the logic diagram of the pak installed in that chassis location.)
- Z-level (1, 2, 3, unassigned): indicates the position of the wire wrap on the connector pin: the higher the number, the greater the distance between the wire wrap and the backpanel. (Unassigned indicates wires may be at any level.)
- Lth: length (in inches) of the wire.

The following list provides additional information about the wire list:

- Two or more Z-level entries beside a pin indicate multiple wire wraps on the pin (the signal is daisy-chained).
- Wiring differences are indicated by notes (1) .

- Crosstab symbology.
- A / indicates that the signal at a pak does not originate from that location (for example, PP031-01/01G). A * indicates signal origin at that location (for example, PPR08-28*28G). A ---- indicates signal pin is grounded (for example, GRND-15G/----).

Study the example in the figure. Be sure to read the explanatory notes.

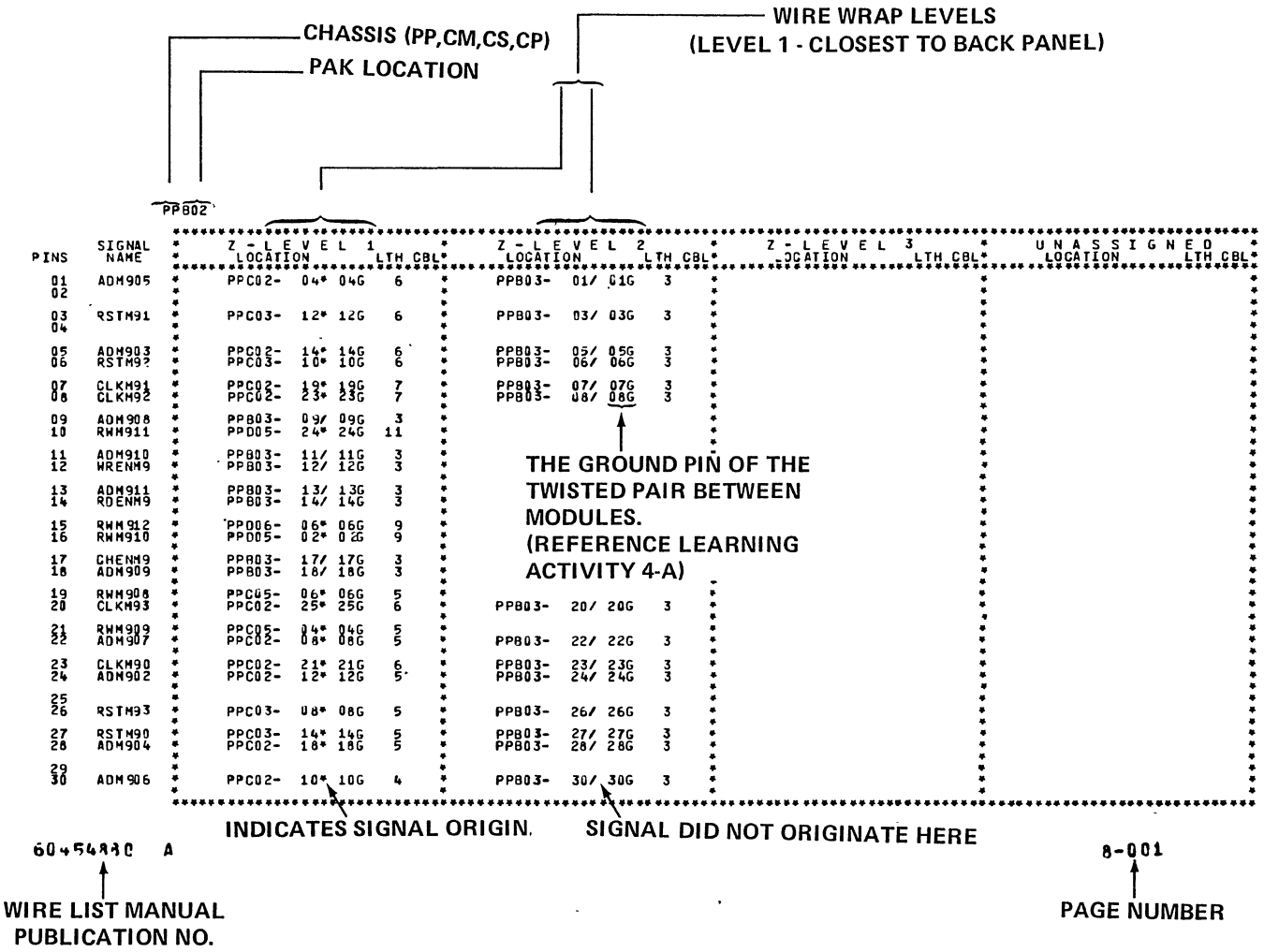


Figure 4-19. Sample Wire List

Let us look at an example. Figure 4-20 is the logic diagram of an AH module (the same diagram you saw in Learning Activity 4-F). Figure 4-21 is the wire list for the AH module at location I38. The AH module in that location is bits 4-7 of the PPS A adder. (Refer to figure 4-17, Learning Activity 4-F, if you wish.)

We will use three different operations with figures 4-20 and 4-21. They are:

- Input Pin Connections
- Output Pin Connections
- Daisy Chain Connections

First of all, look at an input pin. On the logic diagram, module pin 1 is labeled A9G--; further on it is called N+3. On the wire list, module pin 1 is labeled A9G07. Because location I38 contains bits 4-7 of the adder bit, N is bit 4; therefore, bit N+3 would be bit 7. The origination of the signal on module pin 1 is from location PPI37 pin 7, and the wire is a wire-wrap level 1.

By looking at the wire list itself you can often determine if the signal on a pin is an input or output. This is done by looking for a * or a / symbol. The wire list connection for I38-01 has a * in it (I37-07*07G). It means the signal came from I37 to I38.

Now, look at an output pin connection. Module pin 24 of the logic diagram is labeled A9H---, with N+3 just before it. On the wire list, module pin 24 is labeled A9H07, which means it is bit 7 of the adder output (bit N = 4; bit N+3 = 7). This output pin goes to location I39, pin 23. The wire length is 4 inches.

The slash (/) symbol on the wire connection (if there is no other connection) usually can be interpreted as saying that the module pin is an output pin.

Finally, let us look at daisy-chain connections. Module pin 18 has a daisy-chained signal on it. The signal is called "DT0B-3". It originated at J36, pin 24 and goes to I38, pin 18. From there, it goes to I37, pin 14. You would have to look at the wire list for I37 to see if it terminates there or continues on to other modules.

I38, pins 6 and 8, are also daisy-chain connections. However, there is no * symbol on either level, which means that the signal has been passed on at least once before it gets to I38. Also, I38 is passing it on to another module.

This concludes the activity on wire lists. You may review this material if you wish.

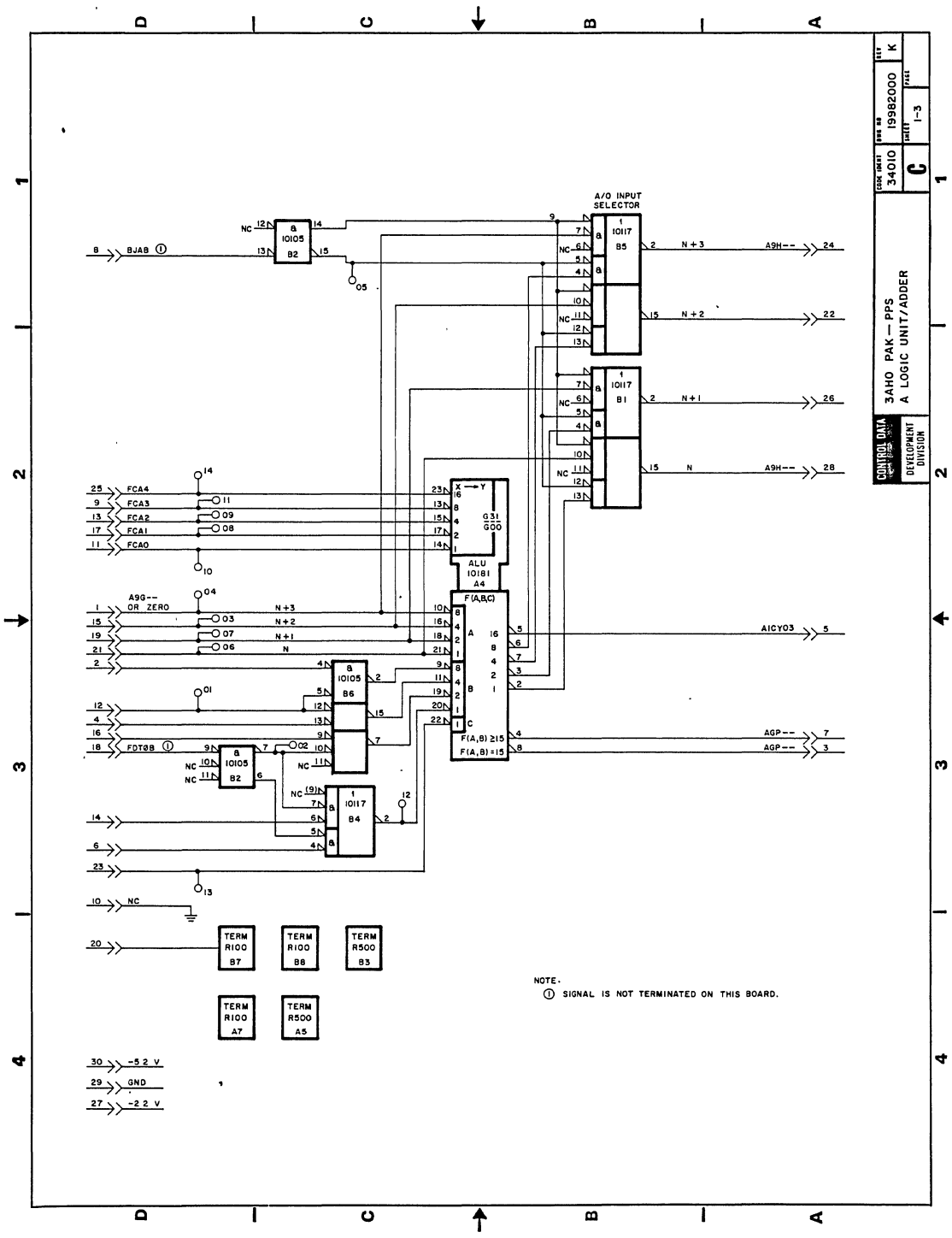
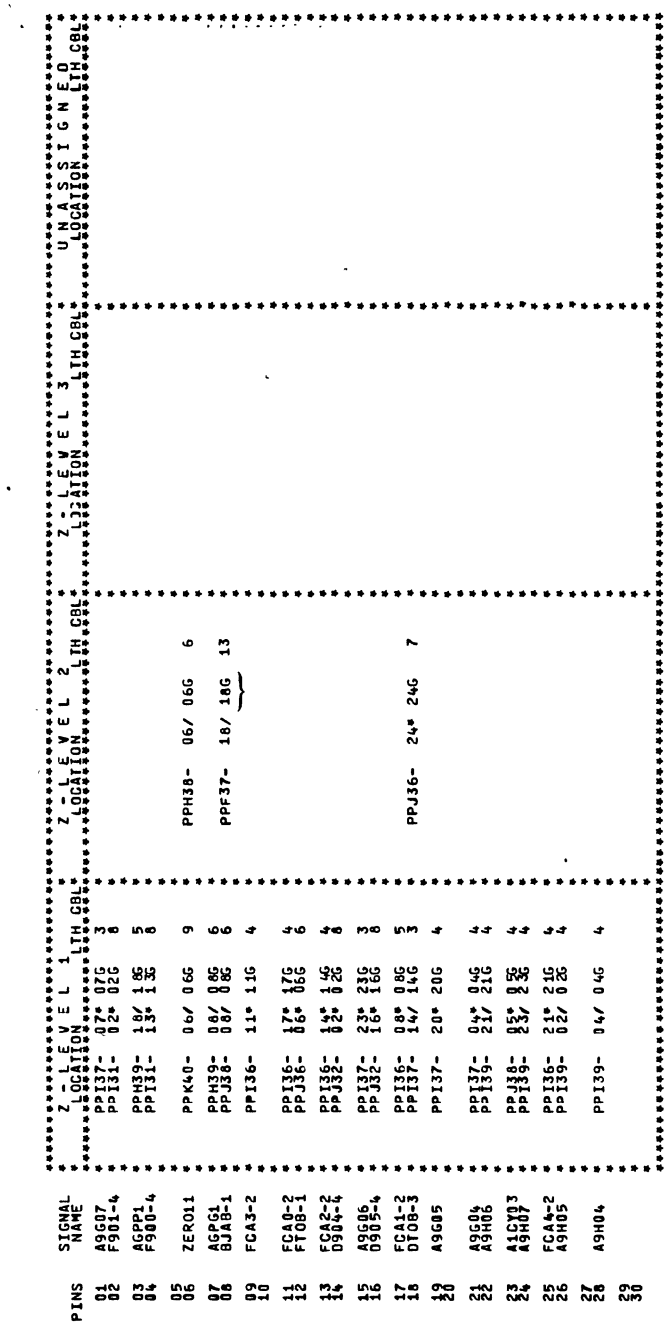


Figure 4-20. Logic Diagram - AH Pak



PINS	SIGNAL NAME	Z-LEVEL 1 LOCATION	LTH	GBL	Z-LEVEL 2 LOCATION	LTH	GBL	Z-LEVEL 3 LOCATION	LTH	GBL	UNASSIGNED LOCATION	LTH	GBL
01	A9G07	PPI37- 07* 07G	3										
02	F901-4	PPI31- 02* 02G	8										
03	AGPP1	PPH39- 19/ 19G	5										
04	F900-4	PPI31- 13* 13G	8										
05													
06	ZERO11	PPK40- 06/ 06G	9		PPH38- 06/ 06G	6							
07	AGPG1	PPH39- 08/ 08G	6										
08	8JA8-1	PPJ38- 08/ 08G	6		PPF37- 18/ 18G	13							
09	FCA3-2	PPI36- 11* 11G	4										
10													
11	FCA0-2	PPI36- 17* 17G	4										
12	FT08-1	PPJ36- 06* 06G	6										
13	FCA2-2	PPI36- 14* 14G	4										
14	D904-4	PPJ32- 02* 02G	8										
15	A9G06	PPI37- 23* 23G	3										
16	D905-4	PPJ32- 16* 16G	8										
17	FCA1-2	PPI36- 08* 08G	5										
18	DT08-3	PPI37- 14/ 14G	3		PPJ36- 24* 24G	7							
19	A9G05	PPI37- 20* 20G	4										
20													
21	A9G04	PPI37- 04* 04G	4										
22	A9H06	PPI39- 21/ 21G	4										
23	A1CY03	PPJ38- 05* 05G	4										
24	A9H07	PPJ39- 23/ 23G	4										
25	FCA4-2	PPI36- 21* 21G	4										
26	A9H05	PPI39- 02/ 02G	4										
27													
28	A9H04	PPI39- 04/ 04G	4										
29													
30													

Figure 4-21. I38-Wire List

LEARNING ACTIVITY 4-H. TEXT READING: CABLES WIRE LISTS

During this activity you learn how to read and use the cable wire lists for the CYBER 170 mainframe. Also, you learn the general cabling scheme that is used to connect chassis in the mainframe bays.

OBJECTIVE

- You will be able to trace and analyze signal paths in a set of wire lists.

Figure 4-22 is the cable connection diagram for the CYBER 170 mainframe, with the optional chassis also shown. This diagram shows every cable in the mainframe itself. As you can see, the system uses many cables to get all the data and signals moved between its various chassis.

The I/O connector panels in the diagram are physically located at the end of the mainframe bays opposite the power control panel end. Using these I/O connector panels makes it easier to add equipment options, and so forth, because the cables can be disconnected and connected at the panel with a minimum of wiring.

Note that some cables have a prefix designation of W. These cables have a connector on one end that goes to the I/O connector panel. However, each individual wire is physically attached to a module pin in the chassis to which the cable goes. There is no connector on the chassis itself.

The WXX cables are each fed through a hole in the chassis frame, and then each wire is connected to the designated module.

Whenever you are following a signal through the cables, use the cable connection diagram to see where it goes before looking at the cable wire list for the actual pin numbers. The diagram is in the front section of the cable wire list manual for your system.

Now, let us follow a data line from its origin in the PPS chassis to its destination in the CMC chassis. We will use data bit 0 of a 60-bit word to be transmitted from PPS to CMC.

On the cable connection diagram the data to CMC from PP0 leaves the PPS-0 chassis on cable W45 and connects to J14 in the I/O connector panel. From the I/O connector panel, it goes to J32 in the CMC chassis. The cable between J14 and J32 is a standard 6-foot cable, with the pin numbers the same on both ends.

Now, let us see how to use the cable wire list to follow the signal. Figure 4-23 is the wire list for cable W45. It has notes describing what each term means.

Data bit 0 has the signal name $PP0D00. You should find that it comes from location 002 of the PPS chassis (from pins 15 and 13 of that module). The same connections are listed in the module wire lists. The W45 cable jack pin numbers for the signal are A01 and A02. These cable pin numbers will be retained until the signal reaches the next chassis.

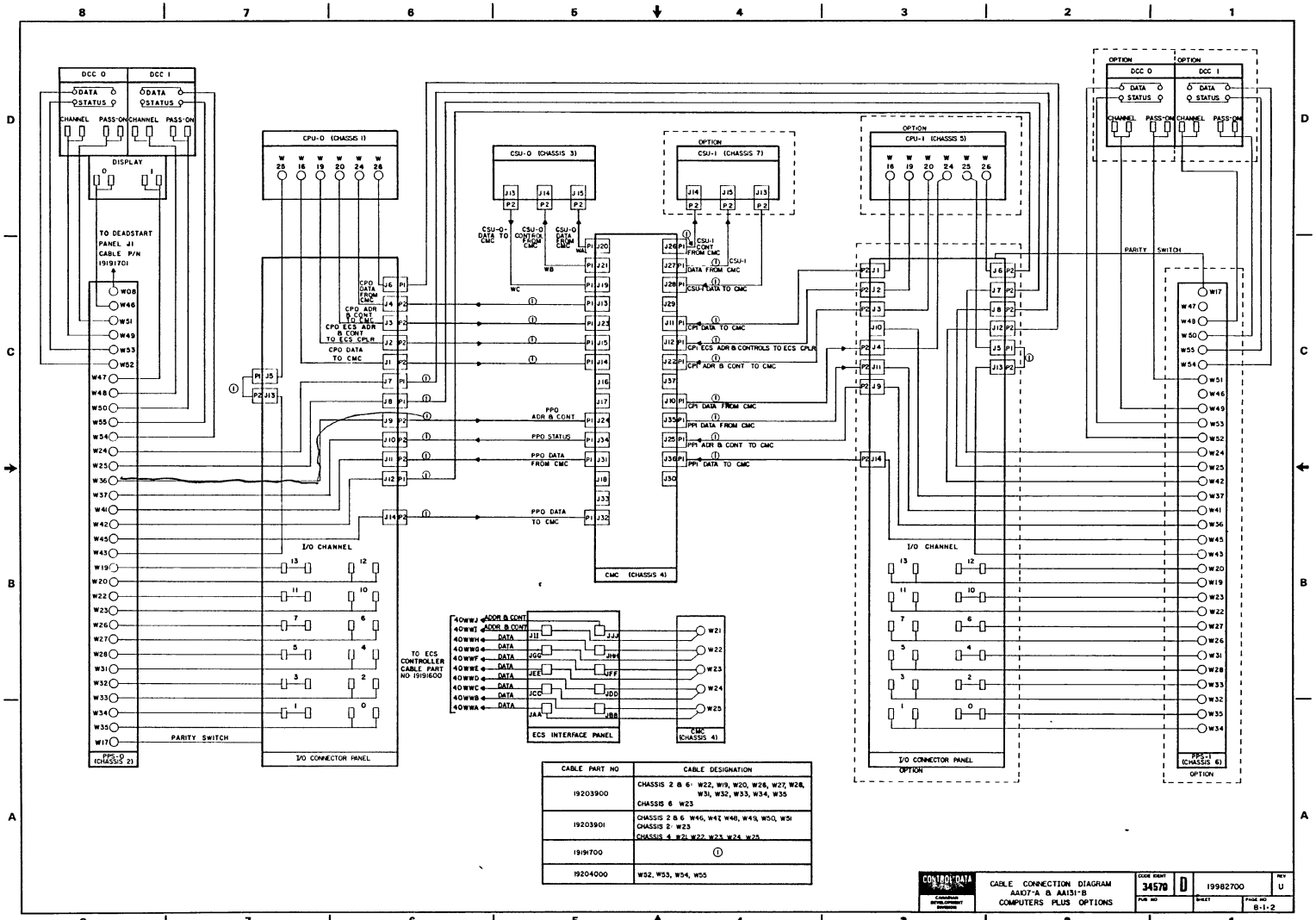


Figure 4-22. CYBER 170 Cable Connection Diagram

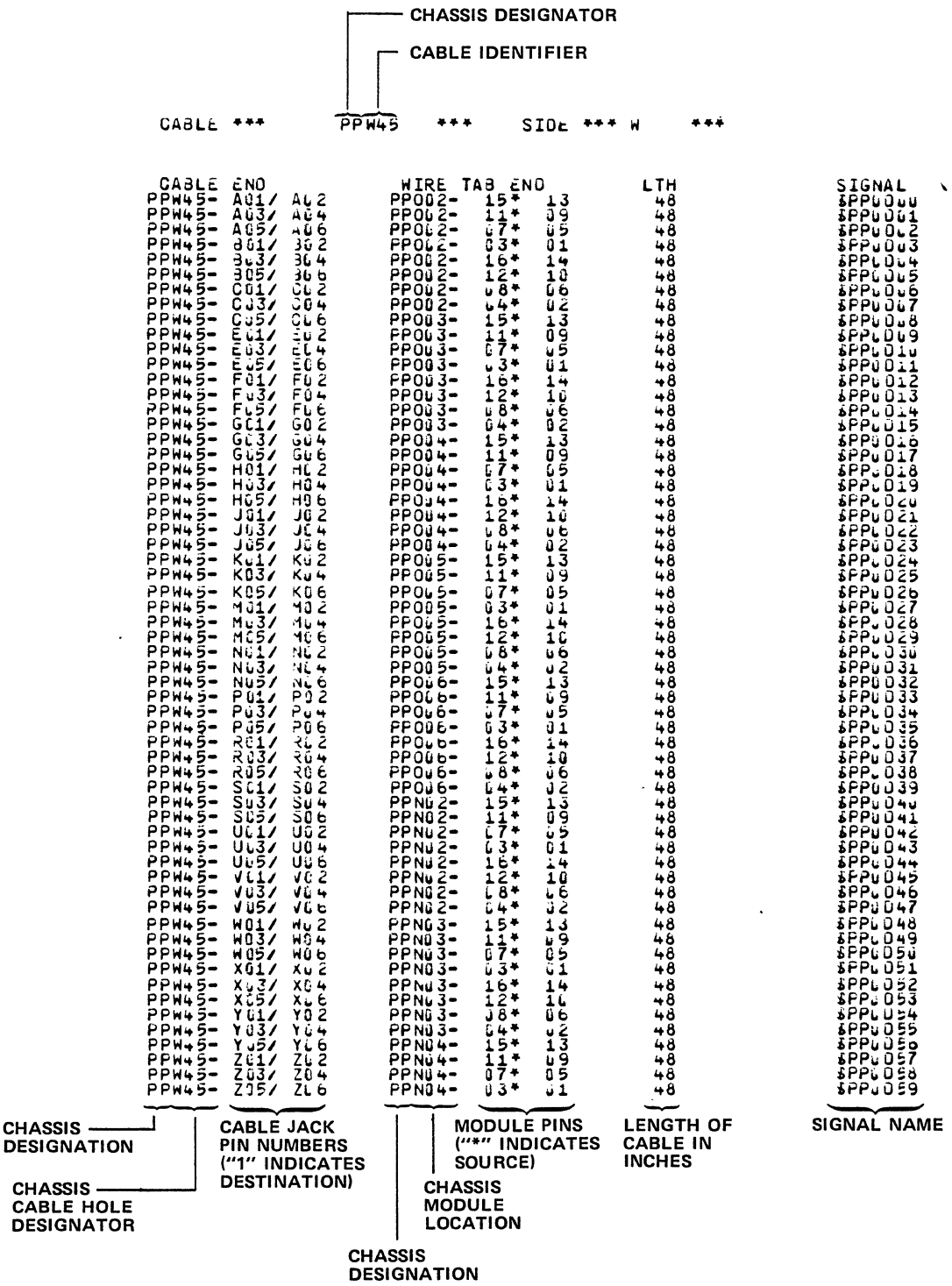


Figure 4-23. Cable Wire List - W45

If we go to the cable list for J32 in the CMC chassis, we should be able to use A01/A02 to find the signal.

Figure 4-24 shows the cable wire list for J32. At the top of the list you will find J32-A01/A02. It is connected to pins 12 and 10 of the module in location 016 through a 24-inch cable. The signal name is $PP0D00, which is what we started with in the PPS chassis.

This activity has given you the ability to read cable wire lists in the CYBER 170 mainframe.

CABLE *** CMJ32 *** SIDE *** JACK ***

CABLE END	WIRE TAB END	LTH	SIGNAL
CMJ32- A01/ AD 2	CMO16- 12* 10	24	$PPU D00
CMJ32- A03/ AL4	CMO16- 16* 14	24	$PPU D01
CMJ32- A05/ AD6	CMO16- 04* 02	24	$PPU D02
CMJ32- B01/ BD 2	CMO16- 08* 06	24	$PPU D03
CMJ32- B03/ BD4	CMO16- 15* 13	24	$PPU D04
CMJ32- B05/ BD6	CMO16- 07* 05	24	$PPU D05
CMJ32- C01/ CD 2	CMO16- 11* 09	24	$PPU D06
CMJ32- C03/ CD4	CMO16- 03* 01	24	$PPU D07
CMJ32- C05/ CD6	CMO15- 12* 10	24	$PPU D08
CMJ32- E01/ ED 2	CMO15- 16* 14	24	$PPU D09
CMJ32- E03/ ED4	CMO15- 04* 02	24	$PPU D10
CMJ32- E05/ ED6	CMO15- 08* 06	24	$PPU D11
CMJ32- F01/ FD 2	CMO15- 15* 13	24	$PPU D12
CMJ32- F03/ FD4	CMO15- 07* 05	24	$PPU D13
CMJ32- F05/ FD6	CMO15- 11* 09	24	$PPU D14
CMJ32- G01/ GD 2	CMO15- 03* 01	24	$PPU D15
CMJ32- G03/ GD4	CMO14- 12* 10	24	$PPU D16
CMJ32- G05/ GD6	CMO14- 16* 14	24	$PPU D17
CMJ32- H01/ HD 2	CMO14- 04* 02	24	$PPU D18
CMJ32- H03/ HD4	CMO14- 08* 06	24	$PPU D19
CMJ32- H05/ HD6	CMO14- 15* 13	24	$PPU D20
CMJ32- J01/ JD 2	CMO14- 07* 05	24	$PPU D21
CMJ32- J03/ JD4	CMO14- 11* 09	24	$PPU D22
CMJ32- J05/ JD6	CMO14- 03* 01	24	$PPU D23
CMJ32- K01/ KD 2	CMO13- 12* 10	24	$PPU D24
CMJ32- K03/ KD4	CMO13- 16* 14	24	$PPU D25
CMJ32- K05/ KD6	CMO13- 04* 02	24	$PPU D26
CMJ32- M01/ MD 2	CMO13- 08* 06	24	$PPU D27
CMJ32- M03/ MD4	CMO13- 15* 13	24	$PPU D28
CMJ32- M05/ MD6	CMO13- 07* 05	24	$PPU D29
CMJ32- N01/ ND 2	CMO13- 11* 09	24	$PPU D30
CMJ32- N03/ ND4	CMO13- 03* 01	24	$PPU D31
CMJ32- N05/ ND6	CMN16- 12* 10	24	$PPU D32
CMJ32- P01/ PD 2	CMN16- 16* 14	24	$PPU D33
CMJ32- P03/ PD4	CMN16- 04* 02	24	$PPU D34
CMJ32- P05/ PD6	CMN16- 08* 06	24	$PPU D35
CMJ32- R01/ RD 2	CMN16- 15* 13	24	$PPU D36
CMJ32- R03/ RD4	CMN16- 07* 05	24	$PPU D37
CMJ32- R05/ RD6	CMN16- 11* 09	24	$PPU D38
CMJ32- S01/ SD 2	CMN16- 03* 01	24	$PPU D39
CMJ32- S03/ SD4	CMN15- 12* 10	24	$PPU D40
CMJ32- S05/ SD6	CMN15- 16* 14	24	$PPU D41
CMJ32- U01/ UD 2	CMN15- 04* 02	24	$PPU D42
CMJ32- U03/ UD4	CMN15- 08* 06	24	$PPU D43
CMJ32- U05/ UD6	CMN15- 15* 13	24	$PPU D44
CMJ32- V01/ VD 2	CMN15- 07* 05	24	$PPU D45
CMJ32- V03/ VD4	CMN15- 11* 09	24	$PPU D46
CMJ32- V05/ VD6	CMN15- 03* 01	24	$PPU D47
CMJ32- W01/ WD 2	CMN14- 12* 10	24	$PPU D48
CMJ32- W03/ WD4	CMN14- 16* 14	24	$PPU D49
CMJ32- W05/ WD6	CMN14- 04* 02	24	$PPU D50
CMJ32- X01/ XD 2	CMN14- 08* 06	24	$PPU D51
CMJ32- X03/ XD4	CMN14- 15* 13	24	$PPU D52
CMJ32- X05/ XD6	CMN14- 07* 05	24	$PPU D53
CMJ32- Y01/ YD 2	CMN14- 11* 09	24	$PPU D54
CMJ32- Y03/ YD4	CMN14- 03* 01	24	$PPU D55
CMJ32- Y05/ YD6	CMN13- 12* 10	24	$PPU D56
CMJ32- Z01/ ZD 2	CMN13- 16* 14	24	$PPU D57
CMJ32- Z03/ ZD4	CMN13- 04* 02	24	$PPU D58
CMJ32- Z05/ ZD6	CMN13- 08* 06	24	$PPU D59

Figure 4-24. Cable Wire List - J32

POST TEST

When you have completed the learning activities assigned for Module 4, sign on to the PLATO terminal and take the Module 4 test. Depending on the results of the test you will be told either to review some of the previous activities, or be awarded mastery of the course.

APPENDIXES

APPENDIX A
USING INDIVIDUALIZED INSTRUCTION

If this is your first experience with Individualized Instruction, you probably have a few questions. The information that follows will help you understand the nature of Individualized Instruction.

WHAT IS INDIVIDUALIZED INSTRUCTION?

Individualized Instruction is a teaching method that is oriented toward the individual rather than the group. Individualized instruction--

- Determines what skills you possess that pertain to the topic of instruction.
- Determines what skills you must acquire.
- Allows you to acquire these skills at your own pace by studying a variety of learning activities.

Individualized Instruction is structured around a student manual that guides you through the course and is also a learning resource. The student manual is divided into modules.

Each module contains information that will help you meet the objectives of that module. The information within the module is presented in learning activities.

MAY I WORK WITH OTHER STUDENTS?

Yes, if two or more of you are taking the course at the same time, it may be beneficial for you to do some of the learning activities together. Whether you work alone or with others depends on your needs.

HOW DO I PROCEED THROUGH THE COURSE?

You begin the course by signing on to the PLATO terminal. See appendix B for detailed instructions for signing on. You may want to take the pretest or you may ask for a full assignment that teaches all of the objectives of the first module. If you take the pretest, PLATO learning management (PLM) will evaluate the results of the test and assign the learning activities that are keyed to the objectives you did not master. Then, study the

assigned learning activities and retake the test. If you are successful, proceed to the next module and repeat the process until course completion. If not, study the assigned learning activities and retake the test until you master all the module objectives.

See figure A-1 for a flowchart illustrating your progress through the course.

HOW DO MODULES, COURSES, AND CURRICULA RELATE TO EACH OTHER?

The structure of the Engineering Services Training Program has three parts:

- Module. A module is made up of learning activities. It contains objectives and test questions. A module teaches specific training tasks. For example, a module could cover electrical/mechanical adjustments.

- Course. A course is made up of modules. A course covers a single subject, for example, a course on the oscilloscope or magnetic tape unit.

- Curriculum. A curriculum is made up of courses. It covers a broad area of knowledge, for example, an entire subsystem. A curriculum may contain courses that range in complexity from introductory to advanced.

WHAT KIND OF RESOURCES ARE USED IN INDIVIDUALIZED INSTRUCTION?

Individualized learning activities use the following resources and combinations of those resources to present information.

- Text Reading. This resource presents information via the student manual and provides simplified explanations, drawings, and examples.

- Reference Reading. This resource directs you to read designated pages in a specified reference manual.

- Exercises. This resource presents information via the student manual. It uses a question/answer presentation. An exercise may be used to present new material or it may determine your comprehension of previously presented material.

- Programmed Text. This resource is a student manual text reading that presents information and asks for immediate feedback to determine your comprehension.

- Laboratory. This resource gives you actual hands-on experience with computer equipment.

- PLATO Assisted Learning. This resource presents information via the PLATO terminal.

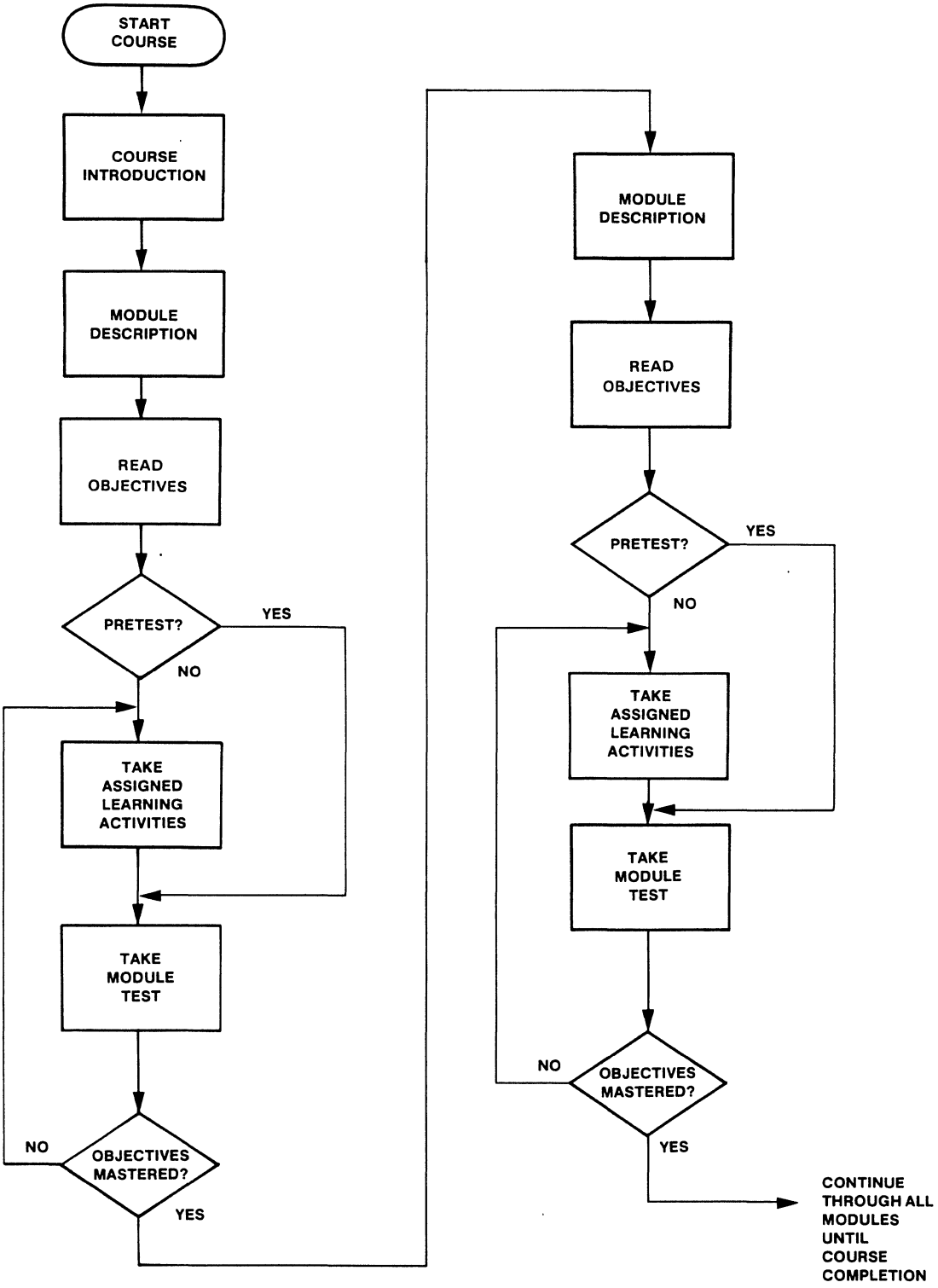


Figure A-1. Student Progress

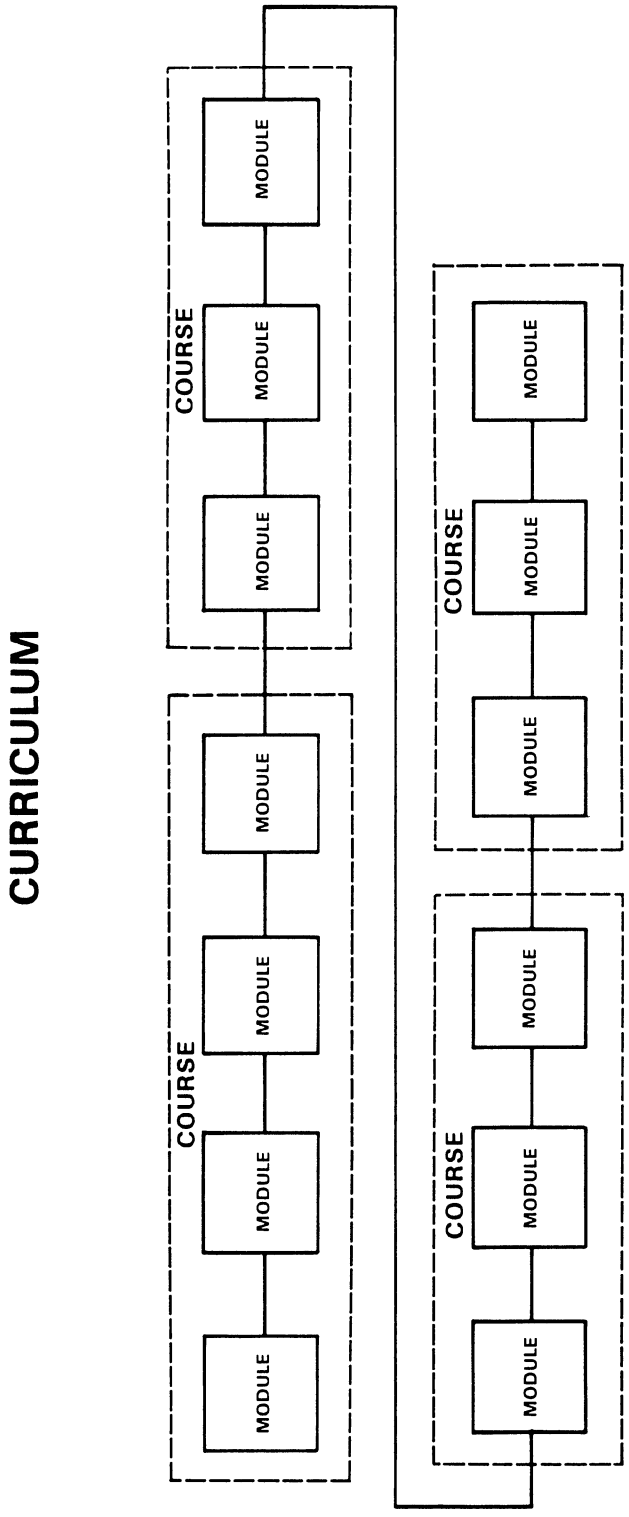


Figure A-2. Program Structure

- Audiotape. This resource presents an audio message via an audiotape machine.

- Microfiche. This resource uses a microfiche viewer and microfiche film to illustrate information.

- Videotape. This resource uses a videotape playback unit and videotape to present information.

You may proceed from one learning activity to another at your own pace. The learning activites are not long, but it is important that you take the time to understand the material before you go on to the next activity.

Each learning activity is coded with a number and a letter. The number stands for the module and the letter represents the order in which the learning activity is presented. The first learning activity of the first module is Learning Activity 1-A. The second activity is 1-B, and so on.

HOW DO I TAKE A TEST?

All testing is managed by PLATO Learning Management (PLM). PLM performs three important functions:

- Administers all tests.

- Assigns learning activities based on the results of the tests.

- Retains your student records for all courses you take within a curriculum.

PLM has two modes of testing, on-line and off-line. On-line testing requires that you sign onto a PLATO terminal to take the test. When you complete the test, PLM will assign learning activities based on the results of your test.

On-line testing is preferred because it saves time and enables you to proceed through your training without any delays.

Off-line testing is the more traditional method. Your administrator will give you a copy of the test and an answer sheet. Do not write on the test; record all your answers on the answer sheet. Return your test to the administrator, who will grade it and enter the results into the PLM system.

WHAT IS THE INDIVIDUALIZED INSTRUCTION TESTING PHILOSOPHY?

A test is a device that determines whether you have met the objectives of the course (module). It determines if you have acquired the skills that the course is designed to teach.

The number of times you take a test or your score on the test is not as important as the information you gain from the test results. The results tell you what areas you need to study.

Do not be upset if you need to take a test more than once. It is not your scores that count, it is your ability to perform your job that is important to you, Engineering Services' customers, and Control Data.

WHO ARE THE PERSONNEL INVOLVED IN INDIVIDUALIZED INSTRUCTION?

Regional Education Manager (REM)

The REM manages the training program for the region/ country. He coordinates and administrates training activities to ensure that training needs are identified and fulfilled.

Regional Training Coordinator (RTC)

The RTC works with the education center manager to provide assistance as required; for example, he orders training materials, processes enrollments/confirmations, etc.

Education Center Manager (ECM)

The ECM administrates and coordinates training activities to ensure training delivery. For example, he provides a technical training advisor and identifies training materials requirements for the RTC. This individual may be a resource center manager, regional education manager, skill center manager or education center manager.

Education Training Coordinator (ETC)

The ETC manages the PLATO learning management (PLM) system. He provides the student with a student sign on and PLM entries, and he works with the education center manager to solve PLM related problems.

Technical Advisor (TA)

The TA deals directly with the student. He monitors activities and provides guidance and assistance as required. A TA may be an engineer-in-charge, regional technical support instructor or a customer engineer with technical expertise.

Subject Matter Expert (SME)

The SME provides technical assistance for training problems that cannot be resolved by the technical advisor.

Learning Center Administrator (LCA)

The LCA works directly with the student to ensure smooth progression through the course.

APPENDIX B
PLATO SIGN-ON PROCEDURE

In order to begin the course you must first sign on to the PLATO system. Depending on where your terminal is located, you may first have to dial up the PLATO computer in order to establish communication between the computer and your terminal. If your terminal is on a direct connection, this is not necessary, and steps 2 and 3 can be skipped.

1. Turn power on.

*2. Dial the number of the PLATO system using the data phone. When the system answers, you will hear a tone. The next step must be performed within three seconds after you hear the tone.

*3. Lift exclusion button (usually located on the telephone cradle). Place the receiver on the table or in front of the cradle. Do not hang up.

NOTE

Some data phones require that you lift the exclusion button to dial, and hang up when the tone is heard.

4. Press the STOP key on the PLATO terminal keyboard.

5. Press the NEXT key on the PLATO keyboard. This causes the "Welcome to PLATO" page to be displayed (figure B-1).

6. Enter your name exactly as you are registered in this course. Normally this will be your last name, followed by a space, and your first initial, with no capital letters (for example, smith j, as shown in figure B-2).

   If you make a mistake, you can erase it by pressing the ERASE key on the right side of the keyboard.

7. Press the NEXT key. You will then be asked to enter the name of your PLATO group . Enter the name of the PLATO group in which you are registered. Once again, the exact spelling is required.

*Dial-up system only.

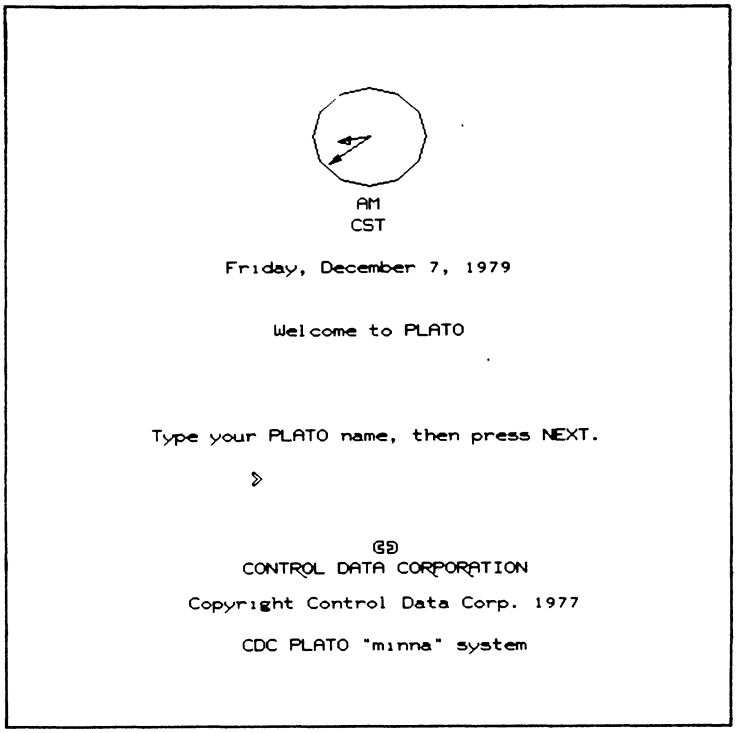


Figure B-1. Welcome to PLATO

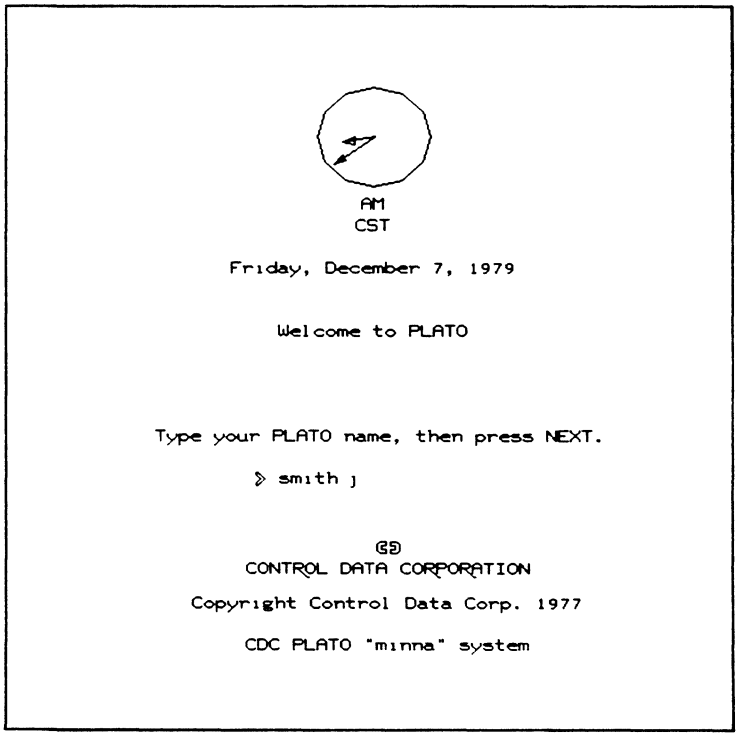


Figure B-2. Repeat

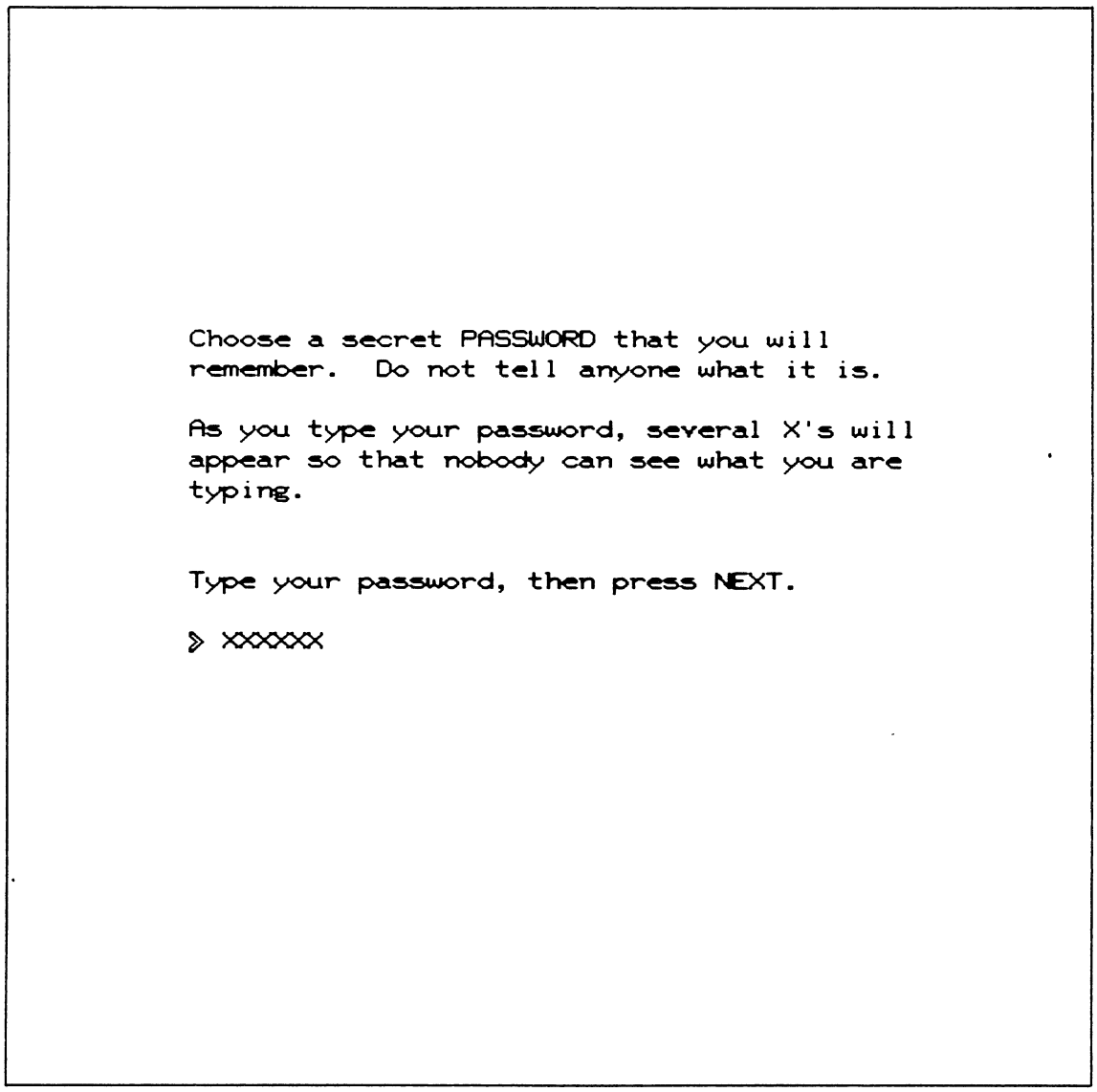


Figure B-3. Password

8. Hold down the SHIFT key and press the STOP key. You will then be asked to enter your password (figure B-3). Your password can be anything you choose, but it must be something that you can easily remember, such as a name, phone number, employee number, etc. Do not forget the password you have selected. It will become your key for gaining access to your lessons.

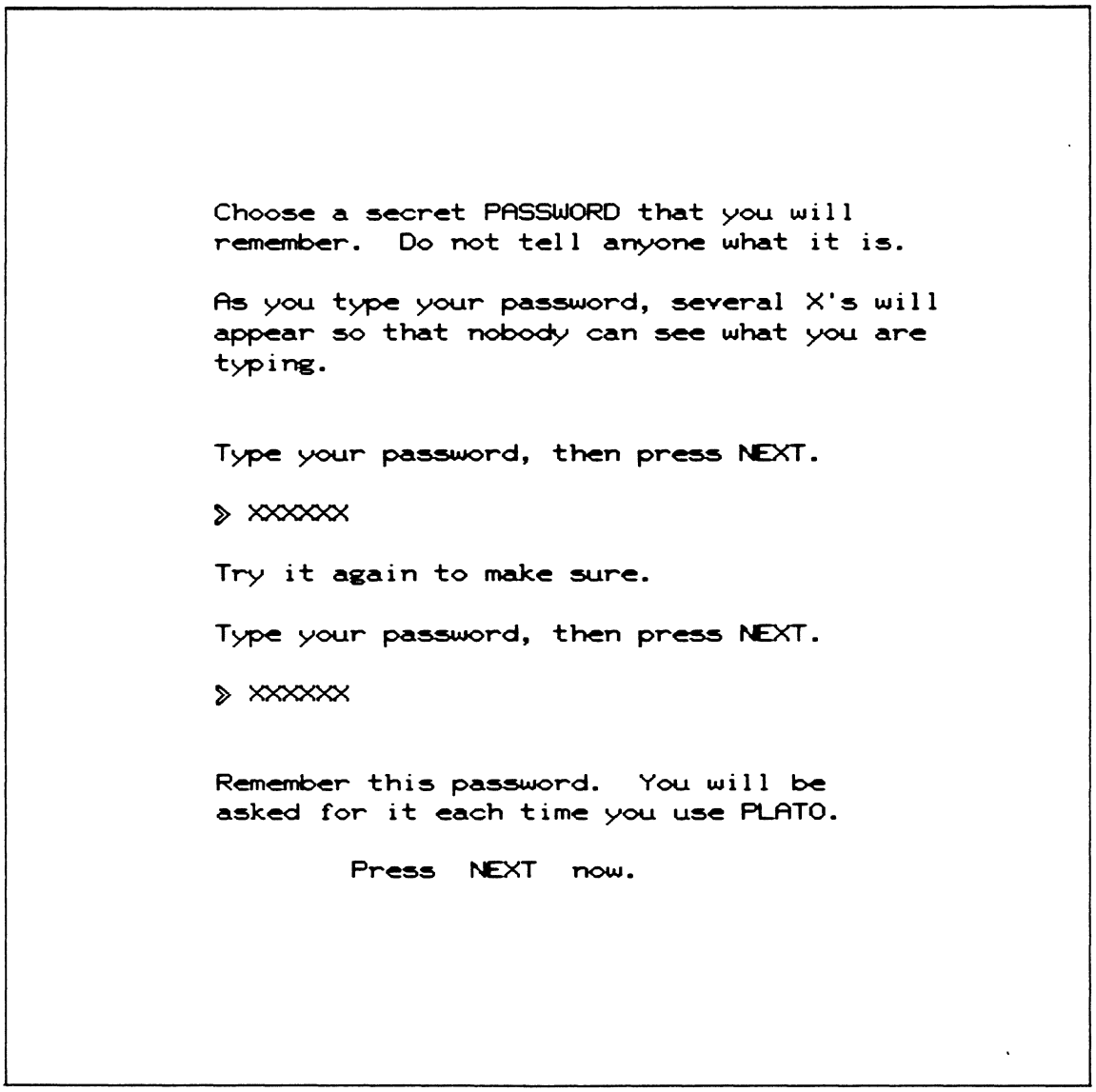


Figure B-4. Password Repeat

9. Press the NEXT key. If this is the first time you have signed onto this course, you will be asked to enter your password again (figure B-4). Enter it again, just as you did before. From this point on you will be required to enter your password only once when you sign on.

10. Press NEXT. You are now signed on to the system.

APPENDIX C
USING MICROFICHE

INTRODUCTION

This appendix provides the basics of selecting, loading, and viewing microfiche on a Micron 780 Microfiche Desk Reader or a similar reader. (See the Microfiche Handbook, available from Information Services, STP109, for more information.)

The portable microfiche desk reader may also be used since it has the same capabilities as the Micron 780.

Consult the operator's manual for specific information on the readers.

SELECTION

Select the proper microfiche by consulting the microfiche header, which contains the title of the contents and the microfiche reference number (figure C-1).

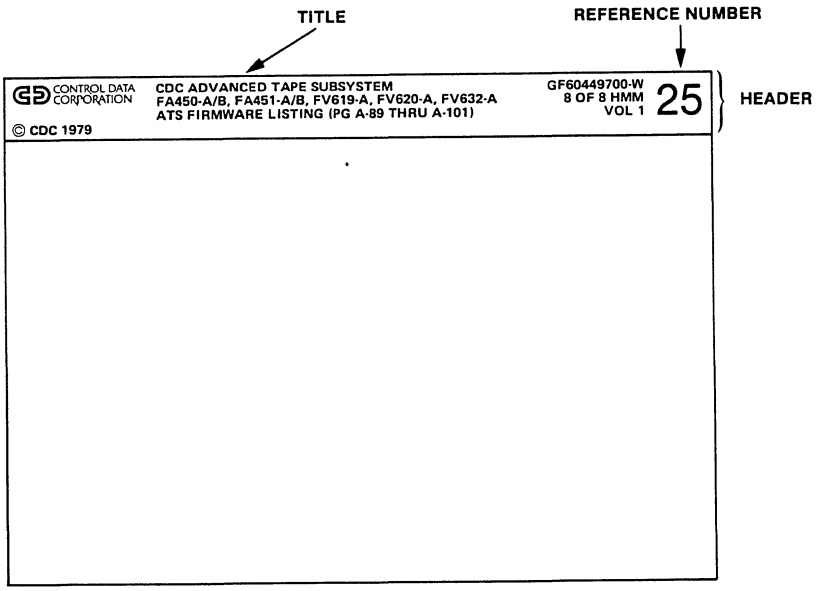


Figure C-1. Microfiche

LOADING

To load the Micron 780 Desk Reader or a similar desk reader, perform the following procedure (figure C-2).

1. Turn on the microfiche desk reader by pushing in on the side of the LOW-OFF-HIGH switch that indicates a low light intensity setting.

2. Pull the carriage assembly toward you until the glass covers flip up.

3. Hold the microfiche by the header with the printed information facing up (figure C-3).

4. Position the microfiche toward the upper right corner of either glass.

5. Push the carriage assembly back and position it so that a full picture with a index grid coordinate number is visible on the screen.

6. Select the proper index grid. Each microfiche desk reader is equipped with two index grids, a 24X index grid for 24X microfiche and a 42X index grid for 42X microfiche; most documentation is on 24X microfiche (figure C-4).

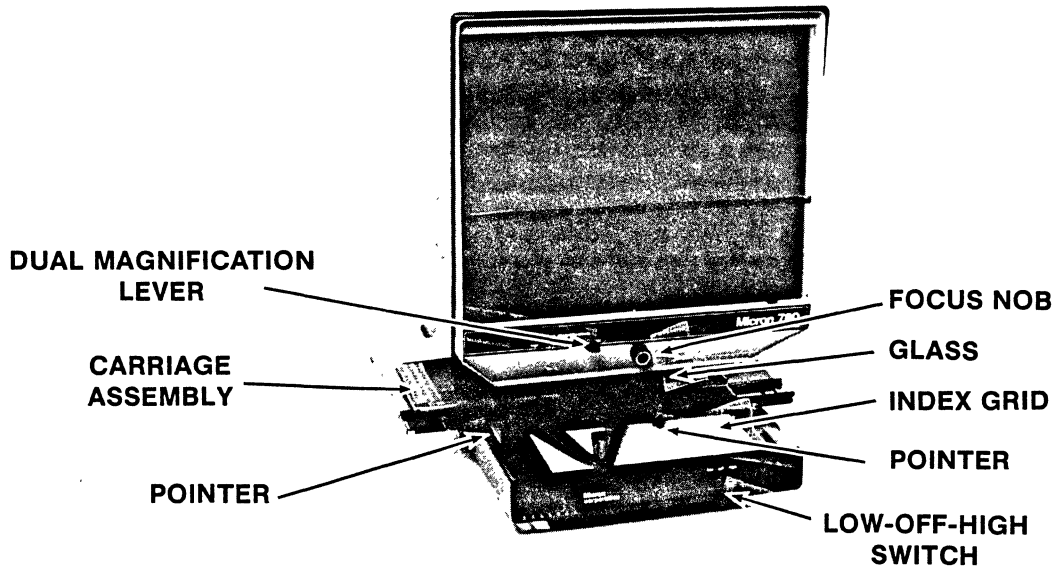


Figure C-2. Microfiche Desk Reader

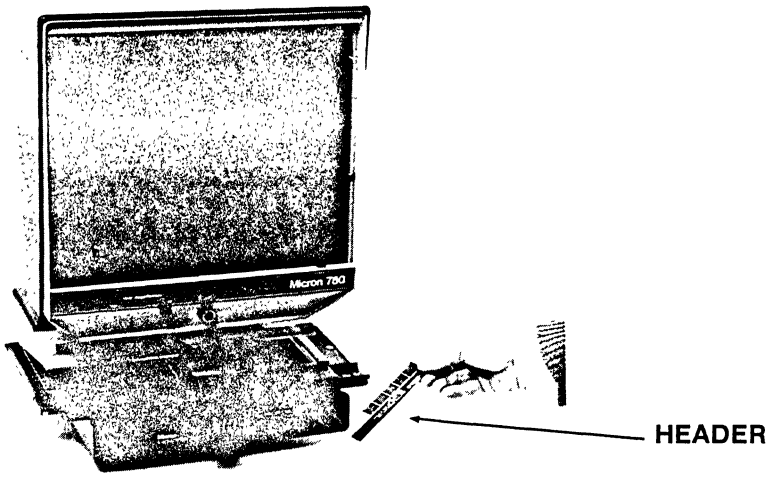


Figure C-3. Inserting Microfiche into Desk Reader

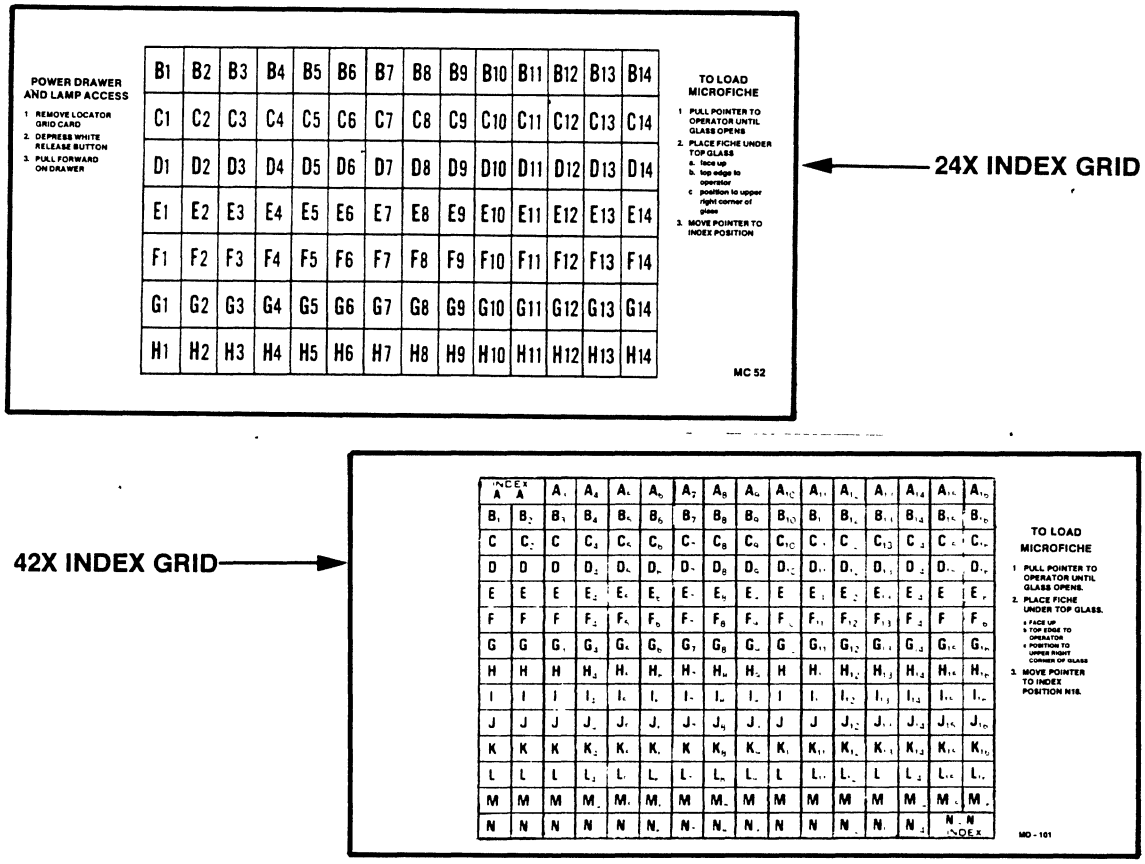


Figure C-4. 24X and 42X Index Grids

a. The 24X microfiche has a 3/8-inch header, and the 24X index grid is divided into 14 horizontal boxes.
b. The 42X microfiche has a 1/2-inch header, and the 42X index grid is divided into 16 horizontal boxes.

7. Place the proper index grid so that the carriage pointer is centered over the index grid coordinate number that appears on the screen.

VIEWING

When viewing a logic diagram with a index grid coordinate number of B1, position the carriage pointer between B1 and B2 on the index grid. Adjust the carriage to obtain a full screen picture. Student manuals and audiotapes may call the coordinates B1/B2 on the index grid. B1/B2 indicates that the carriage pointer should be positioned between B1 and B2 on the index grid (figure C-5).

Other pages of technical manual can be viewed by placing the carriage pointer in the center of the index grid coordinate number (figure C-6).

Screen Quadrants

The desk reader screen is divided into four quadrants to reference any area of the screen (figure C-7). It has a transparent horizontal yellow line for the horizontal axis; you may need to add the vertical axis. Transparent map tape, clear tape, or grease pencil work well as the vertical axis.

Magnification

A dual lense microfiche reader, such as the Micron 780, can magnify any area of a 24X microfiche by using the high (42X) lense in the following procedure.

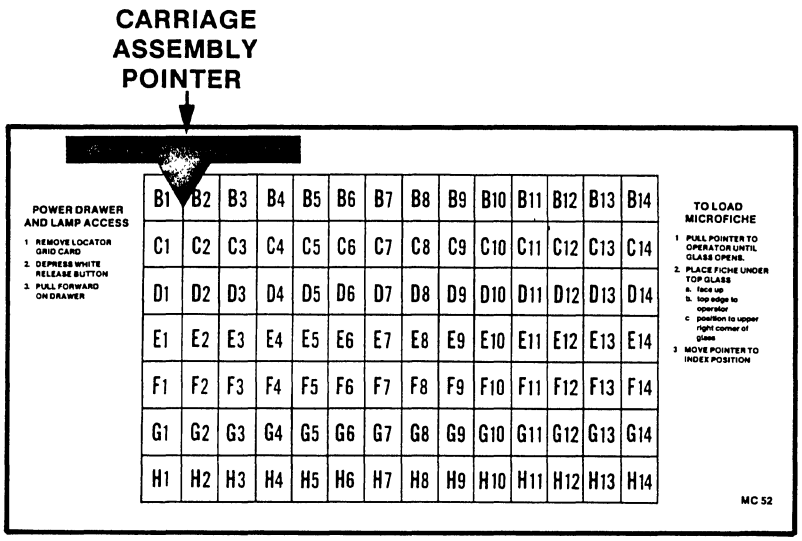


Figure C-5. Carriage Assembly Pointer Position for Technical Manuals

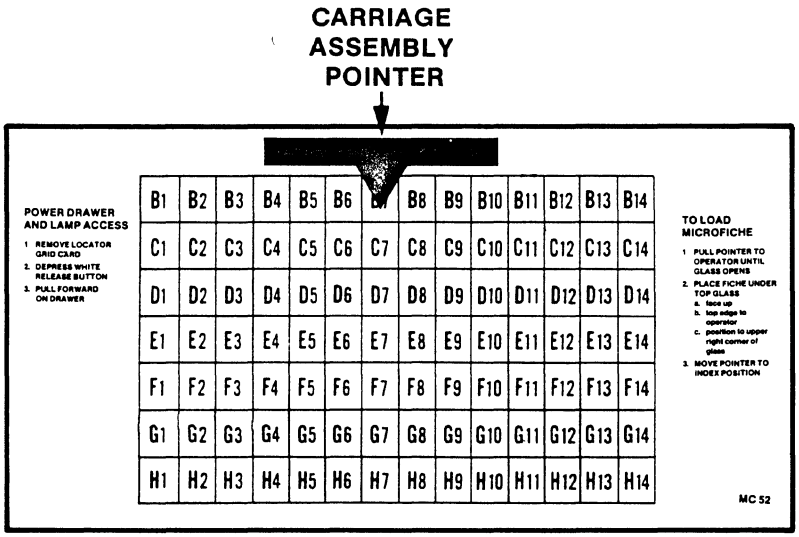


Figure C-6. Carriage Assembly Pointer Position for Logic Diagrams

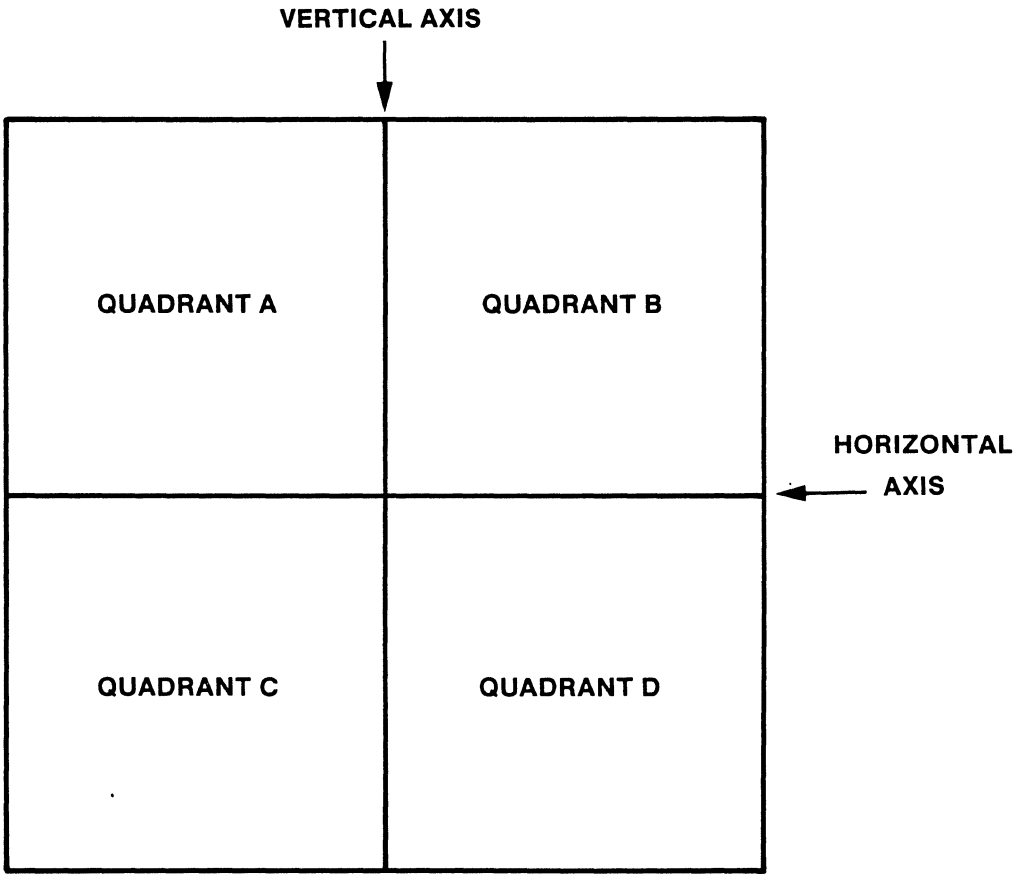


Figure C-7. Screen Quandrants

1. Position the area that you wish to magnify in the center of the screen using the carriage assembly (see figure C-2 for the location of the DUAL MAGNIFICATION lever).

2. Move the DUAL MAGNIFICATION lever to HIGH.

3. Return the magnification lever to LOW before moving on to another frame.

Light Intensity

The microfiche desk reader can deliver high or low light intensity. The Light Intensity switch is part of the LOW-OFF-HIGH switch.

The following suggestions may help reduce eye strain when using a microfiche desk reader for a long time.

- Do not watch the screen while moving to a different frame.
- Use low intensity light for low magnification and high intensity light for high magnification.
- Be sure the image on the screen is focused sharply (see figure C-2 for the location of the focus nob).
- Tilt the projector forward or backward.
- Vary the intensity of the room lighting.

Be sure to turn the viewer off whenever you are not using it. Extended exposure to light will fade the microfiche.

APPENDIX D
DIAGRAMS

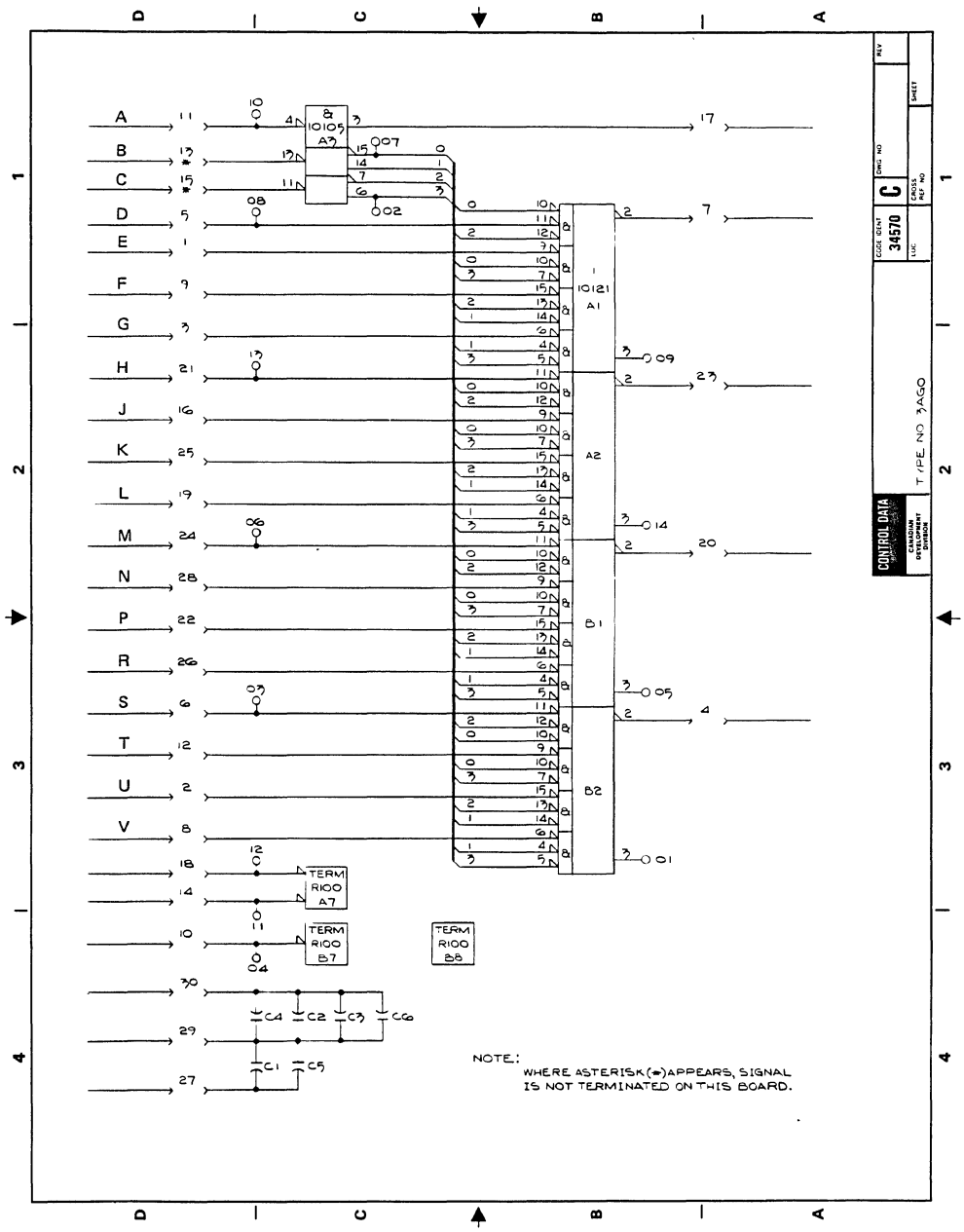


Figure D-1. 3AG0 Module Diagram

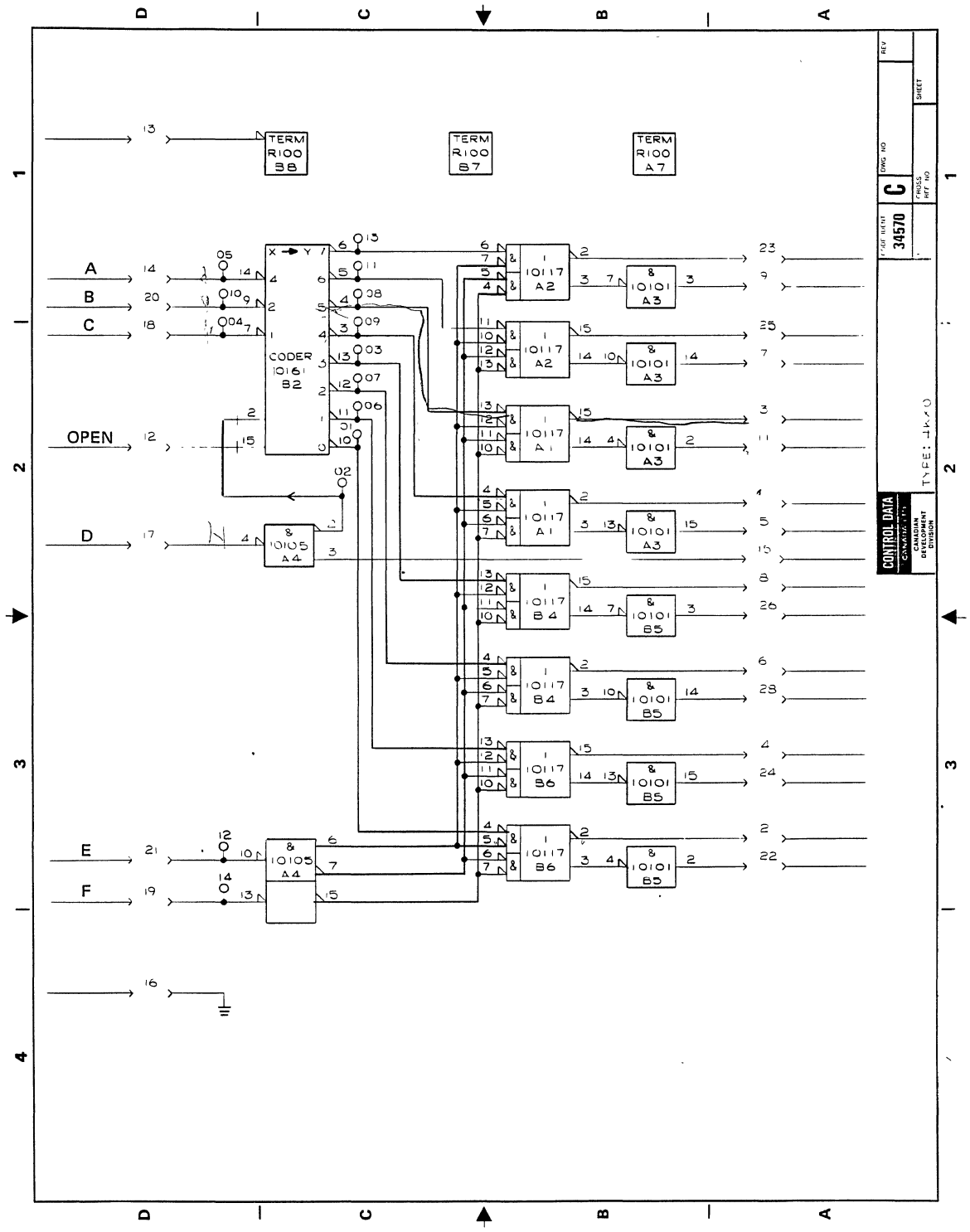


Figure D-2. 4KX0 Module Diagram

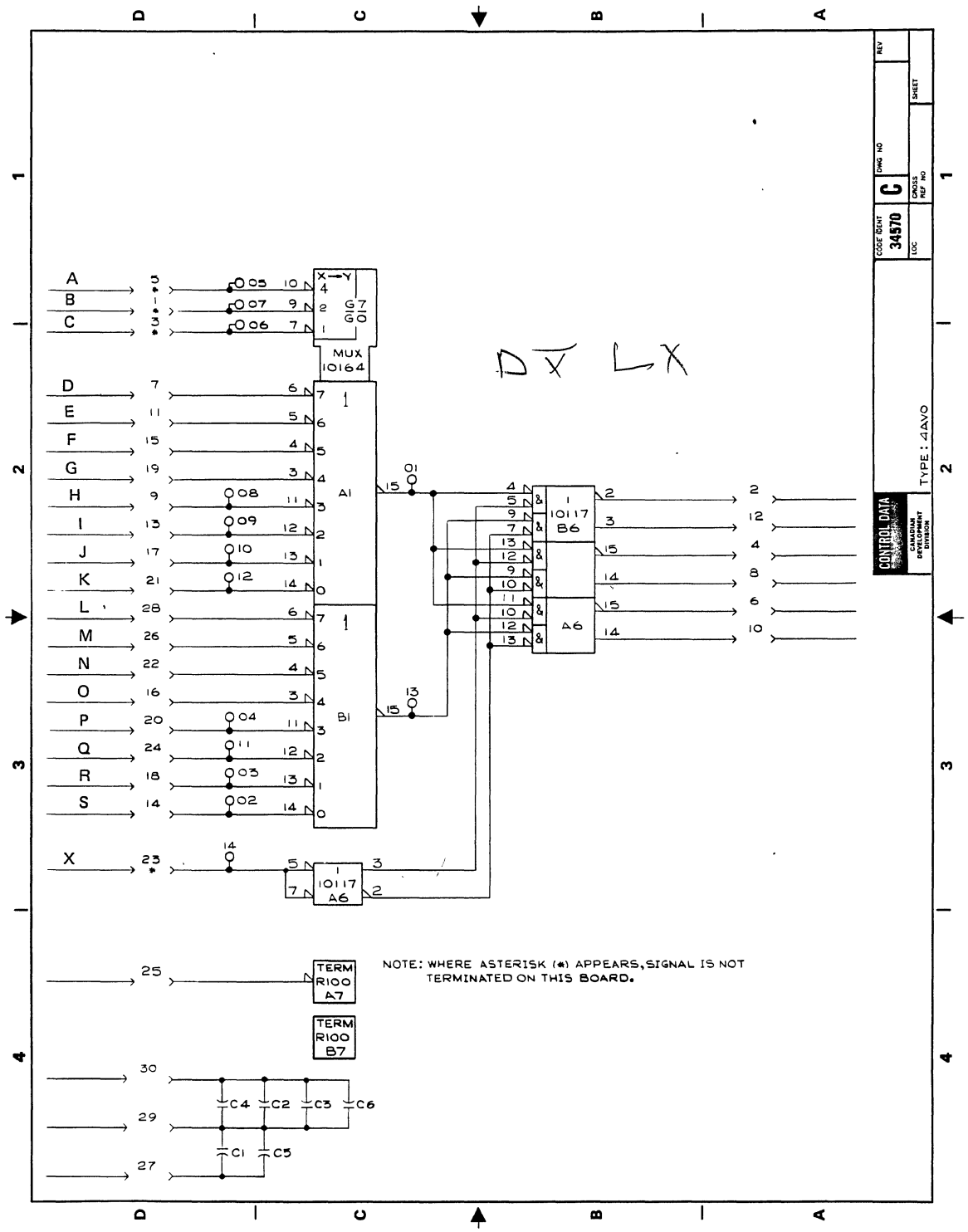


Figure D-3. 4AV0 Module Diagram

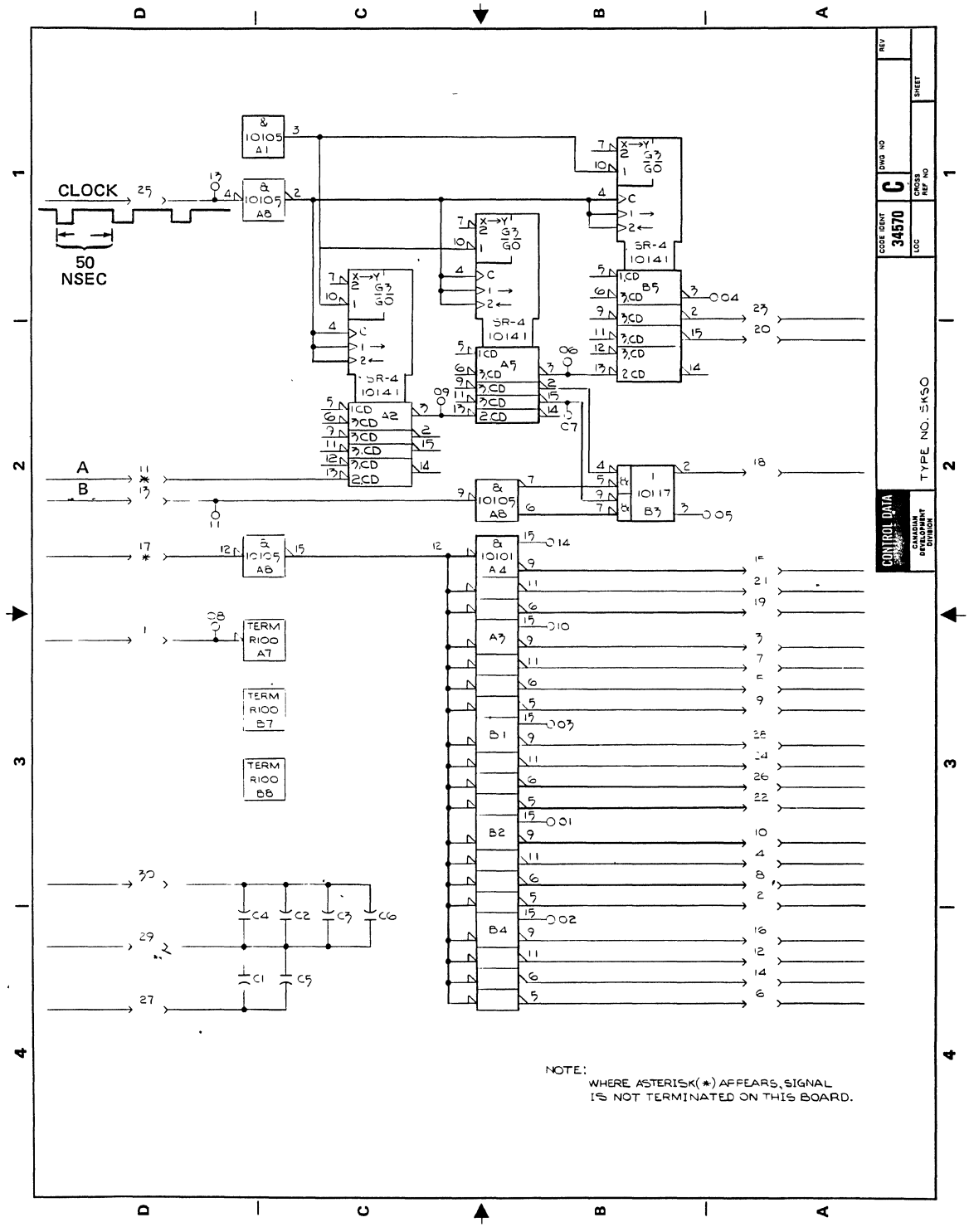


Figure D-4. 5KS0 Module Diagram

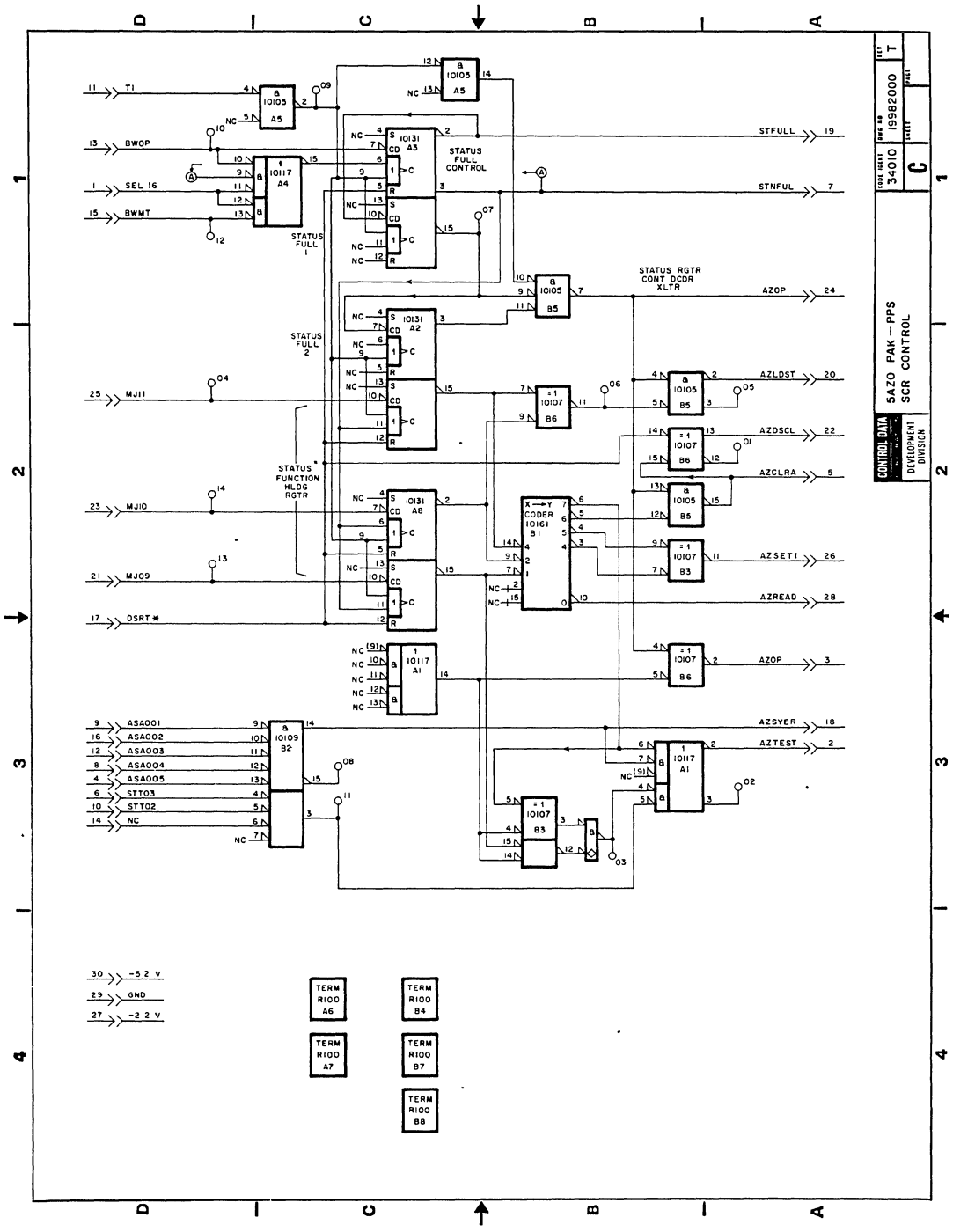


Figure D-5. 5AZ Module Diagram

COMMENT SHEET

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PUBLICATION NO. 75445355 REVISION B Prod. No. R0401

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