Equipment Diagrams

CONTROL DATA 8092
TELEPROGRAMMER

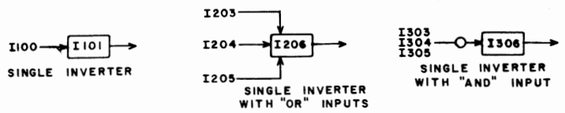
IDP 368 109 01

RECORD OF REVISIONS

REVISION NUMBER	NOTES
368 109 01	(4-15-65) Includes ECO's 1163, 1198, 1268, 1334, 1354, 1402, 1403, 1411, 1431, 1470, 1505, and 1585.
368 109 00b	(8-18-66) INCLUDES ECO NUMBERS 2041 AND 2085. ENTERED 6 FEB 67 BAP

TABLE OF CONTENTS

SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.



FLIP FLOP (FF) - The flip flop is a storage device with two stable states, designated "1" or Set, and "0" or Clear. It is composed of two inter-connected inverters; the logical symbol (figure A) is a square formed by the combination of the two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper part of the symbol and "0" (or Clear) inputs and outputs are shown with the lower part of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in figure B.

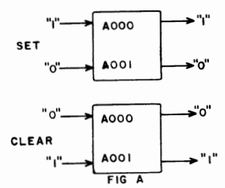


FIG A

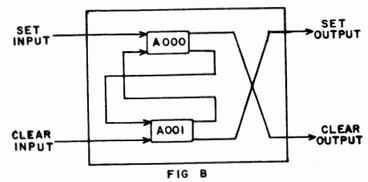
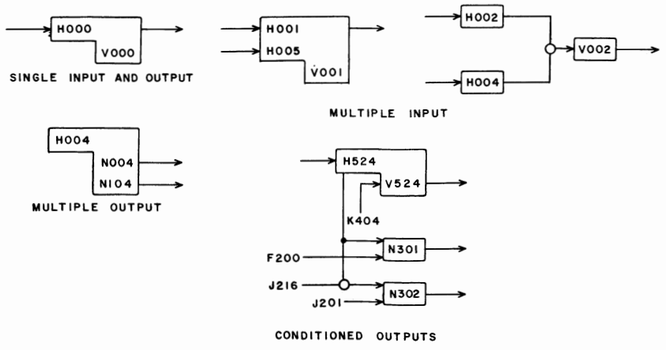


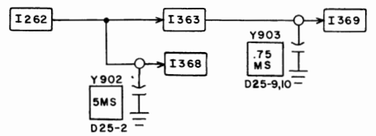
FIG B

CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microsecond). Conventions which apply to control delays are:

1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase; an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.



CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made.



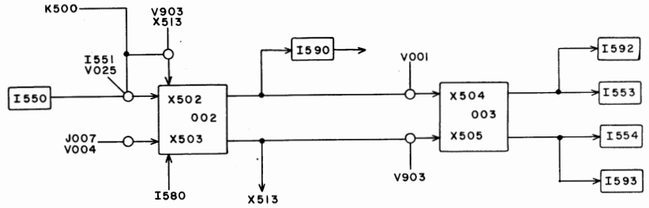
SYMBOLICAL REPRESENTATION OF TYPICAL EQUATIONS

X504 = V001 X503
31 003A: I554: I593:

X505 = V903 X502
31 003C; I592: I553

X502 = V903 X513 X500 + I550 I551 V025 X500
32 002A: X513: X505:

X503 = I580 + J007 V004
32 002C: I590: X504

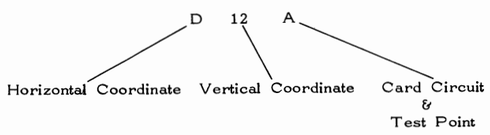


JACK ASSIGNMENTS - The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.

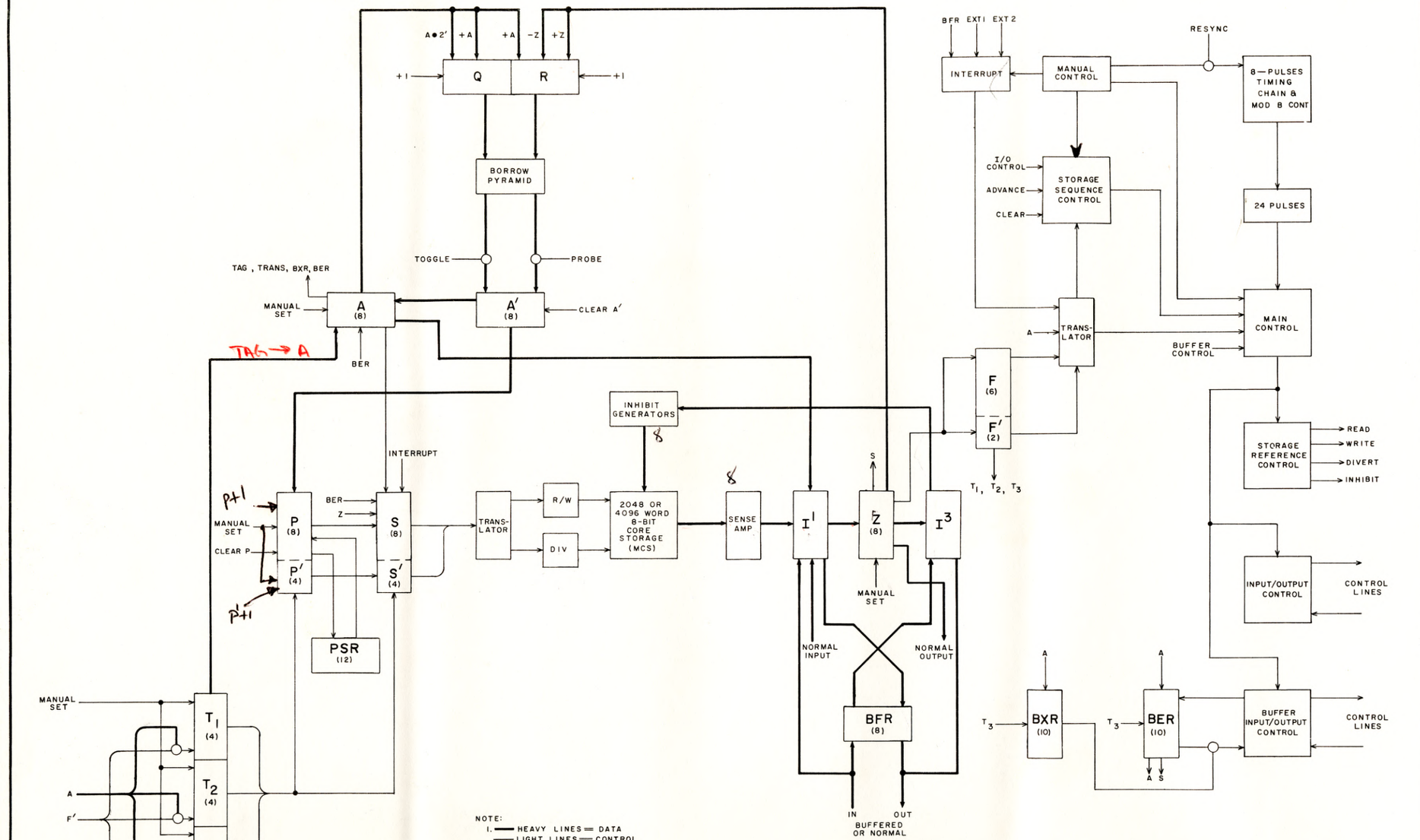
Plug-in cards are designed with from one to four circuits, denoted by the letters A, B, C, or D. The omission of the circuit letter denotes a one circuit card. Two circuit inverter cards are labeled (top circuit, as card is viewed in the chassis connector) and C. Three circuit input (M---) and output (L---) amplifiers are labeled A, B, and C.

Single flip flop cards are not identified by circuit, but it is understood that the even-numbered inverter is associated with circuit A, the odd-numbered inverter with circuit C.

Jack Assignment



KEY TO SYMBOLS USED ON LOGIC DIAGRAMS



REV.	AUTH.	EST DATE	REVISIONS	DRW.	CHK.	APPROVED
A	155	6/1		KH		

DESIGNED , DRAWN , CHECKED , APPROVED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

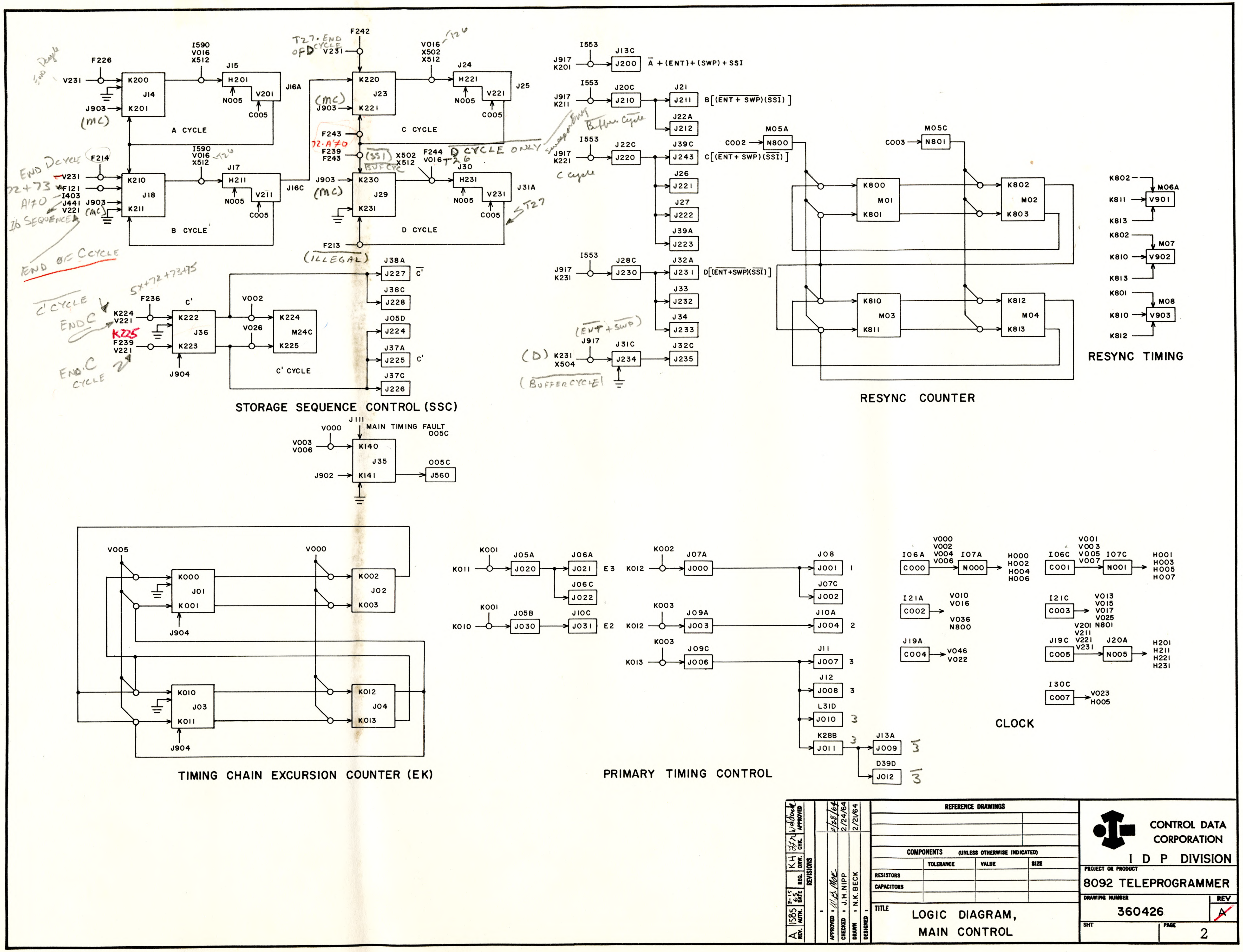
TITLE BLOCK DIAGRAM, TELEPROGRAMMER— MODEL 8092

CONTROL DATA CORPORATION
I D P DIVISION

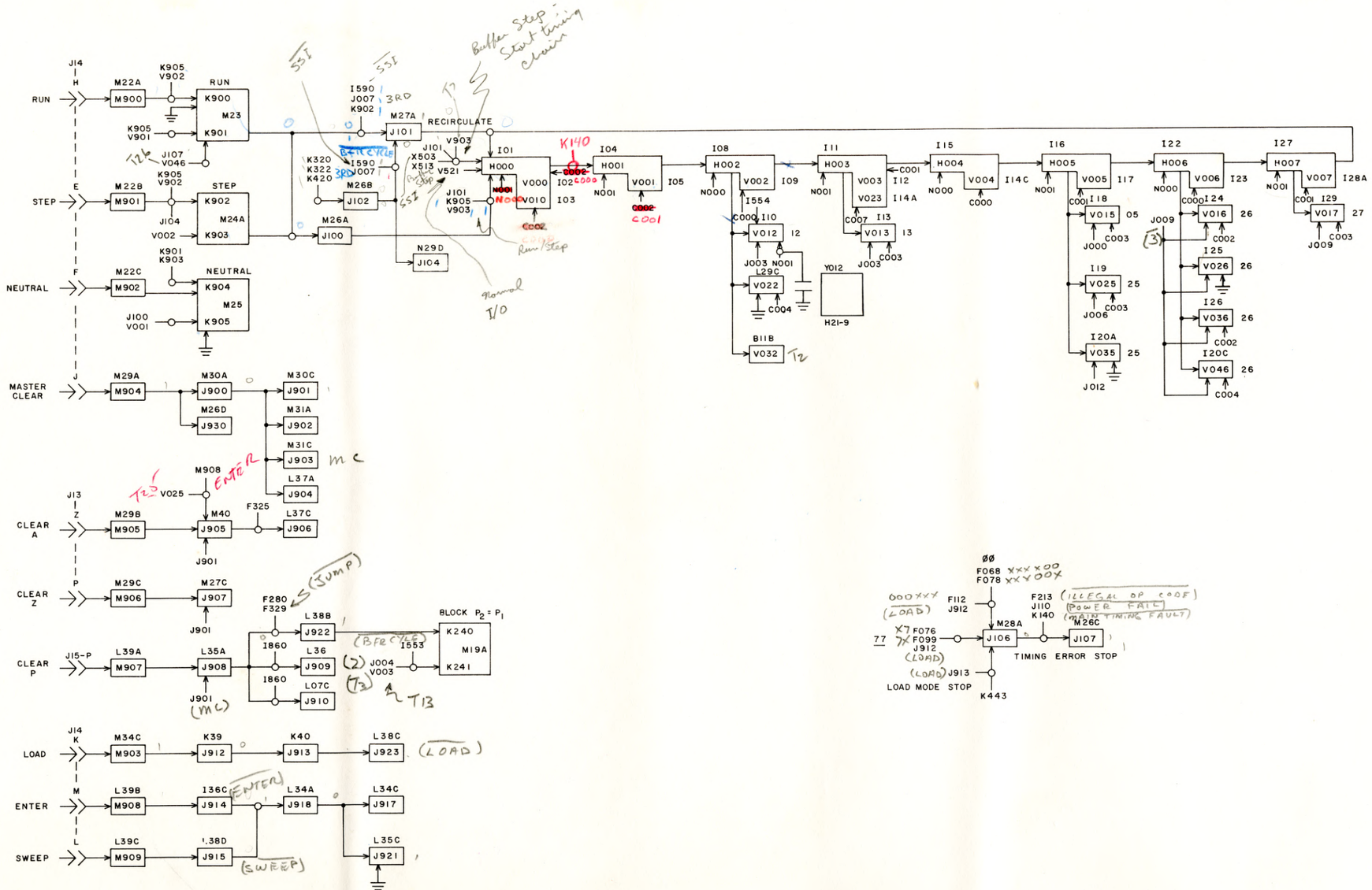
PROJECT OR PRODUCT

DRAWING NUMBER 364038 REV A

PAGE 1



STORAGE SEQUENCE CONTROL (SSC)
A CYCLE
B CYCLE
C CYCLE
D CYCLE
C' CYCLE
MAIN TIMING FAULT
RESYNC COUNTER
RESYNC TIMING
TIMING CHAIN EXCURSION COUNTER (EK)
PRIMARY TIMING CONTROL
CLOCK
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
CONTROL DATA CORPORATION
I D P DIVISION
8092 TELEPROGRAMMER
360426
TITLE LOGIC DIAGRAM, MAIN CONTROL
PAGE 2



REV.	AUTH.	DATE	REVISIONS	CHK.	APPROVED
B	1555	2-5-65			
A					

APPROVED
CHECKED J.H. NIPP 2/24/64
DRAWN N.K. BECK 2/24/64
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
MAIN TIMING

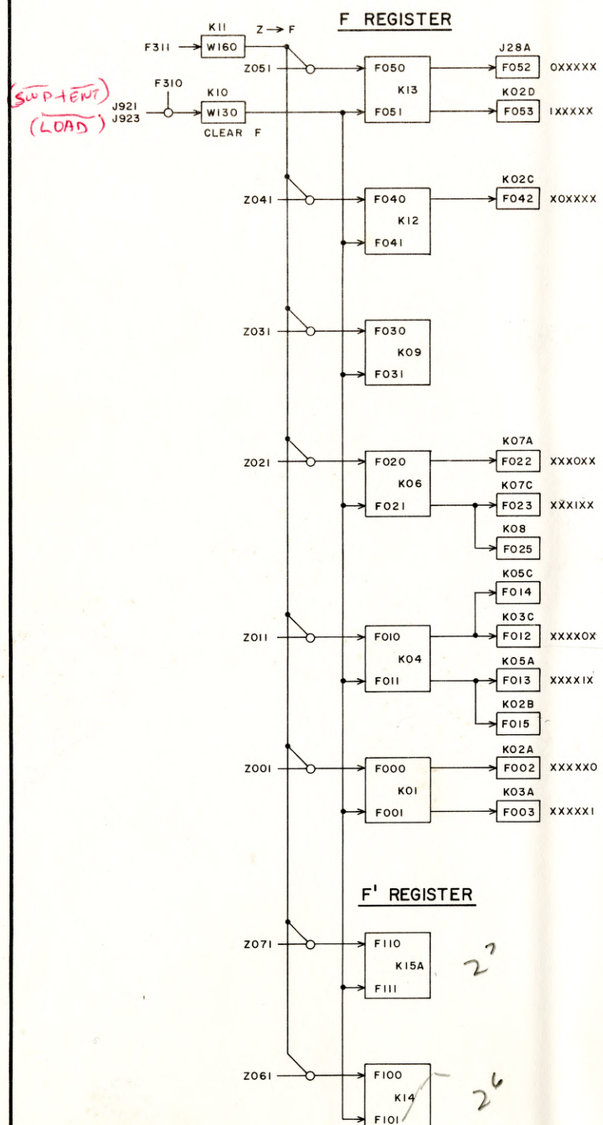
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364156 REV B C

SHT PAGE 3

F REGISTER



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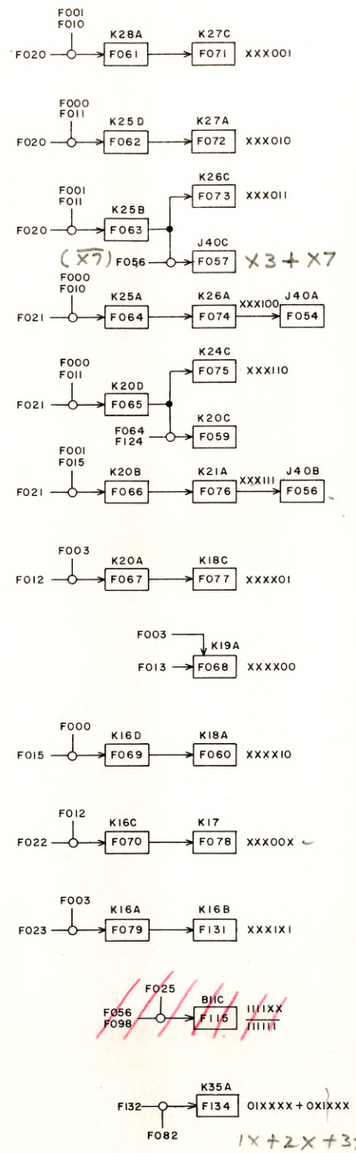
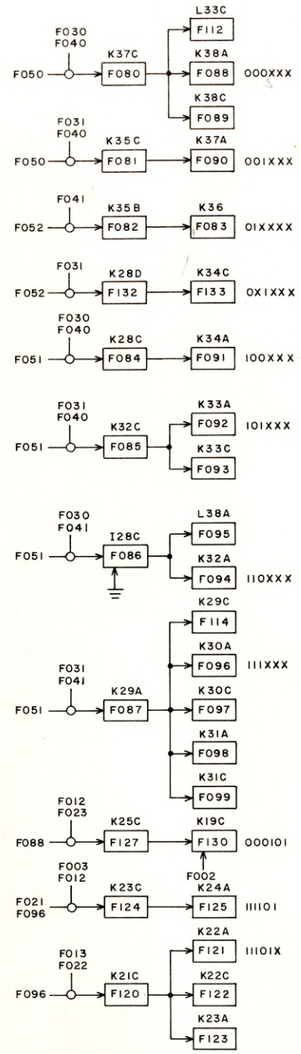




XXX10X
XXXX0X

REV	AUTH.	DATE	REVISIONS	APPROVED	CHK.	DRWR.	REG.
B	1585	3/15/65	-	-	-	-	-
A	M43	10/20/64	-	-	-	KH	JK

APPROVED • W. E. Moe 2/24/64
CHECKED • J. H. NIPP 2/14/64
DRAWN • N. K. BECK
DESIGNED -

REFERENCE DRAWINGS	

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

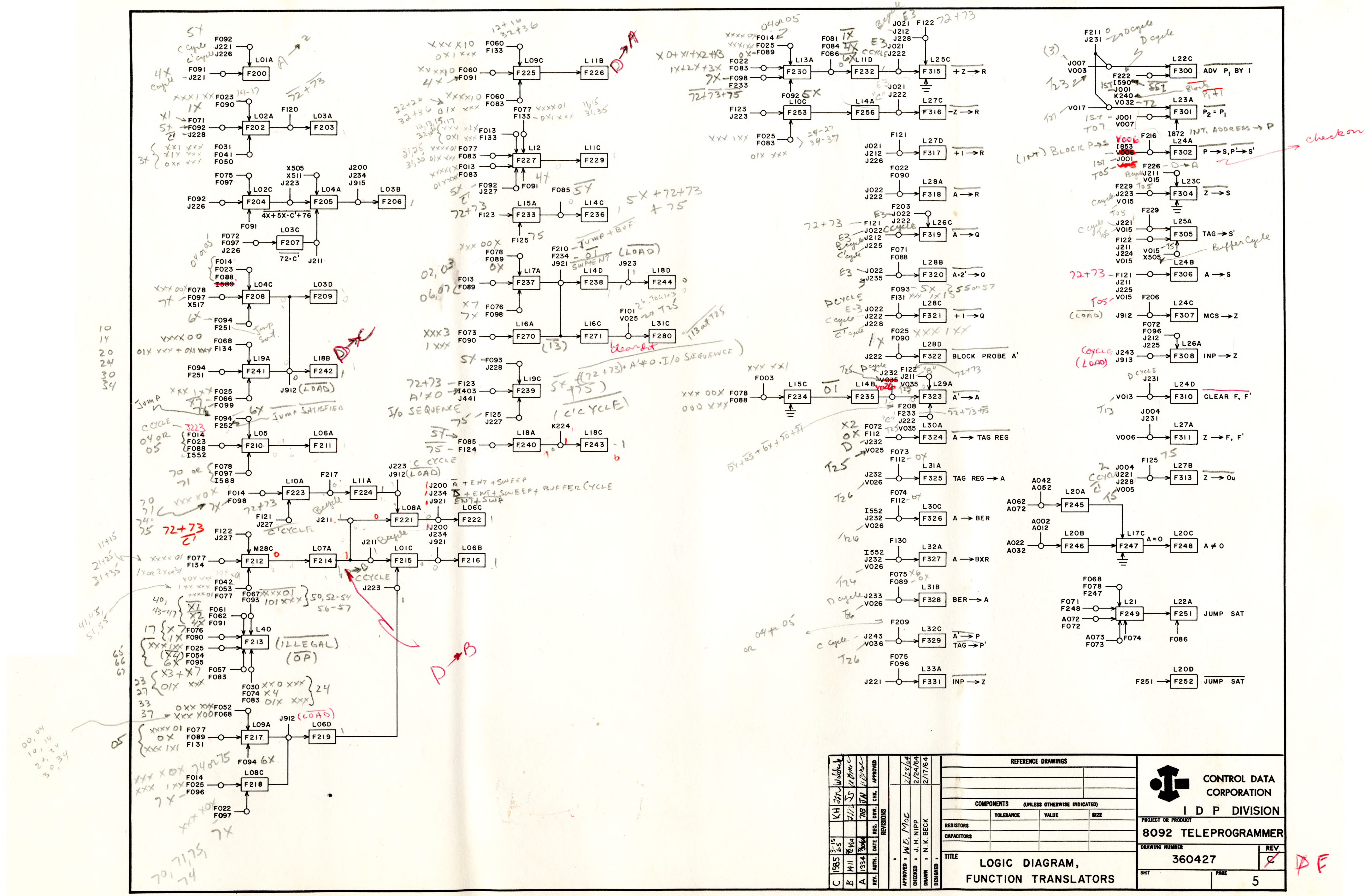
TITLE
LOGIC DIAGRAM,
REGISTERS, F & F' & TRANSLATORS

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360449 REV B C

SHT PAGE 4



REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

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RESISTORS			
CAPACITORS			

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A	1334				
B	1411				
C	1585	3-15-65			

APPROVED W. E. Moe 2/28/64
CHECKED J. H. NIPP 2/24/64
DRAWN N. K. BECK 2/17/64
DESIGNED

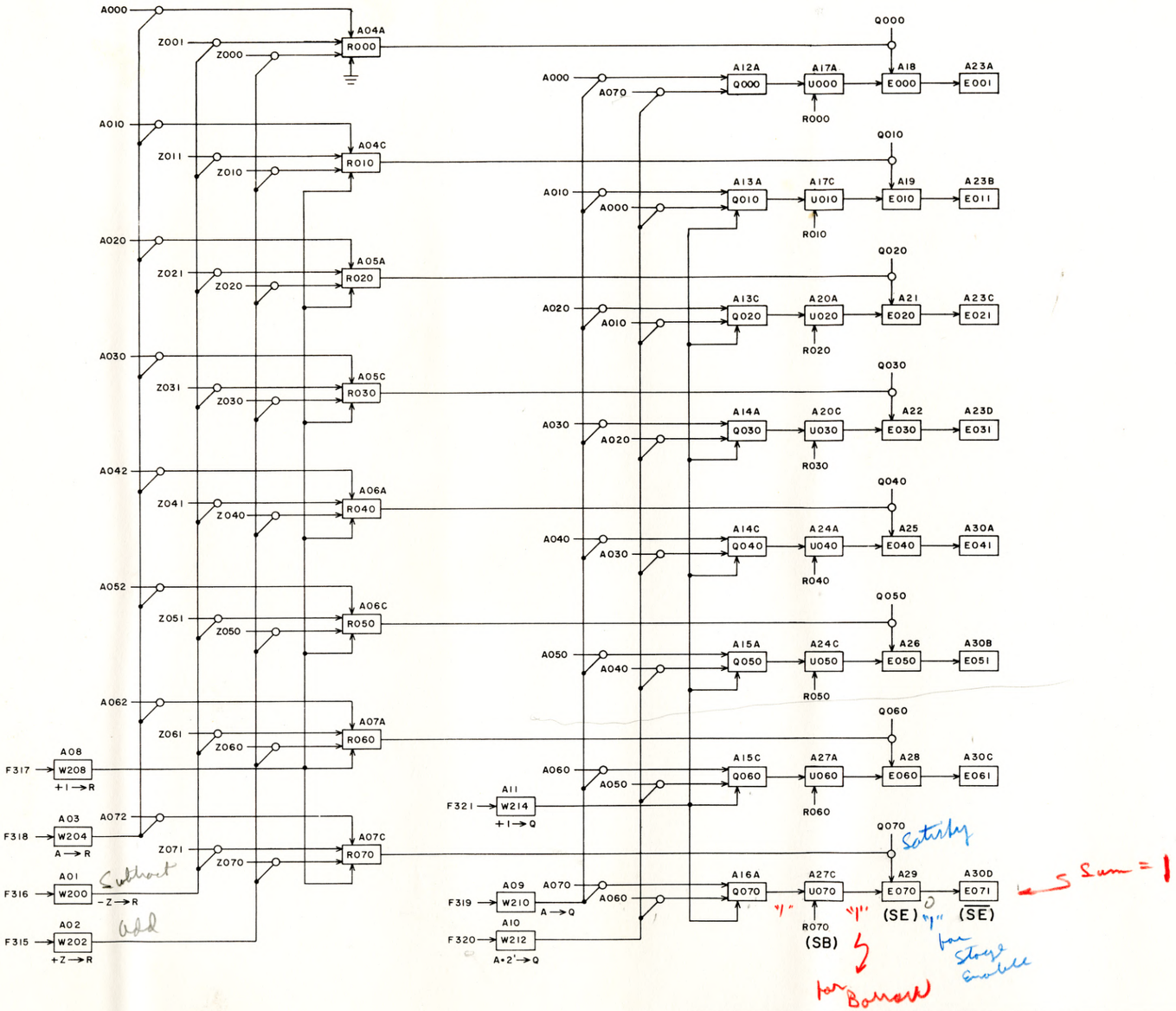
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 360427 REV C

TITLE: LOGIC DIAGRAM, FUNCTION TRANSLATORS

SHT PAGE 5



SUBTRACT
OUTPUTS → R = Z
Q = A

ADD
R = Z
Q = A

REV.	AUTH.	DATE	REVISIONS	APPROVED	CHK.
-			-		
			APPROVED - W.B. Moore	-	2/24/64
			CHECKED - J.H. NIPP		
			DRAWN - N.K. BECK		2/18/64
			DESIGNED -		

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
R AND Q INVERTERS

CONTROL DATA CORPORATION
I D P DIVISION

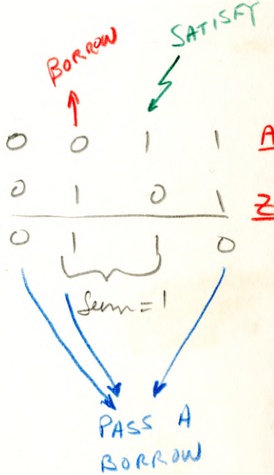
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360428

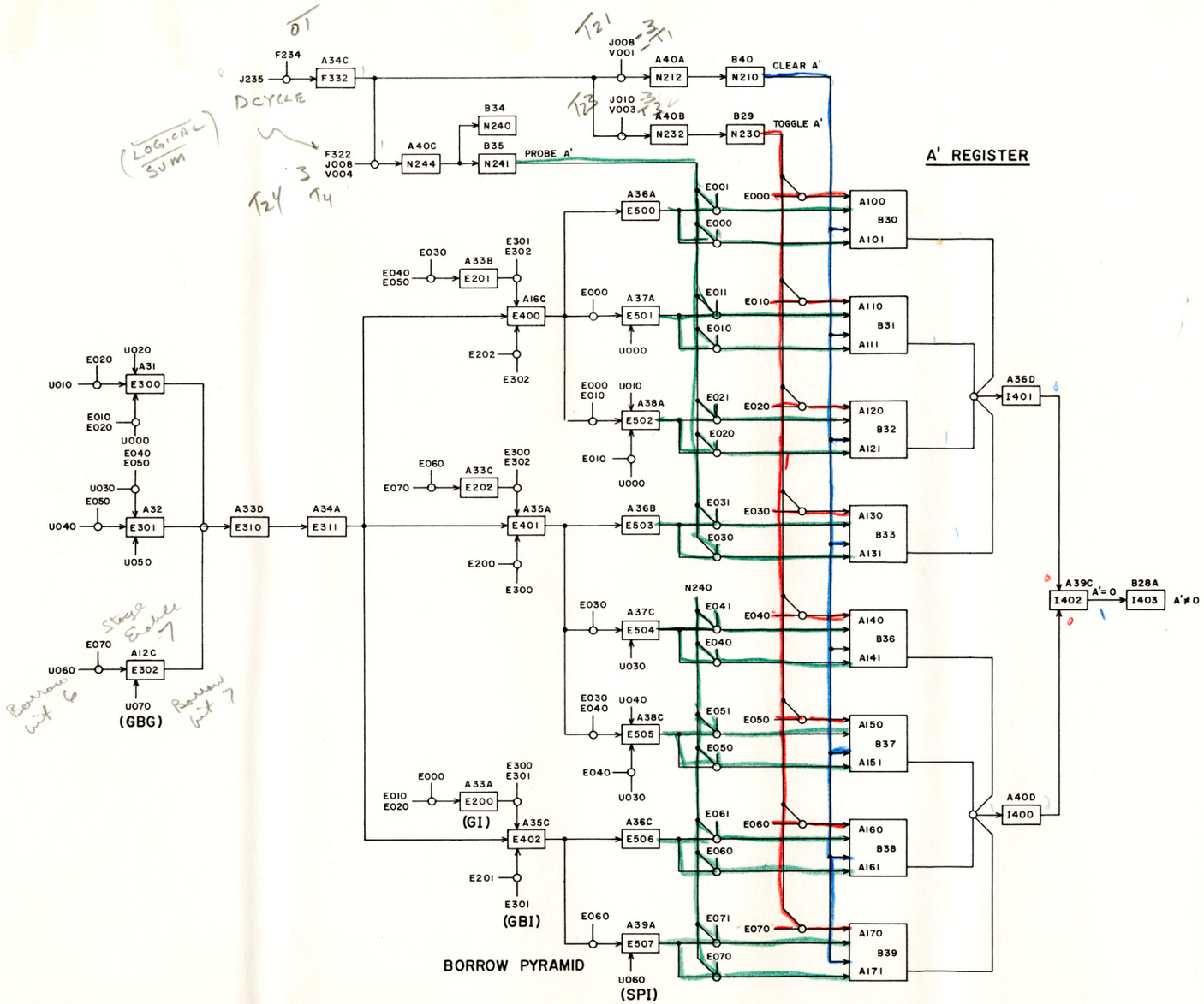
REV

SHT

PAGE
6



A' REGISTER



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REVISIONS					
APPROVED	W.D. Mac				2/28/64
CHECKED	J.H. NIPP				2/24/64
DRAWN	N.K. BECK				2/19/64
DESIGNED					

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

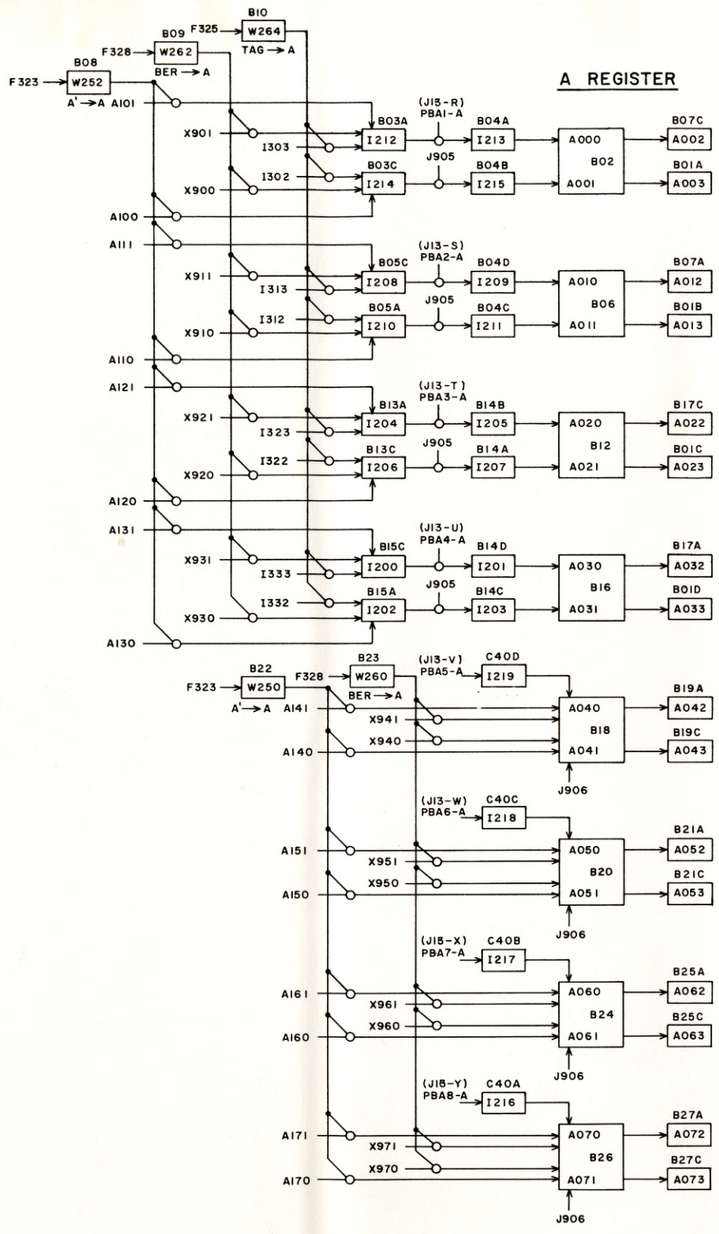
TITLE: LOGIC DIAGRAM, REGISTER – A'

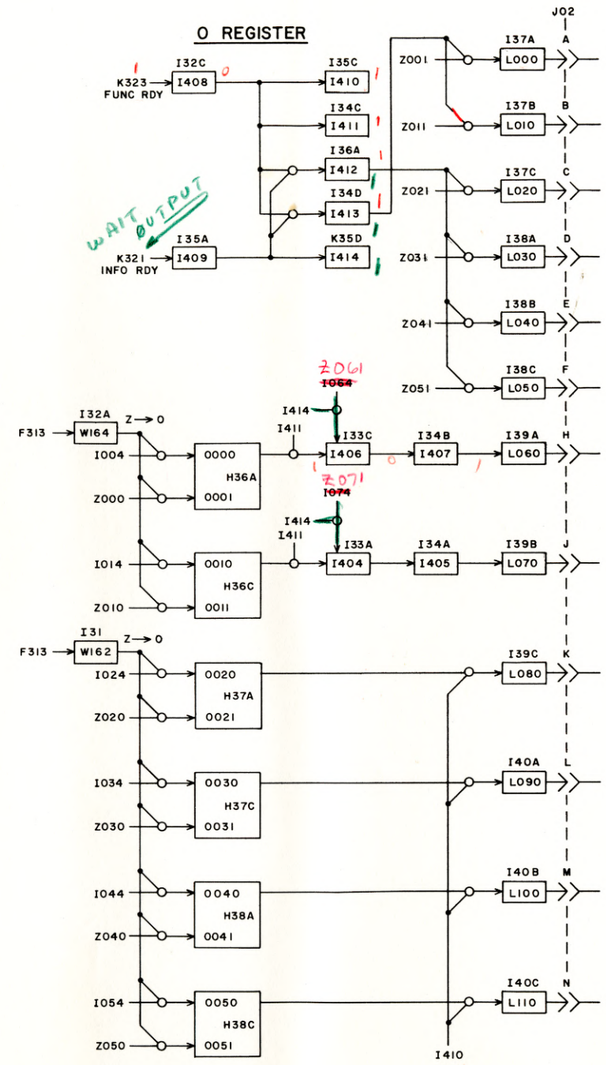
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 364157 REV:

SHT: PAGE: 7





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B	1585	3-15-65	KH	nB	DH	WBMoe
A	1354	10/24/64				

DESIGNED	-	
DRAWN	N.K. BECK	2/6/64
CHECKED	J.H.NIPP	2/24/64
APPROVED	W.B. Moe	2/26/64

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
REGISTERS – A AND O

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360429

REV
B C

SHT

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8

Z REGISTER

SENSE AMPLIFIERS

H01 Y200
H02 Y210
H03 Y220
H04 Y230
H05 Y240
H06 Y250
H07 Y260
H08 Y270

F308 F331 G31 W122 INPUT → Z J01
F200 J914 G32 W124 A → Z BFR CAB → Z 1577
F200 F308 F331 J914 F307 H24 W323
G34 W320 STORAGE → Z W325
J031 V010 H22A W102 J907 G33 W100 CLEAR Z
H22C 1554 W325 H23 W326 BFR → INHIBIT
E39 W327 Z → INHIBIT 1554

A H33A M000 M500 A003 H25A I001 Y200 H21-1 Y900 100 NSEC H25C I002 (J13-E) PBZ1-A H39A I005 Z000 G25 Z001 X700 G26A I004
B H33B M010 M510 A013 H26A I011 Y210 H21-2 Y910 100 NSEC H26C I012 (J13-F) PBZ2-A H39B I015 Z010 G27 Z011 X710 G26C I014
C H33C M020 M520 A023 H27A I021 Y220 H21-3 Y920 100 NSEC H27C I022 (J13-H) PBZ3-A H39C I025 Z020 G28 Z021 X720 G29A I024
D H34A M030 M530 A033 H28A I031 Y230 H21-4 Y930 100 NSEC H28C I032 (J13-J) PBZ4-A H39D I035 Z030 G30 Z031 X730 G29C I034
E H34B M040 M540 A043 H29A I041 Y240 H21-5 Y940 100 NSEC H29C I042 (J13-K) PBZ5-A H40A I045 Z040 G35 Z041 X740 G36A I044
F H34C M050 M550 A053 H30A I051 Y250 H21-6 Y950 100 NSEC H30C I052 (J13-L) PBZ6-A H40B I055 Z050 G37 Z051 X750 G36C I054
H H35A M060 M560 A063 H31A I061 Y260 H21-7 Y960 100 NSEC H31C I062 (J13-M) PBZ7-A H40C I065 Z060 G38 Z061 X760 G39A I064
J H35B M070 M570 A073 H32A I071 Y270 H21-8 Y970 100 NSEC H32C I072 (J13-N) PBZ8-A H40D I075 Z070 G40 Z071 X770 G39C I074

I1 I2 I5 I4

REV.	AUTH.	DATE	REVISIONS	CHK.	APPROVED
B	1585	12-15-65	REQ. DRW.	KH	
A	1402	9-23-64			

APPROVED = W.F. Nipp 2/24/64
CHECKED = J.H. NIPP 2/7/64
DRAWN = N.K. BECK
DESIGNED =

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

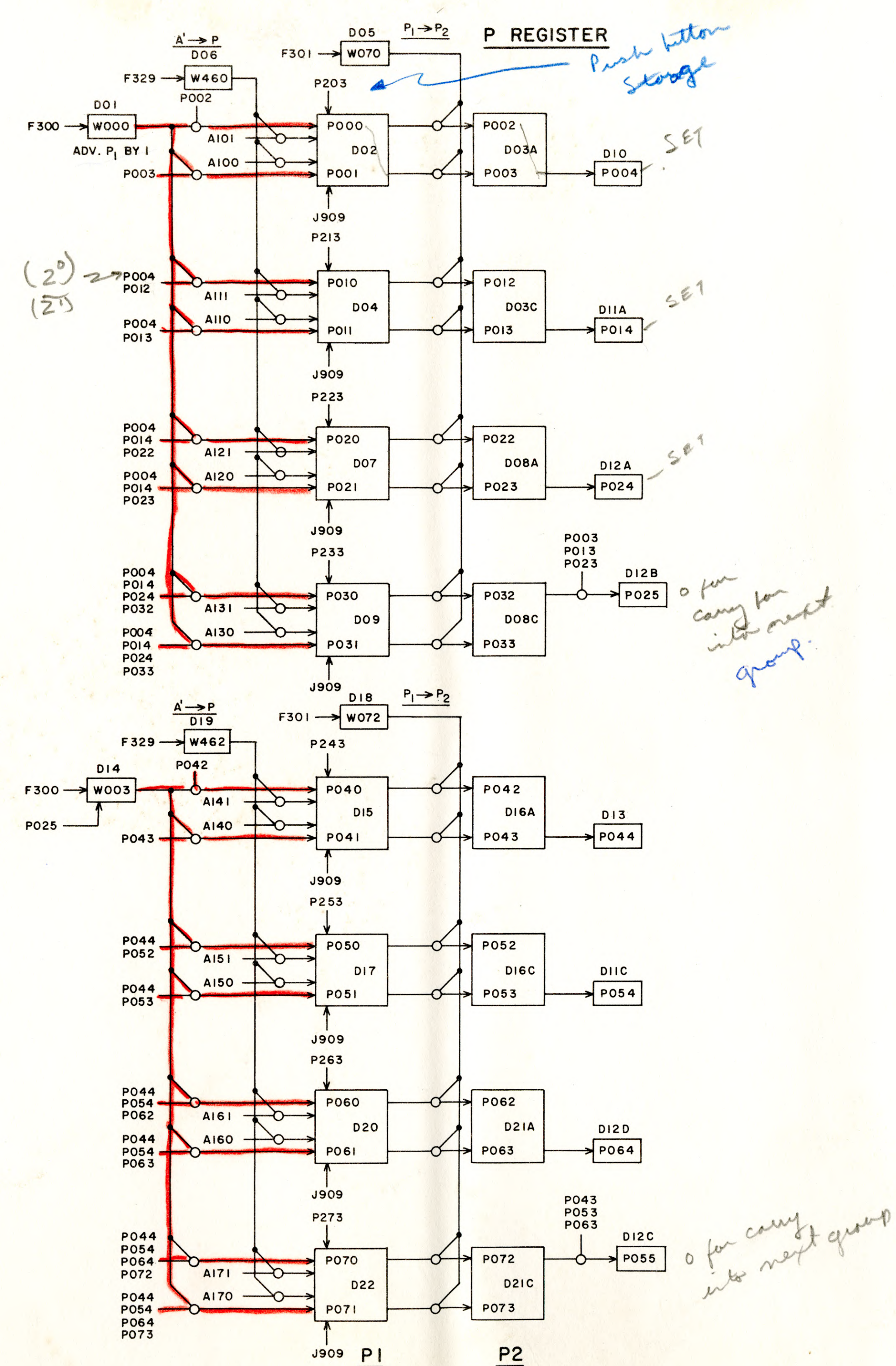
TITLE
LOGIC DIAGRAM
REGISTER-Z

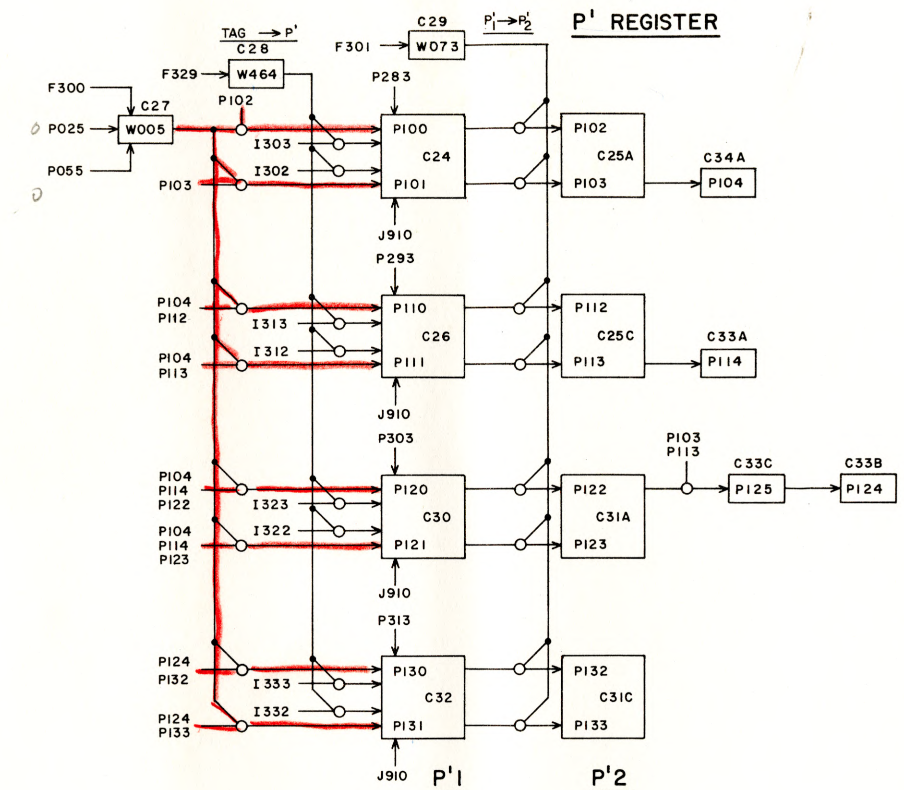
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364158 REV B

SHT PAGE 9





REVISIONS: A | 1585 | 3-15-64 | KH

DRAWN: N. K. BECK 2/4/64
CHECKED: J. H. NIPP 2/24/64
APPROVED: W. B. Moe 2/28/64

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: LOGIC DIAGRAM REGISTERS – P AND P'

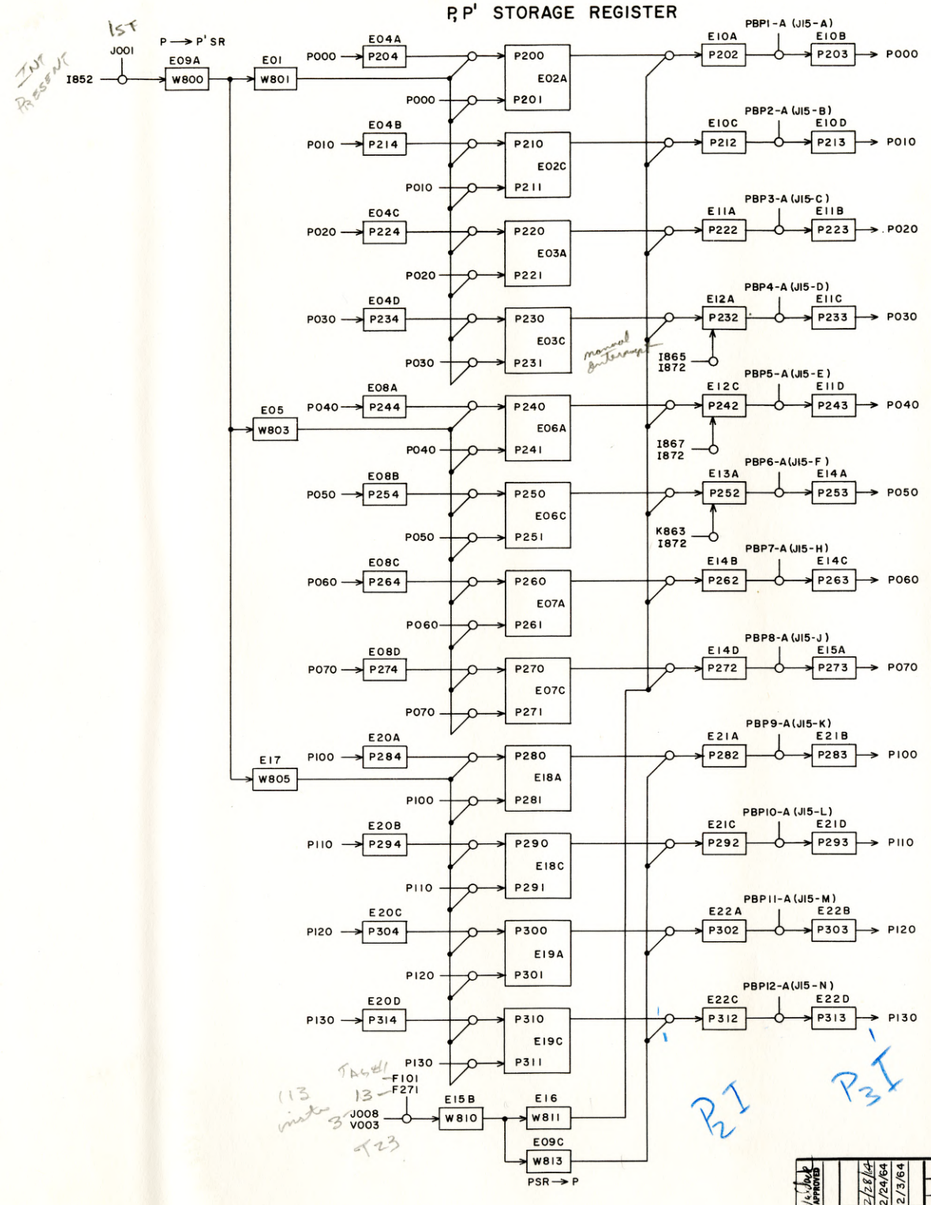
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 360430 REV A

PAGE 10

P, P' STORAGE REGISTER



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A	1585	2.28.64	-	-	-	KH

APPROVED	-	2.28.64
CHECKED	- J.H. NIPP	2/24/64
DRAWN	- N.K. BECK	2/3/64
DESIGNED	-	

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

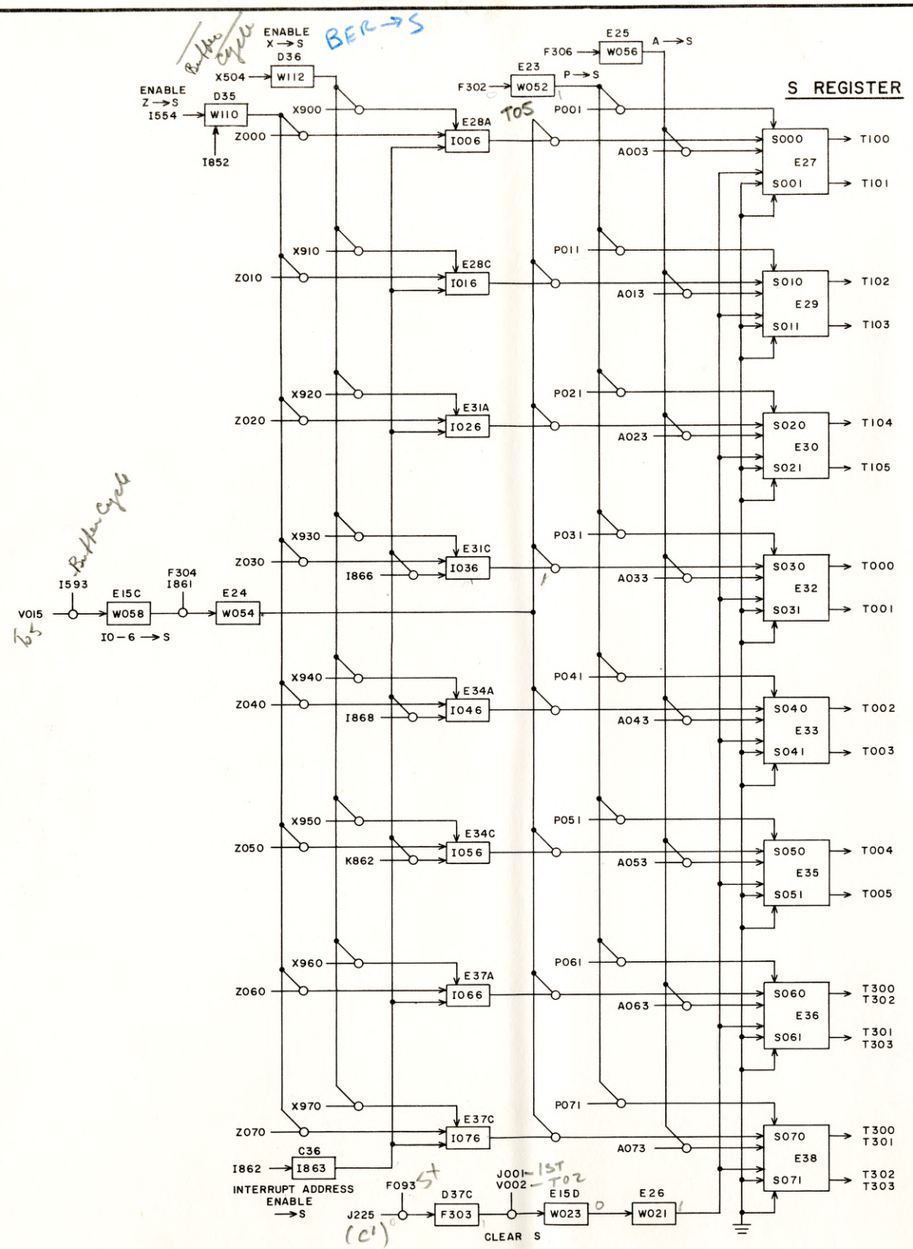
TITLE
LOGIC DIAGRAM
REGISTER – PSR

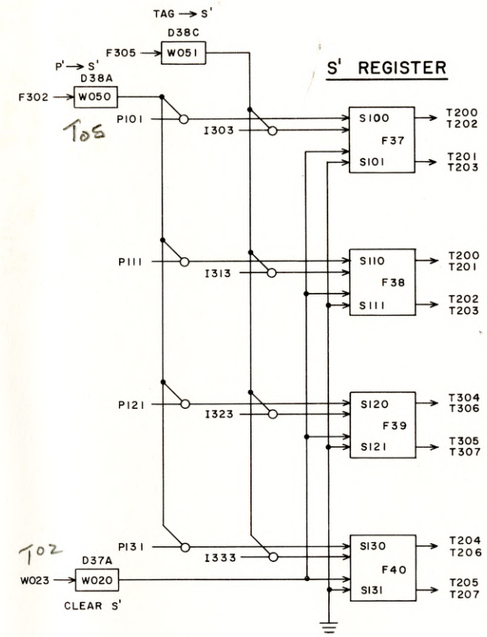
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364159 — REV A

SHT — PAGE 11





REV.	AUTH.	DATE	REGS.	DRW.	CHK.	APPROVED
A	1595	3-5-64			KH	

REVISIONS

APPROVED • W. E. Mose 2/24/64
CHECKED • J. H. NIPP 2/24/64
DRAWN • N. K. BECK 2/5/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

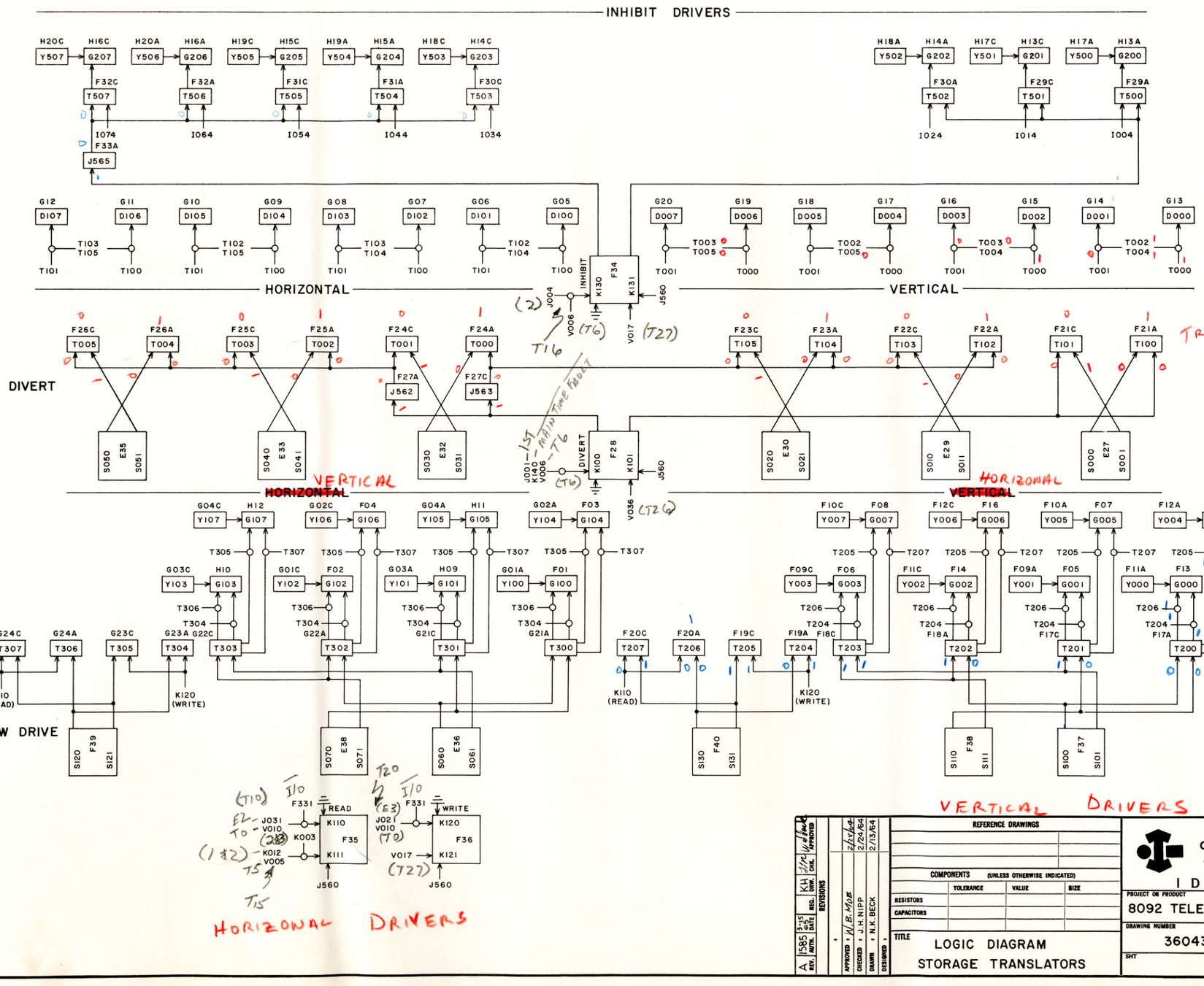
TITLE
LOGIC DIAGRAM
REGISTERS - S AND S'

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364160 REV A

SHT PAGE 12



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A	1585	3-15-64	-	W.B. MOSS	2/24/64	J.H. NIPP	2/13/64

DESIGNED - N.K. BECK

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

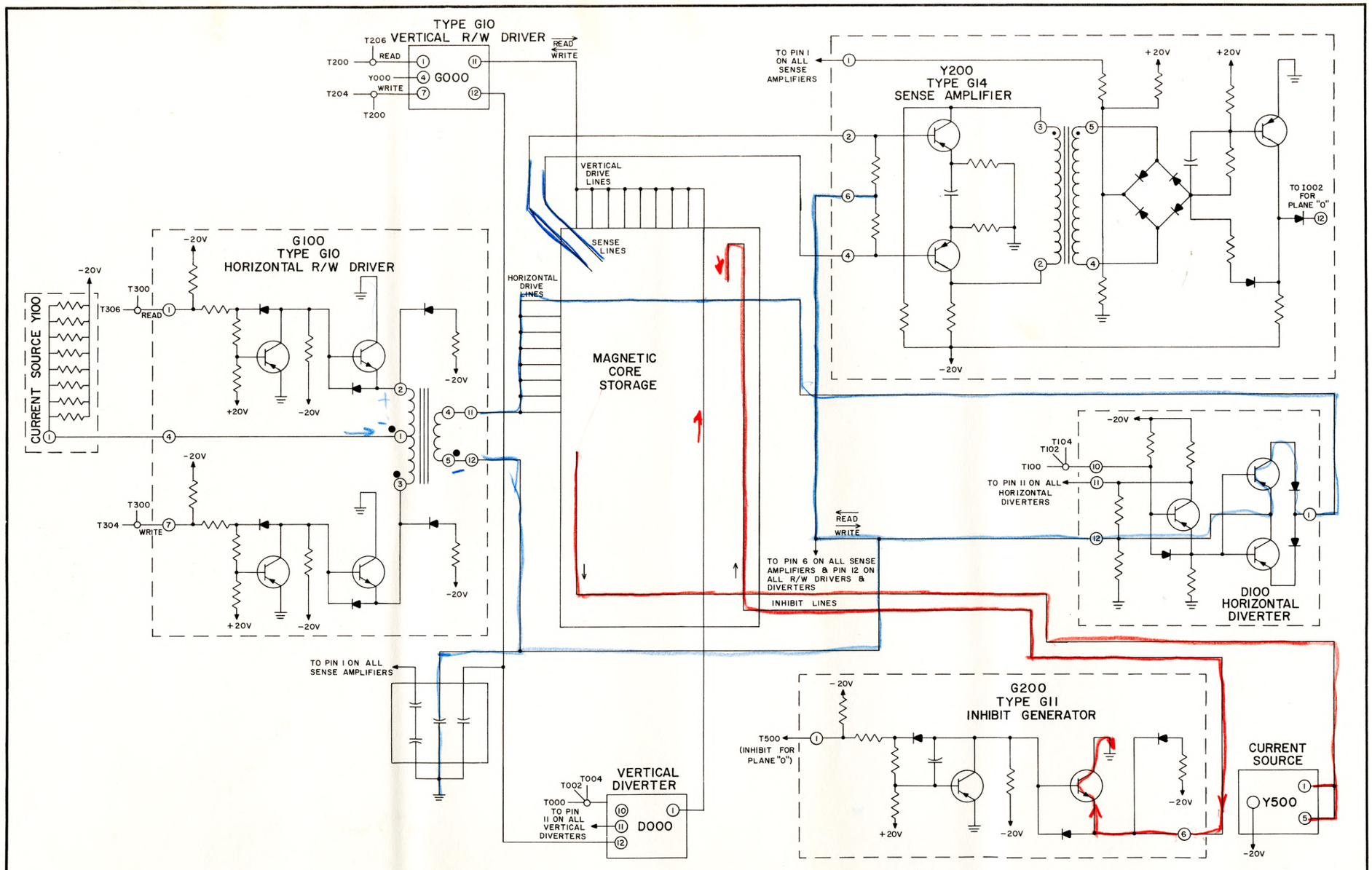
TITLE: LOGIC DIAGRAM STORAGE TRANSLATORS

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 360431 REV: A

SHT PAGE: 13



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A	1585	3/15/65	REG. DRW.	K H	

APPROVED	W.B.Hoe	2/24/64
CHECKED	J.H.NIPP	2/24/64
DRAWN	N.K.BECK	1/27/64
DESIGNED		

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

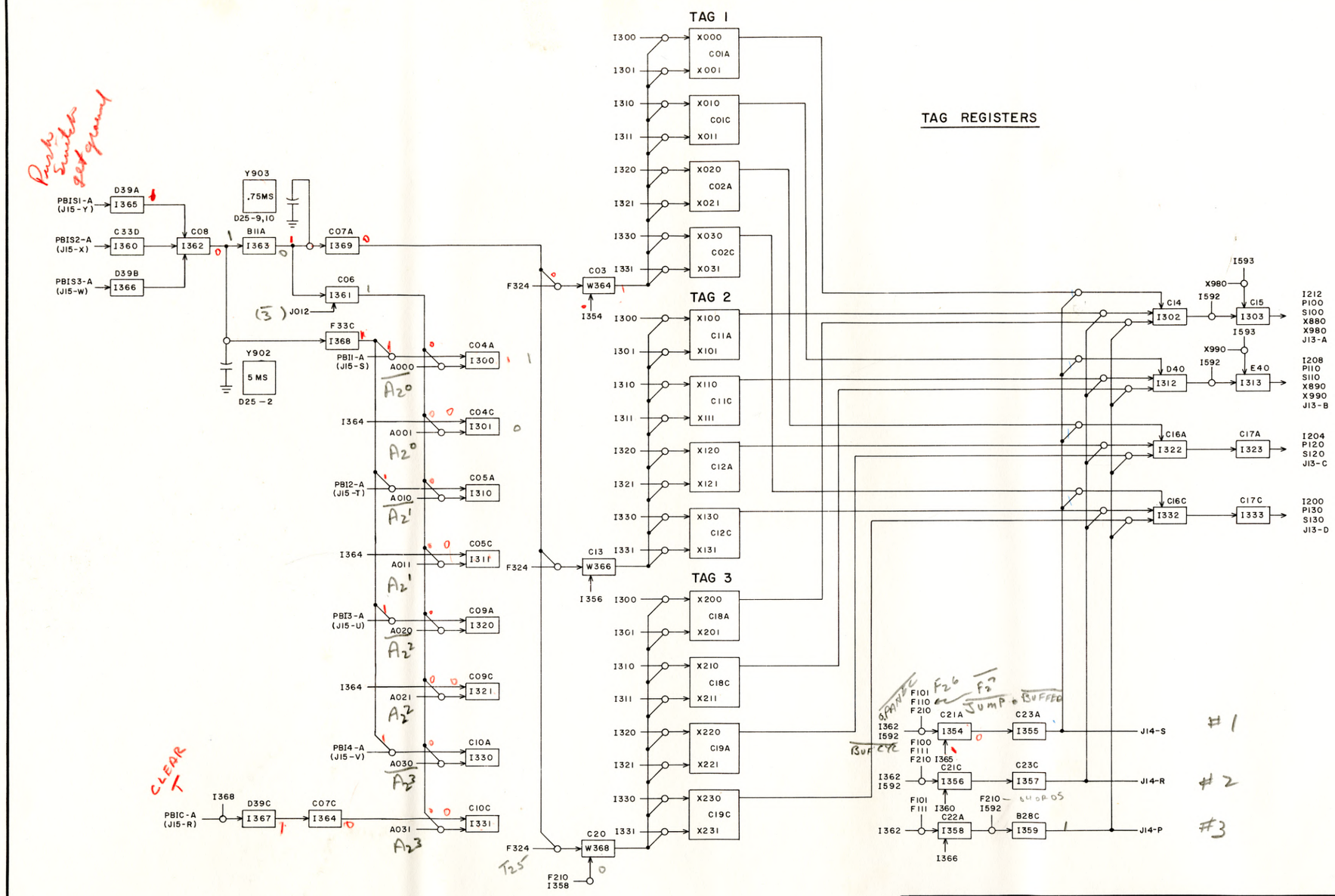
TITLE
SCHEMATIC DIAGRAM,
TYPICAL STORAGE CIRCUITS

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360442 REV A

SHT PAGE 14



REV.	AUTH.	DATE	REVISIONS	DRW.	CHK.	APPROVED
A	1585	2-5		KH		

APPROVED J. W. PAIGE 2/24/64
CHECKED J. H. NIPP
DRAWN N. K. BECK 2/10/64
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

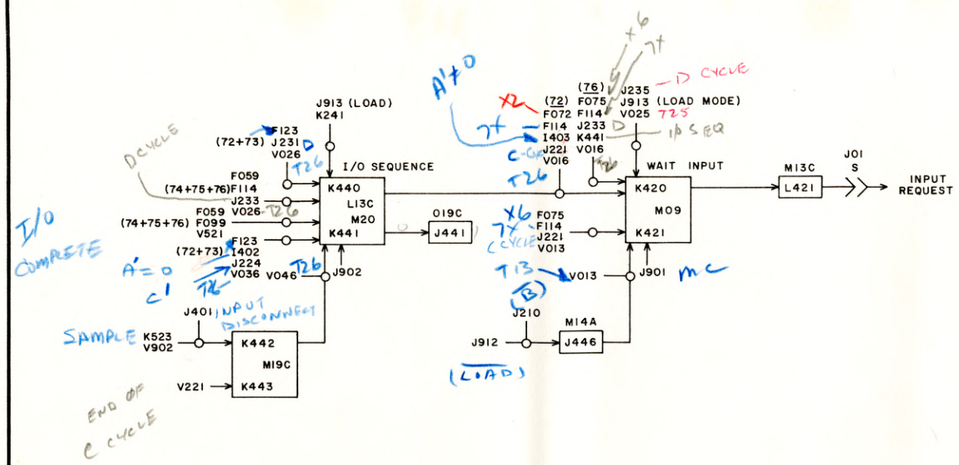
TITLE
LOGIC DIAGRAM, REGISTER – TAG 1,2,& 3

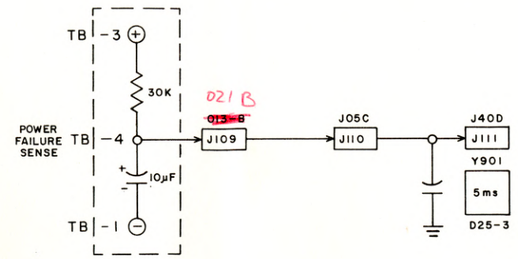
CONTROL DATA CORPORATION
I D P DIVISION

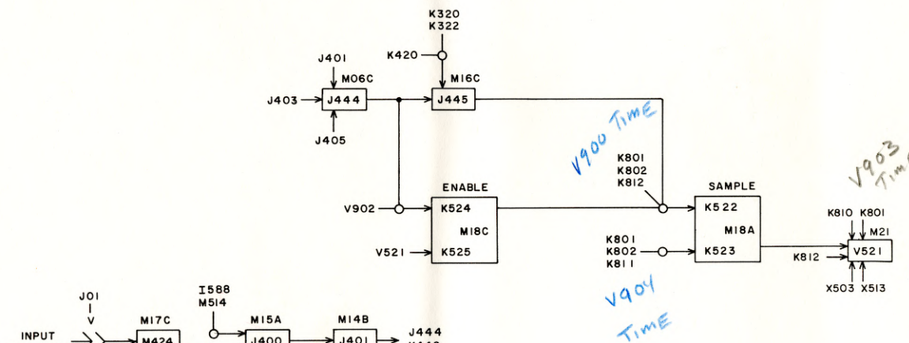
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

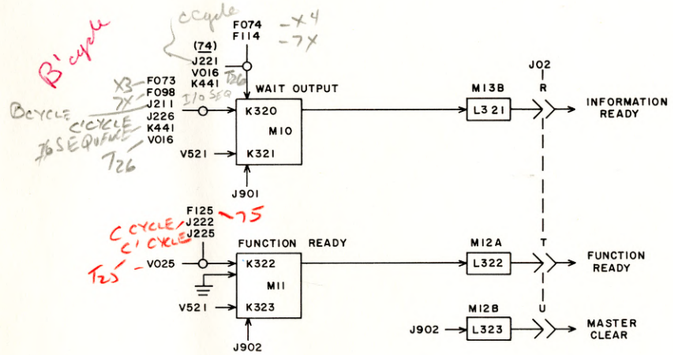
DRAWING NUMBER 360433 REV A

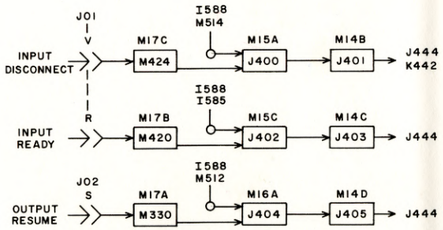
SHT PAGE 15

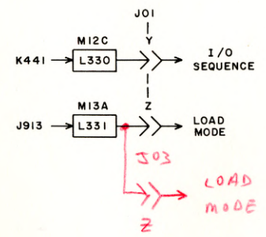












REV.	AUTH.	DATE	REVISIONS	REQ.	DRW.	CHK.	APPROVED
C	1585	1-15-64	-	KH	[illegible]	[illegible]	[illegible]
B	1411	11-26-63	-		[illegible]	[illegible]	[illegible]
A	1354	10-8-63	-		[illegible]	[illegible]	[illegible]

APPROVED - W. E. VOE 2/24/64
CHECKED - J. H. NIPP 2/24/64
DRAWN - N. K. BECK 2/21/64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
INPUT/OUTPUT CONTROL

CONTROL DATA CORPORATION
I D P DIVISION

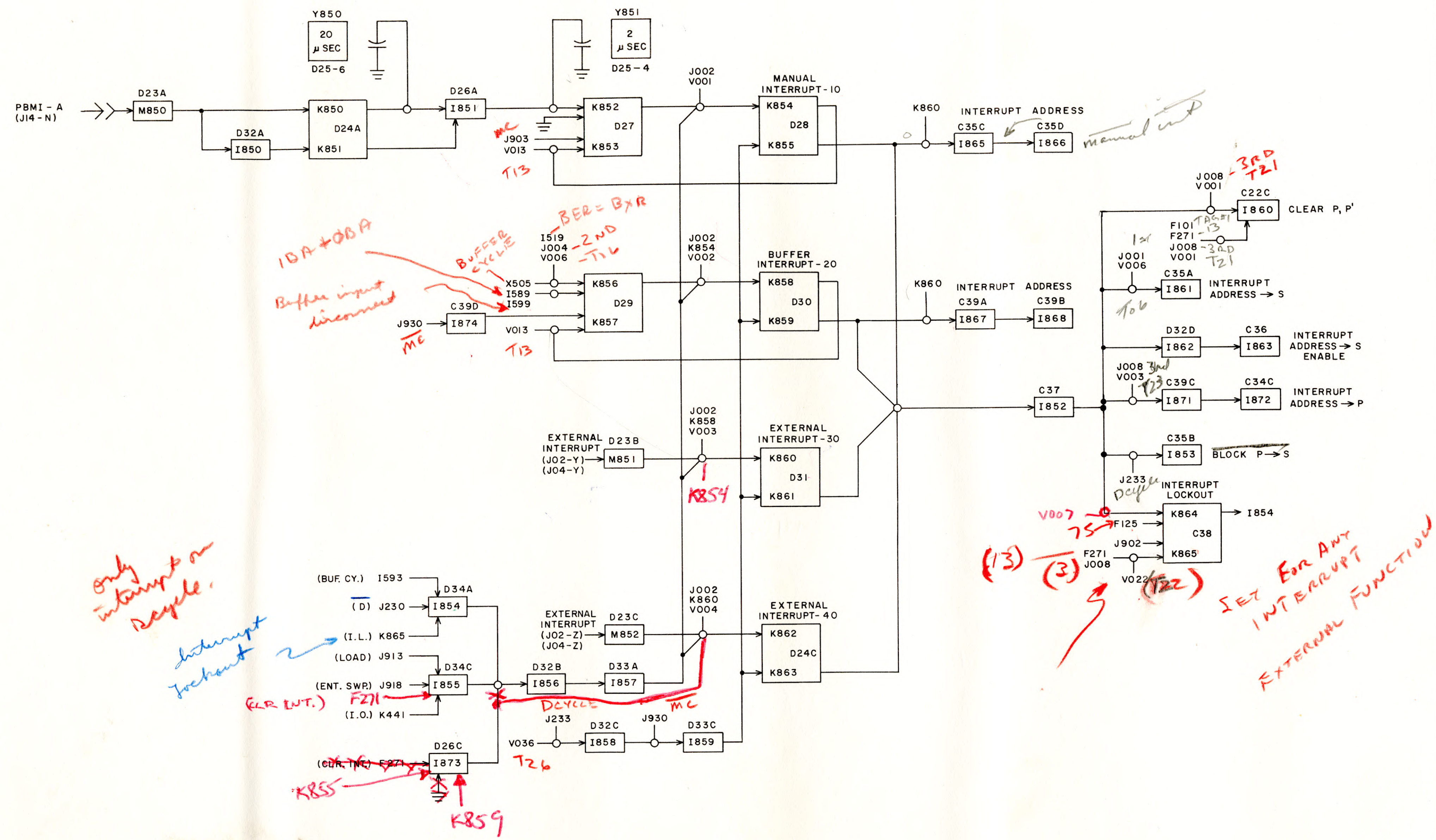
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360425

REV
C

SHT

PAGE
16



C	1585	7/8		
B	1354	7/8		
A	1334			
REV.	AUTH.	DATE	REQ. DRW.	CHK. APPROVED

REVISIONS

APPROVED · W.R. McKee · 2/2/64
CHECKED · J. H. NIPP · 2/24/64
DRAWN · N. K. BECK · 1/31/64
DESIGNED ·

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

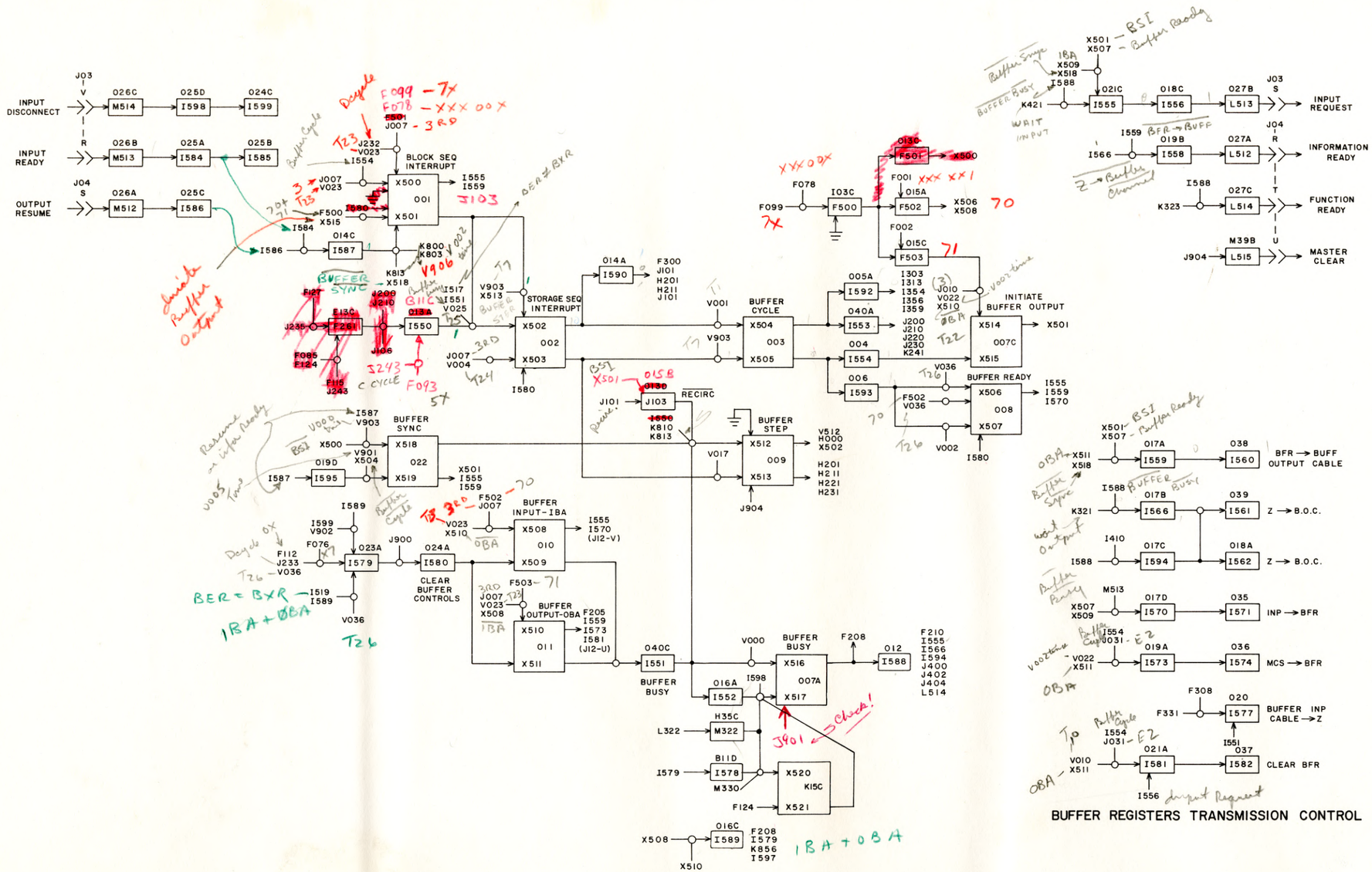
TITLE
LOGIC DIAGRAM
INTERRUPT

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360434
REV C

SHT
PAGE 17



REFERENCE DRAWINGS	

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

APPROVED	W. B. Mac
CHECKED	J.H. NIPP
DRAWN	N.K. BECK
DESIGNED	

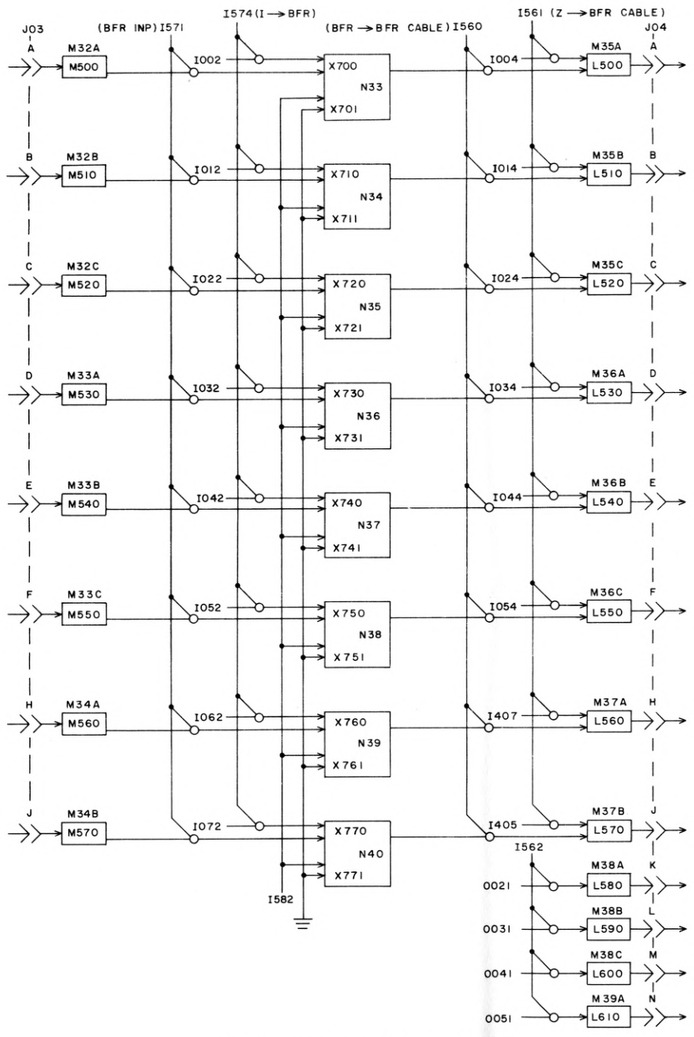
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

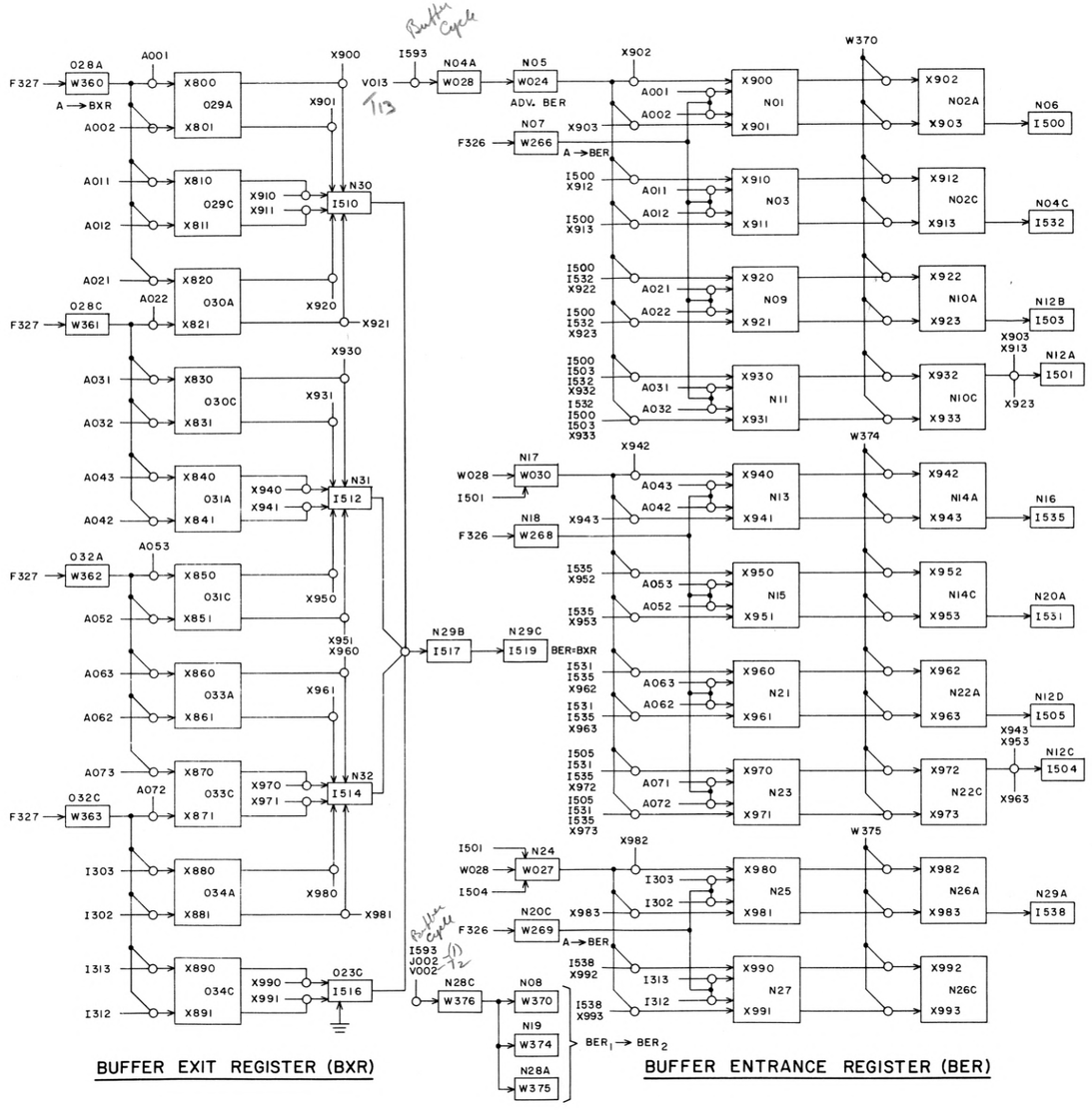
DRAWING NUMBER: 360447 REV: F

SHT: PAGE: 18

TITLE: LOGIC DIAGRAM BUFFER CONTROLS



BUFFER DATA REGISTER (BFR)



BUFFER EXIT REGISTER (BXR)

BUFFER ENTRANCE REGISTER (BER)

REV.	AUTH.	DATE	REVISIONS	DRW.	CHK.	APPROVED
A	1585	3-15-65	-	KH		

APPROVED	- W.E. Peterson	2/24/64
CHECKED	- J.H. NIPP	
DRAWN	- N.K. BECK	1/30/64
DESIGNED	-	

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

LOGIC DIAGRAM
REGISTERS - BFR, BXR, BER

CONTROL DATA CORPORATION
I D P DIVISION

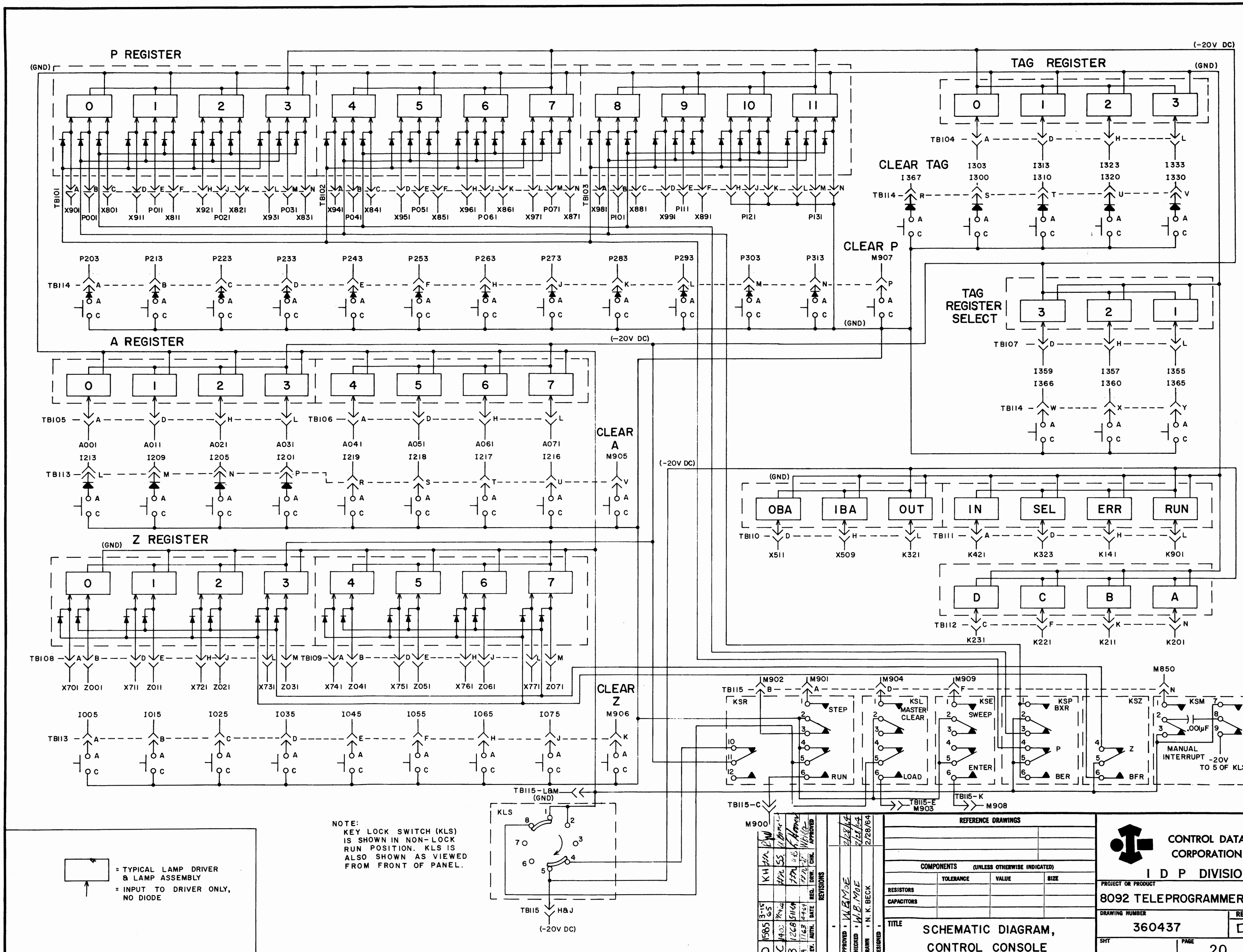
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360432

REV
A

SHT

PAGE
19



NOTE:
KEY LOCK SWITCH (KLS) IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

DESIGNED N. K. BECK 2/28/64
DRAWN W. B. MOE 2/28/64
CHECKED W. B. MOE 2/28/64
APPROVED

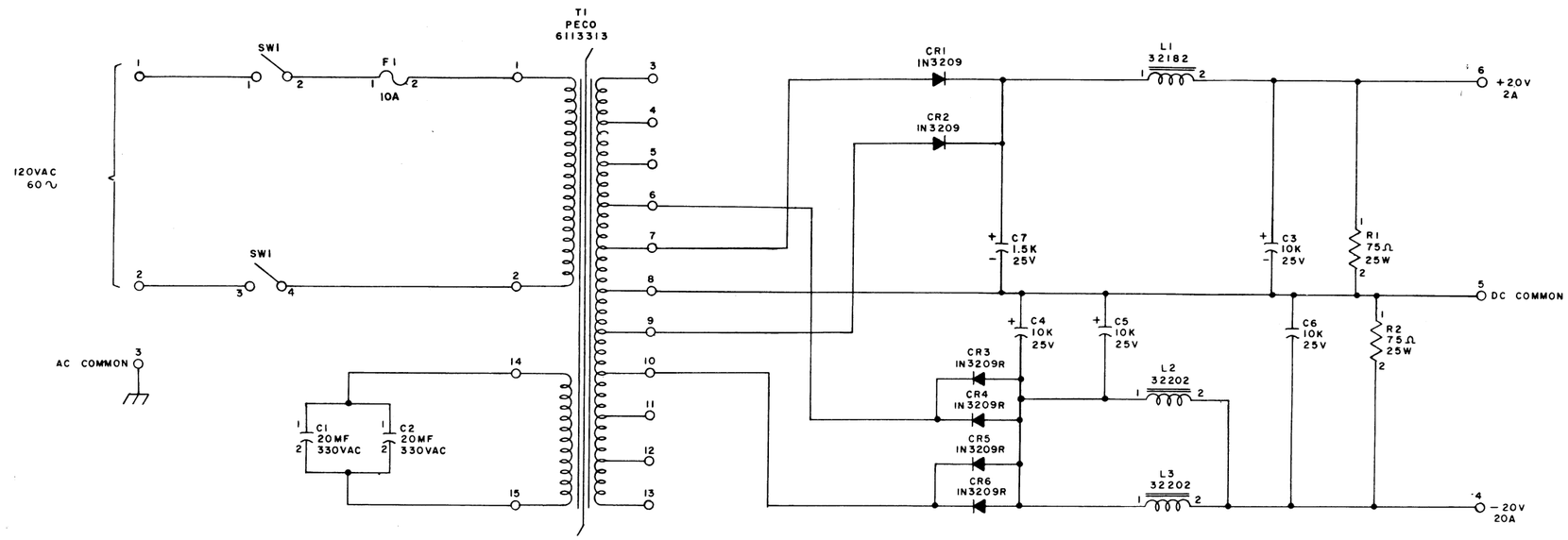
TITLE: SCHEMATIC DIAGRAM, CONTROL CONSOLE

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 360437 REV D

SHT PAGE 20



REV.	AUTH.	DATE	REQ.	DRW.	CHK.	APPROVED

REVISIONS -

APPROVED -

CHECKED -

DRAWN J.F. Fleming 12/20/63

DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
SCHEMATIC, POWER SUPPLY—
MODEL 8606-A

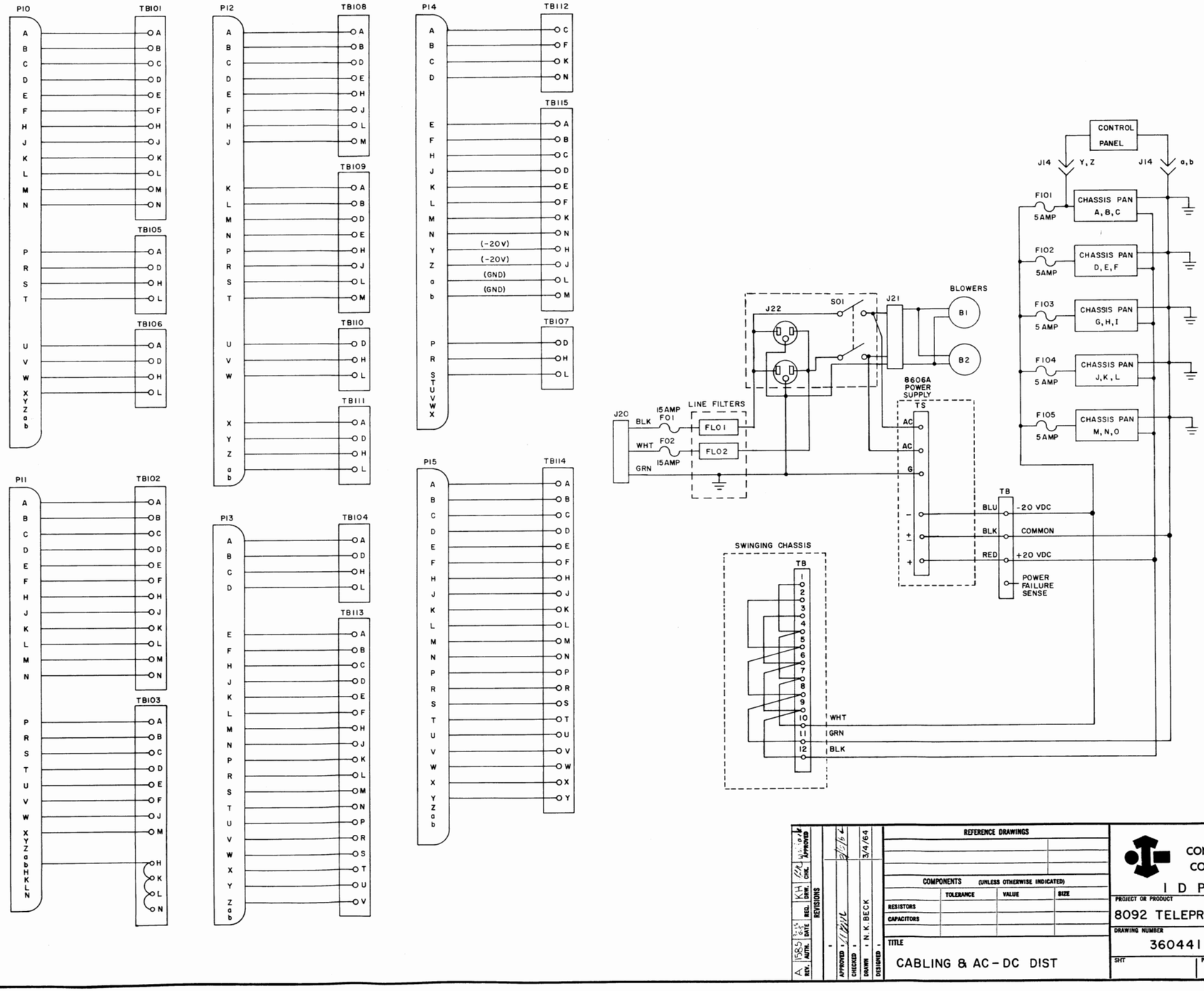
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT

DRAWING NUMBER 364071

REV

PAGE 21



REV.	AUTH.	DATE	REVISIONS	CHK.	APPROVED
A	1585	7-15	REQ. DRW.	KH	

APPROVED
CHECKED
DRAWN N. K. BECK 3/4/64
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
CABLING & AC-DC DIST

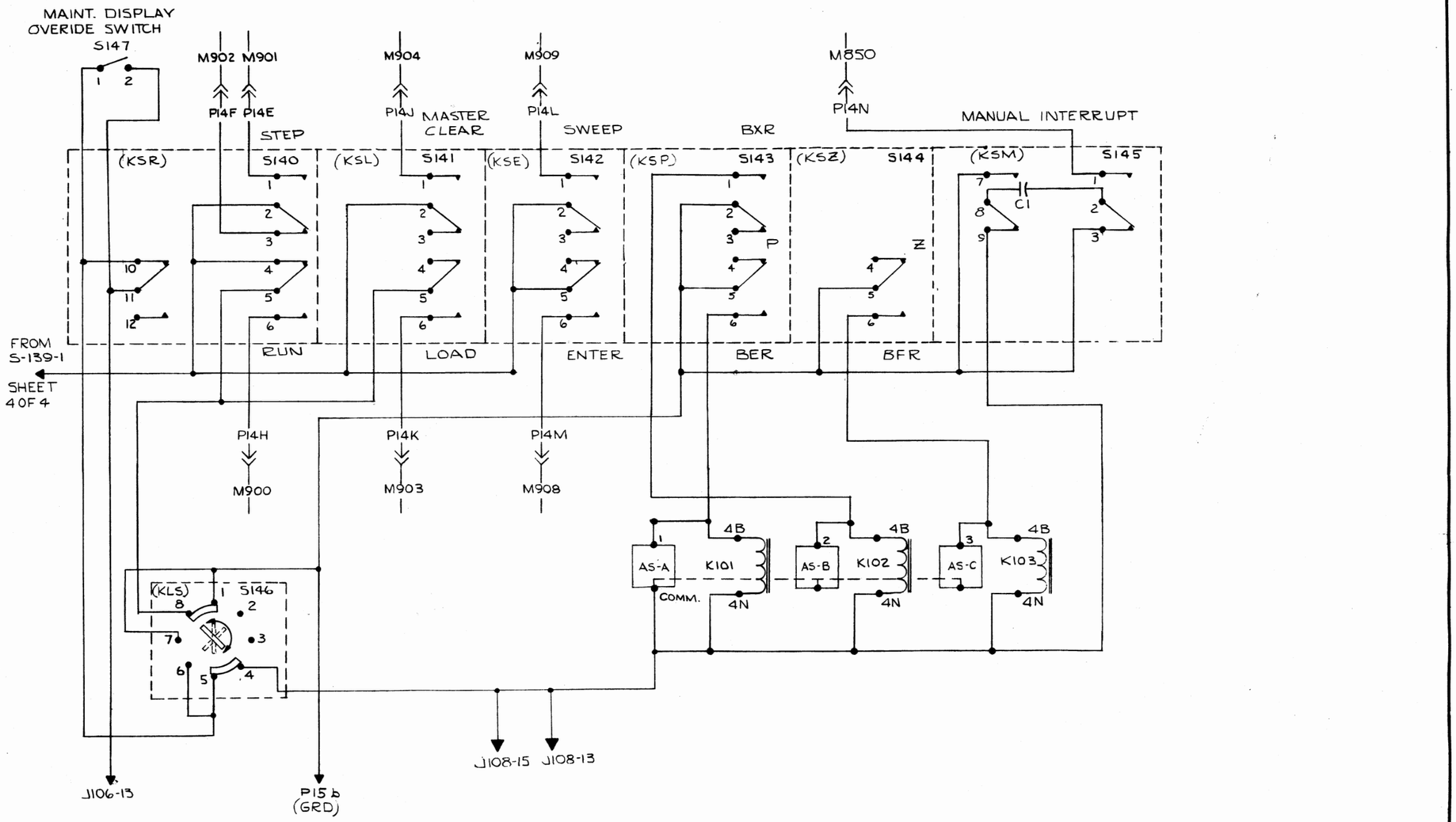
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360441 REV A

SHT PAGE 22

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A	—	—	RELEASED	—	11-10-64	—	[illegible]
B	8230		REVISED PER ECO	RAH	4-5-65	[illegible]	FES



2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.
1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:
± ___ ± ___ ± ___
DO NOT SCALE DRAWING
MATERIAL
FINISH

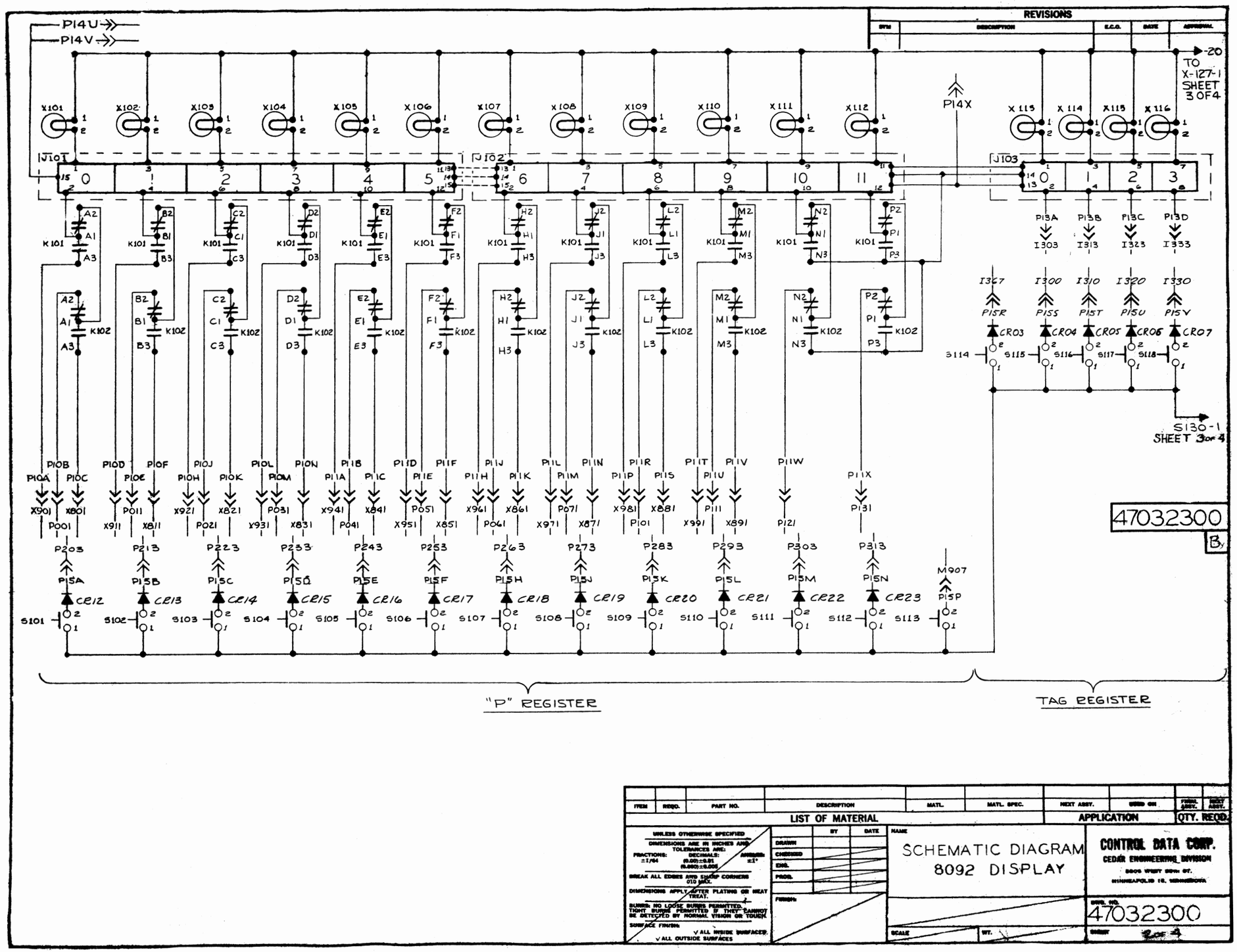
CONTROL DATA CORPORATION
CEDAR ENGINEERING DIVISION
DIGITAL ENGINEERING DEPARTMENT
MINNEAPOLIS, MINNESOTA

PRODUCT	8092 DISPLAY	
DRAWN	R. Alexander	11-13-64
CHECKED	V. Hilgar	11-13-64
ENGINEER	F. Ellison and	11-13-64
APPROVED		

TITLE
SCHEMATIC DIAGRAM
8092 DISPLAY

SIZE	DRAWING NO.	REV
C	47032300	B

SCALE
SHEET 1 OF 4



ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	FINISH ASSY.	DETAIL ASSY.

LIST OF MATERIAL — APPLICATION — QTY. REQD.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS: ±1/64 DECIMALS: (0.00) ±0.01 (0.000) ±0.005 ANGLES: ±1°
BREAK ALL EDGES AND SHARP CORNERS .010 MAX.
DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT.
BURRS: NO LOOSE BURRS PERMITTED. TIGHT BURRS PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH.
SURFACE FINISH: √ ALL INSIDE SURFACES, √ ALL OUTSIDE SURFACES

	BY	DATE
DRAWN		
CHECKED		
ENG.		
PROG.		
FINISH		

NAME: SCHEMATIC DIAGRAM 8092 DISPLAY

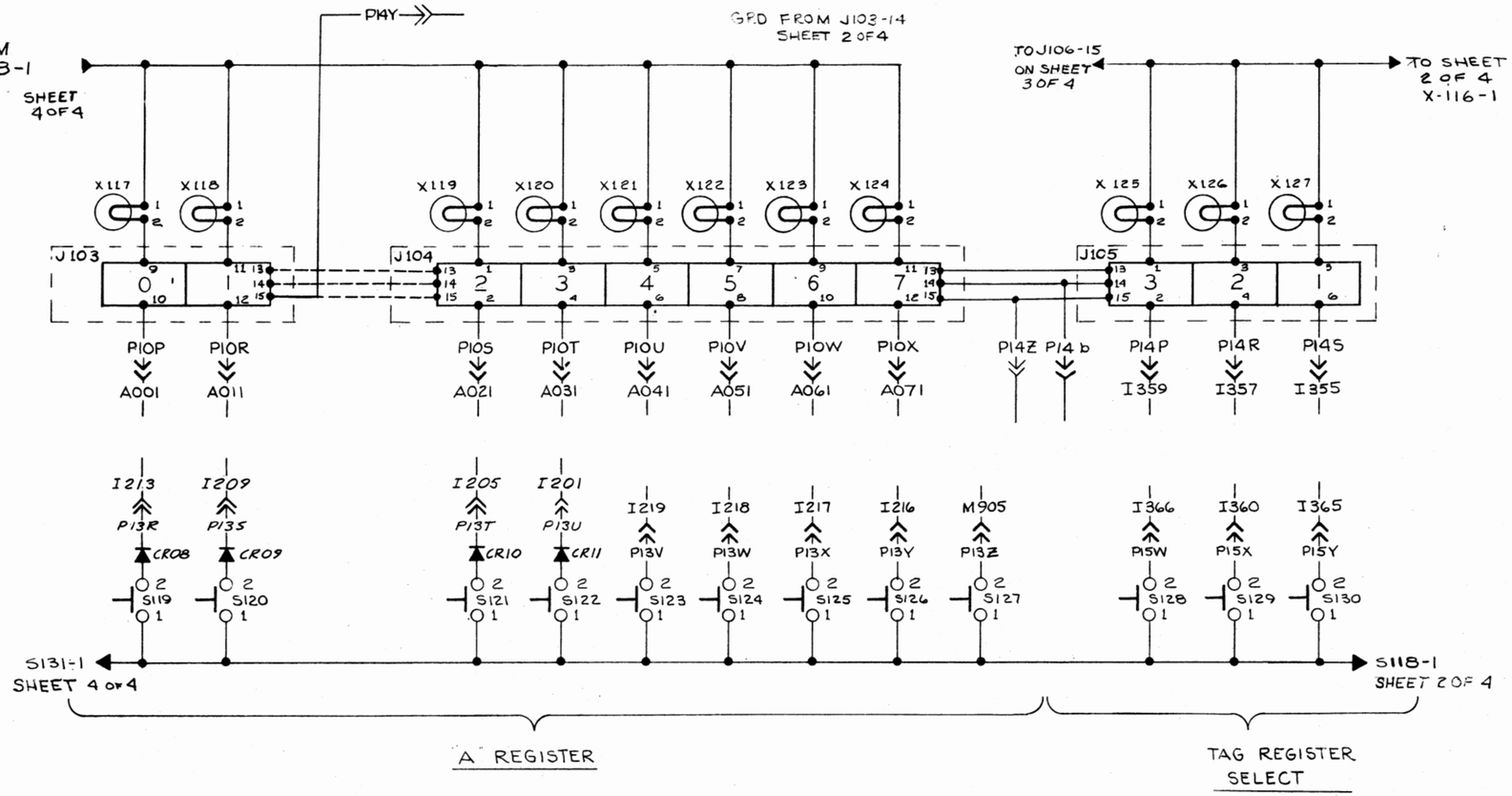
SCALE — WT.

CONTROL DATA CORP.
CEDAR ENGINEERING DIVISION
8609 WEST 36TH ST.
MINNEAPOLIS 16, MINNESOTA

DWG. NO. 47032300

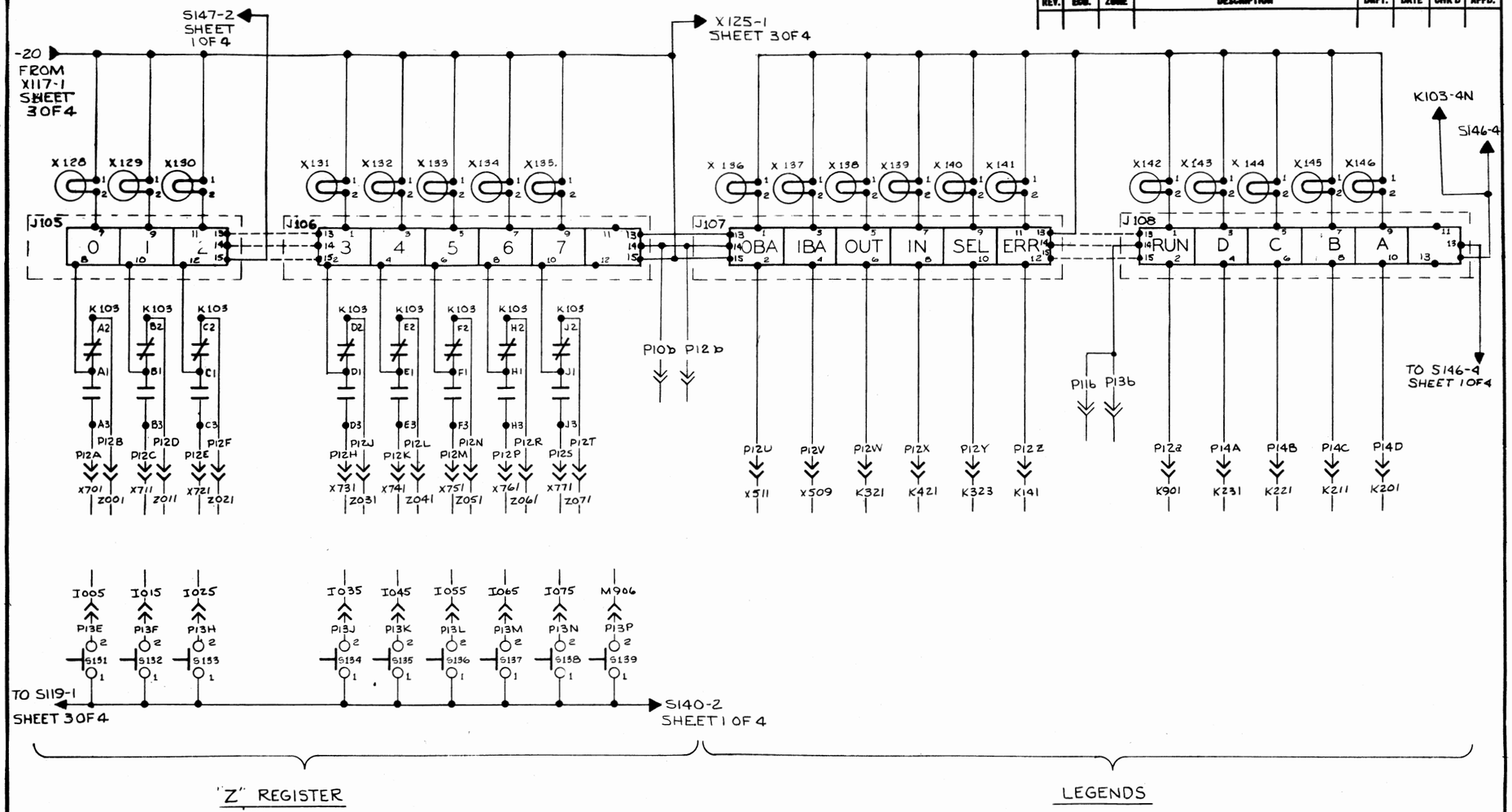
SHEET 2 OF 4

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: ± DECIMALS: ± ANGLES: ±	CONTROL DATA CORPORATION	TITLE	SCHEMATIC DIAGRAM 8092 DISPLAY
DO NOT SCALE DRAWING	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		
MATERIAL	PRODUCT 8092 DISPLAY		
FINISH	DRAWN / CHECKED / ENGINEER / APPROVED	SIZE C	DRAWING NO. 47032300 REV B
		SCALE	SHEET 3 OF 4

REVISIONS							
REV.	BDG.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: ± DECIMALS: ± ANGLES: ±	CONTROL DATA CORPORATION	TITLE	SCHEMATIC DIAGRAM 8092 DISPLAY
DO NOT SCALE DRAWING	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		
MATERIAL	PRODUCT 8092 DISPLAY	SIZE C	DRAWING NO. 47032300 REV B
FINISH	DRAWN / CHECKED / ENGINEER / APPROVED	SCALE	SHEET 4 OF 4