THUR MUSEU MUSEUM MONIMUM ROSE BOSC BOSC BC AC ACA ACAC HOGO 8090 CONTROL DATA COMPUTER REFERENCE MANUAL

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	RECORD of REVISIONS							
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A (6-11-65)	Miscellaneous errors corrected on pages 20, 54 and 59.							
В	Publications Change Order 12551. Added footnote to the description of the INP instruction. Page							
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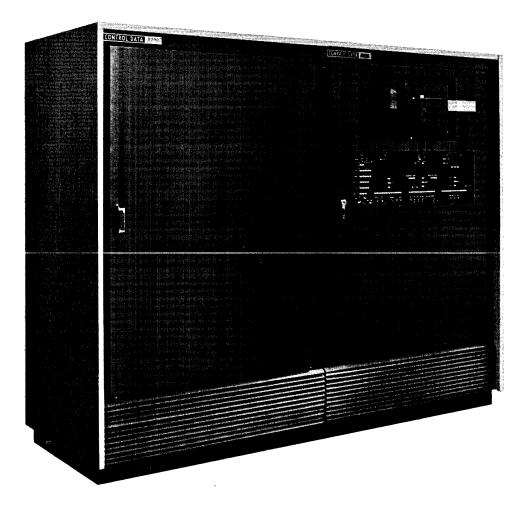
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Rev. E



CONTROL DATA 8090 COMPUTER SYSTEM

# **GENERAL DESCRIPTION**

The CONTROL DATA 8090 Computer System is a small-scale computer system with many features normally found in large scale computer systems. Important features include:

- Buffered input-output
- Internal and external interrupt
- An expandable magnetic core memory (4,096 to 32,768 words)
- High speed paper tape reader and punch
- Extended arithmetic capabilities
- Transistor-diode logic
- Wide temperature range

This system may be expanded to a system which can include the following external equipment:

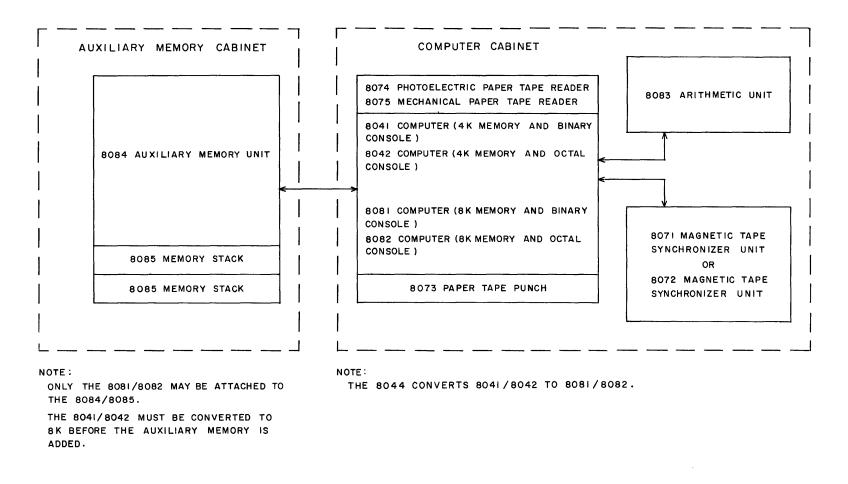
- Up to 40 magnetic tape stations
- Input-output typewriters
- Punched card readers, punches, and low speed line printers
- High speed (1,000 lines/minute) printers
- Plotting and digital display equipment
- Analog-to-digital and digital-to-analog equipment
- Two or more CONTROL DATA computers operating together in a satellite system
- Two CONTROL DATA 8090 Computers operating independently but sharing the same magnetic core memory

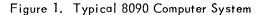
Using a high speed data transfer channel, the CONTROL DATA 8090 may be tied into other CONTROL DATA computers. This allows multi-computer processing and computer control of computers, and two computers may share such input-output equipment as magnetic tape stations to assure high computing performance at a minimum cost.

The 8090 Computer System is constructed in unit form. The design enables the user to expand the basic system easily by the addition of functional units tailored to satisfy specific requirements. Table 1 lists available units by model number and name. Figure 1 shows a typical 8090 system.

TABLE 1.	UNIT DESCRIPTIONS,	8090 SYSTEM
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MODEL	ITEM
8041	Basic 4K Computer; 12-bit high speed digital computer, including 4,096 words of magnetic core storage. Includes binary console, power supply, and computer cabinet.
8042	Basic 4K Computer; same as 8041 except octal display replaces binary display console.
8044	Memory Conversion Kit; increases basic 4K Computer to 8K.
8081	Basic 8K Computer; 12-bit high speed digital computer, including 8,192 words of magnetic core storage. Includes binary console, power supply, and computer cabinet.
8082	Basic 8K Computer; same as 8081 except octal display console re- places binary display console.
8083	Arithmetic Unit; provides 27-bit precision add and subtract, mul- tiply and divide, and allows eight digit FORTRAN format.
8084	Auxiliary Memory; provides memory expansibility of 8,192 12-bit words and an additional buffer channel. Includes auxiliary memory cabinet and power supply. Has control for two additional 8085's.
8085	8K Storage Option; provides memory expansibility for 8084 in mod- ules of 8,192 12-bit words. Includes power supply.
8071	Magnetic Tape Synchronizer; provides communication path with up to four CONTROL DATA 603 Magnetic Tape Transports.
8072	Magnetic Tape Synchronizer; provides communication path with up to eight CONTROL DATA 606 Magnetic Tape Transports.
8073	Paper Tape Punch; prepares fully perforated tape at speeds up to a standard speed of 63.3 characters per second. Includes power supply.
8074 A/B	Paper Tape Reader, Photoelectric; reads up to 350 characters per second of 5, 7, or 8 level tapes of standard width.
8074 C/D	Paper Tape Reader, Photoelectric; reads up to 400 characters per second of 5, 7, or 8 level tapes of standard width.
8075	Paper Tape Reader, Mechanical; reads up to 120 characters per second of 5, 7, or 8 level tapes of standard width.





# THE CENTRAL COMPUTER

The computer is a parallel, single address electronic data processor. Operation is controlled by an internally stored program located in sequential addresses. The basic memory of the Control Data 8090 consists of one or two units (or banks) of magnetic core storage, each with a capacity of 4,096 12-bit binary words and a storage cycle time of 6.4 microseconds. This basic memory may be expanded in a 4,096 module to 8,192 words and then in modules of 8,192 words up to a maximum of 32,768 words. Instructions are executed in one to four storage cycles; the time varies between 6.4 and 25.6 microseconds. The average program execution time for the 130 instructions is approximately 15 microseconds per instruction.

# NOTATION

The following abbreviations will be used throughout the remainder of this manual:

manoar.	
Α	The A register
Р	The P register
Z	The Z register
BER	The BUFFER ENTRANCE register
BXR	The BUFFER EXIT register
BFR	The BUFFER DATA register
E	The 6 low order bits in the first word of a 8090 instruction
F	The 6 high order bits in the first word of a 8090 instruction
G	The 12 bits in the second word of all 2-word 8090 instructions'
Х, Ү	Any octal digit, 0-7
XXXX	An octal operand or EF code
YYYY	An octal address
()	"The contents of" whatever location or register is specified
	within the parentheses. The only exception to this is a reference
	to a specific storage bank control in its numeric value. In this
	case, reference is to the storage bank number, e.g., (0) refers to
	storage bank zero. This is the only time a single digit will be
	enclosed in parentheses.
(d)	The contents of the DIRECT storage bank control
(r)	The contents of the RELATIVE storage bank control
(i)	The contents of the INDIRECT storage bank control
(Ь)	The contents of the BUFFER storage bank control
→	The function or quantity on the left of the arrow replaces the
	function or quantity on the right.
FWA	"First word address." This term is used when reference is made
	to any block of data. The core storage address of the first word
	of such a block is known as its FWA.
LWA	"Last word address." This term is used when reference is made
	to any block of data. The core storage address of the last word
	of such a block is known as its LWA.

# WORD FORMAT AND ARITHMETIC

The computer word contains 12 binary digits. The bits within a computer word are numbered from 0 (least-significant) to 11, starting on the right.

COMPUTER WORD:												
	11	10	09	08	07	06	05	04	03	02	01	00

All arithmetic is binary, one's complement notation. Any number may be represented as combinations of the two binary digits, 0 and 1. Although the computer operates in the <u>binary</u> system, the <u>octal</u> representation of a binary number is more convenient. The computer word can be considered as four octal digits.

EXAMPLE:	0	1	1	1	1	0	0	0	1	0	1	1
	3			6			1			3		

In one's complement notation positive numbers are represented by their binary equivalent; negative numbers are represented by the one's complement of the equivalent positive number. To form the one's complement, reverse each bit of the word.

EXAMPLE:

+5 is represented as: 000 000 000 101 -5 is represented as: 111 111 111 010

The internal arithmetic of the computer is based on subtraction. Addition is performed by subtracting the complement of the addend from the augend. In subtraction no complementing is necessary.

EXAMPLE:

The computer is programmed to add +6 to +5. This operation is performed as follows:

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 $+5 = 000 \ 000 \ 000 \ 101 \\ +6 = 000 \ 000 \ 000 \ 110 \\ and subtraction takes place, \\ +5 = 000 \ 000 \ 000 \ 101 \\ -(+6) = 111 \ 111 \ 111 \ 001 \\ Borrow(1) \ 000 \ 000 \ 001 \ 100 \\ Subtract the borrow - 1 \\ produces 000 \ 000 \ 001 \ 011 = 13_8, which is the correct answer.$ 

During the subtraction process, the borrow from the high order end was carried around and subtracted from the low order end of the word to provide the correct result. This "end-around-borrow" is the feature which makes the arithmetic of the CONTROL DATA 8090 modulus  $2^{12}$ -1.

The value zero can be represented in one's complement notation in either of two separate expressions:

000 000 000 000 (plus zero) 111 111 111 (minus zero)

Both plus and minus zero are acceptable as arithmetic operands. There are only two cases in which a zero arithmetic result will be minus zero; in all other cases result will be plus zero. These two cases are:

-0+(--0) and -0--(+0)

All positive numbers must have a zero in bit 11; all negative numbers must have a one in bit 11. As is implicit from the illustrations above, the sign bit is extended to the most significant bit of the number.

# REGISTERS

Storage units for all data transmission and computation in the computer are known as registers. Contents of the registers are displayed on the console. Those registers available to the programmer by means of computer instructions are called <u>addressable</u> registers; the others are called <u>non-addressable</u> (figure 2). All registers in the computer are 12 bits long.

## ADDRESSABLE REGISTERS

<u>A REGISTER</u>	The A register receives the results of all arithmetic, logi- cal, and shifting operations.
<u>P REGISTER</u>	The P register contains the storage address of the current instruction. At the completion of an instruction which does not require program control to jump out of sequence, the P register is advanced by 1 or 2 to select the address of the next instruction. If control is to be transferred out of se- quence the new control address is sent to the P register and the P register is not advanced.
	If the P register contains 7776 and is advanced by 1 it will contain 0000; if P contains 7777, advancing it by 1 will change the number to 0001. (See previous page.)

BUFFER<br/>ENTRANCEDuring buffered input-output operations BER holds the add-<br/>ress to, or from, which information is being transferred.REGISTER (BER)The contents of this register may be transferred to storage<br/>and to the A register.

<u>BUFFER EXIT</u> <u>REGISTER (BXR)</u> During buffered input-output operations BXR holds the last word address plus 1 to, or from, which information is being transferred.

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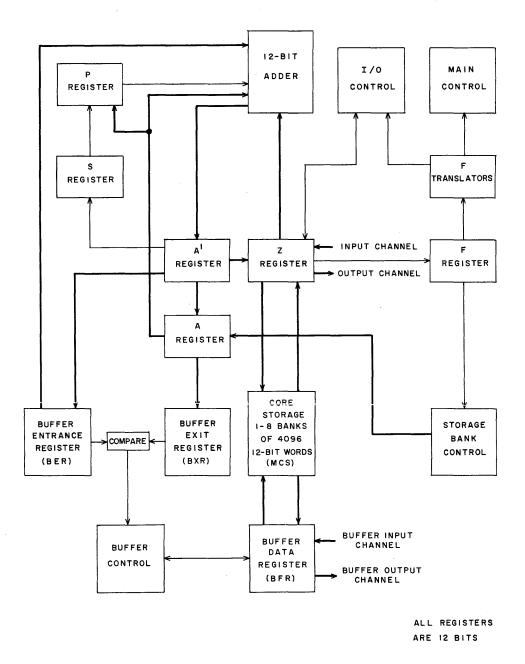


Figure 2. Block Diagram of Registers

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## NON-ADDRESSABLE REGISTERS

- ZREGISTER Z, a transient register, holds information during transfers between storage and peripheral equipment on the normal input-output channel. The Z register also restores information read out of storage.
- <u>SREGISTER</u> The S register contains the storage address currently being referenced either for an instruction or for an operand.
- <u>FREGISTER</u> The F register contains the decoded instruction being executed. The upper 6 bits contain the <u>effective</u> function code and in general, the lower 6 bits the effective E portion of the instruction.
- <u>BUFFER DATA</u> <u>REGISTER (BFR)</u> During a buffer operation BFR holds the word of information being transferred to or from storage.
- <u>A'REGISTER</u> The A' register acts as an auxiliary transmission register for information moving between the other registers. This is the output register of the adder.

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# STORAGE CONTROL

Magnetic core storage in the CONTROL DATA 8090 is composed of one, two, four, six or eight separate banks of cores. Each bank contains 4,096 12-bit words. A minimum memory contains 4,096 words and is expandable to 8,192 words; 16,384 words; 24,576 words to a total of 32,768 words. Each bank is assigned a unique number, 0 through 7, which is never changed. Associated with these banks is a set of four 3-bit registers called STORAGE BANK CONTROLS; each control may be set by a computer instruction to reference any one of the eight possible banks. Each bank has its own set of 10000g addresses numbered from 0000 to 7777. If a bank control is set so that it references a nonexistent bank, the computer will stop with a fault indication if an instruction is executed which uses that particular control.

#### **RELATIVE STORAGE BANK CONTROL (r)**

This control selects which storage bank will be referenced to obtain all instructions for execution. All instructions are executed from the bank to which the (r) control has been set. (r) also selects the bank which will be referenced by all instructions whose operation codes indicate RELATIVE or CONSTANT addressing, and as a first address for MEMORY commands (see section on addressing modes).

#### DIRECT STORAGE BANK CONTROL (d)

This control selects the storage bank referenced by all instructions having DIRECT addressing operation codes. For operation codes indicating INDIRECT addressing, (d) selects the bank used for the first direct address selection.

#### INDIRECT STORAGE BANK CONTROL (i)

For instructions with INDIRECT or MEMORY addressing operation codes, (i) selects which bank will be referenced to select the final operand. An exception is the jump instruction which cause an indirect transfer of control. JPI and JFI cause control to be transferred within (r). During NORMAL input-output operations, (i) selects the bank to or from which information will be transferred.

## BUFFER STORAGE BANK CONTROL (b)

During operations which use the BUFFER input-output channel, (b) selects the storage bank to or from which information will be transferred.

## EXAMPLE

Assume: (r) is set to reference bank 0

- (i) is set to reference bank 1
- (d) is set to reference bank 2
- (b) is not used in this example

The following conditions exist within storage:

(The bank numbers appear in parens.)

Memory Location	Contents
(1) 1577	77 1 7
(1) 2345	5757
(2) 0005	1577
(2) 0067	2345
(2) 0070	temporary storage

Since (r) is set to 0, all program steps will be executed from bank 0. An annotated program appears on following page:

LOCATION	<u>C</u> (	ONTE	<u>NTS</u>	COMMENTS
	SYMBO		NUMERIC	
(0) 0100	<u> </u>	<u>E</u> 10	2210	Load contents of (r) 0110=(0)0110 into A. Upon completion A con- tains 3333.
(0) 0101	STD	70	4070	Store contents of A in location (d) 0070 = (2) 0070. Upon comple- tion A and (2) 0070 both contain 3333.
(0) 0102	LDI	05	2105	<ul> <li>(d) 0005 = (2) 0005 contains 1577.</li> <li>(i) 1577 = (1) 1577 contains the operand 7717. 7717 is loaded into A. Upon completion A contains 7717.</li> </ul>
(0) 0103	ZJF	02	6002	lf A contains all zeros, read next instruction from (r) 0105 = (0)0105.
(0) 0104	JPI	67	7067	Jump via (d) 0067 = (2) 0067. 2345, the contents of (2) 0067 becomes (r) 2345 or (0) 2345, the address of next instruction.
(0) 0105	STB	01	4301	Store current contents of A in (r) 0104 = (0) 0104.
(0) 0106	JFI	01	7101	Jump to address specified by contents of (r) 0107 = (0) 0107. 2121, contents of (0) 0107 become (r) 2121, or (0) 2121, the address of next instruction.
(0) 0107			2121	Jump address.
(0) 0110			3333	Working constant.

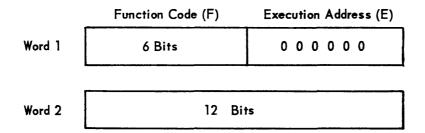
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# INSTRUCTION WORD FORMAT

The 8090 computer instruction word is divided into a 6-bit function code (F) and a 6-bit execution address (E).

Function Code (F)	Execution Address (E)
6 Bits	6 Bits

Most instructions require only one word of storage, but certain expanded instructions are available which occupy two words of storage. The format of <u>2-word</u> instructions is always as shown below; the first word contains a 6-bit function code and a 6-bit execution address. The execution address is <u>always</u> equal to zero. The second word contains a 12-bit address or operand (G), depending on the instruction. Words 1 and 2 <u>must</u> be located in sequential storage addresses of the same bank.



F (and, in some cases, E) determines which instruction in the computer repertoire will be executed. Because E contains only 6 bits it is not possible for E to specify a complete storage address in all cases. Therefore, depending on F, the computer selects, for each instruction, one of eight addressing modes.

#### NO ADDRESS MODE -- N

In the NO ADDRESS mode, E is the lower 6 bits of an implied 12-bit operand whose 6 high-order bits are always zero. Thus the E portion of the instruction word becomes the operand. Example: Location F E (r)0100 LDN 43 (r)0101 next instruction At location (r)0100 is a LOAD NO ADDRESS(LDN) instruction.

A <u>LOAD</u> instruction transmits the operand to the A register. The 12-bit operand for LDN 43 is 0043.\* Therefore the number 0043 will be transferred to the A register. At the completion of a No Address (N) instruction, control always continues at the location in the relative storage bank specified by the contents of P, plus 1. In this case control will continue at location (r)0101.

#### DIRECT ADDRESS MODE--D

In the DIRECT ADDRESS mode, E selects one of the first 77 octal locations in the direct storage bank (d) as the operand address.

Example:	Location	F	Е			
	(d)0076	12	34			
	(r )1075	LDD	76			
	(r)1076	next in	struction			
	At location (r)1075 is a LOAD DIRECT (LDD) instruction.					

E specifies that the operand address is (d)0076. This address contains the quantity 1234 which will be transferred to the A register. At the completion of a Direct Address (D) instruction, control always continues at the location in the relative storage bank specified by the contents of P, plus 1. In this case control will continue at (r)1076.

#### INDIRECT ADDRESS MODE--I

In the INDIRECT ADDRESS mode, E references one of the direct storage bank locations numbered from 01 through 77. The location (d)00E is then referenced and the contents of (d)00E become the operand address in the indirect bank (i).

Example:	Location	F	Е	
	(d)0045	33	65	
	(i)3365	46	57	
	(r )4121	LDI	45	
	(r)4122	next in	struction	
	At location	r)4121	is a LOAD	NDIRECT (LDI) instruction.

\* All numbers are in octal unless stated otherwise.

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Rev. A

E calls for a reference to (d)0045, which contains the address 3365. A final reference is now made to (i)3365, which contains the number 4657. The quantity 4657 will be transferred to the A register. Notice that both the direct (d) and indirect (i) storage bank controls are involved in the Indirect Address (I) mode. At the completion of an (I) instruction, control always continues at the location in the relative storage bank specified by the contents of P, plus 1. In the above example control will continue at (r)4122.

There are two (I) instructions which are exceptions to the above rules: JPI and FJI:

1. In the instruction JPI the initial reference is made to (d)00E. A transfer of control then takes place within the relative (r) bank to the location specified by the contents of (d)00E.

2. In the instruction JFI the initial reference is Relative Forward. A transfer of control then takes place within the relative (r) bank to the address specified in the relative forward reference.

#### RELATIVE FORWARD ADDRESS MODE -- F

In the RELATIVE FORWARD ADDRESS mode, E is added to the contents of the P register. This sum then becomes the effective operand address in the relative storage bank (r).

Example:	Location	F	E				
	(r)0233	LDF	22				
	(r)0234						
	(r)0255	77	03				
	At location	( <b>r)02</b> 33 i	is a LOAD	FORWARD (LE	OF) instruction.		

E is added to the P register to yield the address (r)0255. The contents of (r)0255 will be transferred to the A register. At the completion of this instruction A will contain the quantity 7703. At the completion of an (F) instruction which does not cause control to be transferred, control will continue in the relative storage bank (r) at the location specified by the contents of P, plus 1. In the above example, control continues at location (r)0234. Certain (F) instructions cause control to be transferred E locations forward in the relative bank (see instruction repertoire).

#### RELATIVE BACKWARD ADDRESS MODE -- B

The RELATIVE BACKWARD ADDRESS mode functions in a manner analogous to the RELATIVE FORWARD (F) mode except that E is <u>subtracted</u> from the contents of the P register to form an effective address in the relative storage bank.

#### SPECIFIC ADDRESS MODE --- S

In the SPECIFIC ADDRESS mode E is <u>always</u> equal to zero. The effective address for an (S) instruction is always storage bank zero, location 7777, (0)7777.

Example:	Location	F	Е	G
	(r)0177	LDS	00	
	(r )0200	next in:	xt instruction	
	(0)7777	43	21	

At location (r)0177 is a LOAD SPECIFIC (LDS) instruction. The fact that E equals zero is used in address decoding to specify that the address of the operand of this instruction is (0)7777. Thus the quantity 4321 will be transferred to the A register. At the completion of an (S) instruction, control continues in the relative storage bank at the location specified by the contents of P, plus 1. In the above example control continues at (r)0200.

#### CONSTANT ADDRESS MODE -- C

All CONSTANT ADDRESS mode instructions occupy two sequential storage locations wherein the G portion of the 24-bit instruction word contains the operand. E is always equal to zero.

Example:	Location	F	Е	G
	(r)0101	LDC	00	7337
	(r)0103	STC	00	2345
	(r)0105	next in	struction	2343

At location (r)0101 is a LOAD CONSTANT (LDC) instruction. The operand address is (r)0102 and the quantity 7337 is transferred to the A register. At the completion of a (C) instruction, control continues in the relative storage bank (r) at the location specified by the contents of P, plus 2. In this case, control continues at (r)0103. This address contains a STORE CONSTANT (STC) instruction. A STORE instruction caused the contents of the A register to be transferred to the operand address. In the above example, the operand address of the STC instruction is (r)0104. The quantity 7337 which was in the A register as a result of the LDC instruction in (r)0101 will be transferred to location (r)0104 and will therefore replace the constant 2345 now in (r)0104. The final contents of (r)0104 will be 7337 and control will continue at (r)0105.

## MEMORY ADDRESS MODE -- M

All MEMORY ADDRESS mode instructions occupy two sequential storage locations wherein the G portion of the 24-bit instruction word contains the address of the operand. E is always equal to zero.

Example:	Location	F	Е	G
	(r)3477	LDM	00	1111
	(r)3501	STM	00	0024
	(r)3503	next ins	struction	0024
	(i)1111 (i)0024	67 02	66 34	

At location (r)3477 is a LOAD MEMORY (LDM) instruction. The location (i)1111 becomes the operand address and the quantity 6766 is transferred to the A register. At the completion of an (M) instruction, control continues in the relative storage bank (r) at the location specified by the contents of P, plus 2. In this case, control continues at location (r)3501 which contains a STORE MEMORY (STM) instruction. The operand address of this instruction becomes (i)0024 and the quantity 6766 which was in the A register will be stored in location (i)0024, replacing the quantity 0234. Control will then continue at location (r)3503.

# INSTRUCTIONS

The following pages contain an explanation of the 8090 instructions. Note that:

1. All instruction times are in storage cycles where 1 cycle equals 6.4 microseconds.

2. All numbers are in octal notation unless otherwise stated.

3. In the description of an operation code, the operations involved are listed in sequence if more than one operation is performed.

4. Instructions which may assume more than one address mode are described under the general instruction function. The operand formation for each addressing mode is described in the section on addressing modes.

5. The G portion of an instruction is shown only with those instructions which occupy 2 words of storage and therefore have a G portion.

## 1. DATA TRANSMISSION

F	<u>E</u>	G	MNEMONIC	NAME	TIMING
01	00	YYYY	BLS	BLOCK STORE	(no jump) 1 (jump) 2

Description:	If the buffer is busy	XXXX → P
	If the buffer is not b	ousy, (A) → BFR
		(P) + 2 → P
	Start the cycle:	1. (BFR) → (b) (BER)
		(BER) + 1 → BER
	lf (BER) <i>≠</i> (	BXR), go to 1.
	lf (BER) = (	BXR), terminate buffer operation

BLS is used to set selected positions of storage to any desired value. The FWA of the area to be set is placed in BER, the LWA + 1 of the area to be set is placed in BXR. (b) is then set to reference the storage bank that is to be set. The value to which the area is to be set is placed in A and then the BLS instruction is given. If at the time a BLS instruction is given the buffer is in operation, the program jumps to (r)YYYY. If buffer is not in operation when the BLS instruction is given, the store operation takes place and control continues at (r) (P) + 2.

The BUFFER storage bank control (b) may be set at any time prior to giving the BLS instruction. Note that although BLS is a buffer operation, because of the need to constantly refer to storage for the store operation the next instruction will not be executed until the BLS instruction is completed. The total execution time for the BLS operation is 1 + N cycles, where N is the number of locations to be set, plus one.

<u>F</u>	E	MNEMONIC	NAME	TIMING
01	01	ΡΤΑ	TRANSFER P TO A	1

Description:  $(P) \rightarrow A$  $(P) + 1 \rightarrow P$ 

Transfer the contents of P to A. Control continues at (r)(P)+1. At the time PTA is executed, P will contain the address of the PTA instruction.

F	<u>E</u> <u>G</u>	MNEMONIC	NAME	TIMING
01	05 YYY	Y ATE	A TO BUFFER ENTRANCE REGISTER	(nojump) 1 (jump) 2
Des	scription:	If the buffer is bus		

Description: If the buffer is busy  $YYY \rightarrow P$ If the buffer is not busy (A)  $\rightarrow$  BER (P) + 2  $\rightarrow$  P

Transfer the contents of A to BER. Control continues at (r) (P) + 2. If the buffer is in operation when an ATE instruction is given, A is not transferred and control continues at (r) YYYY.

<u>F</u>	E	G	MNEMONIC	NAME	TIMING
01	06	YYYY	ΑΤΧ	A TO BUFFER EXIT REGISTER	(no jump) 1 (jump) 2

Description: If the buffer is busy,  $YYYY \rightarrow P$ If the buffer is not busy,  $(A) \rightarrow BXR$  $(P) + 2 \rightarrow P$ 

Transfer the contents of A to BXR. Control continues at (r) (P) + 2. If the buffer is in operation when an ATX instruction is given, A is not transferred and control continues at (r) YYYY.

F	E	MNEMONIC	NAME	TIMING
01	07	ETA	BUFFER ENTRANCE REGISTER TO A	1

Description:  $(BER) \rightarrow A$  $(P) + 1 \rightarrow P$ 

Transfer the contents of BER to A. This instruction may be given at any time, even while the buffer is in operation. Control continues at (r) (P) + 1.

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
01	30	СТА	BANK CONTROLS TO A	1
Description:		$(b) \rightarrow A_{11-9} * (d) \rightarrow A_{8-6} (i) \rightarrow A_{5-3} (r) \rightarrow A_{2-0} (P) + 1 \rightarrow P$		

Transfer the contents of the four storage bank controls to A as octal digits which occupy the A register bit positions shown above. Control continues at (r) (P)+1. Note that the storage bank controls are not changed by the execution of a CTA instruction.

EXAMPLE:	Assume	(b) is set to reference bank 4
		(d) is set to reference bank 0
		(i) is set to reference bank 1
		(r) is set to reference bank 2

Under the above conditions, if a CTA instruction were given, A would contain the number 4012 at the completion of the instruction.

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
01	5Y	STP	STORE P AT LOCATION 5Y	3
Description:		(P) → (d) 005Y (P) + 1 → P		

Transfer the contents of P to storage location (d) 005Y, where Y is any octal digit 0-7. Control continues at location (r) P + 1. This instruction allows the contents of P, which will contain the address of the STP instruction to be stored in the direct storage bank at any of the locations 0050-0057.

<sup>\*</sup> Subscripts indicate bit positions in A.

<u>F</u> .	<u>E</u>	MNEMONIC	NAME	TIMING
01 d	6Y	STE	STORE BUFFER ENTRANCE REGISTER AT LOCATION 6Y AND TRANSFER A TO BUFFER ENTRANCE REGISTER	3
Description:		(BER) → (d) 006Y (A) → BER (P) + 1 → P		

Transfer the contents of BER to storage location (d) 006Y, where Y is any octal digit 0-7, and transfer the contents of A to BER. A is unchanged by this instruction. Control continues at location (r) (P) + 1. This instruction allows the contents of BER to be exchanged whenever desired, even while the buffer is in operation. The old contents of BER will be stored in the direct storage bank (d) at any of the locations 0060-0067.

<u>F</u>	E	G	MNEMONIC	NAME	TIMING
• ·					
04	XX		LDN	LOAD NO ADDRESS	1
20	ΥY		LDD	LOAD DIRECT	2
21	00	YYYY	LDM	LOAD MEMORY	3
21	ΥY		LDI	LOAD INDIRECT	3
22	00	XXXX	LDC	LOAD CONSTANT	2
22	ΧХ		LDF	LOAD FORWARD	2
23	00		LDS	LOAD SPECIFIC	2
23	XX		LDB	LOAD BACKWARD	2

Description: operand  $\rightarrow A$ 

Transfer the operand to A. The operand in storage is not altered by the execution of a LOAD instruction. The proper operand is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions LDI, LDF, and LDB cannot be zero or the operation code is interpreted as LDM, LDC, and LDS, respectively.

F	Ē	<u>G</u>	MNEMONIC	NAME	TIMING
05 24 25 25	ΥY	YYYY	LCN LCD LCM LCI	LOAD COMPLEMENT NO ADDRESS LOAD COMPLEMENT DIRECT LOAD COMPLEMENT MEMORY LOAD COMPLEMENT INDIRECT	1 2 3 3
26	00	XXXX	LCC	LOAD COMPLEMENT CONSTANT	2
26	X X		LCF	LOAD COMPLEMENT FORWARD	2
27	00		LCS	LOAD COMPLEMENT SPECIFIC	2
27	X X		LCB	LOAD COMPLEMENT BACKWARD	2

Description: - operand  $\rightarrow A$ 

Transfer the ones complement of the operand to A. The operand in storage is not altered by the execution of a LOAD COMPLEMENT instruction. The one's complement of a number is the arithmetic negative of that number. The proper operand is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions LCI, LCF, and LCB cannot be zero or the operation code is interpreted as LCM, LCC, and LCS respectively.

<u>F</u>	Ĕ	G	MNEMONIC	NAME	TIMING
40	ΥY		STD	STORE DIRECT	3
41	00	YYYY	STM	STORE MEMORY	4
41	ΥY		STI	STORE INDIRECT	4
42	00	XXXX	STC	STORE CONSTANT	3
42	ΧХ		STF	STORE FORWARD	3
43	00		STS	STORE SPECIFIC	3
43	ΧХ		STB	STORE BACKWARD	3

Description: (A) → operand address

Transfer the contents of A to the operand address. The contents of A are not altered by a STORE instruction. The proper operand address is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions STI, STF, and STB cannot be zero or the operation code is interpreted as SFM, STC, and STS respectively.

F	E	MNEMONIC	NAME	TIMING
76	ΥY	HWI	HALF WRITE INDIRECT	4

Description:  $(A)_{L} \rightarrow \text{operand address}_{L}$ (P) + 1  $\rightarrow$  P

Transfer the E portion of A to the E portion of the operand address. A and the higher order 6 bits of the operand address are unchanged. The proper operand address is formed as described in the section on address modes. Control will continue at (r) (P) + 1.

EXAMPLE:	Location	F	E
	(r) 3777	HWI	23
	(d) 0023	41	14
	(i) 4114	75	01
	(A)	46	57

When the HWI instruction at location (r) 3777 is executed, the E portion of A will be transferred to the E portion of location (i) 4114. At the completion of the instruction A will contain the quantity 4657, location (i) 4114 will contain the quantity 7557, location (d) 0023 will be unchanged, and control will continue at location (r) 4000.

If the E portion of the HWI instruction is equal to 00 or 77, the operation code will be interpreted as INA or OTA respectively. The effective indirect address reference ranges from (d) 0001 to (d) 0076.

## 2. ARITHMETIC

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
01	12	MUT	MULTIPLY A BY 10	I
Des	cription:	10 <sub>10</sub> (A) → A (P) + 1 → P		

Multiply the contents of A by  $10_{10}$ . The result is placed in A at the completion of the instruction. For the range of numbers  $-314_8$  to  $+314_8$  the result will be algebraically correct. If (A) >  $+314_8$  or <  $-314_8$ , the result will be correct modulo  $2^{12}$ -1. Control will continue at location (r) (P)+1.

<u>_</u> F	E	MNEMONIC	NAME	TIMING
01	13	MUH	MULTIPLY A BY 100	1

Description:  $100_{10} (A) \rightarrow A$ (P)+1  $\rightarrow$  P

Multiply the contents of A by  $100_{10}$ . The result is placed in A at the completion of the instruction. For the range of numbers  $-24_8$  to  $+24_8$ , the result will be algebraically correct. If (A) >  $+24_8$  or <  $-24_8$ , the result will be correct modulo  $2^{12}$ -1. Control will continue at location (r) (P)+1.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
06	XX		ADN	ADD NO ADDRESS	1
30	ΥY		ADD	ADD DIRECT	2
31	00	YYYY	ADM	ADD MEMORY	3
31	ΥY		ADI	ADD INDIRECT	3
32	00	XXXX	ADC	ADD CONSTANT	2
32	ΧХ		ADF	ADD F ORWARD	2
33	00		ADS	ADD SPECIFIC	2
33	XX		ADB	ADD BACKWARD	2

Description: (A) + operand  $\rightarrow$  A

Form in A the sum of the original contents of A and the operand. The operand is unchanged by an ADD instruction. The proper operand is formed for each address mode and control will continue as described in the section on address modes.

Note that the E portion of the instructions ADI, ADF, and ADB cannot be zero or the operation code is interpreted as ADM, ADC, and ADS respectively.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
07 34	XX YY		SBN SBD	SUBTRACT NO ADDRESS SUBTRACT DIRECT	1 2
35	00	YYYY	SBM	SUBTRACT MEMORY	3
35 36	YY 00	xxxx	SBI SBC	SUBTRACT INDIRECT SUBTRACT CONSTANT	3 2
36 37	X X 0 0		SBF SBS	SUBTRACT FORWARD SUBTRACT SPECIFIC	2 2
37	ХΧ		SBB	SUBTRACT BACKWARD	2

Description: (A) – operand  $\rightarrow$  A

Form in A the difference between the original contents of A and the operand. The operand is unchanged by a SUBTRACT instruction. The proper operand is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions SBI, SBF, and SBB cannot be zero or the operation code is interpreted as SBM, SBC, and SBS respectively.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
50	ΥY		RÁD	REPLACE ADD DIRECT	3
51	00	YYYY	RAM	REPLACE ADD MEMORY	4
51	ΥY		RAI	REPLACE ADD INDIRECT	4
52	00	XXXX	RAC	REPLACE ADD CONSTANT	3
52	ΧХ		RAF	REPLACE ADD FORWARD	3
53	00		RAS	REPLACE ADD SPECIFIC	3
53	XX		RAB	REPLACE ADD BACKWARD	3

Description: (A) + operand → A (A) → operand address

Form in A the sum of the original contents of A and the operand and transfer this sum to the operand address. At the completion of the REPLACE ADD instruction, both the operand address and A will contain the new sum. The proper operand is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions RAI, RAF, and RAB cannot be zero or the operation code is interpreted as RAM, RAC, and RAS respectively.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING		
54	ΥY		AOD	REPLACE ADD ONE DIRECT	3		
55	00	YYYY	AOM	REPLACE ADD ONE MEMORY	4		
55	ΥY		AOI	REPLACE ADD ONE INDIRECT	4		
56	00	XXXX	AOC	REPLACE ADD ONE CONSTANT	3		
56	ХХ		AOF	REPLACE ADD ONE FORWARD	3		
57	00		AOS	REPLACE ADD ONE SPECIFIC	3		
57	ХХ		AOB	REPLACE ADD CNE BACKWARD	3		
Des	Description: operand → A (A) + 1 → A						

(A) → operand address

Form in A the sum of the operand plus one and transfer this sum to the operand address. At the completion of the REPLACE ADD ONE instruction, both the A register and the operand address will contain the original operand increased by 1. The proper operand is formed for each address mode and control continues as described in the section on address modes.

Note that the E portion of the instructions AOI, AOF, and AOB cannot be zero or the operation code is interpreted as AOM, AOC, and AOS respectively.

## 3. SHIFT

F	E	MNEMONIC	NAME	TIMING
01	02	LS1	LEFT SHIFT ONE	1
01	03	LS2	LEFT SHIFT TWO	1
01	10	LS3	LEFT SHIFT THREE	1
01	11	LS6	LEFT SHIFT SIX	1
01	14	RS1	RIGHT SHIFT ONE	1
01	15	RS2	RIGHT SHIFT TWO	1

Description:

Shift A right or left the number of bit positions specified. Control continues at (r) (P) + 1.

All left shifts in the computer are circular; bits shifted out of bit position 11 are shifted into bit position 00. From bit position 00 bits are shifted into bit position 01, etc.

EXAMPLE:	Location	F	Е
	(r) 6173	LS3	
	(A)	61	02

At location (r) 6173 is an LS3 instruction. E is not specified since all the above shift instructions use E as part of the operation code. A contains the number 6102. At the completion of the LS3 instruction A will contain the number 1026 and control will continue at (r) 6174.

All right shifts in the computer are end-of shifts; for each bit position shifted, the sign is extended and the bit in position 00 is shifted off and lost.

EXAMPLE:	Location	F	Е
	(r) 2234 (A)	RS1 40	01

At location (r) 2234 is an RS1 instruction. Again E is not specified since it is part of the operation code. A contains the number 4001. At the completion of the RS1 instruction, A will contain the number 6000 and control will continue at location (r) 2235.

F	<u>E</u>	G	MNEMONIC	NAME	TIMING
44	ΥY		SRD	SHIFT REPLACE DIRECT	3
45	00	YYYY	SRM	SHIFT REPLACE MEMORY	4
45	ΥY		SRI	SHIFT REPLACE INDIRECT	4
46	00	XXXX	SRC	SHIFT REPLACE CONSTANT	3
46	ΧХ		SRF	SHIFT REPLACE FORWARD	3
47	00		SRS	SHIFT REPLACE SPECIFIC	3
47	XX		SRB	SHIFT REPLACE BACKWARD	3

Description: operand  $\rightarrow A$ 

SHIFT A LEFT CIRCULAR 1 BIT POSITION

(A) → operand address

The operand is placed in A, shifted left one bit position (LEFT SHIFT), and the contents of A are transferred back to the operand address. The operand for each address mode is formed and control will continue as described in the section on address modes. At the completion of a SHIFT REPLACE instruction both A and the operand address will contain the shifted original operand.

Note that the E portion of the instructions SRI, SRF, and SRB cannot be zero or the operation code is interpreted as SRM, SRC, and SRS respectively.

4. LOGICAL

F	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
02	хх		L PN	LOGICAL PRODUCT NO ADDRESS	1
10	ΥY		LPD	LOGICAL PRODUCT DIRECT	2
11	00	YYYY	LPM	LOGICAL PRODUCT MEMORY	3
11	ΥY		LPI	LOGICAL PRODUCT INDIRECT	3
12	00	XXXX	LPC	LOGICAL PRODUCT CONSTANT	2
12	XX		LPF	LOGICAL PRODUCT FORWARD	2
13	00		LPS	LOGICAL PRODUCT SPECIFIC	2
13	XX		LPB	LOGICAL PRODUCT BACKWARD	2

Description:

Form in A the logical product of the operand and the original contents of A. The operand in storage is not altered by a LOGICAL PRODUCT instruction. The proper operand is formed for each address mode and control will continue as described in the section on address modes.

The LOGICAL PRODUCT of two operands is defined as follows:

operand 1 (bit value)	0 0 1 1
operand 2 (bit value)	0 1 0 1
Logical Product of 1 and 2	0 0 0 1 (bit value)

From the above definition it will be seen that, using the proper operand as a mask, selected portions of A may be cleared or retained in A.

Note that the E portion of the instructions LPI, LPF, and LPB cannot be zero or the operation code is interpreted as LPM, LPC, and LPS respectively.

<u>F</u>	Ē	<u>G</u>	MNEMONIC	NAME	TIMING
03	XX		SCN	SELECTIVE COMPLEMENT NO ADDRESS	1
14	ΥY		SCD	SELECTIVE COMPLEMENT DIRECT	2
15	00	YYYY	SCM	SELECTIVE COMPLEMENT MEMORY	3
15	ΥY		SCI	SELECTIVE COMPLEMENT INDIRECT	3
16	00	XXXX	SCC	SELECTIVE COMPLEMENT CONSTAN	т2
16	XX		SCF	SELECTIVE COMPLEMENT FORWARD	2
17	00		SCS	SELECTIVE COMPLEMENT SPECIFIC	2
17	XX		SCB	SELECTIVE COMPLEMENT BACKWAR	D 2

Description: Complement  $A^n$  where operand n = 1

Form in A the bit complement of A for each bit in the operand equal to 1. The operand in storage is not altered by the SELECTIVE COMPLEMENT instruction. The proper operand for each address mode is formed and control will continue as described in the section on address modes.

The SELECTIVE COMPLEMENT operation is defined as follows:

(A) register (bit value)	-	0	1	1
operand (bit value)		1	0	1
Final contents of the A register	0	1	1	0 (bit value)

Note that the E portion of the instructions SCI, SCF, and SCB cannot be zero or the operation code is interpreted as SCM, SCC, and SCS respectively.

# 5. STORAGE BANK CONTROL

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
00	1X		SRJ	SET RELATIVE BANK CONTROL AND JUMP	1
00	2X		SIC	SET INDIRECT BANK CONTROL	1
00	3Х		IRJ	SET INDIRECT AND RELATIVE BANK CONTROL AND JUMP	( 1
00	4X		SDC	SET DIRECT BANK CONTROL	1
00	5X		DRJ	SET DIRECT AND RELATIVE BANK CONTROL AND JUMP	1
00	6X		SID	SET INDIRECT AND DIRECT BANK CONTROL	1
00	7X		ACJ	SET DIRECT, INDIRECT, AND RELA- TIVE BANK CONTROL AND JUMP	1
01	4X		SBU	SET BUFFER BANK CONTROL	1

### Description:

Set the specified storage bank control or controls to reference bank X. For the instructions SIC, SDC, SID, and SBU, control will continue at (r) (P) + 1. The remaining instructions of this group, SRJ, IRJ, DRJ, and ACJ, are the only computer instructions which can be used to transfer program control between storage banks. It is the act of setting the RELATIVE bank control (r) which alters the bank from which the next program instruction will be taken. Whenever an instruction is given which sets (r), the next program instruction will be taken from the new (r) at the address specified by the contents of the A register. Notice from the instructions listed above that not only may (r) be set by itself but combinations of memory bank controls may be set at the same time.

### EXAMPLE:

Set (d) to reference storage bank 3 and at the same time transfer program control to storage bank 3, location 2217.

Location	F	Е	G
(r) a	LDC	00	2217
(r) a + 2	DRJ	<u>53</u>	

In the above example, the program to transfer control was not located in any specific place in the (r) bank but rather the letter "a" was used to denote that, wherever the program was placed, the next instruction would be taken from "a + 2". This 2-instruction sequence is all that is required to transfer program control and set (d) as specified. Executing the LDC instruction transfers the number 2217 to A. This number represents the jump address in the <u>new</u> relative (r) bank. The next instruction, DRJ, sets (d) to reference bank 3, sets (r) to reference bank 3, and then jumps to location 2217 (the contents of A) in bank 3.

The contents of A are not changed when the storage bank control instructions are executed.

### 6. JUMP

F	E	G	MNEMONIC	NAME	TIMING
60	хх		ZJF	ZERO JUMP FORWARD	1
61	ΧХ		NZF	NON-ZERO JUMP FORWARD	1
62	ΧХ		PJF	POSITIVE JUMP FORWARD	1
63	ΧХ		NJF	NEGATIVE JUMP FORWARD	1
64	ΧХ		ZJB	ZERO JUMP BACKWARD	1
65	ΧХ		NZB	NON-ZERO JUMP BACKWARD	1
66	ΧХ		PJB	POSITIVE JUMP BACKWARD	1
67	XX		NJB	NEGATIVE JUMP BACKWARD	1

Description:

The above instructions are conditional jump instructions; A is tested for the condition stated in the instruction. If the condition <u>is</u> met control is transferred forward or backward in the relative (r) bank XX locations as described in the section on address modes. If the condition <u>is not</u> met, control continues at location (r) (P) + 1.

The conditions for testing are:

- 1. A Zero: The contents of the A are equal to 0000, or plus zero. Minus zero is not considered equivalent to plus zero to meet the ZERO JUMP condition.
- 2. A not Zero: A contains any quantity other than 0000.
- 3. A positive: Bit 11 of A is 0.
- 4. A negative: Bit 11 of A is 1.

F	E	MNEMONIC	NAME	TIMING
70	ΥY	JPI	JUMP INDIRECT	2

**Description:**  $((d) \ 00YY) \rightarrow P$ 

Transfer program control to the location in the relative (r) bank specified by the contents of (d) 00YY.

EXAMPLE:	Location	F	E
	(r) a	JPI	43
	(d) 0043	36	62

At some location in the (r) bank is the instruction JPI 43. When this instruction is executed, since (d) 0043 contains the number 3662, program control will be transferred to location (r) 3662.

F	E	G	MNEMONIC	NAME	TIMING
71	00	YYYY	JPR	RETURN JUMP	3
Des	cript	ion: (F	<sup>2</sup> ) + 2 →(r)YYYY		

 $\frac{\text{Description:}}{\text{YYY} + 1 \rightarrow P}$ 

The contents of P are increased by 2 to give the address of the instruction following the JPR instruction. This address is transferred to location (r) XXXX. Program control is then transferred to location (r)XXXX+1.

EXAMPLE:	Location	F	Е	G	
	(r) 1173	JPR	00	2100	

At location (r) 1173 is a JPR instruction. When this instruction is executed, the number 1175 will be transferred to location (r) 2100. Program control will then continue at location (r) 2101.

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
71	ΥY	JFI	JUMP FORWARD INDIRECT	2

Description:  $(r)((P) + 00XX) \rightarrow P$ 

Transfer program control to the address in (r) specified by the contents of the storage location XX positions forward of the JFI instruction.

EXAMPLE:	Location	F	E
	(r) 5162	JFI	07
	(r) 5171	04	23

When the JFI instruction at (r) 5162 is executed, a reference is made to the location in the relative bank 0007 positions forward, location (r) 5171. This location contains the number 0423 and program control will be transferred to (r) 0423.

Note that the E portion of the JFI instruction cannot be equal to zero or the operation code will be interpreted as a JPR instruction.

### INPUT-OUTPUT

<u>_</u>	<u>E</u>	MNEMONIC	NAME	TIMING
01	04	CBC	CLEAR BUFFER CONTROLS	1

### **Description:**

Stop all buffer operations in progress and clear the buffer controls. This instruction does not clear BER, BXR, or BFR, but it stops any buffer operation in progress. If an input-output operation is stopped when some piece of unit record equipment (such as magnetic tape, punched cards, etc.) is being read or written, the buffer will disconnect from the unit but the peripheral unit will move to the end of the unit record. The remaining data will not be stored. On non-unit record peripheral equipment such as a paper tape input device, the paper tape will stop in position to read the next frame of tape and the buffer controls will be cleared.

(Paper tape is used as an example only, since the console paper tape reader, CONTROL DATA 8074/8075, cannot be read from the buffer input-output channel.)

No buffer complete (interrupt 20) is generated when the CBC instruction is executed.

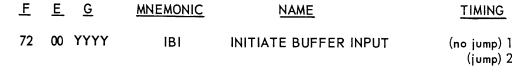
F	<u>E</u>	MNEMONIC	NAME	TIMING
01	20	CIL	CLEAR INTERRUPT LOCKOUT	1

Description:

Clear the interrupt lockout and allow any waiting interrupts to function. When the CIL instruction is executed, interrupt lockout is not cleared until the instruction following the CIL instruction has been executed. Interrupt lockout is set by any of the following:

- 1. Execution of an interrupt.
- 2. Execution of an EXF instruction.

3. Execution of an EXC instruction. (See section on interrupt.)



Description: If buffer is busy, YYYY → P If buffer is not busy, (P) + 2 → P Start input buffering operation and, when complete, generate an interrupt 20 signal.

The instruction IBI initiates an input buffer operation on the buffer inputoutput channel. Prior to an IBI instruction, however, the external device must be selected and BER, BXR, and the buffer storage bank control (b) must be set up. If the buffer is in operation when an IBI instruction is given, no buffer action will be taken and control will continue at location (r) XXXX. If the buffer is not in operation when the IBI instruction is given, the buffering operation will be started and control will immediately continue at location (r) (P) + 2. When the buffer operation terminates, an interrupt signal will appear on interrupt line 20.

<u>F</u>	<u>E</u>	G	MNEMONIC	NAME	TIMING
73	00	YYYY	IBO	INITIATE BUFFER OUTPUT	(nojump)1 (jump)2

Description: If buffer is busy, YYYY → P If buffer is not busy, (P) + 2 → P Start output buffering operation and, when complete, generate an interrupt 20 signal.

The IBO instruction initiates an output buffer operation on the buffer inputoutput channel. Prior to an IBO instruction the external device must be selected, and BER, BXR, and the buffer storage bank control (b) must be set up. If the buffer is in operation when an IBO instruction is given, no buffer action will be taken and control will continue at location (r) XXXX. If the buffer is not in operation when the IBO instruction is given, the buffering operation will be started and control will immediately continue at location (r) (P) + 2. When the buffer operation terminates, an interrupt signal will appear on interrupt line 20.

NOTE: If either of the instructions IBI or IBO is given and no external device has been selected, the computer will continue in operation but the buffer will be placed in an indefinite busy status and no input or output operation will take place. This busy status may be removed by the instruction CLEAR BUFFER CONTROLS (CBC) or by a MASTER CLEAR from the console.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
72	ХХ	YYYY	INP	NORMAL INPUT	*
73	ХХ	YYYY	OUT	NORMAL OUTPUT	*
Description: $(r)(P) + 00XX) =$ the FWA of the input or output area.					

YYYY = the LWA + 1 of the input or output area.

Read or write using the previously selected external device. The inputoutput area is defined as follows:

1. The FWA of the input-output area is found XX locations forward in the relative memory bank (r). This location (r) P+00XX, specifies a FWA in the indirect memory bank (i).

2. The LWA+1 of the input-output area is location YYYY in the indirect memory bank (i) YYYY.

<sup>\*</sup> Since INP and OUT are not buffered instructions their execution time varies with the speed of the external equipment being used.

If the external device has been properly selected, the input or output operation will take place and, at its completion, control will continue at (r)(P) + 2. If no external device has been properly selected, the computer will be indefinitely delayed, which will be indicated on the console status mode indicator.

The instruction INP and OUT are used to read or write data on the NORMAL input-output channel and are not buffered; that is, the computer will wait while the input or output operation is in progress and the next instruction will not be executed until the input-output operation is complete. The contents of A at the completion of an INP or OUT instruction will indicate the LWA + 1 actually read into or out of during the input or output operation. Although the FWA and LWA of the input-output area are found in the relative memory bank (r) they actually specify locations in the indirect memory bank (i).

EXAMPLE:	Location	F	Е	G
	(r) 1134 (r) 1136	INP	33	2000
	(r) 1130 (r) 1167	10	00	

At location (r) 1134 in a NORMAL INPUT instruction. The FWA of the input area is found in location (r) 1167 and is (i) 1000. The LWA + 1 of the input area is found in G and is (i) 2000. The LWA itself is therefore (i) 1777. Assuming an external device had been selected, the INP instruction is interpreted as "Read from selected device 1000 words and store them in the indirect storage bank starting at location 1000."

If 1000 words are read, then, at the completion of the INP instruction, A will contain the number 2000, and control will continue at location (r) 1136.\*

The E portion of the instructions INP and OUT cannot be equal to zero or the instructions are interpreted as IBI and IBO, respectively.

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If the INP instruction is terminated by an Input Disconnect, the A register will contain the address of the last word received, +2. The contents of the address of the last word received, +1, will normally be all zeros.



**Description:** 

Write, on the previously selected output device, one word with zero in the 6 high order bits and XX in the 6 low order bits. The output operation takes place under the NORMAL input-output control. At the completion of the output operation, control continues at location (r) (P) + 1. If an OTN instruction is given and no external device has been properly selected, the computer will be indefinitely delayed and will so indicate on the status mode indicator.

<u></u>	<u>E</u>	MNEMONIC	NAME	TIMING
76	00	INA	INPUT TO A	*
76	77	ΟΤΑ	OUTPUT FROM A	*

**Description:** 

Read or write, on the previously selected external device, one word to or from A. The operation takes place under NORMAL input-output control. On devices which transmit less than one full computer word at a time such as the 8074/8075 Paper Tape Readers, the information will be transmitted to and from the low order portion of A. At the completion of the operation, control continues at location (r) (P) + 1. If an INA or OTA instruction is given and no external device has been properly selected, the computer will be indefinitely delayed and will so indicate on the status mode indicator.

<sup>\*</sup> Execution time varies with the speed of the external equipment being used.

<u>F</u>	E	G	MNEMONIC	NAME	TIMING
75	00	xxxx	EXC	EXTERNAL FUNCTION CONSTANT	2
75	ΧХ		EXF	EXTERNAL FUNCTION FORWARD	2

Description:

Transmit the 12-bit operand to the external equipments. The proper operand for the various address modes is selected and control continues as described in the section on address modes. At the completion of an external function instruction, A will contain the 12-bit external function code.

The 12-bit operand to be transmitted is known as an external function code. A complete list of external function codes will be found in appendix II. The EXTERNAL FUNCTION instruction is used to select an external device to perform some specific function. With the exception of a STATUS REQUEST code, if an illegal selection is attempted the computer will be indefinitely delayed and will so indicate on the console status mode indicator. One example of an illegal selection is the attempt to select a magnetic tape for reading when the magnetic tape is turned off.

Most external devices have a STATUS REQUEST code. When such a code is given and followed with an INA instruction, a 12-bit STATUS RESPONSE code will be sent to A. By examining this response code it is possible to determine whether further selection of the equipment is possible. A STATUS REQUEST may be given even when an external device is turned off.

Only one device may be selected at any one time on each channel. Selection of any device automatically disconnects any other selected device. If a select is given and some other device on the same channel is busy, the computer will be delayed until a selection can be made. If a device is selected for some function and another select is made on the same device for some other function then the previous select is nullified. This applies to STATUS REQUEST so that, if a device was selected for reading and then status was requested of that device, another read selection must be made before any further reading can take place on that device.

## 8. STOP AND SELECTIVE STOP AND JUMP

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
00	00	ERR	ERROR STOP	1
77	00	HLT	HALT	1
77	77	HLT	HALT	1

**Description:** 

Stop computation. When the RUN switch on the console is pressed, control continues at (r) (P) + 1. When one of the stop instructions is executed and the computer stops, the letters ERR will be displayed in the status mode indicator on the console if the ERR instruction was given. There is no difference in the action of the two HLT instructions, 7700 and 7777.

<u>F</u>	<u>E</u>	MNEMONIC	NAME	TIMING
00	0X	NOP	NO OPERATION	1

**Description:** 

When a NOP instruction is executed the computer does not perform any function but passes on to the next instruction at location (r) (P)+1.

<u>F</u>	<u>E</u>	<u>G</u>	MNEMONIC	NAME	TIMING
77 77	0X X0	YYYY	SLS SLJ	SELECTIVE STOP SELECTIVE JUMP	l (no jump) l
					(jump) 2
77	XX	YYYY	SLS	SELECTIVE STOP AND JUMP	(no jump) 2 (jump) 2

### **Description:**

The selective stop and jump instructions are controlled by six switches on the computer console; STOP switches 1, 2, and 4 and JUMP switches 1, 2, and 4. a. SLS: If the appropriate STOP switch is set, stop; otherwise do not stop. If the computer stops, computation may be resumed by pressing the RUN switch on the console. Whether the computer stops or not control will continue at location (r) (P) + 1.

b. SLJ: If the appropriate JUMP switch is set, jump to location (r) YYYY; otherwise control continues at location (r) (P) + 2.

c. SJS: If the appropriate JUMP switch is set, set up to jump to location (r)YYYY; otherwise set up to continue control at (r) (P)+2. Then test the appropriate STOP switch. If the appropriate STOP switch is set, stop before executing the next instruction; control continues as selected by the jump switches. If a stop occurs, computation may be resumed by pressing the RUN switch on the console.

The values of X and the switches they control are:

X = 1	test switch 1.
X = 2	test switch 2.
X = 3	test switch 1 and 2. If either switch is set a stop or jump will be made as defined above.
X = 4	test switch 4.
X = 5	test switch 1 and 4. If either switch is set a stop or jump will be made as defined above.
X = 6	test switch 4 and 2. If either switch is set a stop or jump will be made as defined above.
X = 7	test switches 1, 2, and 4. If any are set a stop or jump will be made as defined above.

The three low order bits of the E portion of the instructions control the testing of the STOP switches and the three high order bits of E control the testing of the JUMP switches.

Any combination of X's is legal except 00 and 77 which are treated as HALT instructions (see HLT instruction).

# INTERRUPT

Certain internal and external conditions arise which make it necessary for the main program to be notified of their presence. An interrupt is the program signal which transfers computer control to some fixed location in memory without losing the information needed to return to the main program.

The 8090 has four interrupt lines; two internal, 10 and 20, and two external, 30 and 40. When an interrupt signal occurs on one of these lines and the interrupt system is not locked out, the computer stores the contents of P at location (d)0010, (d)0020, (d)0030, or (d)0040, depending on the line which generates the interrupt, and then takes its next instruction from (r)0011, (r)0021, (r)0031, or (r)0041.

### **INTERRUPT 10**

Interrupt 10 is a manual interrupt activated from the 8090 control console by momentarily pressing any combination of a Selective Stop Switch and a Selective Jump Switch. When interrupt 10 occurs, the computer stores P at location (d)0010 and transfers to (r)0011.

### **INTERRUPT 20**

The Interrupt 20 line is activated each time a buffer operation is completed or when terminated by an input disconnect. When interrupt 20 occurs, the computer stores P at location (d)0020, and transfers to (r)0021.

### **INTERRUPTS 30 AND 40**

The external interrupt lines 30 and 40 may be activated by any peripheral device designed to provide an interrupt signal. The actual meaning of these interrupts is a function of the device causing the signal. Since several devices may be connected to each line, each must be interrogated following an interrupt to determine which device generated the signal.

Interrupt signals are recognized in a priority sequence; the lower numbered lines are recognized first. If an Interrupt 10 and 20 occur simultaneously, Interrupt 10 will be recognized first. Once an interrupt signal is placed on a line it remains on the line until it is recognized or until a console Master Clear is performed.

Whenever any interrupt is recognized or whenever an external function instruction is executed all further interrupts are locked out until a clear interrupt lockout (CIL) instruction is executed. Any interrupt line which becomes active while interrupt lockout is imposed will remain active until a CIL instruction is executed, at which time all interrupt lines will be checked for activity in priority sequence.

Whenever a console Master Clear is performed, all interrupt lines are set inactive and interrupt lockout is removed.

It is possible to internally impose interrupt lockout for as long as desired by executing any external function instruction (such as a status request) and not executing a CIL instruction.

Once an interrupt has been recognized and the store P and jump executed, the programmer must have some program starting at locations (r)0011, (r)0021, (r)0031, and (r)0041, which will perform the function required by the interrupt.

### EXAMPLE 1:

Problem: Whenever an Interrupt 10 occurs, set location (i) 2100 equal to zero and return to the main program.

Location	<u>F</u>	E	G	Comments
(d) 0010				Return address put here by interrupt's JPR
(r) 0011	JFI	01		Jump to interrupt routine
(r) 0012	02	00		Interrupt routine begins at loc (r) 0200
(r) 0200	STF	05		Save A in (r) 0205
(r) 0201	LDN	00		Set A equal to zero
(r) 0202	STM		2100	Set (i) 2100 equal to zero
(r) 0204	LDC		**	Restore A
(r) 0206	CIL			Clear interrupt lockout
(r) 0207	JPI	10		Return to main program

# EXAMPLE 2:

Problem: Whenever an Interrupt 20 occurs, clear lockout and return to the main program.

<u>Location</u>	<u>F</u>	E	G	Comments
(d) 0020				Return address put here by interrupt's JPR
(r) 0021 (r) 0022		20		Clear lockout Return to main program

-----

# **INPUT - OUTPUT**

The 8090 computer has two input-output channels – the normal channel and the buffer channel. Both channels may be used simultaneously for any combination of input-output operations. An additional buffer channel is available in the 8084/8085 Auxiliary Memory Unit.

When input or output is performed on the normal channel, the computer is not free for computation but must wait until the input-output operation is completed before computing can continue. Once an input or output operation is started on the buffer channel, however, the computer is free to either continue computing or perform some other input-output operation on the normal channel.

#### NOTE

If an Input Disconnect is generated while doing a normal input (72XX) instruction, the address which would have received the next data word will contain all 0's. This applies whether the 72XX uses the normal or the buffer input cable.

No 0's are stored in this manner when doing a buffer input (7200) instruction.

If an automatic disconnect is generated by the 161 typewriter, the last data word will be followed by a location containing the carriage return code (45g), and by a second location containing all 0's.

The general procedure for performing an input-output operation is as follows:

1. Request the status of the selected unit.

2. Test the status of the unit for capability of performing the required function.

3. Select the unit to perform the input-output function.

4. Select the proper storage bank and initiate the input-output operation over the correct channel.

5. At the completion of the input-output operation request the status of the selected unit and test to verify that the input-output operation was successfully completed.

Notice that three of the above five operations are concerned with status requests. In order to allow the computer to have proper input-output control, most peripheral units are designed to transmit codes to the computer which inform the computer as to whether or not a unit can be selected and whether or not an input operation was properly completed. External function codes and status response codes are listed in appendix II. Checking status is not mandatory for input-output operations; steps 3 and 4 may be used alone. If status is not checked, however, and a selected unit is not capable of performing an input-output operation (power to the unit is off, for instance) when an external function command is given to select the unit for inputoutput, the computer will be indefinitely delayed and display SEL on the console Status Mode indicator.

Even if a unit is turned off, its status may be requested and determined.

EXAMPLE: Test the status of the input-output typewriter and, if status is OK, select the typewriter for output. (Refer to appendix II for codes.)

Location	<u>F</u>	E	G	Comments
(r) a	EXC		4240	Code 4240 requests typewriter status
(r) a + 2 (r) a + 3	INA			Read status response to A
(r) a + 3	ZJF	03		Go to select if OK
(r) a + 4	JPR		W	Return jump to subroutine to determine status trouble
(r) a + 6	EXC		4210	Select typewriter
Continue	with pr	oara	m	

Continue with program.

If the status response did not indicate that the unit was ready, JPR is executed to the subroutine starting at location (r) W to determine the exact status response code and take the necessary action. Note from the program and appendix II that a status response code of zero signifies that the typewriter is ready for input-output.

Status is also requested at the completion of an input-output operation to test for conditions which might have occurred during the operation. Not all peripheral devices have codes for such conditions (for example, the typewriter). A peripheral device such as magnetic tape, however, does check for such conditions as:

> End of file End of tape Parity errors

After an initial status check is made, the external device is selected for input or output and the correct input or output commands are given to perform the operation.

A status response code may be read using either INA or INP instruction.

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Input

After the external device has been selected for input, any combination of the following two commands is used to read the incoming information into storage:

INP - Reads from 1 to 7777 words into storage INA - Reads 1 word into A

When the INP command is used, the information will be sent to the storage bank specified by the indirect storage bank control (i).

EXAMPLE: Read 21 frames of paper tape into the area starting at (i) 2222, and then read one more frame into A.

Location	<u>F</u>	<u>E</u>	G	Comments
(r) a	EXC		4102	Select 350 paper tape reader
(r) a + 2	INP	04	2243	2243 is the LWA+1 of where information is to be stored
(r) a + 4	INA			Read one frame to A
(r) a + 5	PJF	02		Continue
(r)a + 6	22	22		2222 is the FWA of where the information is to be stored. That this location ((r) a+6) is se- lected to hold the FWA is indicated by the "04" in the E portion of the INP command at (r) a+2.

## Output

After the external device has been selected for output, any combination of the following commands is used to write the outgoing information from storage onto the selected device:

OUT - Writes from 1 to 7777 words from storage.

OTA - Writes one word from A.

- OTN Writes one word composed of 6 high order zero bits and the 6 low order bits from the E portion of the command itself.
- EXAMPLE: Punch 100 frames of paper tape from the area starting at location (i) 3200 and then punch 120 frames from the area starting at (i) 2701.

F	E	G	Comments
EXC		4104	Select the punch
OUT	05	3300	3300 is the LWA+1 of the first output area
OUT	04	3021	3021 is the LWA+1 of the second output area
PJF	03		Exit to next program step
32	00		3200 is the FWA of the first output area
) 27	01		2701 is the FWA of the second output area
	EXC OUT OUT PJF 32	EXC OUT 05 OUT 04 PJF 03	OUT         05         3300           OUT         04         3021           PJF         03         32

### BUFFER CHANNEL

Before an external device is selected for an input or output operation on the buffer channel, the following operations should be performed:

1. The buffer entrance register is loaded with the FWA of the input-output area.

2. The buffer exit register is loaded with the LWA+1 of the input-output area.

3. The proper storage bank is selected for (b).

After the above steps are completed the external device is selected and, an IBI or IBO instruction starts the buffer operation. It is possible to give the external function instruction to select the external device prior to setting up the buffer registers and (b). However, on certain external equipments such as magnetic tape, the external function instruction actually starts tape motion and the operation will not be properly completed if the correct data is not available to the tape unit at the time a data transfer request is issued by the tape unit.

If an interrupt 20 is wanted at the completion of the buffer operation, a CIL instruction must be given following the external function instruction. The execution of any external function instruction automatically sets Interrupt Lockout. If a CIL instruction is not given, all interrupts will remain on the lines and not take effect until a CIL instruction is given.

EXAMPLE: Read a message of not more than 50 characters from the input-output typewriter over the buffer channel into storage bank 3, location 3700.

Location	<u>F</u>	<u>E</u>	G	Comments
(r) a	LDC		3700	FWA of input area
(r)a + 2	ATE		a+2	Put in BER; if busy, wait
(r)a + 4	LDC		3750	LWA+lof input area
(r)a + 6	ΑΤΧ		a+6	Put in BXR; if busy, wait
(r)a + 10	SBU	3		Set (b) to 3
(r)a + 11	EXC		4240	Request typewriter status
(r)a + 13	INA			Read status
(r)a + 14	ZJF	04		Go if status OK
(r)a + 15	SBN	20		Test to see if input waiting. If yes, go ahead.
				lf no, status response indicates typewriter not ready.
(r) a + 16	SZJF	02		-
(r)a + 17	'HLT			Stop if not ready
(r)a + 20	) EXC		4220	Select typewriter input
(r) a + 22	2 CIL			Clear lockout
(r)a + 23	BI IBI		a + 23	Start buffer operation. Computer is now free to compute and will be interrupted when the buffer operation is complete.
(r) a + 2	5			Continue program while the input is in progress.

A device on the normal channel may be read or written only on the normal channel, but a device on the buffer channel may be read and written on either the normal or the buffer channel; further a device connected to the buffer channel may be only read or written on the normal channel when the buffer channel is not busy.

The 8074/8075 Paper Tape Reader and the 8073 Paper Tape Punch, which are optional equipment on the 8090, are always connected to the <u>normal</u> channel and cannot be buffered. Any other peripheral device may be connected to either the <u>normal</u> or the <u>buffer</u> channel and may be easily changed from one channel to the other by use of jumper connectors.

For the purpose of recognizing external function codes, all external devices, whether input or output, are connected to the normal channel output line. When any external equipment selection is made, all other external devices on both the normal and buffer channels are disconnected logically from the computer and must be reselected to be used. An exception occurs when a device on the normal channel is selected while the buffer channel is in operation. In this case, the normal channel selection will be made and the device on the buffer channel will not be disconnected and the buffer operation will be completed.

# 8084/8085 AUXILIARY MEMORY

The 8084/8085 Auxiliary Memory Unit connects on-line to one or two 8090 computers. The unit increases the storage capacity of the computer by 24,576 words (maximum) and provides the computers with an additional input/output buffer. This buffer, once addressed, operates independently of the computers. (Only the 8081 computer or the 8082 computer can be connected to the 8084/8085 Auxiliary Memory.)

The auxiliary memory unit makes up to five peripheral equipments and six external memory banks available to either computer. Since external buffer and memory circuits function independently, one computer can initiate an external buffer operation while the other uses an external memory module. As long as the computers select separate modules, concurrent external memory references are possible. The 8084/8085 resolves multiple requests for a single module on a word-by-word equal-share basis.

### MEMORY CHARACTERISTICS

The 8084/8085 cabinet holds one, two, or three external memory modules (figure 3). Each module has two 4,096 12-bit word banks, identical of those of the 8081/8082 internal memory. A basic 12-bit storage address designates a a word location in an internal or external bank. Storage cycle time is 6.4  $\mu$ sec.

The computer storage bank controls specify four functional banks.

relative (for instructions) direct (for constants) indirect (for operands) buffer (for internal buffered 1/0 data)

Programmed or manual bank selection by the computer determines the physical bank to be used (banks 0 and 1 in the computer, banks 2 through 7 in the Auxiliary Memory). A physical bank can represent more than one functional bank, but several physical banks cannot operate concurrently as one functional bank. For example, to have banks 2 and 4 represent the relative bank, the computer must make two bank selections, negating the first before selecting the second.

Independent storage cycles eliminate the need for synchronization between external memory modules.

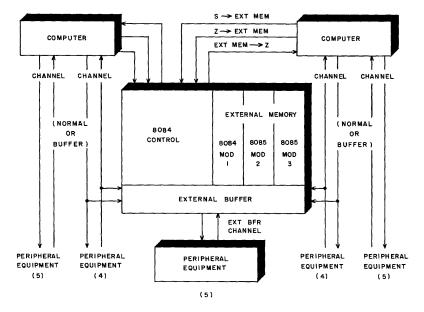


Figure 3. System Diagram

The external buffer and computers share access to each external memory module. Each module contains a scanner which continually monitors module access requests from the computers or external buffer. When it detects such a request, the scanner stops and the module storage cycle starts. During the last quarter of this cycle, the scanning resumes. One device cannot monopolize a module. If the computers and the external buffer try to make concurrent storage references in a module, the scanner allows first one, then another, and finally the third device to use the memory. In the most unfavorable case the waiting period between storage cycles cannot exceed 16  $\mu$ sec. In the most favorable case (one device continuously interrogating a particular module), the scanner cycles back during the fourth quarter of the cycle so that there is no delay between storage references.

# BUFFER CHARACTERISTICS

The external buffer is an I/O circuit that transfers information between external memory and peripheral equipment at rates up to 125 kc. This facility

increases to 14 the number of I/O devices which can be handled by the 8090 Computer System. The external buffer itself is considered an I/O device, and may be connected to either the normal or buffer channel of the computer. The decision as to channel should take into consideration the frequency with which the devices attached to the external buffer are to be selected, and whether or not direct selection of these devices by the computer (through the channel extension mode) is desired. All factors being equal, connection to the normal channel conserves program storage space.

Operation of the external buffer is independent of the computer once the buffer mode has been initiated. During this time the computer can select another equipment or perform internal computation. The computer can simultaneously perform input/output operations on the internal buffer channel, external buffer channel (via the Auxiliary Memory), and the normal I/O channel.

The external buffer may be operated in either the terminating or nontermiating mode. The terminating mode permits reading or writing in a previously designated area of external memory. After the area has been processed, the buffer operation terminates. In the nonterminating mode, a specified area of external memory may be interrogated repeatedly. This mode is useful, for example, in providing a buffer when transferring a continuous flow of data from a relatively slow input device to a fast output device. Input data is entered into computer storage via the nonterminating input buffer. When a sufficient number of words has been stored, the data is transmitted to the output device over another I/O channel. No servicing of the input buffer (via the program) is necessary once the buffer has been established.

Six external function (EF) codes permit different uses of the external buffer.

Code	Selects	Explanation
4701	Buffer mode	Data is transferred between an external module
		and a unit of peripheral equipment; rate de-
		termined by peripheral equipment.
4702	Clear buffer controls	Master clears external buffer controls
4704	Buffer entrance	This code, followed by an INA instruction,
	register (BER) read	transmits the contents of BER (last word
	•	buffered address + 1) to computer A register.
4710	Channel extension	Computer bypasses buffer circuits to com-
	mode	municate directly with peripheral equipment attached to external buffer.
4720	Clear channel	Disconnects direct communication between
	extension mode	computer and equipment attached to external
		buffer.
4740	Buffer status	This code, followed by an INA instruction,
		transmits buffer status information to com-
		puter A register.

During the buffer mode selected by code 4701, three interrupt features are available. One notifies the computer of the end of a buffer operation, the second periodically informs the computer of the progress of a nonterminating buffer, and the third interrupts the other computer.

	Computer	External Buffer
Data transfer times	One computer using one module exclusively: 6.4 µsec/word	External buffer using one module exclusively: 8 μsec/word
	Two computers sharing one module: 14.4 μsec/word maximum	One computer and ex- ternal buffer sharing one module: 16 μsec/word maximum
	Two computers and ex- ternal buffer sharing one module: 22.4 μsec/word maximum	Two computers and ex- ternal buffer sharing one module: 24 μsec/word maximum
External buffer rate	Operates at a rate of periph assuming less than 3 $\mu$ sec around delay.	neral equipment up to 125 kc, c amplifier delay and turn

TABLE 2. TECHNICAL SPECIFICATIONS.

### MEMORY SELECTIONS

The 8090 uses an external storage bank as it does an internal bank. No external function (EF) codes are needed for external memory operations.

Programmed instructions or manual selections from the 8090 console determine which banks are relative, direct, indirect, and buffer. For an external memory operation, the computer sends bank selection information to the Auxiliary Memory. If the external module containing the selected bank is busy, the computer timing chain stops at the end of its first quarter and waits a maximum of 16  $\mu$ sec. When the module becomes available, the Auxiliary Memory completes the selection and restarts the timing chain at the place where it was interrupted. Neither the stopping nor restarting of the computer timing chain is under program control.

# BUFFER SELECTIONS

An EF code selects the external buffer just as an EF code selects any other equipment on the I/O channel (table 3). Except for status or BER read information, only one computer can use the external buffer at a time. The external buffer operates in external buffer and channel extension modes. The first involves a buffered 1/O operation; the second, a direct transmission from the computer. Usually, the computer sends a status request to the Auxiliary Memory before either operation. The status request may be repeated by either computer at any time without affecting operation.

Code	Name
4701	Select External Buffer Mode
4702	Clear External Buffer Controls
4704	Select BER Read
4710	Select Channel Extension Mode
4720	Clear Channel Extension Mode
4740	Select External Buffer Status

TABLE 3. EXTERNAL BUFFER SELECT CODES

### BUFFER MODE

The computer selects the buffer mode to transfer data between the external memory and the peripheral equipment at a rate determined by the peripheral equipment. The computer sends four 12-bit control words to the Auxiliary Memory to specify the type and number of buffer operations and the external storage bank. Upon receipt of the fourth word, the Auxiliary Memory buffers data without further computer control. Both terminating and nonterminating buffer modes are possible. In the terminating mode, the buffer operation stops when the selected block of data has been transferred or when the buffer circuits are cleared by the 4702 code, IBA/OBA button, or SELECT button on the Binary Console. On the Octal Console the buffer clear switch clears the external buffer. In the nonterminating mode, the buffer continues to operate in the selected area of storage until stopped by an Input Disconnect from the peripheral equipment (input buffer), or by the 4702 code, or by manually pressing IBA/OBA button, or the SELECT button (input or output buffer).

The following general steps are used when it is desirable to perform two buffered operations simultaneously with an input/output operation on the normal channel (the order of step 1 and step 2 could be reversed):

1) Initiate operation on device connected to Internal Buffer channel.

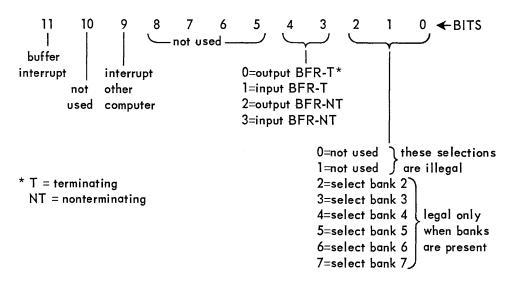
2) Initiate operation on device connected to External Buffer channel.

3) Initiate operation on device connected to the Normal channel.

Generally, for all 8090 input/output operations, the buffered operation(s) should be initiated first and the operation via the normal channel (nonbuffered) last.

### Control Words

The format for control word 1 is:



Bits 11 and 9 select external buffer interrupts. Bit 3 prepares the external buffer for an input to storage or an output from storage. Bit 4 determines whether the buffer will terminate after transferring a block of data, or continue indefinietly. Bits 2-0 select one of the six external storage banks for use by the external buffer.

Control word 2 is the starting address of the first word of the input or output data. Control word 3 is the terminating address (last word address + 1) of the input or output data. (If the starting address of a nonterminating buffer is not 0000, the first pass through storage will begin at the address specified by word 2; succeeding passes will begin at address 0000 and end at an address one less than that specified by word 3. For this reason, nonterminating buffer operations usually specify the starting address-word 2--as 0000.) Control word 4 is the EF code of the peripheral equipment.

### Modulus

The terminating buffer handles data transfers in a memory bank with modulus  $2^{12}$ -1. This characteristic is compatible with the computer, and means that any block of data extending beyond address 7776 will take 0000 (in the same bank) as its next address, thereby skipping address 7777. If the terminating address is 7777, the buffer degenerates into a nonterminating buffer with modulus  $2^{12}$ -1.

The modulus of a nonterminating buffer is variable, at the programmer's option, from modulus  $2^0$  to  $2^{12}$ , as specified by the third control word:

 $\begin{array}{rcl} 0000 &= 212 &= 4096 \\ 7777 &= 212 \\ 7776 &= 212 \\ 212 \\ 2 &= 4094 \\ & \\ & \\ & \\ 0003 &= 2^2 \\ 0002 &= 21 \\ 0002 &= 21 \\ 0001 &= 20 \\ & \\ & \\ \end{array}$ 

**Program Examples** 

These programs select the external buffer by using the normal I/O instructions of the computer rather than the buffer channel instructions. The first program transmits the control words one at a time, the second uses block transfer.

#### EXAMPLE 1

Location	F	Е	Comments
a	EXF	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read Status
a + 3	NZF	AA	Go if status OK; otherwise jump forward and examine
			status
a + 4	EXC	00	Select buffer mode
a + 5	47	01	Operand (select buffer)
a + 6	LDC	00	Load control word 1
a + 7	WX	ΥZ	Word 1 (see control words, above, for WXYZ)
a + 8	ΟΤΑ		Gate information on the output lines to external buffer
a + 9	LDC	00	Load control word 2
a + 10	SS	SS	Word 2 (address of first word of input or output data)
a + 11	ΟΤΑ		Gate information on output lines to external buffer
a + 12	LDC	00	Load control word 3
a + 13	TT	TT	Word 3 (terminating address of input or output data)
a + 14	ΟΤΑ		Gate information on the output lines to external buffer
a + 15	LDC	00	Load control word 4
a + 16	UU	UU	Word 4 (function code of peripheral equipment)
a + 17	ΟΤΑ		Gate information on the output lines to external buffer
a + 18	HLT	(or cont	tinue program)
AA	subro	utine to	examine status

#### EXAMPLE 2

Location	F	E	Comments					
a	EXC	00	Select external buffer for status					
a + 1	47	40	Operand (request buffer status)					
a + 2	INA		Read status					
a + 3	NZF	AA	Go if status OK; otherwise jump forward and examine status					
a + 4	EXC	00	Select buffer mode					
a + 5	47	01	Operand (select buffer)					
a + 6	OUT	XX	Output control words					
a + 7	ΥY	ΥY						
a + 8	HLT	(or cont	inue program) Buffer operation is now independent					
XX	FWA		•					
AA	subro	utine to	examine status					
FWA	WX	ΥZ	Control word 1					
FWA+1	SS	SS	Control word 2					
FWA+2	ΤT	TT	Control word 3					
FWA+3	UU	UU	Control word 4					
YYYY	terminating address for output instruction							

Interrupts During Buffer Mode

If bit 11 of control word 1 is a "1", the buffer returns a line 30 interrupt signal when it terminates. For a nonterminating buffer this interrupt occurs each time a buffer cycle is executed at locations  $1777_8$ ,  $3777_8$ ,  $5777_8$ , and  $7777_8$ . There are  $1024_{10}$  words between each of the above addresses.

Every interrupt sets a status bit in the external buffer so a status check can determine the source of the interrupt. When a computer selects a buffer interrupt, it has priority to use the external buffer until the status response bit, (which indicates buffer complete), clears.

For a terminating buffer operation, any Auxiliary Memory EF selection clears the buffer interrupt signal. For a nonterminating buffer operation, the periodic buffer interrupt is cleared only be reading the buffer status. For both terminating and nonterminating buffer operation, any EF selection (Auxiliary Memory), except buffer status, clears the status response bit that indicates buffer interrupt. For a nonterminating buffer, the buffer status must be read before the interrupt status bit can be cleared.

If, at any time while the buffer is inactive, bit 9 of control word 1 is a "1", a line 30 interrupt is transmitted to the other computer. An interrupt from peripheral equipment goes to both computers via the Auxiliary Memory.

Buffer interrupt or interrupt other computer should not be selected simultaneously. The IBA/OBA button, or SELECT button on the Binary Console, or the Buffer Clear switch on the Octal console, or a clear buffer controls selection by either computer, drops all interrupts and the corresponding status bits.

Program Example for Interrupting the Other Computer. This operation signals the other computer. Only bit 9 of control word 1 can be set. The control words 2, 3, and 4 are not sent, and the external buffer is cleared by the clear channel extension code.

Lo	cation	F	E	Comments					
a		EXC	00	Select external buffer for status					
a	+ 1	47	40	Operand (request buffer status)					
a	+ 2	INA		Read status					
a	+ 3	NZF	AA	Go if status OK, otherwise jump forward and examine					
				status					
a	+ 4	EXC	00	Select buffer mode					
a	+ 5	47	01	Operand (select buffer)					
a	+ 6	LDC	00	Load control word 1					
		10	00	Word 1; all bits zero except bit 9 (interrupt other					
				computer)					
a	+ 7	ΟΤΑ		Gate information on the output lines					
a	+ 8	EXC	00	Select external buffer for clear channel extension					
a	ı + <b>9</b>	47	20	Operand (select clear channel extension)					
a	+ 10	HLT	(or cont	inue program)					
A	A	subro	subroutine to examine status						

#### Clear External Buffer Controls

By executing a clear external buffer controls, either computer can clear all Auxiliary Memory selections, interrupts, and any buffering that is in process. No clear is sent to the peripheral equipment. This code should be used with caution for it clears selections by the other computer.

#### Select BER Read

The buffer entrance register (BER) read selection can be attempted at any time by either computer. The selection cannot be completed while the other computer is doing a BER read or when BER is advanced during each buffer storage cycle. The waiting periods do not affect program control. When this function code is followed by an INA instruction, the contents of BER are sent to the computer A register. If a buffer operation is in progress, the contents of BER contain the address of the next word to be buffered. If no buffer operation is in progress, the contents of BER contain the effective terminating address (last word address + 1) of the completed buffer. <u>Program Example.</u> This program uses a BER read to determine the length of an input buffer. The program does an output of the same words that were buffered in.

Location	F	Е	Comments
a	EXC	00	Clear buffer controls
a + 1	47	02	Operand (clear buffer controls)
a + 2	EXC	00	Select buffer mode
a + 3	47	01	Operand (select buffer mode)
a + 4	OUT	AA	Send control words for input buffer
a + 5		BB+4	
a + 6	EXC	00	Select buffer status
	47	40	Operand (select buffer status)
a + 7	INA	00	
a + 8	NZB	01	Wait until buffer terminates (zero status means buffer is completed)
a + 9	EXC	00	Select BER read
a + 10	47	04	Operand (select BER read)
a + 11	INA	00	Read effective terminating address of input buffer
a + 12	STF	DD+2	Place above address into output buffer control word 3
a + 13	EXC	00	Select buffer mode
a + 14	47	01	Operand (select buffer mode)
a + 15	OUT	CC	Send control words for output buffer
a + 16		DD+4	
a + 17	EXC	00	Select buffer status
a + 18	47	40	Operand (select buffer status)
a + 19	INA	00 ]	Wait until buffer terminates
a + 20	NZB	01 <b>J</b>	wall office borter refinitiates
a + 21	ZJB	a+2	Repeat program
AA		BB	Location of control word 1 for input buffer
CC		DD	Location of control word 1 for output buffer
BB	00	12	Control word 1 for input buffer (specifies bank 2)
BB+1	10	00	Control word 2 for input buffer (start at loc. 1000)
BB+2	20	00	Control word 3 for input buffer (terminate at loc. 2000)
BB+3	42	20	Control word 4 for input buffer (select typewriter input)
DD	00	02	Control word 1 for output buffer (specifies bank 2)
DD+1	10	00	Control word 2 for output buffer (start at loc. 1000)
DD+2	20	00	Control word 3 for output buffer (set by program to (BER))
DD+3	42	10	Control word 4 for output buffer (select typewriter output)

#### CHANNEL EXTENSION MODE

The EF code that selects channel extension mode connects the Auxiliary Memory I/O lines directly to the computer I/O channel. This operation bypasses all external buffer controls. The channel extension mode is cleared by the same computer selecting the buffer mode or executing the clear channel extension function. Either computer can clear the channel extension mode by selecting clear buffer controls.

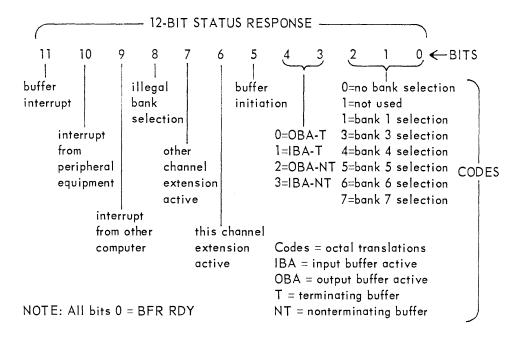
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#### Program Example

Location	F	E	Comments
a	EXC	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read status
a + 3	NZF	AA	Go if status OK, otherwise jump forward and examine
			status
a + 4	EXC	00	Select channel extension mode
a + 5	47	10	Operand (select channel extension)
a + 6	EXC	00	Select peripheral equipment for status
a + 7	UU	UU	Operand (request status of peripheral equipment)
a + 8	INA		Read status
a + 9	NZF	BB	Go if status OK, otherwise jump forward and examine
			status
a + 10	EXC	00	Select peripheral device for output
a + 11	VV	٧V	Operand (select code for peripheral equipment)
a + 12	OUT	ΥY	Transmit output data (YY starting address)
a + 13	WW	WW	(WWWW terminating address of output data)
a + 14	EXC	00	Select clear channel extension
a + 15	47	20	Operand (clear channel extension)
a + 16	HLT	or conti	nue program
AA	subro	utine to	determine cause of non-zero status response
BB			determine cause of non-zero status response
ΥY		SS	Starting address
SS	first v		output data

#### EXTERNAL BUFFER STATUS

Either computer can select status at any time. When an INA instruction follows this function code, a 12-bit status response returns to the computer. The computer subroutine that examines the status response returned by the Auxiliary Memory must check the bit positions:



The status response bits occur in combinations so that one response transmits all status information. In general, the status response bits report on control word 1 selections. Bit 5, buffer initiation, is present between the selection of the buffer mode and the function signal from the peripheral equipment which starts data buffering. If a channel extension is selected, bits 6 and 7 specify which computer made the selection. Bit 8 is a "1" when a computer internal storage bank or an external bank not in the Auxiliary Memory is selected. Bit 10 indicates interrupt conditions which did not originate in the Auxiliary Memory. All bits are zero when buffer mode and channel extension are inactive and no interrupts exist (buffer ready).

Program Example. This program examines each bit position of the 12-bit status response, starting at the left.

#### Main Program Exit-Enter Routine

Location	F	E	Comments
30	Main	program	address
31	STD	37	Save contents of A register at time of interrupt
32	JPR	00	Jump to status response routine
33	Ь		Routine location - 1
34	LDD	37	Restore (A) to value at time of interrupt
35	CIL		Clear interrupt lockout
36	JPI	30	Return to main program
37	Temp	orary st	orage for A register

# Status Response Routine

Location       F       E       Comments         b - 1       JF1       01       Re-enter above routine         b       XX       XX         b + 1       EXC       00       Select status request         b + 2       47       40       Operand (select status)         b + 3       INA       Read status         b + 4       PJF       03       If not status bit, continue routine         b + 5       JPR       00       If status bit, jump to buffer interrupt routine         b + 6       c       Routine location - 1         b + 7       LS1       Shift A left 1         b + 8       PJF       03       If no status bit, continue routine         b + 9       JPR       00       If status bit, jump to peripheral equipment interrupt routine         b + 10       d       Routine location - 1       b + 11         b + 12       PJF       03       If no status bit, continue routine         b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1       b + 15         b + 16       PJF       03       If no status bit, continue routine         .       .       .
b+1EXC 00Select status requestb+24740Operand (select status)b+3INARead statusb+4PJF03If not status bit, continue routineb+5JPR00If status bit, jump to buffer interrupt routineb+6cRoutine location - 1b+7LS1Shift A left 1b+8PJF03If no status bit, continue routineb+9JPR00If status bit, jump to peripheral equipment interrupt routineb+10dRoutine location - 1b+11LS1Shift A left 1b+12PJF03If no status bit, continue routineb+13JPR00If status bit, jump to interrupt from other computer routineb+14eRoutine location - 1b+15LS1Shift A left 1b+16PJF03If no status bit, continue routine
b+24740Operand (select status)b+3INARead statusb+4PJF03If not status bit, continue routineb+5JPR00If status bit, jump to buffer interrupt routineb+6cRoutine location - 1b+7LS1Shift A left 1b+8PJF03If no status bit, continue routineb+9JPR00If status bit, jump to peripheral equipment interrupt routineb+10dRoutine location - 1b+11LS1Shift A left 1b+12PJF03If no status bit, continue routineb+13JPR00If status bit, jump to interrupt from other computer routineb+14eRoutine location - 1b+15LS1Shift A left 1b+16PJF03If no status bit, continue routine <t< td=""></t<>
b + 3INARead statusb + 4PJF03If not status bit, continue routineb + 5JPR00If status bit, jump to buffer interrupt routineb + 6cRoutine location - 1b + 7LS1Shift A left 1b + 8PJF03If no status bit, continue routineb + 9JPR00If status bit, jump to peripheral equipment interrupt routineb + 10dRoutine location - 1b + 11LS1Shift A left 1b + 12PJF03If no status bit, continue routineb + 13JPR00If status bit, jump to interrupt from other computer routineb + 14eRoutine location - 1b + 15LS1Shift A left 1b + 16PJF03If no status bit, continue routine <tr< td=""></tr<>
b + 4       PJF       03       If not status bit, continue routine         b + 5       JPR       00       If status bit, jump to buffer interrupt routine         b + 6       c       Routine location - 1         b + 7       LS1       Shift A left 1         b + 8       PJF       03       If no status bit, continue routine         b + 9       JPR       00       If status bit, jump to peripheral equipment interrupt routine         b + 10       d       Routine location - 1       1         b + 10       d       Routine location - 1       1         b + 11       LS1       Shift A left 1       1         b + 12       PJF       03       If no status bit, continue routine       1         b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1       1         b + 15       LS1       Shift A left 1       1         b + 16       PJF       03       If no status bit, continue routine         .       .       .       .         .       .       .       .         b + 16       PJF       03       If no status bit, continue routine         .
b + 5       JPR       00       If status bit, jump to buffer interrupt routine         b + 6       c       Routine location - 1         b + 7       LS1       Shift A left 1         b + 8       PJF       03       If no status bit, continue routine         b + 9       JPR       00       If status bit, jump to peripheral equipment interrupt routine         b + 10       d       Routine location - 1       1         b + 11       LS1       Shift A left 1       1         b + 12       PJF       03       If no status bit, continue routine         b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1       1         b + 14       e       Routine location - 1       1         b + 15       LS1       Shift A left 1       1         b + 16       PJF       03       If no status bit, continue routine       .         .       .       .       .       .         .       .       .       .       .         .       .       .       .       .         .       .       .       .       .         .       .
b + 6cRoutine location - 1b + 7LS1Shift A left 1b + 8PJF03If no status bit, continue routineb + 9JPR00If status bit, jump to peripheral equipment interrupt routineb + 10dRoutine location - 1b + 11LS1Shift A left 1b + 12PJF03If no status bit, continue routineb + 13JPR00If status bit, jump to interrupt from other computer routineb + 14eRoutine location - 1b + 15LS1Shift A left 1b + 16PJF03If no status bit, continue routine<
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routine b + 10 d Routine location - 1 b + 11 LS1 Shift A left 1 b + 12 PJF 03 If no status bit, continue routine b + 13 JPR 00 If status bit, jump to interrupt from other computer routine b + 14 e Routine location - 1 b + 15 LS1 Shift A left 1 b + 16 PJF 03 If no status bit, continue routine  Check remaining 9 bit positions in same way  b + n JFI 01 Return to main program exit, enter routine
b + 10dRoutine location - 1b + 11LS1Shift A left 1b + 12PJF03If no status bit, continue routineb + 13JPR00If status bit, jump to interrupt from other computer routineb + 14eRoutine location - 1b + 15LS1Shift A left 1b + 16PJF03If no status bit, continue routine
b + 11       LS1       Shift A left 1         b + 12       PJF       03       If no status bit, continue routine         b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1         b + 15       LS1       Shift A left 1         b + 16       PJF       03       If no status bit, continue routine         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .       .       .         .
b + 12       PJF       03       If no status bit, continue routine         b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1         b + 15       LS1       Shift A left 1         b + 16       PJF       03       If no status bit, continue routine         .       .       .         .       .
b + 13       JPR       00       If status bit, jump to interrupt from other computer routine         b + 14       e       Routine location - 1         b + 15       LS1       Shift A left 1         b + 16       PJF       03       If no status bit, continue routine         .       .       .         .
routine b + 14 e Routine location - 1 b + 15 LS1 Shift A left 1 b + 16 PJF 03 If no status bit, continue routine  Check remaining 9 bit positions in same way  b + n JFI 01 Return to main program exit, enter routine
<ul> <li>b + 15 LS1 Shift A left 1</li> <li>b + 16 PJF 03 If no status bit, continue routine</li> <li>.</li> &lt;</ul>
<ul> <li>b + 16 PJF 03 If no status bit, continue routine</li> <li>.</li> <li< td=""></li<></ul>
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b + n JFI 01 Return to main program exit, enter routine
b + n JFI 01 Return to main program exit, enter routine
b - 1 c - 1 JFI 01 Re-enter status response routine
c - 1 JFI 01 Re-enter status response routine c b + 7
c + 1 Buffer interrupt routine
c + n JFI 01
c - 1 Return to status response routine
d - 1 JFI 01 Re-enter status response routine
d b + 11
d + 1 Peripheral equipment interrupt routine
d + n JFI 01
d - 1 Return to status response routine e - 1 JFI 01 Re-enter status response routine
e = b + 15

e + 1 e + n	 JFI	01	Interrupt from other computer routine		
• • •	e - 1	Return to status response	Return to status response routine		
•	•		•		
•	•		•		
•	•		•		

#### . remaining status subroutines

•	•	•
•	•	•
•	•	•

# 8074/8075 PAPER TAPE READER

#### EXTERNAL FUNCTION CODES

Code	Description
4102	Select Reader for Input

There are no status codes or responses for the reader.

#### PROGRAMMING

The 8074-A/B, C/D is a photoelectric paper tape reader that reads 5, 7, or 8 level punched paper tape at a rate of 350 (A/B) or 400 (C/D) frames per second. The 8075 is a mechanical paper tape reader that reads 5, 7, or 8 level punched tape at a rate of 120 frames per second. Functional operation of either the 8074 or the 8075 is identical, except for the noted reading rate. Since each frame of paper tape can contain a character, either 400, 350, or 120 characters per second may be read. Tape made of paper, parchment, Mylar, or Mylar-aluminum laminate is acceptable in any color and either stripes or loops of tape may be read.

The reader can be programmed to read continuously, stopping on any single character, or it can be programmed to read one character at a time and stop between each character.

The reader, which is optional equipment on the 8090 computer, is always connected to the normal input-output channel. Selection is made at the reader itself to transmit either 5,7, or 8 bits of information per frame of tape. This data enters the computer in the least significant portion of each computer word, one frame of paper tape per word, with the upper bits zero.

The only external function code for the reader is the code 4102. This code selects the reader provided it has been turned on and is in proper working order. Once the reader has been selected, it will remain selected until another external function instruction is executed.

In order to read information under program control, the reader must be selected. Then either of the instructions INP or INA may be used in any combination to transmit data from paper tape to the computer. A sample 7 level paper tape is shown in figure 4 on the following page.

Rev. E

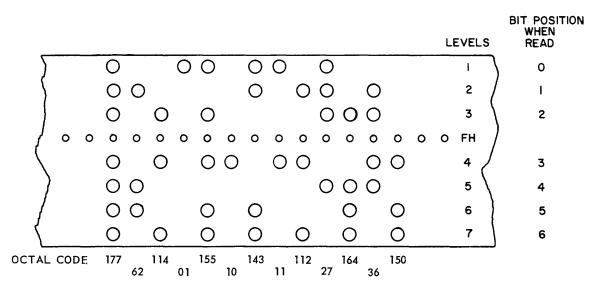


Figure 4. Punched Paper Tape Levels.

Example: Read the sample paper tape as shown in figure 4 into consecutive storage locations starting at location (i)0400. Ignore any blank leader. Stop after the last data frame (octal 150) has been read.

Location	F	<u>E</u>	<u>G</u>	Comments
(r)u	CXC		4102	Select reader
(r)a+2	INA			Read one frame
(r)a+3	ZJB	01		If frame is part of blank reader, go back
(r)a+4	STM		0400	Store data starting at (i)0400
(r)a+6	AOB	01		Increase store address
(r)a+7	INA			Read next frame
(r)a+10	NZB	04		lf data, go to store
(r)a+11	HLT			End of data-stop

When the example above has been executed using the paper tape shown in figure 4, the data read will appear as follows in storage:

Location	<u>F</u>	E	Location	<u>F</u>	E
(i)0400	01	77	(i)0407	00	11
(i)0401	00	62	(i)0410	01	12
(i)0402	01	14	(i)0411	00	27
(i)0403	00	01	(i)0412	01	64
(í)0404	01	55	(i)0413	00	36
(i)0405	00	10	(i)0414	01	50
(i)0406	01	43			

#### MACHINE LOAD FORMAT

The computer has special circuits which allow automatic loading of programs and data from specially prepared paper tapes. The information is prepared on paper tape in a two-frame-per-word format. The first frame of each word contains a 7th level punch and the six higher order bits of the word; the second frame contains the six lower order bits of the word and no 7th level punch.

Successive words must follow each other on tape. The automatic load will stop when a frame is read which should contain a 7th level punch and none exists. Tape may be placed in the reader any place on the leader; the automatic load will not begin until the first 7th level punch is sensed. Prior to starting automatic load, the FWA where the data is to be stored must be placed in P, and A should be cleared. When the load is completed P will contain the LWA where data was stored and A will contain a check sum of the data read, mod 2<sup>12</sup>-1.

Example: If the paper tape shown in figure 4 had been read under machine load control and P had been set initially to zero, at the completion of the load memory the data would appear as follows:

Location	두	E	Location F E
(r)0000	77	62	(r)0004 12 27
(r)0001	14	01	(r)0005 64 36
(r)0002	55	10	(r)0006 50 00
(r)0003	43	11	STOP LOAD

......

# **8073 PAPER TAPE PUNCH**

#### EXTERNAL FUNCTION CODES Code Description 4104 Select Punch

#### PROGRAMMING

The 8073 Punch will punch 5,6,7, or 8 level punched paper tape at a rate of 63.3 frames per second. This punch is always connected to the NORMAL input-output channel and is optional equipment on the 8090.

Each computer word transmitted to the punch causes one frame of paper tape to be punched. The 8 bits which will be punched are taken from the least significant portion of the word. A "one" bit causes a hole to be punched in the corresponding channel; a "zero" bit leaves the corresponding channel blank. The upper bits of the word are ignored.

The only external function code for the punch is the code 4104. This code selects the punch provided it has been turned on and is in proper working order. Once the punch has been selected, it will remain selected until another external function command is executed.

In order to punch information the punch must first be selected. Then any combination or the commands OTN, OTA, or OUT may be used to transmit data to the punch.

Example: Punch out locations (i)0100 to (i)0200 in machine load format (see Reader Programming). Punch a one foot leader before and after the machine load data.

Location (r)a-1 (r)a+1 (r)a+3 (r)a+4 (r)a+5 (r)a+6 (r)a+10	F EXC LDC OTN SBN NZB STM LDC	<u>E</u> 00 01 02	<u>G</u> 4104 0144 0072 0100	<u>Comments</u> Select punch No. frames for leader Punch a blank frame Con — 1 = Con If count not zero, punch more Store
(r)a+12	STD	70		FWA of punch area
(r)a+13	LDI	70		((i)0100) to A
(r)a+14	STD	71		Put lower half in (d)0071
(r)a+15	LPC	01	7700	Clear lower
(r)a+17 (r)a+20		01		Add 1 for 7th level Shift 6
(r)a+20 (r)a+21	LS6 OTA			Output upper
(r)a+21 (r)a+22	LDD	71		l ower half
(r)a+22 (r)a+23	LPN	77		
(r)a+23 (r)a+24	OTA	//		
(r)a+24 (r)a+25	AOD	70		FWA + ]
(r)a+26	SBC	, 0	0201	Test for end
(r)a+30	NZB	15	0201	Go back if not end
(r)a+31	LDB	27		No. frames for leader
(r)a+32	OTN	00		
(r)a+33	SBN	01		
(r)a+34	NZB	02		Punch leader loop
(r)a+35	HLT			· · · · · · · · · · · · · · · · · · ·
· · ·				

End of example.

# 8083 ARITHMETIC UNIT

The 8083 Arithmetic Unit extends the arithmetic capabilities of the computer. It can perform the following operations with positive operands sent to it from the computer.

Divide	Divide 54 bits by 27 bits
Multiply	Multiply two 27-bit numbers
A dd	Add two 27-bit numbers
Subtract	Subtract a 27-bit number from another
Shift Left	Shift the operand k binary places left (end-around)
Shift right	Shift the operand k binary places right (end-off)
Normalize and	Shift the operand left until the most significant bit is a
Count	"1"; record the number of shifts necessary to accomplish
	this.

#### OPERATION

The 8083 is selected and directed by computer external function codes. The unit is loaded by a computer output instruction and unloaded by a computer input instruction. The computer status request is answered by five status responses which indicate the condition of the unit. The Unit Ready (0000) will be present until the load operation is complete. At this time Busy Computing (0040) will be present until the unload phase is reached. Then Unload Not Completed (0020) will be present until all words are received by the computer or a new operation is requested.

Reselect is used if another external equipment has been selected prior to receiving the result of a selected 8083 operation. Any 33XX select code (with the exception of the status request) clears all 8083 registers; the reselect code does not. Reselect does not set up data processing circuits, therefore it cannot be used to initially select the unit.

A divide fault occurs when the divisor is equal to or smaller than the most significant 27 bits of the dividend.

### EXTERNAL FUNCTION CODES

Divide	3300	Divide Result	3314
Multiply	3301	Multiply Result	3315
Left Shift	3302	Left Shift Result	3316
Right Shift	3303	Right Shift Result	3317
Status Request	3304	Add to Result	3335
Reselect	3310	Normalize Result	
		and Count	3356
Addition	3321	Subtract from Result	3375
Normalize Count	4342		
Subtraction	3361		

## STATUS RESPONSE CODES

Unit Ready	0000
Overflow	0010
Unload Not Completed	0020
Busy Computing	0040
Divide Fault	4000

	Function Ready	80.07
COMPUTER	12-Bit Function Code (3301)	8083
	Output Resume	
	Information Ready	
	12-Bit Data Word (least sig. word of multiplier)	
	Output Resume	
	Information Ready	
	12-Bit Data Word (next sig. word of multiplier)	
	Output Resume	
	Information Ready	
	12-Bit Data Word (most sig. 3 bits of multiplier)	
	Output Resume	
	Information Ready	
	12-Bit Data Word (least sig. word of multiplicand)	1
	Output Resume	
	Information Ready	1
	12-Bit Data Word (next sig. word of Multiplicand)	
	Output Resume	
	Information Ready	
	12-Bit Data Word (most sig. 3 bits of multiplicand)	
	Output Resume	
	Input Request	]
	Input Ready	
	12-Bit Data Word (least sig. word of product)	
	Input Request	
	Input Ready	
	12-Bit Data Word (next sig. word of product)	
	Input Request	
	Input Ready	
	12-Bit Data Word (next sig. 3 bits of product)	
	Input Request	
	Input Ready	
	12-Bit Data Word (next sig. word of product)	1
	Input Request	
	Input Ready	
	12-Bit Data Word (next sig. word of product)	1
	Input Request	
	Input Ready	
	12-Bit Data Word (most sig. 3 bits of product)	-
	Input Disconnect*	
L		

\* Sent to computer if additional Input Request is received by 8083.

Figure 5. Control Signal Interplay (Multiply Instruction)

#### TABLE 4. ORDER OF LOAD AND UNLOAD\*

#### Load

#### DIVIDE

- least significant word of the dividend
   next significant word of the dividend
   next significant word of the dividend (bits 0, 1, 2)
   next significant word of the dividend
   next significant word of the dividend
   most significant word of the dividend (bits 0, 1, 2)
   least significant word of the divisor
   next significant word of the divisor
- 9 most significant word of the divisor (bits 0, 1, 2)

# MULTIPLY

1	least significant word of the multiplier	least significant word of the product
2	next significant word of the multiplier	next significant word of the product
3	most significant word of the multiplier (bits 0, 1, 2)	next significant word of the product (bits 0, 1, 2)
4	least significant word of the multiplicand	next significant word of the product
5	next significant word of the multiplicand	next significant word of the product
6	most significant word of the multiplicand (bits 0, 1, 2)	most significant word of the product (bits 0, 1, 2)

\* Timing is in table 5.

Unload

most significant word of the quotient (bits 0, 1, 2)

most significant word of the remainder (bits 0, 1, 2)

least significant word of the quotient

least significant word of the remainder

next significant word of the remainder

next significant word of the quotient

٠,

#### ORDER OF LOAD AND UNLOAD (CONT'D)\*

#### Load

#### Unload

#### ADDITION

least significant word of the augend
 next significant word of the augend
 most significant word of the augend (bits 0, 1, 2)
 least significant word of the addend
 next significant word of the addend
 most significant word of the addend (bits 0, 1, 2)

#### SUBTRACTION

least significant word of the minuend
 next significant word of the minuend
 most significant word of the minuend (bits 0, 1, 2)
 least significant word of the subtrahend
 next significant word of the subtrahend
 most significant word of the subtrahend

#### SHIFTS

least significant word of the operand
 next significant word of the operand

3 most significant word of the operand (bits 0, 1, 2) and, in shift left or right, the shift count (bits 3-7)

\* Timing is in table 5.

next significant word of the result most significant word of the result (bits 0, 1, 2) sign bit 3

least significant word of the result

least significant word of the result next significant word of the result most significant word of the result (bits 0, 1, 2) sign bit 3

least significant word of the result next significant word of the result most significant word of the result (bits 0, 1, 2) and, in normalize and count the count (bits 6-10)

Operation	Multiply	Divide	Add/Subtract	Shifts
Function Ready	3	3	3	3
Load*				
word 1	3	3	3	3
word 2	3	3	3	3 3 3
word 3	3 3 3 3 3	3 3 3 3 3 3 3 3 3 3 3 3 3	3 3 3 3 3 3 3	3
word 4	3	3	3	
word 5	3	3	3	
word 6	3	3	3	
word 7		3		
word 8		3		
word 9		3		
Compute**	41	45 - 110	2	1.6k***
Unload*				
word 1	3	3	3	3
word 2	3	3	3 3 3	3 3 3
word 3	3	3	3	3
word 4	3	3		
word 5	3 3 3 3 3 3 3	3 3 3 3 3 3 3		
word 6	1			
8083 TOTAL	80	93 - 158	32	21+1.6k
COMPUTER†	200	257	173	119
TOTAL <sup>††</sup>	280	350 - 420	205	140+1.6k

TABLE 5. 8083 AND COMPUTER TIME (IN  $\mu$ SEC)

- \* Between each word of the load and unload process, the computer can perform other operations. To return to the next word, reselect if another device has been selected. If not, continue with next word transfer.
- \*\* Computer is free to proceed with other operations.
- \*\*\* k is the number of binary positions the operand is to be shifted.
- t Computer input/output times.
- †† Includes obtaining the operands from computer memory, delivering them to the 8083, performing the desired operation, and storing the result in computer memory.

# 8071/8072 MAGNETIC TAPE SYNCHRONIZER

The 8071 and 8072 Magnetic Tape Synchronizers are input/output devices for the CONTROL DATA 8090 Computer System. The 8071 allows the computer to communicate with up to four CONTROL DATA 603 Magnetic Tape Handlers. The 8072 allows the computer to communicate with up to eight CONTROL DATA 606 Magnetic Tape Handlers. Both synchronizers also\_provide communication channels between one tape handler and a CONTROL DATA 166-2 Line Printer.

Computer-tape handler operation (on-line) is selected by computer EF codes. The EF codes control the following functions:

- Preliminary selection system tape handler word length parity density
- 2) Motion control

backspace one record search backward to file mark search forward to file mark rewind rewind unload

3) Information transfer write write file mark read status Line printer-tape handler operation (simultaneous off-line) is selected by pseudo EF codes generated by the printer select switches. The pseudo EF codes select the following functions:

1) Motion control

backspace one record search backward to file mark search forward to file mark

2) Information transfer read

The on-line and simultaneous off-line circuits permit several system configurations. Two examples of maximum configurations are:

- Tape handler A writing from computer (on-line) Tape handler B reading to printer (simultaneous off-line) Other tape handlers standing by, rewinding, or searching
- Tape handler A reading to computer (on-line) Tape handler B reading to printer (simultaneous off-line) Other tape handlers standing by, rewinding, or searching

# TABLE 6. TAPE SYNCHRONIZER EXTERNAL FUNCTION CODES AND STATUS RESPONSES

EXTERNAL FUNCTION CODES				
CODE	COMPUTER INSTRUCTION	FUNCTION		
Y11X Y11X Y12X Y12X Y13X Y13X Y13X Y14X Y15X Y16X Y171 Y172 210X 110X	OUT (no OUT) INA (no INA) INP (no INP)	Write Write end of file mark Backspace tape one record Search backward to file mark Read Search forward to file mark Status request Rewind unload Rewind load Odd parity (binary) Even parity (binary coded decimal) High density Low density		
Y = 1: 6-bit mode Y = 2: 12-bit mode X = (0 to 7): designates one of the four (eight) 60X's				

STATUS RESPONSES		
0000	Odd parity selected - no errors	
0001	Even parity selected - no errors	
0002	Selected 60X not ready	
0004	Parity error	
0015	Illegal BCD detected on Write	
0020	End of file read	
0040	End of tape or Load point sensed	
0100	High density	
0200	Selected 60X busy	

NOTE: Master bits 12, 13 or 22, 23 are used for second and third 8071/72. Programmer consideration: 6-bit, high density, mode illegal for 8072.

#### TABLE 7. FUNCTIONAL DESCRIPTION

#### ON-LINE PRELIMINARY SELECTIONS

SYSTEM TAPE HANDLER, WORD LENGTH	Selected by the initial EF code Y1nX (Y1 = system, Y = word length, X = tape handler) (Y = 1 or 2, X = 0 through 7).
PARITY	Select by a Y17X code (Y = 1 or 2, X = parity [ 1 - odd, 2 - even ] ).
DENSITY	Selected by a Y10X code (Y = density [1-low, 2- high], X = tape handler.)

ON-LINE MOTION CONTROL

BACKSPACE ONE RECORD	Initiated by the select code Y12X (Y = word length, X = tape handler) and an INA instruction.
	The Synchronizer signals the tape handler to start reverse tape motion. Motion continues automatically until the tape handler recognizes and end of record gap. Motion then stops and the tape handler and the Synchronizer are cleared for future operation.
SEARCH BACKWARD TO FILE MARK	Initiated by the select code Y12X (Y = word length, $X = tape handler$ ) and no INA instruction.
	The Synchronizer signals the tape handler to start reverse tape motion and to ignore end of record gaps. Tape motion continues automatically until a file mark (178 BCD) is sensed. Once the Synchronizer has signalled the tape handler, it is available for oper- ation with other tape handlers. When the initial tape handler has sensed the file mark, it is available for other operation.
SEARCH FORWARD TO FILE MARK	Initiated by the select code Y13X (Y = word length, X = tape handler) and no INP instruction.
	Same as search backward except for tape motion direction.
REWIND	Initiated by the select code Y16X (Y = word length, X = tape handler.)

# ON-LINE MOTION CONTROL (Cont'd)

REWIND (Cont'd)	The Synchronizer sends the rewind signal to the tape handler which starts high-speed reverse tape motion. The Synchronizer is then available for oper- ation with other tape handlers. Motion continues in the initial tape handler until the load point is sensed. The tape handler is then available for new operation using forward motion.
R EWIND UNLOAD	Initiated by the select code Y15X (Y = word length, X = tape handler). Similar to a rewind operation except that the tape does not stop at load point, but is completely un- loaded from the reel. Further operation necessitates manual reloading.

## ON-LINE INFORMATION TRANSFER

WRITE	Initiated by the select code Y11X (Y = word length, X = tape handler) and an OUT instruction.
	The Synchronizer signals the tape handler to start forward tape motion. After a delay equal to the time required to move the tape three-fourths of an inch (record gap), the Synchronizer receives a 12-bit com- puter output word.
	If the assembly mode (12-bit word length) is selected, the Synchronizer disassembles the computer word into two 6-bit words, generates a parity bit for each word, and passes them (highest order word first) to the tape handler.
	If the character mode (6-bit word length) is selected, the Synchronizer takes the lowets order 6-bits of the computer word, generates a parity bit for it, and passes it to the tape handler.
	The tape handler writes each word it receives from the Synchronizer as a seven channel frame.

WRITE (Cont'd)	<ul> <li>Operation continues as long as the computer sends output words to the Synchronizer. When output ceases the Synchronizer generates the following: <ol> <li>Check character gap (duration to move the tape the equivalent of three frames).</li> <li>Check character (longitudinal parity bit for each channel). The check character is passed to the tape handler to be recorded.</li> </ol> </li> </ul>
	Each recorded frame is read back to the Synchronizer and checked for horizontal parity error. These read- back circuits (write reply) activate the end of record circuits when they sense an end of record gap. At that time a check is made on the write reply longitu- dinal parity character. The end of record circuits ter- minate operation and clear the tape handler and the Synchronizer for future operation.
WRITE FILE MARK	Initiated by the select code Y11X (Y = word length, X = tape handler) and no OUT instruction.
	The Synchronizer signals the tape handler to start tape motion and, after a delay equal to the time required to move the tape six inches, sends the file mark to the handler. The file mark $(17_8)$ is written as if it were a one-frame record of BCD information, i.e., data is recorded, a check character gap is left on the tape, and the check character is recorded. When the end of record gap is sensed by the write reply circuit, operation is terminated and the units are cleared for future operation.
READ	Initiated by the select code Y12X(Y = word length, X = tape handler) and an INP instruction.
	The Synchronizer signals the tape handler to start tape motion. The tape handler read heads sense each frame of recorded data and transfers the frame (seven bits) to the Sychronizer.
	If the assembly mode (12-bit word length) is selected, the Synchronizer assembles each two successive 6-bit words into a 12-bit input word (first word - highest order).

ON-LINE INFORMATION TRANSFER (Cont'd)

ON LINE	INFORMATION	TRANSFER	(Cont'd)
---------	-------------	----------	----------

READ (Cont'd)	If the character mode (6-bit word length) is selected, the Synchronizer assembles each 6-bit tape handler word into the lowest order of a 12-bit input word (upper six bits all ''0's'').
	As each tape handler word passes through the Syn- chronizer, a new parity bit is generated for each six bits of data and compared to the recorded parity bit. If they differ, an indicator lights.
	When the end of record is sensed, the longitudinal parity check character is inspected for error, the operation is terminated, and the units are cleared for future operation.
	Tape motion continues until the end of record is sensed, even if the computer stops requesting input. Data, however, is not passed to the computer.
STATUS	Initiated by the select code Y14X (Y = word length, X = tape handler). Completed at any later time by an INA instruction.
	Circuits are enabled in the Synchronizer which gener- ate a pseudo input word. The word reflects conditions existing in the tape handler and the Synchronizer. The computer receives the input word when an INA instruction is sent to the Synchronizer. Translations of the status response word are shown in table 1.

#### OFF-LINE RECORDING MODE

TAPE HANDLER	Selected by manually setting Tape Handler Select switch to "1".
PARITY	Selected by manually setting the Binary/Coded switch on the Synchronizer.
DENSITY	Selected by manually setting the Density switch on the tape handler.
WORD LENGTH	Always 12-bit.

OFF-LINE MOTION CONTROL	
SEARCH FORWARD TO FILE MARK	Initiated by pressing the following printer switches: Tape/Print <u>Tape</u> /Card <u>Master Clear</u> (Press and hold before pressing Step or Continuous; continue holding until motion stops.) <u>Step</u> or <u>Continuous</u>
	The tape moves forward until a file mark is sensed.
BACKSPACE ONE WORD	Initiated by pressing the following printer switches: Tape/Print <u>Tape</u> /Card <u>Backspace</u>
	The tape moves backward until a record gap is sensed.
SEARCH BACKWARD TO FILE MARK	Initiated by pressing the following printer switches: Tape/Print Tape/Card Master Clear (Press and hold before pressing the Backspace switch; continue holding until motion stops.) Backspace
	The tape moves backward until a file mark is sensed.

## OFF-LINE INFORMATION TRANSFER

READ	Initiated by pressing the following printer switches: Tape/Print Tape/Card Step or Continuous
	The Synchronizer assembles each two successive tape handler words into a 12-bit input word (first word - highest order). The 12-bit word is sent to the printer after each of its 6-bit words is checked for parity error. If the tape comes to an end of record, operation stops. If the printer Stop switch is pressed during operation, information transfer stops but tape motion continues until the end of record is sensed.

# CONSOLE

Two types of control consoles – Binary or Octal – are available with the 8090 System. The controls necessary to operate the 8090 System are duplicated on the Binary and Octal consoles, and identical system operation is possible from either one.

#### COMPUTER

#### Computer Register Display

The three register displays on the Binary console are composed of switch – indicators (see figure 6) which serve doubly as a switch for entering information directly into the chosen register and as an indicator of the register content. All information is displayed in binary.

The three register displays on the Octal console are composed of window displays which display all information in octal using arabic numerals. Below each 12-bit register display are 13 miniature push buttons which are used to enter information into the register (see figure 7). The push buttons corresponding to the 12 bits also light.

The three 12-bit register display on both consoles are capable of displaying the contents of nine 8090 registers. On the switch panel beneath each register is a three-position lever switch which determines the particular register to be displayed. The only registers which can be entered or cleared are the P, A, and Z registers. The rightmost button in each group clears the register.

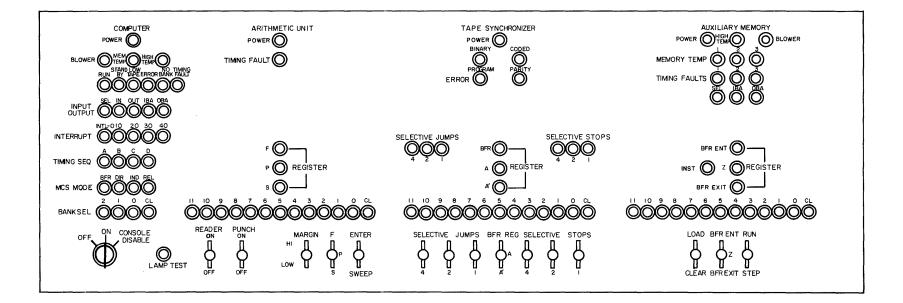


Figure 6. Binary Console Panel

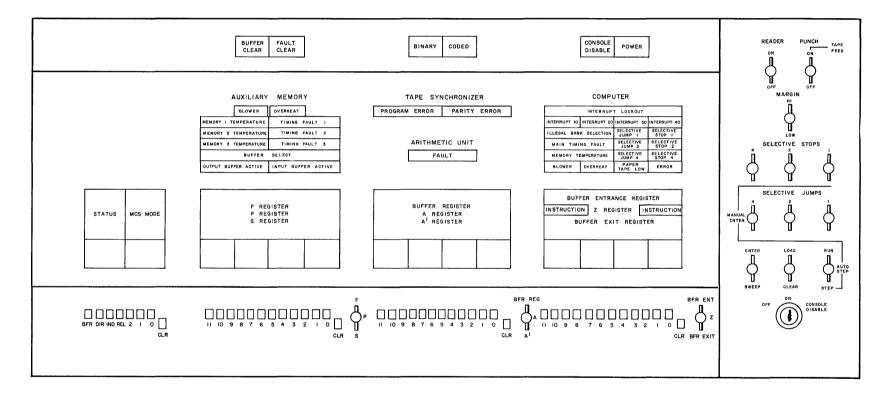


Figure 7. Octal Console Panel

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# P Register Group

F Register	Indicates the current effective function code.
P Register	Indicates the address of the current instruction.
S Register	Indicates the address of the word about to be transfered to or from storage.
A Register Group	
BFR	Indicates the last word processed during the last buffer operation.
A Register	Indicates the current contents of the A register.
A' Register	Indicates the result of the last operation in the adder.
Z Register Group	
BER	Indicates the address of the last word transferred on the buffer channel.
Z Register	Indicates the current contents of the Z register.
BXR	Indicates the LWA + 1 of the last buffer opera- tion.

## Operational Displays

Additional displays and switches provide information concerning 8090 computer performance.

Power	Indicates power to the computer unit is on.
Blower	Indicates computer cabinet blower is not opera- ting.
High Temp. (Binary) Overhead (Octal)	Indicates temperature of computer cabinet is reaching a dangerous level.
Standby	Indicates Run-Switch is cleared.

Low Tape	Indicates paper tape punch is low on tape.
Error	Indicates the computer has executed an ERR instruction and is stopped.
No Bank (Binary) Illegal Bank Selection (Octal)	Indicates a nonexistent storage bank reference, normally a programming error.
Fault (Binary) Main Timing Fault (Octal)	Indicates a main timing fault in the computer. Occurs when the computer is first turned on and can be cleared by performing a console Master Clear. If this condition appears at any other time and cannot be cleared, call Maintenance.

#### Input/Output Displays

The following conditions are displayed by means of indicators on the Binary console, and are displayed within the Status window on the Octal console.

SEL	Displayed each time an EXF or EXC instruction is executed and will remain displayed until the selection is completed. A constant display of SEL with no apparent input-output action usually indicates that the computer has attempted an nonexistent equipment selection.
IN	Displayed during all normal input operations. A constant display of IN with no apparent input action usually indicates that input was attempted without proper function selection. IN is also displayed when the computer is waiting for an external device to supply data, for instance, while data is being entered at the keyboard when typewriter input is requested.
OUT	Displayed during all normal output operations. A constant display of OUT with no apparent output action usually indicates that output was attempt- ed without proper function selection.
IBA	Displayed during all buffer input operations. See IN for additional comments.

OBA	Displayed	during	all	buffer	output	operations.
	See OUT f	or addit	iona	l comm	ents.	

Interrupt Displays

INTL – O	Indicates that an interrupt lockout has been imposed.
10	Indicates manual interrupt 10 is present.
20	Indicates buffer interrupt 20 is present.
30	Indicates external interrupt 30 is present.
40	Indicates external interrupt 40 is present.

Timing Sequence Displays

The following conditions are displayed by means of indicators in the Binary console, and are displayed within the status window on the Octal console.

A, B, C, or D Indicates which storage reference cycle will be executed at the next operation of the Run-Step switch. When a Master Clear is performed, D is displayed indicating that the next operation to be executed when the Run-Step switch is operated will be to fetch the instruction from relative storage bank (r), at the address indicated by the P register.

<u>MCS Mode and Bank Select</u>. The MCS Mode and Bank Select indicator and switches display the storage bank number to which each of the four 8090 storage bank controls have been set. This condition is displayed by means of indicators on the Binary console, and are displayed within the MCS Mode window on the Octal Panel. The alphabetic display indicates the following:

REL	Relative storage bank control (r).
IND	Indirect storage bank control (i).
DIR	Direct storage bank control (d).
BFR	Buffer storage bank control (b).

The lower display will contain one of the digits 0 through 7.

Normally the storage bank to be used with the next storage reference is displayed. However, any of the other controls may be temporarily displayed by pressing one of the four buttons in the MCS mode indicator: BFR, DIR, IND, REL. The Bank Select row of four buttons is used to set any of the storage bank controls from the console as follows:

The rightmost button (white) is a clear button which sets the bank number to zero; the other three buttons control the binary value of the bank number.

- 1) Press the button on the upper row corresponding to the bank control to be set. Hold this button down while performing the remaining steps.
- 2) Press the white clear button on the lower row and then release it. This will set the bank number to zero.
- 3) Enter the bank number into bank control by pressing the correct lower buttons. For instance, buttons 1 and 2 set the bank number to 6.
- 4) Release all buttons.

The relative storage bank control is set to zero when a console Master Clear is performed, but the direct, indirect, and buffer storage bank controls are unaltered.

#### The Switch Panel

OFF-ON-Console Disable	This switch turns power on the Computer, Tape Synchronizer, Arithmetic, and Auxiliary Memory. The Console Disable position disconnects the console from the equipment.
Lamp Test	Turns on all indicators on the console.
Reader ON-OFF	Turns Power On to the paper tape reader.
Punch ON-OFF	Turns Power On to the paper tape punch.
Margin	Maintenance control varies bias on magnetic core storage sense amplifiers. This switch should not be used by the operator.
F, P, S	Three-position switch that chooses the register to be displayed in the P register group.

Enter-Sweep	SWEEP is used to display the contents of the core storage locations.
	ENTER is used for entering information into the core storage of the 8090 from the console.
Selective Jump Switches (4, 2, 1)	UP selects jump conditions for interrogation by SLJ and SJS commands.
BFR, A, A'	Three-position switch that chooses the register to be displayed in the A register group.
Selective Stop Switches (4, 2, 1)	Up position selects stop conditions for interroga- tion by SLS and SJS commands.
Load-Clear	Momentary CLEAR performs a computer Master Clear which:
	a) Clears the P, A, Z, F, and F' Registers
	b) Clears the control flip-flops
	c) Sets (r) - 0
	d) Clears all waiting interrupts and removes interrupt lockout
	This Master Clear does not alter core storage.
	LOAD position enables specially prepared paper tapes to be read into storage by the 8074/8075 reader.
BFR, ENT, Z BFR, EXIT	Three-position switch that chooses the register to be displayed in the Z register group.
Run-Step	In RUN position a program is executed at high speed starting at the location specified by the P register.
	CENTER position stops the computer program. If the switch is in RUN and an ERR, SLS, SJS, HLT instruction is executed, the switch must be returned to STOP and then placed in RUN to continue computation.

IN STEP position one storage cycle of an instruction is executed each time the switch is set. In this manner a program may be executed one instruction at a time for debugging.

By simultaneously holding down the Step switch and any one of the selective jump switched the computer is placed in the AUTOMATIC STEP Mode. In this mode a program is executed at a rate of about three instructions per second with console display.

#### ARITHMETIC UNIT

Power (Binary) Arithmetic Unit (Octal) Indicates arithmetic unit is connected and power is on.

Timing Fault

Indicates a fault in the Arithmetic Unit Timing. A timing fault requires a repeat of the program.

#### TAPE SYNCHRONIZER

Power (Binary) Tape Synchronizer (Octal)	Indicates Tape Synchronizer is connected and power is on					
Binary	This switch-indicator chooses and displays binary mode (odd parity) operation.					
Coded	This switch-indicator chooses and displays coded mode (even parity) operation.					
Program (Binary) Program Error (Octal)	Indicates an illegal BCD or a back space selec- tion was made while the tape was at load point.					
Parity (Binary) Parity Error (Octal)	Indicates a parity error or an illegal BCD					

#### AUXILIARY MEMORY

Power (Binary) Auxiliary Memory (Octal)	Indicates Auxiliary Memory is connected and power is on.						
High Temp. (Binary) Overheat (Octal)	Indicates temperature of Auxiliary Memory Cabinet is reaching a dangerous level.						
Blower	Indicates that blower is not working.						
Memory Temp. 1, 2, 3	Indicates when Memory Stacks 1, 2, 3 are heating. Light drops when stacks reach operating tem- perature.						
Timing Fault 1	Indicates Module 1 Timing Fault caused by:						
	Initial start conditions.						
	Multiple pulses or dropout of pulse.						
	Multiple pulses in module.						
	Timing chain.						
Timing Fault 2	Indicates Module 2 timing fault.						
Timing Fault 3	Indicates Module 3 timing fault.						
Select (Binary) Buffer Select (Octal)	Buffer is waiting to select peripheral equipment.						
IBA (Binary) Input Buffer (Octal)	External Input Buffer active.						
OBA (Binary) Output Buffer Active (Octal)	External Output Buffer active.						

Timing fault switch(s) clears the external memory module controls and cannot be programmed. On the octal console the fault clear does this. On the Binary console, the external buffer can be cleared by the IBA, OBA switch, or the Select switch, or an EF code 4702. On the Octal console, the external buffer can be cleared by the BUFFER CLEAR switch, or an EF code 4702.

#### OPERATION

Start

- 1. Be sure the computer is plugged into the proper power source and that the room temperature is within the prescribed limits.
- 2. Turn the Power Off-On-Disable on the console to ON.
- 3. The Error and Fault indicators will normally light. Master Clear by momentarily pressing the Load-Clear switch to the Clear position.
- 4. The Error and Fault indicators should go out. This indicates that the computer is ready to operate. If repeated Master Clears do not remove the Error and Fault indicator turn the 8090 OFF by turning to the Power Off position, and call Maintenance.

#### Load Paper Tape Load Format

Note: Paper tape load format is described in the input-output programming section.

- 1. Master Clear
- 2. Turn on 8074/8075 reader by pressing the Reader On/Off lever to On.
- 3. Insert paper tape in reader.
- 4. Set P to starting location.
- 5. Set relative storage bank control to select the bank into which the tape will be read.
- 6. Set the Load-Clear switch to load.
- 7. Set the Run-Step switch to Run. The paper tape will load and the computer will stop.

Entering Data From The Console

- 1. Master Clear. Set the Enter-Sweep switch on Enter.
- 2. Set relative storage bank control to select the bank into which data is to be entered.
- 3. Set P to the location into which data is to be entered.
- 4. Enter one word of data into the Z register.
- 5. Press the Run-Step switch to Step, once. At this point Z is clear and the data word is in storage and in A, and P has been advanced by 1. (P advances each time except the first time.)
- 6. If data is to be entered into consecutive locations, go to step 4. If data is to be entered into nonconsecutive locations, clear P. Go to step 3.

Examining The Contents Of Storage At The Console

- 1. Master Clear. Set the Enter-Sweep switch on Sweep.
- 2. Set relative storage bank control to select the bank to be examined.
- 3. Set P to the location to be examined.
- 4. Press the Run-Step switch to Step, once. The contents of the location specified by P will appear in Z, and P will be advanced by 1. (P advances each time except the first time.)
- 5. To examine consecutive locations, go to step 4. To examine nonconsecutive locations, Clear P, go to step 3.

Clearing An Entire Storage Bank

- 1. Master Clear. Set the Enter-Sweep switch on Sweep.
- 2. Set relative storage bank control to select the bank to be cleared.
- 3. Set the Run-Step switch on Run.
- 4. Press the Clear Z button and hold for about a second.

#### 8073 PAPER TAPE PUNCH

The punch is turned on and off from the 8090 console. To the right of the punch On-Off buttons is a button labeled TL. When the punch is on, pressing the TL button will feed blank tape (with sprocket hole only) through the punch as long as the button is held down.

The punch may be operated with the unit remaining in the left pedestal of the computer as the tape feeds out of a special slot in the left side of the computer desk. However, the left pedestal door may be opened and the punch extended.

#### Loading A New Roll Of Tape

- 1. Turn punch on
- Tear off old tape and run all tape out of the punch block by pressing the TL button
- 3. Turn off punch
- 4. Lift the tape reel out of the punch and remove the old reel by unscrewing the X shaped side plate.
- 5. Place a new roll of tape on the reel so that the tape unwinds counterclockwise, and attach the side plate.
- 6. Place the tape reel in the punch. Thread the tape through the loop on the reel brake arm, through the loop at the front of the punch, around the two rollers and into the tape guide.
- Slowly slide the tape through the punch block. Pull the tape through the punch block, lift the tape tension lever and feed the tape between the tape tension lever and the tape feed wheel.
- 8. Turn punch on.
- Gently pull on the tape and press the tape feed lever. The tape will begin to feed automatically into the punch block. After about 6 inches of tape have been fed the sprocket holes will be correctly punched.

#### 8074 PAPER TAPE READER

The Reader is turned on and off from the console.

Tape Loading

- 1. Turn reader on.
- 2. Rotate the tape release handle clockwise to separate the idler rollers and raise the tape guide plate.
- 3. Set the tape width guide by pressing down the guide to release the locking fingers and slide it so that the marker rests above the correct etched mark on the tape deck surface.
- 4. Set the tape level switch for 5, 7, or 8 channel reading.
- 5. Insert the tape in the reader between the idler rollers (figure 8). The highest level hole is toward the open side. Be sure the tape is seated correctly in the tape guide
  - READ STATION TAPE RELEASE HANDLE TAPE EXI g TAPE LEVEL SWITCH IDLER TAPE INPUT À TAPE GUIDE TAPE WIDTH

6. Engage the tape release handle by turning it counterclockwise.

Figure 8. 8074 A/B Paper Tape Reader

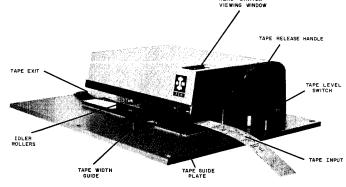
#### **8075 PAPER TAPE READER**

The Reader is turned on and off from the computer console.

Tape Loading

1. Turn Reader on.

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- 2. Raise the lift lever handle and thread tape through the read head. This raises the read head so that the capstan is clear.
- 3. Lay the tape across the capstan so that the pins project through the sprocket holes. Be sure the tape is positioned so that the pins do not project through the holes of a data channel. Also, be certain the tape is threaded with level 1 nearest the operator.
- 4. While holding the tape in position on the capstan, push the lift level down until the lever locks in a slightly over-center position.

#### Splicing Paper Tape

1

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Tape snagging or twisting can be caused by improperly spliced tape. Avoid any splice with a loose edge capable of rising in the direction of tape travel. Feed holes on the strips must be aligned before joining. Acceptable splices are shown in Figure 9.

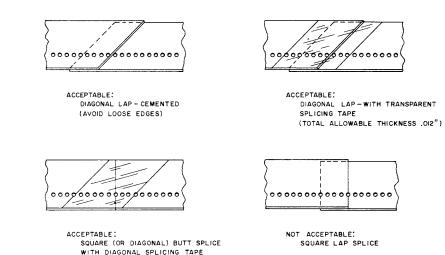


Figure 9. Tape Splices

# GLOSSARY

#### GLOSSARY OF PROGRAMMING TERMS

The following glossary gives the meaning of terms that are used in a relatively specialized sense in this manual.

ADDER	In general, a device used to add two quantities. Spe- cifically, the borrow structure in the subject computer.
ADDRESS	The number designating a storage location; also the storage location itself.
BANK	A unit of core storage with provisions for storing 4096 words. The use of more than one bank permits increas- ing the storage capacity of a computer without increas- ing the word length implicitly necessary to extend the range of storage addresses. In the computer, this ad- dress is effectively increased by a separate instruction (set storage bank control) which determines which bank(s) will be used during a program. Although the total computer storage capacity may be extended to eight banks, no more than four may be addressed at any time.
BIT	Binary digit; may be either ''1'' or ''0''.
BORROW	In a subtractive counter or accumulator, a signal in- dicating that in stage n, a ''1'' was subtracted from a ''0''.
BUFFER	Noun: A device in which data are stored temporarily in the course of transmission from one point to another. Verb: To store data temporarily.
BUFFERED INPUT/OUTPUT	A term indicating that the computer may carry on high speed computation at the same time it is exchanging data with a peripheral device. In the computer, this term must be distinguished from normal I/O, during which the computer cannot engage in computation.
CARRY	In an additive counter or accumulator, a signal indicat- ing that in stage n, a ''1'' was added to a ''1''.
CHANNEL	A transmission path that connects the computer to a given external equipment.
CHARACTER	Information handled by the computer:
	<ol> <li>A group of 6 bits representing bi-octal information; may denote a binary quantity, a digit, letter or symbol. In load mode, two 6-bit characters are assembled into one computer word.</li> </ol>

	2) A group of 7 bits representing an item of information. When the capacity of an input device is 6 or 7 bits, those bits will be deposited in the lower portion of the selected storage address, the remaining bits will be zeros.
CLEAR	A command that removes a quantity from a register by placing every stage in the ''O'' state.
COMMAND	A signal that performs a unit operation, such as trans- mitting contents of one register to another, shifting a register, setting a flip-flop.
COMPLEMENT	Noun: See One's Complement or Two's Complement. Verb: A command which produces the one's complement of a given quantity.
CONTENT	The quantity or word held in a register or storage location.
CORE	A small ferromagnetic toroid used as the bistable de- vice for storing a bit in a memory plane.
COUNTER	A register with provisions for increasing or decreasing its content by 1 upon receiving the appropriate com- mand.
DIRECT ADDRESSING	A mode of addressing wherein the execution address portion (E) of the instruction word contains the address of the operand to be acted upon. In the computer, the 6-bit execution address limits direct addressing to the first 64 of the possible 4096 storage locations ( $2^6 = 64$ ) in the direct bank.

END-AROUND BORROW A borrow that is generated in the highest order of an accumulator or counter, and is sent directly to the lowest order stage.

ENTER To manually place in a register a quantity that is not from storage. In the computer, quantities may be entered in only the A, P, and Z registers.

EXECUTION ADDRESS The lower 6 bits of a 12-bit instruction. Most often used to specify the storage address of an instruction or operand. Sometimes used as the operand.

FUNCTION CODE The upper 6 bits of a 12-bit instruction.

- INDIRECT ADDRESSING A mode of addressing which extends the length of the execution address (E) to a full computer word, thereby permitting operand references to be made upon any location in storage. All indirect addresses must be contained in storage locations which are available by means of direct addressing. In the computer, the constant and memory modes are special forms of indirect addressing.
- INPUT DISCONNECT During an input instruction, a signal sent to the computer by the external device to indicate that the device has completed all available transmissions to the computer.
- INPUT REQUEST A request, by the computer, for information from an external device. Occurs during input instruction only. (See Resume.)
- INSTRUCTION A 12-bit or 24-bit quantity consisting of a function (or operation) code and an execution address.
- INTERRUPT A signal (or class thereof) which, when received and recognized by the computer, forces the computer to forestall its current operation and jump to a subroutine, the starting address of which is determined by the class of the interrupt. A subroutine may have any number of options. It may merely stop the computer, it may determine the nature of the interrupt in order to take corrective measures, or it may return the computer to another phase of the main program.
- LOAD To place a quantity from storage in the A register.
- LOCKOUT Any function (usually of machine logic) that inhibits an action which would normally occur were the lockout not imposed.
- LOGICAL PRODUCT In Boolean algebra, the AND function of several terms. The product is "1" only when all the terms are "1"; otherwise it is "0". Sometimes referred to as the result of "bit-by-bit" multiplication.
- LOGICAL SUM In Boolean algebra, the OR function of several terms. The sum is "1" when any or all of the terms are "1"; it is "0" only when all are "0".

MASK	In the information of the logical products of two quan- tities, one of them may be used as a mask for the other. The mask determines what part of the other quantity is to be considered. Wherever the mask is "O", that part of the other quantity is cleared, but wherever the mask is a "1", the other quantity is left unaltered.
MASTER CLEAR (MC)	A general command produced by placing the Load/Clear switch in the down (CLEAR) position. An MC clears all of the crucial registers and control FFs to prepare for a new mode of operation.
MODULUS	An integer which describes certain arithmetic charac- teristics of registers, especially counters and accum- ulators, within a digital computer. The modulus of a device is defined by $r^n$ for an open ended device and $r^{n-1}$ for a closed (end-around) device, where r is the base of the number system used and n is the number of digit positions (stages) in the device. Generally, de- vices with modulus $r^n$ use two's complement arithmetic procedures, and devices with modulus $r^{n-1}$ use one's complement procedures.
NORMAL JUMP	An instruction that jumps from one sequence of instruc- tions to a second, and makes no preparation for re- turning to the first sequence.
ONE'S COMPLEMENT	With reference to a binary number, that number which results from subtracting each bit of the given number from the bit "1". A negative number is expressed by the one's complement of the corresponding positive number.
OPERAND	Usually refers to the quantity specified by the execu- tion address. This quantity is operated upon in the execution of the instruction.
OPERATION CODE	The upper 6 bits of a 12-bit instruction which identifies the instruction. After the code is translated, it con- ditions the computer for execution of the specified instruction. The letter F is used to designate this code, which is expressed by two octal digits.
OVERFLOW	The condition in which the capacity of a register is exceeded.
PARTIAL ADD	An addition without carries. Accomplished by toggling each bit of the augend where the corresponding bit of addend is a ''1''.

PROGRAM	A precise sequence of instructions that accomplishes a computer routine; a plan for the solution of a problem.
READ	To place a quantity from a storage location into a reg- ister. The quantity in storage remains unchanged.
READY	The input/output control signal sent by either the com- puter or an external equipment to alert the device that is to receive a transmission. The ready signal in- dicates that the word or character has been transmitted.
REFLECTED BINARY (COUNTER)	A reflected binary, or Gray-code counter is one in which only one element changes state for successive counts.
RELATIVE ADDRESSING	A mode of addressing wherein the address of the oper- and is determined by adding (or subtracting) the con- tents of the execution address portion (E) of the in- struction word to (or from) the instruction address.
REPLACE	In the title of an instruction, the result of the execution of the instruction is stored in the location from which the initial operand was obtained.
RESUME	The output control signal sent by an external equip- ment to indicate that it is prepared to receive another word or character. The resume signal is thus a request for data. (See Input Request.)
RETURN JUMP	A jump instruction which prepares for continuing the first sequence after the second is completed.
ROUTINE	The sequence of operations which the computer per- forms under the direction of a program.
SHIFT	To move the bits of a quantity right or left.
SIGN BIT	The bit in the highest-order stage of the register (in registers where a quantity is treated as signed by use of one's complement notation). If the bit is "1", the quantity is negative; if the bit is "0", the quantity is positive.
SIGN EXTENSION	The duplication of the sign bit in the higher-order stages of a register.

STATUS	<ol> <li>The condition of an external device, as reflected in the response given to a status request interrogation by the computer.</li> <li>The condition of the computer as shown by the Status Mode indicator on the console. May variously indicate what it is presently doing, why it stopped, or what it will do when it next starts.</li> </ol>
TRANSMISSION, FORCED	A transmission where both set and clear inputs, only one of which will be a ''1'', are simultaneously gated into a FF which has not been cleared previously.
TRANSLATION	An indication of the content of a group of bit registers. A complete translation gives the exact content, while a partial translation indicates only that the content is within certain limits.
TWO'S COMPLEMENT	That number which results from subtracting each bit of a number from "O". The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the re- quired carries.
WORD	A unit of information which has been coded for use in the computer as a series of bits. The normal word length is 12 bits.
WRITE	To enter a quantity into a storage location.

# **APPENDIX SECTION**

## **APPENDIX I**

## Table of Instructions

	lable of Instructions									
F	E	MNE- MONIC	NAME TIM	IING	F E MONIC NAME	TIMING				
00	00	ERR	Error Štop	1	11 00 LPM Logical Product Memory	3				
00	0X	NOP	No Operation	1	11 YY LPI Logical Product Indirect	3				
00	1X	SRJ	Set Relative Bank Control & Jump	1	12 00 LPC Logical Product Constant	2				
00	2X	SIC	Set Indirect Bank Control	1	12 XX LPF Logical Product Forward	2				
00	3X	IRJ	Set Indirect & Relative Bank Control		13 00 LPS Logical Product Specific	2				
			& Jump	1	13 XX LPB Logical Product Backward	2				
00	4X	SDC	Set Direct Bank Control	1	14 YY SCD Selective Complement Direct	2				
00	5Y	DRJ	Set Direct & Relative Bank Control	1	15 00 SCM Selective Complement Memory	3				
00	6X	SID	& Jump Set Indirect & Direct Bank Control	1	15 YY SCI Selective Complement Indirect	3				
	-	ACJ	Set Direct, Indirect, & Relative Bank	•	16 00 SCC Selective Complement Constant	2				
00	/ ^	ACJ	Control & Jump	1	16 XX SCF Selective Complement Forward	2				
01	00	BLS	Block Store (no jump)	l+n	17 00 SCS Selective Complement Specific	2				
			(jump)	2	17 XX SCB Selective Complement Backward	2				
01	01	ΡΤΑ	Transfer P to A	1	20 YY LDD Load Direct	2				
01	02	LS1	Left Shift One	1	21 00 LDM Load Memory	3				
01	03	LS2	Left Shift Two	1	21 YY LDI Load Indirect	3				
01	04		Clear Buffer Controls	1	22 00 LDC Load Constant	2				
01	05	ATE	A to Buffer Entrance Register (no jump)	1	22 XX LDF Load Forward	2				
			(jump)	2	23 00 LDS Load Specific	2				
01	06	ΑΤΧ	A to Buffer Exit Register (no jump)	1	23 XX LDB Load Backward	2				
			(jump)	2	24 YY LCD Load Complement Direct	2				
01	07	ETA	Buffer Entrance Register to A	1	25 00 LCM Load Complement Memory 25 YY LCI Load Complement Indirect	3				
01	10	LS3	Left Shift Three	1	26 00 LCC Load Complement Constant	3				
01	11	LS6	Left Shift Six	1	26 XX LCF Load Complement Forward	2 2				
01	12	MUT	Multiply A by Ten	1	27 00 LCS Load Complement Specific	2				
01	13	MUH	Multiply A by One Hundred	1	27 XX LCB Load Complement Backward	2				
01	14	RS1	Right Shift One	1	30 YY ADD Add Direct	2				
01	15	RS2	Right Shift Two	1	31 00 ADM Add Memory	3				
01	20	CIL	Clear Interrupt Lockout	1	31 YY ADI Add Indirect	3				
01	30	CTA	Bank Controls to A	1	32 00 ADC Add Constant	2				
01	4X	SBU	Set Buffer Bank Control	1	32 XX ADF Add Forward	2				
		STP	Store P at Location 5Y	3	33 00 ADS Add Specific	2				
01	6Y	STE	Store Buffer Entrance Register at Location 6Y & Transfer A to		33 XX ADB Add Backward	2				
			Buffer Entrance Register	3	34 YY SBD Subtract Direct	2				
02	ΧХ	LPN	Logical Product No Address	1	35 00 SBM Subtract Memory	3				
03	ΧХ	SCN	Selective Complement No Address	1	35 YY SBI Subtract Indirect	3				
04	хх	LDN	Load No Address	1	36 00 SBC Subtract Constant	2				
			Load Complement No Address	1	36 XX SBF Subtract Forward	2				
06	хх	ADN	Add No Address	1	37 00 SBS Subtract Specific	2				
		SBN	Subtract No Address	1	37 XX SBB Subtract Backward	2				
			Logical Product Direct	2	40 YY STD Store Direct	3				

### Table of Instructions (Cont'd)

FΕ	MNE- MONIC	NAME	TIMING	F E MONIC NAME TIM	ING
41 00	STM	Store Memory	4	61 XX NZF Non-Zero Jump Forward	1
41 YY	STI	Store Indirect	4	62 XX PJF Positive Jump Forward	1
42 00	STC	Store Constant	3	63 XX NJF Negative Jump Forward	1
42 X X	STF	Store Forward	3	64 XX ZJB Zero Jump Backward	1
43 00	STS	Store Specific	3	65 XX NZB Non-Zero Jump Backward	1
43 XX	STB	Store Backward	3	66 XX PJB Positive Jump Backward	1
44 YY	SRD	Shift Replace Direct	3	67 XX NJB Negative Jump Backward	1
45 00	SRM	Shift Replace Memory	4	70 YY JPI Jump Indirect	2
45 YY	SRI	Shift Replace Indirect	4	71 00 JPR Return Jump	3
46 00	SRC	Shift Replace Constant	3	71 XX JFI Jump Forward Indirect	2
46 XX	SRF	Shift Replace Forward	3	72 00 IBI Initiate Buffer Input (no jump)	
47 00	SRS	Shift Replace Specific	3	(jump)	2
47 XX	SRB	Shift Replace Backward	3	72 XX INP Normal Input	î
50 YY	RAD	Replace Add Direct	3	73 00 IBO Initiate Buffer Output (no jump)	
51 00	RAM	Replace Add Memory	4	(jump) 73 XX OUT Normal Output	2
51 YY	RAI	Replace Add Indirect	4	74 XX OTN Output No Address	*
52 00	RAC	Replace Add Constant	3	75 00 EXC External Function Constant	2
-		Replace Add Forward	3	75 XX EXF External Function Forward	2
53 00	RAS	Replace Add Specific	3	76 00 INA Input to A	*
-	RAB	Replace Add Backward	3	76 YY HWI Half Write Indirect	4
54 YY	AOD	Replace Add One Direct	3	76 77 OTA Output from A	*
55 00	AOM	Replace Add One Memory	4	77 00 HLT Halt	1
55 YY	AOI	Replace Add One Indirect	4	77 OX SLS Selective Stop	1
56 00	AOC	Replace Add One Constant	3	77 XO SLJ Selective Jump (no jump)	1
	AOF	Replace Add One Forward	3	(jump)	2
57 00	AOS	Replace Add One Specific	3	77 XX SJS Selective Stop & Jump (no jump)	1
•••••	AOB	Replace Add One Backward	3	(jump)	2
60 XX	ZJF	Zero Jump Forward	I	77 77 HLT Halt	1

#### NOTE:

1) All timings are given in memory cycles where 1 memory cycle equals 6.4 usec.

2) All numeric operation codes not listed in the above table will be executed as if they were a NOP instruction.

\* Execution time varies with speed of external equipment in use.

## Table of Instructions Arranged by Functions

-	F	0	MNE- MONIC		TIMIT	No I	-	F	0	MNE-		
<u>F</u>	<u>E</u>	G		NAME	1 HVH		<u>F</u>	<u>E</u>	<u>G</u>	MONIC		MING
		RUCTIC		F 64		,	ARITE	IMEI	IC INST	RUCI		
00	00		ERR	Error Stop			01	12		MUT	Multiply A by 10	1
77	00		HLT	Halt			01	13		MUH	Multiply A by One Hundred	1
77 DATA	• •	NEWLEEL	HLT			1	07	ХΧ		SBN	Subtract No Address	1
				STRUCTIONS		_	34	ΥY		SBD	Subtract Direct	2
01	00	YYYY	BL2	Block Store	(no jump) (jump)	1 2	35	00	YYYY	SBM	Subtract Memory	3
01	01		ΡΤΑ	Transfer P to A	(lomb)	1	35	ΥY		SBI	Subtract Indirect	3
01	05	YYYY		A to Buffer Entrar	ice Register		36	00	XXXX	SBC	Subtract Constant	2
0.	•••			Denor Enna	(no jump)	1	36	ХΧ		SBF	Subtract Forward	2
					(jump)	2	37	00		SBS	Subtract Specific	2
01	06	YYYY	ATX	A to Buffer Exit F		,	37	ХΧ		SBB	Subtract Backward	2
					(no jump) (jump)	1	06	ХΧ		ADN	Add No Address	1
01	07		ETA	Buffer Entrance R		1	30	ΥY		ADD	Add Direct	2
01	30		СТА	Bank Controls to	-	1	31	00	YYYY	ADM	Add Memory	3
01	5Y		STP	Store P at Locatio	on 5X	3	31	ΥY		ADI	Add Indirect	3
01	6Y		STE	Store Buffer Entra	nce		32	00	XXXX	ADC	Add Constant	2
				Register at Loco			32	ΧХ		ADF	Add Forward	2
				Transfer A to Bu Entrance Registe		3	33	00		ADS	Add Specific	2
04	ΧХ		LDN	Load No Address		1	33	ΧХ		ADB	Add Backward	2
20	YY		LDD	Load Direct		2	50	ΥY		RAD	Replace Add Direct	3
21	00	YYYY	LDM	Load Memory		3	51	00	YYYY	RAM	Replace Add Memory	4
21	ΥY		LDI	Load Indirect		3	51	ΥY		RAI	Replace Add Indirect	4
22	00	XXXX	LDC	Load Constant		2	52	00	XXXX	RAC	Replace Add Constant	3
22	хх		LDF	Load Forward		2	52	ΧХ		RAF	Replace Add Forward	3
23	00		LDS	Load Specific		2	53	00		RAS	Replace Add Specific	3
23	ΧХ		LDB	Load Backward		2	53	ΧХ		RAB	Replace Add Backward	3
05	ΧХ		LCN	Load Complement	No Address	1	54	ΥY		AOD	Replace Add One Direct	3
24	ΥY		LCD	Load Complement		2	55	00	YYYY	AOM	Replace Add One Memory	4
25	00	YYYY	LCM	Load Complement		3	55	YΥ		AOI	Replace Add One Indirect	4
25	ΥY		LCI	Load Complement	Indirect	3	56	00	XXXX	AOC	Replace Add One Constant	3
26	00	XXXX	LCC	Load Complement	Constant	2	56	ΧХ		AOF	Replace Add One Forward	3
26	ΧХ		LCF	Load Complement	Forward	2	57	00		AOS	Replace Add One Specific	3
27	00		LCS	Load Complement	Specific	2	57	ΧХ		AOB	Replace Add One Backward	3
27	ΧХ		LCB	Load Complement	Backward	2	SHIFT	INS	TRUCT	ONS		
40	ΥY		STD	Store Direct		3	01	02		LS1	Left Shift One	1
41	00	YYYY	STM	Store Memory		4	01	03		LS2	Left Shift Two	1
41	ΥY		STI	Store Indirect		4	01	10		LS3	Left Shift Three	1
42	00	XXXX	STC	Store Constant		3	01	11		LS6	Left Shift Six	1
42	ХΧ		STF	Store Forward		3	01	14		RS1	Right Shift One	1
43	00		STS	Store Specific		3	01	15		RS2	Right Shift Two	1
43	ΧХ		STB	Store Backward		3	44	ΥY		SRD	Shift Replace Direct	3
76	ΥY		HWI	Half Write Indirect	t	4	45	00	YYYY	SRM	Shift Replace Memory	4

## Table of Instructions Arranged by Functions (Cont'd)

<u>F</u>	E	G	MNE- MONIC	N AME TIMI	VG	Ē	E	G	MNE- MONIC	NAME	TIMIN G
SHIFT	INS	TRUCT	ONS (a	cont'd)		JUMP	INS	TRUCTI	ONS		
45	ΥY		SRI	Shift Replace Indirect	4	60	ΧХ		ZJF	Zero Jump Forward	1
46	00	XXXX	SRC	Shift Replace Constant	3	61	ХΧ		NZF	Non-Zero Jump Forward	1
46	ΧХ		SRF	Shift Replace Forward	3	62	ХΧ		PJF	Positive Jump Forward	1
47	00		SRS	Shift Replace Specific	3	63	ХΧ		NJF	Negative Jump Forward	1
47	ΧХ		SRB	Shift Replace Backward	3	64	ХΧ		ZJB	Zero Jump Backward	1
						65	ХΧ		NZB	Non-Zero Jump Backward	1
LOGIC	AL	INSTRU	CTION	S		66	ХΧ		РJВ	Positive Jump Backward	1
02	ХΧ		LPN	Logical Product No Address	1	67	ХΧ		NJB	Negative Jump Backward	1
10	ΥY		LPD	Logical Product Direct	2	70	ΥY		JPI	Jump Indirect	2
11	00	YYYY	LPM	Logical Product Memory	3	71	00	YYYY	JPR	Return Jump	3
11	ΥY		LPI	Logical Product Indirect	3	71	ХΧ		JFI	Jump Forward Indirect	2
12	00	XXXX	LPC	Logical Product Constant	2	INPU'	τ/οι	ΙΤΡυτ Ι	NSTRI	JCTIONS	
	XX		LPF	Logical Product Forward	2	01	04		CBC	Clear Buffer Controls	1
13	00		LPS	Logical Product Specific	2	01	20		CIL	Clear Interrupt Lockout	1
	XX		LPB	Logical Product Backward	2		00	YYYY	IBI	Initiate Buffer Input	•
	ХХ		SCN	Selective Complement No Address	1					(no jum (jump)	p) 1 2
	ΥY		SCD	Selective Complement Direct	1	73	00	YYYY	IBO	Initiate Buffer Output	
15	00	YYYY	SCM	Selective Complement Memory	3					(no jum (jump)	p) 1 2
15	ΥY		SCI	Selective Complement Indirect	3	72	хx	YYYY	INP	Normal Input	∠ *
16	00	xxxx	SCC	Selective Complement	Ũ	72		YYYY	OUT	Normal Output	*
		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		Constant	2	74	XX		OTN	Output No Address	*
16	ХΧ		SCF	Selective Complement		76	00		INA	Input to A	*
17	00		505	Forward	2		77		ΟΤΑ	Output from A	*
17	00		SCS	Selective Complement Specific	2	75	00	XXXX	EXC	External Function Constan	t 2
17	хх		SCB	Selective Complement		75	ΧХ		EXF	External Function Forward	2
				Backward	2	SELE	сті	E STOP	AND	JUMP INSTRUCTIONS	
STOR	AGE	BANK	CONTR	OL INSTRUCTIONS		00	0X		NOP	No Operation	1
00	1X		SRJ	Set Relative Bank Control		77	0X		SLS	Selective Stop	1
00	2X		SIC	& Jump Set Indirect Bank Control	1	77	X0	YYYY	SLJ	Selective Jump (no jump (jump)	o) 1 2
00	3X		IRJ	Set Indirect & Relative Bank Control & Jump	1	77	ХΧ	YYYY	SJS	Selective Stop & Jump (no jump	p) ]
00	4X		SDC	Set Direct Bank Control	1					(jump)	2
00	5X		DRJ	Set Direct & Relative Bank Control & Jump	1						
00	6X		SID	Set Indirect & Direct Bank Control	1						
00	7X		ACJ	Set Direct, Indirect, & Relative Bank Control & Jump	1	*	Exec	cution ti	me vari	es with speed of external	
01	4X		SBU	Set Buffer Bank Control	1			pment in		the second second second	
						•					

## **APPENDIX II** Table of External Function Codes and Status Responses

#### 1. 8074/8075 PAPER TAPE READER

A. External Function Codes 4102 Select Reader

NOTE: There are no status responses for this equipment.

#### 2. 8073 PAPER TAPE PUNCH

- A. External Function Codes
   4104 Select Paper Tape Punch
- NOTE: There are no status responses for this equipment.

#### 3. 161 INPUT/OUTPUT TYPEWRITER

- A. External Function Codes
  - 4210 Select typewriter output
  - 4220 Select typewriter input
  - 4240 Request typewriter status
- B. Status Response Codes
  - 0000 Typewriter ready
  - 0004 Typewriter power off
  - 0010 Typewriter not in computer status
  - 0020 Input character ready
  - 0040 Output in use
- NOTE: If a second typewriter is added, the master bits will be 43.

#### 4. 8071/8072 MAGNETIC TAPE SYNCHRONIZER

- A. External Function Codes
  - Y11X Write if OUT is given
  - Y11X Write End-of-File mark if no OUT is given
  - Y12X Backspace one record if INA is given
  - Y12X Search backward to End-of-File mark if no INA is given
  - Y13X Read forward if INPUT is given
  - Y13X Search forward to End-of-File mark if no INPUT is given
  - Y14X Request status
  - Y15X Rewind unload
  - Y16X Rewind load
  - Y171 Set tapes to odd parity
  - Y172 Set tapes to even parity
  - 210X High density
  - 110X Low density
- B. Status Response Codes
  - 0000 Odd parity selected no errors
  - 0001 Even parity selected no errors

- 0002 Tape X not ready
- 0004 Parity error
- 0015 lilegal BCD detected on Write
- 0020 End-of-File mark read
- 0040 End-of-Tape or Load Point sensed
- 0100 High density
- 0200 Tape X busy

NOTES: Y = 1: 6-bit mode.

Y = 2: 12-bit mode. X = (0 to 7): designates one of the four (eight) 60X's. The master bits 12, 13, 22, and 23 are used for second and third tape control. If the tape transport is a 606, a 6-bit, high density selection is illegal (a programmer consideration).

#### 5. <u>165 PLOTTER</u>

- A. External Function Codes
   4401 Select Plotter for Write operation
   4440 Select Plotter for Read operation
- B. Follow 4401 with Output instruction and transmit one of these:
  - 0001 Move carriage and pen .01" in +X direction
  - 0002 Move carriage and pen .01" in —X direction
  - 0004 Rotate drum .01" in -Y direction
  - 0005 Carriage and pen move .01" in +X direction, drum rotates in --Y direction .01"
  - 0006 Carriage and pen move .01" in -X direction, drum rotates in -Y direction .01"
  - 0010 Rotate drum .01" in +Y direction
  - 0011 Carriage and pen move .01" in +X direction, drum rotates in +Y direction .01"
  - 0012 Carriage and pen move .01" in -X direction, drum rotates in +Y direction .01"
  - 0020 Move pen down to paper
  - 0040 Move pen away from paper
- C. Status Response Codes Status is obtained by selecting the unit for reading. The obtained status is the value of the 12 switches on the unit.

#### 6. <u>166-2 LINE PRINTER</u>

- A. External Function Codes
  - 0700 Asynchronous print
  - 0710 Synchronous print
  - 0740 Check status
  - 072X Advance forms
- B. Status Response Codes
  - 0000 166-2 ready
  - 0001 Buffer busy
  - 0002 Out of paper
  - 0004 Paper moving
  - 0010 Drum stationary
  - 0020 Off-line

#### 7. 167-1 CARD READER

- A. External Function Codes
  - 4500 EF clear
  - 4501 Free run read
  - 4502 Single cycle read
  - 4540 Check status
- B. Status Response Codes
  - 0000 Card Reader ready
  - 0001 Hopper empty
  - 0002 Stacker full
  - 0004 Feed failure
  - 0010 Program error
  - 0020 Amplifier failure
  - 0040 Motor power off
- 8. 167-2 CARD READER (Hollerith Facility)
  - A. External Function Codes
    - 4500 EF clear
    - 4501 Free run read
    - 4502 Single cycle read
    - 4505 FRR,  $H \rightarrow BCD$  and pack
    - 4506 SCR,  $H \rightarrow BCD$  and pack
    - 4540 Check status

## B. Status Response Codes 0000 Card Reader ready

- 0001 Hopper empty
- 0002 Stacker full
- 0004 Feed failure
- 0010 Program error
- 0020 Amplifier failure
- 0040 Motor power off

#### 9. 168-1 AUXILIARY ARITHMETIC UNIT

- A. External Function Codes
  3300 Short divide
  3301 Short multiply
  3302 Long divide
  3303 Long multiply
  3304 Status request
  3310 Reselect\*
  3323 Addition
  3363 Subtraction
  B. Status Response Codes
  0000 Unit ready
  0004 Add/Subtract overflow
  0010 Divide fault

  - 0020 Unload not completed
  - 0040 Busy computing

#### 10. 8083 AUXILIARY ARITHMETIC UNIT

Α.	Exter	nal Function Codes								
	3300	Divide	3314	Divide result						
	3301	Multiply	3315	Multiply result						
	3302	Left shift	3316	Left shift result						
	3303	Right shift	3317	Right shift result						
	3304	Status request								
	3310	Reselect*								
	3321	Addition	3335	Add to result						
	3342	Norm. & Count	3356	Norm. result & cour						
	3361	Subtraction	3375	Subt.from result						

- B. Status Response Codes 0000 Unit ready
  - 0010 Add Subtract overflow
  - 0020 Unload not completed
  - 0040 Busy computing
  - 4000 Divide fault\*\*
- \*Reselect is used if another external equipment has been selected prior to receiving the result of a selected 168 operation. It cannot be used to initially select the unit.
- \*\*A divide fault occurs when the divisor is equal to or smaller than the most significant 27 bits of the dividend.

#### 11. 8084/8085 AUXILIARY MEMORY UNIT

- A. External Buffer Select Codes
  - 4701 Select external buffer mode
  - 4702 Clear external buffer controls
  - 4704 Select BER read
  - 4710 Select channel extension mode
  - 4720 Clear channel extension mode
  - 4740 Select external buffer status
- B. External Buffer Status Responses
  - 1XXX Interrupt from other computer
  - 2XXX Interrupt from peripheral equipment
  - 4XXX Buffer interrupt
  - X1XX This CHX active
  - X2XX Other CHX active
  - X4XX Illegal bank selection
  - XX0X OBA-T
  - XX1X IBA-T
  - XX2X OBA-NT
  - XX3X IBA-NT
  - XX4X Buffer initiation
  - XXX2-7 External bank selection
  - 0000 External buffer ready

#### 12. 170 CARD PUNCH CONTROL UNIT

- A. External Function Codes
   3002 Punch
   3040 Check status
- B. Status Response Codes
  0000 170 ready
  0200 MS in 1604 position
  2000 Punch not ready

#### 13. 177 CARD READER

- A. External Function Codes
- 4500 EF clear
  - 4501 Free run read
  - 4502 Single cycle read
  - 4505 Negate translate,  $H \rightarrow BCD$ , free run read
  - 4506 Negate translate, H → BCD, single cycle read
  - 4510 Gate card
  - 4540 Status request
- B. Status Response Codes
  - 0001 Input tray empty
  - 0002 Primary or secondary stacker full
  - 0004 Feed failure
  - 0010 Late input request
  - 0020 Pre-read error
  - 0040 Manual on or motor power off
  - 0100 Read comparison error
  - 0200 End of file
  - 0400 Ready

#### 14. 1610 CONTROL UNIT

- A. External Function Codes
  - 0301 Read from primary read
  - 0302 Read from secondary read
  - 0340 Request status of input
  - 3001 Print
  - 3002 Punch
  - 3040 Request status of output
- B. Status Response Codes
  - 0000 All units ready
  - 0001 Reader not ready
  - 0020 1604 selected on input
  - 0200 1604 selected on output
  - 2000 Punch not ready
  - 4000 Printer not ready

#### 15. 1612 HIGH SPEED PRINTER

- A. External Function Codes
  - 0600 Select printer and do not interrupt on ready
  - 0601 Space paper one line
  - 0602 Space paper two lines
  - 0603 Skip to format channel 7
  - 0604 Skip to format channel 8
  - 0605 Print information and advance paper
  - 0606 Do not advance paper after next print
  - 0607 Select printer and interrupt on ready
  - 0610 Clear monitor channels 1-6
  - 0611 Select monitor channel 1
  - 0612 Select monitor channel 2
  - 0613 Select monitor channel 3
  - 0614 Select monitor channel 4
  - 0615 Select monitor channel 5
  - 0616 Select monitor channel 6
- B. Status Response Codes
  - 0000 Printer not ready
  - 4000 Printer ready
- NOTE: Status is always available on the 1612. No request is necessary.
- 16. <u>1614 CARD READER</u> EF and Status Codes same as 177 card reader.
- 17. <u>1615 MAGNETIC TAPE CONTROLLER</u> A. 160 External Function Codes
  - (N = 1→7)

#### Write Operations

- 60N1 Select tape N to write binary
- 60N2 Select tape N to write coded
- 6001 Prepare selected tape to write binary
- 6002 Prepare selected tape to write coded
- 6003 Write End-of-File on selected tape
- 6005 Rewind selected write tape
- 6006 Backspace selected write tape
- 6007 Rewind-unload selected write tape
- 6010 Set Low Density on selected write tape
- 6020 Set High Density on selected write tape
- 6030 Skip bad spot on selected write tape
- 6053 Request status

#### Read Operations

- 50N1 Select tape N to read binary one record
- 50N2 Select tape N to read coded one record
- 52N1 Select tape N to read binary one file
- 52N2 Select tape N to read coded one file
- 5001 Prepare selected tape to read binary one record
- 5002 Prepare selected tape to read coded one record
- 5201 Prepare selected tape to read binary one file
- 5202 Prepare selected tape to read coded one file
- 5003 Move selected read tape forward one record
- 5203 Search file mark forward
- 5005 Rewind selected read tape
- 5006 Backspace selected read tape
- 5206 Search file mark backward
- 5007 Rewind-unload selected read tape
- 5010 Set Low Density on selected read tape
- 5020 Set High Density on selected read tape
- B. Status Response Codes
  - X2XX Ready to read
  - X1XX Ready to write
  - XX4X Read parity error
  - XX2X Write reply parity error
  - XX1X End-of-File mark
  - XXX4 End-of-Tape mark

The following additional select and status codes are available under the program control mode of operation:

A. External Function Codes

#### Write Operations

- 6052 Release write control to 1604
- 6050 Release action request
- 5051 Set communication flag |
- 6055 Clear communication flag |
- 6051 Set communication flag ||
- 6056 Clear communication flag ||

#### Read Operations

- 5052 Release read control to 1604
- 5053 Select interrupt

#### 17. 1615 MAGNETIC TAPE CONTROLLER (Cont'd)

B. Status Response Codes

#### Write Operations

- 2XXX Write control available
- XXX1 Communication flag | set

#### **Read Operations**

- 4XXX Read control available
- 1XXX Direct 160 to 1604
- X4XX Direct 1604 to 160
- XXX2 160 action request

#### 18. 1619 DISK FILE CONTROLLER

- A. Select Codes
  - 7000 Request select
  - 7001 Request select clear positioner power
  - 7002 Request select write check
  - 7003 Request select check mode
  - 7004\* Select interrupt on next available
  - 7005\* Clear interrupt on next available
  - 7006\* Select interrupt on next ready
  - 7007\* Clear interrupt on next ready
  - 7010\* Select interrupt on next fault
  - 7011\* Clear interrupt on next fault
  - 7020 Request status
- B. Status Response Codes
  - XXX1 Not ready
  - XXX2 160 not selected
  - XXX4 1604 selected
  - XX1X Program error
  - XX2X Checkword error
  - XX4X Internal fault
  - 1XXX File off-line
  - 2XXX File warning

## Use This Page for Additional Codes

## **APPENDIX III**

#### TABLE OF POWERS OF 2

## APPENDIX IV

### OCTAL-DECIMAL INTEGER CONVERSION TABLE

			0	1	2	3	4	5	6		ן							-	~	-
0000	0000								6	7	$\left\{ \right.$	<b></b>	0	1	2	3	4	5	6	7
to	to	0000				0003						0400		0257			0260		0262	
0777	0511	0010				0011 0019			0014	0015 0023				0265 0273		0267 0275	0268 0276	0269	0270 0278	0271 0279
(Octal)	(Decimal)	0030							0030										0286	
		0040		0033			0036		0038			0440							0294	
Octol	Decimal	0050	1	0041		0043				0047	1	0450			0298		0300		0302	
	- 4096	0060			0050	0051 0059	0052 0060		0054	0055 00 <b>63</b>		0460 0470			0306			0309	0310 0318	
	- 8192	00.0	10000		0000	0000	0000	0001	0000			0110	0012	0010	0011	0010	0010		0010	0010
	- 12288	0100	1			0067						0500							0326	
	- 16384	0110	1	0073			0076		0078			0510	0328		0330	0331 0339		0333		0335
	- 20480 - 24576	0120	(	0081 0089		0083 0091	0084 0092		0086			0520 0530		0337	0338		0340			0343
	- 28672	0140			0098			0101				0540			0354			0357		0359
		0150	,		0106							0550			0362				0366	
					0114							0560			0370			0373		0375
		0170	0120	0121	0122	0123	0124	0125	0126	0127		0570	0376	03/1	0378	0319	0380	0381	0382	0383
		0200	0128	0129	0130	0131	0132	0133	0134	0135		0600	0384	0385	0386	0387	0388	0389	0390	0391
		0210	0136	0137	0138	0139	0140	0141	0142	0143		1			0394			0397		0399
					0146										0402			0405		0407
					0154 0162							0630 0640	0408		0410	0411		0413	0414	0415
					0170							0650			0426			0429		0431
		0260			0178			0181	0182	0183		0660			0434			0437		0439
		0270	0184	0185	0186	0187	0188	0189	0190	0191		0670	0440	0441	0442	0443	0444	0445	<b>04</b> 46	0447
		0300	0192	0193	0194	0195	0196	0197	0198	0199		0700	0448	0449	0450	0451	0452	0453	0454	0455
					0202							1		-			0460			0463
		0320			0210	_	0212						0464		0466			0469		0471
				0217				0221		0223			0472			0475		0477		0479
					0226 0234			0229 0237		0231			0480 0488			0483 0491	0404	0485		0487
					0242					0247									0502	
		0370	0248	0249	0250	0251	0252	0253	0254	0255		0770	0504	0505	0506	0507	0508	0509	0510	0511
																		-		
			0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
1000	0512	1000	0512	0513	0514	0515	0516	0517	0518	0519		1400	0768	0769	0770	0771	0772	0773	0774	0775
to	to	1010	0512 0520	0513 0521	0514 0522	0515 0523	0516 0524	0517 0525	0518 0526	0519 0527		1410	0768 0776	0769 0777	0770 0778	0771 0779	0772 0780	0773 0781	0774 0782	0775 0783
I		1010 1020	0512 0520 0528	0513 0521 0529	0514 0522 0530	0515 0523 .0531	0516 0524 0532	0517 0525 0533	0518 0526 0534	0519 0527 0535		1410 1420	0768 0776 0784	0769 0777 0785	0770 0778 0786	0771 0779 0787	0772 0780 0788	0773 0781 0789	0774 0782 0790	0775 0783 0791
to 1777	to 1023	1010	0512 0520 0528 0536	0513 0521 0529	0514 0522 0530	0515 0523 .0531 0539	0516 0524	0517 0525	0518 0526	0519 0527 0535 0543		1410 1420 1430	0768 0776 0784 0792	0769 0777 0785 0793	0770 0778 0786 0794	0771 0779 0787 0795	0772 0780 0788	0773 0781 0789 0797	0774 0782 0790 0798	0775 0783
to 1777	to 1023	1010 1020 1030 1040 1050	0512 0520 0528 0536 0544 0552	0513 0521 0529 0537 0545 0553	0514 0522 0530 0538 0546 0554	0515 0523 0531 0539 0547 0555	0516 0524 0532 0540 0548 0556	0517 0525 0533 0541 0549 0557	0518 0526 0534 0542 0550 0558	0519 0527 0535 0543 0551 0559		1410 1420	0768 0776 0784 0792 0800	0769 0777 0785 0793 0801	0770 0778 0786 0794 0802	0771 0779 0787 0795 0803 0811	0772 0780 0788 0796 0804 0812	0773 0781 0789 0797 0805 0813	0774 0782 0790 0798 0806 0814	0775 0783 0791 0799 0807 0815
to 1777	to 1023	1010 1020 1030 1040 1050 1060	0512 0520 0528 0536 0544 0552 0560	0513 0521 0529 0537 0545 0553 0561	0514 0522 0530 0538 0546 0554 0562	0515 0523 0531 0539 0547 0555 0563	0516 0524 0532 0540 0548 0556 0564	0517 0525 0533 0541 0549 0557 0565	0518 0526 0534 0542 0550 0558 0566	0519 0527 0535 0543 0551 0559 0567		1410 1420 1430 1440 1450 1460	0768 0776 0784 0792 0800 0808 0816	0769 0777 0785 0793 0801 0809 0817	0770 0778 0786 0794 0802 0810 0818	0771 0779 0787 0795 0803 0811 0819	0772 0780 0788 0796 0804 0812 0820	0773 0781 0789 0797 0805 0813 0821	0774 0782 0790 0798 0806 0814 0822	0775 0783 0791 0799 0807 0815 0823
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#### OCTAL-DECIMAL INTEGER CONVERSION TABLE

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					1052 1060					1304 1312								(Octal)	(Decimal)
2050	1064	1065	1066	1067	1068	1069	1070	1071	2450	1320	1321	1322	1323	1324	1325	1326	1327		
					1076 1084					1328 1336									Decimal
2100	1088	1080	1000	1001	1092	1003	1094	1095	2500	1344	1345	1346	1347	1348	1349	1350	1351		- 4096 - 8192
2110	1096	1097	1098	1099	1100	1101	1102	1103	2510	1352	1353	1354	1355	1356	1357	1358	1359	30000	- 12288
1 1					1108 1116					1360 1368									- 16384 - 20480
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2200	1152	1153	1154	1155	1156	1157	1158	1159	2600	1408	1409	1410	1411	1412	1413	1414	1415		
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2230	1176	1177	1178	1179	1180	1181	1182	1183	2630	1432	1433	1434	1435	1436	1437	1438	1439		
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2260	1200	1201	1202	1203	1204	1205	1206	1207	2660	1456	1457	1458	1459	1460	1461	1462	1463		
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#### OCTAL-DECIMAL INTEGER CONVERSION TABLE

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4000 2048	4000 4010			2050 2058														2310 2318	
to to 4777 2559	4020	2064	2065	2066	2067	2068	2069	2070	2071									2326	
(Octal) (Decimal)	4030 4040	2072		2074 2082														2334 2342	
	4050	2088	2089	2090	2091	2092	2093	2094	2095		4450	2344	2345	2346	2347	2348	2349	2350	2351
Octal Decimal		2096																2358 2366	
10000 - 4096 20000 - 8192	4070	2104	2105	2106	2107	2100	2109	2110	2111		4410	2300	2301	2302	2303	2304	2303	2300	2301
30000 - 12288		2112																2374	
40000 - 16384		2120 2128																2382 2390	
50000 - 20480 60000 - 24576		2126																2398	
70000 - 28672		2144																2406	
		2152 2160																2414 2422	
		2168																2430	
	4200	2176	2177	2178	2179	2180	2181	<b>2</b> 182	2183		4600	2432	2433	2434	2435	2436	2437	2438	2439
	4210	2184	2185	2186	2187	2188	2189	<b>2</b> 190	2191		4610	2440	2441	2442	2443	<b>Ż</b> 444	2445	2446	2447
		2192 2200																2454 2462	
		2200																2470	
	4250	2216	2217	2218	2219	2220	2221	2222	2223									2478	
	4260 4270	2224	2225	2226 2234	2227	2228	2229	2230	2231									2486 2494	
	4300 4310	2240		2242 2250					1									2502 2510	
	4310			2250														2510	
	4330	2264	2265	2266	2267	2268	2269	2270	2271		4730	2520	2521	2522	2523	2524	2525	2526	2527
	4340			2274 2282														2534 2542	
	4350 4360			2290														2550	
	4370	2296	2297	2298	2299	2300	2301	2302	2303									2558	
	. ,																		
-		0	1	2	3	4	5	6	7	-		0	1	2	3	4	5	6	7
		2560	2561	2562	2563	2564	<b>2</b> 565	2566	2567			2816	2817	2818	2819	<b>2</b> 820	2821	2822	2823
to to	5010	2560 2568	2561 2569	2562 2570	2563 2571	2564 2572	2565 2573	2566 2574	2567 2575		5410	2816 2824	2817 2825	2818 2826	2819 2827	2820 2828	2821 2829	2822 2830	2823 2831
to to 5777 3071	5010 5020	2560 2568 2576	2561 2569 2577	2562 2570 2578	2563 2571 2579	2564 2572 2580	2565 2573 2581	2566 2574 2582	2567 2575 2583		5410 5420	2816 2824 2832	2817 2825 2833	2818 2826 2834	2819 2827 2835	2820 2828 2836	2821 2829 2837	2822 2830 2838	2823 2831 2839
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040	2560 2568 2576 2584 2592	2561 2569 2577 2585 2593	2562 2570 2578 2586 2594	2563 2571 2579 2587 2595	2564 2572 2580 2588 2596	2565 2573 2581 2589 2597	2566 2574 2582 2590 2598	2567 2575 2583 2591 2599		5410 5420 5430 5440	2816 2824 2832 2840 2848	2817 2825 2833 2841 2849	2818 2826 2834 2842 2850	2819 2827 2835 2843 2851	2820 2828 2836 2844 2852	2821 2829 2837 2845 2853	2822 2830 2838 2846 2854	2823 2831 2839 2847 2855
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050	2560 2568 2576 2584 2592 2600	2561 2569 2577 2585 2593 2601	2562 2570 2578 2586 2594 2602	2563 2571 2579 2587 2595 2603	2564 2572 2580 2588 2596 2604	2565 2573 2581 2589 2597 2605	2566 2574 2582 2590 2598 2606	2567 2575 2583 2591 2599 2607		5410 5420 5430 5440 5450	2816 2824 2832 2840 2848 2856	2817 2825 2833 2841 2849 2857	2818 2826 2834 2842 2850 2858	2819 2827 2835 2843 2851 2859	2820 2828 2836 2844 2852 2860	2821 2829 2837 2845 2853 2853 2861	2822 2830 2838 2846 2854 2854 2862	2823 2831 2839 2847 2855 2863
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060	2560 2568 2576 2584 2592	2561 2569 2577 2585 2593 2601 2609	2562 2570 2578 2586 2594 2602 2610	2563 2571 2579 2587 2595 2603 2611	2564 2572 2580 2588 2596 2604 2612	2565 2573 2581 2589 2597 2605 2613	2566 2574 2582 2590 2598 2606 2614	2567 2575 2583 2591 2599 2607 2615		5410 5420 5430 5440 5450 5460	2816 2824 2832 2840 2848 2856 2864	2817 2825 2833 2841 2849 2857 2865	2818 2826 2834 2842 2850 2858 2866	2819 2827 2835 2843 2851 2859 2867	2820 2828 2836 2844 2852 2860 2868	2821 2829 2837 2845 2853 2861 2869	2822 2830 2838 2846 2854	2823 2831 2839 2847 2855 2863 2871
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070	2560 2568 2576 2584 2592 2600 2608 2616	2561 2569 2577 2585 2593 2601 2609 2617	2562 2570 2578 2586 2594 2602 2610 2618	2563 2571 2579 2587 2595 2603 2611 2619	2564 2572 2580 2588 2596 2604 2612 2620	2565 2573 2581 2589 2597 2605 2613 2621	2566 2574 2582 2590 2598 2606 2614 2622	2567 2575 2583 2591 2599 2607 2615 2623		5410 5420 5430 5440 5450 5460 5470	2816 2824 2832 2840 2848 2856 2864 2864 2872	2817 2825 2833 2841 2849 2857 2865 2873	2818 2826 2834 2842 2850 2858 2866 2874	2819 2827 2835 2843 2851 2859 2867 2875	2820 2828 2836 2844 2852 2860 2868 2868 2876	2821 2829 2837 2845 2853 2861 2869 2877	2822 2830 2838 2846 2854 2862 2870 2878	2823 2831 2839 2847 2855 2863 2871 2879
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635	2564 2572 2580 2588 2596 2604 2612 2620 2628 2628 2636	2565 2573 2581 2589 2597 2605 2613 2621 2629 2629 2637	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639		5410 5420 5430 5440 5450 5460 5470 5500 5510	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889	2818 2826 2834 2842 2850 2858 2866 2874 2882 2882 2890	2819 2827 2835 2843 2851 2859 2867 2875 2875 2883 2891	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110 5120	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2626 2634 2642	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647		5410 5420 5430 5440 5450 5460 5470 5500 5510 5520	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2902	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110 5120 5130	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2622 2634 2642 2650	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655		5410 5420 5430 5440 5450 5460 5470 5500 5510 5520 5520 5530	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2904	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2906	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899 2907	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2902 2910	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110 5120 5130 5140 5150	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2657 2665	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2650 2658 2666	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652 2660 2668	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2654 2662 2670	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2647		5410 5420 5430 5440 5450 5460 5470 5500 5510 5520 5530 5530 5540	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2904 2912	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2996 2914	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899 2907 2915	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908 2916	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909 2917	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2902	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911 2919
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110 5120 5130 5140 5150 5160	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664 2672	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2657 2665 2673	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2650 2658 2656 2658 2666 2674	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667 2675	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652 2660 2668 2668 2676	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669 2677	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2654 2654 2654 2670 2678	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2671 2679		5410 5420 5430 5440 5450 5460 5460 5510 5520 5520 5520 5520 5540 5550 5550	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2904 2912 2920 2928	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913 2921 2929	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2906 2914 2922 2930	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899 2907 2915 2923 2931	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908 2916 2924 2932	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909 2917 2925 2933	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2902 2910 2918 2926 2934	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911 2919 2927 2935
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5110 5120 5130 5140 5150 5160	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2657 2665 2673	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2650 2658 2656 2658 2666 2674	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667 2675	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652 2660 2668 2668 2676	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669 2677	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2654 2654 2654 2670 2678	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2671 2679		5410 5420 5430 5440 5450 5460 5460 5510 5520 5520 5520 5520 5540 5550 5550	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2904 2912 2920 2928	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913 2921 2929	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2906 2914 2922 2930	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899 2907 2915 2923 2931	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908 2916 2924 2932	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909 2917 2925 2933	2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2902 2910 2918 2926	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911 2919 2927 2935
to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5070 5100 5120 5130 5130 5140 5150 5160 5170	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664 2664 2664 2688	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2657 2665 2673 2681 2689	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2650 2658 2658 2666 2674 2682 2690	2563 2571 2577 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667 2675 2683 2683 2691	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652 2660 2668 2676 2684 2692	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2663 2677 2685 2693	2566 2574 2582 2598 2606 2614 2622 2630 2638 2646 2654 2662 2670 2678 2686 2694	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2647 2655 2663 2671 2687 2687		5410 5420 5430 5440 5450 5460 5470 5500 5510 5520 5530 5550 5550 5550 5550 5550 555	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2904 2912 2920 2928 2926 2928 2936 2944	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913 2921 2929 2937 2945	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2906 2914 2922 2930 2938 2946	2819 2827 2835 2843 2859 2867 2875 2883 2891 2899 2907 2915 2923 2931 2939 2939 2939	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908 2916 2924 2924 2932 2940 2948	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909 2917 2925 2933 2941 2949	2822 2830 2838 2846 2854 2854 2870 2878 2886 2894 2902 2910 2918 2926 2934 2942 2950	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911 2919 2927 2927 2943 2951
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to 5777 3071 (Octal) (Decimal)	5010 5020 5040 5050 5060 5070 5100 5120 5130 5140 5150 5140 5150 5140 5120 5220	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664 2664 2664 2688	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2655 2665 2673 2681 2689 2697 2705	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2658 2666 2658 2666 2674 2682 2690 2698 2706	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2667 2675 2683 2691 2699 2707	2564 2572 2580 2588 2604 2612 2620 2628 2636 2644 2652 2668 2668 2668 2668 2668 2668 2668	2565 2573 2581 2589 2605 2613 2621 2629 2637 2645 2653 2669 2669 2669 2669 2693 2693 2701 2709	25566 2574 2582 2598 2606 2614 2622 2630 2638 2646 2654 2670 2678 2686 2694 2694 2702 2710	2567 2575 2583 2599 2607 2615 2623 2631 2639 2647 2655 2663 2671 2679 2687 2695 2703 2711		5410 5420 5430 5440 5460 5460 5560 5510 5520 5520 5520 5520 5550 5550 555	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2912 2920 2928 2936 2944 2952 29260	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913 2921 2929 2937 2945 2953 2961	2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898 2906 2914 2922 2930 2938 2946 2954 2954	2819 2827 2835 2843 2859 2867 2875 2883 2891 2899 2907 2915 2923 2931 2939 2947 2955 2963	2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900 2908 2916 2924 2932 2940 2924 2924 2924 2956 2964	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2909 2917 2925 2933 2941 2949 2957 2965	2822 2830 2838 2846 2854 2854 2870 2878 2886 2894 2902 2910 2918 2926 2934 2942 2950	2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903 2911 2919 2927 2935 2943 2951 2959 2951
to 5777 3071 (Octal) (Decimal)	5010 5020 5040 5050 5050 5070 5100 5110 5120 5130 5140 5160 5170 5200 5220 5220 5230	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2648 2648 2656 2664 2672 2688 2696 2702 2688 2696 2712 2712 2712	2561 2569 2577 2585 2593 2609 2617 2625 2633 2641 2649 2657 2665 2673 2661 2689 2697 2705 2705 2713 2711	2562 2570 2578 2586 2594 2610 2618 2626 2634 2650 2658 2666 2674 2682 2690 2698 2706 2698 2704	2563 2579 2579 2603 2611 2619 2627 2635 2643 2651 2659 2667 2675 2683 2691 2699 2707 2715 2723	2564 2572 2580 2596 2604 2612 2620 2628 2632 2644 2652 2660 2668 2676 2684 2692 2700 2708 2700 2708 2716 2724	2565 2573 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669 2677 2685 2693 2701 2709 2707 2717 2717	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2662 2670 2678 2686 2694 2710 2710 2718 2718	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2671 2679 2687 2695 2703 2711 2719		5410 5420 5430 5450 5460 55470 5540 5550 5550 5550 5550 5550 55	2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2896 2912 2920 2924 2920 2928 2934 2936 2952 2968 2936	2817 2825 2833 2841 2849 2857 2865 2873 2861 2887 2905 2913 2929 2937 2929 2937 2945 2953 2969 2969	2818 2826 2834 2842 2850 2858 2866 2874 2890 2994 2990 2938 2946 2954 2954 2970 2978	2819 2827 2835 2843 2851 2857 2875 2883 2891 2997 2915 2923 2931 2939 2947 2955 2963 2971 2979	2820 2828 28366 2844 2852 2860 2868 2876 2900 2908 2916 2924 2930 2948 2930 2949 2949 2949 2956 2954 2956	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901 2917 2925 2933 2941 2949 2957 2955 2973 2981	2822 2830 2838 2846 2854 2870 2878 2878 2878 2994 2910 2918 2916 2934 2942 2950 2958 2956 2954 2956	2823 2831 2839 2847 2855 2863 2879 2887 2895 2903 2911 2919 2927 2935 2943 2951 2959 2967 2975 2983
to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5050 5070 5100 5110 5120 5130 5140 5150 5170 5220 5220 5220 5220 5220 5220 5220 52	2560 2568 2576 2584 2592 2600 2616 2624 2632 2664 2656 2664 2656 2664 2664 2664 266	2561 2569 2577 2585 2593 2601 2617 2625 2663 2641 2649 2655 2663 2665 2663 2665 2665 2665 2665	2562 2570 2578 2594 2602 2618 2626 2658 2658 2656 2658 2666 2674 2682 2666 2674 2682 2666 2674 2668 2714	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2657 2667 2667 2667 2667 2667 2667 2667	2564 2572 2580 2588 2596 2604 2628 2662 2668 2664 2668 2668 2668 266	2565 2573 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669 2677 2685 2693 2701 2709 2717 2725 2773	2566 2574 2582 2590 2598 2606 2622 2630 26632 26632 26632 26634 2662 26674 2662 26674 2662 2670 22778 2686 2694 2710 2718 2776 2776 2776 2776 2776 2776 2776 277	2567 2575 2583 2591 2607 2607 2623 2631 2639 2647 2655 2663 2663 2667 2667 2667 2667 2667 2667		5410 5420 5430 5440 5450 5450 5550 5550 5550 555	2816 2824 2832 2840 2848 2856 2864 2872 2880 2912 2920 2928 2930 2928 2936 2952 2954 2952 2956 2954 2956 2954	2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897 2905 2913 2921 2929 2937 2929 2937 2945 2953 2961 2965	2818 2826 2834 2850 2858 2866 2874 2882 2890 2914 2922 2930 2938 2946 2954 2954 2976 2978	2819 2827 2835 2843 2851 2857 2867 2875 2883 2891 2997 2915 2923 2931 2939 2947 2955 2963 2979 2987	2820 2828 2836 2844 2852 2868 2876 2884 2892 2900 2908 2916 2924 2932 2932 2932 2934 2956 2954 2974 2975	2821 2829 2837 2845 2869 2893 2901 2909 2917 2925 2933 2941 2949 2957 2949 2957 2949 2957 2949	2822 2830 2838 2846 2854 2862 2870 2878 2894 2902 2910 2918 2926 2934 2924 2934 2950 2958 2954 2954 2954	2823 2831 2839 2847 2855 2863 2877 2895 2993 2911 2919 2927 2935 2943 2951 2959 2959 2959 2959 2967 2959 2983 2991
to to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5100 5110 5120 5130 5140 5150 5140 5150 5140 5210 5220 5220 5220 5220 5220 5220 522	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2648 2648 2648 2648 2648 2648 2648	2561 2569 2577 2585 2593 2601 2617 2625 2633 2641 2649 2657 2665 2673 2661 2689 2667 2705 2713 2721 2729 2729 2737	2562 2570 2578 2586 2594 2602 2610 2618 2626 2654 2652 2658 2666 2674 2682 2690 2698 2706 2714 2722 2730 2738	2563 2571 2579 2587 2595 2603 2611 2659 2663 2651 2659 2667 2663 2667 2663 2667 2663 2669 2707 2715 2723 2731	2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644 2652 2660 2668 2668 2668 2668 2668 2676 2668 2770 2770 2770 2772 2772 2732 2740	2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645 2653 2661 2669 2667 2665 2693 2701 2709 2717 2725 2733 2733 2733	2566 2574 2582 2590 2598 2606 2614 2622 2638 2664 2654 2664 2664 2667 26670 2678 2678 2678 2678 2678 2679 27712 27712 2774 27742	2567 2575 2583 2591 2607 2607 2623 2631 2639 2647 2653 2663 2663 2663 2663 2663 2671 2679 2687 2703 2711 2719 2727 2735 2773		5410 5420 5430 5440 5540 5540 5550 5550 5550 555	2816 2824 2832 2840 2848 2856 2864 2912 2920 2928 2920 2928 2928 2928 2936 2944 2952 2952 2952 2954 2954 2954	2817 2825 2833 2841 2849 2857 2865 2873 2885 2895 2905 2913 2921 2929 2937 2945 2953 2961 2969 2977 2985 2993	2818 2826 2834 2858 2858 2858 2858 2858 2858 2890 2898 2996 2994 2992 2938 2944 2954 2954 2955 2962 2970 2978	2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2907 2915 2923 2931 2939 2947 2955 2953 2951 2959 2957	28200 28288 28366 2864 2852 2860 2988 2916 2924 2932 2932 2932 2932 29340 2948 2956 2954 2956 2954 2956 2954	2821 2829 2837 2845 2853 2869 2877 2909 2917 2925 2933 2931 2941 2949 2957 2957 2957 2957 2957 2957 2957	2822 2830 2838 2846 2854 2870 2878 2878 2878 2994 2910 2918 2916 2934 2942 2950 2958 2956 2954 2956	2823 2831 2839 2847 2855 2903 2911 2919 2927 2935 2943 2959 2967 2967 2995 29991
to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5070 5100 5110 5120 5130 5140 5150 5160 5170 5220 5220 5220 5220 5220 5220 5220 52	2560 2558 2558 2584 2592 2600 2608 2616 2624 2648 2648 2648 2648 2648 2648 264	2561 2559 2557 2583 2601 2609 2617 2625 2633 2641 2649 2657 2665 2663 2663 2663 2663 2673 2663 2673 2705 2713 2729 2727 2729 2737 2745	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2650 2658 2656 2658 2666 2658 2666 2658 2662 2674 2682 2674 2690 2698 2714 2732 2730 2738 2746	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667 2665 2663 2667 2665 2663 2667 2675 2663 2677 2675 2663 2777 2715 2723 2773 2773 2773 2773 2774	2564 2572 2580 2588 2596 2604 2612 2620 2628 2634 2652 2666 2664 2664 2662 2666 2668 2664 2662 2676 2676 2700 2708 2710 2724 2724 2724 2724	2565 2573 2581 2589 2605 2613 2629 2637 2645 2653 2669 2667 2669 26677 2685 2669 2701 2709 2717 2725 2733 2741 2749	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2654 2654 2654 2654 2654 2678 2686 2702 2710 2718 2776 2774 2776 2774 27750	2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647 2655 2663 2679 2687 2687 2695 2703 2711 2719 2712 2712 2727 2735 2743 2751		5410 5420 5430 5440 5440 5440 5540 5540 5550 555	2816 2824 2832 2840 2848 2856 2864 2872 2880 2994 2992 2928 2936 2944 2952 2952 2960 2964 2954 2952 2976 2984 2992 3000	2817 2825 2833 2841 2849 2857 2865 2913 2905 2913 2921 2929 2937 2945 2953 2961 2969 2937 2961 2969 2933 3001	2818 2826 2826 2850 2858 2866 2874 2890 29914 2922 2930 2938 2946 2954 2954 2954 2978 2978 2986 2994 3002	2819 2827 2843 2851 2859 2867 2875 2883 2897 2915 2923 2931 2939 2947 2955 2963 2979 2987 2995 3003	2820 2828 2836 2844 2852 2860 2868 2900 2900 2908 2916 2924 2932 2932 2940 2948 2956 2954 2978 29780 2988 2996 3004	2821 2829 2837 2845 2853 2861 2869 2877 2909 2917 2925 2933 2941 2949 2957 2949 2957 2945 2973 2981 2989 2997 3005	2822 2830 2838 2846 2854 2862 2870 2910 2918 2926 2934 2934 2934 2934 2950 2938 2956 2974 2958 2956 2978 2982 2990 2998 3006	2823 2831 2839 2847 2855 2903 2911 2919 2927 2935 2943 2951 2959 2967 2975 2943 29959 2967 2975 2983 2993
to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5100 5110 5120 5130 5150 5150 5150 5210 5220 5220 5220 522	2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640 2648 2656 2664 2672 2680 2688 2696 2704 2712 2772 2778 2774	2561 2569 2569 2593 2601 2609 2617 2625 2633 2641 2649 2657 26657 2663 2663 2663 2663 2705 2713 2729 2775 2737 2745	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2642 2658 2658 2658 2668 2668 2674 2682 2698 2776 2730 2778 2778 27754 2762	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2659 2667 2675 2683 2699 2707 2715 2723 2731 2739 2747 27755 2763	2564 2572 2580 2588 2596 2604 2612 2622 2662 2648 2644 2652 2660 2668 2664 2700 2708 2708 2770 2778 2770 2778 2774 2774	2565 2573 2581 2589 2597 2605 2663 2661 2662 2653 2661 2669 2677 2685 2663 2661 2669 2677 2685 2701 2770 2770 2770 2773 2741 2749 2757 2765	2566 2574 2582 2590 2598 2606 2638 2644 2654 2662 2662 2662 2662 2662 2662	2567 2575 2583 2591 2607 2607 2615 2623 2647 2655 2663 2663 2663 2663 2663 2667 2665 2703 2711 2719 2727 2743 2743 2743 2751		5410 5420 5430 5440 5440 5540 5540 5550 5550 555	2816 2824 2832 2840 2856 2864 2872 2880 2994 2912 2920 2928 2936 2994 2956 2968 2976 2984 2956 2968 2976 2984 2996 3000 3008 3016	2817 2825 2833 2849 2857 2865 2873 2865 2913 2905 2913 2929 2937 2945 2959 2951 2959 2951 2969 2977 2965 2969 2977 2965 2993 3001 3009	2818 2826 2834 2842 2858 2858 2858 2858 2858 2858 2930 2914 2922 2930 2930 2938 2946 2954 2952 2970 2978 2986 2994 3002 3010	2819 2827 2825 2843 2859 2867 2875 2883 2897 2907 2915 2923 2931 2939 2997 2953 2963 2971 2979 2987 2995 3003 3011 3019	2820 2828 2836 2844 2852 2860 2908 2908 2916 2924 2932 2940 2948 2956 2954 2954 2954 2956 2964 2972 2988 2996 3004 3012	2821 2829 2837 2845 2853 2861 2869 2877 2905 2933 2941 2941 2949 2957 2965 2973 2985 2973 2985 2997 3005	2822 2830 2838 2846 2854 2854 2852 2870 2878 2910 2918 2918 2926 2934 2942 2958 2958 2958 2966 2974 2988 3006 3014	2823 2831 2839 2847 2855 2903 2911 2919 2927 2935 2943 2951 2951 2951 2955 2967 2975 2983 2991 3007 3015 3023
to 5777 3071 (Octal) (Decimal)	5010 5020 5030 5040 5050 5060 5060 5100 5120 5130 5130 5140 5150 5150 5150 5220 5220 5220 5220 522	2560 2558 2558 2584 2592 2600 2608 2616 2624 2632 2648 2648 2648 2648 2648 2648 2648 264	2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2649 2657 2665 2633 2667 2705 2713 2705 2713 2721 2729 2737 2745 2745 2745	2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2650 2658 2666 2658 2666 2658 2666 2658 2667 2698 2704 2772 27738 27746 27742 27762 27762	2563 2571 2579 2587 2595 2603 2611 2619 2627 2635 2643 2651 2659 2667 2663 2667 2663 2667 2663 2667 2663 2675 2675 2773 2773 2773 2747 2747 2755 2763 2771	2564 2572 2580 2588 2596 2604 2612 2620 2628 2634 2652 2664 2662 2664 2662 2668 2664 2662 2676 2688 2700 2708 2774 2774 2774 2774	2565 2573 2581 2587 2605 2613 2629 2637 2645 2653 2663 2663 2701 2705 2773 2775 2773 2774 2775 2773 2741 2749 2757 2749	2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646 2654 2662 2670 2678 2668 2678 2678 2702 2710 2718 2774 27750 2750 2758 2774	2567 2575 2583 2591 2599 2607 2615 2623 2631 2632 2647 2655 2663 2671 2663 2671 2687 2673 2777 2733 2771 2733 2751 2755		5410 5420 5430 5450 5460 55470 5510 5550 5550 5550 5550 5550 5550 55	2816 2824 2832 2840 2848 2856 2864 2872 2880 2994 2992 2928 2936 2944 2952 2952 2956 2954 2994 2995 2976 2984 2995 2976 3000 3008 3016 3024	2817 2825 2833 2841 2849 2857 2865 2913 2905 2913 2921 2929 2937 2945 2953 2961 2967 2977 2985 2993 3001 3009	2818 2826 2826 2850 2858 2866 2874 2890 29914 2922 2930 2938 29946 2954 2954 2954 2978 2986 2994 3002 3010 3018 3026	2819 2827 2843 2853 2859 2867 2875 2883 2897 2915 2923 2931 2939 2947 2955 2963 2979 2979 2979 2979 2987 3003 3011 3019	2820 2828 2836 2844 2852 2860 2868 2900 2900 2908 2916 2924 2932 2932 2932 2940 2948 2956 2964 2972 2980 2988 2996 3004 3004	2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2909 2917 2925 2933 2941 2949 2957 2949 2957 2981 2989 2997 3005 3013 3021	2822 2830 2838 2846 2854 2862 2870 2910 2918 2926 2934 2934 2934 2934 2934 2935 2935 2934 2935 2935 2935 2935 2934 2935 3006 3014 3022 3030	2823 2831 2839 2847 2855 2903 2891 2911 2919 2927 2935 2943 2951 2959 2963 2995 2943 2995 2983 2991 2993 3007 3015 3023 3031
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#### OCTAL-DECIMAL INTEGER CONVERSION TABLE

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		3088						5 3086 3 3094			6420					3348		3350		to	to
		3096							3103		6430							3358	3359	6777 (Octal)	3583 (Decimal)
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			3121					5 3126			6460				3379			3382		Octal	Decimal
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			3169					3174			6540			3426	3427		3429		3431	70000 -	
	150 160				3179	3180 3188			3183 3191		6550 6560	3432	3433 3441	3434 3442		3436 3444		3438 3446	3439 3447	,0000	20072
								3198			6570			_		3452		3454	3455		
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			3209	3210							6610	3464	3465	3466	3467	3468	3469	3470	3471		
	220   3 230   3		3217 3225					3222 3230			6620 6630		3473 3481	3474 3482	3475	3476 3484	3477		3479		
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	260 3		3249	3250	3251	3252	3253	3254	3255	- 10	6660	3504	3505	3506	3507		3509		3511		
62	270 3	3256	3257	3258	3259	3260	3261	3262	3263	0	6670	3512	3513	3514	3515	3516	3517	3518	3519		
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1	20 3			3282				3286	3287			3536				3540	3541		3543		
	30 3		3289	3290	3291	3292		3294	3295				3545	3546	3547	3548			3551		
	40 3		3297	3298	3299	3300		3302	3303				355 <b>3</b>		3555				3559		
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701 702 703 704 705 706 707 710 711 712 713 714 715 716 717 720 721 722 723 724 725 726 727 720 721 720 721 720 721 720 721 722 723 724 725 726 727 727 727 727 720 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 705 706 707 707 705 706 707 705 706 707 705 706 707 707 707 707 705 707 707 707 707 707	00         35           010         35           200         36           200         36           200         36           300         36           300         36           300         36           300         36           300         36           300         36           300         36           300         36           300         37      <	584         3           592         3           5600         3           5600         3           5616         3           5624         3           5640         3           5640         3           5640         3           5640         3           5642         3           5643         3           5644         3           7704         3           7720         3           7728         3           762         3           766         3           776         3           7884         3	3585 3593 3601 3609 3617 3625 36633 3641 3669 3657 3665 3663 36649 36657 36657 36657 36657 36657 36657 36649 36697 3705 3713 3729 3737 3745 3753 3761 3769	3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3666 3674 3682 3698 3706 3714 3722 3730 3778 3778 3778	3587 3595 3603 3611 3619 3627 3635 3643 3651 3663 3667 3663 3667 3663 3669 3707 3715 3723 3731 3779 3779 3779 3787	3588 3596 3604 3612 3620 3628 3668 3668 3668 3668 3668 3668 3700 3708 3716 3724 3732 3740 3748 3754 3772 3780	3589 35597 3605 3613 3621 3663 3663 3663 3663 3669 3677 3685 3703 3709 3717 3725 3733 3741 3749 3757 3773 3773 37781	3590 3598 3606 3614 3622 3630 3638 3646 3654 3664 3664 3664 3664 3664 3664	3591 3507 3615 3623 3631 3639 3647 3655 3663 3667 3667 3667 3667 3667 366	77777777777777777777777777777777777777	4410           4420           4430           4430           440           440           450           440           450           440           450           440           450           500           510           520           530           540           550           560           570           600           610           620           630           640           650           670           700	3840 3848 3856 3864 3872 3980 3988 3986 3994 3920 3928 3936 3952 3952 3952 3952 3952 3952 3952 3952	3841 3849 3857 3865 3873 3881 3889 3921 3929 3937 3945 3953 3953 3953 3953 3953 3961 3969 3977 3965 3977 3965 3977 4001 4001 4001 4005 4003 4001	3842 3850 3858 3862 3874 3882 3890 3988 3946 3946 3954 3954 3954 3954 3954 3954 4002 4010 4018 4026 4034 4042	3843 3851 3859 3867 3875 3875 3883 3883 3883 3993 3947 3955 3963 3971 3979 3867 4003 4011 4019 4027 4035 4043	3844 3852 3860 3868 3876 3884 3930 3900 3908 3916 3924 3932 3940 3948 3946 3948 3956 3964 3972 3988 3996 4004	3845 3853 3861 3869 3877 3885 3893 3901 3909 3917 3949 3917 3949 3957 3957 3965 3973 3981 3897 4005 4013 4029 4037 4045	3846 3854 3862 3870 3878 3896 3894 3992 3910 3918 3926 3934 3958 3958 3958 3958 3958 3958 3958 3958	3847 3855 3863 3871 3879 3887 3887 3887 3895 3903 3911 3919 3927 3935 3943 3951 3959 3959 3959 3959 4007 4015 4023 4031 4039 4047	to 7777	to 4095
701 702 703 704 705 706 707 710 710 711 712 713 714 715 716 717 720 721 722 723 724 725 726 727 726 727 726 727 726 727 726 727 726 727 726 727 727	00         35           010         35           020         320           330         36           40         36           300         36           40         36           300         36           300         36           300         36           300         36           300         36           300         36           300         37 <t< td=""><td>584         3           5592         3           5592         3           5600         3           5616         3           5564         3           5566         3           5688         3           7704         3           728         3           760         3           7663         3           992         3           900         3</td><td>3585 3593 3601 3609 3617 36633 3641 3649 3657 3665 3667 3665 3667 3665 3667 3705 3713 3721 3729 3737 3745 3753 3761 3753 3761 3753 3769</td><td>3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3664 3668 3668 3668 3668 3668 3674 3682 3698 3706 3774 3770 3778 3754 3754 3754 3794</td><td>3587 3595 3603 3611 3619 3627 3635 3643 3651 3663 3667 3683 3693 3707 3715 3773 3775 3773 3775 3775 3775 377</td><td>3588 3596 3604 3612 3620 3628 3636 3644 3652 3660 3668 3664 3664 3664 3664 3700 3708 3716 3770 3770 3770 3774 3772 3776 3776 37780 37780 37780 37780 37780</td><td>3589 3597 3605 3613 3621 3623 3623 3645 3663 36645 3663 3667 3665 3693 3701 3772 3773 3775 3773 3775 3773 3757 3757</td><td>3590 3598 3606 3614 3622 3630 3638 3646 3654 3664 3654 3668 3694 3702 3718 37726 3734 37726 37734 3774 3753 3758 3758 3798</td><td>3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3679 3687 3695 3703 3711 3719 3727 3735 3743 3759 3769 3799</td><td>77777777777777777777777777777777777777</td><td>410           4420           4430           4430           4430           4430           4450           4450           4450           4450           4450           4450           4450           4450           550           550           550           550           550           550           550           550           550           560           610           620           630           640           650           670           7700           7730</td><td>3840 3848 3856 3864 3872 3880 3994 3912 3923 3928 3936 3944 3952 3960 3968 3976 3984 3992 4000 4008 40016 4024 4032 4048 4056</td><td>3841 3849 3857 3865 3913 3989 3937 3945 3953 3953 3961 3969 3997 3985 3993 3961 4009 4017 4025 4033 4041</td><td>3842 3850 3858 3866 3974 3996 3914 3922 3930 3938 3945 3954 3962 3970 3978 3986 3994 4002 4010 4018 4026 4034 4058</td><td>3843 3851 3859 3867 3915 3923 3931 3939 3947 3955 3963 3979 3987 3987 3987 3987 4003 4001 4019 4027 4035 4051</td><td>3844 3852 3860 3868 3868 3876 3892 3900 3908 3916 3924 3940 3940 3943 3940 3943 3956 3956 3956 3964 4004 4012 4020 4028 4036 4044 4052</td><td>3845 3853 3861 3869 3877 3909 3917 3925 3993 3991 3941 3949 3957 3965 3973 3965 3981 3989 3997 4005 4013 4021 4021 4023</td><td>3846 3854 3862 3870 3878 3896 3894 3902 3918 3926 3934 3958 3958 3966 3968 3990 3998 3990 3998 4006</td><td>3847 3855 3863 3871 3895 3903 3911 3919 3927 3935 3943 3951 3959 3967 3975 3983 3991 3999 3967 4015 4023 4031 4039 4047</td><td>to 7777</td><td>to 4095</td></t<>	584         3           5592         3           5592         3           5600         3           5616         3           5564         3           5566         3           5688         3           7704         3           728         3           760         3           7663         3           992         3           900         3	3585 3593 3601 3609 3617 36633 3641 3649 3657 3665 3667 3665 3667 3665 3667 3705 3713 3721 3729 3737 3745 3753 3761 3753 3761 3753 3769	3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3664 3668 3668 3668 3668 3668 3674 3682 3698 3706 3774 3770 3778 3754 3754 3754 3794	3587 3595 3603 3611 3619 3627 3635 3643 3651 3663 3667 3683 3693 3707 3715 3773 3775 3773 3775 3775 3775 377	3588 3596 3604 3612 3620 3628 3636 3644 3652 3660 3668 3664 3664 3664 3664 3700 3708 3716 3770 3770 3770 3774 3772 3776 3776 37780 37780 37780 37780 37780	3589 3597 3605 3613 3621 3623 3623 3645 3663 36645 3663 3667 3665 3693 3701 3772 3773 3775 3773 3775 3773 3757 3757	3590 3598 3606 3614 3622 3630 3638 3646 3654 3664 3654 3668 3694 3702 3718 37726 3734 37726 37734 3774 3753 3758 3758 3798	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3679 3687 3695 3703 3711 3719 3727 3735 3743 3759 3769 3799	77777777777777777777777777777777777777	410           4420           4430           4430           4430           4430           4450           4450           4450           4450           4450           4450           4450           4450           550           550           550           550           550           550           550           550           550           560           610           620           630           640           650           670           7700           7730	3840 3848 3856 3864 3872 3880 3994 3912 3923 3928 3936 3944 3952 3960 3968 3976 3984 3992 4000 4008 40016 4024 4032 4048 4056	3841 3849 3857 3865 3913 3989 3937 3945 3953 3953 3961 3969 3997 3985 3993 3961 4009 4017 4025 4033 4041	3842 3850 3858 3866 3974 3996 3914 3922 3930 3938 3945 3954 3962 3970 3978 3986 3994 4002 4010 4018 4026 4034 4058	3843 3851 3859 3867 3915 3923 3931 3939 3947 3955 3963 3979 3987 3987 3987 3987 4003 4001 4019 4027 4035 4051	3844 3852 3860 3868 3868 3876 3892 3900 3908 3916 3924 3940 3940 3943 3940 3943 3956 3956 3956 3964 4004 4012 4020 4028 4036 4044 4052	3845 3853 3861 3869 3877 3909 3917 3925 3993 3991 3941 3949 3957 3965 3973 3965 3981 3989 3997 4005 4013 4021 4021 4023	3846 3854 3862 3870 3878 3896 3894 3902 3918 3926 3934 3958 3958 3966 3968 3990 3998 3990 3998 4006	3847 3855 3863 3871 3895 3903 3911 3919 3927 3935 3943 3951 3959 3967 3975 3983 3991 3999 3967 4015 4023 4031 4039 4047	to 7777	to 4095
701 702 703 704 705 706 707 710 711 712 713 714 715 714 717 712 713 714 717 712 713 714 717 712 713 714 717 712 713 714 717 712 713 714 715 716 717 715 717 715 717 715 717 715 717 715 717 715 717 715 717 717	00         35           10         352           20         320           360         36           40         36           300         36           40         36           300         36           40         36           300         36           300         36           300         36           300         36           300         37	584         3           5592         3           5592         3           5600         3           5616         3           5624         3           5556         3           5566         3           5556         3           5640         3           5556         3           5688         3           5688         3           704         3           720         3           752         3           768         3           768         3           764         3           764         3           768         3           768         3           768         3           768         3           768         3           768         3           768         3           784         3           3000         3           3000         3	3585 3593 3601 3609 3617 3625 3633 3641 3649 3657 3661 3665 3673 3661 3669 3705 3713 3729 3737 3745 3737 3745 3753 3761 3769 3777 3769	3586 3594 3602 3610 3618 3626 3653 3654 3653 3666 3674 3692 3690 3698 3706 3714 3722 3730 3778 3776 3778 3778 3778 3778	3587 3595 3603 3611 3619 3627 3635 3643 3651 3663 3663 3663 3663 3669 3707 3715 3723 3731 3779 3774 3775 3771 3775 3771 3775 3773 3775 3773	3588 3596 3604 3612 3620 3628 3636 3644 3652 3664 3664 3664 3664 3664 3708 3708 3708 3716 3772 37740 3778 37740 3778 37760 3778 37760 3778 37760 37788 37760 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 3788 37960 37660 37760 3780 3780 3780 3780 3780 3780 3780 378	3589 3597 3605 3613 3629 3667 36653 3665 36653 3665 3693 3701 3709 3717 3725 3773 3775 3775 3775 3775 3773 3757 3775 3775 3773 3757 3775	3590 3598 3606 3614 3622 3630 3654 3662 3678 3666 3678 3666 3674 3702 3710 3718 3776 3774 3753 3753 3753 3754 3754 3754 3754	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3671 3695 3703 3771 3795 3743 3759 3767 3775 3775 3775 3775	77777777777777777777777777777777777777	410           4420           4420           4430           4440           4450           4460           500           5510           5500           5500           5500           5500           5600           6600           6600           6600           6600           6600           6700           7000           7000           7100           7400	3840 3848 3856 3864 3872 3880 3988 3988 3992 3928 3936 3928 3936 3936 3936 3936 3944 3952 3960 3968 3976 3984 3992 4000 4008 4016 4024	3841 3849 3857 3865 3873 3889 3897 3905 3913 3929 3937 3945 3953 3961 3965 3993 4001 4009 4007 4025 4033 4041 4049	3842 3850 3858 3868 3874 3993 3996 3914 3923 3938 3945 3954 3954 3954 4002 4010 4018 4026 4034 4042 4058 4066	3843 3851 3859 3867 3875 3883 3899 3907 3915 3923 3939 3939 3947 3955 3963 3979 3987 3995 4003 3997 4003 4011 4019 4027 4035 4043 4059	3844 3852 3860 3868 3876 3884 3910 3992 3990 3948 3940 3948 3956 3964 3972 3988 3996 4004 4012 4028 4004 4028	3845 3853 3861 3869 3877 3909 3917 3925 3933 3941 3949 3957 3965 3973 3989 3987 4005 4013 4021 4029 4037 4045 4051	3846 3854 3862 3870 3878 3886 3992 3910 3918 3922 3950 3934 3950 3934 3950 3958 3956 3958 3990 3998 4006 4014 4022 4030 4024 4030	3847 3855 3863 3863 3871 3879 3887 3895 3903 3911 3919 3927 3935 3943 3951 3955 3943 3951 39567 3983 3991 4007 4015 4023 4031 4023 4031	to 7777	to 4095
701 702 703 704 705 706 707 710 711 712 713 714 715 716 717 720 723 724 725 726 727 730 731 732 733 734 735	00 35 10 35 10 35 10 35 10 35 10 36 10 37 10 38 10 37 10 37 10 38 10 37 10 38 10 37 10 38 10 37 10 37 10 38 10 37 10 38 10 37 10 38 10	584         3           5592         3           5592         3           6600         3           5616         3           5562         3           5563         3           5564         3           5563         3           5564         3           5563         3           704         3           704         3           702         3           704         3           752         3           768         3           3008         3           3008         3           3008         3           3166         3	3585 3593 3601 3609 3617 3625 3633 3641 3649 3657 3665 3665 3665 3665 3667 3705 3713 3721 3729 3775 3775 3775 3775 3775 3776 3777 37765 3777 3785 37793 38001	3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3666 3674 3682 3698 3706 3714 3722 3730 3778 3778 3778 3778 3778 3778 3778	3587 3595 3603 3611 3619 3627 3635 3643 3651 3663 3663 3663 3663 3663 3663 3763 3773 3775 3763 3773 377	3588 3596 3604 3612 3620 3628 3668 3668 3668 3668 3668 3668 3668	3589 35597 3605 3613 3623 36637 36645 36633 36645 36633 36645 36633 36645 36635 36645 36737 36645 36737 37709 37717 37755 37741 37749 37757 37741 37757 37753 37741 37753 37741 37753 37773 3781 37797 38055 3813 3821	3590 3598 3606 3614 3622 3630 3638 3646 3654 3664 3664 3664 3664 3664 3664	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3671 3679 3687 3695 3703 3711 3719 3727 3753 3775 3775 3775 3775 3775 3775	77777777777777777777777777777777777777	410           4420           4420           4430           440           440           440           440           440           440           440           440           440           440           440           440           440           440           500           510           550           550           550           550           550           550           550           550           550           560           570           600           610           620           640           650           700           710           720           740           750	3840 3848 3856 3864 3872 3903 3888 3994 3920 3920 3920 3928 3920 3928 3920 3928 3920 3942 3952 3952 3952 3956 39576 3954 4000 4008 4008 4004 4042 4040 4048 4054 4072	3841 3849 3857 3865 3873 3881 3889 3921 3929 3937 3945 3953 3953 3961 3969 3977 3985 3993 4001 4009 4017 4025 4033 4041 4049 4047	3842 3850 3858 3862 3874 3882 3890 3988 3914 3922 3930 3938 3946 3954 3954 3954 4002 4010 4018 4026 4034 4042 4050 4042 4050	3843 3851 3859 3867 3875 3923 3939 3939 3947 3955 3963 3971 3979 3987 3995 3963 3971 3979 3987 3995 3963 4011 4019 4027 4035	3844 3852 3860 3868 3876 3998 3916 3924 3932 3940 3943 3940 3943 3946 3956 3964 3972 39860 39860 39860 39863 39964 4012 4024 4028 4004 4028	3845 3853 3861 3869 3877 3885 3893 3991 3925 3933 3941 3949 3957 3965 3973 3957 3965 3997 4005 4003 4005 4003 4005 4005 4005 4005	3846 3854 3862 3870 3878 3878 3886 3894 3992 3910 3918 3926 3934 3942 3958 3958 3958 3958 3958 3958 3958 3958	3847 3855 3863 3871 3879 3895 3903 3911 3919 3927 3935 3943 3951 3959 3959 3959 3959 3959 3959 395	to 7777	to 4095
701 702 703 704 705 706 707 710 711 712 713 714 715 716 717 722 723 724 725 726 727 731 722 733 724 733 734 735 736	00         35           10         352           20         3220           360         366           3650         3660           3660         3660           360         3660           360         3660           30         36           40         36           60         3660           30         37	584         3           5592         3           5592         3           5600         3           5616         3           556         3           5566         3           572         3           5888         3           59640         3           7012         3           728         3           728         3           768         3           768         3           7768         3           3000         3           3000         3           3016         3           316         3	3585 3593 3601 3609 3617 3665 3625 3633 3641 3665 3665 3665 3665 3665 3713 3729 3745 3775 3775 3775 3775 3775 3775 3775	3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3666 3674 3682 3698 3706 3714 3722 3730 3738 3776 3778 3776 3778 3778 3778 3794 3802 3818 3826	3587 3595 3603 3611 3619 3627 3635 3643 3651 3667 3663 3667 3663 3667 3663 3675 3763 3777 3715 3723 3731 3737 3747 3775 3763 3771 3775 3767 37771	3588 3596 3604 3612 3620 3628 3668 3668 3664 3668 3668 3668 3668 366	3589 3597 3605 3613 3621 3663 3663 3663 36645 3663 36645 3663 3667 36655 3761 3709 3717 3725 3733 3741 37757 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 377777 3777777	3590 3598 3606 3614 3622 3630 3654 3662 3678 3666 3678 3668 3664 3702 3710 3718 3726 3774 3753 3753 3753 3754 3754 3754 3754	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3671 3679 3687 3687 3687 3695 3703 3711 3719 3727 3753 3773 3751 3759 3767 3775 3775 3783 3799 3807	77777777777777777777777777777777777777	410           4420           4420           4440           4450           4460           500           510           520           530           550           550           550           550           550           660           660           660           660           660           700           7700           7730           7750           7760	3840 3848 3856 3864 3872 3920 3988 3994 3912 3928 3928 3928 3936 3943 3952 3946 3952 3960 3968 3976 3984 3992 3968 4000 4008 4004 4002 4002 4048	3841 3849 3857 3865 3873 3983 3983 3929 3937 3945 3953 3953 3953 3953 3953 3953 3953	3842 3850 3858 3862 3874 3882 3890 3988 3946 3914 3922 3930 3938 3946 3954 3954 3954 3954 3954 3954 4010 4018 4026 4034 4050 4058 4058 4057 4082	3843 3851 3859 3867 3875 3923 3939 3947 3955 3943 3947 3955 3953 3947 3955 3979 3987 3979 3987 3979 4003 40011 4009 4007 4003 4051	3844 3852 3860 3868 3876 3998 3900 3908 3916 3924 3932 3940 3942 3940 3943 3956 3954 3956 3954 3956 3954 3956 3954 4020 4020 4022 4004 4052 4052 4056 4054 4076 4084	3845 3853 3861 3867 3885 3897 3909 3917 3925 3933 3941 3949 3957 3945 3957 3973 3981 3989 3997 3095 4013 4005 4005 4007 4045	3846 3854 3862 3870 3878 3886 3992 3910 3918 3922 3950 3934 3950 3934 3950 3958 3956 3958 3990 3998 4006 4014 4022 4030 4024 4030	3847 3855 3863 3871 3895 3903 3911 3919 3927 3935 3943 3959 3967 3975 3983 3991 3999 3983 3991 3999 3991 3999 3967 4015 4007 4015 4007 4015 4063	to 7777	to 4095

## APPENDIX V

## OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	. 100	. 125000	. 200	. 250000	. 300	.375000
.001	.001953	. 101	.126953	.201	.251953	.301	.376953
.002	.003906	. 102	.128906	. 202	. 253906	. 302	.378906
.003	005859	. 103	130859	. 203	. 255859	. 303	.380859
.004	.007812	.104	.132812	. 204	.257812	.304	.382812
.005	.009765	. 105	. 134765	. 205	. 259765	. 305	.384765
.006		.106	. 136718	. 206	. 261718	.306	
	.011718						.386718
.007	.013671	. 107	.138671	.207	. 263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	,017578	. 111	.142578	.211	, 267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	. 312	.394531
.013	.021484	. 113	.146484	.213	.271484	. 313	.396484
.014	.023437	.114	. 148437	.214	. 273437	.314	.398437
.015	.025390	. 115	. 150390	.215	. 275390	.315	. 400390
.016	.027343	.116	. 152343	.216	. 277343	.316	.402343
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.017	.029296	. 117	.154296	.217	. 279296	.317	.404296
.020	.031250	.120	.156250	. 220	.281250	. 320	.406250
.021	.033203	. 121	.158203	. 221	. 283203	. 321	.408203
.022	.035156	. 122	.160156	. 222	.285156	. 322	.410156
.023	.037109	. 123	.162109	.223	.287109	. 323	.412109
.024	.039062	. 124	.164062	. 224	. 289062	. 324	.414062
.025	.041015	. 125	. 166015	.225	.291015	.325	.416015
.026	.042968	. 126	. 167968	. 226	.292968	.326	.417968
.028	.042908	. 125	. 169921	. 220	. 294921	.327	.419921
.030	.046875	.130	.171875	. 230	. 296875	. 330	.421875
.031	.048828	. 131	.173828	. 231	.298828	. 331	.423828
.032	.050781	. 132	.175781	. 232	.300781	. 332	.425781
.033	.052734	. 133	.177734	. 233	.302734	. 333	.427734
.034	.054687	. 134	.179687	. 234	. 304687	. 334	.429687
.035	.056640	. 135	.181640	. 235	.306640	. 335	.431640
.036	.058593	. 136	. 183593	. 236	.308593	. 336	. 433593
.037	.060546	. 137	. 185546	.237	.310546	.337	.435546
.040	.062500	. 140	.187500	. 240	.312500	. 340	.437500
.041	.064453	.141	. 189453	. 241	.314453	.341	.439453
.042	.066406	. 142	. 191406	. 242	.316406	. 342	.441406
.043	.068359	. 143	. 193359	. 243	.318359	. 343	.443359
.044	.070312	. 144	. 195312	. 244	.320312	. 344	.445312
.045	.072265	. 145	. 197265	. 245	. 322265	. 345	.447265
.046	.074218	. 146	. 199218	.246	.324218	.346	.449218
.047	.076171	. 147	.201171	.247	. 326171	.347	.451171
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.050	.078125	. 150	.203125	. 250	.328125	. 350	.453125
.051	.080078	. 151	.205078	. 251	.330078	. 351	.455078
.052	.082031	. 152	.207031	. 252	.332031	. 352	.457031
.053	.083984	. 153	. 208984	. 253	. 333984	. 353	.458984
.054	.085937	.154	.210937	. 254	. 335937	. 354	.460937
.055	.087890	. 155	.212890	. 255	. 337890	. 355	.462890
,056	.089843	. 156	.214843	. 256	. 339843	. 356	.464843
.057	.091796	. 157	.216796	.250	.341796	.357	.466796
		1				1	
.060	. 093750	. 160	.218750	. 260	. 343750	.360	.468750
.061	.095703	, 161	.220703	. 261	.345703	.361	.470703
.062	.097656	. 162	. 222656	. 262	.347656	. 362	.472656
.063	.099609	. 163	.224609	. 263	.349609	. 363	.474609
.064	.101562	. 164	.226562	. 264	.351562	. 364	.476562
,065	. 103515	. 165	.228515	. 265	.353515	. 365	.478515
.066	. 105468	. 166	.230468	. 266	.355468	. 366	.480468
.067	. 107421	. 167	.232421	. 267	.357421	.367	.482421
		1				1 .	
.070	. 109375	. 170	.234375	. 270	. 359375	. 370	.484375
.071	. 111328	. 171	.236328	.271	.361328	.371	.486328
.072	.113281	. 172	.238281	. 272	.363281	. 372	.488281
.073	, 115234	. 173	.240234	.273	.365234	. 373	.490234
.074	. 117187	. 174	.242187	. 274	.367187	. 374	.492187
.075	.119140	. 175	.244140	.275	.369140	.375	.494140
	. 121093	. 176	.246093	. 276	. 371093	.376	.496093
076							
.076 .077	. 123046	. 177	.248046	. 277	.373046	.377	.498046

#### OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	. 000000	.000100	.000244	.000200	.000488	. 000300	. 000732
000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
000002	.000007	.000102	,000251	.000202	.000495	.000302	.000740
000003	.000011	.000103	.000255	.000203	.000499	. 000303	.000743
000004	.000015	.000104	,000259	.000204	.000503	. 000304	.000747
000005	.000019	.000105	.000263	.000205	.000507	. 000305	,000751
000006	.000022	.000106	000267	. 000206	.000511	.000306	.000755
000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
		.000110	.000274	.000210	.000518	.000310	.000762
000010	.000030	.000111	.000278	.000211	.000522	.000311	.000766
000011	.000034			.000212	.000526	.000312	.000770
000012	.000038	.000112	.000282	4	.000530	.000312	.000774
000013	.000041	.000113	.000286	.000213	•		
000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
000021	.000064	. 000121	.000308	.000221	.000553	. 000321	.000797
000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
000026	.000083	.000126	.000328	.000226	.000572	. 000326	.000816
000020	.000087	.000127	.000331	.000227	.000576	.000327	.000820
	.000091	.000130	.000335	.000230	.000579	.000330	.000823
000030	-	.000130	.000339	.000231	.000583	.000331	.000827
000031	.000095		.000343	.000232	.000587	.000332	.000831
000032	.000099	.000132		.000232	.000591	.000332	.000835
000033	.000102	.000133	.000347				
000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
000037	.000118	.000137	.000362	.000237	.000606	. 000337	.000850
000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
000041	,000125	.000141	.000370	.000241	.000614	.000341	.000858
000042	.000129	.000142	.000373	. 000242	.000617	.000342	.000862
000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
000045	.000141	.000145	.000385	.000245	,000629	.000345	.000873
000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
000050	.000152	.000150	000396	.000250	.000640	. 000350	.000885
000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
		.000153	.000408	.000253	.000652	.000353	.000896
000053	.000164	.000153	.000411	.000254	.000656	.000354	.000900
000054	.000167		.000411			.000355	.000900
000055	.000171	.000155	-	.000255	.000659		
000056	.000175	.000156	.000419	.000256	.000663	. 000356	.000907
000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
000063	.000194	.000163	.000438	.000263	,000682	. 000363	.000926
000064	.000198	.000164	.000442	. 000264	.000686	.000364	.000930
000065	.000202	.000165	.000446	. 000265	.000690	.000365	.000934
000066	,000205	.000166	.000450	.000266	.000694	.000366	.000938
000067	,000209	.000167	.000453	. 000267	,000698	.000367	.000942
000070	.000213	.000170	.000457	. 000270	.000701	.000370	.000946
000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
000072	.000225	.000173	.000469	.000273	.000713	.000373	.000957
000073	.000228	.000174	.000473	.000274	.000717	.000374	.000961
		.000175	.000476	.000275	.000720	.000375	.000965
000075	.000232		.000480			.000376	.000965
000076	.000236 .000240	.000176	.000484	.000276	.000724 .000728	.000377	.000988
000077							

### OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	,000702	.001716
000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	,000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001739
.000412	.001014	.000512	.001258	.000612	.001502		
.000412	.001018	.000513	.001262	.000613	.001506	.000712	.001747
.000413	.001022	.000514	.001266	.000613	.001510	.000713	.001750
				1		1	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	,001804
000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
		-		1			
.000440	.00109	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
. 000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
			.001434			.000770	.001922
.000470	.001190	.000570		.000670	.001678 .001682		.001922
.000471	.001194	.000571	.001438	.000671		.000771	
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701 .001705	.000776 .000777	.001945
.000477	.001216	.000577	.001461	.000677			

# **APPENDIX VI**

### Input/Output Typewriter Codes

CHARA UC	CTERS LC	CODE	CHARAG	CTERS LC	CODE
A	a	30	x	x	27
В	Ъ	23	Y	У	25
C	c	16	Z	Z	21
D	đ	22	)	0	56
E	e	20	¥	1	74
F	f	26	œ	2	<b>7</b> 0
G	g	13	#	3	64
Н	h	05	\$	4	62
I	i	14	%	5	66
J	j	32	¢	6	72
K	k	36	&	7	60
L	l	11	$\frac{1}{2}$	8	33
М	m	07	(	9	37
N	n	06	-	-	52
0	0	03	?	1	44
P	p	15	Π	1	54
Q	q	35	0	+	46
R	r	12	•	•	42
S	8	24	:	;	50
T	t	01	,	,	40
U	u	34	•	=	02
v	v	17	tab	tab	51
W	W	31	spe	ce	04
Backs	pace	61	Carris	ge Return	45
Lower	Case	57	Upper	Case	47

# **APPENDIX VII**

1	6 <b>11/1612</b> ]	PRINTER C	ODES	1	66 PRI	NTER CODES	
CHAR	CODE	<u>CHAR</u>	CODE	CHAR	COD	E <u>CHAR</u>	CODE
BLANK	20	:	00	BLANK	20	:	00
0	12	=	13	0	12	=	13
1	01	ŧ	14	1	01	ŧ	14
2	02	≤	15	2	02	≤	15
3	03	. %	16	3	03	%	52
4	04	E	17	4	04	С	17
5	05	/	21	5	05	/	21
6	06	C	32	6	06	C	32
7	07	,	33	7	07	9	33
8	10	(	34	8	10	(	34
9	11	$\rightarrow$	35	9	11	<b>→</b>	35
А	61	1	36	A	6 <b>1</b>	Ħ	36
В	62	۸	37	В	6 <b>2</b>	~	37
С	63	-	40	С	63	-	40
D	64	v	52	D	64	t	16
Ε	65	\$	53	E	65	\$	53
F	66	*	54	F	66	*	54
G	67	1	55	G	67	t	55
Η	70	ŧ	56	Н	70	¥	56
I	71	>	57	I	71	>	57
J	41	+	60	J	41	+	6 <b>0</b>
K	42	<	72	К	42	<	72
L	43	•	73	L	43	•	73
$\mathbf{M}$	44	)	74	м	44	)	74
Ν	45	2	75	N	45	2	75
0	46		<b>7</b> 6	0	46	?	76
Р	47	;	77	Р	47	;	77
Q	50			ଦ	50		
R	51			R		For scientific	
S	22			S	22	%,~ and \$ may	be replaced
Т	23			Т	23	with V, A or ¬r	espectively.
U	24			U	<b>24</b>		
V	<b>2</b> 5			v	25		
W	<b>2</b> 6			W	<b>2</b> 6		
Х	27			X	27		
Y	30			Y	30		
Z	31			Z	31		139

Rev. D

# **APPENDIX VIII**

## Flexowriter Codes

UC	LC	CODE	UC	LC	CODE
Α	a	30	Y	У	25
в	b	23	Z	a	21
С	с	16	0	0	56
D	d	22	l	1	74
Е	е	20	2	2	70
F	f	26	з	3	64
G	g	13	4	4	62
н	h	05	5	5	66
I	i	14	6	6	72
J	j	32	7	7	60
к	k	36	8	8	33
L	1	11	9	9	37
Μ	m	07	-	-	52
N	n	06	t	1	44
0	ο	03	(	)	54
Р	р	15	+	,	46
Q	q	35	=	•	42
R	r	12	:	;	50
S	S	24	CR Upper (	Case <b>(</b> UC)	45 47
Т	t	01	Lower (	Case (LC) Dace (BS)	57 61
U	u	34	Color S	hift (CS)	02 51
v	v	17	Stop Space	e (TAB)	43 04
w	w	31	Tape Fo Delete	eed	00 77
х	x	27	Defete		
Note:	1)	Leader - Blank tape, Stop - Stop Flexowrit		lete - Deleted	character
	2)	10, 40, 41, 53, 55, 63, 6	5, 67, 71,	73, 75, and 76	- illegal

# APPENDIX IX

## Magnetic Tape BCD Codes

Character	Code (Octal)	Character	Code (Octal)
А	61	2	02
В	62	3	03
С	63	4	04
D	64	5	05
E	65	6	06
F	66	7	07
G	67	8	10
Н	70	9	11
Ι	71	\$	60
J	41	-	<b>4</b> 0
K	42	(blank)	<b>2</b> 0
L	43	1	21
Μ	44	. (period)	73
Ν	45	\$	53
0	46	*	54
Р	47	, (comma)	33
Q	50	%	34
R	51	#	13
S	22	@	14
Т	23	д	74
U	24	0 (numerical zero)	12
v	25	record mark	32
W	26	0 (minus zero)	52
х	27	0 (plus zero)	72
Y	30	group mark	77
Z	31	tape m <b>a</b> rk	17
0	12		
1	01		

# APPENDIX X

## Punched Card Codes

Char	Card	BCD	Char	Card	BCD	Char	Card	BCD	Char	Card	BCD
			+	12	60	-	11	40			20
1	1	01	Α	12 1	61	J	11	<b>4</b> 1	1	0 1	21
2	2	02	в	1 <b>2</b> 2	<del>6</del> 2	к	11	42	S	0 2	22
3	3	03	С	12 3	63	L	11 3	43	Т	0 3	23
4	4	04	D	12 4	64	М	11 4	44	Ū	0 4	24
5	5	05	Е	12 5	65	Ν	11 5	45	v	05	25
8	6	06	F	12 8	66	0	11 6	46	w	0 6	26
7	7	07	G	12 7	67	P	<del>7</del> 1	47	x	9	27
8	8	10	H	12 8	70	ଢ	11 8	50	Y	0 8	30
9	9	11	I	12 9	71	R	11 9	51	Z	0 9	31
0	Ó	12									
Ŧ	8,3	13	•	12 8,3	73	\$	11 8, 3	53		о в, з	33
	8,4	14	)	8,3 12 8,6	74	*	11 8,4	54	(	0 8,4	34

# APPENDIX XI PROGRAMMING EXAMPLES

The following are several internal programming problems with solutions which illustrate various uses of the computer instructions. Some of the problems can be programmed in more than one way; but the method chosen, although in some cases not the best, serves well for illustration.

One programming convention, occurring throughout the examples, is used in most utility and general purpose programs developed by CONTROL DATA: The locations 0070 - 0077 of all storage banks are used for temporary or transient storage of data, counters, etc. These locations should be avoided for program, table, or constant storage.

PROBLEM: Set up a program switch so that as the switch is executed program control is alternately transferred to locations (r)W and (r)V. (W and V are any two arbitrary locations).

Location	<u>F</u>	<u>E</u>	<u>G</u>	Comments
(r)a	SRC		5252	5252 is an alternating pattern of zero and one bits
(r)a+2	PJF	03		If positive — Jump to (r)W
(r)a+3	JFI	01		Jump to (r)V
(r)a+4	V			
(r)a+5	JFI	01		Jump to (r)W
(r)a+6	W			

PROBLEM: Starting at location (i)0200 are 10<sub>8</sub> words of packed BCD data. Unpack these words into a one character per word format starting at location (i)0300 with the character in the lower half of the word. Assume the unpack area to be clear. NOTE: A BCD character is 6 bits long.

Location	E	<u>E</u>	G	Comments
(r)a	LDC		-10	Set loop counter
(r)u+2	STD	77		(d)0077 is counter location
(r)a+3	LDC		0300	FWA of unpacked area
<u>(r)a+5</u>	STD	76		Put in (d)0076
(r)a+6	ADN	01		A + 1 → A = 0301
(r)a+7	STD	75		Put in (d)0075
(r)a+10	LDC		0200	FWA of packed area
(r)a+12	STD	74		Put in (d)0074
(r)a+13	LDI	74		Packed word to A
(r)a+14	HWI	75		Lower character to unpacked area
(r)a+15	LS6			Shift left 6
(r)a+16	HWI	76		Upper character to unpacked area
(r)a+17	AOD	74		Increase addresses
(r)a+20	LDN	02		
(r)a+21	RAD	75		
(r)a+22	LDN	02		
(r)a+23	RAD	76		
(r)a+24	AOD	77		Loop counter + 1
(r)a+25	NZB	12		Return if not done

All done - Continue

PROBLEM:	Transfer 100	<sub>R</sub> words from	m location	(i)0700 to	location	(i)2300 and
	perform this d	s a JPR sul	proutine wh	nose entranc	e line is c	1.

Location	<u>F</u>	<u>E</u>	G	Comments
(r)a-1	JFI	01		Exit line
(r)a	*	*		Return address stored here
(r)a+1	LCC		100	Loop count to A
(r)a+3	STD	77		(d)0077 is count location
(r)a+4	LDC		0700	FWA or area one
(r)a+6	STF	05		Initialize a+13
(r)a+7	LDC		2300	FWA of area two
(r)a+11	STF	04		Initialize a+15
(r)a+12	LDM		**	Parameterized FWA of area one
(r)a+14	STM		**	Parameterized FWA of area two
(r)a+16	AOB	03		FWA + 1
(r)a+17	AOB	02		FWA + 2
(r)a+20	AOD	77		Count + 1
(r)a+21	NZB	07		Loop if not complete
(r)a+22	ZJB	23		Go to exit – all done

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**PROBLEM:** Count the number of positive, negative, and zero numbers in a table stored in (i)0100 to (i)0200. Put the 3 counts in locations (d)0070, (d)0071, and (d)0072. The program should start at location (r)0500.

Location	F	E	G	Comments
(r)0500	LDC		0100	Initialize table address
(r)0502	STF	06		Put in load command (r)0510
(r)0503	LDN	00		Set A = 0 to initialize counts
(r)0504	STD	70		Positive count = 0
(r)0505	STD	71		Negative count = 0
(r)0506	STD	72		Zero count = 0
(r)0507	LDM		0100	Table word to A
(r)0511	ZJF	10		Jump if zero to (r)0521
(r)0512	PJF	11		Jump if positive to (r)0523
(r)0513	AOD	71		Neg. Cnt. + 1
(r)0514	AOB	04		Tbl. addr. + 1
(r)0515	SBC		0201	Test for end of table
(r)0517	NZB	10		Return to (r)0507 if table not finished
(r)0520	ZJF	05		Exit — all done
(r)0521	AOD	72		Zero count + ]
(r)0522	NZB	06		Return to tally
(r)0523	AOD	70		Positive count + 1
(r)0524	NZB	10		Return to tally

**PROBLEM:** Set all storage locations in storage bank (1) between the limits (1) 0100 and (1) 7700 inclusive, equal to zero.

Location	<u>F</u>	<u>E</u>	G	Comments
(r)a	LDC		0100	FWA of area to A
(r)a+2	ATE		a+2	FWA to BER; if buffer busy, delay
(r)a+4	LDC		7701	LWA+1 to A
(r)a+6	ΑΤΧ		a+6	LWA+1 to BXR, if buffer busy, delay
(r)a+10	SBU	1		Set (b) = 1
(r)a+11	LDN	00		Set A = 0
(r)a+12	BLS		a+12	Start clear operation using the buffer
(r)a+14	NEXT	INST	RUCTIO	N

## APPENDIX XII PROGRAMMING SYSTEMS

The computing power, flexibility, and speed of the 8090 Computer are enhanced by the many programming systems developed by Control Data for the 160-A Computer. These programming systems include symbolic assemblers, compilers, and interpretive systems with languages suited for general-purpose calculational tasks. A growing library of SWAP (the 160-A Users Group) programs is also available to all 8090 users.

#### OSAS-A

A symbolic assembler, the OSAS-A provides fully symbolic coding, automatic address correspondence, code-error checking, and listing of source and object program. The object code may be in fixed or relocatable format. Full machine language of the 8090 is available in symbolic operation codes. Pseudo operations control the assembler and its translation of the source program.

#### FORTRAN

FORTRAN includes a compiler, a subroutine library, and an interpreter. Programs are written in an algebraic-like notation using symbolic identifiers. The language of the FORTRAN System is the FORTRAN-II language. The system provides all input-output routines for 8090 peripheral equipment, including the optional multiply-divide unit (8083).

#### SICOM

SICOM for the Control Data 8090 Computer is a general purpose interpretive system utilizing floating point arithmetic. With SICOM the 8090 becomes a decimal, floating point machine with a 10-decimal digit, plus exponent, word length. The SICOM library includes many arithmetic and trigonometric subroutines.

#### INTERFOR

INTERFOR is an interpretive programming system for the 8090 Computer. It contains a symbolic assembler (FLAP), a binary program loader (FLOADER), a library of subroutines, and an interpreter. The system provides six index registers and 33-bit floating point arithmetic. Programs may be written for this system which will also run on the 1604-A Computer.

#### CEPS

CEPS is a programming system for solving civil engineering problems on the Control Data 8090 Computer. It enables the engineer to express the solution of a problem in a language at approximately the same level which he could use in describing his solution to another engineer. CEPS is problem oriented, modular, and the instruction repertoire is expandable.

#### AUTOCOMM

Designed for commercial data processing applications, AUTOCOMM provides a method of quickly and easily translating business problems into 8090 Computer solutions. It includes all input-output, move, compare, and edit routines. In addition, AUTOCOMM is decimally oriented and utilizes powerful instructions to minimize programming time.

### **COMMENT SHEET**

CONTROL DATA 8090 COMPUTER SYSTEM Reference Manual – Pub. No. 60091500

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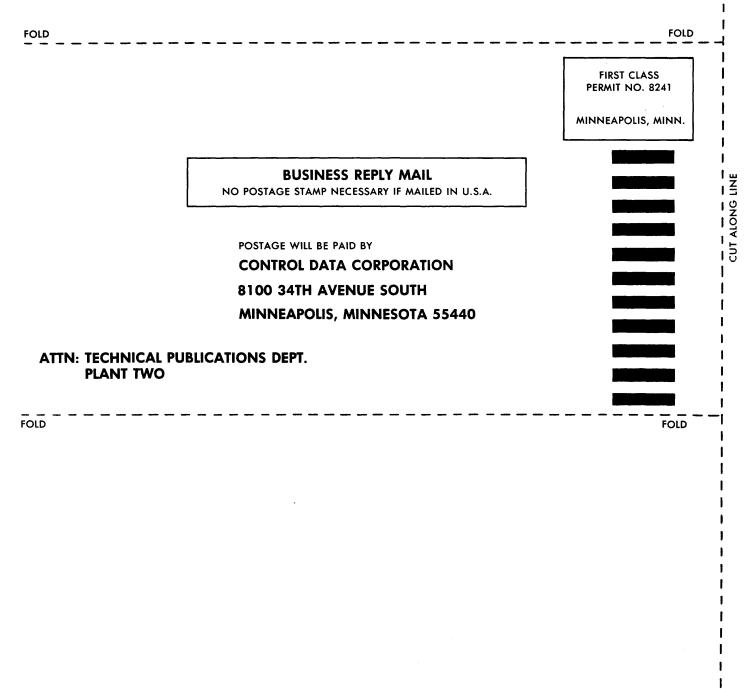
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