CONTROL DATA
CORPORATION

CONTROL DATA® 8092
TELEPROGRAMMER

CUSTOMER ENGINEERING MANUAL

Volume I of II

- Maintenance
- Installation
- Timing Charts
- Card Placement
- Equation Files
- Parts List

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INTRODUCTION

SCOPE

This manual contains maintenance information on the CONTROL DATA 8092-A, 8092-B, 8092-D, and 8092-E TeleProgrammer. Refer to the 8092 Customer Engineering Manual Volume II, publication number 41606100, for Wire Lists and Cable Tabs. The 8092 TeleProgrammer is a stored program processor especially designed as a high-speed buffer memory system and controller. The 8092 TeleProgrammer is used in a variety of data communication applications. The 8092-A, 8092-B, 8092-D, and 8092-E TeleProgrammer models are identical in operation and function with the following distinguishing characteristics:

(1) The 8092-A TeleProgrammer has a memory size of 2048 8-bit words.

(2) The 8092-B TeleProgrammer has a memory size of 4096 8-bit words.

(3) The 8092-D TeleProgrammer has a memory size of 4096 8-bit words and contains a 30-amp, 60-Hertz power supply, part no. 47054200.

(4) The 8092-E TeleProgrammer has a memory size of 4096 8-bit words and contains a 30-amp, 50-Hertz power supply, part no. 47054201.

CHAPTER ONE
MAINTENANCE

GENERAL

This volume presents complete logic maintenance information for the CONTROL DATA® 8092 TeleProgrammer. When mechanical adjustments are needed for the high speed punch, typewriter, etc., refer to commercial manuals supplied with those equipments.

System maintenance may be preventive or corrective. Preventive maintenance is designed to eliminate failures during operation by lubricating, cleaning, running test programs, and checking for worn or marginal parts. Corrective maintenance consists of diagnosing, locating, and remedying the cause of a failure after it has occurred.

TEST EQUIPMENT AND TOOLS

Standard VOM
Oscilloscope (Tektronix 543 or equivalent)
151 Card Tester
Taper Pin Insertion Tool
Taper Pin Crimping Tool
Card Extender
Usual hand tools for electrical and mechanical maintenance

CORRECTIVE MAINTENANCE AIDS

The ability of a maintenance engineer to locate malfunctions in the equipment depends upon knowledge of system logic, insight, and ability to use the maintenance aids. Maintenance aids in the TeleProgrammer instruction book series are:

Publication No.	Manual
368 105 00	Input/Output Specification
368 106 01	General Reference Manual
368 107 01	Programming Reference Manual
368 108 00	Customer Engineering Manual, Volume I
368 109 00	Equipment Diagrams (Logic and Electrical)
368 132 00	Test Routines
368 235 00	Basic Library System
416 061 00	Customer Engineering Manual, Volume II
368 150 00	8606 Power Supply Manual
601 207 00	Control Data Power Supplies (8092-D, -E)

LOGIC MAINTENANCE

TELEPROGRAMMER

Logic maintenance of the TeleProgrammer involves determination of the area to be investigated through maintenance tests, subsequent console diagnosis of instructions causing the malfunction, and examination of this area with an oscilloscope.

Maintenance tests will narrow the field of instruction suspected of giving trouble. The tests to be performed will be determined by the type of trouble: input, output, storage, and so forth.

The console with its display of register contents, status lights and operating controls provide for the first level of diagnosis. A test program indicates a malfunction and the general area of the TeleProgrammer causing it. To localize the failure to a given register or instruction the basic procedure at the console is to execute, in the step mode, the instructions which involve the area containing the malfunction. Compare the results displayed on the console with those known to be correct. Discrepancies may result from several possible causes. Enter more instructions (manually) and step through to eliminate causes. After several repetitions of this procedure, the area of malfunction will be determined.

After console diagnosis has indicated the circuits which may be causing the malfunction, examine these circuits with an oscilloscope.

In some cases observation of circuits in a static condition is sufficient; however, examination of dynamic circuit conditions is often required. This is done by repeated execution of an instruction that uses the circuit. To repeat an instruction, store it and a jump instruction in an unused area of storage to form a loop. The analyzing instruction may be repeated at high speed (Run) or by storage reference cycles (Step).

Information for localizing the malfunction to a group of circuits and then to an individual circuit is contain in:

1) instruction timing charts (chapter 4)
2) file of equations (appendix B)
3) logic diagrams (diagram volume)

The jack location and test point information required in taking waveforms for each circuit are provided by equations and diagrams.

Waveforms taken at the circuit test point by an oscilloscope indicate the circuit output. Test point waveforms are the inversion of the circuit inputs. The common ground connection for the oscilloscope is at the outer chassis edge. A synchronizing signal for the oscilloscope can be obtained from the test point of

another circuit. The synchronizing source should produce a signal just in advance of that time when a circuit is to be examined.

To examine signals on the individual pins of a card, remove the bar which holds the row of cards in position, remove the card, insert the card extender, and plug the card into the extender. Waveforms of representative cards provide a basis for determining the condition of the card under test.

PRINTED CIRCUIT CARDS

Corrective maintenance isolates the trouble to an electrical component such as a blown fuse, loose E-strip connection, broken cable lead, etc., or to an electronic component, such as a printed circuit card. This section provides a series of waveforms against which the individual cards may be compared, and gives procedures for determining which component on the faulty card is defective. A definitive analysis of each card is presented in the 151 Card Tester manual. For all waveforms the oscilloscope has been connected so that negative voltages produce upward deflection.

Logic Cards

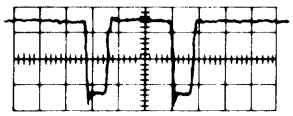
Logic cards are standard inverters (figure 1-1), control delays (figure 1-2), and flip-flops. The flip-flop waveform is not given, since the pulse width from this type of card is an arbitrary value depending on set and clear signals. The rise time of the pulse should be substantially under 0.1 usec. Anything slower than this approaches the area where clock pulses (nominally 0.167 usec wide) may not act on the pulse at the right time or, if they do, produce a runt pulse.

Storage Cards

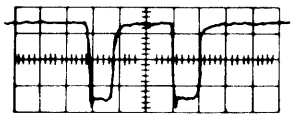
In general, these waveforms were taken with the TeleProgrammer in a loop, which accounts for the composite nature of the oscillograms. In figure 1-4, the waveform shows both the working time of the diverter (rectangular portion) and also the period when it is not in use (base line). Type 53 is omitted due to its similarity to the standard inverter card.

Adequate spares are provided for all card types in the system. If an oscilloscope check points to a card as the source of trouble, that card is replaced. The most definitive check on faulty cards is made with the card tester which will show up low beta transistors as well as shorted, open, or reversed diodes.

If a card tester is not available, the ohmic value of all resistive components, as well as the presence of open or shorted diodes, may be determined by using the OHMS setting of a standard VOM. The diodes used throughout the card types have a back resistance varying from 50K to 200K ohms. The forward resistance is a function of the current flowing through it. Average readings of 4-5 on the X1 scale, or 20-30 on the X10 scale are satisfactory. After determining the direction of current flow in the ohm meter circuit, it is well to mark the meter leads to facilitate future diode checking.



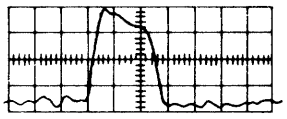
(a) Good inverter output (forced from "1" to "0" as a result of a 1 usec pulse recurring at 3.2 usec intervals.



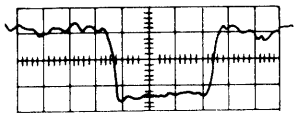
(b) Slow-fall inverter output (conditions as outlined above).

Vertical Sensitivity: 1 volt/cm
Sweep: 1 usec/cm

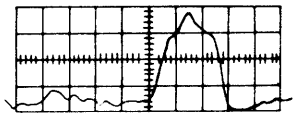
Figure 1-1 Standard Inverter Waveforms



(a) Clocked input to first inverter (H_1).



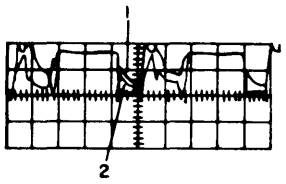
(b) Output from H_1 ("A" side of control delay card).



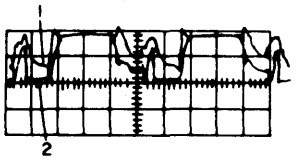
(c) Delayed output from V element.

Vertical Sensitivity: 1 volt/cm
Sweep: 0.1 usec/cm

Figure 1-2 Control Delay Waveforms



Read Side, Test Point A



Write Side, Test Point C

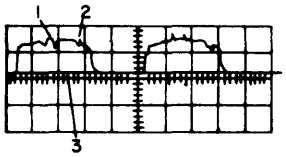
1) Rounded pulse is a reflected read pulse from another driver that is turned on when this one is off.

2) Squared off pulse shows when this driver is turned on.

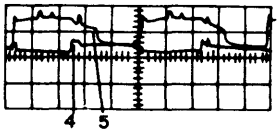
Vertical Sensitivity: 10 volts/cm

Sweep: 2 μsec/cm

Figure 1-3 Drive Generator (G10)



Good diverter



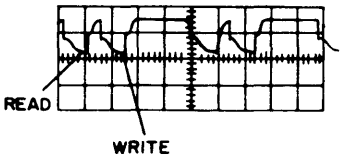
Bad diverter

1) End of read pulse
2) End of write pulse
3) Straight base line (a sign of a good diverter) shows time when diverter is on.
4) Step in base line indicates bad diverter due to faulty output transistor.
5) Slow drop off indicates marginal card.

Vertical Sensitivity: 5 volts/cm

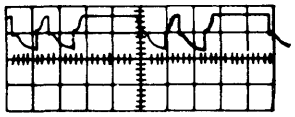
Sweep: 2 μsec/cm

Figure 1-4 Diverter (52A)



Vertical R/W source

Vertical and horizontal sources should be very similar

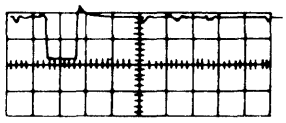


Horizontal R/W source

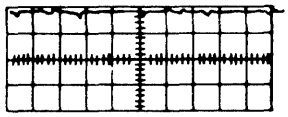
Vertical Sensitivity: 1 volt/cm

Sweep: 2 μsec/cm

Figure 1-5 Current Source (G12 & G13)



all "0's"

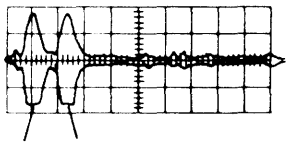


all "1's"

Vertical Sensitivity: 10 volts/cm

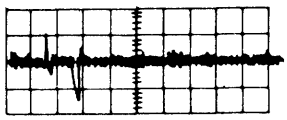
Sweep: 2 μsec/cm

Figure 1-6 Inhibit Generator (G11)

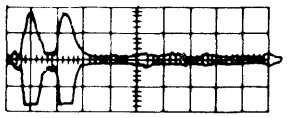


all "1's"

Test Point A



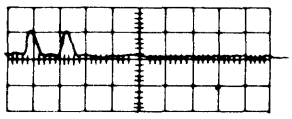
all "0's"



Test Point B

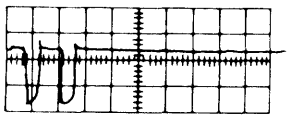
Test points A and B should yield essentially the same waveforms.

all "1's"



Test Point C

all "1's"



Test Point D

Vertical Sensitivity: 1 volt/cm

Sweep: 2 μsec/cm

all "1's"

Figure 1-7 Sense Amplifier (G14)

MAINTENANCE TESTS

A TeleProgrammer test routine manual (publication No. 368 132 00) is shipped with each TeleProgrammer. Consult this manual for test programs and routines that should be run weekly. They consume very little time and are an invaluable aid to preventive maintenance.

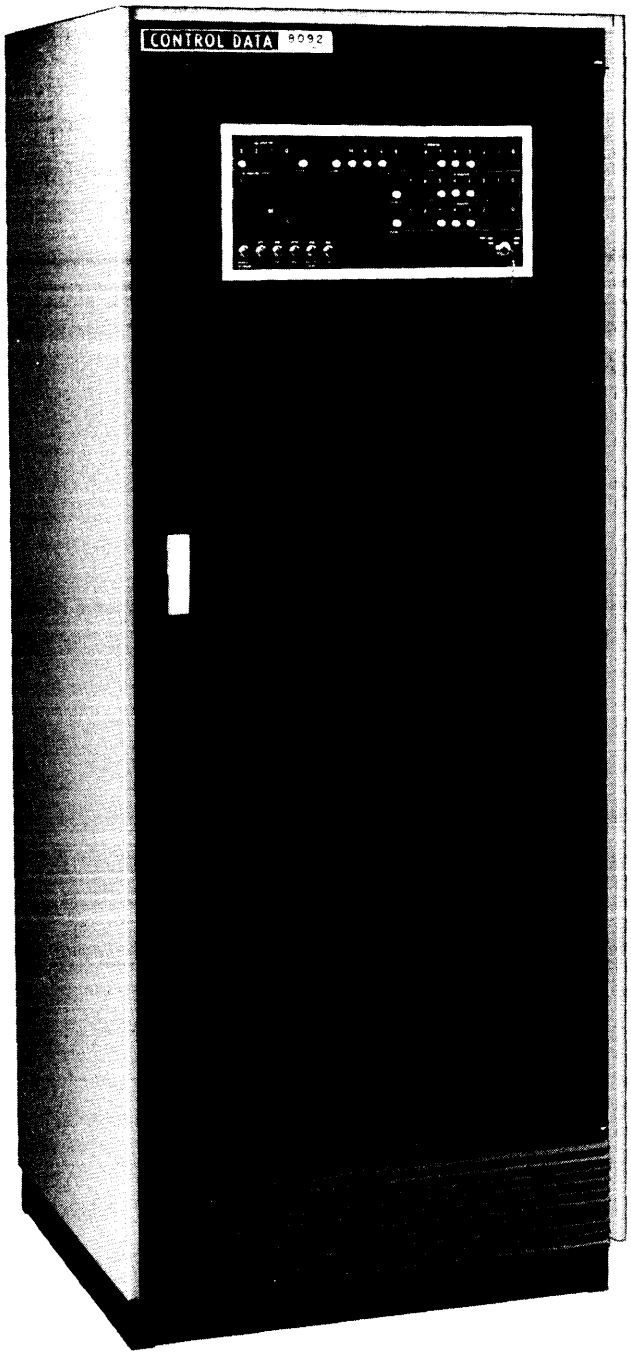
COOLING

All blowers and fans use grease-sealed ball bearings and should require no maintenance for the life of the machine. Blower filters should be cleaned weekly. The filter must be removed from its position immediately below the front door, washed with warm water and a household detergent, and rinsed with cool water. Total heat generated by the system cabinets is given in appendix C, Installation.

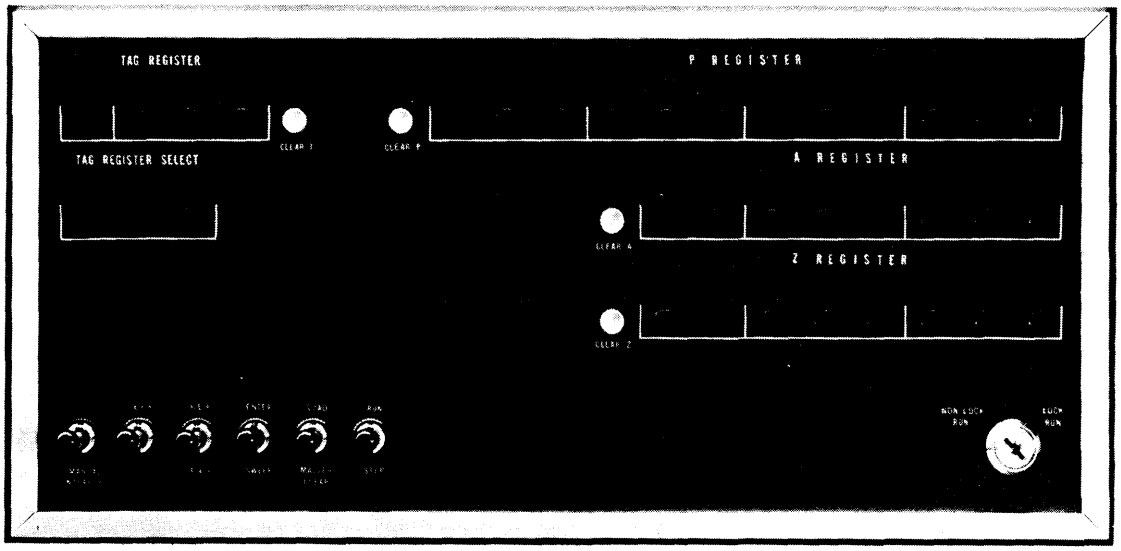
MAINTENANCE SCHEDULES

Typewriter maintenance information is included here. Schedules for magnetic tape maintenance are in the Magnetic Tape System instruction books.

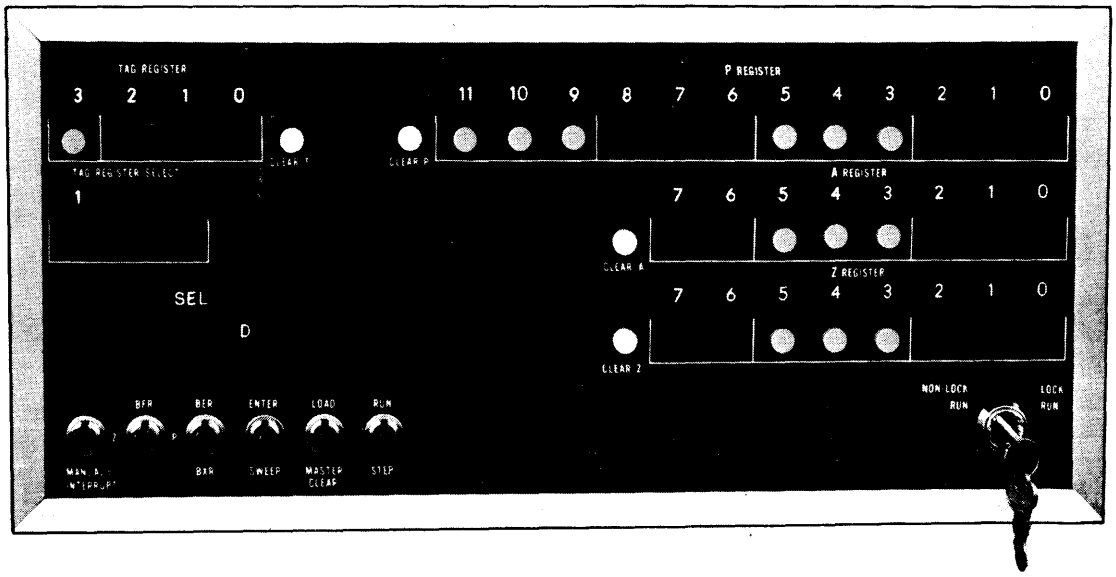
DAILY	Clean:	Computer room: desk top and floors, especially.
WEEKLY	Clean: Lubricate:	Air filters in all cabinets. Typewriter: grease metal-on-metal friction points, oil springs, and pivot points.
MONTHLY	Clean: Inspect:	Typewriter: keys and platen. Typewriter: worn ribbon.
SEMI ANNUALLY	Clean and Lubricate:	Typewriter



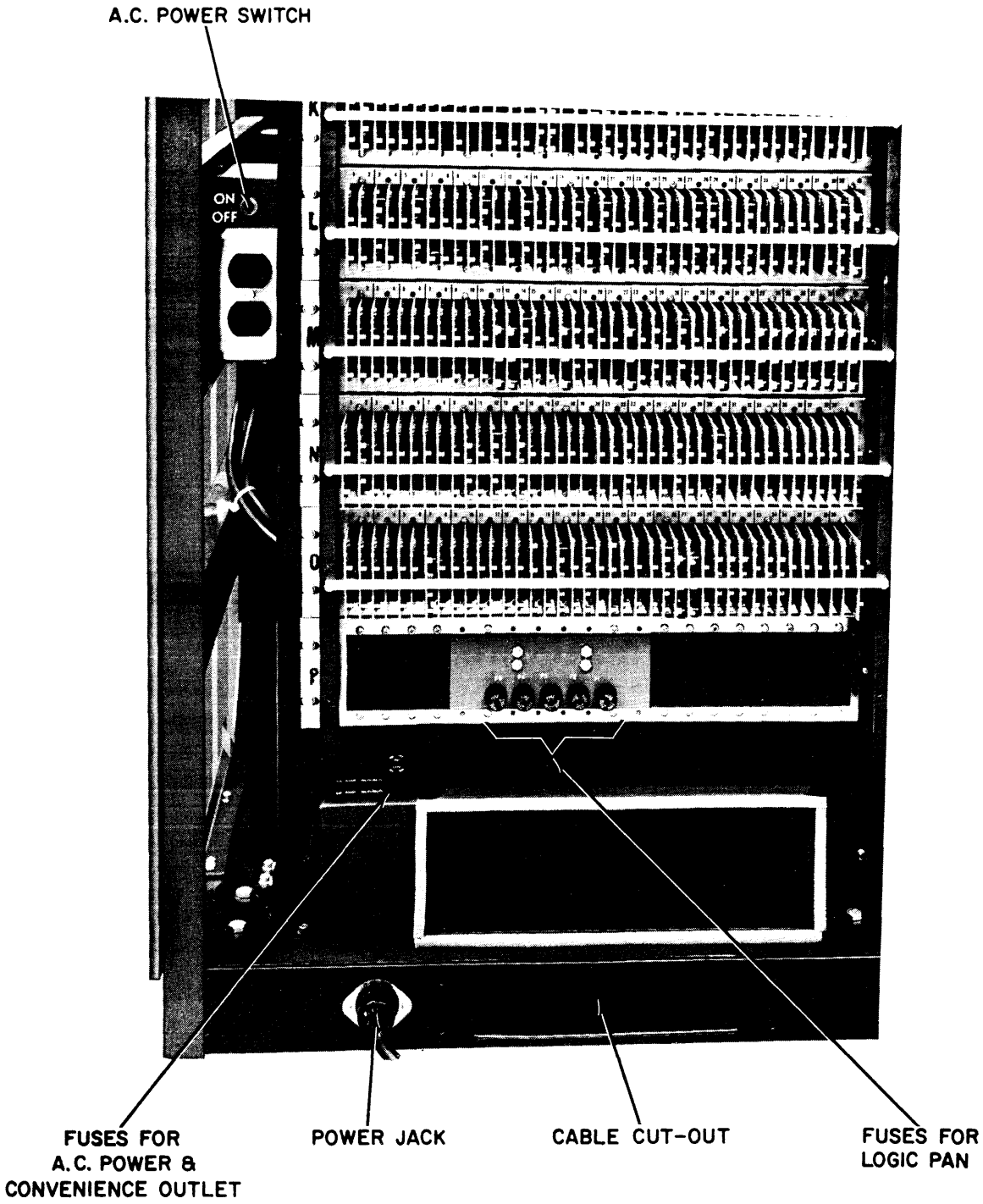
8092 TeleProgrammer



TeleProgrammer Control Panel (part no. 47000000)



TeleProgrammer Control Panel (part no. 47091200)



Lower Portion - Logic Chassis

CHAPTER TWO
BUILDING BLOCK

GENERAL

The basic building block of the TeleProgrammer is a single inverter transistor circuit. This circuit is used: (1) alone, as a single inverter; (2) in a pair to form a flip-flop; and (3) in a configuration of three to form a control delay. The major portion of the TeleProgrammer is constructed by interconnecting these circuits, which are packaged on 2-1/2 by 2-1/8 inch printed circuit cards (figure 2-1). Each card is equipped with a 15-pin male connector for plugging into the major equipment chassis.

ANALYSIS OF SINGLE INVERTER

Two signal levels are used within the TeleProgrammer: -3.5v, logical "1" and -0.5v, logical "0". The single inverter inverts these signal levels: a -3.5v input becomes a -0.5v output, and vice versa.

In the standard inverter circuit shown in figure 2-2, transistor Q01 is connected as an inverter. The collector circuit of the transistor has two feedback loops which prevent the transistor from being driven to cutoff or saturation. As a result, switching from one state to the other is accomplished in from 50 to 100 nanoseconds.

Transistor Q01 provides a beta* current gain in excess of 30. The collector current of Q01 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output line connected to CR10.

An input signal is applied via isolation diode CR01 to a voltage divider network composed of resistors R07, R08, R09, R10 and R11. An input signal of -0.5v (point A) results in -1.5v at point B and 0.8v at the base of Q01 (point C). CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

Diodes CR07 and CR08 form the feedback loops which prevent Q01 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistor. When the transistor approaches cutoff, the collector approaches -3.5v. The collector potential is coupled back to the base through CR08, R09 and R10. As a consequence, the base is held at a sufficiently negative voltage to permit some minimum conduction.

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* The beta current gain is the ratio of collector current to base current.

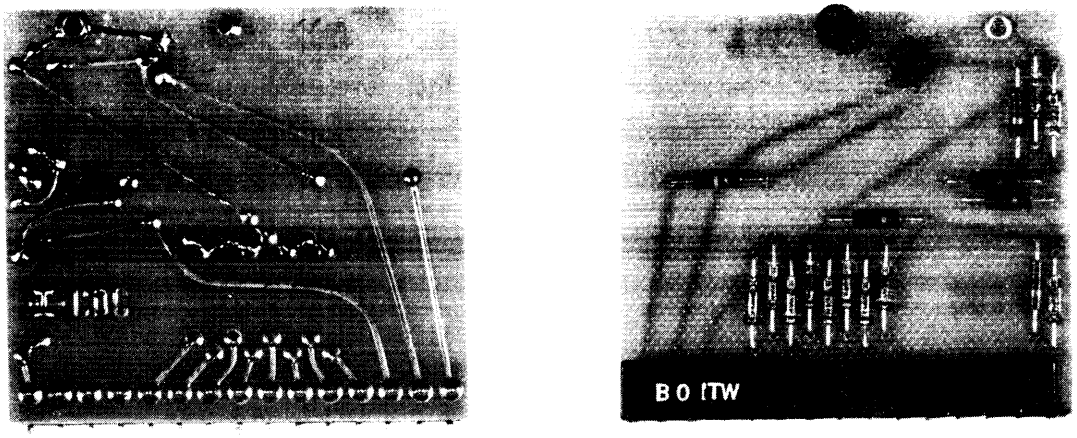

Figure 2-1. Typical Printed-Circuit Card (11A)

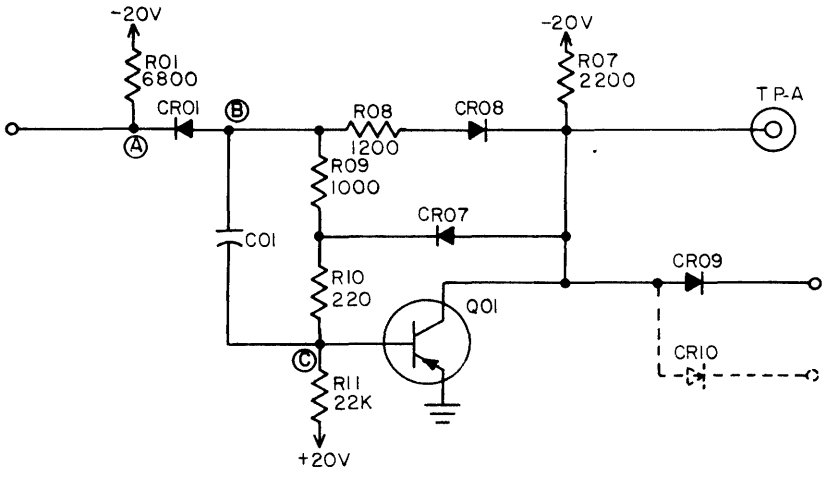

Figure 2-2. Schematic Diagram of Standard Inverter Card (11A)

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.

FLIP-FLOP

All short term storage of information in the TeleProgrammer is accomplished by flip-flops (FFs). A FF is two single inverter circuits interconnected as shown in figure 3 (each rectangle represents a single inverter). One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a set input that is "1". Conversely, it is placed in the "0" (cleared) state by a clear input that is "1". (Set and clear inputs are never "1" at the same time.)

The storage capability of a FF means simply that it remains in a state that is indicative of the last "1" input received. Specifically, if a "1" pulse is present at the set input, then the output of inverter A000 (figure 3) becomes "0". This output is applied as an input to A001 and the output then becomes "1". The output of A001 is fed back to A000. Thus, when the set input returns to "0", the feedback connection between A000 and A001 permits the storage of the state to which the "1" pulse on the set input forced the FF. Should the clear input later receive a "1" pulse, the output of A001 becomes "0", and the feedback input to A000 is "0". Consequently, A000 furnishes a "1" output which is returned to A001 to replace the "1" pulse at the clear input.

When the FF is set, A001 has a "1" output, and A000 has a "0" output. Conversely, when the FF is cleared, A001 has a "0" output and A000 has a "1" output.

The conventional square or box symbol for a FF is used in figure 2-3 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

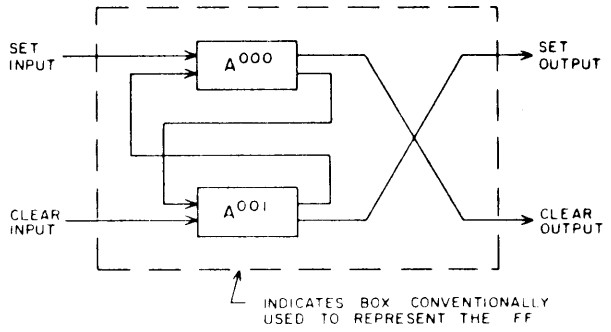

Figure 2-3 Interconnection of Inverters to Form a Flip Flop

CONTROL DELAY

The single inverter and FF described above are static, unclocked devices; the output of the inverter is a steady-state inversion of its input. A set FF provides a steady "1" from the set output and a "0" from the clear output until it is cleared. Timed and properly spaced pulses are essential to TeleProgrammer operation. The control delay (figure 2-4) shapes and resynchronizes the signals to provide timed outputs.

Outputs from the master clock are two sine waves 180^{o} out of phase. Since these waves are clipped and shaped by the inverter circuits to which the clock cards are connected, they are square waves (C000 and C001) in figure 4b. The difference in times that the simplified clock waves remain at 0v and -3v is due to the threshold (approximately -1.5v) of the subsequent inverters.

The control delay consists of a special FF (H^{---}) and one or more inverters (V^{---} or N^{---}) connected to the "0" output of the FF (figure 4a). The special FF has set inputs only, those going to I^{1}. The logic inputs (one of which must be clocked) are always signals from other building blocks. Feedback from I^{2} to I^{1} is gated by one of the clock phases, which is opposite to that applied to the output inverters. Thus, in figure 4a the odd phase (C001) gates the feedback and clocks the input from K025. The even phase C000, goes to output inverter V000.

During the odd clock phase (C001) the input signal sets FF, H000. The internal feedback is gated during this clock phase so that the FF action extends (or delays) the original input signal. The even clock phase (C000) gates the FF output. Duration of the output from V000 is established by the even clock phase.

In the waveforms for the control delay elements shown in figure 4b, the internal switching time of each inverter is the minimum value of 50 nanoseconds. Shaded areas indicate variations in pulses due to external wiring delays. If, for example, wiring delays were reduced to zero, the output of N901 would go to "0" at time 2 and remain "0" until time 5. At the other extreme, if the delay were a maximum of 50 nanoseconds, the output of N901 would go to "0" at time 3 and remain "0" until time 6.

The time at which the output of I^{1} may go to "0" varies over a 100-nanosecond period. The delays introduced at N901 are felt at I^{1} also. If N901 has the maximum delay but I^{1} has no delay, the I^{1} output goes to "0" at time 7 and remains "0" until time 13. If both N901 and I^{1} have the full delay, the I^{1} output is "0" from time 8 to time 14.

If capacitive wiring delays are zero, the leading edge of the output from V000 occurs at time 9 because the clock input to V000 from C000 does not go to "0" until time 8. The logic input signal to the control delay, gated by N901, goes to "0" at time 10; however, C001 allows this signal to be replaced by gating the

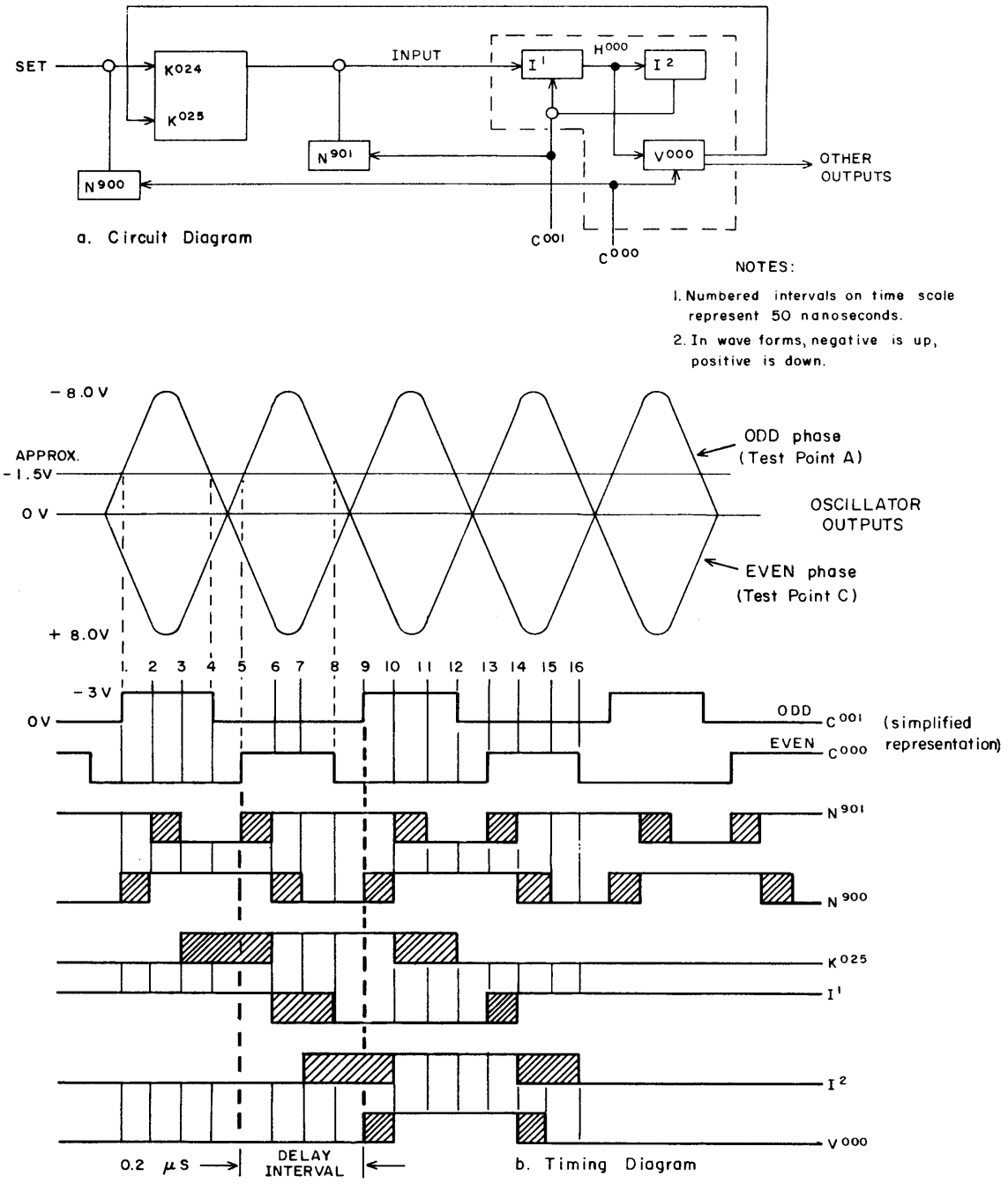

Figure 2-4 Control Delay

feedback from I^2 to I^1 until time 12. As a result, the original input signal is provided as an output from I^1 until at least time 13.

The output of I^1 encompasses the "0" portion of C000 (figure 2-4b). Since the output of V000 is the AND function of NOT C000 and NOT I^1, it is a "1" only when both are "0". Therefore, the occurrence and duration of the V000 output are determined by the period that C000 is a "0".

The delay interval of 0.2 microsecond is the period of the master clock; that is, the interval between the leading (or trailing) edges of successive clock phase pulses.

AND CIRCUIT

The AND circuit is shown in figure 2-5. The diodes of an AND circuit are the output diodes of inverters. As many as four diodes, each from different inverters, may be connected in an AND. The common cathode connection of the diodes is tied to the input of an inverter, which furnishes the remaining elements of the AND circuit. In order for the output of the AND to be a "1", that is, at -3.0v, inputs A, B and C must all three be at -3.0v. If any of the inputs are at -0.5v ("0"), then the cathodes of all three diodes are held at this potential, as is the output at D.

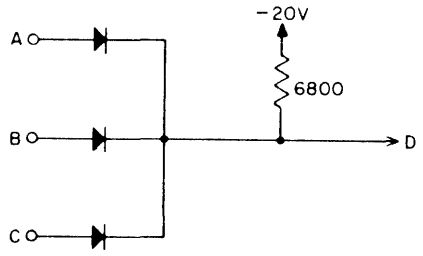

Figure 2-5 AND Circuit

OR CIRCUIT

The OR circuit consists of the input components of an inverter. The inverter shown in figure 2 has a two-input OR circuit, which involves R01, CR01, and R02 as well as voltage divider R09, R10 and R11 connected to -20v.

The potential at B, the common junction of the anodes of the OR diodes, is -1.5 (indicating a "0" in the circuit) only if both inputs at the cathodes of CR01 and CR02 are at 0.5v. If either OR input goes to -3.0v ("1"), then the potential at B is forced more negative than -1.5v. This more negative potential indicates a "1".

LOGIC EQUATIONS

A single inverter is a circuit which provides as an output the inverted form of its input. Thus if any of the inputs to an inverter is a "1", its output is a "0" ; conversely, its output is a "1" only if all of its inputs are "0". An equation is a logic representation of the inverter. For example:

$$K^{310} = K^{311} + V^{220}\ F^{585}\ K^{415} + V^{676}\ F^{940}\ J^{134}$$

The symbol on the left of the equal sign, called the subject term, denotes the inverter described by the equation. The expression on the right of the equal sign describes the logical configuration of the inputs.

The + sign represents the OR function or logical sum; the absence of a sign between symbols represents the AND function or logical product. In the context of equations, the word term designates a single symbol or group of symbols that is a logical product. The equation given above for inverter K310 has three terms, each representing an input to the inverter. Thus K310 has a "0" output if: (1) K311 is a "1"; (2) the AND function of V220, F585 and K415 is satisfied, that is, if each of them is a "1"; or (3) the AND function of V676, F940, F940 and J134 is satisfied, that is, if each of them is a "1".

TeleProgrammer operations are timed by a two-phase master clock. Circuits which receive timing signals from the clock are denoted by symbols H, V and N. The base letter of master clock symbols is C. The even or odd character of the third superscript digit indicates timing relations as follows:

C---	with odd third digit	represents a circuit furnishing odd phase clock pulses
C---	with even third digit	represents a circuit furnishing even phase clock pulses
H--- V--- N---	with odd third digit	provides an output during odd clock phases, receives an input during even clock phases
H--- V--- N---	with even third digit	provides an output during even clock phases receives an input during odd clock phases

Circuits with symbols L and M are not represented by complete equation entries. In these circuits only inputs or outputs (but not both) are represented by equation symbols.

LOGIC DIAGRAM SYMBOLS

The logic diagrams use five basic symbols to represent the logic properties of circuit configurations in the computer (figure 2-6).

Inputs to the diagram symbols are identified by arrows; outputs, by the absence of arrows. The OR function is represented on diagrams by arrows to the inverter. The AND function is represented by a small circle. An input to the AND is represented by a line; the output from the AND (which is input to a logical element such as an inverter) is represented by an arrow.

The FF is a storage device with two stable states, "1" (set) and "0" (clear), and is composed of two inverters. The logic symbol for a FF is a square formed from the rectangles representing the two inverters. The logic designations of the two inverters appear within the square. In a logic diagram, the inverter which receives the set input is at the top and the inverter which receives the clear input is at the bottom. Set outputs are received from the top inverter and clear outputs from the bottom (figure 2-3).

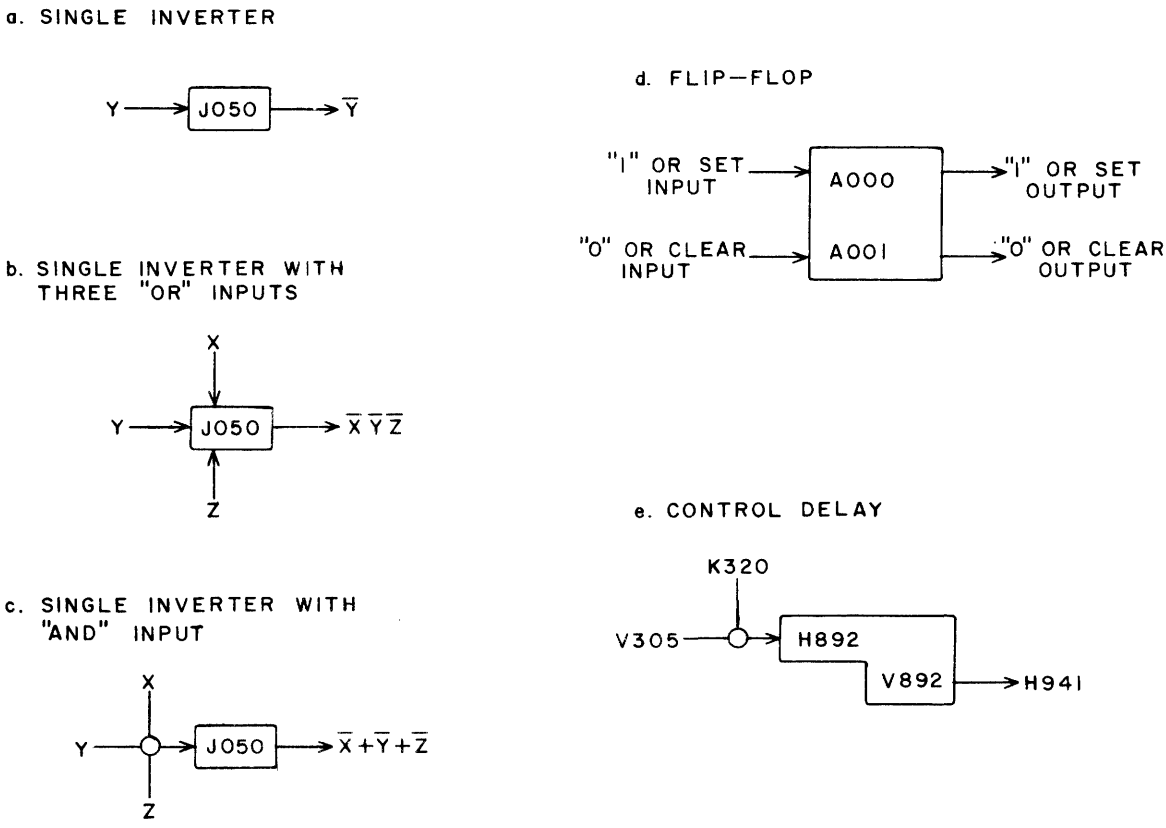

Figure 2-6. Logic Diagram Symbols

The logic designation of the set side of a FF has an even last digit and the clear side of the same FF is designated by the next odd digit; for example, K942/943.

A control delay consists of an H^{---} part, which receives the input, and a V^{---} or N^{---} part, which provides the output. Control delays receive inputs during one clock phase and furnish an output during the opposite clock phase.

STANDARD CARD TYPES

The majority of printed circuit cards consist of one or two standard inverters on a single card. The cards differ in the number of inverters, the number of input and output diodes, and the electrical interconnections. An inverter may have a maximum of six inputs and a maximum of eight outputs. Since an unused input terminal is sensed as a "1" input, no more than the exact number of input terminals required can be present. Inverter cards, therefore, are provided with varying numbers of input and output terminals to handle the various logic requirements.

The inverter cards are assigned two-digit numbers; the higher-order designates the type of card, the lower-order the number of inputs associated with each inverter on the card. (On control delay cards, only one inverter has external inputs.) Inverter card types and the pin assignments for each are listed in table 1. The significance of letters is:

I - input
O - output
A or C - (as subscript) one of two inverters
C - (not as subscript), a clock pulse

CAPACITIVE DELAY NETWORKS

Capacitive delays are used in certain areas of computer logic, particularly input-output circuits, to delay the recognition of a change from the "0" to the "1" state. The delay, accomplished by connecting an integrating circuit to the junction of a pair of logic cards, may be fixed value or variable through a limited range.

In the fixed delay (figure 2-7) the logic input to card B is delayed by a time constant which is the product of the 6800 ohm resistor on card B and the capacitor C. With the output transistor on card A grounded (logical "0" out), C is discharged to ground. When the transistor is switched off (logical "1" out), C begins charging through the 6800 ohm resistor until the threshold level of card B (-1.5v) is realized, a point determined by the time constant RC.

The actual delay time, as observed on an oscilloscope, for any fixed delay may vary considerably due to circuit constants. The delay times selected allow sufficient latitude for the circuits to operate successfully with these variations.

When a critical delay period is necessary a variable delay network will permit accurate adjustment. In the circuit shown in figure 8, a variable resistor on the 73A delay card may be adjusted to the desired time constant. The value of R in the RC factor is the effective parallel resistance of 2200 ohms and the selected setting of R.

TABLE 2-1. DESCRIPTION OF STANDARD CARD TYPES

Type	Title	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
01	Oscillator		O_E						O_O						*	*	*
11	Inverter		I				O	O	O	O	O	O	O	O			
12	Inverter		I	I			O	O	O	O	O	O	O	O			
13	Inverter		I	I	I		O	O	O	O	O	O	O	O			
14	Inverter		I	I	I	I	O	O	O	O	O	O	O	O			
15	Inverter		I	I	I	I	I	O	O	O	O	O	O	O			
16	Inverter		I	I	I	I	I	I	O	O	O	O	O	O			
20	Quadruple Inverter		I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
21	Double Inverter		I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C			
22	Double Inverter		I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C			
23	Double Inverter		I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C			
24	Double Inverter		I_A	I_A	I_A	I_A	O_A	O_A	I_C	I_C	I_C	I_C	O_C	O_C			
30	Double FF		I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
**31	FF		I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C			
**32	FF		I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C			
**33	FF		I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C			
***41	Control Delay		I					I_C	O	O	O	O	O	O			
***44	Control Delay		I	I	I	I		I_C	O	O	O	O	O	O			
52, 53	G10-G14 Memory Cards (See TeleProgrammer Reference Manual, IDP 106, pp. 337-343)																
67	Output		I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
68	Input		I_A		O_A	O_A	I_B		O_B	O_B	I_C		O_C	O_C			
69	Output		I_A		O_A		I_B		O_B		I_C		O_C				
73A	Variable Delay		I	O	O	O	O	O	O	O	O	O	O	O			
32	Variable Delay		I	O	I	O	I	O	I	O	I	O	I	O			

* Unless otherwise noted: pin 13 equals -20v; pin 14 equals ground; pin 15 equals +20v.

** Two inverter units with internal feedback connections.

*** A Clock Pulse applied to pin 6 controls the internal feedback connection.

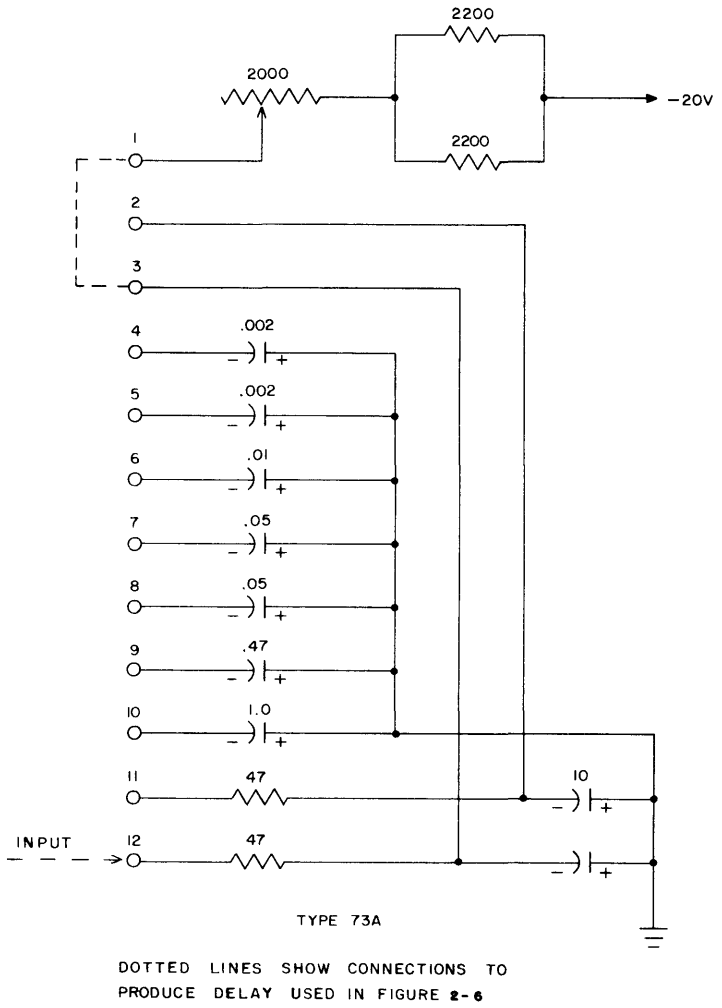

Figure 2-7 Capacitive Delay Card

In this circuit, the driving card is an output amplifier (L-card). This is necessary since the variable resistance on card C may draw more current than could be handled by the output transistor of a conventional logic card. An input amplifier (M-card) is required to return the logic levels to -3v and 0.5v.

When either delay is used, a Y logic symbol and a coordinate position define the location of the delay card. Numbers following the dash identify pins to which the delay components are connected. In the variable delay card in figure 2-7 the variable resistor may be connected to as many individual capacitors as necessary to produce the desired delay range; the exact delay is resolved by adjusting the resistor. It is possible for one 73A card to provide one variable delay (for example, pins 1 and 3), and up to eight fixed delays, or to provide nine fixed delays, (pin 1 not used).

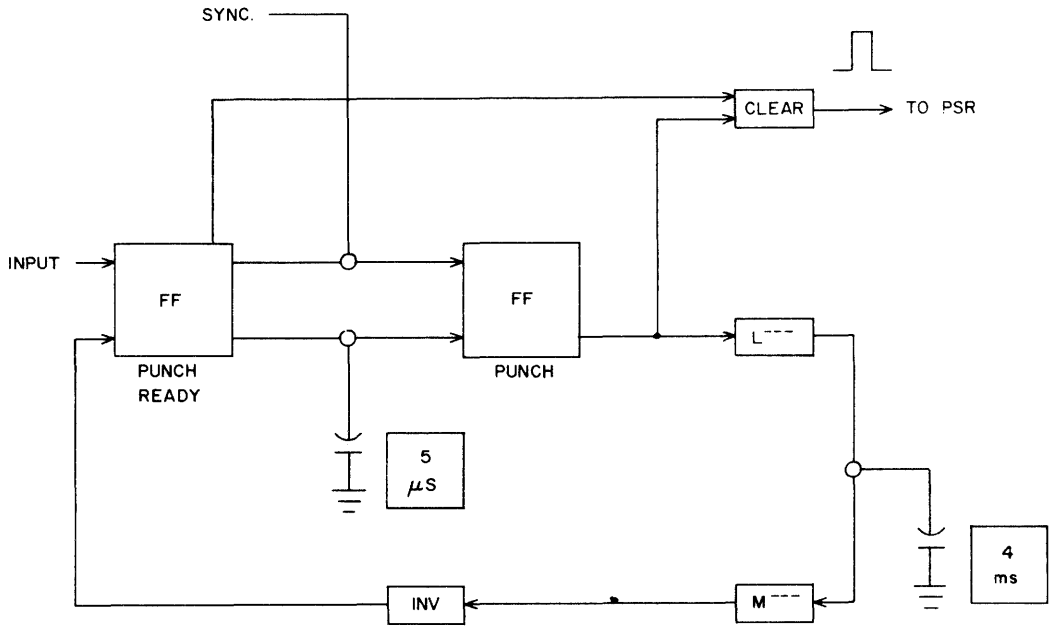

Figure 2-8 Capacitive Delay Application

The control network circuit for the high speed punch uses capacitive delay (figure 10). Requisites for this circuit are a short (5 usec) clear pulse to PSR and an accurately adjusted 4 ms delay to govern the length of the punch cycle.

With both FFs cleared, CLEAR is held to a "0" by the Punch FF, while the L-card output is at ground, thereby negating the delay network. When an input pulse sets Punch Ready, the Punch FF is also set at the next sync pulse. Clear cannot be energized, however, since Punch Ready holds it to a "0". The delay circuit begins to charge, and after 4 ms a pulse from INV clears Punch Ready. The length of the resulting clear pulse is governed by the delay circuit connecting the clear sides of the two FFs.

CHAPTER THREE
INSTALLATION

GENERAL

The Control Data 8092 TeleProgrammer is designed to be used with a minimum of environmental restrictions. This section provides electrical and physical information to aid in the preparation of a suitable site for the system. Detailed data on equipment sizes and power requirements are also included. For information concerning other than the common requirements consult Control Data Corporation.

REQUIREMENTS

TEMPERATURE

Blowers cool the equipment by drawing air through a re-usable filter located below the front door, and circulating the air out of the equipment cabinet through a vent below the rear door. The filter must be regularly cleaned to insure proper circulation.

The system operates in a normal room air environment not exceeding 100°F. Heat generated by the equipment should be quickly removed from the vicinity of the cabinets by circulating the room air.

If tape is used in the system, a low humidity limit of 40% minimizes static build up on the magnetic tape. A high humidity limit of 60% prevents deterioration of punched cards and acetate magnetic tape.

AREA CLEANLINESS

Clean the computer site regularly to avoid dust accumulation. Dust and cigarette ashes in the immediate vicinity of the tape handlers may collect on the magnetic tape and cause errors in operation. Avoid smoking when handling magnetic tapes.

SPACE AND LAYOUT REQUIREMENTS

The position of the equipment cabinets is partially determined by the size and shape of the area available for the system installation. Cabinets should be arranged to permit easy access both for operation and maintenance personnel. There should be a three-foot clearance surrounding each piece of equipment to allow for free movement of test equipment.

Installation, including dimensions and door swings, are given for each equipment on figure 3-1. Dimensions and weights are summarized in table 3-1.

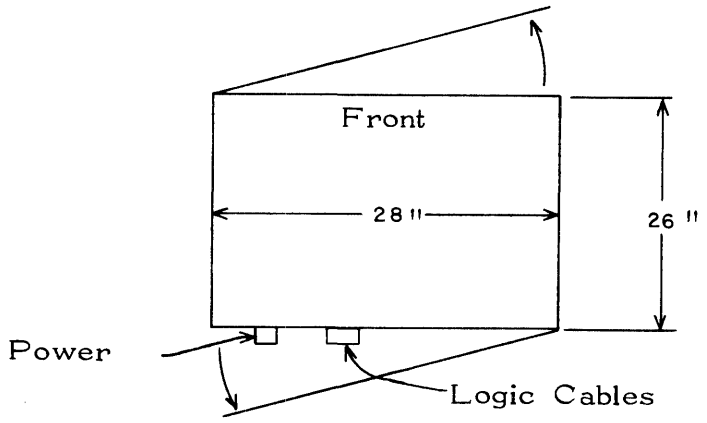

Figure 3-1. Physical Dimensions, 8092 TeleProgrammer)

TABLE 3-1. PHYSICAL CHARACTERISTICS

Dimensions:	
Height	68-3/4 in.
Width	28 in.
Depth	26 in.
Weight	515 lb
Temperature Requirements	32° to 100°F
Electrical Requirements	

Model	Voltage (ac)	Frequency (Hz)	Phase	Maximum Current (amperes)	Maximum Power (watts)
8092-A	120	60	1	12	1450
8092-B	120	60	1	12	1450
8092-D	120	60	1	15	1800
8092-E	120	50	1	16	1920

POWER SERVICE

The power service facilities for the computer system are supplied by the customer and should be installed before arrival of the system. Exceptions are those items specifically noted to be supplied and installed by Control Data Corporation at the time of installation. Power and current requirements are listed in table 3-1. A typical TeleProgrammer system uses normal convenience outlets in the system area for the computer and peripheral equipment. (Magnetic tape handlers require special heavy-duty wiring.) At the customers option, the 120 volt, single phase power may be derived from one leg of a three-phase, y-connected source.

CABLES

The information cables which connect the various elements in the system are delivered at the time of installation. All information cables are identical except for length. Total cable length on any circuit should not exceed 75 feet. The customer can determine the length of the cables (prior to delivery) by referring to the equipment layout plan. If the total length of the cables exceeds 75 feet, revisions should be made.

All cables in the system are supplied by Control Data Corporation at the time of delivery. Standard cable lengths are 15 feet and 25 feet. Any unusual lengths may be purchased from Control Data Corporation or supplied independently by the customer. Pin assignments for Input/Output cables are shown in publication 36810500: 8092 TELEPROGRAMMER INPUT/OUTPUT SPECIFICATIONS.

CHAPTER FOUR
INSTRUCTION TIMING CHARTS

GENERAL

The following pages present a time base analysis of instructions in the Tele-Programmer repertoire. Only those times wherein a command or enable occurs are shown. Common functions such as advancing the excursions counter are omitted. The instructions appear in sequence. Table 4-1 lists each instruction in terms of storage reference cycles. Because in the majority of cases each initial D cycle is similar, it has not been repeated for each instruction.

TABLE 4-1. Steps in Executing Instructions

	Instructions	Phase	Z Reg.	A Reg.
1)	00, 77	D	Instruction	NC*
2)	01	D	Instruction	Result
3)	02, 03, 70, 71	D	Instruction	NC
4)	04, 05, 70, 71	D	Instruction	NC
		C	Jump Address	NC
5)	06	D	Instruction	Result
6)	013, 113	D	Instruction	Result
7)	10, 11, 12	D	Instruction	NC
	14, 15, 16 20, 21, 22	A	Indirect Address	NC
	25, 26, 30 31, 32, 34	B	Operand Address	NC
	35, 36	C	Operand	Result
8)	41, 42	D	Instruction	NC
		A	Indirect Address	NC
		B	Operand Address	NC
		C	Contents of A	NC
9)	51, 55	D	Instruction	NC
		B	Operand Address	NC
		C	Operand	Result
		C'	Contents of A	Result
10)	60, 61, 62	D	Instruction	NC
	63, 64	C	Jump Address	NC

* NC means no register change.

Table 4-1. Steps in Executing Instructions (cont.)

Instructions	Phase	Z Reg.	A Reg.
11) 72, 73	D	Instruction	NC
	B	Starting Address	Starting Address
	C	Ending Address	NC
	B'	I/O Character	Starting Address
Repeated			+1
	C'	Ending Address	NC
12) 74	D	Instruction	NC
	C	Output Address	NC
13) 76	D	Instruction	NC
	C	Input Character	Input Character
14) 75	D	Instruction	NC
	C	Output Upper 6 bits	NC
15) 07,17,23,24, 27,33,37,40, 43,44,45,46, 47,50,52,53, 54,56,57	D	Instrucion Functions Exactly like a Halt (00 or 77)	NC

INSTRUCTION 00 ERROR STOP (ERR)					
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1, Clear S				02
03					03
04					04
05	P → S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25	Clear Divert FF, Clear				25
26	Run FF				26
27	Clear Write, Inhibit FF's				27

INSTRUCTION 01 SHIFT 'A' LEFT ONE BIT (SHA)

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P ⟶ S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS ⟶ Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF,Z ⟶ F				16
17	A.2' ⟶ Q(15 thru 25)				17
20	Set Write FF				20
21	Clear A'				21
22					22
23	Toggle A'				23
24	Probe A'				24
25					25
26	Clear Divert FF **A'** **A**				26
27	Clear Write, Inhibit FF's D Cycle Stays Set				27

INSTRUCTION 02 TRANSFER 'A" TO TAG REGISTER (ATT)					
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P → S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F,F'				16
17	(F' Selects Tag Reg.)				17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25	A Tag				25
26	Clear Divert FF				26
27	Clear Write, Inhibit FF's D Cycle Stays Set				27

INSTRUCTION: 02, NO-OP

NOTE: NO TAG SELECTED

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Adv P_1 By,1 Clear "S"				02
03					03
04					04
05	P → S				05
06	Set Divert F-F				06
07	$P2 = P_1$				07
10	Set Read FF, Clear "Z"				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z FF[1]				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF				26
27	Clear Write, Inhibit FF Set "D" Cycle				

INSTRUCTION	03 TRANSFER TAG REGISTER TO 'A" (TTA)				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P → S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F,F'				16
17	(F' selects Tag Reg.)				17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF,Tag → 'A'				26
27	Clear Write, Inhibit FFs D Cycle Stays Set				27

INSTRUCTION: 03, CLEAR "A" REGISTER

NOTE: NO TAGS SELECTED

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Adv P_1 By 1, Clear "S"				02
03					03
04					04
05	P→S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear "Z"				10
11					11
12	MCS→Z				12
13	Clear "F"				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → "F" "F'"				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF Clear "A"				26
27	Clear Write, Inhibit FF_S, Set "D" Cycle				27

INSTRUCTION	04 SET BUFFER STARTING ADDRESS (ABR) D or DC SEQUENCE			
	05 SET BUFFER ENDING ADDRESS (ABX) D or DC SEQUENCE			
TIME	D CYCLE	B CYCLE	C CYCLE	TIME
00				00
01				01
02	Advance P_1 by 1, Clear S		Clear S, Adv. P_1 by 1	02
03				03
04				04
05	P → S		P → S	05
06	Set Divert FF			06
07	$P_2 = P_1$		Set $P_2 = P_1$	07
10	Set Read FF, Clear Z		Clear Z	10
11				11
12	MCS → Z		MCS → Z	12
13	Clear F			13
14				14
15	Clear Read FF			15
16	Set Inhibit FF, Z → F		+Z → R (15 thru 25)	16
17				17
20	Set Write FF			20
21			Clear A'	21
22				22
23	Adv. P_1 by 1 (Buff Not Busy)		Toggle A'	23
24			Probe A'	24
25				25
26	A → BER, BXR; I_3 → BER, BXR (Buff Not Busy) Clear Divert FF		Tag P', A' P	26
27	Clear Write, Inhibit FF's Set $P_2 = P_1$; D Cycle Stays Set (Buff Not Busy) Clear D Cycle, Set C Cycle (Buffer Busy)		Set D Cycle	27

INSTRUCTION	06 TRANSFER BUFFER ENTRANCE REGISTER TO 'A' (BER)				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P → S				05
06	$P_2 = P_1$				06
07	Set Read FF, Clear Z				07
10					10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF;BER → 'A'				26
27	Clear Write, Inhibit FF's Set 'D' Cycle				27

INSTRUCTION	07 CLEAR BUFFER CONTROLS (CBC)				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P → S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear IBA,OBA,Buff Busy, etc.				26
27	Clear Divert FF Clear Write, Inhibit FF's Set 'D' Cycle				27

INSTRUCTION 10, 11 12 LOGICAL PRODUCT (LPN, LPM, LPI)

DC or DBC OR DABC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S	Adv. P_1 by 1; Clear S	Adv. P_1 by LPM; Clear S	Adv.P_1 by 1(LPN);Clear S	02
03					03
04					04
05	P → S	P → S	P → LPM; Z → S (LPI)	P → S(LPN); Tag → S' (LPM) (LPI) Z S	05
06	Set Divert FF				06
07	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS → Z	MCS → Z	MCS → Z	MCS → Z	12
13	Clear F				13
14					14
15	Clear Read FF			+Z → R; A → R (15 thru 25)	15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23				Toggle A'	23
24				Probe A'	24
25				A' → A	25
26	Clear Divert FF				26
27	Clear Write, Inhibit FF's Set C Cycle (LPN); Set 'B' Cycle (LPM) Set A Cycle (LPI) Clear D Cycle	Set 'B' Cycle, Clear A Cycle	Set 'C' Cycle, Clear B Cycle	Set 'D' Cycle, Clear C Cycle	27

INSTRUCTION	013, 113 CLEAR INTERRUPT LOCKOUT (CIL)				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S				02
03					03
04					04
05	P ⟶ S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS ⟶ Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z ⟶ F				16
17					17
20	Set Write FF				20
21	Clear P (113)				21
22	Clear Interrupt LockoutFF				22
23	PSR P (113)				23
24					24
25					25
26	Clear Divert FF				26
27	Clear Write,Inhbit FF's "D" Cycle Stays Set				27

INSTRUCTION 14, 15, 16 LOGICAL SUM (LSN, LSM, LSI)

DC or DBC or DABC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1, Clear S	Adv. P_1 by 1; Clear S	Adv. P_1 by 1 (LSM); Clear S	Adv. P_1 by 1 (LSN); Clear S	02
03					03
04					04
05	P → S	P → S	P → S (LSM); Z → S (LSI)	P → S (LSN); Z S, Tag S' (LSM + LSI)	05
06	Set Divert FF				06
07	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS → Z	MCS → Z	MCS → Z	MCS → Z	12
13	Clear F				13
14					14
15	Clear Read FF			+Z → R; A → Q (15 thru 25)	15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23				Toggle A'	23
24				Block Probe A'	24
25				A' → A	25
26	Clear Divert FF				26
27	Clear Write, Inhibit FF's Set C Cycle (LSN); Set B Cycle (LSM); Set A Cycle (LSI) Clear D Cycle	Set B Cycle, Clear A Cycle	Set C Cycle, Clear B Cycle	Set D Cycle, Clear C Cycle	27

INSTRUCTION	20, 21, 22 LOAD A DIRECT (LDN, LDM, LDI)				
	25, 26 LOAD A COMPLEMENT (LCM, LCI)				
	DC or DBC or DABC SEQUENCE				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S	Adv.P_1 by 1,Clear S	Adv.P_1 by1(LDM + LCM);	Adv.P_1 by 1(LDN);Clear S	02
03					03
04					04
05	P→S	P→S	P→S(LDM + LCM);Z→S	P→S(LDN);Z S,Tag S'	05
06	Set Divert FF		(LDI + LCI)	(LDM+LDI+LCM+LCI)	06
07	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS→Z	MCS→Z	MCS→Z	MCS→Z	12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF,Z→F			(+Z→R(LD-);-Z→R(LC-)	16
17				(15 thru 25)	17
20	Set Write FF				20
21				Clear A'	21
22					22
23				Toggle A'	23
24				Probe A'	24
25				A'→A	25
26	Clear Divert FF				26
27	Clear Write,Inhibit FF's Set C Cycle(LDN);Set B Cycle (LDM + LCM); Set A Cycle (LDI + LCI) Clear D Cycle	Set B Cycle,Clear A Cycle	Set C Cycle,Clear B Cycle	Set D Cycle,Clear C Cycle	27

INSTRUCTION 30, 31, 32 ADD (ADN, ADM, ADI)

34, 35, 36 SUBTRACT (SBN, SBM, SBI)

DC or DBC or DABC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S	Adv.P_1 by 1; Clear S	Adv.P_1 by 1(ADM);Clear S (SBM)	Adv.P_1 by 1(ADN+SBN) Clear S	02
03					03
04				Tag S'	04
05	P→S	P→S	P→S(ADM) Z→S (ADI)	P→S(ADN+SBN),Z S,	05
06	Set Divert FF		(SBM) (SBI)	(ADM+ADI+SBM+SBI)	06
07	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$	07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS→Z	MCS→Z	MCS→Z	MCS→Z	12
13	Clear F				13
14					14
15	Clear Read FF			+A→Q, +Z→R(AD-),-Z R	15
16	Set Inhibit FF, Z→F			(SB-) (15 thru 25)	16
17					17
20	Set Write FF				20
21				Clear A'	21
22				Toggle A'	22
23				Probe A'	23
24				A'→A	24
25					25
26	Clear Divert FF				26
27	Clear Write,Inhibit FF's Set C Cycle(ADN)(SBN); Set B Cycle(ADM)(SBM); Set A Cycle(ADI)(SBI) Clear D Cycle	Set B Cycle,Clear A Cycle	Set C Cycle,Clear B Cycle	Set D Cycle,Clear C Cycle	27

INSTRUCTION 41, 42 STORE (STM, STI)

DBC or DABC CYCLE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S	Adv. P_1 by 1; Clear S	Adv.P_1 by (STM); Clear S	Clear S	02
03					03
04					04
05	P → S	P → S	P → S(STM); Z → S(STI)	Z,Tag → S; Z S	05
06	Set Divert FF				06
07	$P_2 = P_1$	$P_2 = P_1$	$P_2 = P_1$		07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS → Z	MCS → Z	MCS → Z	A → Z	12
13	Clear F				13
14					14
15	Clear Read FF			+Z → R(15 thru 25)	15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23				Toggle A'	23
24				Probe A'	24
25				A' → A	25
26	Clear Divert FF				26
27	Clear Write,Inhibit FF's				27
	Set B Cycle(STM); Set A Cycle (STI) Clear D Cycle	Set B Cycle ,Clear A Cycle	Set C Cycle ,Clear B Cycle	Set D Cycle ,Clear C Cycle	

INSTRUCTION 51, 55 REPLACE ADD; REPLACE ADD 1 (RAM, RAO)

DBCC' SEQUENCE

TIME	D CYCLE	B CYCLE	C CYCLE	C' CYCLE	TIME
00					00
01					01
02	Adv. P_1 by 1,Clear S	Adv. P_1 by 1; Clear S	Clear S	Set C' Cycle (K225)	02
03					03
04					04
05	P→S	P→S	Tag→S; Z S		05
06	Set Divert FF				06
07	$P_2 = P_1$	$P_2 = P_1$			07
10	Set Read FF, Clear Z	Clear Z	Clear Z	Clear Z	10
11					11
12	MCS→Z	MCS→Z	MCS→Z	A→Z	12
13	Clear F				13
14					14
15	Clear Read FF		A→Q(RAM);+Z→R;+1→Q (RAO) (15 thru 25)	+Z→R(15 thru 25)	15
16	Set Inhibit FF, Z→F				16
17					17
20	Set Write FF				20
21			Clear A'	Clear A'	21
22					22
23			Toggle A'	Toggle A'	23
24			Probe A'	Probe A'	24
25			A'→A	A'→A	25
26	Clear Divert FF				26
27	Clear Write,Inhibit FF's Set B Cycle Clear D Cycle	Set C Cycle,Clear B Cycle	Set C' FF;Block Clear C Cycle	Set D Cycle, Clear C Cycle, Clear C' FF	27

INSTRUCTION	60, 61, 62, 63, 64 JUMP - ZERO; Non-Zero; Positive; Negative; Unconditional (ZJP; NZP; PJP; NJP; UJP)				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S			Adv.P_1 by 1;Clears S	02
03					03
04					04
05	P→S			P→S	05
06	Set Divert FF				06
07	$P_2 = P_1$			$P_2 = P_1$	07
10	Set Read FF, Clear Z			Clear Z	10
11					11
12	MCS→Z			MCS→Z	12
13	Clear F				13
14					14
15	Clear Read FF			+Z R(15 thru 25)	15
16	Set Inhibit FF, Z→F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23	Adv.P_1 by 1.(Jump not Sat.)			Toggle A'	23
24				Probe A'	24
25					25
26	Clear Divert FF			Tag P', A' P	26
27	Clear Write,Inhibit FF's				27
	$P_2 = P_1$(jump not sat.)			Set D Cycle, Clear C Cycle	
	Set C Cycle (Jump Sat.)				
	Clear D Cycle (Jump Sat.)				

INSTRUCTION	70 INITIATE BUFFER INPUT (IBI)				
	D or DC SEQUENCE				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Advance P_1 by 1,Clear S			Adv.P_1 by 1;Clear S	02
03					03
04					04
05	P → S			P → S	05
06	Set Divert FF				06
07	$P_2 = P_1$			$P_2 = P_1$	07
10	Set Read FF, Clear Z			Clear Z	10
11					11
12	MCS → Z			MCS → Z	12
13	Clear F				13
14					14
15	Clear Read FF			+Z→R(15 thru 25)	15
16	Set Inhibit FF, Z→F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23	Adv.P_1 by 1,Set BSI,Set IBA,(Buff not Busy)			Toggle A'	23
24	Clear SSI			Probe A'	24
25					25
26	Clear Divert FF,Set Buff RDY,Send Input Request,			Tag→P', A' → P	26
27	Clear BFR				27
	Clear Write,Inhibit FF's,Set C Cycle,Clear D Cycle			Set D Cycle,Clear C	
	(Buff Busy),Set Buff Busy next V000,and $P_2=P_1$			Cycle	
	(Buff not Busy) D Cycle Stays Set				

INSTRUCTION 71 INITIATE BUFFER OUTPUT (IBO)

D BUFFER or DC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00			Set Buff Busy		00
01			Set Buffer Cycle FF; Clear IBO		01
02	Advance P_1 by 1,Clear S		BER = BER_1; Clear S;	Adv. P_1 by 1;Clear S	02
03					03
04			Clear Buf. RDY.		04
05	P→ S		BER, Tag Reg_3 → S	P→ S	05
06	Set Divert FF				06
07	$P_2 = P_1$			$P_2 = P_1$	07
10	Set Read FF, Clear Z		Clear BFR	Clear Z	10
11					11
12	MCS→Z		MCS→ BFR	MCS → Z	12
13	Clear F		Adv. BER by 1		13
14					14
15	Clear Read FF			+Z→R(15 thru 25)	15
16	Set Inhibit FF, Z→ F				16
17					17
20	Set Write FF				20
21				Clear A'	21
22	Set IBO				22
23	Adv. P_1 by 1,Set BSI,Set OBA,(Buff not Busy)		Set BSI	Toggle A'	23
24	Clear SSI; Clear BSI		Clear SSI	Probe A'	24
25	Set SSI				25
26	Clear Divert FF	Clear D Cycle	Set Buffer RDY,INFO RDY Sent Out	Tag→ P', A'→P	26
27	Clear Write,Inhibit FF's;Set C Cycle (Buff Busy)				27
	Buffer Cycle and $P_2=P_1$ (Buff not Busy)		Clear Buffer Cycle, D	Set D Cycle, Clear C	
			Cycle Still Set	Cycle	

INSTRUCTION 72, 73 NORMAL INPUT/OUTPUT (INN,OUT)

DBC - B'C' - B'C' SEQUENCE

TIME	D CYCLE	B CYCLE	B' CYCLE	TIME
00			(Resume Clears Wait Output)	00
01				01
02	Adv. P_1 by 1,Clear S	Adv.P_1 by 1; Clear S	Clear S	02
03				03
04				04
05	P → S	P → S	Tag → S', A → S	05
06	Set Divert FF			06
07	$P_2 = P_1$	$P_2 = P_1$		07
10	Set Read FF, Clear Z	Clear Z	Clear Z	10
11				11
12	MCS → Z	MCS → Z	INP → Z (72) MCS → Z(73)	12
13	Clear F		Clear Wait Input FF (72)	13
14		(+Z → R)(15 thru 25)		14
15	Clear Read FF		(A → Q);(+1 → R) (15 thru 25)	15
16	Set Inhibit FF, Z → F			16
17				17
20	Set Write FF			20
21		Clear A'	Clear A'	21
22				22
23		Toggle A'	Toggle A'	23
24		Probe A'	Probe A'	24
25		A' → A	A' → A	25
26	Clear Divert FF;Set I/O SEQ. FF		Set Wait Output (73)	26
27	Clear Write,Inhibit FF's Set B Cycle, Clear D Cycle	Set C Cycle , Clear B Cycle	Set C Cycle , Clear B Cycle	27

Note: C and C' Set, C' Cycle Timing

Note: Cycles occur in following order: D, B, C, B', C'; cycle C and C' are shown on page 4-20.

INSTRUCTION	72, 73 NORMAL INPUT/OUTPUT (INN,OUT)		
	DBC - B'C' - B'C' SEQUENCE		
TIME	C CYCLE	C' CYCLE	TIME
00			00
01			01
02	Adv. P_1 by 1, Clear S	Clear S	02
03			03
04			04
05	P→S	P→S	05
06			06
07	$P_2 = P_1$		07
10	Clear Z	Clear Z	10
11			11
12	MCS→Z	MCS→Z	12
13			13
14			14
15	+Z→R, A→Q	-Z→R; A→Q	15
16	(15 thru 25)	(15 thru 25)	16
17			17
20			20
21	Clear A'	Clear A'	21
22			22
23	Toggle A'	Toggle A'	23
24	Probe A'	Probe A'	24
25	Block A'→A	Block A'→A	25
26	Set Wait INP.(72) (A' ≠ 0)	Clear I/O SEQ.(A' = 0), Set Wait INP.(72)	26
27	Set B Cycle (A' ≠ 0), Set D Cycle (A' = 0), Set C' Cycle, Clear C Cycle, Stop Recirc. (72)	Set B Cycle(A' ≠ 0) Set D Cycle (A' = 0) Clear C Cycle, C' Cycle (A' = 0) Stop Recirc., Wait For Resume or Ready	

Note: B and C' Set, Gives B' Cycle

INSTRUCTION 74, 76 OUTPUT NO ADDRESS: INPUT TO A (OTN, INA)

DC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00				Clear I/O Seq. (76)	00
01					01
02	Adv. P_1 by 1,Clear S			Adv. P_1 by 1 (74 only);	02
03				Clears	03
04					04
05	P → A			P → S (74 only)	05
06	Set Divert FF			P' S'	06
07	$P_2 = P_1$			$P_2 = P_1$	07
10	Set Read FF, Clear Z			Clear Z	10
11					11
12	MCS → Z			INP → Z (76) MCS → Z (74)	12
13	Clear F			Clear Wait Input FF	13
14				(76)	14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F			+Z → R (15 thru 25)	16
17					17
20	Set Write FF				20
21				Clear A'	21
22					22
23				Toggle A'	23
24				Probe A'	24
25				A' → A	25
26	Clear Divert FF; Set I/O Seq. Set Wait Input FF (76)			Set Wait Output (74)	26
27	Clear Write, Inhibit FF's Set C Cycle, Clear D			Set D Cycle, Clear C	27

Cycle
Stop Recirc.
Wait For Ready (76)

Cycle
Stop Recirc.
Wait For Resume (74 Only)

INSTRUCTION	75 EXTERNAL FUNCTION (EXF)				
	DCC' SEQUENCE				
TIME	D CYCLE	CYCLE	C CYCLE	C'CYCLE	TIME
00					00
01					01
02	Adv. P_1 by 1,Clear S		Adv.P_1 by 1; Clear S	Adv.P_1 by 1; Clear S	02
03					03
04					04
05	P→S		P→S, P' S'	P→S, P' S'	05
06	Set Divert FF				06
07	$P_2 = P_1$		$P_2 = P_1$	$P_2 = P_1$	07
10	Set Read FF, Clear Z		Clear Z^1	Clear Z	10
11					11
12	MCS→Z		MCS→Z	MCS→Z	12
13	Clear F				13
14					14
15	Clear Read FF		Z 0		15
16	Set Inhibit FF, Z→F				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF Set I/O Seq.			Set Function RDY, Z O_L Output Lines	26
27	Clear Write, Inhibit FF's Set C Cycle, Clear D Cycle		Set C'FF; C Cycle Stays Set	Set D Cycle, Clear C Cycle; C' FF	27

INSTRUCTION 77 PROGRAM HALT (HLT)					
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Adv. P_1 by 1, Clear S				02
03					03
04					04
05	P → S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS → Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF				20
21					21
22					22
23					23
24					24
25					25
26	Clear Divert FF, Clear Run FF				26
27	Clear Write, Inhibit FF's D Cycle Stays Set				27

INSTRUCTION ENTER: SWEEP					
TIME	ENTER	SWEEP	B CYCLE	C CYCLE	TIME
00					00
01					01
02	Adv. P_1 by 1;Clear S	Adv.P_1 by 1; Clears			02
03					03
04					04
05	P→S	P→S			05
06					06
07	$P_2 = P_1$	$P_2 = P_1$			07
10	Clear Z	Clear Z			10
11					11
12	A→Z	MCS→Z			12
13					13
14					14
15	Note: Sweep/Enter use Standard D Cycle Timing for Memory Cycle.				15
16					16
17					17
20					20
21					21
22					22
23					23
24					24
25	Clear A				25
26					26
27	D Cycle Stays Set	D Cycle Stays Set			27

INSTRUCTION	INTERRUPT SEQUENCE				
	OCCURS ON D CYCLE ONLY				
TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00					00
01	Set Interrupt 10				01
02	Adv. P_1 by 1; Clear S				02
03	Set Interrupt 20 Set Interrupt 30				03
04	Set Interrupt 40				04
05	Block P→S; P→PSR; INT. ADD.→S				05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z				10
11					11
12	MCS→Z				12
13	Clear F				13
14					14
15	Clear Read FF				15
16	Set Inhibit FF, Z→F				16
17					17
20	Set Write FF				20
21	Clear P				21
22					22
23	INT. ADD→P				23
24					24
25					25
26	Clear Diver, Interrupt FF's				26
27	Clear Write,Inhibit FF's				27

INSTRUCTION BUFFER CYCLE					
TIME	CYCLE	CYCLE	CYCLE	BUFFER CYCLE	TIME
00	Input Ready or Output Resume Occurs on any Cycle Except C Cycle and 51 or 55 Instructions (V906) Clear BSI				00
01				Set Buffer Cycle FF	01
02				BER = BER_1; Clear S;	02
03				Clear Buf. RDY.	03
04					04
05				Tag Reg_3 → S	05
06				Ber S	06
07	Set Buf Sync				07
10	(V903)(Drop Request or Ready)			Clear BFR	10
11					11
12				INP→BFR(IBA); MCS→BFR (OBA)	12
13				Adv. BER by 1	13
14					14
15					15
16	(V902) Set Buf Step				16
17	(V903) Set SSI	Timing Chain Not Running			17
20					20
21					21
22					22
23				Set BSI	23
24				Clear SSI	24
25	Set SSI (Ber ≠ BXR)				25
26				Set Buffer RDY, Info RDY (IBO), Input Req (IBA)	26
27	Start Timing Chain			Clear Buf Step	27

INSTRUCTION LOAD MODE

DC - DC - DC SEQUENCE

TIME	D CYCLE	A CYCLE	B CYCLE	C CYCLE	TIME
00	Set IO Seq.			(RDY Starts Timing Chain)	00
01					01
02	Adv.P_1 by 1, Clear S			Clear S	02
03	(Block Ist Time)				03
04					04
05	P → S			P → S	05
06	Set Divert FF				06
07	$P_2 = P_1$				07
10	Set Read FF, Clear Z			Clear Z	10
11					11
12				INP → Z	12
13	Clear F (Constant Clear			Clear Wait Input F	13
14	On F Register)				14
15	Clear Read FF				15
16	Set Inhibit FF, Z → F				16
17					17
20	Set Write FF		Note:		20
21			Load Mode Executes		21
22			Continuous D C Cycles		22
23			Until Paper Tape Reader		23
24			Sends A Disconnect,		24
25	Set Wait Input FF		Clears I/O Seq, Stores		25
26	Set Wait INP.		Last Word and Hangs Up		26
27	Clear Divert FF		Waiting For A Master		27
	Clear Write,Inhibit FF's		Clear (F Reg. Has All		
	Set C Cycle, Stop		Zeros, So Executes A	Set D Cycle,Clear C	
	Timing Chain, Clear D Cycle		Halt Inst.)	Cycle	

APPENDIX A
CARD PLACEMENT CHARTS

INTRODUCTION

The Card Placement Charts identify the logic element(s) contained on a card, indicate the card type, and describe the location of the card. They are used primarily as a maintenance aid for the replacement of faulty logic cards when troubleshooting the logic chasis. Often it is desirable to know what logic function a circuit on a card fulfills, and the information contained in the charts enables one to find the needed information in the equation file. The charts are also useful because they indicate the other logic elements contained on the card.

Location	A	B	C	D	Type
A 23	E001	E011	E021	E031	20

Figure A-1

If the card at the juncture of horizontal row A and vertical row 23 on the logic chassis is questionable, the Card Placement Charts are used in the following manner (see figure A-1). The card is found in the charts under location A, at line 23 (page A-2). The card must be replaced with a type 20 card. Information about a card type, including pin connections, is found in table 2-1 on page 2-10. The type 20 card contains four inverters, E001, E011, E021 and E031. They are tested at test points A, B, C, and D respectively. The location letter also refers to the section of the card that contains the element; E021 is located in section C, which is the third section from the top as the card is in its normal installation position. A logic element may be found in the equation file, which indicates its logic function.

Sometimes the location of an element is found first in the equation file. The Card Placement Charts are then used to indicate the other elements on the card.

CHASSIS_____

CARD PLACEMENT

CONTROL DATA

TITLE: TEIEPROGRAMER	C P	DOCUMENT NUMBER: 36044000	REV: M
IDP	PROJECT OR PRODUCT: 8092	BY R.F. 5/23/64 CHECKER APPD	SHEET 1 OF 9

REVISION STATUS OF SHEETS

	1	2	3	4	5	6	7	8	9			1	2	3	4	5	6	7	8	9
A	-	-	-	-	-	-	A	-				K	G	H	G	D	J	E	K	G
B	-	-	-	B	-	-	-	-				L	G	J	G	D	L	E	K	G
	-	-	-	-	C	-	-	-	-			M	G	J	G	D	L	E	M	G
	-	-	-	-	D	-	-	-	D											
E	E	-	-	-	-	E	-	-												
F	-	F	-	D	-	E	A	D												
G	G	F	G	D	-	E	A	G												
H	-	H	-	-	-	-	-	-												
J	G	H	G	D	J	E	J	G												

REVISIONS

REV	ECO		DRFT	DATE	CHKD	APPD
A	1354	MODIFIED CARD PLACEMENT	ADA	9-14-64	[illegible]	[illegible]
B	1401	G19(16) WAS 52(16) - SHT 5	RRC	9-16-4	[illegible]	[illegible]
C	1402	Location H21 was Capacitor, Type 82	LLN	9/23/64	S.S.	[illegible]
D	1411	SEE ECO	LLN	9/24/64	S.S.	[illegible]
E	1431	SEE ECO	WR	10-19-64		[illegible]
F	1585	SEE ECO	KCH	3-5-65	[illegible]	[illegible]
G	2041	SEE ECO	R.W.	3/14/66	[illegible]	[illegible]
H	2383	SEE ECO	JRB	3-1-67	[illegible]	[illegible]
J	2870	SEE ECO	W.R.	1-4-68	R.H.	R.K. Lawson 1-10-67
K	2937	SEE ECO	T.N.O.	3-11-8	R.H.	R.K. [illegible]
L	3130	SEE E.C.O.	J.A.T.	7-31-68	R.H.	R.H.
M	3326	LOCATION M29 CARD TYPE WAS 87	RW	1-8-69	R.H.	R.H.

NOTE

COPIES TO

7384-1

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	G

SHEET 2 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
A 1	W200				11	B 1	A003	A013	A023	A033	20
2	W202				11	2	A000		A001		31
3	W204				11	3	I212		I214		23
4	R000		R010		24	4	I213	I215	I211	I209	20
5	R020		R030		24	5	I210		I208		23
6	R040		R050		24	6	A010		A011		31
7	R060		R070		24	7	A012		A002		21
8	W208				11	8	W252				11
9	W210				11	9	W262				11
10	W212				11	10	W264				11
11	W214				11	11	I363	V032	I550	I578	20
12	Q000		E302		22	12	A020		A021		31
13	Q010		Q020		23	13	I204		I206		23
14	Q030		Q040		23	14	I207	I205	I203	I201	20
15	Q050		Q060		23	15	I202		I200		23
16	Q070		E400		23	16	A030		A031		31
17	U000		U010		22	17	A032		A022		<1
18	E000				12	18	A040		A041		33
19	E010				12	19	A042		A043		21
20	U020		U030		22	20	A050		A051		33
21	E020				12	21	A052		A053		21
22	E030				12	22	W250				11
23	E001	E011	E021	E031	20	23	W260				11
24	U040		U050		22	24	A060		A061		33
25	E040				12	25	A062		A063		21
26	E050				12	26	A070		A071		33
27	U060		U070		22	27	A072		A073		21
28	E060				12	28	I403		I359		21
29	E070				12	29	N230				11
30	E041	E051	E061	E071	20	30	A100		A101		32
31	E300				13	31	A110		A111		32
32	E301				13	32	A120		A121		32
33	E200	E201	E202	E310	20	33	A130		A131		32
34	E311		F332		21	34	N240				11
35	E401		E402		23	35	N241				11
36	E500	E503	E506	I401	20	36	A140		A141		32
37	E501		E504		22	37	A150		A151		32
38	E502		E505		23	38	A160		A161		32
39	E507		I402		22	39	A170		A171		32
40	N212	N232	N244	I400	20	40	N210				11

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	J

SHEET 3 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE
C 1	X000	X001	X010	X011	30
2	X020	X021	X030	X031	30
3	W364				12
4	I300		I301		22
5	I310		I311		22
6	I361				12
7	I369		I364		21
8	I362				13
9	I320		I321		22
10	I330		I331		22
11	X100	X101	X110	X111	30
12	X120	X121	X130	X131	30
13	W366				12
14	I302				13
15	I303				12
16	I322		I332		23
17	I323		I333		21
18	X200	X201	X210	X211	30
19	X220	X221	X230	X231	30
20	W368				12
21	I354		I356		22
22	I358		I860		22
23	I355		I357		21
24	P100		P101		33
25	P102	P103	P112	P113	30
26	P110		P111		33
27	W005				13
28	W464				11
29	W073				11
30	P120		P121		33
31	P122	P123	P132	P133	30
32	P130		P131		33
33	P114	P124	P125	I360	20
34	P104		I872		21
35	I861	I853	I865	I866	20
36	I863				11
37	I852				11
38	K864		K865		32
39	I867	I868	I871	I874	20
40	I216	I217	I218	I219	20

LOCATION	A	B	C	D	TYPE
D 1	W000				11
2	P000		P001		33
3	P002	P003	P012	P013	30
4	P010		P011		33
5	W070				11
6	W460				11
7	P020		P021		33
8	P022	P023	P032	P033	30
9	P030		P031		33
10	P004				11
11	P014		P054		21
12	P024	P025	P055	P064	20
13	P044				11
14	W003				12
15	P040		P041		33
16	P042	P043	P052	P053	30
17	P050		P051		33
18	W072				11
19	W462				11
20	P060		P061		33
21	P062	P063	P072	P073	30
22	P070		P071		33
23	M850	M851	M852		68
24	K850	K851	K862	K863	30
25	Y902	Y901	Y850	Y903	73A
26	I851		I873		22
27	K852		K853		32
28	K854		K855		31
29	K856		K857		32
30	K858		K859		31
31	K860		K861		31
32	I850	I856	I858	I862	20
33	I857		I859		21
34	I854		I855		24
35	W110				12
36	W112				11
37	W020		F303		21
38	W050		W051		21
39	I365	I366	I367	J012	20
40	I312				13

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	G

SHEET 4 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
E 1	W801				11	F 1	G100				G10
2	P200	P201	P210	P211	30	2	G102				G10
3	P220	P221	P230	P231	30	3	G104				G10
4	P204	P214	P224	P234	20	4	G106				G10
5	W803				11	5	G001				G10
6	P240	P241	P250	P251	30	6	G003				G10
7	P260	P261	P270	P271	30	7	G005				G10
8	P244	P254	P264	P274	20	8	G007				G10
9	W800		W813		21	9	Y001		Y003		G12
10	P202	P203	P212	P213	20	10	Y005		Y007		G12
11	P222	P223	P233	P243	20	11	Y000		Y002		G12
12	P232		P242		22	12	Y004		Y006		G12
13	P252				22	13	G000				G10
14	P253	P262	P263	P272	20	14	G002				G10
15	P273	W810	W058	W023	20	15	G004				G10
16	W811				11	16	G006				G10
17	W805				11	17	T200		T201		53
18	P280	P281	P290	P291	30	18	T202		T203		53
19	P300	P301	P310	P311	30	19	T204		T205		53
20	P284	P294	P304	P314	20	20	T206		T207		53
21	P282	P283	P292	P293	20	21	T100		T101		53
22	P302	P303	P312	P313	20	22	T102		T103		53
23	W052				11	23	T104		T105		53
24	W054				11	24	T000		T001		53
25	W056				11	25	T002		T003		53
26	W021				11	26	T004		T005		53
27	S000		S001		33	27	J562		J563		21
28	I006		I016		23	28	K100		K101		32
29	S010		S011		33	29	T500		T501		53
30	S020		S021		33	30	T502		T503		53
31	I026		I036		23	31	T504		T505		53
32	S030		S031		33	32	T506		T507		53
33	S040		S041		33	33	J565		I368		21
34	I046		I056		23	34	K130		K131		32
35	S050		S051		33	35	K110		K111		32
36	S060		S061		33	36	K120		K121		32
37	I066		I076		23	37	S100		S101		32
38	S070		S071		33	38	S110		S111		32
39	W327				11	39	S120		S121		32
40	I313				12	40	S130		S131		32

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	D

SHEET 5 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
G 1	Y100		Y102		G12	H 1	Y200				G14
2	Y104		Y106		G12	2	Y210				G14
3	Y101		Y103		G12	3	Y220				G14
4	Y105		Y107		G12	4	Y230				G14
5	D100				G19	5	Y240				G14
6	D101					6	Y250				G14
7	D102					7	Y260				G14
8	D103					8	Y270				G14
9	D104					9	G101				G10
10	D105					10	G103				G10
11	D106					11	G105				G10
12	D107					12	G107				G10
13	D000					13	G200		G201		G11
14	D001					14	G202		G203		G11
15	D002					15	G204		G205		G11
16	D003					16	G206		G207		G11
17	D004					17	Y500		Y501		G13
18	D005					18	Y502		Y503		G13
19	D006					19	Y504		Y505		G13
20	D007				G19	20	Y506		Y507		G13
21	T300		T301		53	21	Y900	Y910--	Y960	Y970	G20
22	T302		T303		53	22	W102		W325		21
23	T304		T305		53	23	W326				11
24	T306		T307		53	24	W323				11
25	Z000		Z001		32	25	I001		I002		23
26	I004		I014		22	26	I011		I012		23
27	Z010		Z011		32	27	I021		I022		23
28	Z020		Z021		32	28	I031		I032		23
29	I024		I034		22	29	I041		I042		23
30	Z030		Z031		32	30	I051		I052		23
31	W122				11	31	I061		I062		23
32	W124				11	32	I071		I072		23
33	W100				11	33	M000	M010	M020		68
34	W320				11	34	M030	M040	M050		68
35	Z040		Z041		32	35	M060	M070	M322		68
36	I044		I054		22	36	0000	0001	0010	0011	30
37	Z050		Z051		32	37	0020	0021	0030	0031	30
38	Z060		Z061		32	38	0040	0041	0050	0051	30
39	I064		I074		22	39	I005	I015	I025	I035	20
40	Z070		Z071		32	40	I045	I055	I065	I075	20

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	L

SHEET 6 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
I 1	H000				44	J 1	K000		K001		32
2	V000				12	2	K002		K003		31
3	V010		F500		22	3	K010		K011		32
4	H001				41	4	K012		K013		31
5	V001				12	5	J020	J030	J110	J224	20
6	C000		C001		02	6	J021		J022		21
7	N000		N001		21	7	J000		J002		21
8	H002				41	8	J001				11
9	V002				12	9	J003		J006		21
10	V012				14	10	J004		J031		21
11	H003				41	11	J007				11
12	V003				12	12	J008				11
13	V013				13	13	J009		J200		21
14	V023		V004		22	14	K200		K201		32
15	H004				41	15	H201				41
16	H005				41	16	V201		V211		22
17	V005				12	17	H211				41
18	V015				13	18	K210		K211		33
19	V025				13	19	C004		C005		02
20	V035		V046		23	20	N005		J210		21
21	C002		C003		02	21	J211				11
22	H006				41	22	J212		J220		21
23	V006				12	23	K220		K221		32
24	V016				13	24	H221				41 A
25	V026				13	25	V221				12
26	V036				13	26	J221				11
27	H007				41	27	J222				11
28	V007		F086		22	28	F052		J230		21
29	V017				13	29	K230		K231		32
30			C007		02	30	H231				41
31	W162				11	31	V231		J234		22
32	W164		I408		21	32	J231		J235		21
33	I404		I406		22	33	J232				11
34	I405	I407	I411	I413	20	34	J233				11
35	I409		I410		21	35	K140		K141		32
36	I412		J914		21	36	K222		K223		32
37	L000	L010	L020		69	37	J225		J226		21
38	L030	L040	L050		69	38	J227		J228		21
39	L060	L070	L080		69	39	J223		J243		21
40	L090	L100	L110		69	40	F054	F056	F057	J111	20

CHASSIS_____

CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P	DOCUMENT NUMBER	REV
	36044000	E

SHEET 7 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
K 1	F000		F001		31	L 1	F200		F215		22
2	F002	F015	F042	F053	20	2	F202		F204		23
3	F003		F012		21	3	F203	F206	F207	F209	20
4	F010		F011		31	4	F205		F208		23
5	F013		F014		21	5	F210				13
6	F020		F021		31	6	F211	F216	F222	F219	20
7	F022		F023		21	7	F214		J910		21
8	F025				11	8	F221		F218		22
9	F030		F031		31	9	F217		F225		23
10	W130				11	10	F223		F253		22
11	W160				11	11	F224	F226	F229	F232	20
12	F040		F041		31	12	F227				16
13	F050		F051		31	13	F230		K440		24
14	F100		F101		31	14	F256	F235	F236	F238	20
15	F110	F111	X520	X521	30	15	F233		F234		22
16	F079	F131	F070	F069	20	16	F270		F271		21
17	F078				11	17	F237		F247		23
18	F060		F077		21	18	F240	F242	F243	F244	20
19	F068		F130		22	19	F241		F239		23
20	F067	F066	F059	F065	20	20	F245	F246	F248	F252	20
21	F076		F120		21	21	F249				15
22	F121		F122		21	22	F251		F300		22
23	F123		F124		21	23	F301		F304		23
24	F125		F075		21	24	F302	F306	F307	F310	20
25	F064	F063	F127	F062	20	25	F305		F315		23
26	F074		F073		21	26	F308		F319		22
27	F072		F071		21	27	F311	F313	F316	F317	20
28	F061	J011	F084	F132	20	28	F318	F320	F321	F322	20
29	F087		F114		21	29	F323		V022		23
30	F096		F097		21	30	F324		F326		21
31	F098		F099		21	31	F325	F328	F280	J010	20
32	F094		F085		21	32	F327		F329		21
33	F092		F093		21	33	F331		F112		21
34	F091		F133		21	34	J918		J917		21
35	F134	F082	F081	I414	20	35	J908		J921		22
36	F083				11	36	J909				11
37	F090		F080		21	37	J904		J906		21
38	F088		F089		21	38	F095	J922	J923	J915	20
39	J912				11	39	M907	M908	M909		68
40	J913				11	40	F213				16

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CARD PLACEMENT

CONTROL DATA CORPORATION

IDP

C P | DOCUMENT NUMBER 36044000 | REV M

SHEET 8 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
M 1	K800		K801		31	N 1	X900		X901		32
2	K802		K803		31	2	X902	X903	X912	X913	30
3	K810		K811		31	3	X910		X911		32
4	K812		K813		31	4	W028		I532		21
5	N800		N801		21	5	W024				11
6	V901		J444		23	6	I500				11
7	V902				13	7	W266				11
8	V903				13	8	W370				11
9	K420		K421		33	9	X920		X921		32
10	K320		K321		32	10	X922	X923	X932	X933	30
11	K322		K323		32	11	X930		X931		32
12	L322	L323	L330		69	12	I501	I503	I504	I505	20
13	L331	L321	L421		69	13	X940		X941		32
14	J446	J401	J403	J405	20	14	X942	X943	X952	X953	30
15	J400		J402		22	15	X950		X951		32
16	J404		J445		22	16	I535				11
17	M330	M420	M424		68	17	W030				12
18	K522	K523	K524	K525	30	18	W268				11
19	K240	K241	K442	K443	30	19	W374				11
20	K441				15	20	I531		W269		21
21	V521				16	21	X960		X961		32
22	M900	M901	M902		68	22	X962	X963	X972	X973	30
23	K900		K901		32	23	X970		X971		32
24	K902	K903	K224	K225	30	24	W027				13
25	K904		K905		32	25	X980		X981		32
26	J100	J102	J107	J930	20	26	X982	X983	X992	X993	30
27	J101		J907		22	27	X990		X991		32
28	J106		F212		23	28	W375		W376		21
29	M904	M905	M906		68	29	I538	I517	I519	J104	20
30	J900		J901		21	30	I510				16
31	J902		J903		21	31	I512				16
32	M500	M510	M520		68	32	I514				16
33	M530	M540	M550		68	33	X700		X701		32
34	M560	M570	M903		68	34	X710		X711		32
35	L500	L510	L520		67	35	X720		X721		32
36	L530	L540	L550		67	36	X730		X731		32
37	L560	L570			67	37	X740		X741		32
38	L580	L590	L600		69	38	X750		X751		32
39	L610	L515			69	39	X760		X761		32
40	J905				13	40	X770		X771		32

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CARD PLACEMENT

CONTROL DATA CORPORATION

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C P	DOCUMENT NUMBER	REV
	36044000	G

SHEET 9 OF

CARD PLACEMENT

LOCATION	A	B	C	D	TYPE	LOCATION	A	B	C	D	TYPE
0 1	X500		X501		32						
2	X502		X503		32						
3	X504		X505		31						
4	I554				11						
5	I592		J560		21						
6	I593				11						
7			X514	X515	30						
8	X506		X507		32						
9	X512		X513		32						
10	X508		X509		31						
11	X510		X511		31						
12	I588				11						
13	X516		X517		32						
14	I590		I587		21						
15	F502	J103	F503		28						
16	I552		I589		21						
17	I559	I566	I594	I570	20						
18	I562		I556		21						
19	I573	I558	J441	I595	20						
20	I577				12						
21	I581	J109	I555		28						
22	X518		X519		31						
23	I579		I516		23						
24	I580		I599		21						
25	I584	I585	I586	I598	20						
26	M512	M513	M514		68						
27	L512	L513	L514		69						
28	W360		W361		21						
29	X800	X801	X810	X811	30						
30	X820	X821	X830	X831	30						
31	X840	X841	X850	X851	30						
32	W362		W363		21						
33	X860	X861	X870	X871	30						
34	X880	X881	X890	X891	30						
35	I571				11						
36	I574				11						
37	I582				11						
38	I560				11						
39	I561				11						
40	I553		I551		21						

APPENDIX B
EQUATION FILES

INTRODUCTION

The logical interconnections of printed cards in the computer are described in Boolean algebratic equations. The file of these equations, presented on pages 1 - 33, is the most important source of information about the logic of the computer. Nearly all of the detailed treatment is, directly or indirectly, based on this file.

The File of Equations is a concise and highly organized presentation of logical information. Adequate use is made of the file only when one is thoroughly familiar with the general equation format and the organization or grouping of the equations. The following paragraphs present such preliminary information.

EQUATION FORMAT

In the File of Equations, each circuit has a unique symbol that is composed of a base letter and a three digit numerical code. The base letter of the symbol associates the circuit with one of 25 major logical areas, such as the A register, the Function Translators, etc. (See table B-1). The numerical digits provide a unique identification of the circuit within the major logical area. In addition, the odd or even character of the third digit may identify the output clock phase of some circuits, or the side (set or clear) of a flip flop circuit.

In the circuit symbol A001, for example, the base letter A indicates that this building block is a part of the A register. The first and second numerical digits identify the stage of the A register with which this building block is associated: stage 00. The third numerical digit identifies the FF output. An even digit indicates a "clear" output and an odd digit a "set" output.

An equation represents a single inverter (the standard building block) with the exception of two types of circuit in the storage section. In the equation given below, the symbol on the left side of the equal sign is called the <u>subject term</u> and denotes the circuit described by the equation. The expression on the right of the equal sign describes the logical configuration of the inputs.

TERM 1 OR TERM 2 OR TERM 3

K421 = J901 + J221 V013 F114 F075 + J446 V013

Each input symbol (or group of symbols) separated from the next symbol (or group of symbols) by a + sign constitutes an input term. The + sign represents the OR function or logical sum; the absence of a sign between symbols represents the AND function or logical product. The equation given above for inverter K421 has three terms, each representing an input to the inverter. If any one of the input terms (OR)is a "1", the output of K440 will be a "0". For one of the terms to be a "1", the AND function within it must be fulfilled; thus, J446 and V013 both must have a "1" output for that term to be instrumental in causing a

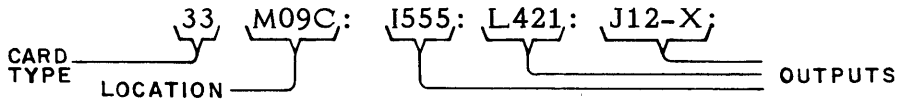
TABLE B-1. Symbol Assignments

A	A Register
C	Clock
D	Diverters
E	Borrow Pyramid
F	F Register and Translators
G	Drive Generators
H	Control Delays
I	Transfer Inverters
J	Second-Level Controls
K	Control Flips Flops
L	Output Amplifiers
M	Input Amplifiers
N	First-Level Controls
O	O Register
P	P Register
Q,R	Pyramid Inputs
S	S Register
T	Storage Control Transfers
U	Stage Borrow Inputs
V	Control Delay Outputs
W	Register Transfer and Pyramid Controls
X	Buffer, Tag Register and Controls
Y	Sense Amplifiers and Non-Logic Elements
Z	Z Register

"0" output from K421.

K420 constitutes the other half of the FF K420/K421, and is connected to K421 within the FF itself. In some instances an equation has two identical input terms. This is done to use all available input pins to the inverter, because an unused input pin is sensed by the inverter as a "1". The number of input pins available varies (see the Description of Standard Card Types table).

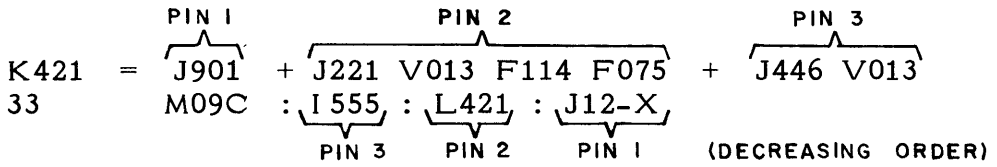
The second line of the equation shows the type of card used, the physical location of the card containing the subject symbol, and the elements connected to the output pins of the logic element. The second line of the equation of the subject term K421 is given below.



The card type and location are explained in the Card Placement Charts. The outputs of K421 are connected to the input of I555 and L421, and terminal J12-X.

PIN ASSIGNMENT

Each input term in an equation is connected to a separate input pin of the card (or section of the card) involved, and each output symbol must be connected to a separate output pin of the subject symbol. Successive input terms are assigned to successive input pin numbers, and successive output symbols to <u>decreasing</u> pin numbers. This system applies to the FF series cards (types 31, 32, 33) only in part, because one input term, and one output term, is a feed-back term wired internally on the printed circuit to the other inverter constituting the FF. The pin assignments for the K421 circuit are shown below:



The card type 33 has 3 input connections and 3 output connections. All 6 pins are used. All the input pins must be used, so the inverter does not sense a logical one from an un-connected pin. The output pins need not all be used, however. Feed back connections (to K420) are not shown in the equation.

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LOGIC EQUATIONS EF

CONTROL DATA

TITLE: LOGIC EQUATIONS 8092 - TelePrOgrammer		DOCUMENT NUMBER 36043800	REV 5
IDP (PROJECT OR PRODUCT)	BY JHN		SHEET 1 OF 34
	CHECKER		
	APPD		

REVISION STATUS OF SHEETS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A	-	-	-	-	-	-	-	-	-	-	A	-	-	-	-	-	-
B	-	-	-	-	B	-	B	-	-	-	-	-	B	-	-	-	-	-	-	-	-	-	-	-	-	B	B	-	-	-	-	-
C	-	-	-	-	-	-	-	C	C	-	-	-	-	-	-	-	-	C	-	-	-	-	-	-	-	-	C	-	-	C	-	-
D						F	E		E	D	D		E	E	E	E			E								D			E	E	
33	34					H		H					F					H	F								H			F	F	
-	-													G																H	G	
-	C																															
D	D																															
J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	-	J	J	J	J	J	J	J	J	J	J

REVISIONS

REV	ECO		DRFT	DATE	CHKD	APPD
A	1291	SEE ECO	K.H.	5-26-64		
B	1343	SEE ECO	LLN	6/26/64		
C	1354	SEE ECO		7-31-64	JW	
D	1402	SEE ECO	LLN	9/24/64		
E	1411	SEE ECO	LLN	9/24/64		
F	1431	SEE ECO	JAK	10/20/64		
G	1470	SEE ECO	MKB	11/9/64		RSW
H	1505	SEE ECO	DRB	1-7-65		RSW
J	1585	SEE ECO	KCH	3-8-65		
K	2041	SEE ECO	R.W.	3-14-66		
L	2085	ADDED V007 TO THE "AND" INPUT TO K864 SHT 8	WDW	3-22-66		
M	2329	SEE ECO	W.B.	2-24-67		
N	2383	SEE ECO	JRB	3-1-67		
P	2870	SEE ECO	D.R.	1-5-68	R.H.	

NOTE SEE SHT 1B FOR REV. LEVEL R.H.

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CONTROL DATA

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TITLE LOGIC EQUATIONS
8092 - TELEPROGRAMMER

PRODUCT

EQ | DOCUMENT NO. 36043800 | REV. R

SHEET 1A OF 34

REVISION STATUS OF SHEETS

1	2	3	4	5	6	7	8	9	10	11	12
K	J	J	J	K	K	K	K	K	K	K	K
L	J	J	J	K	K	K	K	K	K	K	K
M	J	J	J	K	K	K	K	K	K	K	K
N	J	J	J	K	K	K	K	K	K	K	K
P	J	J	J	K	K	K	P	K	P	K	K
13	14	15	16	17	18	19	20	21	22	23	24
K	J	K	K	K	J	K	J	J	–	J	J
K	J	K	K	K	L	K	J	J	–	J	J
K	J	K	K	M	L	K	J	J	-	J	J
K	N	K	K	M	N	K	J	J	-	J	J
P	N	K	K	M	N	K	Q	J	-	J	J
25	26	27	28	29	30	31	32	33	34		
J	J	J	J	J	K	K	J	J	K		
J	J	J	J	J	K	K	J	J	K		
J	J	M	J	J	K	K	J	J	K		
J	J	P	J	J	P	K	J	J	K		

REVISIONS

REV.	ECO	DESCRIPTION	DRFT.	DATE	CHKD.	APPD.
K		SEE SHEET 1				
L		SEE SHEET 1				
M		SEE SHEET 1				
N		SEE SHEET 1				
P	2870	SEE SHEET 1	W.R.	1-568	R.H.	RKL
Q	2937	SEE ECO 2937	T.N.O.	3-11-68	R.H.	RKL
R	3130	SEE E.C.O.	J.A.T.	7-31-68	R.H.	R.H.

NOTES:

SEE SHT 1B FOR REV. LEVEL
R.H.

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FORM 586

CONTROL DATA

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TITLE LOGIC EQUATIONS
8092—TELEPROGRAMMER

PRODUCT

DOCUMENT NO. EQ 36043800

REV. 5

SHEET 18 OF 34

REVISION STATUS OF SHEETS

1	1A	1B	2	3	4	5	6	7	8	9	10
R	R	R	J	J	J	K	K	K	P	K	R
S	R	S	J	J	J	K	K	K	P	K	R
11	12	13	14	15	16	17	18	19	20	21	22
K	K	P	N	K	K	M	N	K	R	J	–
K	K	P	N	K	K	S	N	K	R	J	–
23	24	25	26	27	28	29	30	31	32	33	34
J	J	J	J	P	J	J	R	K	J	J	K
J	J	J	J	P	J	J	R	K	J	J	K

REVISIONS

REV.	ECO	DESCRIPTION	DRFT.	DATE	CHKD.	APPD.
R	3130	SEE E.C.O.	J.A.T.	7-31-68	R.H.	R.H.
5	3333	SEE ECO	RW	1-29-69	R.H.	R.H.

NOTES:

COPIES TO				BY		DATE	CHKD.	R.H.	DATE 8-1-68	APPD.		DATE

AA-1591

N

A000 = I213
31 B02A: A003: I300: Q000: Q010: R000:

A001 = I215
31 B02C: A002: I301: J10-P: X800: X900:

(J) A002 = A001
21 B07C: F246: X801: X901:

A003 = A000
20 B01A: I001: S000:

A010 = I209
31 B06A: A013: I310: Q010: Q020: R010:

A011 = I211
31 B06C: A012: I311: J10-R: X810: X910:

A012 = A011
21 B07A: F246: X811: X911:

A013 = A010
20 B01B: I011: S010:

A020 = I205
31 B12A: A023: I320: Q020: Q030: R020:

A021 = I207
31 B12C: A022: I321: J10-S: X820: X920:

A022 = A021
21 B17C: F246: X821: X921:

A023 = A020
20 B01C: I021: S020:

A030 = I201
31 B16A: A033: I330: Q030: Q040: R030:

A031 = I203
31 B16C: A032: I331: J10-T: X830: X930:

A032 = A031
21 B17A: F246: X831: X931:

A033 = A030
20 B01D: I031: S030:

A040 = I219 + A141 W250 + X941 W260
33 B18A: A043: Q040: Q050:

A041 = X940 W260 + A140 W250 + J906
33 B18C: A042: J10-U:

A042 = A041
21 B19A: F245: X841: X941: R040:

A043 = A040
21 B19C: I041: S040: X840: X940:

A050 = I218 + A151 W250 + X951 W260
33 B20A: A053: Q050: Q000:

A051 = X950 W260 + A150 W250 + J906
33 B20C: A052: J10-V:

A052 = A051
21 B21A: F245: X851: X951: R050:

A053 = A050
21 B21C: I051: S050: X850: X950:

A060 = I217 + A161 W250 + X961 W260
33 B24A: A063: Q060: Q070:

A061 = X960 W260 + A160 W250 + J906
33 B24C: A062: J10-W:

(J) A062 = A061
21 B25A: : F245: X861: X961: R060:

A063 = A060
21 B25C: I061: S060: X860: X960:

A070 = I216 + A171 W250 + X971 W260
33 B26A: A073: Q000: Q070:

A071 = X970 W260 + A170 W250 + J906
33 B26C: A072: J10-X: X970:

(J) A072 = A071
21 B27A: F245: F249: X871: R070: X971

A073 = A070
21 B27C: F249: I071: S070: X870:

A100 = E000 N230 + E001 N241 E500
32 B30A: I214: I401: P001:

A101 = E500 N241 E000 + N210
32 B30C: I212: P000:

A110 = E010 N230 + E011 N241 E501
32 B31A: I210: I401: P011:

A111 = E501 N241 E010 + N210
32 B31C: I208: P010:

A120 = E020 N230 + E021 N241 E502
32 B32A: I206: I401: P021:

A121 = E502 N241 E020 + N210
32 B32C: I204: P020:

A130 = E030 N230 + E031 N241 E503
32 B33A: I202: I401: P031:

A131 = E503 N241 E030 + N210
32 B33C: I200: P030:

```
A140 = E040 N230 + E041 N240 E504
32  B36A:  A041:  I400:  P041:

A141 = E504 N240 E040 + N210
32  B36C:  A040:  P040:

A150 = E050 N230 + E051 N240 E505
32  B37A:  A051:  I400:  P051:

A151 = E505 N240 E050 + N210
32  B37C:  A050:  P050:

A160 = E060 N230 + E061 N240 E506
32  B38A:  A061:  I400:  P061:

(J) A161 = E506 N240 E060 + N210
32  B38C:  A060:  P060:

A170 = E070 N230 + E071 N240 E507
32  B39A:  A071:  I400:  P071:

A171 = E507 N240 E070 + N210
32  B39C:  A070:  P070:

C000 =
02A I06A:   N000:  V000:  V002:  V004:  V006:

C001 =
02A I06C:   N001:  V001:  V003:  V005:  V007:

C002 =
02A I21A:   N800:  V010:  V016:

C003 =
02A I21C:   N801:  V013:  V015:  V017  V025:

C004 =
02A J19A:          V046:  V022:

C005 =
02A J19C:   N005:  V201:  V211:  V221:  V231:

C007 =
02A I30C:   V023:

(J) D000 = T004 T002 T000
G19 G13:

D001 = T004 T002 T001
G19 G14:

D002 = T004 T003 T000
G19 G15:

D003 = T004 T003 T001
G19 G16

(J) D004 = T005 T002 T000
G19 G17:

(J) D005 = T005 T002 T001
G19 G18:

D006 = T005 T003 T000
G19 G19:

D007 = T005 T003 T001
G19 G20:

D100 = T104 T102 T100
G19 G05

D101 = T104 T102 T101
G19 G06

D102 = T104 T103 T100
G19 G07:

D103 = T104 T103 T101
G19 G08:

D104 = T105 T102 T100
G19 G09:

D105 = T105 T102 T101
G19 G10

D106 = T105 T103 T100
G19 G11:

(J) D107 = T105 T103 T101
G19 G12:

E000 = R000 Q000 + U000
12  A18:   A100:  A101:  E001:  E200:  E501:
                                      E502:

E001 = E000
20  A23A:  A100:

E010 = R010 Q010 + U010
12  A19:   A110:  A111:  E011:  E200:  E300:
                                E502:  E502:

E011 = E010
20  A23B:  A110:

E020 = R020 Q020 + U020
12  A21:   A120:  A121:  E021:  E200:  E300:
                                      E300:

E021 = E020
20  A23C:  A120:

E030 = R030 Q030 + U030
12  A22:   A130:  A131:  E031:  E201:  E504:
                                      E505:

E031 = E030
20  A23D:  A130:
```

36043800

```
E040 = R040 Q040 + U040
12  A25:    A140:  A141:  E041:   E201:  E301:
                                  E505:  E505:

E041 = E040
20  A30A:   A140:

E050 = R050 Q050 + U050
12  A26:    A150:  A151:  E051:   E201:  E301:
                                         E301:

E051 = E050
20  A30B:   A150:

E060 = R060 Q060 + U060
12  A28:    A160:  A161:  E061:   E202:  E507:

E061 = E060
20  A30C:   A160:

E070 = R070 Q070 + U070
12  A29:    A170:  A171:  E071:   E202:  E302:

(J) E071 = E070
20  A30D:   A170:

E200 = E020 E010 E000
20  A33A:   E401:  E402:

E201 = E050 E040 E030
20  A33B:   E400:  E402:

E202 = E070 E060
20  A33C:   E400:  E401:

E300 = U020 + E020 U010 + E020 E010 U000
13  A31:    E310:  E401:  E401:   E402:

E301 = U050 + E050 U040 + E050 E040 U030
13  A32:    E310:  E400:  E402:   E402:

(J) E302 = U070 + E070 U060
22  A12C:   E310:  E400:  E400:   E401:

E310 = E302 E301 E300
20  A33D:   E311:

E311 = E310
21  A34A:   E400:  E401:  E402:

E400 = E302 E301 E201 + E311 + E202 E302
23  A16C:   E500:  E501:  E502:

E401 = E302 E300 E202 + E311 + E300 E200
23  A35A:   E503:  E504:  E505:

E402 = E301 E300 E200 + E311 + E201   E301
23  A35C:   E506:  E507:

E500 = E400
20  A36A:   A100:  A101

E501 = U000 + E400 E000
22  A37A:   A110:  A111:

E502 = U010 + E010 E400 E000 + U000 E010
23  A38A:   A120:  A121:

E503 = E401
20  A36B:   A130:  A131:

E504 = U030 + E401 E030
22  A37C:   A140:  A141:

E505 = U040 + E040 E401 E030 + E040 U030
23  A38C:   A150:  A151:

E506 = E402
20  A36C:   A160:  A161:

E507 = U060 + E402 E060
22  A39A:   A170:  A171:

F000 = Z001 W160
31  K01A:   F003:  F062:  F064:   F065:  F069:

F001 = W130
31  K01C:   F002:  F061:  F063:   F066:  F502:

F002 = F001
20  K02A:   F130:  F503:

F003 = F000
21  K03A:   F067:  F068:  F079:   F124:  F234:

F010 = Z011 W160
31  K04A:   F013:  F015:  F061:   F064:

F011 = W130
31  K04C:   F012:  F014:  F062:   F063:  F065:

F012 = F011
21  K03C:   F067:  F070:  F124:   F127:

F013 = F010
21  K05A:   F068:  F120:  F227:   F227:  F237:

F014 = F011
21  K05C:   F208:  F210:  F218:   F223:  F230:

F015 = F010
20  K02B:   F069:  F066:

F020 = Z021 W160
31  K06A:   F023:  F025:  F061:   F062:  F063:
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F021 = W130
31 K06C: F022: F064: F065: F066: F124:

F022 = F021
21 K07A: F070: F120: F218: F230: F318:

F023 = F020
21 K07C: F079: F127: F202: F208: F210:

F025 = F020
11 K08: F218: F230: F241: F253: F322: F213:

F030 = Z031 W160
31 K09A: F080: F084: F086: F213:

F031 = W130
31 K09C: F081: F085: F087: F132: F202:

F040 = Z041 W160
31 K12A: F080: F081: F084: F085:

F041 = W130
31 K12C: F042: F082: F086: F087: F202:

F042 = F041
20 K02C: F212:

F057 = F056 F063
20 J40C: F213:

F054 = F074:
20 J40A: F213:

F050 = Z051 W160
31 K13A: F053: F080: F081: F202:

F051 = W130
31 K13C: F052: F084: F085: F086: F087:

F052 = F051
21 J28A: F082: F132: F217:

F053 = F050
20 K02D: F212:

F056 = F076
20 J40B: F057:

F059 = F064 F065 F124
20 K20C: K440: K441:

F060 = F069
21 K18A: F225: F225: F225:

F061 = F020 F010 F001
20 K28A: F071: F213:

F062 = F020 F011 F000
20 K25D: F072: F213:

F063 = F020 F011 F001
20 K25B: F073: F057:

F064 = F021 F010 F000
20 K25A: F059: F074:

F065 = F021 F011 F000
20 K20D: F059: F075:

F066 = F021 F015 F001
20 K20B: F076: F241:

F067 = F012 F003
20 K20A: F077: F213:

F068 = F013 + F003
22 K19A: F217: F241: F249: J106:

F069 = F015 F000
20 K16D: F060:

F070 = F022 F012
20 K16C: F078:

F071 = F061
21 K27C: F202: F249: F320:

F072 = F062
21 K27A: F207: F249: F308: F324: K420:

F073 = F063
21 K26C: F249: F270: F325: K320:

F074 = F064
21 K26A: F249: F326: K320: F213: F054:

F075 = F065
21 K24C: F204: F328: F331: K420: K421:

F076 = F066
21 K21A: I579: J106: F237: F213: F056

F077 = F067
21 K18C: F212: F212: F217: F227: F277:

F078 = F070
11 K17: F208: F210: F234: F237: F249: F500: J106: X50

F079 = F023 F003
20 K16A F131:

F080 = F050 F040 F030
21 K37C: F088: F089: F112:

F081 = F050 F040 F031
20 K35C: F090: F232:

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F082 = F052 F041
20 K35B: F083: F134:

F083 = F082
11 K36: F225: F227: F227: F230: F253: F213: F213:

F084 = F051 F040 F030
20 K28C: F091: F232:

(K) F085 = F051 F040 F031
21 K32C: F092: F236: F240: F093:

F086 = F051 F041 F030 + GND
22 I28C: F094: F232: F251: F095:

F087 = F051 F041 F031
21 K29A: F096: F097: F098: F099: F114:

F088 = F080
21 K38A: F127: F208: F210: F234: F320:

F089 = F080
21 K38C: F217: F230: F237: F237: F328:

(J) F090 = F081
21 K37A: F202: F270: F318: F322: F213:

F091 = F084
21 K34A: F200: F204: F225: F227: F213:

F092 = F085
21 K33A: F200: F202: F204: F227: F230:

(K) (J) F093 = F085
21 K33C: F213: F239: F303: F331: I550

F094 = F086
21 K32A: F208: F210: F217: F241:

F095 = F086
20 L38A: F213:

F096 = F087
21 K30A: F120: F124: F218: F331: F308:

F097 = F087
21 K30C: F204: F207: F208: F210: F218:

(K) F098 = F087
21 K31A: F223: F230: K320: F237:

F099 = F087
(K) 21 K31C: F241: F500: J106: K441: X500

F100 = Z061 W160
31 K14A: I356:

F101 = W130
31 K14C: I354: I358: W810: I860: F280:

(F) F110 = Z071 W160
30 K15A: I354:

(F) F111 = W130
30 K15B: I356: I358:

F112 = F080
21 L33C: F324: F325: F326: I579: J106:

F114 = F087
21 K29C: K320: K420: K420: K421: K440:

(K)

F120 = F096 F022 F013
21 K21C: F121: F122: F123: F203:

F121 = F120
21 K22A: F223: F306: F317: F319: F210:

F122 = F120
21 K22C: F212: F305: F315: F323:

F123 = F120
21 K23A: F233: F239: F253: K440: K441:

(K) (F) F124 = F096 F021 F012 F003
21 K23C: F059: F125: F240: X521

F125 = F124
21 K24A: F233: F239: F313: K322: K864:

(H) (K) F127 = F088 F023 F012
20 K25C: F130:

F130 = F127 + F002
22 K19C: F327:

F131 = F079
20 K16B: F217: F321:

F132 = F052 F031
20 K28D: F133: F134:

F133 = F132
21 K34C: F225: F227: F227:

F134 = F132 F082
20 K35A: F241: F212:

F200 = J221 J226 F092 + J221 F091
22 L01A: W124: W323:

F202 = F090 F023 + F092 F071 J228 + F050 F041 F031
23 L02A: F023

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F203 = F202 F120
20 L03A: F319:

F204 = F091 + F092 J226 + F097 F075
23 L02C: F205:

F205 = F207 J211 + F204 J223 + X505 X511
23 L04A: F206:

F206 = J234 J915 F205 J200
20 L03B: F307:

(J) F207 = F097 J226 F072
20 L03C: F205:

(E)(K) F208 = F088 F023 F014 + F097 F078
X517 + F094 F251
23 L04C: F209: F242: F323:

F209 = F208
20 L03D: F329:

(E) F210 = F252 F094 + F088 F023 F014 I552 J233+
F097 F078 I588
(J) 13 L05A: F211: F238: I354: I356: W368:
I359:

F211 = F210
20 L06A: F300: F301:

F212 = F122 J227 + F134 F077 + F053 F042
F077
23 M28C: F214:

(J) F213 = F093 F067 + F091 F061 F062 + F090
F076 + F095 F025 F054 + F083
F057 + F074 F030 F083
16 L40: J107: K231:

F214 = F212
21 L07A: F215: F221: K210:

(J) F215 = J211 F214 + J223 F219
22 L01C: F216:

F216 = J200 J921 F215 J234
20 L06B: F302:

F217 = F068 F052 + F089 F077 F131 + F094
23 L09A: F219: F224:

F218 = F096 F025 F014 + F097 F022
22 L08C: F219:

F219 = J912 F217 F218
20 L06D: F215:

F221 = J211 F214 + F224 J912 J223
22 L08A: F222:

F222 = J200 J921 F221 J234
20 L06C: F300:

F223 = F098 F014 + F121 J227
22 L10A: F224:

F224 = F217 F223
20 L11A: F221:

F225 = F133 F060 + F091 F060 + F060 F083
23 L09C: F226:

F226 = F225
20 L11B: F304: K200:

F227 = F091 + F077 F133 + F013 F133 +
F083 F077 + F083 F013 + F092 J227
16 L12: F229:

(J) F229 = F227
20 L11C: F304: F305

F230 = F025 F089 F014 + F092 + F083 F022 +
F098 F233
24 L13A: F232:

F232 = F086 F084 F230 F081
20 L11D: F315:

F233 = F123 + F125
22 L15A: F230: F236: F323:

F234 = F003 F088 F078 + GND
22 L15C: F235: F238: F332:

F235 = F234
20 L14B: F323:

F236 = F233 F085
20 L14C: K222:

F237 = F089 F078 + F089 F013 + F098 F076
23 L17A: F238:

F238 = J921 F270 F237 F234 F210
20 L14D: F244:

F239 = F093 J228 + F123 I403 J441 + F125 J227
23 L19C: K223: K230:

F240 = F085 F124
20 L18A: F243:

F241 = F134 F068 + F094 F251 + F099 F025
F066
23 L19A: F242:

F242 = F241 F208 J912
20 L18B: K220:

F243 = F240 K224
20 L18C: K221: K230:

F244 = J923 F238
20 L18D: H231:

F245 = A072 A062 A052 A042
20 L20A: F247:

F246 = A032 A022 A012 A002
20 L20B: F247:

F247 = F245 + F246 + GND
23 L17C: F248: F249:

F248 = F247
20 L20C: F249:

F249 = F247 F078 F068 + F248 F071 + A072
F072 + A073 F073 + F074
15 L21: F251:

F251 = F249 + F086
22 L22A: F208: F241: F252:

F252 = F251
20 L20D: F210:

F253 = F123 J223 + F083 F025
22 L10C: F256

F256 = F253
20 L14A: F316:

(K)

F280 = F101 F271 V025
20 L31C: J922:

(J) F270 = F073 F090
21 L16A: F238: F271:

F271 = F270
21 L16C: I860: I873: K865: W810 F280:

F300 = K240 J001 V032 I590 F222 + V003 J231
F211 J007
22 L22C: W000: W003: W005:

F301 = F211 J231 V017 + V007 J001 + I872
23 L23A: W070: W072: W073:

F302 = V006 F216 I853 J001
20 L24A: W050: W052:

F303 = F093 J225
21 D37C: W023:

F304 = V015 J211 F226 + F229 J223 V015 + GND
23 L23C: W054:

F305 = V015 J221 F229 + V015 J224 F122 J211 +
X505 V015
23 L25A: W051:

F306 = V015 J211 F121 J225
20 L24B: W056:

F307 = J912 F206
20 L24C: W320:

(J) F306 = J225 J212 F096 F072 + J913 J243
22 L26A: I577: W122: W323:

F310 = V013 J231
20 L24D: W130:

F311 = V006 J231 J004
20 L27A: W160:

F313 = V005 J221 F125 J228 J004
20 L27B: W162: W164:

F315 = GND + J212 J021 J228 F122 + F232 J222
J021
23 L25C: W202:

F316 = J021 J222 F256
20 L27C: W200:

F317 = J021 J212 F121 J226
20 L27D: W208:

F318 = J022 J222 F090 F022
20 L28A: W204:

F319 = F203 J022 J222 + J022 J212 F121 J225
22 L26C: W210:

F320 = J022 J235 F088 F071
20 L28E: W212:

F321 = J022 J222 F093 F131 J228
20 L28C: W214:

F322 = J222 F090 F025
20 L28D: N244:

(P) F323 = V026 J232 F235 + V035 J211 F122 +
V046 J222 F233 F208
23 L29A: W250: W252:

F324 = V025 J232 F112 F072
21 L30A: W364: W366: W368:

F325 = V026 J232 F112 F073
20 L31A: W264: J906:

(E) F326 = V026 J232 F112 F074 I552
21 L30C: W266: W268: W269

(E) F327 = V026 J232 F130 I552
21 L32A: W360: W361: W362: W363:

F328 = V026 J233 F089 F075
(J) 20 L31B: W260: W262:

F329 = V036 J243 F209
21 L32C: J922: W460: W462: W464:

F331 = F096 F075 J221
21 L33A: K110: K120: W122: W323: I577:

F332 = J235 F234
21 A34C: N212: N232: N244:

(K) F500 = F099 F078 + GND
22 I03C: F502: F503: X501:

(K)

(K) F502 = F500 + F001
28 O15A: X508: X506

(K) F503 = F500 + F002
28 O15C: X510: X514:

(J) G000 = Y000 + T206 T200 + T204 T200
G10 F13:

G001 = Y001 + T206 T201 + T204 T201
G10 F05:

G002 = Y002 + T206 T202 + T204 T202
G10 F14:

G003 = Y003 + T206 T203 + T204 T203
G10 F06:

G004 = Y004 + T207 T200 + T205 T200
G10 F15:

G005 = Y005 + T207 T201 + T205 T201
G10 F07:

G006 = Y006 + T207 T202 + T205 T202
G10 F16:

G007 = Y007 + T207 T203 + T205 T203
G10 F08:

G100 = Y100 + T306 T300 + T304 T300
G10 F01:

(J) G101 = Y101 + T306 T301 + T304 T301
G10 H09:

(J) G102 = Y102 + T306 T302 + T304 T302
G10 F02:

G103 = Y103 + T306 T303 + T304 T303
G10 H10:

G104 = Y104 + T307 T300 + T305 T300
G10 F03:

G105 = Y105 + T307 T301 + T305 T301
G10 H11:

G106 = Y106 + T307 T302 + T305 T302
G10 F04:

G107 = Y107 + T307 T303 + T305 T303
G10 H12:

G200 = Y500 + T500
G11 H13A:

G201 = Y501 + T501
G11 H13C:

G202 = Y502 + T502
G11 H14A:

G203 = Y503 + T503
G11 H14C:

G204 = Y504 + T504
G11 H15A:

G205 = Y505 + T505
G11 H15C:

G206 = Y506 + T506
G11 H16A:

G207 = Y507 + T507
G11 H16C:

H000 = J101 V007 + J100 J101 K905 V903 + X503
J101 X513 V903 + V521 + N000
(J) 44 I01: V000: V010:

(K) H001 = V000 K140 + N001
41 I04: V001:

H002 = V001 + N000
41 I08: V002: V012: V022: V032

(J) H003 = V002 + N001
41 I11: V003: V013: V023:

H004 = V003 + N000
41 I15: V004:

H005 = V004 + N001
41 I16: V005: V015: V025: V035:

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H006 = V005 + N000
41 I22: V006: V016: V026: V036: V046:

H007 = V006 + N001
41 I27: V007: V017:

H201 = K201 V016 I590 X512 + N005
41 J15: V201:

H211 = K211 V016 I590 X512 + N005
41 J17: V211:

(P) H221 = X512 K221 X502 V016 + N005
41 J24: V221:

H231 = X512 F244 K231 X502 V016 + N005
41 J30: V231:

I001 = I577 M500 + W122 M000 + W124 A003
23 H25A: I002:

(D) I002 = Y200 W320 Y800 + W323 I001 + GND
23 H25C: Z000: X700:

I004 = Z000 W327 + X700 W326
22 G26A: L500: O000: T500:

I005 = PBZ1-A (J13-E)
20 H39A: Z000:

I006 = X900 W112 + W110 Z000 + I863
23 E28A: S000:

I011 = I577 M510 + W122 M010 + W124 A013
23 H26A: I012:

(D) I012 = Y210 W320 Y810 + W323 I011 + GND
23 H26C: Z010: X710:

(J) I014 = Z010 W327 + X710 W326
22 G26C: L510: O010: T501:

I015 = PBZ2-A (J13-F)
20 H39B: Z010:

I016 = X910 W112 + W110 Z010 + I863
23 E28C: S010:

I021 = I577 M520 + W122 M020 + W124 A023
23 H27A: I022:

(D) I022 = Y220 W320 Y820 + W323 I021 + GND
23 H27C: Z020: X720:

I024 = Z020 W327 + X720 W326
22 G29A: L520: O020: T502:

I025 = PBZ3-A (J13-H)
20 H39C: Z020:

I026 = X920 W112 + Z020 W110 + I863
23 E31A: S020:

I031 = I577 M530 + W122 M030 + W124 A033
23 H28A: I032:

(D) I032 = Y230 W320 Y830 + W323 I031 + GND
23 H28C: Z030: X730:

I035 = PBZ4-A (J13-J)
20 H39D: Z030:

I034 = Z030 W327 + X730 W326
22 G29C: L530: O030: T503:

I036 = X930 W112 + Z030 W110 + I863 I866
23 E31C: S030:

I041 = I577 M540 + W122 M040 + W124 A043
23 H29A: I042:

(D) I042 = Y240 W320 Y840 + W323 I041 + GND
23 H29C: Z040: X740:

I044 = Z040 W327 + X740 W326
22 G36A: L540: O040: T504:

I045 = PBZ5-A (J13-K)
20 H40A: Z040:

I046 = X940 W112 + W110 Z040 + I863 I868
23 E34A: S040:

I051 = I577 M550 + W122 M050 + W124 A053
23 H30A: I052:

(D) I052 = Y250 W320 Y850 + W323 I051 + GND
23 H30C: Z050: X750:

I054 = Z050 W327 + X750 W326
22 G36C: L550: O050: T505:

I055 = PBZ6-A (J13-L)
20 H40B: Z050:

I056 = X950 W112 + W110 Z050 + I863 K862
23 E34C: S050:

I061 = I577 M560 + W122 M060 + W124 A063
23 H31A: I062:

(J)(D) I062 = Y260 W320 Y860 + W323 I061 + GND
23 H31C: Z060: X760:

(K)(J) I064 = Z060 W327 + X760 W326
22 G39A: T506:

I065 = PBZ7-A (J13-M)
20 H40C: Z060:

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I066 = X960 W112 + W110 Z060 + I863
23 E37A: S060:

I071 = I577 M570 + W122 M070 + W124 A073
23 H32A: I072:

I072 = Y270 W320 Y970 + W323 I071 + GND
23 H32C: Z070: X770:

I074 = Z070 W327 + X770 W326
22 G39C: T507:

I075 = PBZ8-A (J13-N)
20 H40D: Z070:

I076 = X970 W112 + W110 Z070 + I863
23 E37C: S070:

I200 = A131 W252 + X931 W262 + I333 W264
23 B15C: I201:

I201 = PBA4-A (J13-U) I200
20 B14D: A030:

I202 = I332 W264 + X930 W262 + A130 W252
23 B15A: I203:

I203 = I202 J905
20 B14C: A031:

I204 = A121 W252 + X921 W262 + I323 W264
23 B13A: I205:

I205 = PBA3-A (J13-T) I204
20 B14B: A020:

I206 = I322 W264 + X920 W262 + W252 A120
23 B13C: I207:

I207 = I206 J905
20 B14A: A021:

I208 = A111 W252 + X911 W262 + I313 W264
23 B05C: I209:

I209 = PBA2-A (J13-S) I208
20 B04D: A010:

I210 = W264 I312 + W262 X910 + W252 A110
23 B05A: I211:

I211 = I210 J905
20 B04C: A011:

I212 = A101 W252 + X901 W262 + I303 W264
23 B03A: I213:

I213 = PBA1-A (J13-R) I212
20 B04A: A000:

I214 = W264 I302 + W262 X900 + W252 A100
23 B03C: I215:

I215 = I214 J905
20 B04B: A001

I216 = PBA8-A (J13-Y)
20 C40A: A070:

I217 = PBA7-A (J13-X)
20 C40B: A060:

I218 = PBA6-A (J13-W)
20 C40C: A050:

I219 = PBA5-A (J13-V)
20 C40D: A040:

I300 = A000 I361 + PBI1-A (J15-S) I368
22 C04A: X000: X100: X200:

I301 = A001 I361 + I364
22 C04C: X001: X101: X201:

I302 = I355 X001 + I357 X101 + I359 X201
13 C14: I214: I303: P101: X881: X981:

I303 = I593 X980 + I302 I592
12 C15: I212: P100: S100: X880: X980:
J 13-A:

I310 = A010 I361 + PBI2-A (J15-T) I368
22 C05A: X010: X110: X210

I311 = A011 I361 + I364
22 C05C: X011: X111: X211:

I312 = I355 X011 + I357 X111 + I359 X211
13 D40: I210: I313: P111: X891: X991

I313 = I593 X990 + I312 I592
12 E40: I208: P110: S110: X890: X990:
J13-B:

I320 = A020 I361 + PBI3-A (J15-U) I368
22 C09A: X020: X120: X220:

I321 = A021 I361 + I364
22 C09C: X021: X121: X221:

I322 = I355 X021 + I357 X121 + I359 X221
23 C16A: I206: I323: P121:

I323 = I322
21 C17A: I204: P120: S120: J13-C:

I330 = A030 I361 + PBI4-A (J15-V) I368
22 C10A: X030: X130: X230:

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I331 = A031 I361 + I364
22  C10C:  X031:  X131:  X231:

I332 = I355 X031 + I357 X131 + I359 X231
23  C16C:  I202:  I333:  P131:

I333 = I332
21  C17C:  I200:  P130:  S130:  J13-D:

I354 = F110 F101 F210 I592 I362 + I365
22  C21A:  I355:  W364:

I355 = I354
21  C23A:  I302:  I312:  I322:  I332:  J14-S:

I356 = F111 F100 F210 I592 I362 + I360
22  C21C:  I357:  W366:

I357 = I356
21  C23C:  I302:  I312:  I322:  I332:  J14-R:

I358 = F111 F101 I362 + I366
22  C22A:  I359:  W368:

I359 = I358 I592 F210
21  B28C:  I302:  I312:  I322:  I332:  J14-P:

I360 = PBIS2-A (J15-X)
20  C33D:  I362:  I356:

(J) I361 = I363 + J012
12  C06:  I300:  I301:  I310:  I311:  I320:
                         I321:  I330:  I331:
I362 = I365 + I360 + I366
13  C08:  I363:  I368:  I354:  I356:  I358:

I363 = I362
20  B11A:  I369:  I361:

I364 = I367
21  C07C:  I301:  I311:  I321:  I331:

I365 = PBIS1-A (J15-Y)
20  D39A:  I362:  I354:

I366 = PBIS3-A (J15-W)
20  D39B:  I362:  I358:

I367 = PBIC-A (J15-R) I368
20  D39C:  I364:

I368 = I362 Y902
21  F33C:  I300:  I330:  I310:  I367:  I320:


I369 = I363 Y903
21  C07A:  W364:  W366:  W368:

I400 = A170 A160 A150 A140
20  A40D:  I402:

I401 = A130 A120 A110 A100
20  A36D:  I402:

I402 = I400 + I401
22  A39C:  I403:  K441:

I403 = I402
21  B28A:  F239:  K210:  K420:

(K) I404 = 0011 I411 + Z07I I414
22  I33A:  I405:

I405 = I404
20  I34A:  L070:  L570:

(K) I406 = 0001 I411 + Z06I I414
22  I33C:  I407:

I407 = I406
20  I34B:  L060:  L560:

I408 = K323
21  I32C:  I410:  I411:  I412:  I413:

(J) I409 = K321
21  I35A:  I412:  I413:  I414:

I410 = I408
21  I35C:  I594:  L080:  L090:  L100:  L110:

I411 = I408
20  I34C:  I404:  I406:

I412 = I408 I409
21  I36A:  L020:  L030:  L040:  L050:

I413 = I408 I409
20  I34D:  L000:  L001:

I414 = I409
20  K35D:  I404:  I406:

I500 = X902
11  N06:  X910:  X911:  X920:  X921:  X930:
                                       X931:

I501 = X903 X913 X933 X923
20  N12A:  W027:  W030:

I503 = X922
20  N12B:  X930:  X931:

I504 = X943 X953 X973 X963
20  N12C:  W027:

I505 = X962
20  N12D:  X970:  X971:

I510 = X900 X801 + X800 X901 + X811 X910 + X911
                   X810 + X920 X821 + X820 X921
16  N30:  I517:
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I512 = X930 X831 + X931 X830 + X841 X940 + X941
X840 + X851 X950 + X850 X951
16 N31: I517:

Ⓙ I514 = X960 X861 + X961 X860 + X871 X970 + X971
16 N32: I517 X870 + X881 X980 + X880 X981

I516 = X891 X990 + X991 X890 + GND
23 O23C: I517:

Ⓕ I517 = I510 I512 I514 I516
20 N29B: I519: X502

I519 = I517
20 N29C: I579: K856:

I531 = X952
21 N20A: X960: X961: X970: X971:

I532 = X912
21 N04C: X920: X921: X930: X931:

I535 = X942
11 N16: X950: X951: X960: X961: X970:
X971:

I538 = X982
20 N29A: X990: X991:

Ⓚ I550 = F093: J243
20 B11C: X502

I551 = X508 X510
21 O40C: I552: I577: X502: X512: X516:

Ⓔ I552 = I551
21 O16A: F210: F326: F327: X517

I553 = X505
21 O40A: J200: J210: J220: I230: K241:

I554 = X504
11 O04: I573: I581: W110: W325: X500:
V012: W327: X515:

Ⓔ I555 = X518 X501 X507 X509 + K421 I588
22 O21C: I556:

I556 = I555
21 O18C: I581: L513:

I558 = I559 I566
20 O19B: L512:

I559 = X511 X501 X518 X507
20 O17A: I558: I560:

I560 = I559
11 O38: L500: L510: L520: L530: L540:
L550: L560: L570:

I561 = I566 I594
11 O39: L500: L510: L520: L530: L540:
L550: L560: L570:

I562 = I594
21 018A: L580: L590: L600: L610:

Ⓔ I566 = K321 I588
20 017B: I561: I558:

I570 = X509 M513 X507
20 O17D: I571:

I571 = I570
11 O35: X700: X710: X720: X730: X740:
X750: X760: X770:

I573 = X511 V022 J031 I554
20 O19A: I574:

I574 = I573
11 O36: X700: X710: X720: X730: X740:
X750: X760: X770:

I577 = I551 + F308 F331
12 O20: I001: I011: I021: I031: I041:
I051: I061: I071:

I579 = V902 I589 I599 + V036 F076 F112 J233 +
V036 I519 I589
Ⓕ 23 O23A: I580: I578

Ⓟ Ⓚ I580 = J900 I579
21 O24A: X503: X509: X511:

I581 = I556 + X511 V010 I554 J031
22 021A: I582:

I582 = I581
11 O37: X701: X711: X721: X731: X741:
X751: X761: X771:

I584 = M513
20 O25A: I585: I587:

I585 = I584
20 025B: J402:

I586 = M512
20 O25C: I587:

I587 = I584 I586
21 O14C: I595: X518: X501:

Ⓔ I588 = X517
11 O12: I566: J400: J402: J404: L514:
F210: I555: I594:

Ⓕ I578 = I579
20 B11O : X520

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(E) (J) I589 = X508: X510
21 O16C: I579: I579: K856: F208

I590 = X503
21 O14A: F300: J101: J101: H201: H211:

I592 = X505
21 O05A: I303: I313: I354: I356: I359:

I593 = X504
11 O06: I303: I313: I854: W058: W376:
X506: X507: W028:

I594 = I410 I588
20 O17C: I561: I562:

I595 = I587
20 O19D: X519:

(G) I598 = M514
20 O25D: I599: X517

I599 = I598
21 O24C: I579: K856:

I850 = M850
20 D32A: K851:

I851 = Y850 K851 + K850
22 D26A: K852:

I852 = K854 K858 K860 K862
11 C37: I853: I860: I861: I862: I871:
K864: W800: W110:

(J) I853 = J233 I852
20 C35B: F302:

(N) I854 = K865 + J230 + I593 + GRD
24 D34A: I856:

(N) I855 = K441 + J918 + J913 + F271
24 D34C: I856:

(N) I856 = I854 I855
20 D32B: I857:

(J) I857 = I856
21 D33A: K854: K858: K860: K862:

I858 = V036 J233
20 D32C: I859:

I859 = J930 I858
21 D33C: K855: K859: K861: K863:

I860 = I852 J008 V001 + V001 F271 J008 F101
22 C22C: J909: J910:

I861 = I852 J001 V006
20 C35A: W054:

I862 = I852
20 D32D: I863:

I863 = I862
11 C36: I006: I016: I026: I036: I046:
I056: I066: I076:

I865 = K854 K860
20 C35C: P232: I866:

I866 = I865
20 C35D: I036:

I867 = K858 K860
20 C39A: I868: P242:

I868 = I867
20 C39B: I046:

I871 = V003 J008 I852
20 C39C: I872:

I872 = I871
21 C34C: P232: P242: P252: F301:

(N) (J) I873 = K855 + K859
22 D26C: K862:

I874 = J930
20 C39D: K857:

J000 = K002 K012
21 J07A: J001: V015: J002:

J001 = J000
11 J08: F300: F301: K100: W023: W800:
F302 I861:

J002 = J000
21 J07C: K854: K858: K860: K862: W376:

J003 = K003 K012
21 J09A: J004: V012: V013:

J004 = J003
21 J10A: F311: F313: K130: K241: K856:

J006 = K003 K013
21 J09C: J007: J008: V025: J011: J010:

J007 = J006
11 J11: F300: J101: J101: X500: X500:
X503: X508: X510:

(J) J008 = J006
11 J12: I860: I860: I871: K865:
N212: N244: W810:

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J009 = J011
21 J13A: V016: V017: V026: V036: V046:

J010 = J006
20 L31D: N232: X514:

J020 = K001 K011
20 J05A: J021: J022:

J021 = J020
21 J06A: F315: F315: F316: F317: K120:

J022 = J020
21 J06C: F318: F319: F319: F320: F321:

J011 = J006
20 K28B: J009: J012:

J012 = J011
20 D39D: V035: I361:

J100 = K900 K902
20 M26A: H000: K905:

J101 = K902 K900 I590 J007 + J007 J102 I590
22 M27A: H000: H000: J103: H000

J102 = K420 K320 K322
20 M26B: J101: J104

(K) J103 = X501 + J101
28 015B X512:

J106 = J912 F112 F078 F068 + F099 F076 J912 + J913 K443
(K) 23 M28A: J107:

J107 = J106 K140 F213 J110
20 M26C: K901:

J109 = Sense Terminal 4 + GND
(K) 28 021B J110:

J110 = J109
20 J05C: J111: J107:

J111 = J110 Y901
(J) 20 J400: K140:

J030 = K001 K010
20 J05B: J031:

J031 = J030
21 J10C: K110: : W102: I573: I581:

(K) J200 = K201 J917 I553
21 J13C: F206: F216: F222:

(K) J210 = K211 J917 I553
21 J20C: J211: J212: J446:

J104 = J102
20 N 29D : K902

J211 = J210
11 J21: F205: F215: F221: F304: F305: F306: F323: K320:

J212 = J210
21 J22A: F308: F315: F317: F319:

J220 = K221 J917 I553
21 J22C: J221: J222: J223: J243:

J221 = J220
11 J26: F200: F200: F305: F313: F331: K320: K420: K421:

J222 = J220
11 J27: F315: F316: F318: F319: F321: F322: K322: F323:

(J) J223 = J220
21 J39A: F205: F215: F221: F253: F304:

J224 = K222
20 J05D: F305: K441:

J225 = K222
21 J37A: F303: F306: F308: F319: K322:

J226 = K222
21 J37C: F200: F204: F207: F317: K320:

J227 = K223
21 J38A: F212: F223: F227: F239:

J228 = K223
21 J38C: F202: F239: F313: F315: F321:

J230 = K231 J917 I553
21 J28C: I854: J231: J232: J233:

J231 = J230
21 J32A: F300: F301: F310: F311: K440:

(J) J232 = J230
11 J33: F323: F324: F325: F326: F327: X500:

J233 = J230
11 J34: F328: I579: K420: K440: I853: I858:

J234 = K231 J917 X504 + GND
22 J31C: F206: F216: F222: J235:

(K) J235 = J234
21 J32C: F320: F332: K420:

(K) J243 = J220
21 J39C: F308: F329: I550

(E) J400 = I553 M514 + M424
22 M15A: J401:

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J401 = J400
20 M14B: J444: K442:

(E) J402 = I585 I588 + M420
22 M15C: J403:

J403 = J402
20 M14C: J444:

(E) J404 = I588 M512 + M330
22 M16A: J405:

J405 = J404
20 M14D: J444:

J441 = K440
20 O19C: F239: K210:

J444 = J401 + J403 + J405
23 M06C: J445: K524:

J445 = K322 K320 K420 + J444
22 M16C: K522:

J446 = J210 J912
20 M14A: K421:

J560 = K140
21 O05C: K101: K111: K121: K131:

J562 = K101
21 F27A: T001: T002: T003: T004: T005:

J563 = K101
21 F27C: T000: T102: T103: T104· T105:

J565 = K131
21 F33A: T503: T504: T505: T506: T507

J900 = M904
21 M30A: I580: J901: J902: J903: J904:

(K) J901 = J900
21 M30C: J905: J907: J908: K321: K421:
x507

J902 = J900
21 M31A: K141: K323: K441: K865: L323:

J903 = J900
21 M31C: K201: K211: K221: K230: K853:

J904 = J900
21 L37A: K001: K011: K223: L515: X513:

(J) J905 = J901 + M905 + V025 M908
13 M40: I203: I207: J906: I211: I215:

J906 = J905 F325
21 L37C: A041: A051: A061: A071:

J907 = J901 + M906
22 M27C: W100:

J908 = J901 + M907
22 L35A: J909: J910: J922:

(J) J909 = J908 I860
11 L36: P001: P011: P021: P031: P041:
P051: P061: P071:

J910 = J908 I860
21 L07C: P101: P111: P121: P131:

J912 = M903
11 K39: F219: F221: F242: F307: J106:
J106: J446: J913:

J913 = J912
11 K40: F308: I855: J106: J923: K420:
K440: L331:

J914 = M908
21 I36C: J918: W124: W323:

I915 = M909
20 L38D: F206: J918:

J917 = J918
21 L34C: J200: J210: J220: J230: J234:

J918 = J914 J915
21 L34A: J917: J921: I855:

J921 = J918 + GND
22 L35C: F216: F222: F238: W130:

J922 = J908 F280 F329
20 L38B: K240:

J923 = J913
20 L38C: F244: W130:

J930 = M904
20 M26D: I859: I874:

K000 = K012 V005 + GND
32 J01A: K003:

K001 = J904 + V005 K013
32 J01C: J020: K002: J030:

K002 = V000 K001
31 J02A: J000:

K003 = V000 K000
31 J02C: J003: J006: K010: K011: K111:

K010 = K012 K003 V005 + GND
32 J03A: K013: J030:

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(J) K011 = J904 + V005 K003 K013
32 J03C: J020: K012:

K012 = V000 K011
31 J04A: J000: J003: K000: K010: K111:

K013 = V000 K010
31 J04C: J006: K001: K011:

K100 = V006 J001 K140 + GND
32 F28A: T100: T101:

(J) K101 = V036 + J560
32 F28C: J562: J563:

(J) K110 = V010 F331 J031 + GND
32 F35A: T206: T207: T306: T307:

K111 = V005 K003 K012 + J560
32 F35C:

K120 = V010 F331 J021 + GND
32 F36A: T204: T205: T304: T305:

K121 = V017 + J560
32 F36C:

K130 = J004 V006 + GND
32 F34A: T500: T501: T502:

K131 = V017 + J560
32 F34C: J565:

(K) K140 = V000 V003 V006 + J111
32 J35A: J107: K100: J560: H001

K141 = J902 + GND
32 J35C: J12-Z:

K200 = V231 F226 + GND
32 J14A:

K201 = V201 + J903
32 J14C: H201: J200: J14-D:

K210 = V201 + V231 F214 + V221 F121
33 J18A: I 403 J441

K211 = V211 + J903 + GND
33 J18C: H211: J210: J14-C:

K220 = F242 V231 + V211
32 J23A:

(J) K221 = J903 + F243 V221
32 J23C: H221: J220: J14-B:

K222 = V221 F236 K224 + GND
32 J36A: J225: J226: K225: J224:

K223 = J904 + V221 F239 K225 (M)
32 J36C: J227: J228: K224:

K224 = V002 K223
30 M24C: F243: K222:

K225 = K222 V026 (M)
30 M24D: K223

K230 = V221 F239 F243 + J903
32 J29A:

K231 = GND + V231 F213
32 J29C: H231: J230: J234: J14-A:

K240 = J922
30 M19A: F300:

K241 = V003 J004 I553
30 M19B: K440:

K320 = J221 V016 F114 F074 K441 + K441 J211 V016 F098 F073 J226
32 M10A: J102: J445:

K321 = J901 + V521
32 M10C: I409: I566: L321: J12-W:

K322 = J222 V025 J225 F125 + GND
32 M11A: J102: J445:

K323 = J902 + V521
32 M11C: I408: L322: L514: J12-Y

(J) K420 = V025 J913 J235 + J233 V016 F114 F075 K441 + K441 J221 F114 F072 V016 I403
33 M09A: J102: J445

K421 = J901 + J221 V013 F114 F075 + J446 V013
33 M09C: I555: L421: J12-X:

K440 = K241 J913 + J231 V026 F123 + J233 F114 F059 V026 + K441
24 L13C: K441: J441:

K441 = K440 + V521 F059 F099 + F123 I402 V036 J224 J243 + K443 V046 + J902 (5)
15 M20: I855: K320: K320: K420: K420: K440: L330:

K442 = V902 J401 K523
30 M19C:

(J) K443 = V221
30 M19D: J106: K441:

K522 = K812 K802 K801 J445 K525
30 M18A: V521:

K523 = K801 K802 K811
30 M18B: K442:

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K524 = J444 V902
30 M18C:

K525 = V521
30 M18D: K522:

K800 = K803 N800
(H) 31 M01A: K803: X501

K801 = K803 N800
31 M01C: K522: K523: K802: V521: V903:

K802 = N801 K801
31 M02A: K522: K523: K800: V901: V902:

K803 = N801 K800
(H) 31 M02C: K801: K810: K811: X501

K810 = K803 N800 K812
31 M03A: K813: V521: V902: V903: X512:

K811 = K803 N800 K813
31 M03C: K523: K812: V901:

K812 = N801 K811
31 M04A: K522: K810: V521: V903:

(H) K813 = N801 K810
31 M04C: K811: V901: V902: X512: X501

K850 = M850
30 D24A: I851:

K851 = I850
30 D24B: I851:

K852 = Y851 I851 + GND
32 D27A:

K853 = J903 + K855 V013
32 D27C: K854:

(N) K854 = V001 K853 I857 J002
31 D28A: I852: I865: K858: K860

(N) K855 = I859
31 D28C: K853: I873

K856 = J004 V006 I519 X505 + I599 I589
32 D29A:

K857 = I874 + V013 K859
32 D29C: K858:

K858 = K854 K857 I857 V002 J002
31 D30A: I852: I867: K860:

(N) K859 = I859
31 D30C: K857: I873

(N) K860 = K858 M851 I857 V003 J002 K854
31 D31A: I852: I865: I867: K862:

K861 = I859
31 D31C:

(N) K862 = K860 M852 I857 V004 J002 I873
30 D24C: I056: I852:

K863 = I859
30 D24D: P252:

(L) K864 = V007 I852 + F125
32 C38A:

K865 = J902 + F271 V022 J008
32 C38C: I854:

K900 = V902 M900 K905 + GND
32 M23A: J100: J101: I361:

K901 = K905 V901 + J107 V046
(J) 32 M23C: K904: J12-a:

(J) K902 = V902 M901 K905 J104
30 M24A: J100: J101:

K903 = V002
30 M24B: K904:

K904 = M902 + K901 K903
32 M24A:

(J) K905 = J100 V001 + GND
32 M25C: H000: K900: K901: K902:

L000 - I413 Z001
69 I37A: J02-A:

L010 = I413 Z011
69 I37B: J02-B:

L020 - I412 Z021
69 I37C: J02-C:

L030 = I412 Z031
69 I38A: J02-D

L040 = I412 Z041
69 I38B: J02-E:

L050 = I412 Z051
69 I38C: J02-F:

L060 = I407
69 I39A: J02-H:

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L070 = I405
69 I39B: J02-J:

L080 = C021 I410
69 I39C: J02-K:

L090 = C031 I410
69 I40A: J02-L:

L100 = C041 I410
69 I40B: J02-M:

L110 = C051 I410
69 I40C: J02-N:

L321 = K321
69 M13B: J02-R:

(E) L322 = K323
69 M12A: J02-T: M322:

L323 = J902
69 M12E: J02-U:

L330 = K441
69 M12C: J01-Y:

(K) L331 = J913
69 M13A: J01-Z: J03-Z

L421 = K421
69 M13C: J01-S:

L500 = X701 I560 + I561 I004
67 M35A: J04-A:

L510 = X711 I560 + I561 I014
67 M35B: J04-B:

L512 = I558
69 C27A: J04-R:

L513 = I556
69 C27B: J03-S:

(E) L514 = I585 K323
69 C27C: J04-T:

L515 = J904
69 M39E: J04-U:

L520 = X721 I560 + I561 I024
67 M35C: J04-C:

L530 = X731 I560 + I561 I034
67 M36A: J04-D:

L540 = X741 I560 + I561 I044
67 M36B: J04-E:

L550 = X751 I560 + I561 I054
67 M36C: J04-F:

L560 = X761 I560 + I561 I407
67 M37A: J04-H:

L570 = X771 I560 + I561 I405
67 M37B: J04-J:

L580 = I562 C021
69 M38A: J04-K:

L590 = I562 C031
69 M38B: J04-L:

L600 = I562 C041
69 M38C: J04-M:

L610 = I562 C051
69 M39A: J04-N:

M000 = J01-A
68 H33A: I001:

M010 = J01-B
68 H33B: I011:

M020 = J01-C
68 H33C: I021:

M030 = J01-D
68 H34A: I031:

M040 = J01-E
68 H34B: I041:

(J) M050 = J01-F
68 H34C: I051:

M060 = J01-H
68 H35A: I061:

M070 = J01-J
68 H35B: I071:

(F) M330 = J02-S
68 M17A: J404: X520

M420 = J01-R
68 M17B: J402:

M424 = J01-V
68 M17C: J400:

M500 = J03-A
68 M32A: I001: X700:

M510 = J03-B
68 M32B: I011: X710:

(F) (E) M322 = L322
68 H35C: X517: X520

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M512 = J04-S
68 O26A: I586: J404:

M513 = J03-R
68 C26B: I570: I584:

M514 = J03-V
68 O26C: I598: J400:

(J) M520 = J03-C
68 M32C: I021: X720:

M530 = J03-D
68 M33A: I031: X730:

M540 = J03-E
68 M33B: I041: X740:

M550 = J03-F
68 M33C: I051: X750:

M560 = J03-H
68 M34A: I061: X760:

M570 = J03-J
68 M34B: I071: X770:

M850 = PBMI-A (J14-N)
68 D23A: I850: K850:

M851 = J02Y J04Y
68 D23B: K860:

M852 = J02Z J04Z
68 D23C: K862:

M900 = J14-H
68 M22A: K900:

M901 = J14-E
68 M22B: K902:

M902 = J14-F
68 M22C: K904:

M903 = J14-K
68 M34C: J912:

(P) M904 = J14-J
87 M29A: J900: J930:

(P) M905 = J12-Z
87 M29B: J905:

(P) M906 = J13-P
87 M29C: J907:

M907 = J15-P
68 L39A: J908:

M908 = J14-M
68 L39B: J914: J905:

M909 = J14-L
68 L39C: J915:

N000 = C000
21 I07A: H000: H002: H004: H006:

(J) N001 = C001
21 I07C: H001: H003: H005: H007: V012:

N005 = C005
21 J20A: H201: H211: H221: H223:

N210 = N212
11 B40: A101: A111: A121: A131: A141:
A151: A161: A171:

N212 = J008 V001 F332
20 A40A: N210:

N230 = N232
11 B29: A100: A110: A120: A130: A140:
A150: A160: A170:

N232 = F332 V003 J010
20 A40B: N230:

N240 = N244
11 B34: A140: A141: A150: A151: A160:
A161: A170: A171:

N241 = N244
11 B35: A100: A101: A110: A111: A120:
A121: A130: A131:

N244 = J008 V004 F332 F322
20 A40C: N240: N241:

N800 = C002
21 M05A: K800: K801: K810: K811:

N801 = C003
21 M05C: K802: K803: K812: K813:

(J) O000 = I004 W164
30 H36A:

O001 = W164 Z000
30 H36B: I406:

O010 = I014 W164
30 H36C:

O011 = W164 Z010
30 H36D: I404:

O020 = I024 W162
30 H37A:

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O021 = W162 Z020
30 H37B: L080: L580:

O030 = I034 W162
30 H37C:

(J) O031 = W162 Z030
30 H37D: L090: L590:

O040 = I044 W162
30 H38A:

O041 = W162 Z040
30 H38B: L100: L600:

O050 = I054 W162
30 H38C:

O051 = W162 Z050
30 H38D: L110: L610:

P000 = P203 + P002 W000 + A101 W460
33 D02A: P003: P201: P204:

P001 = A100 W460 + W000 P003 + J909
33 D02C: P002: S000: J10-B:

P002 = P001 W070
30 D03A: P000: P004:

P003 = P000 W070
30 D03B: P001: P025:

P004 = P002
11 D10: P010: P011: P020: P021: P030: P031:

P010 = P213 + P012 W000 P004 + A111 W460
33 D04A: P013: P211: P214:

P011 = A110 W460 + P004 W000 P013 + J909
33 D04C: P012: S010: J10-E:

P012 = P011 W070
30 D03C: P010: P014:

P013 = P010 W070
30 D03D: P011: P025:

P014 = P012
21 D11A: P020: P021: P030: P031:

P020 = P223 + P022 P014 W000 P004 + A121 W460
33 D07A: P023: P221: P224:

P021 = W460 A120 + P004 W000 P014 P023 + J909
33 D07C: P022: S020: J10-J:

P022 = P021 W070
30 D08A: P020: P024:

P023 = P020 W070
30 D08B: P021: P025:

P024 = P022
20 D12A: P030: P031:

P025 = P003 P023 P033 P013
20 D12B: W003: W005:

P030 = P233 + P014 P004 W000 P024 P032 + A131 W460
33 D09A: P033: P231: P234:

P031 = A130 W460 + P014 P004 P033 W000 P024 + J 909
33 D09C: P032: S030: J10-M:

P032 = P031 W070
30 D08C: P030:

P033 = P030 W070
30 D08D: P025: P031:

P040 = P243 + P042 W003 + A141 W462
33 D15A: P043: P241: P244:

P041 = A140 W462 + W003 P043 + J909
33 D15C: P042: S040: J11-B:

P042 = P041 W072
30 D16A: P040: P044:

P043 = P040 W072
30 D16B: P041: P055:

P044 = P042
11 D13: P050: P051: P060: P061: P070: P071:

P050 = P253 + P052 P044 W003 + A151 W462
33 D17A: P053: P251: P254:

P051 = A150 W462 + W003 P044 P053 + J909
33 D17C: P052: S050: J11-E:

P052 = P051 W072
30 D16C: P050: P054:

P053 = P050 W072
30 D16D: P051: P055:

P054 = P052
21 D11C: P060: P061: P070: P071:

P055 = P063 P073 P043 P053
20 D12C: W005:

P060 = P263 + P062 P044 W003 P054 + A161 W462
33 D20A: P063: P261: P264:

P061 = A160 W462 + P054 P044 W003 P063 + J909
33 D20C: P062: S060: J11-J:

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P062 = P061 W072
30  D21A:  P060:  P064:

P063 = P060 W072
30  D21B:  P055:  P061:

P064 = P062
20  D12D:  P070:  P071:

P070 = P273 + P054 P072 P044 W003 P064 + A171
                                          W462
33  D22A:  P073:  P271: P274:

P071 = A170 W462 + P064 W003 P044 P073 P054 +
                                          J 909
33  D22C:  P072:  S070: J11-M:

P072 = P071 W072
30  D21C:  P070:

P073 = P070 W072
30  D21D:  P055:  P071:

P100 = P283 + P102 W005 + W464 I303
33  C24A:  P103:  P281:  P284:

P101 = W464 I302 + W005 P103 + J910
33  C24C:  P102:  S100:  J11-R:

P102 = W073 P101
30  C25A:  P100:  P104:

P103 = W073 P100
30  C25B:  P101:  P125:

P104 = P102
21  C34A:  P110:  P111:  P120:   P121:

P110 = P293 + P112 W005 P104 + W464 I313
33  C26A:  P113:  P291:  P294:

P111 = W464 I312 + P104 W005 P113 + J910
33  C26C:  P112:  S110:  J11-U:

P112 = P111 W073
30  C25C:  P110:  P114:

P113 = P110 W073
30  C25D:  P111:  P125:

P114 = P112
20  C33A:  P120:  P121:

P120 = P303 + P122 P104 W005 P114 + W464 I323
33  C30A:  P123:  P301:  P304:

P121 = W464 I322 + P114 W005 P104 P123 + J910
33  C30C:  P122:  S120:  J11-W:

P122 = P121 W073
30  C31A:  P120:
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P123 = P120 W073
30 C31B: P121: P125:

P124 = P125
20 C33B: P130: P131:

P125 = P103 P123 P113
20 C33C: P124:

J P130 = P313 + P132 W005 P124 + W464 I333
33 C32A: P133: P311: P314:

P131 = W464 I332 + P124 W005 P133 + J910
33 C32C: P132: S130: J11-X:

P132 = P131 W073
30 C31C: P130:

P133 = P130 W073
30 C31D: P131:

P200 = W801 P204
30 E02A:

P201 = P000 W801
30 E02B: P202:

P202 = P201 W811
20 E10A: P203:

P203 = PBP1-A (J15-A) P202
20 E10B: P000:

P204 = P000
20 E04A: P200:

P 210 = W801 P214
30 E02C

P211 = P010 W801
30 E02D: P212:

P212 = P211 W811
20 E10C: P213:

J P213 = PBP2-A (J15-B) P212
20 E10D: P010:

P 214 = P010
20 E04B: P210:

P220 = W801 P224
30 E03A:

P221 = P020 W801
30 E03B: P222:

P222 = P221 W811
20 E11A: P223:

P223 = PBP3-A (J15-C) P222
20 E11B: P020:

P224 = P020
20 E04C: P220:

P230 = W801 P234
30 E03C:

P231 = P030 W801
30 E03D: P232:

P232 = P231 W811 + I865 I872
22 E12A: P233:

P 233 = PBP4-A (J15-D) P232
20 E11C: P030:

P 234 = P030
20 E04D: P2 30:

P240 = W803 P244
30 E064:

P241 = P040 W803
30 E06B: P242:

P242 = P241 W811 + I867 I872
22 E12C: P243:

P243 = PBP5-A (J15-E) P242
20 E11D: P040:

P244 = P040
20 E08A: P240:

P250 = W803 P254
30 E06C:

P251 = P050 W803
30 E06D: P252:

P252 = P251 W811 + K863 I872
22 E13A: P253:

P253 = PBP6-A (J15-F) P252
20 E14A: P050:

P254 = P050
20 E08B: P250:

P260 = W803 P264
30 E07A:

P261 = P060 W803
30 E07B: P262:

P262 = P261 W811
20 E14B: P263:

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P263 = PBP7-A (J15-H) P262
20  E14C:  P060:

P264 = P060
20  E08C:  P260:

P270 = W803 P274
30  E07C:

P271 = P070 W803
30  E07D:  P272:

P272 = P271 W811
20  E14D:  P273:

P273 = PBP8-A (J15-J) P272
20  E15A:  P070:

P274 = P070
20  E08D:  P270:

P280 = W805 P284
30  E18A:

P281 = P100 W805
30  E18B:  P282:

P282 = P281 W813
20  E21A:  P283:

P283 = PBP9-A (J15-K) P282
20  E21B:  P100:

P284 = P100
20  E20A:  P280:

P290 = W805 P294
30  E18C:

P291 = P110 W805
30  E18D:  P292:

P292 = P291 W813
20  E21C:  P293:

P293 = PBP10-A (J15-L) P292
20  E21D:  P110:

P294 = P110
20  E20B:  P290:

P300 = W805 P304
30  E19A:

P301 = P120 W805
30  E19B:  P302:

P302 = P301 W813
20  E22A:  P303:

(J) P303 = PBP11-A (J15-M) P302
20  E22B:  P120:

P304 = P120
20  E20C:  P300:

P310 = W805 P314
30  E19C:

P311 = P130 W805
30  E19D:  P312:

P312 = P311 W813
20  E22C:  P313:

P313 = PBP12-A (J15-N) P312
20  E22D:  P130:

P314 = P130
20  E20D:  P310:

Q000 = A000 W210 + A070 W212
22  A12A:  E000:  U000:

Q010 = W214 + A010 W210 + A000 W212
23  A13A:  E010:  U010:

Q020 = W214 + A020 W210 + A010 W212
23  A13C:  E020:  U020:

Q030 = W214 + A030 W210 + A020 W212
23  A14A:  E030:  U030:

Q040 = W214 + A040 W210 + A030 W212
23  A14C:  E040:  U040:

Q050 = W214 + A050 W210 + A040 W212
23  A15A:  E050:  U050:

Q060 = W214 + A060 W210 + A050 W212
23  A15C:  E060:  U060:

Q070 = W214 + A070 W210 + A060 W212
23  A16A:  E070:  U070:

R000 = W204 A000 + W200 Z001 + W202 Z000 + GND
24  A04A:  E000:  U000:

R010 = W204 A010 + W200 Z011 + W202 Z010 + W208
24  A04C:  E010:  U010:

R020 = W204 A020 + W200 Z021 + W202 Z020 + W208
24  A05A:  E020:  U020:

R030 = W204 A030 + W200 Z031 + W202 Z030 + W208
24  A05C:  E030:  U030:

R040 = W204 A042 + W200 Z041 + W202 Z040 + W208
24  A06A:  E040:  U040:
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R050 = W204 A052 + W200 Z051 + W202 Z050 + W208
24  A06C:  E050:  U050:

R060 = W204 A062 + W200 Z061 + W202 Z060 + W208
24  A07A:  E060:  U060:

R070 = W204 A072 + W200 Z071 + W202 Z070 + W208
24  A07C:  E070:  U070:

S000 = W052 P001 + W054 I006 + A003 W056
33  E27A:  T101:

S001 = W021 + GND + GND
33  E27C:  T100:

S010 = W052 P011 + W054 I016 + A013 W056
33  E29A:  T103:

S011 = W021 + GND + GND
33  E29C:  T102:

S020 = W052 P021 + W054 I026 + A023 W056
33  E30A:  T105:

S021 = W021 + GND + GND
33  E30C:  T104:

S030 = W052 P031 + W054 I036 + A033 W056
33  E32A:  T001:

S031 = W021 + GND + GND
33  E32C:  T000:

S040 = W052 P041 + W054 I046 + A043 W056
33  E33A:  T003:

S041 = W021 + GND + GND
33  E33C:  T002:

S050 = W052 P051 + W054 I056 + A053 W056
33  E35A:  T005:

S051 = W021 + GND + GND
33  E35C:  T004:

S060 = W052 P061 + W054 I066 + A063 W056
33  E36A:  T301:  T303:

S061 = W021 + GND + GND
33  E36C:  T300:  T302:

S070 = W052 P071 + W054 I076 + A073 W056
33  E38A:  T302:  T303:

S071 = W021 + GND + GND
33  E38C:  T300:  T301:

S100 = W050 P101 + I303 W051
32  F37A:  T201:  T203:

S101 = W020 + GND
32  F37C:  T200:  T202:

S110 = W050 P111 + I313 W051
32  F38A:  T202:  T203:

S111 = W020 + GND
32  F38C:  T200:  T201:

S120 = W050 P121 + I323 W051
32  E39A:  T305:  T307:

S121 = W020 + GND
32  F39C:  T304:  T306:

S130 = W050 P131 + I333 W051
32  F40A:  T204:  T207:

S131 = W020 + GND
32  F40C:  T205:  T206:

T000 = J563 + S031
53  F24A:  D000:  D002:  D004:  D006:

T001 = J562 + S030
53  F24C:  D001:  D003:  D005:  D007:

T002 = J562 + S041
53  F25A:  D000:  D001:  D004:  D005:

T003 = J562 + S040
53  F25C:  D002:  D003:  D006:  D007:

T004 = J562 + S051
53  F26A:  D000:  D001:  D002:  D003:

T005 = J562 + S050
53  F26C:  D004:  D005:  D006:  D007:

T100 = K100 + S001
53  F21A:  D100:  D102:  D104:  D106:

T101 = K100 + S000
53  F21C:  D101:  D103:  D105:  D107:

T102 = J563 + S011
53  F22A:  D100:  D101:  D104:  D105:

T103 = J563 + S010
53  F22C:  D102:  D103:  D106:  D107:

T104 = J563 + S021
53  F23A:  D100:  D101:  D102:  D103:

T105 = J563 + S020
53  F23C:  D104:  D105:  D106:  D107:

T200 = S101 + S111
53  F17A:  G000:  G000:  G004:  G004:
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T201 = S100 + S111
53 F17C: G001: G001: G005: G005:

T202 = S101 + S110
53 F18A: G002: G002: G006: G006:

T203 = S100 + S110
53 F18C: G003: G003: G007: G007:

T204 = K120 + S131
53 F19A: G000: G001: G002: G003:

J T205 = K120 + S130
53 F19C: G004: G005: G006: G007:

T206 = K110 + S131
53 F20A: G000: G001: G002: G003:

T207 = K110 + S130
53 F20C: G004: G005: G006: G007:

T300 = S071 + S061
53 G21A: G100: G100: G104: G104:

T301 = S071 + S060
53 G21C: G101: G101: G105: G105:

T302 = S070 + S061
53 G22A: G102: G102: G106: G106:

T303 = S070 + S060
53 G22C: G103: G103: G107: G107:

T304 = K120 + S121
53 G23A: G100: G101: G102: G103:

T305 = K120 + S120
53 G23C: G104: G105: G106: G107:

T306 = K110 + S121
53 G24A: G100: G101: G102: G103:

T307 = K110 + S120
53 G24C: G104: G105: G106: G107:

T500 = K130 + I004
53 F29A: G200:

J T501 = K130 + I014
53 F29C: G201:

T502 = K130 + I024
53 F30A: G202:

T503 = J565 + I034
53 F30C: G203:

J T504 = J565 + I044
53 F31A: G204:

J T505 = J565 + I054
53 F31C: G205:

J T506 = J565 + I064
53 F32A: G206:

J T507 = J565 + I074
53 F32C: G207:

U000 = R000 + Q000
22 A17A: E000: E300: E501: E502:

U010 = R010 + Q010
22 A17C: E010: E300: E502:

U020 = R020 + Q020
22 A20A: E020: E300:

U030 = R030 + Q030
22 A20C: E030: E301: E504: E505:

U040 = R040 + Q040
22 A24A: E040: E301: E505:

U050 = R050 + Q050
22 A24C: E050: E301:

U060 = R060 + Q060
22 A27A: E060: E302: E507:

U070 = R070 + Q060
22 A27C: E070: E302:

V000 = H000 + C000
12 I02: H001: K002: K003: K012: K013:
K140: X516:

J V001 = H001 + C001
12 I05: H002: I860: I860: K854: N212:
X504: K905

V002 = H002 + C000
12 I09: H003: K224: K858: K903:
W023: W376: X507:

V003 = H003 + C001
12 I12: F300: H004: I871: K140: K860:
N232: W810: K241:

J V004 = H004 + C000
22 I14C: H005: K862: N244: X503

V005 = H005 + C001
12 I17: H006: K000: K001: K010: K011:
K111: F313

V006 = H006 + C000
12 I23: F311: I861: H007: K100: K140:
F302: K856: K130:

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V007 = H007 + C001
22 I28A: F301: H000: K864

V010 = H000 + C002
22 I03A: W102: K110: K120: I581:

(D) V012 = H002 + J003 + N001 Y012 + I554
14 I10: Z000: Z010: Z020: Z030: Z040:
Z050: Z060: Z070:

V013 = H003 + J003 + C003
13 I13: F310: K421: K421: K853: K857:
W028:

V015 = H005 + J000 + C003
13 I18: F304: F304: F305: F305:
F305: F306: W058:

V016 = H006 + J009 + C002
13 I24: H201: H211: H221: H231: K320:
K320: K420: K420:

(J) V017 = H007 + J009 + C003
13 I29: F301: K121: K131: X513:

V022 = H002 + C004 + GND
23 L29C: I573: K865: X514:

V023 = H003 + C007
22 I14A: X500: X500: X508: X510:

V025 = H005 + J006 + C003
13 I19: K322: K420: F280: X502: J905:
F324:

(M) V026 = H006 + J009 + GND
13 I25: F325: F326: F327: F328:
F323: K225: K440: K440:

V032 = H002
20 B11B: F300:

(P) (M) V035 = H005 + J012 + GND
23 I20A: F323:

V036 = H006 + J009 + C002
13 I26: F329: K441: I579: I579: I858:
K101: X506: X506:

(P) V046 = H006 + J009 + C004
23 I20C: K441: K901: F323:

V201 = H201 + C005
22 J16A: K201: K210:

V211 = H211 + C005
22 J16C: K211: K220:

V221 = H221 + C005
12 J25: K210: K221: K222: K223: K230:
K443:

V231 = H231 + C005
22 J31A: K200: K210: K220: K231:

V521 = K801 + K810 + K812 + K522 + X503 + X513
16 M21: H000: K321: K323: K441: K525:

(H) V901 = K802 + K811 + K813
23 M06A: K901: X519:

(J) V902 = K802 + K810 + K813
13 M07: I579: K442: K524: K900: K902:

V903 = K801 + K810 + K812
13 M08: H000: H000: X502: X505: X518:

(J) W000 = F300
11 D01: P000: P001: P010: P011: P020:
P021: P030: P031:

W003 = F300 + P025
12 D14: P040: P041: P050: P051: P060:
P061: P070: P071:

W005 = P025 + F300 + P055
13 C27: P100: P101: P110: P111: P120:
P121: P130: P131:

W020 = W023
21 D37A: S101: S111: S121: S131:

W021 = W023
11 E26: S001: S011: S021: S031: S041:
S051: S061: S071:

W023 = J001 V002 F303
20 E15D: W020: W021:

W024 = W028
11 N05: V900: X901: X910: X911: X920:
X921: X930: X931:

W027 = I501 + W028 + I504
13 N24: X980: X981: X990: X991:

W028 = I593 V013
21 N04A: W024: W027: W030:

W030 = W028 + I501
12 N17: X940: X941: X950: X951: X960:
X961: X970: X971:

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J

W050 = F302
21 D38A: S100: S110: S120: S130:

W051 = F305
21 D38C: S100: S110: S120: S130:

W052 = F302
11 E23: S000: S010: S020: S030: S040:
S050: S060: S070:

W054 = F304 W058 I861
11 E24: S000: S010: S020: S030: S040:
S050: S060: S070:

W056 = F306
11 E25: S000: S010: S020: S030: S040:
S050: S060: S070:

W058 = V015 I593
20 E15C: W054:

W070 = F301
11 D05: P002: P003: P012: P013: P022:
P023: P032: P033:

W072 = F301
11 D18: P042: P043: P052: P053: P062:
P063: P072: P073:

W073 = F301
11 C29: P102: P103: P112: P113: P122:
P123: P132: P133:

W100 = W102 J907
11 G33: Z001: Z011: Z021: Z031: Z041:
Z051: Z061: Z071:

W102 = V010 J031 W325
21 H22A: W100:

W110 = I554 + I852
12 D35: I006: I016: I026: I036: I046:
I056: I066: I076:

W112 = X504
11 D36: I006: I016: I026: I036: I046:
I056: I066: I076:

W122 = F331 F308
11 G31: I001: I011: I021: I031: I041:
I051: I061: I071:

W124 = J914 F200
11 G32: I001: I011: I021: I031: I041:
I051: I061: I071:

W130 = J923 F310 J921
11 K10: F001: F011: F021: F031: F041:
F051: F101: F111:

W160 = F311
11 K11: F000: F010: F020: F030: F040:
F050: F100: F110:

W162 = F313
11 I31: O020: O021: O030: O031: O040:
O041: O050: O051:

W164 = F313
21 I32A: O000: O001: O010: O011:

(J) W200 = F316
11 A01: R000: R010: R020: R030: R040:
R050: R060: R070:

(J) W202 = F315
11 A02: R000: F010: R020: R030: R040:
R050: R060: R070:

(J) W204 = F318
11 A03: R000: R010: R020: R030: R040:
R050: R060: R070:

W208 = F317
11 A08: R010: R020: R030: R040: R050:
R060: R070:

(J) W210 = F319
11 A09: Q000: Q010: Q020: Q030: Q040:
Q050: Q060: Q070:

(J) W212 = F320
11 A10 Q000 Q010 Q020: Q030: Q040:
Q050: Q060: Q070:

W214 = F321
11 A11 Q010: Q020: Q030: Q040: Q050:
Q060: Q070:

W250 = F323
11 B22: A040: A041: A050: A051: A060:
A061: A070: A071:

(J) W252 = F323
11 B08: I200: I202: I204: I206: I208:
I210: I212: I214:

W260 = F328
11 B23: A040: A041: A050: A051: A060:
A061: A070: A071:

W262 = F328
11 B09: I200: I202: I204: I206: I208:
I210: I212: I214:

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W264 = F325
11 B10: I200: I202: I204: I206: I208:
I210: I212: I214:

W266 = F326
11 N07: X900: X901: X910: X911: X920:
X921: X930: X931:

W268 = F326
11 N18: X940: X941: X950: X951: X960:
X961: X970: X971:

W269 = F326
21: N20C: X980: X981: X990: X991:

W320 = F307
11 G34: I002: I012: I022: I032: I042:
I052: I062: I072:

W323 = J914 F200 F331 F308
11 H24: I002: I012: I022: I032: I042:
I052: I062: I072:

W325 = I554
21 H22C: W326: W102:

W326 = W325
11 H23: I004: I014: I024: I034: I044:
I054: I064: I074:

W327 = I554
11 E39: I004: I014: I024: I034: I044:
I054: I064: I074:

W360 = F327
21 O28A: X800: X801: X810: X811: X820:

W361 = F327
21 O28C: X821: X830: X831: X840: X841:

W362 = F327
21 O32A: X850: X851: X860: X861: X870:

W363 = F327
21 O32C: X871: X880: X881: X890: X891:

W364 = F324 I369 + I354
12 C03: X000: X001: X010: X011: X020:
X021: X030: X031:

W366 = F324 I369 + I356
12 C13: X100: X101: X110: X111: X120:
X121: X130: X131:

W368 = F324 I369 + I358 F210
12 C20: X200: X201: X210: X211: X220:
X221: X230: X231:

W370 = W376
11 N08: X902: X903: X912: X913: X922:
X923: X932: X933:

W374 = W376
11 N19: X942: X943: X952: X953: X962:
X963: X972: X973:

W375 = W376
21 N28A: X982: X983: X992: X993:

W376 = I593 J002 V002
21 N28C: W370: W374: W375:

W460 = F329
11 D06: P000: P001: P010: P011: P020:
P021: P030: P031:

W462 = F329
11 D19: P040: P041: P050: P051: P060:
P061: P070: P071:

W464 = F329
11 C28: P100: P101: P110: P111: P120:
P121: P130: P131:

W800 = J001 I852
21 E09A: W801: W803: W805:

W801 = W800
11 E01: P200: P201: P210: P211: P220:
P221: P230: P231:

W803 = W800
11 E05: P240: P241: P250: P251: P260:
P261: P270: P271:

W805 = W800
11 E17: P280: P281 P290: P291: P300:
P301: P310: P311:

W810 = V003 J008 F271 F101
20 E15B: W811: W812:

W811 = W810
11 E16: P202: P212: P222: P232: P242:
P252: P262: P272:

W813 = W810
21 E09C: P282: P292: P302: P312:

(J) X000 = W364 I300
30 C01A:

X001 = W364 I301
30 C01B: I302:

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X010 = W364 I310
30 C01C:

X011 = W364 I311
30 C01D: I312:

X020 = W364 I320
30 C02A:

X021 = W364 I321
30 C02B: I322:

X030 = W364 I330
30 C02C:

X031 = W364 I331
30 C02D: I332:

X100 = W366 I300
30 C11A:

(J) X101 = W366 I301
30 C11B: I302:

X110 = W366 I310
30 C11C:

X111 = W366 I311
30 C11D: I312:

X120 = W366 I320
30 C12A:

X121 = W366 I321
30 C12B: I322:

X130 = W366 I330
30 C12C:

X131 = W366 I331
30 C12D: I332:

X200 = W368 I300
30 C18A:

X201 = W368 I301
30 C18B: I302:

X210 = W368 I310
30 C18C:

X211 = W368 I311
30 C18D: I312:

X220 = W368 I320
30 C19A:

X221 = W368 I321
30 C19B: I322:

X230 = W368 I330
30 C19C:

X231 = W368 I331
30 C19D: I332:

(K) X500 = F078: F099: V023: J232 J007 + I554 V023 J
32 001A: X502: X518: X502:

(K) (H) X501 = I580 + K800 K803 K813 X518 I587 + F500 X515
32 001C: I559: I555: J103

(F) X502 = V903 X513 X500 + X500 I550 V025 I551 I517
32 002A: H221: H231: X505: X513:

X503 = I580 + V004 J007
32 002C: H000: I590: V521: X504:

X504 = V001 X503
31 003A: I554: I593: J234: W112: X519:

X505 = X502 V903
31 003C: F205: F305: I553: I592: K856

X506 = V036 F502 + V036 I593
32 008A:

(P) X507 = I552 + I593 V002
32 008C: I555: I570: I559:

(E) X508 = X510 V023 F502 J007
31 010A: I551: X510: I589:

(J) X509 = I580
31 010C: I551: I555: I570: J12-V

X510 = X508 V023 F503 J007
(E) 31 011A: I551: X508: X514: I589:

X511 = I580
31 011C: F205: I559: I573: I581: J12-U

(K) X512 = K813 X519 I551 J103 K810 + GND
32 009A: H221: H231: H201: H211:

X513 = J904 + X502 V017
32 009C: H000: X502: V521

X514 = X510 F503 V022 J010
30 007C:

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(F) X520 = I578 M322 : M330
30 K15C : X517 :

X521 = F124
30 K15D

X515 = I554
30 O07D : X501 :

(E)(K) X516 = GND + I551 V000
32 013A

(F)(E)(K)(C) X517 = I552 M322 X520 I598 + J901
32 013B I568 : F208 :

(J) X518 = V903 I587 X50C
31 O22A : I555 : I559 : X501 :

X519 = I595 V901 X504
31 O22C : X512 :

X700 = M500 I571 + I002 I574
32 N33A : I004 :

X701 = I582 + GND
32 N33C : L500 : J12-A :

X710 = M510 I571 + I012 I574
32 N34A : I014 :

X711 = I582 + GND
32 N34C : L510 : J12-C :

X720 = M520 I571 + I022 I574
32 N35A : I024 :

X721 = I582 + GND
32 N35C : L520 : J12-E :

X730 = M530 I571 + I032 I574
32 N36A : I034 :

X731 = I582 + GND
32 N36C : L530 : J12-H :

X740 = M540 I571 + I042 I574
32 N37A : I044 :

X741 = I582 + GND
32 N37C : L540 : J12-K :

X750 = M550 I571 + I052 I574
32 N38A : I054 :

X751 = I582 + GND
32 N38C : L550 : J12-M :

X760 = M560 I571 + I062 I574
32 N39A : I064 :

X761 = I582 + GND
32 N39C : L560 : J12-P :

X770 = M570 I571 + I072 I574
32 N40A : I074 :

X771 = I582 + GND
32 N40C : L570 : J12-S :

X800 = A001 W360
30 O29A : I510 :

(J) X801 = A002 W360
30 O29B : I510 : J10-C :

X810 = A011 W360
30 O29C : I510 :

(J) X811 = A012 W360
30 O29D : I510 : J10-F :

X820 = A021 W360
30 O30A : I510 :

X821 = A022 W361
30 O30B : I510 : J10-K

X830 = A031 W361
30 O30C : I512 :

X831 = A032 W361
30 O30D : I512 : J10-N :

X840 = A043 W361
30 O31A : I512 :

X841 = A042 W361
30 O31B : I512 : J11-C :

X850 = A053 W362
30 O31C : I512 :

(J) X851 = A052 W362
30 O31D : I512 : J11-F :

X860 = A063 W362
30 O33A : I514 :

X861 = A062 W362
30 O33B : I514 : J11-K :

X870 = A073 W362
30 O33C : I514 :

X871 = A072 W363
30 O33D : I514 : J11-N :

X880 = I303 W363
30 O34A : I514 :

```
X881 = I302 W363
30 O34B:  I514: J11-S:

X890 = I313 W363
30 O34C:  I516:

X891 = I312 W363
30 O34D:  I516: J11-V:

X900 = X902 W024 + A001 W266
32 N01A:  I006:  I214:    I510:    X903:

X901 = W266 A002 + W024 X903
32 N01C:  I212:  I510:    X902:  J10-A:

X902 = X901 W370
30 N02A:  I500:  X900:

X903 = X900 W370
30 N02B:  I501:  X901:

X910 = X912 I500 W024 + W266 A011
32 N03A:  I016:  I210:    I510:    X913:

X911 = W266 A012 + W024 I500 X913
32 N03C:  I208:  I510:    X912:  J10-D:

X912 = X911 W370
30 N02C:  I532:  X910:

X913 = X910 W370
30 N02D:  I501:  X911:

X920 = I532 X922 I500 W024 + A021 W266
32 N09A:  I026:  I206:    I510:    X923:

X921 = A022 W266 + W024 I500 I532 X923
32 N09C:  I204:  I510:    X922:  J10-H:

X922 = X921 W370
30 N10A:  I503:  X920:

X923 = X920 W370
30 N10B:  I501:  X921:

X930 = I503 X932 I532 I500 W024 + A031 W266
32 N11A:  I036:  I202:    I512:    X933:

X931 = W266 A032 + W024 I500 I532 X933 I503
32 N11C:  I200:  I512:    X932:  J10-L:

X932 = X931 W370
30 N10C:  X930:

X933 = X930 W370
30 N10D:  I501:  X931:

X940 = X942 W030 + A043 W268
32 N13A:  A041:  I046:    I512:    X943:

X941 = W268 A042 + W030 X943
32 N13C:  A040:  I512:    X942:  J11-A:

X942 = X941 W374
30 N14A:  I535:  X940:

X943 = X940 W374
30 N14B:  I504:  X941:

X950 = I535 X952 W030 + A053 W268
32 N15A:  A051:  I056:    I512:    X953:

X951 = W268 A052 + W030 X953 I535
32 N15C:  A050:  I512:    X952:  J11-D:

X952 = X951 W374
30 N14C:  I531:  X950:

X953 = X950 W374
30 N14D:  I504:  X951:

X960 = I531 X962 I535 W030 + A063 W268
32 N21A:  A061:  I066:    I514:    X963:

X961 = W268 A062 + W030 I535 X963 I531
32 N21C:  A060:  I514:    X962:  J11-H:

X962 = X961 W374
30 N22A:  I505:  X960:

X963 = X960 W374
30 N22B:  I504:  X961:

X970 = I531 X972 I535 I505 W030 + A071 W268
32 N23A:  A071:  I076:    I514:    X973:

X971 = A072 W268 + W030 I505 I535 X973 I531
32 N23C:  A070:  I514:    X972:  J11-L:

X972 = X971 W374
30 N22C:  X970:

X973 = X970 W374
30 N22D:  I504:  X971:

X980 = X982 W027 + I303 W269
32 N25A:  I303:  I514:    X983:

X981 = W269 I302 + W027 X983
32 N25C:  I514:  X982:  J11-P:
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X982 = X981 W375
30 N26A: I538: X980:

X983 = X980 W375
30 N26B: X981:

X990 = X992 I538 W027 + I313 W269
32 N27A: I313: I516: X993:

X991 = W269 I312 + W027 I538 X993
32 N27C: I516: X992: J11-T:

X992 = X991 W375
30 N26C: X990:

X993 = X990 W375
30 N26D: X991:

(J) Y850 = GND
73A D25: I851:
Y851 = GND
73A D25: K852:
Y901 = GND
73A D25: J111:

Y902 = GND
73A D25: I368:

Y903 = GND
73A D25: I369:

(J) Y000 =
G12 F11A:G000:

Y001 =
G12 F09A:G001:

Y002 =
G12 F11C: G002:

Y003 =
G12 F09C: G003:

Y004 =
G12 F12A: G004:

Y005 =
G12 F10A: G005:

Y006 =
G12 F12C: G006:

(J) Y007 =
G12 F10C: G007:

(J) (D) VO12 = GND
G20 H21: VO12

(J) Y100 =
G12 G01A: G100:

(J) Y101 =
G12 G03A: G101:

Y102 =
G12 G01C: G102:

Y103 =
G12 G03C: G103:

Y104 =
G12 G02A: G104:

Y105 =
G12 G04A: G105:

Y106 =
G12 G02C: G106:

Y107 =
G12 G04C: G107:

Y200 =
G14 H01: I002:

Y210 =
G14 H02: I012:

Y220 =
G14 H03: I022:

Y230 =
G14 H04: I032:

Y240 =
G14 H05: I042:

Y250 =
G14 H06: I052:

Y260 =
G14 H07: I062:

Y270 =
G14 H08: I072:

Y500 =
G13 H17A: G200:

Y501 =
G13 H17C: G201:

Y502 =
G13 H18A: G202:

(J) Y503 =
G13 H18C: G203:

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Y504 =
G13 H19A: G204: (J)

Y505 =
G13 H19C: G205:

Y506 =
G13 H20A: G206:

Y507 =
G13 H20C: G207:

(D)

Y900 = GND
G20 H21: I002
Y910 = GND
G20 H21: I012
Y920 = GND
G20 H21: I022
Y930 = GND
G20 H21: I032
Y940 = GND
G20 H21: I042
Y950 = GND
G20 H21: I052
Y960 = GND
G20 H21: I062
Y970 = GND
G20 H21: I072 (J)

Z000 = V012 I002 + I005
32 G25A: I004: I006: R000: O001:

Z001 = W100 + GND
32 G25C: F000: R000: J12-B: L000

Z010 = V012 I012 + I015
32 G27A: I014: I016: R010: O011:

Z011 = W100 + GND
32 G27C: F010: R010: J12-D: L010

Z020 = V012 I022 + I025
32 G28A: I024: I026: R020: O021:

Z021 = W100 + GND
32 G28C: F020: R020: J12-F: L020

Z030 = V012 I032 + I035
32 G30A: I034: I036: R030: O031:

Z031 = W100 + GND
32 G30C: F030: R030: J12-J: L030

Z040 = V012 I042 + I045
32 G35A: I044: I046: R040: O041:

Z041 = W100 + GND
32 G35C: F040: R040: J12-L: L040

Z050 = V012 I052 + I055:
32 G37A: I054: I056: R050: O051:

Z051 = W100 + GND
32 G37C: F050: R050: J12-N: L050

Z060 = V012 I062 + I065
32 G38A: I064: I066: R060:

(K) Z061 = W100 + GND
32 G38C: F100: R060: J12-R: I406

Z070 = V012 I072 + I075
32 G40A: I074: I076: R070:

(K) Z071 = W100 + GND
32 G40C: F110: R070: J12-T: I404

APPENDIX C
SPECIAL FUNCTION ASSIGNMENTS

INTRODUCTION

Some logic elements are frequently referred to in a Maintenance program, and are listed here with their specific logic assignments. These logic elements are of primary logic importance, and usually are given special names. Conditions are also given for a resultant logical one on the output of the subject symbols. The elements are listed in alpha-numerical order, and may be used in conjunction with the equation file to describe final operational conditions. Some of these functions are timed, which requires consultation of the Main Timing and Main Control logic diagrams.

Logic Symbol	Function
A000, A010-, A070	A Register
A100, A110-, A170	A' Register
E000, E010-, E070	Stage Enable (SE) FFs
E001, E011-, E071	No Stage Enable (SE) FFs
E200, E201, E202	Group Enable (GI) A' Register
E300, E301, E302	Group Borrow Generators (GBG) A' Register
E400, E401, E402	Group Borrow Input (GBI) A' Register
E500, E501-, E507	Stage Probe Input (SPI) A' Register

F002	XXX XX0	F063	$\overline{\text{XXX 011}}$
003	XXX XX1	064	$\overline{\text{XXX 100}}$
012	XXX X0X	065	$\overline{\text{XXX 110}}$
013	$\overline{\text{XXX X1X}}$	066	$\overline{\text{XXX 111}}$
014	XXX X0X	067	$\overline{\text{XXX X01}}$
015	XXX X1X	068	XXX X00
022	XXX 0XX	069	XXX X10
023	XXX 1XX	070	$\overline{\text{XXX 00X}}$
025	XXX 1XX	071	$\overline{\text{XXX 001}}$
031	$\overline{\text{XX0 XXX}}$	072	XXX 010
041	$\overline{\text{X0X XXX}}$	073	XXX 011
042	X0X XXX	074	XXX 100
050	1XX XXX	075	XXX 110
052	0XX XXX	076	XXX 111
053	1XX XXX	077	XXX X01
054	$\overline{\text{XXX 100}}$	078	XXX 00X
056	XXX 000	079	$\overline{\text{XXX 1X1}}$
057	XXX X11	080	$\overline{\text{000 XXX}}$
059	XXX 1XX, $\overline{\text{XXX 111}}$	081	$\overline{\text{001 XXX}}$
060	XXX X10	082	$\overline{\text{01X XXX}}$
061	$\overline{\text{XXX 001}}$	083	01X XXX
062	$\overline{\text{XXX 010}}$	084	$\overline{\text{100 XXX}}$

F085	$\overline{101}$	XXX
086	$\overline{110}$	XXX
087	$\overline{111}$	XXX
088	000	XXX
089	000	XXX
090	001	XXX
091	100	XXX
092	101	XXX
093	101	XXX
094	110	XXX
095	110	XXX
096	111	XXX
097	111	XXX
098	111	XXX
099	111	XXX
101	X1X	XXX XX

F112	000	XXX
114	111	XXX
115	111	1XX, $\overline{111\ 111}$
120	$\overline{111}$	$\overline{01X}$
121	111	01X
122	111	01X
123	111	01X
124	$\overline{111}$	$\overline{101}$
125	111	101
127	111	01X
130	000	101
131	XXX	1X1
132	$\overline{0X1}$	$\overline{XXX}$
133	$\overline{0X1}$	$\overline{XXX}$
134	$\overline{011}$	$\overline{XXX}$

F200 $C\ [\overline{(Ent. + Swp.)}(\overline{SSI})]\ [4X + SX.C']$

F206 $(SSI)(OBA) + C\ [\overline{(Ent. + Swp.)}(\overline{SSI})]\ (\overline{4X + 5X.C' + 76}) + \overline{72.C'}\ B\ [\overline{(Ent. + Swp.)}\ (\overline{SSI})]\ \overline{A}(Ent)(Swp.)(SSI) + D\ [\overline{(Ent. + Swp.)}(SSI)] + (Swp.)$

F208 $\overline{(Buff\ BSY)(04 + 05 + 70 + 71) + 6X(Jump\ SAT)}$

F209 $\overline{F208}$

F211 $6X(\overline{Jump\ SAT}) + (\overline{Buff\ BSY})(04 + 05 + 70 + 71)$

F213 $\overline{17 + 23 + 24 + 27 + 33 + 37 + 44 + 45 + 46 + 47 + 52 + 56}$

F214 $31 + 35 + 41 + 45 + 51 + 55 + 72.\overline{C'} + 73.\overline{C'}$

F216 $[\overline{(Ent. + Swp.)(SSI)}]\ [B(11 + 15 + 41 + 45 + 51 + 55 + 72.\overline{C'} + 73.\overline{C'}) + C(Load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72 + 73 + 74 + 75)] + A\ [\overline{(Ent.)(Swp.)(SSI)}] + D\ [\overline{(Ent. + Swp.)(SSI)}] + [Ent. + Swp.]$

F222 $[\overline{(Ent. + Swp.)(SSI)}]\ [B(11 + 15 + 41 + 45 + 51 + 55 + 72.\overline{C'} + 73.\overline{C'}) + C(Load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72.\overline{C'} + 73.\overline{C'} + 74 + 75)] + A\ [\overline{(Ent.)(Swp.)(SSI)}] + D\ [\overline{(Ent. + Swp.)(SSI)}] + [Ent. + Swp.]$

F226 $12 + 16 + 22 + 26 + 32 + 36 + 42 + 46$

F229 $11 + 12 + 13 + 15 + 16 + 17 + 22 + 23 + 26 + 27 + 31 + 32 + 33 + 35 + 36 + 5X.\overline{C'} + 4X$

F232 $04 + 05 + 20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + 5X + 70 + 72 + 74 + 75 + \overline{1X} + \overline{4X} + \overline{6X}$

F233 $\overline{72 + 73 + 75}$

F235 01

F236 5X + 72 + 73 + 75

F239 $\overline{5X.C' + 75.C' + (72+73)(A'\neq 0)\ (I/O\ Seq.)}$

F242 (Load) + 6X(Jump SAT) + 40 + 44 + 77 + (Buff BSY)(04 + 05 + 70 + 71)

F243 C' + 55 + 75

F248 A≠0

F251 Jump SAT

F252 $\overline{\text{Jump SAT}}$

F256 20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + (72 + 73)C [$\overline{(\text{Ent.} + \text{Swp.})}\,\overline{(SSI)}$]

F271 13

F300 Adv. P_1 by 1

F301 $P_2 = P_1$

F302 P → S, P' — S'

F303 $\overline{5.C'}$

F304 Z → S

F305 Tag → S'

F306 A → S

F307 MCS → Z

F308 INP → Z: $\overline{(\text{Ent.} + \text{Swp.})}\,\overline{SSI}$ [B.72.C' + C(Load)]

F310 Clear F, F'

F311 Z → F, F'

F313 Z → On

F315 +Z → R

F316 -Z → R

F317 +1 → R

F318 A → R

F319 A → Q

F320 A.2' → Q

F321 +1 → Q

F322 Block Probe A'

F323 $A' \rightarrow A$

F324 $A \rightarrow$ Tag Reg.

F325 Tag Reg. $\rightarrow A$

F326 $A \rightarrow BER$, $I_3 \rightarrow BER$

F327 $A \rightarrow BXR$, $I_3 \rightarrow BXR$

F328 BER A

F329 $A' \rightarrow P$, Tag $\rightarrow P'$

F331 $INP \rightarrow Z$: $\overline{76} + \overline{C} + (Ent. + Swp.) + (SSI)$

F332 $01 + \overline{D} + (Ent. + Swp.) + (SSI)$

F501 $70 + 71$

F502 $[Load + \overline{Clear\ F, F'}) + (Ent. + Swp.)]\ (70 + 71)$

F503 $[(\overline{Load})\ Clear\ F, F')(Ent. + Swp.)]\ (70 + 71)$

I219 Tag $\rightarrow A$

I402 $A' \neq 0$

I403 $A' = 0$

I519 BER = BXR

I550 $A(\overline{Ent.})(\overline{Swp.})(\overline{SSI}) + B\ [(\overline{Ent. + Swp.})(\overline{SSI})] + [74 + 75 + 76]$
$[(D\ (\overline{Ent. + Swp.})(\overline{SSI})]\ )$
$(Load + [(\overline{Ent. + Swp.})(13)(00 + 01 + 02 + 03 + 06 + 07 + 77)(\overline{01})$
$\{\overline{5X(Jump\ SAT) + (04 + 05 + 70 + 71)(Buff\ BSY)}\}]\ ) +$
$C\ [(\overline{Ent. + Swp.})(\overline{SSI})]\ [\overline{55 + 75}]$

I551 $(\overline{IBA}) + (\overline{OBA})$

I554 (Buffer Cycle)

I560 BFR $\rightarrow$ Buff Output Cable (B.O.C)

I561 $Z \rightarrow$ B.O.C.

I562 $Z \rightarrow$ B.O.C.

I570 $(Buff\ RDY) + (IBA) + (\overline{Input\ RDY})$

I571 $INP \rightarrow BFR$

I573 $(Buffer\ Cycle) + (OBA) + (\overline{Time\ 22})$

I574 $MCS \rightarrow BFR$

I577 Buff. INP Cable $\rightarrow Z$

I580 Clear Buffer Controls

I582 Clear Buffer

I588 (Buffer Busy)

I590 (SSI)

I593 (Buff Cycle)

I852 (Int. 10, 20, 30, 40)

I853 Block P $\rightarrow$ S

I857 (Block P $\rightarrow$ S)(I/O Seq.)$(\overline{\text{Ent.} + \text{Swp.}})(\overline{\text{Load}})(\overline{13})$

I859 (Master Clear)(Time 26)(D $[(\overline{\text{Ent.} + \text{Swp.}})(\overline{\text{SSI}})]$)

I860 Clear P, P'

I861 Interrupt Address $\rightarrow$ S

I862 $(\overline{\text{Int. 10, 20, 30, 40}})$

I863 Interrupt Address Enable $\rightarrow$ S

I872 Interrupt Address $\rightarrow$ P

J107 Timing Error Stop

J200 $\overline{A}$ + (Ent.) + (Swp.) + (SSI)

J211, J212 B $[(\overline{\text{Ent.} + \text{Swp.}})(\overline{\text{SSI}})]$

J221, J222, J223 C $[(\overline{\text{Ent.} + \text{Swp.}})(\overline{\text{SSI}})]$

J224, J225, J226 C'

J227, J228 $\overline{C'}$

J231, J232, J233, J235 D $(\overline{\text{Ent.} + \text{Swp.}})(\overline{\text{SSI}})$

J441 (I/O Seq. Set)

J446 (Load) + B $[(\overline{\text{Ent.} + \text{Swp.}})(\text{SSI})]$

J560 $(\overline{\text{Main Timing Fault}})$

J900 $(\overline{\text{Master Clear}})$

J901, J902, J903, J904 (Master Clear)

J907 $(\overline{\text{Master Clear}}(\overline{\text{Clear Z}})$

J908 $\overline{(\text{Master Clear})(\text{Clear P})}$

J909, J910 Clear P'

J912 $\overline{\text{Load}}$

J913 Load

J914 $\overline{\text{Enter}}$

J917, J921 $\overline{(\text{Enter} + \text{Sweep})}$

J923 $\overline{\text{Load}}$

J930 $(\overline{\text{Master Clear}})$

K000, K002, K010, K012 Timing Chain Excursion Counters

K100 Divert

K110 Read

K120 Write

K130 Inhibit

K140 Timing Fault

K200 A Cycle

K210 B Cycle

K220 C Cycle

K222, K224 C' Cycle

K230 D Cycle

K240 Block $P_2 = P_1$

K320 Wait Output

K322 Function Ready

K420 Wait Input

K440 I/O Seq.

K522 Sample

K524 Enable

K800, K802, K810, K812 } Resync. Counter

K850 Manual Interrupt

K852 Manual Interrupt

K854 Manual Interrupt 10

K856 Buffer Interrupt

K858 Buffer Interrupt 20

K860 External Interrupt 30

K862 External Interrupt 40

K864 Interrupt Lockout

K900 Run

K902 Step

K904 Neutral

L000, L010, L110 } 0 Register Inputs

L321 Information Ready

L322 Function Ready

L323 Master Clear

L330 I/O Sequence

L331 Load Mode

L421 Input Request

L500, L510, L610 } BFR Outputs

L512 Information Ready
L513 Input Request
L514 Function Ready
L515 Master Clear

M000
M010 } Z Register Inputs
M070

M330 Output Resume

M420 Input Ready

M424 Input Disconnect

M500
M510 } BFR Inputs
M570

M512 Output Resume

M513 Input Ready

M514 Input Disconnect

M850 Manual Interrupt Input

M851
M852 } External Interrupt Input

M900 Run

M901 Step

M902 Neutral

M903 Load

M904 Master Clear

M905 Clear A

M906 Clear Z

M907 Clear P

M908 Enter

M909 Sweep

N210 Clear A': $\overline{N212}$

N212 $[\overline{(A \rightarrow Tag)} + D + (Ent. + Swp.) + (SSI)]$ (Time 01)

N230 Toggle A': $\overline{N232}$

N232 $[\overline{(A \rightarrow Tag)} + \overline{D} + (Ent. + Swp.) + (SSI)]$ (Time 23)

O000
O010 } O Register
O050

P000
P010 } P_1 Register
P070

P002
P012 } P_2 Register
P072

P100
P110
P120 } P_1' Register
P130

P102
P112
P122 } P_2' Register
P132

Q000
Q010 } Q Inverters
Q070

R000
R010 } R Inverters
R070

S000
S010 } Divert FF's, S Register
S050

S060
S070 } R/W Drive FF's, S Register

S100
S110
S120 } R/W Drive FF's, S' Register
S130

U000
U010 } Stage Borrow FF's (SB)
U070

W024 Adv. BER: ($\overline{\text{Buff Cycle}}$) (Time 13)

W028 $\overline{\text{Adv. BER}}$

W058 IO-6 $\longrightarrow$ S

W100 Clear Z

W102 Strobe

W110 Enable Z $\longrightarrow$ S

W112 $(\overline{\text{Buff, Cycle}})$

W323 INP $\rightarrow$ Z

W370, W374, W375 $(\overline{\text{Buff Cycle}})$ (Time 02)

W800 P $\rightarrow$ P'

W810 $\overline{13}$ + (Load) + $(\overline{\text{Clear F}})$ + (Ent. + Swp.) + $(\overline{\text{Time 23}})$

W813 13$(\overline{\text{Load}})$(Clear F)$(\overline{\text{Ent. + Swp.}})$ $(\overline{\text{Time 23}})$

X000, X010, X020, X030 Tag 1 Register

X100, X110, X120, X130 Tag 2 Register

X200, X210, X220, X230 Tag 3 Register

X500 Block Seq. Interrupt (FF)

X502 Storage Seq. Int. (SSI)(FF)

X504 Buffer Cycle (FF)

X506 Buffer Ready (FF)

X508 Buffer Input (IBA)(FF)

X510 Buffer Output (OBA)(FF)

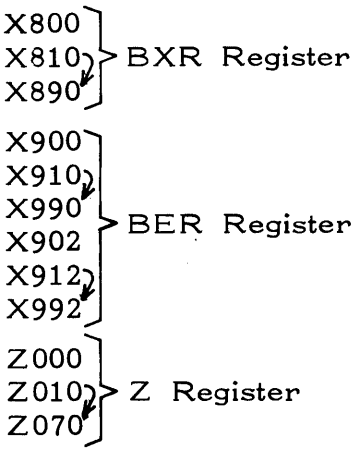
X512 Buffer Step (FF)

X514 Initiate Buffer Output (FF)

X516 Buffer Busy (FF)

X518 Buffer Sync. (FF)

X700, X710, X770 BFR Register


X800
X810
X890
BXR Register
X900
X910
X990
X902
X912
X992
BER Register
Z000
Z010
Z070
Z Register

APPENDIX D
PARTS LIST

8092 TeleProgrammer

PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
	8092 TeleProgrammer Final Assembly	
36407900	Cable assembly, control panel	1
364148-00	Cord assy, 3 cond	1
364147-00	Cord assy, 3 cond	1
13681200	Connector Plug, 3 wire, 15 amp	2
36099300	Receptacle, 3 wire, 10 amp	1
13697400	Cord assy, power	1
	Cabinet Assembly	
36046000	Grille, air intake	1
36059200	Handle, door	2
36059300	Handle, filter	2
36059400	Filter, modified	1
36084300	Power Supply (8092-A & 8092-B)	1
36098300	Control Panel	1
00815500	Blower	2
47054200	Power Supply, 30 amp, 60 Hz (8092-D)	1
47054201	Power Supply, 30 amp, 50 Hz (8092-E)	1
	Chassis Assembly	
100018	Connector, 30 socket	300
245120-1	Receptacle, 24 pin	18
361008-02	Connector plug, 17 pin	2
361008-04	Connector plug, 33 pin	8
10233-1	Card assy, type 02A	4
102018	Card assy, type 11A	75
102019	Card assy, type 12A	25
102020	Card assy, type 13A	18
102025	Card assy, type 14A	1
102026	Card assy, type 15A	2
102027	Card assy, type 16A	6
102322	Card assy, type 20A	54
102028	Card assy, type 21A	75
102034	Card assy, type 22A	37
102035	Card assy, type 23A	35
102036	Card assy, type 24A	5

PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
10232501	Card assy, type 28A	2
103344	Card assy, type 30A	37
102037	Card assy, type 31A	24
102038	Card assy, type 32A	61
102039	Card assy, type 33A	26
102040	Card assy, type 41A	11
102048	Card assy, type 44A	1
100063	Card assy, type 53A	18
102102	Card assy, type 67	3
102116	Card assy, type 68	12
102121	Card assy, type 69	9
10335200	Card assy, type 73A	1
36041500	Card assy, type G10	16
36041800	Card assy, type G11	4
36045301	Card assy, type G12-1	8
36045601	Card assy, type G13-1	4
36050600	Card assy, type G14	8
36722600	Card assy, type G19	16
36699900	Card assy, type G20 (previously 52A)	1
	Cable Assembly, Control Panel	
245139-1	Connector, plug, male 24 pin	6
36083201	Connector, card edge, 22 contacts	1
36083202	Connector, card edge, 18 contacts	1
36083204	Connector, card edge, 12 contacts	13
	Cover Assembly, Line Filter	
24513500	Fuse holder	2
51650229	Fuse, slow-blow, 15 amp 250 volt type MDA	2
36104500	Filter, interference	2
360399-02	Cord assembly, 3 cond	1
36039905	Cord assembly, 3 cond	1
	Outlet Box Assembly	
245136	Switch, toggle	1
8135	Grommet	3
8151	Receptacle, duplex	1

COMMENT SHEET

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