CONTROL DATA® 6675

Data Set Controller

EQUIPMENT DIAGRAMS
CIRCUIT DESCRIPTIONS
CARD PLACEMENT
MAINTENANCE
PARTS LIST

RECORD OF REVISIONS

REVISION	DATE ENTERED	INITIALS	NOTES
A	1-30-67		ECO number CF373, update and correct pages 1-1, 1-3, 1-4,
			1-6, 1-7, 1-9, 1-10, 1-11, 1-15, 1-17, 1-18, and 1-30.
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*includes card placement

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PART 1

EQUIPMENT DIAGRAMS AND CIRCUIT DESCRIPTIONS

INTRODUCTION

The CONTROL DATA* 6675 Data Set Controller enables remote computers to communicate with a Control Data 6000 Series Computer System over leased telephone transmission lines. The remote computers may be any computers using data sets compatible with the 6675.

The Control Data 6675 consists of a Data Channel Adaptor (DCA), a multiplexer, up to four data set controllers (DSC's), and a DATA-PHONE** Data Set for each controller. Each installation, job performed, and the software operating system determines the number of DSC's and type of data sets used.

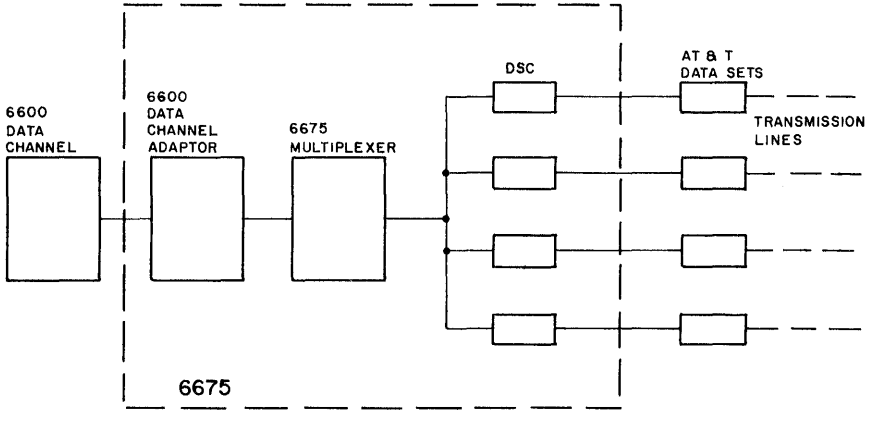

Figure 1-1. 6675 Simplified Block Diagram

An identifying letter designates the number of DSC's in each 6675 configuration. These letters are:

6675A	includes one DSC
6675B	includes two DSC's
6675C	includes three DSC's
6675D	includes four DSC's

DATA-PHONE** Data Set 301B is the standard data set for the 6675 although any of the listed data sets may be used or intermixed as long as the remote data set is the same as the local data set. Maximum transmission rate for the 6675 is 240 kilobits/second.

Bell System Data Set	Serial bit transfer rate
301B	40.8 kilobits/second
201A	2.0 kilobits/second
201B	2.4 kilobits/second
X303A10	19.2 kilobits/second
X303A20	50.0 kilobits/second
X303A30	230.4 kilobits/second

Figure 1-1 shows a 6675 equipped with four DSC's. The multiplexer assigns individual DSC's to transmit or receive. Each DSC converts 12-bit parallel words from the computer (via the DCA) to serial bits for the data set. The data set transmits serial data from the DSC's over a leased transmission line.

Customer engineering information contained in this publication covers the multiplexer and the DSC. Since all DSC's are identical, only one DSC is described in this manual. The Data Channel Adaptor (DCA) is described in the QSE 649 Data Channel Adaptor Reference/Customer Engineering Manual, publication number CDC 38700100. Control Data Peripheral Controller Cabinets CE Manual, publication number 60097300, discusses the cabinet cooling system, power supply, control wiring and temperature monitoring. The chassis maps, equation summary, and wire tabs for the 6675 are included in publication number CDC 38710000. Bell System Data Communication reference manuals describe the data sets.

This manual includes the following for the multiplexer and data set controller (DSC):

1) Circuit theory and diagrams
2) Card placement
3) Cable connections and pin assignments
4) Applicable tests and maintenance
5) Parts list

The equipment diagrams on pages 1-7 and 1-9 illustrate the multiplexer circuitry; the remaining diagrams relate to the DSC.

Programming information for the 6675 is given in the 6675 Data Set Controller Reference Manual, publication number 38701400.

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SYMBOL LIST

A000	C20A	1-13	C133	F34C	1-23	I005	B15C	1-11	I067	D11C	1-15	I150	E17A	1-23
A001	C20C	1-13	C134	F35A	1-23	I006	A14B	1-11	I071	E18C	1-15	I151	E17B	1-23
A002	C21A	1-13	C135	F35C	1-23	I007	E16B	1-11	I075	D14A	1-15	I152	E18D	1-23
A003	C21C	1-13	C136	F36A	1-23	I008	D15D	1-11	I076	E19B	1-15	I153	E20B	1-23
A004	C22A	1-13	C137	F36C	1-23	I009	B04B	1-11	I077	D18B	1-15	I154	E17C	1-23
A005	C22C	1-13	C138	F37A	1-23	I010	D41A	1-11	I078	B36A	1-15	I155	E19C	1-23
A006	C23A	1-13	C139	F37C	1-23	I011	D06B	1-11	I079	B35D	1-15	I156	E21B	1-23
A007	C23C	1-13	C140	F38A	1-23	I012	A12C	1-11	I080	D22B	1-15	I157	E18A	1-23
A008	C24A	1-13	C141	F38C	1-23	I013	B04C	1-11	I081	D23B	1-15	I158	D21B	1-23
A009	C24C	1-13	C142	F39A	1-23	I014	D15C	1-11	I082	D24B	1-15	I159	D20A	1-23
A010	C25A	1-13	C143	F39C	1-23	I015	D13B	1-11	I083	D25B	1-15	I160	E26C	1-23
A011	C25C	1-13	C144	F40A	1-23	I016	D16B	1-11	I084	D26B	1-15	I161	E23B	1-23
A012	C26A	1-13	C145	F40C	1-23	I017	B12B	1-11	I085	D27B	1-15	I162	E27A	1-23
A013	C26C	1-13	C146	F41A	1-23	I018	A13B	1-11	I086	D28B	1-15	I163	E24B	1-23
A014	C27A	1-13	C147	F41C	1-23	I019	A11B	1-11	I087	E25A	1-15	I164	E27C	1-23
A015	C27C	1-13	C148	F42A	1-23	I020	D12B	1-11	I100	B32A	1-17	I165	E25C	1-23
A016	C28A	1-13	C149	F42C	1-23	I021	D15A	1-11	I101	B32B	1-17	I166	E28A	1-23
A017	C28C	1-13				I022	D11A	1-11	I102	B32C	1-17	I167	B04D	1-23
A018	C29A	1-13	F900	A19B	1-7	I023	B03A	1-11	I103	B33A	1-17	I168	E28C	1-23
A019	C29C	1-13	F901	A19C	1-7	I024	C35A	1-13	I104	B33B	1-17	I169	D10A	1-11
A020	C30A	1-13	F902	A22A	1-7	I025	C32A	1-13	I105	B33C	1-17	I170	D09C	1-11
A021	C30C	1-13	F903	A20A	1-7	I026	C33A	1-13	I106	B34A	1-17	I171	E22B	1-23
A022	C31A	1-13	F904	A20C	1-7	I027	C34A	1-13	I107	B35A	1-17	I172	E26A	1-23
A023	C31C	1-13	F905	A21B	1-7	I028	C35B	1-13	I108	B35B	1-17	I173	E31B	1-23
			F906	A22B	1-7	I029	C32C	1-13	I109	B35C	1-17	I174	E29B	1-23
C100	F18A	1-23	F908	A23A	1-7	I030	C33C	1-13	I110	B34B	1-17	I175	E30B	1-23
C101	F18C	1-23	F909	A23B	1-7	I031	C34C	1-13	I111	B34C	1-17	I176	E38D	1-23
C102	F19A	1-23	F910	A23C	1-7	I032	C17B	1-13	I112	B36B	1-17	I177	B06B	1-11
C103	F19C	1-23	F911	A23D	1-7	I033	B17C	1-13	I113	B36C	1-17	I179	B03C	1-11
C104	F20A	1-23	F920	B14A	1-7	I034	C18A	1-13	I114	A15C	1-17	I180	E32B	1-23
C105	F20C	1-23	F921	B14B	1-7	I035	C18C	1-13	I115	B37A	1-17	I181	E33B	1-23
C106	F21A	1-23	F922	A18A	1-7	I036	C19A	1-13	I116	B37B	1-17	I182	E34B	1-23
C107	F21C	1-23	F923	A19A	1-7	I037	C19C	1-13	I117	B04A	1-17	I183	E19A	1-23
C108	F22A	1-23	F924	A18C	1-7	I038	E36A	1-13	I123	D34A	1-19	I184	B14C	1-11
C109	F22C	1-23	F925	A28A	1-7	I039	B16B	1-13	I124	D34C	1-19	I185	D14C	1-11
C110	F23A	1-23	F930	A25A	1-7	I040	B17A	1-13	I125	D38A	1-19	I186	D38C	1-11
C111	F23C	1-23	F931	A25C	1-7	I041	B18A	1-13	I126	D09A	1-19	I187	B11D	1-11
C112	F24A	1-23	F932	A26B	1-7	I042	B18C	1-13	I127	D38B	1-19	I188	D10B	1-11
C113	F24C	1-23	F933	B32A	1-7	I043	B19A	1-13	I128	D09B	1-19	I189	D10C	1-11
C114	F25A	1-23	F934	A27B	1-7	I044	B19C	1-13	I129	D39B	1-19	I190	D31A	1-11
C115	F25C	1-23	F940	B01A	1-7	I045	E36B	1-13	I130	D40B	1-19	I191	D15B	1-17
C116	F26A	1-23	F941	B01C	1-7	I046	B13A	1-13	I131	D41C	1-19	I192	B36D	1-11
C117	F26C	1-23	F942	B02A	1-7	I047	B14A	1-13	I137	E35A	1-21	I200	E02A	1-25
C118	F27A	1-23	F943	B02C	1-7	I048	B15A	1-13	I138	E35C	1-21	I201	E02C	1-25
C119	F27C	1-23	F950	B38A	1-7	I049	A16D	1-13	I139	E36C	1-21	I202	E08A	1-25
C120	F28A	1-23	F951	B03B	1-7	I050	B13C	1-13	I140	E37A	1-21	I203	E08C	1-25
C121	F28C	1-23	F952	B15A	1-7	I051	D19A	1-13	I141	E35B	1-21	I204	E02D	1-25
C122	F29A	1-23	F953	B04B	1-7	I052	D19C	1-13	I142	E35D	1-21	I800	B34A	1-9
C123	F29C	1-23	F954	B05B	1-7	I053	D20G	1-13	I143	E36D	1-21	I801	B34B	1-9
C124	F30A	1-23	F955	B06B	1-7	I054	A12A	1-15	I144	E37C	1-21	I802	B34C	1-9
C125	F30C	1-23	F956	B07B	1-7	I055	D31B	1-15	I145	D29B	1-21	I803	B35A	1-9
C126	F31A	1-23	F957	B08B	1-7	I057	D31C	1-15	I146	D30B	1-21	I804	B35B	1-9
C127	F31C	1-23				I058	B37C	1-15	I147	D31D	1-21	I805	B35C	1-9
C128	F32A	1-23	I000	A16A	1-11	I059	B37D	1-15	I148	D32B	1-21	I806	B37A	1-9
C129	F32C	1-23	I001	A15A	1-11	I060	D33A	1-15	I149	D33C	1-21	I807	B36B	1-9
C130	F33A	1-23	I002	A16B	1-11	I061	C07B	1-15						
C131	F33C	1-23	I003	A16C	1-11	I062	C08B	1-15						
C132	F34A	1-23	I004	C35C	1-11	I063	E18B	1-15						

SYMBOL LIST CONTINUED

I808	B37B	1-9	I947	B15C	1-9	K087	C42B	1-15	L201	E09C	1-25	S012	B11A	1-17
I809	B37C	1-9	I948	B14D	1-9	K088	C40A	1-15	L202	E11C	1-25	S013	B11B	1-17
I810	B38B	1-9				K089	C40C	1-15	L203	E11A	1-25	S014	A08A	1-17
I811	B38C	1-9	K000	A01A	1-11	K090	C42C	1-15	L204	E10A	1-25	S015	A08C	1-17
I812	B16A	1-9	K001	A01C	1-11	K091	C42D	1-15	L205	E10C	1-25			
I813	B16b	1-9	K002	B01A	1-11	K096	C36A	1-13	L206	E13A	1-25	X001	E08	1-11
I814	B16C	1-9	K003	B01C	1-11	K097	C36C	1-13	L207	E13C	1-25			
I815	B16D	1-9	K004	B02A	1-11	K098	C37A	1-13				Y000	B05	1-11
I816	B17A	1-9	K005	B02C	1-11	K099	C37C	1-13	M100	B39A	1-15	Y001	C01	1-11
I817	B17B	1-9	K010	D01A	1-11	K100	D35A	1-19	M101	B39C	1-15	Y002	B05	1-11
I818	B17C	1-9	K011	D01C	1-11	K101	D35C	1-19	M102	B40A	1-15	Y003	D07	1-11
I819	B17D	1-9	K012	D02A	1-11	K102	D36A	1-19	M103	B40C	1-15	Y004	D07	1-11
I820	B18A	1-9	K013	D02C	1-11	K103	D36B	1-19	M104	B41A	1-15	Y005	D07	1-11
I821	B18B	1-9	K014	D03A	1-11	K104	D37A	1-19	M105	B41C	1-15	Y006	C01	1-15
I822	B18C	1-9	K015	D03C	1-11	K105	D37C	1-19	M200	E12A	1-25	Y007	C02	1-15
I823	B18D	1-9	K016	D04A	1-11	K106	D36C	1-19	M201	E12A	1-25	Y008	C02	1-15
I824	B19A	1-9	K017	D04C	1-11	K107	D36D	1-19	M202	E14A	1-25	Y010	C01	1-15
I825	B19B	1-9	K018	D05A	1-11	K108	E39A	1-19	M203	E14C	1-25	Y011	D07	1-15
I826	B19C	1-9	K019	D05C	1-11	K109	E39C	1-19				Y012	D07	1-15
I827	B19D	1-9	K020	D08A	1-11	K110	E40A	1-19	O000	B20A	1-13	Y013	D07	1-15
I828	B20A	1-9	K021	D08C	1-11	K111	E40B	1-19	O001	B20C	1-13	Y014	D07	1-15
I829	B20B	1-9	K042	B07A	1-15	K112	E41A	1-19	O002	B21A	1-13	Y015	D07	1-15
I830	B20C	1-9	K043	B07C	1-15	K113	E41C	1-19	O003	B21C	1-13	Y016	B05	1-17
I831	B20D	1-9	K044	B08A	1-15	K114	E40C	1-19	O004	B22A	1-13	Y017	A09B	1-17
I832	B21A	1-9	K045	B08C	1-15	K115	E40D	1-19	O005	B22C	1-13	Y020	B05	1-19
I833	B21B	1-9	K046	B09A	1-15	K116	E42A	1-19	O006	B23A	1-13	Y021	C02	1-15
I834	B21C	1-9	K047	B09C	1-15	K117	E42C	1-19	O007	B23C	1-13	Y022	C01	1-15
I835	B21D	1-9	K048	B10A	1-15	K118	C41C	1-19	O008	B24A	1-13	Y023	C02	1-15
I900	B22A	1-7	K049	B10C	1-15	K119	C41D	1-19	O009	B24C	1-13	Y024	C01	1-15
I901	B22C	1-7	K050	C03A	1-15	K120	D42A	1-19	O010	B25A	1-13	Y025	C02	1-13
I902	B23A	1-7	K051	C03C	1-15	K121	D42C	1-19	O011	B25C	1-13	Y026	C01	1-11
I903	B23C	1-7	K052	C04A	1-15	K130	E38A	1-23	O012	B26A	1-13	Y027	C01	1-15
I904	B24A	1-7	K053	C04C	1-15	K131	E38C	1-23	O013	B26C	1-13	Y028	C01	1-15
I905	B24C	1-7	K054	C05A	1-15	K200	E01C	1-25	O014	B27A	1-13	Y029	D07	1-17
I906	B25A	1-7	K055	C05C	1-15	K201	E01C	1-25	O015	B27C	1-13	Y030	B05-1	1-17
I907	B25C	1-7	K056	C06A	1-15	K203	E07C	1-25	O016	B28A	1-13	Y200	E04	1-25
I908	B26A	1-7	K057	C06C	1-15	K900	A30A	1-7	O017	B28C	1-13	Y201	E03	1-25
I909	B27B	1-7	K060	C09A	1-15	K901	A30C	1-7	O018	B29A	1-13	Y202	E03	1-25
I910	B28B	1-7	K061	C09C	1-15	K902	B09A	1-7	O019	B29C	1-13	Y204	E06	1-25
I911	B29B	1-7	K062	C10A	1-15	K903	B09C	1-7	O020	B30A	1-13	Y205	E06	1-25
I912	A17C	1-7	K063	C10C	1-15	K904	B10A	1-7	O021	B30C	1-13	Y206	E03	1-25
I913	B26C	1-7	K064	C11A	1-15	K905	B10C	1-7	O022	B31A	1-13	Y207	E03	1-25
I914	B30B	1-7	K065	C11C	1-15	K906	B11A	1-7	O023	B31C	1-13	Y900	B42	1-9
I915	B31B	1-7	K066	C12A	1-15	K907	B11C	1-7				Y901	B42	1-9
I916	B32D	1-7	K067	C12C	1-15	K908	B12A	1-7	S000	A02A	1-17	Y902	B42	1-9
I917	B33C	1-7	K068	C13A	1-15	K909	B12C	1-7	S001	A02C	1-17	Y903	B42	1-9
I918	A22D	1-7	K069	C13C	1-15	K910	B39A	1-9	S002	A03A	1-17	Y904	B42-3	1-7
I919	B32B	1-7	K070	C14A	1-15	K911	B39C	1-9	S003	B11C	1-17			
I921	A24B	1-7	K071	C14C	1-15	K912	B40A	1-9	S004	A04A	1-17	F935	A22C	1-7
I926	A28C	1-7	K072	C15A	1-15	K913	B40B	1-9	S005	A04C	1-17	F936	A17C	1-7
I927	A29B	1-7	K073	C15C	1-15	K914	B41A	1-9	S006	A05A	1-17	F937	B32C	1-7
I930	A31B	1-7	K074	C16A	1-15	K915	B41C	1-9	S007	A05C	1-17			
I931	A32B	1-7	K075	C16C	1-15	K916	B40C	1-9	S008	A06A	1-17			
I932	A33B	1-7	K080	C38A	1-15	K917	B40D	1-9	S009	A06C	1-17			
I933	A34B	1-7	K081	C38C	1-15				S010	A07A	1-17			
I934	B33A	1-7	K082	C41A	1-15	L000	B38A	1-17	S011	A07C	1-17			
I940	B13A	1-9	K083	C41B	1-15	L001	B38B	1-17						
I942	B13B	1-9	K084	C39A	1-15	L002	B38C	1-17						
I944	B13C	1-9	K085	C39C	1-15	L101	B42C	1-11						
I946	B14C	1-9	K086	C42A	1-15	L200	E09A	1-25						

Rev. A

BLOCK DIAGRAM

The Control Data 6675 interfaces the Control Data 6000 Series with up to four DATA-PHONE* Data Sets. The DCA uses 12-bit parallel words to communicate with the computer; communication with the data set is by serial bits.

Each DSC in the 6675 communicates with a similar DSC at a remote station. A leased transmission line connects the stations through terminating data sets. The DSC operates in half-duplex to send data, but utilizes the full-duplex capability of the transmission line for response and control signals. When one DSC is in the Transmit mode, the other must be in the Receive mode; to exchange data in the opposite direction, both DSC's must reverse modes.

TRANSMIT MODE

When the local computer desires to transmit data, the external function (EXF) code translated by the multiplexer selects the desired DSC. The DSC originates the Send Request signal and the local data set responds with a Clear-to-Send signal. The DSC then sends out a sync word (4257) to the receiving controller. The receiving DSC detects the sync word and returns a 3-bit response (100_2 code). This response disables the Sync Word Not Acknowledged status bit.

When the DSC is selected to transmit and the Input/Output (I/O) register is empty, the DSC enables the Transmit and Empty status-all bit. The status-all bit Transmit and Empty is recognized by the computer, enabling it to output a data word to the DSC via the multiplexer. The data word is loaded into the DSC's I/O register. Before processing this data word the DSC gates a 12-bit sync word out to the data set. After transfer of the sync word (approximately 295 usec) the data word in the I/O register transfers to the Assembly/Disassembly (A/D) register.

The Serial Clock Transmit (SCT) pulses from the data set enable the A/D counter to gate each data bit in the A/D register onto the line serially, highest order bit first. Each clock pulse (24.8 usec) enables one serial data bit.

Each bit of serial data gated out on the Send Data (SD) line is also gated the Cyclic Encoder/Decoder (E/D). This enables the E/D circuitry to generate a code word which is used by the data set controller at the remote site for transmission error checking.

Between transmission of each data word the computer samples status-all. Whenever the status-all bits for the selected DSC indicate a Transmit and Empty (I/O empty) condition, the computer outputs another data word.

After the last word of the data block is sent out as serial data, the DSC automatically sends out the Cyclic code word. Upon completion of code word transmission, the Transmit operation terminates, and the Clear-to-Send and Send Request signals drop.

RECEIVE MODE

To receive data from a remote station the computer outputs an external function code that is translated by the multiplexer. The multiplexer then selects the designated DSC to receive.

The selected DSC monitors idle pattern (0111_2) transmission and waits for a sync word (4257). The local data set is providing a Carrier On/Off signal all this time. When the DSC recognizes a sync word, it enables the receive circuitry and sends a 3-bit response (100 code) to the remote station. Serial data received from the remote station is gated to the A/D register and to the Cyclic E/D. The A/D register assembles data into 12 bit words and transfers it to the I/O register. The Serial Clock Receive (SCR) pulses from the data set enable the A/D counter to assemble data words.

If the I/O register contains a data word, the status-all bits for the selected DSC indicate a Full and Receive condition. When the computer samples status-all and detects this condition, it inputs the data word contained in the I/O register.

After the last data word transfers to the computer, the next A/O → I/O transfer loads the code word from the remote DSC into the I/O register. The code word also enters by Cyclic E/D and drives it to zero. The cyclic code error status bit sets if it is not driven to zero.

When the code word is loaded in the I/O register and data block transmission is complete, the Receive operation terminates.

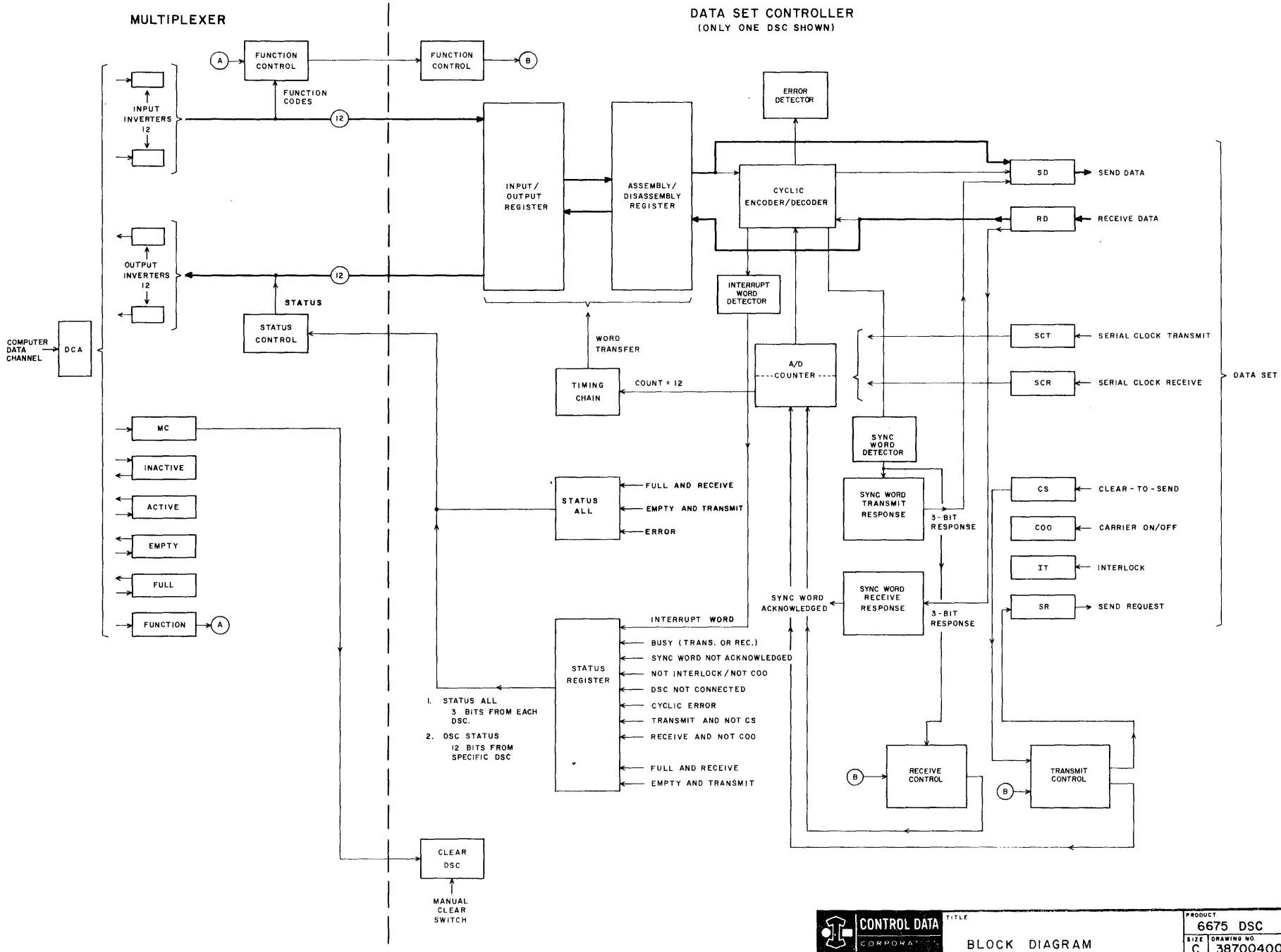
INTERRUPT

When the DSC is not in the Receive mode or the Transmit mode, it constantly monitors idle bit pattern on the Receive Data (RD) line. If an interrupt word (7622) is detected, the Interrupt word Received status bit sets.

STATUS-ALL

The computer samples the status-all word until it detects that a DSC requires service. The multiplexer assembles the status-all word, three bits from each DSC. The three bits from each DSC indicate whether that DSC is in the Transmit mode and the I/O register is empty, if the DSC is in Receive mode and the I/O register is full, or if an error is detected.

*Registered trademark of Bell Telephone System.



CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION

TITLE: BLOCK DIAGRAM

PRODUCT	
6675 DSC	
SIZE: C	DRAWING NO: 38700400
REV	
SHEET: 3	1-5

INPUT LINES

The input lines receive data and function codes from the DCA. Toggle switches S^0, S^1, and S^2 permit changing bits 9 through 11 of the EXF code. The switches assign the 6675 an equipment number on the Data Channel.

MULTIPLEXER CLEAR

Activating the multiplexer Clear circuit clears selected circuits in the multiplexer and generates a clear to the DSC's. An S5XX EXF code activates the Clear circuit if the Function signal from the DCA is On. A Master Clear signal from the DCA also activates the multiplexer Clear circuit.

CONTROLLER SELECT

The controller select inverters translate the DSC designator portion of the EXF code. The controller select inverters monitor bits 0 through 2 of the input lines.

CONTROL SIGNALS FROM DCA

The control signals from the DCA are designated in the same manner as standard 6000 Series I/O control signals. The 6600 Computer I/O Specifications manual, CDC publication number 60045100, defines these control signals.

TABLE 1-1. DCA CONTROL SIGNALS

SIGNAL	DEFINITION
Master Clear	A static "1" signal clears both the multiplexer and the DSC's.
Active	A static "1" signal is produced when the data channel is activated.
Inactive	A static "1" signal indicates that the computer has deactivated the data channel.
Full	A static "1" accompanies each word of output data. The signal indicates that output data is present on the lines.
Empty	A static "1" signal indicates that the DCA has accepted an input word.
Function	A static "1" signal is produced on the line when an EXF code is present on the data lines for examination and translation by the 6675.

FUNCTION SELECT

The function select inverters translate the function portion of the EXF code. These inverters monitor bits 3 through 5 of the input lines. The 6675 codes are listed on the following page.

TABLE 1-2. EXTERNAL FUNCTION CODES

DEFINITION	CODE	NOTES
Request Status-All	S504	Enables three status-all bits from each of the 4 DSC's.
Request Status	S51N	Enables a status word (12 bits) from DSC "N". "N" represents the number assigned to the selected DSC.
Select	S52N	Selects DSC "N".
Clear	S53N	Clears DSC "N".
Select Transmit	S54N	Selects DSC "N" for data transmission.
Select Receive	S55N	Selects DSC "N" to receive data from the Data Set for transfer to the computer.
Clear Interrupt Word Received Status bit	S56N	Clears Interrupt Word Received FF and status bit 2^0 in controller "N" (interrupt word = 7622).

STATUS

The Request Status circuits consist of a Request Status-All circuit and the individual DSC Request Status flip-flops.

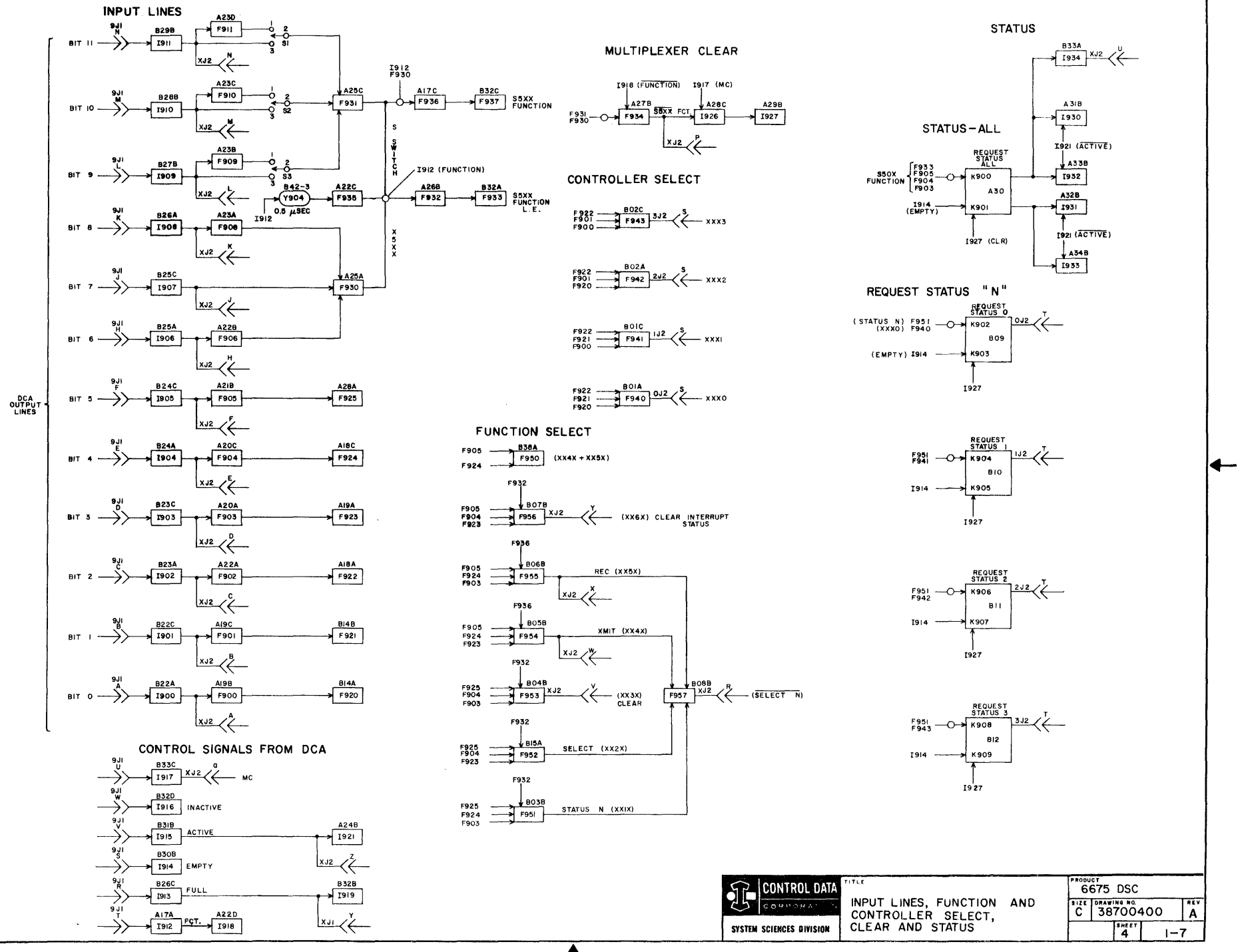
REQUEST STATUS-ALL

The Request Status-All FF sets when the 6675 receives an S504 EXF code. With this FF set, terms I931 and I933 enable three status-all bits from each DSC to the multiplexer output lines and terms I930 and I932 lock out the data inputs to the multiplexer output lines. When this flip-flop is clear, the status inputs are locked out and the data inputs are enabled if the active signal is up.

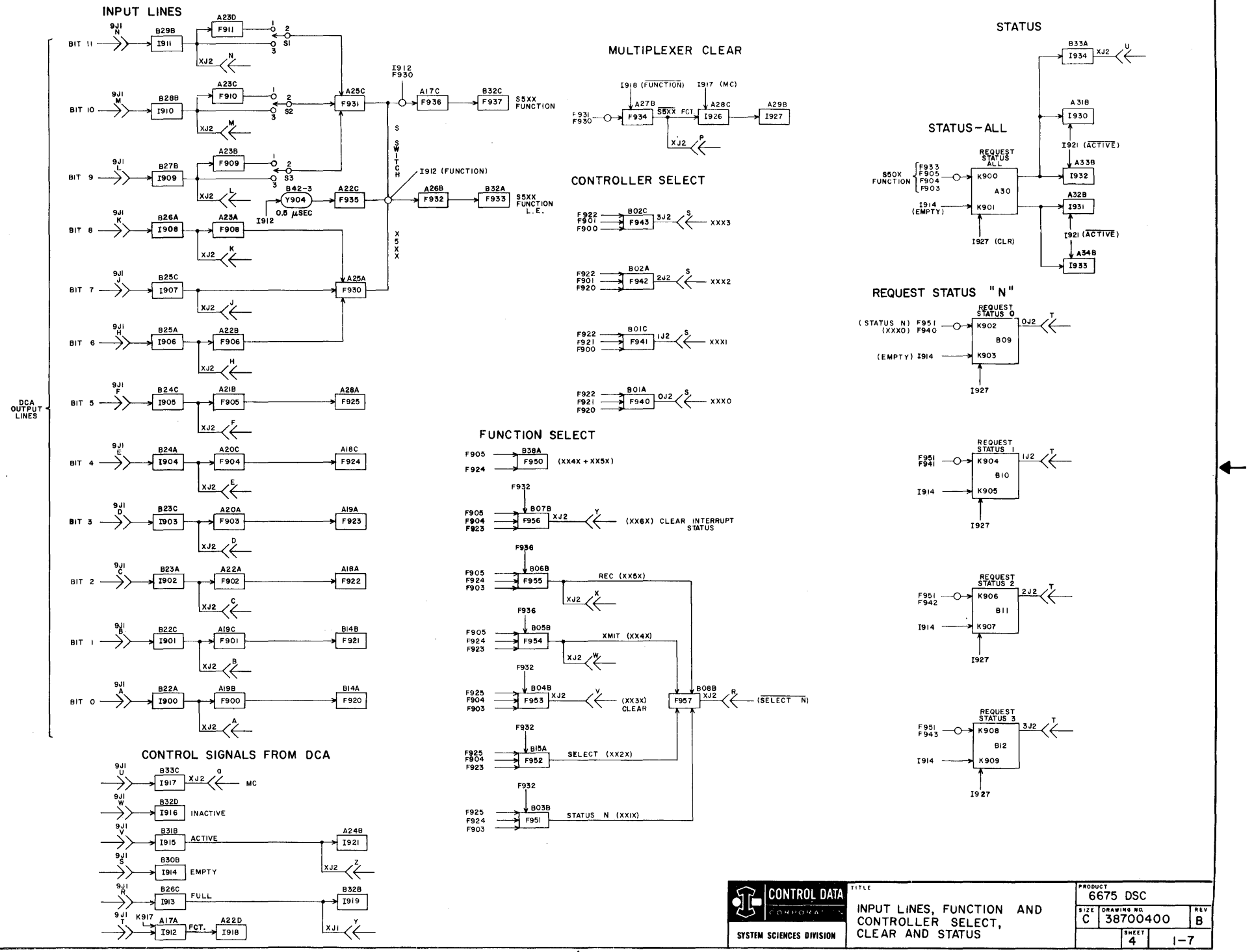
Term I921 has a "0" output when the Active signal from the DCA is On (data channel is activated). When the Active signal drops, I921 has a "1" output and I930-I933 disable the status and data gates in the multiplexer output lines. When the computer accepts the status-all word, the DCA returns an Empty signal. This clears the Request Status-All FF.

REQUEST STATUS N

An individual Request Status FF sets when the 6675 receives an S51N EXF code. ("N" represents the number assigned to the selected DSC.) Setting a Request Status FF enables the status word from the selected DSC to the multiplexer output lines. When the computer accepts the status word, the Empty signal returned by the DCA enables I914 to clear the Request Status "N" FF.



CONTROL DATA CORPORATION SYSTEM SCIENCES DIVISION	TITLE INPUT LINES, FUNCTION AND CONTROLLER SELECT, CLEAR AND STATUS	PRODUCT 6675 DSC	
		SIZE C	DRAWING NO. 38700400 REV A
			SHEET 4 1-7



CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION

TITLE: INPUT LINES, FUNCTION AND CONTROLLER SELECT, CLEAR AND STATUS

PRODUCT		
6675 DSC		
SIZE C	DRAWING NO. 38700400	REV B
	SHEET 4	1-7

OUTPUT LINES

The output lines transfer data and status information from the four DSC's, through the multiplexer, to the DCA. The I932 or I930 gates enable data to the output inverters; the I931 or I933 gates enable status-all information. When one set of gates is enabled, the other set is disabled. Thus, a word gated to the DCA is either data or status-all information. Terms I930 - I931 are in the Status-All circuit shown on page 1-7.

The four gates to the output inverter of bit 7 indicate whether the selected DSC is disconnected physically or is in the Test mode during a Status operation. The K90- term enables the gate from the selected DSC for a status response (page 1-7).

COMMUNICATION SIGNALS FROM CONTROLLER

The I94- inverters (page 1-17) receive communication signals from the individual DSC's. These communication signals permit the multiplexer to send control signals to the DCA.

For example, if DSC #2 is full and selected to receive, an S522 EXF code (Select DSC # 2) enables the gate to I116 (page 1-17). This causes I942 to have a "1" output if the Active signal from the DCA is On.

CONTROL SIGNALS TO DCA

The control signals to the DCA are: Full, Empty, Active, and Inactive. These static signals are developed as follows:

FULL
The Full signal to the DCA indicates that the status/data output lines of the selected DSC contain a status or data word.

The Full FF sets when a data word is loaded in the I/O register of the selected DSC or a status or status-all word is requested. In either case, the Active signal from the DCA must be On.

An Empty signal from the DCA clears the Full FF (Full signal turns Off). The DCA turns on the Empty signal when it accepts the input word from the 6675. A Master Clear signal or an S5XX EXF code also clears the Full FF.

EMPTY
The Empty signal to the DCA indicates that the 6675 has accepted the data word from the DCA.

The Empty FF sets when the I/O register of the selected DSC is empty and the Full signal from the DCA is On. The Full signal from the DCA indicates that the DCA has placed an output word on the lines.

The Empty FF clears when the Full signal from DCA is turned Off.

ACTIVE
The Active signal to DCA indicates that 6675 is prepared to accept data.

The Active FF sets when one of the DSC's has been selected and the DCA Active signal is On, or when a status or status-all word is requested, or the DCA Active signal is On.

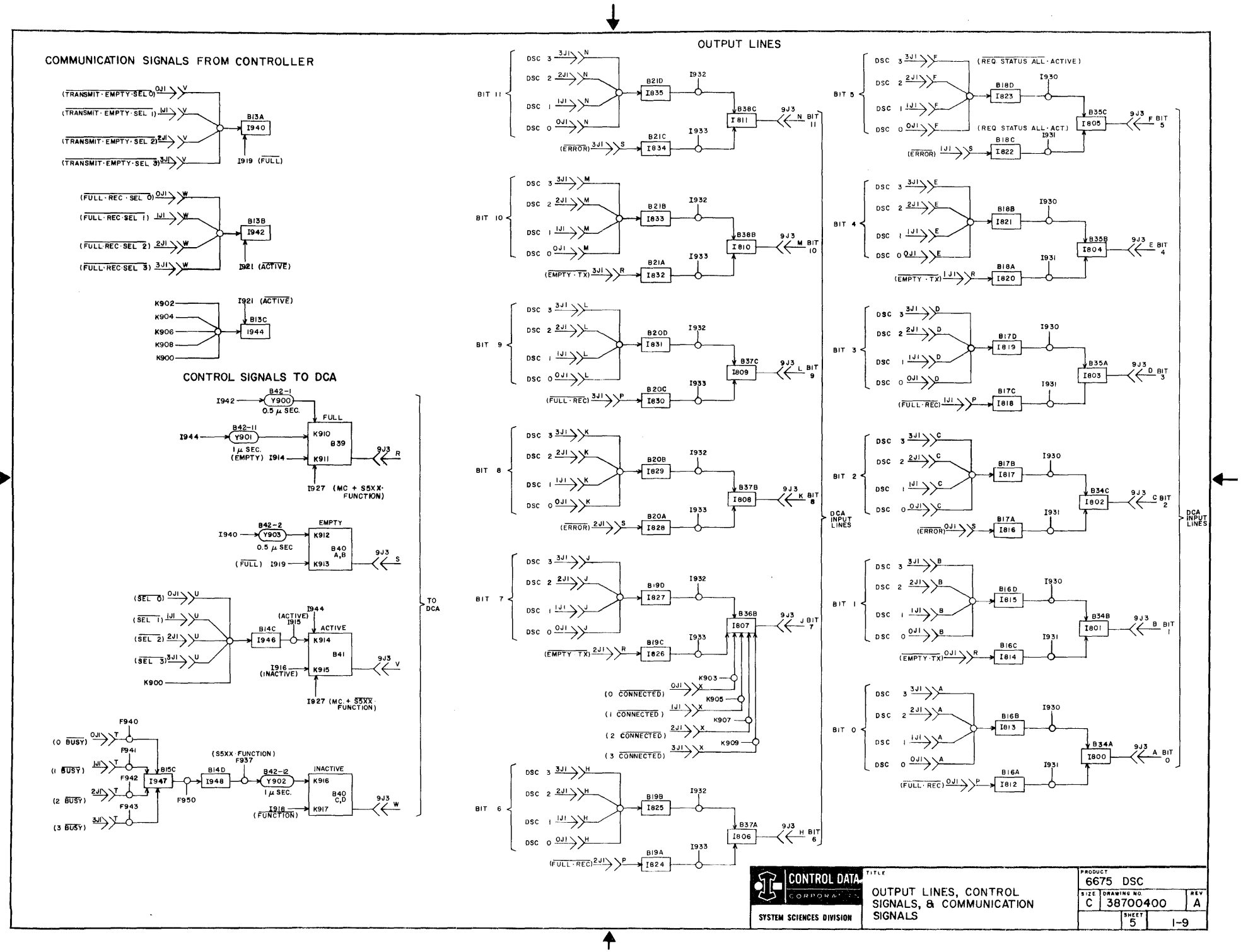
The Active FF clears upon receipt of an Inactive signal from DCA or by a multiplexer clear.

INACTIVE
The Inactive signal to DCA indicates that a DSC is selected and not busy in response to an EXF select code.

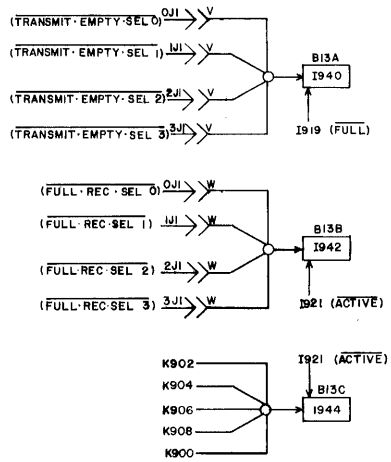
The Inactive FF sets upon receipt of an S5XX EXF select code. This code selects an individual DSC if it is not busy.

The Inactive FF clears when the Function signal from the DCA is turned Off.

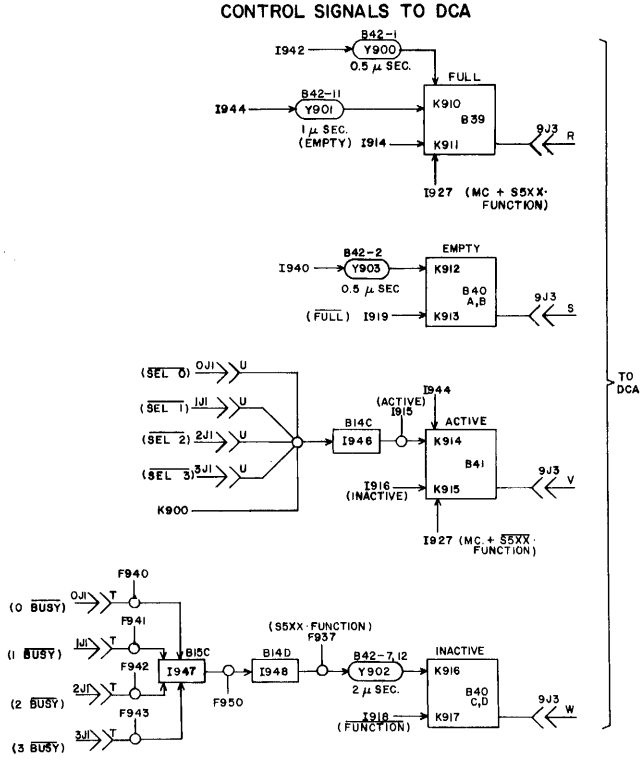
TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION
F940	B01A	1-7	XXX0	I919	B32B	1-7	$\overline{\text{Full}}$	K902	B09A	1-7	$\overline{\text{Request Status 0}}$
F941	B01C	1-7	XXX1	I921	A24B	1-7	$\overline{\text{Active}}$	K903	B09C	1-7	Request Status 0
F942	B02A	1-7	XXX2	I927	A29B	1-7	(MC) + ($\overline{\text{S5XX}}$) (FCT)	K904	B10A	1-7	$\overline{\text{Request Status 1}}$
F943	B02C	1-7	XXX3	I930	A31B	1-7	($\overline{\text{Req. Status All}}$) (Active)	K905	B10C	1-7	Request Status 1
F950	B38A	1-7	(XX4X) + (XX5X)	I931	A32B	1-7	(Req. Status All) (Active)	K906	B11A	1-7	$\overline{\text{Request Status 2}}$
I915	B31B	1-7	Active	I932	A33B	1-7	($\overline{\text{Req. Status All}}$) (Active)	K907	B11C	1-7	Request Status 2
I916	B32D	1-7	Inactive	I933	A34B	1-7	(Req. Status All) (Active)	K908	B12A	1-7	$\overline{\text{Request Status 3}}$
I918	A22D	1-7	$\overline{\text{Function}}$	K900	A30A	1-7	$\overline{\text{Request Status All}}$	K909	B12C	1-7	Request Status 3


COMMUNICATION SIGNALS FROM CONTROLLER
(TRANSMIT·EMPTY·SEL 0) 0J1 V
(TRANSMIT·EMPTY·SEL 1) 1J1 V
(TRANSMIT·EMPTY·SEL 2) 2J1 V
(TRANSMIT·EMPTY·SEL 3) 3J1 V
B13A I940
I919 (FULL)
(FULL·REC·SEL 0) 0J1 W
(FULL·REC·SEL 1) 1J1 W
(FULL·REC·SEL 2) 2J1 W
(FULL·REC·SEL 3) 3J1 W
B13B I942
I921 (ACTIVE)
K902 K904 K906 K908 K900
I921 (ACTIVE)
B13C I944
CONTROL SIGNALS TO DCA
I942 B42-1 Y900 0.5 μ SEC. FULL
I944 B42-11 Y901 1 μ SEC. (EMPTY) I914
K910 K911 B39 9J3 R
I927 (MC + S5XX· FUNCTION)
I940 B42-2 Y903 0.5 μ SEC (FULL) I919
EMPTY K912 K913 B40 A,B 9J3 S
(SEL 0) 0J1 U
(SEL 1) 1J1 U
(SEL 2) 2J1 U
(SEL 3) 3J1 U
K900
B14C I946
(ACTIVE) I915
I944
ACTIVE K914 K915 B41 9J3 V
I916 (INACTIVE)
I927 (MC + S5XX· FUNCTION)
F940
(0 BUSY) 0J1 T
F941
(1 BUSY) 1J1 T
F942
(2 BUSY) 2J1 T
F943
(3 BUSY) 3J1 T
B15C I947
F950
B14D I948
(S5XX·FUNCTION) F937
B42-12 Y902 1 μ SEC.
I918 (FUNCTION)
INACTIVE K916 K917 B40 C,D 9J3 W
TO DCA
OUTPUT LINES
BIT 11
DSC 3 3J1 N
DSC 2 2J1 N
DSC 1 1J1 N
DSC 0 0J1 N
B21D I835 I932
(ERROR) 3J1 S
B21C I834 I933
B38C I811 9J3 N BIT 11
BIT 10
DSC 3 3J1 M
DSC 2 2J1 M
DSC 1 1J1 M
DSC 0 0J1 M
B21B I833 I932
(EMPTY·TX) 3J1 R
B21A I832 I933
B38B I810 9J3 M BIT 10
BIT 9
DSC 3 3J1 L
DSC 2 2J1 L
DSC 1 1J1 L
DSC 0 0J1 L
B20D I831 I932
(FULL·REC) 3J1 P
B20C I830 I933
B37C I809 9J3 L BIT 9
BIT 8
DSC 3 3J1 K
DSC 2 2J1 K
DSC 1 1J1 K
DSC 0 0J1 K
B20B I829 I932
(ERROR) 2J1 S
B20A I828 I933
B37B I808 9J3 K BIT 8
BIT 7
DSC 3 3J1 J
DSC 2 2J1 J
DSC 1 1J1 J
DSC 0 0J1 J
B19D I827 I932
(EMPTY·TX) 2J1 R
B19C I826 I933
B36B I807 9J3 J BIT 7
(0 CONNECTED) 0J1 X K903
(1 CONNECTED) 1J1 X K905
(2 CONNECTED) 2J1 X K907
(3 CONNECTED) 3J1 X K909
BIT 6
DSC 3 3J1 H
DSC 2 2J1 H
DSC 1 1J1 H
DSC 0 0J1 H
B19B I825 I932
(FULL·REC) 2J1 P
B19A I824 I933
B37A I806 9J3 H BIT 6
DCA INPUT LINES
BIT 5
DSC 3 3J1 F
DSC 2 2J1 F
DSC 1 1J1 F
DSC 0 0J1 F
(REQ STATUS ALL·ACTIVE)
B18D I823 I930
(REQ STATUS ALL·ACT)
B18C I822 I931
(ERROR) 1J1 S
B35C I805 9J3 F BIT 5
BIT 4
DSC 3 3J1 E
DSC 2 2J1 E
DSC 1 1J1 E
DSC 0 0J1 E
B18B I821 I930
(EMPTY·TX) 1J1 R
B18A I820 I931
B35B I804 9J3 E BIT 4
BIT 3
DSC 3 3J1 D
DSC 2 2J1 D
DSC 1 1J1 D
DSC 0 0J1 D
B17D I819 I930
(FULL·REC) 1J1 P
B17C I818 I931
B35A I803 9J3 D BIT 3
BIT 2
DSC 3 3J1 C
DSC 2 2J1 C
DSC 1 1J1 C
DSC 0 0J1 C
B17B I817 I930
(ERROR) 0J1 S
B17A I816 I931
B34C I802 9J3 C BIT 2
BIT 1
DSC 3 3J1 B
DSC 2 2J1 B
DSC 1 1J1 B
DSC 0 0J1 B
B16D I815 I930
(EMPTY·TX) 0J1 R
B16C I814 I931
B34B I801 9J3 B BIT 1
BIT 0
DSC 3 3J1 A
DSC 2 2J1 A
DSC 1 1J1 A
DSC 0 0J1 A
B16B I813 I930
(FULL·REC) 0J1 P
B16A I812 I931
B34A I800 9J3 A BIT 0
DCA INPUT LINES
CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION
TITLE
OUTPUT LINES, CONTROL SIGNALS, & COMMUNICATION SIGNALS
PRODUCT 6675 DSC
SIZE C
DRAWING NO. 38700400
REV A
SHEET 5
1-9

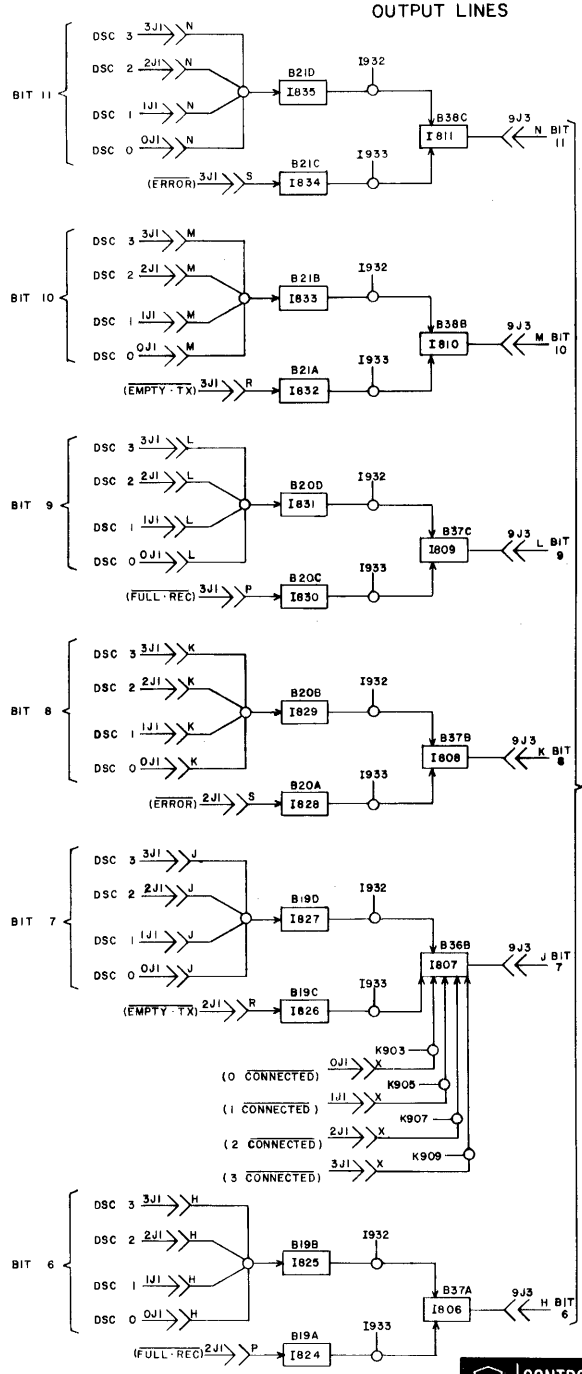
COMMUNICATION SIGNALS FROM CONTROLLER



CONTROL SIGNALS TO DCA



OUTPUT LINES



CONTROL DATA
SYSTEM SCIENCES DIVISION

TITLE: OUTPUT LINES, CONTROL SIGNALS, & COMMUNICATION SIGNALS

PRODUCT		
6675 DSC		
SIZE	DRAWING NO.	REV
C	38700400	B
	SHEET 5	1-9

TRANSMIT CONTROL

The Transmit Control circuit enables the various transmit functions (Transmit Sync Word, Transmit Data, and Transmit Code Word) during Transmit mode. The circuit also enables the transmit response during the Receive mode.

An EXF code received by the multiplexer sets the Select Transmit FF if the DSC is not busy or in the Test mode. Positioning the Transmit Test switch to any of the four test positions also sets the flip-flop. Setting the Select Transmit FF enables the Transmit Sync FF and the Transmit FF. When the Transmit Sync FF sets, I007 forces the sync word into the E/D shift register. I007 has a "1" output for 1 usec and clears. The No Data Flow circuit and E/D Control (page 1-23) enable serial transmission of the sync word. When the A/D counter equals 12 (page 1-15) the Transmit Sync FF clears. (See transmit timing, page 1-26).

The Transmit FF must be set to send out the sync word, transmit data, and the code word. The transmit response (3 bit code = 100) is sent out when K121/122 sets. The latter occurs during a Receive operation and utilizes the full duplex capability of the transmission line.

When the Transmit FF sets, L101 sends a Send Request (SR) signal to the remote data set. Turning on the SR signal notifies the data set that the DSC is ready to transmit data. The data set responds with a CS signal.

The Transmit Code FF sets when the multiplexer completes the data transfer and the I/O register is empty. The No Data Flow circuit activates when the FF sets and enables the code word (page 1-23).

The Complete Code FF is used if a 24-bit code is used. When using the 12-bit code that is described in this text, the Complete Code FF is bypassed. The Clear Transmit FF sets when the code word is transmitted. The Clear Transmit FF clears when the Transmit FF clears.

NO DATA FLOW

This circuit enables the code or sync word when the respective Transmit flip-flop is set.

RECEIVE CONTROL

The Receive Control circuit provides the enabling pulses used during the Receive mode. The Select Receive FF sets when an S55X EXF code selects the DSC to receive and the DSC is not busy or in the Test mode. Receipt of the sync word from the transmitting data set and activation of the carrier signal (COO) enable the gate to the Receive FF. Setting the Receive FF clears the Select Receive FF. (See receive timing, page 1-27). When the computer has accepted the entire block of data, the last A/D → I/O transfer loads the cyclic code word into the I/O register and the Receive FF clears.

CLEAR CIRCUIT

CONTROLLER CLEAR: This circuit clears all major circuits in the DSC. The circuit is activated by the manual pushbutton on the DSC chassis, by a clear (S53X) EXF code, or by a Master Clear signal when the DSC in not in the Test mode.
SELECT CONTROLLER CLEAR: This circuit clears the Select N flip-flop. The circuit is activated by a controller clear, by a request status-all, or by functioning another device on the data channel. A DSC request for a status word disables the I013 function.

SELECT

The Select "N" FF must be set before the corresponding DSC can perform operations in the Transmit or Receive mode. The Select "N" FF sets when the multiplexer detects an S52X EXF code, where "2" is translated as the select function and "X" as the respective DSC (0, 1, 2, or 3). The Select "N" FF clears when the computer selects another DSC or upon receipt of a signal from the Controller Clear circuit (I013).

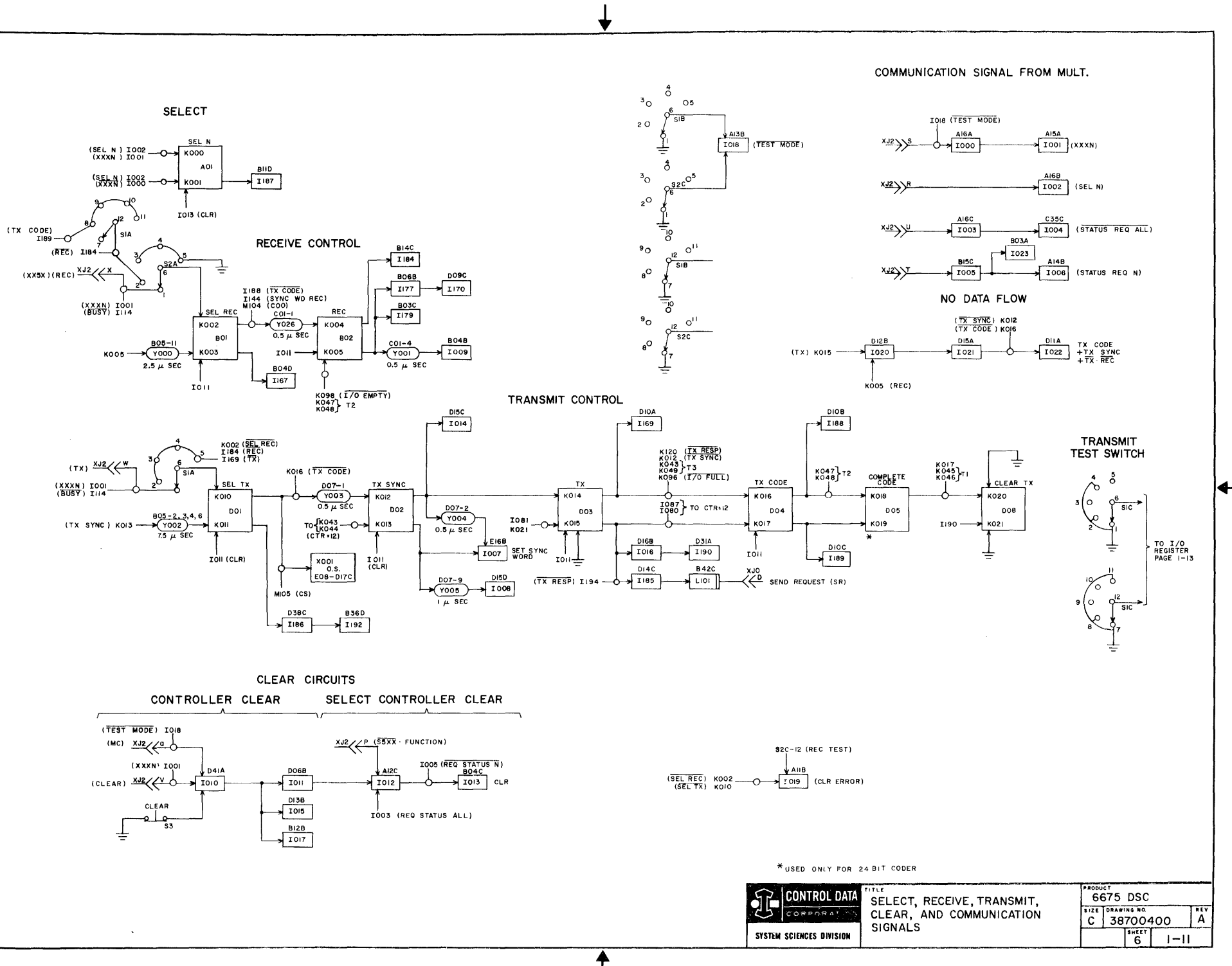
COMMUNICATION SIGNALS FROM MULTIPLEXER

Communication signals from the multiplexer select the individual DSC's (page 1-7). These signals also enable status or status-all responses.

TERM	LOC'N	PAGE	DESCRIPTION
I054	A12A	1-15	$\overline{SCT}$
I080	D22B	1-15	XX00 } A/D Counter Translation
I087	E25A	1-15	11XX }
I114	A15C	1-17	$\overline{Busy}$
I128	D09B	1-19	Count = 3
I144	E37C	1-21	Sync Wd Rec
K043	B07C	1-15	Timing Chain

TERM	LOC'N	PAGE	DESCRIPTION
K044	B08A	1-15	} Timing Chain
K045	B08C	1-15	
K046	B09A	1-15	
K047	B09C	1-15	
K048	B10A	1-15	
K049	B10C	1-15	
K096	C36A	1-13	I/O Full For TX

TERM	LOC'N	PAGE	DESCRIPTION
K098	C37A	1-13	$\overline{I/O\ Empty\ For\ Rec}$
K120	D42A	1-19	$\overline{TX\ Resp.}$
K121	D42C	1-19	TX Resp.
M100	B39A	1-15	SCT
M104	B41A	1-15	COO
M105	B41C	1-15	CS


SELECT
SEL N
K000
A01
K001
(SEL N) I002
(XXXN) I001
(SEL N) I002
(XXXN) I000
B11D
I187
I013 (CLR)
(TX CODE) I189
(REC) I184
S1A
RECEIVE CONTROL
(XX5X)(REC)
XJ2
X
(XXXN) I001
(BUSY) I114
S2A
SEL REC
K002
B01
K003
K005
B05-11
Y000
2.5 μ SEC
I011
B04D
I167
I188 (TX CODE)
I144 (SYNC WD REC)
M104 (COO)
C01-1
Y026
0.5 μ SEC
REC
K004
B02
K005
I011
K098 (I/O EMPTY)
K047
K048
T2
B14C
I184
B06B
I177
B03C
I179
C01-4
Y001
0.5 μ SEC
D09C
I170
B04B
I009
S1B
S2C
A13B
I018 (TEST MODE)
COMMUNICATION SIGNAL FROM MULT.
I018 (TEST MODE)
A16A
I000
A15A
I001
(XXXN)
XJ2
S
A16B
I002
(SEL N)
R
A16C
I003
C35C
I004
(STATUS REQ ALL)
U
B03A
I023
B15C
I005
A14B
I006
(STATUS REQ N)
T
NO DATA FLOW
(TX) K015
D12B
I020
D15A
I021
D11A
I022
TX CODE
+TX SYNC
+TX · REC
(TX SYNC) K012
(TX CODE) K016
K005 (REC)
TRANSMIT CONTROL
(TX)
XJ2
W
(XXXN) I001
(BUSY) I114
S1A
SEL TX
K010
D01
K011
I011 (CLR)
(TX SYNC) K013
B05-2, 3, 4, 6
Y002
7.5 μ SEC
K002 (SEL REC)
I184 (REC)
I169 (TX)
K016 (TX CODE)
D07-1
Y003
0.5 μ SEC
TX SYNC
K012
D02
K013
I011 (CLR)
TO K043 K044 (CTR÷12)
X001 O.S. E08-D17C
M105 (CS)
D38C
I186
B36D
I192
D15C
I014
D07-2
Y004
0.5 μ SEC
E16B
I007
SET SYNC WORD
D07-9
Y005
1 μ SEC
D15D
I008
I081
K021
TX
K014
D03
K015
I011
D10A
I169
K120 (TX RESP)
K012 (TX SYNC)
K043
K049
T3
K096 (I/O FULL)
I087
I080
TO CTR÷12
D16B
I016
D31A
I190
D14C
I185
B42C
L101
XJ0
D
SEND REQUEST (SR)
(TX RESP) I194
I011
TX CODE
K016
D04
K017
I011
D10B
I188
K047
K048
T2
D10C
I189
COMPLETE CODE
K018
D05
K019
*
K017
K045
K046
T1
I190
CLEAR TX
K020
D08
K021
TRANSMIT TEST SWITCH
SIC
SIC
TO I/O REGISTER PAGE 1-13
CLEAR CIRCUITS
CONTROLLER CLEAR
SELECT CONTROLLER CLEAR
(TEST MODE) I018
(MC) XJ2 a
(XXXN) I001
(CLEAR) XJ2 V
D41A
I010
CLEAR
S3
D06B
I011
D13B
I015
B12B
I017
XJ2 P (55XX · FUNCTION)
A12C
I012
I005 (REQ STATUS N)
B04C
I013
CLR
I003 (REQ STATUS ALL)
S2C-12 (REC TEST)
(SEL REC) K002
(SEL TX) K010
A11B
I019
(CLR ERROR)
* USED ONLY FOR 24 BIT CODER
CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION
TITLE
SELECT, RECEIVE, TRANSMIT, CLEAR, AND COMMUNICATION SIGNALS
PRODUCT
6675 DSC
SIZE C
DRAWING NO. 38700400
REV A
SHEET 6
1-11

INPUT/OUTPUT REGISTER

This 12-stage register holds input and output data to and from the DSC. The multiplexer gates transmit data into the I/O register; the A/D register gates receive data into the I/O register. Transmit data is gated out of the I/O to the A/D register. The I/O and A/D control enables the gates.

The SIC-12 or SIC-6 inputs to the set side of the FFs apply a forced input during the Test mode. The four Transmit Test switch positions (page 1-11) enable the following words:

Position 1	000 000 000 000
Position 2	111 111 111 111
Position 3	000 001 101 101
Position 4	111 110 010 010

I/O FULL FOR TRANSMIT FF
This FF indicates when data is transferred in and out of the I/O register during the Transmit mode.

During the Test mode, one-shot X001 enables the gate to the set side of the I/O Full for Transmit FF provided the Transmit Test switch is turned to any of the positions 1 through 4.

I/O EMPTY FOR RECEIVE FF
This FF indicates the transfer of data into and out of the I/O register during Receive mode.

ASSEMBLY/DISASSEMBLY REGISTER

The Assembly/Disassembly (A/D) register holds data that is counted out serially by the Disassembly circuit during the Transmit mode. In the Receive mode, counter translations (page 1-15) gate serial data received by the DSC into A/D register FFs. Inverters I158 and I159 represent the serial data received (page 1-23).

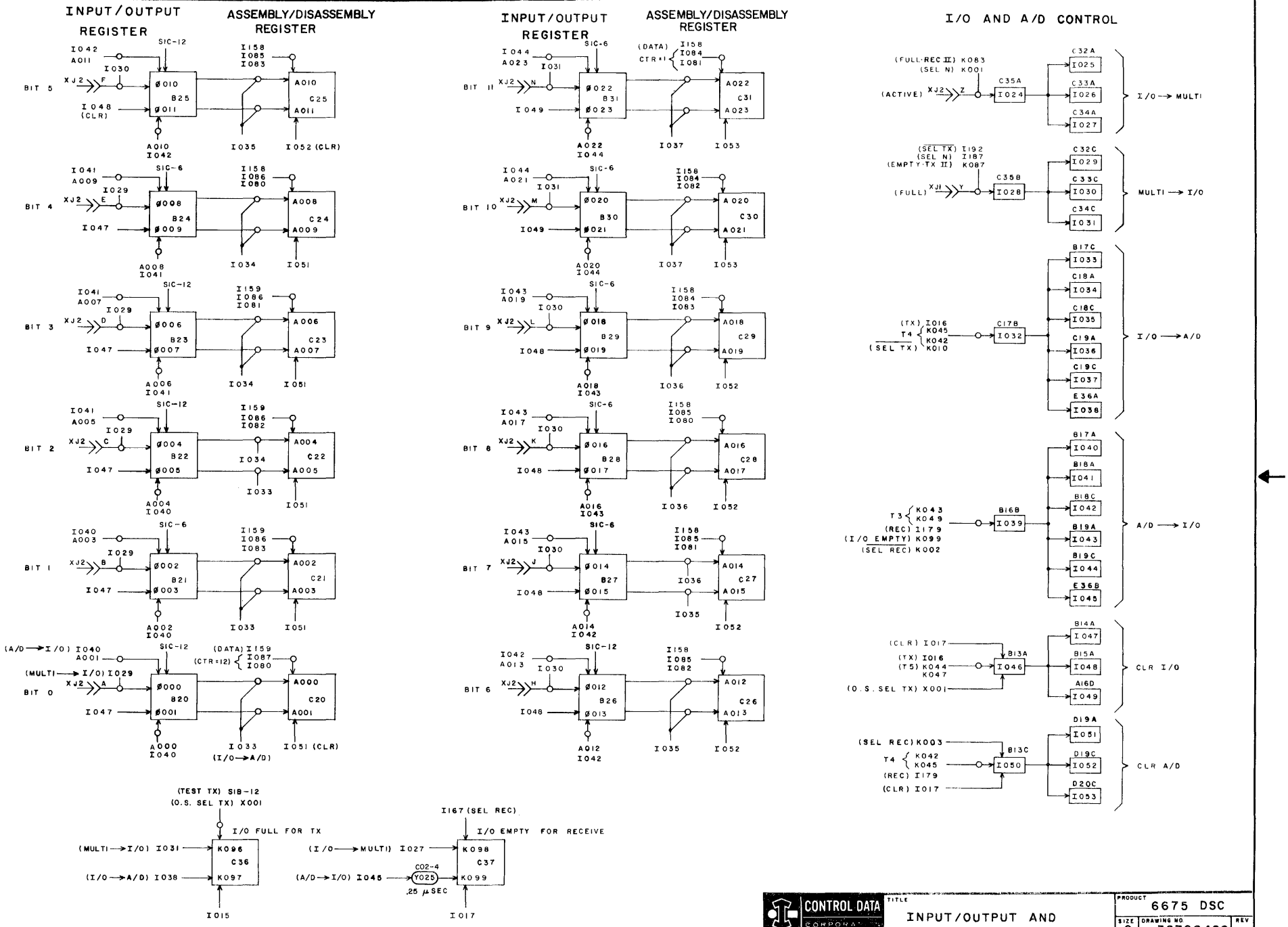
I/O AND A/D CONTROL

These control terms regulate I/O and A/D register transfers and clearing. The timing chain (page 1-15) enables transferring and clearing.

TERM	LOC'N	PAGE	DESCRIPTION
I015	D13B	1-11	Controller Clear
I016	D16B	1-11	TX
I017	B12B	1-11	Controller Clear
I080	D22B	1-15	XX00
I081	D23B	1-15	XX01
I082	D24B	1-15	XX10
I083	D25B	1-15	XX11 } A/D Counter Trans.
I084	D26B	1-15	00XX
I085	D27B	1-15	01XX
I086	D28B	1-15	10XX
I087	E25A	1-15	11XX

TERM	LOC'N	PAGE	DESCRIPTION
I158	D21B	1-23	Serial Data Rec'd.
I159	D20A	1-23	Serial Data Rec'd.
I167	B04D	1-11	Sel. Rec.
I179	B03C	1-11	Rec.
I185	D14C	1-11	TX
I187	B11D	1-11	Sel. N
I192	B36D	1-11	Sel. TX
K001	A01C	1-11	Sel. N
K002	B01A	1-11	$\overline{\text{Sel. Rec.}}$
K003	B01C	1-11	Sel. Rec.

TERM	LOC'N	PAGE	DESCRIPTION
K010	D01A	1-11	$\overline{\text{Sel TX}}$
K042	B07A	1-15	} Timing Chain
K043	B07C	1-15	
K044	B08A	1-15	
K045	B08C	1-15	
K047	B09C	1-15	
K049	B10C	1-15	
K083	C41B	1-15	(Full) (Rec.)
K087	C42B	1-15	(Empty) (TX)
X001	D17C	1-11	One Shot = (Sel. TX) (CS)



CONTROL DATA CORPORATION SYSTEM SCIENCES DIVISION	TITLE: INPUT/OUTPUT AND ASSEMBLY/DISASSEMBLY REGISTERS	PRODUCT: 6675 DSC	
		SIZE: C	DRAWING NO: 38700400 REV:
			SHEET: 7 — 1-13

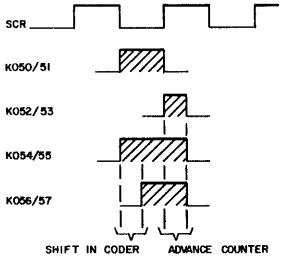
TIMING

COUNTER CONTROL

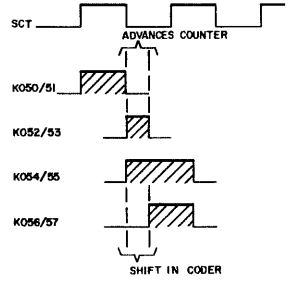
This circuit provides the Advance and Transfer signals for the counter. During Transmit mode the SCT Data Set signal functions as the master timing source. During the Receive mode the SCR signal supplies the clock pulses.

Three gates start counter control: the receive gate, the transmit gate and the $\overline{\text{transmit}}$ gate. The SCT signal from the data set pulses the transmit gate. The SCT triggers one counter advance and one transfer each time it makes a logic "0" to "1" transition (every 24.8 μsec) as observed at M100. Transmission of the transmit code word enables the $\overline{\text{transmit}}$ gate. Enabling at least 12 bits of idle pattern assures detection of a break between two separate data blocks. The receive gate enables the control during the Receive mode by SCR.

RECEIVE OPERATION TIMING



TRANSMIT OPERATION TIMING



CYCLIC ENCODER/DECODER CONTROL

This circuit provides timing signals to Encoder/Decoder Controls on page 1-23. The timing signals enable the cyclic encoder/decoder (E/D) Shift and Transfer operations.

Three gates start the E/D control: generate transmit code, generate receive code, and check for sync word or interrupt word. During the Transmit mode, the transmit gate enables timing signals (SCT) from Counter control to start the cyclic E/D control. The receive gate requires receipt of a sync word and setting of the Receive FF (page 1-11). The SCR signal from the data set enables the gate.

When the DSC is not in the Receive or Transmit mode, SCR signals enable the third gate. This gates idle pattern, a sync word, or an interrupt (the RD signals from the data set) into the cyclic E/D.

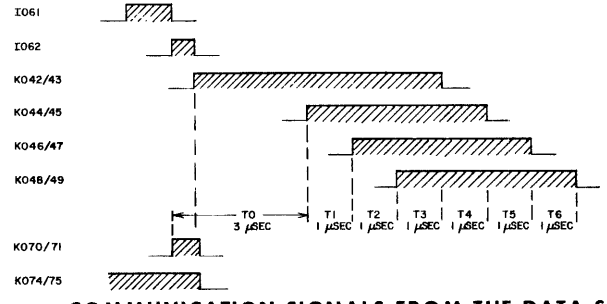
A/D COUNTER

The counter provides clocking pulses that count the 12 serial bits of each word in or out of the 6675. The A/D counter translator translates counter status. On the count of 12, the counter enables the last bit (bit 12) of serial data, starts the timing chain, and clears the counter.

TIMING CHAIN

The timing chain starts each time the counter equals 12. The chain provides 7 timing pulses that enable various Control, Transfer, and Clear operations.

TIMING CHAIN



COMMUNICATION SIGNALS FROM THE DATA SET

The AT&T 301B data set communicates via the following signals: Serial Clock Transmit (SCT), Serial Clock Receive (SCR), Receive Data (RD), Carrier On-Off (COO), Interlock (IT), and Clear-to-Send (CS). The 6675 Data Set Controller Reference Manual, publication number 38701400, describes these signals.

STATUS ALL

When the multiplexer requests status-all, each DSC transmits three bits to form the status-all word at the multiplexer. The Status-All FFs set and clear during DSC Transmit and Receive operations. Term I004 indicates a Request Status-All from the multiplexer (page 1-11) and gates the content of FF I to FF II.

FULL AND RECEIVE

An A/D → I/O transfer (page 1-13) sets the Full and Receive FF. This transfer occurs at time T3 if the Receive FF is set, the I/O register is empty, and the Select Receive FF is clear. An I/O → multiplexer transfer clears the Full and Receive FF. With the respective DSC selected and an Active signal on the line, the data word in the I/O register transfers from the DSC and the Full and Receive FF clears.

EMPTY AND TRANSMIT

One-shot X001 sets the Empty and Transmit FF at the beginning of a Transmit operation. The one-shot also clears the I/O register at this time. This enables loading the first data word into the I/O register. During each Transmit operation the Empty and Transmit FF sets at T6. At T5 an I/O → A/D transfers data out of the I/O register. Transferring data into the I/O register (Multi → I/O) clears the FF.

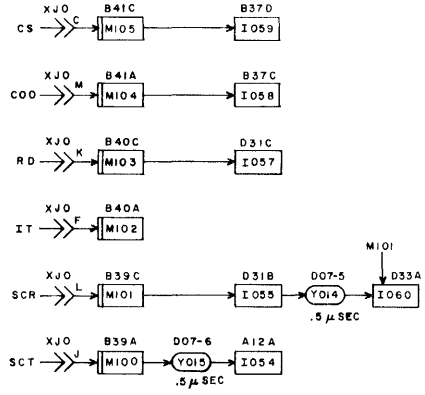
ERROR

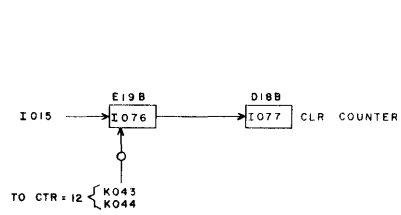
The Error FF sets if S012 (page 1-7) indicates that the Transmit and $\overline{\text{CS}}$ FF, or Receive and $\overline{\text{COO}}$ FF, or the Cyclic Error FF is set. Reselecting the Transmit or Receive modes or enabling a controller clears the Error FF.

TERM	LOC'N	PAGE	DESCRIPTION
I004	C35C	1-11	$\overline{\text{(Status Req → All)}}$
I007	F16B	1-11	Set Sync Word
I009	B04B	1-11	$\overline{\text{Rec}}$ (Delayed)
I015	D13B	1-11	Controller Clear
I016	D16B	1-11	TN
I018	A13B	1-11	$\overline{\text{(Test Mode)}}$
I019	A11B	1-11	CLR Error
I020	D12B	1-11	$\overline{\text{(TN + Rec)}}$
I027	C34A	1-13	I/O → Multi
I031	C34C	1-13	Multi → I/O
I044	B19C	1-13	A/D → I/O
I169	D10A	1-11	$\overline{\text{TN}}$
I179	B03C	1-11	Rec
I184	B14C	1-11	$\overline{\text{Rec}}$
I[illegible]	D14C	1-11	TN
I[illegible]	D10B	1-11	$\overline{\text{TN}}$ Code
I[illegible]	D10C	1-11	TN Code
O004	B02A	1-11	$\overline{\text{Rec}}$
O005	B02C	1-11	Rec
O01[illegible]	D04C	1-11	TN Code
O012	B11[illegible]	1-11	Error

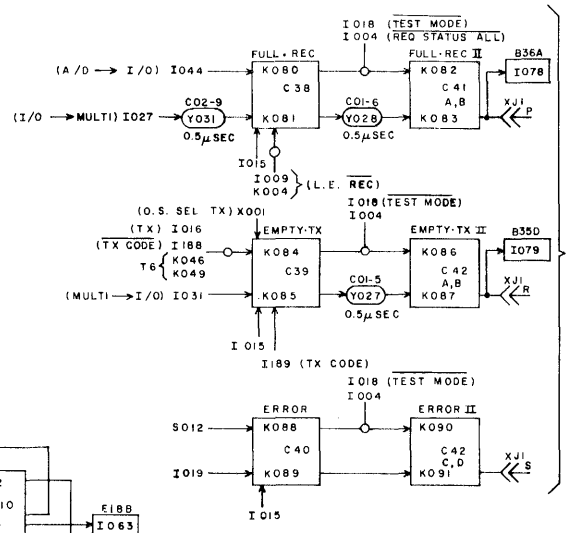
COMMUNICATION SIGNALS FROM DATA SET

FROM DATA SET



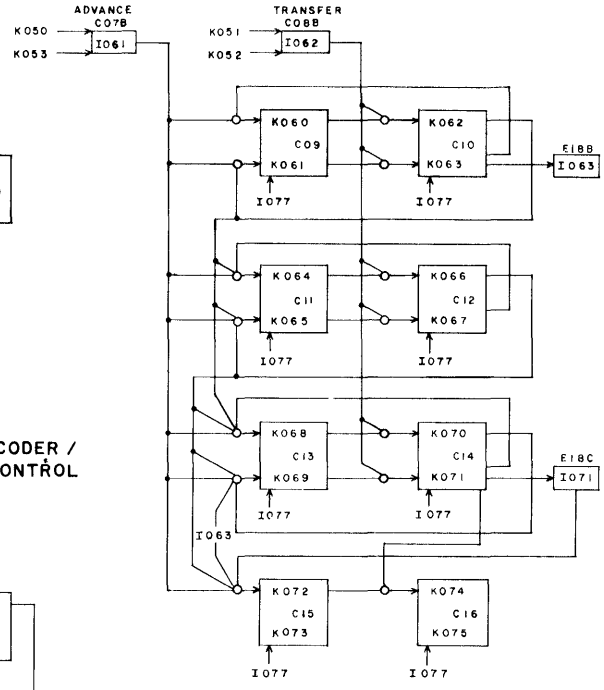


STATUS ALL

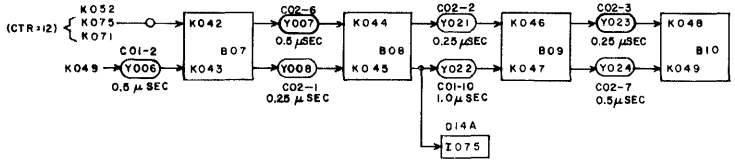


TIMING

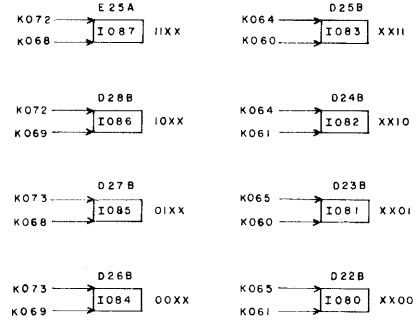
A/D COUNTER



TIMING CHAIN

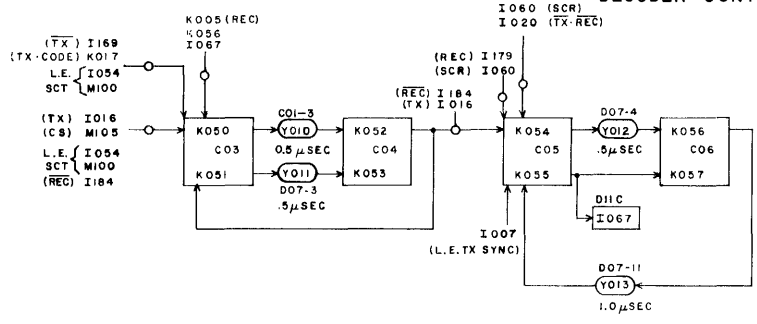


A/D COUNTER TRANSLATOR



COUNTER CONTROL

CYCLIC ENCODER / DECODER CONTROL



* USED ONLY WITH 24 BIT CODER

CONTROL DATA COMPORATION SYSTEM SCIENCES DIVISION	TITLE: A/D COUNTER, TIMING CHAIN, STATUS ALL, AND COMMUNICATION SIGNALS	PRODUCT: 6675 DSC	
		SIZE: C	DRAWING NO.: 38700400 REV: A
			SHEET: 8 1-15

STATUS BITS

INTERRUPT WORD RECEIVED (0001)

The Interrupt Receive FF sets when an interrupt word (7622) is detected by the Interrupt circuit (page 1-21) and the 6675 is not in Transmit or Receive modes. The interrupt word indicates that the remote station requires attention.

BUSY (0002)

The S003 supplies a "1" to the status/data output lines if the DSC is selected to transmit or receive, or if a Transmit or Receive operation is in process. Term K018 is present only in installations utilizing a 24-bit code word. K013 assures that the output of S003 remains a "1" until transmission of the second 12-bit code word.

SYNC WORD ACKNOWLEDGE (0004)

The Sync Word Acknowledge FF sets when the transmit sync word is sent out. If the receiving data set does not return a response (100_2 code), the FF remains set and enables the Sync Word Acknowledge status bit.

CYCLIC ERROR (0010)

The cyclic Error FF sets at T1 when the DSC is in Receive mode, the Keeper FF in the cyclic E/D error detection circuit is set, and the I/O register is full. The Keeper FF (page 1-23) sets before the last Receive operation. During the last Receive operation an I/O → Multi transfer does not occur because the entire data block has been transferred and the I/O register presently contains the code word. During testing procedures, when the S2B manual switch is positioned at 1-4, the Cyclic Error FF sets if the Error Detection circuit does not equal 0 when the Receive FF clears.

RECEIVE AND $\overline{\text{COO}}$ FF (0020)

This FF sets when the DSC is in the Receive mode and COO (the Transmission Line Carrier signal) is not present.

TRANSMIT AND $\overline{\text{CS}}$ (0040)

This FF sets when the DSC is in the Transmit mode and the Clear-to-Send (CS) signal is not present at the data set. Reselecting the DSC clears the FF.

ERROR INDICATOR

Any one of three status FFs enables the Error Indicator circuit. If the Transmit and $\overline{\text{CS}}$ FF, or the Receive and $\overline{\text{COO}}$ FF, or the Cyclic Error FF is set, it disables the gate to S012 and S012 sets flip-flop S014/015. When the flip-flop sets, error indicating lights DS1 and DS2 go On. After 200 ms, one-shot Y017 clears the FF and the lights turn Off. The Y017 delay circuit is non-inverting in relation to the input, but changes from "1" to "0" are delayed at the output. When the gate to S012 disables, S012 enables the Error FF (K088/089) in the Status-All circuits (page 1-15).

OPERATIONS INDICATORS

The Transmit or Receive indicating lights go On when the DSC is in the Receive or Transmit mode. The lights are mounted on the DSC control panel.

COMMUNICATION SIGNALS TO MULTIPLEXER

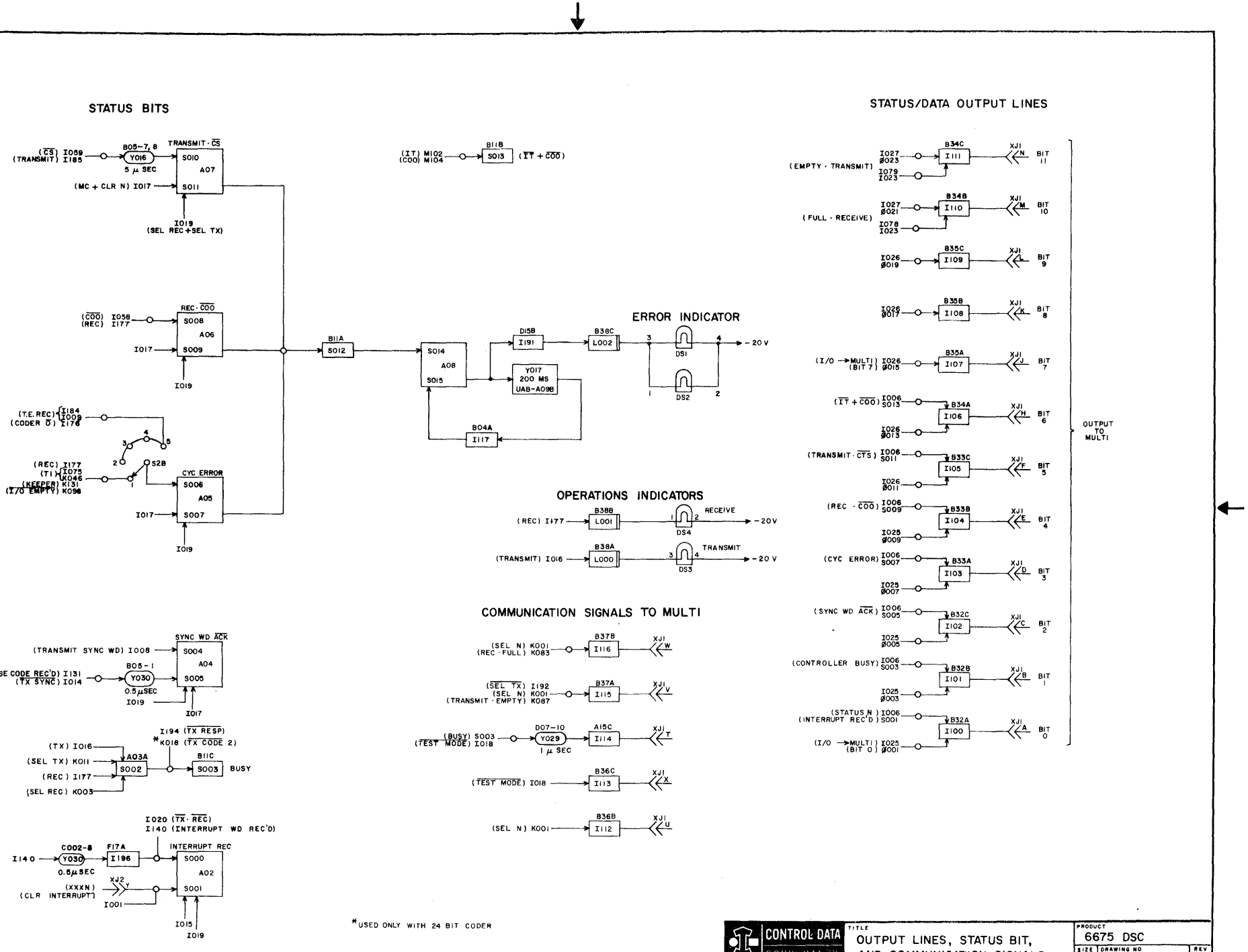
These signals indicate the operational status of the respective DSC. The multiplexer utilizes these signals to form the transmit and empty, full and receive, and active and inactive indications.

STATUS/DATA OUTPUT LINES

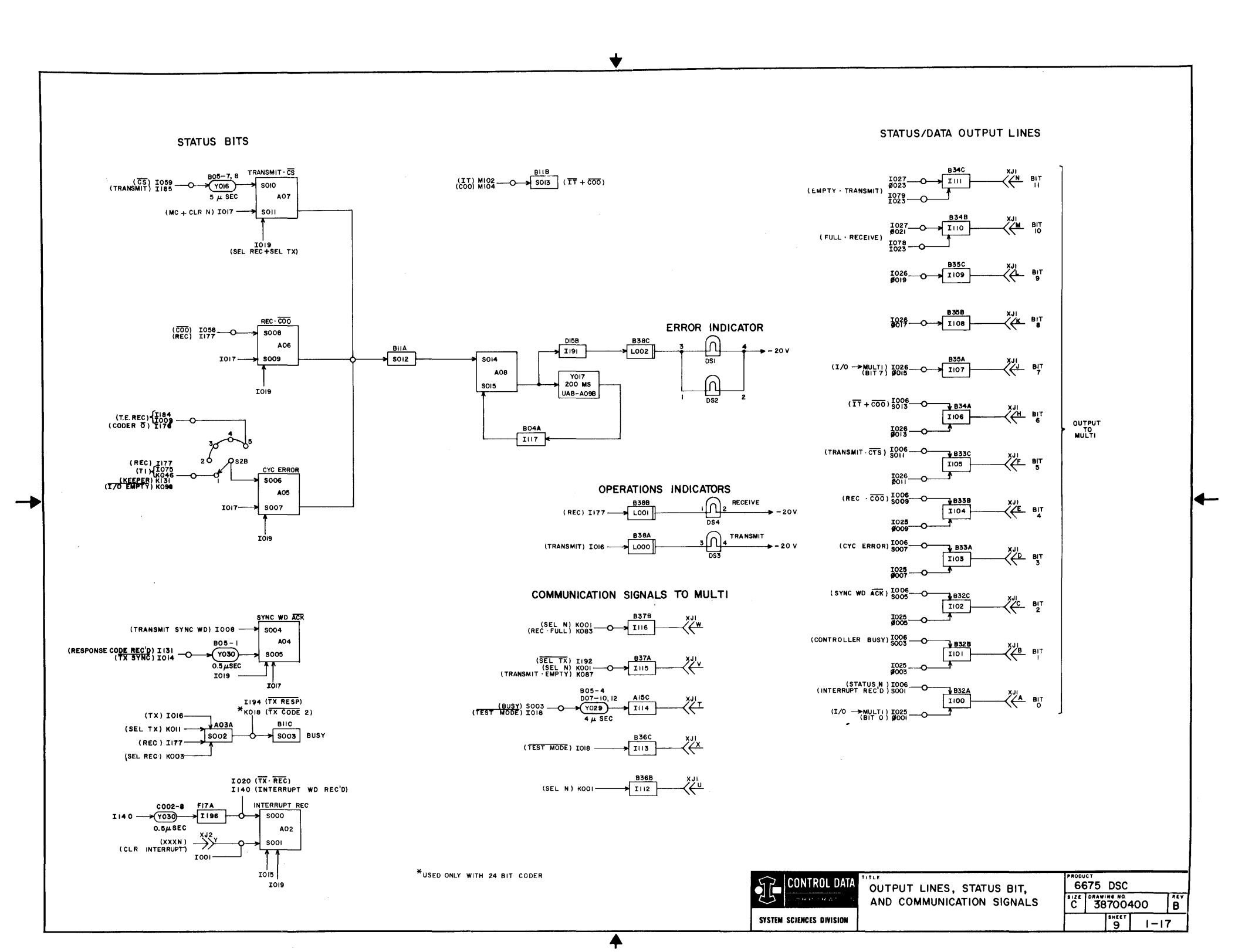
The DSC output lines transfer data and status information to the multiplexer. The I/O register gates data onto the lines. The respective FF or inverter gates status information out onto the lines if the Request Status FF for this DSC (at the multiplexer) is set.

TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION
I001	A15A	1-11	XXXN	I075	D14A	1-15	Timing Chain	K098	C37A	1-13	$\overline{\text{I/O Empty For Receive}}$
I006	A14B	1-11	Status Req. N	I078	B36A	1-15	(Full) (Rec.)	K131	E38C	1-23	Error Detected
I008	D15D	1-11	TX Sync (Delayed)	I079	B35D	1-15	(Empty) (TX)	M102	B40A	1-15	IT
I009	B04B	1-11	Rec. (Delayed)	I131	D41C	1-19	Sync Word Response Received	M104	B41A	1-15	COO
I015	D13B	1-11	Controller Clear	I140	E37A	1-21	Interrupt Word Received	Q001	B20C	1-13	Bit 0
I016	D16B	1-11	TX	I176	D38D	1-23	Error Detected	Q003	B21C	1-13	Bit 1
I017	B12B	1-11	Controller Clear	I177	B06B	1-11	Rec	Q005	B22C	1-13	Bit 2
I018	A13B	1-11	$\overline{\text{Test Mode}}$	I184	B14C	1-11	$\overline{\text{Rec}}$	Q007	B23C	1-13	Bit 3
I019	A11B	1-11	CLR Error	I192	B36D	1-11	$\overline{\text{Sel. TX}}$	Q009	B24C	1-13	Bit 4
I020	D12B	1-11	($\overline{\text{TX}}$) ($\overline{\text{Rec.}}$)	K001	A01C	1-11	Sel. N	Q011	B25C	1-13	Bit 5
I023	B03A	1-11	Status Req. N	K003	B01C	1-11	Sel. Rec.	Q013	B26C	1-13	Bit 6
I025	C32A	1-13	I/O → Multi	K011	D01C	1-11	Sel. TX	Q015	B27C	1-13	Bit 7
I026	C33A	1-13	I/O → Multi	K018	D05A	1-11	$\overline{\text{Complete Code}}$	Q017	B28C	1-13	Bit 8
I027	C34A	1-13	I/O → Multi	K046	B09A	1-15	Timing Chain	Q019	B29C	1-13	Bit 9
I058	B37C	1-15	$\overline{\text{COO}}$	K083	C41-B	1-15	(Full) (Rec.)	Q021	B30C	1-13	Bit 10
I059	B37D	1-15	$\overline{\text{CS}}$	K087	C42-B	1-15	(Empty) (TX)	Q023	B31C	1-13	Bit 11

I/O Register



CONTROL DATA CORPORATION	TITLE: OUTPUT LINES, STATUS BIT, AND COMMUNICATION SIGNALS
SYSTEM SCIENCES DIVISION	PRODUCT: 6675 DSC
	SIZE: C — DRAWING NO: 38700400 — REV: A
	SHEET: 9 — 1-17


STATUS BITS
STATUS/DATA OUTPUT LINES
ERROR INDICATOR
OPERATIONS INDICATORS
COMMUNICATION SIGNALS TO MULTI
OUTPUT TO MULTI
TRANSMIT · CS
REC · COO
CYC ERROR
SYNC WD ACK
INTERRUPT REC
BUSY
RECEIVE
TRANSMIT
*USED ONLY WITH 24 BIT CODER
CONTROL DATA
SYSTEM SCIENCES DIVISION
OUTPUT LINES, STATUS BIT, AND COMMUNICATION SIGNALS
6675 DSC
38700400
B
C
9
1-17

TRANSMIT RESPONSE (FOR SYNC WORD DETECTED DURING RECEIVE MODE)

The Transmit Response circuit supplies a 3-bit response when the DSC is in the Receive mode and detects a sync word. It also supplies a response when it detects an interrupt word.

If the DSC is in the Receive mode, the Transmit Response FF sets when I144 (page 1-21) indicates that the detection circuit recognizes a sync word. Thereupon, the SCT signals from the data set pulse the Transmit Response counter. The counter supplies three pulses, and clears the Transmit Response FF on the third count. When this FF clears, it disables Transmit Response.

During the time Transmit Response FF is set, the 3-bit response code (100_2) is gated to I183 (page 1-23) and transmitted at the SCT rate.

When the DSC is not in the Transmit or Receive mode and the Interrupt Detection Circuit (page 1-21) recognizes an interrupt word, the Transmit Response FF sets. This enables the 3-bit response code in the manner described above.

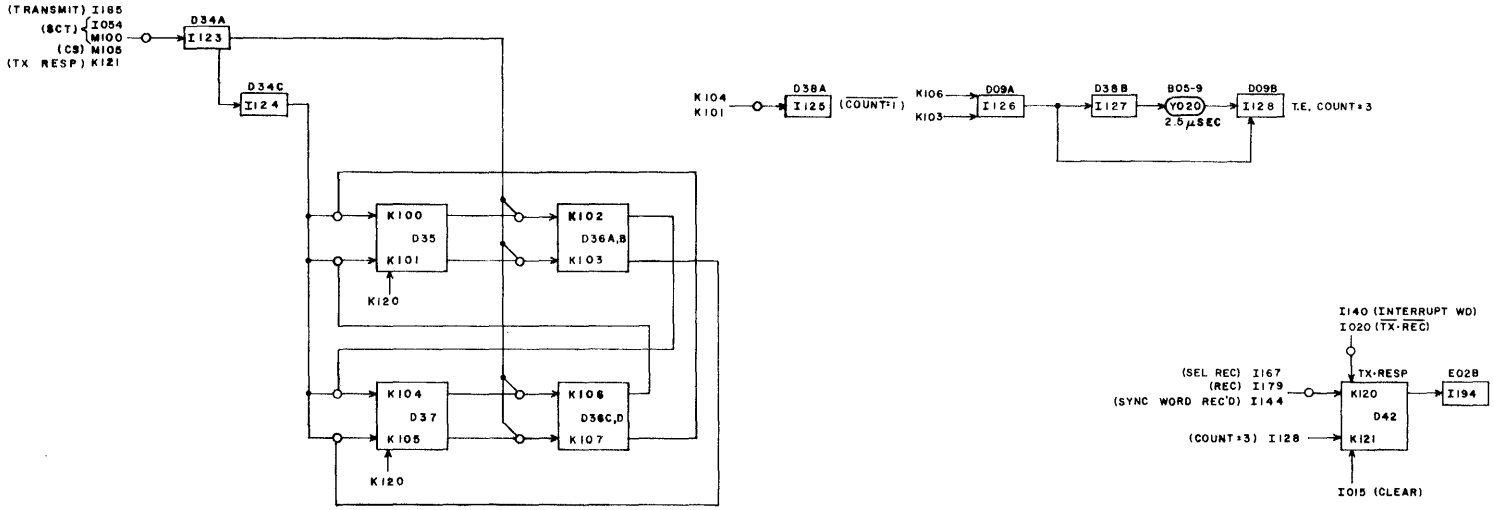
RECEIVE RESPONSE (FOR SYNC WORD SENT DURING TRANSMIT MODE)

When the DSC is in the Transmit mode, the Receive Response circuit activates at the time the transmit sync word is enabled and the Sync Word $\overline{\text{Acknowledge}}$ FF sets. With this FF set, SCR signals shift the response code on the RD line through the Receive Response flip-flops. Receiving the response code (100_2) in the register causes I131 to have a "1" output and clear the Sync Word $\overline{\text{Acknowledge}}$ FF. When this FF clears it disables the Receive Response FFs.

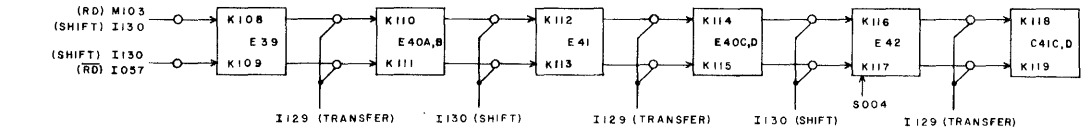
TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION
I015	D13B	1-11	Controller Clear	I140	E37A	1-21	Interrupt Word Received	M100	B39A	1-15	SCT
I022	D11A	1-11	No Data Flow	I144	E37C	1-21	Sync Wd. Received	M103	B40C	1-15	RD
I054	A12A	1-15	SCT (Inverted)	I179	B03C	1-11	Rec.	S004	A04A	1-17	Sync Wd. Ack.
I057	D31C	1-15	RD (Inverted)	I185	D14C	1-11	TX	S005	A04C	1-17	Sync Wd. $\overline{\text{Ack}}$.
I060	D33A	1-15	SCR (Inverted)								

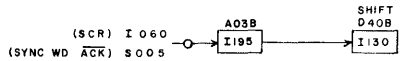
TRANSMIT RESPONSE (FOR SYNC WORD PRECEEDING RECEIVE DATA OR INTERRUPT WORD)

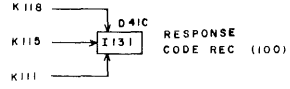
TRANSMIT RESPONSE COUNTER

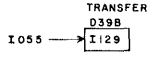


RECEIVE RESPONSE (FOR SYNC WORD PRECEEDING TRANSMIT DATA)









CONTROL DATA / SYSTEM SCIENCES DIVISION	TITLE: SYNC WORD TRANSMIT AND RECEIVE RESPONSE CIRCUITS	PRODUCT: 6675 DSC	
		SIZE: C	DRAWING NO.: 38700400 REV
		SHEET: 10	1-19

DISASSEMBLY CIRCUIT

The A/D counter enables the 12 input gates to the circuit. Each count gates an A/D Register FF into the serial data stream. The highest-order bit (bit 11) is gated first.

The I148 and I149 deliver each bit read out of the A/D register to E/D logic for cyclic encoding and to C148/149 for output to the data set (page 1-23).

Terms I148 and I149 function during both Transmit and Receive modes. During the Transmit mode, I147 gates serial data to these inverters; during the Receive mode, M103 gates receive serial data.

INTERRUPT WORD (7622) DETECTOR

When the 6675 is not in the Receive or Transmit mode, the interrupt circuit monitors the cyclic E/D FFs for a 7622 interrupt word. When the interrupt circuit detects a 7622 among the idle bit-pattern, I140 sets status bit 0001, Interrupt Receive FF (page 1-17). The interrupt word also enables transmission of a 3-bit response by setting the Transmit Response FF (page 1-19).

SYNC WORD (4257) DETECTOR

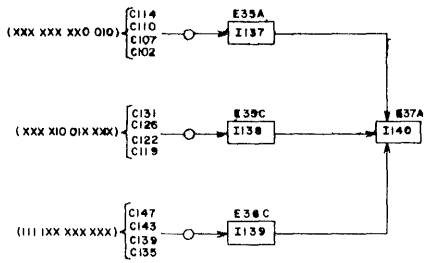
This circuit monitors the cyclic E/D FFs for a 4257 sync word. When a sync word is detected among the idle bit pattern, I144 enables the gate to the Receive FF (page 1-11). Thereupon, the Receive FF and I144 enable the gate to the Transmit Response FF (1-19). The response circuit acknowledges receipt of the sync word with a 3-bit response.

TERM	LOC'N	PAGE	DESCRIPTION
A001	C20C	1-13	Bit 0
A003	C21C	1-13	Bit 1
A005	C22C	1-13	Bit 2
A007	C23C	1-13	Bit 3
A009	C24C	1-13	Bit 4
A011	C25C	1-13	Bit 5
A013	C26C	1-13	Bit 6
A015	C27C	1-13	Bit 7
A017	C28C	1-13	Bit 8
A019	C29C	1-13	Bit 9
A021	C30C	1-13	Bit 10
A023	C31C	1-13	Bit 11
			A/D Register
C101	F18C	1-23	
C102	F19A	1-23	
C105	F20C	1-23	
C107	F21C	1-23	
C109	F22C	1-23	
			Cyclic Encoder/Decoder

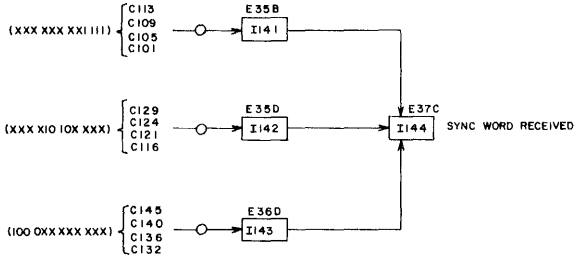
TERM	LOC'N	PAGE	DESCRIPTION
C110	F23A	1-23	
C113	F24C	1-23	
C114	F25A	1-23	
C116	F26A	1-23	
C119	F27C	1-23	
C121	F28C	1-23	
C122	F29A	1-23	
C124	F30A	1-23	
C126	F31A	1-23	
C129	F32C	1-23	
C131	F33C	1-23	
C132	F34A	1-23	
C135	F35C	1-23	
C136	F36A	1-23	
C139	F37C	1-23	
C140	F38A	1-23	
			Cyclic Encoder/Decoder

TERM	LOC'N	PAGE	DESCRIPTION
C143	F39C	1-23	
C145	F40C	1-23	
C147	F41C	1-23	
			Cyclic Encoder/Decoder
I022	D11A	1-11	No Data Flow
I080	D22B	1-15	XX00
I081	D23B	1-15	XX01
I082	D24B	1-15	XX10
I083	D25B	1-15	XX11
I084	D26B	1-15	00XX
I085	D27B	1-15	01XX
I086	D28B	1-15	10XX
I087	E25A	1-15	11XX
			A/D Counter Trans.
I170	D09C	1-11	$\overline{\text{Rec}}$
I179	B03C	1-11	Rec
I185	D14C	1-11	TX

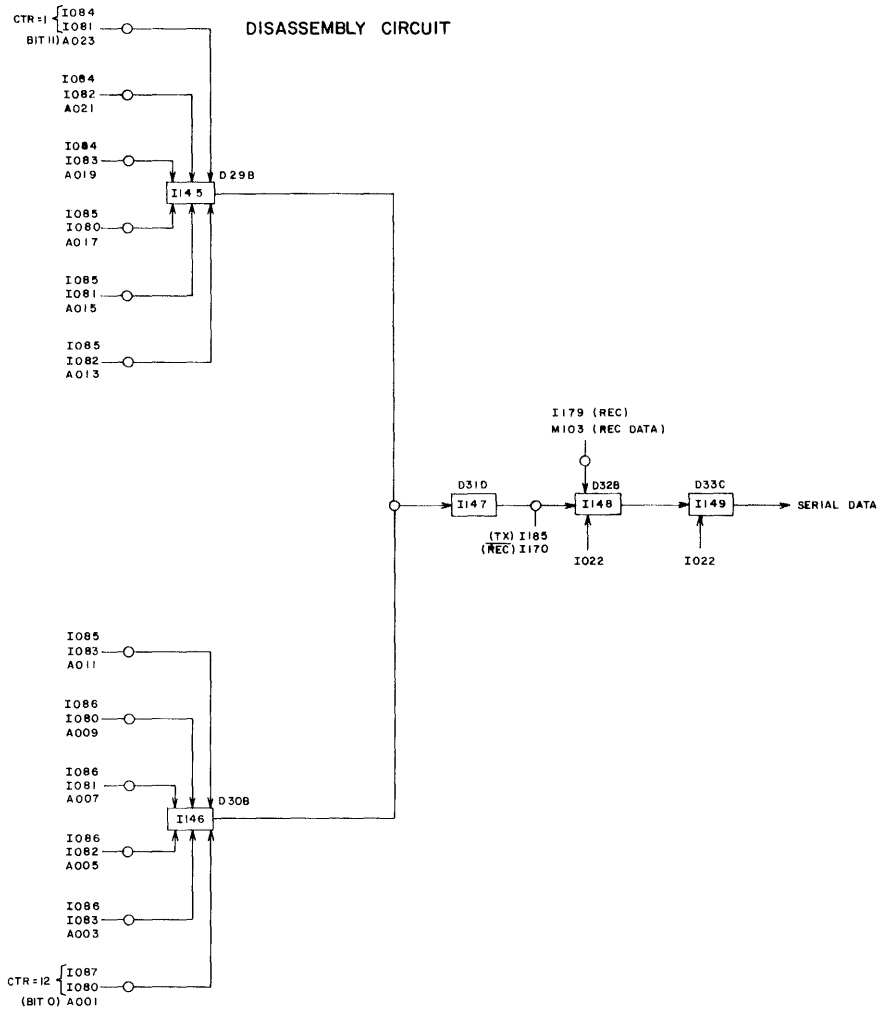
INTERRUPT WORD (7622) DETECTOR



SYNC WORD (4257) DETECTOR



DISASSEMBLY CIRCUIT



CONTROL DATA SYSTEM SCIENCES DIVISION	TITLE: INTERRUPT, SYNC WORD, AND DISASSEMBLY CIRCUITS	PRODUCT: 6675 DSC	
		SIZE: C	DRAWING NO.: 38700400 REV
		SHEET: 11	1-21

CYCLIC ENCODER/DECODER

An efficient method of detecting errors utilizes what is called a cyclic code. The encoder of the transmitting DSC performs a computation on the data bits and uses the results as a 12-bit code added to the end of the data transmission. The decoder at the receiving DSC performs the identical computation on the data plus code bits. The mathematics of the system are such that the decoder derives a result of all zeros for a correct transmission.

The cyclic encoder/decoder (E/D) consists basically of a 12-stage shift register with special feedback logic. The Cyclic E/D performs the following functions. Two are associated with cyclic codes, two are not. Refer to page 1-29 for a flow chart of Encoder/Decoder functions.

1) It transmits a sync word (preset by I007) preceding a data transfer in Transmit mode. This word is shifted out at the SCT rate.

2) It generates a 12-bit cyclic code word during a Transmit operation and shifts it out as the last 12 bits of the message.

3) It checks whether the code word received as the last word of the string during a Receive operation compares with the code word generated in the Cyclic E/D. If the words compare, the E/D is driven to zero; if the words do not compare, the error detection circuit sets the Keeper FF.

4) It monitors idle-pattern from the remote data set when the DSC is neither transmitting nor receiving. When the respective monitor circuit (page 1-21) detects a sync word (4257), the Receive FF sets (page 1-11); when it detects an interrupt word (7622), the Interrupt Received FF sets (page 1-17).

If C146/147 (Bit 11) is set, the serial data is toggled (complemented) as it enters C100/101. If C146/147 is clear, serial data enters unchanged with C100/101. Refer to page 1-28 for a flow chart of Encoder/Decoder internal operation.

FF C148/149 receives serial data from the Disassembly circuit and gates it out to the A/D register (receive data) or to the data set (transmit data). Serial transmit data is gated out through L100. Receive data is gated to the A/D register by I062. Since I062 enables the rank II transfer in the A/D counter (page 1-15), I062 synchronizes the gating of data with the counter advance.

Receipt of a sync word by the DSC in Receive mode sets the Receive FF (page 1-11), sets the Transmit Response FF (page 1-19), and enables a 3-bit response word. The full duplex nature of the Telpak transmission line permits transmission of the response while serial data is being received. The Transmit Response FF disables the gate from C148/149, sets the Transmit FF (page 1-11), and enables a 100_2 code.

ERROR DETECTOR

The Error Detection circuit checks the E/D Shift register for all zeros after each word transfer. The Keeper FF sets if the circuit detects a "1". If the Keeper FF is set after the last data word transfers to the multiplexer during the Receive mode and the I/O register contains the code word, the Keeper FF enables the Cyclic Error FF (page 1-17).

ENCODER CLEAR

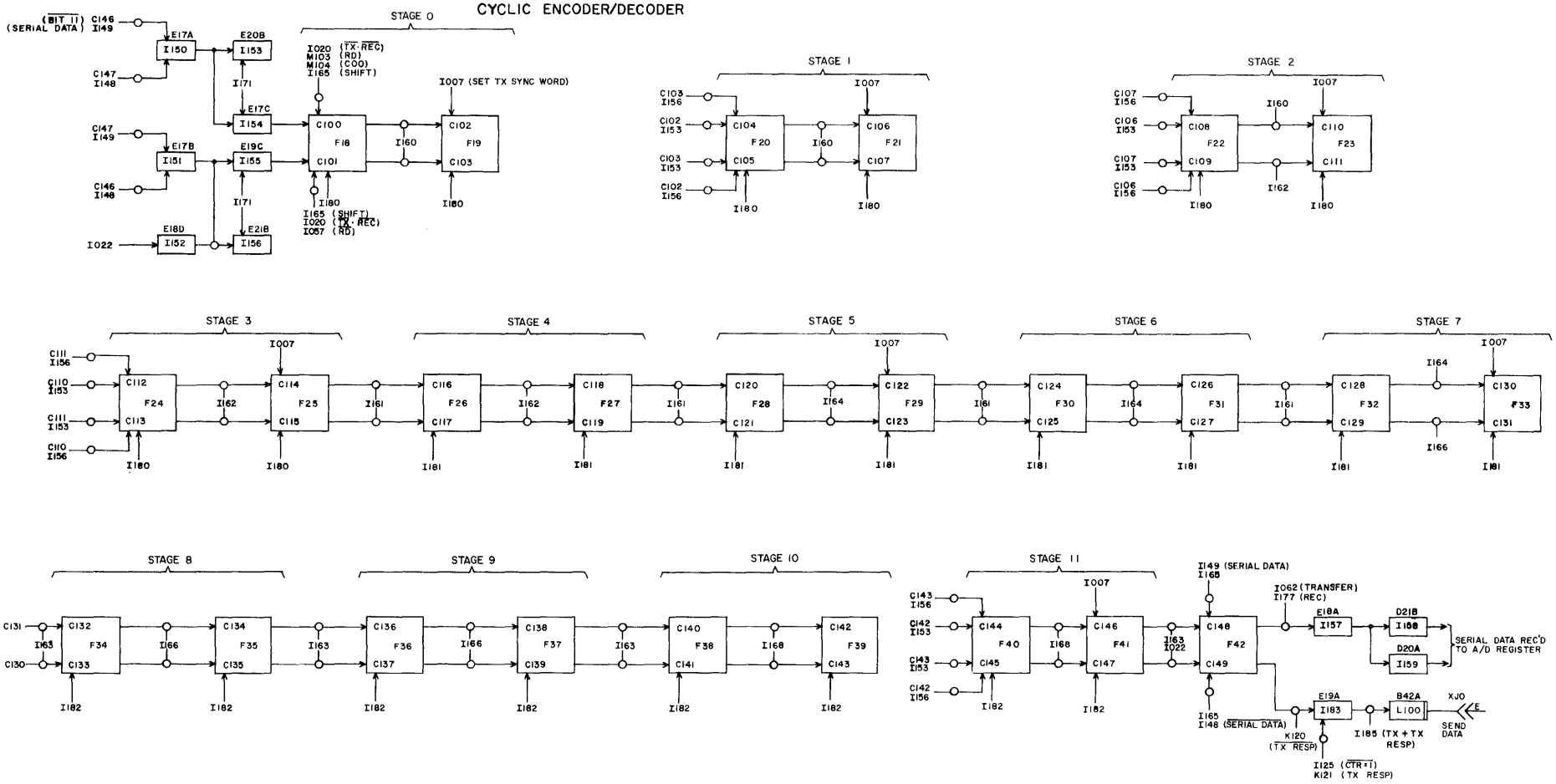
Selection of the Transmit mode or the Receive mode, or shifting the transmit sync word out of the 12-stage shift register enables the Clear circuit. A Controller Clear also enables the Clear circuit.

ENCODER/DECODER CONTROLS

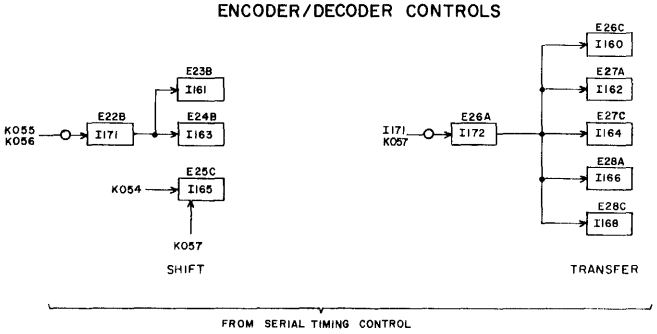
This control provides the shift and transfer pulses for the Cyclic E/D. The Cyclic Encoder/Decoder control (page 1-15) triggers the circuits.

TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION	TERM	LOC'N	PAGE	DESCRIPTION
I007	E16B	1-11	Set Sync Word	I062	C08B	1-15	A/D Counter Rank 1 → Rank 2	K042	B07A	1-15	Timing Chain
I008	D15D	1-11	TX Sync (Delayed)	I075	D14A	1-15	Timing Chain	K054	C05A	1-15	Cyclic Encoder/Decoder Cont.
I014	D15C	1-11	$\overline{\text{TX Sync}}$	I125	D38A	1-19	Count = 1	K055	C05C	1-15	Cyclic Encoder/Decoder Cont.
I015	D13B	1-11	Controller Clear	I148	D32B	1-21	Serial Data	K056	C06A	1-15	Cyclic Encoder/Decoder Cont.
I016	D16B	1-11	TX	I149	D33C	1-21	Serial Data	K057	C06C	1-15	Cyclic Encoder/Decoder Cont.
I017	B12B	1-11	Controller Clear	I169	D10A	1-11	TX	K120	D42A	1-19	$\overline{\text{TX Resp.}}$
I020	D12B	1-11	($\overline{\text{TX}}$) ($\overline{\text{Rec.}}$)	I177	B06B	1-11	Rec.	K121	D42C	1-19	TX Resp.
I022	D11A	1-11	No Data Flow	I186	D38C	1-11	Sel. TX	M103	B40C	1-15	RD
I057	D31C	1-15	RD (Inverted)	K003	B01C	1-11	Sel. Rec.	M104	B41A	1-15	COO

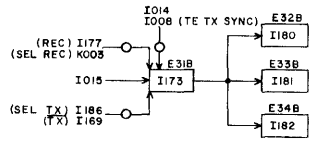
CYCLIC ENCODER/DECODER



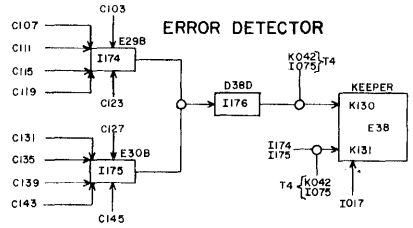
ENCODER/DECODER CONTROLS



ENCODER CLEAR



ERROR DETECTOR



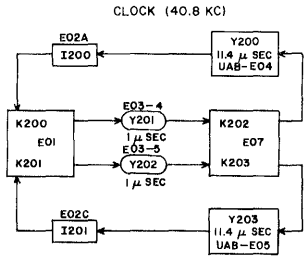
CONTROL DATA CORPORATION SYSTEM SCIENCES DIVISION	TITLE: CYCLIC ENCODER/DECODER	PRODUCT: 6675 DSC SIZE: C · DRAWING NO.: 38700400 · REV: SHEET: 12 · 1-23	

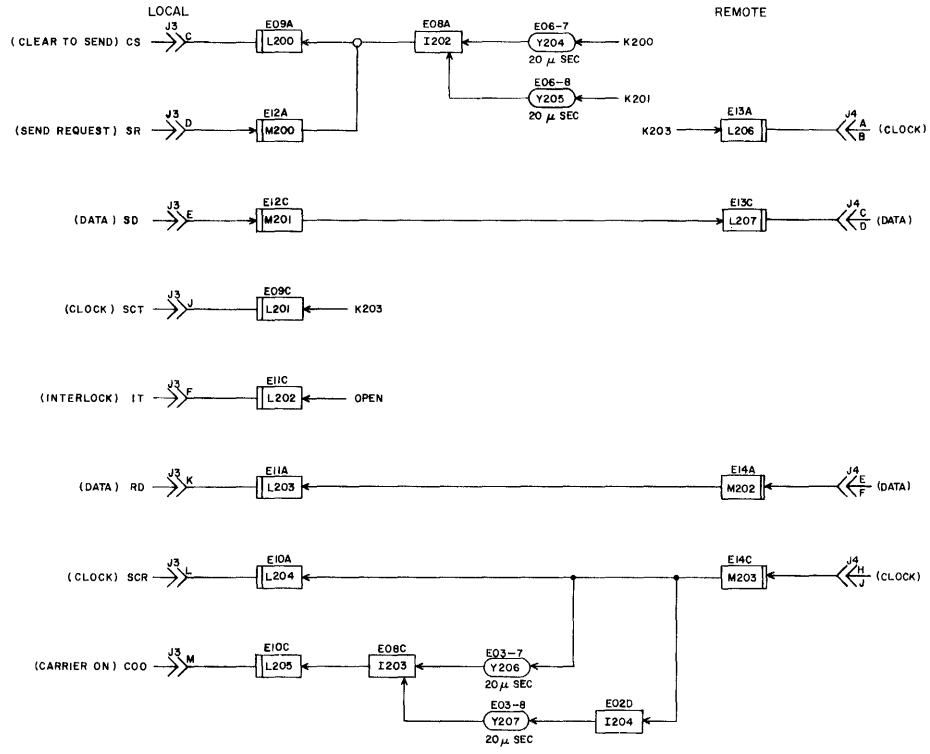
DATA SET SIMULATOR

The data set Simulator circuit, built into each DSC, enables maintenance personnel to checkout two DSC's without the use of data sets. To use the simulator, certain DSC cables must be disconnected and others must be connected. Part 2, Maintenance, describes the test operation.

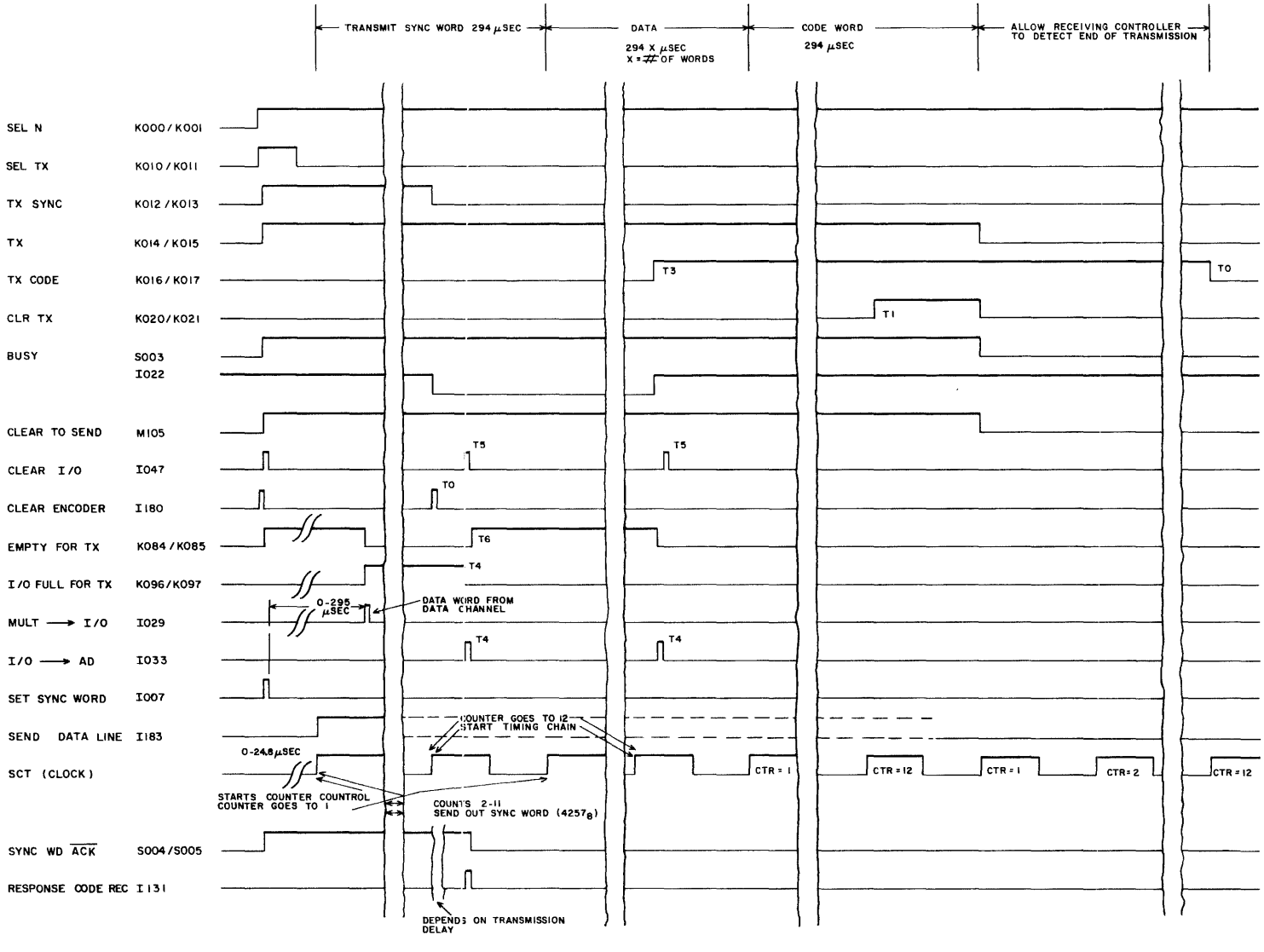
The simulator circuitry includes the 40.8 kc Clock shown at the top of page 1-25. The 40.8 kc oscillator simulates 301B data set timing signals. If the 6675 uses a data set having higher or lower transmission rates, the oscillator is modified accordingly.

DATA SET SIMULATOR





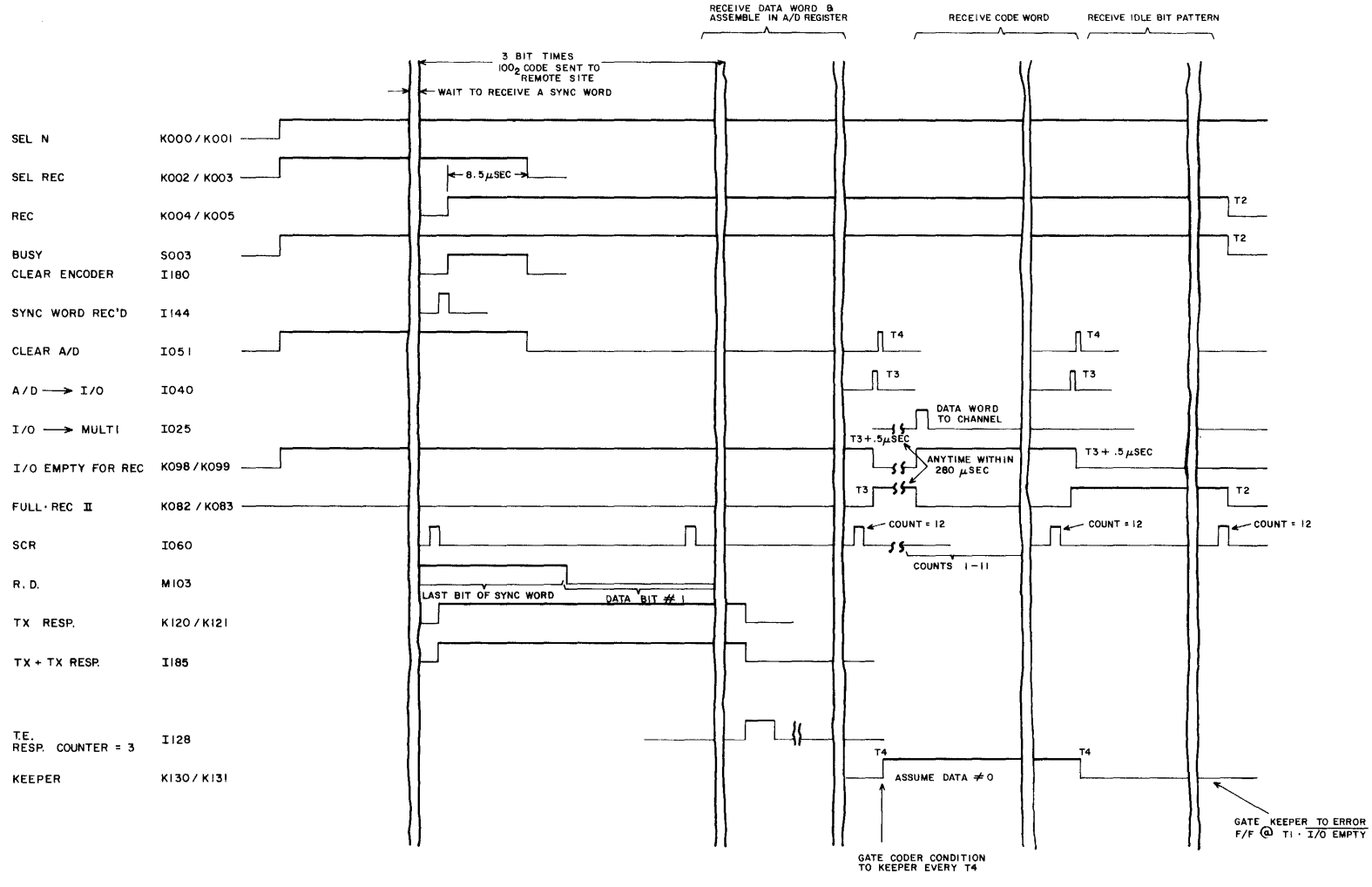
CONTROL DATA CORPORATION SYSTEM SCIENCES DIVISION	TITLE: DATA SET SIMULATOR	PRODUCT: 6675 DSC	
		SIZE: C	DRAWING NO.: 38700400 REV:
			SHEET: 13 1-25



CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION

TITLE: TRANSMIT TIMING CHART

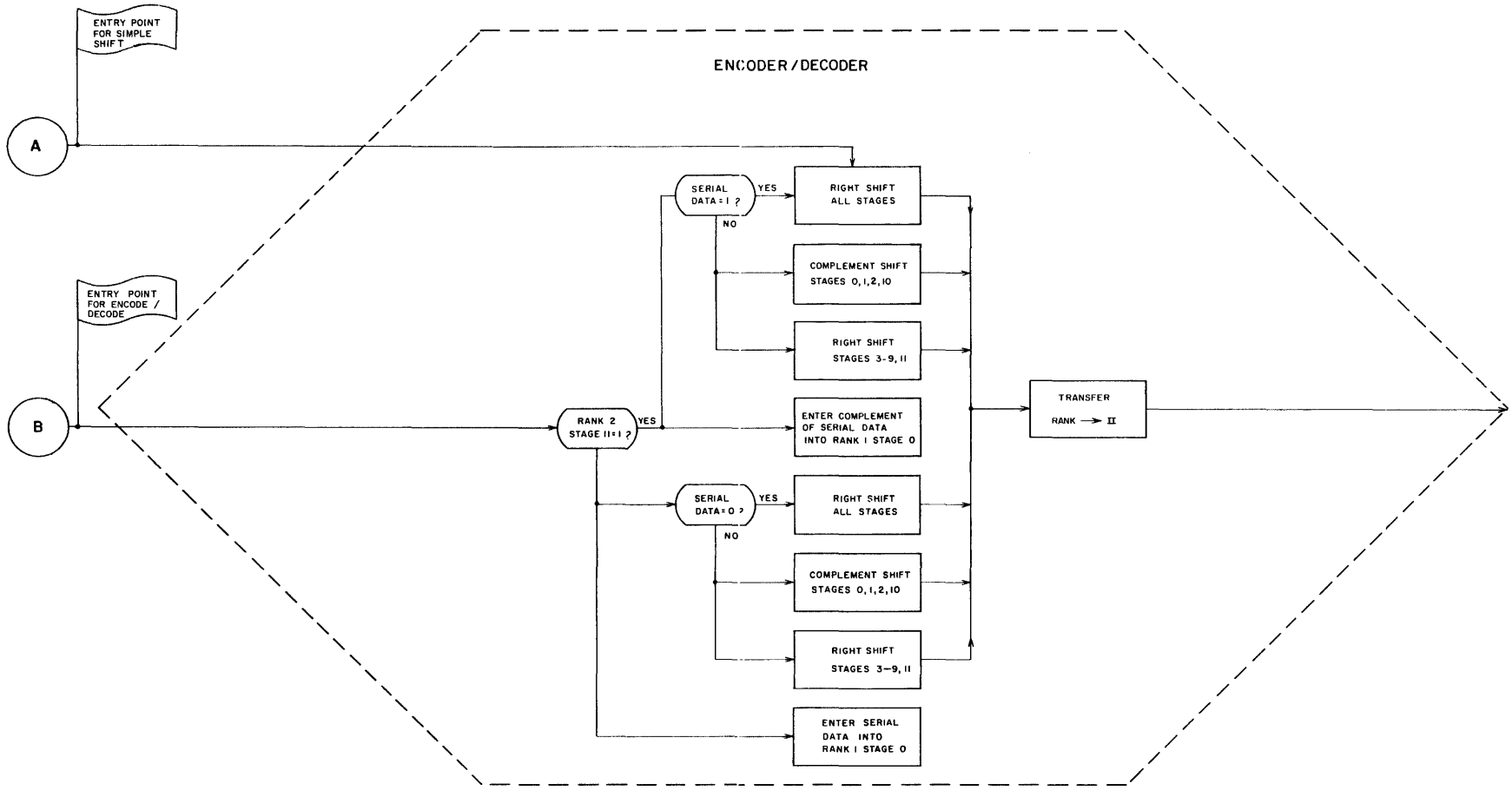
PRODUCT: 6675 DSC
SIZE: C | DRAWING NO.: 38700400 | REV:
SHEET: 14



CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION

TITLE: RECEIVE TIMING CHART

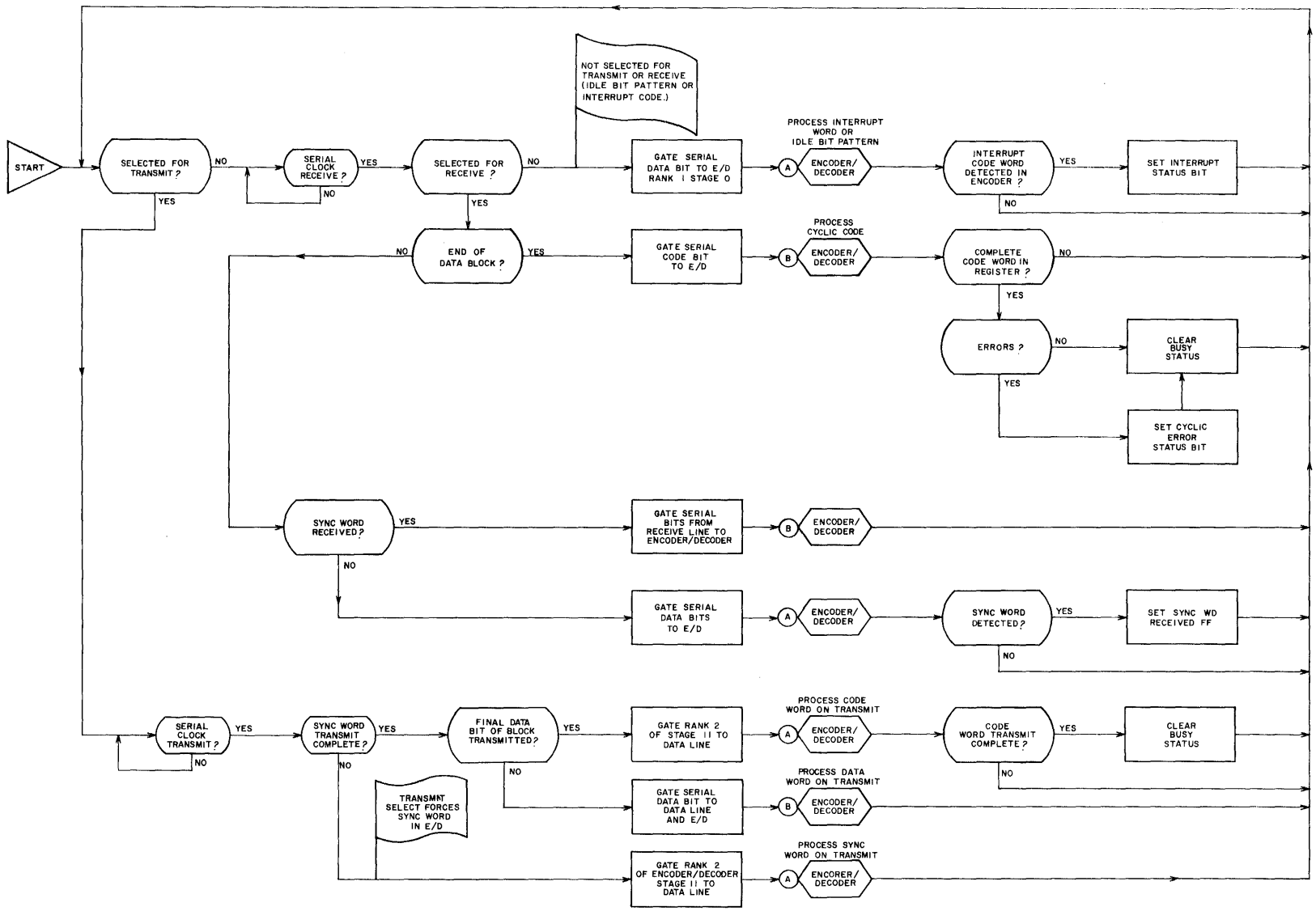
PRODUCT		
6675 DSC		
SIZE	DRAWING NO.	REV
C	38700400	
	SHEET 15	1-27



"COMPLEMENT SHIFT" INDICATES COMPLEMENTING RANK 2 OF A STAGE AND SHIFTING IT TO RANK 1 OF THE NEXT STAGE.

"RIGHT SHIFT" INDICATES SHIFTING RANK 2 OF A STAGE TO RANK 1 OF THE NEXT STAGE. RIGHT SHIFT OF STAGE 11 IS ALWAYS END OFF.

CONTROL DATA CORPORATION SYSTEM SCIENCES DIVISION	TITLE CYCLIC ENCODER / DECODER OPERATION	PRODUCT 6675 DSC SIZE C DRAWING NO. 38700400 REV DRAWN SHEET 0F1-28	



CONTROL DATA CORPORATION
SYSTEM SCIENCES DIVISION

TITLE
CYCLIC ENCODER / DECODER FUNCTIONS

PRODUCT 6675 DSC
SIZE C | DRAWING NO. 38700400 | REV
SHEET 1-29

CONTROLLER

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16
A	K000 K001	S000 S001	S002 I195	S004 S005	S006 S007	S008 S009	S010 S011	S014 S015	RELAY CONTROLS	RELAY CARD	I019	I054 I012	I018	I006	I001 I114	I000 I002 I003 I049
	(32)	(33)	(24)	(33)	(32)	(32)	(32)	(31)	(IIAB)	(77)	(12)	(23)	(12)	(11)	(21)	(20)

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
B	K002 K003	K004 K005	I023 I179	I117 I009 I013 I167	RELAY	I177	K042 K043	K044 K045	K046 K047	K048 K049	S012 S013 S003 I187	I017	I046 I050	I047 I184	I048 I005	I039	I040 I033	I041 I042	I043 I044	Ø000 Ø001	Ø002 Ø003	Ø004 Ø005	Ø006 Ø007	Ø008 Ø009	Ø010 Ø011	Ø012 Ø013	Ø014 Ø015	Ø016 Ø017	Ø018 Ø019	Ø020 Ø021	Ø022 Ø023	I100 I101 I102	I103 I104 I105	I106 I110 I111	I107 I108 I109 I079	I078 I112 I113 I192	I115 I116 I058 I059	L000 L001 L002	M100 M101	M102 M103	M104 M105	L100 L101
	(32)	(32)	(21)	(20)	(50)	(11)	(31)	(31)	(31)	(31)	(20)	(11)	(23)	(21)	(21)	(11)	(21)	(21)	(21)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(33)	(28)	(28)	(28)	(20)	(20)	(20)	(62)	(M64)	(M64)	(M64)	(M63)

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
C	RELAY		K050 K051	K052 K053	K054 K055	K056 K057	I061	I062	K060 K061	K062 K063	K064 K065	K066 K067	K068 K069	K070 K071	K072 K073	K074 K075	I032	I034 I035	I036 I037	A000 A001	A002 A003	A004 A005	A006 A007	A008 A009	A010 A011	A012 A013	A014 A015	A016 A017	A018 A019	A020 A021	A022 A023	I025 I029	I026 I030	I027 I031	I024 I028 I004	K096 K097	K098 K099	K080 K081	K084 K085	K088 K089	K082 K083 K118 K119	K086 K087 K090 K091
	(E11)	M73A	(33)	(31)	(33)	(31)	(12)	(12)	(32)	(32)	(32)	(32)	(32)	(32)	(31)	(31)	(11)	(21)	(21)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(21)	(21)	(21)	(29)	(32)	(32)	(33)	(33)	(32)	(30)	(30)

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
D	K010 K011	K012 K013	K014 K015	K016 K017	K018 K019	I011	RELAY K021	K020	I126 I128 I170	I169 I188 I189	I022 I067	I020	I015	I075 I185	I021 I191 I014 I008	I016	X001	I077	I051 I052	I159 I053	I158	I080	I081	I082	I083	I084	I085	I086	I145	I146	I190 I055 I057 I147	I148	I060 I149	I123 I124	K100 K101	K102 K103 K106 K107	K104 K105	I125 I127 I186 I176	I129	I130	I010 I131	K120 K121
	(32)	(32)	(33)	(32)	(31)*	(11)	(E11)	(32)	(28)	(29)	(21)	(12)	(11)	(21)	(20)	(11)	(E08)	(11)	(21)	(21)	(11)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(16)	(16)	(20)	(13)	(22)	(21)	(32)	(30)	(32)	(20)	(11)	(11)	(23)	(32)

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
E	K200 K201	I200 I194 I201 I204		Y200	Y203		K202 K203	I202 I203	L200 L201	L204 L205	L203 L202	M200 M201	L206 L207	M202 M203		I007	I150 I151 I154	I157 I063 I071 I152	I181 I074 I155	I153	I156	I171	I161	I163	I087 I165	I172 I160	I162 I164	I168 I188	I174	I175	I173	I180	I181	I182	I137 I141 I138 I142	I038 I045 I139 I143	I140 I144	K130 K131	K108 K109	K110 K111 K114 K115	K112 K113	K116 K117
	(31)	(20)	(73A)	(UAB)	(UAB)	(73A)	(31)	(22)	(M63)	(M63)	(M63)	(M64)	(P14)	(P18)	(P15)	(12)	(28)	(20)	(28)	(12)	(12)	(11)	(11)	(11)	(22)	(21)	(21)	(21)	(16)	(16)	(14)	(11)	(11)	(11)	(20)	(20)	(23)	(32)	(31)	(30)	(31)	(32)

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
F	I196	C100 C101	C102 C103	C104 C105	C106 C107	C108 C109	C110 C111	C112 C113	C114 C115	C116 C117	C118 C119	C120 C121	C122 C123	C124 C125	C126 C127	C128 C129	C130 C131	C132 C133	C134 C135	C136 C137	C138 C139	C140 C141	C142 C143	C144 C145	C146 C147	C148 C149
	(20)	(33)	(31)	(33)	(32)	(33)	(32)	(33)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(32)	(33)	(32)	(32)

*ONLY USED FOR 24 BIT CODER

MULTIPLEXER

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
A	I912 F936	F922 F924	F923 F900 F901	F903 F904	F905	F902 F906 F935 I918	F908 F909 F910 F911	I921	F930 F931	F932	F934	F925 I926	I927	K900 K901	I930	I931	I932	I933
	(21)	(21)	(20)	(21)	(11)	(20)	(20)	(11)	(23)	(11)	(12)	(22)	(11)	(32)	(12)	(12)	(12)	(12)

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
B	F940 F941	F942 F943	F951	F953	F954	F955	F956	F957	K902 K903	K904 K905	K906 K907	K908 K909	I940 I942 I944	F920 F921 I946 I948	F952 I947	I812 I813 I814 I815	I816 I817 I818 I819	I820 I821 I822 I823	I824 I825 I826 I827	I828 I829 I830 I831	I832 I833 I834 I835	I900 I901	I902 I903	I904 I905	I906 I907	I908 I913	I909	I910	I911	I914	I915	F933 I919 F937 I916	I934 I917	I800 I801 I802	I803 I804 I805	I807	I806 I808 I809	F950 I810 I811	K910 K911	K912 K913 K916 K917	K914 K915	Y900 Y901 Y902
	(23)	(23)	(14)	(14)	(14)	(14)	(14)	(14)	(32)	(32)	(32)	(32)	(28)	(20)	(24)	(20)	(20)	(20)	(20)	(20)	(20)	(21)	(21)	(21)	(21)	(21)	(11)	(11)	(11)	(11)	(11)	(20)	(21)	(28)	(28)	(16)	(28)	(28)	(32)	(30)	(32)	(E11)

KEY TO LOGIC SYMBOLS

(STANDARD 1604 OR 3600 CARD TYPES)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA Corporation logic, two signals, a logical "0" and a logical "1", are the possible input or output conditions of a circuit. A circuit with an output of "1" is "up" and a circuit with an output of "0" is "down". Detailed descriptions of logic symbols and their associated building block circuit cards are contained in the Printed Circuit Card Manual (Pub. No. 60042900).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for CONTROL DATA equipment using 1604- or 3600-type cards are inverters, flip-flops, control delays, and capacitive and inductive delays.

Inverters

An inverter is a logic element which provides an output that is an inversion of its input. When more than one input is provided to an inverter, 1's take precedence over 0's and drive the output of the inverter to "0". Because any "1" input of several inputs drives the output to a "0", an inverter may be considered an inverting OR (or NOR) gate when more than one input is present.

Inverters are shown in the logic diagrams as rectangles (Figure 1). J001 and J002 are arbitrarily-assigned term numbers which designate these specific inverters. Note that the output of J002 is "0" if input A, or input B or input C is a "1".

Figure 1. Inverter Symbols

Acceptable conventions for showing multiple OR inputs are given in Figure 2.

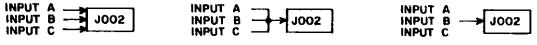


Figure 2. OR Circuit Conventions

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states - designated as Set and Clear - and is composed of two or more inverters. The logic symbols (Figure 3) are formed by the combination of inverter symbols. By convention, Set inputs and outputs are shown in the upper part of the symbol and Clear inputs and outputs are shown in the lower part of the symbol.

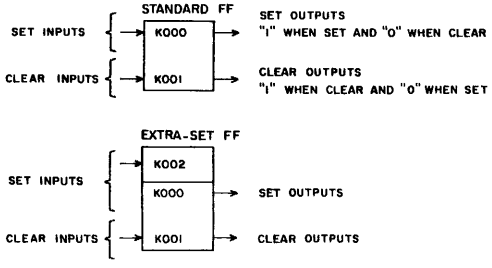


Figure 3. Flip-Flop Symbols

Figure 4 illustrates the interconnection of inverter symbols to form a flip-flop symbol. The term numbers assigned to each flip-flop are the term numbers of the internal inverters as seen by comparing the terms in Figure 3 with those in Figure 4. Notice that the Set output is the output of inverter K001, and the Clear output is the output of inverters K000 and K002.

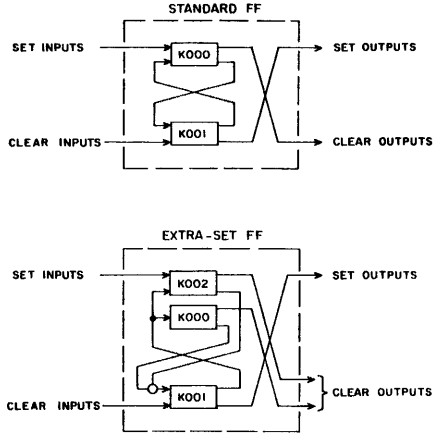


Figure 4. Internal Inverter Connections for a Flip-Flop

AND Gate

An AND gate requires that all its inputs be 1's in order that its output be a "1". If one or more of the inputs to an AND gate are "0", the output is a "0". Figure 5 illustrates conventions for showing AND gates feeding an inverter.

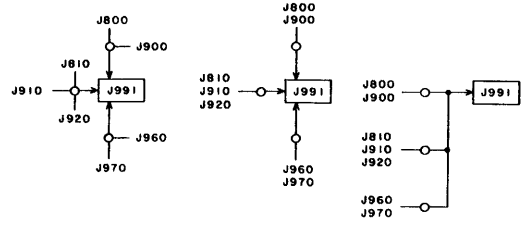


Figure 5. AND Circuit Conventions

Control Delay

A control delay is a timing device consisting of an H term which receives the input and one or more V, Y, or N terms to provide the outputs. The H term is essentially a flip-flop with controlled feedback and occupies an entire printed circuit card. The output term(s) are inverter(s) located elsewhere on the logic chassis. The "1" outputs from a control delay are clocked pulses which are delayed one phase time from the "1" inputs. Clock inputs are not shown on the logic diagrams for any H, V, Y, or N terms; these terms, which control the start and duration of the delayed output pulses, may be found in the Equation Summary. Figure 6 illustrates two representative forms of the control delay symbol, with possible inputs and outputs labelled. Figure 7 shows the electrical connections for the two forms.

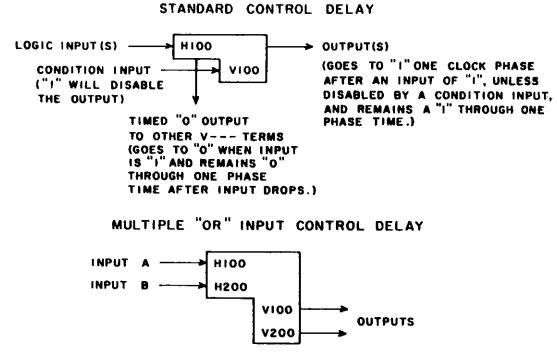


Figure 6. Control Delay Symbols

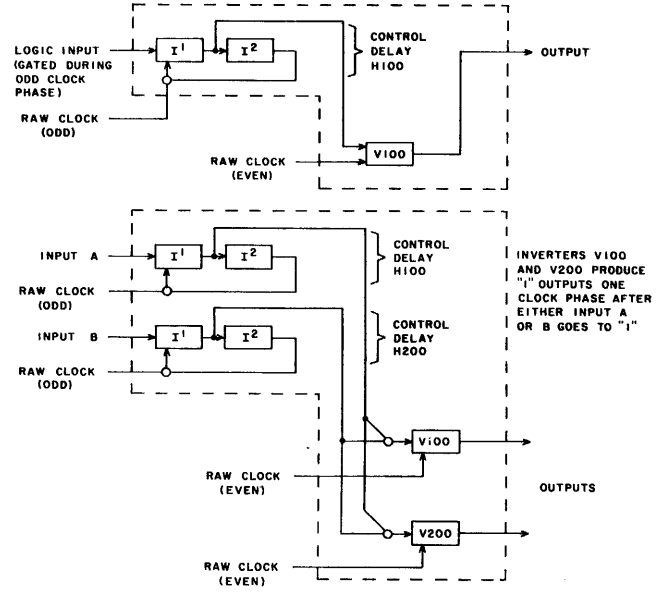


Figure 7. Electrical Connections for Control Delay

Control delays may have multiple inputs and/or multiple outputs. When a control delay has multiple output terms (i.e., more than one V, Y, or N term), each output term may have a separate conditioning input.

Capacitive Delays

A capacitive delay is used to delay the input to a logic element. Capacitive delays may be active or passive, depending upon whether or not transistors are used as part of the delaying circuit. Delay periods are checked by using a dual-trace scope connected to the input and output of the delay-producing element. The actual connection points for the scope probes will vary for different cards and should be determined by referring to the Printed Circuit Manual, Pub. No. 60042900 (Volume 2).

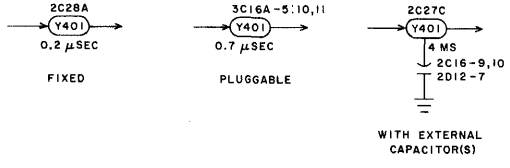


Figure 8. Active Capacitive Delays

Active delays may be recognized by the circuit letter always present as part of the card location. Pin numbers are also shown when external wiring is needed to connect the proper capacitance. In Figure 8, the pluggable delay uses this wiring to connect to capacitors on the same card. In the third example, this wiring connects to capacitors located on two separate capacitor cards.

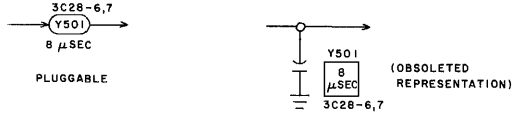


Figure 9. Passive Capacitive Delays

All passive capacitive delays (Figure 9) are formed by wiring grounded capacitors, located on one or more capacitor cards, as an AND input to the affected logic element. For this reason, all passive delays show pin numbers to provide this external wiring data.

Figure 10. Adjustable Capacitive Delays

Capacitive delays may be adjustable or non-adjustable, depending on the card type and/or the external wiring connections on the card. When it is necessary to adjust the delay period in order to obtain specified circuit operation (usually done by varying a potentiometer in the RC network), a diagonal arrow is added to the delay symbol as shown in Figure 10.

Inductive Delays

An inductive delay is used to delay the input to a logic element or as a tapped delay line for timing of operations. The symbol for this delay is an elongated oval with a double vertical line just within the input end of the oval. When used as a tapped delay line, the inductive delay is terminated in its characteristic impedance. Inductive delays are identified in the same manner as capacitive delays (except for the vertical lines) unless they are used as delay lines. On multi-section cards where no identifying circuit letters are present, pin numbers are shown adjacent to the input and output arrows. Figure 11 shows both kinds of inductive delays.

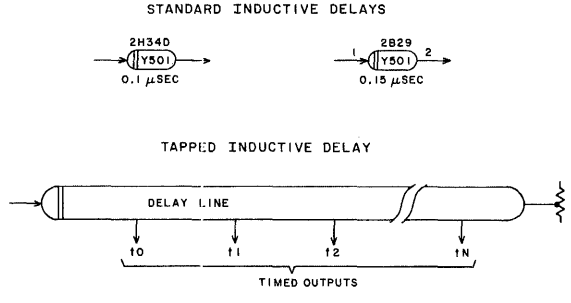


Figure 11. Inductive Delays

Line Drivers/Receivers

Voltage levels used to represent 1's and 0's on cables are different from those used for internal logic. The level shift to and from internal logic is made by line drivers and line receivers. These cards may be considered as inverting the signal electrically, but not logically. The letters commonly associated with these cards are L & M (1604) and R & T (3000 Series). A 3000 Series Receiver may also be used to perform a logical inversion by swapping the twisted pair wires. This usage is indicated by a circle on the input side of the symbol. In Figure 12, 1's and 0's have been added to clarify the logic states - they are not part of the symbol.

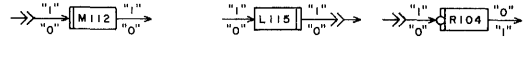


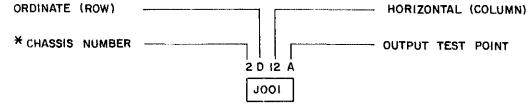
Figure 12. Typical Line Driver/Receiver Symbols

NON-LOGIC CONVENTION

The use of the double vertical bar, as in Figure 12, denotes a shift in signal voltage level from that used in internal logic. The double bar appears on the input or output side of the symbol, depending on which side connects to the non-logic-level signal. No particular voltage level is implied by the double bar; only that it is non-logic.

JACK ASSIGNMENTS

Each numbered term in the logic diagrams contains a jack assignment showing the physical location of that hardware element, and the test point (circuit section) associated with it. For some card types, the test point letter is replaced by a pin number. For these cases, a card extender must be used in order to test that section of the card. Also, some single inverters show no test point - test point A is assumed in these cases. Figure 13 illustrates the inverter J001, with 2D12A representing its jack assignment.



* When most or all jack assignments are located on one chassis, the chassis numbers for that chassis are omitted.

Figure 13. Jack Assignment Scheme

CABLE IDENTIFICATION

Cable connections are represented by the MIL STD-15 symbol and identified as to connector location and pins used, as shown in Figure 14.

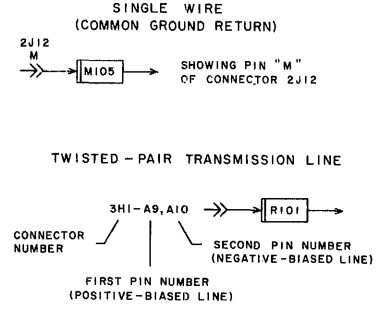


Figure 14. Cable Connections

PART 2
MAINTENANCE

INTRODUCTION

This section contains testing information for checking out the DSC's. The manuals listed on this page describe general maintenance information for cabinet, logic and power components. Since maintenance personnel are familiar with Control Data logic diagrams, cabling information contained in the equipment diagrams is not repeated in tabulated form.

INFORMATION	AVAILABLE PUBLICATION
Cabinet Cooling System, Control Wiring and Temperature Monitoring, and Power Supply.	Control Data Peripheral Controller Cabinets, Customer Engineering Instruction Manual, publication number 60097300
6675 Equation File, Wire Tabs, and Chassis Map.	CDC publication number 38710000

TESTING

The 6675 has a number of built-in testing features to facilitate quick and easy checkout of DSC circuitry. These features include test switches and circuitry to simulate a data set.

LOCAL-TO-REMOTE STATION TESTING

The following tests enable checkout of a 6675 installation that includes one or more DSC's. The tests check local-to-remote transmit and receive functions. The test operation requires the use of the Test and Clear switches on the DSC console.

Transmit Test

This transmit test does not require the use of a DSC at the remote station.

1) Use the Clear switch to clear the local DSC.
2) Turn the Transmit Test switch to one of the four test positions. This enables the following:
   a) Enables Transmit circuit (page 1-11)
   b) Transmits sync word
   c) Transmits one data word (transmits test word selected by Test switch)
   d) Transmits code word

After transmission of the code word, the Select Transmit FF sets again and the operation repeats. The DSC continues to cycle and simulate a one word transmission until the Transmit Test switch is positioned at Off. The four Transmit Test switch positions enable the following test words:

TRANSMIT TEST	TEST WORD	TEST
Switch Position 1	000 000 000 000	Checks for constant "1" on line
Switch Position 2	111 111 111 111	Checks for constant "0" on line
Switch Position 3	000 001 101 101	Checks 7622 interrupt code
Switch Position 4	111 110 010 010	Complement of interrupt code

3) The transmit section and the cyclic encoder/decoder may be checked out while the DSC is cycling in the Transmit mode. Since the remote DSC is not used for this test, the Sync Word $\overline{\text{Acknowledge}}$ status bit cannot be checked.
4) Upon completion of the test, clear the DSC.

Receive Test

1) Clear DSC.
2) Position Receive Test switch at REC.
3) Have Transmit Test switch on the DSC at the remote station position at one of the four test positions.
4) DSC at local station will receive a sync word, the selected data word and a code word. Check the Receive operation, response, and check cyclic code for error (Check cyclic code error status bit).
5) Clear the DSC.
6) Position Receive Test switch at INT.
7) Position Transmit Test switch at DSC at the remote station to Position 3 (interrupt word).
8) This checks the Interrupt Detection circuit of the local DSC.
9) Clear the DSC.

Transmit and Receive Test

1) Clear DSC (both at the local and at the remote stations).
2) Position Transmit Test switches at both the local and remote DSC's to one of four test positions and the Receive test switches to REC.
3) Each DSC alternately transmits and receives (one data word) and keeps cycling. Check the operation by observing the TX and REC indicators on the control console.
4) Clear DSC when test is complete.

USE OF DATA SET SIMULATOR

The data set simulator enables maintenance personnel to checkout two DSC's in the same cabinet. This permits testing without the use of data sets, a transmission line, or a remote station on 6675B-D.

To use the simulator, disconnect the cable leading from J0 on the DSC to the data set. Then connect J0 to the Local connector (J3) as shown in Figure 2-1. A cable is provided with the DSC for this purpose. Make this cable change on both DSC's.

Connect another cable from the Remote connector (J4) on one DSC to the Remote connector (J4) on the other DSC.

Perform Transmit and Receive test described previously.

When testing is complete, disconnect test cables and reconnect data set cables.

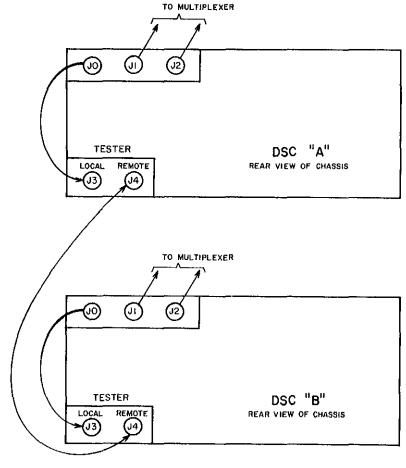


Figure 2-1. Simulator Cable Connections

PART 3
PARTS LIST

INTRODUCTION

The parts list provides the identification and ordering data necessary for the replacement of electrical and hardware parts for The CONTROL DATA 6675 Data Set Controller.

Electrical Contents: All chassis and final assembly items are included except lead wires and bulk wire.

Hardware Contents: All chassis and final assembly items are included except standard hardware such as screws, nuts, bolts, washers and raw material.

The chassis assembly and subassemblies are broken down into individual parts, listed in alphabetical rather than disassembly order.

Parts listing for the Data Channel Adaptor chassis assembly are contained in Publication Number CDC 38700100, SSD-SQ5003 Data Channel Adaptor.

The following publications contain information on printed circuit card assemblies, peripheral cabinets, and power supplies necessary to complete a total parts listing of the equipment:

Printed Circuit Card Assemblies	Pub. No.	60040800 60040900	Vols. I & II
CDC Power Supply Manual	Pub. No.	60120700	
Peripheral Controller Cabinets Customer Engineering Instruction Manual	Pub. No.	60097300	
Peripheral Equipment Cabinets Manual	Pub. No.	60097300	

ORDERING OF PARTS

When ordering Control Data parts, include the following information: CDC drawing number, description, quantity needed, equipment used on. When ordering vendor parts use the procedure indicated by that vendor.

6675 DATA SET CONTROLLER CDC Dwg. No. 38616200
PARTS LIST

Multiplexer Chassis Assembly DATE: _____

CDC-DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
25152900	Bar, Mounting, Connector	
30008700	Bracket, Angle, Chassis Frame	
30116600	Bracket, Mounting, Shield	
10028603	Cable Assembly, 30 inch, 24 pin connectors	
10028604	Cable Assembly, 36 inch, 24 pin connectors	
10028609	Cable Assembly, 72 inch, 24 pin connectors	
10028618	Cable Assembly, 54 inch, 24 pin connectors	
38614900	Cable Assembly, Test, 24 inch	
38615000	Cable Assembly, Test, Long, 12 feet	
30002201	Capacitor, Fixed, Electrolytic, 10-10 UF, 50 WVDC	
38710000	Card Placement	
31531200	Card Spacer Assembly →	
31531300	Card Spacer Assembly ←	
10001800	Connector, Receptacle, 30 Sockets	
24512001	Connector, Receptacle, 24 Sockets	
24531800	Connector, Receptacle, 14 Sockets	
24513901	Connector, Plug, 24 Pin	
24531701	Connector, Plug, 14 Pin	
38614500	Shield, Connector, Lettered	
30104800	Hinge, Input/Output Connector Panel	
38697900	Identification Plate, SSD, Small	
25159700	Latch, Connector, Panel	
25153701	Member, Frame, Bottom	
38613100	Member, Frame, Chassis, right	
38613200	Member, Frame, Chassis, left	
38613300	Panel, Switch, Multiplexer	
25156802	Plate, Retainer, Connector	
30103800	Plate, Retaining, Cable	
38614800	Plate, Retaining, Connector	
30013802	Spacer, Strip, Marker	
10031700	Strip, Marker, Wide 01-21	
10040900	Strip, Marker, Wide 22-42	
22201900	Strip, Marker, Narrow 01-34	
25153100	Strip, Marker, Narrow 01-21	

PARTS LIST

Multiplexer Cont'd. DATE: _____

CDC-DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
25153200	Strip, Marker, Narrow, 22-42	
30103900	Stud, Extension	
30104600	Support, Connector Assembly	
24515900	Switch, Toggle, SPDT	
24526700	Terminal Block, 20 Contacts	
00856604	Thumbscrew	
38710000	Wire Tabs	

PRINTED CIRCUIT CARD ASSEMBLY, MULTIPLEXER CHASSIS
PARTS LIST

DATE: _____

CDC-DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
17678800	Printed Circuit Card Assembly; Type E11	
10201801	Printed Circuit Card Assembly; Type 11	
10201901	Printed Circuit Card Assembly; Type 12	
10202501	Printed Circuit Card Assembly; Type 14	
10202701	Printed Circuit Card Assembly; Type 16	
10232201	Printed Circuit Card Assembly; Type 20	
10202801	Printed Circuit Card Assembly; Type 21	
10203401	Printed Circuit Card Assembly; Type 22	
10203501	Printed Circuit Card Assembly; Type 23	
10203601	Printed Circuit Card Assembly; Type 24	
10232501	Printed Circuit Card Assembly; Type 28	
10232901	Printed Circuit Card Assembly; Type 29	
10334401	Printed Circuit Card Assembly; Type 30	
10203801	Printed Circuit Card Assembly; Type 32	

6675 DATA SET CONTROLLER
PARTS LIST
Controller Chassis

CDC Dwg. No. 38616300
CDC Dwg. No. 38616301

DATE: _____

CDC-DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
21331600	Bar, Mounting, Connector	
25152900	Bar, Mounting, Connector	
30002201	Capacitor, Fixed, Electrolytic, 10-10 UF, 50 WVDC	
38710000	Card Placement, Controller Chassis	
31531200	Card spacer assembly →	
31531300	Card spacer assembly ←	
38614200	Card spacer assembly (used on 38616301 only)	
10001800	Connector, Receptacle, 30 socket	
24512001	Connector, Receptacle, 24 socket	
24531801	Connector, Receptacle, 4 hole panel mount, 14 sockets	
38697900	Identification plate, SSD small	
00827900	Jack, Banana	
00815701	Knob, with pointer, 1 1/4" long	
24511601	Lampholder, horizontal	
24516803	Lamp, Incandescent-slide type base, 24 volts	
24511747	Lens, Indicator, light, "Error"	
24515607	Lens, Indicator, light, divided "TX/REC"	
38612900	Member, Frame, right, controller chassis	
38613000	Member, Frame, left, controller chassis	
38612400	Panel, connector, bottom, controller chassis	
38613600	Panel, switch, Controller	
38614300	Panel, connector, Controller	
30013802	Spacer, strip, marker	
10031700	Strip, Marker, Wide, 01-21	
10040900	Strip, Marker, Wide, 22-42	
22315800	Strip, Marker, Narrow, 01-16	
25153100	Strip, Marker, Narrow, 01-21	
25153200	Strip, Marker, Narrow, 22-42	
24527400	Switch, Rotary, 8 pole, 2-5 positions	
24541002	Switch, Pushbutton, Momentary, Normally Closed, black	
38710000	Wire Tabs, Controller chassis	

PRINTED CIRCUIT CARD ASSEMBLIES, CONTROLLER CHASSIS
PARTS LIST

DATE: _____

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
50007400	Printed Circuit Card Assembly; Type UAB	
17678200	Printed Circuit Card Assembly; Type E08	
17678800	Printed Circuit Card Assembly; Type E11	
23445201	Printed Circuit Card Assembly; Type M63	
23445501	Printed Circuit Card Assembly; Type M64	
17683900	Printed Circuit Card Assembly; Type P14	
17684200	Printed Circuit Card Assembly; Type P15	
17684500	Printed Circuit Card Assembly; Type P16	
10335201	Printed Circuit Card Assembly; Type 73A	
10201801	Printed Circuit Card Assembly; Type 11	
10201901	Printed Circuit Card Assembly; Type 12	
10202000	Printed Circuit Card Assembly; Type 13	
10202501	Printed Circuit Card Assembly; Type 14	
10232201	Printed Circuit Card Assembly; Type 20	
10202801	Printed Circuit Card Assembly; Type 21	
10203401	Printed Circuit Card Assembly; Type 22	
10203501	Printed Circuit Card Assembly; Type 23	
10203601	Printed Circuit Card Assembly; Type 24	
10232501	Printed Circuit Card Assembly; Type 28	
10232801	Printed Circuit Card Assembly; Type 29	
10334401	Printed Circuit Card Assembly; Type 30	
10203701	Printed Circuit Card Assembly; Type 31	
10203801	Printed Circuit Card Assembly; Type 32	
10203901	Printed Circuit Card Assembly; Type 33	
10339201	Printed Circuit Card Assembly; Type 50	
10005900	Printed Circuit Card Assembly; Type 62	
10213501	Printed Circuit Card Assembly; Type 77	

6675 DATA SET CONTROLLER CDC Dwg. No. 38616100 thru. 38616103
PARTS LIST

*Final Assembly

DATE: _____

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
38612800	Angle, Mounting, Plate (2 used on 38616102 and 38616103)	
25163000	Angle, Mounting, Plate, chassis lower (3 used on 38616102 and 38616103)	
25151800	Cabinet, Assembly, Type B (2 used on 38616102 and 38616103 - see Publication No. 60097300)	
38606100	Chassis Assembly, D.C.A. (see Publication No. 38700100)	
38616200	Chassis Assembly, Multiplexer (see Page 3-2)	
38616300	Chassis Assembly, Control (2 used on 38616101, 3 used on 38616102, 4 used on 38616103 - see Page 3-3)	
38695600	Data Set (2 used on 38616101, 3 used on 38616102, 4 used on 38616103) (Specify Model No.)	
38614600	Emblem	
38613700	Member, Frame, Left Hand (used on 38616102 and 38616103 only)	
38613800	Member, Base, Full (used on 38616102 and 38616103 only)	
38613900	Member, Frame, Right Hand	
38613901	Member, Frame, Right Hand (used on 38616102 and 38616103 only)	
38614400	Member, Frame, Panel, Top, Full (used on 38616102 and 38616103 only)	
38614000	Panel, Filler (used on 38616100 and 38616102 only)	
38612500	Plate, Mounting, Shelf, Long (used on 38616102 and 38616103 only)	
38612600	Plate, Mounting, Shelf, short	
38612700	Plate, Mounting (used on 38616102 and 38616103 only)	
25162800	Plate, Mounting, Chassis	
38616000	Power Supply	
25151702	Power Supply (used on 38616102 and 38616103 only)	
38695300	Serial Plate; SSD, Large	
38613500	Shelf (3 used on 38616102 and 4 used on 38616103)	
38710000	Wire Tabs	

*These items are used in conjunction with the Controller and Multiplexer Chassis

CONTROL DATA
CORPORATION

SPECIAL SYSTEMS DIVISION

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