CONTROL DATA®
SINGLE ADDRESS ASYNCHRONOUS COMMUNICATIONS ADAPTERS

DJ142-A, DJ143-A

INSTALLATION AND
CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA

CONTROL DATA
CORPORATION
CUSTOMER ENGINEERING MANUAL

REVISION RECORD

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

MANUAL REV	FCO OR ECO	EQUIPMENTS					
		DJ142-A	DJ143-A				
B	ECO30102	A01	A01				
C	FCO30729	A02	A01				
D	FCO30730	A02	A02				
E	ECO31598	A03	A03				
F	ECO33325	A03	A03				
G	ECO34438	A03	A03				
H	ECO35699	A03	A03				

PREFACE

The DJ142-A and DJ143-A Single Address Asynchronous Communications Adapters (CAs) are integrated circuit communications devices which may be used separately for either sending or receiving data between a computer and the communications facility or may be used together as one unit. Each CA consists of two printed circuit board assemblies.

This manual contains installation and checkout procedures, a theory of operation, maintenance information and a parts list for each of the four printed circuit boards. The companion reference manual contains an introduction to and a detailed description of the CAs as well as relevant programming considerations.

This manual is intended for use with the publications listed below. These documents furnish information relative to the CAs but are beyond the scope of this manual.

361-1/2/3 Communications Adapter, Reference Manual
Pub. No. 41612200

364-1/2 Communications Multiplexer Reference Manual
Pub. No. 41610900

DJ808-A Communications Multiplexer Customer Engineering Manual
Pub. No. 41611000

364-4/5 Communications Multiplexer Reference Manual
Pub. No. 41612700

GH407-A Cabinet Assembly Reference/Customer Engineering Manual
Pub. No. 41614300

See the Literature Distribution Catalog for the latest revision.

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FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

SECTION 2

OPERATION AND PROGRAMMING

Information on these sections is contained in the 361-1/2/3 Communications Adapter Reference Manual, Pub. No. 41612200.

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION AND CHECKOUT

GENERAL

This section contains procedures for crating and uncrating, installation and checkout, and information on the environmental and electrical requirements pertaining to the units which comprise the two communication adapters (CAs).

CRATING AND UNCRATING

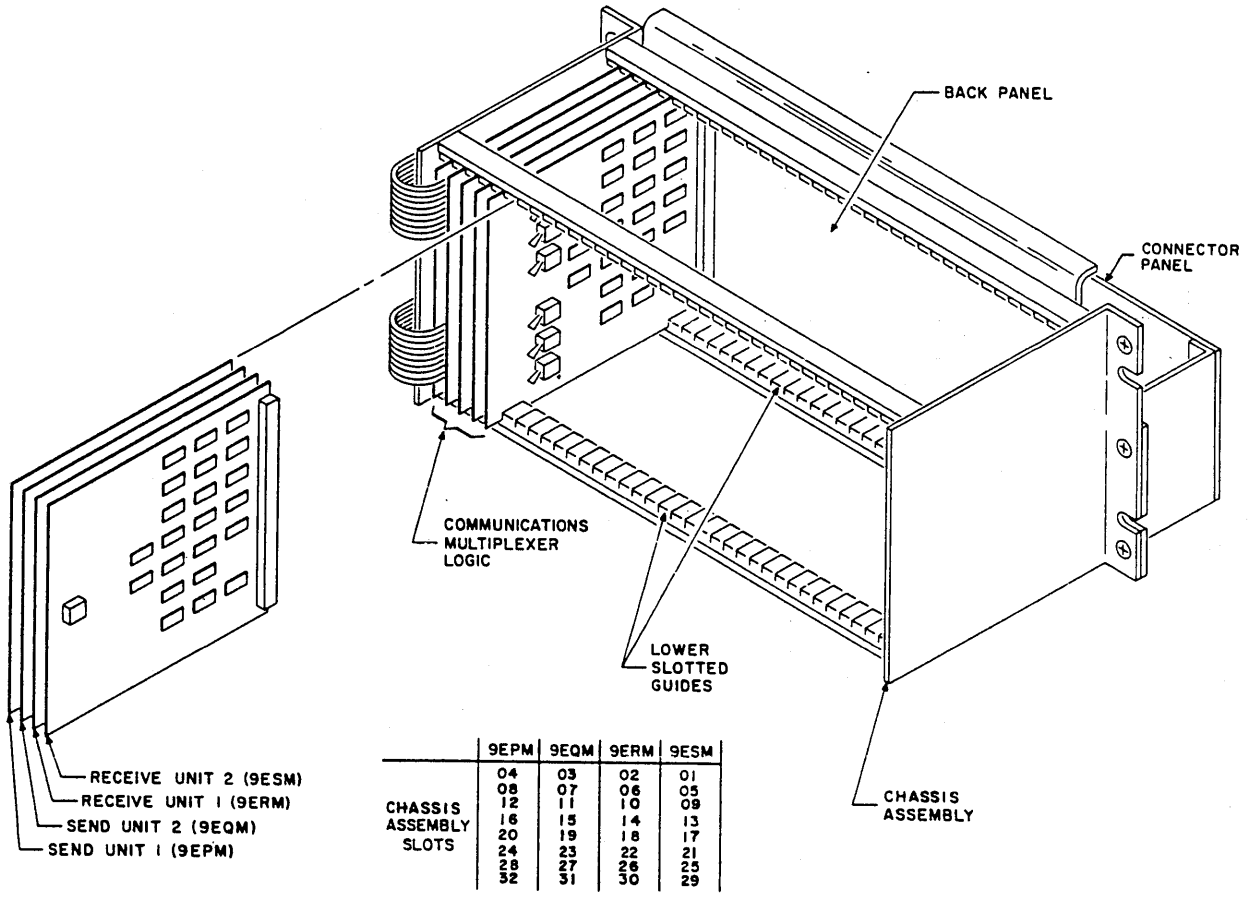
CAUTION

Although the integrated circuits and individual components mounted on the individual printed circuit boards can withstand a considerable amount of shock, the units must be handled with care. In no case should units ever be stacked one upon another because the printed circuit foil, components, or integrated circuits may be loosened or broken by such action.

The CA printed circuit boards are shipped installed in a chassis assembly or separately in a specially padded cardboard carton. When shipped in a cardboard carton, carefully unpack the units and inspect them for damage. If any unit is irreparably damaged in transit, refer to the Equipment Delivery and Inspection procedure (8:503:00) of the Field Procedures Guide for Customer Engineers to determine proper disposition of the damaged unit.

INSTALLATION

If both CAs are required in a communications system, four locations are required in a chassis assembly (see Figure 3-1) which is installed in a communications multiplexer cabinet. Slide both printed circuit boards of both CAs into the channel locations (as shown) of the chassis assembly via the upper and lower slotted guides provided. Be sure the boards make proper contact with the cage back-panel connectors. Table 3-1 lists pertinent installation data for each unit.



	9EPM	9EQM	9ERM	9ESM
CHASSIS ASSEMBLY SLOTS	04	03	02	01
	08	07	06	05
	12	11	10	09
	16	15	14	13
	20	19	18	17
	24	23	22	21
	28	27	26	25
	32	31	30	29

Figure 3-1. CA Installation

TABLE 3-1. INSTALLATION DATA

UNIT DIMENSIONS (Each Unit)	
Length	6.8 in.
Width	0.45 in.
Height	5.8 in.
Weight	5.0 oz.
OPERATING ENVIRONMENT	
Ambient Temperature	40° F to 120°F (5°C to 50°C)
Relative Humidity	10% to 90%
Cooling	Forced air from communications multiplexer cabinet blower
Heat Dissipation	20.5 Btu/hr
Power Dissipation	6.5 watts
STORAGE ENVIRONMENT	
Ambient Temperature	-30°F to 150°F (-34.5°C to 65°C)
Relative Humidity	5% to 95% (no condensation)
ELECTRICAL REQUIREMENTS	
Logic Voltages	+5.0 ± 0.5 vdc @ 1.2 amperes +12.0 ± 1.2 vdc @ 0.025 ampere -12.0 ± 1.2 vdc @ 0.020 ampere

PREPARATION FOR USE

SHORTING BLOCKS

Shorting blocks used for decoding, detecting, or generating specific signals or types of characters are installed on the printed wiring board which contains the logic circuit for that

NOTE

Equipment after series code A02 have wire wrap terminals in place of shorting block sockets. Shorting blocks short circuit two sockets together therefore, short circuit the wire posts by adding a wire between them.

function. Shorting blocks connect the foil path or paths of one circuit to the paths of another circuit on a printed wiring board and do not short out components. The units containing shorting block receptacles and their associated circuit functions are shown in Figure 3-2 and are listed as follows:

1. Send Unit 1 9EPM

   Enable/Disable Break signal selector (EN BRK/DIS BRK)

   Half-duplex/full-duplex selector (HDX/FDX)

2. Send Unit 2 9EQM

   5-, 6-, 7-, or 8-bit data signal generator

   1-, 1.5-, or 2-bit stop pulse generator (1 SP/1.5 SP/2SP)

   Restraint signal selector (EN/DIS)

   Clock speed selector (W1/W2)

3. Receive Unit 2 9ESM

   5-, 6-, 7-, or 8-bit data signal generator

   Clock speed selector (P1/P2)

Install shorting blocks on the printed wiring board(s) according to the type of function desired. For example, if detection of a Restraint signal is required, insert a shorting block in the EN and ground (center) jacks on Send Unit No. 2 (9EQM assembly).

CLOCK ADJUSTMENT

Clock circuits in both the Send and Receive Units must be adjusted to synchronize with the bit rate of the incoming data. The specific clock speed depends upon the type of communications facility and communications line used. The clock in either unit is capable of operating within either of two ranges: 50 to 250 bits per second (bps) or 225 to 3000 bps.

Proceed as follows.

1. Using an oscilloscope such as the Tektronix Type 545B or equivalent, set the TIME BASE A TRIGGERING MODE rotary switch to DC and the TRIGGER SLOPE rotary switch to INT.
2. Place the oscilloscope probe on test point 18 for checking or adjusting the clock in the send section (see logic diagrams, output of I241 on 9EQM board). All test points are located on the outer edge of each board and are numbered 1 through 30.

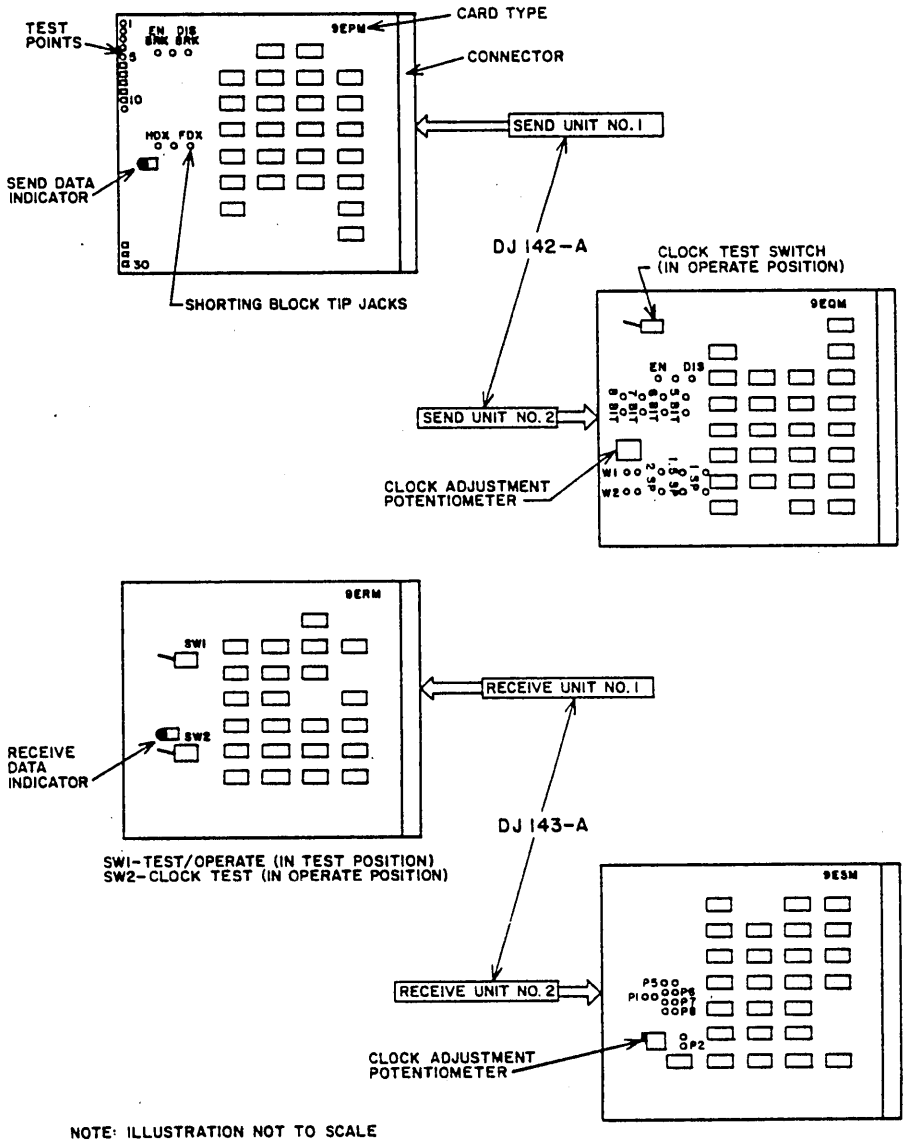


Figure 3-2. CA Card Layout

3. To start the clock, switch the Clock Test switch from Operate to Test.

4. If necessary, adjust the clock adjustment potentiometer (Figure 3-2) with a hexagonal screwdriver so that two consecutive clock pulses correspond to the period of the bit. The bit rate (bits per second) varies inversely with the period (pulse width) of the bit.

5. Use the same procedure as given in steps 1 through 4 to adjust the clock in the receive section. However, place the oscilloscope probe on test point 20 (output of I162) on the 9ESM board.

FINAL CHECKS

Prior to releasing the CA for service, check the following:

1. Is the Test/Operate switch on Receive Unit 1 in the Operate (up) position?

2. Are the Clock Test switches on Receive Unit 1 and Send Unit 2 in the operate (up) position?

3. Is Break signal character detection required? If so, install a shorting block in the appropriate jacks.

4. Is Restraint signal detection required? If so, install the shorting block in the EN position on Send Unit 2 printed wiring board.

5. Are the shorting blocks installed in the appropriate character length jacks on the Send and Receive Unit printing wiring boards?

6. Do the shorting blocks occupy the correct Stop pulse generator jacks on Send Unit 2?

7. On Send Unit 1, are the jacks properly selected for Half- or Full-Duplex operation?

SECTION 4

THEORY OF OPERATION

THEORY OF OPERATION

GENERAL

This section contains a detailed theory of operation for the DJ142-A Send Unit and the DJ143-A Receive Unit. This section also contains a functional description of the overall operation of the two units, which is followed by a detailed logical description.

FUNCTIONAL DESCRIPTION

SEND UNIT

Refer to Figure 4-1, Send Unit Functional Block Diagram, in understanding the discussion of the following paragraphs.

The Send Unit may request a 12-bit output word provided the communications multiplexer has previously enabled the character request circuit in the Send Unit. This request is made via the data channel when the communications multiplexer generates the proper address and the Select Input control signal.

Eight bits received via the output word are data and are in turn serially transmitted to the data set. Bits 8 and 9 of the 12-bit word are unassigned, and bits 10 and 11 control the break circuit.

The Enable Character Request signal must be present in the Send Unit before an output operation can begin for either Half- or Full-Duplex operation. In Half-Duplex operation, receipt of the Enable Character Request signal from the communications multiplexer activates the request-to-send circuit in the Send Unit and inhibits the receive logic circuits in the Receive Unit. In Full-Duplex operation, the Enable Character Request signal does not control the request-to-send circuit. When the Send Unit receives the Select Output control signal from the communications multiplexer, the data character is gated into the holding register, the character request circuit is disabled, and tne clock control circuits begin operation. The clock control circuit starts the clock which gates the character currently in the holding register to the serializing shift register. An even clock pulse also forces the Send Unit to transmit a start pulse to the data set.

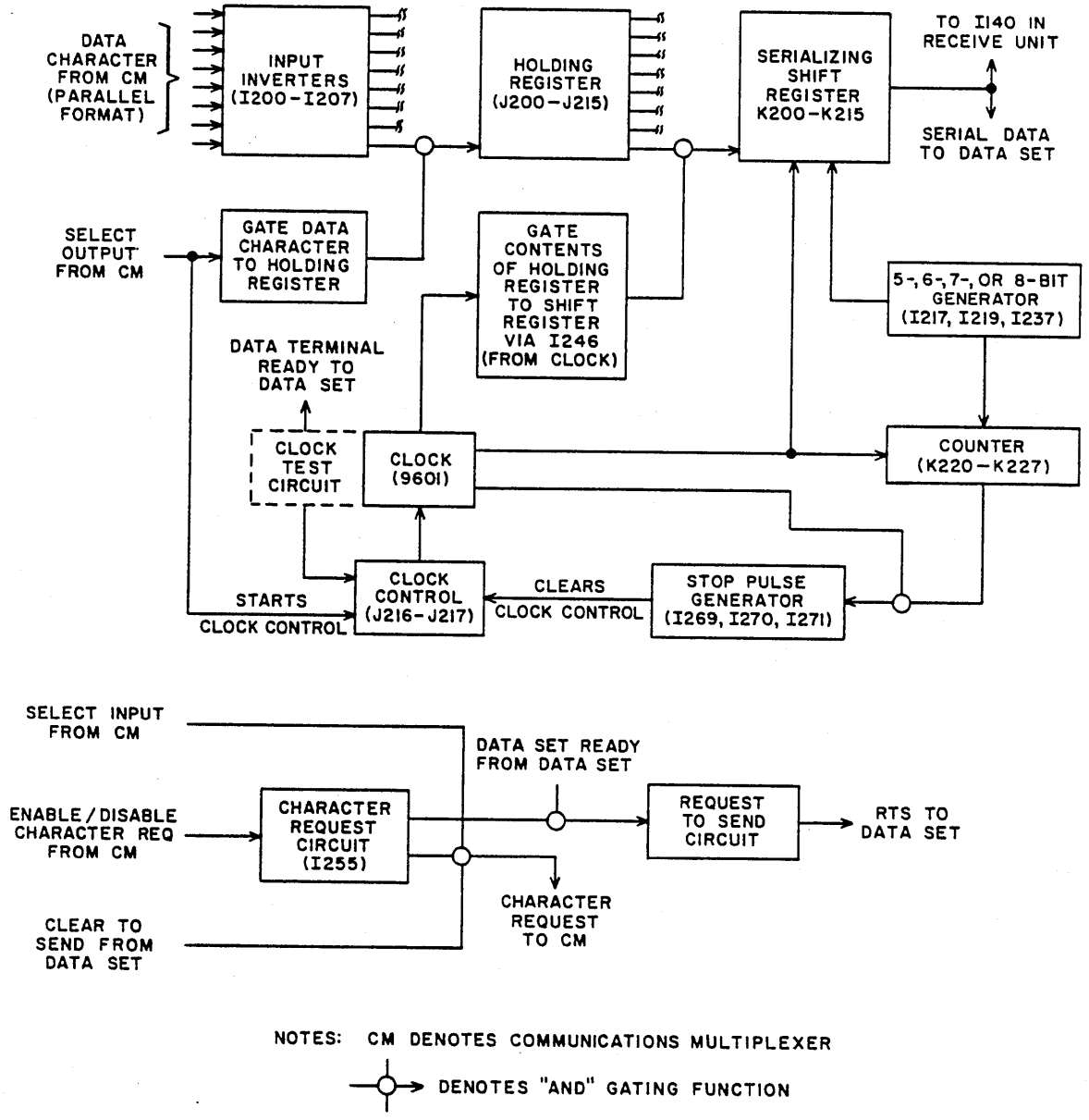


Figure 4-1. Send Unit Functional Block Diagram

The character request circuit is re-enabled because the holding register can accept a new data word before the current data word is completely gated through the serializer. (The Select Input control signal gates the Character Request signal (bit 10) to the communications multiplexer.) If a new data word is available, it is gated into the holding register and, simultaneously, the character request circuit is disabled.

Following the first odd clock pulse from the clock circuit, the next even clock pulse and succeeding even clock pulses gate the first data word through the serializer. A four-stage counter decodes the even clock pulses and enables the appropriate gate in the stop pulse circuit. The new, or second, data word temporarily stored in the holding register is then transferred to the serializing shift register and sent to the data set.

RECEIVE UNIT

The Receive Unit accepts serial data from the data set and transfers an 11-bit input word to the communications multiplexer data channel when the communications multiplexer generates the Select Input control signal and the proper address. The input word contains eight data bits and three data status bits which indicate a break, a lost character, or a character ready condition. Refer to Figure 4-2 as an aid to understanding the following discussion.

Receipt of a start pulse from the data set starts the clock, which in turn, initiates operation of the clock control circuits. The clock control circuits maintain operation of the clock and terminate its operation at the proper count of the counter. The clock output starts the counter and gates the incoming serial data into the shift register (serial-to-parallel conversion). Outputs of both the clock and the counter gate the contents of the shift register to the holding register. The Select Input signal from the communications multiplexer gates the data character contained in the holding register and the status bits to the communications multiplexer. The Receive Unit also contains a circuit which generates a signal to make it compatible with systems using 5-, 6-, or 7-bit, as well as 8-bit, data characters.

LOGIC DESCRIPTION

As an aid to understanding the following logic discussion, use the logic diagrams in Section 5 and the table of interconnections (Table 7-2) in Section 7.

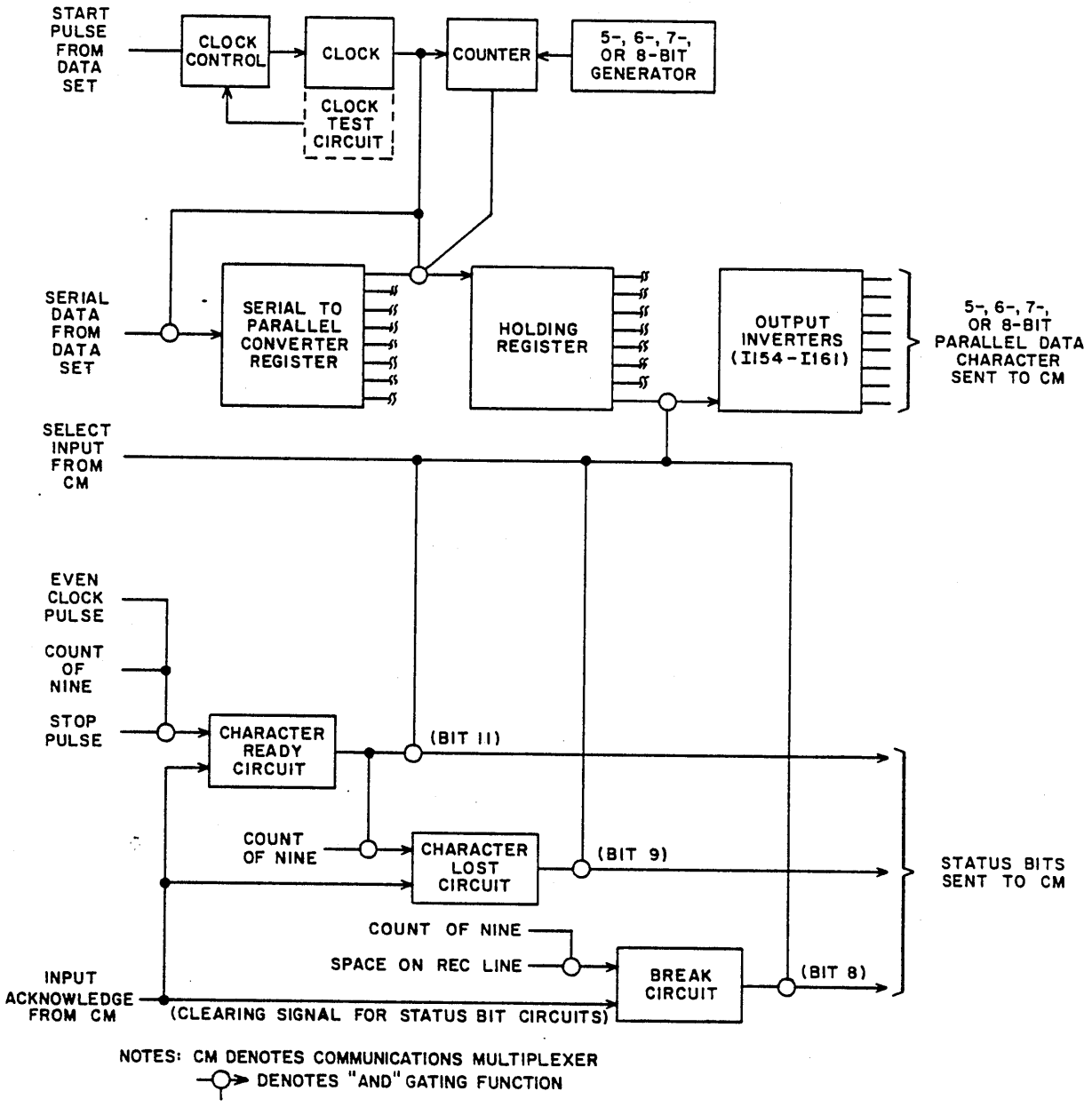


Figure 4-2. Receive Unit Functional Block Diagram

DJ142-A SEND UNIT

When the communications multiplexer is ready to transfer data to the data set, the communicatons multiplexer issues the Select Output control signal which is received as a "0" at I253 in the Send Unit. The output data word (eight data bits) is also received at inverters I200 through I207. As soon as the output of I253 becomes a "1", the output data word is gated to the output holding register FF's via inverters I208 through I215. Also the "0" output of I254 sets FF's 226/227 and J218/219. FF J218/219 initiates operation of the clock control circuits via I249. Refer to the paragraph, Request-to-Send signal, for a description of the sequence of events related to the setting of FF J226/227.

Clock and Clock Control

Refer to Figure 4-3 as an aid to understanding the following logic disucssion.

The Send Unit uses a 9601 retriggerable monostable multivibrator as an internal source of clocking signals. The multivibrator requires four inputs for proper operation. Two inputs must be logical "1's" and of the remaining two, one must be a logical "0". Each time the triggering conditions at the multivibrator input are met, the external capacitor is discharged in a proportionate length of time, and another cycle is complete.

Initially, the Send Unit Start FF (J216/217)in the clock control circuit and FF K228/229 are clear, and the clock is not operating. As soon as FF J218/219 sets, and provided the Clock Test switch (see Figure 3-2) is in the operate (Up) position, the Start FF sets, conditioning the gate at the clock (multivibrator). The set output of the Start FF is applied to I235 where it is AND gated with the output of I243. The output of I235, a 1.5 μsec pulse, enables the gate at I234. The output of I234 provides a positive pulse which completes the triggering requirements at the multivibrator when I234 changes to logical "0", thereby starting the clock. The length of time that the logical "0" output of the clock is available at pin 6 is determined by the external variable resistor R2 and capacitor C10 or C11. The clock output is applied to I283 and I252, which in turn controls the feedback signal to I234. When the clock output returns to a logical "1", it initiates the charging operation of capacitor C12. While the capacitor is charging, the AND gate at I252 is enabled and provides a "0" input for I234, which in turn supplies a positive pulse at pin 1 of the clock. The clock, therefore, recycles on the trailing edge of the positive pulse, repeating the sequence (see Figures 4-3 and 4-4).

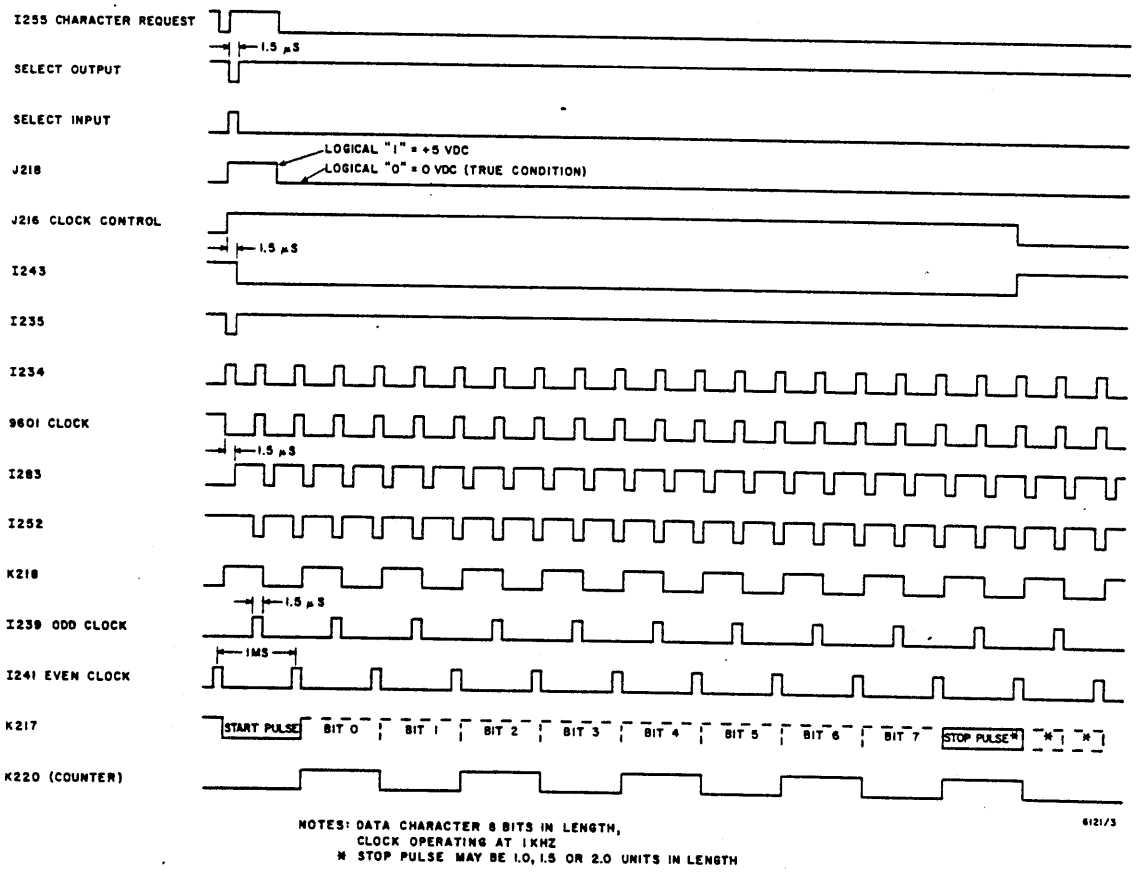


Figure 4-3. Send Unit Clock Timing Diagram

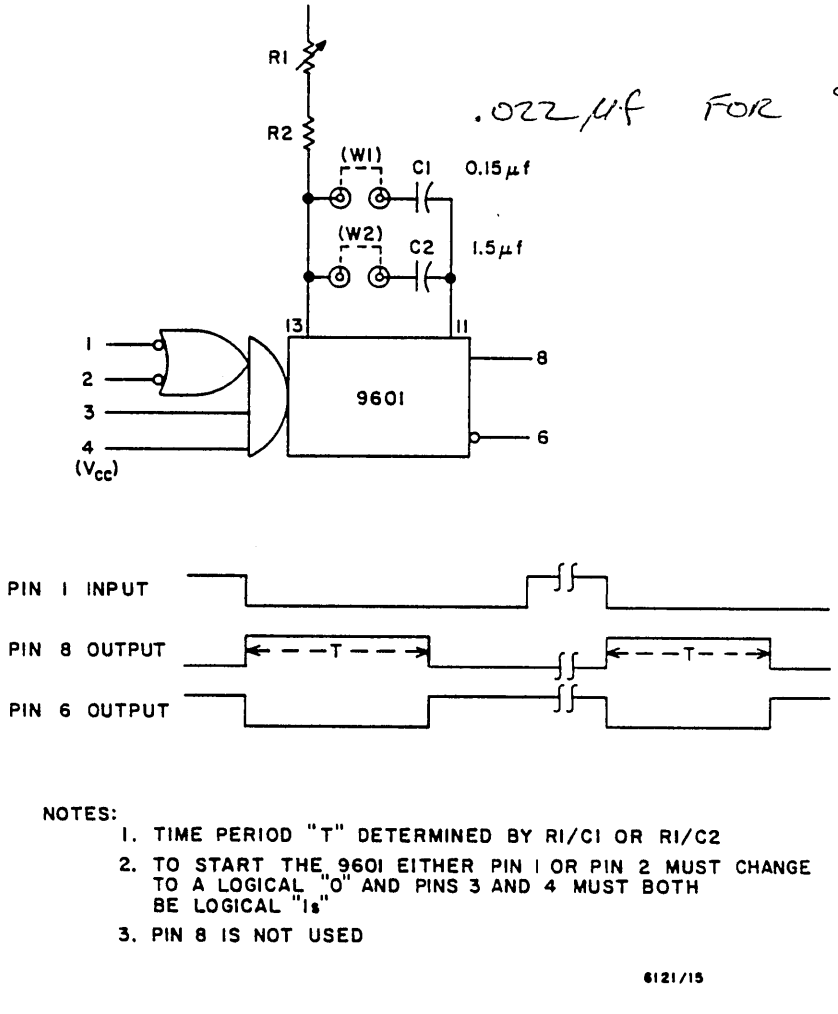


Figure 4-4. Monostable Multivibrator Timing Diagram

The alternating output of I234 is also used as the trigger input to JK FF K218/219, which in turn causes I239 and I241 to produce the odd and even clock pulses, respectively. Each time the output of I234 changes from logical "1" to logical "0", K218/219 either sets or clears, depending upon the conditions at the J or K inputs. The first pulse output of I234 sets the FF, while the second clears it, and so on.

The output of the odd clock inverter (I239) is applied to I270 in the stop pulse generator and to I242 in the shift register control circuit. The signal applied to I270, however, does not become effective until the count specified by the counter is established. Since K228/229 is initially clear, the first logical "1" odd clock pulse output of I239 forces I242 to a logical "0", thereby causing I236 to clear J218/219 via I251, and causing I244 to set K228/229.

Output of the even clock inverter (I241) is applied to I269 and I271 in the stop pulse generator circuit, to the gating circuit related to the output shift register (I247 and I248), and to the circuit which controlls the counter trigger pulse (I245 and I246).

Clock Test

If it is either desirable or necessary, the clock-initiation circuit, the clock, and the counter may be tested using the clock test switch that is mounted on the 9EQM printed circuit board of the Send Unit. During normal operation, the switch is set to the Operate position as shown on the logic diagrams (refer to Section 5) and on Figure 3-2. However, when set to the Test position, a logical "0" sets the clock control FF J216/217 which initiates operation of the clock via I235 and I234. When the switch is returned to the Operate position, I233 and I263 form a negative pulse of approximately 100 ms clearing the clock control FF and stopping the clock and counter. In the Operator position, the logical "1" output of I262 is transferred to the data set via S202 as the Data Terminal Ready signal and remains on as long as the switch is set at Operate.

Counter (8-Bit Operation)

The counter consists of four JK FF's, K220/221 through K226/227, and is capable of counting to a maximum value of 15. Initially, all stages in the counter are clear. The first odd clock pulse of I239 sets FF K228/229, thereby enabling the gate at I245. This allows the next even clock pulse of I241 and succeeding even clock pulses through the gate. The trailing edge of the second even clock pulse sets K220/221. The set output of K220/221 is applied to its own K input and provides the trigger input for the second stage, K222/223. The third even clock pulse of I246 clears K220/221 thereby changing the level at K222/223 to logical "0" and setting the FF. Since the clear output of K220/221 is fed back to its own J input, the fourth even clock pulse sets K220/221 and allows K222/223 to remain set. The fifth even clock pulse

from I246 clears K220/221 which in turn changes the trigger level at K222/223 to logical "0", clearing the FF. In this manner, a new count is established with each even clock trigger pulse supplied by I246. (See Figure 4-5.)

Outputs of the first two stages of the counter are gated with the odd or even clock pulses in the stop pulse generator which, with I285, clears Start FF J216/217. Clearing the Start FF stops the clock and the counter.

Counter (5-, 6-, and 7-Bit Operation)

The Send Unit may be used in systems with 5-, 6-, or 7-bit, as well as 8-bit, data characters and, therefore necessitates a change in operation of its counter circuit. To initiate proper operation of the counter, a shorting block is installed in the appropriate jacks on the 9EQM printed circuit board prior to system operation.

When a 5-bit data character is in use, the constant "1" output of I237 (representing the 5-bit signal) is applied to I273 and I223, force-setting the first two stages of the counter. The first odd-clock pulse via I244 enables the gates at I223 and I273 which force-set the first two stages of the counter, thereby starting at a count of three. Subsequent operation of the counter is then identical with the description given in preceding paragraphs for counter operation associated with 8-bit data characters.

When either a 6- or 7-bit data character is used, the constant "1" output of either I217 or I219 is applied to either I225 or I221. The first odd clock pulse via I244 enables either I225 or I221 force-setting either stage two or stage one of the counter for the 6-bit or 7-bit data character respectively. Therefore, the counter begins counting from a count of two for the 6-bit character and a count of one for the 7-bit character. Subsequent operation of the counter remains the same as that for an 8-bit data character operation.

Holding Register

The holding register consists of eight RS FF's, J200/201 through J214/215. Eight data bits are received in parallel format from output inverters I200 through I207 as gated to I208 through I215 by I253.

If the holding register is accepting 5-bit data characters, the 5-bit signal from I237 via I294 sets stage two of the register. If 6-bit data characters are received, the 6-bit signal from I217 via I295 sets stage two. The "1" output of I253 represents the NOT Select Output signal from the communications multiplexer and gates data from the output inverters to the holding register. The output of I246 is also applied to I276 and I277 which set or clear the Break FF J244/225.

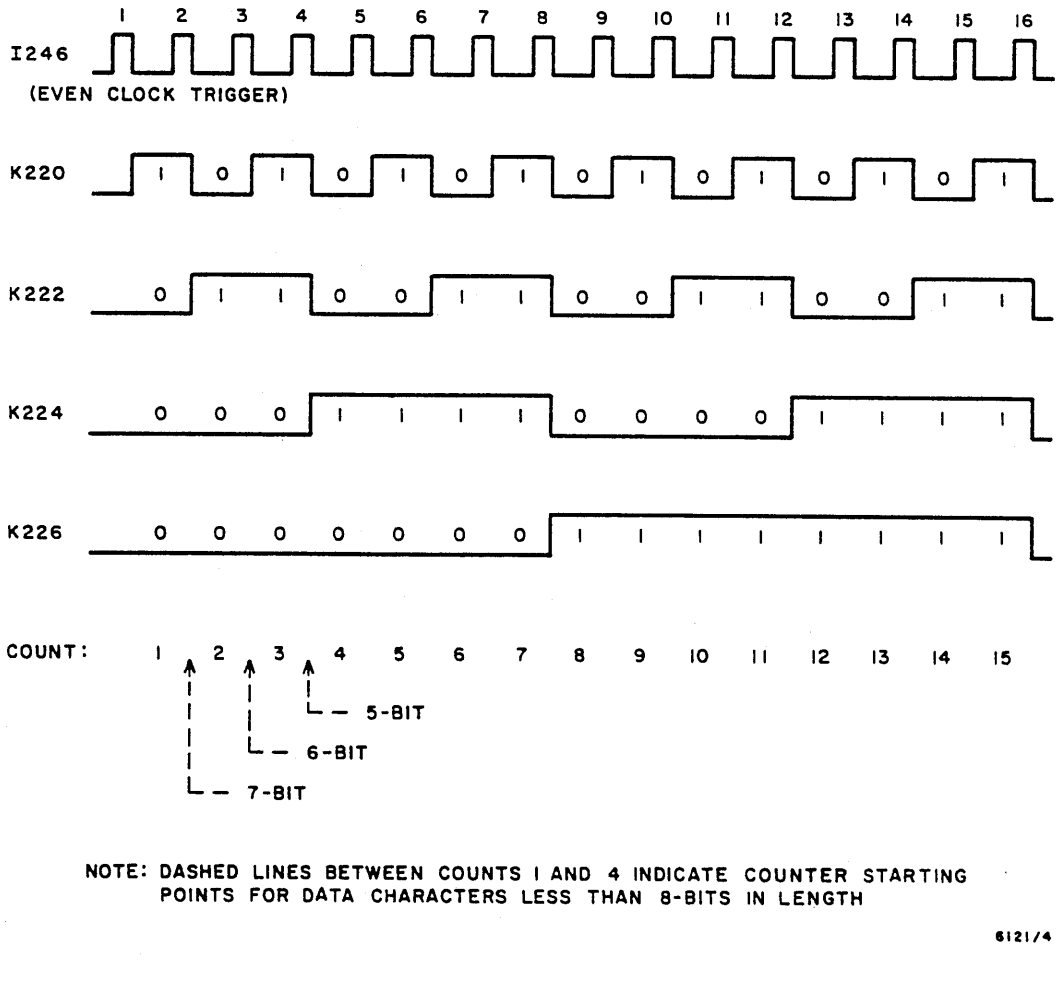


Figure 4-5. Send Unit Counter Timing Diagram (8 Bit Operation)

Shift Register

Outputs of the holding register FF's are gated to the serializing shift register (JK FF's K200/201 through K216/217) via inverters I216 through I230, which in turn receive the second even clock gating pulse from I248 (Figure 4-6). Since the first even clock pulse occurs before the first odd clock pulse, the second even clock pulse is gated through I247, forcing I248 to a "1" and thereby gating the character in the holding register to the serializing shift register. Since the first odd clock pulse sets FF K228/229 via I242 and I244, the gate at I245 is enabled and allows subsequent even clock pulses to pass through I246. For each stage in the holding register which was set, the corresponding stage in the shift register is forced to set via the corresponding output inverter when I246 is a "1".

The outputs of the even clock inverter, I241 and K228/229, provide the means by which data is gated through the serializing shift register to the send data line. The output of I246 provides the even clock trigger pulse for the first-stage counter FF, K220/221, and for the serializing shift register FF's.

The second even clock trigger pulse of I246 occurs after the transfer of data from the holding register to the shift register and the bits in each JK FF are simultaneously shifted to the next stage thereby sending one bit through the serializer circuits. Beginning with K200/201, the second even clock trigger pulse from I246 either sets or clears the FF which in turn becomes the input for the next stage. The third even clock trigger pulse either sets or clears the second stage. The process continues until each data bit in each stage of the serializing register is transferred to the succeeding stage. Providing Break FF J224/225 is clear, data bits are transferred to the data set via JK FF K216/217 and logic elements I278, I229, and S200. Indicator lamp L2 lights each time a data bit from K216/217 is gated through I296.

Request to Send Signal

The Send Unit generates the Request-to-Send signal and conditions the data set to transmit. During the transmission of the Request-to-Send signal, the data set transmits its Carrier signal. However, the generation of the Request-to-Send signal is directly controlled by FF J222/223 and is indirectly controlled by FF's J226/227 and J228/229.

During the half-duplex mode of operation, FF J222/223 is controlled by the Enable Character Request FF, J220/221. The Request-to-Send signal stays active as long as FF J220/221 is set. FF J220/221 is cleared by the logical "0" output of I288 or by a Master Clear signal via I260 and I261.

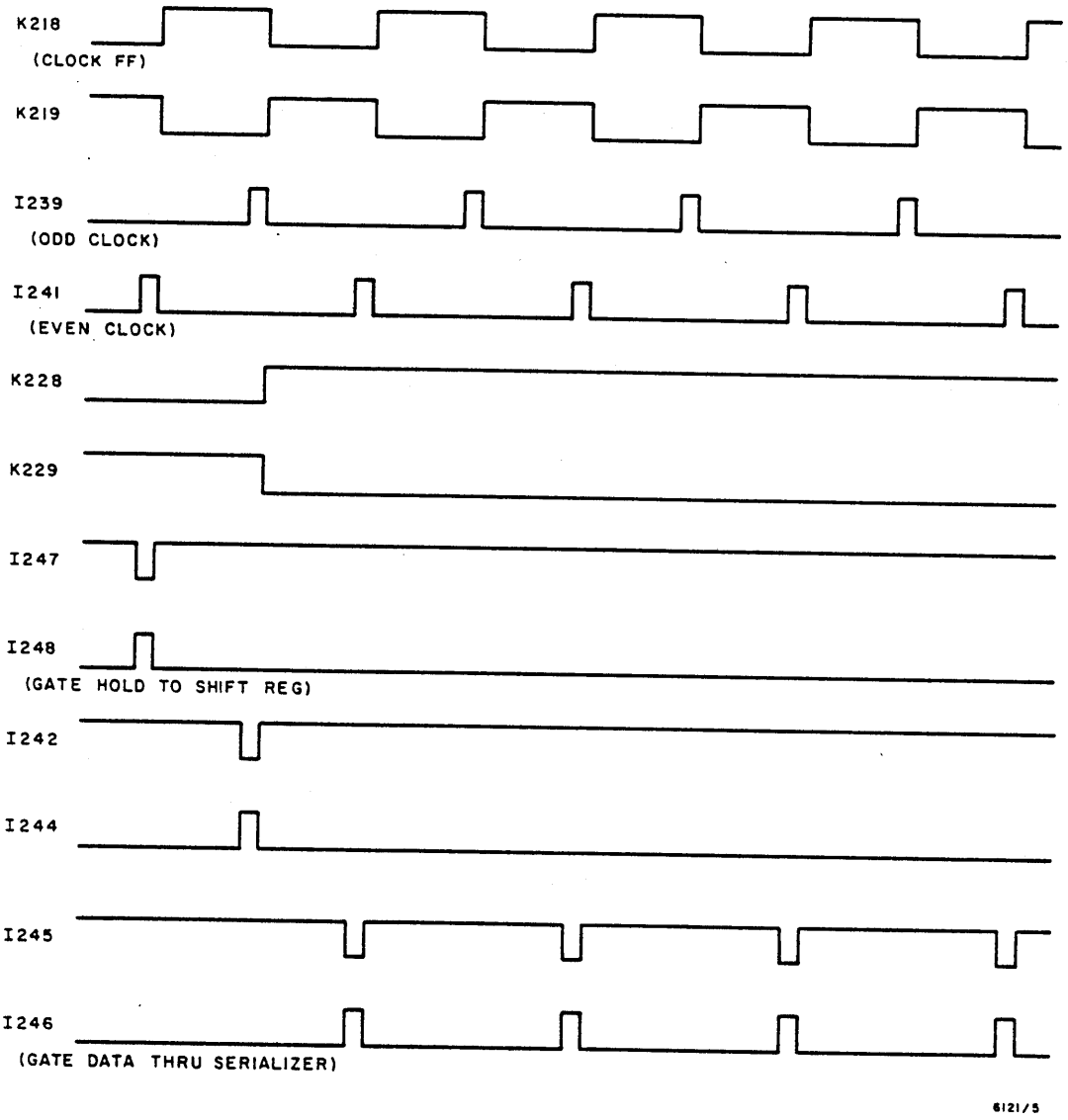


Figure 4-6. Gating Contents of Holding Register to Shift Register Timing Diagram

In the full-duplex mode of operation, the shorting block grounds the set input of FF J222/223, setting the FF. The set output enables I281, provided a Data Set Ready signal is received from the data set via R200 and I282. Therefore, the Request-to-Send signal is sent to the data set via S201 and remains on as long as J222/223 remains set.

Stop Pulse Generator

The stop pulse circuit generates any one of three signals following each serial data character: a 1-bit stop pulse, a 1.5-bit stop pulse, or a 2-bit stop pulse. A shorting block installed on the 9EQM printed circuit board prior to initial operation determines which of the three pulses will be generated. The even and odd clock pulses and the counter provide the inputs to I269, I270, or I271 which in turn are applied to I250. If the shorting block is inserted to obtain a 2-bit stop pulse, I271 becomes a "0" when K222 in the counter sets and when an even clock pulse from I241 is received. The "1" output of I250 is applied to the AND gate at I285 which becomes enabled at a count of 10 (K224/225 cleared, K226/227 set). When NAND gate I285 is enabled, the "0" output clears Start FF J216/217 and stops the clock and the counter.

Character Request/Restraint Signals

When the Send Unit receives an Enable or Disable Character Request control signal from the communications multiplexer, either I256 or I258 is forced to a "1". The particular Character Request signal is accompanied by the Select Input signal, which forces I272 to a "1" which in turn is one of five signals required for enabling I255. If the Enable Character Request signal is received, I257 is forced to a "0" and FF J220/221 sets, providing one of the required inputs at I255. Since the Select Output signal is not present at I253, FF J218/219 does not set. However, the "0" output of I236 from the previous character clears FF J218/219 and applies a logical "1" to I255. The "1" from I242 forces I236 to a "1" and I268 transfers this "1" to I255, enabling its gate. The fifth input required by I255 is received from I267, and indicates whether a Restraint, Clear-to-Send, or Test signal is present at R202, R201, or I267, respectively.

If a shorting block is installed on the 9EQM printed circuit board to detect the reception of a Restraint signal at I289, the output of I266 is forced to a "1" even if a Clear-to-Send signal is received at R201. If the NOT Test Mode signal (a "1" from I262) is present at I267, NAND gate I255 becomes disabled, and the Character Request signal is not transferred to the communications multiplexer. Therefore, the Restraint signal prevents the Send Unit from requesting another data character from the computer for transmission to the data set.

If the Restraint signal detection option is disabled, the gate at I266 is enabled, thereby allowing the Clear-to-Send signal which was received from the data set at R201 to force the output of I266 to a "0" and I267 to a "1". Therefore, the gate at I255 is enabled and the Character Request signal is sent to the communications multiplexer.

Either the disable Character Request or Master Clear signal received from the communications multiplexer at I258 or I260, respectively, may clear the Enable Character Request FF J220/221. The cleared state of J220/221 keeps I255 disabled and again prevents the transfer of the Character Request signal to the communications multiplexer.

Break Generator

When bit 10 of the Send Unit's input word is received as a "0" at I274 and is accompanied by a Select Output signal from the communications multiplexer at I253, NAND gate I276 is enabled, and the Break FF J224/225 sets. Therefore, the gate at I278 is disabled, and data cannot be transferred to the data set. Setting of the Break FF transfers a constant spacing signal to the data set via S200 (send data line).

A shorting block, inserted in the proper jacks on the 9EPM printed circuit board, enables or disables break circuit FF J224/225. In the Enable Break position, the Break FF is cleared by a "0" from the communications multiplexer in bit position 11 as received at I275 in the Send Unit.

The Select Output signal from I253 enables NAND gate I277, and the Break FF clears. However, if the shorting block is inserted in the Disable Break position, I275 is forced to a "1" which is gated with I253, clearing the Break FF.

Master Clear Signal

When a Master Clear signal is received from the communications multiplexer at I260, I261 is forced to a "0" and provides the signal to accomplish the following logical operations:

1. Clears Enable Character Request FF J220/221.
2. Clears Start FF J216/217.
3. Clears Clock FF K218/219.
4. Indirectly clears J218/219 via I251 and I236, and indirectly clears J226/227 via I251 and I236.
5. Indirectly disables Character Request NAND gate (I255) via I268.
6. Clears Request to Send FF J222/223.
7. Clears Break FF J224/225.

After the proper exchange of signals (refer to Functional Description) between the communications multiplexer and the Receive Unit and between the Receive Unit and the data set, the Receive Unit may accept data from the data set. As soon as the logical "0" start pulse of the first data character is received at R100, the clock control and clock circuits are activated (see Figure 4-2).

Clock and Clock Control

Use the Receive Unit Functional Block Diagram (Figure 4-2) and the logic diagrams in Section 5 as aids to understanding the following logic discussion.

Like the Send Unit, the Receive Unit also uses a 9601 retriggerable monostable multivibrator as the source of clocking signals. The multivibrator requires four inputs for proper operation. Two of these inputs must be logical "1's" and, of the remaining two, one must be a logical "0". Initially, the output of I105 is a "1" but provides one of the required logical "0" inputs during start pulse time. Inverter I103 provides one of the required logical "1" inputs to the multivibrator during character reception time. The alternating output of I143 provides the second logical "0" input, and the second logical "1" input is supplied at pin 4. The external variable resistor (R1) and capacitor (C1 or C2) connected between pins 11 and 13 of the multivibrator determine the length of time that the logical "0" output of the clock is available at pin 6.

As soon as the Receive Unit detects the logical "0" start pulse from the data set via R100, I140 forces I141 to a "0" and I146 enables the gate at I105. The logical "0" output of I105 provides the initial pulse to start the multivibrator. The logical "1" output of I146 also conditions the gate at I100 in the clock control circuit. Because the output of the multivibrator at pin 6 is delayed by the external resistance and capacitance network connected between pins 11 and 13, capacitor C3 begins to charge when the signal at pin 6 becomes a "1". The output from pin 6 is also applied to I142. Logic elements I142 and I175 and capacitor C3 constitute a pulse forming network and produce a 1.5 μsec pulse at the conclusion of the multivibrator's delay time. Therefore, the pulse output of I176 enables I100 in the clock control circuit. The "0" output of I100 sets the Start/Stop FF J100/101 which conditions I144 and also initiates the operation of a 1.5 μsec delay developed by capacitor C7 connected to I170. The set output of the Start/Stop FF is also applied to I144 and I173. The network of I173, I174, and FF I101/102 is used to ensure that the even clock pulses occur at the midpoint of each bit period. When capacitor C7 is fully charged, I144 becomes a "1", enabling the gate at I143. The "0" output of I143 (the trailing edge of a positive pulse) again completes the triggering requirements of the multivibrator at pin 1, thereby causing it to recycle each time I104 produces a logical "0" pulse (Figure 4-7).

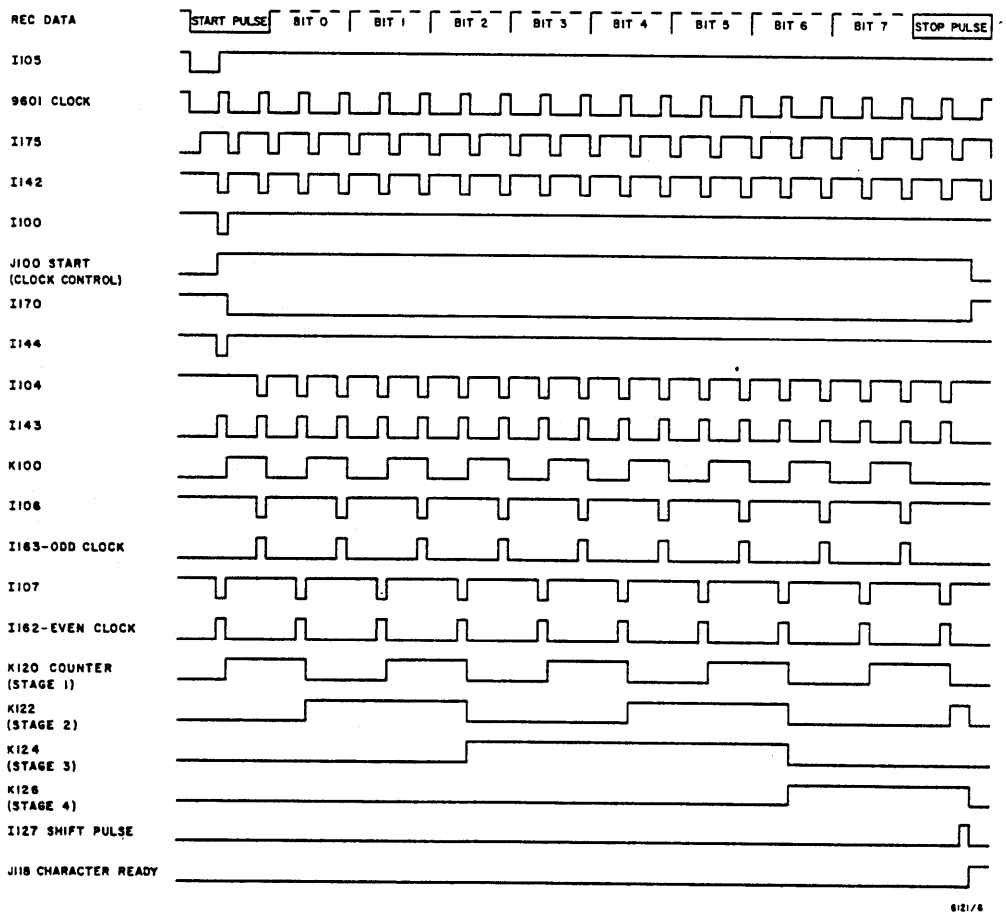


Figure 4-7. Receive Unit Clock Timing Diagram

The alternating output of I143 provides the trigger input to JK FF K100/101 which in turn causes I163 and I162 to produce the odd and even clock pulses, respectively. Each time I143 changes from logical "1" to logical "0", K100/101 either sets or clears. Because the set output of the Start/Stop FF J100/101 initially cleared K100/101, the first "0" pulse output of I143 sets K100/101, while the second clears it, and so on. Output of the even clock inverter (I162) provides the trigger pulse for gating serial data into the converter. It is also gated with K120 and K126 (count of nine from the counter) at I128 to clear the Start/Stop FF, and provide the trigger pulse required for starting the counter.

Clock Test

The clock control circuit, the clock, and the counter may be tested using the Clock Test switch that is mounted on the 9ERM printed circuit board of the Receive Unit. During normal operation, the switch is set to OPERATE, as shown on Figure 3-2 and on the logic diagrams in Section 5. However, when set to the TEST position, a logical "0" sets Start/Stop FF J100/101 which initiates operation of the clock via I170, I144, and I143. When the switch is returned to the OPERATE position, I168 and I145 form a negative pulse of approximately 100 ms and I145 clears the clock control FF, stopping the clock and the counter.

Counter (8-Bit Operation)

The counter consists of four JK FF's, K120/121 through K126/127. Initially, all stages in the counter are clear. When the output of I162 becomes a logical "0", I162 provides the first even clock trigger pulse which sets K120/121. The set output of K120/121 is applied to its own K input and to the trigger input of the second stage, a K122/123. The second even clock trigger pulse from I162 clears K120/121, thereby changing the level at K120/121 to logical "0", setting the FF. Since the clear output of K120/121 is fed back to its own J input, the third even clock trigger pulse sets K120/121 and allows K122/123 to remain set. The fourth even clock trigger pulse clears K120/121 which in turn changes the level at K122/123 to logical "0", clearing the FF. In this manner, a new count is established with each even clock pulse supplied by I162. Refer to Send Unit Counter Timing Diagram (Figure 4-5) for timing relationships which also apply to the Receive Unit counter. Outputs of the first and last stages of the counter are applied to I128 which, when enabled, forces I194 to a logical "1", thereby enabling the gates which transfer the contents of the serial-to-parallel converter to the holding register. NAND gate I128 also monitors the outputs of K120/121 and K126/127 in the counter. When an even clock pulse (I162) and a count of nine (K120 and K126) are present at I128, the Start-Stop FF clears and stops the clock. The clear output of the Start-Stop FF and the output of I132 are gated at I098, which, when enabled, force-clears all stages of the counter.

Counter (5-, 6-, and 7-Bit Operation)

Like the Send Unit, the Receive Unit may be used in systems with 5-, 6-, or 7-bit, as well as 8-bit, data characters. To initiate operation of the counter for use with data characters containing less than eight bits, a shorting block is installed in the appropriate jacks on the 9ESM printed circuit board prior to system operation.

When a 5-bit data character is in use, the constant "1" output of I164 is applied to I178 and I184 preceding the first two stages of the counter. When the output of I144 becomes a "0", I177 is forced to a "1" and conditions I178 and I184. The 5-bit signal, generated by I164, enables I178 and I184 which in turn force-set the first two stages of the counter, thereby starting it at the count of three. Subsequent operation of the counter is then identical with the description given in preceding paragraphs for counter operation associated with 8-bit data characters. When either a 6- or 7-bit data character is used, the logical "1" output of either I181 or I182 is applied to either I185 or I183. When the output of I144 becomes a "0", either I185 or I183 is enabled via I177. Either the second counter stage force-sets for 6-bit data character operation, or stage one force-sets for 7-bit data characters. Therefore, the counter begins with a count of two for the 6-bit data character and a count of one for the 7-bit character. Subsequent operation of the counter remains the same as that for 8-bit data character operation.

Shift and Holding Registers

Data pulses are received at R100 and gated at I140 which is enabled by the logical "1" from I280 in the Send Unit, a "1" output from the TEST MODE switch, and the logical "1" data pulses received at R100. Since the data bits alternate from one logical state to the other, the gate at I140 is alternately enabled or disabled, depending upon the logical state of the data bits received. Therefore, these data bits and the 8-bit signal from I180 enable or disable the gate at I147. The outputs of I148 and I147 are applied to the J and K inputs, respectively, of the first stage (K102/103) of the serial-to-parallel converter register. This register, consisting of the eight JK FF's K102/103 through K116/117, is used for loading the eight serial data bits of each data character into the Receive Unit and for shifting that data character in a parallel format to the holding register.

The Even Clock signal of I162 is inverted by I124 and is gated at I125 with set output of the Start-Stop FF. When enabled, the output of I125 provides the trigger pulse for each of the eight JK FF's. As data bits are loaded into the first stage of the register via I147 or I148, the trigger pulse enables the transfer of information to the second stage (Figure 4-8). In this manner, the received data bits are shifted in succession from one stage to the next, until the eight stages of the register contain the information representing one 8-bit character.

When the register is loaded and the counter reaches a count of eight, the data character is ready for transfer from the converter register to the holding register. Approximately 5 μsec after the even clock pulse occurs from I128, after the counter reaches a count of nine, the gate at I131 is enabled and forces I127 to a "1". The data character is gated from the converter register to the holding register (FF's J102/103 through J116/117) via gates I108 through I123. The stop pulse at the end of each data character is monitored by I135. If the stop pulse is absent, I135 is forced to a "0" setting the Break FF, J122/123. Setting the Break FF indicates that a malfunction such as a temporary interruption in line current or an open line has occurred somewhere in the communications line.

The Select Input signal from I137 gates the contents of the holding register, in parallel, to the communications multiplexer.

When the next even clock pulse occurs (after an odd clock pulse and the count of nine have occurred) I128 is enabled. The output of I128 forces I194 to a "1" and I132 to a "0" which in turn is applied to I131 and I195. The "0" output of I128 clears Start/Stop FF J100/101 which in turn stops the clock and the counter. A logical "1" from I099 and a stop pulse from the data set via R100, I140, and I141 set the Character Ready FF, J118/119. This indicates to the communications multiplexer that the holding register contains a data character which is ready for transfer.

When 7-bit data characters are in use, the 7-bit signal from I182 is gated with received data at I186. If the first data bit received is a "1", I186 is enabled and forces I187 to a "1". As soon as a trigger pulse from I125 occurs, FF K104/105 sets and I187 and I188 begin to load serial data bits into the converter register at the second stage of the register. Data bits are then loaded into the register in succession from one stage to the next as they are for 8-bit data characters. When 6-bit characters are used, the 6-bit signal from I181 is gated with the received data at I189 and data is loaded into the register beginning with the third stage (FF K106/107). A similar progression of events occurs for 5-bit data character operation. The 5-bit signal from I164 is gated with data at I126. Data is loaded into the register via I179 and I153 beginning with the fourth-stage FF (K108/109) and continues with the loading process until the five stages contain the complete 5-bit data character.

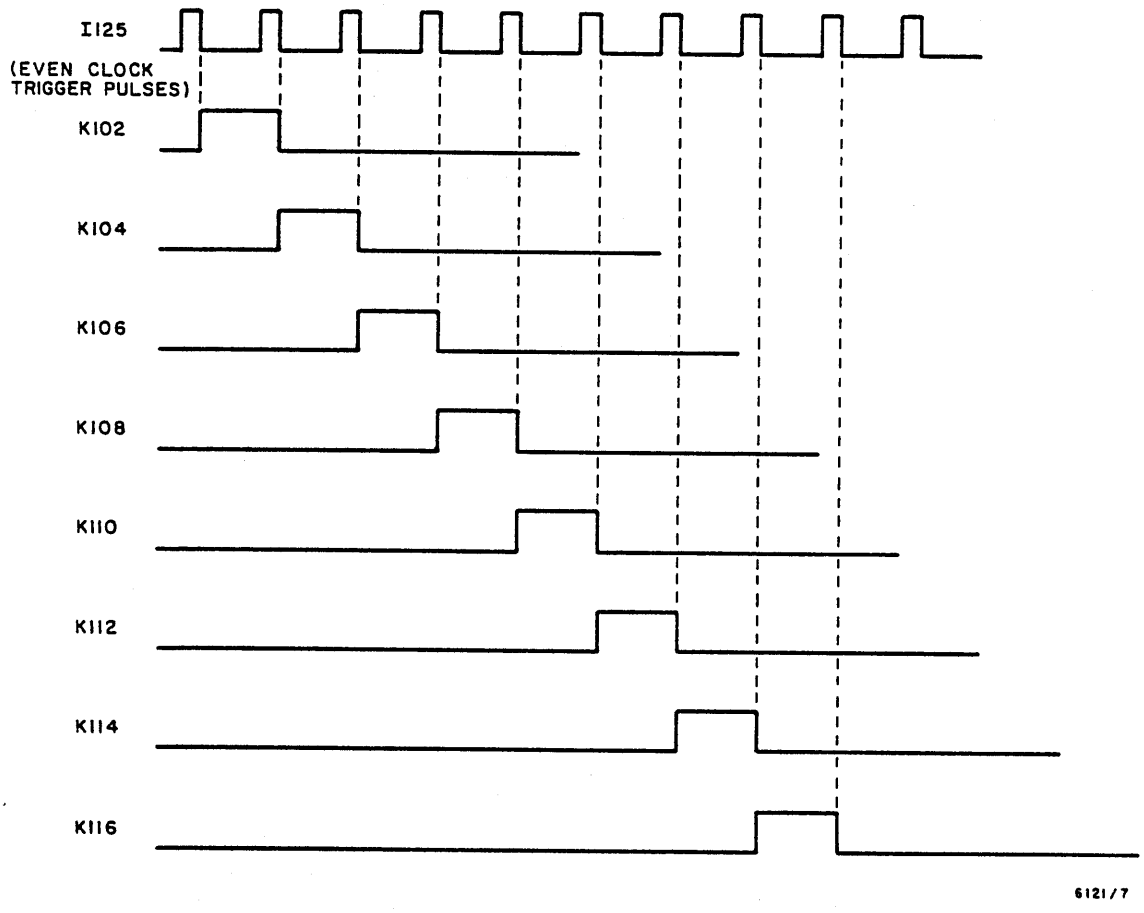


Figure 4-8. Receive Unit Converter Register Timing Diagram

Status Bits

The Receive Unit supplies three signals to the communications multiplexer which represent the status of the communications line or the data character. The three signals are the Break (bit 8), Character Lost (bit 9), and the Character Ready (Bit 11). A fourth signal, Character Request (bit 10), is also sent to the communications multiplexer but is controlled by the Send Unit and therefore is not discussed in the following paragraphs. The status bits accompany the input data character and are transferred to the communications multiplexer whenever it issues the Select Input signal to the Receive Unit. As soon as the computer samples the status bits, the communications multiplexer issues the Input Acknowledge signal on computer command, thereby clearing all status bit circuits via I192, I193, I138, and I152 in the Receive Unit. The following paragraphs contain a brief description of each status bit circuit associated with the Receive Unit.

Character Ready Signal

The Character Ready signal (bit 11) informs the communications multiplexer that the holding register in the Receive Unit contains a data character which is ready for transfer to the computer. FF J118/119 generates the Character Ready signal via I134 when the first even clock pulse occurs. This occurs after the counter has reached a count of nine and the output of I141 (stop pulse from data set) becomes a "1".

Character Lost Signal

The Character Lost signal (bit 9) informs the communications multiplexer that a new data character was shifted into the holding register before the preceding character was transferred to the computer. Consequently, one data character was lost. FF J120/121 generates the Character Lost signal via I136 when the counter reaches a count of nine and the Character Ready FF is still set from a previous data character transfer to the communications multiplexer.

Break Signal

The Break signal (bit 8) informs the communications multiplexer that a break or interruption has occurred in the communications line between the Receive Unit and the remote data set. Logically, FF J122/123 generates the Break signal via I135 when the counter reaches a count of nine provided a stop pulse is not present on the received data line.

Master Clear Signal

When a Master Clear signal (logical "0") is received from the communications multiplexer, the following logical operations are performed:

1. Clears Character Ready, Character Lost, and Break FF's via I129, I130, I138, and I152.
2. Clears Start/Stop FF via I129 and I130.
3. Conditions gates via I127 which transfer contents of shift register to holding register so that the next set output of the Start/Stop FF clears the holding register.

SECTION 5

DIAGRAMS

DIAGRAMS

GENERAL

This section contains a table of terms and the logic diagrams for the card assemblies used in the CA. Table 5-1 is included to aid maintenance personnel in locating logic elements on the logic diagrams and physically within the unit. Wherever possible, the table includes a definition of the signal associated with each term.

TABLE 5-1. TABLE OF TERMS

TERM	SHEET OR PAGE	LOCATION	DEFINITION
I087	5-9	51	
I089	5-7	42	
I090	5-7	62	
I091	5-7	31	
I093	5-7	31	
I094	5-7	31	
I095	5-9	51	
I096	5-9	32	
I097	5-9	52	
I098	5-7	52	
I098	5-7	11	
I099	5-7	22	
I100	5-7	43	
I101	5-9	63	
I102	5-9	63	
I103	5-9	63	
I104	5-9	62	
I105	5-9	63	
I106	5-9	62	
I107	5-9	62	
I108	5-9	33	
I109	5-9	33	
I110	5-9	33	
I111	5-9	33	
I112	5-9	22	
I113	5-9	22	
I114	5-9	22	
I115	5-9	22	
I116	5-9	12	
I117	5-9	12	
I118	5-9	12	
I119	5-9	12	
I120	5-9	03	
I121	5-9	03	
I122	5-9	03	
I123	5-9	03	
I124	5-9	52	
I125	5-9	32	
I126	5-9	42	
I127	5-7	61	
I128	5-7	23	
I129	5-7	63	
I130	5-7	63	
I131	5-7	21	
I132	5-7	22	
I133	5-7	22	
I134	5-7	21	
I135	5-7	11	
I136	5-7	31	
I137	5-7	52	Not Select Input
I138	5-7	62	
I139	5-7	34	
I140	5-7	44	
I141	5-7	44	
I142	5-9	62	
I143	5-9	42	
I144	5-7	42	
I145	5-7	62	
I146	5-7	34	
I147	5-9	42	
I148	5-9	52	
I149	5-7	51	Character Ready signal (Bit 11)
I150	5-7	51	Character Lost signal (Bit 9)
I151	5-7	51	Break Signal (Bit 8)
I152	5-7	63	
I153	5-9	41	
I154	5-9	24	Data Bit 7
I155	5-9	24	Data Bit 6
I156	5-9	24	Data Bit 5
I157	5-9	24	Data Bit 4
I158	5-9	14	Data Bit 3
I159	5-9	14	Data Bit 2
I160	5-9	14	Data Bit 1
I161	5-9	14	Data Bit 0
I162	5-9	52	Even Clock Receive Unit
I163	5-9	52	Odd Clock Receive Unit
I164	5-9	41	5-bit signal Receive Unit
I167	5-7	52	
I168	5-7	61	
I169	5-7	34	
I170	5-7	43	
I171	5-7	54	
I172	5-7	42	
I173	5-9	61	
I174	5-9	53	
I175	5-9	61	
I176	5-9	52	
I177	5-7	22	
I178	5-7	12	
I179	5-9	42	
I180	5-9	51	8-bit signal Receive Unit
I181	5-9	41	6-bit signal Receive Unit
I182	5-9	41	7-bit signal Receive Unit
I183	5-7	12	
I184	5-7	12	
I185	5-7	12	
I186	5-9	43	
I187	5-9	43	
I188	5-9	41	
I189	5-9	43	
I190	5-9	43	
I191	5-9	41	
I192	5-7	63	Not Input Acknowledge
I193	5-7	62	
I194	5-7	23	
I195	5-7	32	
I196	5-7	22	
I197	5-7	42	
I198	5-7	52	
I199	5-7	32	
I200	5-11	21	Not Data Bit 7
I201	5-11	21	Not Data Bit 6
I202	5-11	21	Not Data Bit 5
I203	5-11	21	Not Data Bit 4
I204	5-11	02	Not Data Bit 3
I205	5-11	02	Not Data Bit 2
I206	5-11	02	Not Data Bit 1
I207	5-11	02	Not Data Bit 0
I208	5-11	41	Data Bit 7
I209	5-11	41	Data Bit 6
I210	5-11	31	Data Bit 5
I211	5-11	31	Data Bit 4
I212	5-11	12	Data Bit 3
I213	5-11	12	Data Bit 2
I214	5-11	01	Data Bit 1
I215	5-11	01	Data Bit 0
I216	5-11	51	
I217	5-13	31	NOT 6-bit signal
I218	5-11	51	
I219	5-13	31	NOT 7-bit signal
I220	5-11	31	
I221	5-13	51	
I222	5-11	31	
I223	5-13	51	
I224	5-11	22	
I225	5-13	51	
I226	5-11	22	
I227	5-13	31	
I228	5-11	11	
I229	5-11	43	Send Data to Receive Unit
I230	5-11	11	
I231	5-11	43	NOT Test Mode
I232	5-13	52	
I233	5-13	42	
I234	5-13	60	
I235	5-13	52	
I236	5-11	23	
I237	5-13	31	NOT 5-bit signal
I238	5-13	50	
I239	5-13	30	Odd clock Send Unit
I240	5-13	50	
I241	5-13	30	Even clock Send Unit
I242	5-13	21	
I243	5-13	52	
I244	5-13	31	
I245	5-13	20	
I246	5-13	22	Counter trigger; gate shift register, to serializer
I247	5-13	50	
I248	5-13	22	Gate holding register to Shift register
I249	5-13	62	
I250	5-13	61	
I251	5-11	33	
I252	5-13	50	
I253	5-13	42	Select Output
I254	5-13	43	

TABLE 5-1. TABLE OF TERMS (Cont'd)

TERM	SHEET OR PAGE	LOCATION	DEFINITION
I255	5-13	23	Character Request
I256	5-13	43	NOT Enable Character Request
I257	5-13	33	
I258	5-13	43	NOT Disable Character Request
I259	5-13	33	
I260	5-13	43	
I261	5-13	33	NOT Master Clear
I262	5-13	43	
I263	5-13	52	
I264	5-13	30	
I265	5-13	30	
I266	5-13	21	
I267	5-13	21	
I268	5-13	03	
I269	5-13	60	1.0 unit stop pulse
I270	5-13	60	1.5 unit stop pulse
I271	5-13	60	2.0 unit stop pulse
I272	5-13	43	NOT Select Input
I273	5-13	51	
I274	5-11	43	NOT Bit 10
I275	5-11	13	NOT Bit 11
I276	5-11	33	
I277	5-11	33	
I278	5-11	42	
I279	5-11	43	
I280	5-11	13	NOT Enable Character Request to Rec Unit
I281	5-11	52	
I282	5-11	43	
I283	5-13	61	
I285	5-13	62	
I286	5-13	20	
I287	5-13	30	
I288	5-13	10	
I289	5-13	21	
I290	5-13	31	
I291	5-11	60	NOT 5-bit signal
I292	5-11	60	NOT 6-bit signal
I293	5-11	60	NOT 7-bit signal
I294	5-11	60	
I295	5-11	60	
I296	5-11	42	
I297	5-13	10	
I298	5-13	30	
J100	5-7	53	Start Clock Control
J101	5-7	53	Stop Clock Control
J102	5-9	34	Receive Unit holding register
J103	5-9	34	Receive Unit holding register
J104	5-9	34	Receive Unit holding register
J105	5-9	34	Receive Unit holding register
J106	5-9	23	Receive Unit holding register
J107	5-9	23	Receive Unit holding register
J108	5-9	23	Receive Unit holding register
J109	5-9	23	Receive Unit holding register
J110	5-9	13	Receive Unit holding register
J111	5-9	13	Receive Unit holding register
J112	5-9	13	Receive Unit holding register
J113	5-9	13	Receive Unit holding register
J114	5-9	04	Receive Unit holding register
J115	5-9	04	Receive Unit holding register
J116	5-9	04	Receive Unit holding register
J117	5-9	04	Receive Unit holding register
J118	5-7	21	Break FF
J119	5-7	21	
J120	5-7	41	Character Lost FF
J121	5-7	41	
J122	5-7	41	Break FF
J123	5-7	41	
J200	5-11	41	Send Unit holding register
J201	5-11	51	
J202	5-11	41	Send Unit holding register
J203	5-11	51	
J204	5-11	32	Send Unit holding register
J205	5-11	32	Send Unit holding register
J206	5-11	32	Send Unit holding register
J207	5-11	32	Send Unit holding register
J208	5-11	12	Send Unit holding register
J209	5-11	22	Send Unit holding register
J210	5-11	12	Send Unit holding register
J211	5-11	22	Send Unit holding register
J212	5-11	01	Send Unit holding register
J213	5-11	11	Send Unit holding register
J214	5-11	01	Send Unit holding register
J215	5-11	11	Send Unit holding register
J216	5-13	72	Start Clock control
J217	5-13	72	Stop Clock control
J218	5-13	13	
J219	5-13	13	
J220	5-13	33	Enable Character Request
J221	5-13	23	
J222	5-11	53	Full duplex
J223	5-11	53	
J224	5-11	33	Break FF
J225	5-11	23	
J226	5-13	13	
J227	5-13	13	
J228	5-13	20	
J229	5-13	20	
K100	5-9	64	
K101	5-9	64	
K102	5-9	31	Receive Unit shift register
K103	5-9	31	Receive Unit shift register
K104	5-9	31	Receive Unit shift register
K105	5-9	31	Receive Unit shift register
K106	5-9	21	Receive Unit shift register
K107	5-9	21	Receive Unit shift register
K108	5-9	21	Receive Unit shift register
K109	5-9	21	Receive Unit shift register
K110	5-9	11	Receive Unit shift register
K111	5-9	11	Receive Unit shift register
K112	5-9	11	Receive Unit shift register
K113	5-9	11	Receive Unit shift register
K114	5-9	01	Receive Unit shift register
K115	5-9	01	Receive Unit shift register
K116	5-9	01	Receive Unit shift register
K117	5-9	01	Receive Unit shift register
K200	5-11	50	Send Unit shift register
K201	5-11	50	Send Unit shift register
K202	5-11	50	Send Unit shift register
K203	5-11	50	Send Unit shift register
K204	5-11	30	Send Unit shift register
K205	5-11	30	Send Unit shift register
K206	5-11	30	Send Unit shift register
K207	5-11	30	Send Unit shift register
K208	5-11	20	Send Unit shift register
K209	5-11	20	Send Unit shift register
K120	5-7	14	Receive Unit Counter
K121	5-7	14	Receive Unit Counter
K122	5-7	13	Receive Unit Counter
K123	5-7	13	Receive Unit Counter
K124	5-7	03	Receive Unit Counter
K125	5-7	03	Receive Unit Counter
K126	5-7	03	Receive Unit Counter
K127	5-7	03	Receive Unit Counter
K210	5-11	20	Send Unit shift register
K211	5-11	20	Send Unit shift register
K212	5-11	10	Send Unit shift register
K213	5-11	10	Send Unit shift register
K214	5-11	10	Send Unit shift register
K215	5-11	10	Send Unit shift register
K216	5-11	40	Send data
K217	5-11	40	
K218	5-13	40	
K219	5-13	40	
K220	5-13	53	Counter
K221	5-13	53	Counter
K222	5-13	63	Counter
K223	5-13	63	Counter
K224	5-13	73	Counter
K225	5-13	73	Counter
K226	5-13	73	Counter
K227	5-13	73	Counter
K228	5-13	32	
K229	5-13	32	
R100	5-7	64	Received serial data
R101	5-7	64	Carrier on
R200	5-11	63	Data Set Ready
R201	5-13	41	Clear to Send
R202	5-13	41	Restraint

TABLE 5-1. TABLE OF TERMS (Cont'd)

TERM	SHEET OR PAGE	LOCATION	DEFINITION	TERM	SHEET OR PAGE	LOCATION	DEFINITION
S200	5-11	73	Send data	9601	5-9	60	Receive Unit Clock
S201	5-11	73	Request to Send	9601	5-13	70	Send Unit Clock
S202	5-11	73	Data Terminal Ready				

KEY TO LOGIC SYMBOLS

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building-block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In Control Data Corporation logic, two signals, a logical "0" and a logical "1" are the possible input or output conditions of a circuit. A circuit with an output of logical "0" is "low" or "off". A circuit with an output of logical "1" is "high" or "on". Direct current voltages of 0.0 ± 0.5 volts and 5.0 ± 0.5 volts correspond to logical "0" and logical "1", respectively, unless stated otherwise.

The symbols used on the logic diagrams in this section include NAND gates, NOR gates, capacitive delays, and RS and JK flip flops. In the logic diagrams, small circles are attached to the input and/or output leads of logic elements to denote the electrical conditions at the input and/or output terminals of a logic element. A circle at the input of an element indicates that a logical "0" input signal activates the function. A circle at the output of the activated element is a logical "0". Numbers are arbitrarily assigned to logic elements and denote the type of circuit, the term number, and the physical location of an integrated circuit on a printed circuit board.

Figure 1 illustrates two blank 30-pack printed circuit boards and the numbering system used for locating integrated circuits on a board. For example, if it is desirable to locate a logic element within a specific integrated circuit, it is necessary to know the type of printed circuit board on which the chip is mounted, the logic element number, and the location number. The inset next to view B in figure 1 indicates that the logic element, 1012, is contained within the integrated circuit occupying location number 22 on the printed circuit board.

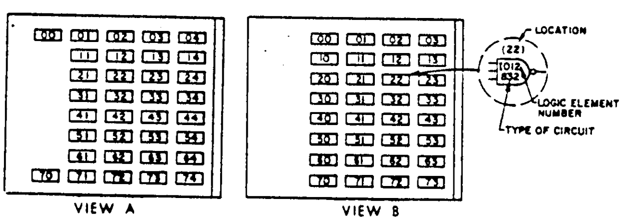


Figure 1. Integrated Circuit Locations

RECEIVER/TRANSMITTER

Two symbols are used to identify receiver/transmitter circuits and are shown in figure 2. The symbol in view A identifies the Control Data Intebrid receiver/transmitter circuits commonly used at the computer/multiplexing equipment interface. These circuits function as differential amplifiers and convert bipolar signals to unipolar signals or unipolar to bipolar, depending upon the direction of data flow. The symbols in view B identify EIA standard RS-232 receiver/transmitter circuits commonly used at the communications adapter/data set or modem interface.

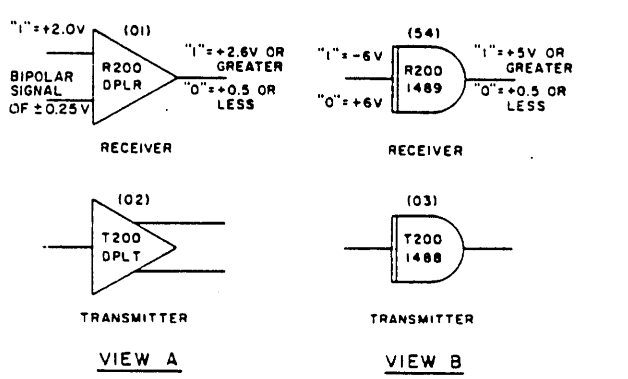


Figure 2. Receiver/Transmitter Symbols

NAND/NOR GATE

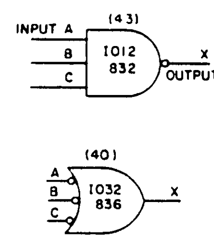
The NAND gate (view A, figure 3) requires that all inputs be logical "1"s so that its output be a logical "0". A circle attached to the output lead denotes inversion of the gate's output with respect to its input. Outputs follow the pattern explained in the truth table next to views A and B of figure 3.

The NOR gate (view B, figure 3) also operates according to the pattern in the accompanying truth table. As opposed to the NAND gate, the inclusive NOR gate requires only one logical "0" input to become active.

View C lists the possible combinations or applications for a two-input AND/NAND gate or a two-input OR/NOR gate and its equivalent logic element variation.

VIEW A

VIEW B



A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	0

VIEW C

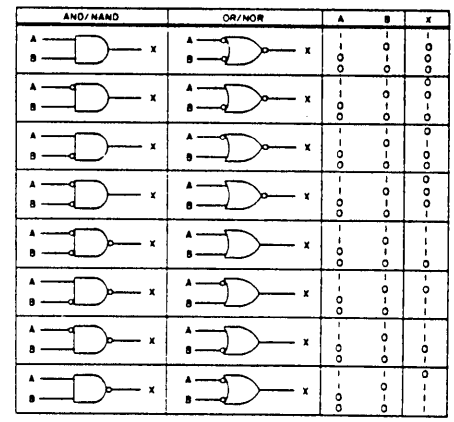


Figure 3. NAND/NOR Gate Symbols

EXTENDED INPUT

When another circuit is used to add inputs to a NAND gate or to a NOR gate, an extended input is used and connected as shown in figure 4.

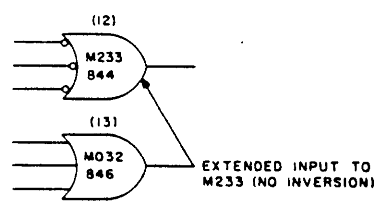
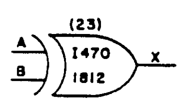


Figure 4. Extended Input Symbols

EXCLUSIVE OR GATE

The exclusive OR gate (figure 5) does not invert and produces a high output if, and only if any one input is high and all other inputs are low.



A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Figure 5. Exclusive OR Symbol

MULTIVIBRATOR

The 9601 is a retriggerable monostable multivibrator usually used as an internal source of clocking pulses. To start the 9601, either pin 1 or pin 2 must change to a "0" and pins 3 and 4 must both be "1"s. The time period "T" on the waveshape is determined by R1 and C1 or R1 and C2.

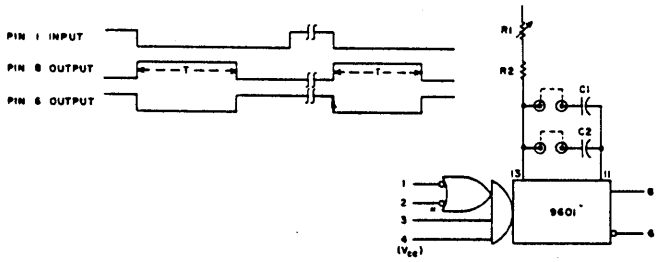


Figure 6. Multivibrator Symbol

BISTABLE LATCH

The bistable latch is normally used as a temporary storage circuit for binary information and usually contains more than one latching circuit per integrated circuit chip. Information present at the data input is transferred to the set (Q) output when the clock input is "high". The Q output will follow the D input as long as the clock remains "high". When the clock changes to a "low", data is retained within the latch until the clock again becomes high.

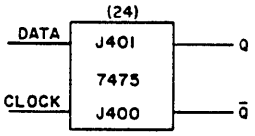


Figure 7. Bistable Latch Symbol

RS FLIP-FLOP

The RS flip flop is used as a temporary storage device having two stable states: set and clear. The RS flip flop is usually composed of two NOR gates as shown in figure 8. Numbers within the gates are arbitrarily assigned, as they are for most other logic elements. A logical "0" is required to set or to clear the flip flop. When set, the set output of the flip flop is a logical "1".

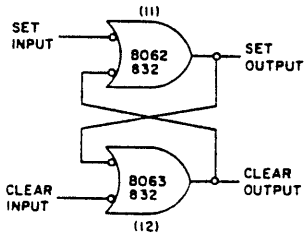
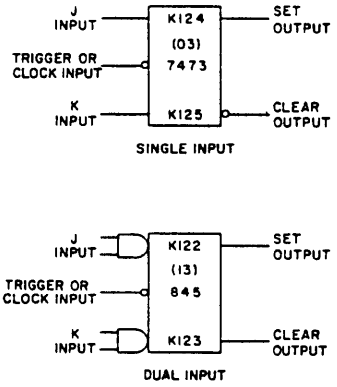


Figure 8. RS Flip Flop Symbol

JK FLIP-FLOP

The JK flip flop is also a temporary storage device containing two separate flip flop sections based on the master-slave principle. A trigger or clock pulse controls the inputs to the master flip flop section and also regulates the state of the coupling transistors which in turn connect the master and slave sections. In a typical sequence of operation, master and slave sections are isolated from one another. J and K inputs are entered at the master section, gates at the J and K inputs are then disabled, and the information is then transferred from the master to the slave section. Note that logical "0"s can be used to force-set or to force-clear the slave section directly. Figure 9 illustrates the symbols used for the JK flip flop and figure 10 illustrates the functional block diagram of the JK.



INPUT		OUTPUT	
J	K	Q	Q̄
0	0	NO CHANGE	
0	1	0	1
1	0	1	0
1	1	COMPLEMENT	

Figure 9. Flip Flop Symbols

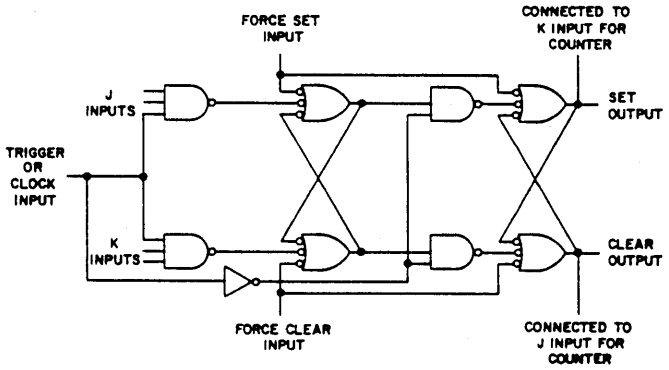
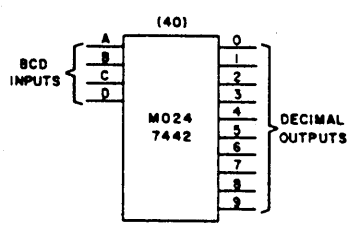


Figure 10. Functional Representation for JK Flip Flop

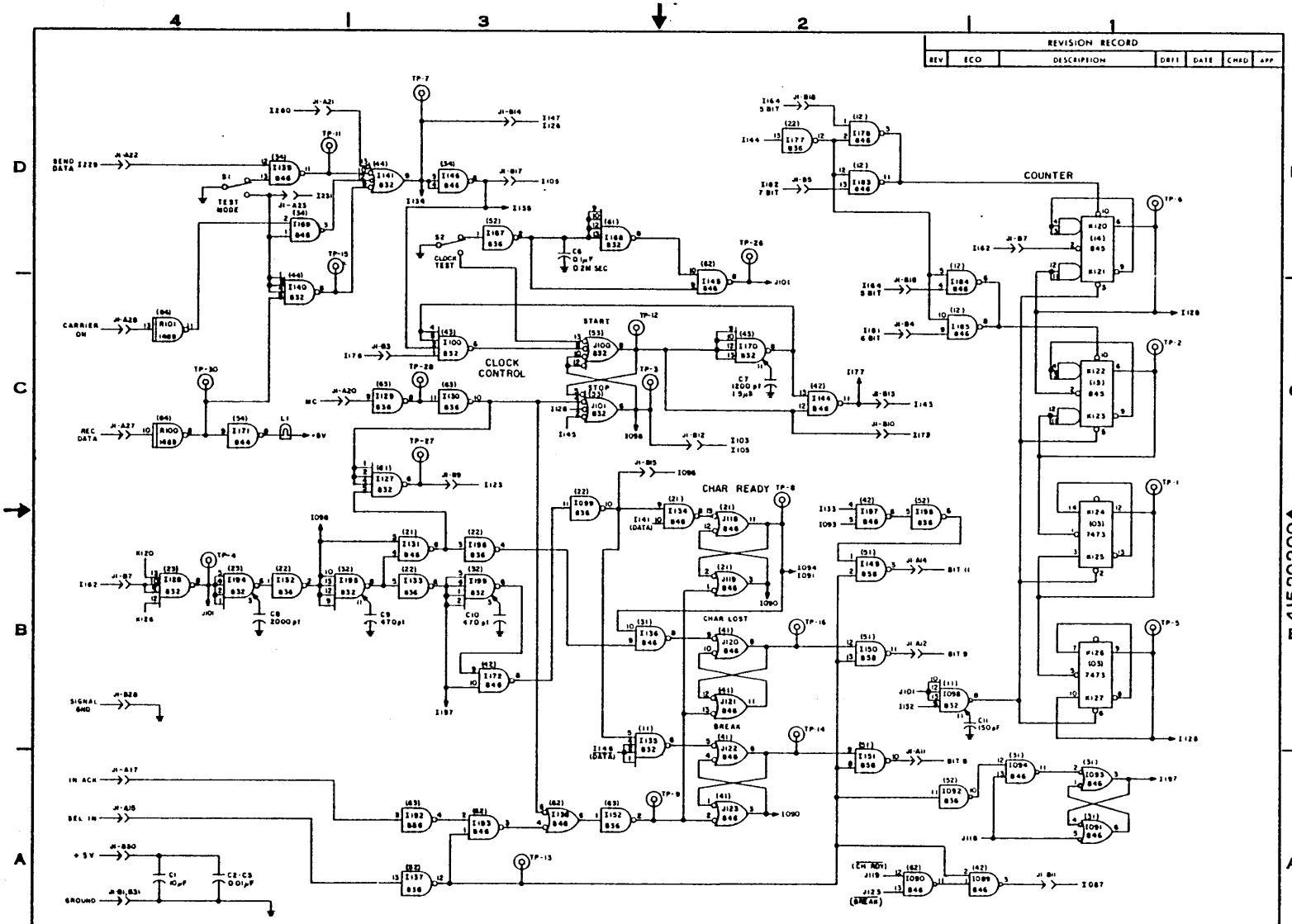
DECODER

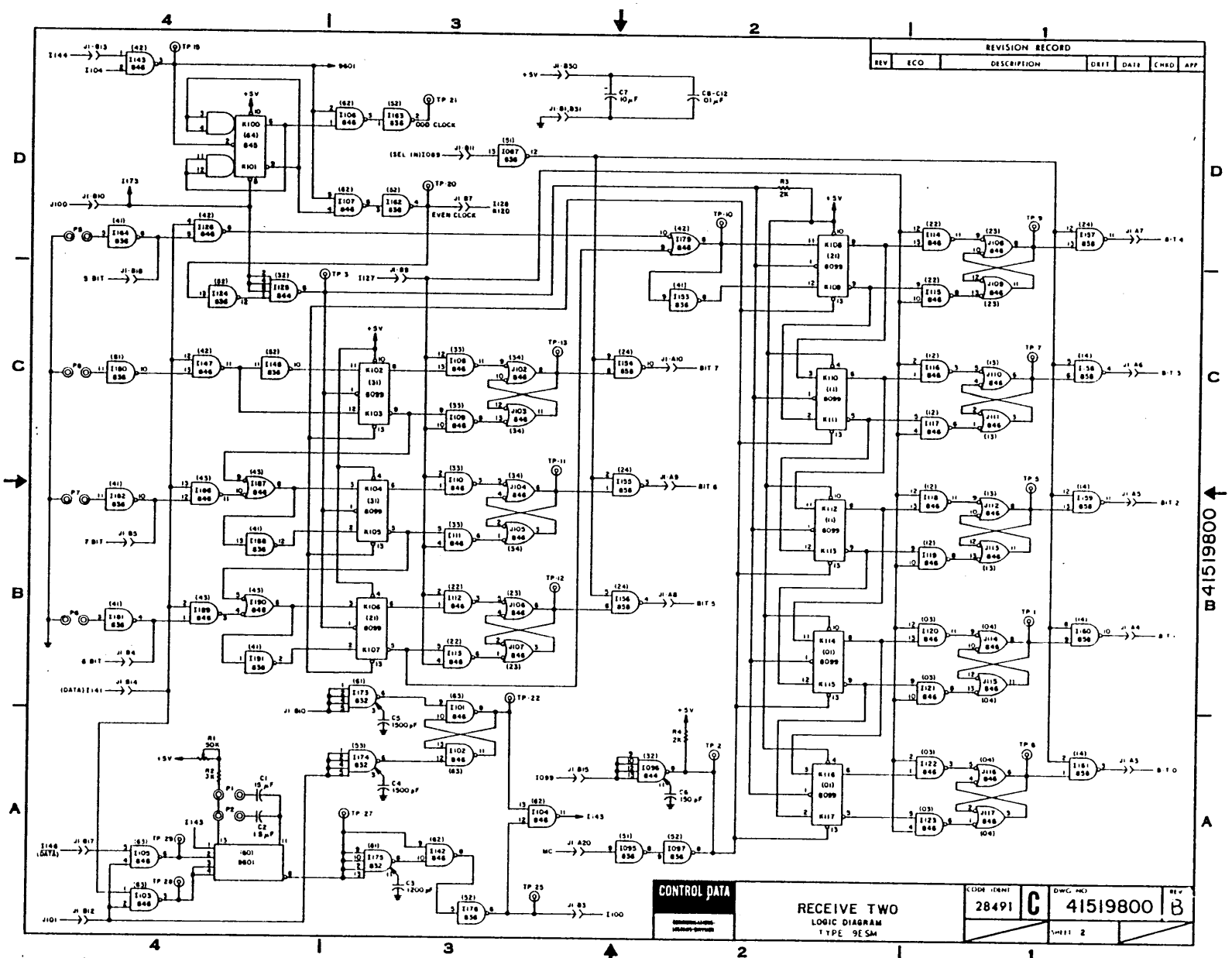
Decoders are used within the multiplexing equipment to convert a BCD character to a decimal output. The decoder consists of eight inverters and 10 four-input NAND gates. The inverters are connected in pairs to make the BCD input data available for decoding by the NAND gates. The decoder symbol and schedule of inputs and outputs are shown in figure 11.



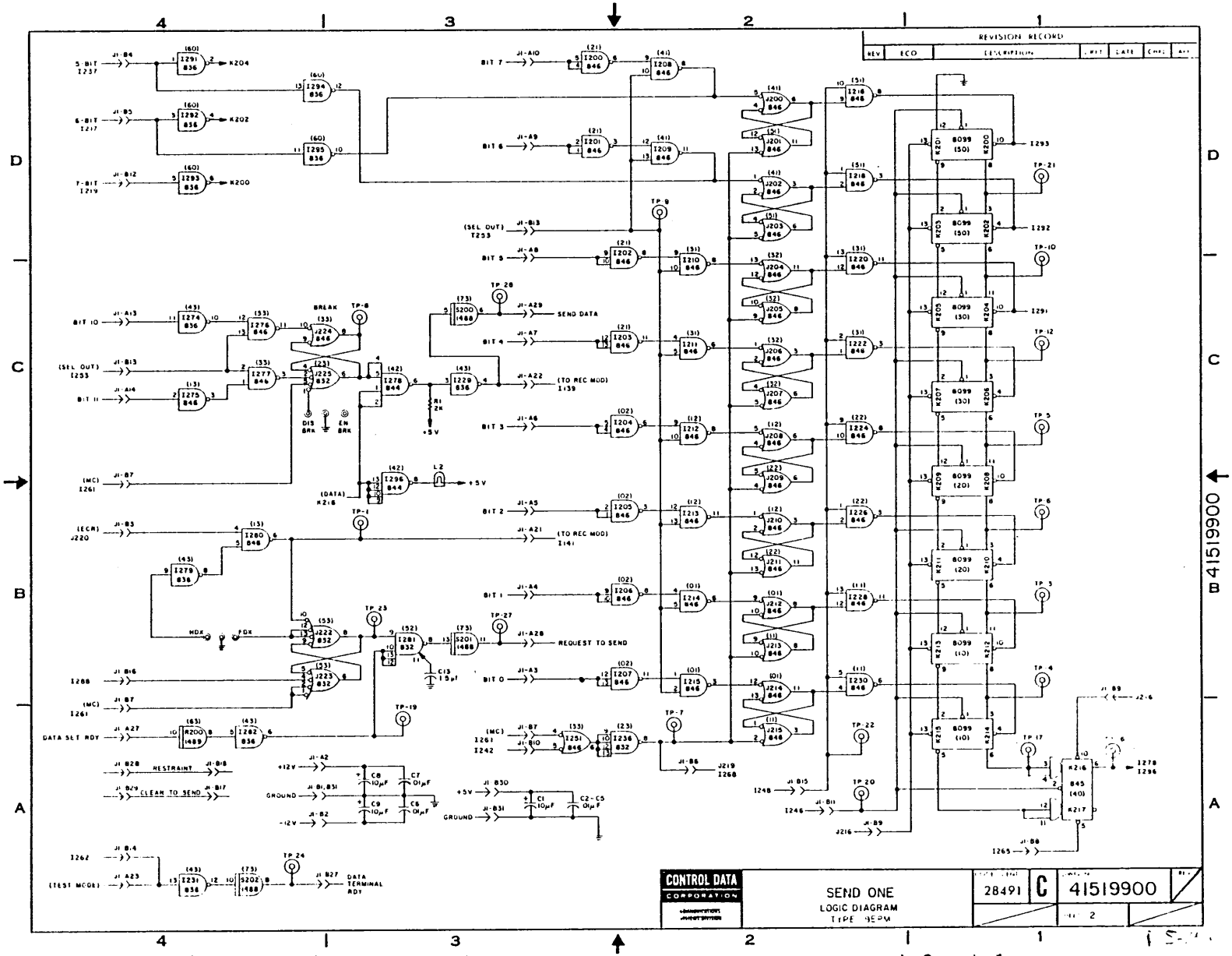
BCD INPUTS				DECIMAL OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 11. Decoder Symbol

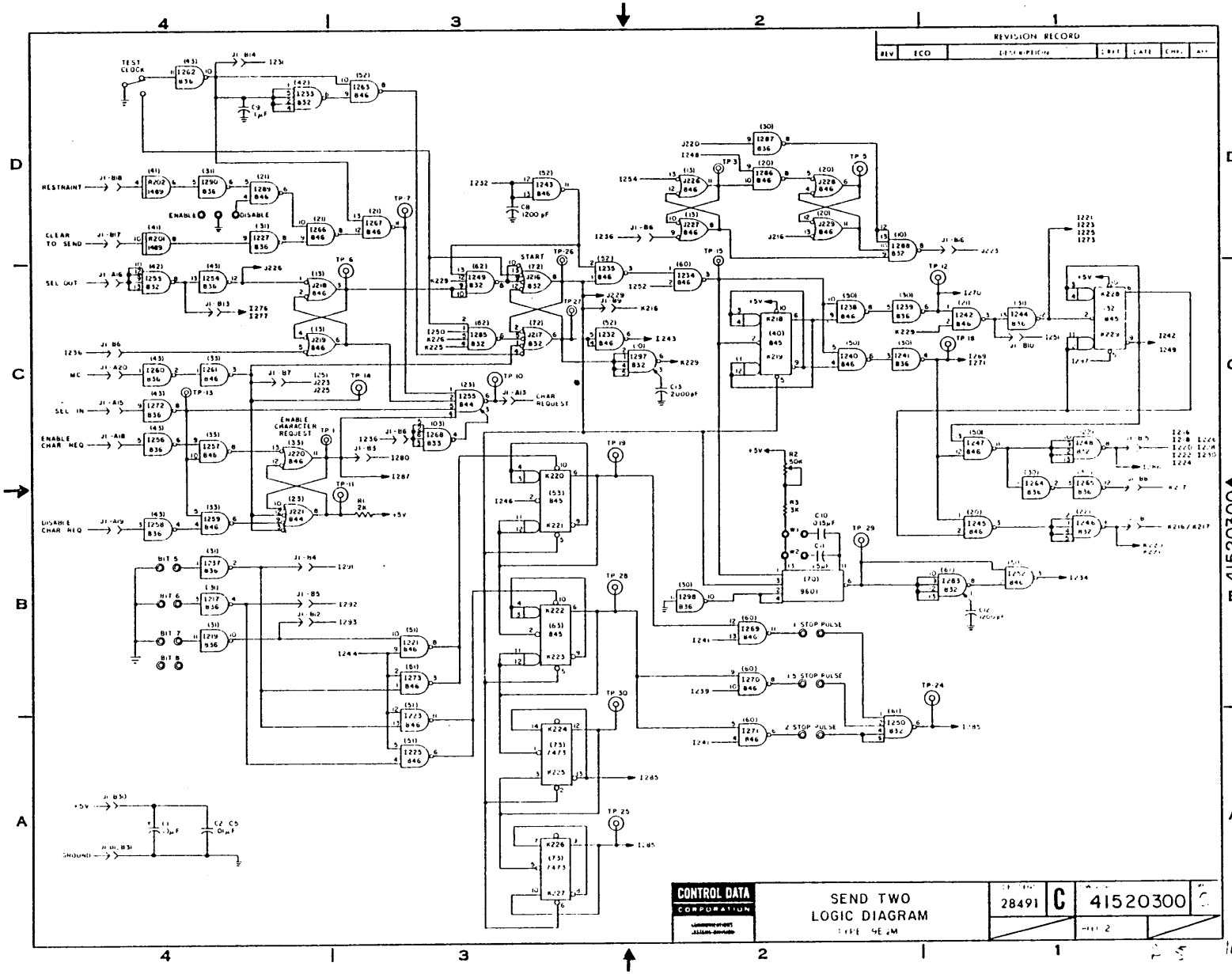

REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
COUNTER
CLOCK CONTROL
START
STOP
CHAR READY TP-8
CHAR LOST
BREAK
BIT 11
BIT 9
BIT 8
BIT 7
CARRIER ON
REC DATA
SEND DATA
TEST MODE
CLOCK TEST
SIGNAL GND
IN ACK
SEL IN
+5V
GROUND
NOTE: This diagram applies to series codes A01 and A02. See Appendix A for Series A03 and above.
DATA RECEIVE
RECEIVE ONE
LOGIC DIAGRAM
TYPE 9ERM
CODE IDENT
28491
C
DWG NO
41520200
REV
B
SHEET 2 OF 2
41520200 B



NOTE: This diagram applies to series A01 and A02. See Appendix A for series A03 and above.



NOTE: This diagram applies to series A01 and A02. See Appendix A for series A03 and above.



NOTE: This diagram applies to series A01 and A02. See Appendix A for series A03 and above.

SECTION 6

MAINTENANCE

MAINTENANCE

GENERAL

This section contains the procedures necessary for maintaining the CA. Maintenance procedures for equipment with which the CA operates are contained in manuals listed in the Preface.

LOGIC LEVELS

Internal logic signal voltages of 0.0 ± 0.5 volts and +5.0 ± 0.5 volts dc correspond to logical "0" and logical "1" respectively. External logic voltage levels between the CA and communications multiplexer are defined by logical "0" representing +0.5 volt dc or less and logical "1" representing +2.6 volts dc or more.

External voltage levels at the CA/data set interface representing serialized data are defined by a mark signal corresponding to -6 volts dc and a space signal corresponding to +6 volts dc. Signal ground is the reference potential for both signals. RS232-C line drivers and receivers are used at the CA/data set interface.

External voltage levels at the CA/data set interface representing control signals are defined as on (+6 vdc) and off (-6 vdc).

CAUTION

Since the units are very compact, the ±5-volt, ±12-volt power, and ground paths of the printed circuit foil are often separated by only 1/16th of an inch or less. Use care when connecting oscilloscope probes and especially the sync leads to the test points on the board.

PREVENTIVE MAINTENANCE

Generally, maintenance of the CA consists of replacement of any of the discrete components on any one of the four printed wiring boards or replacement of the complete printed wiring assembly, if an integrated circuit malfunctions. Replacement of individual integrated circuit chips on a printed wiring board is recommended only in cases of emergency at the field level. If it is necessary to troubleshoot a logic card assembly with an extender, use P/N 41527200.

Perform periodic maintenance on the CA as directed in Table 6-1 and accompanying instructions.

TABLE 6-1. PERIODIC MAINTENANCE CHART

Level 1 Monthly, or every 500 hours

Level		Item	Maintenance Action
1	2		
X		1.1	Check the clock adjustments on the send and receive units.
X		1.2	Check voltage margins

PREVENTIVE MAINTENANCE PROCEDURE

1.1 Clock Adjustments

Follow the procedure outlined in Section 3, Installation and Checkout.

1.2 Voltage Margins

Vary voltage margins per conditions in Table 1 and run either of the following diagnotic test programs.

3316/3516 CSPL Diagrnostics Program (U203*1)
1748-2 CSPL Diagnostic Program (U201*1)

	VOLTAGES				
CONDITION	+5	+6	-6	+12	-12
1	+5	+6	-6	+12	-12
2	+5.5	+6	-6	+12	-12
3	+4.5	+6	-6	+12	-12
4	+5	+6.6	-6.6	+12	-12
5	+5	+5.4	-5.4	+12	-12
6	+5	+6	-6	+13.2	-13.2
7	+5	+6	-6	+10.8	-10.8
8	+5	+6	-6	+12	-12

Voltage Test Conditions

TABLE I

SECTION 7

MAINTENANCE AIDS

MAINTENANCE AIDS

GENERAL

This section contains information on the repair of the printed circuit board. A list of pin assignments for the CA printed circuit board/communications multiplexer connector interface is found in Table 7-1. Figure 7-1 illustrates the physical pin connections to and electrical schematics of the various types of integrated circuits used in the CAs. Tables 7-2 and 7-3 are included as aids to maintenance personnel and provide information related to the interconnections between CA connectors, and connections between the CA and data set.

PRINTED CIRCUIT BOARD REPAIR

The maintenance and repair of 30-pak assemblies includes removing and replacing integrated circuits, cutting copper foil conductors to facilitate wiring changes, and adding discrete wires and components.

Usually, failure analysis is effective only when the defective circuits are received in an "as-failed" condition. Therefore, the following general precautions are given to minimize further damage to either the printed circuit board or any component (integrated circuit or discrete component) on the board.

1. Refrain from multiple bending of component leads. A lead may break off after being bent only a few times.
2. To avoid damage to the substrate of an integrated circuit chip, do not twist its leads.
3. Heat application from a soldering iron must not exceed five seconds. Excessive heat damages and shortens the life of components and loosens the copper foil from the printed circuit boards.

REMOVAL OF INTEGRATED CIRCUITS

1. Heat the solder connections on the back side of the board with a miniature soldering iron. Use a slight rocking motion to help spread the heat. Solder will flow in about two seconds. Immediately withdraw melted solder from the connection with the "solder sucker". Repeat this procedure for all connections.
2. Using an Exacto knife, loosen the wire leads on the chip from the holes. If some of the leads do not come free of the holes, it may be necessary to remove solder

from the front side of the board also. Carefully lift integrated circuit chip from board.

3. Remove excess solder and clean the board with a soft bristle brush and a solvent, preferably trichloroethylene.

REPLACEMENT OF INTEGRATED CIRCUITS

1. Correctly position a new integrated circuit on the board. Using the miniature soldering iron, solder the two end pins of the circuit to the board (typically pins 1 and 8). Make sure solder does not flow above the first bend of the circuit pin.
2. Solder the remaining pins to the board, using the crochet hook to press the pins down while being soldered.
3. Clean the board and inspect all solder joints.

CUTTING COPPER FOIL CONDUCTORS

1. Using an Exacto knife, cut the copper foil in two places, approximately 1/32" apart.
2. Peel off the copper strip between the two knife cuts. It is not necessary to remove the entire copper strip.

ADDING DISCRETE WIRES .

A maximum of 20 discrete wires is permissable on all types of 30 PAKS. Number 30 solid insulated wire with approximately 1/8" of insulation removed at each end is preferred.

A tinned wire may be soldered to the pad on a printed circuit board or to an integrated circuit pin, but not to the very thin copper foil paths. It is not necessary to twist the wire around the pin of the integrated circuit before soldering.

A discrete wire may be soldered to a lifted integrated circuit pin also. This is done only when the integrated circuit lead is disconnected from the pad, bent parallel to the surface of the board and cut off, leaving a 1/8" stub. The wire is held against the stub of the pin and soldered. This type of joint must be insulated with a plastic sleeve or equivalent insulator.

TABLE 7-1. CA/CM INTERFACE PIN ASSIGNMENTS

Receive Unit/CM*			Send Unit/CM*		
Board	Pin	Signal or Function	Board	Pin	Signal or Function
9ESM	A3	Bit 0 Data	9EPM	A3	Bit 0 Data
9ESM	A4	Bit 1 Data	9EPM	A4	Bit 1 Data
9ESM	A5	Bit 2 Data	9EPM	A5	Bit 2 Data
9ESM	A6	Bit 3 Data	9EPM	A6	Bit 3 Data
9ESM	A7	Bit 4 Data	9EPM	A7	Bit 4 Data
9ESM	A8	Bit 5 Data	9EPM	A8	Bit 5 Data
9ESM	A9	Bit 6 Data	9EPM	A9	Bit 6 Data
9ESM	A10	Bit 7 Data	9EPM	A10	Bit 7 Data
9ERM	A11	Bit 8 Break	9EPM	A11	Bit 8 Not assigned
9ERM	A12	Bit 9 Character Lost	9EPM	A12	Bit 9 Not assigned
9ERM	A14	Bit 11 Character Ready	9EPM	A13	Bit 10 Set Break
9ERM	A15	**Select Input	9EPM	A14	Bit 11 Clear Break
9ERM	A16	**Input Acknowledge	9EQM	A13	Bit 10 Character Request
9ERM	A20	**Master Clear	9EQM	A15	**Select Input
			9EQM	A17	**Select Output
			9EQM	A18	**Enable Character Request
			9EQM	A19	**Disable Character Request
			9EQM	A20	**Master Clear

*CM-communications multiplexer
**Control signal

TABLE 7-2. CA CONNECTOR INTERCONNECTIONS VIA COMMUNICATIONS MULTIPLEXER BACK PANEL

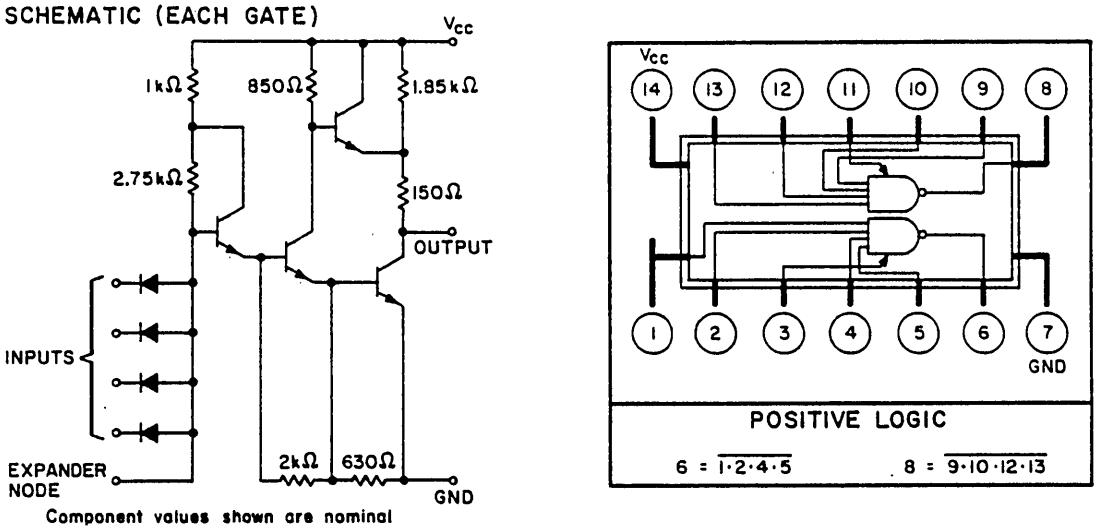
9EPM Pin	To 9EQM Pin	9ERM Pin	To 9ESM Pin	9EPM Pin	To 9ERM Pin	9EQM Pin	To 9ESM Pin
B3	B3	B3	B3	A21	A21	A21	A21
B4	B4	B4	B4	A22	A22	A22	A22
B5	B5	B5	B5	A23	A23	A23	A23
B6	B6	B6	B6	A24	A24	A24	A24
B7	B7	B7	B7	A25	A25	A25	A25
B8	B8	B8	B8	A26	A26	A26	A26
B9	B9	B9	B9				
B10	B10	B10	B10				
B11	B11	B11	B11				
B12	B12	B12	B12				
B13	B13	B13	B13				
B14	B14	B14	B14				
B15	B15	B15	B15				
B16	B16	B16	B16				
B17	B17	B17	B17				
B18	B18	B18	B18				
B19	B19	B19	B19				
B20	B20	B20	B20				

TABLE 7-3. CA/DATA SET INTERFACE CONNECTIONS

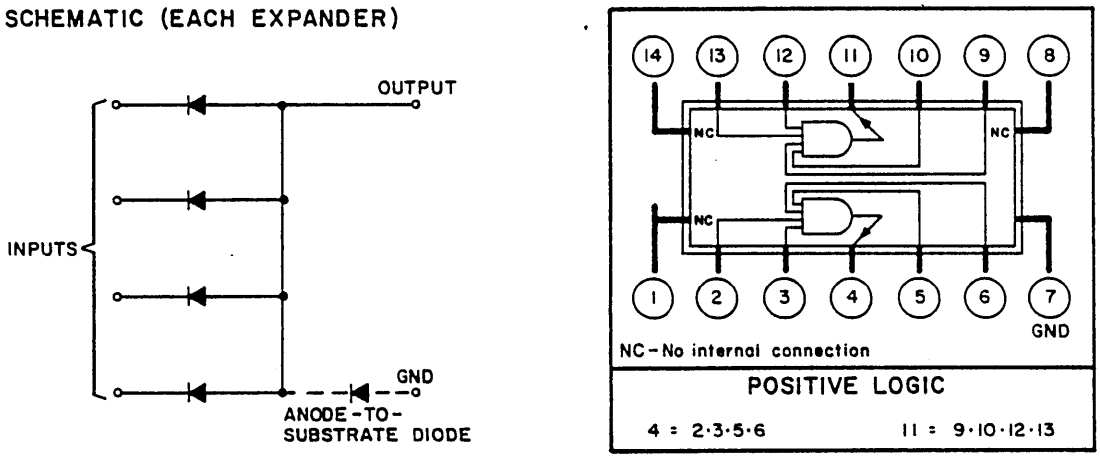
Board	Pin	Signal or Function	Data Set or RS 232-C Connector Pin	CCITT Circuit Number
		Frame Ground*	1	101
9EPM	A29	Transmitted data	2	103
9ERM	A27	Received data	3	104
9EPM	A28	Request to Send	4	105
9EQM	B17	Clear to Send	5	106
9EPM	A27	Data Set Ready	6	107
9ERM	B28	Signal Ground	7	102
9ERM	A28	Carrier On	8	109
9EQM	B18	Restraint	17	None
9EPM	B27	Data Terminal Ready	20	108/1 or 108/2**

*Part of chassis assembly wiring

**No exact equivalent due to options available



SNI5 832 DUAL 4-INPUT NAND/NOR BUFFER

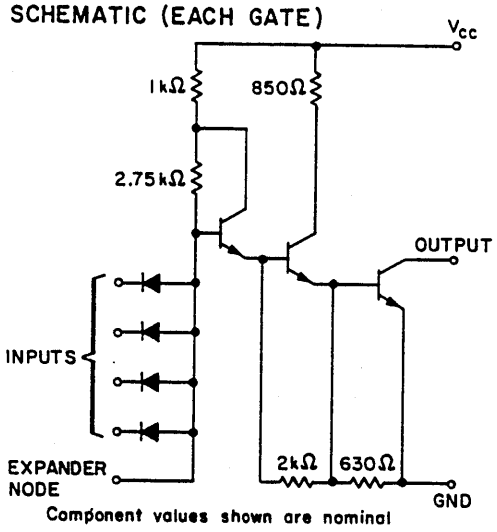


SNI5 833 DUAL 4-INPUT EXPANDER

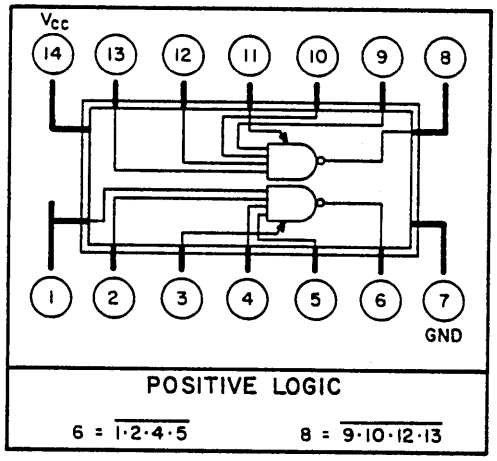
6121/8

Figure 7-1. Integrated Circuit Schematics and Pin Connections (Sheet 1 of 5)

SCHEMATIC (EACH GATE)



Component values shown are nominal



SN15 844 DUAL 4-INPUT NAND/NOR POWER GATE

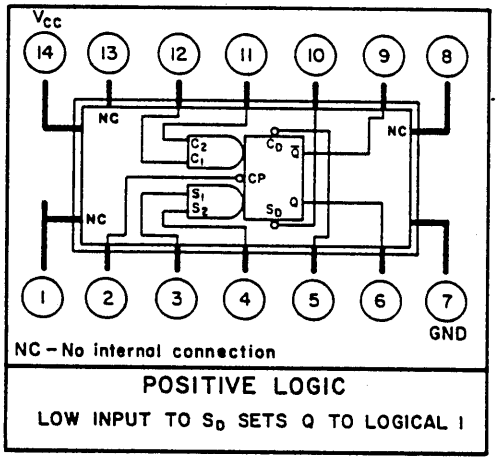
LOGIC

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	Qn

NOTES: 1. t_n = BIT TIME BEFORE CLOCK PULSE
2. t_{n+1} = BIT TIME AFTER CLOCK PULSE
3. X INDICATES THAT EITHER A LOGICAL 1 OR A LOGICAL 0 MAY BE PRESENT
4. LOGICAL 1 IS MORE POSITIVE THAN LOGICAL 0
5. FOR OPERATION IN THE J-K MODE CONNECT S_2 TO $\bar{Q}$ AND C_2 TO Q



SN15 845 FLIP-FLOP WITH SET AND CLEAR

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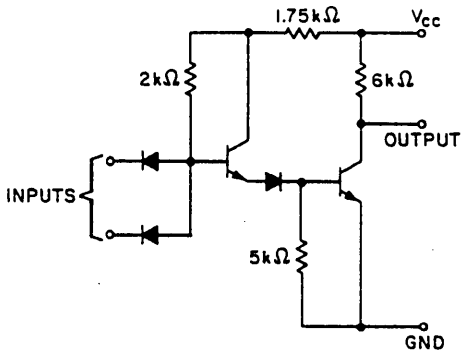
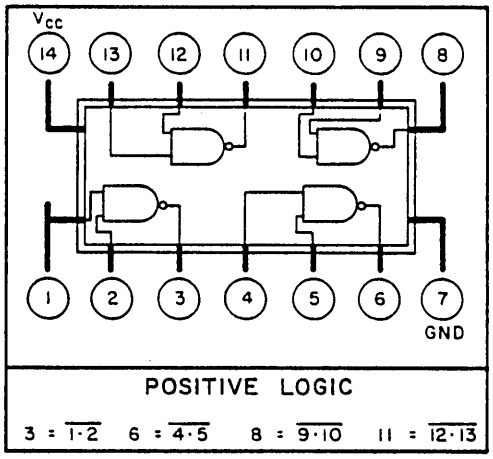
Figure 7-1. Integrated Circuit Schematics and Pin Connections (Sheet 2 of 5)

SCHEMATIC (EACH GATE)



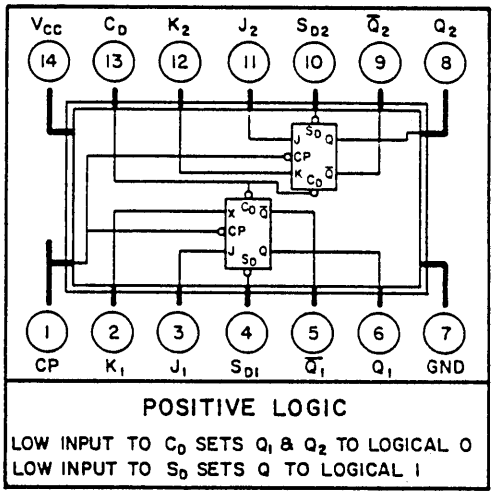
Component values shown are nominal



SNI5 846 QUADRUPLE 2-INPUT NAND/NOR GATE

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

NOTES: 1. t_n = BIT TIME BEFORE CLOCK PULSE
2. t_{n+1} = BIT TIME AFTER CLOCK PULSE



SNI5 8099 DUAL J-K MASTER-SLAVE FLIP-FLOP WITH COMMON CLEAR AND COMMON CLOCK

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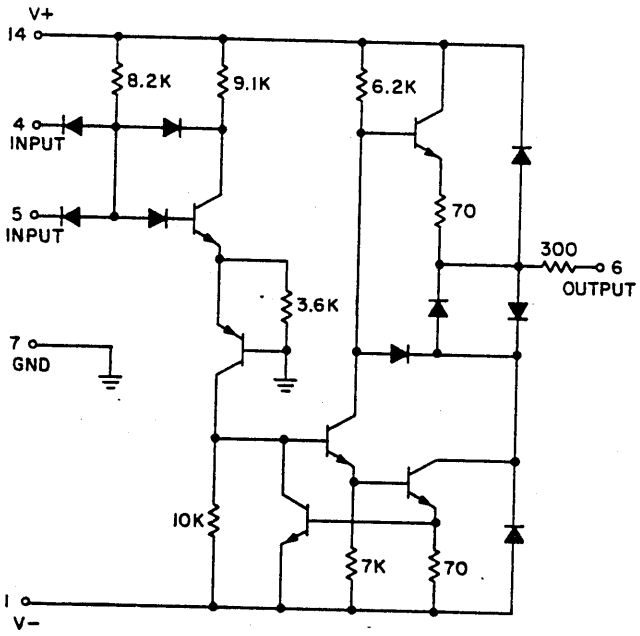
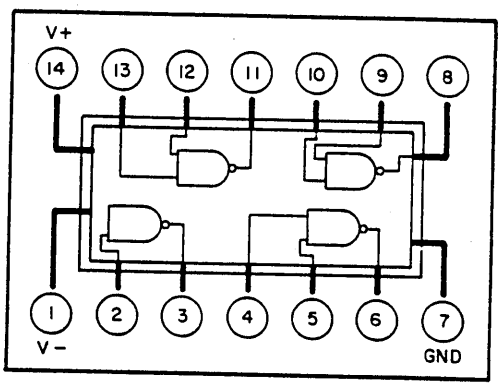
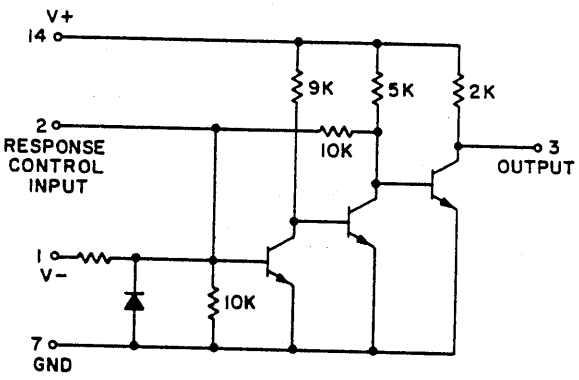
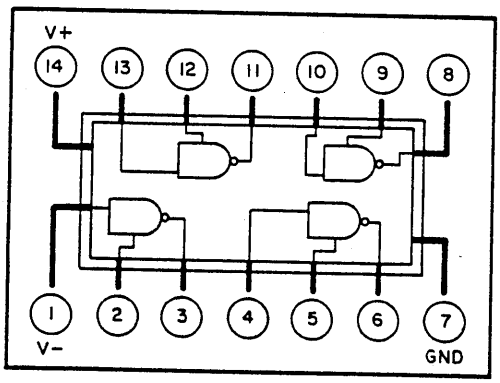
Figure 7-1. Integrated Circuit Schematics and Pin Connections (Sheet 3 of 5)





MC 1488 QUADRUPLE 2-INPUT LINE DRIVER





MC 1489 QADRUPLE 2-INPUT LINE RECEIVER

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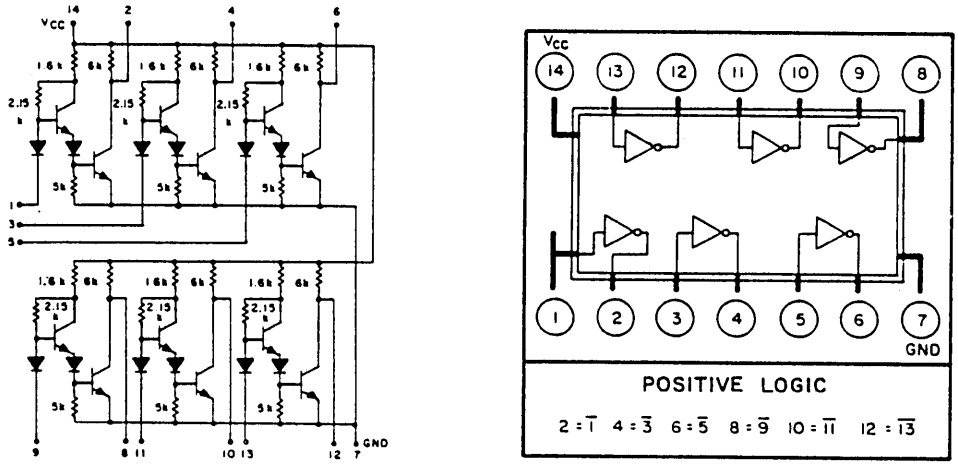
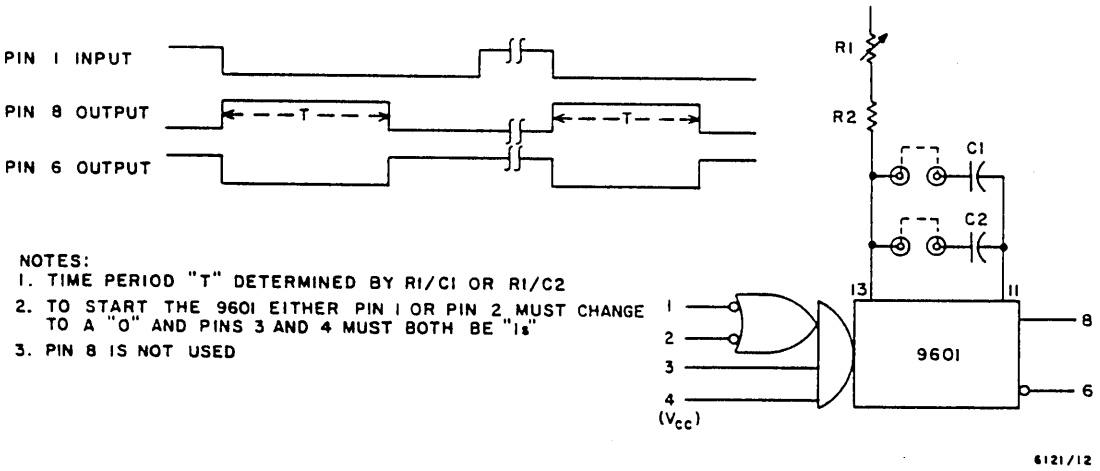
Figure 7-1. Integrated Circuit Schematics and Pin Connections (Sheet 4 of 5)



SN15 836 HEX INVERTERS



9601 MONOSTABLE MULTIVIBRATOR

Figure 7-1. Integrated Circuit Schematics and Pin Connections (Sheet 5 of 5)

SECTION 8

PARTS DATA

TABLE 8-1. REPLACEABLE PARTS

Part No.	Description	Units Per Assembly
41523800	Card assembly, type 9EPM (Send unit 1-1/2 of DJ142-A)	1
51577600	Integrated circuit, chip type SN15832	3
51654400	Integrated circuit, chip type SN15836	2
51577800	Integrated circuit, chip type SN15844	1
94825007	Integrated circuit, chip type SN15845	1
51577900	Integrated circuit, chip type SN15846	12
36186400	Integrated circuit, chip type MC1488	1
36186500	Integrated circuit, chip type MC1489	1
36189300	Integrated circuit, chip type SN158099	4
36185600	Lamp, no. 683 (L2)	1
36143002	Lens, lamp, red (for L2)	1
36143001	Socket, lamp (for L2)	1
24504382	Capacitor, fixed, 10 uf ±20%, 20 vdc (C1, C8, C9)	3
24504305	Capacitor, fixed, 0.01 uf ±20%, 35 vdc (C2-C7)	6
24505231	Capacitor, fixed, 1.5 uf ±10%, 35 vdc (C13)	1
24500070	Resistor, fixed, 2K ohms ±5%, 1/4 watt (R1)	1
36178800	Block, shorting (EN BRK/DIS BRK, HDX/FDX)	2
41524201	Card assembly, type 9EQM (Send Unit 2-1/2 of DJ142-A)	1
51577600	Integrated circuit, chip type SN15832	6
51577700	Integrated circuit, chip type SN15833	3
51654400	Integrated circuit, chip type SN15836	3
51577800	Integrated circuit, chip type SN15844	1
94825007	Integrated circuit, chip type SN15845	4
51577900	Integrated circuit, chip type SN15846	8
36186500	Integrated circuit, chip type MC1489	1
84746500	Integrated circuit, chip type SN7473	1
51518600	Integrated circuit, chip type 9601	1
24504382	Capacitor, fixed, 10 uf ±20%, 20 vdc (C1)	1
92496227	Capacitor, fixed, 0.01 uf ±20%, 35 vdc (C2-C5)	4
36137625	Capacitor, fixed, 1200 pf ±10%, 100 vdc (C8, C12)	2
24504317	Capacitor, fixed, 0.1 uf ±20%, 35 vdc (C9)	1
24521127	Capacitor, fixed, 0.15 uf ± 5%, 100 vdc (C10)	1
24505231	Capacitor, fixed, 1.5 uf ±10%, 35 vdc (C11)	1
24516134	Capacitor, fixed, 2000 pf ±10%, 50 vdc (C13)	1
24500070	Resistor, fixed, 2K ohms ±5%, 1/4 watt (R1)	1
24503614	Resistor, variable, wire wound, 50K ohms, 1 watt (R2-Clock)	1
24500074	Resistor, fixed, 3K ohms, 1/4 watt (R3)	1
41347800	Switch, toggle, SPST (SW1)	1
36178800	Block, shorting (P1/P2, 1SP/1.5SP/2SP, 5 bit/6 bit/7 bit/8 bit, EN/DIS)	4
41523400	Card assembly, type 9ERM (Receive Unit 1-1/2 of DJ143-A	1

NOTE: This parts list applies to series A01 and A02. See Appendix A for series A03 and above.

TABLE 8-1. REPLACEABLE PARTS (Cont'd)

Part No.	Description	Units Per Assembly
51577600	Integrated circuit, chip type SN15832	7
51654400	Integrated circuit, chip type SN15836	3
51577800	Integrated circuit, chip type SN15844	1
94825007	Integrated circuit, chip type SN15845	2
51577900	Integrated circuit, chip type SN15846	7
36186300	Integrated circuit, chip type MC858	1
36186500	Integrated circuit, chip type MC1489	1
84786500	Integrated circuit, chip type SN7473	1
36185600	Lamp, no. 683 (L1)	1
36143002	Lens, lamp, red (for L1)	1
36143001	Socket, lamp (for L1)	1
24504382	Capacitor, fixed, 10 uf ±20%, 20 vdc (C1)	1
92496227	Capacitor, fixed, 0.01 uf ±20%, 35 vdc (C2-C5)	4
24504317	Capacitor, fixed, 0.1 uf ±20%, 35 vdc (C6)	1
36137625	Capacitor, fixed, 1200 pf ±10%, 100 vdc (C7)	1
24516134	Capacitor, fixed, 2000 pf ±10%, 50 vdc (C8)	1
24516127	Capacitor, fixed, 470 pf ±10%, 50 vdc (C9, C10)	2
41347800	Switch, toggle, SPST (SW1, SW2)	2
41524401	Card assembly, type 9ESM (Receive Unit 2-1/2 of DJ143-A)	
51577600	Integrated circuit, chip type SN15832	1
51654400	Integrated circuit, chip type SN15836	2
51577800	Integrated circuit, chip type SN15844	3
94825007	Integrated circuit, chip type SN15845	1
51577900	Integrated circuit, chip type SN15846	1
36186300	Integrated circuit, chip type MC858	12
36189300	Integrated circuit, chip type SN8099	2
51518600	Integrated circuit, chip type 9601	4
24521127	Capacitor, fixed, 0.15 uf ± 5%, 100 vdc (C1-Clock)	1
24505231	Capacitor, fixed, 1.5 uf ±10%, 35 vdc (C2-Clock)	1
36137625	Capacitor, fixed, 1200 pf ±10%, 100 vdc (C3)	1
36137626	Capacitor, fixed, 1500 pf ±10%, 100 vdc (C4, C5)	1
31637614	Capacitor, fixed, 150 pf ±10%, 20 vdc (C6)	2
24504382	Capacitor, fixed, 10 uf ±20%, 20 vdc (C7)	1
92496227	Capacitor, fixed, 0.01 uf ±20%, 35 vdc (C8-C12)	1
24503614	Resistor, variable, wire wound, 50K ohms, 1 watt (R1-Clock)	5
24500074	Resistor, fixed, 3K ohms, 1/4 watt (R2)	1
24500070	Resistor, fixed, 2K ohms, 1/4 watt (R3, R4)	1
36178800	Block, shorting (P1/P2, 5 bit/6 bit/7 bit/8 bit)	2

SECTION 9

WIRE LISTS

(Refer to Table 7-2 for information on this section.)

SECTION 10

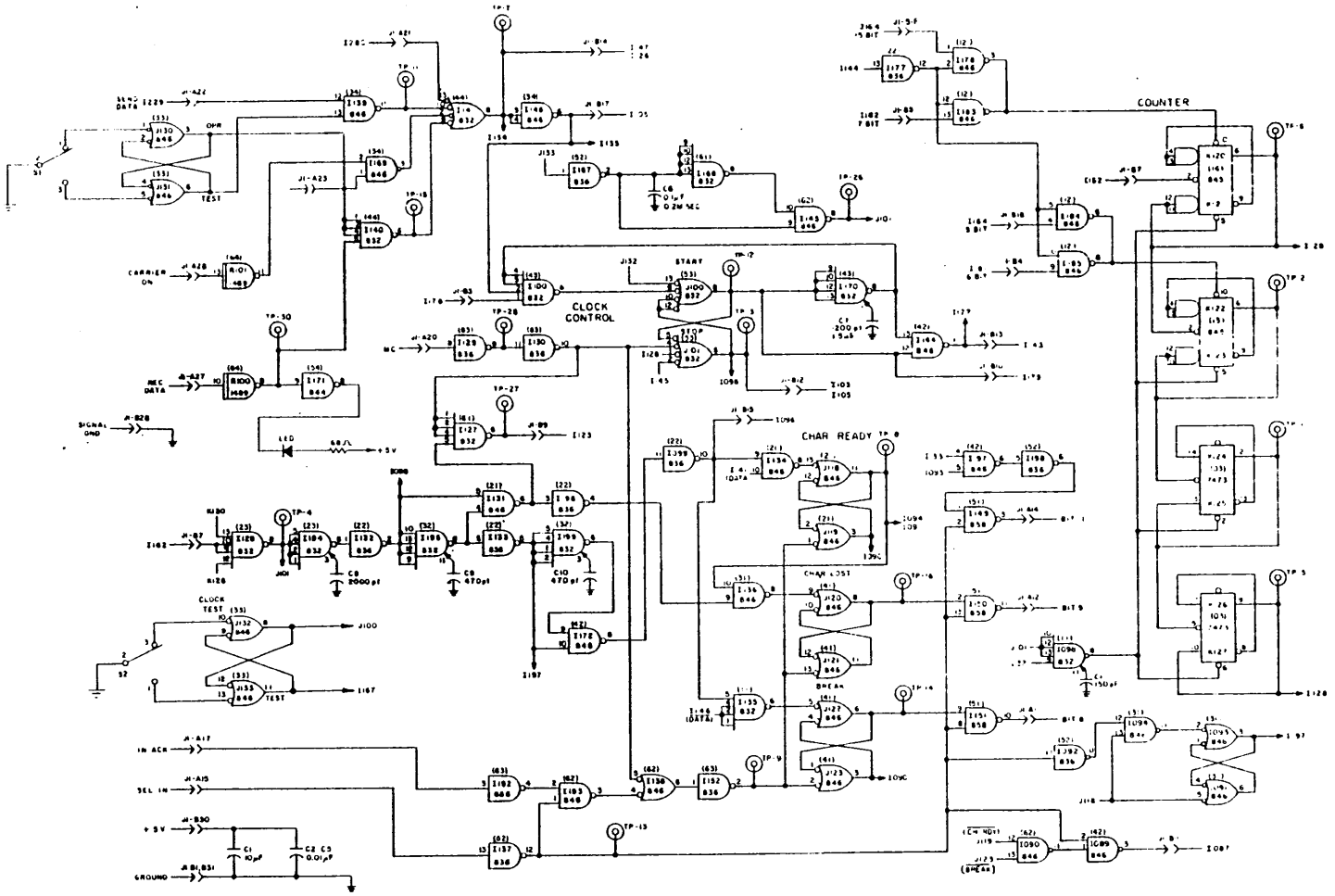
EQUATION SUMMARY

Not applicable to this equipment

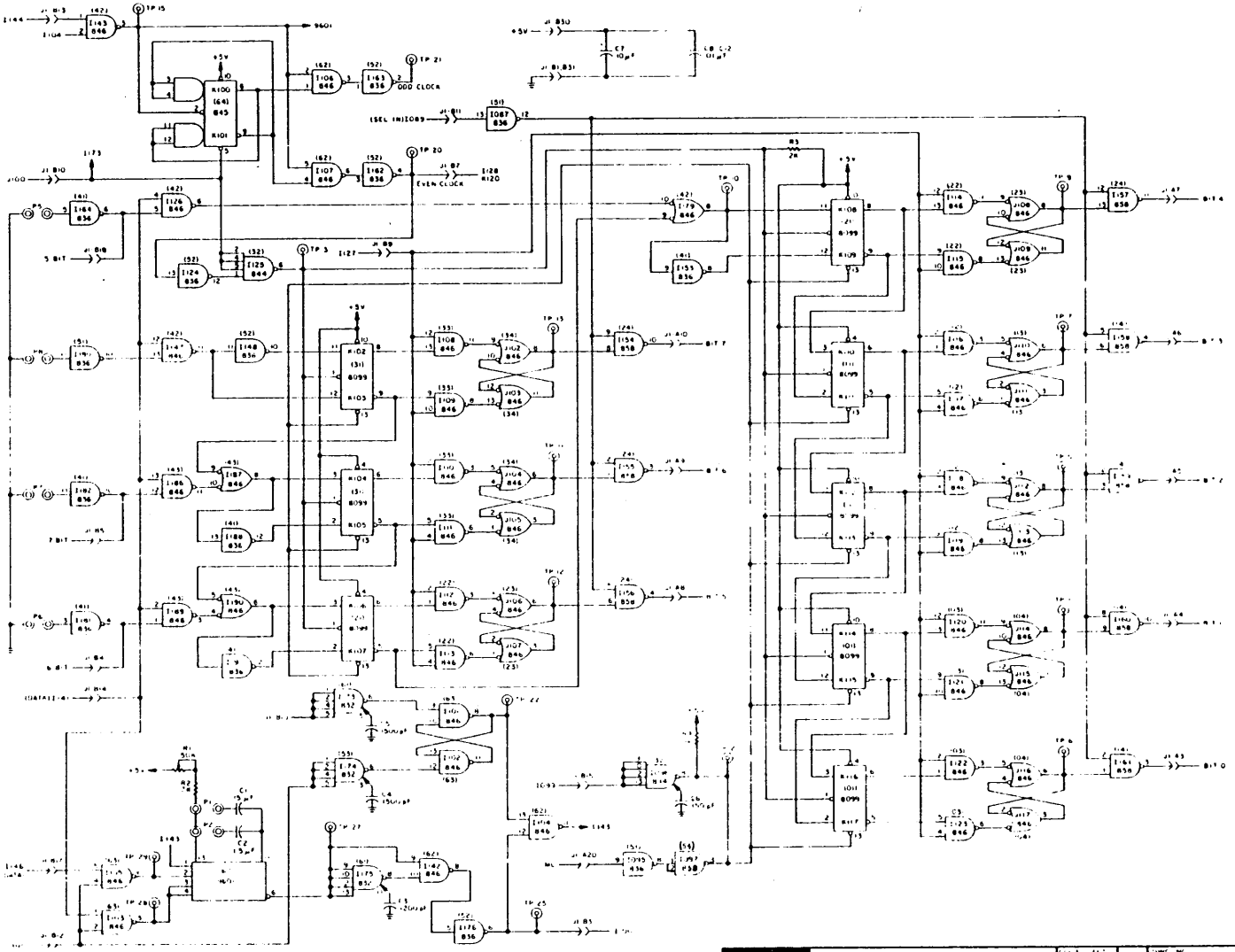
APPENDIX A

DJ142/DJ143 Series A03 and above.

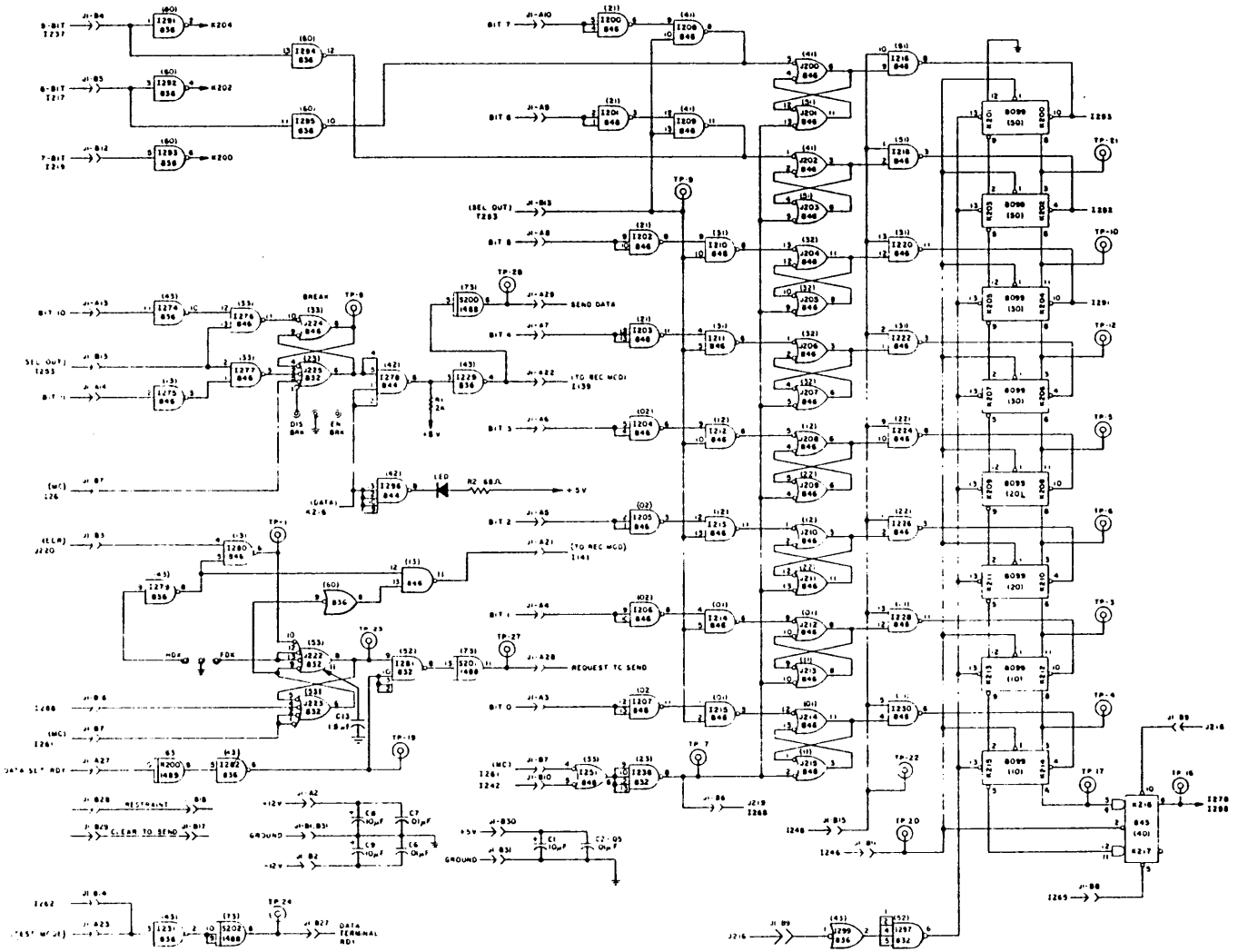
Diagrams and Parts Data



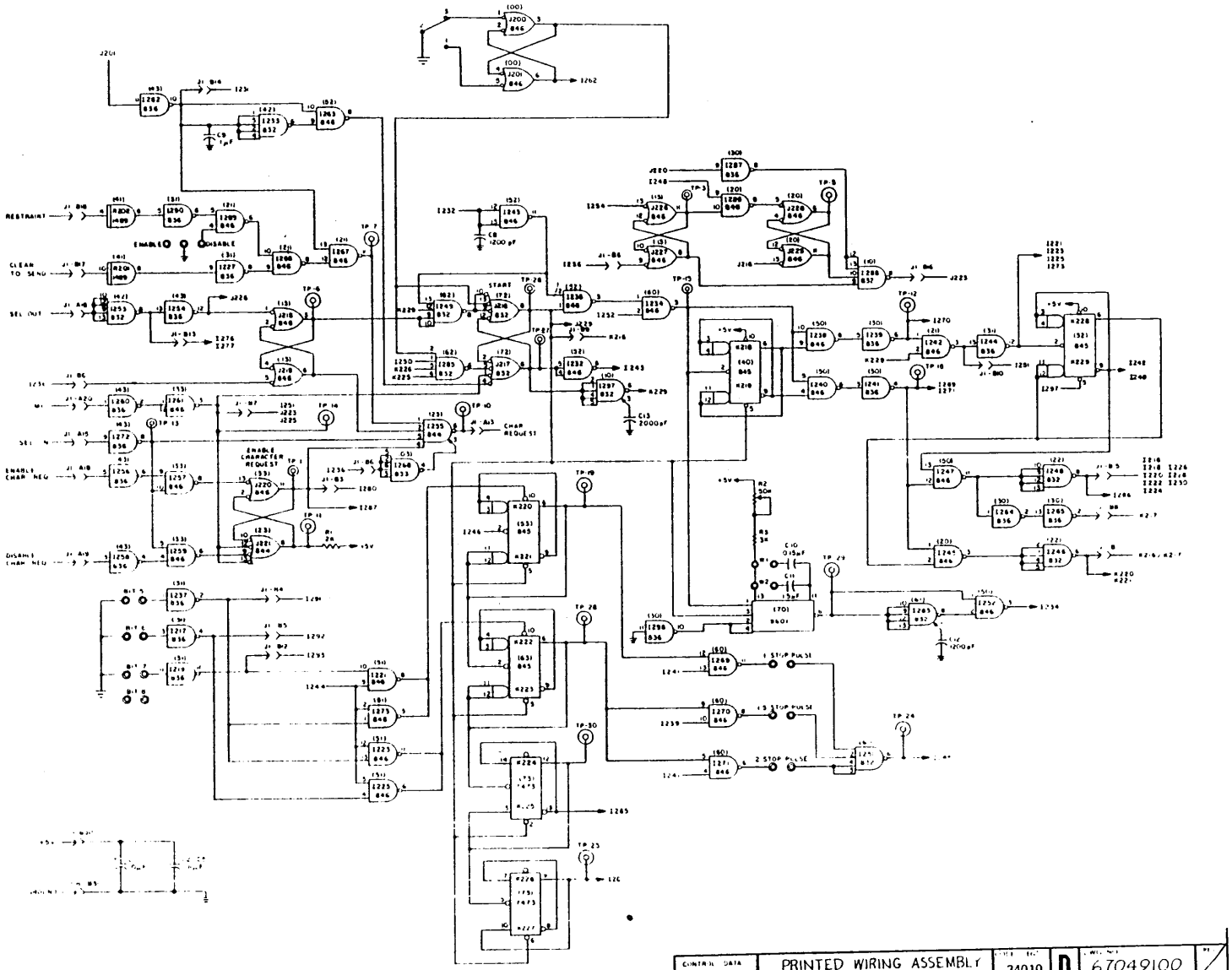
CONTROL DATA	PRINTED WIRING ASSEMBLY RECEIVE ONE (LOGIC DIAGRAM)	34010	D	67049600
ARDEN HILLS OPERATIONS				



CONTROL DATA ARDEN HILLS OPERATIONS	PRINTED WIRING ASSEMBLY RECEIVE TWO (LOCIC DIAGRAM)	34010	D	67049100	REV
				SHT 2	



CONTROL DATA ARDEN HILLS OPERATIONS	PRINTED WIRING ASSEMBLY SEND BOARD ONE (LOGIC DIAGRAM)	34010	D	60-49200	
				SHEET 2	


PRINTED WIRING ASSEMBLY
SEND TWO
(LOGIC DIAGRAM)
34010
D
67049100
SHT 2

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
67049600			D	P/W ASSY RECEIVE ONE (9ERM)	CA	DJ143A	04/27/72	

MF

PROCESSING DATE	PAGE NUMBER
05/09/74	1/ 1

CONTROL DATA

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	C	18696000	2[illegible]	PC	SWITCH TOGGLE	IN					PPP4		N
26	C	24500035	1[illegible]	PC	RES FXD .25W 68 OHMS	IN					PPP4		N
15	C	24504317	1[illegible]	PC	CAP FIXED SOLID TANTALUN	IN					PPP4		N
18	C	24504382	1[illegible]	PC	CAP,FXD SOLID TANTALUM	IN					PPP4		N
21	C	24516127	2[illegible]	PC	CAP FXD CER TANTALUM	IN					PPP4		N
20	C	24516134	1[illegible]	PC	CAP FXD CER DIELECTRIC	IN					PPP4		N
19	C	36137614	1[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
16	C	36137625	1[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
13	A	36186300	1[illegible]	PC	IC CHIP,TYPE 858	IN					PPP4		N
12	A	36186500	1[illegible]	PC	IC CHIP,TYPE 1489	IN					PPP4		N
9	A	51577600	7[illegible]	PC	IC CHIP TYPE 832	IN					PPP4		N
11	A	51577800	1[illegible]	PC	IC CHIP TYPE 844	IN					PPP4		N
6	A	51577900	8[illegible]	PC	IC CHIP TYPE 846	IN					PPP4		N
10	A	51654400	3[illegible]	PC	IC CHIP TYPE 836	IN					PPP4		N
7	A	52339200	2[illegible]	PC	ACCEPT.TEST -CLOCKED F.F. 845	IN					PPP4		N
8	A	52339400	1[illegible]	PC	ACCEPT.TEST DUAL JK F.F. 7473	IN					PPP4		N
2	C	52537300	1[illegible]	PC	CONNECTOR 62 CONTACT	IN					PPP4		N
1	D	67049700	1[illegible]	PC	BD/MA PRINTED CKT	IN					PPP4		N
17	C	92496227	4[illegible]	PC	CAP,FIXED	IN					PPP4		N
22	C	94256300	1[illegible]	PC	DIODE- LIGHT EMITTING	IN					PPP4		N
5	C	95324603	1[illegible]	PC	EJECTOR,CARD	IN					PPP4		N

NUMBER OF LINE ITEMS = 21
HIGHEST FIND NUMBER = 26

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
67049400			D	P/W ASSY RECEIVE TWO (9ESM)	CA	DJ143A	04/27/72	

MF

PROCESSING DATE	PAGE NUMBER
05/09/74	1/ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
26	C	24500070	2[illegible]	PC	RES FXD .25W 2000 OHMS	IN					PPP4		N
21	C	24500074	1[illegible]	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
20	C	24503614	1[illegible]	PC	RES VAR WW 1W	IN					PPP4		N
17	C	24504382	1[illegible]	PC	CAP,FXD SOLID TANTALUM	IN					PPP4		N
14	C	24505231	1[illegible]	PC	CAP FXD SOLID TANTALUM	IN					PPP4		N
13	C	24521127	1[illegible]	PC	CAP FXD METALIZED MYLAR	IN					PPP4		N
19	C	36137614	1[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
15	C	36137625	1[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
18	C	36137626	2[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
11	A	36186300	3[illegible]	PC	IC CHIP,TYPE 858	IN					PPP4		N
8	A	36189300	4[illegible]	PC	IC CHIP,TYPE 8099	IN					PPP4		N
9	A	51577600	2[illegible]	PC	IC CHIP TYPE 832	IN					PPP4		N
25	A	51577800	1[illegible]	PC	IC CHIP TYPE 844	IN					PPP4		N
6	A	51577900	12[illegible]	PC	IC CHIP TYPE 846	IN					PPP4		N
10	A	51654400	3[illegible]	PC	IC CHIP TYPE 836	IN					PPP4		N
12	A	51718600	1[illegible]	PC	IC CHIP TYPE 9601	IN					PPP4		N
7	A	52339200	1[illegible]	PC	ACCEPT.TEST -CLOCKED F.F. 845	IN					PPP4		N
23	C	52524504	12[illegible]	PC	CONTACT WIRE WRAP	IN					PPP4		N
2	C	52537300	1[illegible]	PC	CONNECTOR 62 CONTACT	IN					PPP4		N
1	D	67049500	1[illegible]	PC	BD/MA PRINTED CKT	IN					PPP4		N
16	C	92496227	5[illegible]	PC	CAP,FIXED	IN					PPP4		N
5	C	95324603	1[illegible]	PC	EJECTOR,CARD	IN					PPP4		N

NUMBER OF LINE ITEMS = 22
HIGHEST FIND NUMBER = 26

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
67049200			D	P/W ASSY SEND ONE (9EPM)	CA	DJ142A	04/27/72	

MF

PROCESSING DATE	PAGE NUMBER
05/09/74	1/ 1

CONTROL DATA

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
24	C	24500035	1	PC	RES FXD .25W 68 OHMS	IN					PPP4		N
19	C	24500070	1	PC	RES FXD .25W 2000 OHMS	IN					PPP4		N
18	C	24504382	3	PC	CAP,FXD SOLID TANTALUM	IN					PPP4		N
16	C	24505231	1	PC	CAP FXD SOLID TANTALUM	IN					PPP4		N
11	A	36186400	1	PC	IC CHIP,TYPE 1488	IN					PPP4		N
12	A	36186500	1	PC	IC CHIP,TYPE 1489	IN					PPP4		N
5	A	36189300	4	PC	IC CHIP,TYPE 8099	IN					PPP4		N
9	A	51577600	3	PC	IC CHIP TYPE 832	IN					PPP4		N
8	A	51577800	1	PC	IC CHIP TYPE 844	IN					PPP4		N
6	A	51577900	12	PC	IC CHIP TYPE 846	IN					PPP4		N
7	A	51654400	2	PC	IC CHIP TYPE 836	IN					PPP4		N
10	A	52339200	1	PC	ACCEPT.TEST -CLOCKED F.F. 845	IN					PPP4		N
21	C	52524504	6	PC	CONTACT WIRE WRAP	IN					PPP4		N
2	C	52537300	1	PC	CONNECTOR 62 CONTACT	IN					PPP4		N
1	D	67049300	1	PC	BD/MA PRINTED CKT	IN					PPP4		N
17	C	92496227	6	PC	CAP,FIXED	IN					PPP4		N
13	C	94256300	1	PC	DIODE- LIGHT EMITTING	IN					PPP4		N
22	C	95324603	1	PC	EJECTOR,CARD	IN					PPP4		N

NUMBER OF LINE ITEMS = 18
HIGHEST FIND NUMBER = 24

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER		PROCESSING DATE	PAGE NUMBER
67049100			D	P/W ASSY SEND TWO (9EQM)	CA	DJ142A	04/27/72		PR	05/15/74	1/ 1

CONTROL DATA
CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
21	C	18696000	1[illegible]	PC	SWITCH TOGGLE	IN					PPP4		N
4	C	24500070	1[illegible]	PC	RES FXD .25W 2000 OHMS	IN					PPP4		N
28	C	24500074	1[illegible]	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
3	C	24503614	1[illegible]	PC	RES VAR WW 1W	IN					PPP4		N
8	C	24504317	1[illegible]	PC	CAP FIXED SOLID TANTALUN	IN					PPP4		N
5	C	24504382	1[illegible]	PC	CAP,FXD SOLID TANTALUM	IN					PPP4		N
7	C	24505231	1[illegible]	PC	CAP FXD SOLID TANTALUM	IN					PPP4		N
11	C	24516134	1[illegible]	PC	CAP FXD CER DIELECTRIC	IN					PPP4		N
6	C	24521127	1[illegible]	PC	CAP FXD METALIZED MYLAR	IN					PPP4		N
10	C	36137625	2[illegible]	PC	CAPACITOR, FIXED,CERAMIC	IN					PPP4		N
17	A	36186500	1[illegible]	PC	IC CHIP,TYPE 1489	IN					PPP4		N
12	A	51577600	6[illegible]	PC	IC CHIP TYPE 832	IN					PPP4		N
13	A	51577700	1[illegible]	PC	IC CHIP TYPE 833	IN					PPP4		N
20	A	51577800	1[illegible]	PC	IC CHIP TYPE 844	IN					PPP4		N
16	A	51577900	9[illegible]	PC	IC CHIP TYPE 846	IN					PPP4		N
14	A	51654400	3[illegible]	PC	IC CHIP TYPE 836	IN					PPP4		N
18	A	51718600	1[illegible]	PC	IC CHIP TYPE 9601	IN					PPP4		N
15	A	52339200	4[illegible]	PC	ACCEPT.TEST -CLOCKED F.F. 845	IN					PPP4		N
19	A	52339400	1[illegible]	PC	ACCEPT.TEST DUAL JK F.F. 7473	IN					PPP4		N
23	C	52524504	21[illegible]	PC	CONTACT WIRE WRAP	IN					PPP4		N
2	C	52537300	1[illegible]	PC	CONNECTOR 62 CONTACT	IN					PPP4		N
1	D	67049000	1[illegible]	PC	BD/MA PRINTED CKT	IN					PPP4		N
9	C	92496227	4[illegible]	PC	CAP,FIXED	IN					PPP4		N
26	C	95324603	1[illegible]	PC	EJECTOR,CARD	IN	033233	02[illegible]73			PPP4		N

NUMBER OF LINE ITEMS = 24
HIGHEST FIND NUMBER = 28

COMMENT SHEET

MANUAL TITLE CDC DJ142-A, DJ143-A Communications Adapters

Customer Engineering Manual

PUBLICATION NO. 41612100 REVISION H

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