CONTROL DATA
CORPORATION

CONTROL DATA® 3553 MASS STORAGE CONTROLLER COMPUTER SYSTEM

REFERENCE MANUAL

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or use Comment Sheet in the back of this manual.

PREFACE

This publication contains operation and programming information for the CONTROL DATA® 3553-1 and 3553-2 Mass Storage Controllers which are used with CONTROL DATA® 3000 Series Data Channels. Some models of the controllers contain error recovery logic. Refer to the controller customer engineering manuals for a listing and description of the various models. The user of this manual should be familiar with the Control Data 3000 Series Data Channel I/O specifications and operating characteristics.

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FUNCTIONAL DESCRIPTION 1

INTRODUCTION

The CONTROL DATA® 3553 Mass Storage Controller, together with a CONTROL DATA® 841 Multiple Disk Drive (MDD) and/or a CONTROL DATA® 821 Disk File, operates as a nonvolatile mass storage subsystem. The MDD uses CONTROL DATA® 871 Disk Packs.

There are two variations of the controller, 3553-1 and 3553-2. The 3553-2 Controller interfaces with one or two 3000 Series Data Channels, contains a buffer memory, and has a sector length of 320 12-bit words. The 3553-1 Controller interfaces with one or two 6000 Series Data Channels via 6681 Data Channel Converters, includes no buffer memory, and has a sector length of 322 12-bit words.

The mass storage subsystem interfaces with one or two 3000 Series Data Channels and provides large-scale storage capabilities. The equipment comprising the subsystem is briefly defined as follows:

- The controller synchronizes data transfer between the peripheral storage units; that is, MDD and disk file, and the data channel. It consists of logic cards, controls, and a power supply housed in a cabinet.
- The MDD includes the associated disk pack and the cabinet in which the circuitry and drive mechanism are contained. The average data transfer rate is 2,148,000 bits per second. The disk pack consists of 11 disks mounted on a common vertical spindle. The disk packs are portable and interchangeable among other MDD units providing that the units are operated with the same type of 3553 Controller.
- The disk file consists of a number of disks mounted on a spindle, a disk drive mechanism, and associated circuitry and logic. The average data transfer rate is 2,232,000 bits per second. Two disk file models are available; the 821-1, containing 36 disks and the 821-2, containing 72 disks. The 821-2 Disk File is considered as two storage units.

This manual contains a functional description, codes, and operation and programming information. It is assumed that the manual user is familiar with 3000 Series input/output, interrupt, and parity procedures.

SUBSYSTEM CONFIGURATION

The mass storage subsystem has expandable capabilities. The minimum subsystem consists of a controller and one or more peripheral storage units interfacing with a single data channel (Figure 1-1). The subsystem can be expanded with the addition of more storage units or another controller. The second controller can be added if Dual Access Option 10163 is installed in the MDD. The dual access capability is a standard feature of the Disk File. Two data channels can be connected to each controller and operate on a time-shared basis. The maximum subsystem consists of two controllers and eight storage units (Figure 1-2). An additional storage unit is included as a standby device. Four data channels are used to interface the maximum subsystem.

CONTROLLER

The controller synchronizes and controls data flow between the data channel and the disk storage units. Operations in the controller are directed by standard 3000 Series signals and programmed instructions from the computer.

These instructions consist of function codes which select operating modes and interrupts, and supply address information used in data transfer. A 12-bit connect code selects the controller (equipment) and peripheral storage unit. When the connect is completed, status information on conditions within the controller become available to the computer.

Function codes condition the controller to interrupt when certain situations develop. A function code specifies the mode of operation (read or write) and prepares the controller and selected peripheral unit for an I/O operation. A Load Address function code causes the controller to prepare for a Seek operation within the selected storage unit. The computer then issues address information to the controller to select the address at which the I/O operation will commence. The data is loaded into the Address register of the controller and the Seek operation commences immediately upon termination of the output operation. If the Address loaded is a legal address, the selected storage unit seeks the position specified.

A Sector Verify operation, which ensures that the Seek operation is correct, follows the Seek operation. If no Load Address operation is performed prior to receipt of a Read or Write (R/W) signal, the I/O operation commences at the address presently held in the Address register except when a unit is at the last legal address. In the latter case, a new Seek operation must be initiated, or an Address Error is generated.

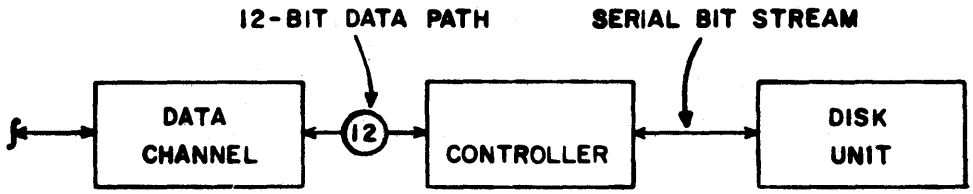

Figure 1-1. Minimum Subsystem

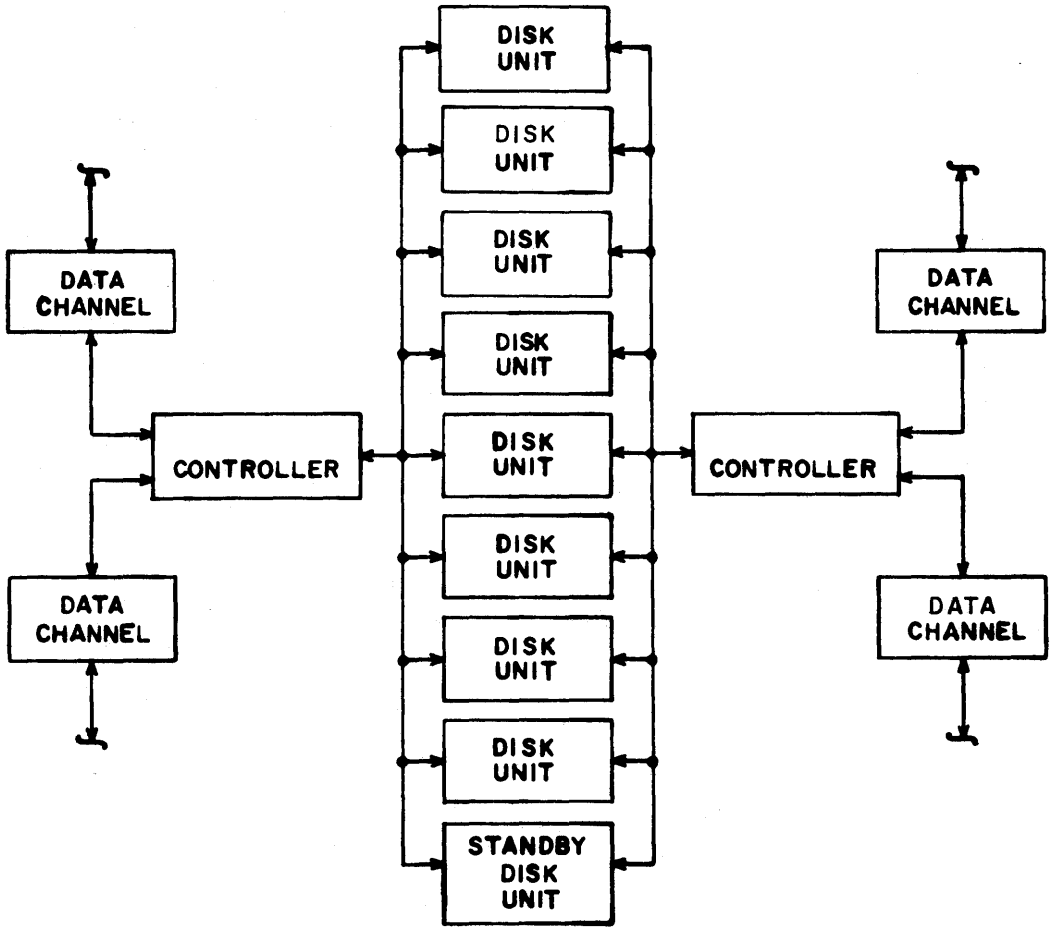

Figure 1-2. Maximum Subsystem

NOTE

The address presently held in the address register is the address of the last operation plus one. When an I/O operation is in progress (or ends) the controller automatically updates the address registers at the end of each sector except when an Address Error is detected, or when the abnormal EOP interrupt is selected and an abnormal condition occurs.

In the I/O operation the controller accepts data from the channel in parallel format (12-bit, bytes) disassembles it, and transmits the data serially to the selected storage unit. In a similar manner, the controller accepts serial data from the selected storage unit, assembles it into 12-bit bytes, and transfers it in parallel to the appropriate data channel. Error recovery procedures are also available. A variety of functions are provided to facilitate error identification and correction, depending upon the type of error present.

PERIPHERAL STORAGE UNITS

The MDD and Disk File use the cylinder concept of recording to provide optimum efficiency by minimizing physical (positioner) movement (Figure 1-3). In this concept, the data is read (and written) consecutively from sector to sector within a track on one disk surface to the corresponding track on the opposite side of the same disk. This scheme is repeated sequentially for each disk in the stack. The final result is a sequential multiple of records on the disks in a cylindrical drum pattern. This process is accomplished by electronic switching from one R/W head to the next to provide minimum access time. Both the MDD and Disk File use a ferrous oxide coating as the magnetic recording medium.

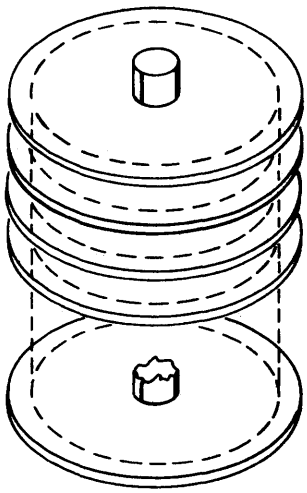

Figure 1-3. Cylinder Concept of Data Recording

MULTIPLE DISK DRIVE

The Multiple Disk Drives access mechanism consists of 20 arms mounted in pairs on a movable carriage (Figure 1-4). Each pair of arms is positioned between two disks. A single R/W head is mounted on the extremity of each arm. On an initial Seek operation (performed by loading a disk pack, closing the drawer, and pressing the START switch) the carriage moves horizontally from an initially retracted position to the first track near the edge of the disk. After a delay to permit purging of the air, the unit moves the heads to the innermost track (a distance of 2 inches from the initial position) and then withdraws the heads to track 000. During the latter process, the heads are loaded (placed in a recording attitude near the surface of the disks). The packs rotate at approximately 2400 rpm.

Five models of the MDD are available and accommodate from four to nine disk packs. The 841-3 includes four access mechanisms for four disk packs (three on line, one off line) and each higher model variety includes one more access mechanism for an additional disk pack. The 841-8 has nine access mechanisms and holds nine disk packs (eight on line, one off line).

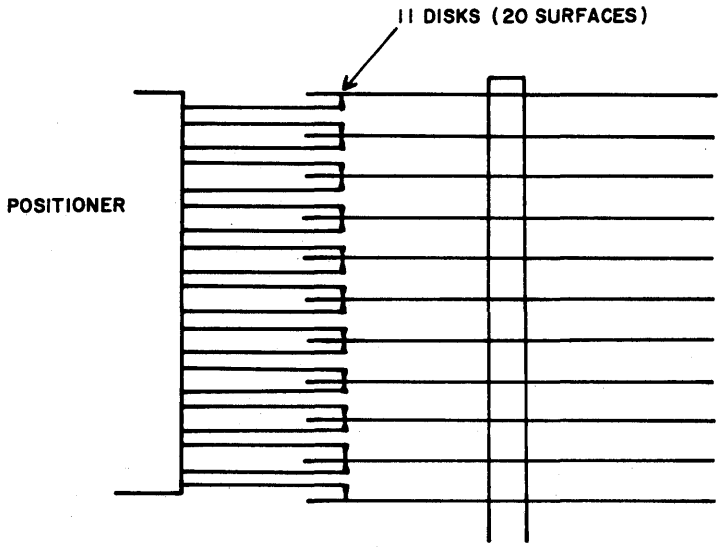

Figure 1-4. MDD Access Mechanism

There are 4060 data tracks in the MDD. The access mechanism can be stopped at any one of the 203 positions. All 20 heads are oriented on a vertical line, thus, at any position, 20 tracks are available without movement of the carriage. These 20 tracks are numbered vertically from 0 to 19, top to bottom, and can be considered a cylinder of data. The concentric cylinders are numbered 0 to 202 from the outside towards the center. Thus, the address of an individual track in a given disk storage drive unit consists of the cylinder number and R/W head number.

DISK FILE

The Disk File cabinet contains two drive spindles (Figure 1-5). A stack of 18 disks is mounted on each half of one spindle. The 18 disks provide a total of 32 recording surfaces. Each stack is subdivided into two groups; the top and bottom surfaces of each group are not used for recording. The spindles rotate (non-synchronously) at approximately 1800 rpm less induction slip.

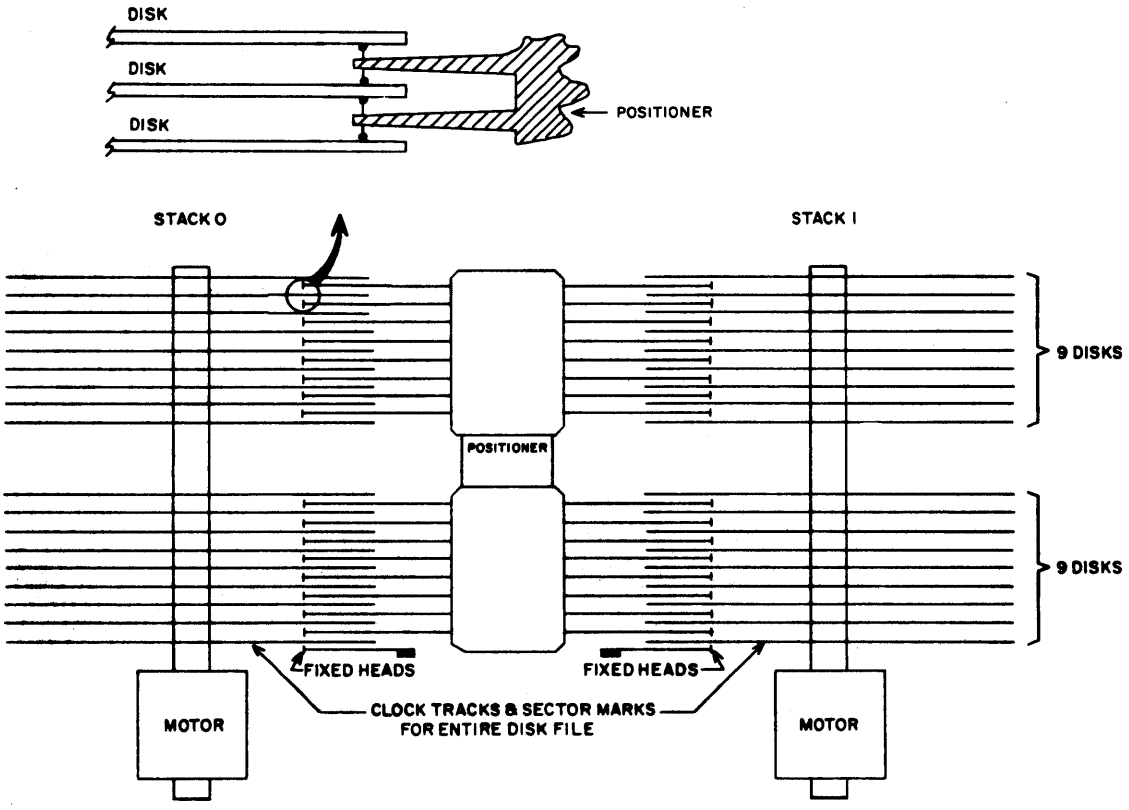

Figure 1-5. 821-1 Disk File Access Mechanism

Each disk is approximately 26 inches in diameter; each stack is approximately 18 inches high.

Two models of the 821 Disk File are available. The 821-1 Disk File contains two stacks of disks mounted on the single upper half of the spindles (Figure 1-5). A single hydraulically positioned access assembly serves the two stacks with two separate horizontally opposed groups of R/W head arms (16 arms per group). Mounted on the end of each head arm are two head pads, each containing one R/W head. There is one R/W head for each of the 32 recording surfaces in a stack. The accesses (which move simultaneously in opposite directions) can be positioned to any one of the 512 data positions to provide a total of 512 recording cylinders per stack or a non-data position (retract).

The 821-2 Disk File contains four stacks mounted on two spindles (Figure 1-6). Two independent hydraulically positioned access assemblies serve the four stacks. Each half (upper disks and positioner, or lower disks and positioner) of the 821-2 is considered as an independent file unit (units 0 and 1) and is addressed, accessed, and operated independently. Thus, access and operation of either half of an 821-2 is identical to the accessing and operation of an 821-1.

DATA ORGANIZATION

DEFINITIONS

The following definitions apply to the MDD and Disk File.

TRACK

A track is defined as the recording surface under a read/write head when it is properly positioned.

CYLINDER

A cylinder is defined as all of the recording surfaces at one position of the read/write head positioner assembly.

SECTOR

The smallest subdivision of the file.

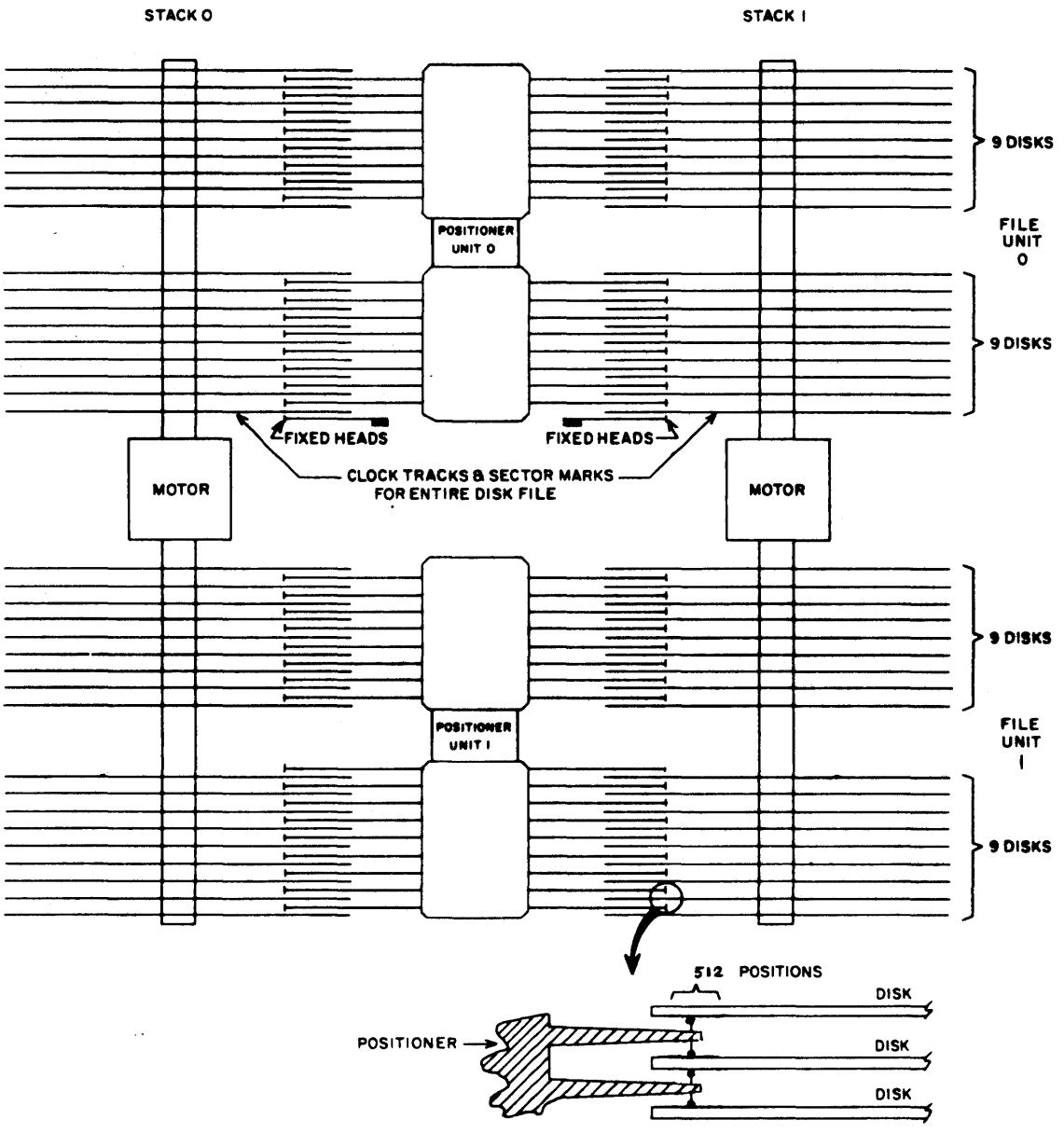

Figure 1-6. 821-2 Disk File Access Mechanism

FILE

A file is defined as all of the data contained in one logical unit (one spindle of an 841, an 821-1, or one-half of an 821-2).

MAXIMUM RECORD LENGTH

The maximum record that can be written or read without readdressing is the entire unit.

TRANSFER AND ACCESS TIMES

DATA TRANSFER

MULTIPLE DISK DRIVE

The recording frequency is 2.53 megabits per second. The average transfer rates (for 3553-2 only) are as follows:

At 1:1 interlace 2.15 megabits per second.

At 2:1 interlace 1.08 megabits per second.

DISK FILE

The recording frequency is 2.51 megabits per second. The average transfer rates (for 3553-2 only) are as follows:

At 1:1 interlace 2.19 megabits per second.

At 2:1 interlace 1.10 megabits per second.

ACCESS TIME

MULTIPLE DISK DRIVE

The average random seek time is 75 milliseconds, with a maximum time of 135 milliseconds. The average track to track seek time is 25 milliseconds.

The rotational latency is 26.78 maximum (one revolution plus one sector).

DISK FILE

The average track to track seek time is 20 milliseconds, with a maximum of 29 milliseconds. The maximum random seek time is 140 milliseconds. The maximum stack to stack access is 14 milliseconds.

CAPACITIES

The physical arrangement of the tracks and cylinders in the storage device varies dependent upon the type of storage device. Table 1-1 indicates the sector, track, and cylinder capacities of the various storage devices.

TABLE 1-1. DISK UNIT CAPACITY

	3553-1		3553-2	
	821	841	821	841
BYTE	12 BITS	12 BITS	12 BITS	12 BITS
SECTOR	322 BYTES 3,864 BITS	322 BYTES 3,864 BITS	320 BYTES 3,840 BITS	320 BYTES 3,840 BITS
TRACK	20 SECTORS 77,280 BITS	14 SECTORS 54,096 BITS	20 SECTORS 76,800 BITS	14 SECTORS 53,760 BITS
CYLINDER	64 TRACKS 4,945,920 BITS	20 TRACKS 1,081,920 BITS	64 TRACKS 4,915,200 BITS	20 TRACKS 1,075,200 BITS
LOGICAL UNIT	(1) 508 CYLINDERS 2,512,527,360 BITS	(2) 200 CYLINDERS 216,384,000 BITS	(1) 508 CYLINDERS 2,496,921,600 BITS	(2) 200 CYLINDERS 215,040,000 BITS
TOTAL OF 8 LOGICAL UNITS	1,675,018,240 BYTES 20,100,218,880 BITS	144,256,000 BYTES 1,731,072,000 BITS	1,664,614,400 BYTES 19,975,372,300 BITS	143,360,000 BYTES 1,720,320,000 BITS

NOTE

(1) plus 4 spare tracks

(2) plus 3 spare tracks

DATA FORMAT

Double frequency recording is used. With this type of recording, a clock bit is recorded at the beginning of each cell time. Data bits are recorded between the clock bits. The presence of a bit between adjacent clock bits signifies a "one", and the absence signifies a "zero" (Figure 1-7).

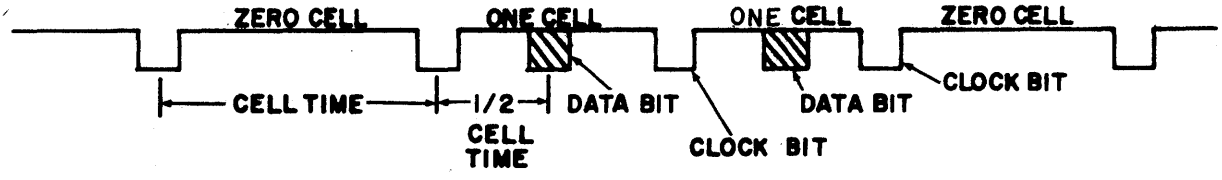

Figure 1-7. Clock and Data Bits

SECTOR FORMAT

Data is stored and addressed in discrete block (sectors). A data word (byte) consists of 12 bits. Multiple bytes are recorded in each sector. Each of the disks is divided into 14 sectors. Figure 1-8 shows the sector format. The MDD format contains 4509 bits and the disk file format contains 4380 bits. Divisions of the sector are described as follows:

3553-1 CONTROLLER

		ADDRESS FIELD					DATA FIELD				
STORAGE UNIT	TOLERANCE GAP 1	SYNC PATTERN	UPPER ADDRESS	LOWER ADDRESS	CHECK-WORD	HEAD GAP	SYNC PATTERN	DATA	CHECK-WORD	END OF RECORD	TOLERANCE GAP 2
MDD	120	112	12	12	12	120	112	3864	12	1	132
DISK F.	120	112	12	12	12	120	72	3864	12	1	43

3553-2 CONTROLLER

		ADDRESS FIELD					DATA FIELD				
STORAGE UNIT	TOLERANCE GAP 1	SYNC PATTERN	UPPER ADDRESS	LOWER ADDRESS	CHECK-WORD	HEAD GAP	SYNC PATTERN	DATA	CHECK-WORD	END OF RECORD	TOLERANCE GAP 2
MDD	120	112	12	12	12	120	112	3840	12	1	156
DISK F.	120	112	12	12	12	120	72	3840	12	1	67

Figure 1-8. Sector Format

TOLERANCE GAP 1

This 120-bit gap provides time for electronically switching the read/write heads.

SYNC PATTERN

This pattern, which consists of zero bits (71 for the 821, 111 for the 841) followed by a one bit, allows the controller to become synchronized with the address field.

ADDRESS FIELD

The address field (Figure 1-9) contains the 36-bit address header format. This consists of the upper address, lower address, and address checkword, each of which contains 12 bits. The checkword contains the cyclic code for the address field.

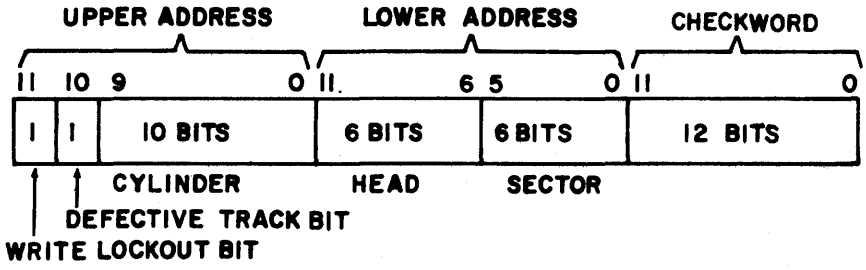

Figure 1-9. Address Field

If the write lockout bit is a one, data cannot be written in this track via program control unless the Maintenance Key Switch is on and the write lockout switch is off. If the defective track bit is a zero, it indicates that the whole track was marked as defective from the control panel and no operations can be performed on this track (an Address Error and Abnormal Interrupt occurs).

HEAD GAP

This 120-bit gap provides time for electronically switching the read/write heads.

SYNC PATTERN

This pattern, which consists of zero bits followed by a one bit allows the controller to become synchronized with the recorded data.

DATA FIELD

The data field contains 3840/3864 bits of data. An additional 12-bit byte is reserved for the checkword.

END OF RECORD BIT

This bit is recorded at the end of the sector in which the computer channel went inactive if the controller was writing in the End of Record mode.

TOLERANCE GAP 2

This gap, which allows for motor speed tolerances, is 156 bits for the MDD and 67 bits for the Disk File.

CHECKWORD

Address and data transfers are checked for accuracy by the generation of a 12-bit redundant checkword in the controller. During operations, the controller generates and verifies checkwords to determine the accuracy of addresses and data transferred between the controller and the peripheral storage devices. If checkword verification does not occur, a Checkword Error or Address Error indication is generated.

DATA TRANSFER

Data is addressed and written in a storage unit in discrete blocks (sectors); however, the data channel can read or record as little as one byte or as many bytes as necessary to reach the end of the file. When reading or writing, the operation must commence at the start of a sector. When writing less than a full sector, the remainder of the sector is automatically filled with zeros.

ADDRESSING

After transmitting the Connect code, if the operation is to start or continue at the address location presently held in the controller Address register, the Select and I/O operating mode codes are set up on completion of the connect. The address currently held in the Address register is the one in which the next I/O operation will take place. This address is automatically incremented after each sector is written or read from the selected storage unit unless:

1. The equipment becomes Not Ready during an operation.
2. The Abnormal End of Operation Interrupt is selected and any abnormal condition occurs.
3. An Address Error occurs.

This process takes place throughout the entire file from the starting address up to and including the last available address. If the I/O operation attempts to continue beyond the last available address, an Address Error occurs, and if selected, the Abnormal End of Operation Interrupt is generated. Once the last available address has been utilized, the Address register must be reset. This may be done by loading a specific address (via the Load Address function) or by executing a Master Clear, or a Clear or a Restore function instruction, which sets the register to zero.

LOAD ADDRESS

On initiation of an output operation following receipt of the Load Address function code, the controller commences loading 12-bit bytes from the data channel. These bytes form a 24-bit address word which is automatically loaded into the Address register by the controller. The first byte of the address is loaded into the upper portion of the register; the second byte into the lower portion. The output from the computer may consist of several words. The controller continues to load the bytes into the Address register as previously described until the end of the operation. Thus, the last two bytes transferred comprise the address remaining in the Address register.

NOTE

3000 Series computers disassemble words upper byte first.

ADDRESS FORMAT

Figure 1-10 shows the address format. The address specifies the cylinder and the track and sector within that cylinder at which the next operation takes place.

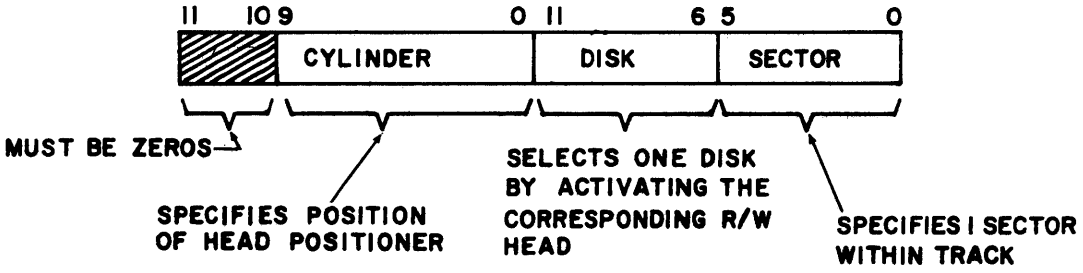

Figure 1-10. Address Format

TABLE 1-2. ILLEGAL ADDRESSES

	MDD	DISK FILE
CYLINDER	313_8 AND ABOVE	2000_8 AND ABOVE
TRACK	24_8 AND ABOVE	40_8 AND ABOVE
SECTOR	16_8 AND ABOVE	24_8 AND ABOVE

BUFFER MEMORY

To allow the minimum channel byte rate, a buffer memory is used in conjunction with the 3000 Series Data Channel(s) to average the data transfer over the entire time the channel is active instead of only within the data field. The buffer memory operates in such a manner that it can be loading from the data channel while unloading to the storage device or vice versa. The only requirement is that the buffer memory be full (320 bytes) before reaching a data field where a Write operation will occur, or empty before reaching a data field where a Read operation will occur.

INTERLACE

The controller may be used to average the channel data rate over a longer period of time by interlacing sectors. Interlacing is a system of using a sector, skipping a fixed number of sectors, using the next sector and so on. When recording headers on the pack to initialize it, the interlace desired is entered in the maintenance panel and the proper header is written in the correct sector. Every sector is used sequentially under normal operations (1:1 interlace). Every other sector is used at 2:1 interlace. With a 1:1 interlace, a track is completely processed in one revolution. With a 2:1 interlace, two revolutions are required to completely process a track. With a 2:1 interlace, the average minimum transfer time is 89,000 bytes per second for the MDD and 93,000 bytes per second for the disk file.

ACCESS TIME

Access time is equal to cylinder positioning time plus rotational latency time. Table 1-3 lists the possible access times.

TABLE 1-3. ACCESS TIMES

Multiple Disk Drive	Maximum move	135 msec
	Maximum one track move	25 msec
	Average random move	75 msec
	Maximum latency	26.8 msec
	Average latency	12.5 msec
Disk File	Maximum move	145 msec
	Maximum one track move	29 msec
	Average random move	80 msec
	Maximum latency	36 msec
	Average latency	17 msec
	STACK to STACK	14 msec

CODES 2

INTRODUCTION

This section explains all function and status codes applicable to the 3553 Disk Storage Controller and associated subsystem.

Table 2-1 lists all of the codes.

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES

CONNECT	
Connect 3553 and Storage Unit	N0DU*
FUNCTION	
Channel Release	0000
Restore	0001
+1 Cylinder Seek***	0002
-1 Cylinder Seek***	0003
Clear	0005
Drive Release	0007
Load Address at 1:1 Interlace	0010
Return Address	0011
Load Address at 2:1 Interlace**	0012
Read Disk Address***	0013
Load Address at 4:1 Interlace**	0014
Load Address at 8:1 Interlace**	0016
Select Interrupt on Ready and Not Busy	0020
Release Interrupt on Ready and Not Busy	0021
Select Interrupt on End of Operation	0022
Release Interrupt on End of Operation	0023

* N = equipment number of controller
D = device type (1 = MDD; 2 = Disk File)
U = logical unit number of storage device
** 3553-2 only
*** Applies only to models containing error recovery logic.

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES (Cont'd)

Select Interrupt on Abnormal End of Operation	0024
Release Interrupt on Abnormal End of Operation	0025
Select Interrupt on Opposite Channel Release	0026
Release Interrupt on Opposite Channel Release	0027
Select Interrupt on End of Seek	0030
Release Interrupt on End of Seek	0031
Disk File Status***	0032
Clear Disk File Status***	0033
Disable Sector Verify***	0034
Write Address Normal***	0035
Write Address Defective***	0036
Write Address Write Lockout***	0037
Margin Selection***	04XX
Read	0040
Write	0041
Search Compare	0042
Marked Search Compare	0043
Checkword Verify	0044
Read Checkword	0045
Magnitude Search (Record $\leq$ Buffer)	0050
Magnitude Search (Record $\geq$ Buffer)	0051
Equality Search (Record = Buffer)	0052
Buffer Mode	0053
End of Record Mode	0054

*** Applies only to models containing error recovery logic.

TABLE 2-1. CONNECT, FUNCTION, AND STATUS CODES (Cont'd)

STATUS		
Ready	0	XXX1
Busy	1, $\overline{2}$	XXX2
Abnormal/Unavailable	2	XXX4
Unit Reserved	1, 2	XXX6
On Sector	3, $\overline{2}$	XX10
Address Error	3, 2	XX14
No Compare	4, $\overline{2}$	XX20
Operation Error *	4, 2	XX24
Lost Data **	4, 2	XX24
End of Record	5, $\overline{2}$	XX40
Checkword Error	5, 2	XX44
Write Lockout on Read (normal)	6, $\overline{2}$	X1X0
Write Lockout on Write (abnormal)	6, 2	X1X4
Positioner Ready	7	X2XX
End of Operation Interrupt	8	X4XX
Abnormal End of Operation Interrupt	9	1XXX
Seek Interrupt	10	2XXX
Reserved	11, $\overline{2}$	4XX0
Defective Track	11, 2	4XX4

* 3553-2

** 3553-1

CONNECT CODE

The 12-bit Connect code (Figure 2-1) designates the equipment (controller), the peripheral device type (MDD or Disk File) and the unit with which the computer is to communicate.

Reservation in the controller is set up on a data channel basis. Reservation in the storage unit is controller basis. Once the data channel is connected to the controller and unit, they are both reserved until specifically released by that channel via a MC, channel clear, Drive Release, or Release function code.

Upon receipt of the Connect code by the controller, a Reply or Reject is returned to the data channel. If the desired controller and unit are available, and no transmission Parity Error occurs, a Reply is returned. If the controller is unable to accept and perform the connect, a Reject is returned. Upon receipt of a Reject, the computer may request a status response and sense the status bits in order to determine whether the Reject was a result of the controller being reserved, the storage type being non-existent, or the unit being unavailable or reserved by another controller. Refer to the explanation of status response bits Unavailable (XXX4), Unit Reserved (XXX6), or Controller Reserved (4XXX).

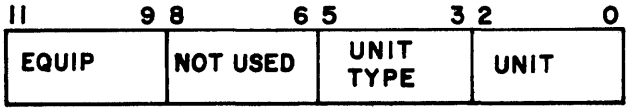

Figure 2-1. Connect Code

BITS 0-2

These 3 bits designate the logic unit (0-7) with which the program communicates. The number designated is variable from 0-7 by means of the unit designation Plug located on the Storage device.

BITS 3-5

These 3 bits designate the type of peripheral device.

XX1X MDD

XX2X Disk File

BITS 6-8

These bits are not used.

BITS 9-11

These 3 bits designate the equipment (controller). The number is variable from 0-7 by means of the rotary Equipment Number switch located on the controller Maintenance Panel.

FUNCTION CODES

The function codes consist of control and address codes which affect the reservation of the controller and the positioning of the R/W heads. The interrupt codes set and remove interrupt selections. The error recovery codes allow flexibility and control in the determination and correction of various error conditions. The I/O codes define the input and output operations and the mode select codes are used to set parameters of the search-compare operation.

A Reject is issued upon receipt of a function code whenever the controller is busy with an operation other than a seek.

A Reply is issued upon receipt of an unassigned function code, but the code does not produce action in the controller.

CONTROL AND ADDRESS CODES

The control codes provide the computer with a means of releasing the subsystem, removing all reserves, I/O selections, interrupt signals, and deselecting the data channel. The address codes are used to address the selected storage unit or to return the current address. In either case the address is loaded into or taken from the controller Address register.

CHANNEL RELEASE (0000)

This code logically releases the subsystem from the data channel. It causes all controller and unit reserves to be removed, clears all interrupt signals (except Interrupt on Opposite Channel Release), removes all I/O code selections, clears the read parity and write check error conditions, and drops the status response lines.

RESTORE (0001)

This code initiates a seek to position (cylinder) zero.

+1 CYLINDER SEEK (0002)*

This code initiates a forward one-cylinder seek. A seek forward and a difference count of one is sent to the disk unit without computing the difference or restoring to zero. The automatic restore is cleared. This function does affect the contents of the address register in the controller, cylinder, head, and sector register in the drive. Interrupts resulting from this operation are the same as a seek operation, except for the seek interrupt. It is generated if the last operation was a seek. It is not generated if the last operation was a read or write. The seek interrupt generated by this function is identical to that of a Restore code (0001).

–1 CYLINDER SEEK (0003)*

This code is identical to the 0002 function, except that a seek is initiated in the reverse direction.

CLEAR (0005)

This code clears all major components in the subsystem, but does not affect the connect, reserved, or unit select status of the subsystem.

DRIVE RELEASE (0007)

This code logically releases the drive unit addressed when the function is initiated and clears the On Sector status in the storage unit.

LOAD ADDRESS AT 1:1 INTERLACE (0010)

This code causes the next output data to be loaded into the 24-bit controller Address register. The data is continuously loaded into the Address register until the output operation terminates. On completion, a Seek operation is automatically initiated in the selected storage unit. All subsequent Load Address functions to ANY storage unit are rejected until the controller has instructed the unit to seek, and has generated an EOP or the positioner ready drops.

The storage device provides an on-sector signal two sectors before the desired section with a 3553-2 and one sector before the desired sector with a 3553-1.

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* Applies only to models containing error recovery logic.

RETURN ADDRESS (0011)

This code, in conjunction with an input operation, causes the controller to return the content of the 24-bit Address register to the data channel. The address is continuously returned until the input operation terminates.

LOAD ADDRESS AT 2:1 INTERLACE (0012) **

This function is similar to the Load Address function. Address headers should be written at a 2:1 interlace. The on-sector signal is provided three sectors prior to the desired address.

READ DISK ADDRESS (0013)*

This code causes a 36-bit input buffer to return the address read from the disk unit. The address read will be that specified by the address register. An End of Operation interrupt is generated after the third 12-bit byte of data. An End of Record is sent on the fourth byte, if requested.

LOAD ADDRESS AT 4:1 INTERLACE (0014) **

This function is similar to the Load Address function. Address headers should be written at a 4:1 interlace. The on-sector signal is generated at on-cylinder plus sector zero time.

LOAD ADDRESS AT 8:1 INTERLACE (0016)**

This function is similar to the Load Address function. Address headers should be written at an 8:1 interlace. The on-sector signal is generated at on-cylinder plus sector zero time.

INTERRUPT CODES

These codes establish and remove the interrupt selections which determine which conditions send an Interrupt signal to the data channel.

The interrupt signal and status are cleared by Master Clear, Channel Clear, or any function.

An Interrupt selection is cleared by Master Clear, Channel Clear, Function Clear, Clear Selected Interrupt, and Channel Release. The Channel Release function does not clear the release interrupt.

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* Applies only to models containing error recovery logic.

** 3553-2 only.

SELECT INTERRUPT ON READY AND NOT BUSY (0020)

Selection of this code causes the interrupt line to be activated and the associated status bit set the next time the subsystem becomes Ready and Not Busy (at the end of the next operation). For an explanation of Ready and Not Busy conditions, refer to the associated status response bit description.

RELEASE INTERRUPT ON READY AND NOT BUSY (0021)

This code removes the associated interrupt selection set up by the 0020 code. No interrupt notification of Ready and Not Busy is sent until the condition is reselected.

SELECT INTERRUPT ON END OF OPERATION (0022)

This code causes the interrupt line to be activated and the associated status bit to be set on completion of the next operation whether the end of operation is normal or abnormal.

Most operations are completed at the end of a sector; however, if the operation is completed before the end of the sector is reached, the End of Operation signal is delayed until the end of that sector.

RELEASE INTERRUPT ON END OF OPERATION (0023)

This code removes the associated interrupt selection set up by the 0022 code. No interrupt indication of end of operation is sent until the condition is reselected.

SELECT INTERRUPT ON ABNORMAL END OF OPERATION (0024)

This code causes the interrupt line to be activated and the associated status bit set on the stopping of an operation due to any abnormal condition within the controller or selected storage unit.

The following conditions are considered abnormal:

1. An Address Error is detected.
2. Any attempt to write at a location which is in a Write Lockout state.
3. Occurrence of a Checkword Error (indication of an error in the data read from the selected storage unit).
4. Occurrence of a Operation Error (a hardware failure in the controller that results in the loss of data).
5. Any attempt to perform an operation on a defective track.

RELEASE INTERRUPT ON ABNORMAL END OF OPERATION (0025)

This code removes the associated interrupt selection set up by the 0024 code. No interrupt indication of Abnormal End of Operation is sent until the condition is reselected.

SELECT INTERRUPT ON OPPOSITE CHANNEL RELEASE (0026)

This code causes an Interrupt signal to be sent and the associated status bit set whenever the opposite data channel (the channel presently maintaining Reserved state of the controller) releases its reservation of the controller and storage units. If only one data channel is connected to the controller, this code is not applicable and should not be used.

NOTE

The interrupt is conditioned upon the dropping of the reserve. Therefore, a Master Clear causes the interrupt only if the data channel executing the Master Clear has the subsystem reserved.

RELEASE INTERRUPT ON OPPOSITE CHANNEL RELEASE (0027)

This code removes the associated interrupt selection set up by the 0026 code. No interrupt indication of a release by the opposite channel is sent until the condition is reselected.

SELECT INTERRUPT ON END OF SEEK (0030)

This code causes the interrupt line to be activated and the associated status bit set at the end of the Seek operation (in any storage unit) regardless of whether the seek was complete or incomplete.

RELEASE INTERRUPT ON END OF SEEK (0031)

This code removes the associated interrupt selection set up by the 0030 code. No interrupt indication of an End of Seek operation is sent until the condition is reselected.

ERROR RECOVERY CODES *

These codes provide positive error identification and recovery techniques. They allow, when needed, sampling of conditions in the disk file, disabling sector verify, or the writing of address headers without certain restrictions. The margin selection function allows movement of the positioner in small increments to circumvent track defects, if necessary. It also provides for varying the read strobe to adjust for fluctuations in read timing.

* Applies only to models containing error recovery logic.

DISK FILE STATUS (0032)

This code brings up the Read Status Select line to enable the file fault status on to the control bus. The controller switches the channel status lines to receive the file status. This function is accepted by the controller and a reply generated whether the controller is ready or not, provided there is no transmission parity error. A reject is generated if the controller is busy. This function is cleared by a 0033, 0000, 0005 code, or a Master Clear.

The file status is displayed on the maintenance panel by setting the REGISTER SELECT switch to FILE STATUS. The status bit assignments are as follows.

Bit 0	Clock 0 Error	Bit 6	Pack 3 Error
Bit 1	Clock 1 Error	Bit 7	Logic Error
Bit 2	Voltage Error	Bit 8	Channel Error
Bit 3	Pack 0 Error	Bit 9	On Cylinder Error
Bit 4	Pack 1 Error	Bit 10	Not Used
Bit 5	Pack 2 Error	Bit 11	Not Used

CLEAR DISK FILE STATUS (0033)

This code clears the Disk File Status function selection. The Reply and Reject conditions are the same as for the 0032 function.

DISABLE SECTOR VERIFY (0034)

This code suppresses the need to verify the address before a read, write, or search operation. This function must precede the 004X functions and clears on the next End of Operation. Multi-sector operations are possible. The Defective Sector and Write Lockout Status are suppressed during this operation.

Selection of this code requires the correct address of the pack or disk to be specified in the last seek operation. A Read Disk Address code (0013) should precede this function to ensure that the head is properly positioned.

WRITE ADDRESS NORMAL (0035)

This code, when followed by a Load Address operation, writes a new header in the sector specified by the Address register. The Load Address operation initiates the write header operation. No seek interrupt occurs on a programmed write header. An End of Operation is generated if previously selected. A Read Disk Address code (0013) should precede this function to ensure that the read/write head is properly positioned.

WRITE ADDRESS DEFECTIVE (0036)

This code is identical to the 0035 code except the defective sector bit is added in the header.

WRITE ADDRESS LOCKOUT (0037)

This code is identical to the 0035 code except the write lockout bit is added in the header.

MARGIN SELECTION (04XX)

This code sends eight bits to the disk resulting in small increments in cylinder movement or small variations in the read strobe time, depending on the bit assignments (Figure 2-2). A Reply is sent to the channel if the controller is Ready and Not Busy, and if no transmission parity error exists. A Reject is generated if the controller is Busy or Not Ready, with one exception; the Clear Fault function (0600) is accepted if the controller (or unit) is Not Ready.

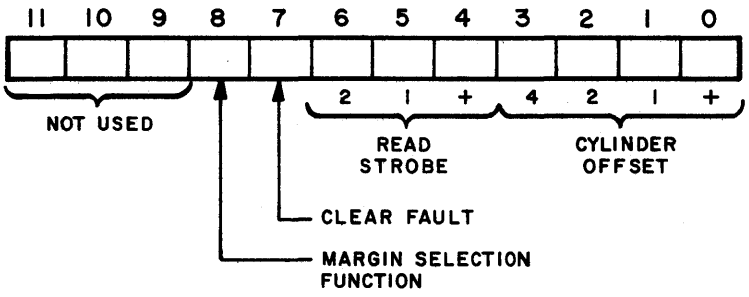

Figure 2-2. Margin Selection Code Bit Assignments

CYLINDER OFFSET

This portion of the function moves the positioner in increments of 0.0005 of an inch in the 821 Disk File. The disk file drops to an On Cylinder condition for a minimum of 10 milliseconds. The maximum time will be less than one cylinder move. The Busy status goes up during the function, and drops when the On Cylinder condition comes up. Only Read operations are allowed off cylinder. A Write operation in any offset position other than zero generates a fault, and drops Ready. No interrupts are generated during this operation.

Function	Offset (inch)	Function	Offset (inch)
0400	-0.0000	0410	-0.0020
0401	+0.0000	0411	+0.0020
0402	-0.0005	0412	-0.0025
0403	+0.0005	0413	+0.0025
0404	-0.0010	0414	-0.0030
0405	+0.0010	0415	+0.0030
0406	-0.0015	0416	-0.0035
0407	+0.0015	0417	+0.0035

READ STROBE

This portion of the function varies the read strobe in increments of 10 nanoseconds in the 821 Disk File. No Busy status or interrupts are generated other than the normal Reply or Reject signals.

Function	Offset (nanoseconds)
0400	-00
0420	+00
0440	-10
0460	+10
0500	-20
0520	+20
0540	-30
0560	+30

CLEAR FAULT (0600)

This bit, when set, clears all fault status conditions in the disk file except when a solid fault condition is present.

Examples of Margin Selection functions are as follows:

- 0407 - Select offset +0.0015, and clear read strobe.
- 0527 - Select offset +0.0015, and select read strobe +20 nsec.
- 0537 - Select offset +0.0035, and select read strobe +20 nsec.
- 0417 - Select offset +0.0035, and clear read strobe.
- 0400 - Clear offset and clear read strobe.
- 0600 - Clear fault, clear offset, and clear read strobe.

INPUT/OUTPUT CODES

These codes define the conditions for the various data handling operations which cause the transfer of data between the data channel and/or the controller and the selected peripheral storage device. With the exception of Checkword Verify, all codes require initiation of an input or output operation in order to activate the subsystem. See Programming Considerations for timing diagrams of buffered I/O operations.

READ (0040)

This code, in conjunction with an input operation causes the controller to initiate a Read operation from the selected storage unit at the address specified by the content of the controller Address register. The operation continues until halted by one of the conditions listed under Interrupt on End of Operation. When operating in End of Record mode, an EOR signal is transmitted to the data channel on detection of a record mark at the end of a data block.

WRITE (0041)

This code, in conjunction with an output operation, causes the controller to initiate a Write operation to the selected storage unit at the address specified by the content of the controller Address register. The operation continues until halted by one of the conditions listed under the Interrupt on End of Operation. If an output operation terminates before the end of the current data block, the remainder of the block is automatically filled with zeros. The checkword is always written at the end of the sector. When operating in EOR mode, an EOR mark is recorded at the end of the last block written.

SEARCH COMPARE (0042)

This code, in conjunction with an output operation, causes the controller to initiate a Read operation from the selected storage unit at the address specified by the content of the controller Address register.

The output operation transmits data to the controller which is compared by bytes on a bit-by-bit basis with the data read from the storage unit. The compare is performed according to the previous settings of the Mode Select functions.

Upon occurrence of a miscompare (unsuccessful comparison) the No Compare status bit is set.

MASKED SEARCH COMPARE (0043)

This code, in conjunction with an output operation, causes the controller to initiate a Read operation from the selected storage unit at the address specified by the content of the controller Address register.

The output operation transmits data to the controller which is compared by bytes on a bit-by-bit basis with the data read from the storage unit; however, if a byte in the output data contains all ones (7777_8) no comparison is made on the associated byte read. This compare is performed according to the previous settings of the Mode Select function.

Upon occurrence of a miscompare (unsuccessful comparison) the No Compare status bit is set.

CHECKWORD VERIFY (0044)

On receipt of this function code by the controller, the data within the current cylinder is read and checked for an illegal checkword. Operation commences at the present address position of the Read/Write heads and continues to the end of that cylinder.

When operating in End of Record mode, only one record is verified or if no record mark is present, the rest of the file is verified.

READ CHECKWORD (0045)

This operation, in conjunction with an input operation, causes the controller to initiate a Read operation from the selected storage unit at the address specified by the content of the controller Address register. This operation is identical to the 0040 Read function except that all data checkwords read are returned to the data channel along with the data. In the 3553-2 controller, this operation is limited to one sector.

There is one 12-bit checkword per sector in the disk file and disk drive units.

The operation continues until halted by one of the conditions listed under Interrupt on End of Operation.

MODE SELECT CODES

These codes select and specify the conditions under which the 0042 Search Compare or 0043 Masked Search Compare functions operate, and determine the conditions under which an end of operation occurs.

MAGNITUDE SEARCH (RECORD $\leq$ BUFFER) (0050)

This code modifies the Search Compare operation such that the comparison is satisfied if the data read (searched) is equal to or less than the output data.

The search is unsuccessful (no compare status bit sets) when the first (high order) output data bit is a "0" and the record bit is a "1".

MAGNITUDE SEARCH (RECORD $\geq$ BUFFER) (0051)

This code modifies the Search Compare operation such that the comparison is satisfied if the data read (searched) is equal to or greater than the output data.

The search is unsuccessful (no compare status bit sets) when the first (high order) output data bit is a "1" and the record bit is a "0".

EQUALITY SEARCH (RECORD = BUFFER) (0052)

This code modifies the Search Compare operation such that the comparison is satisfied only if the data read (searched) is equal to the output data. Any MC operation automatically selects the mode of operation.

The search is unsuccessful (no compare status bit sets) when the first unmasked output data bit is different from the record bit read.

BUFFER MODE (0053)

This code prepares the controller for a subsequent I/O operation wherein the end of operation is defined as the word count of the I/O operation. (Refer to Buffer Restrictions under Programming Considerations.)

END OF RECORD MODE (0054)

This code prepares the controller for a subsequent I/O operation wherein the end of operation is defined as the limit of the record as follows:

- Write - a record mark is recorded at the end of the sector in which the output operation ended. The original output operation may be from less than a single sector to an entire file in length.
- Read - an End of Record signal is sent to the data channel each time the record mark is detected.

Any MC automatically selects this mode of operation.

STATUS CODES

In order for the computer to determine the state of the controller and storage units, a 12-bit status response is available to the data channel. The computer initiates a Copy Status instruction and samples the status response on the lines from the controller. The computer may sample a status response whenever connected, or after a connect attempt is rejected because the controller and/or peripheral units are under control or reservation by a different data channel. The status response may be a combination of any of the available response bits.

The status response bits (Table 2-1) indicate the state of the controller and storage unit to which the data channel is connected or last attempted to connect. A "1" in the bit position

indicates the condition is present (or has occurred); a "0" indicates the condition is not present (or has not occurred). It should be noted that an interrupt must previously have been selected or the associated interrupt status bit will be a "0" even though a condition that would normally set the interrupt has occurred (for example, a copy status does not indicate that an abnormal end of operation has occurred unless the Abnormal End of Operation Interrupt is selected). If the Abnormal End of Operation Interrupt is selected, the operation ends, the Interrupt Error status bits are set and the interrupt is sent to the data channel immediately upon occurrence of the error condition. However, if the Abnormal End of Operation Interrupt is not selected, the error status bits are set immediately upon occurrence of the error condition even though the operation may not end until the buffer is completed.

READY (XXX1) - BIT 0

The presence of this bit indicates the unit last connected is in an operable condition and ready for use. A storage unit is considered Ready when it is available and ready to operate. The unit becomes Not Ready for the following conditions:

Disk File and Disk Drive Units

1. Disk Pack not loaded (applicable to disk drive unit only)
2. R/W heads not landed
3. Disk motor not up to speed
4. File or disk drive Unsafe condition from selected unit (refer to Unsafe Conditions)
5. No such unit
6. Unit reserved by another controller
7. Unit is in OFF line mode

Only conditions 5, 6, and 7 cause a Reject on Connect.

Any 1X, 4X, or 5X function code is rejected when the controller is Not Ready; other function codes are accepted even if the controller is not Ready. If a unit becomes Not Ready during an operation, the operation ceases immediately and (if selected) the Abnormal End of Operation interrupt is sent to the data channel.

BUSY (XXX2) - BIT 1

The presence of this bit indicates the controller and/or peripheral unit specified by Connect code are currently performing an operation and are unable to initiate any new action at this time. The bit becomes a "0" at the end of operation.

The Busy status normally follows the Channel Busy signal; however, the Busy status remains until the checkword has been written or read and the Address register updated. The End of Operation interrupt occurs at this time. Any abnormal condition which causes an end of operation to occur causes the Busy status to drop.

In the case of a Checkword Search even though no I/O Operation is initiated, the subsystem is busy until the search is finished.

A storage unit is Busy following a Seek initiation until the seek is completed; however, the controller is available for operation to a different unit as soon as the Positioner Ready signal drops.

ABNORMAL/UNAVAILABLE (XXX4) - BIT 2

When the system is connected and reserved, the presence of this bit indicates that an abnormal condition exists in the controller or storage unit and assigns a different meaning to the status bits XX1X through X1XX and 4XXX.

If a connect attempt is rejected, the presence of this bit indicates that the storage unit requested by the Connect code was unavailable.

Two types of unavailability exist, permanent and temporary.

Permanent Unavailability: When a unit is unavailable and Not Ready it is considered to be permanently unavailable (manual intervention is necessary to remove the cause of unavailability).

Temporary Unavailability: When a unit is Reserved it is considered to be temporarily unavailable.

UNIT RESERVED (XXX6) - BITS 1, 2

The presence of this code indicates that the unit is reserved by another controller.

ON SECTOR (XX10) - BITS 3, $\overline{2}$

The On Sector status bit comes up prior to the addressed sector with or after the Positioner Ready status. This allows the computer a time slot in which to initiate an operation on the addressed sector. If no operation is initiated within this time slot, the On Sector status bit drops and comes up again one revolution later.

ADDRESS ERROR (XX14) - BITS 3,2

The presence of this code indicates that an Address Error has been detected due to one of the following conditions:

1. The Address register contains an illegal address.
2. The content of the Address register does not compare with the address being read from the storage unit.
3. The controller has been requested to operate beyond the storage unit address limits.
4. The Seek operation initiated by the Load Address was incomplete.
5. Defective Track bit is present.
6. Checkword error occurs during address verification.
7. A Seek Error from the disk file or disk drive.

If an error occurs during an operation, the operation ends immediately, and if selected, an Abnormal End of Operation Interrupt is transmitted. A new Load Address function should be performed before any new I/O is attempted.

For the models containing error recovery logic, the following additional bits further define the Address Error status. Other bit combinations are possible.

(0255) Address Error with checkword error - This results from a read error which causes a header checkword error.

(4355) Address Error with checkword error, defective sector, and write-lockout detected. This condition is the same as 0255 except that the incorrect sync bit causes other bits to be detected.

(4205) Defective Sector status - The defective sector bit without Address Error indicates the header was tagged defective by the computer or the maintenance panel.

NO COMPARE (XX20) - BITS $4,\overline{2}$

The presence of this status code indicates that a miscomparison was detected during the preceding Search Compare Operation.

OPERATION ERROR (XX24) - BITS 4,2 *

This bit is present when the following errors occur:

1. Failure to get a Resume from memory.
2. Receiving a sector mark before EOP.

If previously selected, an ABN EOP will be transmitted.

LOST DATA (XX24) - BITS 4,2 **

This bit is present when the computer has not responded soon enough to record all data correctly from the selected storage unit.

If previously selected, an ABN EOP will be transmitted.

END OF RECORD (XX40) - BITS 5,$\overline{2}$

The presence of this bit indicates that an End of Record bit has been detected at the end of the last sector when operating in End of Record mode. If the subsystem is not operating in the End of Record mode this bit is a "0" even if an End of Record bit is present at the end of a sector.

CHECKWORD ERROR (XX44) - BITS 5,2

The presence of this status code indicates that an incorrect checkword has been detected during a Read, Search Compare, or Checkword Verify operation.

WRITE LOCKOUT ON READ (X1X0) - BITS 6,$\overline{2}$

On an input (Read) operation it is permissible to operate in a Write Protected area and other than setting this status bit, operation proceeds in a normal manner.

WRITE LOCKOUT ON WRITE (X1X4) - BITS 6,2

For an output (Write) operation this is an abnormal condition, and if the Abnormal End of Operation Interrupt is selected, operation ends immediately upon initiation of the operation and the Abnormal End of Operation Interrupt sets.

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* 3553-2 only.

** 3553-1 only.

If the Abnormal End of Operation Interrupt is not selected, the output data is accepted by the controller; however, the data accepted is ignored and no data is written on the selected storage unit.

POSITIONER READY (X2XX) - BIT 7

The presence of this bit indicates that a Positioner Ready signal has been received from the selected storage unit. In the disk file and disk drive units this signal comes up as soon as the positioner is settled on the cylinder. The Positioner Ready must come up before On Sector can come up.

The Positioner Ready status stays up until a new Load Address operation is initiated. If selected, an End of Operation interrupt sets when the Positioner Ready is dropped.

See Programming Considerations for timing diagrams showing the relationship between the On Sector and Positioner Ready signals.

END OF OPERATION INTERRUPT* (X4XX) - BIT 8

The presence of this bit indicates the interrupt caused by an End of Operation.

ABNORMAL END OF OPERATION INTERRUPT* (1XXX) - BIT 9

The presence of this bit indicates the interrupt was caused by an Abnormal End of Operation.

SEEK INTERRUPT (2XXX) - BIT10

The presence of this bit indicates the interrupt was caused by the end of a Seek operation (in any storage unit) regardless of whether the Seek was complete or incomplete.

RESERVED (4XX0) - BITS 11, $\overline{2}$

The presence of this status code indicates the last Connect attempted to the subsystem was rejected because the controller was reserved by the opposite data channel.

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*For an explanation of End of Operation and an Abnormal End of Operation (see Interrupt codes 0022 and 0024).

DEFECTIVE TRACK (4XX4) - BITS 11, 2

The presence of this status code indicates a Defective Track bit has been detected at the address referenced by the content of the controller Address register. Once a track is marked defective, any I/O operation attempted on that track hangs up and an Address Error occurs (see Abnormal EOP interrupt). The Defective Track bit is written manually into the header via the maintenance panel.

SWITCHES AND INDICATORS 3

INTRODUCTION

The maintenance panel (Figure 3-1) and the switch panel (Figure 3-2) contain the switches and indicators for controlling and monitoring conditions within the equipment during operation and maintenance. The functions of the switches and indicators are described as follows.

MAINTENANCE PANEL SWITCH/INDICATORS

CONTROL PANEL (KEY SWITCH)

For normal programmed operation, this switch should be off. The switch is used to activate other switches on the maintenance panel.

DEVICE SELECT SWITCH

This rotary switch selects the device type (disk drive, disk file) from the maintenance panel.

REGISTER SELECT SWITCH

This rotary switch provides the capability for displaying and entering information via the Register Indicators/Switches to or from the register selected.

DEFECTIVE TRACK SWITCH

For normal programmed operations this switch should be OFF. This toggle switch is used to write a Defective Track bit in each sector of the Address Headers (refer to Procedures for Writing Address Headers).

DATA SWITCH

For normal programmed operations, this switch should be in the READ position. In the WRITE position, this toggle switch provides for writing data from the panel via the Register

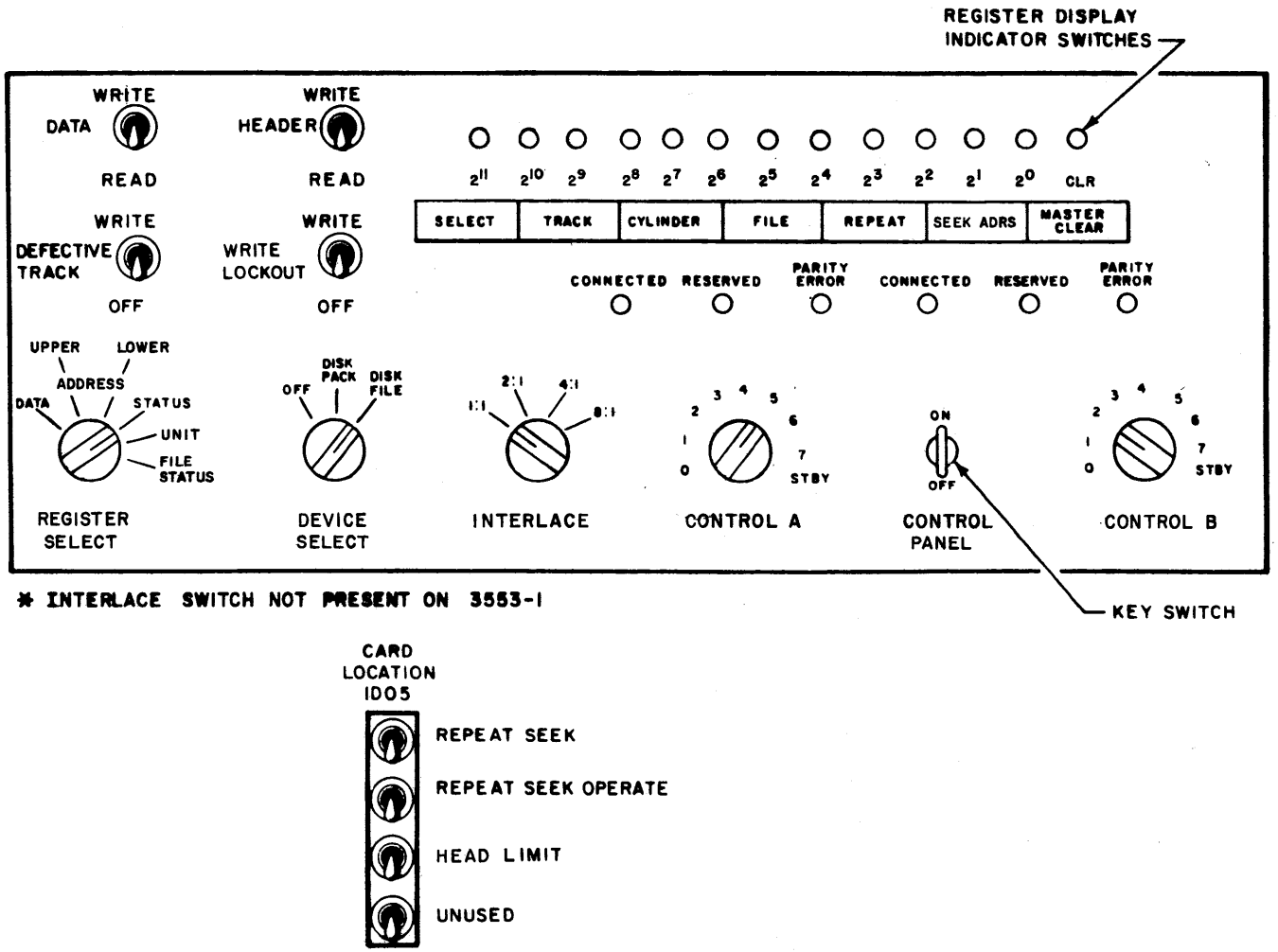

Figure 3-1. Maintenance Panel and Controls

indicator/switches. The same data (byte) is written in the entire storage area specified by the mode selected (TRACK, CYL and File).

In the READ position this switch provides for reading data from the selected storage area. The data read IS NOT displayed in the Data register when operating from the panel; however, a checkword error and other errors are displayed in the Status register.

HEADER SWITCH

For normal programmed operations this switch should be in the READ position. This toggle switch provides for writing or reading address headers in the storage area selected during a control panel operation according to the setting of the ending mode switches (see Procedures for Writing Address Headers).

WRITE LOCKOUT SWITCH

This switch, with the Key Switch in the designated positions, operates as follows.

WRITE LOCKOUT	KEY	DATA
ON/OFF	OFF	Data is protected during a computer Write operation if the WLO bit is present in the address headers.
ON	ON	Same as above.
OFF	ON	Data is Not protected even if the WLO bit is present.

CAUTION

Data is not protected during panel operations if the HEADER switch is in the WRITE position.

INTERLACE SWITCH (3553-2 ONLY)

This switch selects one of four interlace patterns at which the headers will be written.

NOTE

The following three switches located at card location 1D05A (Figure 3-1) are on controller models which do not contain error recovery logic. On the models containing error recovery logic, these switches are replaced by a switch panel (Figure 3-2).

REPEAT SEEK SWITCH

This switch is for maintenance purposes only and causes the disk unit to seek alternately between cylinder zero and the selected cylinder when:

1. It is on (up position), lights SEEK ADRS indicator.
2. Track or cylinder mode is selected.
3. The SEEK ADRS switch is pressed.

REPEAT SEEK AND OPERATE SWITCH

This switch is for maintenance purposes only and causes the disk unit to seek alternately between cylinder zero and the selected cylinder and perform an operation when:

1. It is on (up position).
2. The REPEAT SEEK switch is on.
3. Track or cylinder mode is selected.
4. The SEEK ADRS switch is pressed.

The controller will stop for an error condition and the REPEAT switch will not override an error.

HEAD LIMIT SWITCH

This switch is for maintenance purposes only and causes the controller to operate on only one head (specified by the Address register) when:

1. It is on (up position), lights indicator in SEEK ADRS switch.
2. File mode selected.
3. The head number entered in Address register.
4. The SEEK ADRS switch pressed.

CONTROL A AND CONTROL B SWITCH/INDICATOR

CONTROL A and CONTROL B are two sets of switches and indicators which provide individual control for each data channel physically connected to the controller. Each set consists of nine position rotary switch which permits varying the equipment (controller) designation from 0-7 or STANDBY, and a CONNECTED, RESERVED, and PARITY ERROR indicator which light when the associated condition exists in the controller.

SELECT SWITCH/INDICATOR

Selects and reserves the unit specified by the unit register. The unit number should be entered before turning on the select switch to avoid reserving unnecessary units. This applies to dual controller systems.

TRACK SWITCH/INDICATOR

Selects Track mode wherein the remainder of the track designated by the content of the Address register is operated upon, starting at the address held in the Address register. Operation ceases at the end of the selected track.

CYLINDER SWITCH/INDICATOR

Selects Cylinder mode wherein the remainder of the cylinder designated by the content of the Address register is operated upon, starting at the address held in the Address register. Operation ceases at the end of the selected cylinder.

FILE SWITCH/INDICATOR

Selects File mode wherein the remainder of the file designated by the content of the Address register is operated on starting at the address held in the Address register. When using this switch the REPEAT switch should be off since a file will not be repeated automatically.

REPEAT SWITCH/INDICATOR

This switch causes the selected mode of operation (Track Cylinder or file) to be continuously repeated. This switch should not be used by the programmer operator. It is meant for maintenance purposes only. When this switch is used, the controller does not stop for any abnormal conditions unless it is unable to continue. When in File mode, this switch should be off. A File will not be repeated.

SEEK ADDRESS SWITCH/INDICATOR

This switch initiates a Seek operation on the selected unit to the address indicated by the content of the Address register. On completion of the Seek, the selected I/O operation commences. The indicator is lighted only when the REPEAT SEEK or the HEAD LIMIT switch is on, or if the MODE switch on the switch panel (Figure 3-2) is not in the NORMAL position.

MASTER CLEAR SWITCH/INDICATOR

This switch causes a MC in the controller. If a MC is performed while a Write operation is in progress, operation ceases immediately. That sector now contains information which will generate a checkword error if a Read operation is attempted.

REGISTER INDICATOR/SWITCHES

Thirteen indicator type pushbutton switches (CLEAR and bits 0-11) provide for displaying and/or entering information to and from the register indicated by the setting of the REGISTER SELECT switch when the key switch is on.

The CLEAR switch clears only the selected register.

SWITCH PANEL SWITCHES

The switch panel (Figure 3-2) is an extension of the maintenance panel and is used in conjunction with it.

MODE SWITCH

This switch is used for maintenance purposes. When in any position other than NORMAL, the SEEK ADRS indicator on the maintenance panel will light. The positions are as follows:

- NORMAL - Inactive position.
- REPETITIVE SEEK - Causes the disk unit to seek alternately between cylinder zero and the selected cylinder when track or cylinder is selected and the SEEK ADRS switch is pressed.
- REPETITIVE OPERATION - Causes the disk unit to seek alternately between cylinder zero and the selected cylinder, and perform an operation when the track or cylinder mode is selected and the SEEK ADRS switch is pressed.

MARGIN SELECT SWITCH

When pressed, this push switch transmits to the file positioner the values selected on the OFFSET and STROBE switches.

OFFSET AND STROBE SWITCHES

These toggle switches are used to simulate the Margin Selection function offset and strobe values. The switches are set to the desired value and the MARGIN SELECT switch is pushed to pass the information to the file.

FAULT CLEAR SWITCH

This toggle switch, when up, clears fault status conditions in the file when the MARGIN SELECT switch is pressed.

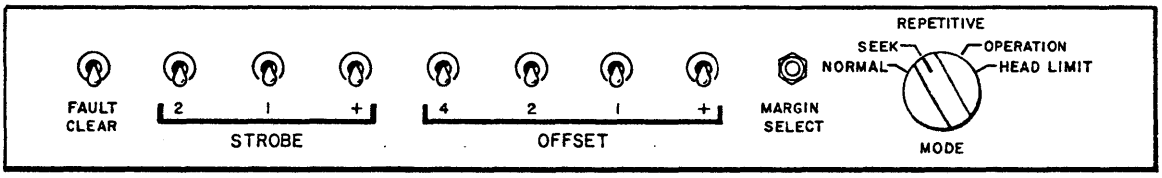

Figure 3-2. Switch Panel

OPERATION AND PROGRAMMING 4

OPERATION

Operation of the disk storage subsystem is under program control from the computer through the use of the Connect and function codes. Initial manual starting procedures include turning the power on, selecting the various switch settings, and loading a disk pack into the associated unit. Disk packs and files must have headers recorded before they can be used for programmed operations.

INITIAL START-UP

The following procedure turns on the power for the subsystem.

MULTIPLE DISK DRIVE

Turn on the main power switch and terminator power switch in the controller (located on top of the power distribution box in the back of the cabinet).

The disk drive units automatically enter a Power On sequence. Each disk drive unit requires approximately 1 minute to come up to speed and land the R/W heads. In a multiple unit system, each succeeding disk drive motor is automatically sequenced.

The sequencing overlaps and a full complement of drive units should be up to speed in approximately 2 minutes. As soon as the disk drive units become operable (R/W heads landed) and the PHYSICAL UNIT NUMBER indicator lights, operation of the disk drives may begin; however, a 15 minute warm-up period is recommended when commencing from a cold start.

DISK FILE

Normally the disk file and associated hydraulic unit should have all switches in the proper position and only step 7 should be necessary to activate the units.

CAUTION

The blowers should remain on at all times to prevent dirt accumulation on the disk surfaces.

If the units must be started from a completely shut down position, the following steps should be performed:

1. Open front doors on the disk file and hydraulic unit and the right side door on the disk file.
2. Place all front panel circuit breakers of both units to the ON position.
3. Set both positioner switches to the NORMAL position.
4. Set all manual/automatic switches to the AUTOMATIC position.
5. Set FILE OPERATION switch to the AUTOMATIC position.
6. Set main circuit breaker (located below power distribution panel) to the ON position.
7. Press START and observe START indicator light. The following indicators light temporarily: LOW FILE TEMP, STACK RPM 0, STACK RPM 1, and dc voltages.

   The disk file requires approximately 3 minutes to come up to operating speed; the hydraulic unit requires approximately 15 minutes.

LOADING AND UNLOADING PROCEDURES

The storage medium of the disk file units cannot be changed. To load or change the storage medium in the disk storage drive the procedures listed should be followed:

1. If the unit is operating, turn power OFF by pressing the START switch located on the front of the disk drive unit. Wait until the spindle stops rotating and the SPIN light turns OFF.
2. Pull the appropriate drawer forward as far as possible.
3. Load or unload the pack.

   Loading:
   Place the pack on the spindle and turn the cover handle clockwise to a full stop position. The pack should now be tight on the spindle and the protective cover lifts off easily.

   Unloading:
   Engage the protective cover over the disk pack and rotate the cover three times in a counterclockwise direction. The pack releases from the spindle and can be lifted from the drive unit.
4. Close the disk drive unit drawer and press the START switch on the front of the drive unit. This causes the unit to perform on initial Seek operation which positions and loads the R/W heads and brings the unit to the Ready state.

READY STATE

The controller is always Ready when power is available; however, the subsystem readiness (indicated by the Ready status bit) depends upon the state of the selected storage unit.

The requirements and time necessary to bring the subsystem components to the Ready state are as follows:

DISK FILE

The disk file units are Ready only when all of the following are present:

1. Power is available to the disk and hydraulic units.
2. The hydraulic and air systems are operating.
3. Hydraulic temperature ($100^{o}F$) and pressure (1100 psi) are up to normal.
4. The disks are spinning and up to speed (1750 rpm).
5. The positioner is in the landing area and the R/W heads are landed and in an operating position.

MULTIPLE DISK DRIVE

The disk drive units are Ready only when all of the following are present:

1. A pack is loaded.
2. The drawer is closed.
3. The disks are spinning and up to speed (2400 rpm).
4. An initial Seek has been performed to position the R/W heads.

PROGRAMMING CONSIDERATIONS

CONNECT

Device type codes other than XX1X and XX2X are illegal.

SIMULTANEOUS CONNECT

If the two data channels attached to the same controller simultaneously attempt to connect to the controller, neither channel is given preference. The controller will connect to the data channel recognized first.

Initiation of the operation need not take place immediately after the connect is made; once the connect is made, the channel has the controller and subsystem reserved until specifically released by that channel.

MODE RESTRICTIONS

Operations which are inconsistent with the mode selected cause the computer to hang up (that is, initiation of an output, or write, when Read mode is selected). An output or input operation must always be preceded by a 1X or 4X function.

MASTER CLEAR AND RELEASE

CONTROLLER

A manual or program (channel) MC, Clear function, or Restore function cause the Address register to be cleared to zero. A Channel Release has no effect on the content of the Address register. The MC, Clear function, and Channel Release remove all interrupt selections except the interrupt on opposite channel release. An MC automatically selects End of Record mode.

DISK UNIT

Any MC to a unit which is busy with a Write operation causes the operation to cease immediately; however, the previously recorded data and checkword in the remainder of the sector are unaltered (and now useless). Therefore, a subsequent Read operation causes a checkword error to be generated from the inconsistent data recorded in the sector.

Any MC to a disk unit busy with a Read operation causes operation to cease immediately, but has no other affect on the present or subsequent operations.

INTERRUPTS

An Interrupt signal may be dropped by a MC or by any new function code, however, the Interrupt on Opposite Channel Release interrupt selection remains when a Release operation is performed.

NOTE

The Interrupt on Opposite Channel Release can be cleared by a MC or Clear function only when the opposite channel is Not Reserved (that is, the Channel B Release Interrupt selection can be cleared only if Channel B is not reserved).

Any interrupt selection may be removed by its associated Release interrupt code.

A data channel which has the subsystem reserved receives all interrupts selected. The channel not in control (reservation) of the subsystem can be interrupted only by a previously selected Interrupt on Opposite Channel Release. All other interrupts from the controller to the data channel not in control are inhibited even though the interrupt is selected.

ABNORMAL EOP INTERRUPT

The Abnormal End of Operation interrupt should always be used when performing any I/O operation (4X codes) other than the Load and Return Address functions. If the interrupt is not used and either an Address Error or Not Ready condition occur, the channel hangs up in a busy condition. With the interrupt selected, Interrupt Signal and Interrupt Lockout Override is sent back to the data channel to allow the program (via a Stop Channel Activity instruction) to recover from the hung condition.

SEEK/SECTOR VERIFICATION

When any I/O code (4X) operation is initiated an automatic Seek is performed to the address specified by the content of the controller Address register.

The new (automatic) header verification takes place at the sector following the one in which the last operation ended unless the new I/O is initiated in a different unit than the one last referenced*. In the latter case if the positioner is not in the proper cylinder, both a Seek and Header Verify sequence are automatically initiated.

OVERLAP SEEK

Overlap Seek capability is incorporated within the units and can be performed on any storage unit in the subsystem as follows:

1. Select unit, select Seek Interrupt, and initiate a Seek operation (by performing a Load Address function).
2. Repeat step 1 for other desired storage units.

*When any I/O is in progress (or ends), the controller automatically updates the address registers at the end of each sector except when an Address Error is detected or if the Abnormal EOP Interrupt is selected and an abnormal condition occurs.

3. On detection of an interrupt*, search the selected storage units for an On Sector status bit to determine which unit is ready for operation.
4. Initiate and perform I/O operation.
5. Continue from step 3 for other storage units.

The On Sector status is returned from a storage unit in which a Seek operation is completed (positioner ready) until a Read/Write (or MC) is performed on that unit. Therefore, if several overlapped seeks are initiated, but with no read/write operations, a Seek Interrupt is generated only on the first unit completed.

The controller will not generate another Seek Interrupt until an operation is performed that generates an EOP (Load Address, Read, Write, etc.).

NOTE

The Seek Interrupt is generated from a line common to all units such that an interrupt can be generated by a unit in which a Seek was initiated even though the controller is no longer connected to that particular storage device.

SEEK INTERRUPTS

The On Sector status is returned from a storage unit after a Seek operation has been completed. The On Sector status line remains active until a Read, Write, or new Seek is performed on that unit; or if a drive release, controller release, or channel clear is issued. If more than one unit is given a Seek, the unit which completes its seek first will generate a Seek Interrupt (this unit can be determined by selecting each unit and checking On Sector status). This interrupt can be cleared by issuing any function. However, even though another unit sends back an On Sector signal, another interrupt will not occur. Another Seek Interrupt can occur only if an operation is performed. The end of operation enables the next On Sector to set the Seek Interrupt, if it is selected.

It should be noted that any function sent to the controller will clear an interrupt, and that if the controller is in the condition of expecting a Seek Interrupt (that is, Seek Interrupt selected and one or more units with Seeks in progress), a function issued during this period could occur at the same time as an On Sector signal from a unit. If this occurred, the Seek Interrupt could be cleared before the computer had time to respond, and since the interrupt cannot

* An alternate method is to omit the interrupt and immediately (on completion of seek initiations) commence a continuous search of the On Sector status bits.

occur again until an operation is performed, the result is a lost interrupt. It should also be noted that if more than one unit has a Seek in progress, and the computer receives a Seek Interrupt from one unit and performs an operation on it, the possibility exists of a lost interrupt at the time the end of operation occurs. A possible solution is to deselect the Seek Interrupt before the operation is performed, and reselect after the operation is complete.

On a Seek operation the busy status remains up until the seek is completed, but the controller will accept a new connect or function as soon as the controller has sent the Seek pulse to the unit. If the end of operation interrupt is set, the interrupt is generated when the controller is ready to accept a new connect or function.

MEMORY OPERATION DURING SEARCH

The operation of the buffer memory during a search is identical to a write operation if the operation ends with a partial sector wordcount, the remainder of the memory is filled with zeros and the entire sector is then compared with the memory contents. It is, for example, not possible to compare only the first 10 words of a completely filled sector, since a miscompare is likely in the remainder of the sector. However, a partial sector search would be possible if the write operation which filled the sector ended with exactly the same wordcount as the search.

1X AND 4X FUNCTION CODES

When preparing the subsystem for operation via the issuance of the various function codes, the 1X (address) or 4X (I/O codes) must be issued last or they will be cleared out by the next function code issued. With the exception of the 0044 (Checkword Verify code) the 1X and 4X function codes are designated to be followed by a buffered operation. All inputs or outputs must be preceded by a 1X or 4X function code.

RECORDS

Records consist of full sectors only. If an output from the data channel consists of less than a full sector when operating in End of Record mode, the remainder of the sector is automatically filled with zeros and the record mark is written at the end of the sector. It is possible to count and locate record marks in the various storage units by performing a Checkword Verify in End of Record mode, and then performing a Return Address. The sector address returned is one greater than the address in which the record mark was detected. The difference between the starting and ending addresses is one greater than the number of sectors in the record.

UNSAFE CONDITIONS

The presence of an Unsafe condition indicates the selected storage unit has one or more of the following fault conditions which causes the controller to become Not Ready:

1. More than one R/W head selected.
2. Both the Read and Write Controls set.
3. Read or Write on and Not Ready set.
4. Read and erase drivers both on.
5. Write driver on and erase driver off.

SYSTEM ERRORS

The controller detects the following error conditions:

Transmission Parity Error

Write Lockout

Checkword Error

Address Error

Seek Error

Head Verification Error

Defective Track

With the exception of the Transmission Parity Error, the presence of errors may be detected by interrupts or a status response.

Unsafe conditions in the selected storage unit cause the subsystem to go to the Not Ready state. The Not Ready condition may be detected by the status response.

TRANSMISSION PARITY ERROR

The Transmission Parity circuits examine each byte transmitted to the controller from the data channel, generate a new parity bit for that byte, and compare the parity bit generated with the parity bit accompanying the byte. If the bits do not agree, the PARITY ERROR indicator lights. Transmission of the error indication to the data channel is dependent upon the code or data causing the error as follows:

TRANSMISSION PARITY ERROR ON CONNECT

If the error is detected on a Connect code, the controller will not connect, and if connected will disconnect (including its status lines). The transmission PARITY ERROR indicator lights, but no Reply, Reject, or Transmission Parity Error signals are sent to the data channel.

TRANSMISSION PARITY ERROR ON FUNCTION

If an error occurs on the function code, the Transmission Parity Error signal is sent to the data channel and the error indicator lights; however, the function code is ignored by the controller. (No Reply or Reject is sent.)

TRANSMISSION PARITY ERROR ON DATA TRANSFER

If an error is detected on a data byte received from the data channel, the Transmission Parity Error signal is sent and the error indicator lights. The controller returns a Reply and uses the data in the normal manner.

WRITE LOCKOUT

To prevent accidental destruction of data, each sector address is equipped with a Write Lockout bit. Setting the bit to a "1" prevents any computer operation from writing in that sector. Note, however, the smallest segment of storage area that can be locked out is a track.

Attempting to write in a sector or track that has the Write Lockout bit set generates an abnormal condition (Write Lockout Error). The Write operation is then performed in a normal manner except that no writing or erasing takes place (the Write amplifier is disabled by the lockout). If selected, the Abnormal End of Operation Interrupt is set and operation ends immediately.

Reading and searching from a sector/track that has the Write Lockout bit set is accomplished in a normal manner and is not considered an abnormal condition even though the Write Lockout status bit sets. No Abnormal End of Operation Interrupt is generated even though it is selected (see WRITE LOCKOUT switch under Switches and Indicators).

CHECKWORD ERROR

During Write operations, a cyclic encoder in the controller generates a 12-bit check character referred to as a checkword. This checkword is written at the end of each sector.

During a Read/Search operation a new checkword is generated from the data read, and compared against the checkword previously written. If the two do not agree an error has occurred in writing, reading, or transferring of data between the controller and selected storage unit and a Checkword Error is generated.

On detection of a Checkword Error the associated status bit sets, and if selected, an Abnormal End of Operation interrupt is generated. If the Abnormal End of Operation Interrupt is not selected, the Checkword Error status bit sets; however, operation continues in a normal manner.

ADDRESS ERROR

An address operation consists of two phases:

1. A Seek operation wherein, upon completion of an output operation following a Load Address function, the R/W heads are positioned to the addressed cylinder.
2. A Header Verification sequence wherein, upon initiation of an operation, an automatic seek operation takes place, and the address header is read and verified for the addressed sector.

An Address Error can occur in either the previously initiated Seek operation or during the Header Verification sequence. Therefore, since initiation of an operation (and Header Verification) may occur anytime and is semi-unrelated to any preceding Seek operation, an Address Error can occur at two distinct and mutually independent times (upon detection of a Seek Error, or on detection of a Header Verification Error).

SEEK ERROR

An Address Error occurs during a Seek operation if either of the following conditions are detected:

1. The controller Address register contains an illegal address. (The controller is being requested to operate beyond the address limitations of the selected storage unit, on all models, indicated by status 0215).
2. The Seek operation initiated by the preceding Load Address function and buffer is incomplete (as indicated by a Seek Error signal for the selected unit, on all models, indicated by status 0015).

HEADER VERIFICATION ERROR

An Address Error occurs during a Header Verification sequence if any of the following are detected:

1. The contents of the controller address register do not compare with the address being read from the selected storage unit. On all models it is indicated by status 0215.
2. A checkword error is detected in the address being read. On models containing error recovery logic, this is indicated by status 0255. On all other models, it is indicated by status 0215.
3. An address in which the defective sector bit is being read. On models containing error recovery logic, this is indicated by status 4205. On all other models, it is indicated by 4215.
4. An address in which the incorrect sync bit has been detected, causing the lockout bits to be detected. On models containing error recovery logic, this is indicated by status 4355. On all other models, it is indicated by status 4315.

On detection of an Address Error the associated status bit sets, and if selected the Abnormal End of Operation Interrupt is generated on initiation of an operation. If the Abnormal End of Operation Interrupt is not selected, the channel hangs up on initiation of the operation.

DEFECTIVE SECTOR

In order to prevent reading or writing in a sector which contains a defective (faulty) recording medium, a Defective Sector bit is normally written in each faulty sector. The sector is defective when this bit is a "0".

On detection of a defective sector, the associated status and Address Error bits set (except for models containing error recovery logic, in which no address error occurs), and if selected the Abnormal End of Operation Interrupt is generated upon initiation of an operation (see DEFECTIVE SECTOR switch under Switches and Indicators). In models containing error recovery logic, individual sectors may be labeled defective by software.

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