

CONTROL DATA® SYSTEM 17 REAL TIME CLOCK

GENERAL INFORMATION PROGRAMMING CONSIDERATIONS

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PREFACE

This document describes the CONTROL DATA $^{\circledR}$ 10336-1 Real Time Clock used with the 1784 Computer.

The following CONTROL DATA CORPORATION publications may be useful as references:

Publication	Pub. No.
AT229-A Real Time Clock Hardware Maintenance Manual	89638900
1784 Computer Reference Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
BT148-A TTL A/Q and DSA Expansion Enclosure Controller	89758600
I/O Specification Manual - System 17	89673100
SMM17 System Maintenance Monitor Manual	89673100
System 17 Installation Manual	88996000

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GENERAL INFORMATION

INTRODUCTION

The CONTROL DATA ® 10336-1 Real Time Clock (RTC) is mounted on a single N-PAK PW-Board which is inserted in one of the A/Q Channel slots of the 1784 Computer System or 1783-1 Expansion Enclosure. When the expansion enclosure is used the expansion enclosure controller must also be used. The RTC is used to generate interrupts after a selected time interval, or to measure elapsed time which is available to the computer program as input to the A-Register.

Typical applications of the RTC unit include:

- Control of the sample rate of a data acquisition system by producing repetitive time intervals.
- Accumulation of elapsed time, either for time correlation of data in a data acquisition system, or to determine the response times of external devices.
- Initiation of execution of specific programs at either a fixed or program selectable interval.

FUNCTIONAL DESCRIPTION

The RTC uses a 20 MHz inter al crystal oscillator to generate selectable clock frequencies. Any one of these basic clock rates can be selected for 1, 10, or 100 microseconds, 1, 10 or milliseconds, or 1 second by using a manually placed jumper plug. These rates represent frequencies of 1 MHz, 100, 10 and 1 kHz, 100, 10 and 1 Hz, respectively. The Clock can be started or stopped and restarted when required under program control.

ELECTRICAL DESCRIPTION

The RTC unit contains two major parts:

- 1) The general part with station address circuitry for interfacing the A/Q channel.
- 2) The device specific circuits are as follows:
 - A 16-bit Holding Register that is loaded from the computer's A-Bus data lines by an OUTPUT COMMAND.
 - A 16-bit Binary Counter that is incremented by one of seven time rates, manually selectable. The counter is enabled and disabled under program control (START/STOP CLOCK function).
 - A Comparator that determines coincidence with the contents of the counter and the value held in the Holding Register, and produces an output when they are equal.

 The Comparator output is enabled and disabled under program control.
 - A 16-bit Output Buffer Register that holds the last count for READ STATUS purpose.
 - An Interrupt logic which generates an INTERRUPT RESPONSE whenever the Register and Counter are equal. The Interrupt may be enabled and disabled under program control.
 - A Time Base Unit with a manual input selector which allows the choice between seven time rates. The unit may be enabled and disabled under program control.
 - A Control Unit which recognizes commands from the data and controllers and manages the overall operation of the device.

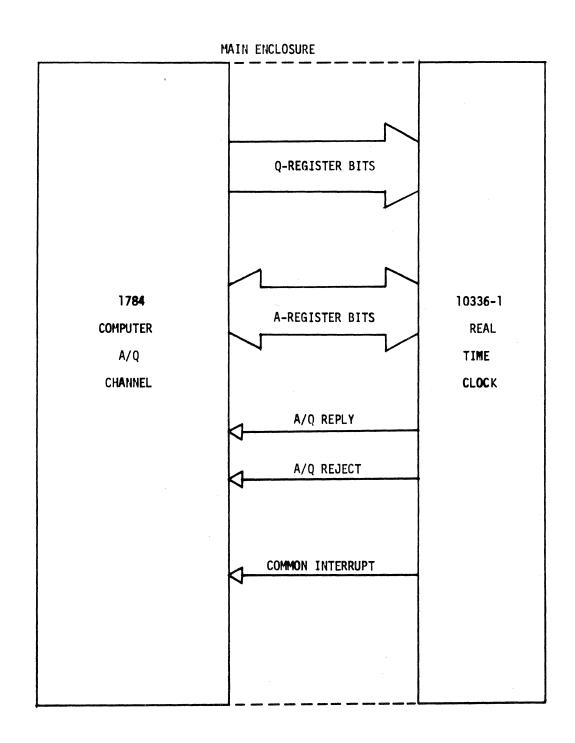


Figure 1. Real Time Clock System Configuration

PHYSICAL DESCRIPTION

The equipment logic circuitry is mounted on a single N-PAK PW-Board and occupies any one of the A/Q channel slots in the AB107/AB108 computer's chasses.

The Equipment Number and the Basic Clock Rate desired can be selected by placing the accompanying jumper plugs in the desired position on the PW as indicated in Table 1 and Figure 2.

OPERATING MODE

The RTC unit may be operated in the Interval Time mode (with Interrupts) or in the Elapsed Time mode (without Interrupts). When operated in the Interval Time mode, the program loads the Holding Register with a count value which corresponds to the desired time interval. This action automatically clears the Counter. The Counter advances at a rate controlled by the frequency of the selected clock rate until the Counter and Holding Register are equal. When equality is reached, the INTERRUPT RESPONSE (COMM INT) is generated. The Counter then resets to zero and without a START command, starts again automatically. Resetting and counting occurs even if the INTERRUPT is not acknowledged by the CPU. The Counter can accumulate a maximum of 65,535 counts, which corresponds to FFFF16 in the Holding Register.

The Elapsed Time mode is selected when the RTC controller is issued START CLOCK and DISABLE INTERRUPT commands. The 16-bit Counter is clocked at the jumper selected rate, reaches its maximum count of ${\rm FFFF}_{16}$, goes to zero and repeats, ad infinitum. The value in the Holding Register (zero or greater) has no effect.

TECHNICAL SPECIFICATIONS

Time Base Unit

Function:

An internal 20 MHz crystal oscillator is used for generating clock pulses.

Frequency Tolerance of the crystal $< \pm .005\%$ Stability over 0° - 70° temperature < .001%

Basic Time Periods:

1 µsec, 10 µsec, 100 µsec, 1 msec, 10 msec, 100 msec or 1 second. Any one of these seven basic cycles may be selected by a manually placed jumper plug.

Station Addresses

Any of the 15 addresses may be coded by manually positioned jumper plugs. See Tables 1 and 2, and Figure 2.

Interrupt

Interrupt Command may be connected to any of the 15 Interrupt lines available in the AB107/AB108 (See Table 3). The RTC INTERRUPT RESPONSE (COMM INT) is available at pin P1B08.

Power Requirements

The RTC uses less than 1.5 amperes of the 5 volts provided by the AB107/AB108 or BT148-A power supply.

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TABLE 1. INTERNAL SELECTIONS

то	SELECT	AT LOCATION	ACTION		
EQUIPMENT CODE -	Q-REGISTER	Between			
(Refer to Table 2 and Figure 2)	Q7 = "1" Q8 = "1" Q9 = "1" Q10 = "1" Q7 = "0" Q8 = "0" Q9 = "0" Q10 = "0"	U38 and U40	Install Jumper Plug """"""""""""""""""""""""""""""""""""		
BASIC CLOCK	<u> </u>	Between			
	l µsec 10 µsec .00 µsec 1 msec 10 msec .00 msec 1 sec	U6 - U7 U5 - U6 U4 - U5 U3 - U4 U2 - U3 U1 - U2 U1 - U2	Install Jumper Plug		

CAUTION

It is illegal to install more than one Basic Clock Rate
jumper plug on the RTC.

TABLE 2. EQUIPMENT CODE REPRESENTATION

HEXADECIMAL CODE	INSTALL JUMPER PLUGS BETWEEN U38 AND U40*					
OF E-FIELD (Q07-Q10)	Q10	Q09	Q08	Q07		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	. 1	0		
.3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
A	1 .	0	1	0		
В	1	0	1	1		
С	1	1	0	0		
D	1	1	0	1		
E	1	1	1	0		
F	1	. 1	1	1		
<u> </u>						

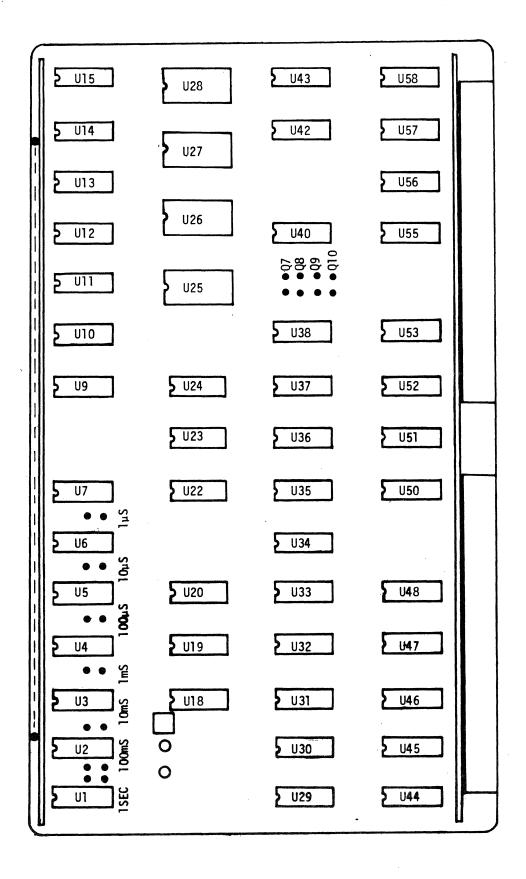
NOTE

A "1" in the binary code indicates the presence of a jumper plug for the setting of the equipment code and "0" indicates its absence.

^{*} See Figure 2.

TABLE 3. INTERRUPT PIN ASSIGNMENTS

RTC CONTROLLER									
INTERRUPT RESPONSE (COMM INT) P1B08									
Connection may be made to any of the following:									
BACK PLANE (Position)									
CPU Interrupt	Line	e 1				25	P1B10		
11 11	11	2				25	P1A07		
11 11	11	3				25	P1B07		
11 11	11	4				25	P1A05		
11 11	11	5				25	P1A06		
11 11	11	6				25	P1B06		
11 11	11	7				25	P1B05		
14 11	11	8				26	P1A10		
	11	9				26	P1B10		
11 11	11	10				26	P1A07		
11 11	11	11				26	P1B07		
11 11	11	12				26	P1A05		
11 11	11	13				26	P1A06		
11 11	11	14				26	P1B06		
11 11	11	15				26	P1B05		



PROGRAMMING CONSIDERATIONS

PROGRAMMING

Q-Register Figure 3 represents the Q-Register format.

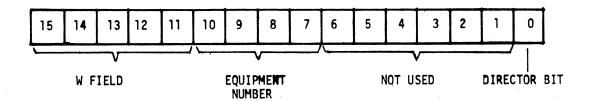


Figure 3. Q-Register Format

The W Field must be zero for all operations.

The E Field must contain the EQUIPMENT NUMBER.

The DIRECTOR bit defines the transfer operation.

Bits Q01 through Q06 are ignored by the RTC.

Three different operations may be performed:

- Load Register (WRITE DATA)
 Output to the RTC loads the Register with the contents of computer's A-Register and clears the Counter (WRITE signal with Q00=0).
- 2. Read Counter (READ STATUS)

 Input from the RTC copies the Counter contents into the A-Register of the computer (READ signal with Q00=1).

3. Director Function (WRITE).

The output to the RTC with control functions indicated by "1" in the computer's A-Register as shown in Figure 4 (WRITE signal with Q00=1).

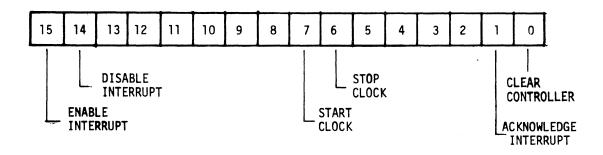


Figure 4. A-Register Format (Q00=1).

A-Register

Only one bit from each of the following groups may be set in any one function command:

Bits 6 or 7
Bits 14 or 15

When bits 6 and 7 or 14 and 15 are both set, an EXTERNAL REJECT is generated and the FUNCTION COMMAND is not executed. All other combinations in FUNCTION COMMAND are legal, where the PROGRAM CLEAR function is executed first, and then all other functions.

Bits A02 through A05 and A08 through A13 are ignored by the RTC.

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CLEAR CONTROLLER (and MASTER CLEAR)

Leaves the device in the following state:

- Register cleared.
- Counter and Output Buffer cleared.
- Clock stopped.
- INTERRUPT REQUEST disabled.
- INTERRUPT RESPONSE reset.

STOP CLOCK

When bit A06 is set, it stops the advance of the 16-bit Counter. The Counter maintains its value until reset by the START CLOCK function or CLEAR CONTROLLER function.

START CLOCK

When bit A07 is set, it clears the time base frequency counter, and the 16-bit Binary Counter, and enables incrementing the Binary Counter at the jumper plug selected frequency.

ACKNOWLEDGE INTERRUPT

This is generated when bit AO1 is set. It clears the INTERRUPT RESPONSE (COMM INT) signal generated by the RTC.

DISABLE INTERRUPT

When bit Al4 is set, it disables the INTERRUPT and clears the INTERRUPT RESPONSE (COMM INT) if it exists. If the device is in START CLOCK and DISABLE INTERRUPT state, the 16-bit Counter is continuously running.

ENABLE INTERRUPT

When bit Al5 is set, it enables the INTERRUPT RESPONSE.

EXTERNAL REJECT

Occurs if:

- FUNCTION COMMAND for INTERRUPT ACKNOWLEDGE is sent while the INTERRUPT RESPONSE (COMM INT) is not set.
- READ FUNCTION with Q00=0
- Bits 6-7 or 14-15 are both set in FUNCTION COMMAND.

NOTE

When an EXTERNAL REJECT occurs, no operation is executed.

INTERNAL REJECT

Occurs if:

- RTC unit is not addressed correctly (or is not present in the system).
- READ or WRITE function applied with W-Field different from zero.

TIME MODES <u>Interval Time Mode</u>

The Interval Time mode is initiated by a director function LOAD REGISTER command, and then by ENABLE INTERRUPT and START CLOCK commands. INTERRUPT RESPONSES are generated each time comparison is achieved. When an INTERRUPT RESPONSE is generated, the Binary Counter is cleared to zero and restarted automatically; a START CLOCK command is not required.

NOTE

- 1. If the Holding Register contains all zeros, this corresponds to $10000_{16} = 65536$ counts.
- 2. The Holding Register holds the value entered by the LOAD REGISTER command. The programmer is not required to reload it after INTERRUPT or ACKNOWLEDGE INTERRUPT responses.

 This register is cleared by CLEAR CONTROLLER or MASTER CLEAR.

Elapsed Time Mode

The Elapsed Time mode is initiated by director function DISABLE INTERRUPT and START CLOCK. The START CLOCK command clears the Time-Base counter and the 16-bit Binary Counter, and enables the incrementing of the Binary Counter. No comparison takes place, the Binary Counter is clocked at the jumper plug selected frequency, reaches FFFF₁₆, goes to zero and repeats ad infinitum. The Counter value is available at any time when requested by a READ CLOCK command, thereby providing the capability to measure Elapsed Time from

initiation (START CLOCK command is applied) until an event occurs.

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COMMENT SHEET

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