60182000

CONTROL DATA CORPORATION

CONTROL DATA®
1700 SYSTEM
MAINTENANCE MONITOR

Volume 3 of 3

REFERENCE MANUAL

RECORD of REVISIONS

REVISION	NOTES
01	Original Printing, preliminary edition.
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02	Publications Change Order 14307. Reprint with revision which obsoletes all previous editions.
(8-8-66)	Tests were updated and the following new tests were added: 1711/1712 Teletype, 1729 Card Reader,
	1731 Magnetic Tape, 1706/1716 Buffered Data Channel and Coupling, Random Protect, 1700 SMM
	Edit Routine, and Enter Program.
A	Manual released. Publication Change Order 16368. The following new tests are added: 0B (1718
(5-1-67)	Satellite Coupler Test), 0C (1742 Line Printer Test), and 3D (Enter Program). Other tests were
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Address comments concerning this manual to:

Control Data Corporation
Publications and Graphics Division
4201 North Lexington Avenue
St. Paul, Minnesota 55112

or use Comment Sheet in the back of this manual.

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PREFACE

MANUAL STRUCTURE

This manual is intended to serve as a reference aid for field and checkout personnel involved in the running of the CONTROL DATA® 1700 System Maintenance Monitor (SMM17). It consists of two sections:

SMM17 DESCRIPTION

A detailed description of the operation and use of the monitor, instructions for the operator, restrictions and necessary parameters. An asterisk (*) on the left of the page will highlight operator tasks. Supplements are included in the back of this section.

TESTS

Detailed test descriptions complete the three volume reference manual.

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1718 SATELLITE COUPLER TEST

(SC1A0B Test No. 0B)

I. OPERATING INSTRUCTIONS

A. RESTRICTIONS

1. Test SC1 on the 3000 side should be called first.
2. No other 1700 test may be run with this test. This test does not return control to the monitor.

B. LOADING PROCEDURE

This program is called as test number 0B via SMM17. The 3000 side is called as SC1 via the SMM3L or SMM3U. The 3000 side is the master and should be called first.

C. PARAMETERS

1. First stop

   A = Test ID word (0B21)
   Q = Test Stop/Jump parameter
   Selective stops and jumps

   Bit 0 - Parameter word (no typeout occurs)
   Bit 1 - End of section (no typeouts)
   Bit 2 - End of pass through test (typeout unless bit 8 is set)
   Bit 3 - Error stop (typeout unless bit 8 set)
   Bit 4 - Repeat conditions
   Bits 5, 6, 7 - Not used
   Bit 8 - No typeouts
   Bit 9 - Return address corresponds to memory location rather than program listing
   Bit 11 - Selects shift cable option (Set this bit when using a special data cable which is wired to shift the data cable bits left by 4 bits. When running with this option character mode is disabled.)

2. Second Stop

   A = Interrupt line
   If bit 0 of the Stop/Jump parameter word is set, a Stop occurs with bit 6 in the A register set. This bit specifies interrupt line 6. If

the 1718 uses a different interrupt line, the operator must clear the A register, set the bit corresponding to the correct interrupt line, and run.

Q = 6000 flag
Bit 15 = 1 (6000 system)
Bit 15 = 0 (3000 system)
Sections can be selected only on the master side, the 3000 Series Computer.

D. MESSAGES

1. Normal Messages

a. SC1A0B, 1718 SATELLITE COUPLER TEST 1A = XXXX, FC = XX.

Start of test. Initial address is XXXX, frequency count is XX.

b. PROTECT STATUS SET

The Protect switch on the 1718 is set according to the status.

c. 0B24 XXXX 00YY ZZZZ

End of test. 0B is the test number. 2 is the number of stops, if any, and the number of pairs of words typed. 4 (bit 2) is the type of stop (End of Test stop) which occurs if bit 2 of the Stop/Jump parameter word is set.

XXXX is the Stop/Jump parameter.

00YY - YY is the pass number.

ZZZZ is the return address. This is relative to the initial address (program listing) of the test unless bit 9 of the Stop/Jump parameter is set, in which case ZZZZ is the memory location.

2. Error Messages

a. Errors

All error typeouts are prefixed by 0BV8 XXXXX 0SYY ZZZZ. 0B is the test number.

V is the number of stops (if any), or the number of pairs of words to be typed.

8 (bit 3) is the type of stop (Error stop) which will occur if bit 3 of the Stop/Jump parameter word is set.

S is the section number.
YY is the error code.
ZZZZ is the return address.

If V = 2, there is no error typeout suffix.
If V = 3, there is a suffix depending on the error code.

b. Error Codes

01 - Insufficient core for test

02 - Equipment address in error. Start over.

03 - Interrupt line selection in error. Start over.

04 - Internal reject of status input

05 - Internal reject of select

06 - Internal reject of AQ channel input or internal reject of direct input to BDC channel

07 - Internal reject of AQ channel output or internal reject of direct output from BDC channel

08 - Not used

09 - Not used

0A - Unexpected status.

A = actual status, Q = expected status.

0B - Data error after read.

A = actual data, Q = expected data.

After a data error is found, no more data checking is performed for that input unless bit 4 (repeat conditions) of the Stop/Jump parameter is set.

0C - Alarm interrupt, division A channel parity error

A = Status upon interrupt
Q = Selected interrupts
Bit 2 of Q set - Data
Bit 3 of Q set - End of Operation
Bit 4 of Q set - Alarm

0D - Alarm interrupt, division A computer inactive

A and Q same as for error 0C

0E - Interrupt status bit not set when interrupt occurred

A and Q same as for error 0C

0F - Non-selected interrupt occurred

A and Q same as for error 0C

10 - Flag interrupt did not occur when expected

A = current status
Q = current 1718 mask, 1700 side

11 - Not used

12 - Non terminating buffer occurred

13 - End of Operation status set before other computer

Write status is clear during Direct Read

14 - Not used

15 - Unexpected number of words read

A = actual word count

Q = expected word count

16 - No End of Operation interrupt during Read

17 - No End of Operation interrupt during Write.

3. Error Stops

Error stops occur if bit 3 of the Stop/Jump parameter is set. Error typeouts occur unless bit 8 of the Stop/Jump parameter is set. At error stops, the contents of the A and Q registers are the same as the typeout.

II. DESCRIPTION

A. GENERAL

1. The test is divided into three sections, selectable on the 3000 (master) side. These are Flag/Status section, Write/Read section, Mask/Interrupt section.
2. Each operational check is performed first from the 3000 side to the 1700, then from the 1700 to the 3000 side.
3. Each operational check is repeated 64 times.

B. DESCRIPTION OF TEST SECTIONS

1. Preliminary

Because flags 6 and 7 are used for communication, these flags are checked by each side prior to entering Section 1.

2. Section 1- Flag/Status Test

a. Set all flags and check flags.

b. Set individual flags and check.

c. Set all but one flag and check.

d. Clear individual flags and check.

e. Clear all but one flag and check.

f. Clear flags, check other computer Write/Read "1's", check for flags clear.

g. Set flags, check other computer Read/Write "0's", check for all flags set.

3. Section 2, Write/Read Test

   a. Check other computer Write/Read.

   b. Check other computer Read/Write.

   c. Read and check data, Write.

   d. Repeat c for lengths of 4, 32, 256 words.

   e. Repeat c and d for each of seven patterns.

   f. Read random lengths of random pattern. Check data.

   g. Repeat f.

   In Sections 1 and 2, reads and writes are not in Interrupt mode except for some of the random length reads. The buffered reads of random length are executed in Interrupt mode. Buffered and Direct mode for reads and writes are selected at random. Character and Word mode for reads and writes are selected at random. Reads and writes in section 3 are in Interrupt mode. Alarm and End of Operation interrupts are selected for reads and writes in Interrupt mode. Also, Data interrupt is selected for reads and writes in Interrupt mode, but not in Buffered mode.

4. Section 3, Mask/Interrupt Test

   a. Clear all flags, set all masks, expect no interrupts

   b. Set all flags, set individual masks, expect interrupts

   c. Set individual flags, set corresponding masks, expect interrupts.

   d. Set all but one flag, each flag. Set mask for flag not set. Expect no interrupt.

   e. Set individual flags. Set masks except flag set. Expect no interrupts.

   f. Read in Interrupt mode.

   g. Write in Interrupt mode.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIRED - About 2500_{10} locations

B. TEMPORARY STORAGE - Current status of the 1718 is stored at memory location 11_{16}.

C. PATTERNS

1. 000 (all "0's")
2. FFF (all "1's")
3. 000 FFF (all "0's", all "1's" alternate)
4. 555 AAA ("0", "1"; "1", "0")
5. F11 88F 47C 3E2 (3-bit end-around left shift)
6. F19 8CF 67C 3E3 (3-bit end-around left shift)
7. F11 0EE 88F 770 (complement, complement-shift) 47C B83 3E2 C1D
8. Random (word N+1 = word n + addend, first word random 12-bit number, addend random 12-bit number, 12 bit end-around carry addition used)

D. TIMING - About 4 minutes for all three sections.

E. EQUIPMENT CONFIGURATION

1. 1704 Computer with 4K memory
2. 1705 Interrupt Data Channel
3. 1706 Buffer Data Channel (optional)
4. 1718 Satellite Coupler
5. 3000 Series Computer with one data channel, or 1 0A Computer with a 3681 Data Channel Converter.
6. A device for loading program.

f. Clear flags, check other computer Write/Read "1's", check for flags clear.

g. Set flags, check other computer Read/Write "0's", check for all flags set.

3. Section 2, Write/Read Test

   a. Check other computer Write/Read.

   b. Check other computer Read/Write.

   c. Read and check data, Write.

   d. Repeat c for lengths of 4, 32, 256 words.

   e. Repeat c and d for each of seven patterns.

   f. Read random lengths of random pattern. Check data.

   g. Repeat f.

   In Sections 1 and 2, reads and writes are not in Interrupt mode except for some of the random length reads. The buffered reads of random length are executed in Interrupt mode. Buffered and Direct mode for reads and writes are selected at random. Character and Word mode for reads and writes are selected at random. Reads and writes in section 3 are in Interrupt mode. Alarm and End of Operation interrupts are selected for reads and writes in Interrupt mode. Also, Data interrupt is selected for reads and writes in Interrupt mode, but not in Buffered mode.

4. Section 3, Mask/Interrupt Test

   a. Clear all flags, set all masks, expect no interrupts

   b. Set all flags, set individual masks, expect interrupts

   c. Set individual flags, set corresponding masks, expect interrupts.

   d. Set all but one flag, each flag. Set mask for flag not set. Expect no interrupt.

   e. Set individual flags. Set masks except flag set. Expect no interrupts.

   f. Read in Interrupt mode.

   g. Write in Interrupt mode.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIRED - About 2500_{10} locations

B. TEMPORARY STORAGE - Current status of the 1718 is stored at memory location 11_{16}.

C. PATTERNS

1. 000 (all "0's")
2. FFF (all "1's")
3. 000 FFF (all "0's", all "1's" alternate)
4. 555 AAA ("0", "1"; "1", "0")
5. F11 88F 47C 3E2 (3-bit end-around left shift)
6. F19 8CF 67C 3E3 (3-bit end-around left shift)
7. F11 0EE 88F 770 (complement, complement-shift) 47C B83 3E2 C1D
8. Random (word N+1 = word n + addend, first word random 12-bit number, addend random 12-bit number, 12 bit end-around carry addition used)

D. TIMING - About 4 minutes for all three sections.

E. EQUIPMENT CONFIGURATION

1. 1704 Computer with 4K memory
2. 1705 Interrupt Data Channel
3. 1706 Buffer Data Channel (optional)
4. 1718 Satellite Coupler
5. 3000 Series Computer with one data channel, or 1 0A Computer with a 3681 Data Channel Converter.
6. A device for loading program.

DSC 1700 DATA SET CONTROLLER

(DSCA11 Test No. 11)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Test must be run with 6X00/6675 Data Set Controller Test (6000 → RT3).
2. Operator must make section selections, and stop/jump options correspond to those of the 6X00 operator.
3. Test must be loaded first (it does not return control to SMM after an I/O operation).
4. This test MUST be started before the 6675 test is initiated.

B. LOADING PROCEDURE

1. Loads under SMM17
2. Test mnemonic DSC
3. Test number 11

C. PARAMETERS

Parameter selection follows standard 1700 SMM format. Bit 11 of the stop/jump parameter word must be set for Input/Output from A mode; if not set, test runs in Buffer mode. The test parameter stops for section selection in A (preset to 000F) and interrupt mask in Q (preset to 0000). To set the interrupt mask parameter, the bit in Q matching the interrupt line should be set to "1" (i.e. bit 5 for interrupt line 5). For a normal run, the Stop at End of Section parameter bit should not be set.

D. MESSAGES

1. Normal Messages

```
DSCA11, 1700 DATA SET CONTROLLER TEST
IA = XXXX, FC = XX
```

This message is typed at the beginning of the test. All other typeouts appear in standard SMM17 format.

2. Error Codes

01 Unidentified interrupt

02 Either an expected interrupt did not occur or an unexpected interrupt did occur

A = actual status
Q = expected status

03 Either an expected status is not present or an unexpected status is present

A = actual status
Q = expected status

04 Data compare error between data sent and data received. If more than 10_{16} errors occur or the errors occur in section 5, then

A = number of errors
Q = pattern number

05 Cyclic code from the remote controller does not compare with the cyclic code generated.

06 Internal reject on an I/O attempt. (Repeats attempt following error display)

07 Interrupt status bit is set following a Clear Interrupt function

08 W of the equipment code is not 0, 02, 07, or 0C.

09 Sync Word Not Acknowledged status bit is in error. Following a select transmit, the status bit should be set, if not, the program records the error and proceeds to attempt the output. If the status bit is not down, the output is attempted 20_{16} more times before the error is reported.

13 Insufficient memory for test

14 Status after an input operation does not compare with the expected status (see error code 3).

II. DESCRIPTION

This test is written to interface with 6X00/6675 DATA SET CONTROLLER TEST (SCT) (See Appendix).

During initialization of the test, the program halts for a parameter entry. The lower four bits of the A register hold the section selections (bit 0 for section 3, bit 1 for section 4, etc.). The bit corresponding to the interrupt line number should be set in the Q register (bit 2 for interrupt line 2, etc.). By setting the JUMP switch, each section will stop for a parameter change at the operators option.

A. SECTION 3 - TRANSFER INTERRUPTS

Upon entering this section, the Interrupt Word interrupt is selected and the program loops until the interrupt is received from the 6X00. Upon receiving the interrupt, the section sends the Interrupt Word to the 6X00 and waits for a second interrupt. This exchange is repeated forty-nine more times. Due to the simplicity of this section the Repeat Condition option is not present.

B. SECTION 4 - TRANSFER DATA

Upon entering this section, the test puts the controller in Receive mode and waits for the 6X00 test to send the first pattern. Upon receiving the pattern, the data is checked against a generated pattern and produces error code 4 if there is a data compare error. After checking the data, the section returns the data pattern or a one word transmission if the operator wishes to repeat the last pattern transfer and again sets the controller to receive mode. If the test receives a one word transmission from the 6X00, the last pattern is again transmitted to the 6X00. Beginning with pattern thirty-one, an extra word is added to the input to get the cyclic code. This code is checked against one generated by the test from the data pattern. If they do not compare, error 5 is given. Following the cyclic check the test continues with the data check and transmissions. After sending pattern 60, the 6X00 sends a "wasted" pattern and the section gains control to send random data patterns to the 6X00. The 6X00 returns the pattern and they are checked against the generated patterns. Following the check of pattern 74, a "wasted" pattern is sent to the 6X00 and the section is completed.

C. SECTION 5 - RETURN TRANSMISSION FOR 6X00

Upon entering the section, the controller is set to Receive mode and waits for a 6X00 transmission to the test. When the data is received it is checked against a generated pattern and the data that is received is returned to the 6X00. If a data error occurs, only the pattern number (See Appendix) and the number of errors will be reported.

D. SECTION 6 - (OPTIONAL) 6X00 DATA TURN AROUND

Upon entering this section, the test clears the teletype and a carriage return and two line feed character codes to notify the operator that the test is ready for input. The operator may type any message up to 320_{10} characters. Two consecutive periods ends the input if less than 320_{10} characters are to be transmitted. After two periods or when the count reaches 320_{10}, the data list is send to the 6X00 and returned by the 6X00 to be typed on the teletype.

NOTE

For best results, the first two characters of an input should be a carriage return and a line feed.

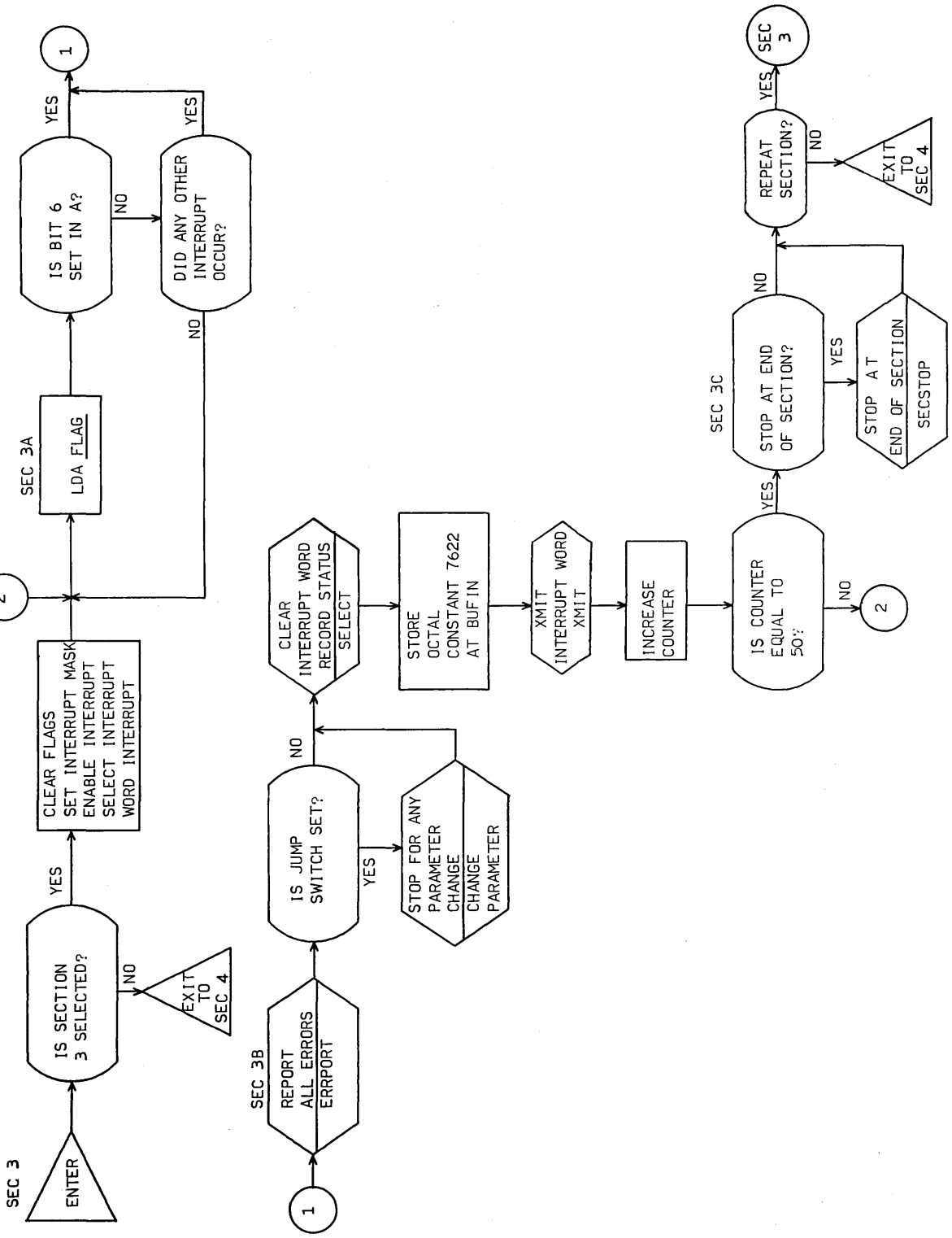
To type in more than one pattern, the Repeat Conditions option must be selected or Repeat Section option.

E. END TEST

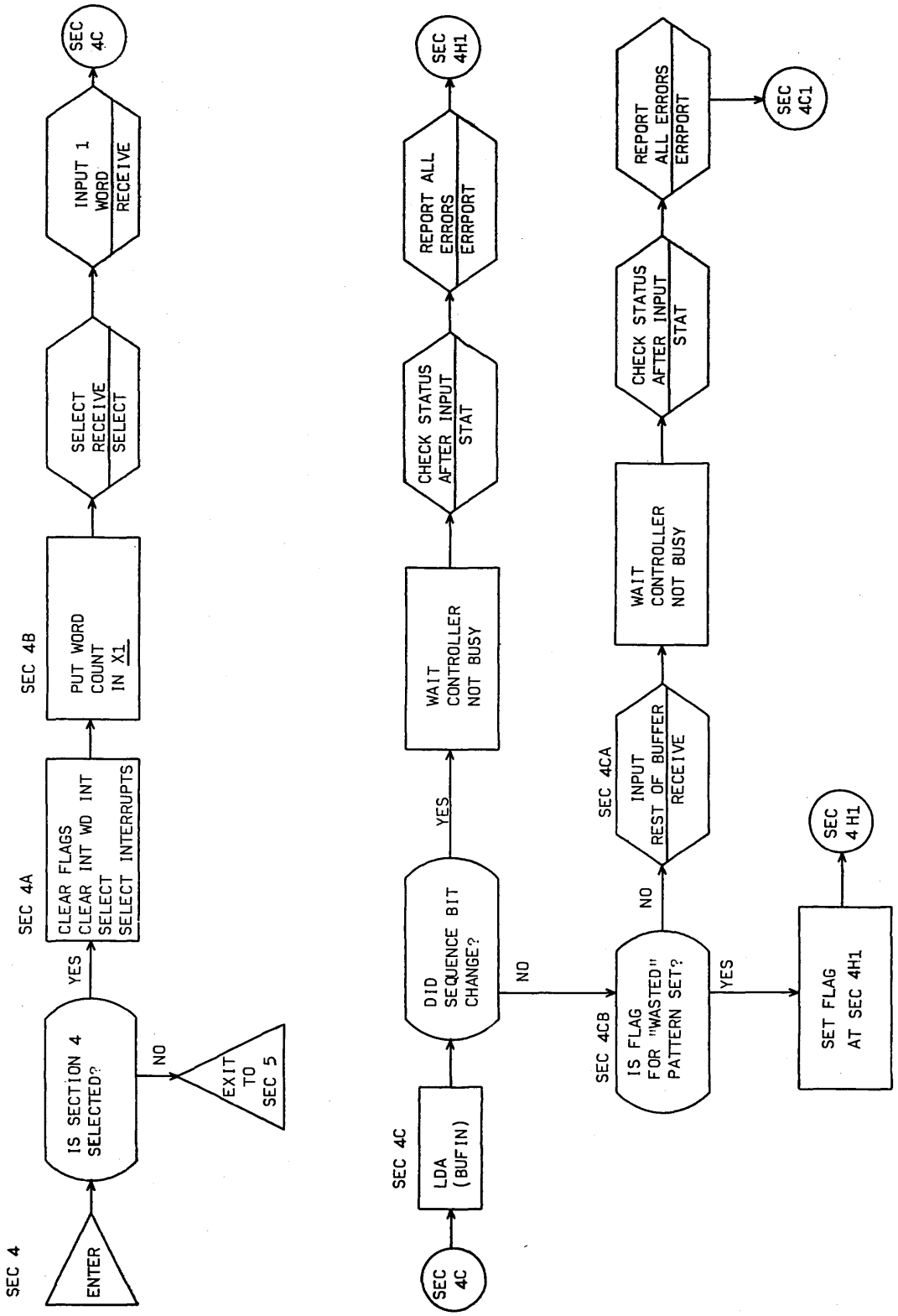
If the Stop At End Of Test option is selected, the test stops for a new parameter entry. A will hold the section selection and Q the interrupt line (this cannot be changed).

APPENDIX A

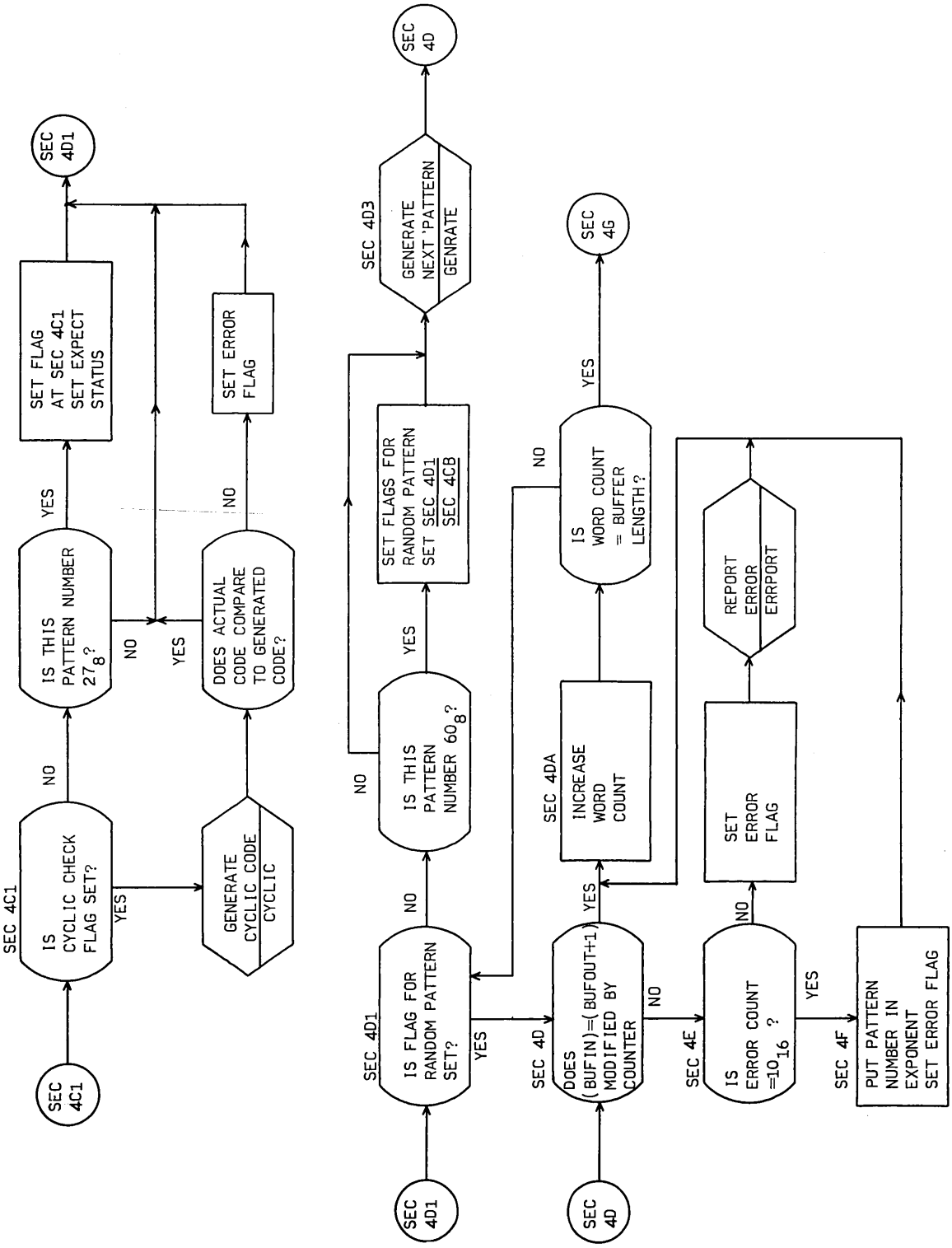
FLOW CHARTS



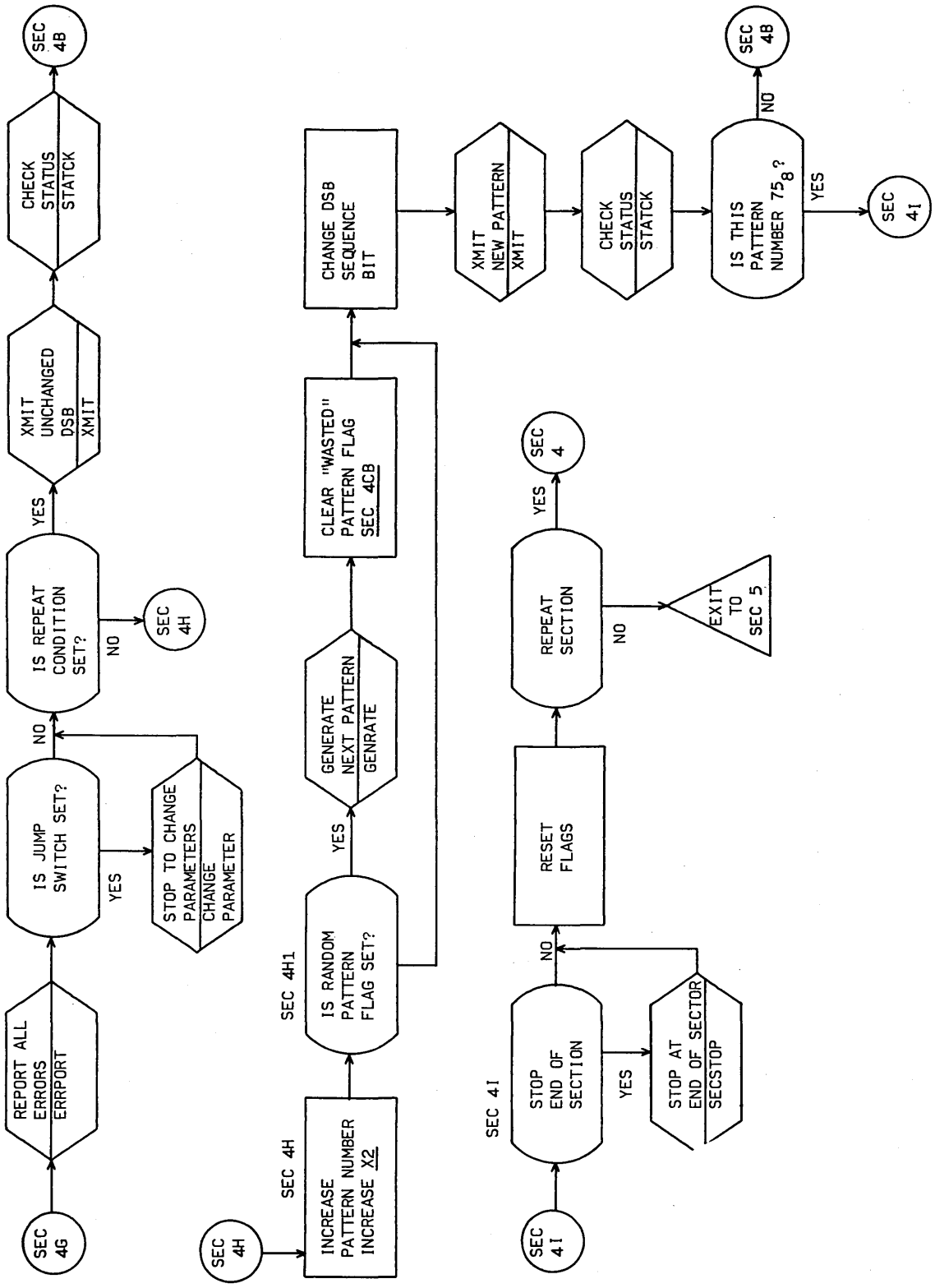
Section 3: Interrupt Transfer



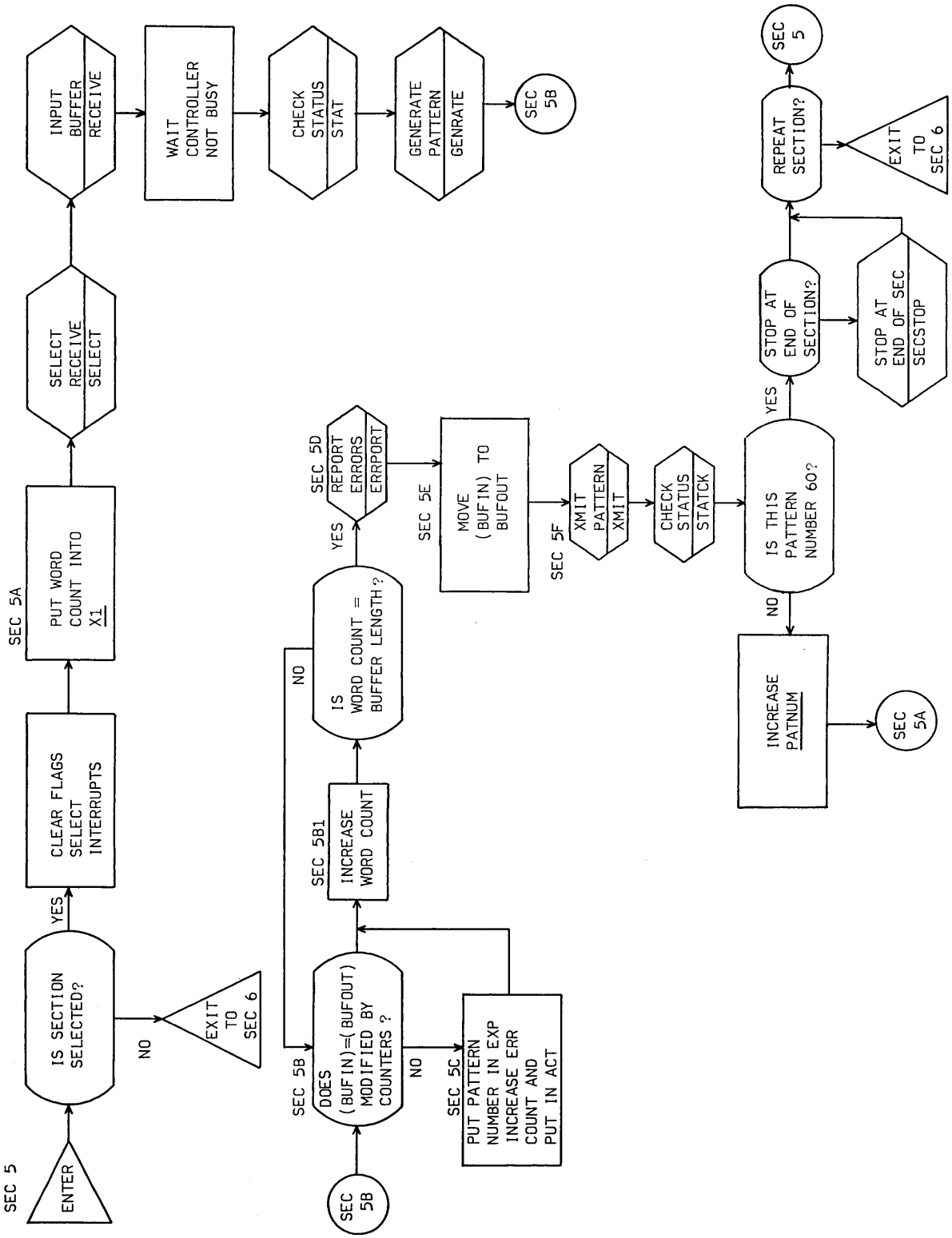
Section 4: Data Transfer



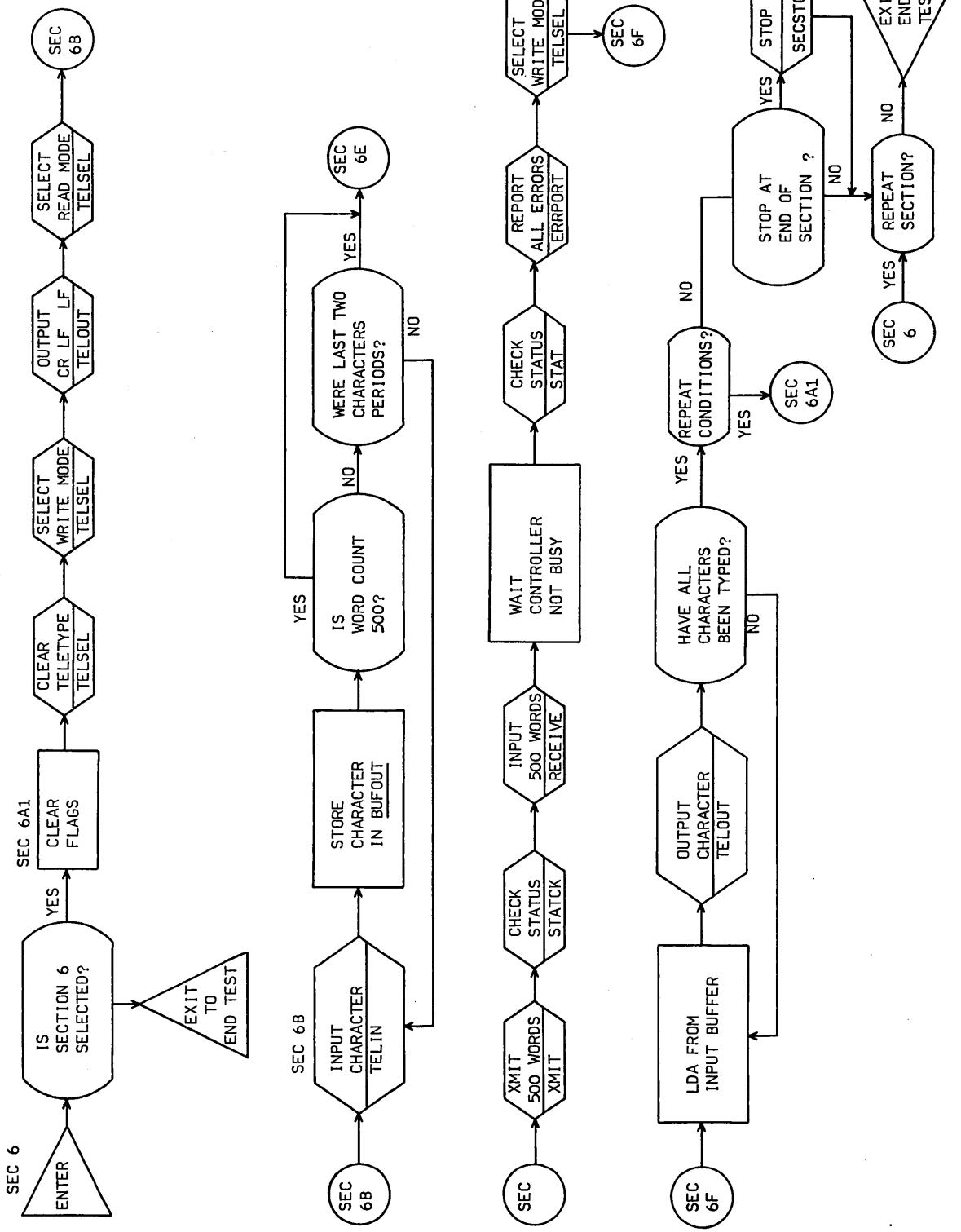
Section 4: Data Transfer (Cont'd)



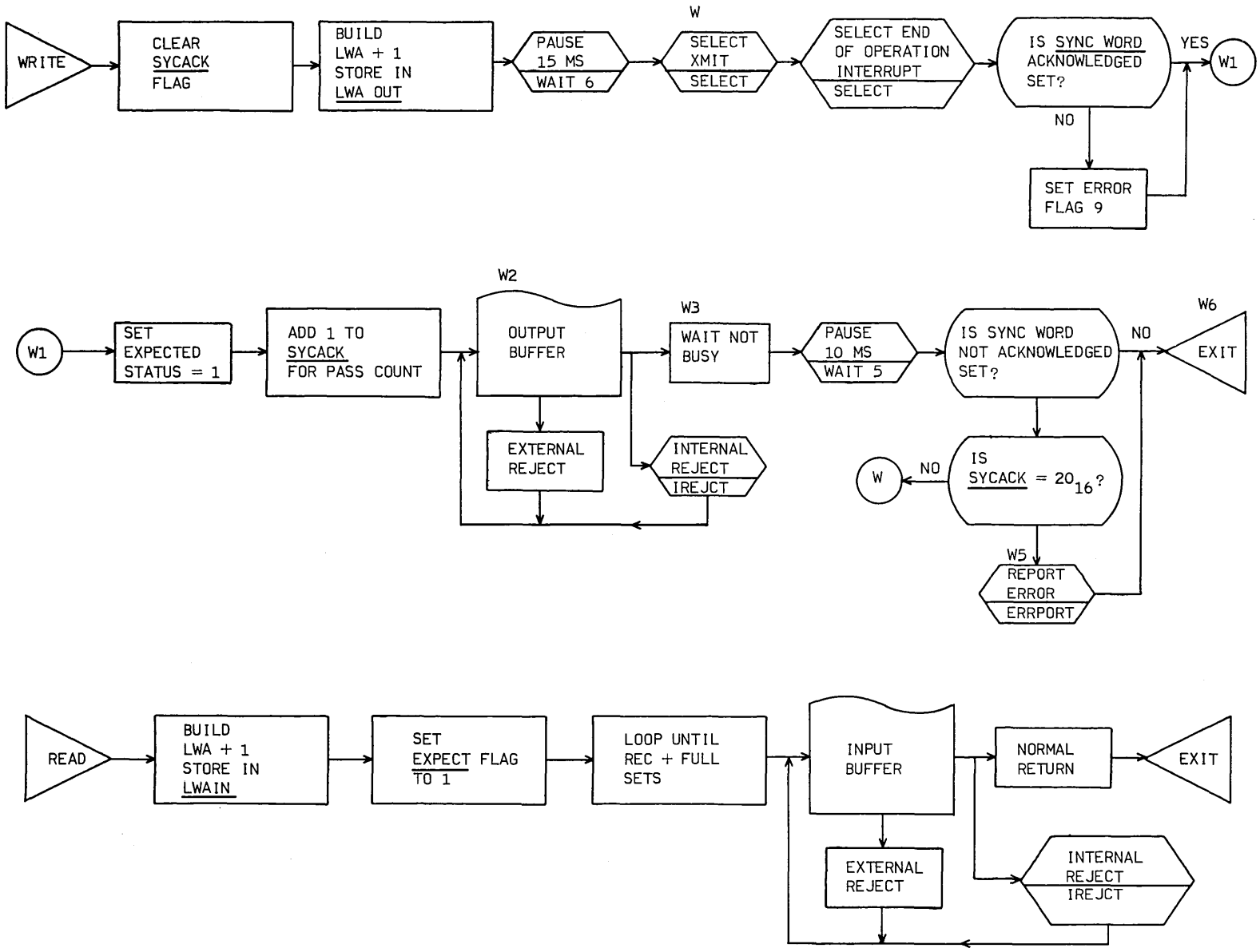
Section 4: Data Transfer (Cont'd)

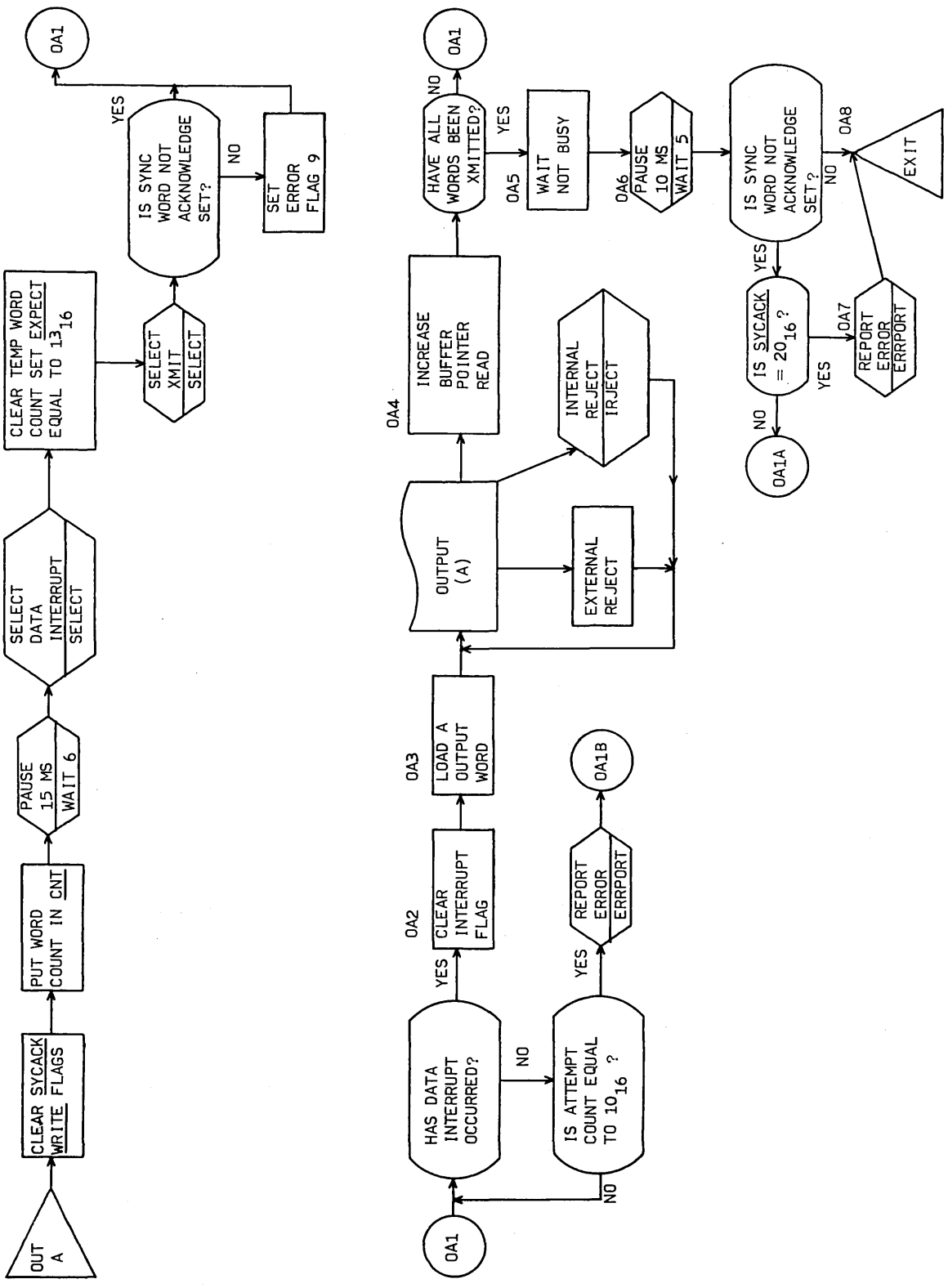


Section 5: Return Transmission

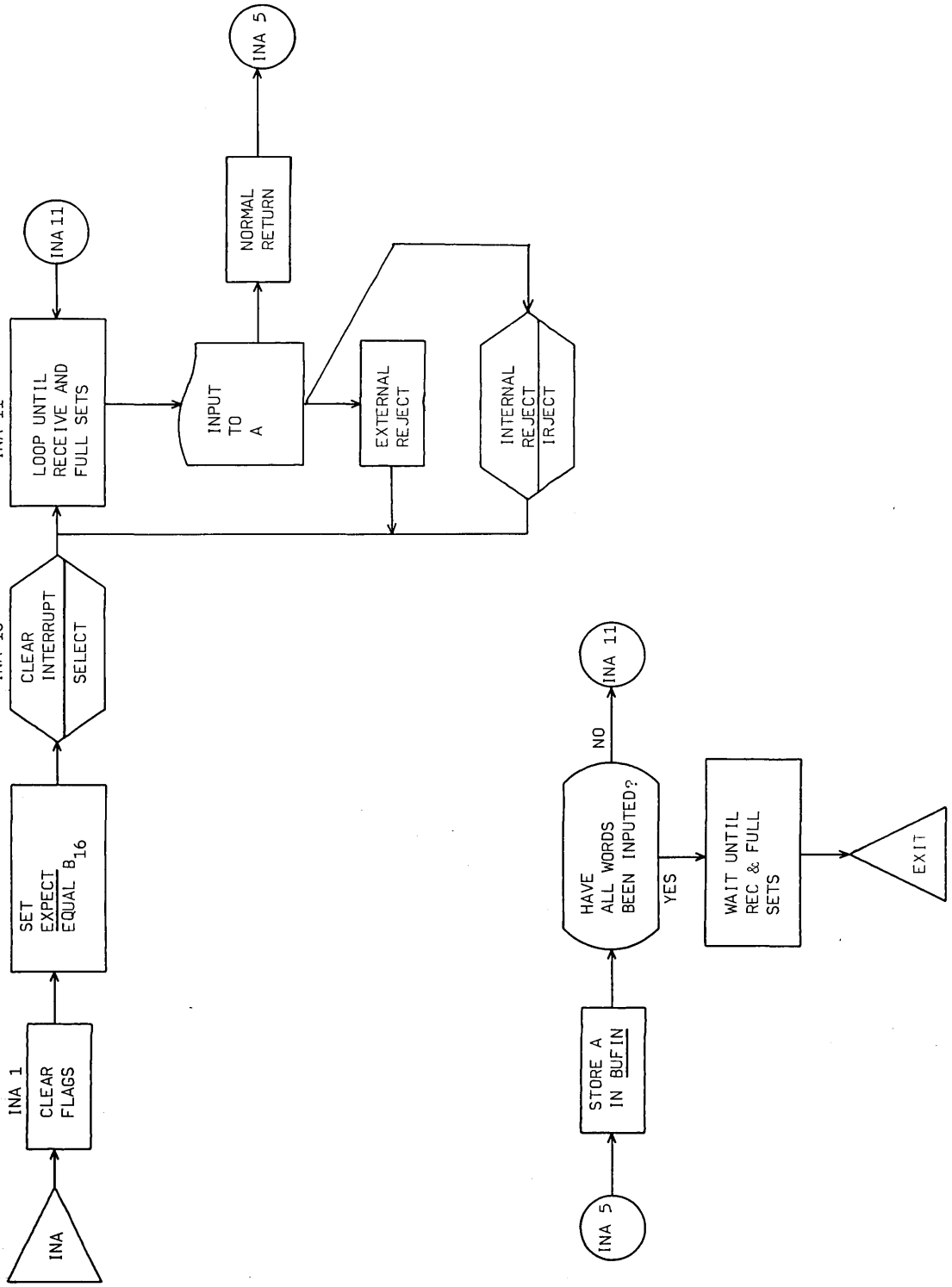


Section 6: Operator I/O


WRITE
CLEAR SYCACK FLAG
BUILD LWA + 1 STORE IN LWA OUT
PAUSE 15 MS
WAIT 6
W
SELECT XMIT
SELECT
SELECT END OF OPERATION INTERRUPT
SELECT
IS SYNC WORD ACKNOWLEDGED SET?
YES
W1
NO
SET ERROR FLAG 9
W1
SET EXPECTED STATUS = 1
ADD 1 TO SYCACK FOR PASS COUNT
W2
OUTPUT BUFFER
EXTERNAL REJECT
INTERNAL REJECT
IREJCT
W3
WAIT NOT BUSY
PAUSE 10 MS
WAIT 5
IS SYNC WORD NOT ACKNOWLEDGED SET?
NO
W6
EXIT
W
NO
IS SYCACK = 20 16 ?
W5
REPORT ERROR
ERRPORT
READ
BUILD LWA + 1 STORE IN LWAIN
SET EXPECT FLAG TO 1
LOOP UNTIL REC + FULL SETS
INPUT BUFFER
EXTERNAL REJECT
NORMAL RETURN
EXIT
INTERNAL REJECT
IREJCT



I/O From A Mode



I/O From A Mode (Cont'd)

APPENDIX B

SOFTWARE INTERFACING

between

A Remote Computer/Data Set Controller Test

and

The 6X00/6675 Data Set Controller Test (SCT)

SOFTWARE INTERFACING

between

A Remote Computer/Data Set Controller Test

and

The 6X00/6675 Data Set Controller Test (SCT)

A. Establishing Communication With Central (6X00)

1. The remote test will be started before the central test.

2. After the remote test receives its parameters from its operator and completes its initialization, it should inform its operator that it is waiting for the first interrupt from central.

3. The central test will then be started and will complete its initial status checks and optional segments before sending the first interrupt to the remote test.

4. After the remote test receives this first interrupt, it should return an interrupt and communication will then be established.

B. Interrupt Transfers (Section 3)

1. Forty-nine more interrupts will be exchanged, with the remote test being the last to send an interrupt.

2. If errors occur, they should be reported between the time the remote receives an interrupt and the time it returns the interrupt. The central test will be waiting for an interrupt while the remote test reports its error and communication between the two programs will not be lost. (The central test follows the same procedure for reporting its errors).

C. Data Transfers (Section 4)

1. After sending the last interrupt of section 3, the remote test should place its controller in the Receive mode and wait for pattern number 1 to be transmitted from central.

2. After checking pattern number 1 for errors, the remote test should generate pattern 1 and transmit it to the 6X00 and place its controller in Receive mode and wait for pattern number 2.

   a. Just as errors were reported in Section 3, errors in Section 4 should be reported between the time the remote test receives a transmission and the time it returns a transmission.

   b. An exception to C.2.a. is the case when status bits indicate equipment failure (transmission line, data set, etc.). These errors should be reported when they occur and a jump to the test's parameter entry halt should be executed.

3. The exchange of patterns will continue until pattern number 60_8 is sent by the remote to the 6X00. Up until this time the 6X00 sent the first transmission of each exchange. After this point the remote will send the first transmission of each exchange. This change of control will allow the remote computer to control the contents of the random patterns (pattern numbers $61_8 \rightarrow 74_8$).

   a. After the remote sends pattern number 60_8 to the 6X00, the 6X00 will send a "wasted" transmission back to the remote to indicate that the remote now has control and should generate and send pattern number 61_8 to the 6X00.

   b. The remote program will have control until the 6X00 transmits pattern number 74_8. At this point the remote program should transmit a "wasted" transmission to the 6X00 to return control to the 6X00 for section 5.

4. Patterns Exchanged

   a. The remote program should contain Table 1. Patterns sent to the 6X00 should be generated from this table. (The 6X00 has the same table and generates its patterns from its own table).

   b. Each three-word entry in the table is used to generate a pattern in the Data Transfer Format (see Figure 2). The Word Count as found in the table entry is the length of the entire transmission (including the sequence word). The Base Word as found in the table will always be the second word of the transmission.

   c. The rest of the pattern will be generated according to bits b, c, d, and e (see Table Entry, Figure 2).

(The pattern number is included in the Data Transfer Format for debugging purposes only. The remote test should not, upon receiving a transmission, use the pattern number received to generate data for comparison).

d. When the remote has control during the exchange of patterns 61_8 to 74_8, the remote determines what the base word will be. The 6X00 program will use the random algorithm to generate its comparison pattern.

5. Use of Sequence Bit

a. Every transmission in section 4 will contain a sequence bit as the first bit transmitted. This bit will allow either the 6X00 or the remote to have a pattern re-transmitted to itself.

b. The terminology used in following paragraphs regarding the sequence bit technique is the same as that found in the Import/Export Manual (Pub. No. 38707300). All transmissions from the 6X00 to a remote are called Status Transfers. The sequence bit in these transmissions is called the Status Sequence bit or SSB. All transmissions from a remote to the 6X00 are called the Directive Sequence bit or DSB.

RANDOM ALGORITHM

The 6X00 Test and the remote test will use the same random algorithm to generate the random patterns (61_8 - 74_8). The remote test will pack the base word, generate the pattern, and then transmit the base word and pattern in the Data Transfer Format (see Figure 2). The 6X00 will use the base word transmitted to generate its comparison pattern. The following algorithm is used by the 6X00 test and should be used in the remote test also:

1. Load previous word (or base word).
2. Add 7 (mode 2^{12} - 1).
3. Left Shift 1 End-Around (mod 2^{12} - 1).
4. Store.

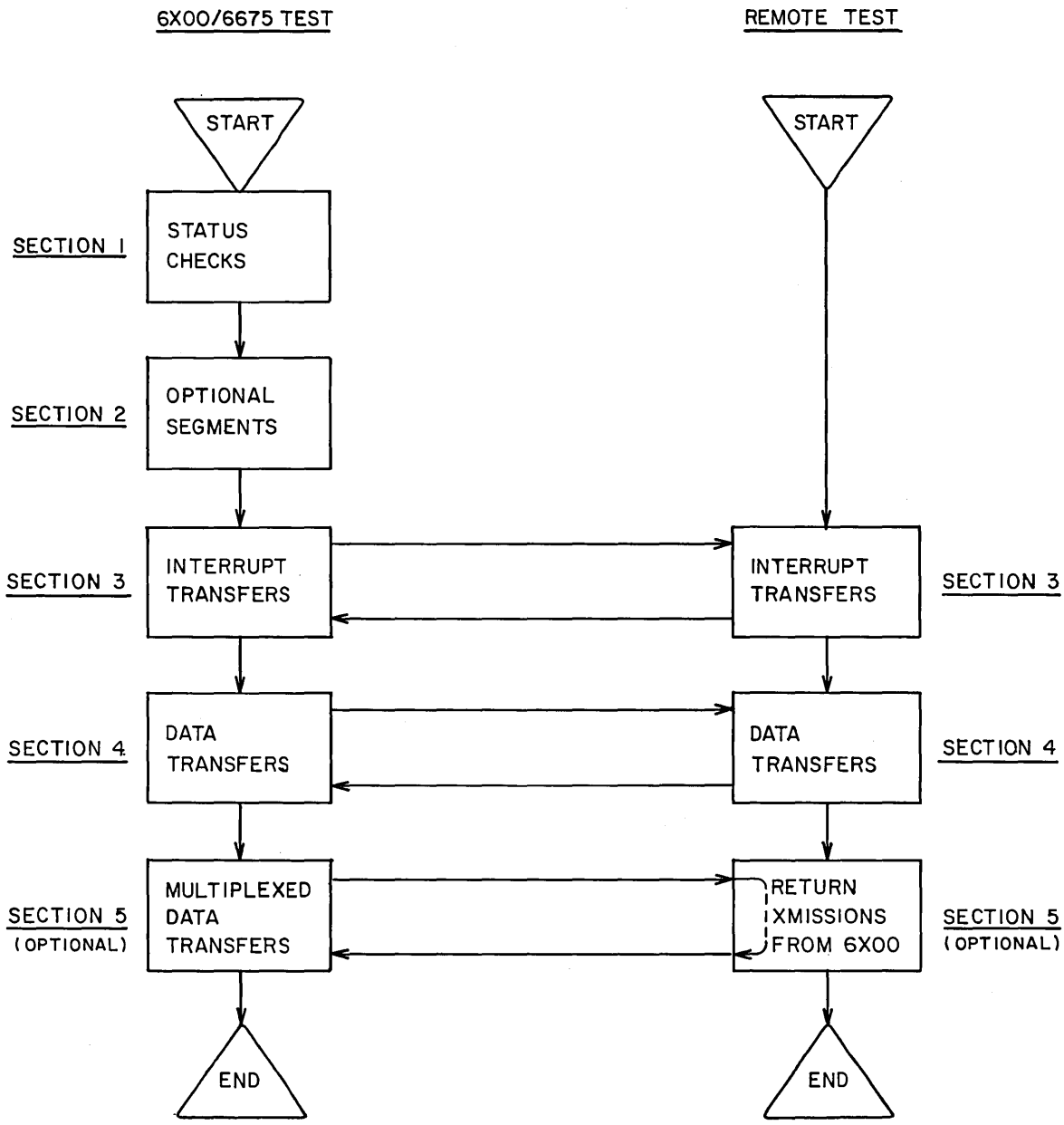
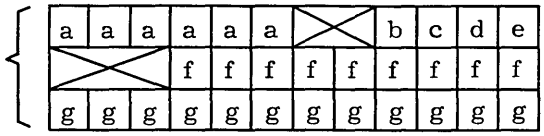


Figure 1. Remote Test

TABLE 1. PATTERNS SENT TO THE 6X00

COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5
0101	1501	3104	4502	6110
0002	0002	0010	0032	0004
0001	2525	2525	0001	XXXX
0201	1601	3204	4602	6210
0002	0004	0100	0100	0006
7776	2525	2525	7776	XXXX
0301	1701	3304	4702	6310
0004	0006	0500	0200	0010
0001	5252	2525	0001	XXXX
0401	2001	3404	5002	6410
0004	0010	0500	0400	0032
7776	5252	0001	7776	XXXX
0501	2101	3504	5102	6510
0006	0032	0500	0500	0100
7070	2525	1463	0001	XXXX
0601	2201	3604	5202	6610
0010	0100	0500	0500	0300
0001	5252	7070	7776	XXXX
0701	2301	3704	5302	6710
0010	0200	0500	0500	0500
7776	2525	7431	6314	XXXX
1001	2401	4004	5402	7010
0032	0300	0500	0500	0500
0001	5252	7700	7431	XXXX
1101	2501	4104	5502	7110
0032	0400	0500	0500	0500
7776	2525	0101	7700	XXXX
1201	2601	4204	5602	7210
0100	0500	0500	0500	0500
0001	5252	6060	7070	XXXX
1301	2701	4304	5702	7310
0100	0500	0500	0500	0500
7776	2525	5511	1234	XXXX
1401	3001	4404	6002	7410
0500	0500	0500	0500	0500
7776	5252	3232	4321	XXXX

TABLE ENTRY
(see Table 1)



a = 6-bit pattern number

b = bit is set if random algorithm is to be used (see Random Algorithm)

c = bit is set if each word is to be the complement of the previous word

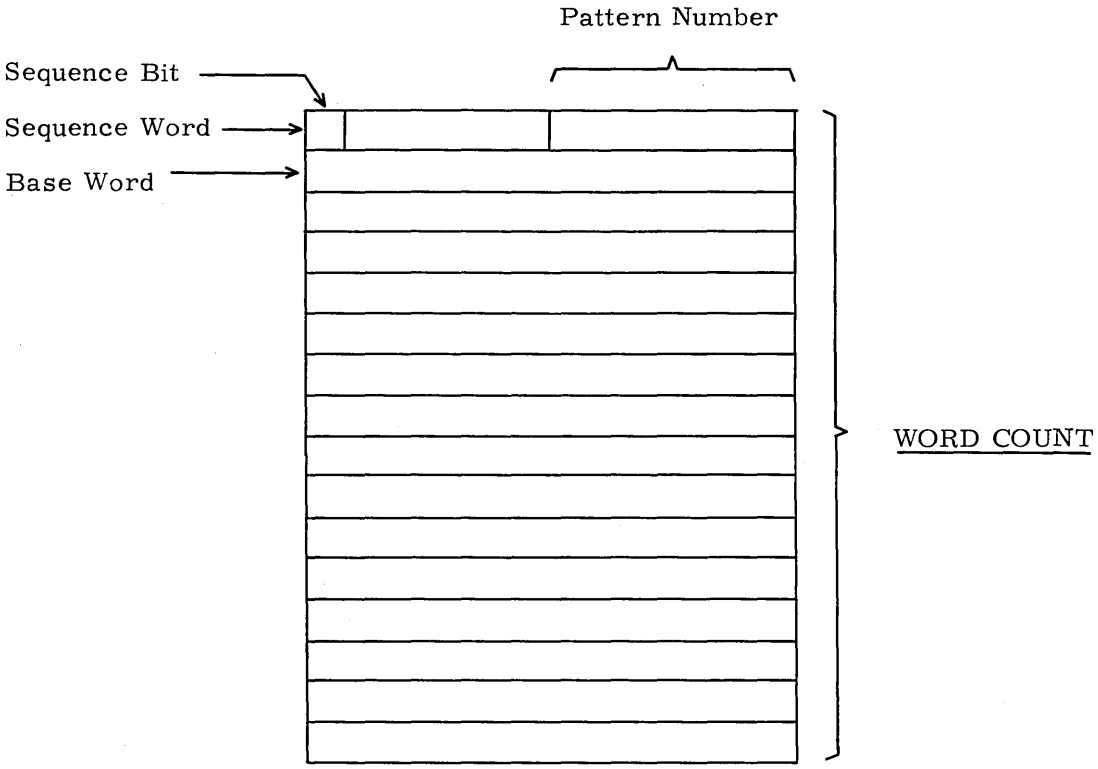
d = bit is set if each word is to be left-shifted one from previous word

e = bit is set if entire pattern is fixed (base word)

f = word count of entire transmission

g = base word

DATA TRANSFER FORMAT



c. The 6X00 only changes the state of the SSB. The remote computer only changes the state of the DSB.

d. The remote program will see the SSB change state on every transmission if the 6X00 does not want the remote to repeat a transmission. If, however, the SSB does not change its state (0 to 1 or 1 to 0), the remote should repeat its last transmission to the 6X00.

e. The remote should change the state of the DSB on every transmission to the 6X00 unless the remote program wants the 6X00 to repeat its last transmission.

f. The remote program should expect an SSB of zero on the first transmission it receives from the 6X00 and should therefore have a Ghost 1 bit in its status Sequence Bit Storage location.

g. The 6X00 will also expect a DSB of zero on the first transmission from the remote program (unless, of course, the remote program wants the first transmission from the 6X00 repeated).

h. Figure 3 is a flow chart which should help clarify the communication scheme between the 6X00 program and the remote program.

D. RETURN TRANSMISSIONS FROM 6X00 (SECTION 5)

1. This section should not normally run in the test but should be selectable in the parameter entry at the beginning of the test.

2. The remote program should go to Receive Mode and expect a transmission of pattern number 1 from the 6X00.

3. After the receive operation is complete, the remote program should delay for 100 milliseconds. This will allow the 6X00 program time to set up for a multiplexed receive operation.

4. When the delay runs out, the remote program should send the pattern as it was received from the 6X00, back to the 6X00 and go into Receive Mode for the next pattern.

5. This process will continue until all of the patterns (60_8) have been exchanged.

6. Equipment Failure errors and Sync Word Not Acknowledged errors should be reported as they occur.

7. If any data errors occur, the total number and the pattern number should be reported before returning the transmission to the 6X00.

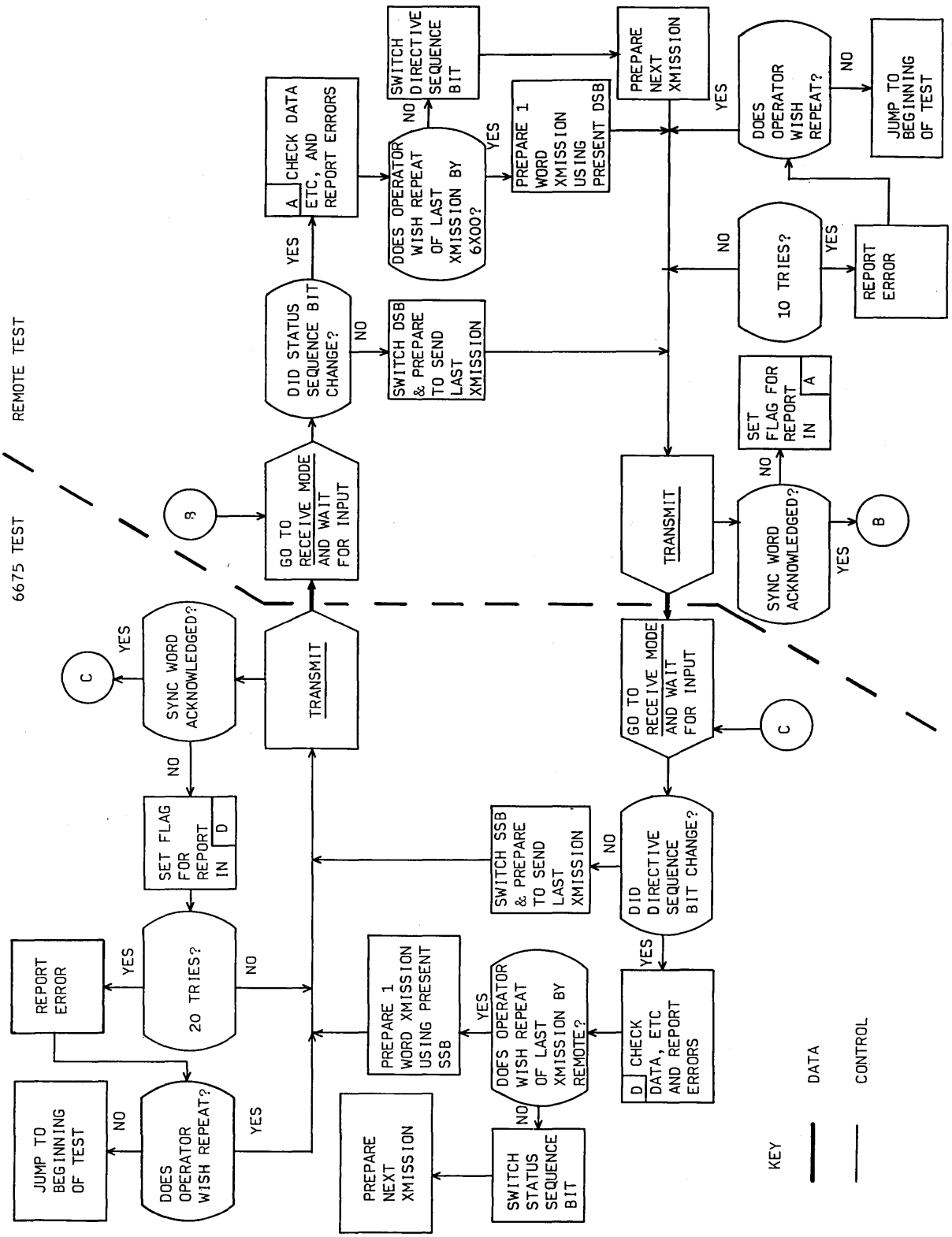


Figure 3: Communication Scheme Between the 6X00 Program and Remote Program

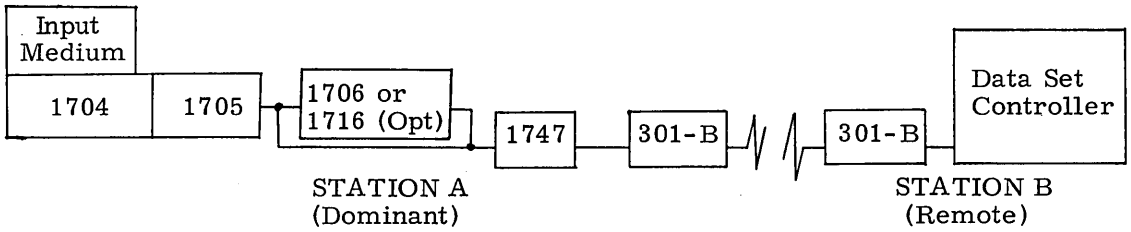
1747 DATA SET CONTROLLER TEST

(DS1020 Test No. 20)

I. GENERAL

This specification is for a 1747 DSC (Data Set Controller) unit diagnostic test that is designed to operate under Control Data's 1700 Maintenance Monitor System. Sufficient information, necessary to the specific operation and interpretation of the diagnostic, is contained within this specification and the SMM17 Reference Manual. The installation and operation of the diagnostic is in accordance with the standard procedures as defined in the SMM17 Reference Manual.

II. EQUIPMENT



Equipment necessary to the complete operation of the test:

A. One 1704 Computer

B. One 1705 Interrupt Data Channel

C. One 1712/13 Teletype*

D. The following input media:

1. 1731 Magnetic Tape Controller
2. 1712/13 Teletype*
3. 6673
4. 6674

*The teletype is not required if the test is executed with the prestored test selection parameter.

E. Two 1747 DSC's or one 1747 and one of the following DSC's:

1. 8529B
2. 3275C
3. 6673
4. 6674

F. An interconnecting wideband common-carrier facility with two 301-B Data Sets.

As optional equipment, the 1747 DSC may be interfaced with the 1706 or 1716 Data Channel. Capabilities are provided for exercising the 1706 or 1716 through the use of converter codes that are generated by the diagnostic.

III. SOFTWARE DEPENDENCIES

A. The 1747 diagnostic is designed to operate under Control Data's 1700 Maintenance Monitor System (SMM17).

B. Interface between the system and the diagnostic is through programs that are contained within SMM17.

C. All tables required by the diagnostic are contained internally within SMM17 and the 1747 diagnostic program.

IV. LIMITATIONS

A. As required by the SMM17 test specifications, core residence for the test does not exceed 2500 decimal locations.

B. Only one 1747 DSC is software tested per each execution of the diagnostic. The diagnostic makes no attempts to concurrently test more than one DSC at the dominant station, nor are any attempts made to diagnose troubles at the remote station. Faults at the remote station must be diagnosed by a diagnostic that is compatible with the remote station or by an attendant who is able to observe and/or scope the remote DSC while it is being exercised by the 1747 diagnostic.

C. Although only one computer system is required to run the test (the 1700 at Station A; see Par. II), coordination is required between Station A and Station B. While the diagnostic is executed, the operator at Station A and Station B. While the diagnostic is executed, the operator at Station A must coordinate with Station B the positioning of test switches at the remote DSC.

D. Message transmission and cyclic generation testing is limited to the use of one-word data buffers. This is a hardware restriction imposed by the remote DSC's capability of receiving and transmitting fixed-length records that consist of:

a sync word
one data word
a cyclic word
a space word

The dominant station is further limited because it cannot verify (self-check) its own transmissions by means of a hardware echoing technique. Reception at the dominant station is also limited because the remote DSC is capable of transmitting only nine distinct patterns:

One 4257_8 (Sync word)
four data patterns
four cyclic code words (generated from the four data patterns)

E. Test section 3 requires an extensive amount of manual intervention. If section 3 is selected, the 1747 DSC test should be run alone.

F. Before the diagnostic is executed, DSC switches should be positioned as follows:

Local DSC Switches	Position
1. POWER	ON
2. TRANSMIT TEST	OFF
3. RECEIVE TEST	OFF
4. PROTECT	UNPROTECTED

Remote DSC Switches	Position
1. POWER	ON
2. TRANSMIT TEST	Any position except the INTERRUPT word
3. RECEIVE TEST	Any position
4. PROTECT (if a 1747)	Any position
5. SYNC WORD LENGTH	12
6. INTERRUPT WORD (if an 8529-B)	7622

V. OPERATING INSTRUCTIONS

A. LOADING PROCEDURE

1. The test is loaded under the control of the 1700 System Maintenance Monitor (SMM17). Loading procedures are as explained in SMM17 for an external test under SMM17.

2. The calling sequence is as specified by SMM17 for an external test. The test number is 20.

B. PARAMETERS

1. If Bit 0 of the Stop/Jump word is not set, the test is run using prestored parameters. The prestored parameters assume the following:

   a. The 1747 is not connected to a 1706 or 1716. All I/O is through the AQ channel and test sections 3 through 8 are not executed.

   b. All 1747 interrupts are received on interrupt line number 2.

   c. The 1747 is designated as equipment number 2.

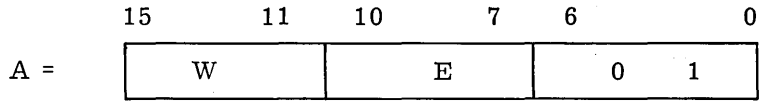
   Note: If the prestored parameters do not fit a particular site's configuration, they may be changed by following the procedures in the SMM17 Edit Routine.

2. If Bit 0 of the Stop/Jump word is set, the program makes three stops for test parameter display and/or entry.

   First Stop

   Displays the identification word in a (2031) and the Stop/Jump word in Q. The overflow indicator is lit for this stop.

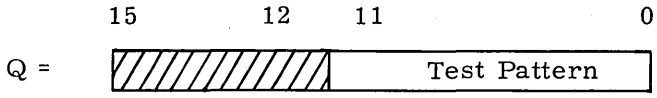
   Second Stop



   The W field (pre-stored value of 0) is used to identify a 1706 or 1716 data channel. This field is to be changed by the operator only if a 1706 or 1716 is interfaced with the 1747. Change W to equal:

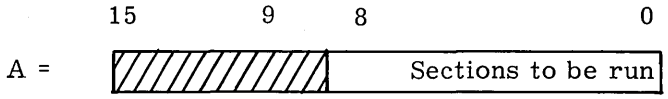
   00010 - for 1706/16 number 1
   00111 - for 1706/16 number 2
   01100 - for 1706/16 number 3

The E field (pre-stored value of 2) should contain a value that is equal to the equipment switch setting of the 1747 to be tested.

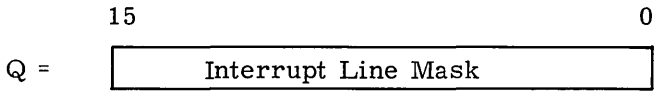


Bits 11 thru 0 (pre-stored to all 0's) may be used by the operator to enter a special test pattern. This pattern is used as transmission data by sections 4 and 8.

Third Stop



Bits 8 thru 0 (pre-stored value = 0007; i.e., only test sections 0, 1, and 2 are preselected) are the section select bits. A set bit in the nth bit position selects test section n; if all bits are set, all the test sections are selected.



A single bit set in this mask designates the interrupt line for the 1747. Only one bit is set in this word. Bit position n designates interrupt line n. The pre-stored value in this word designates interrupt line 2.

C. SELECTIVE SKIP AND STOP SETTINGS

1. The STOP switch must be set for running SMM17.
2. The SKIP switch, when set, causes the Stop/Jump word to be displayed in the Q register during the first stop in any series of stops.

D. CONSOLE PROTECT SWITCH SETTING

Set the console protect switch to UNPROTECTED.

E. MESSAGES

No typeouts occur if Bit 8 of the Stop/Jump parameter is set.

1. Typeouts or Alarms

a. Normal Program Display

1) Test identification typeout at start of test

DS1020, 1747 DSC TEST
IA = XXXX, FC = XX

(XXXX = Starting address of the test)
(XX = Frequency count)

2) Request typeouts for operator intervention.

See the description of test section 3 in this document for a list of typical request typeouts.

3) End of test typeout

A	Q	A	Q
2024	Stop/Jump Word	Pass Number	Return Address

b. Error Display

Errors are displayed according to the format prescribed by SMM17:

STOPS 1 and 2

A	Q	A	Q
Information Word	Stop/Jump Parameter	Section Number and Error Code	Return Address

ADDITIONAL STOPS

A	Q	A	Q

One or more additional stops are made to display information related to the specific error.

2. Error Codes

An error code is displayed in the lower two digits of the A register on the second stop of all error-display sequences. A description of the error codes used and the information displayed during the additional stops follows:

Error Code	Meaning
01	Incorrect test parameter was entered. The program will make another parameter stop when restarted.
02	External reject on input status attempt Current test section is aborted after display A = 0000 or 1706 status if reject was caused by 1706 Q = 1747 address code
03	Internal reject on input status attempt Current test section is aborted after display A = 0000 or 1706 status if reject was caused by 1706 Q = 1747 address code

Error Code (Cont'd)	Meaning
04	Unexpected external reject on output function attempt A = Rejected function code Q = 1747 address code A = 1747 status prior to output Q = 0000
05	Unexpected internal reject on output function attempt A = Rejected function code Q = 1747 address code A = 1747 status prior to output Q = 0000
06	1747 is in the test mode A = Status Q = 0000
07	1747 is not Ready Control is returned to SMM until DSC is made Ready A = Status Q = 0000
08	Unexpected alarm interrupt Current test section is aborted after display A = Status Q = Insignificant value
09	Data interrupt expected but not received Current test section is aborted after display A = Status Q = Insignificant
0A	EOP interrupt expected but not received Current test section is aborted after display A = Status Q = Insignificant value

Error Code (Cont'd)	Meaning
0B	Interrupt word interrupt expected but not received Current test section is aborted after display A = Status Q = Insignificant value
0C	External reject expected but not received A = Contents of A when output was attempted Q = 1747 address code A = 1747 status prior to output Q = 1747 status after functioning
0D	Internal reject expected but not received A = Contents of A when output was attempted Q = 1747 address code A = 1747 status prior to output Q = 1747 status after functioning
0E	Cyclic error forced but no status A = Status Q = Insignificant value
0F	A = Status Q = Insignificant value
10	Unexpected cyclic error A = Status Q = Insignificant value
11	Unexpected status A = Actual status Q = Expected status
12	Unexpected status after function select A = Actual status Q = Expected status A = Function code selected Q = 1747 status prior to function select

Error Code (Cont'd)	Meaning
13*	External reject on attempt to input 1706 status Current test section is aborted after display A = 0000 Q = Contents of Q when status input was attempted
14*	Internal reject on attempt to input 1706 status Current test section is aborted after display A = 0000 Q = Contents of Q when status input was attempted. 1706 status input is attempted only if a reject was received from a 1747 status input attempt and the W field of the address code indicates that the 1747 is connected to a 1706.
15	External reject on clear interrupt attempt while in the interrupt state. This error is fatal to this test and may affect the operation of other tests by destroying their return links to SMM. A = Rejected function code Q = 1747 address code A = 1747 status prior to output Q = 0000
16	Internal reject on clear interrupt attempt while in the interrupt state. This error is fatal to this test and may affect the operation of other tests by destroying their return links to SMM. A = Rejected function code Q = 1747 address code A = 1747 status prior to output Q = 0000
17	Interrupt occurred, but interrupt status bit not set A = Status Q = 0000

Error Code (Cont'd)	Meaning
18	Alarm interrupt expected, but not received. Current test section is aborted after display. A = Status Q = Insignificant value
19	Unexpected data interrupt Current test section is aborted after display A = Status Q = Insignificant value
1A	Unexpected end of operation interrupt. Current test section is aborted after display. A = Status Q = Insignificant value
1B	Unexpected interrupt word interrupt. Current test section is aborted after display. A = Status Q = Insignificant value
1C	Unexpected external reject on data output attempt. A = Status Q = Rejected data word
1D	Unexpected internal reject on data output attempt. A = Status Q = Rejected data word
1E	Unidentified interrupt. An interrupt occurred, but status does not indicate the type. Current test section is aborted after display. A = Status Q = Insignificant value
1F	Data pattern from remote DSC incorrect A = Data word received Q = 0000

Error Code (Cont'd)	Meaning
20	Unexpected external reject on data input A = Status Q = Insignificant value
21	Unexpected internal reject on data input A = Status Q = Insignificant value
22**	Manual interrupt received but will not clear
23**	Rejected on attempt to clear teletype interrupt
24**	Rejected on attempt to input teletype status
	** Error codes 22, 23, 24 are associated with processing a manual interrupt response. The manual interrupt response is used to signify operator's compliance to a typeout request for operator intervention. These codes are fatal to this test and may affect the operation of other tests by destroying their return links to SMM.
25	Internal reject expected on attempt to input status while 1747 is off but was not received. A = 1747 address code Q = Insignificant value
26	The 1747 test executive requires that the DSC status be exactly equal to 0001 before it calls in a test section for execution. After issuing a Clear Controller function, status is not 0001. The DSC is probably in the test mode or protected. Control is returned to SMM until the status becomes 0001. A = Status Q = 0000
27	Time delay ended because instructions for that section were not accomplished. A = Status Q = Insignificant value

Error Code (Cont'd)	Meaning
28	Internal reject expected on data input but was not received. A = Status Q = Insignificant value
29	Internal reject expected on data output but was not received. A = Status Q = Insignificant value
30	External reject expected on data input. A = Status Q = Insignificant value
31	External reject expected on data output. A = Status Q = Insignificant value
32	Cyclic word generated for the pattern being sent is incorrect. A = Cyclic word sent Q = Expected cyclic word
33	Space word sent is incorrect. A = Space word sent Q = Expected space word of 0000
34	Sync word sent is incorrect. A = Sync word sent Q = Expected sync word

F. COMPLIANCE TO TEST SWITCH POSITION SETTINGS

1. All test sections except 0, 1, and 2 require the test switches to be set at certain positions before execution. The messages are typed out at the beginning of each test section followed by the instruction MI WHEN READY. This allows the operator to make the necessary test switch settings. During the time of intervention, test control is returned to SMM. When the instructions are completed, the operator can return control back to the test by pressing MANUAL INTERRUPT.

2. There are two message typeouts in test section 3 which are exceptions to 1. These instructions have a time limitation in which the operator must comply. If compliance is not received within the allotted time, the test will type out an error message and then abort that subroutine. These messages are:

   FLIP 1747 TTS IN POSIT 1 OR LOCAL RTS TO REC*

   When this message is typed out, the operator has approximately 72 seconds in which to comply.

   DISCONNECT LOCAL DATA SET

   When this message is typed out, the operator has approximately 7 minutes in which to comply.

3. Name references in the messages have the following implications:

   1747 implies Local 1747 DSC
   CONSOLE implies 1704 computer console
   TTS implies Transmit Test switch
   RTS implies Receive Test switch
   REC implies Normal test switch receive position

4. The remote transmit light must be lit after selecting the Remote Transmit Test position except in the case where both the Transmit and Receive Test switches are selected at the remote DSC.

G. NORMAL TEST INDICATIONS

1. Test section 5 will cause the remote error indicator to light.
2. Test section 6 runs approximately 90 seconds with the local DSC error indicator light on.
3. Test section 7 causes the local DSC error indicator to light.
4. Test section 8 runs approximately 150 seconds with the local TX-REC indicators lit.

VI. DESCRIPTION

The test sections are structured in a pyramid fashion, with simple tests first. They are designed to attempt to isolate possible error conditions. They check all functions and combinations of functions for correct response, and all status bits for Set and Clear conditions. Data handling capabilities are also tested so as to simulate normal use of

*If Stop/Jump bit 4 is set and an error occurs, the condition requested must be removed (i.e. switch turned back to OFF) and then reset.

the 1747, as well as driving it at its maximum operating speed. Critical operations are timed and errors are reported if expected events do not occur within the allotted time. Once an error is isolated, the operator may cause the error condition to be repeated by setting bit 4 of the Stop/Jump word. The test is then in a Loop mode so that the loop may be used in troubleshooting. The loops are as short as possible to aid in scooping-out the problem. In no case does the test "hang" on reject or error conditions unless it is so directed by the control parameters. Descriptions of the test's initialization and the selectable test sections follow:

A. INITIALIZATION

1. Convert first word address of test, and frequency count to ASCII and store in typeout routine.
2. Type out the test title.
3. Set up return address.
4. Make parameter stop if Bit 1 of Stop/Jump word is set.
5. Set up restart address (IA) to test's section controller.
6. Check parameters for correct entries, i.e.;
   a. W field must be equal to 0, 2, 7, or C.
   b. At least one test section is selected.
   c. Only one interrupt line is selected.

   Display Error Code 1 if any of the above are not true.
7. Return control to SMM.

B. SECTION CONTROLLER

1. Check for Ready status and clear controller, display error if 1747 status is not 0001.
2. Execute Section n ($0 \leq n \leq 8$), if selected.
3. Stop at end of section if Bit 1 of Stop/Jump word is set.
4. Go to 1 (repeat section) if Bit 5 of Stop/Jump word is set.
5. Increment n.
6. Go to 1 if n is less than or equal to the last section number.
7. Increment pass counter.
8. Stop at end of test if Bit 2 of Stop/Jump word is set.
9. Go to 1 if Bit 6 of Stop/Jump is set (repeat test).

10. Stop for new parameters if Bits 10 and 6 of Stop/Jump word are set.

11. Return to SMM.

12. Go to 1 if SMM returns control (test frequency greater than 1).

C. Test Sections

Section 0 - Function Acceptance/Status Verification

This section issues legal function codes and combinations of legal function codes. The function selections are ordered so that no rejects, internal or external, are expected. Status is monitored to verify correct response for each function code or combination code that is issued. All rejects are reported by error code 04 or 05. Incorrect status responses are reported by error code 11 or 12. Any internal or external rejects that are encountered on attempts to input the 1747 status are reported by error code 02 or 03.

Section 1 - Internal Function Reject/Status Verification

This section is similar to Section 0, except that function codes are issued in a manner to cause internal rejects. Legal function codes are issued with Bit 0 of the address code equal to "0". Error code 28 or 29 is displayed whenever an expected internal reject is not received. This section is aborted if the test is functioning through a 1706 or 1716.

Section 2 - External Function Reject/Status Verification

Like sections 0 and 1, except that this section expects external rejects. Error code 0C is displayed if an expected external reject is not received.

Section 3 - Function/Status Verification with Manual Intervention

The objectives for this section are the same as for Sections 0, 1, and 2. However, this section requires manual intervention to supplement the testing of the 1) Protect system, 2) Alarm system, and 3) Interrupt Code Word detection system. The test types messages that request the operator to change switch settings. They are:

FLIP 1747 PROTECT SWITCH TO p (p = PROTECTED OR UNPROTECTED)
FLIP CONSOLE PROTECT SWITCH TO p (p = PROTECTED OR UNPROTECTED)
FLIP 1747 TTS (Transmit Test Switch) IN POSITION p (p = 1, 2, 3, 4, or OFF)
FLIP REMOTE TTS TO p (p = 1, 2, 3, 4, or OFF)
p CONNECT LOCAL DATA SET (p = blank or "DIS")
MI WHEN READY
FLIP CONSOLE PROTECT SWITCH TO PROTECT
FLIP 1747 PROTECT SWITCH TO PROTECT

FLIP CONSOLE PROTECT SWITCH TO UNPROTECTED
FLIP 1747 PROTECT SWITCH TO UNPROTECTED
FLIP 1747 TTS IN POSIT 1 OF LOCAL RTS TO REC
FLIP 1747 TTS TO OFF OR LOCAL RTS TO OFF
FLIP REMOTE TTS TO OFF - FLIP REMOTE RTS TO REC
DISCONNECT LOCAL DATA SET
CONNECT LOCAL DATA SET
FLIP REMOTE TTS TO 4 OR 3 OR 2 OR 1 - FLIP REMOTE RTS TO OFF
FLIP REMOTE TTS TO 4 - RTS TO OFF
FLIP REMOTE TTS TO 4 - RTS TO OFF

Section 4 - Transmit Test

This section tests the capabilities of the 1747 to transmit one-word data patterns. The patterns are generated and transmitted to the remote DSC under interrupt control; status is monitored for correct response, and paths are provided to process any internal or external rejects. All abnormal or unexpected conditions are reported by appropriate error codes.

Interrupts tested are:

a. Data

b. End of Operation

c. Alarm (selected and expected but not forced)

Functions selected:

a. Select Data Interrupt

b. Select End of Operation Interrupt

c. Select Alarm Interrupt

d. Select Transmit

Patterns transmitted:

a. All 0's

b. All 1's

c. Sliding 0, surrounded by all 1's

d. Sliding 1, surrounded by all 0's

e. Alternate 1's and 0's

f. Alternate 0's and 1's

g. 4257_8 (This pattern and its complement are also left-shifted end around and right-shifted end off to generate 12-bit data streams that closely resemble the DSC synchronization word.)

h. Operator's pattern (if supplied during parameter entry; i.e., does not equal 0000).

i. 7622 (Same as g. above).

A synchronizing word (4257_8) and a cyclic code word (both hardware generated by the 1747) are automatically transmitted to the remote DSC by the 1747. These words occupy positions 1 and 3 in the 1747-to-remote DSC transmission:

i.e. 1. 12-bit Sync Word (generated by the 1747)

2. 12-bit data pattern (generated by the test)

3. Cyclic code word (generated by the 1747, according to the pattern in 2.)

Note: Cyclic generation is not verified by the diagnostic when the 1747 is in the Transmit mode. Transmissions should be verified at the remote site.

Section 5 - Force Cyclic Error at Remote DSC

The purpose of this section is to force a cyclic code error at the remote DSC by transmitting two consecutive data patterns. The remote DSC in the RECEIVE TEST mode, expects transmissions to be ordered:

1. 12-bit sync word
2. 12-bit data pattern
3. Cyclic code word
4. Space word of all 0's

The remote DSC interprets the second transmitted data pattern as a cyclic code word, thereby forcing an error when the remote DSC compares the data word with its own generated cyclic code word.

Note: The 1747 diagnostic program is not capable of monitoring error conditions at the remote DSC. This test section is provided only as an aid to the operator at the remote station.

Section 6 - Receive Test

Under interrupt control, this section tests the capabilities of the 1747 to receive one-word data patterns from the remote DSC. Status is monitored for correct response, error-recovery paths are provided for possible reject conditions, and any abnormal conditions or unexpected conditions are reported by an appropriate error code. The test expects that the remote DSC is capable of transmitting the following 12-bit patterns:

1. 4257
2. 0000_8
3. 7777_8
4. 0155_8
5. 7622_8
6. Cyclic code word for 0000
7. Cyclic code word for 7777
8. Cyclic code word for 0155
9. Cyclic code word for 7622

Data comparisons are made by the test between the transmitted patterns and the expected patterns. Any discrepancies are reported by appropriate error codes. The test also verifies that the remote DSC is transmitting the Sync, Data, Cyclic, and Space (if generated) words correctly.

Interrupts tested are:

a. Data
b. End of Operation

Functions selected:

a. Select Data Interrupt
b. Select End of Operation Interrupt

Patterns Received

All those generated by the remote DSC.

Section 7 - Force Cyclic Errors at Dominant Site

This section forces a 1747 cyclic error at the dominant site by failing to input.

1. The pattern that is transmitted by the remote DSC.
2. The space word that is transmitted by the remote DSC.

Either of these conditions causes the 1747 to assume that the preceding transmission word (sync or cyclic) ended the receive operation and that the present word (pattern or space) is the cyclic code word. The 1747 then performs an error check with this word (pattern or space) against its own generated cyclic value. Failures to generate an Alarm Interrupt and the corresponding Alarm and Cyclic Error status are reported by appropriate error codes.

Section 8 - Transmit/Receive Synchronization

All the functions and objectives of sections 4 and 6 are combined in this section. Dependent upon the remote DSC's ability to automatically toggle from Receive to Transmit, this section operates the 1747 as fast as possible, alternating between Transmit and Receive. The transmitted data, received data, function selects, and status verification are as described in sections 4 and 6.

VII. REFERENCE DOCUMENTS

A. Control Data 1700 System Maintenance Monitor (SMM17). Pub. No. 60182000.

B. Design Objectives for 1747 Unit Diagnostic, dated 3/14/68.

C. Report on the 1747 Design Objectives Meeting, dated 4/1/68.

D. FJ412-A, B, C, Data Set Controller, Engineering Specification No. 36076300, dated 11/28/67.

E. Control Data QSE 974 Data Set Controller, Customer Engineering Manual, Pub. 38707700.

F. Control Data SMM17 Diagnostic Program Listings for the DSC 1747 Data Set Controller, Pub. 60221600.

G. Data Set Simulator, Dwg. No. 13658600.

H. 1747 Logic Prints, Dwg. No. 13658600.

I. Data Set 301B Interface Specification, March 1967.

J. External Reference Specification for the 1747 Unit Diagnostic dated 4/29/68.

1749 COMMUNICATIONS TERMINAL CONTROLLER

(CTCA43 Test No. 43)

I. INTRODUCTION

A. IDENTIFICATION

TITLE:	1749 Communications Terminal Controller Test Routine
TYPE OF PROGRAM:	Real-Time Test Routine
COMPUTER:	CONTROL DATA 1700

B. PURPOSE

This test routine verifies the operating capabilities of the 1749 communications terminal controller (CTC) and 321 telegraph terminal units (TTUs) in the echo mode of operation.

C. USAGE

1. Equipment Preparation

   a. Place all communications lines in the 1749 in echo mode.

   b. Turn on the 1749 CTC.

2. Error Stops

   An error stop occurs if the Selective Stop key is set and a typewriter reject occurs. All operation and data errors from the 1749 CTC are typed.

3. Alarms and Printouts

   a. Printouts or typeouts are of two (2) types: questions and error information.

      1) Questions - in preparation for the 1749 CTC test, the program asks the operator various questions pertaining to the equipment on the system and the subtests to be executed. The typeouts are further explained under the "parameter entry" section.

      2) Error Information - the computer types out any error information that is detected during the execution of the various subtests. If the Selective Skip key is set, all error typeouts are eliminated. The error information identifies the equipment number, the subtest, the TTU (if applicable), and the error detected.

b. List of Error Codes and Messages

Error Code	Typeout	Meaning
03	NO PARAMETERS	Not enough information to run the test.
13	ILL. CODE, TRY AGAIN	Wrong character received.
14	DUP. CHAR, TRY ANOTHER	Number already exists in tables.
20	NOT IN TABLE	Number entered is not in tables, nonexistent.
27	INTERNAL REJ.	Internal reject.
28	NO REJ.	Expected a reject, received none.
29	EXTERNAL REJ.	External reject.
32	TOO MANY CABS.	Test tables full, unable to accept more cabinets.
33	INT. STATUS SET	Interrupt status set, should not be.
34	COUNTER SHOULD BE 15	Counter should equal 15, does not.
45	CNTR EXP	Counter expected.
46	INT. STATUS NOT SET	Expected interrupt status, received none.
50	NO CHAR. REQ IN 300 MS	Waited 300 ms, character request not up.
51	UNABLE TO DROP CHAR.	Character Ready, will not drop.
54	NO INT.	Expected interrupt, did not happen.
56	INT. OCCURRED	Interrupt occurred, expected none.
61	NO BUFF TERM	Allowed total time for data to be transferred and received; test did not complete in allotted time.

c. The remainder of the typeouts is used for parameter entry and is self-explanatory.

4. Caution to User

   Test "0" and "3" should not be selected to execute if no intervention is wanted. These two subtests require that the operator perform certain functions upon program request. See individual test writeups.

5. Equipment Configuration

   a. From one to eight 1749 CTCs

   b. From one to 128 321 TTUs

   c. One 8909-C test board or test board drawers as needed

   d. One 1711, 1712, or 1713 teletypewriter

6. References - Refer to the Control Data Literature Catalog for publication numbers and latest revision levels.

   Control Data 1700 Reference Manual
   Control Data 1749 Reference Manual

II. OPERATIONAL PROCEDURE

A. INITIALIZATION

1. Enter Parameters - Description

   a. This routine inputs all information needed to execute the test. The equipment on the system may be any equipment number (0-F), and be made up as any number of TTUs in the cabinets. The parameters are entered through the teletypewriter. The appropriate questions are typed out and the operator responds by typing a "Y" or "N" or a numeric digit, whichever is applicable.

   b. Parameters can be added, deleted, or equipment can be changed if necessary. See "change parameter".

2. Parameter Entry Method

   Up to eight 1749 CTCs may be tested. They may be any equipment number (0 F).

   The following questions are typed out upon loading of the program. The operator must answer certain questions to set the test up. He must answer "Y" or "N" or other numeric data when requested.

a. 1749 Test

Total no. of cabinets - answer with the number of 1749s, a numeric digit 1-8. If more than one entered, questions 2 through 7 will repeat until all information is received.

b. Equip no. x - answer with a digit 0-F.

c. Int. level - answer with two digits 01-15.

d. All TTUs - if TTUs are a complete set (16), answer with a "Y", if not all one level, answer with an "N".

(4. A) All one level - if TTUs are all one level answer with a "Y". If mixed levels in cabinet, answer with an "N".

e. 0 1 2 3 4 5 6 7

f. 8 9 10 11 12 13 14 15

If 'N" is answered to all TTUs of all one level, 0-7 will be typed and the operator must enter the level of each TTU. If non available, answer "N". A total of 16 answers must be received.

g. Level - if "Y" is answered to all one level the operator must enter in the level of all TTUs in this particular cabinet.

h. Equip Tests

All tests - answer can be a "Y" or "N". If a "Y" is received all tests are selected to run on all equipments.

i. 0 1 2 3 4 5 6 7 - If an "N" is typed to all tests, the operator must answer a "Y" or "N" for tests to run. A total of eight must be received. Note: See caution to user.

j. Single Bit Test

Level typed out if test 5 is selected. The operator must answer with a digit 5-8.

Note: If 5 is answered to level, it is assumed that it is meant to be binary, not baudot. All levels are assumed binary.

3. Start Portion - Description

Upon completion of "initialize" or "change parameters" control will come to this portion. Subtests will be selected in an order of 0-7 if selected. Tests will terminate upon manual interrupt or master clear.

B. CHANGE PARAMETER - DESCRIPTION

1. This routine allows the operator to delete, add, change any piece of equip on the system or change the tests to be executed.

2. Entry into this routine is accomplished by pressing M. I. (manual interrupt) on the typewriter. Also by master clear and run from zero.

3. Upon entry into this routine the following will be typed:

   a. Change Parameters - answer "Y" to delete, add, change equip, or change tests. Answer "N" to omit any changes and start tests. Tests will start to operate if "N" is answered.

   b. Delete - answer "Y" to delete any piece of equipment from the test. Answer "N" to proceed to the next portion and omit this feature.

      If a "Y" is answered, the operator must give an equipment to delete when asked. This equipment is no longer available for test.

   c. Add - answer "Y" to enter a new equipment to test. Answer "N" to proceed to change equipment.

      a. If a "Y" is answered, the operator will go through the sequence of a 2.2-7, before continuing on to change equipment.

   d. Change Equip - answer a "Y" to alter a piece of equipment in the tests table. Answer "N" to proceed to "change tests".

      If a "Y" is answered the operator will go through the sequence A. 2. 2-7 before continuing on to "change tests".

   e. Change Tests - answer a "Y" to alter the tests to be run. Answer an "N" to continue on to "change parameters"

      If a "Y" is answered the operator will be asked to answer the questions in A. 2. 8 before continuing on to "change parameters".

C. SUBTESTS

1. Protect Switch Test - 0

   a. The Protect switch test operates the cabinets to check the protect feature of the 1749 CTC. To do this it sets the protect bit in core memory and checks for rejects from the 1749. The first check is for reject on the initial addressing. The switches are asked to be set at this time on the 1749 and the 1700 and addressing is tried again. If a reject occurs an error is typed. The Protect switch on the 1749 is asked to be disabled

and addressing is attempted again, checking for reject. If a reject occurs, an error exists. The switch on the 1749 is asked to be set and the protect bit is cleared in memory. Addressing is attempted, rejects should occur. To complete this subtest both switches are asked to be removed and a check is made that all cabinets have been tested, if not this sequence is repeated until all cabinets are checked.

b. This test must have manual intervention, it is not recommended to be run unless problems are found in program protect features in the cabinets. This test is non real time.

2. Counter Test - 1

a. This subtest checks each 1749 on the system to verify the counter will function properly. It does this by setting the counter to 15 and verifying a count of fifteen. It will then advance the counter from zero through fifteen. Each time the counter is advanced it is checked against a fixed counter in the program. Upon completion of the counter advancing to fifteen a pattern of A, 5 is sent to the selected device to check switching capabilities.

b. It is possible to get three errors from one equipment that rejects the program. The program checks each cabinet in three different parts explained above.

3. Clock Interrupt Test - 2

a. The clock interrupt test times the cabinets on the system to determine their interrupt clock speed. To do this the program enables interrupts after the first interrupt, the program counts the time before a second interrupt is received. It will print the time if it varies from the previous time located in its table on each cabinet. This test uses the interrupt on clock function.

4. Interrupt on Character Request - 3

a. This subtest checks the interrupt on character request function in each cabinet on the system. To do this the program enables the interrupt function in a cabinet and waits for the interrupt. If no interrupt occurs an error is asked to "remove all TTU's" from this particular cabinet being tested, enables the interrupt function again and waits for the interrupt. An error exists if an interrupt occurs. Upon timeout the operator is asked to "replace TTUs" and checks whether all cabinets have been tested.

b. This subtest needs manual intervention. It cannot be run under a real-time application.

5. Interrupt on Character Ready - 4

This subtest checks the interrupt on Character Ready function from each cabinet and all TTUs on the system. To do this the program finds an equipment number in its tables, checks for TTUs available and outputs a character to each TTU (one TTU at a time), and waits for an interrupt. Upon interrupt it checks for proper status and updates to find if all TTUs have been checked. This routine is repeated until all cabinets are checked.

6. Pattern Tests - 5, 6, 7

a. These subtests use a common input output and verify routine called "data transfer". Test five is the single bit test. It builds the output buffer with the character entered in during initialization. Test six is a pattern test which uses A A, 5 5 as its pattern. It will build the output buffers to contain this pattern. Test seven builds the buffers with one character, transfers control to the data transfer routine for I/O and gets control back, updates the buffers by one until a total count of 256 has been transferred before exiting to "start control" to select another test to run.

b. The common I/O routine called "data transfer" outputs to all cabinets and TTUs on the system. It will do this seven times before verifying the output against the input. Any errors are typed at this time. After validation, the interrupt is switched from clock to character ready to character request. Each cabinet will be used as the base interrupt and each interrupt function is checked within the cabinet.

c. Total time for the I/O buffers is calculated by multiplying the total number of cabinets of the system by a fixed value of 11 seconds for each cabinet. If the transfer of seven characters per TTU is not complete when the timeout expires an error is typed and control is returned to find whether all cabinets are complete.

III. INTERNAL TABLES

1.	CCTABL	(9)	Communication equipment table
2.	CCTTAB	($78)	Communication TTU table
3.	CCTSTB	(9)	Communication equipment test table

4.	CCITOB	($300)	Output buffer area table
5.	CCITIB	($300)	Input buffer area table
6.	INTTB1	(9)	Cabinet interrupt level table
7.	CCITTL	(9)	Cabinet interrupt time table
8.	CCTTAD	(9)	TTU address table per cabinet
9.	CCIBAD	(9)	Input buffer address table per cabinet
10.	CCOBAD	(9)	Output buffer address table per cabinet
11.	CCTSTA	(9)	Test jump address table

SUPPLEMENT TO 1749 TEST

A. IDENTIFICATION

TYPE: Add on to 1749-321 test

B. PURPOSE

This addition to the 1749 test will allow the testing of 311B's in UNIVERSAL, ASC 2 or IBM 4 of 8 mode.

C. USAGE

1. Equipment Preparation

Place 211B in Echo mode. This is usually accomplished by changing J04, J20 DECODER plugs to full duplex. Data set must be a half-duplex set.

2. Error Stops

See 1749 test write-up (See 1749 write-up.)

3. Alarms and Printouts

a. Data Errors (See 1749 write-up.)

b. List of error codes and messages

Error Code	Typeout	Meaning
31	311B mode	The test is asking for the mode of operation of the 311B. The operator should answer "I" for IBM 40F8 mode, "U" for Universal mode, or "A" for ASC2 mode of operation.
64	Status error	Expected all control side status bits to be set. Each 311B mode (except UNIVERSAL) has control word status bits. All control word status bits should have been set. Error status if typed.
65	Parity	The test is asking for the 311B Parity mode setting. Operator must answer with letter "O" for odd parity.
66	SYNC code	The test expects three digits to be typed which equal the SYNC code of all 311B's to be tested. Convert binary code to hex. before entering the code in the system.
67	No parity error status	The test is asking for the mode of operation of the 311B. The operator should answer "I" for IBM 40F8 mode, "U" for a UNIVERSAL mode, or "A" for ASC 2 mode of operation.

4. Caution to User

   a. 311B's cannot be tested if there are two or more cabinets in the system to check. All 311B modules must be in one cabinet at a time. The reason is, interrupts are used from each cabinet separately, thus data from the off line cabinet will not complete in the Interrupt on Character Ready mode.

   b. If 311B modules are in the cabinet being checked but are not in use, the control side Bit 11 must be disabled. This bit will cause an interrupt when Interrupt on Character Ready is selected in the cabinet. An extra character will be received by the 321's being tested if this bit is not turned off.

   c. Clear to send must be returned to the 311B in less than 200 ms. Transmission errors will occur if Clear to Send is not received from the data set.

d. The 311B Sync character must be entered in hexadecimal codes. The operator must convert the binary Sync code to hex. format and answer the Sync code question with three digit hex. number.

e. Test number four cannot be run if only 311B modules are in the system to check.

f. Place all communication lines in the Echo mode.

g. Do not attempt to check unit with equipment switch set to 1. This number belongs to the low speed controller.

h. All 311B modules are assumed to have Odd parity.

i. Set 1749 interrupt clock to 1/10 less than fastest module to check.

j. Interrupt must not be less than 1.5 ms.

5. Operation

a. Typical system events

To test a 311B in a cabinet the operator must define during parameter entry/ initialize phase the 311B to the system. This is accomplished by defining the data side of the 311B with the letter "D" and the control side with the letter "C". These two letters are defined to the test when TTU levels are asked of the modules to test.

Example:

If the 311B is in the first and second slots in the 1749, the following should be entered:

01234567
DC etc.

This will define the 311B in slots "0" and "1" of the 1749. The 311B can be at any address inside the 1749 as long as the operator defines the correct address of the 311B. The test will ask for 311B mode, the operator must enter a "U" for Universal mode, a "1" for IBM 4 of 8 mode of "A" for ASC2 mode. The Sync character is asked for and the operator must reply with a three digit number. The Sync code entered in is assumed to be the Sync code for all 311B's being checked. During the execution phase all data tests (5-7) will run on the 311B's along with the 321's. The exceptions to the data being transferred are: no control characters will be transferred that are equal to 4 of 8 or ASCII control characters plus the system Sync character.

This is accomplished by adding one to the output word if it equals a control/SYNC character. Upon completion of the data tests, the 311B routine will check the status bits on the odd channel of the 311B if the 311B is plugged for 4 of 8 or ASCII mode. The routine will send all the control characters for the proper 311B mode in operation to the 311B. It checks that all status bits on the odd channel can be set. If an error is found a typeout will occur and the bad status is typed for operator reference.

4 of 8 and ASCII parity error status is checked by sending specific code that will get a parity error indication. Errors are typed with the word in error if no parity error status is received with each word sent. These are the checks that are made on the 311B.

1748-2 MULTIPLEXER CONTROLLER, CSPL COMMUNICATIONS ADAPTER
(MCCA48 Test No. 48)

32K MODE

I. IDENTIFICATION

A. EQUIPMENT TESTED

1748-2 Multiplexer Controller (MC)

DJ808A Communications Multiplexer (MUMOD) - 364-1,2

DJ813A Communications Multiplexer (MUMIX) - 364-3

DJ144A Synchronous Communication Adapter (SCA-1) - 361-5

DJ145A Synchronous Communication Adapter (SCA-2) - 361-6

DJ122A Asynchronous Communication Adapter (ACA-1) - 361-4

DJ142A, DJ143A Communication Adapter (SACA) - 361-1

II. INTRODUCTION

The 1748-2 MC CSPL Diagnostic Program checks the function, status, and data handling capabilities of the multiplexer controller, communication multiplexers, and communication adapters (SCA-1, SCA-2, ACA, and SACA) through the use of individually selectable sections. Up to 512 single address communication adapters (CAs) or any combination of single and dual address CAs, not to exceed 512 addresses, may be tested at one time.

III. REQUIREMENTS

A. HARDWARE

1748-2 Multiplexer Controller (MC)

DJ808A Communication Multiplexer (MUMOD)

DJ813A Communication Multiplexer (MUMIX)

DJ144A, DJ145A Synchronous Communications Adapter (SCA-1, SCA-2)

DJ122A Asynchronous Communication Adapter (ACA)

DJ142A, DJ143A Communication Adapter (SACA)

(See Figure 1)

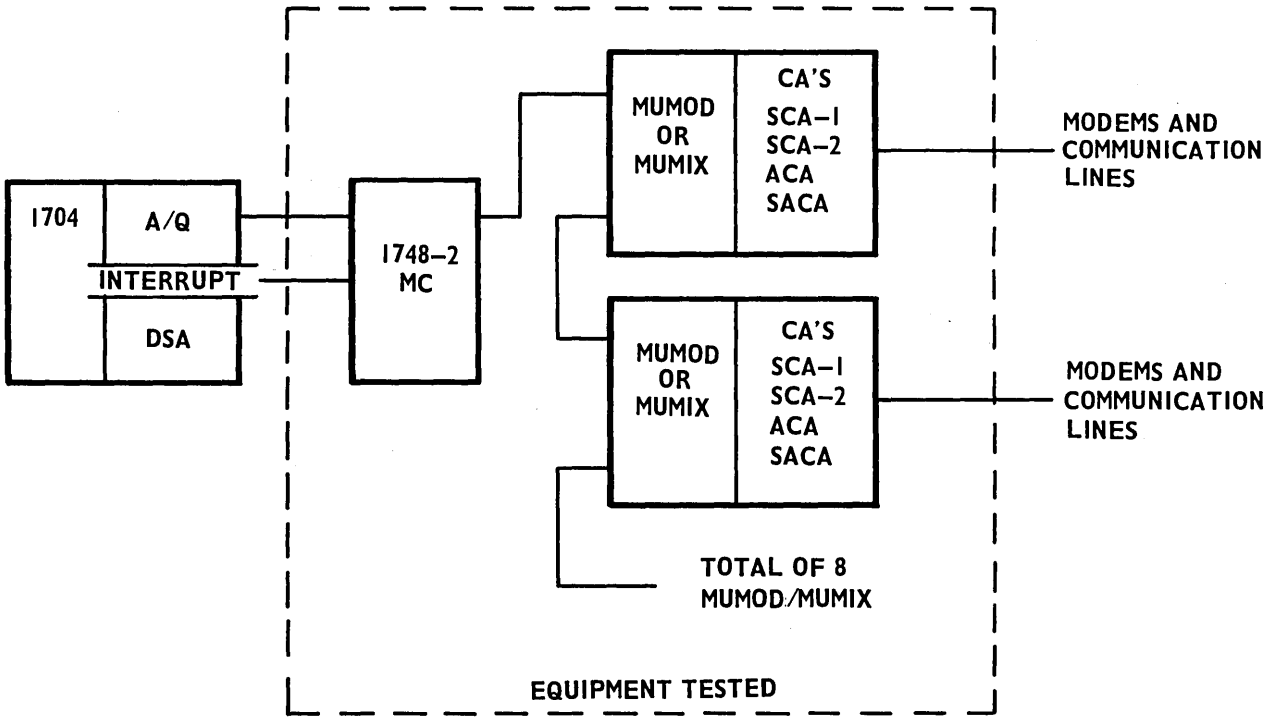

1704
A/Q
INTERRUPT
DSA
1748–2
MC
MUMOD
OR
MUMIX
CA'S
SCA–1
SCA–2
ACA
SACA
MODEMS AND
COMMUNICATION
LINES
MUMOD
OR
MUMIX
CA'S
SCA–1
SCA–2
ACA
SACA
MODEMS AND
COMMUNICATION
LINES
TOTAL OF 8
MUMOD/MUMIX
EQUIPMENT TESTED

Figure 1.

B. SOFTWARE

The 1748-2 MC CSPL Diagnostic Program operates under the SMM17 Diagnostic Monitor as a type 7 test.

C. ACCESSORIES

No special accessories are required for test execution.

IV. LIMITATIONS

A. Due to the limited computer hardware and time, the test is not capable of the following:

1. Testing the DJ146A (ACUCA).
2. DSA test.
3. Generating a Character Lost interrupt (bit 09), and parity (bit 08).
4. Transparent mode.
5. SACA Set and Clear Break test.

B. The following equipment is the only CSPL hardware on which the test has been executed.

1. Three DJ808A's (MUMOD)
2. Sixteen DJ142's (SACA)
3. Four DJ144A's (SCA-1)
4. Four DJ145A's (SCA-2)
5. One DJ122A's (ACA)

All of the above equipments have been simultaneously tested by this diagnostic.

C. When selecting pluggable options on the asynchronous communication adapter, the send clock rate and bit level must equal the receive clock rate and bit level.

D. When testing synchronous communication adapters, a data set or equivalent must be connected to the CA. The following data sets and their equivalents are compatible.

1. Data Sets 201-A/B
2. Data Sets X203-A
3. Data Set 303

E. The single address communication adapter (SACA) must be placed in the echo mode before testing.

F. Run in 32K mode only when using 1714.

G. Prestoring Parameters - The parameters for the DJ808/813 can only be prestored in this test using edit Prestored Parameters feature. The parameter A6, Q6, however, cannot be effectively prestored.

The CA parameters may be prestored using Program Modification feature in edit for a maximum of 14 CA's.

V. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

1. Load the SMM17 library.

2. The computer will halt with the Overflow light lit. Set the A register equal to the desired SMM parameter word configuration (for normal operation, set bits 4 and 5 and the appropriate loader designation bit). Set the Q register equal to the desired SMM Stop/Jump parameter configuration and place the STEP/RUN switch in the Run position.

3. When the computer stops, set the A register to the desired SMM ID word configuration with the upper eight bits equal to 48. Set the Q register bits 7 through 10 equal to the 1748-2 MC equipment number and set bit 0. Place the SELECTIVE SKIP switch in the Off position. Place the STEP/RUN switch in the Run position.

4. The typewriter will type:
MCCA48, 1748-2 MC CSPL DIAGNOSTIC - TEST. VRS. 3.1
IA = XXXX. FC = XXXX CP 03

5. The computer will halt with the Overflow light lit. The A register will contain the test ID word and the Q register will contain the Stop/Jump word. The Stop/Jump parameter word in the Q register may be changed at this time if desired. No change is required for normal operation of the program.

6. The following stops will be parameter stops necessary for test execution.

NOTE

If only function tests are to be run, it is necessary to enter parameters for at least one CA, even though there is no CA to test (in the multiplexer rack).

B. PARAMETERS

1. General

Parameters are entered through the A and Q registers at the computer control console and are divided into two basic groups, the system parameters and the CA parameters. The first five stops, after the SMM ID/Stop/Jump are required to enter the system parameters. The remaining stops, up to 548, are required to enter the CA parameters.

NOTE

Any time that the Overflow light is lit and the A register contains $48XX_{16}$ during parameter entry, the A and Q registers contain the SMM ID/Stop/Jump word. Care must be taken not to change these parameters at this time. The SMM ID/Stop/Jump word will be displayed at the beginning of parameter entry, between system and CA parameter entry, and after every 14 CA parameter stops.

2. System Parameters

a. First Stop

Set the A register (bits 07 through 10) equal to the 1748-2 MC Equipment number switch settings. Set the Q register bit that is equal to the 1748-2 MC interrupt line number.

Place the STEP/RUN switch in the Run position.

b. Second Stop

The A register contains the least significant hexadecimal number that the CONTROL WORD BANK switches on the 1748-2 MC can be set to. These switches can be set to any number greater than this number providing there is enough core remaining to contain the next 2048 locations required for the buffer control words. The A register and the CONTROL WORD BANK switches must be set to equal the same number (bits 11 through 14). It is recommended that the CONTROL WORD BANK switches be set equal to the number contained in the A register at this stop.

The Q register contains the least significant hexadecimal number that the INTERRUPT CONTROL WORD ADDRESS switches on the 1748-2 MC can be set to. These switches can be set to this number or any number greater than this number, providing the number does not fall within the Buffer Control Word Bank location. The Q register and the

INTERRUPT CONTROL WORD ADDRESS switches must be set to equal the same number. It is recommended that the INTERRUPT CONTROL WORD ADDRESS switches be set equal to the number contained in the Q register at this stop.

Place the STEP/RUN switch in the Run position.

c. Third Stop

The A register contains a bit configuration corresponding to the first 15 CA data subtests. Bit 01 corresponds to subtest 01, bit 02 to subtest 02, etc. To select a subtest, set its corresponding bit in the A register. Setting bit 00 in the A register is an illegal entry. CA data subtests are described in Section III of this document. To run the first 15 data subtests, do not change the contents of the A register at this stop.

The Q register contains a bit configuration corresponding to the second 15 CA data subtests. Bit 00 corresponds to subtest 10_{16}, bit 01 to subtest 11_{16}, etc. To select a subtest, set its corresponding bit in the Q register. Setting bit 15 in the Q register is an illegal entry.

NOTE

All subtests selected at this stop will be run on all CAs selected later in parameter entry.

Place the STEP/RUN switch in the Run position.

d. Fourth Stop

The A register contains a bit configuration corresponding to the 1748-2 MC function subtests. Bits 01 through 11 correspond to function subtests 41_{16} through $4B_{16}$. To select a subtest, set its corresponding bit in the A register. To run all subtests selectable at this stop, do not change the contents of the A register. The function subtests are described in Section III of this document.

Set the Q register to the maximum CA address generated by the communications expansion network. This maximum scan address corresponds to three octal digits (bits 00 through 08) that represents the highest CA address generated by the expansion network (Figure 2).

08 07 06	05 04 03	02 01 00
3rd-Level, generated by a communications expansion unit	2nd-Level, generated by the 1748-2 MC	CA Address, generated by the communication multiplexer

Figure 2.

Place the STEP/RUN switch in the Run position.

e. Fifth Stop

Set the A register to the hexadecimal equivalent of the total number of CA addresses to be tested. Dual address CAs equal two addresses and single address CAs equal one. This parameter will determine the number of parameter stops made in the remaining portion of the parameter entry as in the following example.

The system to be tested contains the following CAs.

CA Type	No. of Addr.
SCA-1	2
SCA-1	2
SCA-2	2
SCA-2	2
ACA-1	2
SACA	1
SACA	1
	12 = OC_{16}

Enter the A register with a hexadecimal 000C.

NOTE

Bits 15 of the A register is used to preserve previously entered CA parameters. If bit 15 is cleared, the CA parameters will be preserved. If bit 15 is set, the unused portion of the parameter entry table (PETBL = 1024 locations) will become available to the program as data buffers.

Clear the Q register.

Place the STEP/RUN switch in the Run position. The computer will halt with the Overflow light lit and the ID/Stop/Jump words in the A and Q registers. Place the STEP/RUN switch in the Run position. The following stops will be CA parameter stops.

3. CA Parameters

a. General

CA parameters must be entered in the A and Q registers for every address containing a CA to be tested. In the case of dual address CAs the parameters for the even side CA address must be entered first with the next consecutive parameter stop containing the odd side CA address parameters. Excluding the above exception, CA parameters may be entered in any order with respect to CA type or address. Figures 3 and 4 will define the A and Q register bit configurations for the CA parameters.

NOTE

Remember that after every 14 CA parameter stop, the ID/Stop/Jump words will be displayed in the A and Q registers with the Overflow light lit. Do not change these parameters.

A Register Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	A	A	A	A	B	B	B	B	B	B	B	B	B	C	C
CA Type					CA Address									CA Parity	

BIT DEFINITIONS

CA Type (AAAAA)

00000 = Illegal Type

00001 = SCA-1 (Dual Address)

00010 = SCA-2 (Dual Address)

00011 = ACA-1 (Dual Address)

00100 = ACA-2 (Dual Address)

10000 = SACA (Single Address)

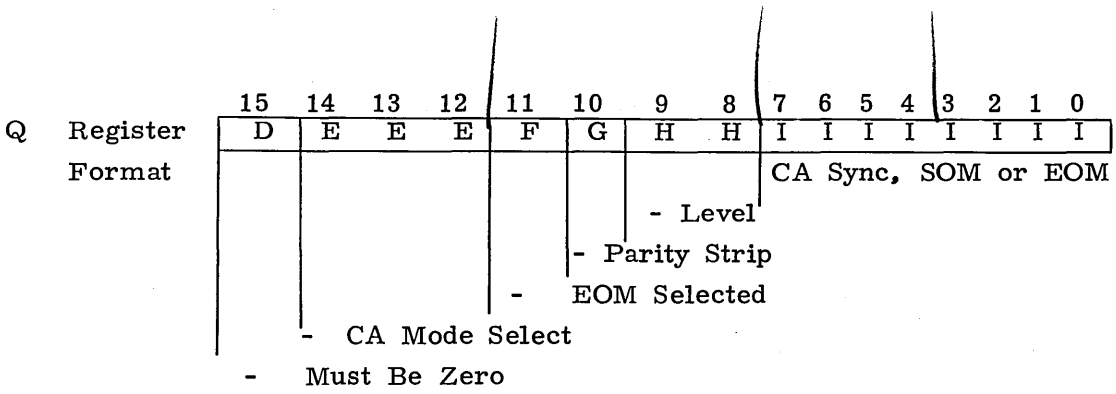
01001 = Illegal Type

CA Address (BBBBBBBBB) = Any three octal digits equal to the CA address.

CA Parity (CC)

00 = No parity selected or available.
01 = Odd parity selected.
10 = Even parity selected.
11 = Illegal parity selection.

Figure 3. CA A Register Parameter Format



BIT DEFINITIONS

Q register bit 15 must always be zero (D).

MODE SELECT (EEE)

000 = Illegal Selection
001 = ASCII Mode
010 = Universal Mode
011 = Four-of-Eight Mode
100 = IBM-A Mode
101 = IBM-B Mode
110 = IBM Master Mode
111 = IBM Slave Mode

EOM SELECT (F) = 1 when end of message interrupt (bit 08) is selected.

PARITY STRIP (G) = 1 when parity (bit 07) will be stripped on input. A feature of some CAs.

LEVEL (HH)

00 = Five Level (5 bits including parity)
01 = Six Level (6 bits including parity)
10 = Seven Level (7 bits including parity)
11 = Eight Level (8 bits including parity)

CA Sync, SOM or EOM (IIII IIII) = Any 8-bit combination equal to the sync character on synchronous CAs. On dual address CAs where Start of Message (SOM) and and End of Message (EOM) characters are variable and selectable (ACA-1, etc.) enter the SOM in the even address Q parameter and the EOM in the odd address Q parameter. On dual address synchronous CAs (SCA-1, etc.) enter the sync character in both even and odd Q parameters.

Figure 4. CA Q Register Parameter Format

4. No parameters are assumed or automatic. All parameters are manual and must be selected by the operator.

5. Stop/Jump Parameter Bit Definitions

   Stops

   Stop 0 (bit 0 = 1) Stop to enter parameters.

   Stop 2 (bit 1 = 1) Stop at end of test section.

   Stop 4 (bit 2 = 1) Stop at end of test.

   Stop 8 (bit 3 = 1) Stop on error.

   Jumps

   Jump 0 (bit 4 = 1) Undefined.

   Jump 1 (bit 5 = 1) Repeat section just completed.

   Jump 2 (bit 6 = 1) Repeat test just completed.

   Jump 3 (bit 7 = 1) Undefined.

   Jump 4 (bit 8 = 1) Omit typeouts.

   Jump 5 through 10 (bits 9 to 14) Undefined.

   Jump 11 (bit 15 = 1) Omit end of test typeout only.

C. SECTION DESCRIPTION INDEX

Test No. (Reg. Bit)	Name and Description	Page	Run Time
01(A01)	Data Test, Zeros, Word Mode		
02(A02)	Data Test, Ones, Word Mode		
03(A03)	Data Test, Checkerboard (CB), Word Mode		
04(A04)	Data Test, Sliding One, Word Mode		
06(A06)	Data Test, Sliding CB, Word Mode		
07(A07)	Data Test, Zeros, Buffered Word In/Out		
08(A08)	Data Test, Ones, Buffered Word In/Out		
09(A09)	Data Test, CB, Buffered Word In/Out		
0A(A10)	Data Test, Sliding One, Buffered Word In/Out		
0B(A11)	Data Test, Sliding Zero, Buffered Word In/Out		
0C(A12)	Data Test, Sliding CB, Buffered Word In/Out		
0D(A13)	Data Test, Zeros, Buff. Char. In, Buff. Word Out		
0E(A14)	Data Test, Ones, Buff. Char. In, Buff. Word Out		
0F(A15)	Data Test, CB, Buff. Char. In, Buff. Word Out		
10(Q00)	Data Test, Sliding One, Buff. Char. In, Buff. Word Out		
11(Q01)	Data Test, Sliding Zero, Buff. Char. In, Buff. Word Out		
12(Q02)	Data Test, Sliding CB, Buff. Char. In, Buff. Word Out		
13(Q03)	Data Test, Zeros, Buff. Word In, Buff. Char. Out		
14(Q04)	Data Test, Ones, Buff. Word In, Buff. Char. Out		
15(Q05)	Data Test, CB, Buff. Word In, Buff. Char. Out		
16(Q06)	Data Test, Sliding One, Buff. Word In, Buff. Char. Out		
17(Q07)	Data Test, Sliding Zero, Buff. Word In, Buff. Char. Out		
18(Q08)	Data Test, Sliding CB, Buff. Word In, Buff. Char. Out		
19(Q09)	Data Test, Zeros, Buffered Char. In/Out		
1A(Q10)	Data Test, Ones, Buffered Char. In/Out		
1B(Q11)	Data Test, CB, Buffered Char. In/Out		
1C(Q12)	Data Test, Sliding One, Buffered Char. In/Out		
1D(Q13)	Data Test, Sliding Zero, Buffered Char. In/Out		
1E(Q14)	Data Test, Sliding CB, Buffered Char. In/Out		

Test No. (Reg. Bit)	Name and Description	Page	Run Time
41(A01)	Function Test, Start/Stop Scan		
42(A02)	Function Test, Status, Clear Interrupt and Status		
43(A03)	Function Test, Set/Clear CA Address Register		
44(A04)	Function Test, Word Mode Interrupt		
45(A05)	Function Test, End of Operation Interrupt		
46(A06)	Function Test, Scan Failure Interrupt		
47(A07)	Function Test, Busy Check		
48(A08)	Function Test, Program Protect Fault		
49(A09)	Function Test, Single Scan, Dual Scan		
4A(A10)	Function Test, Clear Lockout and Status		
4BCA(1)	Adder Test		
	Total Running Time		

VI. OPERATOR COMMUNICATION

A. MESSAGE FORMATS

1. Test Execution Error (typeout) Format

A	Q	A	Q	A	Q	A	Q
XXXX	STJP	XXYY	RRRR	EERR	DDDD	DDDD	DDDD

XXXX is the SMM ID word.

STJP is the SMM Stop/Jump parameter.

XX-- is the test section number.

--YY is the error number.

RRRR is the return address of the error reporting routine.

EERR is the listing address of the routine detecting the error.

DDDD is data or information relevant to the error.

2. Test Execution Error (halt on error) Format.

The halt on error format is the same as the typeout format.

3. Parameter Entry Errors

Parameter entry errors follow the above format. The test section number will always be zero and the error code number will indicate the type of parameter entry error detected. Parameter errors detected during system parameter entry will return the program to the beginning of system parameter entry for error correction and parameter re-entry after the error has been reported. Errors detected during CA parameter entry will, after reporting the error, return to the beginning of CA parameter entry for corrections and re-entry of the parameters. Refer to the message dictionary for error code number definitions and locations.

B. MESSAGE DICTIONARY

Error Code	Message	Page No.
0001	No Subtest Selected	
0002	No CA Selected	
0003	Illegal BCW Switches	
0004	Illegal ICW Switches	
0005	Previously Entered CA	
0006 0010-65K	CA Parameter Transfer Error	
XX11	Interrupt With No Interrupt Status Set	
XX12	Prior End of Input Buffer Received	
XX13	Reject on Program Clear	
XX14	Input Term Before Output Term Received	
XX15	Prior End of Output Buffer	
XX16	Could Not Program Clear CA	
XX17	Output Terminated After Input	
XX18	End of Input and Output Together	
XX19	CA Bit 08 Set	
XX1A	CA Bit 09 Set	
XX1B	Input Acknowledge Failure	
XX1C	Output Acknowledge Failure	
XX1E	Unexpected Real Time Interrupt	
XX1F	CA Timed Out	
XX20	Scan Failure, This Unit	
XX21	Ext. Reject On Status, Start Scan Routine	
XX22	Int. Reject On Status, Start Scan Routine	
XX23	Ext. Reject On Start Scan Function ($B)	
XX24	Int. Reject On Start Scan Function ($B)	
XX30	Can Not Clear CA Address Register	
XX31	CA Address Register Busy, Could Clear	
XX32	Ext. Reject On Status Request	
XX33	Int. Reject On Status Request	
XX34	Int. Reject On Function	
XX35	Ext. Reject On Function	
XX36	No EOP Status Bit Received (A08)	
XX37	Data Verify Error	
XX38	CA Control Side Status Error	
0040	CA Type Undefined	

Error Code	Message	Page No.
0041	Parity Selection Error	
0042	Bit 15 of the Q Parameter Word Not Zero	
0043	Mode Selection Error	
0044	EOM Selection Error	
0045	Parity Strip Bit Error	
0046	Level Selection Error	
0047	Sync Character Selection Error	
004A	CA Address Greater than Max Scan	
004B	Illegal CA Parameter	
XX50	Int. Reject On Stop Scan	
XX51	Ext. Reject On Stop Scan	
XX52	Int. Reject On Status	
XX53	Ext. Reject On Status	
XX54	Unexpected Status	
XX55	Int. Reject On Start Scan	
XX56	Ext. Reject On Start Scan	
XX57	Scan Failure-Int. Not Received	
XX58	Scan Failure-Did Not Clear With an Int. Status Req. (Q = Status Received)	
XX59	Int. Rej. Enable Word M.I.	
XX5A	Ext. Rej. Enable Word M.I.	
XX5B	Busy After Clear CA Address Register	
XX5C	Int. Rej. on Set CA Address Register	
XX5D	Ext. Rej. on Set CA Address Register	
XX5E	Int. Rej. on Clear CA Address Register	
XX5F	Ext. Rej. on Clear CA Address Register	
XX60	Int. Rej. Disable Word M.I.	
XX61	Ext. Rej. Disable Word M.I.	
XX62	Word Mode Int. Not Received	
XX63	Word Mode Int. Status Did Not Clear	
XX64	EOP Status Did Not Clear After Int. Was Processed	
XX65	EOP Int. Not Rcved (CA Odrs ZERO)	
XX66	EOP Int. Not Rcved (CA Max. Scan Setting)	
XX67	Scan Failure-This Unit Did Not Drop (After Start Scan)	
XX69	Int. Reject on Single Scan	
XX6A	Ext. Reject on Single Scan	
XX6B	Int. Reject on Dual Scan	

Error Code	Message	Page No.
XX6C	Ext. Reject on Dual Scan	
XX6D	Int. Reject on Clear, Lock Out and Status	
XX6E	Ext. Reject on Clear, Lock Out and Status	
XX6F	Unexpected Int. received	
XX70	Adder Error	

1. Message Explanation

0001 - No Subtest Selected

A	Q	A	Q
4828	STJP	0001	RRRR

STJP = Stop/Jump Parameter

RRRR = Return Address of Error Routine

Explanation - This error indicates that no subtest was selected during the third and fourth system parameter entry stops. After this error is reported, control is returned to the beginning of system parameter entry for correction of the error condition.

0002 - No CA Selected

A	Q	A	Q
4828	STJP	0002	RRRR

STJP = Stop/Jump Parameter

RRRR = Return Address

Explanation - This error indicates that no entry was made in A register at the fifth system parameter entry stop indicating that no CA had been selected for test. Control is returned, after the error report, to the start of system parameter entry for correction of the error condition.

0003 - Illegal BCW Switches

A	Q	A	Q
4828	STJP	0003	RRRR

STJP = Stop/Jump Parameter

RRRR = Return Address

Explanation - This error indicates that the number entered in the A register at the second system parameter stop (CONTROL WORD BANK switches) was either less than the last word address of the program or greater than the maximum core available. Control is returned to the start of system parameter entry for correction of the error.

0004 - Illegal ICW Switches

A	Q	A	Q
4828	STJP	0004	RRRR

STJP = Stop/Jump Parameter

RRRR = Return Address

Explanation - This error indicates that the number entered in the Q register at the second system parameter stop was either less than the last word address of the program or greater than the maximum core available. Control is returned to the start of system parameter entry for correction of the error.

0005 - Previously Entered CA

A	Q	A	Q	A	Q	A	Q	A	Q
4858	STJP	0005	RRRR	AAAA	BBBB	CCCC	DDDD	EEEE	FFFF

STJP = Stop/Jump Parameter

RRRR = Return Address

AAAA = Address of Error Detecting Routine

BBBB = Parameter A of previously entered CA parameter

CCCC = Parameter Q of previously entered CA parameter

DDDD = Parameter A of matching CA parameter

EEEE = Parameter Q of matching CA parameter

FFFF = Number of CA parameters checked before match detected

Explanation - This error indicates that two CA parameters have been entered for the same CA address. This is an illegal condition and one of the two must be changed. Control is returned to the start of CA parameter entry.

0006 - CA Parameter Transfer Error

A	Q	A	Q
4828	STJP	0006	RRRR

STJP = Stop/Jump Parameter

RRRR = Return Address

Explanation - This error indicates that an error was detected in the number of CA parameters entered through the A/Q registers and the number of CA parameters stored in the parameter entry table (PETBL). Control is returned to the start of CA parameter entry.

XX11 - Interrupt With No Interrupt Status Set

A	Q	A	Q	A	Q
4838	STJP	XX11	RRRR	AAAA	BBBB

STJP = Stop/Jump Parameter

XX-- = Subtest Number (Section)

RRRR = Return Address

AAAA = Address of Error Detecting Routine

BBBB = 1748-2 Status Involved With Error

Explanation - This error indicates that an interrupt was received from the 1748-2 on the interrupt line and that inspection of the 1748-2 status did not indicate an interrupt status bit set.

XX12 - Prior End of Input Buffer Received

A	Q	A	Q	A	Q	A	Q	A
4878	STJP	XX12	RRRR	AAAA	PRMA	PRMQ	ICW1	ICW2

Q	A	Q	A	Q
OCW1	OCW2	OPST	CAIW	DTBF

STJP = Stop/Jump

XX-- = Subtest Number

RRRR = Return Address

AAAA = Address of Error Detecting Routine

PRMA = CA Parameter A (A register entry)

PRMQ = CA Parameter Q (Q register entry)

1CW1 = Input Control Word One (when available)

ICW2 = Input Control Word Two (when available)

OCW1 = Output Control Word One (when available)

OCW2 = Output Control Word Two (when available)

OPST = CA Operational Status where:

Bit 00 = Character request enabled for CA

Bit 14 = Output buffer terminate int. received

Bit 15 = Input buffer terminate int. received

CAIW = CA Interrupt Word (when resulting in error)

DTBF = First word address of data buffer active when error detected, plus internal status information. To find the data buffer first word address, remove bits 15, 04, 03, 02, 01, 00.

Explanation - This error indicates that two CA interrupt words were received for this CA with bit 15 (End of Input Buffer) set during the indicated subtest.

XX13 - Reject On Program Clear

A	Q	A	Q	A	Q
4838	STJP	XX13	RRRR	AAAA	BBBB

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

AAAA = Address of Error Detecting Routine

BBBB = CA Address

Explanation - This error indicates that an attempt to program clear a CA resulted in an internal or external reject.

XX14 - Input Terminate Before Output Terminate Received

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word was received with bit 15 (End of Input Buffer) set before a CA interrupt word with bit 14 (End of Output Buffer) set was received. In all buffered tests in this program the output buffer should always terminate before the input buffer terminates.

XX15 - Prior End of Output Buffer

Format is the same as XX12 error format.

Explanation - This error indicates that two CA interrupt words were received for this CA with bit 14 (End of Output Buffer) set during the indicated subtest.

XX16 - Could Not Program Clear CA

A	Q	A	Q	A	Q
4838	STJP	XX16	RRRR	AAAA	BBBB

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

AAAA = Address of Error Detecting Routine

BBBB = CA Address

Explanation - This error indicates that the busy bit (bit 01) of the 1748-2 status did not drop after an attempt to enable character request for a word mode output to program clear the indicated CA.

XX17 - Output Terminated After Input

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word with bit 14 (End of Output Buffer) set was received after receiving a CA interrupt word with bit 15 (End of Input Buffer) set.

XX18 - End of Input and Output Together

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word with both bit 15 (End of Input Buffer) and bit 14 (End of Output Buffer) set was received.

XX19 - CA Bit 08 Set

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word with bit 13 (CA status bit 08 set) set was received when this condition was not expected.

XX1A - CA Bit 09 Set

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word was received with bit 12 (CA status bit 09 set) set when not expected.

XX1B Input Acknowledge Failure

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word was received with bit 01 (CA Acknowledge Failure, Input) set.

XX1C - Output Acknowledge Failure

Format is the same as XX12 error format.

Explanation - This error indicates that a CA interrupt word was received with bit 00 (CA Acknowledge Failure, Output) set.

XX1E - Unexpected Real Time Interrupt

A	Q	A	Q	A	Q	A	Q
48X8	STJP	XX1E	RRRR	AAAA	INST	INST	INST

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

AAAA = Address of Error Detecting Routine

INST = 1748-2 status resulting in the error. There may be more than one status reported here.

Explanation - This error results when an interrupt is received from the 1748-2 and the status contains one or more unexpected interrupt status bits set (bits 02, 04, 05, 09, and 10). These bits correspond to Word Mode Interrupt (02), Scan Failure Interrupt This Unit (04), Scan Failure Interrupt Other Unit (05), Input Acknowledge Failure Lockout (09), and Program Protect Fault (10).

XX1F - CA Timed Out

Format is the same as XX12 error format.

Explanation - This error results when the expected sequence of events does not occur within a given amount of time. Evaluation of the control words, CA operational status, and CA interrupt word will indicate the cause of the error. The expected sequence of events for a CA in a buffered data subtest is Character Request Enabled, Output Buffer Terminated, and Input Buffer Terminated. In word mode data subtests (01 through 06) the timeout is used to terminate the subtest since no buffer terminates are available and the CA operational status will not have bits 15 and 14 set.

XX20 - Scan Failure, This Unit

A	Q	A	Q	A	Q
4838	STJP	XX20	RRRR	AAAA	BBBB

STJP - Stop/Jump

XX-- = Subtest Number

RRRR = Return Address

AAAA = Address of Error Detecting Routine

BBBB = 1748-2 status involved with error

Explanation - This error results when an interrupt is received from the 1748-2 and the status has bit 04 (Scan Failure, This Unit) set. Once this error is detected the program will attempt to re-start the scanner and will remain in this loop until the scanner starts or the program is halted. This loop may be used as a troubleshooting aid by setting the stop/jump bit to eliminate typeouts.

XX21 - External Reject On Status, Start Scan Routine

Format is the same as XX20 error format.

Explanation - This error results when an external reject is received while attempting to input status from the 1748-2. The status reported in this error may or may not be valid due to the nature of the error.

XX22 - Internal Reject On Status, Start Scan Routine

Format is the same as XX20 error format.

Explanation - This error results when an internal reject is received while attempting to input status from the 1748-2. The status reported in this error may or may not be valid due to the nature of the error.

XX23 - External Reject On Start Scan Function ($B)

Format is the same as XX20 error format.

Explanation - This error results when an external reject is received while trying to output a Start Scan function ($B). The status reported in this error may or may not be valid due to the nature of the error.

XX24 - Internal Reject On Start Scan Function ($B)

Format is the same as XX20 error format.

Explanation - This error results when an internal reject is received while trying to output a Start Scan function ($B). The status reported in this error may or may not be valid due to the nature of the error.

XX30 - Can Not Clear CA Address Register

Format is the same as XX12 error format.

Explanation - This error results after an attempt to enable character request for the indicated CA address has failed. If No End of Operation interrupt is received and the busy status bit does not drop after five passes through the program, a clear CA Address Register function is issued to the 1748-2. If the busy status bit does not drop, the error is reported and the test is terminated.

XX31 - CA Address Register Busy, Could Clear

Format is the same as XX12 error format.

Explanation - This error results after an attempt to enable Character Request has failed. When busy status does not clear, a Clear CA Address Register function is issued to the 1748-2. If busy status is cleared by this function an XX31 error is reported; if not, an XX30 error is reported.

XX32 - External Reject On Status Request

Format is the same as XX12 error format.

Explanation - This error results when an external reject is received on a status request while trying to enable Character Request for the indicated CA address. Activity during the indicated subtest is terminated for this CA address.

XX33 - Internal Reject On Status Request

Format is the same as XX12 error format.

Explanation - This error results when an internal reject is received on a status request while trying to enable Character Request for the indicated CA address. Activity during the indicated subtest is terminated for this CA address.

XX34 - Internal Reject On Function

Format is the same as XX12 error format.

Explanation - This error results when an internal reject is received while trying to issue a Set or Clear CA Address Register function. Further activity on the CA is terminated for the indicated subtest.

XX35 - External Reject On Function

Format is the same as XX12 error format.

Explanation - This error results when an external reject is received while trying to issue a Set or Clear CA Address Register function. Further activity on the CA is terminated for the indicated subtest.

XX36 - No End of Operation Status Bit Received (A08)

Format is the same as XX12 error format.

Explanation - This error results when No End of Operation status bit (A08) is received after an attempt to enable Character Request for the indicated CA address. This error is not reported until five passes have been made through the program waiting for busy status to drop and for the End of Operation interrupt status to be received.

XX37 - Data Verify Error

A	Q	A	Q	A	Q	A	Q	A	Q	A	Q	A	Q
4908	STJP	XX37	RRRR	EERR	AAAA	BBBB	ICW1	ICW2	OCW1	OCW2	OPST		
INDT	INDT	INDT	INDT	INDT	INDT	INDT	INDT	INDT	INDT	OTDT	OTDT		
OTDT	OTDT	OTDT	OTDT	OTDT	OTDT	OTDT	OTDT						

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = CA Parameter A (A register entry)

BBBB = CA Parameter Q (Q register entry)

ICW1 = Input Control Word One (when available)

ICW2 = Input Control Word Two (when available)

OCW1 = Output Control Word One (when available)

OCW2 = Output Control Word Two (when available)

OPST = CA Operational Status where:

Bit 00 = Character Request Enabled for CA

Bit 14 = Output Buffer Terminate Int. Received

Bit 15 = Input Buffer Terminate Int. Received

INDT = Input Data Buffer

OTDT = Output Data Buffer

Explanation - This error results when the input data does not correspond to the output data. Before execution of the subtest the complement of the output data is stored in the input data buffer. Ten character transfers are performed during each buffered data subtest regardless of the submode (character or word). The complete data buffer is displayed during this error, so the subtest number must be referenced to determine the input and output mode. Buffered word mode will equal ten data buffer locations for ten character transfers where buffered character mode will equal five data buffer locations for ten character transfers. The input data on a buffered word mode input will contain status bits (bits 08 through 11) when available from the CA.

XX38 - CA Control Side Status Error

A	Q	A	Q	A	Q	A	Q	A	Q	A
4888	STJP	XX38	RRRR	EERR	AAAA	BBBB	ICW1	ICW2	OCW1	OCW2
	OPST	CCCC	DDDD	0000	EEEE					

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = CA Parameter A (A register entry)

BBBB = CA Parameter Q (Q register entry)

ICW1 = Input Control Word One (when available)

ICW2 = Input Control Word Two (when available)

OCW1 = Output Control Word One (when available)

OCW2 = Output Control Word Two (when available)

OPST = CA Operational Status where:

Bit 00 = Character Request Enabled for CA

Bit 14 = Output Buffer Terminate Int. Received.

Bit 15 = Input Buffer Terminate Int. Received

CCCC = First Expected CA Status (control side)

DDDD = First CA Status Received (control side)

OOOO = Second Expected CA Status

EEEE = Second CA Status Received (control side)

Explanation - This error results when either the first CA status received contains bits indicating an error condition or when a second and unexpected CA status is received. When each dual address CA is set up for a subtest, a two word input buffer is enabled for the control side of the CA. One status request is output to the CA and only one status input is expected. The normal state of the control side at completion of a subtest would be output buffer terminated and input buffer not terminated (CA operational status equal to 4001_{16}). Any deviation from this state results in the error.

0040 - CA Type Undefined

A	Q	A	Q	A	Q	A	Q
4848	STJP	0040	RRRR	EERR	AAAA	BBBB	0000

STJP = Stop/Jump Parameter

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = CA Parameter A (A register entry)

BBBB = CA Parameter Q (Q register entry)

0000 = Always zeros

Explanation - This error results during CA parameter entry if the type entered for the indicated CA is not defined in the CA type table in the program. Program control is returned to the beginning of CA parameter entry.

0041 - Parity Selection Error

Format is the same as 0040 error format.

Explanation - This error results when the parity selected for the indicated CA is an illegal parity condition. Program control is returned to the beginning of CA parameter entry.

0042 - Bit 15 of the Q Parameter Word Not Zero

Format is the same as 0040 error format.

Explanation - This error results when bit 15 of the CA parameter entered in the Q register is not zero. Program control is returned to the beginning of CA parameter entry.

0043 - Mode Selection Error

Format is the same as 0040 error format.

Explanation - This error results when the mode selected for the indicated CA is an illegal mode for that CA program control is returned to the beginning of CA parameter entry.

0044 - EOM Selection Error

Format is the same as 0040 error format.

Explanation - This error results when End of Message is selected for a CA that does not have End of Message capability. Program control is returned to the beginning of CA parameter entry.

0045 - Parity Strip Bit Error

Format is the same as 0040 error format.

Explanation - This error results when the parity strip function is selected for a CA that does not have this capability. Program control is returned to the beginning of CA parameter entry.

0046 - Level Selection Error

Format is the same as 0040 error format.

Explanation - This error results when a level has been selected for a CA and the CA is not capable of operating at the level. Program control is returned to the beginning of CA parameter entry.

0047 - Sync Character Selection Error

Format is the same as 0040 error format.

Explanation - This error results when a Sync, Start of Message, or End of Message character has been selected for a CA with non-selectable character or with no character required. Program control is returned to the beginning of CA parameter entry.

004A - CA Address Greater Than Maximum Scan

Format is the same as 0040 error format.

Explanation - This error results when the indicated CA address is greater than the maximum scan address entered in the Q register on the fourth stop of the system parameter entry. Program control is returned to the beginning of CA parameter entry.

004B - Illegal CA Parameter

Format is the same as 0040 error format.

Explanation - This error results when a search for one of the parameters for the indicated CA turns up undefined. Program control is returned to the beginning of CA parameter entry.

XX50 - Internal Reject On Stop Scan Function

A	Q	A	Q	A	Q
4838	STJP	XX50	RRRR	EERR	AAAA

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

EERR = Address of Error Detecting Routines

AAAA = 1748-2 status when error occurred

Explanation - This error occurs when an attempt to issue a Stop Scan function during a 1748-2 function test results in an internal reject.

XX51 - External Reject On Stop Scan

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Stop Scan function during a 1748-2 function test results in an external reject.

XX52 - Internal Reject On Status

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to take status during a 1748-2 function test results in an internal reject.

XX53 - External Reject On Status

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to take status during a 1748-2 function test results in an external reject.

XX54 - Unexpected Status

A	Q	A	Q	A	Q	A	Q
4848	STJP	XX54	RRRR	EERR	AAAA	BBBB	0000

STJP = Stop/Jump Parameter

XX-- = Subtest Number

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = Expected Status Return

BBBB = Status Received

0000 = Always Zeros

Explanation - This error results when the received status does not equal the expected status. This error is detected in the 1748-2 function tests only. Evaluation of the expected and received status as well as the subtest will indicate the error.

XX55 - Int. Reject On Start Scan Function

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Start Scan function during a 1748-2 function test results in an internal reject.

XX56 - Ext. Reject On Start Scan Function

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Start Scan function during a 1748-2 function test results in an external reject.

XX57 - Scan Failure Interrupt Not Received

A	Q	A	Q	A	Q
4838	STJP	XX57	RRRR	EERR	AAAA

STJP = Stop/Jump Parameter

XX57 = Subtest Number and Error Code

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = Zero

Explanation - This error occurs after a Stop Scan function was issued (1748 was scanning) and a sufficient time delay had elapsed.

XX58 - Scan Failure Not Cleared

A	Q	A	Q	A	Q	A	Q
4848	STJP	XX58	RRRR	EERR	AAAA	BBBB	CCCC

STJP = Stop/Jump Parameter

XX58 = Subtest Number and Error Code

RRRR = Return Address

EERR = Address of Error Detecting Routine

AAAA = Expected Status to be Cleared

BBBB = Received Status

CCCC = Zero

Explanation - This error occurs after the following sequence of events:

1. Start Scan Function
2. Stop Scan Function
3. Scan Failure Interrupt
4. Request Interrupt Status

Status was then requested, checked, and found bit 04 (Scan Failure) was still set.

XX59 - Internal Reject On Enable Word Mode Interrupt

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue an Enable Word Mode Interrupt function during a 1748-2 function test results in an internal reject.

XX5A - External Reject On Enable Word Mode Interrupt

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue an Enable Word Mode Interrupt function during a 1748-2 function test results in an external reject.

XX5B - Busy After Clear Address Register

Format is the same as XX58 error format.

Explanation - This error occurs after the following sequence of events:

1. Stop Scan Function
2. Set Address Register (CA-001)
3. Busy Status Checked and Verified
4. Clear Address Register

Status was then requested, checked, and found to have bit 02 (Busy) still set.

XX5C - Internal Reject On Set CA Address Register

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Set CA Address Register function during a 1748-2 function test results in an internal reject.

XX5D - External Reject On Set CA Address Register

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Set CA Address Register function during a 1748-2 function test results in an external reject.

XX5E - Internal Reject On Clear CA Address Register

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Clear CA Address Register function during a 1748-2 function test results in an internal reject.

XX5F - External Reject On Clear CA Address Register

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Clear CA Address Register function during a 1748-2 function test results in an external reject.

XX60 - Internal Reject on Disable Word Mode Interrupt

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Disable Word Mode Interrupt function during a 1748-2 function test results in an internal reject.

XX61 - External Reject on Disable Word Mode Interrupt

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Disable Word Mode Interrupt function during a 1748-2 function test results in an external reject.

XX62 - Word Mode Interrupt Not Received

Format is the same as XX57 error format.

Explanation - This error occurs after the following sequence of events:

1. Start Scan Function
2. Enable Word Mode Interrupt Function

A Word Mode interrupt was not received within the allotted period of time.

XX63 - Word Mode Status Did Not Clear

Format is the same as XX58 error format.

Explanation - This error occurs after the following sequence of events:

1. Start Scan Function
2. Enable Word Mode Interrupt
3. Disable Word Mode Interrupt

A sufficient amount of time had elapsed, status was requested and word mode status bit was set.

XX64 - EOP Status Did Not Clear

Format is the same as XX58 error format.

Explanation - This error occurs after the following sequence of events:

1. Set CA Address Register Function
2. EOP Interrupt Received
3. Interrupt Status Requested

Status was then requested, checked, and found bit 08 (End of Operation) was still set.

XX65 - EOP Interrupt Not Received (CA Zero)

Format is the same as XX57 error format.

Explanation - This error occurs after a Set CA Address Register function with zero in the A register (CA zero) and a sufficient time had elapsed.

XX66 - EOP Interrupt Not Received (CA Max Scan)

Format is the same as XX57 error format.

Explanation - This error occurs after a Set CA Address Register function with maximum CA address (as received from the operator during parameter entry) and a sufficient time had elapsed.

XX67 - Scan Failure This Unit Did Not Clear

Format is the same as XX58 error format.

Explanation - This error occurs after a Start Scan function was issued to the 1748-2, status requested and bit 04 still set.

XX69 - Internal Reject On Single Scan

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Single Scan function during a 1748-2 function test results in an internal reject.

XX6A - External Reject On Single Scan

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Single Scan function during a 1748-2 function test results in an external reject.

XX6B - Internal Reject On Dual Scan

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Dual Scan function during a 1748-2 function test results in an internal reject.

XX6C - External Reject On Dual Scan

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Dual Scan function during a 1748-2 function test results in an external reject.

XX6D - Internal Reject On Clear Lockout and Status

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Clear Lockout function during a 1748-2 function test results in an internal reject.

XX6E - External Reject On Clear Lockout and Status

Format is the same as XX50 error format.

Explanation - This error occurs when an attempt to issue a Clear Lockout function during a 1748-2 function test results in an external reject.

XX6F - Unexpected Interrupt

A	Q	A	Q	A	Q	A	Q
4848	STJP	XX6F	RRRR	EERR	AAAA	BBBB	CCCC

STJP - Stop/Jump Parameter

XX6F - Subtest Number and Error Code

RRRR - Return Address

EERR - Address of Error Detecting Routine

AAAA - CA Address

BBBB - Expected Interrupt Word (not including CA address)

CCCC - Unexpected Interrupt Word

Explanation - This error occurs if an interrupt other than End of Output (bit 14) is detected on the data side of the CA being used in the Adder Test Section.

XX70 - Adder Error

A	Q	A	Q	A	Q	A	Q
4848	STJP	XX70	RRRR	EERR	AAAA	BBBB	CCCC

STJP - Stop/Jump Parameter

XX70 - Subtest Number and Error Code

RRRR - Return Address

EERR - Address of Error Detecting Routine

AAAA - CA Address

BBBB - Expected OBCW-2

CCCC - Received OBCW-2

Explanation - This error occurs when the Output Buffer Control Word 2 of the CA being used did not advance to what was expected during the Adder Test Section.

VII. DESCRIPTION

A. GENERAL

Each test section performed by this program requires a sequence of events determined by the selected section. An example of a typical sequence is:

1. Find a CA to test and determine the type.

2. If it is a single address CA, go to step 8. If it is a dual address CA, find the control side of the CA.

3. Get a data buffer for the control side and set up a two-word input buffer and an output buffer with the required functions.

4. Set up the Buffer Control Words, Input Control Word 2, Output Control Word 2, Input Control Word 1, and Output Control Word 1.

5. Enable Character Request for the control side of the CA.

6. Look for the next CA in the parameter entry table (PETBL) to set up.

7. Set up and start a time out on the control side.

8. If the next CA is a single address CA or the data side of a dual address CA on which the control side has been set up, find a data buffer.

9. Determine the required data pattern and mode of operation.

10. Set up the output data buffer and load the complement of the output data into the input data buffer.

11. Set up the Buffer Control Words as follows:

    Input Control Word 2, Output Control Word 2, Input Control Word 1, Output Control Word 1.

12. Enable Character Request for the CA address just set up.

13. Set up and start a timeout on the CA just set up.

14. Check CA interrupt words for interrupts related to the CAs already set up and enabled. Record the expected interrupts and queue any errors detected.

15. If the proper sequence of interrupts are received and no errors are detected, verify the data.

16. If an error is queued, wait for timeout and report the error. Verify the data.

17. If at any time the data does not verify, report the error.

18. If no errors are detected on the CAs to be run and the CAs operation terminates normally, go on to the next selected test section.

The above sequence of events is controlled by the test executive. When a test section is found to run, all selected CAs are run on that section. No errors are reported or further sections run until all CAs have either terminated normally, timed out, or errored out.

B. SECTION DESCRIPTION

1. Data Subtest 01 - Word Mode, Zeros

   This subtest performs one data output and one data input in the Word mode on all selected CAs. The data pattern is all zeros. Before performing the output, the input storage area contains the complement of the output data. At completion of the data transfer the input data is verified. Any unexpected status, unexpected interrupt, or reject will result in an error.

2. Data Subtest 02 - Word Mode, Ones

   This subtest is the same as Data Subtest 01 with the exception that the data pattern is all ones. The data pattern will contain the number of bits defined by the CA level parameter received during parameter entry.

3. Data Subtest 03 - Word Mode, Checkerboard

   This subtest is the same as Data Subtest 01 with the exception that the data pattern is alternate ones and zeros (checkerboard).

4. Data Subtest 04 - Word Mode, Sliding Zero

   This subtest is the same as Data Subtest 01 with the exception that the data pattern contains all ones with one bit zero. The bit location containing zero is shifted left (end around) one location every time the subtest is run.

5. Data Subtest 05 - Word Mode, Sliding One

   This subtest is the same as Data Subtest 04 with the exception that the data pattern contains all zeros with a single bit location containing a one.

6. Data Subtest 06 - Word Mode, Sliding Checkerboard

   This subtest is the same as Data Subtest 04 with the exception that the data pattern contains alternate ones and zeros.

7. Data Subtest 07 - Buffered, Word Mode, Zeros

   This subtest performs the data transfer in the Buffered Word mode. The buffer contains ten words. The output data pattern is all zeros. The input buffer, before data transfer, contains the complement of the output buffer. Data is verified at completion of the data transfer. Any unexpected status, unexpected interrupt, or reject will result in an error.

8. Data Subtest 08 - Buffered, Word Mode, Ones

   This subtest is the same as Data Subtest 07 with the exception that the data pattern is all ones.

9. Data Subtest 09 - Buffered, Word Mode, Checkerboard

   This subtest is the same as Data Subtest 07 with the exception that the data pattern is alternate ones and zeros.

10. Data Subtest 0A - Buffered, Word Mode, Sliding Zero

    This subtest is the same as Data Subtest 07 with the exception that the data pattern contains all ones with one bit zero. The bit location containing zero is shifted left (end around) one location in each successive data word.

11. Data Subtest 0B - Buffered, Word Mode, Sliding One

    This subtest is the same as Data Subtest 0A with the exception that the data pattern contains all zeros with a single bit location containing a one.

12. Data Subtest 0C - Buffered, Word Mode, Sliding Checkerboard

    This subtest is the same as Data Subtest 0A with the exception that the data pattern contains alternate ones and zeros.

13. Data Subtest 0D - Buffered, Word Out, Character In, Zeros

    This subtest is the same as Data Subtest 07 with the exception that the input transfer is performed in the character sub-mode.

14. Data Subtest 0E - Buffered, Word Out, Character In, Ones

    This subtest is the same as Data Subtest 08 with the exception that the input transfer is performed in the character sub-mode.

15. Data Subtest 0F - Buffered, Word Out, Character In, Checkerboard

    This subtest is the same as Data Subtest 09 with the exception that the input transfer is performed in the character sub-mode.

16. Data Subtest 10 - Buffered, Word Out, Character In, Sliding Zero

    This subtest is the same as Data Subtest 0A with the exception that the input transfer is performed in the character sub-mode.

17. Data Subtest 11 - Buffered, Word Out, Character In, Sliding One

    This subtest is the same as Data Subtest 0B with the exception that the input transfer is performed in the character sub-mode.

18. Data Subtest 12 - Buffered, Word Out, Character In, Sliding Checkerboard

    This subtest is the same as Data Subtest 0C with the exception that the input transfer is performed in the character sub-mode.

19. Data Subtest 13 - Buffered, Character Out, Word In, Zero

    This subtest is the same as Data Subtest 07 with the exception that the output transfer is performed in the character sub-mode.

20. Data Subtest 14 - Buffered, Character Out, Word In, Ones

    This subtest is the same as Data Subtest 08 with the exception that the output transfer is performed in the character sub-mode.

21. Data Subtest 15 - Buffered, Character Out, Word In, Checkerboard

    This subtest is the same as Data Subtest 09 with the exception that the output transfer is performed in the character sub-mode.

22. Data Subtest 16 - Buffered, Character Out, Word In, Sliding Zero

    This subtest is the same as Data Subtest 0A with the exception that the output transfer is performed in the character sub-mode.

23. Data Subtest 17 - Buffered, Character Out, Word In, Sliding One

    This subtest is the same as Data Subtest 0B with the exception that the output transfer is performed in the character sub-mode.

24. Data Subtest 18 - Buffered Character Out, Word In, Sliding Checkboard

    This subtest is the same as Data Subtest 0C with the exception that the output transfer is performed in the character sub-mode.

25. Data Subtest 19 - Buffered, Character Out, Character In, Zeros

    This subtest is the same as Data Subtest 07 with the exception that the output and input transfers are performed in the character sub-mode.

26. Data Subtest 1A - Buffered, Character Out, Character In, Ones

    This subtest is the same as Data Subtest 08 with the exception that the output and input transfers are performed in the character sub-mode.

27. Data Subtest 1B - Buffered, Character Out, Character In, Checkerboard

This subtest is the same as Data Subtest 09 with the exception that the output and input transfers are performed in the character sub-mode.

28. Data Subtest 1C - Buffered, Character Out, Character In, Sliding Zero

This subtest is the same as Data Subtest 0A with the exception that the output and input transfers are performed in the character sub-mode.

29. Data Subtest 1D - Buffered, Character Out, Character In, Sliding One

This subtest is the same as Data Subtest 0B with the exception that the output and input transfers are performed in the character sub-mode.

30. Data Subtest 1E - Buffered, Character Out, Character In, Sliding Checkerboard

This subtest is the same as Data Subtest 0C with the exception that the output and input transfers are performed in the character sub-mode.

31. Subtest 41 - Start/Stop Scan

This subtest is a 1748-2 MC function test that verifies acceptance by the 1748-2 MC of the Start and Stop Scan functions. No attempt is made in this subtest to verify that the 1748-2 MC is scanning. Scanner operation is verified in subtest No. 45 (End of Operation Interrupt). Subtest 41 checks for rejects, unexpected status, or unexpected interrupts caused by issuing a Start or Stop Scan function.

32. Subtest 42 - Status, Clear Interrupt and Status

This subtest is a 1748-2 MC function test that verifies operation of the Status function and the Clear Interrupt and Status function. A Scan Failure interrupt is caused by issuing Start Scan function and then a Stop Scan function to the 1748-2 MC. Status is then requested three times to ensure that the interrupt is not cleared. A Clear Interrupt and Status function is then issued to clear the Scan Failure interrupt. Status is again taken to make sure that the interrupt was cleared. Any reject, unexpected status or unexpected interrupt will cause an error.

33. Subtest 43 - Set/Clear CA Address Register

This subtest is a 1748-2 MC function test that verifies operation of the Set CA Address Register and Clear CA Address Register functions. CA

Address 001 is sent to the 1748-2 MC along with a Set CA Address Register function. The 1748-2 is checked for Busy status. A Clear CA Address Register function is issued to the 1748-2 MC and status is checked for Not Busy. Any unexpected status, interrupt or reject will result in an error.

34. Subtest 44 - Word Mode Interrupt

This 1748-2 MC function test checks operation of the Word Mode Interrupt. Start Scan and Start Word Mode Interrupt functions are issued to the 1748-2 MC. If periodic Word Mode Interrupts are not received from the 1748-2 MC, an error is reported. If the interrupts are received, Stop Scan and Stop Word Mode Interrupt functions are issued to the 1748-2 MC. No further Word Mode Interrupts should be received. Any reject, unexpected status or unexpected interrupt, will result in an error.

35. Subtest 45 - End of Operation Interrupt

This 1748-2 MC function test verifies operation of the scanner and checks the End of Operation Interrupt. The scanner is started and the CA Address register is cleared. CA address 000 is issued and the 1748-2 MC is checked for Busy status and End of Operation Interrupt. If the interrupt is not received and/or the Busy status does not clear, an error is reported. If the End of Operation interrupt is received and the 1748-2 MC goes Not Busy, the CA address equal to the maximum scan setting is issued. The maximum scan setting is a parameter received during parameter entry which indicates the last or highest CA address to be generated by the 1748-2 MC and expansion network (MUMOD's and/or MUMIX's). If an End of Operation interrupt is not received and/or Busy status does not drop, an error is reported. Any reject, unexpected status or unexpected interrupt, will result in an error report.

36. Subtest 46 - Scan Failure Interrupt

This 1748-2 MC function test checks the Scan Failure this Unit Interrupt. Status is first checked for Not Scanning other Unit Set. The scanner is started and status is checked for bit 4 clear (Scan Failure this Unit). The scanner is stopped, a Scan Failure Interrupt this Unit is expected, error code 57 is reported if not received. Any unexpected interrupt, unexpected status, or reject will also result in an error.

37. Subtest 47 - Busy Check

This 1748-2 MC function test verifies operation of the Busy status. The CA Address register is cleared, CA address 000 is issued, and the 1748-2 MC is checked for Busy status. If Busy the CA Address register is cleared and the 1748-2 MC is checked for Not Busy. CA address 000 is issued again and Busy is checked. The scanner is then started, CA address equal to the Maximum Scan setting plus one is issued to the 1748-2 MC and Busy is checked. If the 1748-2 MC remains Busy, the CA Address register is cleared and Not Busy status is checked. Any reject, unexpected status, unexpected interrupt, or any variation from the expected will result in an error.

38. Subtest 48 - Program Protect Fault

This 1748-2 MC function test checks the Program Protect Fault Status bit. It is assumed that the 1748-2 MC and the console PROGRAM PROTECT switch is in the OFF or UNPROTECTED position. The test will issue three clear Interrupt and Status functions with the program protect bit clear and then three clear Interrupt and Status functions with the program protect bit set. With the PROGRAM PROTECT switch OFF, no Program Protect faults should be detected. This test may be selected by itself and run with the 1748-2 MC and the console PROGRAM PROTECT switch ON. In this situation three SMM 02 errors should be generated for the three unprotected Clear Interrupt and Status functions. Any unexpected status, unexpected interrupt, or reject will also result in an error.

NOTE

If SLS is set, a stop will be performed at the location Program Protect was detected. If SLS is left off, this stop will not occur and SMM will display the error.

39. Subtest 49 - Single Scan, Dual Scan

This 1748-2 MC function test verifies operation of the Single Scan and Dual Scan functions in a communications system operating in the single scan mode. Single Scan functions and Dual Scan functions are issued to the 1748-2 MC. It is assumed the DMU is not connected to the 1748, an external reject will then be expected on Dual Scan function. Any unexpected status, unexpected interrupt, or reject will also result in an error.

40. Subtest 4A - Clear Lockout and Status

This 1748-2 MC function test issues Clear Lockout and Status functions. Any unexpected interrupt, unexpected status, or reject will result in an error.

41. Subtest 4B - Adder Test

This subtest sends one buffered word in such a way that the adder when incremented by one will carry to the next bit. For example:

a. 1000 to 1001, 1001 to 1002, etc.

b. 17FF to 1800, 0FFF to 1000, etc.

The output buffer terminate interrupt is checked. If an unexpected interrupt is received, error code 6F is displayed. The OBCW-2 is then checked to verify it incremented properly. If not, error code 70 is displayed to the operator.

VIII. APPLICATIONS

A. WORST CASE SITUATIONS

Due to the limited hardware availability, no worst case situations have been determined.

B. HUNG CONDITIONS

This test will go into a loop condition when a Scan Failure this Unit (XX20) error is detected. Upon detection of this error, the test will attempt to restart the scanner until the error condition is cleared or until the program is restarted.

C. FAILING LOOPS

When it is desired to loop on an error condition, the following steps are recommended:

1. Determine the CA address and test section that are failing.
2. Halt the program with the SELECTIVE SKIP switch, Master Clear, and restart the program at P=0602.
3. Set the Omit Typeout bit (bit 08) in the Q register Stop/Jump word.
4. Go through System Parameter entry to the third stop, subtest selection, and select only the test causing the error.

5. Go to the fifth System Parameter Stop and set the A register to a 1 if a single address CA is failing or to 2 if a dual address CA is failing.

NOTE

The control side of a dual address CA can be selected by itself just as a single address CA.

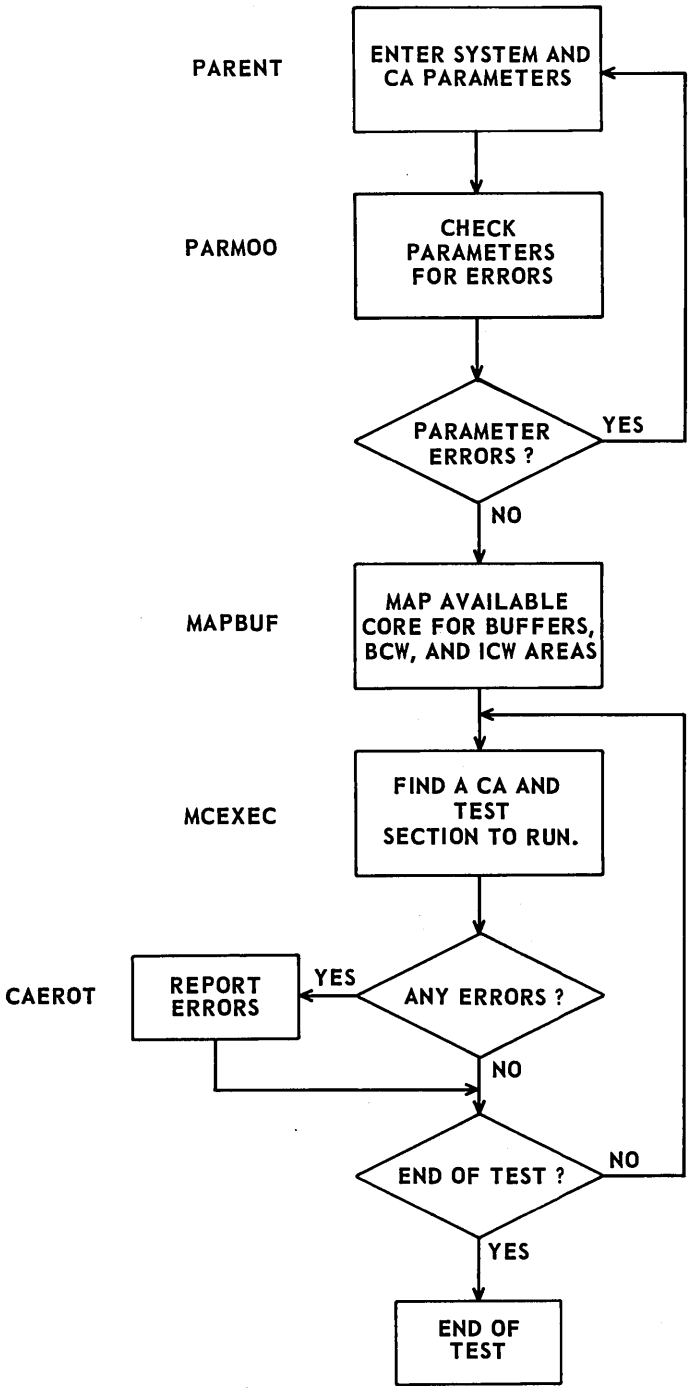
6. Continue on to CA parameter entry and enter the required parameters for the failing CA.

7. Placing the program in execution now will produce a loop with one CA and one test section selected.

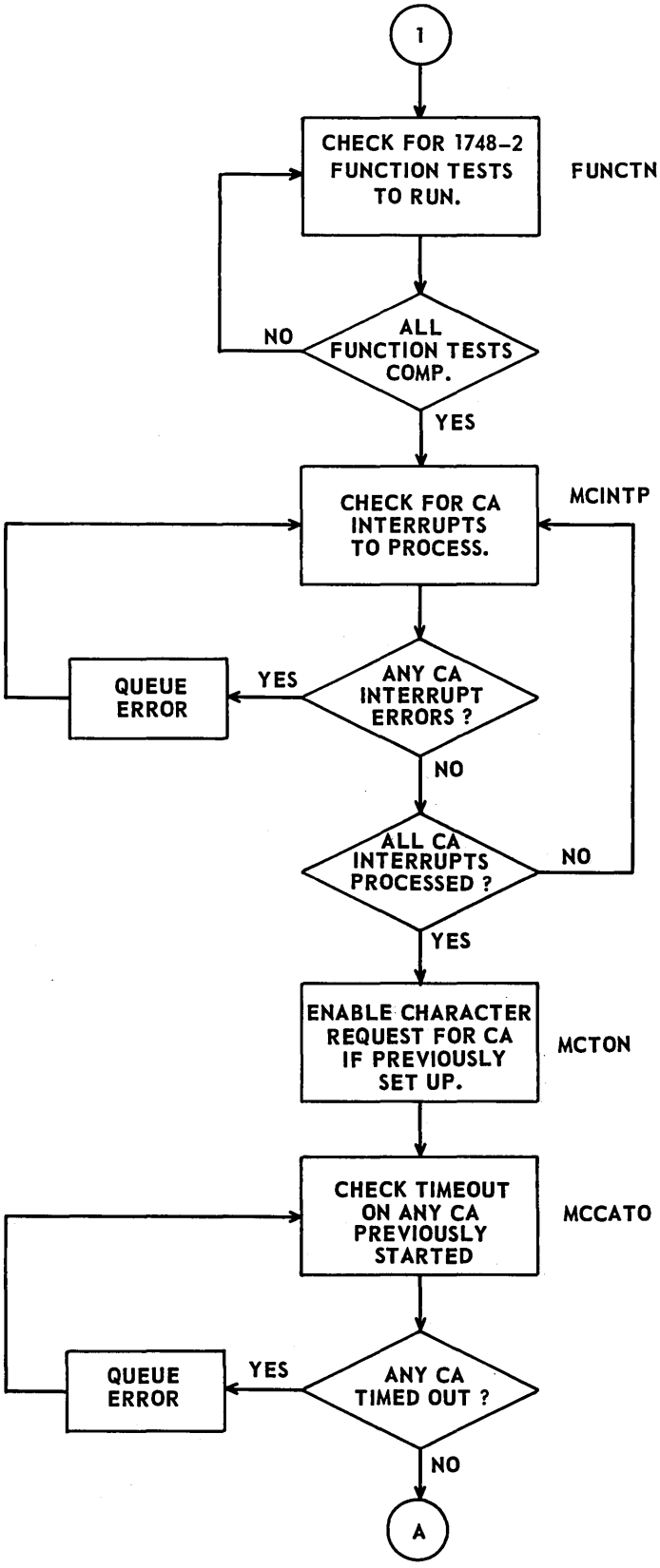
8. To return to normal program execution, return the parameters changed in steps 3 through 6 above, to their original values.

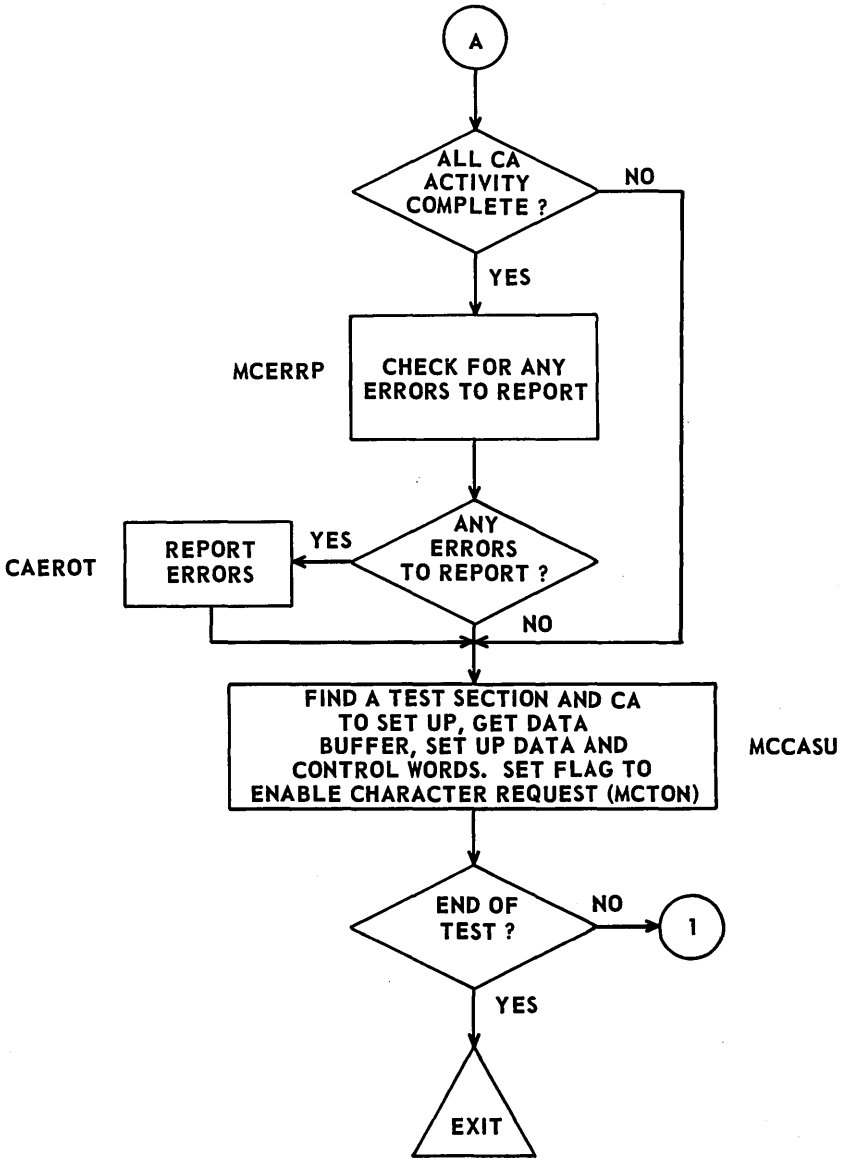
IX. FLOW CHARTS

GENERAL FLOW



TYPICAL SECTION EXECUTION (MCEXEC)




A
ALL CA ACTIVITY COMPLETE ?
NO
YES
MCERRP
CHECK FOR ANY ERRORS TO REPORT
ANY ERRORS TO REPORT ?
YES
CAEROT
REPORT ERRORS
NO
FIND A TEST SECTION AND CA TO SET UP, GET DATA BUFFER, SET UP DATA AND CONTROL WORDS. SET FLAG TO ENABLE CHARACTER REQUEST (MCTON)
MCCASU
END OF TEST ?
NO
1
YES
EXIT

DJ814A A/Q COMMUNICATIONS MULTIPLEXER (NUMOD)
(AQMA36 TEST NO. 36)
(CP = 2F)

I. IDENTIFICATION

A. EQUIPMENT TESTED

DJ814A Communications Multiplexer (NUMOD)
DJ142A, DJ143A Communications Adapter (SACA)
DJ144A Communications Adapter (SCA-1)
DJ145A Communications Adapter (SCA-2)
DJ122A Communications Adapter (ACA)
DJ146A Automatic Call Control Unit (ACUCA)

II. INTRODUCTION

The 17X4 NUMOD/CA Diagnostic test is a "stand alone" test written under the control of the SMM17 Diagnostic Monitor.

The diagnostic checks the function, status, and data handling capability of the DJ814A A/Q Multiplexer (NUMOD) and the associated communications adapters (SACA, ACA, SCA-1, SCA-2, ACUCA) through the use of individually selectable sections. Up to 8 single address communication adapters (CAs) or any combination of single and dual address CAs, not to exceed 8 addresses, may be tested at one time.

The NUMOD subtest, ACUCA test, and the CA subtest are not executed simultaneously. If the ACUCA test is selected for execution (see NUMOD parameters, Third Stop), only this test is executed. At the completion of the ACUCA test, parameters must be reloaded strating with 2.b. Second Stop. If the NUMOD subtest is selected with a CA subtest (see NUMOD Parameters, Second Stop), the NUMOD test runs to completion prior to initiating a CA subtest.

If "loop on test" is selected, the diagnostic will only loop on that portion (NUMOD test or CA test) of the diagnostic that is currently in execution.

A. SPECIAL FEATURES

Bit 15 of the Stop/Jump parameter is used to eliminate end of test displays and end of subtest halts. Only error messages will be displayed.

B. PROGRAM RESTRICTIONS

This diagnostic program will not simultaneously test multiple NUMOD's. Each program execution will test only one NUMOD with its associated CAs.

C. CAUTION TO USERS

Bits 2 and 3 of the SMM parameter word must specify the correct machine type.

The test is a clock interrupt driven diagnostic, requiring the clock to interrupt at a constant rate. Since all program timing (delays, CA data processing, etc.) is a function of the NUMOD interrupt clock, care must be taken to enter the correct clock setting during parameter entry (see Section IV.B.2.c).

The NUMOD clock can be adjusted in the range of 100 microseconds to 100 milliseconds. However, since the combined interrupt processors of SMM and the NUMOD test require from 98 microseconds to 116.8 microseconds, the diagnostic will not function if the clock is set between 98 microseconds and 117 microseconds. Furthermore, if the clock is set in the 100 microsecond to 400 microsecond range (shorting block setting W5 and W10), the diagnostic will spend up to 3/10 of the time in the interrupt processor.

Subtest 7 (Clear Test mode) must not be selected if the modem is strapped for constant carrier. An error code OA will be displayed. The error results from the fact that the Clear Test Mode function will not select resync unless carrier is down.

Section 9 should not be selected for execution when running with an ACA.

Teletype must be in non-interrupt mode (bit 5 of SMM parameter word) for proper execution of the test.

III. REQUIREMENTS

A. HARDWARE

1. Minimum Configuration

One 17X4 Mainframe
One 17X8 Storage Increment
One 17X5 Interrupt Data Channel
One Interrupt Line Required

2. Core Requirements

The minimum amount of core required is 8K.

3. Peripheral Requirements

One standard SMM17 input device

1721/1722 Paper Tape Reader
1728/1729 Card Reader Controller
1726 Card Reader (405) Controller
1712/1713 Teletypewriter
1731/1732 Magnetic Tape Controller
1738 Disk Pack Controller
8000 Tape Drives

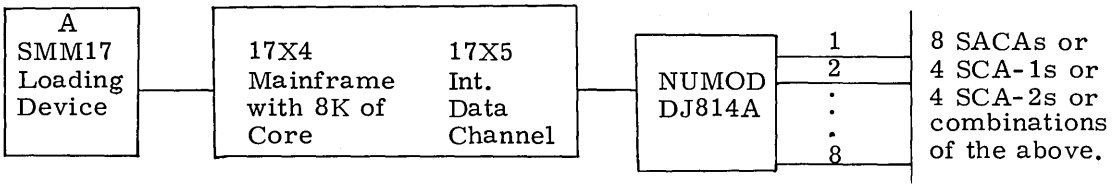
One NUMOD Communications Multiplexer

4. Maximum Configuration

All items referenced in the above paragraph, plus expansion of the CAs to the following limits:

Eight SACAs, or
Four SCA-1s, or SCA-2s, or
Combinations of SCA-1, SCA-2, and SACAs (SCA-1, ACA, and SCA-2 requires two addresses per CA, SACA requires one address per CA).

5. Equipment Configuration



B. SOFTWARE

1. Environment

The diagnostic program operates under control of the SMM17 Monitor in the teletypewriter non-interrupt mode. The monitor and the test require parameters which can either be supplied each time the test is initiated or the test can execute with a prestored set of parameters.

2. External References

The diagnostic test makes reference to the monitor-based subroutines and tables. Linkages are through low core via equates. These equates are incorporated in the diagnostic test.

IV. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The diagnostic is loaded using the standard SMM17 Monitor Test loading procedure.

B. PARAMETERS

Prestore parameter location for NUMOD Test

CATOTS + 0	First CA Parameter	First Stop	(A)	0F3D
CATOTS + 1			(Q)	0F3E
CATOTS + 2		Second Stop	(A)	0F3F
CATOTS + 3			(Q)	0F40
CATOTS + 4	Second CA Parameter	First Stop	(A)	0F41
CATOTS + 5			(Q)	0F42
CATOTS + 6		Second Stop	(A)	0F43
CATOTS + 7			(Q)	0F44
CATOTS + 8	Third CA Parameter	First Stop	(A)	0F45
CATOTS + 9			(Q)	0F46
CATOTS + A		Second Stop	(A)	0F47
CATOTS + B			(Q)	0F48
CATOTS + C	Fourth CA Parameter	First Stop	(A)	0F49
CATOTS + D			(Q)	0F4A
CATOTS + E		Second Stop	(A)	0F4B
CATOTS + F			(Q)	0F4C

CATOTS + 10	Fifth CA Parameter	First Stop	(A)	0F4D
CATOTS + 11			(Q)	0F4E
CATOTS + 12		Second Stop	(A)	0F4F
CATOTS + 13			(Q)	0F50
CATOTS + 14	Sixth CA Parameter	First Stop	(A)	0F51
CATOTS + 15			(Q)	0F52
CATOTS + 16		Second Stop	(A)	0F53
CATOTS + 17			(Q)	0F54
CATOTS + 18	Seventh CA Parameter	First Stop	(A)	0F55
CATOTS + 19			(Q)	0F56
CATOTS + 1A		Second Stop	(A)	0F57
CATOTS + 1B			(Q)	0F58
CATOTS + 1C	Eighth CA Parameter	First Stop	(A)	0F59
CATOTS + 1D			(Q)	0F5A
CATOTS + 1E		Second Stop	(A)	0F5B
CATOTS + 1F			(Q)	0F5C
ONOINT	Interrupt line number		*	0EF9
CCANUM	Number of CAs to test and NUMOD Test		*	0EFA
CDELAY	NUMOD Interrupts Clock Time		**	0EFB
CEQBAD	Illegal equipment number		**	0EFC

1. Prestored Parameters

   The diagnostic is set to run with a prestored set of parameters. No parameter changes are required if the prestored list of parameters are valid for the CAs being tested.

   The following is a list of the prestored parameters.

   a. NUMOD equipment E.

   b. Interrupt line number 3.

   c. Illegal equipment number 0.

   d. NUMOD subtest selection 0 through 5.

   e. NUMOD clock prestored as $64 (1 millisecond).

---

* 2.b. Second stop (A) (Q) respectively.

** 2.c. Third stop (A) (Q) respectively.

f. Three communications adapters are selected:

1) SCA-1 addresses 0 and 1
2) SACA address 2
3) SCA-2 addresses 4 and 5

g. All CAs set for 8 bits of data.

To alter the prestored parameters, follow the directions stated in SMM17 Reference Manual.

2. NUMOD Parameters (DJ814A)

a. First Stop (overflow light on)

(A) = 3631 - Test ID Stop
(Q) = Stop/Jump Parameter

b. Second Stop

(A) = Interrupt Line assigned to NUMOD
(Q) = WXZZ (prestored as 303F)
where: W = Q (bits 15 through 12) - Number of CAs to be tested
X = Q (bits 11, 10, 9, 7) = 0
(bit 8) - ACUCA Test Selection
ZZ = Q (bit 6 through 0) - NUMOD subtest selection (see Section IV.B.3.c)

c. Third Stop

(A) = (1/10 NUMOD clock setting in microseconds $_{16}$)
Example: Clock set at 16 milliseconds
1) Convert to microseconds $16X1000 = 16,000_{10}$
2) Divide by 10 $16,000 \div 10 = 1600_{10}$
3) Convert to hexadecimal $1600_{10} = 640_{16}$
(Q) = Illegal equipment number (see Section VI.B.1.a.)

NOTE

If the ACUCA test is selected for execution, the next parameter stop will be the ACUCA parameter stop C.(4).

3. CA Parameters

a. SACA, SCA-1, SCA-2, ACA

The following stops (4 through 6) are required if any CAs are to be tested. Two stops are required for each CA. If eight SACAs are to be tested, stops (4 through 6) will be repeated for the last CA to be tested.

1) Fourth Stop (Overflow light on)

(A) = 36Y1 - Test ID Stop

where Y = Twice the number of CAs to be tested +1. Y max = 15 (F)

(Q) = Stop/Jump Parameter

2) Fifth Stop

(A) - CA ID Word

A =

15-13	12	11-10	9-8	7-5	4	3-0

where: A(15-13) - CA Address (even number if a 2 address CA).

A(12) - Mode; SCA's 0 = Universal
1 = ASCII
ACA's 0 = SOM/EOM Not Selected
1 = SOM/EOM Selected
SACA = N/A

A(11-10) - Bits to test; 0=5, 1=6, 2=7, 3=8. 0 or 1 selection illegal for SCA-1, SCA-2.

A(9-8) - Parity (SCAs and ACA only);
00 = No Parity
01 (bit 8) = Even Parity
10 (bit 9) = Odd Parity
11 (bits 8, 9) = Illegal Selection

A(7-5) - Not Used

A(4) - EOM (SCAs ACA only); 0 = EOM Not Selected
1 = EOM Selected

A(3-0) - CA type; 4 = SACA
D = ACA
E = SCA-1
F = SCA-2

Q(15-8) = EOM only character (ACA)

Q(7-0) = SOM only character (ACA)
SYNC only character (SCA-1, SCA-2)

3) Sixth Stop

(A) = Subtest Selection, Subtests 0 through 0F
SACA has only 12 (bits 0 through 11) subtests

Q(15-8) = Selectable Data Pattern for CA Test (ACA, SCA's subtest 11, SACA subtest B)

Q(07-04) = 0

Q(03-00) = Subtest Selection, Subtests 10 through 13 (used only for ACA and SCA's)

If a bit is set, the corresponding subtest will be selected.

For example, A(9) = Subtest 9; Q(1) = Subtest 11, etc.

Return to CA parameter for each CA selected - Step 2 (fifth stop)

4) ACUCA Parameter Stop (ONE) A=FFF

(Q) = 801 (ACU) Abandon Call Retry Time-out

000A = 7 second time-out

000E = 10 second time-out

0014 = 15 second time-out

0020 = 25 second time-out

0030 = 40 second time-out

A(2-0) = ACUCA Address

A(15-3) = Not Used

(1) Next ACUCA Stops A = 0000 Q = (digit count)

A(3-0) = Dial Digits (max. 10 digits)

A(14-4) = Not Used

A(15) = Setting of this bit indicates all numbers have been entered, ACUCA testing begins.

NOTE

If the ACUCA has the capability of detecting the EON code, to place the associated data set in data mode, this number "C" must be entered after the last dial digit.

C. SECTION DESCRIPTION INDEX

1. NUMOD Test

Test No.	Name	Page	Run Time
00	Internal, External Reject Subtest		
01	Status Subtest		
02	Clear Controller Subtest		
03	Clear Interrupt Subtest		
04	Clock Interrupt Request Subtest		
05	Multiple Function Subtest		
06	NUMOD Protect Subtest		
		Total Run Time	

2. SACA Test

Test No.	Name	Page	Run Time
00	Disable CA Function Subtest		
01	Enable CA Function Subtest		
02	Clear Break Subtest		
03	Set Break Subtest		
04	Lost Previous Character Subtest		
05	Zero Data Pattern Subtest		
06	Ones Data Pattern Subtest		
07	Alternate ones Data Pattern Subtest		
08	Alternate Zero Data Pattern Subtest		
09	Sliding Zero Data Pattern Subtest		
0A	Sliding Ones Data Pattern Subtest		
0B	Operator Select Data Pattern Subtest		
		Total Run Time	

3. SCA-1, SCA-2, ACA Test

Test No.	Name	Page	Run Time
00	Enable CA (Control Channel) Subtest		
01	Select Test Mode Subtest		
02	Enable CA (Data Channel) Subtest		
03	Disable CA (Control Channel) Subtest		
04	Disable CA (Data Channel) Subtest		
05	Program Clear Subtest		
06	Status Request Subtest		
07	Clear Test Mode Subtest		
08	Character Ready Subtest		
09	Parity Error Subtest (SCA's only)		
0A	Character Lost Subtest		
0B	Zero Data Pattern Subtest		
0C	Ones Data Pattern Subtest		
0D	Alternate Ones Data Pattern Subtest		
0E	Alternate Zeros Data Pattern Subtest		
0F	Sliding Zero Data Pattern Subtest		
10	Sliding Ones Data Pattern Subtest		
11	Operator Select Data Pattern Subtest		
12	Data Message Subtest		
13	ASCII Pattern Subtest SCA-2 Transparent Mode		
		Total Run Time	

4. ACUCA Test

00 Dial a phone and check status.

V. OPERATOR COMMUNICATION

A. MESSAGE FORMATS

1. Normal Program Typeout

a. DJ814 Test Identification during initialization

```
AQMA36, NUMOD/C.A. Test
CP2F, VER. 3.1
IA = XXXX, FC = XX
```

b. End of Test

A	Q	A	Q
3624	Stop/Jump Parameter	Pass Number	Return Address

2. Error Message

All Error Message displays use the standard SMM17 Error message format:

A	Q	A*	Q	A Q . . . A Q
36X8	Stop/Jump Parameter	Subtest/ Error	Return Address	(See individual Error message)

X = Number of AQ Displays

3. Loop On Subtest Halt

A	Q	A	Q
3622	Stop/Jump Parameter	Subtest/ Device	Return Address

4. Loop On Test Display

A	Q	A	Q
3624	Stop/Jump Parameter	Pass Number	Return Address

5. Operator Intervention Halt (NUMOD Subtest 06)

A	Q	A	Q
3621	Stop/Jump Parameter	0001 (set NUMOD PROTECT and P.P. switches)	0806
3621	Stop/Jump Parameter	0002 (clear NUMOD PROTECT and P.P. switches)	0806

*FFXX is typed if an error occurs while in Interrupt mode, where XX is the error number.

B. MESSAGE DICTIONARY

1. Parameter Entry Errors (Device 09)

Error Code	Message	Page No.
01	EQUIPMENT NUMBER NOT LEGAL	
02	INTERRUPT LINE NUMBER ERROR	
03	NO NUMOD SECTIONS SELECTED AND NO CAs SELECTED TO TEST	
04	ILLEGAL NUMBER OF CAs TO TEST	
05	ILLEGAL CA TYPE SELECTED	
06	ILLEGAL CA ADDRESS FOR DUAL ADDRESS CA	
07	NOT USED	
08	CA ADDRESS PREVIOUSLY USED	
09	NO SUBTESTS FOR THE SELECTED CAs	
0A	ILLEGAL PARITY SELECTION	
0B	BIT SELECTION FOR SCA-1, SCA-2 ILLEGAL	

2. NUMOD Errors (Device 08)

Error Code	Message	Page No.
01	NO EXPECTED INTERNAL REJECT	
02	NO EXPECTED EXTERNAL REJECT	
03	NO INTERRUPT RECEIVED WHEN EXPECTED	
04	PROTECT FAULT	
05	NUMOD STATUS ERROR	
06	NO INTERRUPT DURING CA TESTING	
07	INPUT OR OUTPUT REJECTED	

3. Interrupt Mode Error (Subtest Portion Of Display = FF)

Error Code	Message	Page No.
05	NUMOD STATUS ERROR	
07	INPUT OR OUTPUT REJECTED	

4. SACA Errors (Device Is CA Address In Error)

Error Code	Message	Page No.
01 through 03	NOT USED	
04	ENABLE CA ERROR	
05	DISABLE CA ERROR	
06	NOT USED	

Error Code	Message	Page No.
07	INPUT OR OUTPUT REJECTED	
08 through 0C	NOT USED	
0D	CA INPUT DATA ERROR	

5. SCA-1, SCA-2, ACA Errors (Device Is CA Address In Error)

Error Code	Message	Page No.
01	ENABLE CA (CONTROL CHANNEL) ERROR	
02	NOT USED	
03	SELECT TEST MODE ERROR	
04	ENABLE CA (DATA CHANNEL) ERROR	
05	DISABLE CA (DATA CHANNEL) ERROR	
06	PROGRAM CLEAR ERROR	
07	INPUT OR OUTPUT REJECTED	
08	DISABLE CA (CONTROL CHANNEL) ERROR	
09	STATUS REQUEST ERROR	
0A	CLEAR TEST MODE ERROR	
0B	NOT USED	
0C	CHARACTER READY ERROR	
0D	CA DATA INPUT ERROR	
0E	CHARACTER PARITY ERROR	
0F	CHARACTER LOST	
10	EOM ERROR	
11	CONTROL CHANNEL PARITY ERROR	
12	CONTROL CHANNEL STATUS ERROR	

C. ERROR DESCRIPTIONS

1. Parameter Entry Errors

If a parameter error is detected during the parameter entry phase of the diagnostic, parameters will be requested again depending upon where the error occurred. If the error occurred in the NUMOD parameter section (stops 1 through 3), all parameter requests will be made. If an error occurred in the CA parameter section (stops 4 through 6), only stops 4 through 6 will be repeated.

Error Code	Description
01	Equipment number not legal, for example, W field not zero, Director bit zero. A = 0009_{16} (device in error) Q = Equipment number supplied
02	Interrupt line no. error for example, multiple lines selected or line 0 selected. A = 0009_{16} (device in error) Q = Interrupt line no. selected
03	No NUMOD sections selected and no CAs selected to test. See Section IV.B.2.6 contents of Q register. A = 0009_{16} (device in error). Q (15-12) = Number of CAs to test Q (11-7) = 0 Q (6-0) = NUMOD section number
04	Illegal number of CAs selected to be tested. Selection greater than 8. A = 0009_{16} (device in error) Q = CAs to test/NUMOD subtests, see Q register of error 03
05	Illegal CA type. A = 0009_{16} (device in error) Q = CA ID word, see Section IV.B.3.a.2)
06	Illegal CA address for example, odd address for a dual address CA. A = 0009_{16} (device in error) Q = CA ID word, see Section IV.B.3.a.2)
07	Not used.
08	CA address previously used. A = 0009_{16} (device in error) Q = CA ID word, see Section IV.B.3.a.2)
09	No sections (subtests) selected for the selected CA. Section selection is by CA type. The first CA initialized for each type (SACA, SCA-1, SCA-2, ACA, ACUCA) must have the subtests selection.
0A	Illegal parity selection. Parity bits 8 through 9 selected together. A = 0009_{16} (device in error) Q = CA ID word, see Section IV.B.3.a.2)

Error Code	Description
0B	Bit selection for SCA-1 or SCA-2 illegal SCA-1 and SCA-2 must be selected for either 7 or 8 bits. A = 0009_{16} (device in error) Q = CA ID word, see Section IV.B.3.a.2)

2. NUMOD Errors

Error Code	Description
01	No expected internal reject. Illegal equipment no. (see Section VI.B.1.a) supplied during parameter entry does not cause a reject. A = 0008 (device in error) Q = Illegal equipment no. used
02	No expected external reject. Each CA address is sent a data word, since the CAs have not been enabled, each CA should reject the output. A = 0008 (device in error) Q = CA address (0 through 7)
03	No interrupt received. NUMOD functioned to interrupt, however, no interrupt was received within the selected time. A = 0008 (device in error) Q = Function issued A = Interrupt line no. Q = 0000
04	Protect fault, no external reject. NUMOD subtest 06 is the protect test, a clear interrupt function is issued with the NUMOD protected, the 1700 protect switch set, and the instructions unprotected. An external reject was expected but not received. A = 0008 (device in error) Q = Q at time of output A = A at time of output Q = 0000
05	NUMOD Status error. A = 0008 (device in error) Q = Expected status A = Received status Q = 0000

Error Code	Description
06	No Interrupts during CA testing. A = 0008 (device in error) Q = Interrupt line no. (see Section H.C.)
07	Input or output rejected. A = 0008 (device in error) Q = (Q) at reject Q(0-11) = Q at reject Q(12) = External reject - input Q(13) = Internal reject - input Q(14) = External reject - output Q(15) = Internal reject - output A = (A) at reject Q = 0000

3. Interrupt Mode Errors

The subtest portion of the error display (A(15-8) of 2nd stop) will contain FF in the upper 8 bits, indicating that the error occurred while in the interrupt processor.

Error Code	Description
05	NUMOD Status Error (see above Section error no. 15).
07	Input or Output Rejected (see above Section error no. 07).

4. SACA Errors

The device word for all CAs is the address of the erroring CA in the NUMOD. The type of CA is identified by its address.

Error Code	Description
01 through 03	Not used.
04	Enable CA error. CA bit 10 not set after character request (enable CA) function sent to CA. A = 0000 to 0007 (device in error) Q = Expected CA data (12 bits) A = Received CA data (12 bits) Q = 0000
05	Disable CA error. CA bit 10 not clear after disable character request (disable CA) function sent to CA. A = 0000 to 0007 (device in error) Q = Expected CA data (12 bits) A = Received CA data (12 bits) Q = 0000

Error Code	Description
06	Not used.
07	Input or output rejected (see Section V. C. 2 error no. 07).
08 through 0C	Not used.
0D	CA input data error. Data received from the CA was not as expected. A = 0000 to 0007 (device in error) Q = Expected CA data (12 bits) A = Received CA data (12 bits) Q = Sent CA data (12 bits)

5. SCA-1, SCA-2, ACA Errors

The device word for all CAs is the address of the erroring CA on the NUMOD. The type of CA is identified by its address.

Error Code	Description
01	Enable CA (control channel) error CA status word bit 10 (function request) not set after enable CA function to CA. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = 0000
02	Not used.
03	Select Test Mode error. CA status word bit 0 (test mode) not set aftet Select Test Mode function to CA. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA function word (12 bits)
04	Enable CA (data channel) error. CA data word bit 10 (character request) not set after enable CA function to CA. A = Even no. 0000 through 0006 (device in error) Q = Expected CA data word (12 bits) A = Received CA data word (12 bits) Q = 0000

Error Code	Description
05	Disable CA (data channel) error. CA data word bit 10 (character request) not cleared after disable CA function to CA. A = Even no. 0000 through 0006 (device in error) Q = Expected CA data word (12 bits) A = Received CA data word (12 bits) Q = 0000
06	Program Clear error. CA status word not cleared after program Clear function to the CA. Only bits 11, 10, 9, 8, 7, 1, 0 are checked; of these, only bit 1 should be set. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA function word (12 bits)
07	Input or output reject. A = 0000 through 0007 (device in error) (Remainder of display see Section V.C.2 error no. 07).
08	Disable CA (control channel) error. CA status word bit 10 (function request) not cleared after disable function to CA. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = 0000
09	Status Request error. CA status word bit 11 (status ready) not as expected. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA function word (12 bits)
0A	Clear Test Mode error. CA status word bit 0 (Test mode) not cleared after Clear Test Mode function to CA. A = Odd no. 0001 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA function word (12 bits)
0B	Not used.

Error Code	Description
0C	Character Ready error. CA data word bit 11 (character ready) not set after transmission of data word to CA. A = Even no. 0000 through 0006 (device in error) Q = Expected CA data word (12 bits) A = Received CA data word (12 bits) Q = Sent CA data word (8 bits)
0D	CA Data Input error. Data received from the CA was not as expected. A = Even no. 0000 through 0006 (device in error) Q = Expected CA data (12 bits) A = Received CA data (12 bits) Q = Sent CA data (8 bits)
0E	Character Parity error. Data parity bit not set after forced parity error (test 9). A = Odd no. 0000 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA data (8 bits)
0F	Character Lost error. CA data word bit 9 (character lost) not as expected.
10	EOM (bit 8 data word) error bit 8 not as expected. A = 0000 through 0006 (device in error) Q = Expected CA data (12 bits) A = Received CA data (12 bits) Q = Sent CA data (8 bits) or 000, if waiting for EOM
11	Control Channel Parity error bit 9 not as expected. A = 0000 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = 0000
12	Control Channel Status error. CA status word bit 9 (parity error) is set after ETB/ETX is received. A = 0000 through 0007 (device in error) Q = Expected CA status word (12 bits) A = Received CA status word (12 bits) Q = Sent CA data (8 bits)

VI. DESCRIPTION

A. GENERAL

The diagnostic is divided into two main parts; the NUMOD tests and the CA tests. The CA tests are further divided into CA type tests, with the single address CAs (ACUCA, SACA), and the dual address CAs (ACA, SCA-1, SCA-2), using different test coding but using common coding for: Control, Parameter Entry, Interrupt Processing, Input and Output, Error Messages, End of Subtest, End of test repeating, and Elapses timing.

Control is returned to the test executive after any successful output, any successful input, data verification at the end of a subtest, and after any error messages.

The ACUCA test is a go - no go test. If an error is detected, the test will automatically repeat the condition; errors are not reported in SMM format. At the end of the test, with the SLS set, the test will stop with (Q) = FFFF. At this time the operator can repeat the test by placing the computer in run, or can start NUMOD/CA testing by setting P = IA and reentering parameters without the ACUCA test bit selected.

If an error occurs and "Loop on Error" is selected, the current subtest being executed will enter the shortest loop possible to again generate the error.

B. TEST DESCRIPTION

1. NUMOD Test

The diagnostic is designed so that the NUMOD test, if selected, is executed prior to any of the CA tests being initiated. The NUMOD test is divided into seven subtests (00 through 06). Subtests 00 through 05 are part of the prestored parameter list.

a. Subtest 00 - Internal External Reject Subtest

This subtest is responsible to check that a reject does occur when an illegal I/O operation is performed. Internal reject is generated by outputting to an equipment not on the system. The illegal equipment no. is supplied during parameter entry. The equipment number is prestored as equipment zero. External rejects are generated by outputting to each CA address. Since the CA has not been enabled an external reject should occur for each address.

b. Subtest 01 - Status Subtest

This subtest is responsible to check that no reject occurs when a status request is made. No attempt is made to validate the status clock bit or the protect bit. The clock bit is validated each time an interrupt occurs and the protect feature is validated by subtest 06.

c. Subtest 02 - Clear Controller Subtest

This subtest is responsible for functioning the NUMOD to clear controller, checking if a reject occurs. Clear controller function is used in subtest 00 to ensure that all the CAs are disabled.

d. Subtest 03 - Clear Interrupt Subtest

This subtest is responsible for functioning the NUMOD to clear the interrupt. A check is made to ensure that no reject has occurred.

e. Subtest 04 - Clock Interrupt Request Subtest

This subtest is responsible for functioning the NUMOD to request an interrupt. A check is made to ensure that no reject has occurred, that an interrupt does occur within the specified time (taken in as a parameter), and that the clock status bit is set when an interrupt occurs.

f. Subtest 05 - Multiple Function Subtest

This subtest is responsible to function the NUMOD with all the combinations of multiple functions (3, 5, 6, 7) to ensure that no rejects occur. Those requesting the clock interrupt (5, 6, 7) are checked for interrupts, and that the interrupt status bit (3) is set.

g. Subtest 06 - NUMOD Protect Subtest

This subtest is responsible to function the NUMOD when the equipment is protected. A Reject signal should occur. The operator is asked, at the appropriate times, to set and clear the NUMOD PROTECT switch and the 1700 PROGRAM PROTECT switch. See Section V.A.4.

2. Single Address CA (SACA) Test

The SACA test is designed to test from one to eight SACAs simultaneously. Subtests 00 through 0B are part of the prestored parameter list. Each SACA to be tested must be set (manually) in test mode and connected for Full Duplex operation. Subtests 01 through 0B are checked to ensure that no rejects occur. All subtests check all the status bits (8, 9, 10, 11) to ensure they are set or clear as required.

a. Subtest 00 - Disable CA Function Subtest

This subtest is responsible to function each selected SACA and determine if a reject occurred. Bit 10 of the input is checked to ensure that it is clear.

b. Subtest 01 - Enable CA Function Subtest

This subtest is responsible to function each selected SACA and determine if a reject occurred. Bit 10 of the input is checked to ensure that it is set.

c. Subtest 02 - Clear Break Subtest

This subtest is responsible to function each selected SACA with a Clear Break, checking for a reject and bit 8 clear.

d. Subtest 03 - Set Break Subtest

This subtest is responsible to function each selected SACA and determine if a reject occurred. Bit 8 of the input is checked to ensure that it is set. A Clear Break function is issued each time an SACA is tested.

e. Subtest 04 - Lost Previous Character Subtest

This subtest is responsible to output two data characters and input only the second data character; checking that the lost character bit (9) is set and that the data bits (0 through 7) contain the second data character sent out, checking for a reject after each I/O operation.

The following subtests (05 through 0B) are SACA data pattern tests. Each subtest used a different data pattern in testing the SACA. Each test, however, functions in the same way.

Data is sent out and then input and verified. The CA Data Status bits (8, 9, 10, 11) are also verified.

f. Subtest 05 - Zero Data Pattern Subtest, Pattern 00_{16}

g. Subtest 06 - Ones Data Pattern Subtest, Pattern FF_{16}

h. Subtest 07 - Alternate Data Pattern Subtest, Pattern AA_{16}

i. Subtest 08 - Alternate Data Pattern Subtest, Pattern 55_{16}

j. Subtest 09 - Slide Zero Data Pattern Subtest, Pattern $FFFE_{16}$, $FFFD_{16}$, $FFFB_{16}$, etc.

k. Subtest 0A - Slide Ones Data Pattern Subtest, Pattern 0001_{16}, 0002_{16}, 0004_{16}, etc.

1. Subtest 0B - Operator Select Data Pattern Subtest. Pattern selected during parameter entry, two hexadecimal digits. Prestored as $C3_{16}$.

3. Subtest Description For SCA-1, SCA-2, and ACA

The SCA-1, SCA-2, ACA (dual address CAs) subtests consist of function tests and data tests. The only significant difference in testing the SCA-1 and SCA-2 is in the data message tests. The SCA-2 has the capability of ASCII Transparent mode. The SCA-1 is not capable of handling ASCII Transparent mode.

The SCA-1, SCA-2, and ACA test is divided into 19 subtests (00 through 12_{16}). Subtest 09 is the forced data parity error test, since it is not possible to force a parity error when testing an ACA, this test is bypassed whenever an ACA is to be tested. The test is bypassed for the ACA, through a software check in Subtest 09.

Subtest 00 through 02 are preselected as part of the prestored parameters. See Section 8.3.24.

At completion of inputs, the received data/status is compared with the expected data/status. Any deviation from that which is expected will result in an error. The SCA-1, SCA-2, ACA subtests are executed in test mode. The following functions are non-testable in test mode, and are not tested by this diagnostic program:

- Resync
- Set Reverse Channel
- Clear Reverse Channel
- Disconnect
- Request Send
- Stop Send

In test mode, the status is not available for the following, and they are not tested by this program.

- Data Terminal Ready
- Carrier On
- Data Set Ready

a. Initialization Routine

The Initialization Routine clears counter and flags, constructs control tables from parameter entry data, determines the number of active SCA-1s, SCA-2s, and ACAs, and performs the initial execution of Subtest 00 - Enable CA (Control Channel), Subtest 01 - Select Test

Mode and Subtest 02 - Enable CA (Data Channel). The initial execution of these subtests ensures that all CAs are capable of being enabled and set in test mode, which is essential for the proper operation of all the subtests. Any rejects or unexpected status will result in an error.

b. Enable CA (Control Channel) Routine

This routine activates the CA control channel when the CA is in a disabled condition upon entry to a subtest. This routine does not test the enabling function. See Subtest 00.

c. Enable CA (Data Channel) Routine

The routine's purpose is to activate the CA data channel when the CA is in a disabled condition upon entry to a subtest. This routine does not test the enabling function. See Subtest 02.

d. Select Test Mode Routine

This routine selects test mode operation when the CA is not in test mode upon entry to a subtest. This routine does not test the Select Test Mode function. See Subtest 01.

e. Subtest 00 - Enable CA (Control Channel)

This subtest is a function test that verifies the activation of the SCA-1 SCA-2, and ACA control channel. Subtest 00 checks for rejects and unexpected status. Any reject or unexpected status will cause an error to be reported. Regardless of subtest selection, this subtest will automatically be executed during the program initialization to establish a test base.

f. Subtest 01 - Select Test Mode

This subtest is a function test that verifies the operation of the SCA-1, SCA-2, and ACA programmable option (Select Test mode) of connecting the transmit logic to the receiver logic. Subtest 01 checks for rejects, failure to effect selection of test mode, and unexpected status. Any reject, function failure, or unexpected status will result in an error. Regardless of subtest selection, this subtest will automatically be executed during the program initialization to establish a test base.

g. Subtest 02 - Enable CA (Data Channel)

This subtest is a function test that verifies the activation of the SCA-1, SCA-2, and ACA data channel. Subtest 02 checks for rejects and unexpected

status. Any reject or unexpected status will result in an error. Regardless of subtest selection, this subtest will automatically be executed during the program initialization to establish a test base.

h. Subtest 03 - Disable CA (Control Channel)

This subtest is a function test that verifies the capability to deactivate the SCA-1, SCA-2, and ACA control channel. Subtest 03 checks for rejects and unexpected status. Any reject or unexpected status will result in an error.

i. Subtest 04 - Disable CA (Data Channel)

This SCA-1, SCA-2, and ACA function test checks the capability to deactivate the data channel. This subtest checks for rejects and unexpected status. Any reject or unexpected status will result in an error.

j. Subtest 05 - Program Clear

This subtest is a function test that verifies the clearing of the control counter and all registers in both the control and data channels of the SCA-1, SCA-2, and ACA. Subtest 05 checks for rejects and unexpected status. Any reject or unexpected status will result in an error.

k. Subtest 06 - Status Request

This subtest is a function test that verifies only the setting of the Status Ready bit in the input status word. The Status Request function is redundant when the SCA-1, SCA-2, and ACA is operating in the NUMOD configuration. Subtest 06 checks for rejects and unexpected status, either of which will result in an error.

l. Subtest 07 - Clear Test Mode

This subtest is a function test that verifies the capability of the SCA-1, SCA-2, and ACA to switch from test mode to the normal operational mode. This subtest checks for rejects and unexpected status. Any rejects or unexpected status will result in an error. See Section H. C.

m. Subtest 08 - Character Ready

This subtest is a function test to verify the capability of the SCA-1, SCA-2, and ACA to indicate the ready status of a character for input to the computer. Subtest 08 checks for rejects and unexpected status. Any rejects or unexpected status will result in an error.

n. Subtest 09 - Parity Error (SCAs Only)

This subtest is a data test that verifies that parity errors will be indicated by the SCA-1/SCA-2 in the event of Character Parity error or an incorrect generation of CRC/LRC. This subtest checks for rejects and unexpected character status. Any rejects or unexpected status will result in an error. $C6 used for odd parity error, and $B9 used for even parity error.

o. Subtest 0A - Character Lost

This subtest is a data test that verifies the correct operation of the SCA-1, SCA-2, and ACA logic which determines and indicates that a character has been lost, as a result of receiving another character prior to the receipt of acknowledgement of the previous character. This subtest checks for rejects and unexpected character status. Any rejects or unexpected status will result in an error.

p. Subtest 0B - Data Pattern, Zeros

This subtest performs one data output and one data input on all selected SCA-1s, SCA-2s, and ACAs. The data pattern is all zeros. At completion of the data transfer the input data is verified. Any reject, unexpected status, or deviation in the data pattern will result in an error.

q. Subtest 0C - Data Pattern, Ones

This subtest is the same as Subtest 0B - Data Pattern, Zeros with the exception that the data pattern is all ones. The data pattern will contain the number of bits defined by the CAs level parameter received during parameter entry.

r. Subtest 0D - Data Pattern, Alternate Zeros and Ones

The subtest is the same as Subtest 0B - Data Pattern, Zeros with the exception that the data pattern is alternate ones and zeros.

s. Subtest 0E - Data Pattern, Alternate Ones and Zeros Complement

This subtest is the complement of Subtest 0D - Data Pattern, Alternate Ones and Zeros

t. Subtest 0F - Data Pattern, Sliding Zero

This subtest is the same as Subtest 0B - Data Pattern, Zeros with the exception that the data pattern contains all ones with one single bit location containing a zero. The bit location containing a zero is shifted

left (end around) one location every time the subtest is run. The subtest is repeated until the zero is shifted end around to its initial starting location.

u. Subtest 10 - Data Pattern, Sliding One

This subtest is the same as Subtest 0F - Sliding Zero with the exception that the data pattern contains a one in the high order position and all zeros with one other bit location containing a one, which is shifted.

v. Subtest 11 - Data Pattern, Selectable Bit Configuration

This subtest is the same as Subtest 0B - Data Pattern Zeros with the exception that the data pattern is selectable by the user during parameter entry. If an SCA is operating in ASCII mode, the following control character hexadecimal may cause multiple errors in this test, therefore, they should not be selected: SOH (0001), STX (0002), ETX (0003), ACK (0006), DLE (0010), NAK (0015), ETB (0017), SYNC (character as plugged).

w. Subtest 12 - Data Message

This subtest consists of a series of data transfers using 13 characters. The SCAs use the same data pattern whether in ASCII mode or Universal mode. The ACA uses the same data pattern whether in SOH/EOM Detection mode or not.

The first and last character are changed, depending whether the CA is an ACA or SCA. When testing an ACA, the parameter supplied SOH and EOM characters are used. When testing an SCA the ASCII SOH (01) and ETX (03) characters are used.

The character stream is designed to test Transparent mode when testing an SCA-2 in ASCII mode. The SCA-1 and ACA do not have the Transparent mode feature.

The following is the data characters stream used for the test:

$01 or SOM	$01 used for SCAs, SOM used for ACA. See Section IV.B.3.1.a.2).		
$46	ASCII	F	
$10	ASCII	DLE	This selects Transparent mode for the SCA-2.
$02	ASCII	STX	
$10	ASCII	DLE	In Transparent mode the first DLE is stripped off by the SCA-2.
$10	ASCII	DLE	

$4A	ASCII	J	
$42	ASCII	B	
$10	ASCII	DLE	This terminates the Transparent mode
$17	ASCII	ETB	
$02	ASCII	STX	
$10	ASCII	DLE	
$10	ASCII	DLE	
$03 or EOM	$03 used for SCAs, EOM used for ACA. See Section IV.B.3.a.2).		

Each character is checked for character parity (if parity selected) and data verify. The parity bit on the control channel is checked after the ETB character and the EXT (03) or EOM character.

When testing an SCA and the character sent is an ETX or ETB, a delay of 5 character times is selected. Whenever the ETX, ETB character is input, bit 8 (EOM), if selected, also received with the data.

When testing an ACA and the character sent is the selectable EOM character, bit 8 (EOM), if selected, is also received with the data.

Any rejects, unexpected status, or deviation in the message data will result in an Error message.

x. Subtest 13 - ASCII Transparent Mode

This subtest is designed to test Transparent mode, when testing an SCA-2 (DJ-145A). The subtest is not executed on an ACA or SCA-1.

In execution of this subtest, the following data block is sent and received.

$01	SOH
$10	DLE
$10	DLE
$1F	ITB
$7F	PAD
$10	DLE
$02	STX

$10	DLE		
$10	DLE	*	SCA-2 is in Transparent mode at this output time.
$58	X		
$50	P		
$41	A		
$52	R		
$10	DLE		
$03	ETX		

*The SCA-2 (DJ145-A) will strip the second DLE of DLE, DLE sequence when in Transparent mode.

The only check made by the subtest to assure the CA is in Transparent mode is that the second DLE character is stripped and parity is not received. If data is not received properly, error code $0D (Input error) is displayed. It is left up to the operator to determine the possible cause when error code 0D (CA Data Input error) is displayed. The last Q display will equal the input count.

EOM Enable should not be selected on the CA when running this test. If selected illegal (10-EOM bit 8 not as expected), errors will be displayed.

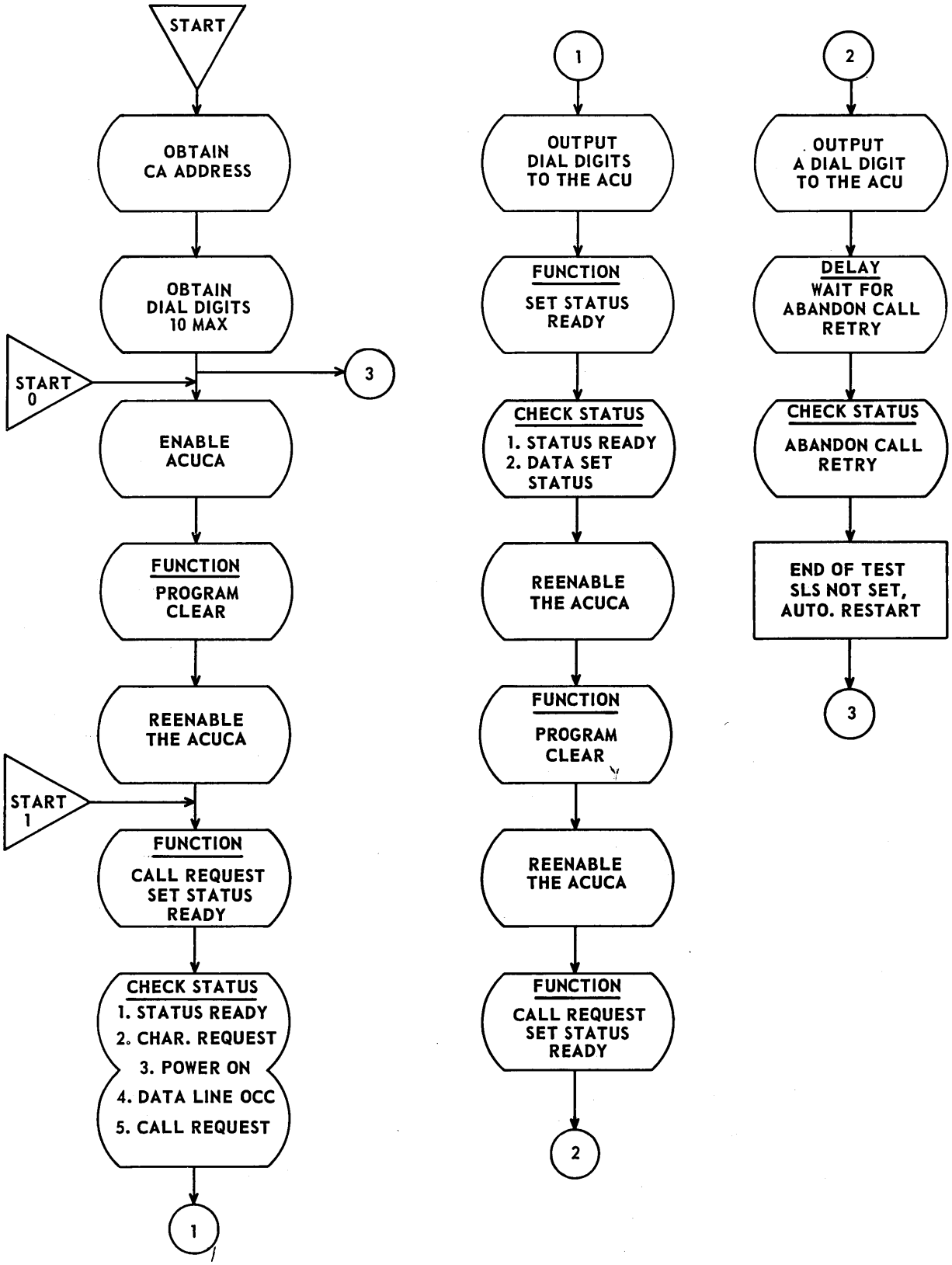
4. ACUCA Test

The ACUCA test is a go-no-go test. If an error is detected, the test will automatically loop. Errors are not reported in SMM17 format. At the end of the test, with SLS set, the test will stop with (Q) = FFFF. At this time the operator can repeat the test by placing the computer in run, or can start NUMOD/CA testing by setting P = 0602 and reentering parameters without the ACUCA test bit selected. If SLS is not set, the test will automatically repeat test. If a status error occurs with the SLS set, the computer will stop with (A) = expected status, (Q) = received status. If the test appears to be hung in a loop, it is suggested the operator determines the cause by the use of SLS (status error), flow chart, and listing. Only one ACUCA is tested at one time.

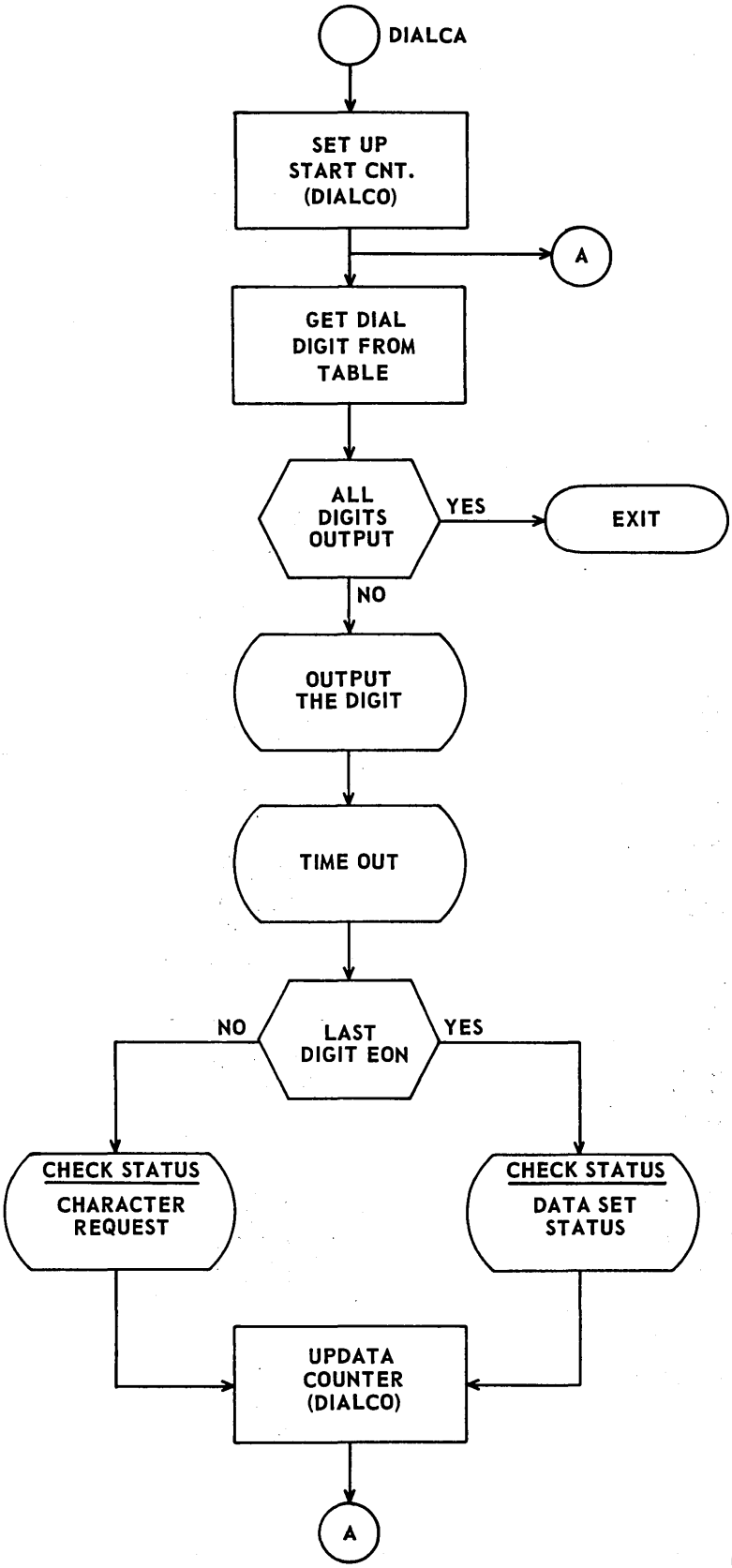
5. Subtest Selection

When two or three types of CAs (SCAs, ACA) are selected to be tested simultaneously, the subtest selection must be identical for all dual address CAs.

ACCUCA FLOW CHART



OUTPUT DIAL DIGITS ROUTINE



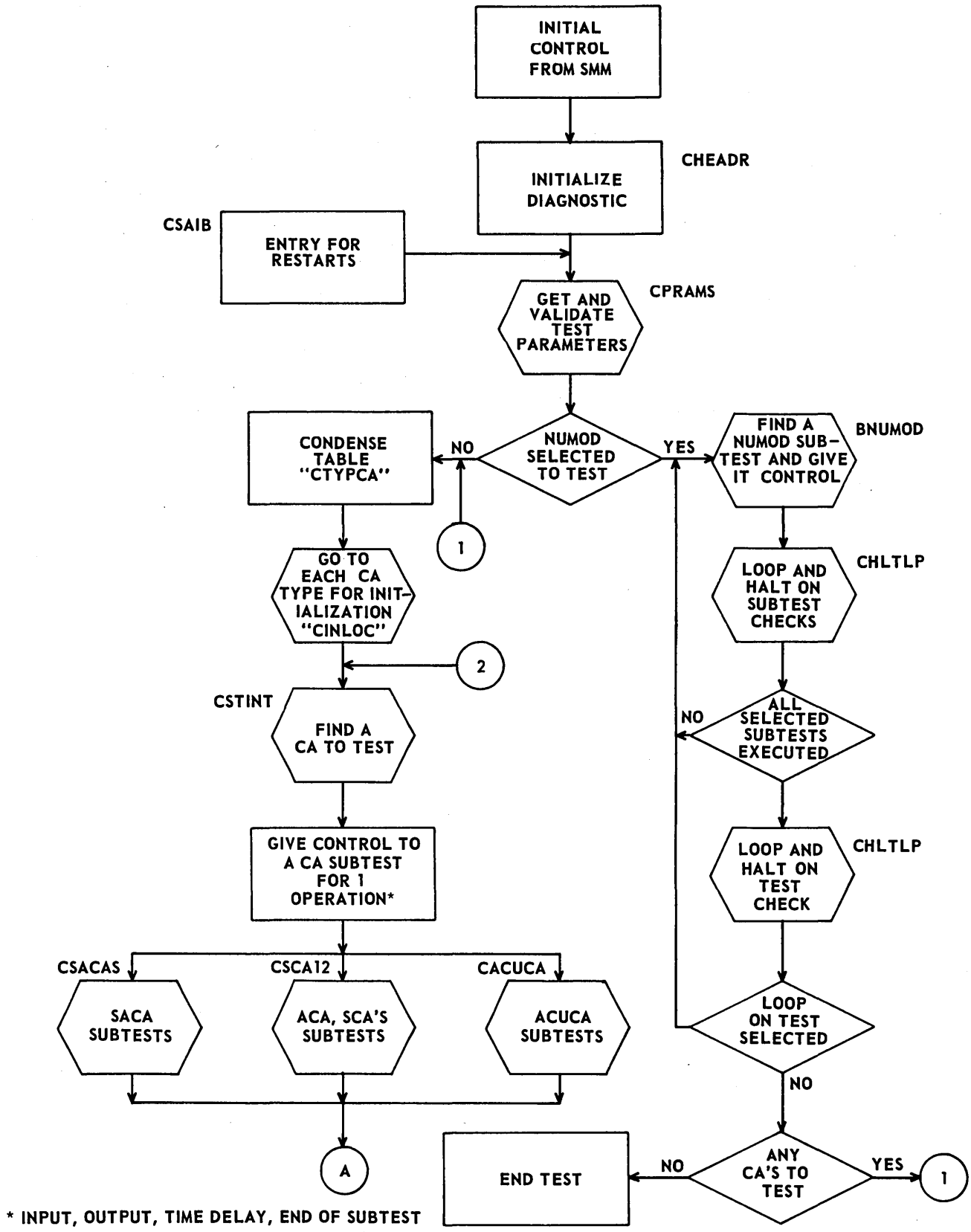
VII. APPLICATIONS

A. WORST CASE SITUATIONS

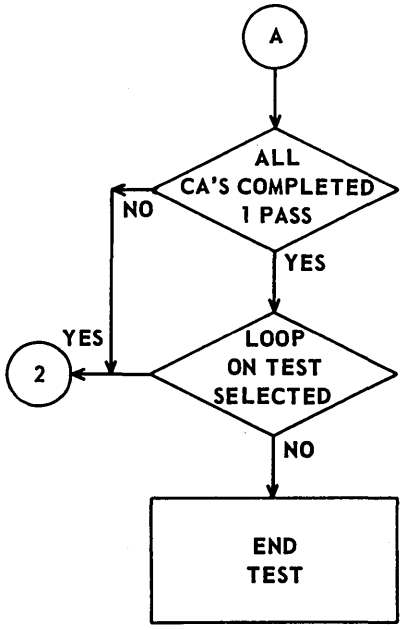
Due to the limited hardware availability, no worst case situations have been determined.

B. HUNG CONDITIONS

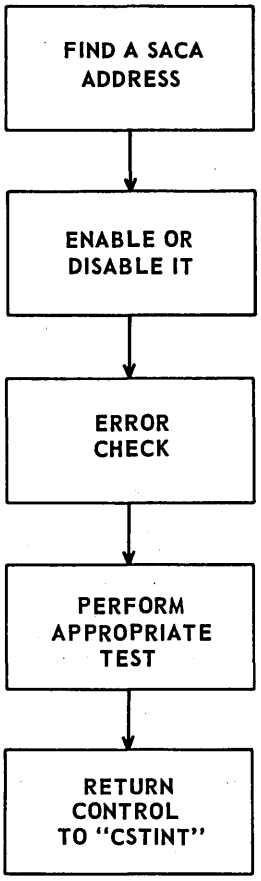
If the diagnostic appears to be hung in a loop while testing NUMOD, location BSTPIK contains the NUMOD subtest number. If the diagnostic appears to be hung in a loop while testing the CAs, two locations should be checked. Location CURTYP contains the CA type last given control (4=SACA, D=ACA, E=SCA-1, F=SCA-2, 0=ACUCA), location CASTA0+1 + (the number of CA types being tested); for example, 2 CAs being tested and CASTO = 1430, 1430+1+2 = 1433. This location contains the subtest number currently in control.



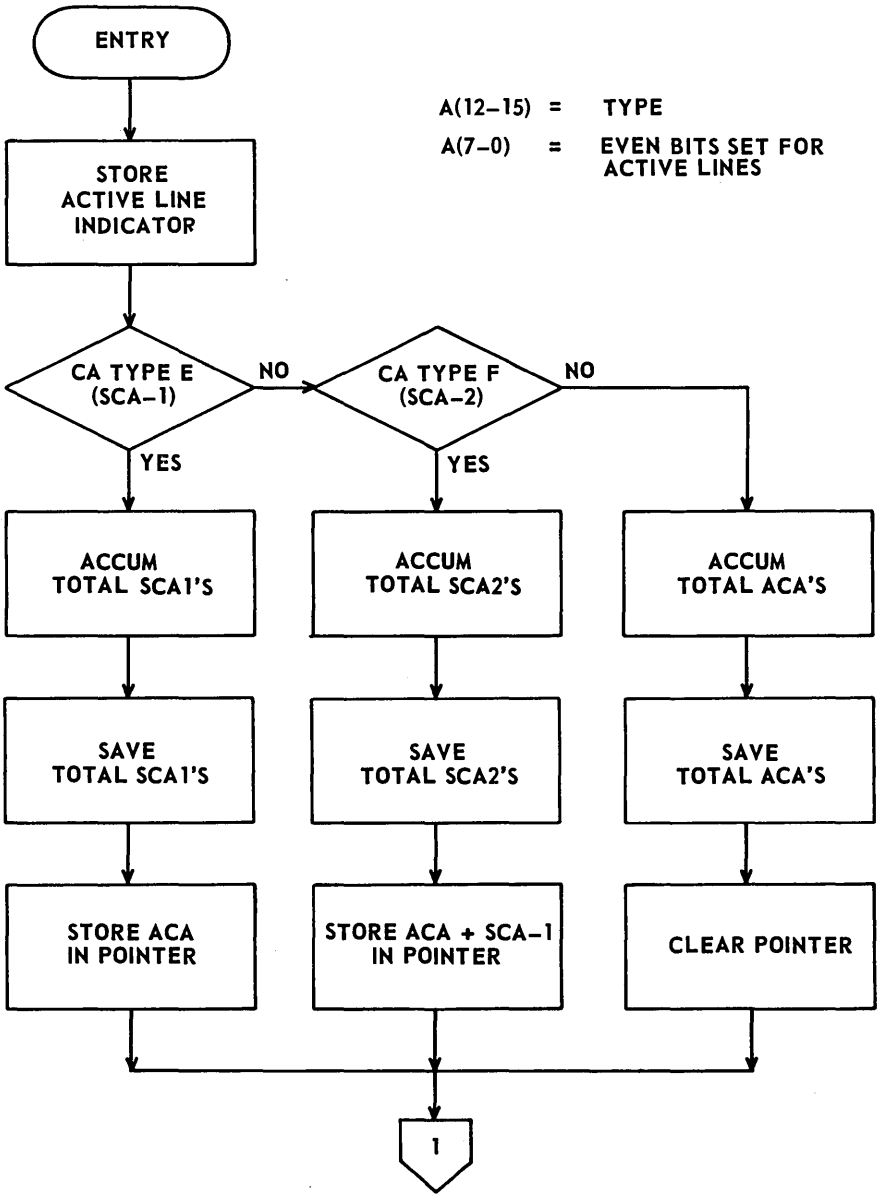
* INPUT, OUTPUT, TIME DELAY, END OF SUBTEST

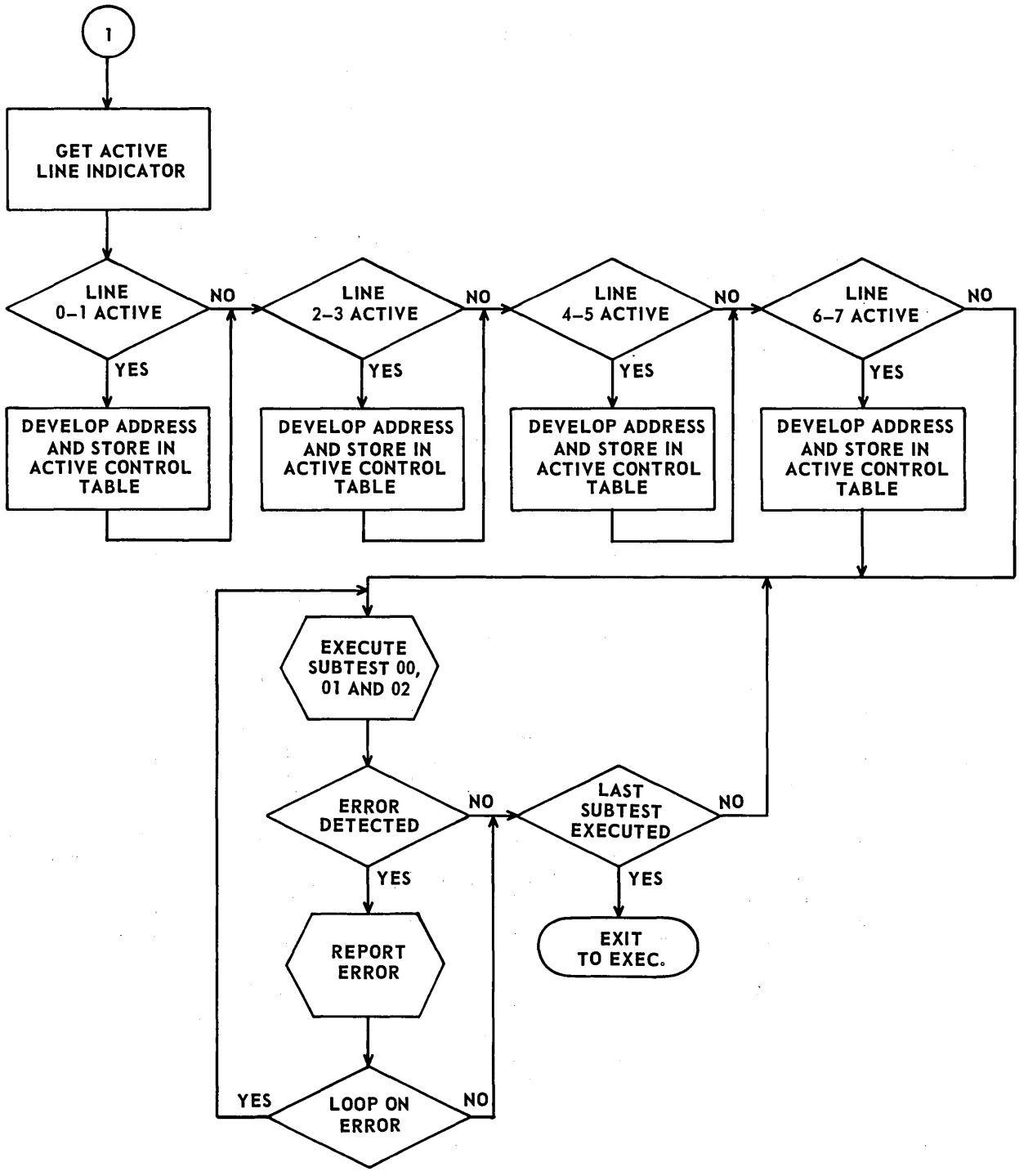

A
ALL
CA'S COMPLETED
1 PASS
NO
YES
YES
2
LOOP
ON TEST
SELECTED
NO
END
TEST

TYPICAL SACA SUBTEST

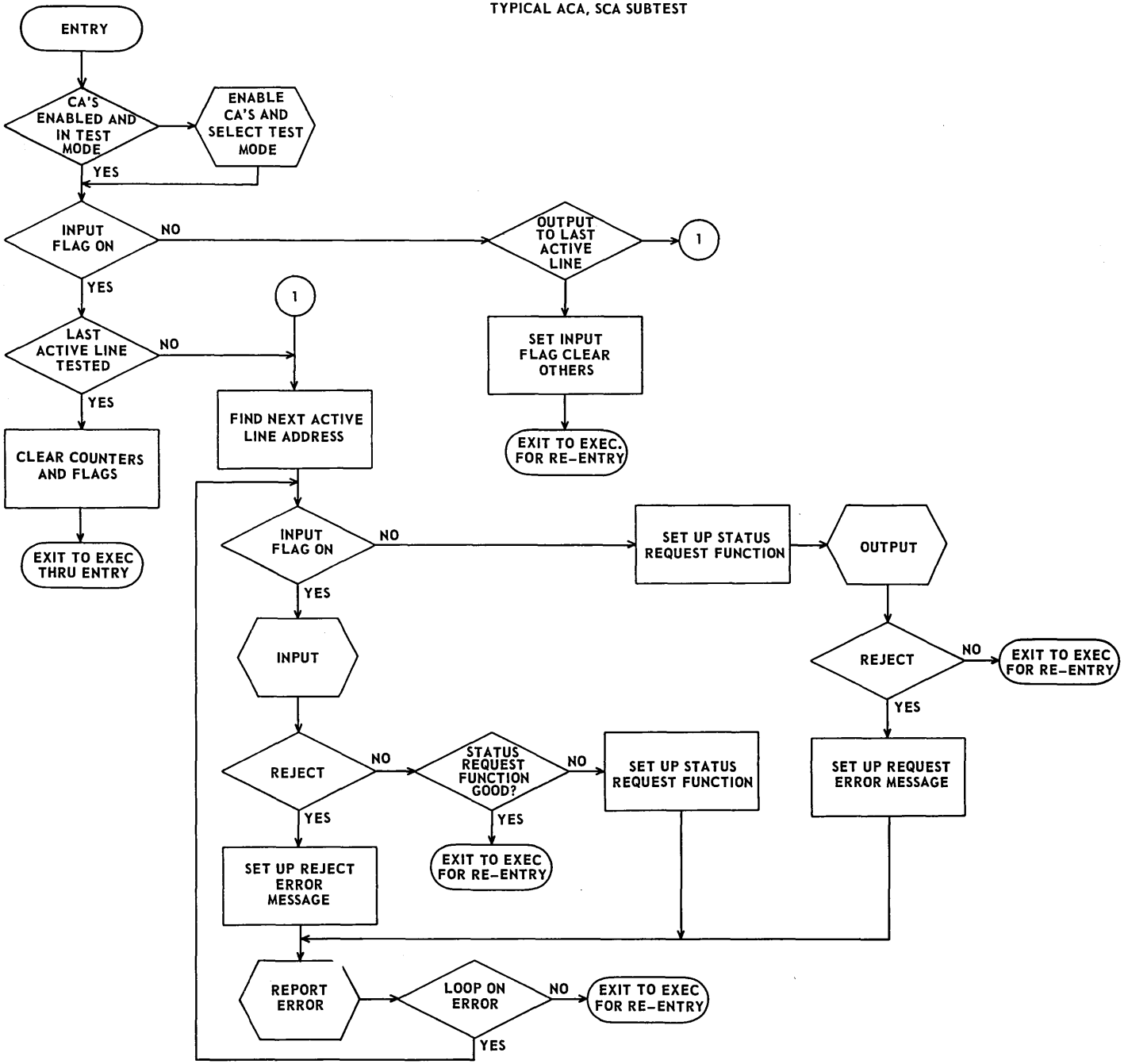


ACA, SCA INITIALIZATION




1
GET ACTIVE LINE INDICATOR
LINE 0–1 ACTIVE
NO
YES
DEVELOP ADDRESS AND STORE IN ACTIVE CONTROL TABLE
LINE 2–3 ACTIVE
NO
YES
DEVELOP ADDRESS AND STORE IN ACTIVE CONTROL TABLE
LINE 4–5 ACTIVE
NO
YES
DEVELOP ADDRESS AND STORE IN ACTIVE CONTROL TABLE
LINE 6–7 ACTIVE
NO
YES
DEVELOP ADDRESS AND STORE IN ACTIVE CONTROL TABLE
EXECUTE SUBTEST 00, 01 AND 02
ERROR DETECTED
NO
YES
REPORT ERROR
LOOP ON ERROR
YES
NO
LAST SUBTEST EXECUTED
NO
YES
EXIT TO EXEC.

TYPICAL ACA, SCA SUBTEST



1743-2 ASYNCHRONOUS COMMUNICATION CONTROLLER TEST
(ACCO86 Test No. 86)

I. OPERATIONAL PROCEDURE

A. REQUIREMENTS

1784-1 or -2 with 8K of memory
1743-2 Asynchronous Controller - DJ815
Distribution panel jumper plug or wires (optional)
CRT or equivalent to run Section 6 - Echo Test (optional)

B. LOADING PROCEDURE

This test loads and executes correctly under SMM17. The calling sequence is specified by the SMM17 system being used. If the equipment address is zero when called, the test will use the prestored equipment address (IA+6).

C. TESTING PROCEDURE

The 1743-2 is tested in various configurations. Self-jumpered channels, channels connected to other channels, and channels connected to an I/O device are tested. The test is interrupt-driven and times out interrupts. It will release control to multiplex with other tests while awaiting an interrupt.

D. PARAMETERS

1. Stop 1

   A1 = 8671 — Test ID (86), seven stops (7), parameter stop (1)
   Q1 = STJP — Test unique Stop/Jump parameter (see TSTJP)

2. Stop 2

   A2 = 00FF — Section Select parameter, bit 2 = Section 2, bit 3 = Section 3 (There are eight sections (0-7).)
   Q2 = 0200 — Interrupt line select (Single bit represents interrupt line.) Example: 0200 = Interrupt line 10.

3. Stop 3

   A3 = 0XXX — Channel 0 selector (see Channel Select Codes)
   Q3 = 1XXX — Channel 1 selection

4. Stop 4

   A4 = 2XXX — Channel 2 selection
   Q4 = 3XXX — Channel 3 selection

5. Stop 5

   A5 = 4XXX Channel 4 selection
   Q5 = 5XXX Channel 5 selection

6. Stop 6

   A6 = 6XXX Channel 6 selection
   Q6 = 7XXX Channel 7 selection

7. Stop 7

   A7 = Special data pattern (If bit 15=1, continuously send out selected character in Section 5.)
   Q7 = Test mode pattern (If set to 0, random data will be used as a test mode pattern.)

8. Channel Select Codes

   If channel word = 0, no modem or test cable is present.
   Format of channel word:

   PCDT

   Where: P = Present channel number (bits 14-12)
   C = Channel number (0-7), connected to present channel if test jumpers are installed (bits 10-8)
   D = Number of data bits/characters (5-8), this channel jumpered for (bits 7-4).
   T = Type of channel connection where (bits 2-0):
   0 = No connection to this channel
   1 = Modem connected to input/output device
   2 = Modem in test mode or channel self-jumpered
   3 = This channel test-jumpered to another channel

   Examples:

   A3 = 0080 Channel 0, eight data bits, no connection
   Q3 = 1081 Channel 1, eight data bits, modem to I/O device
   A4 = 2072 Channel 2, seven data bits, channel self-jumpered
   A5 = 4563 Channel 4, six data bits, test-jumpered to channel 5
   Q5 = 5463 Channel 5, six data bits, test-jumpered to channel 4

NOTE

Since internal hardware limits parameter's selection such as baud rate, data bits, parity, etc. to pairs (0-1, 2-3, 4-5, 6-7), only these pairs should be test-jumpered.

9. TSTJP - Test Stop/Jump parameters

   Q1 bits 0-8 = Same meaning as SMM STJP.

E. STOPS

1. Type 1 - Parameter Entry

   For information on parameters, see Parameters section. This stop will occur if STJP bit 0 is set.

   A1 = 8671
   Q1 = TSTJP (see Parameters)

2. Type 2 - End of Section

   Stop at end of section. This stop will only occur if the test STJP bit 1 is set.

   A1 = 8622 (86) test ID, (2) number of stops, (2) end of section
   Q1 = TSTJP

   A2 = 0S00 (S=section number)
   Q2 = RTA Return address

3. Type 4 - End of Test

   Stop at end of test. This stop will only occur if STJP bit 2 is set.

   A1 = 8624 (86) test ID, (2) number of stops, (4) end of test
   Q1 = TSTJP

   A2 = NNNN (NNNN = number of passes)
   Q2 = RTA Return address

F. WORD MESSAGES

Word messages are available only if there is a TTY or equivalent available. (The following messages are information to the operator.)

1. Initialization of the Test

   ACC086 ASYNCHRONOUS COMMUNICATION CONTROLLER TEST
   CP2F, VER. 3.1-1
   IA = XXXX FC = XX

2. Parameter Selection

   ERROR IN CHANNEL PARAMETER
   This indicates that an error was made in the description of channel configurations. After the message is typed, parameter selection will be re-entered.

3. Echo Section - Section 6

   ACC086 ECHO SECTION - CHARS TYPED ON TEST I/O
   DEV WILL BE ECHOED BACK WHEN RETURN KEY DEPRESSED.
   TYPE (Control E) TO EXIT SECTION.

   This message alerts the operator that it is not actively testing but awaiting characters to echo.

G. ERROR CODES

There is a common error routine; therefore, the error parameters always have the same meanings. A description of the error parameters and codes follow.

1. A = 8658 (test number, number of stops, type of stops)
   Q = Stop/Jump word
2. A = CXZZ (C=channel, X=section, ZZ=error)
   Q = Return address
3. A = Last local I/O routine call address
   Q = Enabled-channels (bit position = 1 = ENBLD)
4. A = Input data/status word
   Q = Clock/protect status word
5. A = Function output (A register)
   Q = Equip/channel output (Q register)
6. A = Bad data word (if appropriate)
   Q = Good data word (if appropriate)

Error Number	Error Description
01	Data compare error
02	Interrupt with CLK request clear
03	No interrupt with CLK request set
04	Controller internal reject
05	Controller external reject
06	No reject output to disable channel
07	Reject on output to enable channel
08	Internal reject on input during interrupt service
09	Internal reject on output during interrupt service
0A	External reject on input during interrupt service
0B	External reject on output during interrupt service
0C	Unused bit set in clock status
0D	Unused bit set in data status

Error Number	Error Description
0E	Parity error set
0F	Character lost set
10	Break error set
11	Clock status set after clear controller
12	Clock status clear after 100 milliseconds
13	Clock set after clear interrupt
14	Clock status clear after 1000 milliseconds
15	More than one interrupt for interrupt request
16	Timed-out waiting for interrupt
17	Character request not set
18	Bit set in data word after clear
19	Wrong channel replies another enabled
1A	No character request after 250 clock pulses
1B	Reject on input from disable channel
1C	Channel enabled by a write
1D	Character ready did not set
1E	No character request after first character
1F	Character request set after two characters
20	No character request after 100-millisecond wait
21	Character lost did not set
22	No character ready after 250 clock pulses

II. SECTION DESCRIPTION

A. SECTION 0 - CONTROLLER STATIC TEST

The following is tested.

1. Controller can be addressed.
2. Clock status is clear after clear controller.
3. Clock status sets.
4. Clock status clears with clear interrupt.
5. Clock status stays set after long delay.
6. Unused bits in clock status word are not set.
7. Controller is not causing unexpected interrupt.
8. Clock can cause interrupt if enabled.
9. Only one interrupt occurs when clock interrupt request is enabled.

B. SECTION 1 - CHANNEL STATIC TEST

The following is tested.

1. A data input will not cause external reject if channel is disabled.
2. A data output will cause external reject if channel is disabled.
3. A data input will reply if channel is enabled; character request will be set (all other bits are clear).
4. If one channel is enabled, all others will reject using data output.
5. A data output will reply if channel is enabled and will reject if the channel is disabled by channel disable.

C. SECTION 2 - CHARACTER REQUEST TEST

The following is tested.

1. Write function does not enable channel.
2. Output null character to DTR channels. Check character request; it should be set due to double buffering.
3. Output another null character. Character request should not be set.
4. Wait 100 milliseconds; character request should be set.

D. SECTION 3 - CHARACTER READY/LOST TEST

This section tests the following on channels with modems in test mode and channels test-jumpered.

1. Character Ready sets.
2. Character Lost does not set erroneously.
3. Character Lost sets.
4. Do 1, 2, and 3 transmitting in other direction.

E. SECTION 4 - TEST MODE DATA TEST

This section exercises channels with modems in test mode or channel pairs test-jumpered.

1. Use data in test mode pattern to exercise receiver and transmitter.
2. If data in parameter is equal to zero, random data is set.

F. SECTION 5 - TRANSMIT SPECIAL PATTERN TO ALL DTR CHANNELS

1. Enable all DTR channels.
2. Transmit special pattern to all channels.
3. Check for last character (send 80).

G. SECTION 6 - ECHO TEST

1. Enable all DTR channels.
2. Scan for input.
3. Echo and store each character until 72 characters are received or carriage return is received.
4. Print a buffer of characters received.

H. SECTION 7 - TRANSMIT ASCII RIPPLE PATTERN TO ALL DTR CHANNELS

1. Enable all channels.
2. Transmit carriage return and line feed.
3. Transmit character to all channels and start pattern with a different character for each channel.
4. Update character and check for end of line (72 columns).
5. Output 64 lines.

III. MISCELLANEOUS

A. JUMPER PLUGS

The following test jumper configurations must be followed to jumper channels for self-test.

1. Channel Connected to Self
   Pin 2 is connected to pin 3, and pin 4 is connected to pin 5 on appropriate channel plugs on the distribution panel.
2. Channel Pair Test Jumpered
   The following example uses channels 0 and 1. This can be followed for any other legal channel pair (2-3, 4-5, 6-7).

   Pin 2 (channel 0) to pin 3 (channel 1)
   Pin 3 (channel 0) to pin 2 (channel 1)
   Pin 4 (channel 0) to pin 5 (channel 0)
   Pin 4 (channel 1) to pin 5 (channel 1)

B. CRT OR EQUIVALENT

The CRT cable has to be modified if a modem is not used.

On either end of cable, remove wires from pins 4 and 5 and install jumpers between pins 4 and 5.

On distribution panel end of cable, remove wire from pin 6 and connect to pin 20.

1743-1 SYNCHRONOUS COMMUNICATION CONTROLLER
(SCCA87 Test No. 87)
(FJ 606-A)

I. OPERATIONAL PROCEDURE

A. REQUIREMENTS

1784-1 or -2 with 8K of memory
1743-1 Synchronous Communication Controller and Distribution Panel and RS-232-C Interface
Jumper plug or wires (optional)
TTY or Equivalent and a terminal to execute Section 6 - Transmit Message
TTY or Equivalent to execute Section 7 - Loop Characters and Output on Comment Device
Furnished message to terminal device (Section 6 - optional)

B. LOADING PROCEDURES

This test loads and executes correctly under SMM17. The calling sequence is specified by the SMM17 system being used. If the equipment address is zero when called, the test will use the prestored equipment address (IA+6).

C. TESTING PROCEDURE

The 1743-1 is tested in various configurations. Self-jumpered channels or channels jumpered to another are tested. If neither of the above is specified, the test will use the channel command Test Mode. Five to eight bits/character and any sync character bit configuration that is compatible with the hardware are tested. Messages, composed and entered by the operator, are sent to the terminal. The test is interrupt-driven and times out interrupts. It is stand-alone because of the response time necessary to service the incoming data.

D. STOPS

1. Type 1 - Parameter Entry (Start of Test)

   a. Stop 1

      A1 = 8751 test ID (87), five stops (5), parameter stop (1)
      Q1 = STJP test Stop/Jump parameter

b. Stop 2

A2 = 01FF — Section select parameter, bit 2 = Section 2, bit 3 = section 3 (There are nine sections (0-8); $BF is prestored.)

Q2 = 0020 — Interrupt line select (Single bit represents interrupt line. $20 is prestored. Example: 0020 = interrupt line 5.)

c. Stop 3

A3 = 00XX — Channel 0 selector (See Channel Select Codes)

Q3 = 00XX — Channel 1 selector

d. Stop 4

A4 = 00XX — Test mode pattern for Section 4 (If set to 0, the character A will be used as a test mode pattern.)

Q4 = X0XX — Special data pattern for Section 5 (If set to X000, the character A will be used as a pattern. If set, bit 15 indicates the character will be sent continuously.)

e. Stop 5

A5 = 0XX0 — Repeat flags (If bit is set, character or message will be repeated continuously.)

Bit 6 - Repeat Section 6
Bit 7 - Repeat Section 7
Bit 8 - Repeat Section 8

Q5 = 000X — Controller and duplex flags, bit 0, controller number (0 or 1) bit 1, 0 = full duplex, 1 = half duplex (Half duplex requires special hardware setup for testing.)

f. Stop 6

A6 = 00XX — Sync character (This parameter must coincide with the hardware jumpers, prestored with $16.)

Q6 = 00XX — Special output character for Sections 1 and 3 (Prestored as $20.)

g. Channel Select Codes

If channel word = 0, no test is to be performed for this channel.

Format of channel word:

Bits 0 through 3:

0 = No test for this channel
1 = This channel test jumpered to other channel
2 = This channel test jumpered to self
3 = Modem connected to I/O device
4 = No terminal connection and no jumpers
5 = Jumpered for Section 8

The channel select codes execute program sections only as follows:

Channel Select Code	Executed Section
0	None
1	0, 4, 5, 7
2	0, 4, 5, 7
3	0, 1, 2, 3, 4, 5, 6, 7
4	0, 1, 2, 3, 4, 5, 7
5	0, 1, 2, 3, 4, 5, 7, 8

Bits 4 through 7:

Number of data bits (5-8) this channel jumpered for; 8 is prestored.

Section 7 will execute with 7- or 8-bit configuration only.

Bits 8 through 15:

Not used.

NOTE

When one channel is jumpered to the other channel, the recipient channel must have a select code of zero.

When Section 6 is executed, the select code must be 3.

When Section 8 is executed, the select code must be 5.

Examples:

A3 = 0000	Channel 0, no test for this channel
Q3 = 0080	Channel 1, no test for this channel
A3 = 0082	Channel 0, eight data bits, channel jumpered to self
Q3 = 0073	Channel 1, seven data bits, channel connected to I/O device

2. Type 1 - Parameter Entry (Section 6)

   This stop is presented when Section 6 is executed.

   a. Stop 1

      A1 = 8721 Test ID (87), two stops (2), parameter stop (1)
      Q1 = STJP Test Stop/Jump parameter

   b. Stop 2

      A1 = 00XX Character n of message
      Q1 = 00XX Character N+1 of message

      Parameter entries will be repeated until zeros are entered in a stop which indicates end of the message. A maximum of 80 characters may be entered (one character per register).

3. Type 2 - End of Section

   a. Stop 1

      A1 = 8722 Test ID (87), two stops (2), end of section stop (2)
      Q1 = STJP Test Stop/Jump parameter

   b. Stop 2

      A2 = 0X00 Section number
      Q2 = XXXX Return address

4. Type 4 - End of Test

   a. Stop 1

      A1 = 8724 Test ID (87), two stops (2), end of test (4)
      Q1 = STJP Test Stop/Jump parameter

   b. Stop 2

      A2 = XXXX Pass count
      Q2 = XXXX Return address

5. Type 8 - Error

   There is a common error routine; therefore, the error parameters always have the same meanings. A description of the error parameters and codes follow.

   a. Stop 1

      A1 = 8778 Test ID (87), seven stops (7), error stop (8)
      Q1 = STJP Test Stop/Jump parameter

b. Stop 2

A2 = CXZZ (C=channel, X=section, ZZ=error code)
Q2 = Return address

c. Stop 3

A3 = Last local I/O call address
Q3 = Second level I/O call address

d. Stop 4

A4 = First level I/O call address
Q4 = Channel status word

e. Stop 5

A5 = Data/status word
Q5 = Clock/protect status word

f. Stop 6

A6 = Function output (A register)
Q6 = Equip/channel output (Q register)

g. Stop 7

A7 = Input data word (if appropriate)
Q7 = Output data word (if appropriate) (The upper bits/character filler bits are included.)

Error Number	Error Description
1	Data compare error
2	Interrupt with clock request clear
3	No interrupt with clock request set
4	Controller internal reject
5	Controller external reject
6	No reject output to disable channel
7	Reject on input to enable channel
8	Internal reject on input during interrupt service
9	Internal reject on output during interrupt service
A	External reject on input during interrupt service
B	External reject on output during interrupt service
C	Unused bit set in clock status
D	Unused bit set in data status
E	Parity error

Error Number	Error Description
F	Character lost
10	Break error
11	Clock status set after clear controller
12	Clock status clear after 100 milliseconds
13	Clock set after clear interrupt
14	Clock status clear after 1000 milliseconds
15	More than one interrupt for interrupt request
16	Timed out waiting for interrupt
17	Character request not set
18	Bit set in data word after clear
19	Wrong channel replies another enabled
1A	No character request after 100 clock pulses
1B	Reject on input from disabled channel
1C	External reject when selecting test mode
1D	Data terminal ready bit not set after channel clear
1E	External reject when disconnecting
1F	Data terminal ready bit set after disconnecting
20	External reject when connecting
21	Data terminal ready bit not set after connecting
22	Test mode bit not set after select test mode
23	Test mode bit set after clear controller
24	Test mode bit set after clear adapter
25	Illegal bits set after clear adapter
26	External reject when clearing test mode
27	Test mode bit set after clear test mode
28	Data set ready status bit not set after request to send
29	Character ready bit set before test mode is on
2A	Function request not set after enable channel
2B	No character ready after 100 clock pulses
2C	Sync character not sent but was received
2D	Character received not a sync character
2E	Sync not established after two sync characters sent
2F	Sync not established after four sync characters sent
30	External reject when disabling channel
31	External reject when request to send
32	External reject when character request
33	Sync not established after 5 milliseconds
34	External reject when stop send

Error Number	Error Description
35	Character request should not be set
36	External reject when clear adapter
37	External reject when getting channel status
38	Sync-not-established is not set after clear
39	Function request is not set after clear
3A	Status ready is not set when carrier-on changes
3B	Ring-indicator bit is not set
3C	Status-ready is not set when ring indicator sets
3E	Character-lost status should be set when more than one character sent
40	Function request is set after disable channel
41	External reject when output character
42	Sync is established after four sync characters are sent
43	External reject when output resync command
44	Sync-not-established bit is not set after resync command
45	Character is not sent but was received
46	Carrier-on bit is not set
47	Sync-not-established bit is set after looping character
48	Character received is not the same as character sent
49	External reject when input data
4A	Character-ready is not set
4B	Character-request is set after stop send
4D	No character request after 250 clock pulses
4E	Status-ready is not set on parity error
4F	External reject when stop is sent
50	Status ready bit should not be set
51	Status ready bit should be set
52	External reject when status request
53	Illegal bit in control channel status

E. WORD MESSAGES

Word messages are available only if there is a TTY or equivalent available. The following messages are information to the operator.

1. Initialization of the Test

```
SCCA87 SYNCHRONOUS COMMUNICATION CONTROLLER TEST. (FJ606-A)
CP2F, VER. 3.1-1
IA=XXXX, FC=XX
```

2. Parameter Selection

   ERROR IN CHANNEL PARAMETER
   This indicates that an error was made in the description of channel configurations. After the message is typed, parameter selection will be reentered.

3. Section 6 - Transmit Furnished Characters to Terminal Device

   SCCA87 SECTION 6 - SUBMIT CHARS (THE OLD ARE DISPLAYED) INCLUDE ANY SYNC CHARS, MSG HEADERS AND EOT, AND PARITY MAX 80 CHARACTERS. 0 = END OF MESSAGE
   This message alerts the operator that the test is not actively testing but awaiting characters to send.

4. Section 7 - Results of either Test Mode, Single Channel Jumpered Loop, or Two Channel Jumpered Loop

   SCCA87 SECTION 7 - CHANNEL n LOOP RESULTS
   This message alerts the operator that the complete character set ($20 through $5F) will follow after looping through the channel.

II. SECTION DESCRIPTIONS

A. SECTION 0 - CONTROLLER STATIC TEST

The following is tested.

1. Controller can be addressed.
2. Clock status is clear after clear controller.
3. Clock status sets.
4. Clock status clears with clear interrupt.
5. Clock status stays set after long delay.
6. Unused bits in clock status word are not set.
7. Controller is not causing unexpected interrupt.
8. Clock can cause interrupt if enabled.
9. Only one interrupt occurs when clock interrupt request is enabled.

B. SECTION 1 - CHANNEL STATIC TEST

The following is tested.

1. A program clear causes bits 1, 2, and 10 of channel status to be set (all others except bit 6 should be reset), a disable channel command causes bit 10 of channel status to be reset, and an enable channel causes bit 10 to be set.
2. A data input will not cause external reject if channel is disabled.
3. A data output will cause external reject if channel is disabled.
4. A data input will reply if channel is enabled; character request will be set. (All other bits are clear.)
5. If one channel is enabled, all others will reject using data output.
6. A data output will reply if channel is enabled and will reject if the channel is disabled by channel disable.
7. A program clear causes bit 2 of channel status to be set, a disconnect causes bit 2 to be reset, and a connect causes bit 2 to be set.
8. A stop send command resets character-request status bit.
9. A request status command sets the status ready bit of the input control channel.

C. SECTION 2 - TEST MODE BIT TEST

The following is tested.

1. Select-test-mode and clear-controller causes test mode status bit to be set and reset.
2. Select-test-mode and clear-adapter causes test mode status bit to be set and reset.
3. Select-test-mode and clear-test-mode causes test mode status bit to be set and reset.

D. SECTION 3 - ADAPTER LOOP (ECHO) TEST

This section tests the following:

1. Character-ready status bit will not set before test mode is on.
2. A character can be sent and received by the same channel when in test mode.
3. The receipt of sync characters clears the sync-not-established bit.

4. A resync command sets the sync-not-established status bit.

5. Check if sync-not-established status bit sets when complete character set (except $16) is sent.

6. Send random characters in test mode and check received character against that sent (Loop Test).

E. SECTION 4 - TEST MODE DATA TEST

Send specified characters in test mode and check received character against that sent (Loop Test).

F. SECTION 5 - CHARACTER READY/LOST TEST

The following is tested.

1. Character-ready sets and character- lost does not set erroneously.

2. Character-lost sets correctly.

This test may be repeated if operator enters flag in parameter.

G. SECTION 6 - TRANSMIT FURNISHED CHARACTERS TO TERMINAL DEVICE

1. Pick up message from operator.

2. Clear adapter, enable channel, and request to send.

3. Transmit all characters submitted.

4. Keep looping through submitted characters if prescribed by parameter A5.

5. Do both channels before waiting for interrupt.

H. SECTION 7 - LOOP CHARACTERS AND OUTPUT OF COMMENT DEVICE

Loop the complete character set ($20 through $5F) through each active channel and output on the comment device. The test will be repeated if prescribed by parameter A5.

I. SECTION 8 - CHECK CARRIER-ON, RING-INDICATOR, AND STATUS-READY STATUS BITS

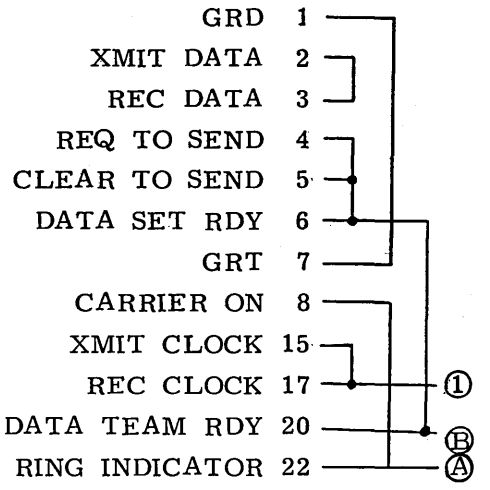
This section tests internal hardware logic only and must be jumpered from request-to-send.

III. TEST FIXTURES

It is necessary to fabricate the following fixtures if Single Channel Loop or Channel to Channel Loop Tests of test 87 are to be run. The Single Channel Loop Test fixture must also be utilized if Internal Test Mode Tests are to be run and there is no available modem.

A. SINGLE CHANNEL LOOP TEST (Transmit and receive on the same channel)

Use connector P/N 93609008 and make the following connections.

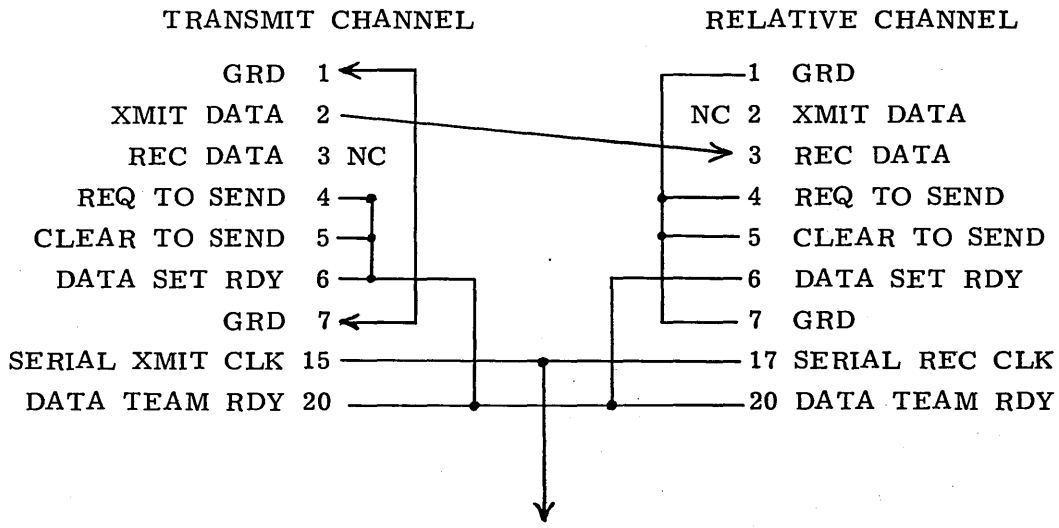


Square wave input 10 vpp; frequency determines baud rate.
Ⓐ and Ⓑ are tied together for Section 8. This checks ring indicator and carrier on.

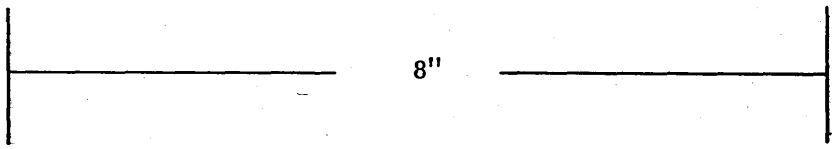
① This signal must be supplied by a square wave generator or an oscilloscope calibrate output of the proper amplitude. If a modem exists on the system, jumper this line to pin 15 of the connector of the cable connected to the modem.

B. CHANNEL TO CHANNEL LOOP TEST

Use two connectors each (P/N 93609008) and make the following connections.



SEE ① ON THE PREVIOUS PAGE.



EVENT COUNTER SUBSYSTEM

(CTRP81 Test No. 81)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

Bit 8 of SMM control word must be set at load time to select MBS.

When selecting the 1573 Line Sync Clock alone to drive the Event Counter System, certain hardware limitations and software considerations must be observed. These are:

1. When executing Section O (Ripple Carry Test) the 1573 must be jumpered at 480 Hz or slower. Software overhead dictates this low rate. Due to the Event Counter configuration, only the low order 4 channels may be tested, four 8-bit counters or two 16-bit counters.
2. When executing Section 1 (Event Per Unit Time Test) the 1573 must be jumpered at 480 Hz or slower. Software overhead dictates this low rate. Due to the Event Counter configuration, only channel addresses 0 and 2 may be checked.
3. When executing Section 2 (Full Register Count) the 1573 must be jumpered at 480 Hz or slower. At this frequency the test will be complete execution in 8 minutes.

When selecting the shorting connector as a driving device only Section 0 may be executed. Initialization error F1 will be reported if more than Section 0 is selected. One shorting connector will handle only 16 channel addresses, 16 8-bit registers or 8 16-bit registers.

B. LOADING PROCEDURE

The SKIP switch must be set during execution of quick look to force a monitor parameter stop. When this monitor stop occurs, bit 08 of the Stop/Jump parameter word must be set to retain the Modular Based Subroutines (MBS) package required to execute this test.

C. PARAMETERS

If bit 0 of the Stop/Jump parameter word is set, the test will stop for one monitor stop and seven test parameter stops as follows:

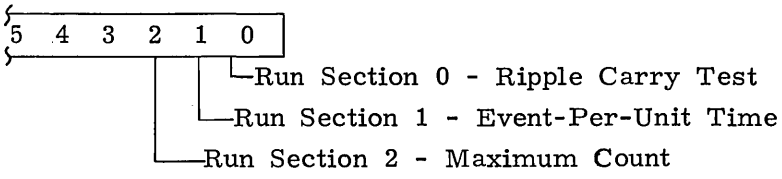
First Stop: A = ID Word

Q = Stop/Jump Parameter

Second Stop: A = Test Sections to be Executed

Q = DCT/MDC Equip Addr Associated with the ECU *

A Register



Third Stop: A = First Channel Addr Assigned to the ECU

Q = Last Channel Addr Assigned to the ECU

Fourth Stop: A = First Channel Addr to be Tested

Q = First Channel Addr Assigned to the Driving Device **

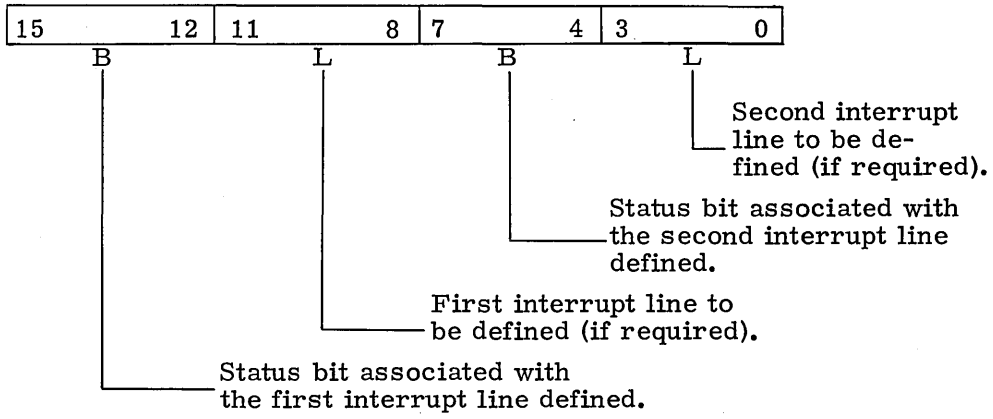
Fifth Stop: A = Encoded Bits Defining Each 8-Bit Counter, For Counters 0-15

Q = Encoded Bits Defining Each 8-Bit Counter, For Counters 16-31

If A register bit 0, and 1 are set, 2 and 3 are not set. Counters 0 and 1 defined as two-8-bit counters and counters 2 and 3 are tied together to form a 16-bit counter.

Sixth Stop: A = Status Bit/Interrupt Lines Assigned to ECU

Q = Unused



Seventh Stop: A = First Station Address Assigned to the ECU

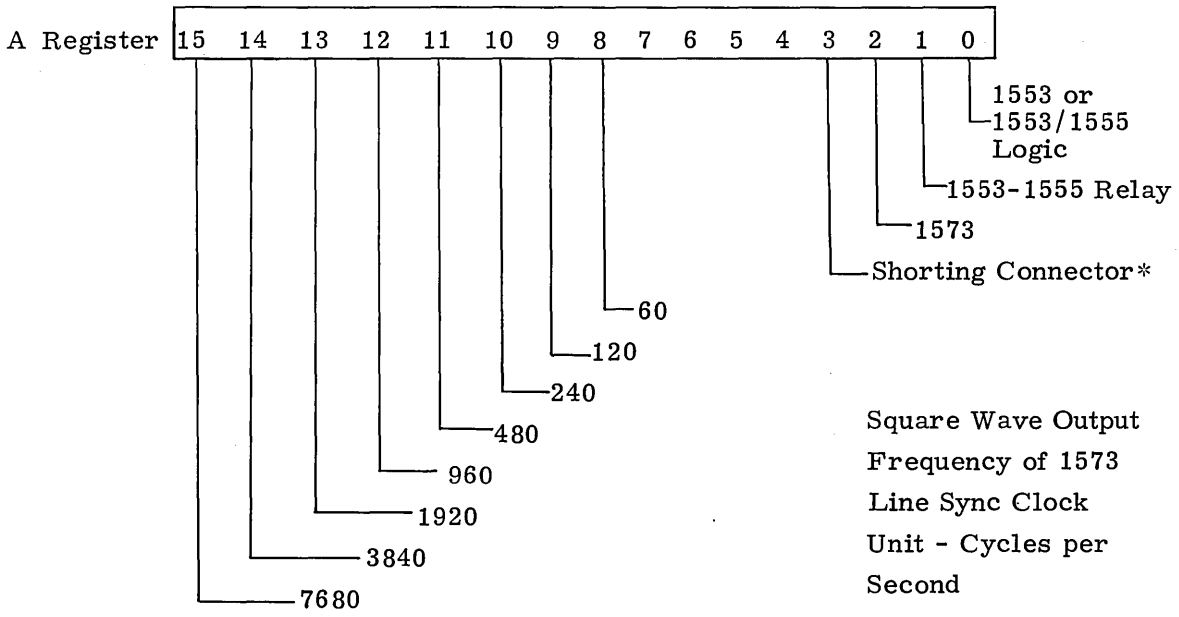
Q = First Station Address Assigned to the Driving device, if required

* Set bit 15 if running on a DCT.

** A shorting connector driving device may only execute Section 0.

Eighth Stop: A = Encoded Bits Defining the Driving Device

Q = DCT/MDC Equip Addr Associated with the Device Driving the ECU



D. STOP AND JUMP SETTINGS

Bit settings in the Stop/Jump word are the standard SMM assignments.

Bit	Stops
0	Stop to Enter Test Parameters
1	Stop at End of Test Section
2	Stop at End of Test
3	Stop on Error
	Jumps
4	Repeat Conditions
5	Repeat Test Section
6	Repeat Test
7	Not Used
8	Omit Typeouts
9	Display Memory Return Address
10	Re-Enter Test Parameters

Each individual test running under control of SMM17 3.0 may have unique Stop/Jump words. The monitor may have a unique Stop/Jump word. To im-

* A shorting connector driving device may only execute Section 0.

plement this capability the Stop/Jump processor maintains a table of Stop/Jump words for the monitor and each of the loaded tests. Only the Stop/Jump word for the test or monitor requesting the current monitor stop (as when the SKIP switch is set) will be updated. In this fashion only the monitor's Stop/Jump word, or a single tests Stop/Jump word, can be altered.

A problem may exist when the operator attempts to change a tests Stop/Jump word while the test is running, i.e., after an error so to omit typeouts and repeat conditions. It is possible to change the monitor's Stop/Jump word rather than the tests Stop/Jump word. One of two actions may be taken to prevent this from happening:

1. Execute the test with bit 03 set, stop on Errors. When the test stops to report an error, the tests Stop/Jump word may successfully be changed.
2. When a monitor stop is executed by setting the SKIP switch, set the A register of the first stop (the ID word) to all zeros. This will cause all the individual Stop/Jump words to be set to the same value.

E. MESSAGES

1. Initial Program Typeout

   FR117 ECS TEST 81
   IA = XXXX

2. Completed Pass Typeout

A	Q	A	Q
8124	NUM1	NUM2	NUM3

   NUM1 - SMM Parameter Word
   NUM2 - Pass Count
   NUM3 - Return Address

3. Error Typeouts

   The errors of test CTR can be grouped into two general categories. Those associated with each unique diagnostic section and those associated with the I/O cycle, which are common to all diagnostic sections.

   a. I/O Cycle Error Reporting
      I/O cycle error reporting can be identified by the test error pointer being between 00 and 0F. The first 4 pairs of A/Q typeouts in this report have a standardized definition. These definitions are as follows:

A	Q	A	Q	A	Q	A	Q
ID	ST/JP	SS/EE	RTN	MBSERR	IO/RP	(A)	(Q)

ID = SMM Identifier Word

ST/JP = SMM Stop/Jump Parameter Word

SS/EE = Test Section Number and Test Error Pointer

RTN = Return Address

MBSERR = MBS Monitor Detected Error Code

- 00 - Status Time Out Error
- 01 - I/O Time Out Error
- 02 - I/O Response Error
- 03 - Status Error
- 04 - Interrupt Time Out Error

IO/RP = Last I/O Operations Performed and the Associated Response

- IO - 10 = Write
  - 20 = Read
  - 30 = Function
- RP- 10 = Reply
  - 20 = External Reject
  - 30 = Internal Reject

(A), (Q) = Register Contents Relative to the Last I/O Operation

b. The next 3 pairs of A/Q typeouts vary with the type of MBS monitor detected error code. The content of these 3 pairs of typeouts are as follows:

MBS Error Code	A	Q	A	Q	A	Q
00	ACT STS1	ACT STS2	CLOCK	OCBS	-	-
01	ACT STS1	ACT STS2	CLOCK	-	-	-
03	ACT STS1	EXP STS1	ACT STS2	EXP STS2	-	-
04	ACT STS1	ACT STS2	CLOCK	INT LINE	INT MASK	ASGN LINES

ACT STS1, ACT STS2 - Actual status 1 and status 2 copied from the ECS.

EXP STS1, EXP STS2 - Expected status 1 and status 2.

CLOCK - The time limit in milliseconds which expired waiting for the specified condition to occur.

OCBS - The control word being used during a dynamic status check.

C = 1 Repeating the status check if the specified bit was on.
= 2 Repeating the status check if the specified bit was off.

B = A hexadecimal number 0 through F defining the status bit 0 through 15 within the status word being monitored.

S = 0 - Monitoring director 1 status.
1 - Monitoring director 2 status.

INT LINE - The line number of the interrupt which occurred.

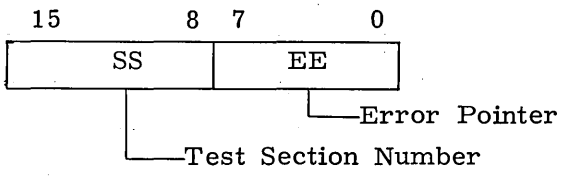
INT MASK - The interrupt mask being used at the time of the interrupt.

ASGN LINES - A summation of all the interrupt lines assigned to the device.

c. I/O Cycle Error Pointers

The following 16 error pointers relate to not only what condition was in error, but where it occurred within the I/O cycle. Refer to Figure 1 for the sequence of possible error pointers. These error pointers must be interpreted in relation to the MBSERR error code of the error message.

SSEE =



The test section numbers are defined as follows:

00 - Ripple - Carry - Test
01 - Event - Per - Unit Time Test
02 - Maximum Count Test

The error pointers are defined as follows:

00 - An error was detected attempting to connect to the ECS subsystem.
01 - An error was detected attempting to preload a counter register.
02 - Interrupt status was not all zeros or the ECS did not respond to the interrupt status request.

03 - An error was detected attempting to function the 1573 to enable sync.

04 - An error was detected attempting to function the 1573 to disable sync.

05 - An error was detected attempting to function the 1572.

06 - An error was detected communicating to the 1500 device driving the ECS.

07 - An error was detected communicating to the 1500 device driving the event counter system.

08 - An error was detected attempting to function the 1573 to disable sync.

09 - An error was detected attempting a Read-No-Execute command to the ECS.

0A - Interrupt status was not as expected, or the ECS did not respond to the interrupt status request.

0B - An error was detected attempting a Read-Execute command to the ECS.

0C - Interrupt status was not as expected, or the ECS did not respond to the interrupt status request.

0D - An error was detected attempting a Read-Execute command to the ECS.

0E - Interrupt status was not all zeros, or the ECS did not respond to the interrupt status request.

0F - An error was detected attempting to connect to the driving device subsystem.

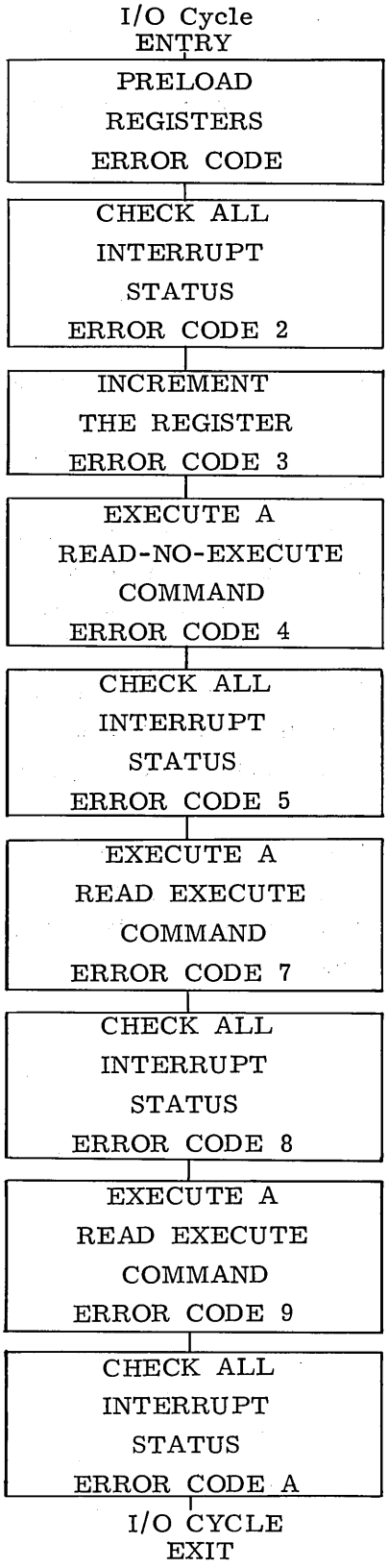


Figure 1. Sequencing of I/O Cycle Error Codes

d. Test Section Error Reporting

Errors detected by the test sections not associated with I/O operations are reported in 4 pairs of A/Q typeouts, identified by error pointer greater than 10, defined as follows:

A	Q	A	Q	A	Q	A	Q
ID	ST/JP	SS/EE	RTN	ACT	EXP	COUNT	ADDR

ID = SMM Id Word
ST/JP = SMM Stop/Jump Parameter Word
SS/EE = Test Section Number and Test Error Pointer
RTN = Return Address
ACT = The Actual Condition Found
EXP = The Expected Condition
COUNT = The I/O Cycle Pass Count
ADDR = The Event Counter Register Address Containing the Reported error

1) Error Codes For Section 0 - Ripple Carry Test
   10 - The counter register did not increment by 1 count.
   11 - A Read-No-Execute command did not leave the counter register undisturbed.
   - Shorting plug only: The Read-No-Execute command did not increment the register by one count.
   12 - A read Execute command did not clear the counter register to zero.

2) Error Codes for Section 1 - Event - Per - Unit - Time
   20 - A register counted prior to sync enable.
   21 - Basic counting error.
   22 - A register counted after the disabling sync.

3) Error Codes for Section 2 - Maximum Count Test
   031 - The lower 8 bits of an A register input from an even channel address 8-bit register does not contain the correct count.
   032 - The upper 8 bits of an A register input from an even channel address 8-bit register are not all zeros.
   033 - The A register input of an even channel address 8-bit or 16-bit register are not all zeros.
   034 - The lower 8 bits of an A register input from an odd channel address 8-bit register are not all zeros.

035 - The upper 8 bits of an A register input from an odd channel address 8-bit register does not contain the correct count.

036 - The lower 8 bits of an A register input from an even channel address 16-bit register does not contain the correct count.

037 - The upper 8 bits of an A register input from an even channel address 16-bit register does not contain the correct count.

e. Initialization Errors

0F0 - No driving device was selected.

0F1 - Sections not defined correctly when running with a shorting plug.

0F2 - ECS response error when trying to enable the lower group interrupt (counter address 0 to 15).

0F3 - ECS response error when trying to enable the upper group interrupt (counter addresses 16-31).

0F4 - 1573 frequency not defined correctly.

f. Error Codes for the Interrupt Processor

040 - An interrupt did not occur when expected.

II. DESCRIPTION

A. SECTION 0 - RIPPLE CARRY TEST

Section 0 tests each register singly for the proper execution of the following:

1. Each bit of every register can be preloaded to logical zero or to logical one.
2. Each register can increment by one count.
3. A Read-No-Execute command does not change the contents of the addressed register.
4. A Read Execute command after reading the register clears the contents of the addressed register to zero.
5. Overflowing each register sets an interrupt status and produces an interrupt.
6. Reading interrupt status resets the interrupt status to zero.

After each of 16 passes through the common I/O cycle, Section 0 will execute the following:

1. Preload the addressed register with a value equal to 2^N-1 where $0 \leq N \leq 8$ for 8-bit registers and $0 \leq N \leq 16$ for 16-bit registers.
2. Check all interrupt status to be zero.
3. Increment the addressed register by one count.
4. Read without clearing the value contained within the addressed register.
5. Check all interrupt status. If overflow occurred due to the increment, verify the status accordingly.
6. Read and clear the value contained within the addressed register.
7. Check all interrupt status to be zero.
8. Read and clear the value contained within the addressed register.

Any errors detected by the monitor during execution of this I/O cycle will be reported as described in the I/O cycle error reporting section.

After executing each pass through the I/O cycle, Section 0 verifies the data read back from the register. A check is made to verify:

1. The Read-No-Execute command read a value equal to the preload value + 1.
2. The first Read-Execute command read the same value as the Read-No-Execute command.
3. The second Read-Execute command read all zeros.

Each register in turn is checked throughout its full count range - 0 to $00FF for 8-bit registers and 0 to $FFFF for 16-bit registers. The section terminates when all registers have been individually cycled up and checked.

In the event full testing is not possible, Section 0 may be executed with a shorting plug connected to J02 and/or J03, the cable input connectors to the events counter. In this configuration a quick check of 75 percent of the events counter may be made.

With a shorting plug connected as an input, the logic within the control sections is such that changing the channel address will cause all registers to increment by one count.

Section 0 will execute in the normal fashion with the shorting plug installed with one exception; the section normally verifies that a Read-No-Execute instruction followed by a Read Execute instruction both yield the same value, and a second Read Execute instruction yields all zeros. With the shorting plug installed, the first Read Execute instruction will yield a value one greater than that read in the Read-No-Execute instruction.

B. SECTION 1 - EVENT - PER - UNIT - TIME TEST

Section 1 tests all registers in parallel for the proper execution of the following:

1. Each register does not count before an enabling sync pulse.
2. Each register counts properly after an enabling sync pulse.
3. Each register stops counting after a disabling sync pulse.

Section 1 verifies that each register will not count until receipt of an enabling sync pulse. This pulse will be generated by a 1573/1572. The section will then produce counts to all the registers configured for the test until a second sync pulse is generated. The section will then produce another series of counts to verify the register will not count beyond the disabling sync.

On the first pass through the I/O cycle, Section 1 will do the following:

1. Preload all registers to zero.
2. Produce counts to all the counter registers configured for the test.
3. Do Read-No-Executes from each of the counter registers.

The section will then verify that all the registers have not counted. The second pass through the I/O cycle Section 1 will do the following:

1. Set up the 1572 and 1573 to produce a sync pulse as defined in the Stop/Jump parameters.
2. Produce counts to the counter registers for 2-1/2 sync pulse periods.
3. Disable the 1573 sync output.
4. Do Read-No-Executes from each of the counter registers.

The section will then verify that each register has counted properly. After the third pass through the I/O cycle, Section 1 will do the following:

1. Produce counts to all the counter registers configured to the test.
2. Do Read-No-Executes from each of the counter registers.

The section will then verify the registers did not count.

C. SECTION 2 - MAXIMUM COUNT TEST

Section 2 tests all registers for the proper execution of the following:

1. Properly incrementing over the entire register range.
2. Not incrementing when all other registers within the module increment (cross talk check).
3. Produce an interrupt and interrupt status when overflow occurs.

Section 2 counts all registers from 0 to their full count-$00FF for 8-bit registers and $FFFF for 16-bit registers. All registers within the module are tested simultaneously. Incrementing is executed in a "sliding zero" concept (all registers increment except one) the one non-incrementing counter changing from one register to another. At completion of the counting cycle, all registers will have incremented 16 counts greater than their preload value. In an events counter module configured with both 16-bit and 8-bit registers, the 16-bit registers will make one full count (0 to $FFFF) per pass through Section 2. The 8-bit counters will make 256 full count passes (0 to $00FF) through each pass. Each of the passes through the common I/O cycle, Section 2 will do the following:

1. Preload all registers with a value equal to 0, $10, $20, $30, etc. up to $00F0 for 8-bit registers and $FFF0 for 16-bit registers.
2. Check all interrupt status to be zero.
3. Increment all registers by 16 counts.
4. Read without clearing the new value in each of the registers.
5. Check all interrupt status. If overflow occurred due to the incrementing, verify the status accordingly.
6. Read and clear the value contained in each of the registers.
7. Check all interrupt status to be zero.
8. Read and clear the value contained in each of the registers.

Any errors detected by the monitor during execution of this I/O cycle will be reported as described in I/O cycle error reporting.

After executing each pass through the I/O cycle, Section 2 verifies the data read back from each register. A check is made to verify that the Read-No-Execute read a value in which:

1. The unused bits of the A register were zero.
2. The counter register value was equal to the preload value +16.

III. PHYSICAL REQUIREMENTS

A. CODE REQUIREMENTS

This test requires 970_{16} core locations. The SMM monitor must contain the MBS package for a total monitor length of $0D00_{16}$ words. A minimum core requirement to run this test alone is 1670_{16} locations.

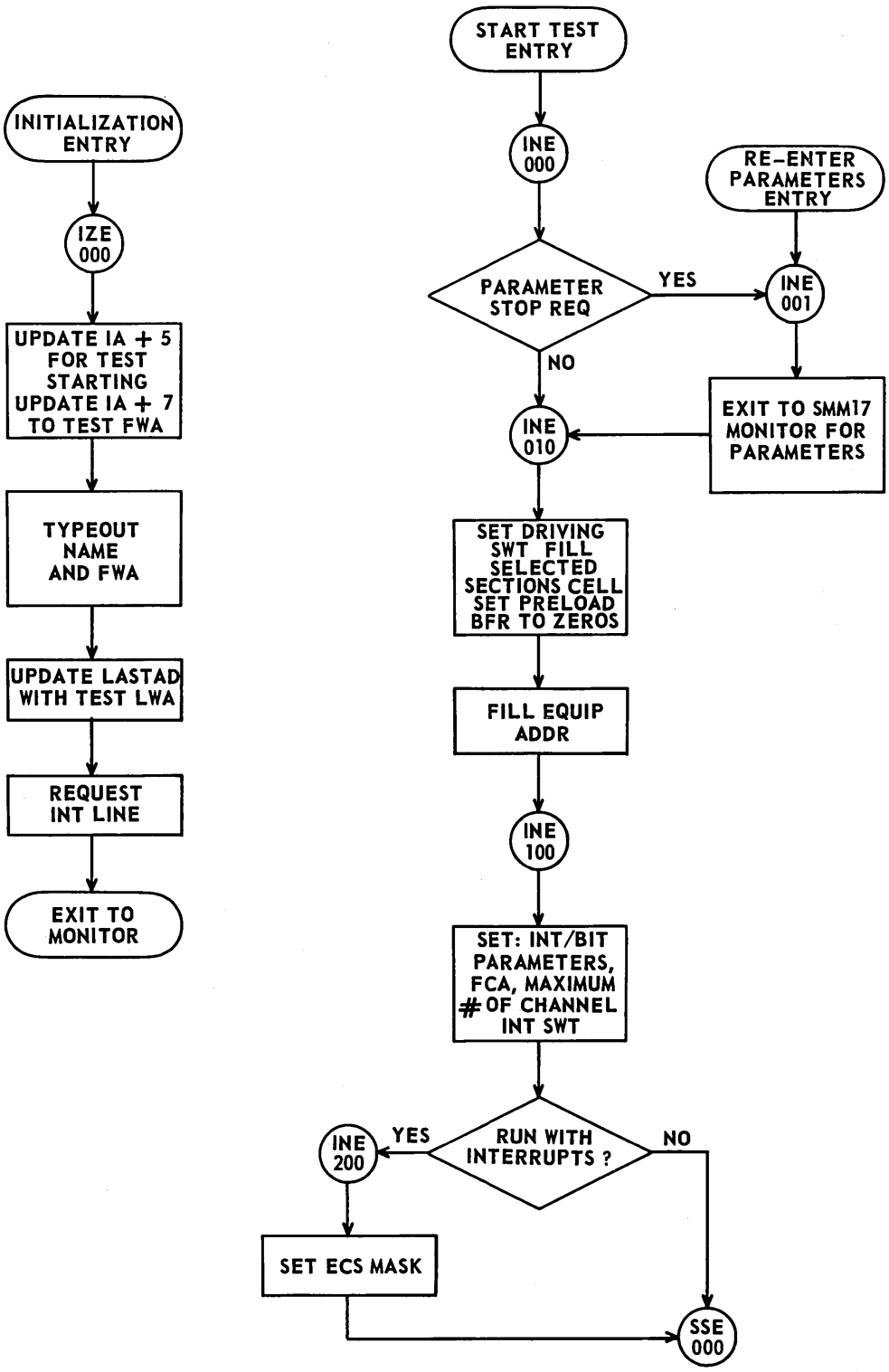
B. EXECUTION TIME

To execute all test sections with a full complement of registers requires approximately 70 seconds.

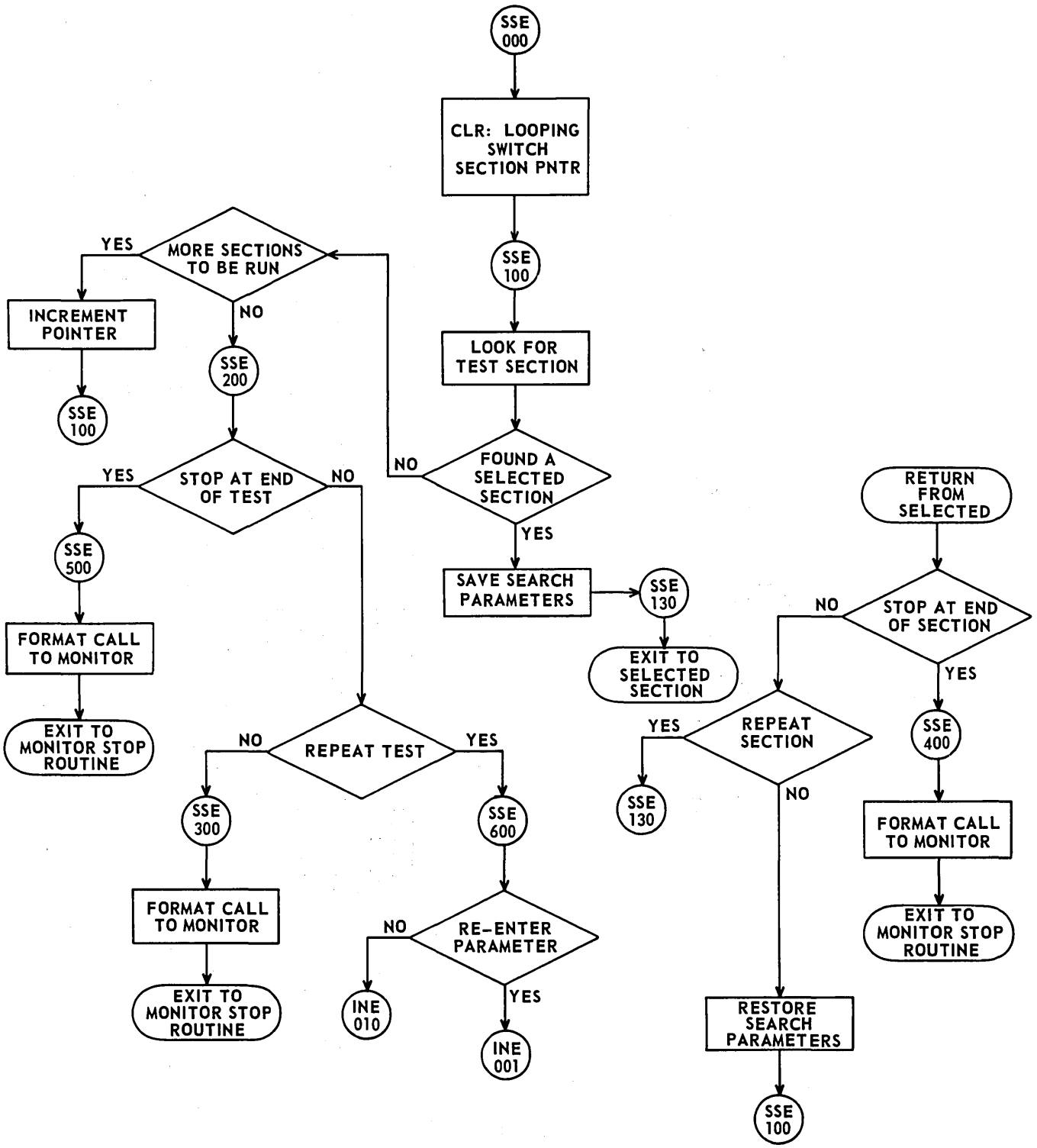
C. SPECIAL EQUIPMENT

To execute Sections 0 and 2, a minimum of 1 and maximum of 2 cables are required to connect the driving device to the events counter.

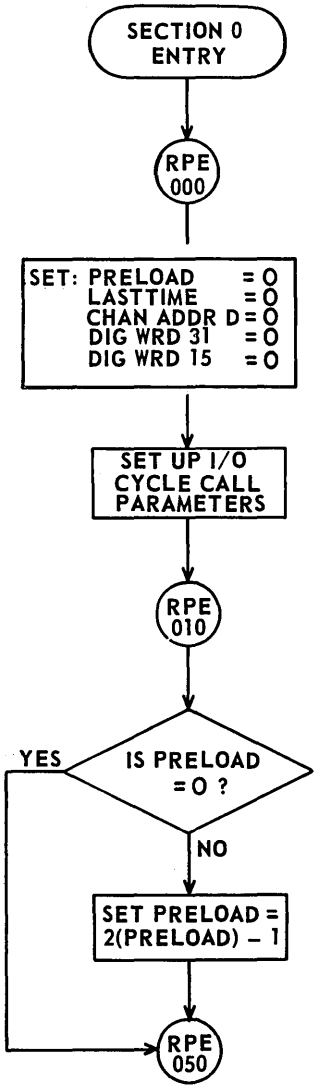
An alternate test setup is to execute only Section 0 with a shorting plug located in the cable inputs of events counter module.

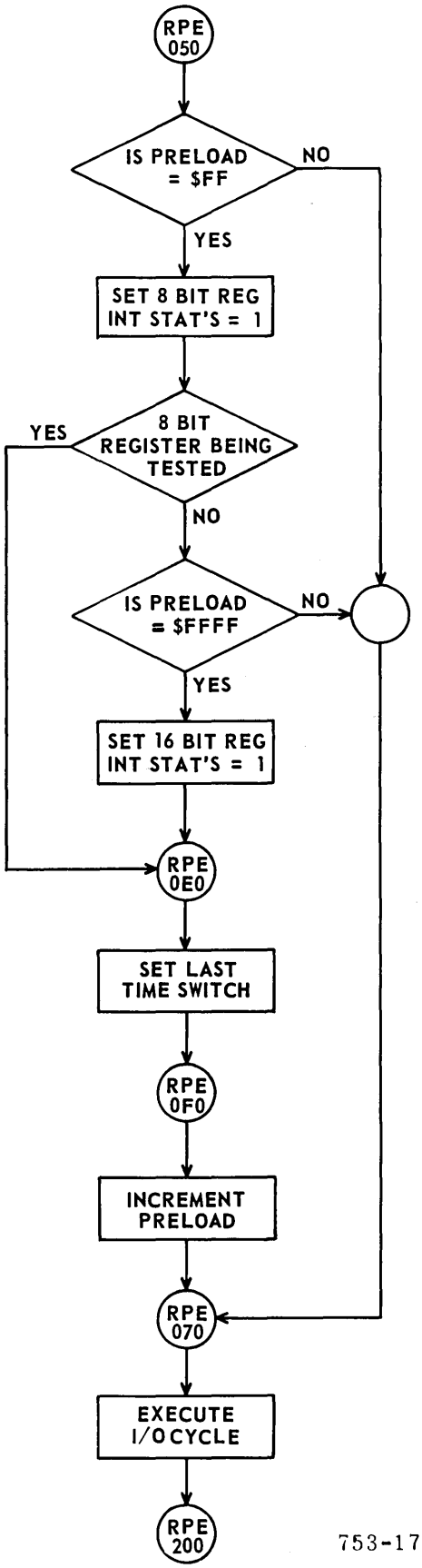


TEST COUNTER INITIALIZATION AND START UP

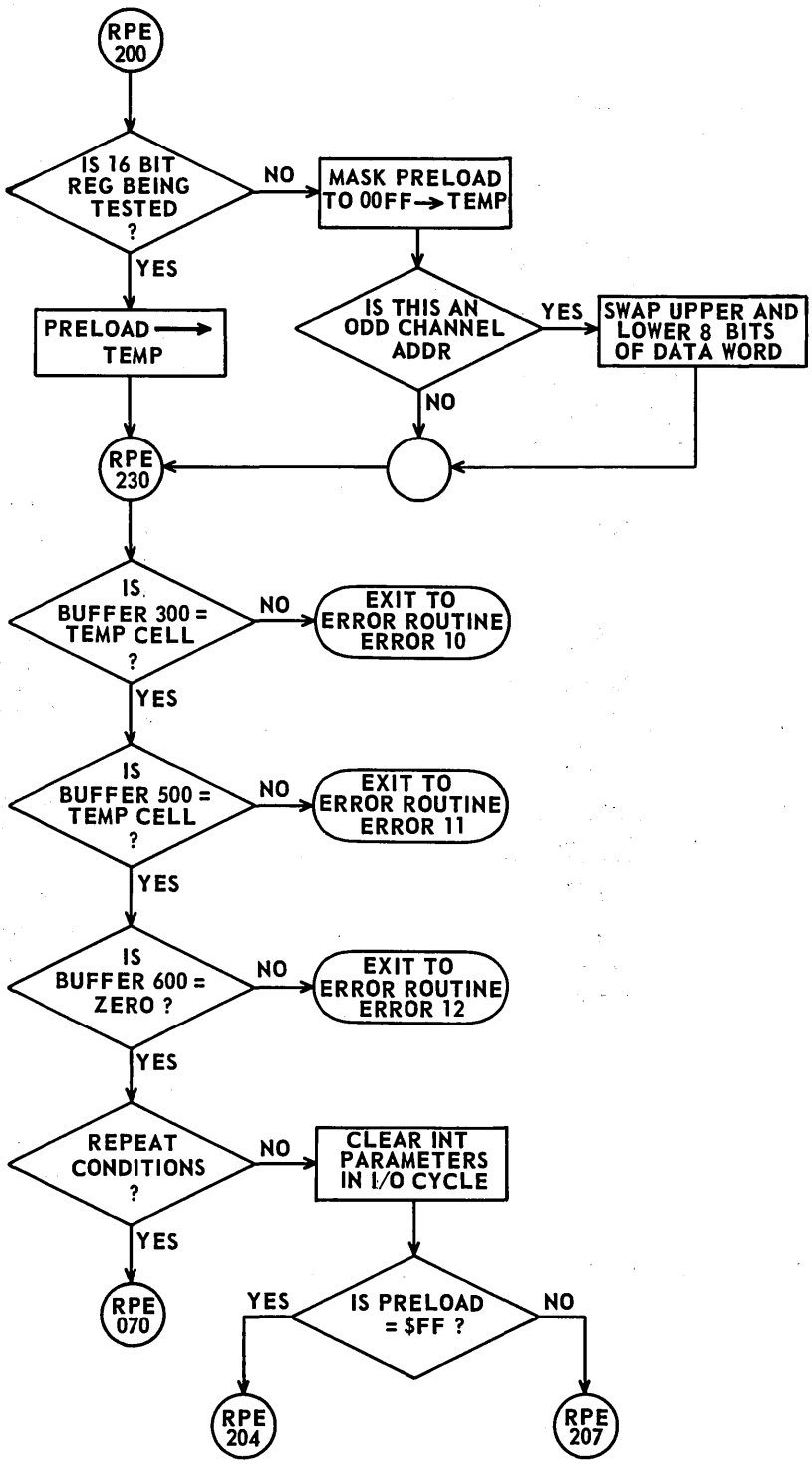


TEST COUNTER SECTION SEARCH & EXECUTION CONTROL

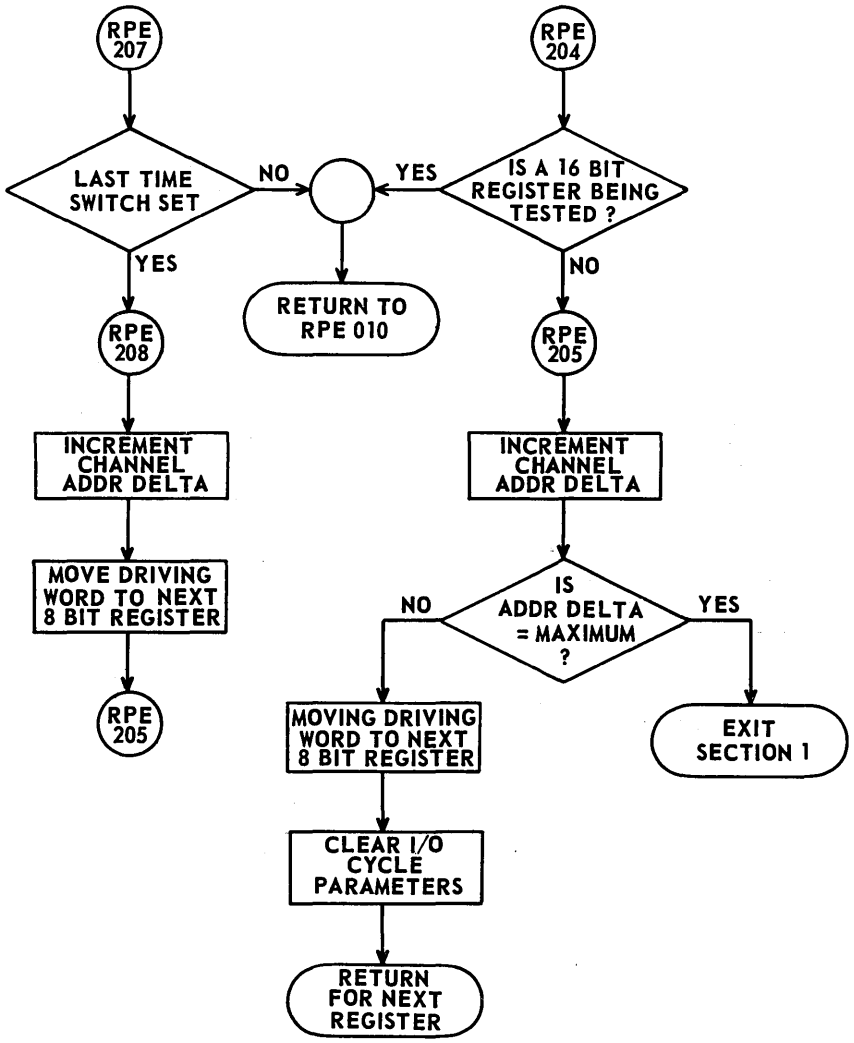




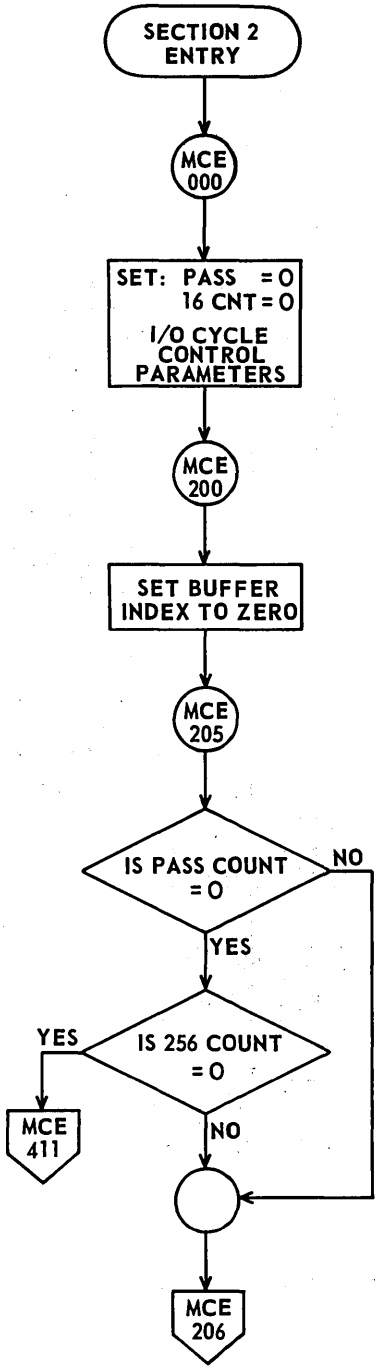
TEST COUNTER SECTION 0 RIPPLE CARRY (1)



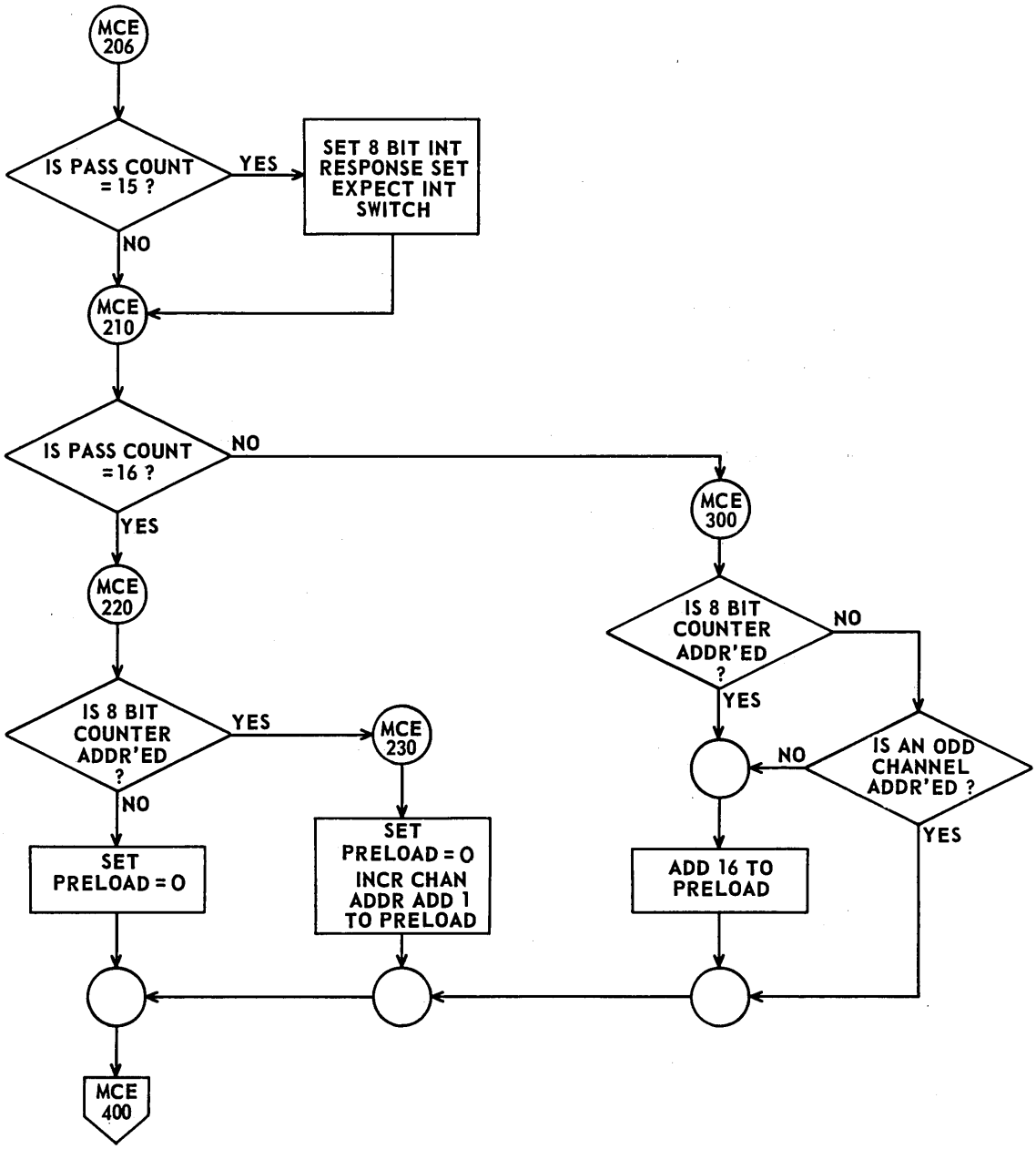
TEST COUNTER SECTION 0 RIPPLE CARRY (2)



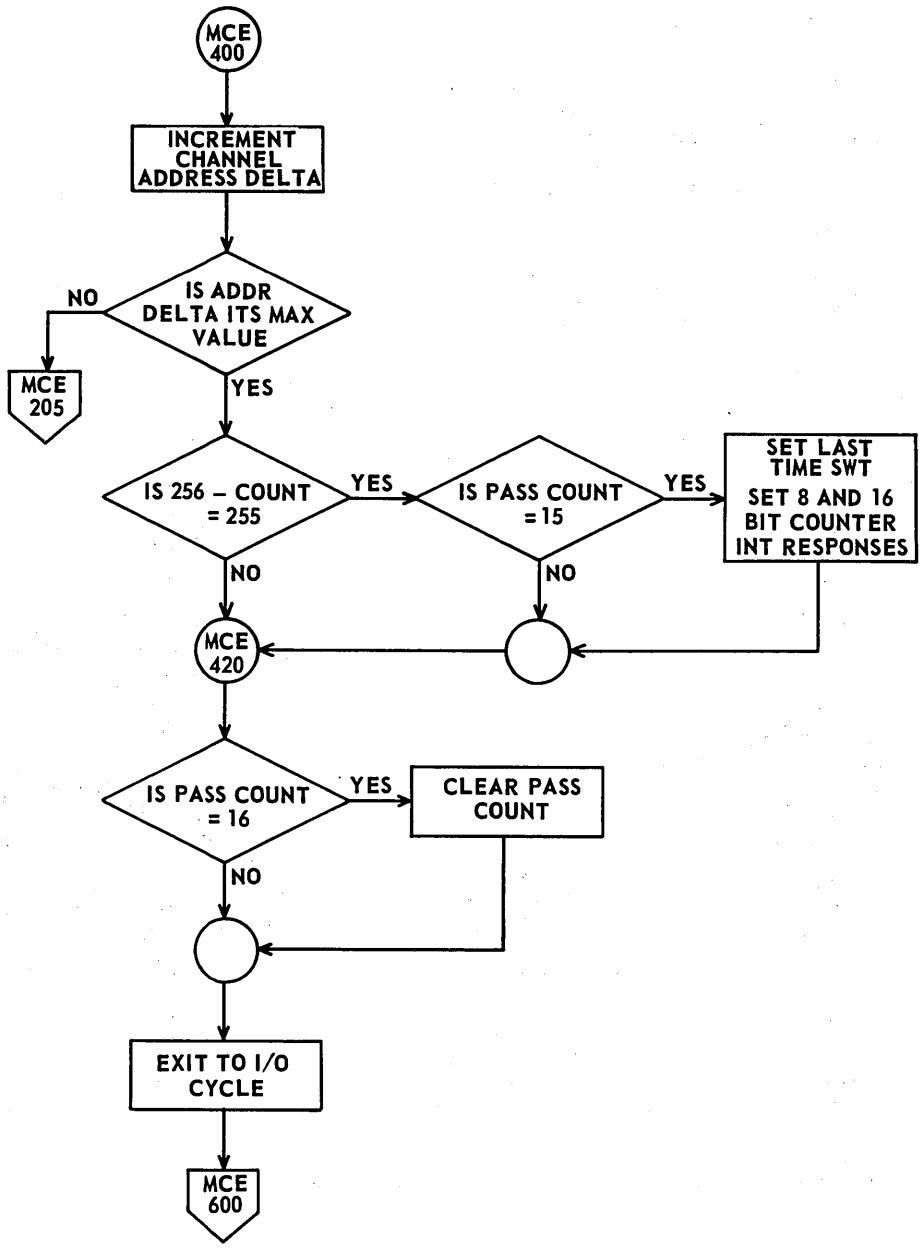
TEST COUNTER SECTION 0 RIPPLE CARRY (3)



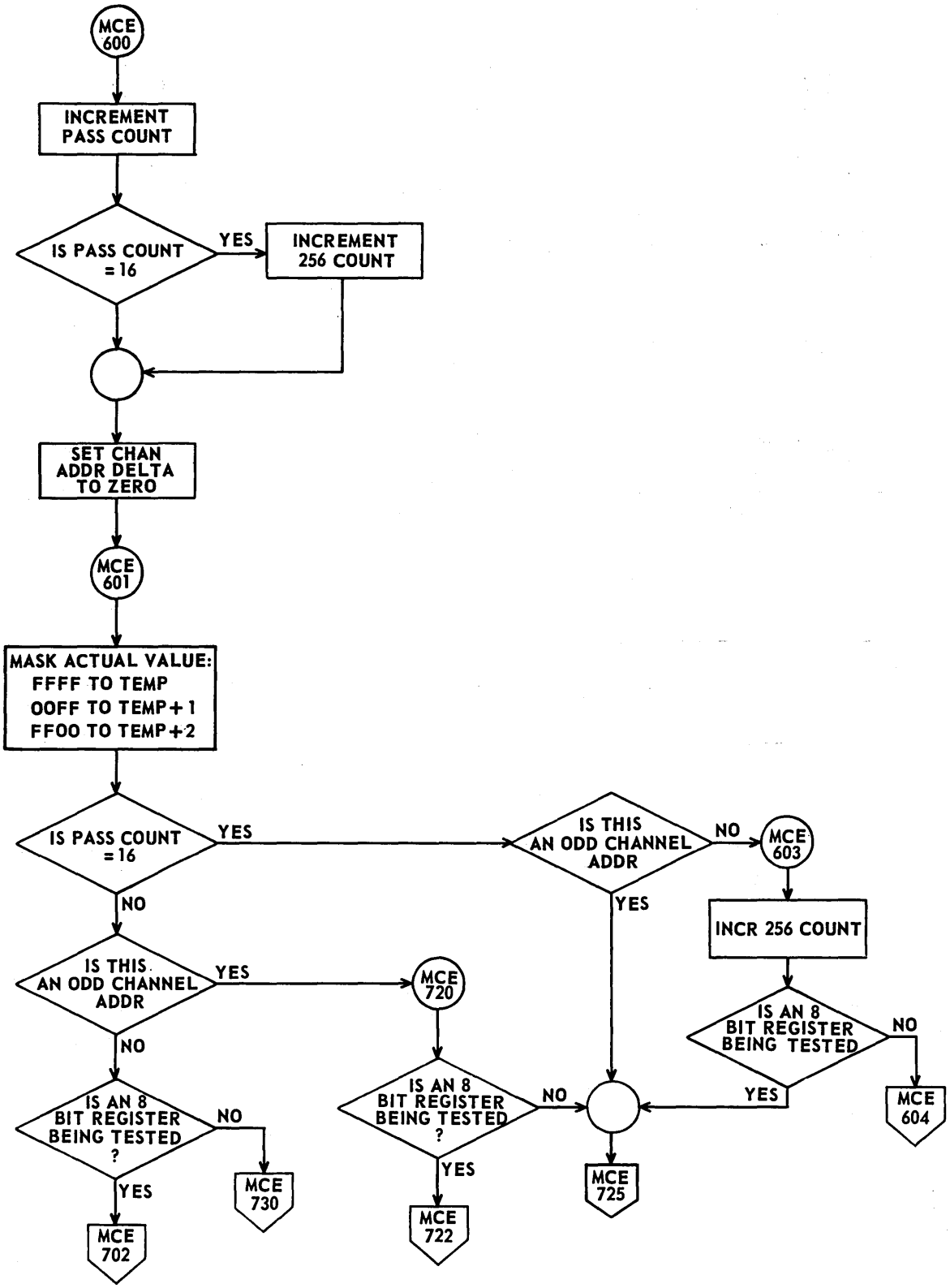
TEST COUNTER SECTION 2 MAXIMUM COUNT (1)



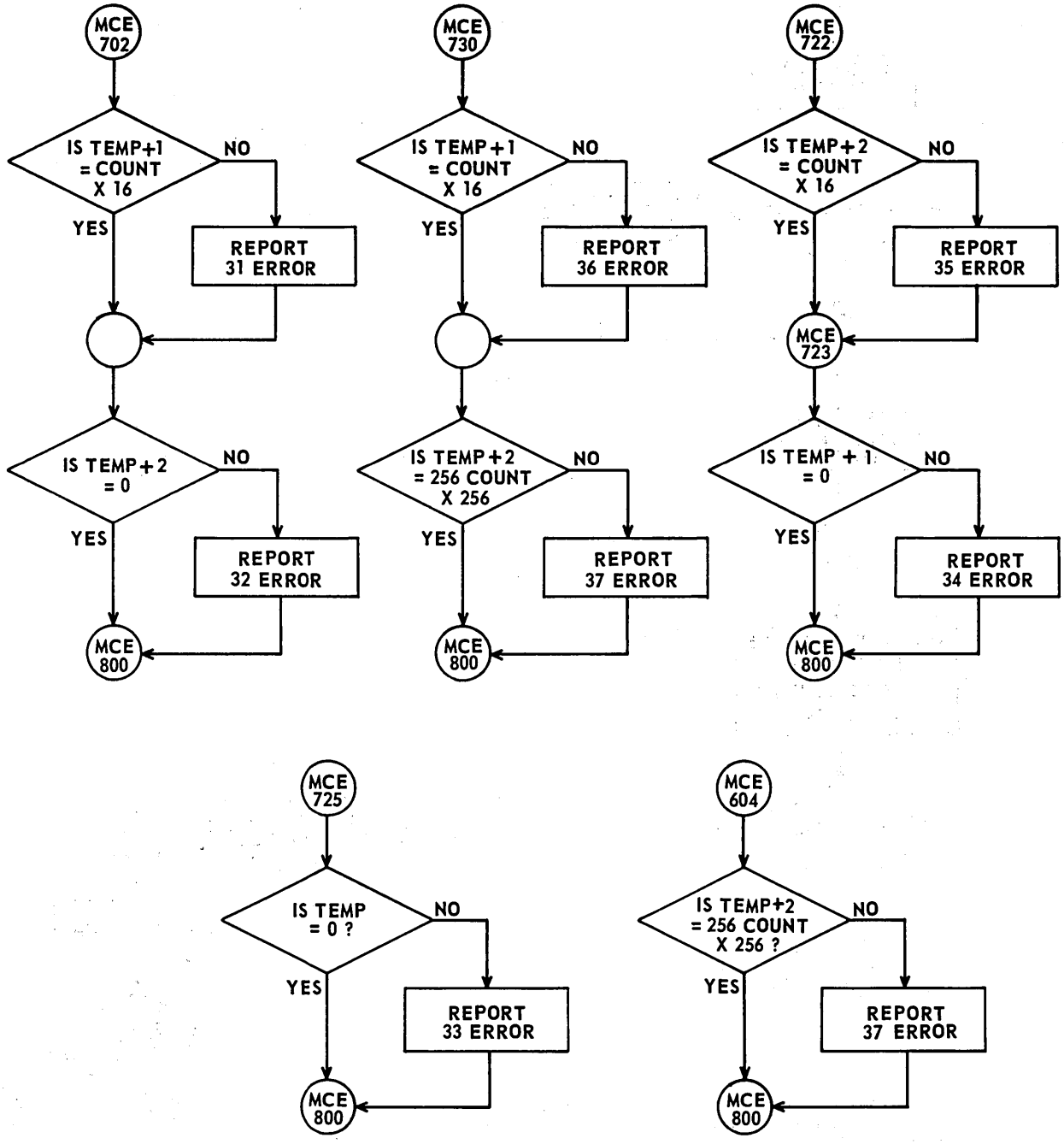
TEST COUNTER MAXIMUM COUNT (2)



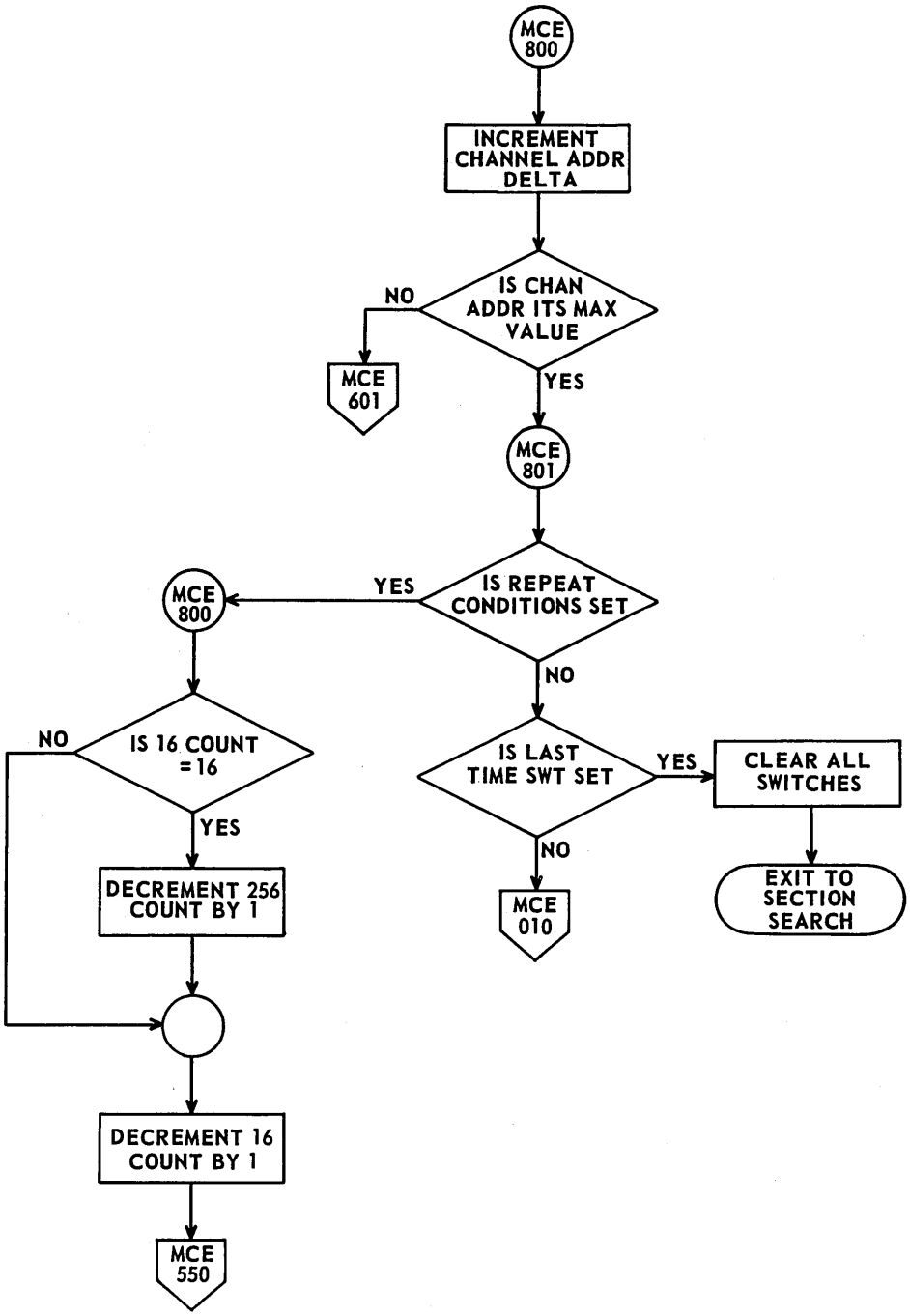
TEST COUNTER MAXIMUM COUNT (3)



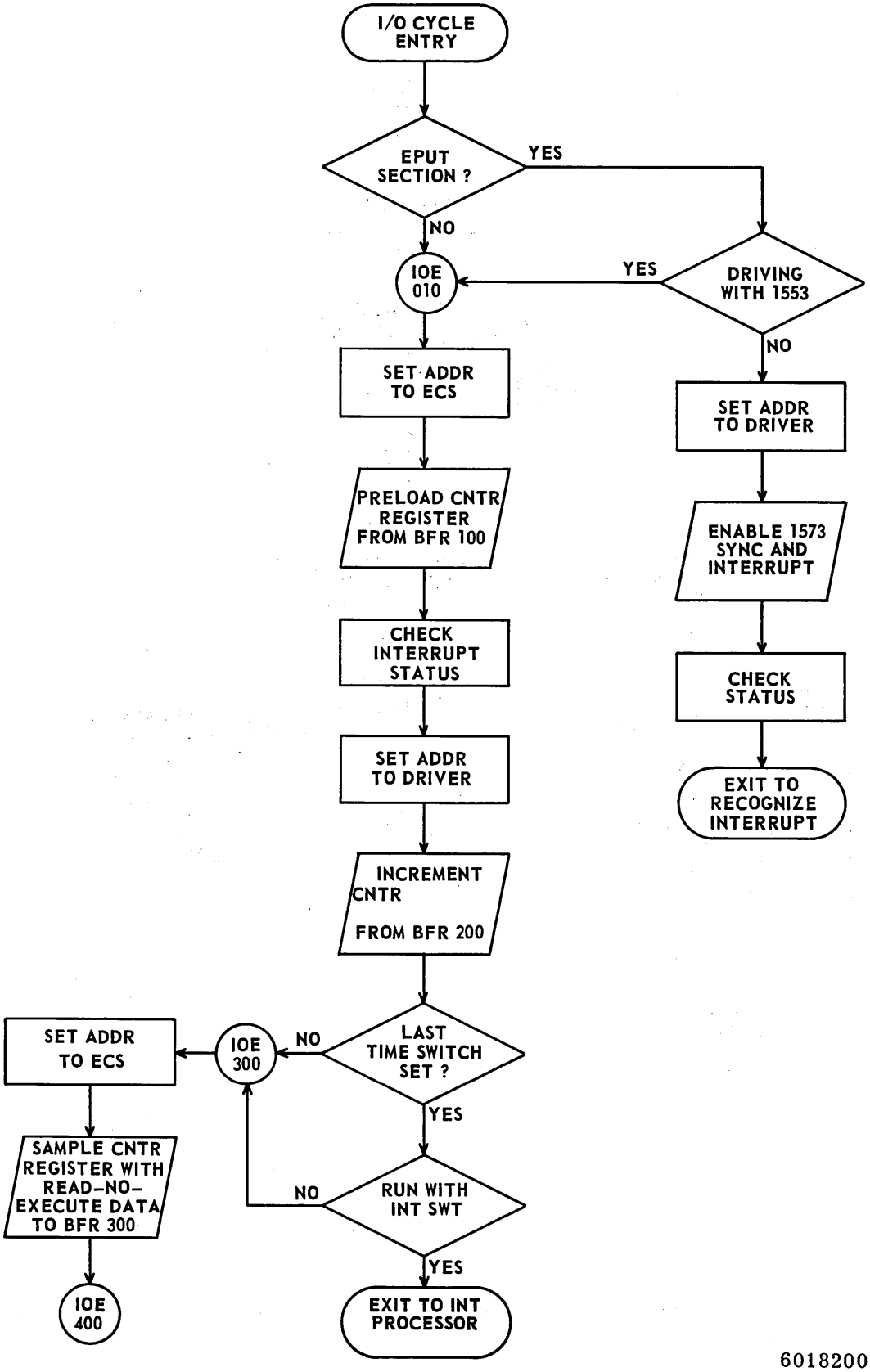
TEST COUNTER SECTION 2 MAXIMUM COUNT (4)



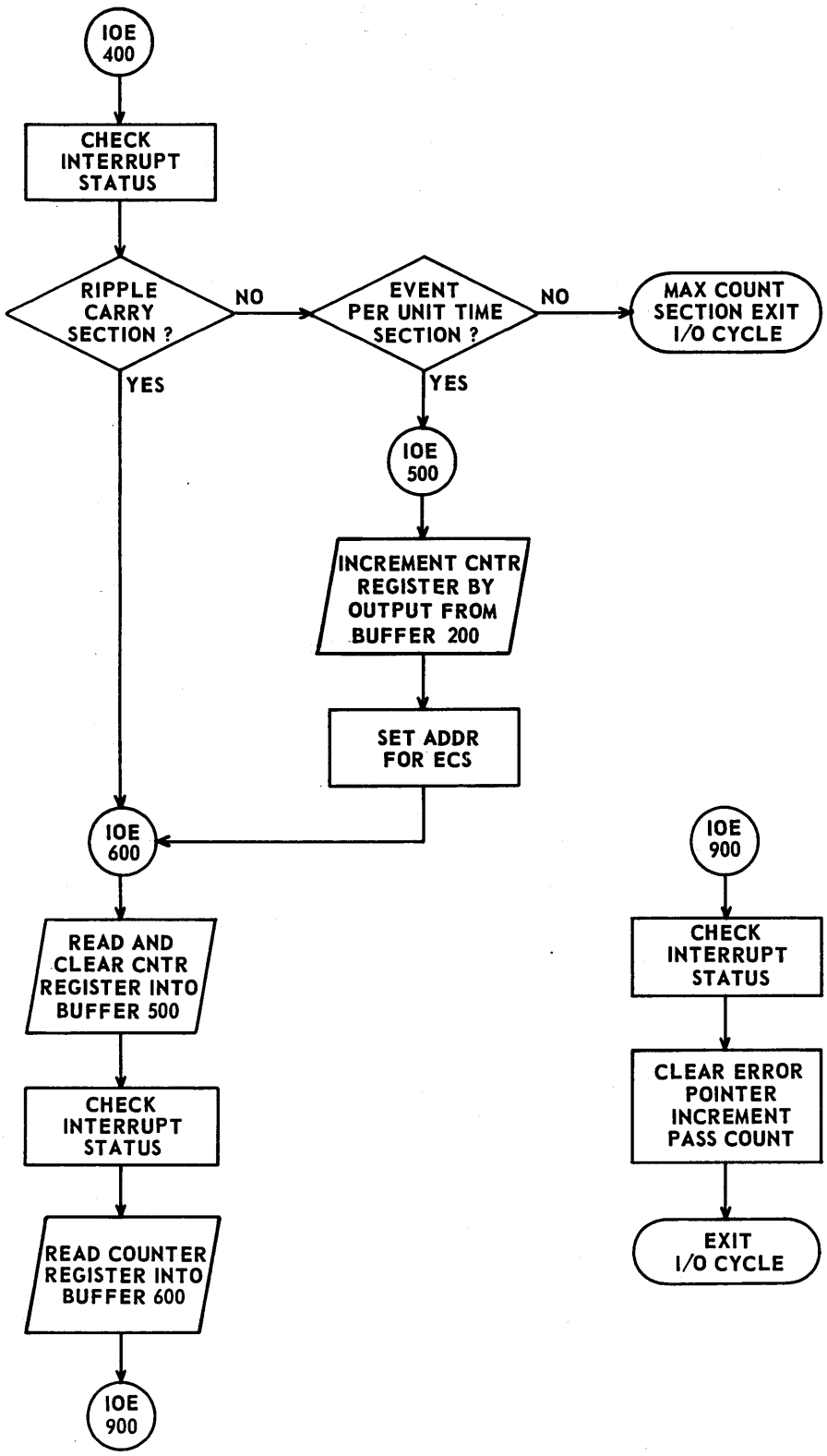
TEST COUNTER SECTION 2 MAXIMUM COUNT (5)



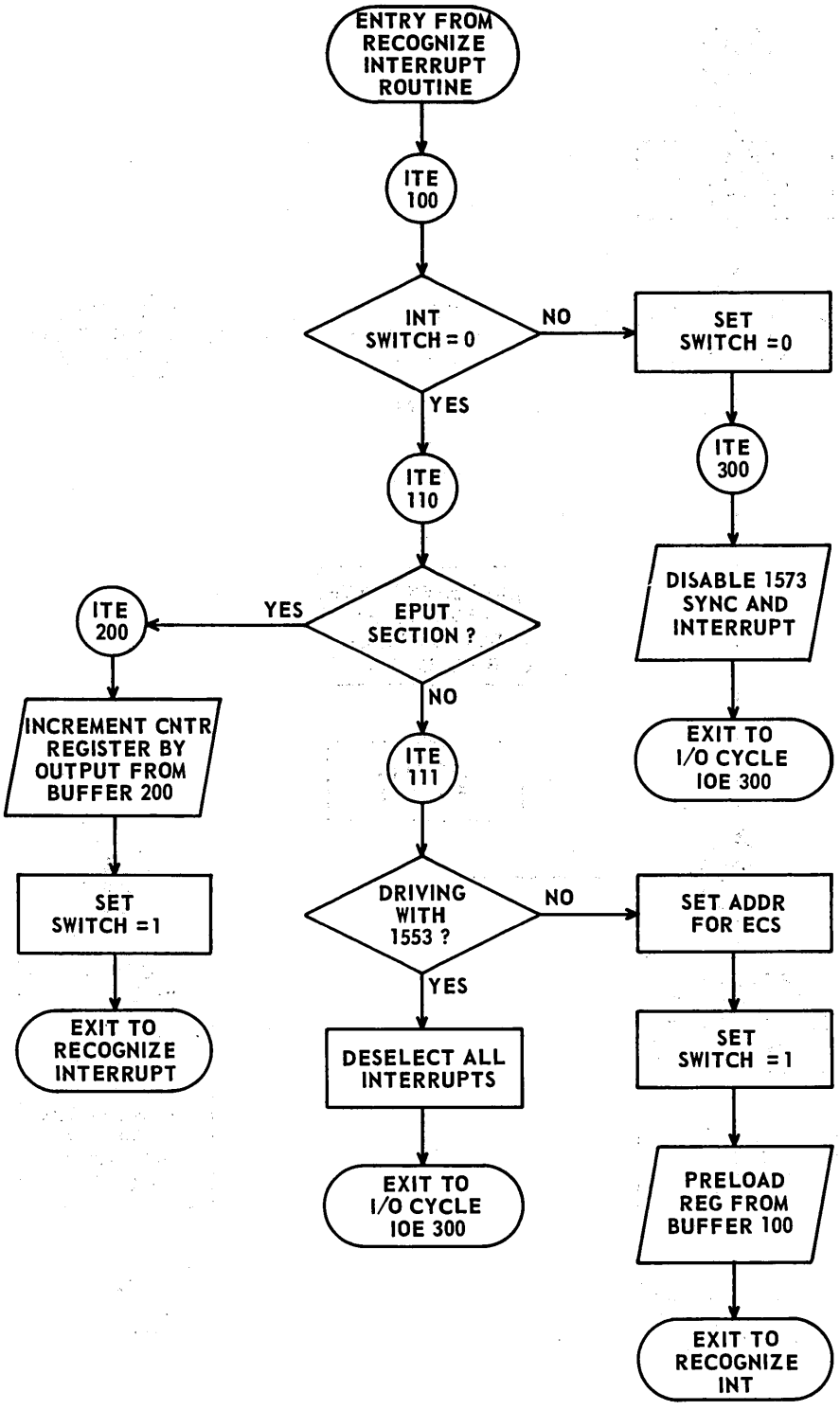
TEST COUNTER SECTION 2 MAXIMUM COUNT (6)


I/O CYCLE ENTRY
EPUT SECTION ?
YES
NO
IOE 010
YES
DRIVING WITH 1553
NO
SET ADDR TO ECS
SET ADDR TO DRIVER
PRELOAD CNTR REGISTER FROM BFR 100
ENABLE 1573 SYNC AND INTERRUPT
CHECK INTERRUPT STATUS
CHECK STATUS
SET ADDR TO DRIVER
EXIT TO RECOGNIZE INTERRUPT
INCREMENT CNTR FROM BFR 200
SET ADDR TO ECS
IOE 300
NO
LAST TIME SWITCH SET ?
YES
SAMPLE CNTR REGISTER WITH READ-NO-EXECUTE DATA TO BFR 300
NO
RUN WITH INT SWT
YES
IOE 400
EXIT TO INT PROCESSOR

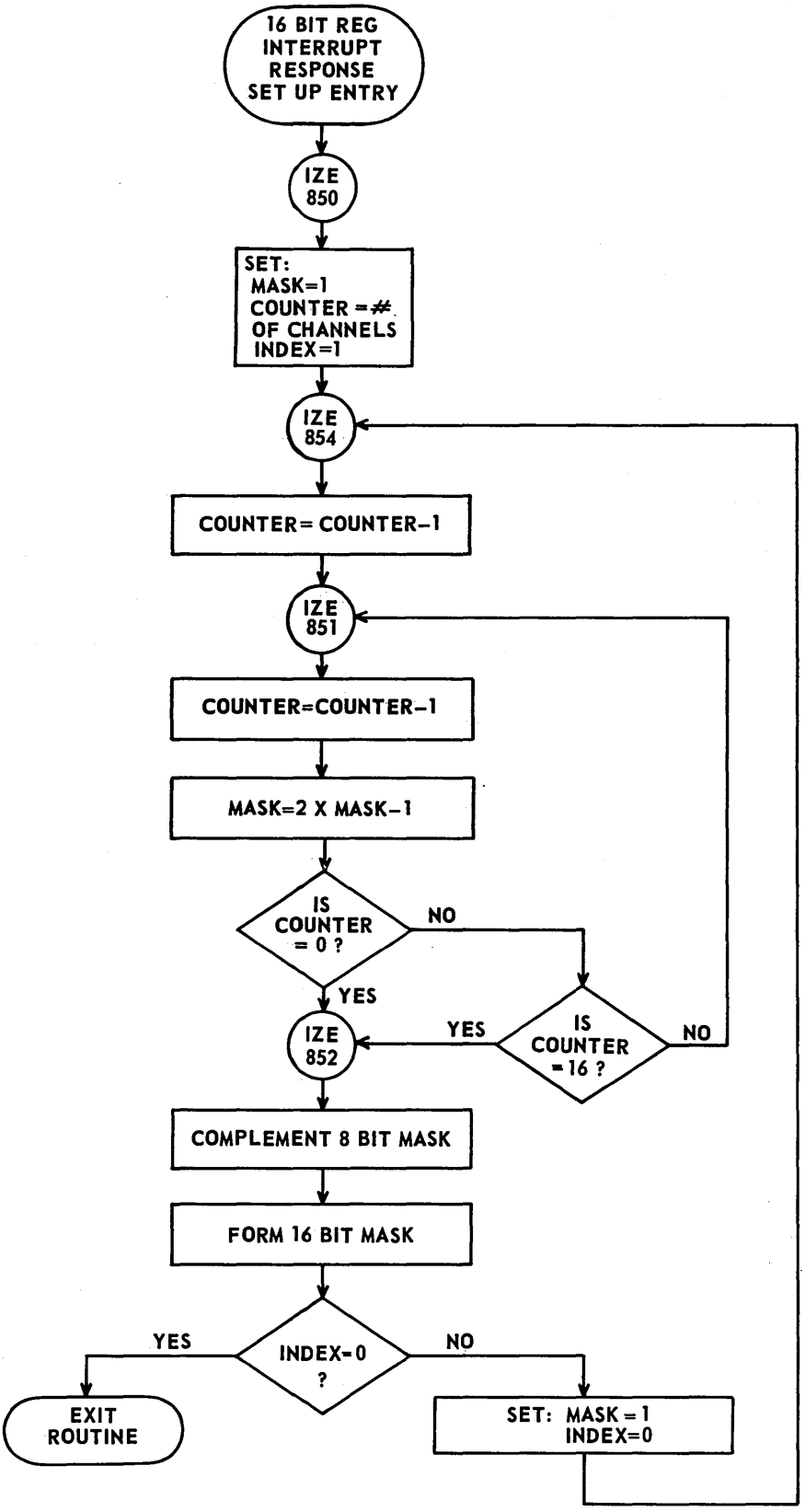
TEST COUNTER I/O CYCLE FLOW DIAGRAM (2)



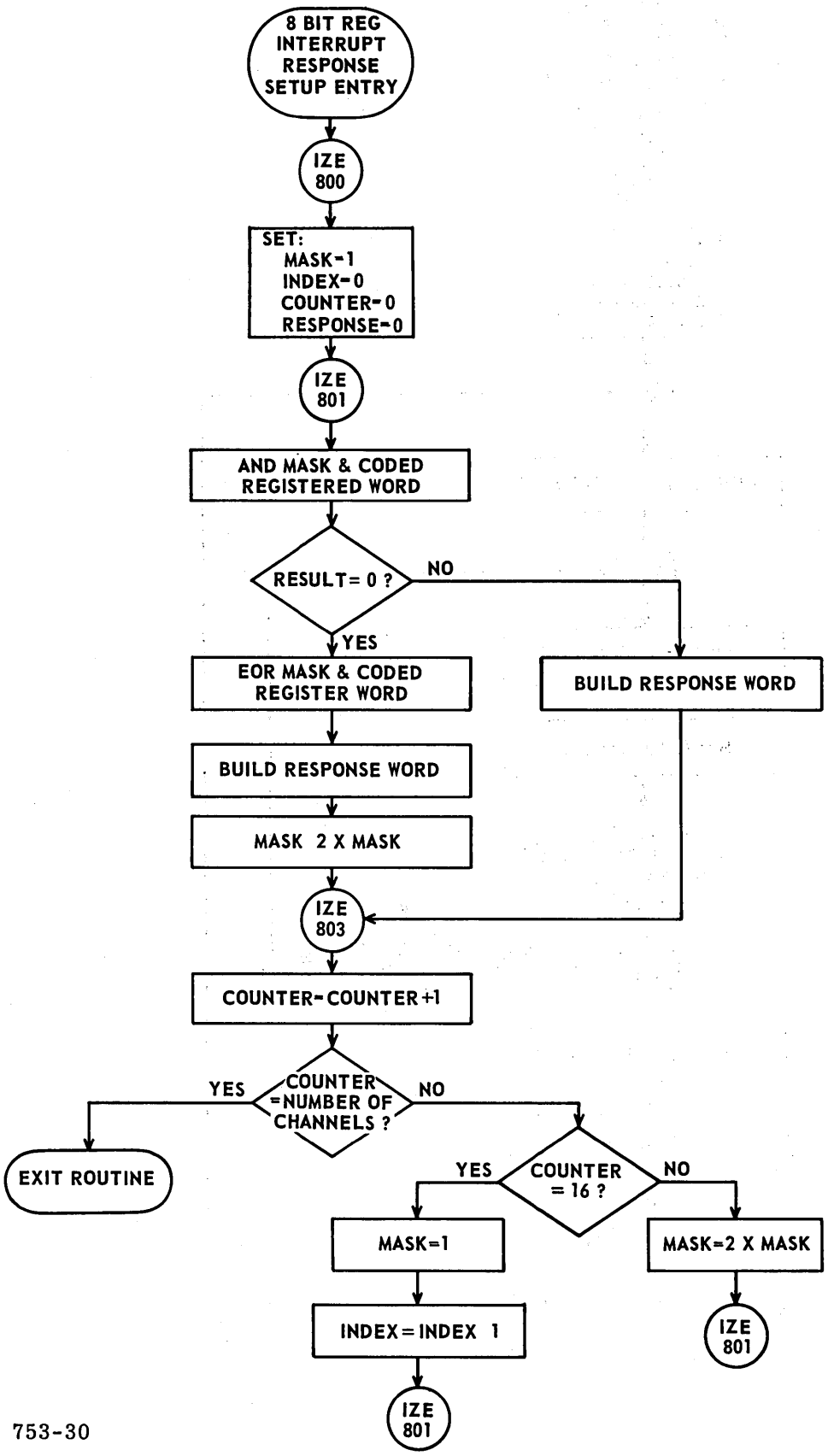
TEST COUNTER INTERRUPT PROCESSOR



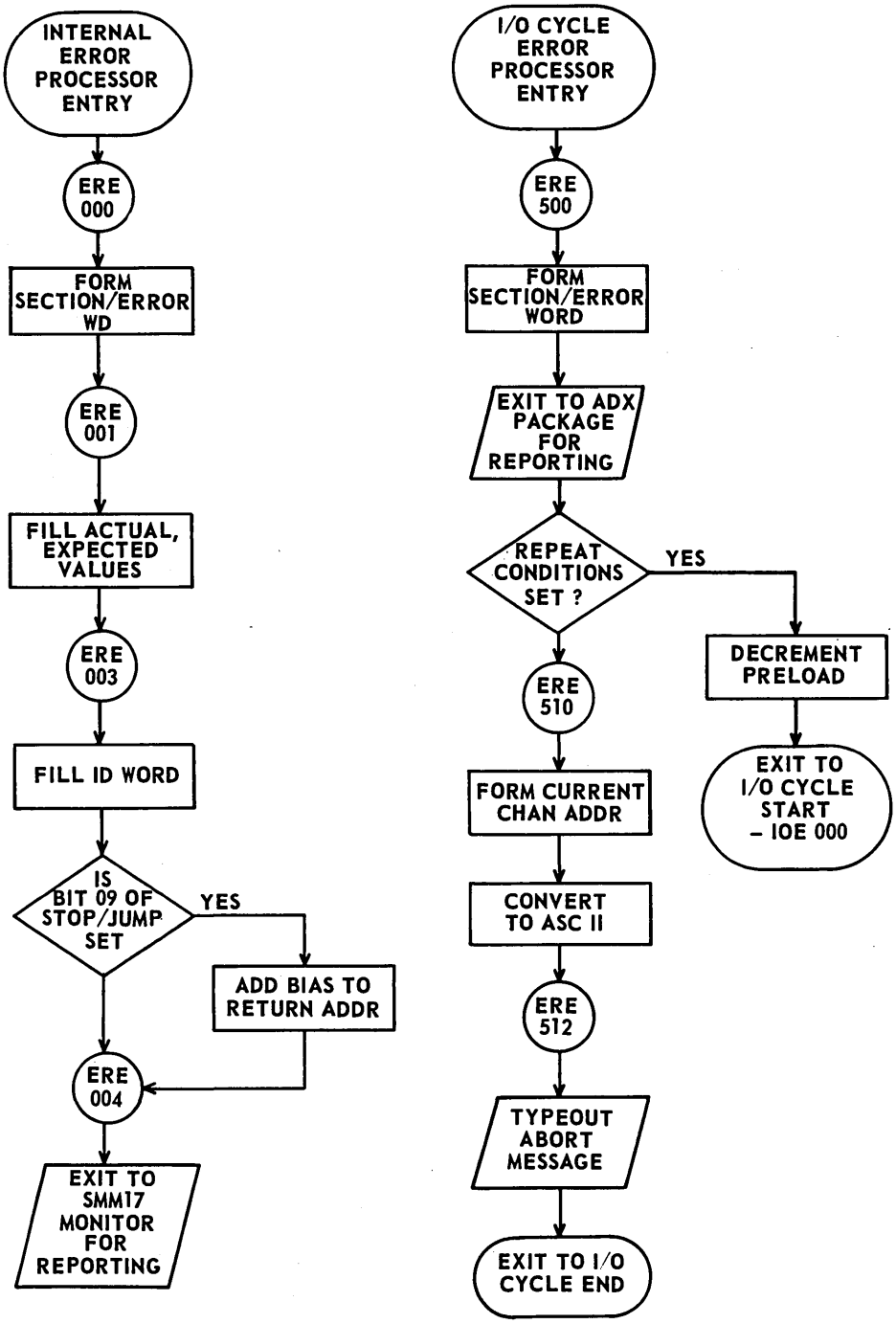
TEST COUNTER – INTERRUPT SETUP – 16 BIT REGISTERS



TEST COUNTER – INTERRUPT SETUP – 8 BIT REGISTERS



TEST COUNTER ERROR ROUTINES FLOW DIAGRAM



DIGITAL INPUT/OUTPUT SUBSYSTEM

(DIO083 Test No. 83)

I. OPERATING PROCEDURES

A. RESTRICTIONS

1. Interrupt lines may not be defined in stop 5 without also defining sync timing in stop 6. Sync timing may be defined without defining interrupts.
2. The data values defined in stop 4 will be used only if bits 10 or 11 of stop 2 (test sections and data patterns) are selected. If bit 10 is selected (non-changing data), the first digital data value defined in stop 4 will be repeated as the output value. If bit 11 is selected (alternating data), both digital values defined in stop 4 will be output.
3. Any combination of data patterns may be defined with any combination of data transfer test sections.
4. Only one type of sync may be defined for test execution. Repetitive sync (bit 0) is to accommodate a cyclic sync signal as would be available from a test oscillator or peripheral equipment. Multiple words will be transferred through each data channel. Manual sync (bit 05) is to accommodate 1 sync pulse per data channel, which might be generated by switches or test clip leads. Only one word is transferred through each data channel.

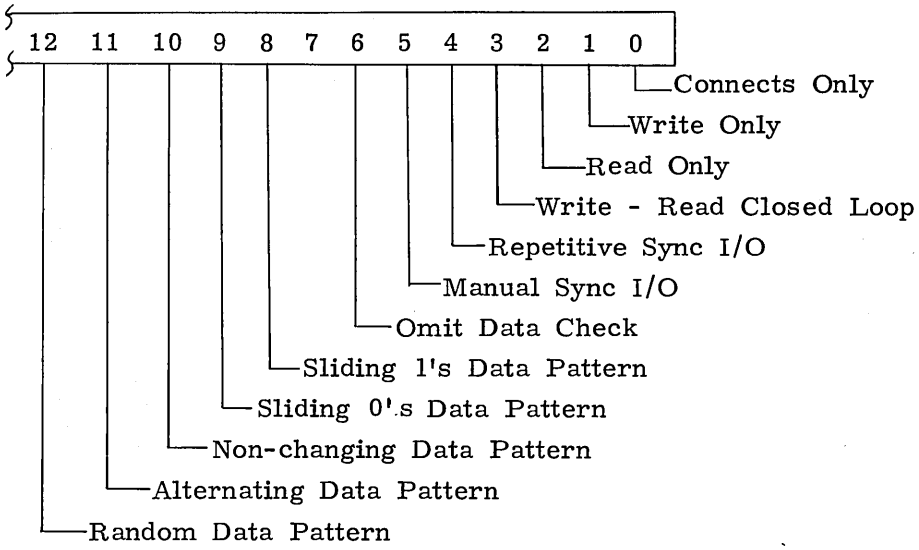
B. PARAMETERS

If bit 0 of the Stop/Jump parameter word is set, the test will stop for one monitor stop and six parameter stops as follows:

First Stop: A: ID Word
Q: Stop/Jump Parameter

Second Stop: A: Test sections, Data Patterns to be Executed
Q: Equipment Adder of the digital Output Unit

A REGISTER:

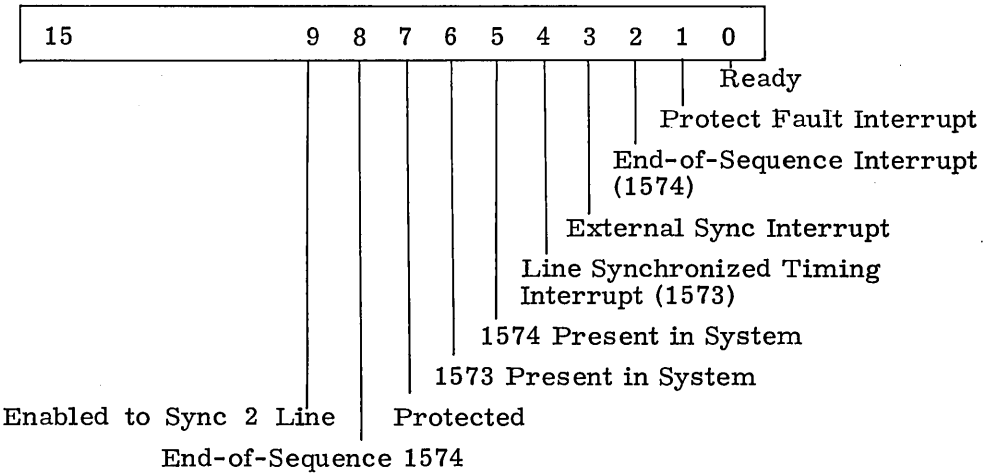


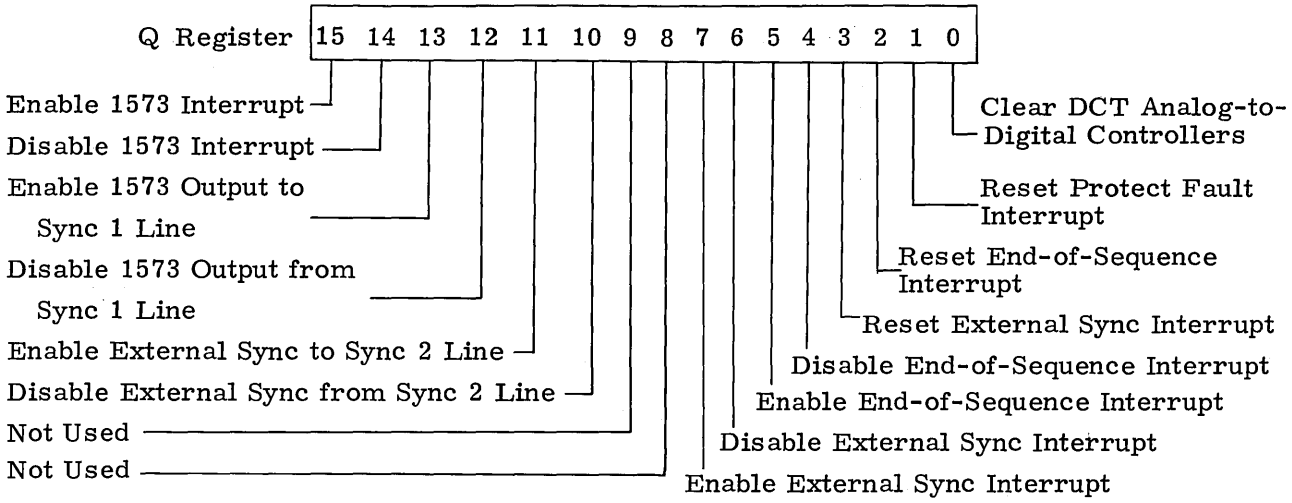
Third Stop: A: First Channel Address of the Digital Output Unit
Q: Last Channel Address of the Digital Output Unit

Fourth Stop: A: First Digital Data Value
Q: Alternate Digital Data Value

Fifth Stop: A: Expected Status 1 Status of DCT
Q: Function Word for Station 0 Output

A Register





Sixth Stop:	A:	Interrupt Line for Output Unit
	Q:	Interrupt Line for Input Unit
Seventh Stop:	A:	Time between Sync Pulses, if in Milliseconds
	Q:	Time between Sync Pulses, if in Microseconds
Eighth Stop:	A:	First Channel Address of the Digital Input Unit
	Q:	Not Used

C. STOP AND JUMP SETTINGS

Bit settings in the Stop/Jump word are the standard SMM assignments:

Bit	Stops
0	Stop to Enter Test Parameters
1	Stop at End of Test Section
2	Stop at End of Test
3	Stop on Error
	Jumps
4	Repeat Conditions
5	Repeat Test Section
6	Repeat Test
7	Not Used
8	Omit Typeouts
9	Display Memory Return Address
10	Re-enter Test Parameters

D. MESSAGES

1. Initial Program Typeout

1553/54-1544/45 DIGITAL I/O TEST 83
IA=xxxx
xxxx = Test Initial Address

2. Completed Pass Typeout

A	Q	A	Q
8324	NUM1	NUM2	NUM3

NUM1 = SMM Parameter Word
NUM2 = PASS Count
NUM3 = Return Address

3. Error Messages

A	Q	A	Q	A	Q	A	Q	A	Q
ID	STJP	SSEE	RTN	MTRERR	IORP	A1	Q1	A2	Q2

Definitions:

ID: SMM Identification Word
STJP: SMM Stop/Jump Parameter Word
SSEE: Test Section and Error Pointer
RTN: Return Address
MTRERR: Monitor Error Code
02 - I/O Response Error
03 - Status Error
04 - Interrupt Time Out Error
05 - Data Compare Error

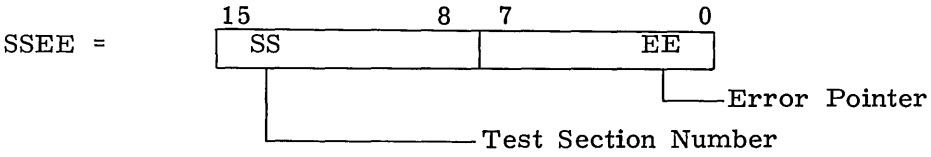
IORP: Last I/O operation performed and the associated response
IO: 10-Write
20-Read
30-Function
40-Status

RP: 10-Reply
20-External reject
30-Internal reject

The information reported in A1, Q1, A2, and Q2 varies with the monitor error code, as defined below:

MTRERR:	A1	Q1	A2	Q2
02	Contents A Reg.	Contents Q Reg.	-	-
03	Contents A Reg.	Contents Q Reg.	Actual Status	Expected Status
04	-	-	Interrupt Line	Expired Time, MS
05	Input Data	Output Data	Input Chan Addr	Output Chan Addr

The SSEE parameter reports the specific location within the test the monitor error code has occurred. This parameter is defined as follows:



The test section numbers are defined as follows:

00- Connects only - Bit 00 of stop 2 A register
01- Writes only - Bit 01 of stop 2 A register
02- Reads only - Bit 02 of stop 2 A register
03- Closed loop - Bit 03 of stop 2 A register

The error pointers are defined as follows:

01- Inputting status from 1750, DCT
02- Outputting function to 1750, DCT
03- Writing data to 1553/1554
04- Reading data from 1544/1545
05- Waiting for write data interrupt
06- Waiting for read data interrupt
0F- Comparing data blocks

See Figure 1 for a flow diagram relating the sequence of error pointers.

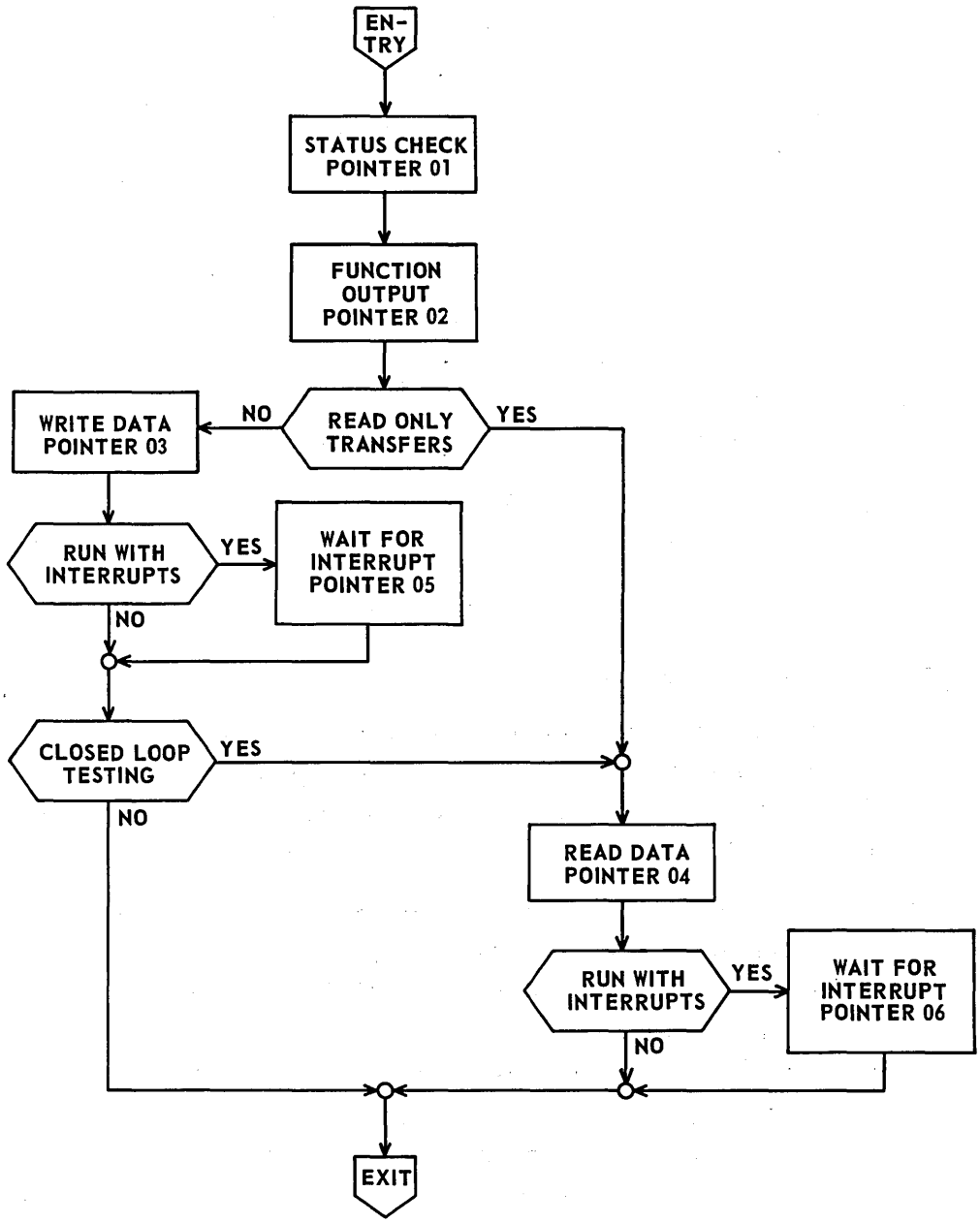


Figure 1. Error Pointer Sequencing

II. DESCRIPTION

A. SECTION 0 - CONNECTS ONLY

The purpose of Section 0 is to exercise the status response and function response of the 1750 (DCT). Section 0 executes I/O to the DCT in three sequences:

1. Two status are input and checked 1000_{16} times.
2. A function is output 1000_{16} times.
3. Status is input and a function is output 1000_{16} times.

For maximum flexability and usefulness, status 1 response and the function word may be defined by the operator. Status 1 is preset to expect only ready status, the function word is preset for clear controller. Status 2 response will always be zero (no interrupts).

B. SECTION 1 - WRITES ONLY

The purpose of Section 1 is two-fold:

1. To output selectable data patterns to the 1553 Digital Output module for use in failure isolation.
2. To provide a driver for exercising and use in failure isolation of the 1554 sync option of the digital output module.

Execution of test Section 1 is controlled by the parameters defined by the operator in stop 2 (see Section I.C.). Five data patterns are available, and each pattern may be run without external sync, repetitive sync, or single manual sync, with or without interrupts.

If only one I/O channel is selected for testing, the test will transfer data through that channel at a 70 kc data rate. If multiple I/O channels are selected, the data rate will be:

$$\text{Data Rate} = \frac{50}{N} \text{ kc}$$

N = Number of I/O Channels, 2 or greater

C. SECTION 2 - READS ONLY

The purpose of Section 2 is two-fold:

1. To repeatedly input data from the 1544 Digital Input module for use in failure isolation.

2. To provide a driver for exercising and use in failure isolation of the 1545 sync option of the digital input module.

Execution of test Section 2 is controlled by the parameters defined by the operator in stop 2 (see Section I.C.). This section may be run without external sync, repetitive sync, or single manual sync, with or without interrupts. The selectable data patterns have no meaning, in that the digital input module will input whatever signals are available at the cable input connector.

If only one I/O channel is selected for testing, the test will transfer data through that channel at a 70 kc data rate. If multiple I/O channels are selected, the data rate will be:

$$\text{Data Rate} = \frac{50}{N}\text{kc}$$

N = Number of I/O Channels, 2 or greater

D. SECTION 3 - WRITE - READ CLOSED LOOP

The purpose of Section 3 is to "echo check" the data path from the A register, out through the 1553 Digital Output module back in through the 1544 Digital Input module. Any or all of the five data pattern options may be used. If test facilities are available, either or both digital output or digital input modules may be run with external sync, with or without interrupts.

The closed loop data transfer is accomplished in the following manner:

1. One word is output to each digital output I/O channel.
2. One word is input from each digital input I/O channel.
3. A and B are repeated until a 256-word data input buffer is full.

At this point the input data buffer is checked against the output data buffer for data accuracy.

III. SUBROUTINES

A. READ - WRITE DATA DRIVER

1. Program Call

RTJ	RDE000/WRE000	
NUM	$xxxx	Number of Words
NUM	$xxxx	First Channel Address
NUM	$xxxx	Number of Channels
ADC	BFR	FWA of Data Buffer
NUM	$xxxx	Number of Reject Retries
JMP*	TAG 1	Busy Return
JMP*	TAG 2	Error Return
JMP*	TAG 3	Normal Return

2. External Characteristics

   a. 96 usec from call to first data transfer.
   b. Single I/O channel data transfers - 14 usec for each word - 70 kc
      multiple I/O channel data transfers 20 usec for each word - 50 kc.
   c. 10 usec from last data transfer to program return.
   d. 20 usec for each reject loop.
   e. Runs with data word interrupts if specified.

3. Internal Characteristics

   a. Routine requires 173 ($AD) core locations.
   b. Run anywhere.
   c. No low core cells required.
   d. Test must set switch to indicate RUN with data interrupts.

B. FUNCTION OUTPUT DRIVER

1. Program Call

RTJ	FNE000	
NUM	$xxxx	Function Word
NUM	$xxxx	Director Bits
NUM	$xxxx	Number of Reject Retries
JMP*	TAG 1	Error Return
JMP*	TAG 2	Normal Return

2. External Characteristics

   a. 28 usec from call to function output execution.
   b. 10 usec from output execution to program return.
   c. 13 usec for each reject loop.

3. Internal Characteristics

   a. Routine requires 58 ($3A) code locations.
   b. Run anywhere.
   c. No low core cells required.
   d. The equipment address to be used is formed by exclusive or'ing the specified director bits with the address contained in the cell WE.

C. STATUS CHECK DRIVER

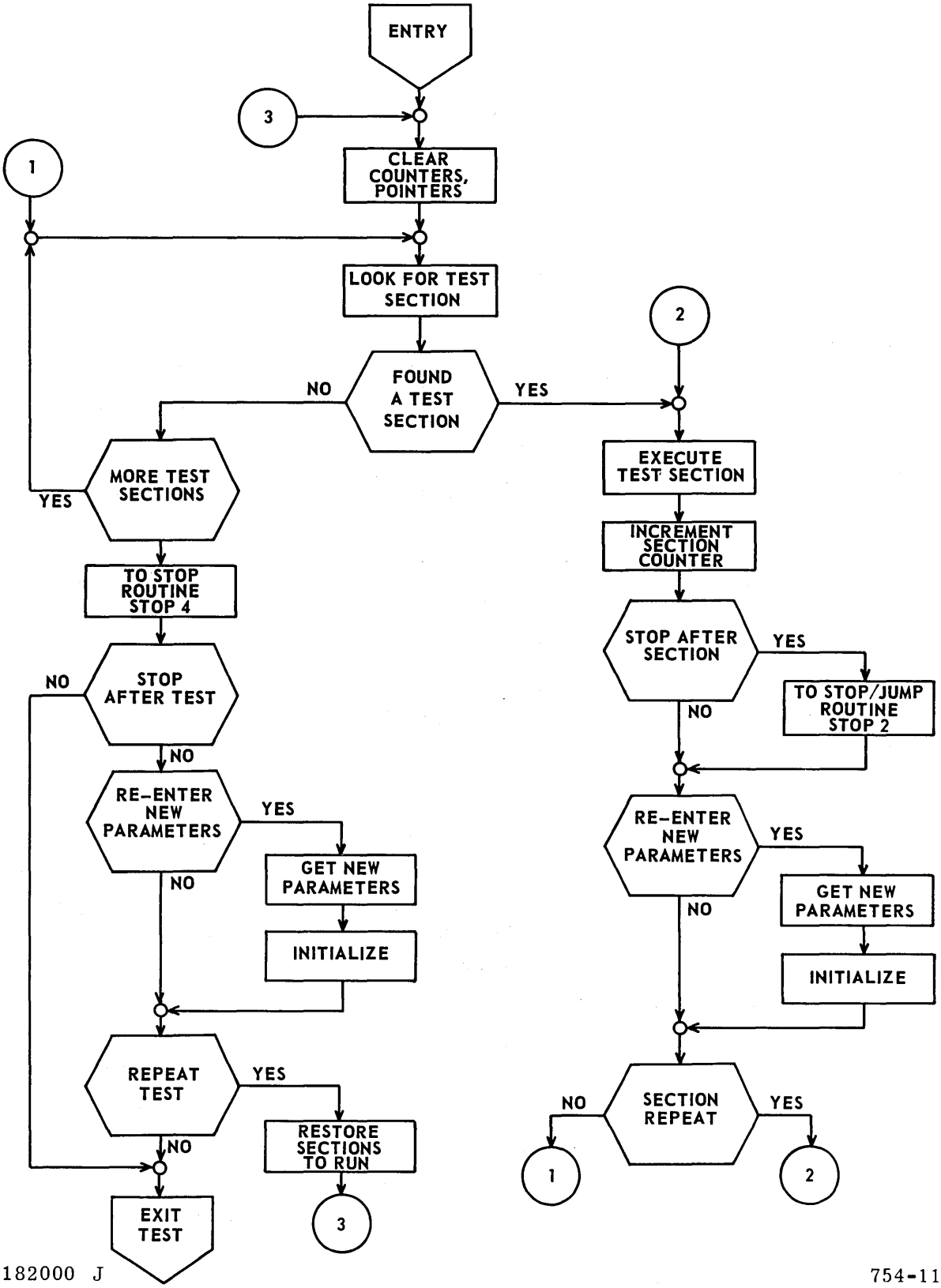
1. Program Call

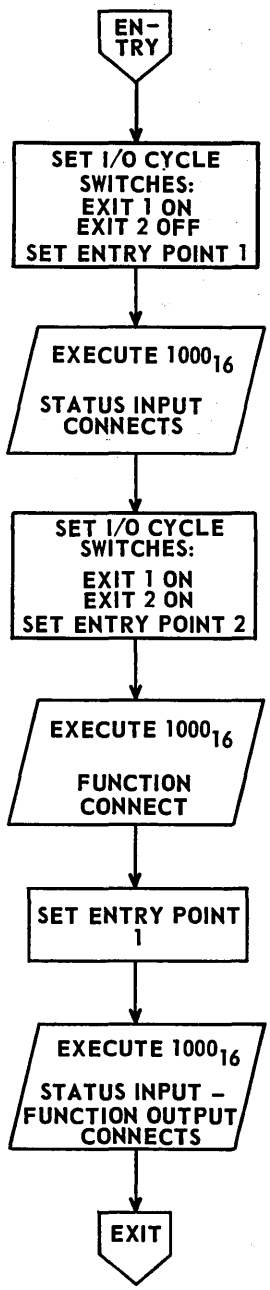
RTJ	CKST	
NUM	$nnnn	Number of Status to Check
NUM	$mmmm	Mask for First Status Value
NUM	$vvvv	Expected Value of First Status
NUM	$mmmm	Mask for Second Status Value
NUM	$vvvv	Expected Value of Second Status
JMP*	TAG 1	Error Return
JMP*	TAG 2	Normal Return

2. External Characteristics

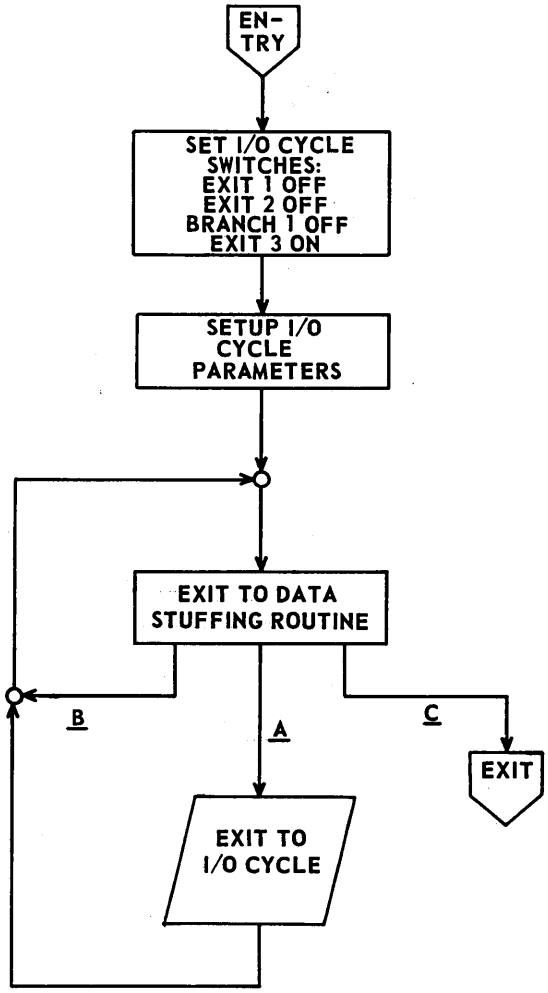
   a. Up to four status may be checked.
   b. 18 usec from call until first status copied.
   c. 14 usec between each succeeding status copied.

DIO TEST EXECUTION CONTROL



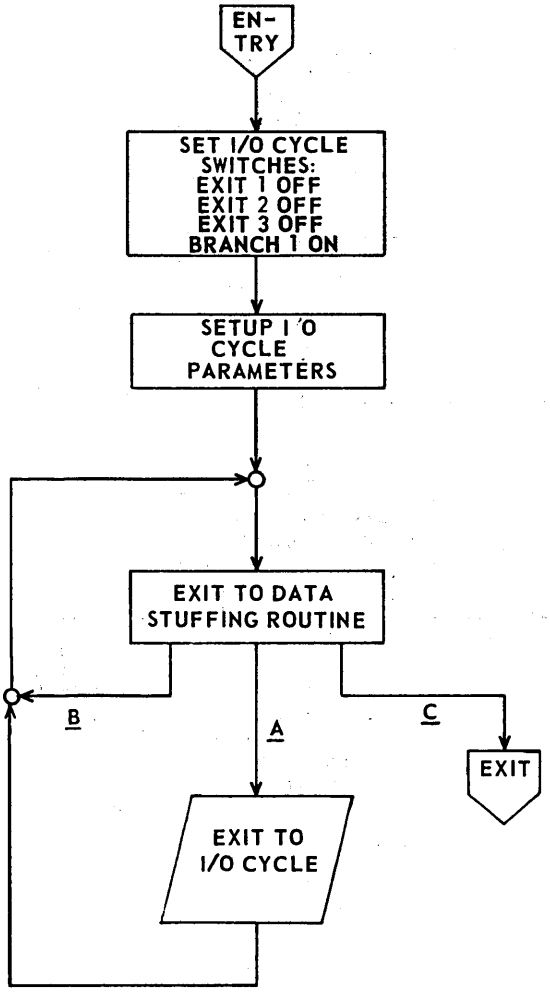


DIO TEST SECTION 0 – CONNECTS



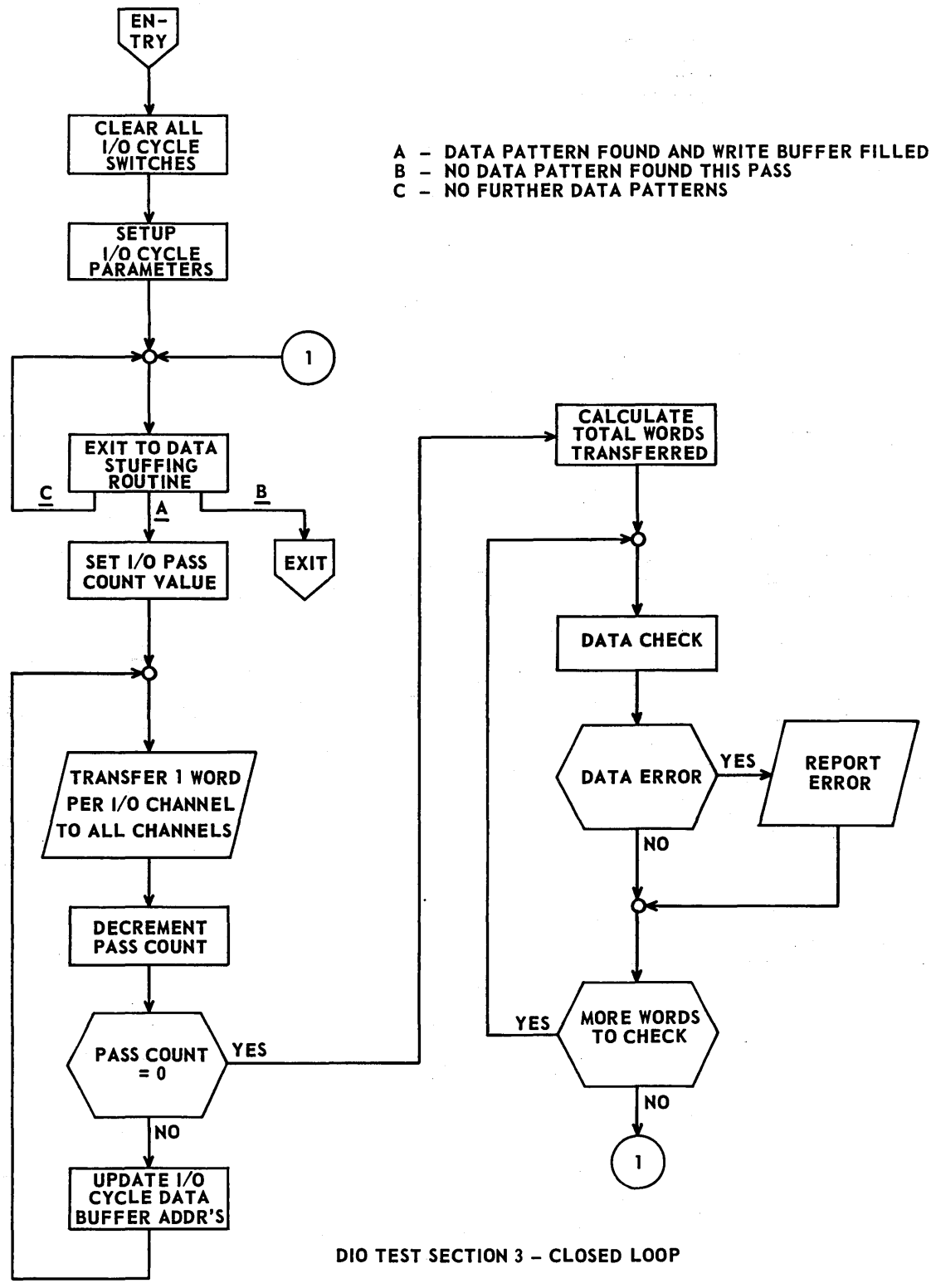
A – FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER
B – NO DATA PATTERN FOUND THIS PASS
C – NO FURTHER DATA PATTERNS

DIO TEST SECTION 1 – WRITES

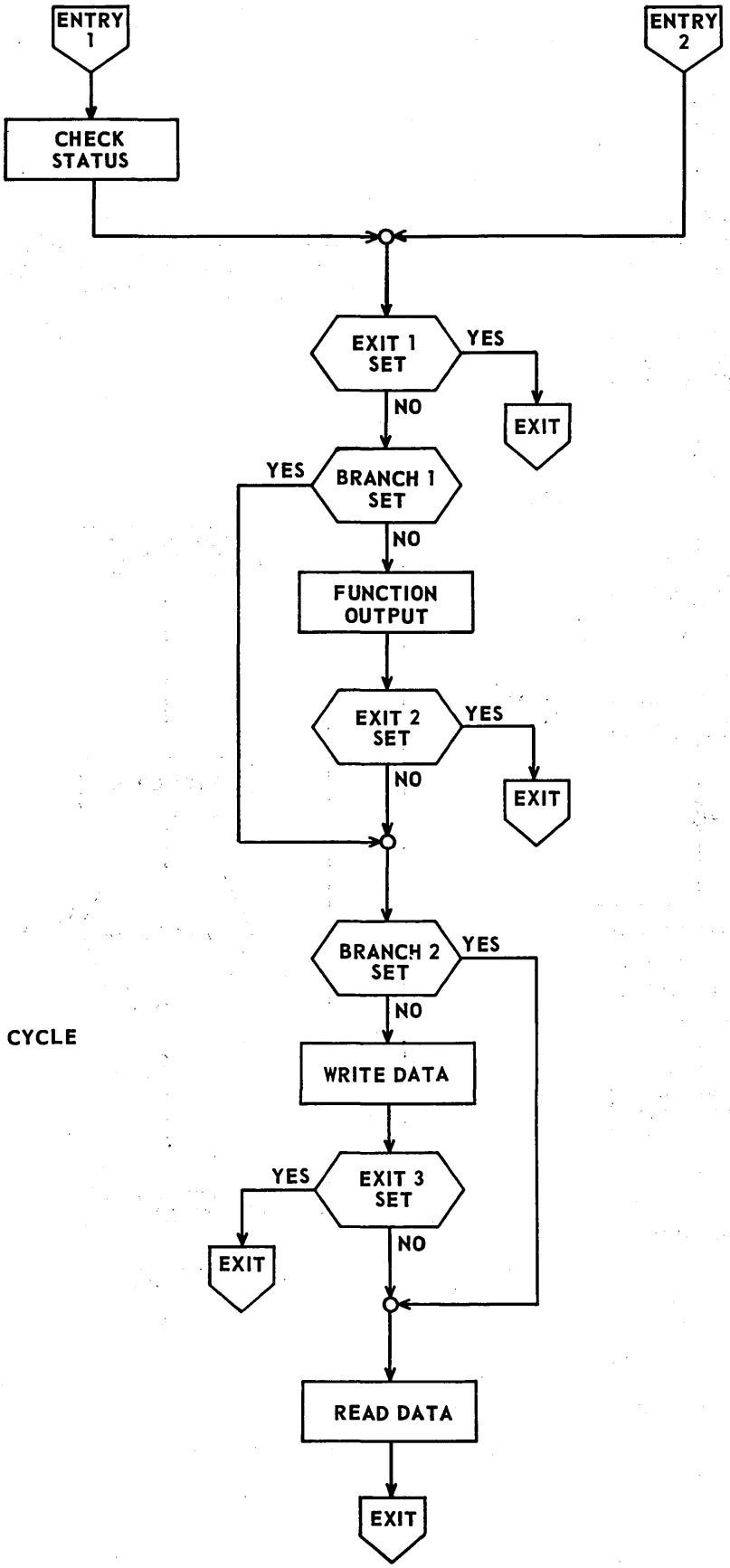


A – FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER
B – NO DATA PATTERN FOUND THIS PASS
C – NO FURTHER DATA PATTERNS

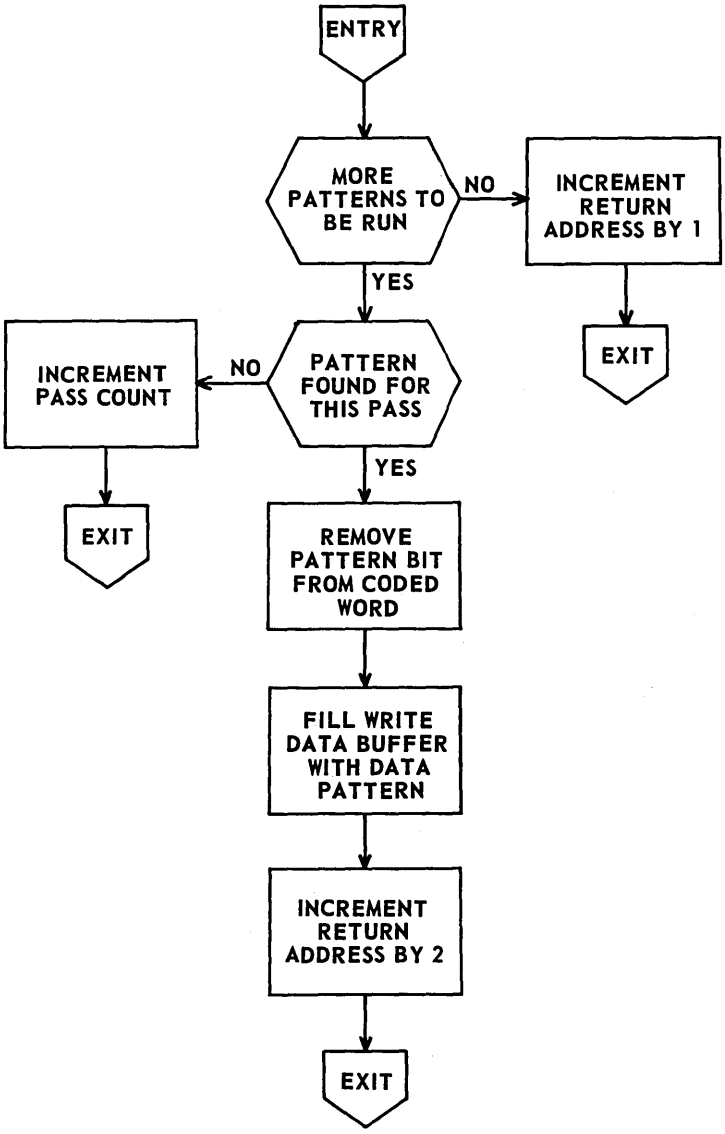
DIO TEST SECTION 2 – READS



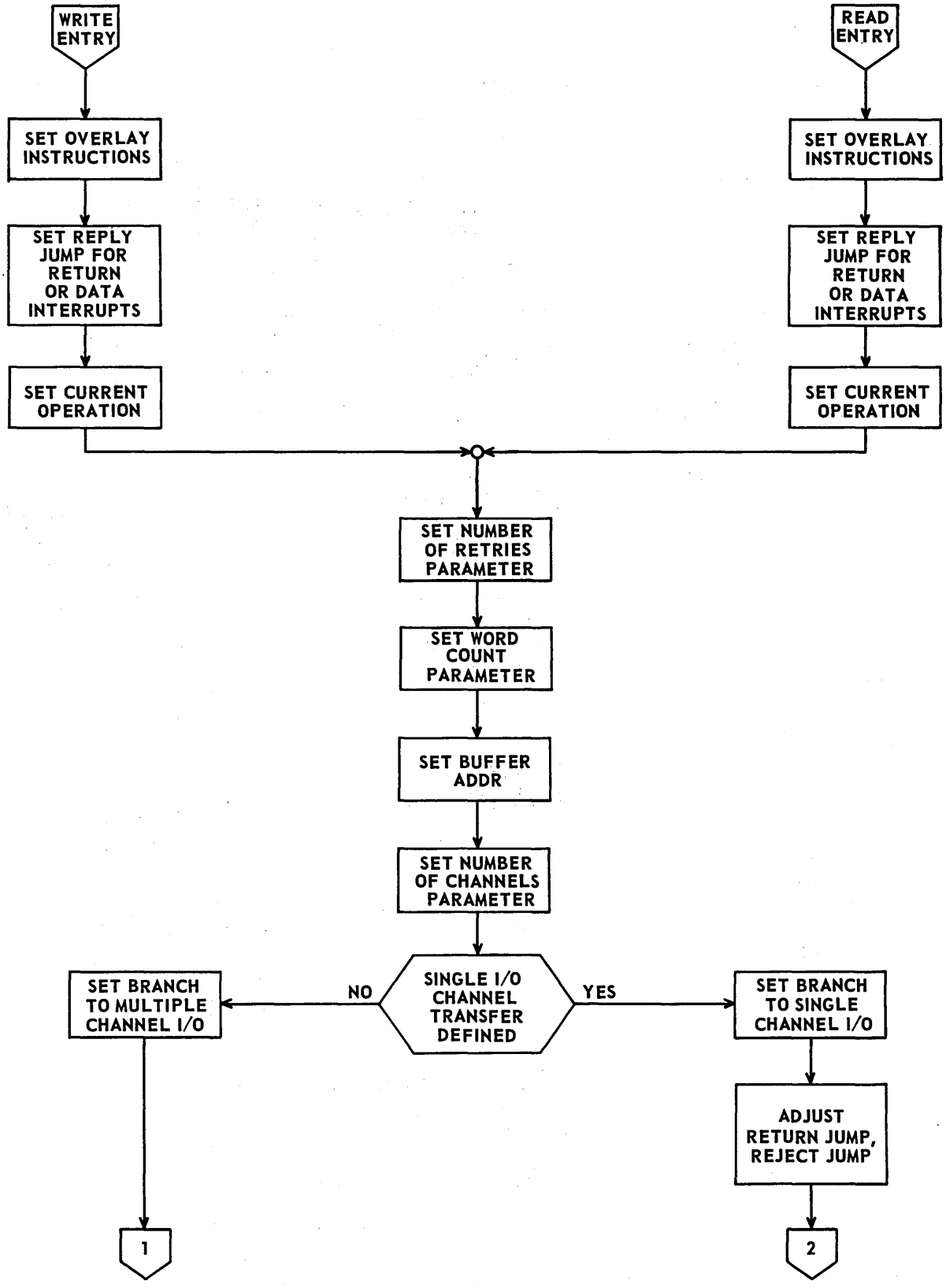
DIO TEST SECTION 3 – CLOSED LOOP



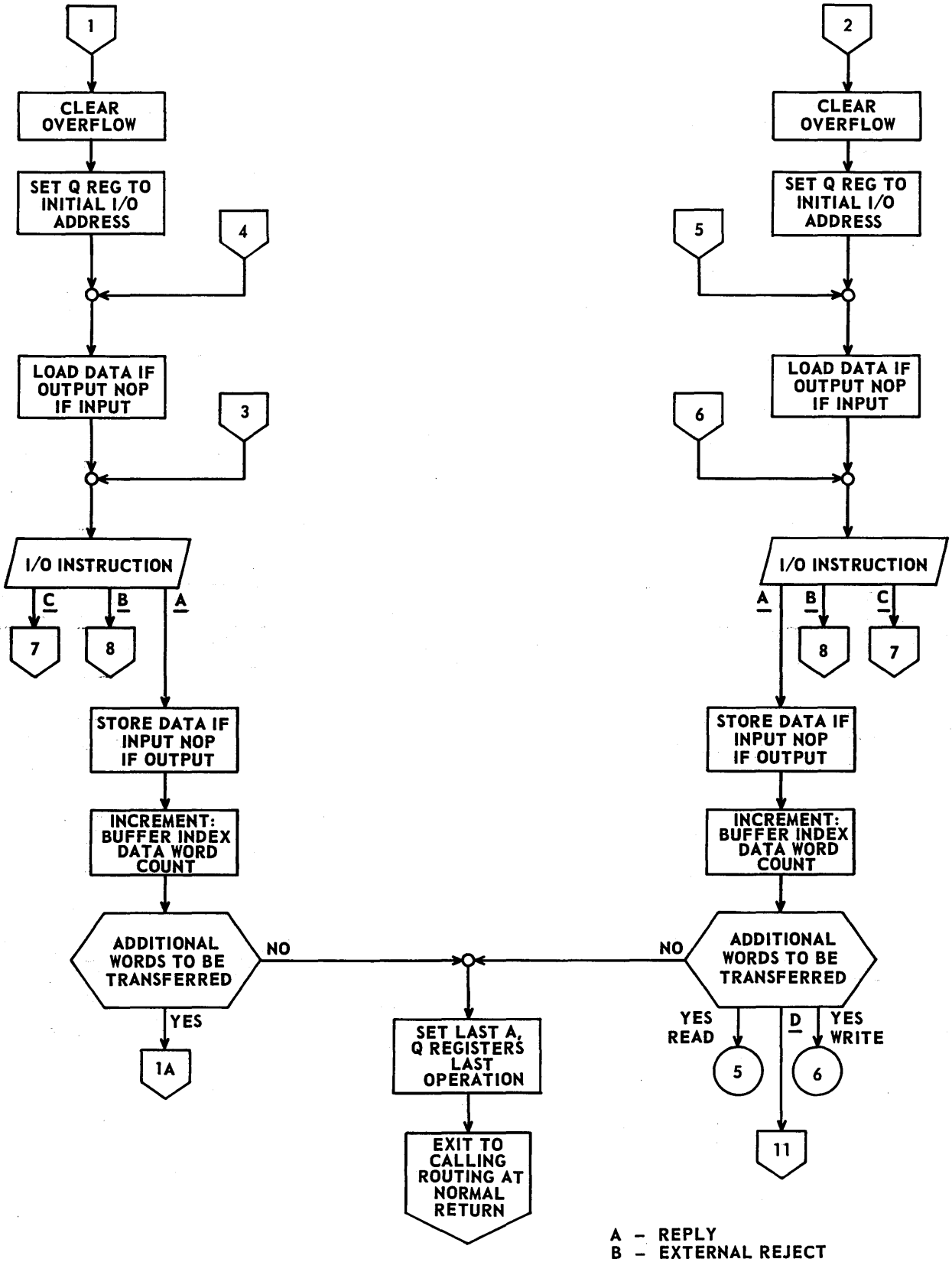
DIO TEST I/O CYCLE



DIO TEST DATA STUFFING ROUTINE

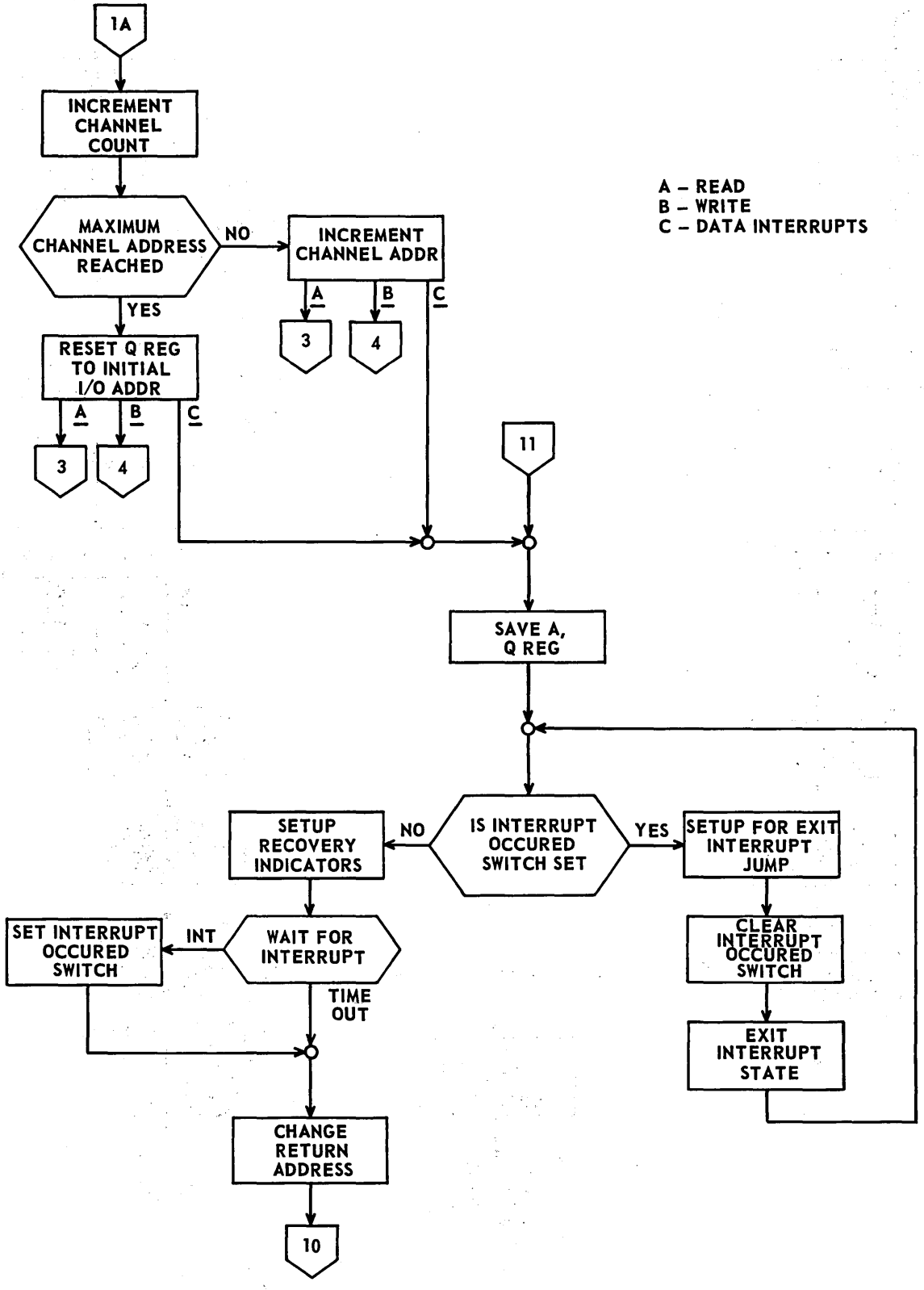


READ/WRITE DRIVER – SETUP

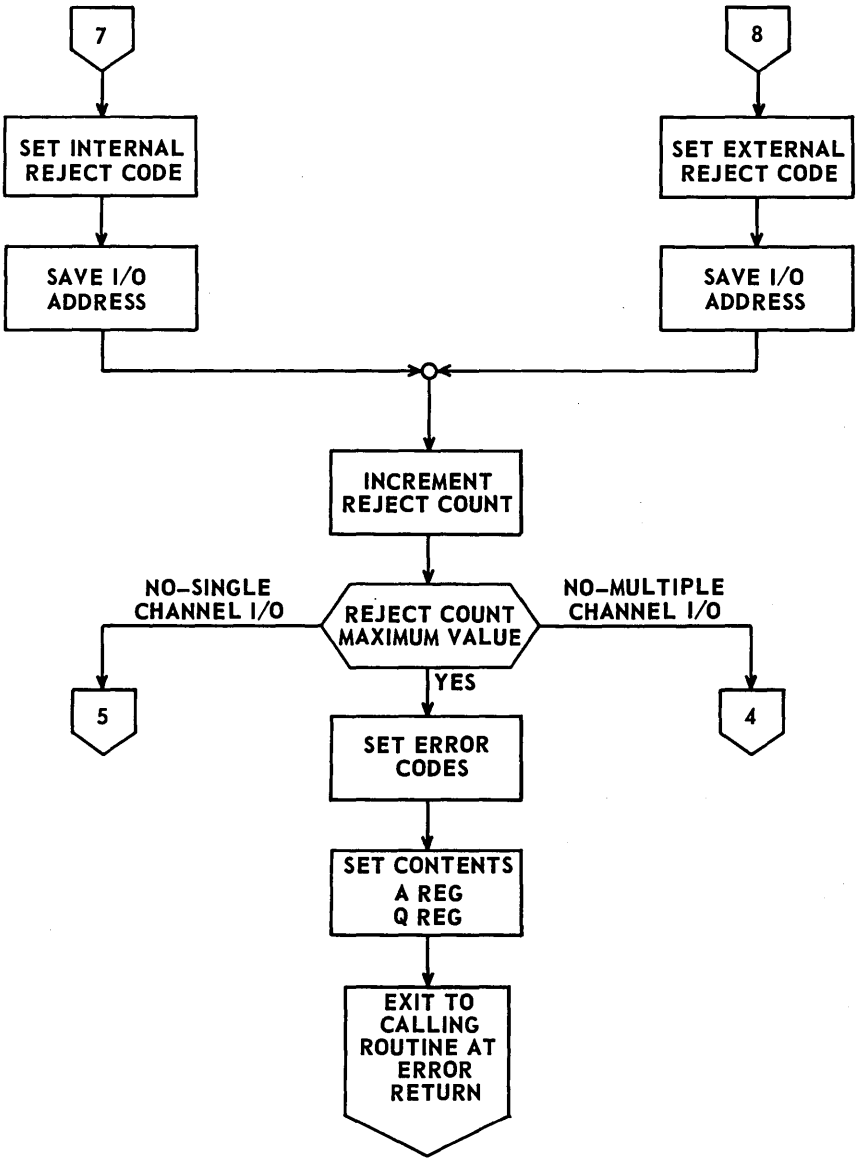


A – REPLY
B – EXTERNAL REJECT
C – INTERNAL REJECT
D – INTERRUPTS

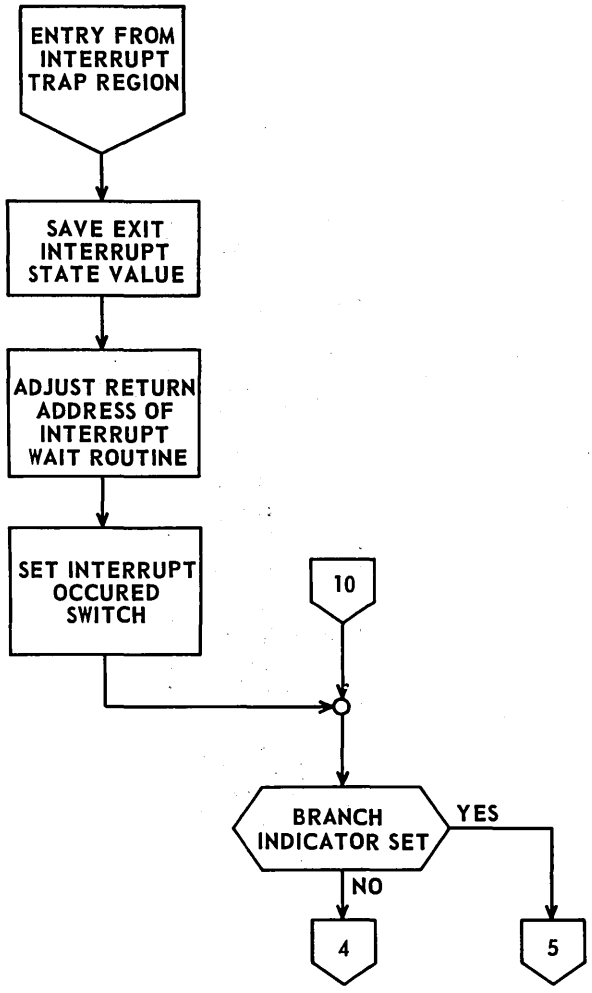
READ/WRITE DRIVER – DATA TRANSFERS



READ/WRITE DRIVER – INTERRUPT PROCESSOR



READ/WRITE DRIVER – REJECT PROCESSING



READ/WRITE DRIVER – INTERRUPT SETUP

IOM MOTHER UNIT DIAGNOSTIC

(IOM090 Test No. 90)

I. OPERATING PROCEDURES

A. RESTRICTIONS/LIMITATIONS

1. Interrupt lines may not be defined in Stop 7 without also defining sync timing in Stop 8. Sync timing may be defined without defining interrupts.
2. The data values defined in Stop 6 will be used only if bits 5, 9, or 11 of A register Stop 3, test sections and data patterns, are selected. If Q register bit 02 is selected (non-changing data), the first digital data value defined in Stop 6 will be repeated as the output value. If bit 3 is selected (alternating data), both digital values defined in Stop 6 will be output.
3. Any combination of data patterns may be defined with any combination of data transfer test sections.
4. Only one type of sync may be defined for test execution. Repetitive sync (bit 12) is to accommodate a cyclic sync signal as would be available from a test oscillator or peripheral equipment. Multiple words will be transferred through each data channel. Manual sync (bit 13) is to accommodate one sync pulse per data channel, which might be generated by switches or test clip leads. Only one word is transferred through each data channel.
5. Test Section 6 requires that the operator ground a test point to produce an interrupt. This ground must be maintained at least for 2 seconds to combat contact bounce.
6. Bit A15 of Stop 3 (Address Increment) must be set to properly execute test Sections 0 through 5. With this bit set, the I/O address will increment when a monitor stop is processed. If not set, the address will not change.

B. LOADING PROCEDURE

This test is to be loaded as a standard SMM17 3.0 Library Test. The test may be loaded anywhere in core memory by using the following optional procedure when building the test execution list:

1. (A) is normally the test number and number of times to be run. Set the A register to $FF00 test number $FF to be run 0 times.

2. (Q) is normally the equipment number of the device under test. Set the Q register to the desired core location to begin loading the test. This location must not be less than $0D00 so as not to destroy the monitor.

Standard execution parameters from load time are to execute test Sections 9, 10, and 11 (write only, read only, and write/read closed loop). These sections will be executed using all six data patterns (sliding 1's, sliding 0's, unchanging (repetitive 0's) alternating data (all 0's, all 1's), pseudo - random data, and frequency sensitive data). This data will be output on unit address 000 through 003 and read back in through addresses 004 through 007. The equipment code used will be that established while building the test list. These data transfers will be asynchronous without interrupts. For a valid data check, 1 to 1 cables must be used to transfer the data from the digital outputs to the digital inputs.

Sections 0 through 6 are to be used when troubleshooting suspected hardware. Flexibility has been built in through the operator defined parameters to cover most if not all failure modes. Hand routines should not be required.

C. PARAMETERS

If bit 0 of the Stop/Jump parameter is set, the test will stop for one monitor stop and seven parameter stops as follows:

Stop 1:	A:	ID Word
	Q:	SMM Stop/Jump Word
Stop 2:	A:	Unused
	Q:	Equipment Number for Data Writes
Stop 3:	A:	Sections to Run (Figure 1)
	Q:	Data Patterns to Run (Figure 1)
Stop 4:	A:	Starting Unit Address - Writes
	Q:	Ending Unit Address - Writes
Stop 5:	A:	Starting Unit Address - Reads
	Q:	Equipment Number for Reads
Stop 6:	A:	First Digital Output Word
	Q:	Alternate Digital Output Word
Stop 7:	A:	Interrupt Line for Output Units*
	Q:	Interrupt Line for Input Units*
Stop 8:	A:	Time to Wait for Interrupts, milliseconds
	Q:	Time to Wait for Interrupts, microseconds

*Bit 1 defines line 1, Bit 2 defines line 2, etc.

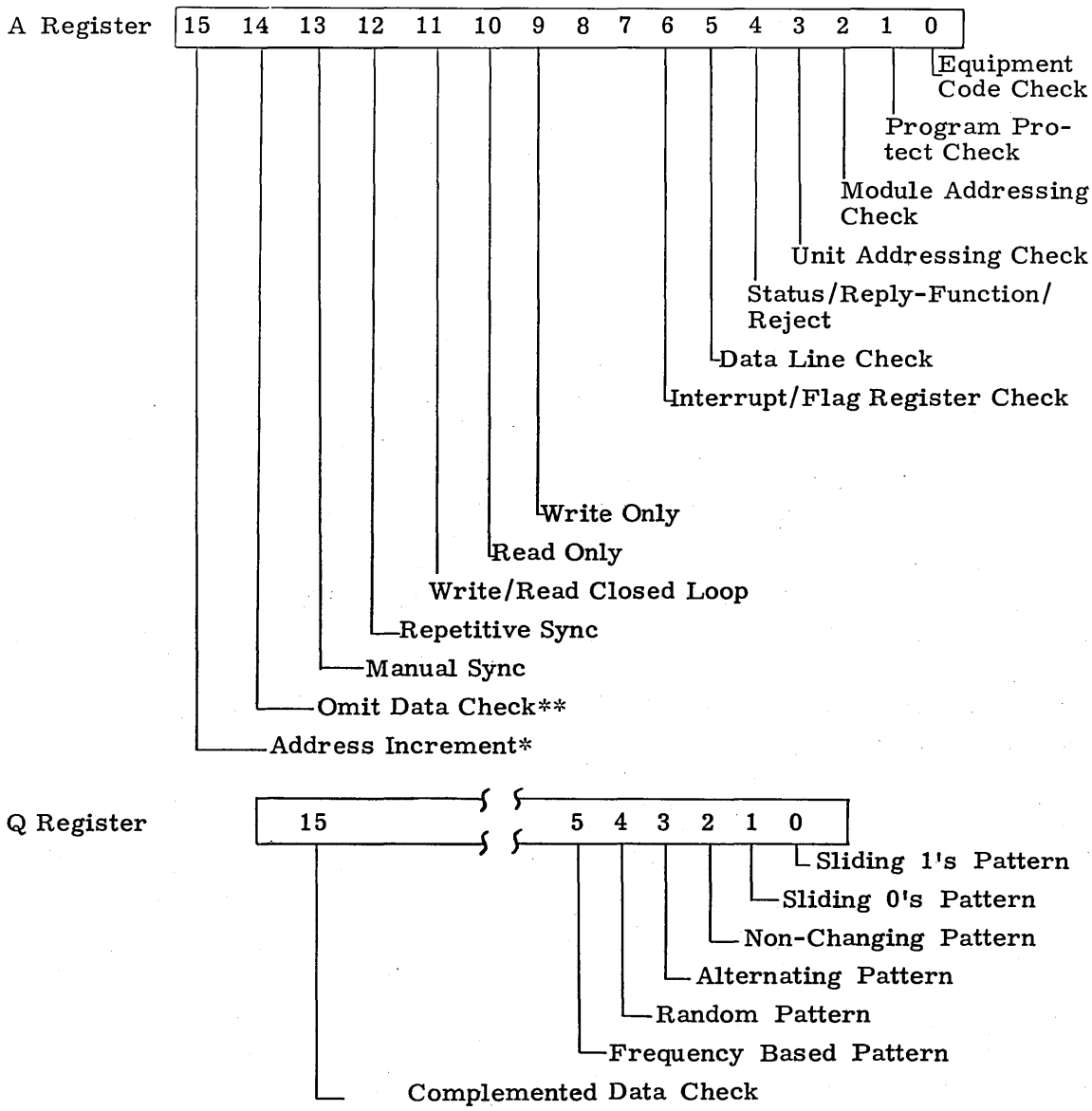


Figure 1. Parameter Stop 3
Test Sections/Data Patterns

*Must be set to increment the I/O address in Sections 0 through 5.
**Set to delete the data check of Section 11.

D. STOP AND JUMP SETTINGS

Bit settings in the Stop/Jump word are the standard SMM assignments.

Bit	Stops
0	Stop to Enter Test Parameters
1	Stop at End of Test Section
2	Stop at End of Test
3	Stop on Error
	Jumps
4	Repeat Conditions
5	Repeat Test Section
6	Repeat Test
7	Not Used
8	Omit Typeouts
9	Display Memory Return Address
10	Re-enter Test Parameters

E. MESSAGES

1. Initial Program Typeout

   IOM Mother Unit

   Digital Output/Input Test 90

   VER 3.1 IA = aaaa FC = xxxx

   aaaa = Test Initial Address

2. Completed Pass Typeout

A	Q	A	Q
9024	NUM 1	NUM 2	NUM 3

   NUM 1 = SMM Stop/Jump Word
   NUM 2 = Pass Count
   NUM 3 = Return Address

3. Parameter Stop Typeout

   After completing each parameter stop (Stop 0), the parameter block will be typed out. For this test there will be eight A/Q pairs of data presented.

4. Teletype Input Driver

Setting bit 6 of the monitor control word prior to executing quick look or during any monitor parameter stop, will select the teletype input driver. This driver will allow all operator intervention to be done through the TTY rather than from the console registers. The following are the general guide lines controlling the use of this driver:

a. The driver will first type two 4-character hexadecimal numbers which represent an A/Q pair of standard or current parameters to be altered, followed by a line feed, carriage return = 9001/0600.

b. The operator now has the following options:

1) A carriage return will signify the input is complete. If this is the only input, no parameter changes will take place.

2) A slash will signify the end of one parameter input. An input of:

/0 CR will indicate the parameter output is to be changed in core to be 9001/0000.

3) All hexadecimal numbers on input must be preceded by a dollar sign. No prefixing character signifies a decimal number.

4) The operator may set selected bits in a parameter word by preceding the bit numbers by a B, using commas as number separators:

/B, 15, 11, 7, 3 CR would result in the parameter being changed to 9001/8888.

5) Pressing MANUAL INTERRUPT will result in calling for an immediate monitor parameter stop.

5. Error Messages

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
ID	STJP	SSEE	RTN	MTRERR	IORP	A4	Q4	A5	Q5

Definitions:

ID: SMM Identification Word
STJP: SMM Stop/Jump Parameter Word
SSEE: Test Section and Error Pointer
RTN: Return Address
MTRERR: Monitor Error Code

02 - I/O Response Error
03 - Status Error
04 - Interrupt Time Out Error
05 - Data Compare Error

IORP: Last I/O Operation Performed and the Associated Response

IO: 10-Write
20-Read
30-Function
40-Status

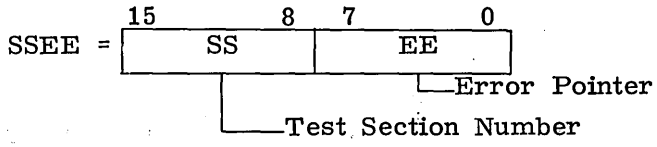
RP: 10-Reply
20-External Reject
30-Internal Reject

For monitor error code MTRERR=05, and text section error pointer SSEE=XX20, IORP=word count of data miscompare.

The information reported in A4, Q4, A5, and Q5 varies with the monitor error code, as defined below.

MTRERR:	A4	Q4	A5	Q5
02	Contents A Register	Contents Q Register	-	-
03	Contents A Register	Contents Q Register	Actual Status	Expected Status
04			Interrupt Line	Expired Time, ms
05	Input Data	Output Data	Input Channel Addr.	Output Channel Addr.

The SSEE parameter reports the specific location within the test the monitor error code has occurred. This parameter is defined as follows:



The test section numbers are defined as follows:

00 - Equipment Code Check
01 - Program Protect Check
02 - Module Addressing Check
03 - Unit Addressing Check
04 - Status/Reply - Function/Reject Check
05 - Data Line Check
06 - Interrupt/Flag Register Check
09 - Write Only
0A - Read Only
0B - Write/Read Closed Loop

The error pointers are defined as follows:

01 - Copying Status from the IOM
02 - Outputting A Function to the IOM
03 - Outputting Data to the IOM
04 - Inputting Data from the IOM
05 - Processing a Write Interrupt
06 - Processing a Read Interrupt
F0 - Operator Error - Sync I/O Defined, But No Time Period Defined
F1 - Section 6, No Interrupt Line Defined
10 - Section 6, Interrupt Time Out Error
11 - Section 6, Status Error Prior to Receiving an Interrupt
12 - Section 6, Status Error After Receiving an Interrupt
13 - Section 6, Status Time Out Error After Receiving an Interrupt
20 - Section 11, Data Compare Error

II. DESCRIPTION

A. SECTION 0: EQUIPMENT CODE CHECK

The purpose of Section 0 is to allow checking of the equipment number decoding within the IOM mother unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

1.	Section 0	A00	Stop 3
2.	Address Increment	A15	Stop 3

The section will begin executing repetitive I/O to equipment number 0.

The section will remain looping on one address indefinitely without operator intervention. Test point 23 or used position 2 is the end result of the select logic and should be a 7 kHz pulse train if the hardware equipment code is jumped to match the address output by the test.

After all pertinent observations have been made, the operator must set the SKIP switch to request a monitor stop to continue the test.

During the monitor stop, the operator is to change the IOM equipment select jumper in order to select the next equipment number from 0 to 1, 1 to 2, etc., if such a check is required.

After processing the monitor stop, the test will continue execution with the equipment number incremented by 1, the I/O address incremented by $0080.

To increment each succeeding equipment number, the operator is to change the equipment jumper and call for a monitor stop. The section will be completed after processing the monitor stop following I/O address $0780.

B. SECTION 1: PROGRAM PROTECT CHECK

Section 1 executes repetitive reads from the IOM using the following address:

1. The equipment code defined in Q, Stop 2.
2. The module address defined in A, Stop 4.
3. Unit addresses of zero.

To execute this section, the operator must select or define the following:

1.	Equipment Code	Q Register	Stop 2
2.	Section 1	A01	Stop 3
3.	Address Increment	A15	Stop 3
4.	Module Address	A Register	Stop 4

All pertinent errors are reported by this test section.

Messages will be presented to the operator, if a TTY is present in the system, on how to set and clear the console PROTECT switch, and when to protect and unprotect the IOM. The section will increment through all four protect conditions in the following order:

1. Unprotected core executing I/O to an unprotected IOM.
2. Protected core executing I/O to an unprotected IOM.
3. Protected core executing I/O to a protected IOM.
4. Unprotected core executing I/O to a protected IOM.

The section will proceed to the next protect condition 10 seconds after each monitor stop. The operator is expected to set the console switches and/or change the IOM protect jumpers during the monitor stop or during the 10 second delay. Possible monitor protect violations may occur if this is not observed.

The section will exit after processing the monitor stop following the fourth protect condition.

C. SECTION 2: MODULE SELECT CHECK

The purpose of Section 2 is to allow checking of the module select decoding of the IOM mother unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the module select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

1.	Equipment Code	Q Register	Stop 2
2.	Section 2	A02	Stop 3
3.	Address Increment	A15	Stop 3
4.	Starting Module Address	A Register	Stop 4
5.	Ending Module Address	Q Register	Stop 4

The section will begin executing repetitive I/O to the starting address defined in Stops 2 and 4. The section will remain looping on one address indefinitely without operator intervention.

The following test points on card 2 will become logical 0 (during the read cycle) only for the respective address listed.

Address	Card 2 Test Point
$0600	12
$0610	13
$0620	14
$0630	15
$0640	16
$0650	17
$0660	18
$0670	19

Test point 29 on card 5 (master) will go to a logical 1 when a read cycle is performed on address $0600. Test point 29 on card 5 (slave) will go to a logical 1 when a read cycle is performed on address $0610, and so on for all slave units configured within the system.

The operator must set the SKIP switch to request a monitor stop to continue the test.

During the monitor stop, the operator is to change the slave select jumper so to select the next slave unit. After processing the monitor stop, the test will continue execution, now with the module address incremented by 1 - the I/O address incremented by $0010.

To increment each succeeding module address, the operator is to change the slave select jumper and call for a monitor stop. The section will be conpleted after processing the monitor stop following the testing of the ending module address.

D. SECTION 3: UNIT SELECT CHECK

The purpose of Section 3 is to allow checking of the unit select decoding within an IOM mother or slave unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the unit select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

1.	Equipment Code	Q Register	Stop 2
2.	Section 3	A03	Stop 3
3.	Address Increment	A15	Stop 3
4.	Starting Unit Address	A Register	Stop 4
5.	Ending Unit Address	Q Register	Stop 4

The section will begin executing repetitive I/O to the starting address defined in Stops 2 and 4. The section will loop on one address indefinitely without operator intervention.

The following test points on card 5 (master) will become logical 0 (during the read cycle) only for the respective address listed.

Address	Card 5 Test Point
$0600	1
$0601	2
$0602	3
$0603	4
$0604	5
$0605	6
$0606	7
$0607	8
$0608	9
$0609	10
$060A	11
$060B	12
$060C	13

Address	Card 5 Test Point
$060D	14
$060E	15
$060F	16

After all observations have been made, the operator must set the SKIP switch to request a monitor stop to continue the test. After processing the monitor stop, the test will continue execution, now with the unit and I/O addresses incremented by 1. The section will be completed after processing the monitor stop following the testing of the ending unit address.

After observing any suspect logic, the operator must set the SKIP switch to request a monitor stop to continue the test.

After processing each monitor stop, the I/O addresses will be incremented by $0010 and status inputs will again be executed, this time from the next module present. After processing the monitor stop following testing of the ending module address, the section will reset the addresses to the starting module address and begin executing repetitive function outputs.

To verify proper reject logic operation the operator should do the following:

1. Place an extender board in card position 8 (master). Connect a jumper between extender board pin A13 and test point 18 on card 5 (master).
2. The test will perform Write operations to the starting address. Verify 425 nanosecond ±10 percent time delay between test point 20 (negative trigger) on card 2 and test point 18 on card 5 (master). Verify delay of 640 nanoseconds ±10 percent between test point 20 (positive trigger) on card 5 (master) and test point 28 on card 4 (master). External rejects will occur. The test will report any replies or internal rejects as errors.

After observing any suspect logic, the operator must set the SKIP switch to request a monitor stop to continue the test.

After processing each monitor stop, the I/O addresses will be incremented by $0010 and function outputs will again be executed, this time to the next module present. The address incrementing will be as for the status input portion of this section. The section will exit after processing the monitor stop following testing of the ending module address.

E. SECTION 4: STATUS REPLY/FUNCTION REJECT

The purpose of Section 4 is to allow checking of the status and function responses of IOM module control cards. The section will expect replies from the flag/status logic during status inputs and external rejects during function outputs.

To execute this section, the operator must define or select the following entry parameters:

1.	Equipment Code	Q Register	Stop 2
2.	Section 4	A04	Stop 3
3.	Address Increment	A15	Stop 3
4.	Starting Module Address	A Register	Stop 4
5.	Ending Module Address	Q Register	Stop 4

The section will begin executing repetitive status inputs from the starting address defined in Stops 2 and 4. The section will loop on the starting address, doing status inputs, until operator intervention.

To verify proper reply logic operation, the operator should do the following:

Verify 425 nanosecond ±10 percent time delay between test point 21 (negative trigger) on card 2 and test point 1 on card 5 (master). Verify delay of 640 nanoseconds ±10 percent between test point 19 (positive trigger) on card 5 (master) and test point 27 on card 4 (master). The test will report any rejects as an error.

F. SECTION 5: DATA LINE OUTPUT CHECK

Section 5 executes repetitive outputs to the IOM using the following address:

1. The equipment code defined in Q, Stop 2.
2. The module and unit addresses between the limits defined by the starting and ending addresses in Stop 4.

This section will expect internal rejects when executing the data outputs.

To execute this section, the operator must define or select the following:

1.	Equipment Code	Q Register	Stop 2
2.	Section 5	A05	Stop 3
3.	Address Increment	A15	Stop 3
4.	Starting Unit Address	A Register	Stop 4
5.	Ending Unit Address	Q Register	Stop 4
6.	First Data Pattern	A Register	Stop 6
7.	Second Data Pattern	Q Register	Stop 6

Both data patterns of Stop 6 will be output to each of the addresses within the limits specified in Stop 4. The two data patterns will alternate, a new pattern output each time a monitor stop is processed. Every second monitor stop, after both patterns have been output to a channel, the I/O address will increment by $0001. The section will exit after processing the monitor stop following the outputting of both data patterns to the ending I/O address.

G. SECTION 6: INTERRUPT FLAG STATUS CHECK

The purpose of Section 6 is to check all 8 interrupt lines of an IOM module and all 16 flag status bits. This section will report all appropriate errors during the interrupt processing and status checking.

To execute this section, the operator must define or select the following entry parameters:

1.	Equipment Code	Q Register	Stop 2
2.	Section 6	A06	Stop 3
3.	Manual Sync	A13	Stop 3
4.	Input Interrupt Line*	Q Register	Stop 7
5.	Interrupt Wait Time	A or Q Register	Stop 8

This test section is to be executed with manually producing interrupts and manually moving the interrupt cable from connector to connector on the IOM module. To allow enough time to accomplish this and to prevent diagnostic time out errors, the interrupt wait time should be set to a large number in the A register, Stop 8, representing a large time in milliseconds. An A register parameter of $4000 milliseconds will allow 16.3 seconds for an interrupt to be generated.

To begin Section 6 execution, the interrupt cable must be connected to the IOM interrupt line 1 connector. With the test running, the operator is to ground test point 1 of the flag/status card to produce a status of $0001 and an interrupt on IOM line 1. The diagnostic will have been checking the flag status to verify that no status bits are set prior to receiving the interrupt. When the ground is made, an interrupt will be generated and sent to the mainframe, and the flag/status will be set to $0001. The diagnostic will verify the receipt of the interrupt and the proper status, and then ring the teletype bell to verify this to the operator.

After the bell, the operator is to advance the interrupt cable to the next IOM connector (1 to 2, 2 to 3, etc.) then ground the next test point in sequence (1 to 2, 2 to 3, etc.).

* Defined at the mainframe, not the IOM.

After grounding test points 1 through 8 to check interrupts 1 through 8 and flag/status bits 0 through 7, the operator need only ground the remaining test points 9 through 16 without moving the interrupt cable. Only the flag/status bits are checked. Again the TTY bell will signal to the operator receipt of the proper flag/status bit.

The section will be completed after processing the eight interrupts associated with flag/status bits 0 through 7 and receiving flag/status bits 8 through 15.

H. SECTION 9: WRITE ONLY

The purpose of Section 9 is to execute repetitive writes to the unit addresses defined, in asynchronous or synchronous mode, with or without interrupts, as defined by the operator parameters. This is an open ended test, no data checking is attempted.

To execute this section, the operator must select or define the following:

1.	Equipment Code	Q Register	Stop 2
2.	Section 9	A09	Stop 3
3.	Data Patterns	Q Register	Stop 3
4.	Starting Unit Address	A Register	Stop 4
5.	Ending Unit Address	Q Register	Stop 4
6.	First Data Word	A Register	Stop 6
7.	Alternate Data Word	Q Register	Stop 6

If the section is to run synchronous, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Sync Wait Time	A or Q Register	Stop 8

If the section is to run synchronous with interrupts, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Write Interrupt Line	A Register	Stop 7
3.	Interrupt Wait Time	A or Q Register	Stop 8

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred.

When operating in manual sync mode, the operator must short card pin A29 (request) to card test point 22 (reply). The Reply signal is used as a pulse to trigger the sync circuits. If request is grounded, or remains connected to test point 22 for any length of time, the test will apparently execute two passes per sync. In reality the Request signal is not being removed fast enough by the operator and one pass is completed on setting the Request signal, and one pass is completed on clearing the Request signal.

I. SECTION 10: READ ONLY

The purpose of Section 10 is to execute repetitive reads to the unit addresses defined, in asynchronous or synchronous mode, with or without interrupts, as defined by the operator parameters. This is an open ended test, no data checking is attempted.

To execute this section, the operator must select or define the following:

1.	Section 9	A09	Stop 3
2.	Data Patterns	Q Register	Stop 3
3.	Starting Unit Address	A Register	Stop 4
4.	Ending Unit Address	Q Register	Stop 4
5.	Starting Unit Address	A Register	Stop 5
6.	Equipment Code	Q Register	Stop 5

If the section is to run synchronous, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Sync Wait Time	A or Q Register	Stop 8

If the section is to run synchronous with interrupts, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Write Interrupt Line	A Register	Stop 7
3.	Interrupt Wait Time	A or Q Register	Stop 8

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred.

This section calculates the number of channels of digital input for testing by comparing the starting and ending addresses of Stop 4. Actual transfers begin with the read starting unit address as defined in the A register of Stop 5.

When operating in manual sync mode, the operator must short card pin B28 (request) to card test point 20 (reply). The Reply signal is used as a pulse to trigger the sync circuits. If request is grounded, or remains connected to test point 20 for any length of time, the test will apparently execute two passes per sync. In reality the Request signal is not being removed fast enough by the operator and one pass is completed on setting the Request signal, and one pass is completed on clearing the Request signal.

J. SECTION 11: WRITE-READ CLOSED LOOP

The purpose of Section 11 is to output data through the digital output unit, input this data through the digital input unit, and check the validity of the input against the original output data.

To execute this section, the operator must select or define the following:

1.	Equipment Code-Writes	Q Register	Stop 2
2.	Section 11	A09	Stop 3
3.	Data Patterns	Q Register	Stop 3
4.	Starting Write Unit Address	A Register	Stop 4
5.	Ending Write Unit Address	Q Register	Stop 4
6.	Starting Read Unit Address	A Register	Stop 5
7.	Equipment Code - Reads	Q Register	Stop 5
8.	First Data Word	A Register	Stop 6
9.	Alternate Data Word	Q Register	Stop 6

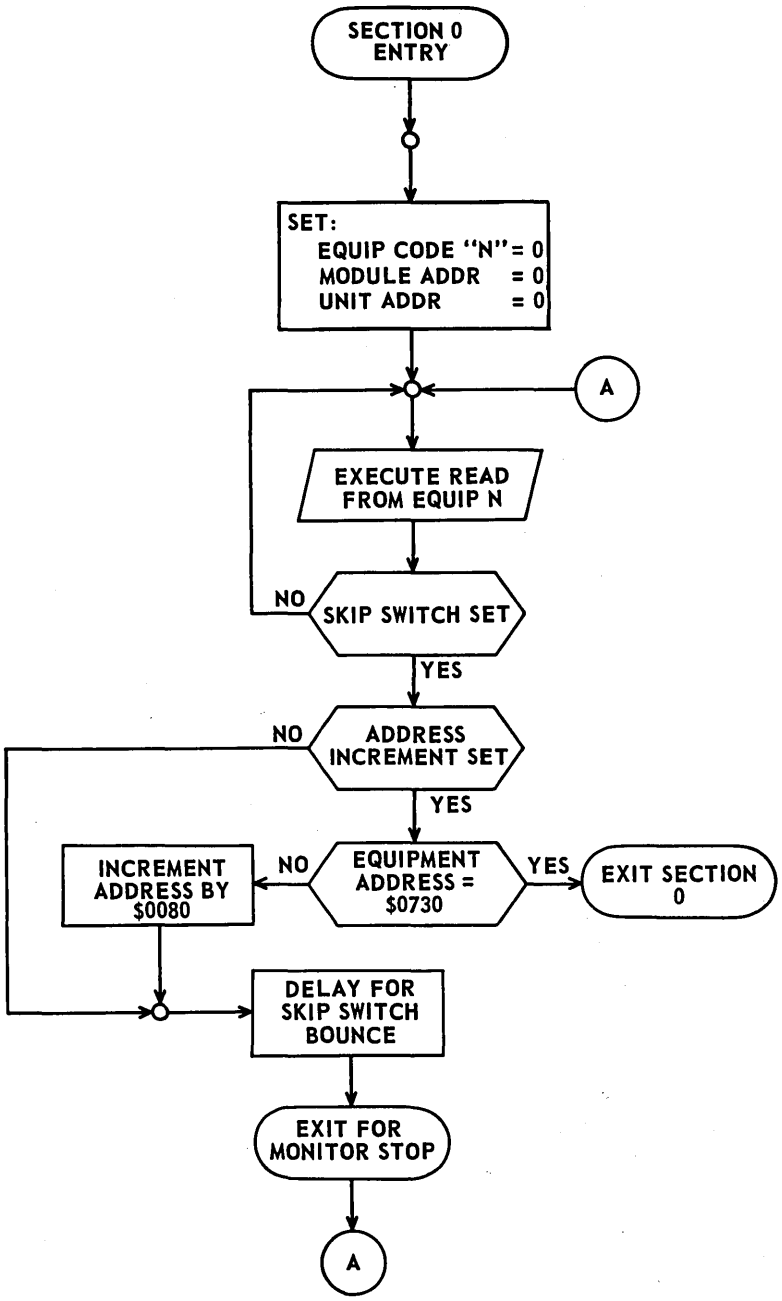
If the section is to run synchronous, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Sync Wait Time	A or Q Register	Stop 8

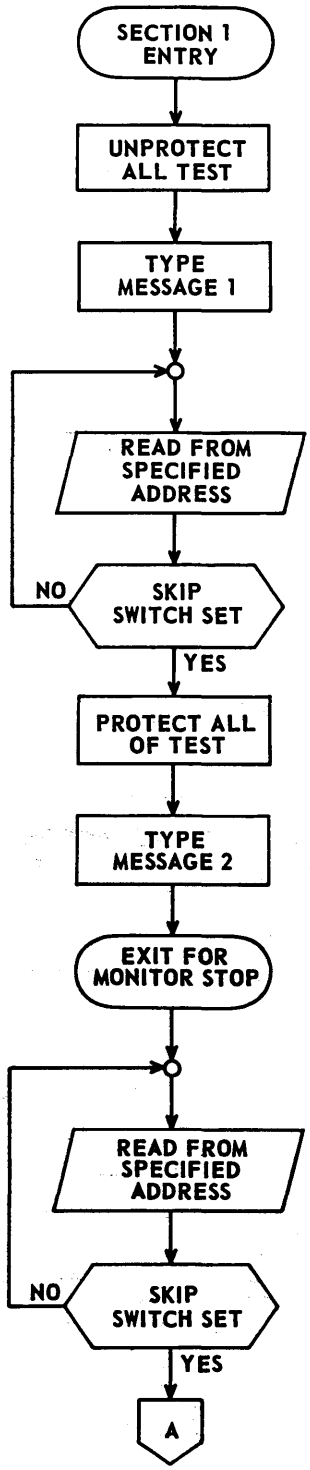
If the section is to run synchronous with interrupts, the operator must define the following:

1.	Manual Sync or	A13	Stop 3
	Repetitive Sync	A12	Stop 3
2.	Write Interrupt Line	A Register	Stop 7
3.	Interrupt Wait Time	A or Q Register	Stop 8

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred. If this section is to run synchronously, the write channels must be enabled prior to the execution of the I/O. A good time to do this is during the parameter entry sequence. Here the mainframe will wait indefinitely while the hardware is readied. If the I/O is begun to an un-abled synchronous write channel, the hardware can never be made ready, and thus the write I/O will always be rejected.



SECTION ZERO – EQUIPMENT CODE CHECK



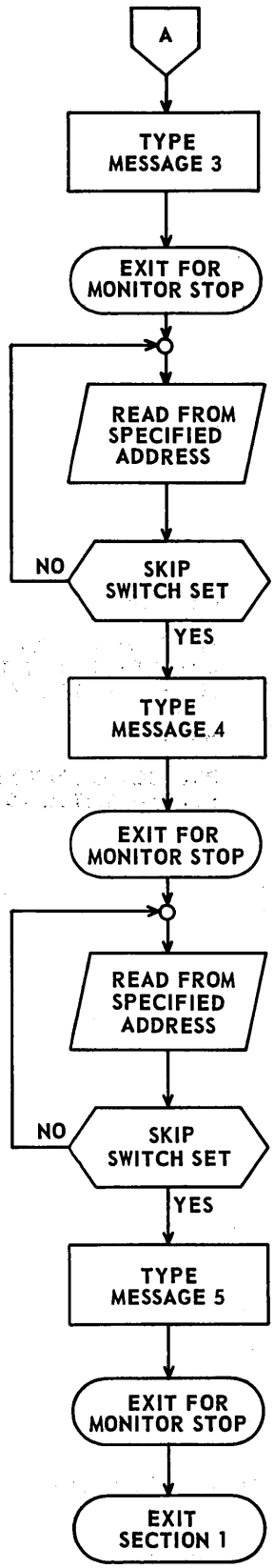
MESSAGE 1:

**SET PROTECT SWITCH. CLEAR STOP SWITCH.
UNPROTECTED I/O TO UNPROTECTED IOM.
SET SKIP SWITCH TO ADVANCE TEST**

MESSAGE 2:

**PROTECTED I/O TO UNPROTECTED IOM.
SET SKIP SWITCH TO ADVANCE TEST.**

SECTION ONE – PROTECTED I/O CHECK



MESSAGES

MESSAGE 3:

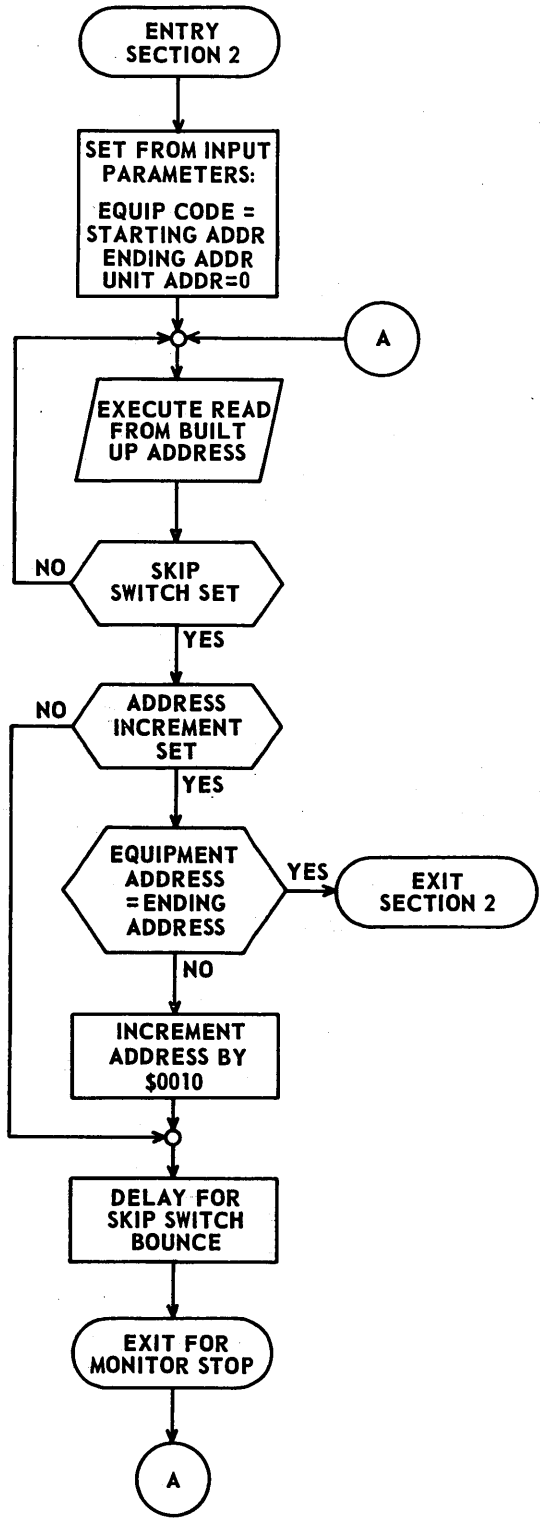
PROTECT IOM.
PROTECTED I/O TO PROTECTED IOM.
SET SKIP SWITCH TO ADVANCE TEST

MESSAGE 4:

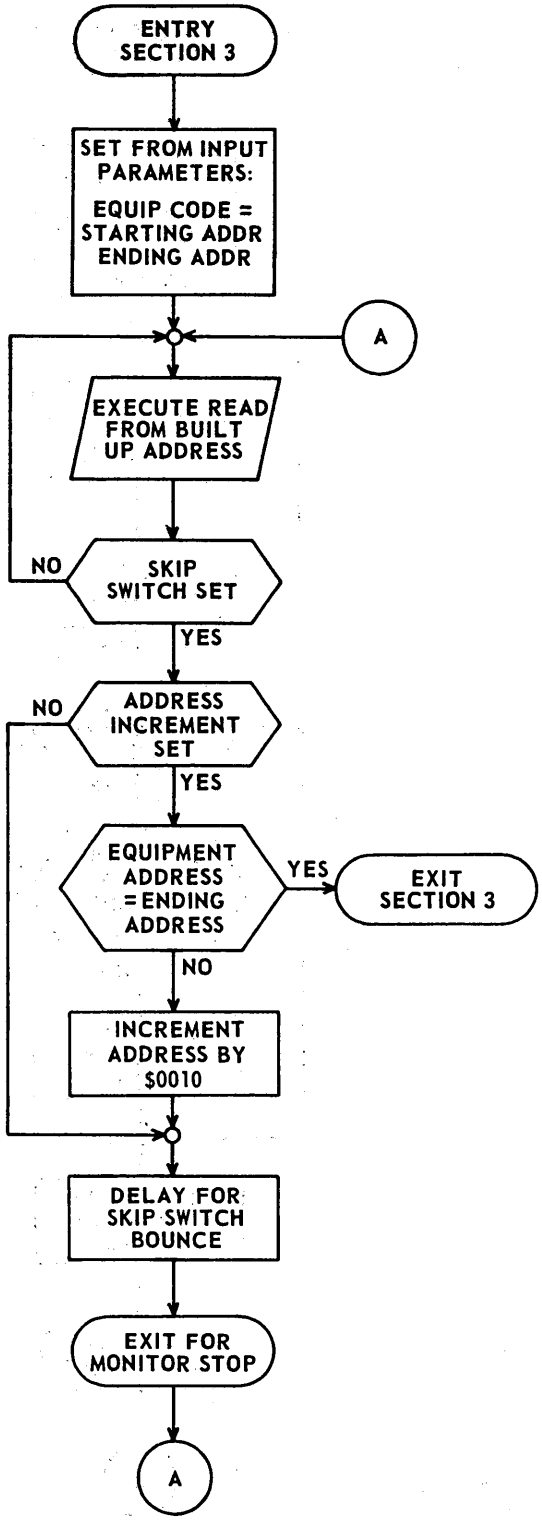
UNPROTECTED I/O TO PROTECTED IOM.
SET SKIP SWITCH TO ADVANCE TEST.

MESSAGE 5:

CLEAR PROTECT SWITCH.
SET STOP SWITCH.
SET SKIP SWITCH TO ADVANCE TEST.

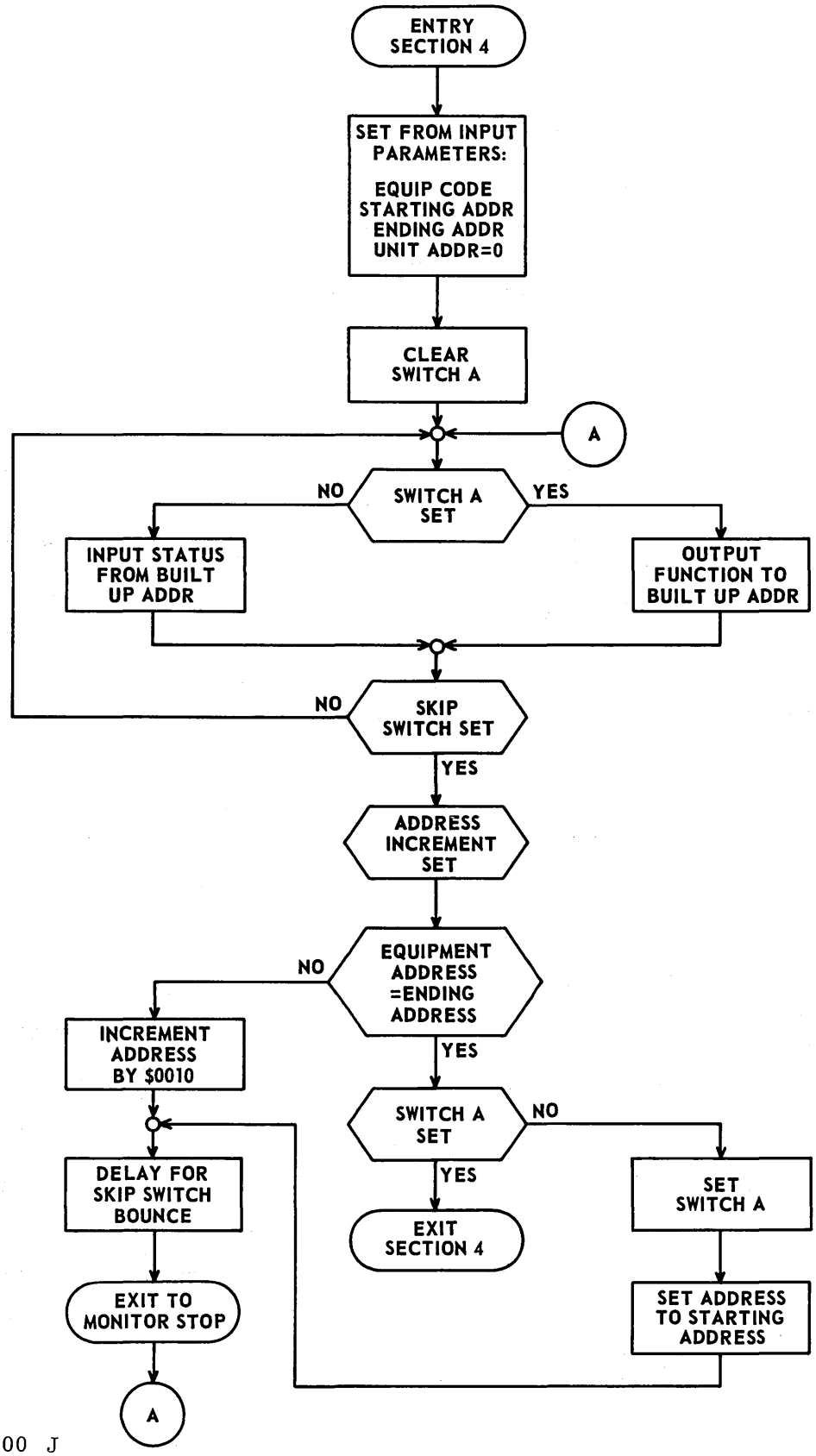


SECTION TWO – MODULE SELECT CHECK

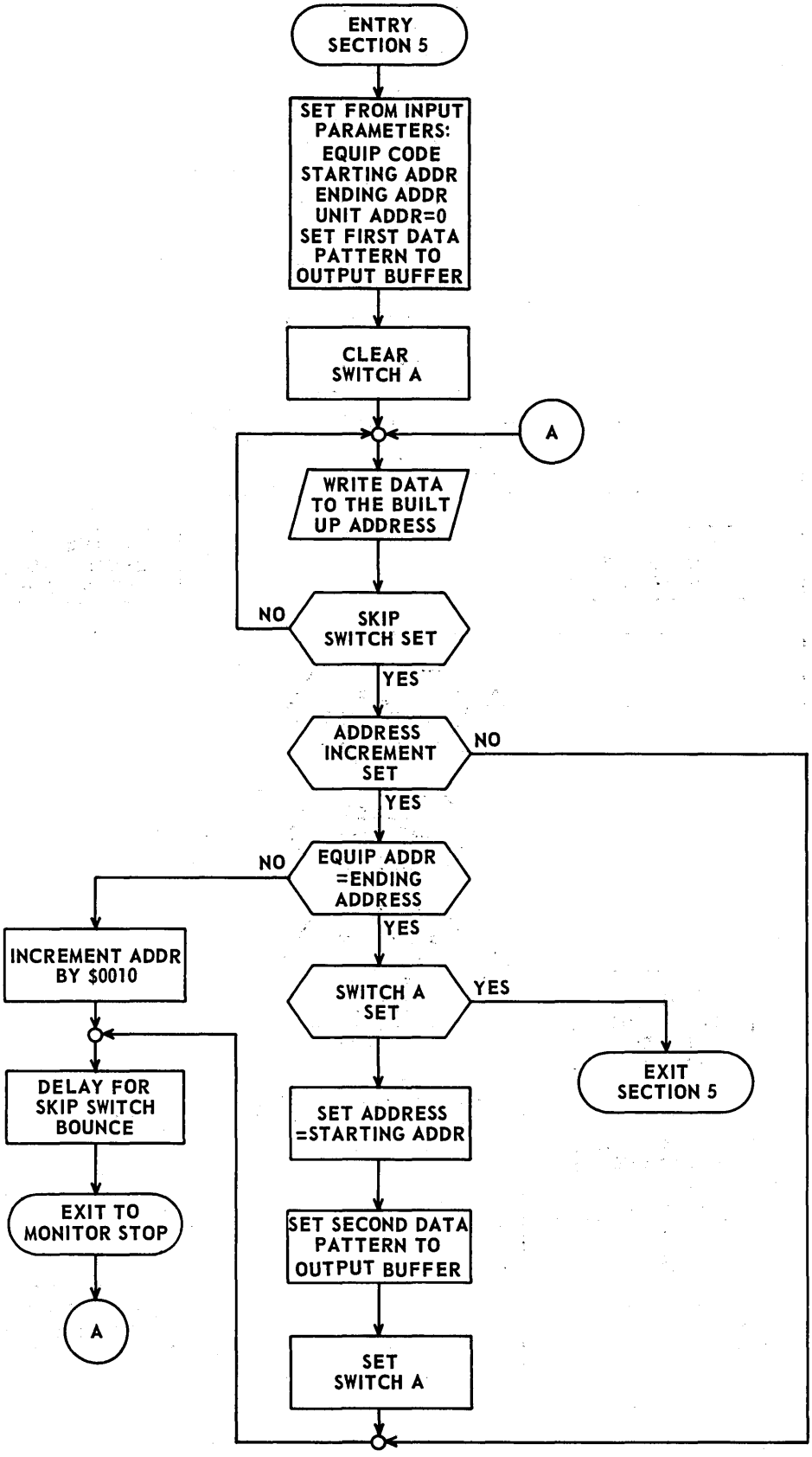


SECTION THREE – UNIT SELECT CHECK

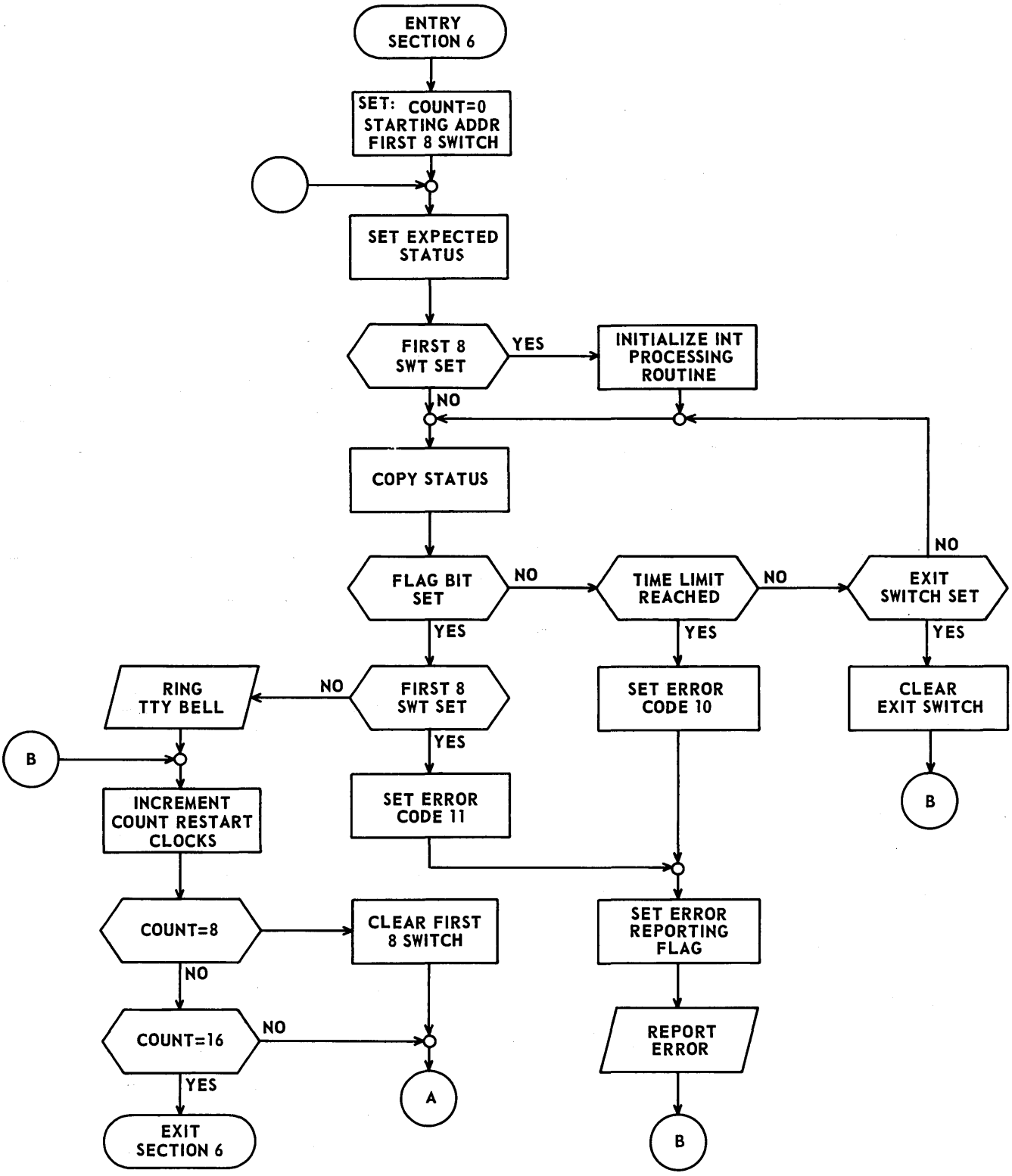
SECTION FOUR – STATUS REPLY – FUNCTION REJECT

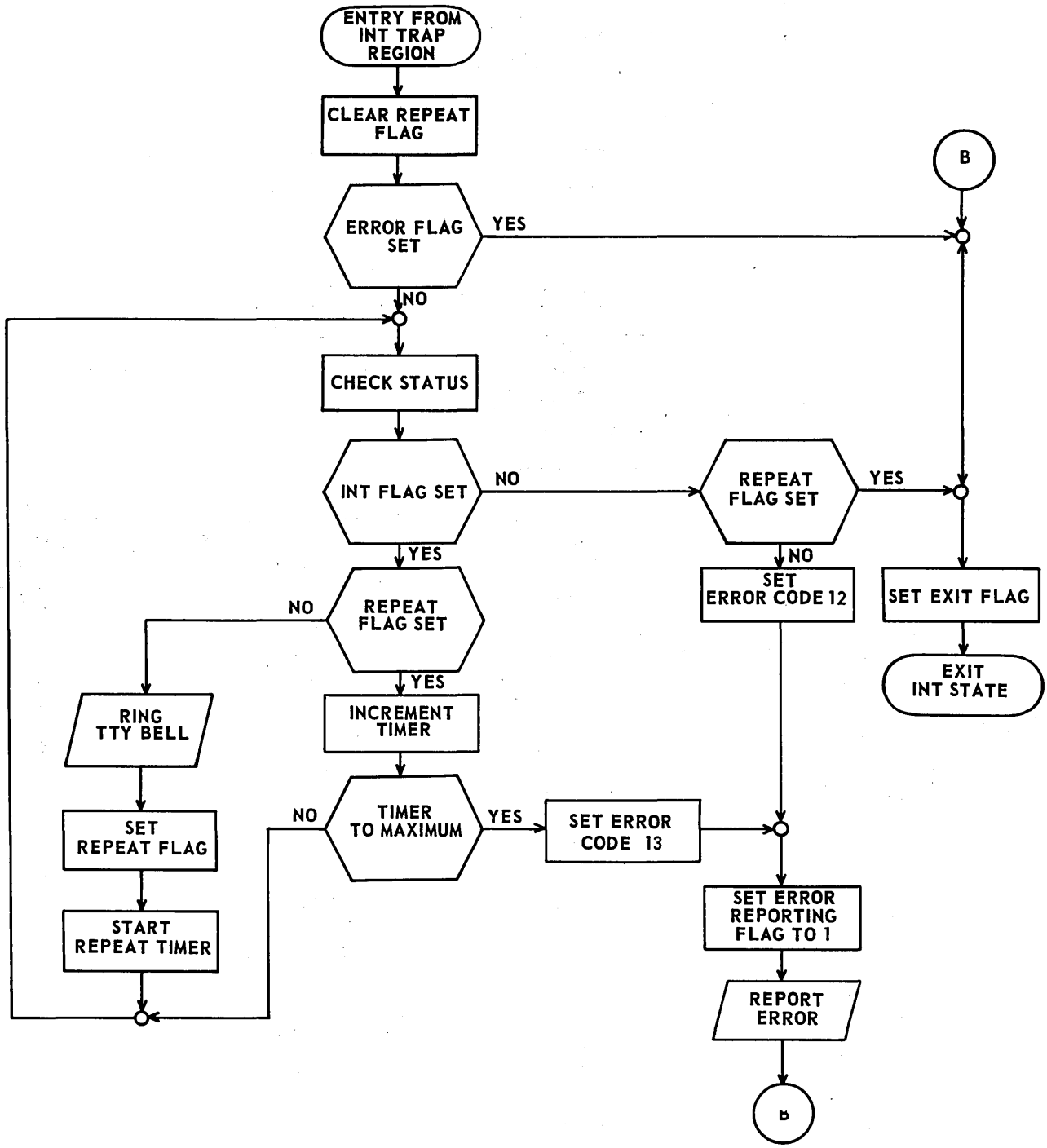


SECTION FIVE – DATA OUTPUT CHECK

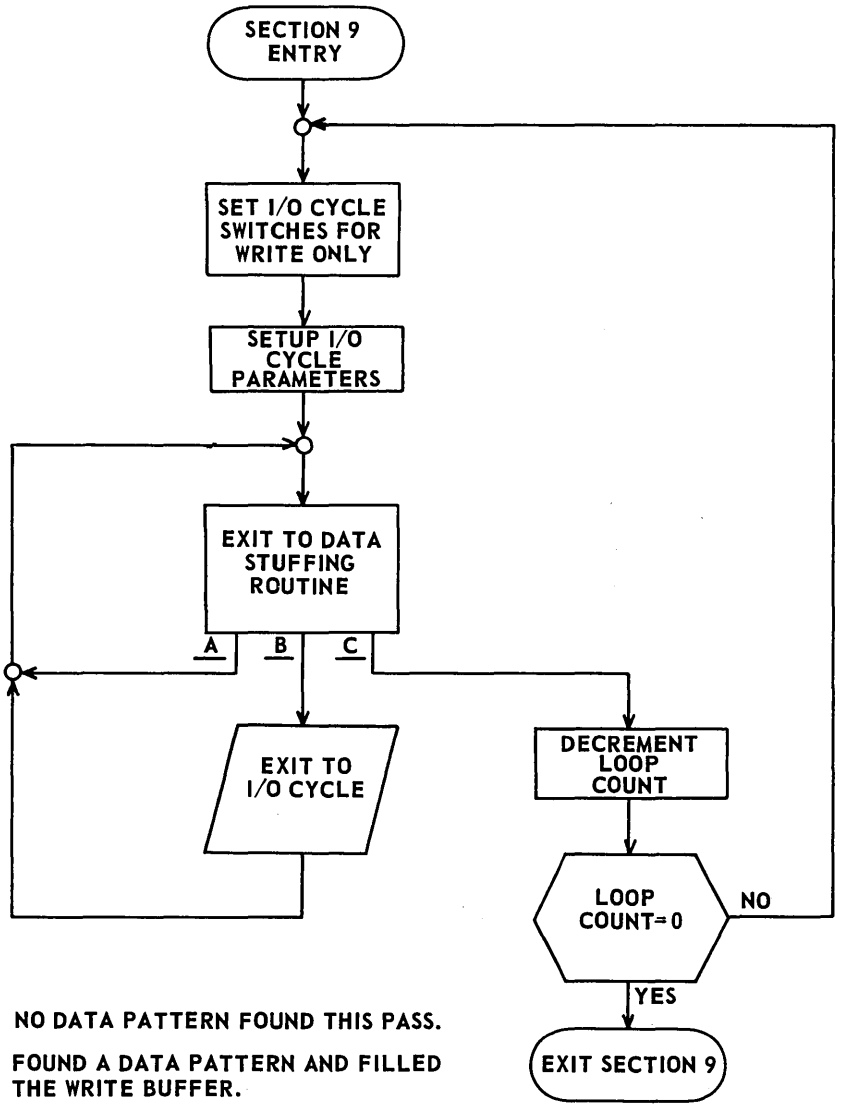


SECTION SIX – INTERRUPT/FLAG STATUS CHECK




ENTRY FROM INT TRAP REGION
CLEAR REPEAT FLAG
ERROR FLAG SET
YES
NO
B
CHECK STATUS
INT FLAG SET
NO
REPEAT FLAG SET
YES
YES
NO
SET ERROR CODE 12
SET EXIT FLAG
EXIT INT STATE
NO
REPEAT FLAG SET
YES
RING TTY BELL
INCREMENT TIMER
SET REPEAT FLAG
NO
TIMER TO MAXIMUM
YES
SET ERROR CODE 13
START REPEAT TIMER
SET ERROR REPORTING FLAG TO 1
REPORT ERROR
B

SECTION 9 – WRITE ONLY CHECK

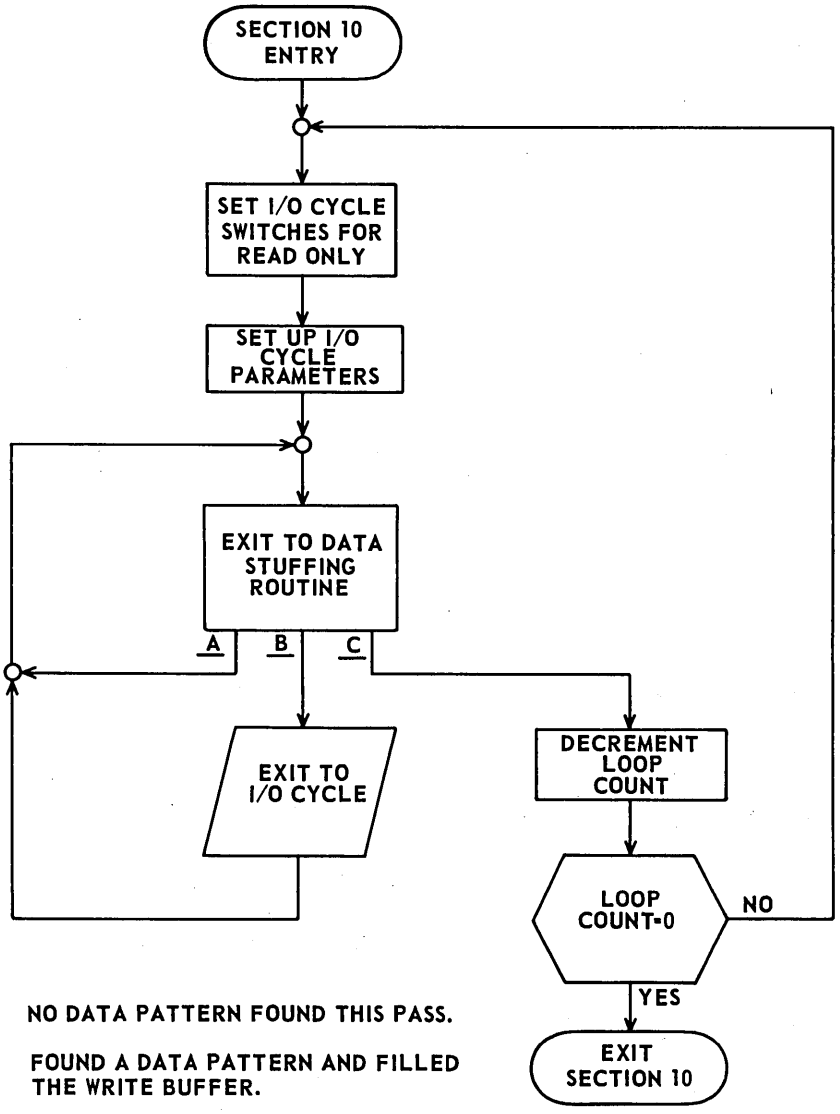


A NO DATA PATTERN FOUND THIS PASS.

B FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER.

C NO ADDITIONAL DATA PATTERNS.

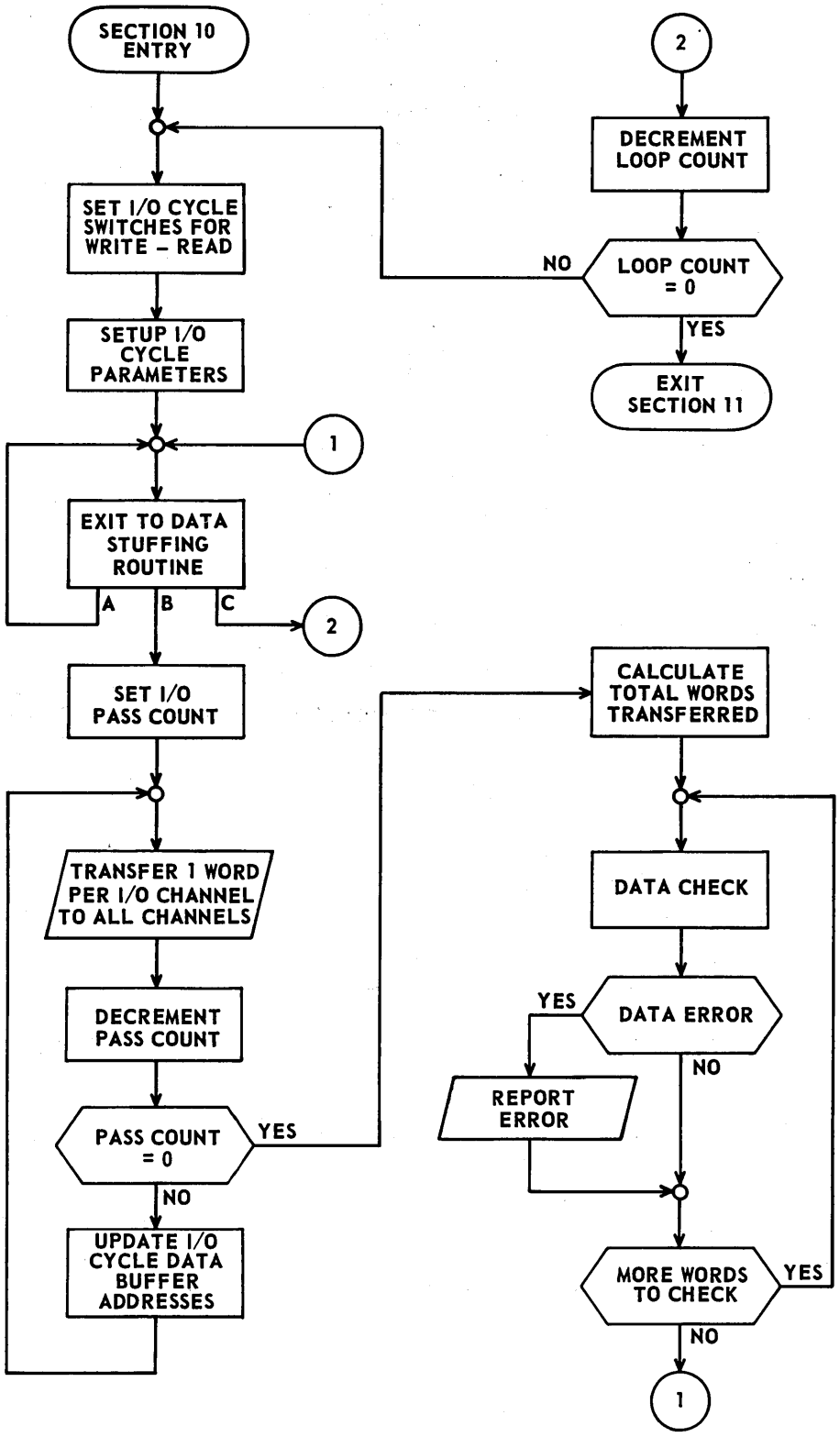
SECTION TEN – READS ONLY



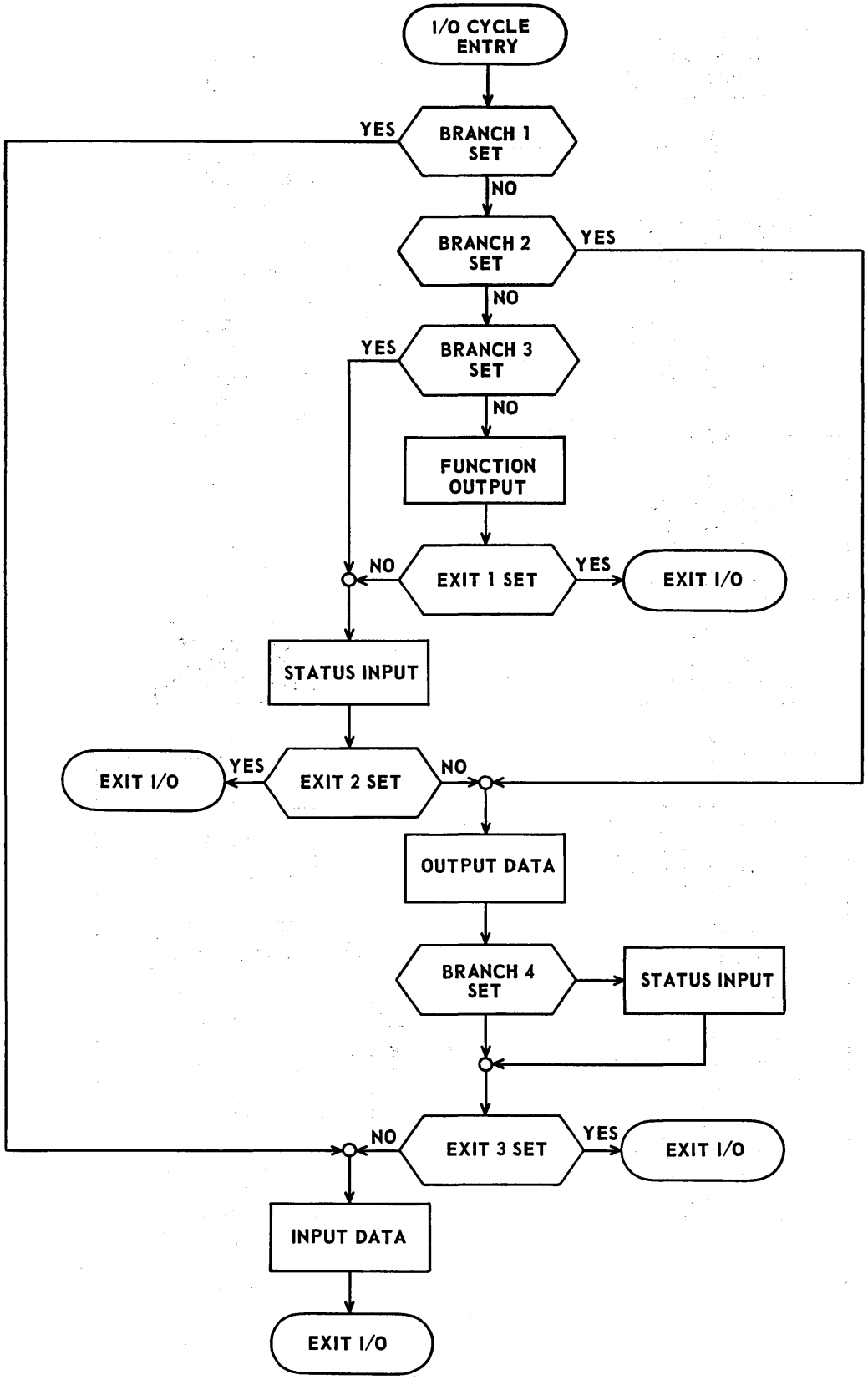
A NO DATA PATTERN FOUND THIS PASS.

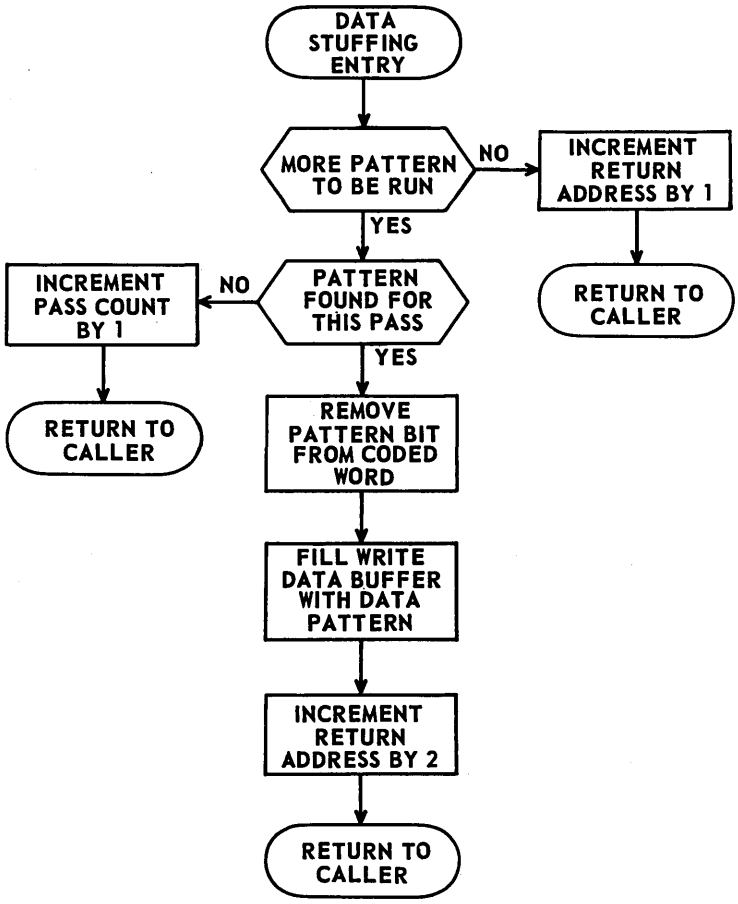
B FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER.

C NO FURTHER DATA PATTERNS.



SECTION ELEVEN – WRITE READ CLOSED LOOP


I/O CYCLE ENTRY
BRANCH 1 SET
YES
NO
BRANCH 2 SET
YES
NO
BRANCH 3 SET
YES
NO
FUNCTION OUTPUT
EXIT 1 SET
NO
YES
EXIT I/O
STATUS INPUT
EXIT 2 SET
YES
NO
EXIT I/O
OUTPUT DATA
BRANCH 4 SET
STATUS INPUT
EXIT 3 SET
NO
YES
EXIT I/O
INPUT DATA
EXIT I/O



DATA STUFFING ROUTINE

1500 SERIES REMOTE PERIPHERAL CONTROLLER DIAGNOSTIC
(HORA4C Test No. 4C)

I INTRODUCTION

HORA4C is a stand alone diagnostic which detects 95 percent of the single hardware detectable errors. The method used is constant status prediction and checking. Each hardware module is tested as much as possible before attempting operations upon the next level of hardware.

II REQUIREMENTS

A. HARDWARE REQUIREMENTS

1704 Processor	(32K Mode)
Section 1	1590-2 Remote I/O Adapter
Section 2	1591-2 Remote I/O Station
Section 3	Same as Section 2
Section 4	Same as Section 3
Section 5	1558 Latch Relay Control
Section A	Same as Section 5
Section F	1559D and/or 1559H Latch Relays

B. SOFTWARE REQUIREMENTS

This diagnostic runs under the control of SMM17 Version 3.0. It is a stand alone diagnostic and follows all appropriate SMM rules.

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

HORA4C is loaded using standard SMM17 means. There are no overlays, and MBS subroutines are not used.

Entry Points

INITAL	Runs initialization at load time. INITAL is not overwritten.
SSR	Section selection routine entry point from SMM after initialization.
SSRR	Run next section entry.

B. PARAMETER ENTRY

In all SMM17 calls, error or parameter:

A1 = XXYZ, Where XX = Test ID (HORA4C=4C)
Y = Number of stops
Z = Type of call (1=parameter)
(8=error), etc.

Q1 = The SMM17 Stop/Jump parameter word (SJ)

1. Stop Series 1 Parameters

A1	Q1	A2	Q2	A3	Q3
4C31	SJ	PRTEQ	PINT	PRC	PSUB1

PRTEQ = Address of printer where bits 7-10 are equipment number, bit 12 is buffered channel flag.

PINT = Interrupt line from the local coupler.

PRC = Remote couplers. Where Bit 0 = RC0
1 = RC1

No other bits are legal.

PSUB1 = Sections to run. Where Bit 1 = Section 1
2 = Section 2
---
15 = Section F

Section 0 does not exit, and bit is ignored if set.

NOTE

Stop series 1 defines all parameters needed to test LC and RC in Sections 1, 2, 3, and 4.

2. Stop Series 2-N Remote I/O Parameters

This stop series is repeated until all entries are zero. This flags completion of entries and allows the test to continue. The entries per stop are:

A1	Q1	A2	Q2	A3	Q3	A4	Q4
4C41	SJ	RC ADDR	STATION ADDR	FCA	LCA	STATION INTERRUPT LINE	----

RC ADDR — The RC address is a right-justified 3-bit number which must have the corresponding bit set in the stop series 1 parameter word (PRC).

STATION ADDRESS — The station address is a right-justified 7-bit number.

FCA — The first channel address (FCA) is a 12-bit right-justified number, the upper two bits declaring mode (digital, etc.). FCA must be less than or equal to the last channel address (LCA).

LCA — The last channel address (LCA) is a 12-bit right-justified number, the upper two bits declaring mode (digital, etc.). LCA must be greater than or equal to the first channel address (FCA).

The upper two bits (bits 10 and 11) of FCA and LCA must agree as they define the mode of operation of the end device.

For FCA and LCA, bit 15 states whether it is an input or output device. 8XXX is an input and 0XXX is an output. FCA and LCA must have these bits matching.

STATION INTERRUPT LINE — The station interrupt line is a 1 bit entry stating which bit in RCI will come up at station interrupt time. This parameter cannot be zero unless all entries are zero to terminate parameter entry.

All errors in parameter entry will be reported as 0X errors, and that parameter stop will be requested again.

Only one station address zero entry is allowed per RC. This station address must contain all CAs to test which have no associated station.

To clear an entry, set RC, FCA, LCA, and leave the station interrupt line zero. This will give you an error, clearing the legal address bit in the parameter list and clearing the entry.

C. SECTION DESCRIPTION INDEX

Section 1	LC Testing
Section 2	RC Status Checks
Section 3	Echo Check
Section 4	NA, EOS Test
Section 5	FA, PA, LA Test
Section A	1558 Status Response Test
Section F	House of Representatives Light Test

IV OPERATOR COMMUNICATION

A. MESSAGE FORMATS

The first two stops are common to all error message types.

A1	Q1	A2	Q2
4CX8	SJ	XXEC	CADD

EC = Error Code

CADD = Call Address (address call originated from)

B. MESSAGE DICTIONARY

01	No subtest selected	Re-enter	
02	No remote equipments selected	Re-enter	
03	No interrupt line selected	Re-enter	
04	Extra bits in equipment parameter	Re-enter	
05	Extra bits in RC parameter	Re-enter	
06	Station address out of range	Re-enter	
07	First CA address out of range	Re-enter	
08	Last CA address out of range	Re-enter	
09	LCA and FCA out of order	Re-enter	
0A	Entered RC not legal	Re-enter	
0B	Remote coupler out of range	Re-enter	
0C	Mode bits in LCA, FCA conflict	Re-enter	
0D	Legal CA rejected functions		
0E	Illegal CA accepted function(s)		
		A3	Q3
11	Timeout waiting for data ready status	$\overline{\text{LCS}}$	$\overline{\text{LCI}}$
12	Timeout waiting for LC not busy	LCS	LCI
14	Timeout waiting for EOS interrupt	LCS	LCI
15	Interrupt when not enabled	LCS	LCI
16	No end of operation interrupt	LCS	LCI
17	Timeout station busy	LCS	LCI
18	External reject on station address	LCS	LCI
19	Internal reject on station address	LCS	LCI
20	External reject on LC status	OPA	OPQ
21	Internal reject on LC status	OPA	OPQ
22	External reject on interrupt status	OPA	OPQ
23	Internal reject on interrupt status	OPA	OPQ
24	External reject on write	OPA	OPQ
25	Internal reject on write	OPA	OPQ
26	External reject on function	OPA	OPQ
27	Internal reject on function	OPA	OPQ
28	RC rejected function	OPA	OPQ
29	No station interrupt occurred in 10 milliseconds	OPA	OPQ
2A	External reject on read	OPA	OPQ
2B	Internal reject on read	OPA	OPQ
2C	External reject on no-operation	OPA	OPQ
2D	Internal reject on no-operation	OPA	OPQ

		A3	Q3
30	Local coupler status compare error	ACT	EXP
31	Echo data compare error	ACT	EXP
32	RC status compare error	ACT	EXP
33	NA register compare error	ACT	EXP
34	No EOS status when NA = LA	ACT	EXP
35	Remote equipment stayed busy too long	ACT	EXP
36	LC interrupt status compare error	ACT	EXP
37	RC interrupt status compare error	ACT	EXP
38	NA not incremented by 1	ACT	EXP
39	EOP interrupt status not sent	ACT	EXP
3A	Station status compare error	ACT	EXP
3B	FC address compare error	ACT	EXP
40	No reject when U=F=NON-ZERO		
41	Reject after INT=LCS		
42	Reject after INT = LCI		
43	Reject after INT = LCS, LCI		
44	Reject after INT = RCS		
45	Reject after INT = RCS, LCS		
46	Reject after INT = RCS, LCI		
47	Reject after INT = RCS, LCS, LCI		
48	Reject after INT = RCI		
49	Reject after INT = RCI, LCS		
4A	Reject after INT = RCI, LCI		
4B	Reject after INT = RCI, LCS, LCI		
4C	Reject after INT = RCI, RCS		
4D	Reject after INT = RCI, RCS, LCS		
4E	Reject after INT= RCI, RCS, LCI		
4F	Reject after INT = RCI, RCS, LCS, LCI		
54	External reject on RC status	LCS	LCI
55	Internal reject on RC status	LCS	LCI
56	External reject on RC INT status	LCS	LCI
57	Internal reject on RC INT status	LCS	LCI
58	External reject on RC connect	LCS	LCI
59	Internal reject on RC connect	LCS	LCI
60	No reject reading with no data ready	OPA	OPQ
61	No reject on output when LC busy	OPA	OPQ
F0	Report normal system status		
F1	Report interrupt system status		
F2	Report configuration		

C. ADDITIONAL ERROR INFORMATION

F0, F1, and F2 are messages which the CE can produce by setting bits 12, 13, and 14 respectively in the SMM Stop/Jump parameter word.

The format for F0 and F1 are the same.

A3	Q3	A4	Q4	A5	Q5
LCS	LCI	RCS	RCI	NA	STATION STATUS

F0 is normal system status and F1 is the system status at interrupt time.

F2 is the system configuration where

A3	Q3	A4	Q4	A5	Q5
LC ADDR	RC ADDR	STATION ADDR	FCA	LCA	STATION INTERRUPT LINE

Setting these bits in the Stop/Jump word will cause these messages to be printed out after an error has been reported.

V DESCRIPTIONS

A. GENERAL

Q=0 means Q=0 + equipment address in bits 7-10. Rejects are errors unless otherwise specified. All items labeled with a number, i.e.: 1) XXXXXXXXXX
2) YYYYYYYYYY
. .....
N)ZZZZZZZZZZ
are repeatable with the repeat condition Stop/Jump bit.

B. SECTION DESCRIPTIONS

1. Local Coupler Function and Status Test

Tests the LC without regard to what is connected. It will fail, however, if power is not applied to, or if continual errors are transmitted from, the RC.

a. No-operation. A=Q=0, output; expect no reject.
b. Read LC status. Expect no reject.
c. Master clear and set full duplex. LCS = 405 ignoring repeat bit.
d. Set half duplex mode. LCS = 005.
e. Reject when: U = F = non-zero.
f. Reject on read with no data ready. A=0, Q = 0030.
g. Reject on output when LC busy.

2. Remote Coupler Communications/Status

   Some LC operations dependent on RC.

   a. Check RC status after master clear.
   b. Check EOP status bit and interrupt.
   c. Force RC reject status bit (station 0 read).
   d. Test lost data status bit.
   e. Test LC master clear.

3. Echo Check

   a. Echo check and compare data.

4. Test Next, Last Address Register

   a. Run echo data through NA and check EOS status for being there.

5. Test PA, FA, LA, NA

   a. Test PA + 1 adder.
   b. Test for EOS interrupt, FA to NA.

6. 1558 Status Function and Interrupt Test

   a. Test clear and disable functions and status bits.
   b. Test busy status coming up.
   c. Test busy going away.
   d. Reject bit (RCS) when 1558 not ready and not wait for ready.
   e. Test wait for ready.
   f. Test interrupt and status bit.
   g. Test select error interrupt.

7. House of Representatives Light Test

   a. Bulb test on/off.
   b. Florescence on.
   c. Pull all relays one at a time, 200-millisecond delay between.
   d. Clear display.

C. SUBROUTINE DESCRIPTIONS

EPT	Enter parameter table with stop 1 and stop 2 parameters.
BQR	Build Q register, add equipment address and EOP interrupt flag to Q, save A, Q.
CEI	Clear and enable interrupts on preselected station address, check station status. Enable RC interrupts.
CLC	Clear LC and set to half duplex.

CRC	Clear RC and check status after.
ECHO	Output, input, compare word found in (DATA) (used by Section 3 only).
ERR	Error reporting routine used by entire test.
FLC	Function LC with RC data and expect busy to come up.
IRH	Interrupt handler routine, inputs LCS, LCI, RCS, RCI, NA value, station status, every time interrupt occurs. Sets bit in (ILEGAL) if given status is rejected. No error reporting is done from IRH.
LAL	Light a light, send (DATA) to CA (A), expect station interrupt within 11 microseconds.
LCF	Local coupler function, no status checking.
RAB	Read a byte, expect data ready, and do a U=11 input.
RDS	Read device status, input LCS, LCI.
REM	Report error messages, report up to five error messages which have been logged since last time buffer was emptied. Empties buffer.
RNA	Read next address register.
RRC	Read RCS, RCI.
RRD	Read remote data from RC.
RSS	Read station status put in STS.
SEM	Save error messages for later reporting.
SNE	Select next equipment, put RC address in REMEQ, set interrupts. Exit P + 1 if found. Exit P + 2 if end of list.
SNS	Select next station address, put in STADD. Exit P + 1 if found, exit P + 2 if end of list.
SRC	Sense repeat condition. See if repeat condition bit is set in Stop/Jump word. Exit P + 1 if it is, P + 2 if not.
SSR	Section select routine. Selects and executes sections, senses repeat sections/test, reports end of section/test, and checks for request parameter entry.
STM	Set test mode, sets test mode in RC, check status.
WDR	Wait data ready or 100 microseconds, which ever is first. Exits P + 1 if data ready, P + 2 if timeout.
WFI	Wait 100 microseconds for interrupt and check for status input errors if interrupted.
WMS	Wait (A) milliseconds on a 1704.
WNB	Wait LC not busy. Wait 20 microseconds for LC to go not busy, report LC status errors and report timeout.
W1704	Wait (A) seconds on a 1704.

VI APPLICATIONS

Normally this test will be run using only Sections 1, 2, 3, 4, 5, and A as these sections require no observation. Those sections should be run with stop on error set.

Upon an error stop, the status series (normal, interrupted) which pertain to the error code should be listed by setting the bits in the Stop/Jump word. Interrupt error status words will always be from the occurrence of the interrupt. Normal errors may not have all status words with the latest status. Some knowledge of what the test was doing is necessary to determine what is legal. It is not possible to impart this knowledge through documentation. Only study of the listing can lead to thorough enough understanding.

For communication line noise, this test has the option to run without type-out and error stops. The last five errors will be recorded continuously. To retrieve this information, merely set bit 11 in the test Stop/Jump parameter word. There will be up to five errors reported, depending on the number of errors since the last error dump or test initialization. The total number of errors is also typed out on the teletype.

HORA4C has another feature to aid the unfamiliar CE in fixing the 1500, **TRACE**. When bit 15 in the Stop/Jump word is a one, the entry address, (A), (Q), and present P address are listed on the printer, if a printer unit is defined. This feature is good for debug, and understanding how HORA4C operates. If **TRACE** is used because of a failure, be warned that timing differences do exist when **TRACE** is in operation. No errors which occur - only - with **TRACE** on should be considered real. Its primary purpose is to define sequences, not failures.

TRACE calls exist in almost all I/O subroutines and since it affects nothing but timing, the internal documentation does not reference a call to it.

A. GLOSSARY OF TERMS AND ABBREVIATIONS USED IN THIS DIAGNOSTIC

ACT	Actual data or status
CA	Sequential channel address
CADD	Address error call came from
ECHO	Remote coupler data turn around
EOP	End of operation (LC)
EOS	End of sequence (NA=LA) (RC)
EXP	Expected data or status
E-FIELD	Equipment field in Q (bits 7-10)
FA	First sequential address register
FCA	Beginning sequential channel address

F	See F-FIELD
F-FIELD	RC function in Q (bits 0-3)
I	See I-FIELD
I-FIELD	LC enable EOP bit (bit 6)
LA	Last sequential address register
LC	Local coupler
LCA	Ending sequential channel address
LCI	Local coupler interrupt status
LCS	Local coupler status
LOCAL COUPLER	1590-2 remote I/O adapter
NA	Next sequential address register
OPA	Operator in A for an I/O output instruction
OPQ	Operator in Q for an I/O instruction
PA	Present sequential address register
RC	Remote coupler
RCI	Remote coupler interrupt status
RCS	Remote coupler status
REMOTE COUPLER	1591-2 remote I/O station
SJ	SMM Stop/Jump parameter word
U	See U-FIELD
U-FIELD	LC usage field in Q (bits 4, 5)
X	Variable digit in error message
(Q)	Contents of Q for operation
(A)	Contents of A for operation

10126 INTERVAL TIMER TEST

(CLK042 Test No. 42)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

   An error typeout of the form:

A	Q	A	Q	A	Q
0038	STJP	0004	XXXX	XXXX	0000

   will result if this test is reinitiated from parameter entry. The subtest requests an interrupt line and only releases this line at the end of the test.

2. Subtest 1 will be run only once before the end of test typeout unless it is the only subtest selected.

B. LOADING PROCEDURE

1. The test operates as a subprogram under control of the 1700 System Maintenance Monitor (SMM17).

2. The calling sequence is that specified by SMM17.

C. PARAMETERS

1. Normal operation requires no parameters.

   a. All subtests will be run under this condition.

   b. Subtest 1 will be run only once under this condition.

   c. The test will be run on equipment 8, and interrupt line 8 will be used.

2. To alter the parameters, follow the directions stated in the SMM17 Reference Manual. If the bit is set, the corresponding subtest or condition will be selected. The parameter words to be displayed are as follows:

   a. First stop:

      A = 4261
      Q = Stop/Jump Parameter

b. Second stop:

A = Equipment address (Prestored as equipment 8)
Q = Interrupt line (e.g. bit 8 set for line 8)
(Prestored as interrupt line 8)

c. Third stop:

A = Test Selection (Prestored to run all 6 subtests)
Bit 0 of A = Subtest 1 - Unused and illegal functions
Bit 1 of A = Subtest 2 - One-msec interval
Bit 2 of A = Subtest 3 - All intervals
Bit 3 of A = Subtest 4 - Selected interval
Bit 4 of A = Subtest 5 - Tenth minute - minute verification
Bit 5 of A = Subtest 6 - Time of day clock subtest
Bits 6 - 15 of A are not used

Q = 0XXX (Prestored as $03E8_{16}$ for 1 second interval)
XXX = Interval selected for testing in subtest 4
Interval selected must be equal to or less than $3FF_{16}$

d. Fourth stop:

A = XXXX (Prestored as 0100_{16})
XXXX = Number of times selected interval in subtest 4 is to be tested.
Q = YYYY (Prestored as 0100_{16})
YYYY = Number of times 1-msec interval in subtest 2 is to be tested.

e. Fifth stop:

A = 00X (Prestored as 0007_{16})
X = Number of passes through SMM17 per msec
Q = YYYY (Prestored as $0E1D_{16}$)
YYYY = Number of passes through SMM17 per 6 sec

f. Sixth stop:

A = XXXX (Prestored as $000F_{16}$)
XXXX = Time limit in minutes (hex) for subtest 6 to run
Q = YYYY (Prestored as 0005_{16})
YYYY = Time limit in minutes (hex) for subtest 5 to run
This Q-register time limit must not exceed 30_{16}.

3. Selective Jump and Stop Settings

Bits 0, 1, 2, and 3 of the Stop/Jump parameter are used in this test. For usage, refer to SMM17 Reference Manual.

D. MESSAGES

1. Normal Program Typeouts

a. Interval timer - day clock indentification during test initialization.

CLK042, 10126 INTERNAL TIMER - DAY CLOCK TEST
IA = XXX, FC = XX

b. End of Test typeout

A	Q	A	Q
4224	Stop/Jump	Pass Number	0000

2. Error Typeouts

a. All information shown is displayed after General Display Format.

General Display Format

A	Q	A	Q
Identification Word (eg. 42X8 X is no. of stops)	Stop/Jump Parameters	Section/Error Code	0000

b. Section/Error Code Descriptions

0001 - Internal reject occurred during interrupt routing on input/output command.

A = number of times internal reject occurred
Q = 0000

A = Contents of A after last internal reject
Q = Contents of Q after last internal reject

0002 - External reject occurred during interrupt routine on input/output command.

A = number of times external reject occurred
Q = 0000

A = contents of A after last external reject
Q = contents of Q after last external reject

0003 - All unused status bits not cleared

A = number of times unused status bits not cleared
Q = E13A - status bits expected to be cleared

A = last set of unused status bits
Q = last complete status with error 0003

0004 - Ready bit not set

A = number of times ready bit not set
Q = last complete status with error 0004

0005 - Interrupt status bit (2) not set when interrupt routine entered

A = number of times interrupt bit not set
Q = last complete status with error 0005

0006 - Specific interrupt bit(s) not set by interrupt condition

A = number of times no specific interrupt bits set by interrupt condition
Q = last complete status with error 0006

0007 - Interrupt status bits not cleared by clear interrupt command

A = interrupt status bits not dropped on command
Q = all possible interrupt status bits

A = status before clear interrupt command given
Q = status after clear interrupt command given

0008 - Lost interrupt bit set

A = number of lost interrupts counted
Q = last complete status with error 0008

0101 - Reply returned for invalid input command
Expected internal reject
Equipment address - director code varies from XX04 to XXFE, where XX is equipment address

A = FFFF = input attempted
Q = invalid equipment address - director code

A = 0000 - contents of A before input
Q = contents of A after input

0102 - Reply returned for invalid output command
Expected internal reject
Equipment address - director code varies from XX04 to XXFE, where XX is equipment address

A = 0000 - output attempted
Q = invalid equipment address - director code

A = 0000 - contents of A before output
Q = contents of A after output

0103 - External reject for invalid input command.
Expected internal reject. Equipment address - director code varies from XX04 to XXFE, where XX is equipment address.

A = invalid equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0104 - External reject for invalid output command. Expected internal reject. Equipment address - director code varies from XX03 to XXFE, where XX is equipment address.

A = 0000 - output attempted
Q = equipment address - director code

0105 - Internal reject for invalid output command. Expected reply. Equipment address - director code XX01 used.

A = function bits output
Q = XX01 - equipment address - director

0106 - External reject for invalid output command. Expected reply. Equipment address - director code XX01 used.

A = function bits output
Q = XX01 - equipment address - director code

0107 - Internal reject returned for invalid output command. Expected external reject to occur. Equipment address - director code = XX00 used.

A = function bits output
Q = XX00 - equipment address - director code

0200 - One - millisecond interval timed out with no interval interrupt received.

A = 0001 - one (1) msec internal being tested
Q = number of subtest passes completed

A = number of subtest passes permitted
Q = 0000

0201 - Subtest 2 (1-msec interval) current timer count greater than selected interval in timing interval register.

A = current timer count
Q = 0001 - interval being tested (1-msec)

0202 - Internal reject on function attempting to read current timer count.

A = XX00 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0203 - External reject on function attempting to read current timer count.

A = XX00 - equipment address - director code 0
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0204 - Current timer count not reset to zero by function output to reset timing interval.

A = non-zero timing interval count just read
Q = 0000

0205 - Internal reject on function input or output.

A = equipment address - director code
Q = FFFF - input command; = 0000 - output command

A = contents of A before input/output
Q = contents of A after input/output

0206 - External reject on function input or output.

A = equipment address - director code
Q = FFFF - input command; = 0000 - output command

A = contents of A before input/output
Q = contents of A after input/output

0207 - Unexpected interval interrupt(s).

A = unexpected interval interrupt counter
Q = 0000

0300 - Variable interval subtest timed out with no interval interrupt received.

A = interval timed out, in msec
Q = 0000

0301 - Subtest 3 (all intervals) current timer count greater than interval currently being tested.

A = current timer count
Q = current interval being tested, in msec

0302 - Internal reject on function attempting to read current timer count.

A = XX00 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0303 - External reject on function attempting to read current timer count.

A = XX00 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0400 - Subtest 4 (selected interval) timed out with no interval interrupt received.

A = selected interval being tested, in msec
Q = number of test passes completed

A = number of test passes permitted
Q = 0000

0401 - Subtest 4 (selected interval) current timer count greater than interval selected.

A = current timer count
Q = interval selected for testing, in msec

0402 - Internal reject on function attempting to read current time count.

A = XX00 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0403 - External reject on function attempting to read current timer count.

A = XX00 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

0500 - Six hundred (600) tenth second interrupts occurred without receiving a 1 minute interrupt

A = tenth second interrupt count
Q = tenth minute interrupt count

A = minute interrupt count
Q = 0000

0501 - Tenth minute interrupts received are incorrect for number of tenth second interrupts received

A = tenth second interrupt counter
Q = tenth minute interrupt counter

A = minute interrupt counter
Q = 0000

0502 - Minute interrupts received are incorrect for number of tenth second interrupts received

A = tenth second interrupt counter
Q = tenth minute interrupt counter

A = minute interrupt counter
Q = 0000

0601 - Unexpected minute interrupt. Time of day clock subtests 5 and 6 inactive

A = number of unexpected minute interrupts received
Q = 0000

0602 - Unexpected tenth minute interrupt. Time of day clock subtests 5 and 6 inactive

A = number of unexpected tenth minute interrupts received
Q = 0000

0603 - Time of day clock tenth minute interrupt request bit set

A = hardware hours-minutes at last minutes interrupt
Q = hardware tenth minutes at last tenth minutes interrupt

A = software clock hours-minutes
Q = software clock tenth minutes

0604 - Time of day clock minute interrupt time out Minute interrupt request bit set

Display same as for error code 0603.

0605 - Time of day clock tenth minute update error. Software clock tenth minutes do not equal hardware clock tenth minute value inputted during last tenth minute interrupt routine.

A = hardware hours - minutes at last minutes interrupt
Q = hardware tenth minutes at last tenth minutes interrupt

A = software clock hours - minutes
Q = software clock tenth minutes

A = minute interrupt count used in last software clock update
Q = tenth minute interrupt count used in last software clock update
A = lost interrupt count
Q = software clock minutes carry

0606 - Software clock minutes carry does not equal minute interrupt count. Display same as for error code 0605.

0607 - Time of day clock minutes-hours update error. Software clock hours-minutes do not equal hardware clock hours-minutes value inputted during last minute interrupt routine.

Display same as for error code 0605.

0609 - Internal reject on function attempting to input hardware hours-minutes time.

A = XX02 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

060A - External reject on function attempting to input hardware hours-minutes time.

Display same as for error code 0609.

060B - Internal reject on function attempting to input hardware tenth minutes time.

A = XX03 - equipment address - director code
Q = 0000

A = contents of A after input
Q = 0000 - contents of A before input

060C - External reject on function attempting to input hardware tenth minutes time.

Display same as for error code 060B

060D - Internal reject on function output to start day clock tenth minute and minute interrupts.

A = function output
Q = XX01 - equipment address - director code

060E - External reject on function output to start day clock tenth minute and minute interrupts.

Display same as for error code 060D.

060F - Internal reject on function output attempting to halt day clock tenth minute and minute interrupts.

Display same as for error code 060D.

0610 - External reject on function output attempting to halt day clock tenth minute and minute interrupts.

Display same as for error code 060D.

II. DESCRIPTION

A. OVERALL CONTROL

1. This test has a main control section which passes control sequentially to each of the six subtests.
2. Each subtest, once it has control, initializes if necessary and runs to completion before the next subtest is begun.
3. Subtest 1, if selected at parameter entry, will be run only once if any other subtests are selected. If no other subtests are selected, subtest 1 will be rerun until stopped. Subtest 1 uses no interrupts and, therefore, cannot be run while any interrupt-type subtests are selected.

4. Subtest 6, if selected at parameter entry, will be initialized and started running during the subtest selection sequence. After initialization, control will periodically be transferred to subtest 6 until the time limit from parameter entry is reached.

B. SUBTEST DESCRIPTION

1. Subtest 1 - Unused and illegal function subtest.

   a. Set flag to allow internal rejects.

   b. Set for first illegal function input.

   c. Input illegal function.

   d. Check for error.

   e. Set up for next illegal input.

   f. Loop to step c. 252 times.

   g. Loop to step b. 9 times.

   h. Set flag to allow internal rejects.

   i. Set for first illegal function output.

   j. Output illegal function.

   k. Check for error.

   l. Set up for first illegal output.

   m. Loop to step j. 252 times.

   n. Loop to step i. 9 times.

   o. Set flag to allow external rejects.

   p. Output illegal function.

   q. Loop to step o. 9 times.

   r. Clear flags to disallow internal and external rejects.

   s. Set for 1st unused function bit output.

   t. Output unused function.

   u. Loop to step s. 7 times.

   v. Loop to step s. 8 times.

   w. Stop on end of subtest.

   x. Clear initialized flag.

   y. Set completed flag.

2. Subtest 2 - 1 msec interval subtest

   a. Check for interrupt routine errors.

   b. Read interval timer, verify timer count valid.

   c. Check for time out.

   d. If interval interrupt, continue. Else exit with control to return to step a.

   e. If subtest finished, jump to step j.

   f. Reset time-out counter.

   g. Stop interval timer.

   h. Start interval timer.

   i. Exit with control to return to step a.

   j. Stop interval timer.

   k. Clear initialized flag.

   l. Set completed flag.

   m. Stop on end of subtest.

3. Subtest 3 - Test all possible intervals

   a. Check for interrupt routine errors.

   b. Read interval timer, verify timer count valid.

   c. Check for time out.

   d. If no interval interrupts, exit with control to return to step a.

   e. If all intervals tested, jump to step k.

   f. Set up next interval.

   g. Reset time out counter.

   h. Stop interval timer.

   i. Restart timer with new interval.

   j. Exit with control to return to step a.

   k. Clear initialized flag.

   l. Set completed flag.

   m. Stop on end of subtest.

4. Subtest 4 - Selected interval subtest

   a. Check for interrupt routine errors.

   b. Read interval timer, verify timer count valid.

   c. Check for time out.

   d. If no interval interrupts, exit with control to return to step a.

   e. If subtest finished, jump to step j.

   f. Reset time-out counter.

   g. Stop interval timer.

   h. Restart interval timer.

   i. Exit with control to return to step a.

   j. Stop interval timer.

   k. Clear initialized flag.

   l. Set completed flag.

   m. Stop on end of subtest.

5. Subtest 5 - Minute and tenth-minute verification subtest.

   a. Check for interrupt routine errors.

   b. If interrupt routine has initiated subtest, jump to step 3.

   c. Check if minute elapsed without interrupt.

   d. If subtest finished, jump to step i. Else exit with control to return to step a.

   e. Transfer interrupt counters.

   f. Check if tenth minute interrupts correct.

   g. Check if minute interrupts correct.

   h. If subtest not finished, exit with control to return to step a.

   i. Clear day clock interrupt request bits if subtest 6.

   j. Stop interval timer.

   k. Clear all interrupt counters.

   l. Clear initialized flag.

   m. Set completed flag.

   n. Stop on end of subtest.

6. Subtest 6 - Time of Day Clock Subtest

   a. Clear all flags.

   b. Check for unexpected interrupts if subtests 5 and 6 both not initialized.

   c. Transfer and clear counters.

   d. Check for tenth minute interrupt time out.

   e. Check for minute interrupt time out.

   f. Update software clock and compare hardware and softward clocks for errors.

   g. If subtest time limit not exceeded, exit.

   h. If subtest time limit up, continue.

   i. Clear interrupt counters and requests.

   j. Clear initialized flag.

   k. Set completed flag.

   l. Stop on end of subtest.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

About 2380 memory locations are required.

B. TIMING (Subtest running alone, no errors)

1. Subtest 1 = 1/5 sec approximately.

2. Subtest 2 - The time required varies with the test count selected 1/2 sec for 100_{16} test count.

3. Subtest 3 - 8 minutes; 47 seconds.

4. Subtest 4 - The time required varies with the interval and/or test count selected.

   4 min. 19 sec 1-sec interval 100_{16} test count
   2 min. 10 sec 1/2-sec interval 100_{16} test count
   1 min. 05 sec 1/2-sec interval 80_{16} test count

5. Subtest 5 - The time required is set at parameter entry.

6. Subtest 6 - The time required is set at parameter entry.

10336-1 REAL-TIME CLOCK
(RTC091 Test No. 91)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

Timing is critical; therefore, control is not returned to the monitor when checking the free running clock. Thus, while Section 1 is running, no other test is able to run.

B. LOADING PROCEDURE

1. This test operates under control of the 1700 System Maintenance Monitor (SMM17)
2. The calling sequence is that specified by SMM17.
3. Restart test after loading by Master Clear, set P = IA, and RUN.

C. PARAMETERS (Order in which they are entered)

A2 = SECTNS — Section Select parameter, prestored as $000F_{16}$

Q2 = PRINLN — Interrupt Line parameter, prestored as 2000_{16}

A3 = BASCYL — Clock Basic cycle, prestored as 5.

0 - 1 sec
1 - 100 ms
2 - 10 ms
3 - 1 ms
4 - 100 usec
5 - 10 usec
6 - 1 usec

Q3 = TIMLIM — Time limit in minutes for testing the free running clock in Section 1, prestored as 5

A4 = SINTER — Selected interval to be tested in Section 2, prestored as $000F_{16}$

Q4 = NUMTIM — Number of times selected interval is to be tested, prestored as 0100_{16}

D. MESSAGES

1. Test title.

   RTC091 SYSTEM 17 REAL TIME CLOCK TEST.
   CPC, VER. 3.1-1

2. Initial Address Message

   IA = XXXX, FC = XX
   (XXXX = starting address of test and XX = frequency count.)

3. Error Messages

   a. FATAL ERROR, ENDING SECTION XX
   Output when an error occurs which causes the entire section to malfunction (XX = section number).

   b. All error messages are in the format specified by SMM17.

   c. Individual Error Codes

Error Code	Description
1	Unexpected interrupt
2	Internal reject during interrupt processing
3	External reject during interrupt processing
4	Invalid count
5	Timeout
6	Interrupt early
7	Interrupt not enable while clock is running
8	External reject during input
9	Internal reject during input
A	External reject during function output
B	Internal reject during function output
C	External reject during read
D	Internal reject during read
E	Count not used by clear controller
F	Interrupt not disabled by clear controller
10	Reply received when reading with Q0=0
11	Internal reject when reading with Q0=0
12	Internal reject with A6 and A7 set on function output
13	Reply received with both A6 and A7 set on function output
14	With clock stopped, count changed
15	Clock stopped after an interrupt
16	Internal reject with A14 and A15 set on function output
17	Reply received with A14 and A15 set on function output
18	External reject when W $\neq$ 0
19	Reply received when W $\neq$ 0

E. ERROR STOPS

1. First Stop
   A1 = ID word
   Q1 = Stop/Jump parameter
2. Second Stop
   A2 = Section number/error code
   Q2 = Return address
3. Third Stop
   A3 = Local I/O routine call address
   Q3 = Number of times error occurred (Section 0 only) or old clock counter value (Sections 1, 2, and 3)
4. Fourth Stop
   A4 = A register (function output)
   Q4 = Q register (equipment code)
5. Fifth Stop
   A5 = Interval being tested
   Q5 = Clock counter

II. TEST DESCRIPTION

A. INITIALIZATION

1. Type out test title.
2. Return control to the monitor.
3. Enter parameters if selected.
4. Request interrupt line.
5. Return control to the monitor.

B. SECTION 0 - TIMER STATIC TEST

1. Clear the controller.
2. Check for counter zeroed.
3. Check for interrupt disabled.
4. Read with Q = 0, repeat $100 times.
5. Check for errors (reply received or internal reject).
6. Return control to the monitor.
7. Output with A6 and A7 set. Repeat $100 times.

8. Check for errors (reply received or internal reject).
9. Return control to the monitor.
10. Output with A14 and A15 set. Repeat $100 times.
11. Check for errors (reply received or internal reject).
12. Return control to the monitor.
13. Output with W field = 0. Repeat $100 times.
14. Check for errors (reply received or external reject).
15. Return control to the monitor.
16. Stop the clock; check if count changes after a long delay.
17. Check for unexpected interrupts.
18. Return control to the monitor.
19. Set up for an interrupt.
20. Check to see if the clock is still running after interrupt occurs.
21. Clear controller.
22. Start the clock.
23. Check to see that interrupts can be enabled while clock is running.
24. End of section.

C. SECTION 1 - FREE RUNNING CLOCK TEST

1. Set up Clock register and number of times to loop through section based on the clock's basic cycle and the time unit.
2. Delay.
3. Get counter value and see if it is valid.
4. Check if done; if not, jump to 2.
5. Otherwise, end of section.

D. SECTION 2 - SELECTED INTERVAL TEST

1. Load Clock register with selected interval.
2. Wait for interrupt to occur.
3. Check if counter value is valid.
4. Check for timeout.
5. No interrupt, go to 2.

6. Otherwise, check if interrupt is early.
7. Check for error during interrupt processing.
8. If done, end of section.
9. Return control to the monitor with IA+5 set to step 1.

E. SECTION 3 - TEST EACH BIT IN CLOCK REGISTER

1. Select interval.
2. If done, end of section.
3. Otherwise, load the Clock register with selected interval.
4. Wait for interrupt to occur.
5. Check if counter value is valid.
6. Check for timeout.
7. No interrupt, go to 4.
8. Otherwise, check if interrupt is early.
9. Check for error during interrupt processing.
10. Return control to the monitor with IA+5 set to step 1.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

Approximately 1200 locations

B. TIMING

Variable, depending on the clock's basic cycle.

C. EQUIPMENT CONFIGURATION

1. 1784 Computer with 4K memory
2. 10336-1 Real-Time Clock
3. Device for loading test

QSE TESTS

Many of the following QSE tests consist of the standard test with changes and additions. These QSE tests have been assigned new test numbers for purposes of distinguishing them from the standard tests on the SMM17 library. However, most of the documentation and typeouts reflect the standard tests' number.

1700/6600 (QSE 3604/3308) ROVER MULTIPLEXER TEST

(RMTA16 Test No. 16)

OPERATING PROCEDURE

RESTRICTIONS

'RMT' must be the only test loaded.

(Part of the monitor is destroyed, so the boot strap should be located at address 2000 above).

All 1700's must be loaded and running before deadstarting the 6600. The 1700 designated for control (number 0) must be the last 1700 loaded. The SLS must be left set until the 6600 is beyond parameter stop. See Section 6 for special restrictions regarding simultaneous operations.

LOADING PROCEDURE

Call as external test number 16 under SMM17.

PARAMETER ENTRIES

1st STOP

Will occur after typeout, 'BEGIN RMT IA = XXXX'
Enter in (A) - EE00
E = E and W fields set up for a direct output.

Enter in (Q) - Stop Jump Parameter

NOTE

Bits 1, 2, 8-14 are pertinent to Control Processor 0 only. Normally Error Stop (Bit 3) should be set only on the control processor.

Bit 0 = Not used.
Bit 1 = Stop at end of section.
Bit 2 = Stop at end of test.
Bit 3 = Stop on error.
Bit 4 = Repeat conditions.
Bit 5 = Repeat section.
Bit 6 = Repeat 2 conditions.
Bit 7 = Suppress typeout.
Bit 8 = Run Section 0 (1700/1700 Switch Test)
Bit 9 = Run Section 1 (Write & Read in all of cm.)
Bit 10 = Run Section 2 (Test Read P Function)
Bit 11 = Run Section 3 (Test Exchange Jump)
Bit 12 = Run Section 4 (Test Monitor Exchange)
Bit 13 = Run Section 5 (Test M.A. Exchange)
Bit 14 = Run Section 6 (Simultaneous Operations Test)
Bit 15 = Suppress Error output on deep end data error.

2nd STOP

Enter in (A) - Interrupt line (I), and Bit corresponding to processor number designation (P).

A = OIPP

Enter in (Q) - Que (Bit corresponding to the processor number of the processor that will maintain preceding control).

NOTE

A Stop Jump Parameter entry stop may be affected by setting the SWS, however, the Stop Jump Parameter may be changed during any stop by entering the desired bits in (Q).

STOP DISPLAYS

Error Stop: (A) = Return address (actual machine).
(Q) = Stop Jump parameter.

Parameter Stop: (A) = Bit to be compared to existing (Q).
(Q) = Stop jump parameter.

End of Test Stop: (A) = FFFF
(Q) = Stop jump parameter.

End of section: (A) = 800S S = Section Number.
(Q) = Stop jump parameter.

MESSAGES

'BEGIN RMT 1A = XXXX'
'WAITING FOR INT.' Will repeat itself until 6000 is deadstarted.
'RESTART ONLY AFTER 6600 PARAMETER STOP' Will follow receipt of deadstart interrupt. Restarting will allow test to commence.
'SET LOCKOUT SWITCH AND TIE LINE FROM SPP0 TO SPP1'
Occurs upon entry into optional test section 0. Restarting will cause section 0 to run.
'RELEASE LOCKOUT AND TIE LINE' Occurs prior to exit from section 0. Restart after release to continue test.

ERROR MESSAGES

'1ER EX 2222 AC 3333 SC 44'

1 = Type of error S = Status error
D = Data error
P = Cm. address error
C = Clear monitor flag failure
2 = Expected
3 = Actual
4 = Section number

'11T REJ A = 2222 Q = 3333'

1 = EX - External reject
IN - Internal reject
2 = Contents of A at time of reject
3 = Contents of Q at time of reject

UNEXPECTED INTERRUPT

Unexpected interrupt received on MUX interrupt line.

UNIDENTIFIED LEVEL XX INT

Unexpected and unselected interrupt received on line XX.

NO EXCHANGE TO XXXX

Exchange jump not performed while running Section 6.

1700/6600/1700 INTER-COMMUNICATION

Communication between 1700's and the 6600 is accomplished through CM. address 0. Zero contains the CCP (Central Control Parameter) which enables sychronization and the passing of control between eight 1700's and one 6600.

CCP

Bits 0 - 7 = Assigned processor bit number.
Bits 8 - 14 = Literal section number.
Bit 15 = Terminator bit (used when one 1700 has completed a section and passes control to another).

Control

Each 1700 that is not in control scans the CCP once every 5 ms. for a terminator bit. When the terminator bit is set and the processor's QUE is set, the processor will wait for the 6600 to clear the QUE and then proceed to assume control and commence testing.

SECTION DESCRIPTION

Subsection 0 (Arbitrary - not parameter selectable)

Perform M. C. function
Read Status
Expect = 0001
Write at C. M. address 0
All zeroes
All ones
Alternate zeroes and ones
Alternate ones and zeroes
Check Status

Expect = 0001

Read patterns written at C. M. address 0

Check Status

Expect = 0001

Check data patterns

Select interrupt function

Typeout 'WAITING FOR INT.' while waiting for deadstart.

Check status after interrupt -

Expect = 0425

Clear interrupt function

Check status

Expect = 0001

Select interrupt function

Typeout - 'RESTART ONLY AFTER 6600 PARAMETER STOP.'

STOP - After restart on QUE control will pass to 1st selected section.

Section 0 (Bit 8 of stop jump parameter) Non-standard. 1700/1700 switch test for processors 0 and 1 only.

Typeout - 'SET LOCKOUT SWITCH AND TIE LINE FROM SPP0 TO SPP1.

A. If processor 1 go to C, otherwise continue at B.

B. Write pattern (1600 word buffer)
Check Status.
If processor 1 go to D, other wise continue.

C. Read pattern (1600 word buffer).
Check status.
Check data.
If processor 1 to A, otherwise exit, continue.

D. Typeout - 'RELEASE LOCKOUT AND TIE LINE'

NOTE

The 1700 waiting for a data flow (either Read or Write) will typeout the rejects until the data is accepted.

Section 1 (Bit 9 of Stop Jump Parameter) Standard. Write to and read from all of Central memory.

Write data equal to the C. M. address at all C. M. locations except 0.
Check status.
Terminate for next 1700 to write and pause for 6600 to check data compliment.
On QUE read all of C. M. and verify that the data is equal to the compliment of the address of each C. M. location.
Check status.

Section 2 (Bit 10 of Stop Jump Parameter) Standard. Read C. M. P address.

Read P and check.
Terminate to allow each 1700 to read same P.
When SSP0 terminates the 6600 will update P (sliding 1's and 0's pattern) repeat for 32 patterns.

Section 3 (Bit 11 of Stop Jump Parameter) Standard. Perform exchange jumps and verify P.

Sequence will repeat itself through the 32 sliding '1s and 0's pattern. Write a double exchange package (primary immediately precedes secondary) Perform Exchange Jump to Primary Package.
Read C. M. P and check.
Pause to allow 6600 to check P. Repeat for new address.

Section 4 (Bit 12 of Stop Jump Parameter) Standard. Perform Monitor Exchange Jumps and verify P.

Same addressing sequence as Section 3 (sliding 1's and 0's)
Write a double Exchange Package.
Perform a Monitor Exchange Jump to primary.
Read P and verify.
Attempt Monitor Exchange to secondary.
Read P and verify no change.
Pause for 6600 to check P.
Clear Monitor Flag (by performing a regular Exchange to a Central Exchange).

Section 5 (Bit 13 of Stop Jump Parameter) Standard. Perform M. A. Exchange Jumps and verify P.

Same addressing sequence as Section 3 (sliding ones and zeroes).
Write a double Exchange package.
Perform a regular Exchange to secondary.
Read P and verify.
Perform M. A. Exchange to primary.
Read P and verify.
Attempt Monitor Exchange to secondary.
Read P and verify.
Attempt M. A. Exchange to secondary.
Read P and verify.
Pause to allow 6600 to verify P.
Clear Monitor Flag.
Repeat for new sliding address.

Section 6 (Bit 14 of Stop Jump Parameter) Non-Standard. Simultaneous PP and SPP test.

In this section all 1700's will be running simultaneously without pause or termination while the 6600 repeatedly writes Exchange Packages and performs Exchange Jumps from all PP's. The SPP's dedicated area of C. M. is equal to the processor number times 5000.

NOTE

End of test stop (Bit 2) must be set in Control Processor before running this section. In order to loop on this section, repeat section (Bit 5) must be set in all 1700's before starting section 6.

Perform M. C. function.
Write 400 words to C. M.
Check status.
Read 400 words from C. M.
Check status.
Check data.
Write an Exchange Package.
Perform a Exchange Jump.
Read P and verify that it is not equal to previous P.
Write 100 words to C. M.
Check status.

Read 100 words from C. M.
Check status.
Check data.
Write an Exchange Package.
Perform an Exchange Jump.
Read P and verify that it is not equal to previous P.
Write 100 words to modified C. M. address.
Read 100 words from modified C. M. address.
Check data.
Modify dedicated core area and repeat once.

1706 Buffered Data Channel Test
W/QSE 3247
Section 6 (Added) (Non-terminating Buffer)
BD3018 Test No. 18
Modification to Test No. A

I. OPERATIONAL PROCEDURES

A. Restrictions

No change.

B. Loading Procedures

No change.

C. Parameter

Add to stop 3 - If all sections were to be run, Q would be set to 003F. Section 6 is an optional section.

D. Selective Skip and Stop Settings

No change.

E. Messages

1. Typeouts or alarms

Normal program typeout

Test identification at start of test. 1706 BDC Test with non-terminating buffer added. Section 6 (optional) added QSE 3247.

2. Error Codes

Added -
Error 2F = The buffer current address was not equal to expected first word address.

A = Actual Current Address
Q = Expected address

Error 30 = Unexpected current address.

A = Actual current address
Q = Expected address

Error 31 - No interrupt when expected. The buffer reached the terminal address with EOP selected, but no interrupt occurred.

Error 32 - Non-terminate status bit (bit 3) did not set after the function.

A = Actual status
Q = Expected status

Error 33 - Unexpected interrupt - Premature, EOP interrupt was received.

II. DESCRIPTION

Added -

G. Section Six (S6)

This section tests non-terminate mode

1. Get control of BDC
2. Rewind tape
3. Select 200 BPI
4. Test for write enable
5. Select non-terminate mode
6. Test status
7. Initiate 500 word output
8. Monitor current address register
9. Test for turn around
10. Terminate buffer
11. Select non-terminate and EOP interrupt
12. Initiate 500 word output
13. Test for premature interrupt
14. Monitor current address register
15. Test for interrupt
16. Test for turn around
17. Increase buffer length by $100
18. Repeat steps 8 through 16

19. Decrease buffer length by $200
20. Repeat steps 8 through 16
21. Terminate buffer
22. Clear non-terminate mode
23. Rewind tape
24. Give up control of BDC
25. Exit

1700 DUAL ACCESS DISK TEST 19

(DAD019 Test No. 19)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions And Instructions To User

a. A large number of typeouts and/or stops may occur for error codes 14 and 1B unless bit 11 of the stop/jump parameter is set.

b. There may be insufficient core for a long buffer operation if memory is only 8K and more than one test is loaded before the disk pack test is loaded. In this case, neither sections 6 or 9 will be run unless the operator selects one or both of them. If the operator selects 6 or 9 in this case, short buffer operations are performed and considerable time will be expended in these sections.

c. At parameter entry time, the operator must select an interrupt line. This line should be hooked to spigot G and is specified in A of the 3rd stop of parameter entry.

If sections 7 or 14 are selected, the operator must select another interrupt line. This line should be hooked to spigot H of the same access and is specified in Q of the 4th stop of parameter entry. For section 14, two lines must be selected on each computer. (See also discussion of parameter entries.)

d. Section 7 (overlap seek) requires at least two disk packs. (See parameter entry discussion for selection of units.) Section 7 should not be chosen if running simultaneously with other SMM tests.

e. When using a new pack, first run section 6 to ensure that the pack is filled with correct data and checkwords.

f. Section 14 assumes the reserved status bit is set and cleared when expected.

g. Section 14 is divided into two parts - Side A and Side B. Two computers are required. Bit 11 of the stop/jump parameter selects Side A and must be selected on one and only one of the two computers. The Side A computer must be placed in Run first. The stop at end of test bit (bit 2) must be set on both computers when running section 14.

h. Section 14 is optional and runs alone when selected.

i. Section 12 will not run unless the controller has the Read Check Word capability.

B. LOADING PROCEDURE - This test is included under the 1700 System Maintenance Monitor (SMM17) and is called in the manner specified by SMM17. The test can be restarted after loading by MC, set P = IA and RUN.

C. PARAMETERS

At the beginning of the test, the parameter stop below will occur, if selected in the stop/jump parameter of SMM.

First Stop: A = ID word (overflow light is on)
Q = Stop/Jump Parameter

Second Stop: A = Section select parameter and 853/854 flag.

Bit 0 - Section 1 - Static status check
Bit 1 - Section 2 - Random positioning
Bit 2 - Section 3 - Write and Read with data check
Bit 3 - Section 4 - Write, Read and check data, using alarm and End of Operation interrupts.
Bit 4 - Section 5 - Force address errors; check Read and Write into next cylinder
Bit 5 - Section 6 - Surface test, using alarm and End of Operation interrupts
Bit 6 - Section 7 - Check overlap seek on all units selected (2 or more units necessary)
Bit 7 - Section 8 - Same as section 4 except uses Alarm and Ready, Not Busy interrupts
Bit 8 - Section 9 - Same as section 6 except uses Alarm and Ready, Not Busy interrupts

Bit 9 - Section 10 - Write address tags
Bit 10 - Section 11 - Positioning timing check
Bit 11 - Section 12 - Read check word test
Bit 12 - Section 13 - Check for recoverable errors
Bit 13 - - Not used
Bit 14 - Section 14 - Dual access control check (CAUTION - see restrictions)
Bit 15 - Set to 0 for 853; set to 1 for 854.

If the operator makes no change in this parameter, Sections 1-5, 8, 9 and 13 are run on an 853.

Q = XXYY, where XX = lowest cylinder on which data is written; YY = highest cylinder on which data is written.

If the operator makes no change in this parameter, the limits XX = 00, YY = 63_{16} are used on 853 packs; XX = 00, YY = CA_{16} are used on 854 packs.

Third Stop: A = Alarm interrupt line (used for Alarm, End of Operation and Ready, Not Busy interrupts. This line is used on spigot G in section 7 and is the "first" interrupt line in section 14. Set bit X for line X.)

Q = Equipment, channel type, and director code. Set Q exactly as it would be for status inputs on the controller.

If the operator makes no change in these parameters, the test uses A = 2 (interrupt line 1); Q = whatever value SMM passed to this test.

Fourth Stop: A = Select unit code. Set bit x to select unit x. The lowest unit selected is used in all sections except section 7. Section 7 uses all units selected. The operator should not select any units which are not physically present.

Q = Other interrupt line, used in section 7 and 14.

If the operator makes no change in these parameters, the test uses A = 1 (unit 0); Q = 0 (no other line specified).

D. SELECTIVE JUMP AND STOP SETTINGS

It is advisable to set bit 11 of the stop/jump parameter to decrease the number of error typeouts for errors 14 and 1B.

II. MESSAGES

A. NORMAL

1. Title typeout:

a. Message: DAD019 1700 Dual Access Disk Pack Test IA - XXXX, FC = XX

b. There is no corresponding stop.

2. Parameter stop, End of Section stops, and End of Test stops if specified in stop/jump parameter.

B. ERROR

1. Format: All error typeouts/halts will operate in the standard SMM 17 error format, namely:

A	Q	A	Q	A	Q
ID	STJP	Sect. #; error code	Rtn. Add.	Act.	Exp. .....

The corresponding error stops are:

Stop 1 - (A) = ID word
(Q) = Stop/Jump Parameter

Stop 2 - (A) = XXYY, where XX = section number, YY = error code
(Q) = Return address

Stops 3, 4, 5 - (A) = Actual
(Q) = Expected

(See individual errors for what the Actual and Expected above represent on stops 3, 4, and 5.)

2. Individual Errors:

Error Code	Comments
01	Internal reject on input to A A = BADD Q = Contents of Q upon input to A A = Contents of A upon last output from A Q = Contents of Q upon last output from A
02	Internal reject on output from A A = Director status Q = Address register status A = Contents of A upon last output from A Q = Contents of Q upon last output from A
03	Interrupt status bit not set when interrupt occurred. A = Selected interrupts 1. Ready, Not Busy 2. End of Operation 4. Alarm 8. Seek interrupt Q = Status upon interrupt A = Contents of A upon last output from A Q = Contents of Q upon last output from A
04	A non-selected interrupt occurred, or a selected interrupt occurred too soon. The display is the same as for error 03.
05	Interrupt status bits not cleared by a Clear interrupt function. A = Status upon interrupt Q = Status after attempting to clear interrupts. A = Contents of A upon last output from A (other than clear interrupt function). Q = Contents of Q upon last output from A (other than clear interrupt function).

2. Individual Errors: (Cont'd)

Error Code	Comments
06	Ready status not present A = Director status Q = Address register status A = Contents of A upon last output from A (other than clear interrupt function). Q = Contents of Q upon last output from A (other than clear interrupt function).
07	On cylinder status not present A = Director status Q = Address register status
08	Busy not present after output from A. Display same as for error code 06.
09	Seek interrupt status when not expected. Display same as for error code 06.
0A	Defective track. Display same as for error code 06.
0B	Address error. Display same as for error code 06.
0C	Seek error. Display same as for error code 06.
0D	Lost data. Display same as for error code 06.
0E	Checkword error. Display same as for error code 06.
0F	Other access reserved (unexpected). Display same as for error code 06.
10	Alarm condition present, but alarm status bit not set. Display same as for error code 06.
11	Address register status does not equal loaded address after loading address and waiting for Not Busy.

2. Individual Errors: (Cont'd)

Error Code	Comments
12	Unexpected Busy status after End of Operation comes up on a Read or Write.
13	Internal reject on status input from buffer channel.
14	Word written does not equal word read (this may occur in sections 3, 4, 5 and 8 of the test). Set bit 11 in the stop/jump parameter to ignore checking for more errors in this sector. A = Address register status Q = Number of word in error A = Word written Q = Word read
15	Not used
16	Alarm interrupt did not occur when attempting to force address error by loading illegal address. A = Director status Q = Address status A = Interrupt line Q = Selected interrupts (see error code 03)
17	An address error was forced but the address error status bit was not set. A = Loaded address Q = Director status
18	No alarm interrupt occurred when attempting to force address error by initiating checkword check with illegal address. Display same as for error 16.
19	Address error status not present when writing off the end of disk pack. Display same as for error 17.
1A	Not used
1B	Unexpected data was read during surface test. Set bit 11 in stop/jump parameter to ignore rest of errors in this sector or track.

2. Individual Errors: (Cont'd)

Error Code	Comments
	A = Sector in error Q = Number of word in error A = Data expected Q = Data read
1C	Maximum positioning time (145 ms) was exceeded. A = Time required (ms, hexidecimal) Q = Loaded address
1D	Not used
1E	End of Operation status not present. Display same as for error code 16.
1F	Status other than Ready, On cylinder is present (ignoring protect status) during static status check. Display same as for error code 07.
20	Alarm interrupt did not occur when writing off the end of disk pack. Display same as for error code 16.
21	No interrupt occurred when End of Operation or Ready, Not Busy interrupt was selected. A = Selected interrupts (see error code 03) Q = Director status A = Contents of A upon last output from A Q = Contents of Q upon last output from A
22 and 23	Not used
24	Alarm status bit set; no alarm conditions. Display same as for error code 06.
25- 2F	Not used
30	Address upon completion of a Read, Write or Checkword check is not equal to the expected address.

2. Individual Errors: (Cont'd)

Error Code	Comments
	A = Contents of Q upon last output from A (other than Clear interrupt function). Q = Director status A = Address register status Q = Expected address
31	Recoverable error occurred during checkword check (section 13). A = Address of track causing error Q = Director status when last error occurred
32	Non-recoverable error occurred during checkword check (section 13). Display same as for error code 31.
33	Not used
34	Unexpected interrupt on reserve release - first interrupt line.
35	Unexpected interrupt on reserve release - other interrupt line.
36	No expected interrupt on reserve release - first interrupt line.
37	No expected interrupt on reserve release - other interrupt line.
38	Release reserve function on Side B (Computer B) failed to drop reserve status on Computer A.
39	Release reserve function on Side A failed to drop reserve status on Side B.
3A, 3B	Not used
3C	Reserve override request failure - Side B failed to override Side A.
3D	Reserve override request failure - Side A failed to override Side B.

2. Individual Errors: (Cont'd)

Error Code	Comments
3E	Not used
3F	Not used
40	Reject on Select function (unexpected).
41	Reject on either a Release Reserve function or on a Clear Controller function (unexpected).
42	Reject on load address (unexpected)
43	Reject on Write (unexpected).
44	Reject on Read (unexpected).
45	Reject on checkword check (unexpected).
46	Unexpected Reserve status (Side A).
47	Unexpected Reserve status (Side B).
48	No Reserve status when expected (Side A).
49	No Reserve status when expected (Side B).
4A	No expected reject on Select function.
4B	No expected reject on load address.
4C	No expected reject on Write.
4D	No expected reject on Read.
4E	No expected reject on checkword check.
4F	Reject on non-reserved Director function.
50	Not used
51	Reject on status input.
52	Reserve overridden with bit 15 of A alone set when executing a non-reserved Director function (Side B).
54 - 6F	Not used

2. Individual Errors: (Cont'd)

Error Code	Comments
70	Operator error - parameters were incorrectly entered (multiple lines specified on alarm interrupt line, equipment address in error; or no unit specified).
71 - 7F	Not used
80	Internal reject on Select function in seek interrupt processor (spigot G)
81	Internal reject on status input in seek interrupt processor (spigot G).
82	Interrupt on seek occurred, but there is no expected Seek Interrupt status (spigot G). A = First unit Q = Second unit A = Actual status read on first unit Q = Actual status read on second unit A = Address to which first unit is positioning Q = Address to which second unit is positioning
83	Seek interrupt occurred, but neither of the selected units have selected On-sector status (spigot G). A = First unit Q = Second unit A = Actual status on first unit Q = Actual status on second unit A = Address to which first unit is positioning Q = Address to which second unit is positioning
84	Internal reject on load address function in seek interrupt processor (spigot G).
85	Internal reject on input of one word is seek interrupt processor (spigot G).

2. Individual Errors: (Cont'd)

Error Code	Comments
86	Internal reject on re-select of seek interrupt in seek interrupt processor (spigot G).
87 - 8D	Same as 80 - 86, except on spigot H.
8E	Expected seek interrupt did not occur on unit specified. A = Unit Q = Address to which this unit was being positioned.
8F	Actual check word did not = simulated A = Actual checkword Q = Simulated checkword
90	External reject on output from A A = Director status Q = Address Register status A = Contents of A upon last output from A Q = Contents of Q upon last output from A

III. DESCRIPTION

A. SECTION 1. STATIC STATUS CHECK

Check for presence of Ready and On Cylinder status, and that no other status (other than protected) is present. Loop 499 times.

B. SECTION 2. RANDOM POSITIONING CHECK

Generate 96 random numbers, convert to legal addresses, select a unit, load address on it, and check for the expected address. Alarm conditions and End of Operation status are also checked.

C. SECTION 3. WRITE, READ AND CHECK DATA

Ninety-six random words and one random address are generated. The unit is positioned to the random address, a sector is written and Alarm and End of Operation status is checked. The Select, Load address and Write are repeated if Repeat conditions are selected. We then re-select, output a load address and read. Loop on this if repeat conditions.

III. DESCRIPTION (Cont'd)

C. SECTION 3 (Cont'd)

Re-select and execute a checkword check, checking Not Busy, Alarm, and End of Operation statuses. Loop if Repeat conditions. Check input buffer area against output buffer area. The entire procedure is repeated 95 times before going on.

D. SECTION 4. WRITE, READ AND DATA CHECK UNDER INTERRUPT CONTROL

This section is similar to section 3, but with the following differences:

1. Interrupts on Alarm and End of Operation are selected prior to performing a load address, Write, Read and Checkword Check operation. After the interrupt occurs, the status upon interrupt is checked for alarm conditions.

2. This section writes only a partial sector and Reads are executed on the entire sector, checking proper zero fill.

E. SECTION 5. GENERATE ILLEGAL ADDRESS (00F0) AND SELECT INTERRUPT ON ALARM

Load the illegal address and check that the interrupt occurs and that Address Error status is present. Repeat for a checkword check. Generate illegal address (FF00) and repeat the above. Form the last sector address of the unit (CA9F for 854, 639F for 853) and write off end of pack (unless cylinder CA9F of 639F is excluded at parameter entry). Check Alarm and Address Error statuses. Write 97 words at a legal address. Write 97 words (into next cylinder), read the 97 words and check data. The entire procedure is checked 95 times before continuing.

F. SECTION 6. SURFACE CHECK

Set up read and write routines for a 1536 word buffer (one sector) depending on available core. Generate a 6161 pattern on first pass-through section; CECE pattern on second, and fill the buffer area with the pattern, alternate words complemented. This process is repeated for every track (or sector) of the disk. Then read the data and check for proper pattern, repeating for every track.

III. DESCRIPTION (Cont'd)

G. SECTION 7. CHECK OVERLAP SEEK

The test examines all units selected at parameter entry time, picks a pair of them and generates a pair of random addresses to be used in address seeks. The first unit is selected, seek interrupt on spigot G is selected, and a load address is performed. The second unit is selected and seek interrupt is selected on spigot H. Check for expected seek interrupts, for seek interrupt status upon the interrupt, and for selected on-sector status on one of the two units when interrupt occurs. Reverse the roles of the two units and repeat. Repeat these two permutations using different addresses twenty times and then pick another combination of two units. This process is repeated until all combinations of units, taken two at a time, have been tested.

H. SECTION 8. WRITE, READ AND CHECK DATA UNDER INTERRUPT CONTROL

Same as section 4, except interrupts on Alarm and Ready, Not Busy are selected.

I. SECTION 9. SURFACE CHECK

Same as section 6, except interrupts on Alarm and Ready, Not Busy are used.

J. SECTION 10. WRITE ADDRESS TAGS

Write address tags on the entire disk.

K. SECTION 11. POSITIONING TIME CHECK

Generate 96 random legal addresses and overlay with several of the highest and lowest possible addresses. Check that the positioning time never exceeds 145_{10} ms.

L. SECTION 12. READ CHECK WORD TEST

Write four fixed data records at random addresses. Select checkword read and read 97 words, check data and checkword. Repeat 91 times using random data.

III. DESCRIPTION (Cont'd)

M. SECTION 13. CHECK RECOVERABLE ERRORS

Select unit and position to 0. Initiate checkword check and Wait Not Busy. Check status for checkword check, lost data, defective track errors. Tally any errors found and go on. Repeat until all tracks have been checked.

N. SECTION 14. TEST DUAL ACCESS FEATURES (requires two 1704 processors - one on each access).

This section sets up interrupts, and then each side tests bit 11 of the stop/jump parameter to determine whether it is Side A or Side B. Side A is put in Run first.

SIDE A Side A of the test performs the following:

1. Select unit and check that there is no reserved status. Report error if there is. Flash overflow to tell the operator to place Side B in Run at this point.
2. Check all combinations of the non-reserved director function bits A12 - A15 (interrupt on release reserve, enable interrupt 1 (spigot G), enable interrupt 2 (spigot H), and interrupt select.) Check that interrupts on reserve release do occur when expected, and do not occur when unexpected.
3. Clear Side A and wait for Side B. Side B now tests interrupts on release reserve in the same manner as Side A did in step 2. Side A selects and releases the controller as required by Side B.
4. Select Side A and wait for Side B to execute reserve override function.
5. Execute a non-reserved director function of bit A15 only (interrupt select). Check that it does not clear Reserve status.
6. Check Reads, Writes, checkword checks, load addresses and unit selects on Side A. These reserved functions should reject.
7. If repeat condition is chosen, loop to 4.
8. Execute and check Override function with bit A15 also set.
9. Check reserved functions to be sure they do not reject. During this time, Side B is performing the same operations as Side A did in steps 4 through 7.
10. Await Side B to execute override function. Exit when it does.

III. DESCRIPTION (Cont'd)

SIDE B Side B of the test performs the following:

1. The computer halts, waiting until Side A flashes its OVERFLOW indicator. At this time, the operator should place Side B in Run.
2. Select and release the controller while Side A tests interrupts.
3. Select the controller and check all combinations of the non-reserved director functions A12 - A15 (interrupt on release reserve, enable interrupt 1 - spigot G, enable interrupt 2 - spigot H, and interrupt select). Check that interrupts on reserve release do occur when expected, and do not when unexpected.
4. Wait until Side A reserves the controller and execute reserve override function.
5. Check Reads, Writes, checkword checks, load addresses and unit selects on Side B. These reserved functions should not reject, as Side B has the controller at this time.
6. Await override by Side A.
7. Check reserved functions to be sure they reject (Side A now has control).
8. Loop to 7 if repeat conditions is chosen.
9. Execute a non-reserved director function of bit A15 only (interrupt select). Check that it does not clear Reserve status.
10. Override Side A. This flags Side A that we are finished. Exit.

Please note: A failure on one side may cause error messages on the other side also. For example, a failure in the override function on one side would cause failures in rejects on reserved functions on the other side. Section 14 depends upon the reserved status bit for control.

IV. EQUIPMENT CONFIGURATION

1704/Dual Access Controller/ one 853 or 854 pack for sections 1 through 6; 8 through 13.

1704/Dual Access Controller/ 2 or more 853 or 854 packs for section 7.

Two 1704's, one on each access of the Dual Access Controller, and one 853 or 854 pack for section 14.

1700/415 CARD PUNCH
(CP1021 and CP2022 Test No. 21 and 22)
QSE 5986

I. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

This test operates under the control of the 1700 SMM. The calling sequence is that specified by SMM. The test can be restarted at initial address +2. The tests are divided into two separate tests - Test 21 including Sections 0-5 and Test 22 including Sections 6-C. The two tests are run alone type tests and cannot be loaded with additional tests.

NOTE

Compare errors are forced in Test 21 - Sec. 1.

B. PARAMETERS

The initialization portion of the test sets parameters to test the punch. It also sets the interrupt line(s) parameters. If a parameter stop is selected, these parameters may be altered.

1. Selective Stops

   a. Parameter

      1. A = 2141
         Q = Stop/Jump

      2. A = Selected Sections
         Q = 0 - 320 Word Memory
             1 - 512 Word Memory

      3. A = Data Interrupt Line
         Q = Alarm Interrupt Line

      4. A = EOP Interrupt Line
         Q = 0 - AQ I/O
             1 - Buffer I/O

b. End of Section

1. A = 2122
   Q = Stop/Jump

2. A = 0X00 (X = Section Number)
   Q = Return Address

c. End of Test

1. A = 2124
   Q = Stop/Jump

2. A = Pass Count
   Q = Return Address

d. Error (See Section D)

2. Selecting Stops and Jumps (Stop/Jump Word)

Bit	Stops
0	Enter Parameters
1	End of Section
2	End of Test
3	Error
Bit	**Jumps**
4	Repeat Identical Condition on Error
5	Repeat Section
6	Repeat Test
7	Omit Simulation
8	Omit Typeouts
9	Bias Return Address Display

C. MESSAGES

1. Normal Program Typeouts

a. Initialization of Test

CP1021, 415 Card Punch Test or CP2022, 415 Card Punch Test
1A = XXXX, FC = XX

b. End of Pass Through Test

A	Q	A	Q
2124	Stop/Jump	Pass Count	Return Address

2. Error Types

00 - Punch Not Ready
01 - No data status
02 - Data compare error in punch memory
03 - Illegal reply on rejectable function
04 - Punch should be Busy
05 - Should have EOP
06 - Should have interrupt status on EOP interrupt
07 - Interrupt response not cleared
08 - Compare error
0B - No alarm interrupt on Not Ready.
0C - No alarm status on Not Ready.
0E - No alarm interrupt on Maintenance Mode.
0F - No alarm status on Maintenance Mode.
14 - No blank fill in card buffer memory on Single Pick.
12 - No maintenance mode status
13 - No Protect status
15 - No feed Fail status
16 - No alarm interrupt on Compare Error.
18 - No alarm status on Compare Error.
7F - Internal reject.
7F - External reject from controller.
19 - No compare error status
1A - No data interrupt
1B - No EOP interrupt
1C - No Punch Disable Status
1D - Ready Status On Punch Disable
1E - Constant Busy Status From Controller
1F - Timing Fault Status After Punch

D. ERROR STOPS AND TYPEOUTS

A	Q	A	Q	A	Q
TNX8	Stop/Jump	0SZZ	Ret. Adr.	VVVV	WWWW

Where TN = Test Number
X = Number of Stops
S = Section Number
ZZ = Error Code
VVVV = 1) Failing Data Word
2) (A) When Illegal Reject Occurred
WWWW= 1) Correct Data Word
2) (Q) When Illegal Reject Occurred.

II. DESCRIPTION

The program consists of eleven sections, plus two optional sections, and is divided into two tests. Test 21 includes Sections 0-5 and test 22 includes Sections 6-C. Each section starts with a title card followed by the specific cards of the section ending with two end-of-file cards. The title card consists of one BCD character in column one; the end-of-file cards have 7-8 in column one.

PART I.

Title A. Section 0 - Basic Data Line, Function, Memory, and Status Check

1. Check for Ready and Data status
2. Clear controller function
- Check for Ready and Data
3. Load memory function
- Check for Ready and Data
4. Write pattern in controller memory (0's)
- Check for Ready and Data
5. Clear controller function
- Check for Ready and Data
6. Read from memory function
- Check for Ready
7. Input all memory
- Check for Ready
- Check for correct data
8. Clear controller function
- Check for Ready and Data

Repeat from 3, using patterns of FFF_{16}, AAA_{16}, sliding one bit, sliding zero bit, and worst pattern - CCC_{16}.

9. Issue one function at a time
(01, 02, 03, 04, 09, 10, 11, 12)

01 - Clear interrupt - Check Ready, Data
02 - Data interrupt request - check Ready, Data
03 - EOP interrupt request - check Ready, Data
04 - Alarm interrupt request - check Ready, Data
09 - Load memory - check Ready, Data
10 - Select binary mode - check Ready, Data
11 - Select coded mode - check Ready, Data
12 - Read from memory - check Ready

10. Check for illegal reject following each function

11. Clear controller for each function

12. Repeat 1-11 20 times

13. Punch BDC A in column one

Punch 1 20B 40B 100B 200B 400B 1000B	holes	Holes start in row 9 and fill successive even columns starting in column 2 until number of holes is punched - 1000B holes then uses row 7 of successive odd columns to punch the last 32 holes
Punch 4	holes	7-8 column 1, 4-5 column 2 (file card)
Punch 10B	holes	7-8 column 1, 4-5-6-7-8-9 column 2 (file card)

14. While punch is Busy, issue these functions separately for each card punched.

00 - Clear controller - check Ready, Busy
07 - Repunch - check Ready, Busy
09 - Load Memory - check Ready, Busy
10 - Select binary - check Ready, Busy
11 - Select coded - check Ready, Busy
12 - Read memory - check Ready, Busy
- Check for legal reject after each function
01 - Clear interrupt - check Ready, Busy
- Check for illegal reject after each function

Title L. Section 1 - Compare Error and Alarm Interrupt (Non-Standard Section)

1. Punch 40 laced (all 1's) cards and issues an "Alarm Interrupt" function after the punch has gone Busy. After each card is punched, one of 80 column bits in card buffer 1 or card buffer 2 memory is changed from a "1" to "0" until 40 columns are. The rows are alternated from 12 through 9. After each card:

   a. Verify that Alarm interrupt occurred.

   b. Verify status (compare error, alarm).

   c. Clear interrupt and clear controller - use to clear interrupt

   - Verify they do clear interrupt.

2. Same as 1 except "Alarm Interrupt" function is issued before the punch goes Busy. Check second group of 40 columns after each card.

   a. Verify interrupt occurred.

   b. Verify status (compare error, and alarm).

3. Same as 1 and 2 except using blank cards and changing from "0" to a "1".

4. On last 40 cards, re-toggle changed bit in memory, and issue repunch function.

Title B. Section 2 - Sequence Cards

Punch binary 10 - 27 in column 1

Title C. Section 3 - Binary Cards

1. Using binary mode, punch from 5-124 in columns 1-80 (three cards).

2. Punch alternate columns of 5252 and 2525 with 7-9 in column 1 (three cards).

3. Punch alternate columns of 2525 and 5252 (three cards).

4. Alternate 12 columns of 2525 and 12 columns of 5252 (three cards).

5. Punch blank card.

Title D. Section 4 - Single Punch Cards

1. Punch row sequence 12 to 9 and repeat. Issue a "Data Interrupt" request and select interrupt after punch goes busy (three cards).

- Verify status (Data)

- Check clear interrupt functions.

2. Punch row sequence 9 to 12 and repeat. Issue "Data Interrupt" request when punch is Not Busy.

- Verify status and clears

3. Heavy punching on upper portion of card (three cards)

4. Heavy punching on lower portion of card (three cards)

5. 12 punch in column 1 (three cards)

6. 9 punch in column 1 (three cards)

7. 12 punch in column 80 (three cards)

8. 9 punch in column 80 (three cards)

9. 12 - 9 column 1 (three cards)

10. 12 - 9 column 80 (three cards)

Title E. Section 5 - Punch Pattern Cards

1. Punch alternate four columns of 2525 and four columns of 5252

1463	6314
0707	7070
7417	0360
6037	1740

2. Punch each column 2525, 3333, 3567, 6757, 3737, 4034, 1601

3. Alternate four column sets of 6334, 5322, 3555, 5276, & 2450
   5322, 3555, 5276, 2450, & 6334
   3555, 5276, 2450, 6334, & 5322
   5276, 2450, 6334, 5322, & 3555
   2450, 6334, 5322, 3555, & 5276

4. Alternate four column sets of 3777, 7767, & 7757 (ten cards)

PART II.

Title F. Section 0 - Hollerith Cards

1. Using coded mode, punch BCD codes 00 to 77 in columns 1-64 (five cards)

2. Punch random BCD codes (fifteen cards)

3. Punch blank card

Title G. Section 1 - Punch Memory Cards

1. After each write function, issue and select an "End of Operation" interrupt
   - Verify that interrupt occurred
   - Check Clear interrupt and status (EOP, interrupt)
   - Repeat for 1st two cards
2. Alternate eight columns 1030 eight columns 4102 (2)
   0604 2041 (2)

   eight columns 4102 eight columns 1030 (2)

2041	0604 (2)
5132	2645 (1)
2645	5132 (1)
6747	3675 (2)
7173	5736 (2)
3675	6747 (2)
5736	7173 (2)

3. The second cards of a pattern are punched after one pass is made on each pattern.

Title H. Section 2 - Full and Part Laced Cards

1. Punch full laced card (three cards)
2. Punch 1-2 laced, use "Start Motion function" to punch card
3. Punch 1-4 laced, use "Start Motion function"
   1-8
   1-16
   1-32 laced plus 12 column 80
4. Punch 79-80 laced
   77-80
   73-80
   65-80
   49-80 laced plus 12 column 1

Title I. Section 3 - Half Random Cards

1. Punch random data past column 40 (10 cards)
2. Punch random data before column 41-two card write (10 cards)

Title J. Section 4 - Random Cards

1. Punch 100 - random hole count, random hole placement
2. Offset every other card, varying the time between the punch going Not Busy until the time to issue the function from 0 to 54 msec.
3. Vary the time between punching each card from 0-10 seconds.

Title M. Section 5 (optional) - Non-Standard Codes 0-10 seconds

1. Load memory with non-standard codes in conversion table
2. Punch BCD codes 0-77 using non-standard codes in table

   Non-Standard Code Table:

   Non-Standard BCD Code 00 = Standard BCD 40
   01 = 41
   ... = ...
   37 = 77

   Non-Standard BCD Code 40 = Standard BCD 00
   ... = ...
   77 = 37

Title N. Section 6 (optional) - Alarm Interrupt on punch Not Ready, Maintenance Modes; Feed Fail; Protect Status

1. Issue "Alarm Interrupt" function
2. Type out message - "Set Punch Not Ready"

- Operator makes punch Not Ready
- Verify that alarm interrupt occurred
- Check status (Alarm, Interrupt)
- Clear controller

3. Issue 00, 01, 09, 10, 11, 12 functions separately.

   00 - Clear controller
   01 - Clear interrupts
   09 - Load memory
   10 - Select binary
   11 - Select coded
   12 - Read memory

- Check for illegal reject
- Clear controller after each function

4. Issue 02, 03, 04, 07, 08 functions separately

   02 - Data interrupt
   03 - EOP interrupt
   04 - Alarm interrupt
   07 - Repunch
   08 - Offset

- Check for legal Reject
- Clear controller after each function

5. Type message - "Make Punch Ready."

- Issue "Alarm Interrupt" function
- Type Message "Set Punch Disable"
- Check for punch disable status
- Check for Not Ready status
- Type message - "Clear Punch Disable"

6. Type message "Maintenance Mode"

- Operator makes punch Ready, sets Maintenace Mode
- Verify Alarm interrupt occurred
- Check status (Maintenance Mode, Ready, Alarm Interrupt)

7. Type message - "Clear maintenance mode - Set PROTECT switches"

- Clear Controller
- Operator performs task
- Check for protected status
- Issue function with a without protect bit set checking for rejects
- Should reject with protect bit cleared.

8. Type message - "Clear Console PROTECT Switch."

- Check Card buffer for blanks code (008_{16}) - coded mode used.
- Assure acceptance of functions.
- Type message - "Clear Equipment PROTECT Switch."

9. Type message - "Empty the Hopper"

- Operator should remove all cards from hopper.

10. Issue "Start Motion" function

- Check status for Feed Fail.

BCD CODE TABLE

BCD	HOLLERITH	N-S
00	0	40
01	1	41
02	2	42
03	3	43
04	4	44
05	5	45
06	6	46
07	7	47
10	8	50
11	9	51
12	2, 8	52
13	3, 8	53
14	4, 8	54
15	5, 8	55
16	6, 8	56
17	7, 8	57
20	12	60
21	12, 1	61
22	12, 2	62
23	12, 3	63
24	12, 4	64
25	12, 5	65
26	12, 6	66
27	12, 7	67
30	12, 8	70
31	12, 9	71
32	12, 0	72
33	12, 3, 8	73
34	12, 4, 8	74
35	12, 5, 8	75
36	12, 6, 8	76
37	12, 7, 8	77
40	11	00
41	11, 1	01
42	11, 2	02

BCD CODE TABLE (Cont'd)

BCD	HOLLERITH	N-S
43	11, 3	03
44	11, 4	04
45	11, 5	05
46	11, 6	06
47	11, 7	07
50	11, 8	10
51	11, 9	11
52	11, 0	12
53	11, 3, 8	13
54	11, 4, 8	14
55	11, 5, 8	15
56	11, 6, 8	16
57	11, 7, 8	17
60	Blank	20
61	0, 1	21
62	0, 2	22
63	0, 3	23
64	0, 4	24
65	0, 5	25
66	0, 6	26
67	0, 7	27
70	0, 8	30
71	0, 9	31
72	0, 2, 8	32
73	0, 3, 8	33
74	0, 4, 8	34
75	0, 5, 8	35
76	0, 6, 8	36
77	0, 7, 8	37

QSE 1811
1738 DISK PACK TEST
SECTION 14 (ADDED TO TEST 08) (DUAL ACCESS CONTROLLER)
(DP2A25 Test No. 25)

I. OPERATIONAL PROCEDURES

A. RESTRICTIONS

1. Section assumes that Reserved Status bit is set and cleared when expected.
2. Section is divided into two parts - side A and side B. Bit 11 of the Stop/Jump parameter selects side A and must be set on only one computer.
3. Section 14 is optional and will run alone when selected.
4. Side A must be placed in Run first.
5. Stop at End of Test (bit 2) must be set on both computers.

B. LOADING PROCEDURES

1. Side B - Autoload and call as test number 25. Do not set Bit 11 of Stop/Jump. parameter. Call section 14.
2. Side A - Autoload and call as test number 25. Set Bit 11 of Stop/Jump Parameter. Call section 14.
3. When overflow indicator flashes on computer selected as side A, place side B in run.

II. MESSAGES

A. NORMAL MESSAGES

No change.

B. ERROR MESSAGES (Added to Test 08)

33 - Reject of Select function
34 - Reject of De-select function
35 - Unexpected status
A = Actual
Q = Expected

36 - Reject of Load Address
37 - Reject of Write
38 - Reject of Read
39 - Reject of Compare
3A - Reject of Check Word Check
3B - Not used
3C - No reserved status when expected
3D - No reject of Load Address when expected
3E - No reject of Select Function when expected
3F - No reject of Write when expected
41 - No reject of Read when expected
42 - Reject of a Select Interrupt function
43 - Reserved status when not expected
44 - No interrupt when expected
45 - No reject of compare when expected
46 - No reject of Check Word Check when expected
47 - No reject of Write Address when expected
48 - Reject on initial Connect
49 - Reject of status input

III. DESCRIPTION

A. Unit is de-selected to eliminate the Connect from the autoload.

B. Bit 11 of the Stop/Jump parameter is tested to determine whether this is side A or side B of the test.

C. SIDE A

1. Status is tested expecting no Reserved status.

2. The unit is selected.

3. The following functions and operations are executed expecting no reject.

a. Select

b. Load address

c. Write

d. Read

e. Compare

f. Check Word Check

4. The unit is de-selected.
5. Stop/Jump parameter is tested for repeat conditions.
6. The unit is selected.
7. Next Not Busy and Not Reserved interrupt is selected.
8. The unit is de-selected.
9. The overflow indicator is flashed waiting for reserved status from side B operations. (Place side B in Run.)
10. The following functions and operations are executed expecting to be rejected.
    a. Select
    b. Load address
    c. Write
    d. Read
    e. Compare
    f. Check Word Check
11. Status is tested waiting for Not Reserved.
12. The unit is selected.
13. Status is tested expecting Interrupt and Ready.
14. The interrupt flag is tested to determine whether interrupt occurred as expected.
15. Unit is de-selected.
16. Status is tested waiting for Not Reserved.
17. Exit section.

D. SIDE B

1. Side B is placed in Run.
2. Status is tested expecting No Reserved status.
3. Unit is selected.
4. The same functions as paragraph 3 side A are executed expecting no Rejects.
5. Stop/Jump parameter is tested for Repeat conditions.
6. Interrupt on next Not Busy and Not Reserved is selected.
7. Unit is de-selected.

QSE 3311
1706/1716 CHANNEL TEST
(BD4026 Test No. 26)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

Section 7 should be run only on 1706 Channels with look-ahead features. (Equipment - Configurator DT 106A)

B. LOADING PROCEDURE

1. The test operates under control of 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17. The test number for the 1706/1716 test is 26.

C. PARAMETERS

1. If bit 0 of the Stop/Jump word is set, the program will allow for test parameter display and/or entry. The first stop made in the parameter sequence displays the identification word in A (0F31) and the Stop/Jump word in Q.

   The second and third stops display the test parameters. The test parameters can be changed by the operator at the time when they are displayed. The contents of the A and Q registers on the second and third stops are defined below.

   a. Stop 2

      For non look-ahead 1706 channels and 1716 buffer channels, A = WE01, where the W field is bits 15-11 and identifies the 17X6* equipment address. The allowable values for the 5-bit W field are:

      00010 - for 17X6 number 1
      00111 - for 17X6 number 2
      01100 - for 17X6 number 3

      The E field is bits 10-7 and identifies the 1731 Magnetic Tape Controller. (Q = 000U, where U specifies the 601 or 602 Magnetic Tape Unit which will be used for I/O in sections 2, 3, and 4).

*17X6 refers to either 1706 or 1716, whichever is being used or tested.

For look-ahead 1706 buffer channels, A = WE01 where the W field is bits 15-10 and identifies the 1706 equipment address. The allowable values for the 6 bit W field are:

000100 - for 1706 number 1
001110 - for 1706 number 2
011000 - for 1706 number 3
000101 - for 1706 number 4
001111 - for 1706 number 5
011001 - for 1706 number 6

The E field is bits 9-7, and identifies the 1731 Magnetic Tape Controller. Note the tape controller may be only equipment 0-7, as bit 10 is now used to specify the upper or lower three 1706's.

b. Stop 3

A = The End of Operation interrupt line for the 17X6. Only one bit is set in this word. The bit position must identify the interrupt line. For example, if the End of Operation interrupts from the 17X6 are to be received on line 5, only bit 5 of this word would be set. Q register contents are described below:

Bit 15 = 1: A 1716 is connected to this computer.

Bit 15 = 0: A 1706 is connected to this computer.

Bit 14 = 1: This computer will initiate the first output if section 6 is selected to be run.

Bit 14 = 0: The other computer will initiate the first data transfer if section 6 is selected to be run.

Bit 13 = 1: A 1706 with look-ahead memory features is connected to this computer.

Bit 13 = 0: The 1706 or 1716 connected to this computer does not contain look-ahead features.

Bit 6 = 1: Run test section 7. This section tests the look-ahead features of the 1706 channel.

Bit 5 = 1: Run test section 6. This section will use the 1716 to transfer data between two computers which are necessary to run this section. A common 1716 must be connected to both the computers. Bit 14 of this parameter must be set in one of the computers. Bit 14 of the other computer must be equal to zero. The decision to repeat section 6 must be made in the computer which has bit 14 = 0.

Bit 4 = 1: Run test section 5. This section will use the 1716 to make block transfers of data within a computer's core storage.

Bit 3 = 1: Run test section 4. This section uses the 17X6, 1731, and a 601 or 602 to test direct output/input of data.

Bit 2 = 1: Run test section 3. This section uses the 17X6, 1731, and a 601 or 602 to test the current word address of the 17X6.

Bit 1 = 1: Run test section 2. This section will use the 17X6, 1731, and a 601 or 602 to test buffered output/input.

Bit 0 = 1: Run test section 1. This section will check the ability of the 17X6 to accept all legal functions (reject should not be received). If a 1716 is connected, this section will also test the flags, masks, and interrupts when corresponding masks and flags are both set.

2. If bit 0 of the Stop/Jump word is not set, the test will be run using the set of prestored parameters. These parameters assume the following:

   a. 1706 number 1 and equipment number of the 1731 Magnetic Tape Controller is 3.

   b. Tape unit 7 is Ready and write-enabled.

   c. The End of Operation interrupts from the 17X6 will be received on line 4.

   d. Test sections 1, 2, 3, and 4 will be run.

3. Selective Skip and Stop Settings

   a. STOP switch must be set for running SMM17.

   b. SKIP switch, when set, displays the Stop/Jump word in Q.

D. MESSAGES

1. Typeouts or Alarms

   a. Normal Program Typeouts

      1) Test identification at start of test
      1706/1716 DATA CHANNEL TEST (F)
      IA = XXXX

      2) End of test typeout

A	Q	A	Q
0F24	S/J Word	Pass Number	Return Address

b. Error Typeouts

If an error occurs, the following information is typed out:

1) Identification word

2) Stop/Jump word

3) Test section/error number

4) Return address

5) Additional information related to the specific error

A sample error typeout is shown and described below:

A	Q	A	Q	A	Q
0F38	000F	0107	0507	0201	1800

0F38 is the identification word where

F is the test number
3 is the number of stops in this error stop sequence
8 identifies the stop as an error stop (bit 3 set)

000F is the Stop/Jump word

0107 is the section number and error number (Section 1, error number 7)

0507 is the address in the program (list address) where the error occurred.

0201 was the status of the 17X6 prior to the attempt to terminate the buffer (see information under error 7).

2. Error Codes

An error code is displayed in the lower two digits of the A register on the second stop of all error stop sequences. A description of the error codes used and the additional information displayed on each error is described below.

II. DESCRIPTION

A. METHOD

1. Initialization

a. Convert first word address of test to ASCII.

b. Type out the test title.

c. Make parameter stop if bit 1 of Stop/Jump word is set.

d. Set up for control to be given to distributor on return from SMM.

e. Return control to SMM.

2. Distributor

a. Run section 1 if selected.

b. Stop at End of Section if bit 1 of Stop/Jump word is set.

c. Repeat section if bit 5 of Stop/Jump word is set.

d. Run section 2 if selected.

e. Stop at End of Section if bit 1 of Stop/Jump word is set.

f. Go to step d if bit 5 of Stop/Jump word is set.

g. Run section 3 if selected.

h. Stop at End of Section if bit 1 of Stop/Jump word is set.

i. Go to step g if bit 5 of Stop/Jump word is set.

j. Run section 4 if selected.

k. Stop at End of Section if bit 1 of Stop/Jump word is set.

l. Go to j if bit 5 of Stop/Jump word is set.

m. Run section 5 is selected.

n. Stop at End of Section if bit 1 of Stop/Jump word is set.

o. Go to step m if bit 5 of Stop/Jump word is set.

p. Run section 6 if selected.

q. Add 1 to pass counter.

r. Stop at End of Test if bit 2 of Stop/Jump word is set.

s. Go to step b if bit 6 of Stop/Jump is set (repeat test).

t. Check if new parameters are to be entered (bit 10 of Stop/Jump word set).

u. Load bias and exit to SMM.

v. Go to step a if SMM returns control (test frequency was greater than 1).

3. Section 1

a. Purpose: Check the static conditions of a 17X6. Checks for No Rejects on all legal functions which will not initiate data transfer.

b. Procedure:

1) Check for Ready set on 17X6.

2) Check for No Reject Received on input of current address.

3) Check for No Reject Received on Terminate Buffer.

4) Check for reserve clear if 1716.

5) Check for No Reject Received on Select and Clear interrupt functions.

6) If 1706 return to distributor.

7) Clear all masks and flags.

8) Test for interrupts after setting each mask and then the corresponding flag.

9) Return to distributor.

4. Section 2

a. Purpose: to test the data transfer capabilities of the 17X6. Interrupt on End of Operation is also tested.

b. Procedure:

1) Set reserve bit if 1716.

2) Check for selected tape unit write-enabled and non-protected.

3) Rewind.

4) Select 200 BPI.

5) If this is an Odd record of the current data pattern, select binary; if Even, select BCD.

6) Select interrupt from 17X6 on end of operation.

7) Initiate buffer output.

8) Check for Busy set in 17X6 status.

9) Check for device Reject set.

10) Determine whether we are on a look-ahead 1706 which has no "stacked" request. If not, check for a Reject on output to 17X6 while the 17X6 is Busy. If we are on the look-ahead 1706 (without "stacked" requests) check for No Reject on output to 1706 while it is busy.

11) Check for device Reply set in 17X6 status.

12) Return control to SMM.

13) Check for End of Operation bit set after Busy clears.

14) Check if interrupt occurred on End of Operation.

15) Check if Interrupt and End of Operation bits were set in 17X6 status when interrupt occurred.

16) Check tape status.

17) If 20 records of current data pattern have not been written, go to 5).

18) If all data patterns have not been used, change patterns and go to 5).

19) Rewind.

20) If Odd record, select binary; if Even, select BCD.

21) Select Interrupt on End of Operation from 17X6.

22) Initiate buffer input.

23) Check for Busy set on 17X6.

24) Check for device Reject set in 17X6 status.

25) Determine whether we expect a Reject or not on output to 17X6 while Busy. If expected, check for its presence, if not expected, check for its absence. (See item 10 above)

26) Check for device Reply set in 17X6 status.

27) Return control to SMM.

28) Check for End of Operation bit set when Busy clears.

29) Check if Interrupt on End of Operation occurred.

30) Check if Interrupt and End of Operation bits were set in 17X6 status when interrupt occurred.

31) Check tape status.

32) Check data.

33) If 20 records of current data pattern have not been read, go to 20).

34) If all data patterns have not been read, change patterns and go to 20).

35) Rewind.

36) Clear reserve if 1716.

37) Return to distributor.

5. Section 3

a. Purpose: Check the ability of the 17X6 to increment the current address correctly.

b. Procedure

1) Set reserve if 1716.

2) Rewind and select 200 BPI.

3) Initiate buffer output with FWA = 0007.

4) Input current address of 17X6 and check for 0008.

5) Input current address and check for equal or one greater than the previous one input.

6) If End of Operation is not set go to 5).

7) Clear reserve if 1716.

8) Return to distributor.

6. Section 4

a. Purpose: Check the direct I/O of data to a 601 or 602 via the 17X6.

b. Procedure:

1) Set Reserve bit if 1716.

2) Rewind and select 200 BPI.

3) If Odd record of current data pattern, select binary; if Even, select BCD.

4) Do direct output of 500 words.

5) Check for alarm up on tape unit.

6) If 20 records of current data pattern have not been written go to 3).

7) If all data patterns have not been used, change patterns and go to 3).

8) Rewind.

9) Initialize data pattern and record count.

10) If Odd record, select binary; if Even, select BCD.

11) Do direct input of 500 words.

12) Check for alarm up on tape unit.

13) Check the data.

14) If twenty records of current pattern have not been read, go to 10).

15) If all data patterns have not been used, change patterns and go to 10).

16) Rewind.

17) Return to distributor.

7. Section 5

a. Purpose: Check the ability of a 1716 to transfer a block of data from an area of storage to a different area within the same computer.

b. Procedure

1) Set reserve on 1716.

2) Set up output area.

3) Select Interrupt on End of Operation.

4) Initiate buffered transfer and exit to SMM until complete.

5) Check if interrupt occurred.

6) Check data.

7) Go back to 3) if the current data pattern has not been buffered 100 times.

8) Change data patterns and go back to 2) if all patterns have not been used.

9) Clear reserve.

10) Return to distributor.

8. Section 6

a. Purpose: Check the ability of a 1716 to transfer data between two 1704 computers.

b. Procedure: In the following sequence of steps, Computer A is initially defined as the computer in which bit 14 of Q equals 1 on the third parameter stop. The other computer is B. TMESS is an absolute location in "this" computer (location 0052). OMESS is the same absolute location in the "other" computer.

1) If computer B, go to 22).

Computer A

2) Set reserve on 1716.

3) Wait for B to set OMESS to its FWA of data area.

4) Initiate buffered transfer to B.

5) Set flags equal to the lower 5 bits of code which identify the data pattern.

6) Transfer data to OMESS.

7) Wait for OMESS to change values.

8) If negative, B found at least one data error.

9) Initiate buffered transfer from B to A.

10) Check data.

11) Go to 4) if current pattern has not been transferred 100 times.

12) Go to 14) if all data patterns have been transferred.

13) Change data patterns and go to 4).

14) If this computer was initially B, go to 18).

15) Clear reserve on 1716.

16) Store 0 at TMESS, -0 at OMESS.

17) Switch names of computers and go to 22).

18) Stop at End of Section.

19) If section is to be repeated, go to 15).

20) Store 0 at TMESS, 0 at OMESS.

21) Clear reserve and return to distributor.

Computer B

22) Clear reserve on 1716.

23) Set TMESS equal to FWA of buffer area.

24) Wait for TMESS to change values.

25) If TMESS is -0, go to 31).

26) If TMESS is 0, go to 32).

27) Check for flags equal to same configuration as lower 5 bits of TMESS.

28) Check data.

29) If data errors, store the complement of the number of errors at TMESS and go to 24).

30) Go to 32).

31) Store 0 at TMESS, change names, and go to 2).

32) Stop at End of Section.

33) Return to distributor.

9. Section 7

a. Purpose: to check proper operation of the look-ahead features of the new 1706 data channels (Equipment configurator DT106A).

b. Procedure:

1) Enable Int. on End of Operation and initiate one buffer output on the 1706 channel (7F Hex. words)

2) Check for Busy status

3) Initiate another buffer output on the 1706 while the first is still active.

4) Check to be sure the second output does not reject.

5) Execute terminate buffer function.

6) Check occurrence of End of Operation interrupt. Disenable Int. on End of Operation interrupt.

7) Check to see whether the 1706 is still Busy (the second buffer should begin when the terminate buffer function is executed on the first buffer).

8) Wait until Busy drops.

9) Check that End of Operation interrupt did not occur.

10) Return to distributor.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIRED - Approximately 2600_{10} locations.

B. INPUT AND OUTPUT TAPE MOUNTINGS - If Section 2, 3, or 4 is selected to be run, a 601 or 602 Tape Unit must be write-enabled and non-protected.

C. EQUIPMENT CONFIGURATION

1. Section 1 - 1704, 17X6
2. Section 2 - 1704, 17X6, 1731 and 601 or 602.
3. Section 3 - 1704, 17X6, 1731 and 601 or 602.
4. Section 4 - 1704, 17X6, 1731 and 601 or 602.
5. Section 5 - 1704 and 1716.
6. Section 6 - two 1704's and one 1716.
7. Section 7 - 1706 with look-ahead feature, 1704, 1731, and 601 or 602.

QSE 4777

1738/853, 854 DISK PACK TEST

(DP4A28 Test No. 28)

This test is identical to DP1 test No. 8 described in the Reference Manual (SMM17) with the following changes in the above description.

Insert after I. A. 1. f.

g. This test contains a section which tests the QSE 4777 Channel Switch. This section is always run before the other sections and cannot be deselected. The test will not work properly on a configuration which does not include the QSE 4777 Channel Switch.

Insert after I. C. 2. c.

d. Fourth Stop

A = Channel number for QSE 4777 Channel Switch.
Bit 0 = Channel 1. Bit 1 = Channel 2.
Q Bits 7-10 = The switch equipment code.

Insert after II. A. 13.

14. Channel Switch Test

a. Check that an equipment code and a channel number has been given for the switch. (If not the test must be reloaded).

b. Input status of switch and report protect status.

c. Deselect both channels.

d. Input status checking for neither channel selected.

e. Select channel chosen at the parameter stop.

f. Input status checking for only the chosen channel to be selected.

g. A check is also made for reject of function output and status input.

Replace III. A. with

A. STORAGE REQUIREMENTS

About 2660 memory locations are required. If sufficient core is available, 1440 additional locations will be used.

QSE 3694
1706 BUFFERED DATA CHANNEL TEST
WITH NON-TERMINATING BUFFER
(BD5029 Test No. 29)

I. OPERATIONAL PROCEDURE (This test is a modification of test 0A. See test 0A for more information)

A. RESTRICTIONS

Must have 8K.

B. LOADING PROCEDURE

No change.

C. PARAMETERS

(Added - Section 6 (Optional) to test 0A
Set Bit 5 at Section Parameter stop.

D. SELECTIVE SKIP AND STOP SETTINGS

No change.

E. MESSAGES

1. Normal messages.

No change.

2. Error Codes

(Added to test 0A)
Error 2F - Unexpected interrupt (EOP when not expected).
Error 30 - Buffer current address register is not equal to expected first word address.

A = Actual address
Q = Expected

Error 31 - End of Operation interrupt did not occur when expected.
Error 32 - Unexpected current address.

II. DESCRIPTION

(Added to test 0A)

G. Section 6 (S6) - Optional

This section tests the non-terminating buffer.

1. Request interrupt line from SMM.
2. Clear interrupt flag.
3. Select non-terminating mode.
4. Select tape.
5. Rewind tape.
6. Select 200 BPI.
7. Select binary.
8. Re-set current address register from 0 through $1F_{16}$.
9. Test tape unit for write enable.
10. Select End of Operation interrupt and non-terminating mode.
11. Initiate output.
12. Test for interrupt. Error if occurred.
13. Test current address register for First Word address or First Word address + 1.
14. Wait for current address to increment.
15. Update expected address.
16. Is current address register equal to expected? Error if not.
17. Update expected address.
18. Is this the turn around point? Yes. Go to 22.
19. Wait for current address to increment.
20. Is current address register equal to expected? Error if not.
21. Go to 17.
22. Wait for current address to increment.
23. Is current address register equal to first word address? Error if not.
24. Have all lengths from 1F to 1FFF been tested? No Set now length, go to 12.)
25. Terminate output.

26. Select End of Operation.
27. Write two words.
28. Did interrupt occur? Error if not.
29. Clear interrupt function.
30. Terminate buffer.
31. Initiate 10-word Write at new first word address.
32. Get current address.
33. Is current address equal to new first word address? Error if not.
34. Terminate buffer.
35. Rewind tape.
36. Clear non-terminating mode.
37. Clear interrupt request from SMM.
38. Release control of BDC.
39. Exit test.

DC215 DATA TRANSFER BUFFER/405 CARD READER TEST
(CR4A2F Test No. 2F)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

This test requires a 1700 computer having 8K (or more) core.

B. LOADING PROCEDURE

The test operates as a subprogram under control of the 1700 System Maintenance Monitor (SMM17). The calling sequence is that specified by SMM17. This test is number 2F (hexadecimal) on the SMM17 tape.

C. PARAMETER STOPS

At the beginning of the test, the parameter stop below will occur if stop 1 (bit 0) of the stop jump parameter has been selected. The parameter stop is a three-stop set:

First Stop:
A = ID word
Q = Stop jump parameter

Second Stop:
A = Select special conditions

Bit 0 — Cycle section if selected. This will cycle the section of the test selected.

Bit 1-10 — Select the sections or section desired to be tested. Any combination of sections may be selected except under the Cycle condition. When the Cycle condition is selected, only one section may be selected.

Bit 1 - A	Bit 6 - F
Bit 2 - B	Bit 7 - G
Bit 3 - C	Bit 8 - H
Bit 4 - D	Bit 9 - I
Bit 5 - E	Bit 10 - J

Bit 12 Cycle specific card. The card number is selected in the Q register at this stop. To cycle a card the test must start at the beginning of the section in which the card to be cycled is contained. The additional cards to be cycled must be added after the card in the section to be cycled. The rest of the cards in the section are to remain off.

Bit 13 If Bit 13 is set, then section F will be gated by the 405 card reader.

Q = Card number of card desired to repeat. Any card may be repeated except the first card in each section. Any number of random binary cards may be added to section J. Section J is the only section that does not require an exact number of cards. It needs only two end-of-file cards at the end and the J card at the beginning of the deck.

D. TEST DECK

The test deck used in checking the DC215 DTB/405 Card Reader is to be structured as described in the following:

1. Standard Test Deck

Each section of the 415/430 Card Punch test punches an independent deck as far as the 405/430 Card Reader test is concerned. Each section starts with a title card followed by the specific cards of the section ending with two end-of-file cards. The title card has one BCD character punched in column one with the rest of the card blank. The specific letter punched on the title card can be found in the 405/415/430 Card Test Deck. (Description in Figure 1.) The end-of-file cards have 7-8 punched in column one, and the rest of the card is blank.

a. Section A. Generate Prepunch Compare Error Deck

These cards are used to check the compare error circuitry. The deck is arranged such that the first card is a title card, and the last two are file cards. The arrangement of the holes in the cards was arbitrary and was decided upon for reasons of ease in programming and physical card strength of the card with 1000 octal holes punched.

b. Section B. Sequence Cards

The objective of the sequenced card section was to provide an ordered deck of cards to make sure the card reader wasn't slipping a card by or shuffling any cards.

c. Section C. Binary Cards

All the pattern cards in the binary section have 7-9 punched in column one. This deck is used by the reader to ensure that the 7-9 punch will cause the card to be read in binary. The 5-124 (pattern 33) card is used by the punch to ensure that each column is punching in its proper location; that is, that two columns aren't swapped. The 52 and 25 (patterns 34 and 35) cards are used as a card reader memory test. The reader setup (pattern 36) card is a card that may be used for card reader setup.

d. Section D. Single Punch Cards

Patterns in this section check skew on a column punch and on the reader mechanism. The purpose of the single punch cards is to check skew on the card reader and to ensure that the reader can keep track of column position with no holes to orient on.

e. Section E. Punch Pattern Cards

The purpose of the punch patterns is to check the mechanical ability of the punch to punch cards. The punch checker cards (patterns 51 to 55) are designed to test for flux interference between adjacent solenoids. The punch progressive cards (patterns 56 to 62) are designed to test the ability of the punch to latch up after punching successive rows in a column. The Reader Slip cards (pattern 63 to 64) are designed to check card reader slippage. The punch rotate

cards (patterns 65 to 71) are worst mechanical punch patterns. The punch frequency card (pattern 72) is designed to check the punch's ability to do high frequency punching.

f. Section F. Hollerith Cards

The Hollerith Card (pattern 73) is designed to check the conversion of all legal BCD codes. The Random BCD card (pattern 74) was added to detect BCD problems missed by the standard Hollerith card.

g. Section G. Punch Memory Cards

The Punch Memory Cards (patterns 75 to 106) are designed to test the punch memory. They place ones surrounded by zeros and zeros surrounded by ones in memory and rotate these patterns through core as well as complementing core.

h. Section H. Full and Part Laced Cards

The Full Laced Card (pattern 107) checks whether the punch can punch all holes in a card and not jam and whether the card reader can read a physically weak card without jamming. The Part Laced Cards (pattern 110 to 121) are designed to check whether the card punch can feed a card that is heavy on one side without skewing it.

i. Section I. Half Random Cards

The Half Card (pattern 122) was designed as a card reader memory test. It also tests the ability of the reader to orient on a random starting column. The one and a half card (pattern 123) was also designed to test the card reader memory as well as check the ability of the equipments to read and punch more than one card at a time.

j. Section J. Random Cards

The Random Card (pattern 124) is designed to detect problems not found by the planned patterns. See paragraph 2 for description of the Random Pattern Generators.

2. Random Pattern Generators

a. Random BCD Pattern Generator (Pattern 74)

The random BCD generator forms a patterned random buffer by adding one of eight 12-bit constants to one 12-bit entry to form the next. The same constant is used in each add on any one pattern. The starting 12-bit value is the real time clock, if available, for the first card. The starting value of the remaining cards is last column generated plus the real time clock. The lowest order digit on the first 12-bit value is used to determine which of the eight constants to use. The eight constants which are added to one 12-bit value to form the next are as follows in octal:

4321 for column 1 =	XXX0
6543	XXX1
7654	XXX2
3210	XXX3
4132	XXX4
1423	XXX5
7465	XXX6
3021	XXX7

b. Half Card Random Generator (Pattern 122)

The one and a half card random generator (3.3.2) is used to generate the half card pattern. After the buffer has been prepared for a one and a half card, the mirror image is taken off the buffer by swapping column 1 with column 80, column 2 with column 79, and so on down to swapping column 40 with 41.

c. Random Binary Card Generator (Pattern 124)

The objective of this generator is to produce a card with both random hole placement as well as random hole density and to have the card predictable hole for hole by the card reader test. The objective was obtained by generating a reproducable random pattern, biasing its density by combinations of 9, 1 or 2 selective sets and/or clears, and finally placing a key value two places on the card to allow two chances of regenerating the card when read. These three steps in detail are as follows:

Generating Random Hole Placement

This is the basic random number generator used.

a. Starting Value

The starting value is last random number generated plus the real time clock. The first time through the generator the starting value is an arbitrary constant (2525) plus the real time clock.

b. Buffer Size

The buffer is 86 columns or 86 12-bit bytes in length. The card image starts with the 2nd byte and ends with the 81st byte. The first byte is the starting value, and bytes 82 to 86 are used to bias the hole density.

c. Generator

The generator uses this formula to generate the next random column.

$2(13A + B) = C$

Where A is the last generated 12-bit byte

B is one of 2 constants (7135B and 1703B)

C is the newly generated 12-bit byte

The quantity

$(13A + B)$

within the formula is generated with all carries to the 13th bit cleared.

The constant B of 7135 octal is used to generate odd number columns on the card, that is, if it is the first constant used.

The constant B of 1703 octal is used to generate even number columns on the card. The constants are, therefore, alternately used, starting with 7135 octal.

The multiply of (13A + B) by 2 is performed by doing an end around lift shift of 1. That is, this multiply by 2 has an end around carry.

3. Generating Random Hole Density (RNDMB)

A random number generator will by nature produce a set of binary numbers in which about half of the bits are set and half are clear.

This leads to a card on which about half the holes are punched. To bias the number of bits set or clear, the idea of selectively setting and selectively clearing random numbers together was used. For example: If two numbers with 1/2 the bits set are selectively set together, the result will be a number which has on the average 3/4 of the bits set. If this number is then selectively cleared by a third 1/2 set number, the result will be a number which has an average of 3/8 of the bits set.

This approach is used to bias the average densities about seven values rather than the unbiased 1/2 set numbers.

The lower three bits of the starting value, that was used to generate the raw random pattern, is used to determine which density to produce. The following table shows the relationship between the starting number, the density in the fraction of the holes set, and the operation performed to obtain the bias.

Density	Starting Number	Operation
1/8	XXX0	Selectively clear the current column with three columns beyond the current column and selectively clear the result with the column 5 beyond the current column.
1/4	XXX1	Selectively clear the current column with the column 5 beyond the current column.
3/8	XXX2	Selectively set the current column with the column 3 beyond the current column and selectively clear the result with the column 5 beyond the current column.
1/2	XXX3	Not biased.
1/2	XXX4	Not biased.
5/8	XXX5	Selectively clear the current column with the column 3 beyond the current column

Density	Starting Number	Operation
		and selectively set the result with the column 5 beyond the current column.
3/4	XXX6	Selectively set the current column with the column 5 beyond the current column.
7/8	XXX7	Selectively set the current column with the column 3 beyond the current column and selectively set the result with the column 5 beyond the current column.

4. Starting Value Placement

The unbiased 12-bit starting value used to generate the raw random buffer is placed on the card image twice after the density of the buffer has been biased. The starting value is placed on the lower half of the card from row 4 through row 9 and in columns 10, 12, 30, and 22 as follows:

Starting Value

a. Bits 5 to 0 in row 4 to 9 of column 12
   Bits 11 to 6 in row 4 to 9 of column 10

b. Bits 4 to 0 in row 4 to 8 of column 22
   Bits 10 to 5 in row 4 to 9 of column 20
   Bit 11 in row 9 of column 22

Example: Given a starting value of 1234

Column 10 = XX12
Column 12 = XX34
Column 20 = XX24
Column 22 = XX70

E. MESSAGES

1. Normal

a. Title typeout

Typeout message: CR4A2F DTB/405 CARD READER TEST
IA = XXXX

There is no corresponding stop.

b. End typeout

Typeout message: END DTB/405 TEST

2. Error

Format: There are two types of error stops in the following formats. They will occur if stop 8 (bit 3) is set in the jump stop parameter.

Type I

Stop 1 (A) = ID word
(Q) = Stop jump parameter

Stop 2 (A) = Error code
(Q) = Card number of error

Stop 3 (A) = Column number of error
(Q) = Code expected

Stop 4 (A) = Actual code
(Q) = ID word

Type II

Stop 1 (A) = ID word
(Q) = Stop jump parameter

Stop 2 (A) = Error code
(Q) = Return address

In each error stop type, stop 1, (A, Q) and stop 2, (a) are the same for every error stop type. "A" of stop 2 is always the error code.

Error Code:

00 Type I stop - This is a card error stop. If the data input does not equal the data expected, this stop will occur.

01 Type II stop - An unexpected 405 card reader status of Hollerith to BCD conversion has been received.

02 Type II stop - A 405 card reader End-of-File status has been received.

03 Type II stop - A 405 card reader read comparison status has been received.

04 Type II stop - A 405 card reader manual on motor power off status has been received.

05 Type II stop - A 405 card reader pre-read error status has been received.

06 Type II stop - A 405 card reader late input status has been received.

07 Type II stop - A 405 card reader feed failure status has been received.

08 Type II stop - A 405 card reader stacker full or jammed status has been received.

09 Type II stop - A 405 card reader input tray empty has been received. After the type II stop, a parameter stop is made as described in section I. C. The test then continues after the input tray is reloaded.

0A Spare

0B Type I stop - Program expected section A

0C Type I stop - Program expected section B

0D Type I stop - Program expected section C

0E Type I stop - Program expected section D

0F Type I stop - Program expected section E

10 Type I stop - Program expected section F

11 Type I stop - Program expected section G

12 Type I stop - Program expected section H

13 Type I stop - Program expected section I

14 Type I stop - Program expected section J

15 Type II stop - Data transfer buffer failed to input data from the 405 card reader.

16 Type II stop - The 405 interrupt did not occur in the given time limit, 47.3 usec.

17 Type II stop - The program cannot connect to the data transfer buffer.

18 Type II stop - The program cannot connect to the 405 card reader.

19 Type II stop - An external reject was received.

1A Type I stop - A random starting column error was received in test section I.

1B Type I stop - A random ending column error was received in test section I.

1C Type I stop - Data in columns 10 and 12 does not compare with data in columns 20 and 22 of the random card. At stop 3, Q will equal the code developed from columns 20 and 22. "A" in stop 4 will equal the code developed from columns 10 and 12.

1D Type II stop - A data transfer buffer disconnect interrupt was expected but not received.

1E Type II stop - Program not able to input DTB status.

1F Type II stop - The DTB can not input 405 status. An input disconnect has been generated by the DTB.

II. DESCRIPTION

This test checks the proper operation of the 405 card reader attached to the DC215 data transfer buffer using the AQ channel of the 1704 computer. See section I. D. for a description of the test deck. The test is divided into seven operating sections which may be selected at parameter entry time. Repeat conditions, sections test, etc. are chosen as described in section I. C. Operations of the test sections are briefly described below along with a description of the initialization procedure. Each section of the card deck to be tested must begin with a letter card A-J and end with two end-of-file cards (7-8 punch).

INITIALIZATION SECTION

A. Checks the proper connection of the DTB and the 405 to the computer.

B. Status the 405 card reader for proper status at beginning of the test.

Section A

The cards are read in binary and are meant to check the compare error circuitry of the 405. Each card is checked against an internal stored expected pattern.

Section B

The cards are read in binary and their objective is to provide an ordered deck of cards to make sure the card reader is not slipping or shuffling any cards. Each card is checked against an internal stored expected pattern.

Section C

The cards are read using the BCD function. This section is used to ensure that the 7-9 punch will cause the card to be read in binary even while in the BCD mode. Also the 52 and 25 patterned cards are used in this section as a card reader memory test. Each card in this section is checked against an internal stored expected pattern.

Section D

The cards are read in binary. The objective of this section is to check skew on the card reader and to ensure the reader can keep track of column position with no holes to orient on. The cards are all checked against internally stored expected pattern.

Section E

The cards are read in binary. The cards in this section are used mainly as a punch test, but also several patterns are used to check card reader slippage. These cards are checked against an internal expected pattern.

Section F

The cards in this section are read in BCD. They first check all legal BCD codes. The random cards are to detect other problems missed by the standard Hollerith cards. In this test the random cards are read in and not checked because their origination could not be determined.

Section G and H

The cards are read in binary. They are designed to test the card punch. Section H tests the card reader's ability to read physically weak cards without jamming. These cards are checked against internally stored expected patterns.

Section I

These cards are read in binary. The cards in this section where designed as a card reader memory test. They also test the ability of the reader to orient on a random starting column. Cards in this section are checked against internally stored patterns expected.

Section J

These cards are read in binary. They are random cards designed to detect problems not found by the planned patterns. Random data is generated from the contents of the lower half of columns 10, 12, 20, and 22 of the card. Note the random cards have random densities, ranging from approximately 1/8 of the holes punched on the card to 7/8 of the holes punched. The patterns are checked against computer generated patterns.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS - approximately 2500_{10} locations.

B. TIMING - variable depending upon the size of the test deck.

C. EQUIPMENT CONFIGURATION

1. 1704 Computer with 8K memory.
2. 1705 Interrupt Data Channel.
3. DC215 Data Transfer Buffer/405 Card Reader.

Section Title Card Letter	Pattern Number	Pattern Name	Number Punched	Description	
A					
	1	COMPARE ERR	1	2 holes punched	BCD A in column 1 (act as title card)
	2		1	1 holes punched	Holes start in row 9 and fill
	3		1	20B holes punched	successive even columns
	4		1	40B holes punched	starting in column 2 until the
	5		1	100B holes punched	prescribed number of holes
	6		1	200B holes punched	are punched - 1000B hole card
	7		1	400B holes punched	then uses row 7 of successive
	10		1	1000B holes punched	odd columns to punch the last 32 holes.
	11		1	4 holes punched	7/8 column 1, 4/5 column 2 (act as file card)
	12		1	10B holes punched	7/8 column 1, 4/5/6/7/8/9 column 2 (act as file card)
B					
	13	SEQUENCE	1	Binary 10 in column 1	
	14		1	11	
	15		1	12	
	16		1	13	
	17		1	Binary 14 in column 1	
	20		1	15	
	21		1	16	
	22		1	17	

Figure 1. 405/415/430 Card Test Deck Description

Section Title Card Letter	Pattern Number	Pattern Name	Number Punched	Description
	23		1	20
	24		1	21
	25		1	22
	26		1	23
	27		1	24
	30		1	25
	31		1	26
	32		1	27
		EOF	2	
C				
	33	5-124	3	Sequenced columns from 5 in column 1 to 124 in column 80
	34	52 W/709	3	Alternate columns of 5252 and 2525 with 7/9 column 1
	35	25	3	Alternate columns of 2525 and 5252
	36	READER SETUP	3	Alternate 12 columns of 2525 and 12 columns of 5252
		BLANK CARD	1	
		EOF	2	
D				
	37	READER CHECK	3	Row Sequence 12 to 9 and Repeat
	40	READER CHECK	3	Row Sequence 9 to 12 and Repeat
	41	SKEW CHECK	3	Heavy punching on upper portion of card
	42	SKEW CHECK	3	Heavy punching on lower portion of card
	43	SINGLE PUNCH	3	12 punch in column 1
	44		3	9 punch in column 1
	45		3	12 punch in column 80

Section Title Card Letter	Pattern Number	Pattern Name	Number Punched	Description
	46		3	9 punch in column 80
	47		3	12/9 column 1
	50		3	12/9 column 80
		EOF	2	
E				
	51	PUNCH CHECKER	1	Alternate 4 columns of 2525 and 4 columns of 5252
	52		1	1463 6314
	53		1	0707 7070
	54		1	7417 0360
	55		1	6037 1740
	56	PUNCH PROGRESS	1	Each column is 2525
	57		1	3333
	60		1	3567
	61		1	6757
	62		1	3737
	63	SLIP	1	Each column is 4034
	64		1	1601
	65	PUNCH ROTATE	1	Alternate 4 column sets of 6334, 5322, 3555, 5276, 2450
	66		1	5322, 3555, 5276, 2450, 6334
	67		1	3555, 5276, 2450, 6334, 5322
	70		1	Alternate 4 column sets of 5276, 2450, 6334, 5322, 3555
	71		1	2450, 6334, 5322, 3555, 5276
	72	PUNCH FREQUENCY	10	Alternate 4 column sets of 3777, 7767, 7577
		EOF	2	

Figure 1. 405/415/430 Card Test Deck Description (Cont'd)

Section Title Card Letter	Pattern Number	Pattern Name	Number Punched	Description
F				
	73	HOLLERITH	3	BCD codes 00 to 77 in column 1 to 64
	74	BCD RANDOM	15	Patterned Random BCD
		BLANK CARD	1	
		EOF	2	
G				
	75	MEMORY	2	Eight columns 1030 Eight columns 4102
	76		2	0604 2041
	77		2	4102 1030
	100		2	2041 0604
	101		1	5132 2645
	102		1	2645 5132
	103		2	6747 3675
	104		2	7173 5736
	105		2	3675 6747
	106		2	5736 7173
		EOF	2	
H				
	107	FULL LACE	3	All holes punched
	110	PAER LACE	1	Columns 1-2 laced rest blank
	111		1	1-4
	112		1	1-8
	113		1	1-16
	114		1	Columns 1-32 laced rest blank plus 12 column 80

Figure 1. 405/415/430 Card Test Deck Description (Cont'd)

Section Title Card Letter	Pattern Number	Pattern Name	Number Punched	Description
	115		1	Columns 79-80 laced rest blank
	116		1	77-80
	117		1	73-80
	120		1	65-80
	121		1	Columns 49-80 laced rest blank plus 12 column 1
		EOF	2	
I				
	122	HALF CARD	10	Patterned Random past column 40
	123	ONE AND HALF CARD	10	Patterned Random before column 41 - two card write
		EOF	2	
J				
	124	RANDOM	100	Random hold count, Random hole placement
		EOF	2	

Figure 1. 405/415/430 Card Test Deck Description (Cont'd)

FAST FOURIER TRANSFORM ALGORITHM TEST

(FFTA41 Test No. 41)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. This test requires 16K of core to run.
2. The test is loaded under normal SMM17 procedures, but once the test receives control to run, it does not release control to SMM until the test is completed.

B. LOADING PROCEDURE

The test loads and runs under SMM17. The test mnemonic is FFT and test number is 41. A detailed loading procedure is available in SMM17 manual, and is also given at the front of the program listing.

C. PARAMETERS

1. Normal SMM Entry Parameters

   Upon requesting test number 41 under normal SMM17 procedures, no request to enter parameters need be made if the following four conditions are met:

   a. The FFT module is connected to the 1706 BDC channel fixed in the listing.

   b. The FFT equipment switch is to setting fixed in the listing.

   c. The FFT equipment uses interrupt line fixed in the listing.

   d. All standard sections are to run.

   If any one of the previous conditions is not met, the SMM parameter bit to enter parameters must have been set.

2. Change Or Re-enter Parameters

   To alter or re-enter parameters required four AQ stops.
   The four stops are listed in order:

   a. Stop 1
      A = Identification Word
      Q = Stop/Jump Parameter

b. Stop 2

A = Memory sections to run section 0 = bit 0

Q = Interrupt and algorithm sections to run
Section 10 = bit 0
Section 14 = bit 4

c. Stop 3

A = FFT status command (should be same as original entry unless equipment or channel changed after test was loaded).

Q = Alarm Interrupt Line

d. Stop 4

A = Alarm Interrupt Line

Q = Unused

3. Special Parameters

a. Bit 12 in the stop/jump word is used for isolation either after a weighting operation error or a transform error.

Bit 12 is also used in the memory test to Read and Write to the last errored address in the FFT memories. A one-word Read and Write is thus accomplished on the location in question. Those sections of FFT 41 diagnostic capable of using isolation are sections 1, 2, 3, 4, 5, and 6 of the memory verification and sections 12, 13, 16, 17, 18, 19, 1A, 1B, and 1C.

b. Restart program at initial biased address.

D. MESSAGES

1. Normal Messages

a. Test identification with starting address indicated.

b. Any messages from monitor not dealing with test.

c. End of test message.

d. Four AQ stops and typeouts at end of test. SMM17 explains these end of test AQ typeouts and stops.

2. Error Messages

a. Error Typeouts

Error typeouts are in standard SMM17 format with the first two AQ typeouts always indicating the same information.

The first two stops will be identified as follows for all error codes:

STOP 1

A = 41X8 Iden word (X = number of stops)
Q = XXXX Stop/Jump parameter listed by bit identification in the SMM17 manual.

STOP 2

A = XXYY Section $XX and Error Code $YY
Q = XXXX Return Address

Starting with error stop 3, a varying number of error stops will be listed after each individual error code.

In addition to the initial typeout of all the stops, the actual individual stops also occur.

b. Error Codes (Also shown in program listing)

* ERROR CODE 00 (3 Stops)

Unacceptable Equipment status I/O parameter.
Converter code should be a 02, 07, or 0C, which identifies 1706 number 1, 2, or 3.

STOP 3

A = Converter code that was entered
Q = Unused

* ERROR CODE 01 (3 Stops)

FFT status is incorrect while checking Ready/Busy status.

STOP 3

A = Actual FFT status
Q = Expected FFT status

* ERROR CODE 02 (3 Stops)

FFT status shows constant busy for 4 seconds.

STOP 3

A = Actual 1706 BDC status

Q = Actual FFT status

* ERROR CODE 03 (3 Stops)

1706 BDC status shows constant busy for 4 seconds.

STOP 3

A = Actual 1706 BDC status

Q = Unused

* ERROR CODE 04 (3 Stops)

Internal reject on I/O instruction

STOP 3

A = Contents of A during rejected I/O

Q = Command code during rejected I/O

* ERROR CODE 05 (3 Stops)

External reject on I/O instruction

STOP 3

A = Contents of A during rejected I/O

Q = Command code during rejected I/O

* ERROR CODE 06 (3 Stops)

Unexpected interrupt received and FFT status indicates no EOP or Alarm status.

STOP 3

A = FFT status at interrupt

Q = Unused

* ERROR CODE 07 (4 Stops)

Function clear does not terminate FFT operation listed in stop 4.

STOP 3

A = Actual FFT status after clear function

Q = Expected FFT status to show Ready bit

STOP 4

A = Command code of FFT function performed before function Clear was initiated.

Q = Unused

* ERROR CODE 08 (5 Stops)

Data compare error in operand Transfer mode. The contents of buffer area (field) are compared against the contents of the FFT operand memory. A sequential One For One Compare was being made at the time of the data Mismatch.

STOP 3

A = Actual real part (1st 16-bit operand)

Q = Expected

STOP 4

A = Actual imaginary part (2nd 16-bit operand)

Q = Expected

STOP 5

A = Present field length

Q = FFT address of data error

* ERROR CODE 09 (3 Stops)

FFT rescale Count status does not compare with the simulated count.

STOP 3

A = Actual FFT status (resc CNT bits 12-15)

Q = Expected value bits 12 through 15

* ERROR CODE 0A (4 Stops)

Data compare error on Algorithm mode read input

STOP 3

A = Actual magnitude value

Q = Expected magnitude value

STOP 4

A = Present field length setting
Q = Answer number that errored

STOP 5

A = Real part of complex answer involved
Q = Imaginary part of complex answer involved

* ERROR CODE 0B (2 Stops)

On attempting isolation after a transform compare error (doing one level transforms). No compare error occurred through the entire transform.

* ERROR CODE 0C (3 Stops)

Did not receive expected alarm interrupt after overflow occurred during simulation. A 2-second time out allowed for interrupt.

STOP 3

A = FFT status after time out
Q = Level indication if error occurred during a transform, check return address.

* ERROR CODE 0D (3 Stops)

Did not receive End of Operation interrupt after functioning the FFT module.

STOP 3

A = FFT status after time out
Q = Unused

* ERROR CODE 0E (3 Stops)

Received unexpected alarm interrupt

STOP 3

A = FFT status at interrupt
Q = Unused

* ERROR CODE 0F (3 Stops)

Received unexpected End of Operation interrupt

STOP 3

A = FFT status at interrupt
Q = Unused

* ERROR CODE 10 (4 or 5 Stops)

Data compare in memory test. If the compare error occurs while testing the 32-bit memories, a 5th stop is needed to show expected and actual data for the additional 16 bits.

STOP 3

A = FFT memory address where compare error occurred.
Q = Command code to show what memory is being tested.

STOP 4

A = Actual data from FFT memory
Q = Expected data

STOP 5 (Only when checking 32-bit memories)

A = Actual data from FFT memory (2nd 16-bits)
Q = Expected data

* ERROR CODE 11 (3 Stops)

Priority access failure while transferring data to/from the FFT module. This possible error condition is continually checked in the memory test as all transfers in excess of 32 bits will have the priority bit set.

STOP 3

A = Present FFT status
Q = Command code to show memory being tested

* ERROR CODE 12 (5 Stops)

Indicates a data compare error in memory test after completing an ordered output and a normal input from the weight memory.

STOP 3

A = FFT memory address where compare error occurred
Q = Command code at time of error

STOP 4

A = Actual data from FFT memory
Q = Expected data

STOP 5

A = Actual data from FFT memory (2nd 16 bits)

Q = Expected data

* ERROR CODE 13 (5 Stops)

Indicates a data compare error in memory test after completing a transfer to the operand memory and an ordered input from that memory. All stops have the same meaning as error code 12.

* ERROR CODE 14 (5 Stops)

Indicates a data compare error in memory test after completing an ordered output, a weight memory input, an operand memory output, and an ordered input.

All stops have the same meaning as in error code 12.

* ERROR CODE 15 (3 Stops)

Did not receive alarm interrupt as expected, but did process the interrupt indicated in the FFT status (3rd A stop).

STOP 3

A = FFT status at interrupt

Q = Level indication if error occurred during a transform, check return address.

* ERROR CODE 16 (4 Stops)

Real part of overflow values did not compare. While simulating a weighting operation, overflow occurred. The FFT did give an alarm interrupt, but the overflow data did not compare on the 1st 16 bits (Real part).

STOP 3

A = FFT address where overflow should occur

Q = Present field length setting

STOP 4

A = Actual data from FFT operand memory

Q = Expected data

* ERROR CODE 17 (5 Stops)

Imaginary part of overflow values did not compare. This error is similar to error 16, except the compare error was on the 2nd 16-bit operand (Imaginary part).

STOP 3

A = FFT address where overflow should occur

Q = Present field length setting

STOP 4

A = Actual data (Real) from FFT operand memory

Q = Expected value

STOP 5

A = Actual data (Imag) from FFT operand memory

Q = Expected value

* ERROR CODE 18 (7 Stops)

Data compare error during Weighting operation isolation mode. The two 32-bit operands are loaded at zero addresses in both the weight and operand memories. The field length is set equal to one.

STOP 3

A = Actual value (Real) from FFT operand memory

Q = Expected value

STOP 4

A = Actual value (Imaginary) from FFT operand memory

Q = Expected value

STOP 5

A = Real portion of operand memory before weighting

Q = Imaginary portion of operand memory before weighting

STOP 6

A = Real portion of weight memory before weighting

Q = Imaginary portion of weight memory before weighting

STOP 7

A = Present field length

Q = Previous FFT error address on weight operand

STOP 8

A = AC product least significant bits before scale

Q = AC product most significant bits before scale

STOP 9

A = BD product least significant bits before scale

Q = BD product most significant bits before scale

STOP 10

A = AD product least significant bits before scale

Q = AD product most significant bits before scale

STOP 11

A = BC product least significant bits before scale

Q = BC product most significant bits before scale

* ERROR CODE 19 (6 Stops)

This error gives notification of unacceptable data during a transform. The original data caused overflow while doing a transform. The overflow data from the simulated transform is shown along with the FFT locations where the overflow should have occurred. The FFT data at those predicted locations is also displayed.

A test is made for the alarm interrupt.

STOP 3

A = Actual data (Real) from FFT operand memory.

Q = Expected data (Real)

STOP 4

A = Actual data (Imag) from FFT operand memory

Q = Expected data (Imag)

STOP 5

A = Present field length
Q = Level when error occurred

STOP 6

A = FFT operand address where should overflow
Q = 1700 core address of overflow

* ERROR CODE 1A (4 Stops)

This error can only occur in section 15 and indicates a compare error occurred after filling the phase memory with the sine and cosine values. The error occurred upon rechecking those values.

STOP 3

A = Actual value from FFT phase memory
Q = Expected value

STOP 4

A = FFT phase memory address of data error
Q = Present field length

* ERROR CODE 1B

This error code and stop occurs once after isolation on a previous transform error. The stops involved give information that pertains to error code 1C.
This error will only occur if there is an error detection upon isolating.

STOP 3

A = 1st 16-bit answer expected after SIM FL=2
Q = 2nd 16-bit answer expected after SIM FL=2

STOP 4

A = 3rd 16-bit answer expected after SIM FL=2
Q = 4th 16 bit

STOP 5

A = Original operands 1st 16-bit number A
Q = Original operands 2nd 16-bit number 1B

STOP 6

A = Original operands 3rd 16-bit number C
Q = Original operands 4th 16-bit number 1D

STOP 7

A = Cosine value involved
Q = Sine value involved

STOP 8

A = Level at which 1st error compare occurred.
* This level indication is a decremental
* count. The original starting level will
* be the exponent N in the original field
* length of 2**N. This original count is
* known from the original error $08.
* An example is an error on original FL
* of 4096 or hex of 1000. This number is
* represented by 2**12, so the starting
* level is 12, and decrements to 1 for
* completion. If the level at which the
* error occurred was $A, this is actually
* the third one-level transform.

Q = FFT address of 1st error compare

STOP 9 — Stops 9 through 12 provide cross

A = 1D X SIN — products involved in a trans-
Q = 1D X SIN — form of field length equal 2.

STOP 10

A = C X SIN — To further identify, let the
Q = C X SIN — two-16-bit difference remaining

STOP 11 — after the algorithm subtract

A = C X COS — be identified as C + 1D.
Q = C X COS — the complex MUI is as follows

STOP 12

A = 1S X COS — (C + 1D) (COS X + I SIN X)
Q = 1D X COS

* ERROR CODE 1C

This error code can only occur during an isolation transform of field length = 2.

Error code 1B will be typed out previously if the transform that errored can repeat the error on isolation. Error code 1B will show the original operands and the simulated results.

Error code 1C will show the expected results from the simulation and the actual results received from the FFT after the transform of field length = 2.

STOP 3

A = Actual 1st 16-bit answer FL=2
Q = Expected 1st 16-bit answer FL=2

STOP 4

A = Actual 2nd 16-bit answer FL=2
Q = Expected 2nd 16-bit answer FL=2

STOP 5

A = Actual 3rd 16-bit answer FL=2
Q = Expected 3rd 16-bit answer FL=2

STOP 6

A = Actual 4th 16-bit answer FL=2
Q = Expected 4th 16-bit answer FL=2

II. DESCRIPTION

This test is divided into two main parts. The parts are memory and algorithm verification. The sections of the test are listed in hexidecimal order. Also, an explanation of simulation and isolation is provided.

A. MEMORY VERIFICATION (Sections 0 through 7)

1. Section 0-Assures Ready and Busy status are operational in order to initiate I/O operations during the memory test.
2. Section 1-The zero's and all one test on all FFT memories (phase, operand, and weight memories) are performed in this section.

3. Section 2 performs addressing tests on all FFT memories and checks ordered mode addressing for all field lengths.

4. Section 3 performs the worst pattern and complement worst pattern tests on all FFT memories.

   Performs the optimal worst pattern test on the phase memory. Before each location is checked, a zero word in the pattern (worst or complement worst pattern) is referenced in each inhibit group and then a diagonal of all ones ($FFFF) words are referenced. This is done to raise the noise level in the half referenced cores. After a compare check is made of the location, the complement of its original contents is stored in the location, the noise level is again raised, another compare check is made, and the original contents are restored. This test requires approximately 4 minutes to run, and is, therefore, optional.

5. Section 5 is the optimal worst pattern test on the operand memory. Reference section 4 for remarks.

6. Section 6 is the optimal worst pattern test on the weight memory. Reference section 4 for remarks.

7. Section 7 checks the contents of the weight and phase memories to ensure their capability to retain original contents after being referenced during weighting and transforming operations.

   Weight and phase memory are given worst pattern and operand memory is filled with zeros. The FFT is then functioned to do eleven weighting and transforming operations in succession. The contents of the weight and phase memories are then checked for original contents.

B. ALGORITHM VERIFICATION (Sections 10 through 1C)

1. Section 10 is interrupt checking. This section checks all the functions and conditions that can set or clear the FFT interrupts (end of operation and alarm).

2. Section 11 is the first check of the weighting operation and the multiplier network. The field length is set to 4096, a pattern of $3FFF is sent to weight memory and zeros to operand memory. A weighting function is performed and the operand memory is checked for zeros. The same check is made with the data patterns reversed. The third check is with $3FFF

in all locations of the operand memory and zeros in the weight memory. A weighting operation is performed on varying incremental field lengths from 2 to 4096. The expected pattern will remain in the field area to compare against the operand memory, and this correct comparison assures that the weighting operation terminates correctly.

3. Section 12 accurately simulates the weight operation. The data area used is the normal buffer area labeled "field". This area is 8,192 sixteen-bit locations. The first 4,096 locations will be used to hold the 32-bit operands (2048) that will be the data sent to the operand memory. Starting at field +4096 will be the actual weight memory data. After the weighting simulation the answers will be stored over the operand memory data.

   The original data is stored in the phase memory for repeat conditions and for isolation on a weighting operation.

   All field lengths from 2 to 2048 are checked by simulation. Simulated results are then compared with FFT results.

4. Section 13 checks the weighting operation using random data. The same simulator used in section 12 is used here, but the field length is set to 2048 through the entire section. First the data is checked in operand mode. Next, a completely new operation is completed. Finally, data is compared in Magnitude mode. Each operation is in a loop that is executed for 20 cycles before exiting.

5. Section 14 phase memory referencing check checks phase memory referencing on all field lengths. A one-level straight transform is completed with data in the operand memory that causes the phase memory data to be placed in the operand memory as results. The phase memory data has the contents of each location equal to its address.

   Isolation on transform error is not allowable here as the results are predetermined and not found through simulation. Also, having done only a one-level transform, error identification can be referenced directly.

   This section also performs the previous operation with the phase memory containing the trigonometric tables used in the actual transform.

6. Section 15 transfers the sine and cosine tables to the phase memory and inputs the transferred data for a compare check.

7. Section 16 is one-level transform check. This section assumes the phase memory contains the sine/cosine tables. The operand memory is filled with real and imaginary values equal to 5FFF - 0000 in the 1st half of the field.

   Transforms are functioned to the FFT module and also simulated in 1700 field area. The field length is 4096. Twelve one-level transforms are completed. The following checks are made after each transform:

   a. Check for EOP interrupt

   b. Check correct Rescale status

   c. Compare results in Operand mode AQ input

8. Section 17 checks the FFT module for straight Fourier transforms of a varying incremental field length from 2 to 4096. This consists of twelve different transform lengths.

   The original data in this section has the first half of the field, to be transformed, equal to $2AAA. The second half will be the operand $1555. After functioning and simulation, the following steps are completed.

   a. Check EOP interrupt.

   b. Check correct Rescale status.

   c. Compare results by Algorithm mode read (Magnitude mode).

   d. Check for repeat condition bit set, after compare error stop, to allow repeat of present level transform.

   e. End of section.

9. Section 18 is similar to section 17. The two differences are that inverse transforms are checked into this section and the original data field is reversed, 1st half ($1555), 2nd ($2AAA).

10. Section 19 is Fourier transform on random data (field length is 4096).

    This section performs the following steps:

    a. Sets FFT field length to 4096.

b. Functions FFT to enable interrupts (End of operation and alarm interrupt).

c. Generates 8192 sixteen-bit operands in the Fourier simulation area.

d. Rescales the data to assure no overflow can occur when the initial sum and differences are obtained.

e. Transfers this data to the operand memory.

f. Transfers this data to the weight memory to allow original data to be recalled for repeating the initial conditions.

g. Functions the FFT to do a straight Fourier transform.

h. Simulates the FFT operation (TFL). Rescaling is simulated to check against overflow. If overflow does occur at any time during the simulation, the FFT status is monitored to assure reception of an alarm interrupt or error code $E is given. The data is then identified as unacceptable (error code 19) and a jump is executed to check repeat condition or repeat section.

i. After simulation is complete, the FFT status is monitored to assure reception of EOP.

j. Rescale status is checked (simulated against FFT status result).

k. Compares simulated results against FFT results in magnitude mode. (FFT functioned to do algorithm mode read).

l. On a compare error, provision is made for setting of isolation bit in stop jump parameter (bit 12), which executes a jump to isolate routine.

m. Repeat original condition is also allowed after exit from isolate routine.

11. Section 1A inverse Fourier transform on random data (field length is 4096). This section performs the same checks as section 19 (refer to section 19) except an inverse transform is performed.

12. Section 1B ordered Fourier transform on random data (field length is 4096).

This section performs essentially the same checks as section 19 (refer

to section 19). The difference is in the type of FFT transform and the manner of simulation to check the FFT results.

The simulation is accomplished by doing a forward transform algorithm on random data that is not initially bit reversed. The initial random data in the FFT operand memory is bit reversed. This was accomplished by initially transferring the random data to the weight memory in ordered mode write.

The weight memory bit reversed data is then brought back into the computer and transferred directly to the FFT operand memory.

The original data in the FFT operand memory is then transferred back to the 1700 simulation area (field) in ordered read. This leaves the data in the simulation area not bit reversed, while the data in the FFT operand memory is bit reversed. Results from an FFT ordered transform, unloaded in ordered mode should now equal the results from a simulated straight transform.

All isolation and repeat condition capabilities remain the same as for section 19.

13. Section 1C ordered inverse Fourier transform on random data (field length is 4096).

This section uses the same procedures as section 1B (ref comments 1B).

The only difference is the FFT function checked in this section is the ordered inverse transform. (OFLAG and TFLAG are both set for simulation).

C. WEIGHTING SIMULATION AND ISOLATION

Setting up the data to initiate a weighting operation was explained in the comments on section 12. The maximum field length that can be simulated is 2048. Once the data is set, the actual simulation is accomplished by executing a return jump to mnemonic "WGTNG." The results are stored in place over the original operand data located in field to field +4095 (actual number of operands determined by the field length). If an error on comparing results occurs, setting bit 12 of the stop jump word and passing through stops will cause a jump to mnemonic "ISOWT", which stands for isolation on a weighting operation. The actual error address

is known on entering "ISOWT", and from this the original operand results are brought back in from the phase memory and the original data involved in the error can be obtained.

Both the weight and operand memory data involved in the error, are relocated to zero, simulation and compare at a field length equal to two are accomplished. If a compare occurs here, error code 18 is typed out with the information stated in that error code.

D. TRANSFORM SIMULATION AND ISOLATION

Use of the trigonometric tables located in the program are used for simulation on all transforms. The correct values are also assumed to be stored in the phase memory. The original data must be sent to the operand memory and stored in the buffer area labeled "field" to field +8192. This data is also sent to the weight memory to save the original data for repeat condition and for isolation. The simulation is accomplished by executing a return jump to mnemonic "TFL". The results are stored in place over the original operand area. Rescale status is also generated in this subroutine for compare before actual operand compare.

If a compare error ($08) occurs after a transform in any of the sections 16, 17, 18, 19, 1A, 1B, and 1C, the setting of bit 12 in the stop/jump word will execute a jump to the routine "isolate".

The routine isolate brings in the original data, and one-level transforms and compares are executed until the original data, that caused the first error to occur, is relocated to perform a transform of field length equal to two.

The first typeout (error code 1B is explained under error code explanation), and will only occur if the error repeats while doing one-level transforms. The cosine and sine values are also obtainable at this time and are included in typeout 1B.

These operands are now used for simulation at a field length of two and these expected results and cross products are included in error code 1B.

At this point, we now have the original operands to perform a field length transform of two and also all expected results.

The original data is now sent to the FFT module to perform a transform of field length equal to two. The FFT is functioned and a compare is made of the transformed data. If the data does not compare, error code 1C is executed.

If the data does compare, the original data will be sent again to the FFT, a transform functioned, and data compare completed. This loop will be continuously executed until a compare error occurs or the SKIP switch is set and bit 12 is cleared.

If repeat condition bit is set at this time and run is executed, the original data and transform will be completed.

If the section is repeated, section initialization will clear the isolation bit automatically by masking out bit 12 in the stop/jump word.

E. COSINE AND SINE TABLE

The trigonometric values, in the FFT diagnostic program listing, consist of the sine values from zero to ninety degrees.

From this table, the cosine and sine values from zero to one hundred and eighty degrees can be developed. The actual values of the sine functions are complemented before shipment to the FFT phase memory.

Transform simulation obtains the trig values by incrementing and decrementing through the table in the listing.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS - approximately 6700_{10} locations

B. TIMING - 15 min.

C. EQUIPMENT CONFIGURATION

1. 1704 with 16K of memory
2. 1705 Interrupt Data Channel
3. 1706 Buffered Data Channel
4. FFT Algorithm Module

QSE 4557

1700/200 REMOTE USER TERMINAL DIAGNOSTIC

(CTUA44 Test No. 44)

Equipped with 1700 Computer, 1749 CTC, 311B DSA, 201 MODEM

CTU Test No. 44 (Communications Terminal User)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. The real time operation of the 200 User Terminal requires this Diagnostic to be run alone type test. The test will be called and run separately.
2. Telephone communication must be established between the 200 User Terminal and the Computer.
3. The switch settings on the 200 User Terminal are assumed to be in the following positions:

   External BCD
   Poll - Normal
   Error - Enable
   Attended Mode
   Block Mode

4. The 311B Data Set Adapter is assumed to have coding plugs for operating in the Universal Mode.

B. LOADING PROCEDURE

1. The test loads under control of SMM17.
2. The test number 44 is used for the calling sequence under SMM17.

C. PARAMETERS

If Bit 0 of the Stop/Jump word is set, the program will make one initial stop following initialization.

Initial Stop	(A) = ID Word
	(Q) = Stop/Jump Word
2nd Stop	(A) = Sections to run ($7FF)
	(Q) = 1749 Equipment Number ($280)

3rd Stop (A) = DSA Even Channel Assignment ($0)
(Q) = Set Site Address ($71) = (Oct 161)

4th Stop (A) = Display size ($410 = 1040) ($3E8 = 1000)
(Q) = Printer Line Size ($88 = 136) ($50 = 80)

The above parameters can be changed initially or by setting bit 10 in the Stop/Jump parameter on re-run. This can be done by setting the SKIP switch and running from initial address.

Stop/Jump Parameters

Bit 0 - Stop to enter parameters
Bit 1 - Stop at end of test section
Bit 2 - Stop at end of test
Bit 3 - Stop if error occurs
Bit 4 - Repeat condition
Bit 5 - Repeat test section
Bit 6 - Repeat Test
Bit 7 - Unused
Bit 8 - Omit typeouts
Bit 9 - Bias return address display
Bit 10 - Stop to re-enter parameters
Bit 11 - Speed-up (Limit to one compare error)
Bit 12 - Hold H pattern display (Section 2)

Bit 4 - Repeat Condition Bit

All repeat condition loops reference the main part of the program (no repeat condition loop possible in a subroutine).

Setting the repeat condition bit, after an error stop, will cause the last output and input to be repeated irregardless of the error reoccurring. Clearing bit 4 (set SKIP Switch to stop) will allow program to continue.

When a compare of Data is called for, the repeat condition (on the last output and input) will take place after the compare. (See speed-up bit parameter)

Bit 11 - Speed-up Bit Parameter

This bit set in the Stop/Jump parameter will cause the data compare routine to compare data till the first error occurs and then do a normal exit from the routine, unless repeat condition is set.

Bit 12 - Hold H Pattern Display

This bit causes section 2 (Display Test) to hold a pattern of Alpha Character H on the entire screen. Exit section will occur when send is depressed.

II. MESSAGES

A. NORMAL

1. Test identification at start of test "200 User Diagnostic CTU IA = XXXX"
"Make Phone connect"

2. End of section typeout
"End section XX"

3. End of test typeout
"End CTU"

B. ERROR MESSAGES

1. The 1st two stops and AQ typeouts will have the following format for all error messages:

1st stop (A) = Identification word
(Q) = Stop/Jump parameter

2nd stop (A) = Section (Bits 8-15) error (Bits 0-7)
(Q) = Return address

(The return address will always reference the main program to provide an address in the main program where the error occurred)

2. Error Code Description

Following is a description of the possible error codes and the meaning of the additional stops if applicable.

Error 01 - Incorrect entry in W field of Q for 1749 equipment. (W must equal zero)

3rd Stop

(A) = Equipment parameter
(Q) = Unused

Error 10 - No character request status from 311B after time-out.

3rd Stop

(A) = Even Channel status (311B DSA)
(Q) = Odd Channel status (311B DSA)

Error 23 - Received incorrect Site Address in Message Format

3rd Stop

(A) = Actual Site address received
(Q) = Expected

Error 24 - Received Incorrect Station Address in Message Format

3rd Stop

(A) = Actual Station address received
(Q) = Expected

Error 25 - Received Incorrect Control Code in Message Format

3rd Stop

(A) = Actual Control code
(Q) = Expected

Error 26 - Did not receive an escape code preceding the E code

3rd Stop

(A) = Code received
(Q) = Expected Escape code

Error 27 - Received Incorrect E Code in message format

3rd Stop

(A) = Actual E code received
(Q) = Expected

Error 28 - MPC Compare Error

3rd Stop

(A) = Actual MPC received
(Q) = Expected MPC

Error 29 - Did not receive the expected response within a timeout of approximately 1 minute.

3rd Stop

(A) = Actual Response received
(Q) = Expected Response

Error 30 - Character Phase not established. After functioning the 311B to Go to Receive mode, character phase was not established in sufficient time.

3rd Stop

(A) = Even Channel status (311B DSA)
(Q) = Odd Channel status (311B DSA)

Error 31 - No initial data. Character phase was established in Receive mode, but no initial data was received (Activity Bit 11 was not received with data).

3rd Stop

(A) = Even Channel status (311B DSA)
(Q) = Odd Channel status (311B DSA)

Error 32 - Stopped receiving data before End of Message (EOM). Activity bit not set.

3rd Stop

(A) = Even Channel status (311B DSA)
(Q) = Odd Channel status (311B DSA)

Error 33 - No MPC was received after EOM was received.

3rd Stop

(A) = Even Channel status (311B DSA)
(Q) = Odd Channel status (311B DSA)

Error 34 - Did not recognize an SOM (Start of Message) code after initial reception of data. (A timeout of 40 ms was completed)

3rd Stop

(A) = Last code received
(Q) = Expected an SOM code

Error 35 - 1050 Characters were received without an EOM code being recognized.

3rd Stop

(A) = Last character received (1050th)
(Q) = Unused

Error 40 - Data Compare Error

3rd Stop

(A) = Actual Data received
(Q) = Expected Data

4th Stop

(A) = Number of Characters compared at the time of error.
(Q) = Unused

Error 41 - Card Reader Section Compare Error

3rd Stop

(A) = Actual Data received
(Q) = Expected Data

4th Stop

(A) = Column Count at time of error
(Q) = Card Count at time of error

Error 50 - A 1700 Internal Reject Occurred

3rd Stop

(A) = Contents of A at Reject
(Q) = Contents of Q at Reject

4th Stop

(A) = 1749 CTC Status
(Q) = Unused

Error 51 - An External Reject Received from the 1749 CTC.

3rd Stop

(A) = Contents of A at Reject
(Q) = Contents of Q at Reject

4th Stop

(A) = 1749 CTC status
(Q) = Unused

A separate error message typeout indicates when 1749 CTC status cannot be obtained.

III. DESCRIPTION

The sections described below use the routine 'WRITE' for output to the 200 user terminal, routine 'READ' for input, routine 'RESP' to check message format, and routine 'COMPAR' for data checking.

The tag names refer to actual listing locations.

Refer to Paragraph I. C. 2 for parameters to repeat condition, repeat section, repeat test.

Timing - Due to the necessary manual intervention, the time for the test to complete all sections is variable, but the average time should range from 5 to 10 minutes.

SECTOA The instructions from this location in the listing to SECTOD consist of a loop that completes the following sequence of events. Each numbered operation is repeated nine times before the next numbered sequence is executed.

"Message to Display" or Condition to Test	Control Code	Response Code
1. "Write Being Tested"	$11	$06
2. "Reset Write Being Tested"	$0C	$06
3. "Clear Write Being Tested"	$12	$06
4. "Diag Write Being Tested"	$10	$13
5. "Reject Poll Being Tested"	$12	$06
6. No Message - Poll for Reject	$05	$18
7. "Error Being Tested"	$12	$06
8. (Unacceptable Control Code to 200 User)	$00	$15
9. "Poll Error Being Tested"	$12	$06
SECTOE (Poll with incorrect station address)	$05	$15
10. "Station 161 Being Tested"	$12	$06
SECOE2 "Station 161 Being Tested: (Changed Station address to Octal 161).	$12	$06
11. "Station 161 Being Tested"	$12	$06
SECOE4 (Poll with Station address of 160)	$05	$18
12. "Error Being Tested"	$12	$06
SECTOG "Error Being Tested" (Force Word Parity error and check for error response)	$12	$15
13. "Error Being Tested"	$12	$06
SECOG2 "Error" (Force MPC Error)	$12	$15
14. "Error Being Tested"	$12	$06
SECOG4 "Error" (Send message without E Code)	$12	$15

"Message to Display" or Condition to Test	Control Code	Response Code
15. "Error Being Tested"	$12	$06
SECOG6 "Error Being Tested" (Do not send an EOM Code).	$12	$15
16. "Error Being Tested"	$12	$06
SECOG8 "Error" (Diagnostic write with incorrect word parity. Check for space codes received in place of forced parity error).	$10	$13
17. "Error Being Tested"	$12	$06
SECOGA "Error" (Diagnostic write with no E Code sent. Check for read and input to end of page).	$10	$13
18. "Alert Poll Being Tested"	$12	$06
SECTOH "Hit send on Alert"	$12	$06
Send Alert Code	$07	$06
Poll for a read when send	$05	$13
(This loop executed only three times)		
19. No Message - Poll for auto read response from previous alert.	$05	$13
SECTOH "Hit send on Alert"	$12	$06
Send Alert Code	$07	$06
Poll for Read	$05	$13
(This loop executed only 3 times)		

MEMORY TEST

	Message to Display or Condition to Test	Control Code	Response Code
SEC1A	Generate Field of Random Data		
SEC1B	(Full screen of Random Data) Check Data received Repeat from SEC1A 3 more times	$10	$13
SEC1C	Generate Field of all ones ($01)		
SEC1D	(Full screen of all ones) Check Data received Hold display for 10 seconds and exit	$10	$13

Section 2 DISPLAY TEST

	Message to Display or Condition to Test	Control Code	Response Code
SEC2A	"0123456789 - ABCDEFGHIJKLMNOPQRSTUVWXYZ - (. . . Special Characters . . .)"	$12	$06
	Repeat above data 3 times	$11	$06
SEC2B	Hold all character display for 10 seconds		
SEC2E	(Full screen of all H)	$0C	$06
EOSRT	Check Bit 12 of Stop/Jump Parameter if not set, hold all H Display for 10 seconds. If set, hold display until send is depressed. Exit Section 2.		

	"Message to Display" or Condition to Test	Control Code	Response Code
SEC3A1	"Set INT/EXT switch to INT and Depress Send -0123456789 ABCDEFGHIJKLMNOPQRSTUVWXYZ" (Special characters displayed on this line)	$12	$06
SECT3B	Poll for Read Check for proper internal BCD Codes received.	$05	$13
SECT3D	Send following Message in INT BCD "Set INT/EXT switch to EXT and Depress Send -123456789 ABCDEFGHIJKLMNOPQRSTUVWXYZ" (Special characters displayed on this line)	$12	$06
SECT3E	Poll for Read Check proper external BCD Codes received.	$05	$13
	Exit Section		

Section 4 ENABLE/DISABLE SWITCH TEST

	"Message to Display" or Condition to Test	Control Code	Response Code
SECT4B	"Set ERROR/DISABLE to DISABLE and send"	$12	$06
SECT4C	Poll for read after switch set.	$05	$13
SECT4D	"Error" output message with E character parity error (Expect no response).	$12	$00
SECT4E	"Set error/disable to enable and send"	$12	$06
SECT4F	Poll for read (send) to indicate switch back to enable.	$05	$13
	Exit Section		

POLL NORMAL/WAIT SWITCH TEST

	"Message to Display" or Condition to Test	Control Code	Response Code
SECT5B	"Set Poll NORM/WAIT to WAIT and send"	$12	$06
SECT5C	Poll for acknowledge when switch is thrown. Reject till then.	$05	$06
SECT5D	Poll for read when send depressed	$05	$13
SECT5E	"Set Poll NORM/WAIT to NORM and send"	$12	$06
SECT5F	Poll for reject when switch thrown. Acknowledge till then.	$05	$18
SECT5G	Poll for read when send depressed.	$05	$13
	Exit Section		

Section 6 ATTENDED/UNATTENDED SWITCH TEST

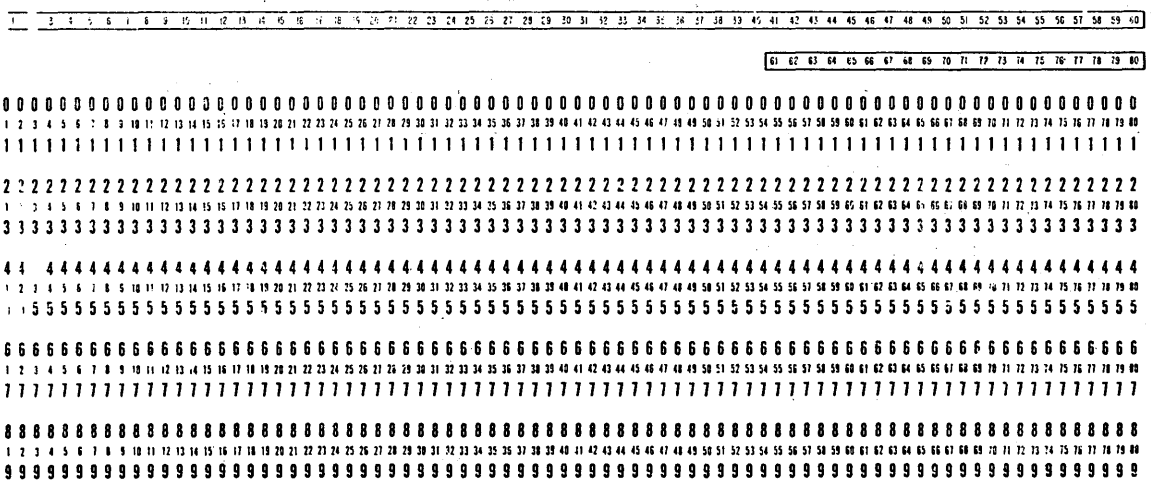
	"Message to Display" or Condition to Test	Control Code	Response Code
SECT6B	"Place in unattend and send"	$12	$06
SECT6C	Poll for read (send) to indicate switch is in unattend position.	$05	$13
SECT6E	"Alert should not be active Unattend Indicator should now be on. Wait 10 seconds." Unattend position is now active.	$11	$06
SECT6F	Send Alert Message Should receive automatic acknowledge. Display should now be clear.	$07	$06
SEC6F1	Poll for automatic read to assure alert activated read.	$05	$13
SECT6G	"This should be only message on screen. Place in attend (Indicator goes out) and send."	$0C	$06
SECT6H	Poll for read to assure attend position.	$05	$13
	Exit Section		

KEY BOARD ECHO TEST

	"Message to Display" or Condition to Test	Control Code	Response Code
SECT7A	"Keyboard Test Place message on screen and send. Your message as received will be echoed. To end section clear display and send."	$12	$06
SECT7B	Poll for Read (send). If no data, exit section.	$05	$13
SECT7C	Move rec'd data to output buffer.		
SECT7D	Send the received message.	$11	$06
	Loop to SECT7B		

CARD READER TEST

	"Message to Display" or Condition to Test	Control Code	Response Code
SEC8A	"Card Reader Test - Ready Reader, Feed one card, - Depress load and depress "Send When Ready."	$12	$06
	Poll for read (send). Continue when read received.	$05	$13
SEC8C	"Card" followed by E 3 to start reading cards. Poll to Read CArd Data.	$0C $05	$06 $13
SEC8C1	Check 1st Char. of read message for end card, go to SEC8E2 if not end card, continue.		
SEC8D	Check card image for 12 cards, or until an END card is encountered.		
SEC8F	If no end card has been received in the 12 card images, check for an E3. If an E3 Code is received go to SEC8C. If any other E Code is received exit section.		
SEC8E2	Check for the expected E2 Code and exit section 8.		



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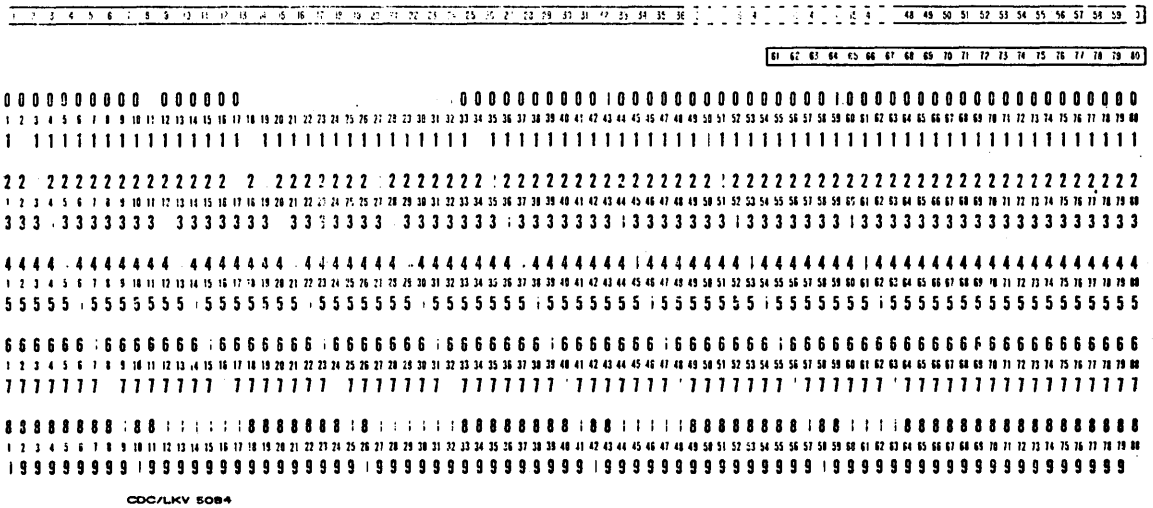

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Section 9 PRINTER TEST

	"Message to Display" or Condition to Test	Control Code	Response Code
SEC9	"Printer Test -		
	Hit Send When Ready"	$12	$06
	Poll for read (send).	$05	$13
	Continue when read received.		
S9A	Generate a ripple left pattern of all printable codes.		
S9G	(Six full printer lines of ripple).	$12	$06
	Poll for read (send from printer).	$05	$13
	Check for E3 from printer.		
	Repeat S9G for full printed page.		
SEC9A	(29 printed lines to include all compress Codes) - page eject code, "Top of Form" - one space code, "One Space" Two space Code "Two spaces" - One Space Code, "Suppress Space" - Suppress Space Code, "Suppress Space" - Suppress Space Code, "Suppress Space" - Suppress Space Code, "Suppress Space" - Page Eject Code, "Top".	$12	$06
	Poll for read (Send from printer)	$05	$13
	Check for E3 from printer.		
	Exit Section 9		

Printout description on following pages:

	"Message to Display" or Condition to Test	Control Code	Response Code
SECTA1	"1. Set to Line Mode. Set Line Indicator to Line 1. 2. Depress send Indicator once and send."	$12	$06
SECTA2	Poll for read (send). Should input Line 2. Compare input buffer for Line 2.	$05	$13
SECTA4	"3. Line Indicator should be on Line 5. 4. Place in Block Mode and send."	$11	$06
SECTA5	Poll for send to exit section.	$05	$13

1700/1749/332/2-103s/REMOTE TELETYPE TEST

(CTTA45 Test No. 45)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. This test may be loaded and run with other tests when section 2 is not selected. If section 2 is selected the test must be run alone because the section depends upon receiving uninterrupted data from a remote station.
2. Section 2 requires the presence of a remote teletype operator.
3. Only one remote teletype station will be checked at a time.
4. Function codes may be tested in section 2. (See II. E. 3. FUNCTION CODES for explanation.)

B. LOADING PROCEDURE

Call as an external test under SMM17.

C. PARAMETERS - (in the order in which they are entered)

1. SECTNS - This parameter selects desired sections according to set bits; it is prestored as 0003_{16}. Section 2, bit 3, may be selected by the operator; however, if bit 3 is set, the test must run alone.
2. SWADDO - Selecting the proper data terminal for direct addressing this parameter is formatted as OE1T. The E field, bits 10-7, contains the equipment number of the 1749 Communications Terminal Controller; and the T field, bits 3-0, contains the address of the desired data terminal.
3. DATRAT - Prestored as 0013_{16} this parameter corresponds to the printing rate of the remote teletype; and therefore, it may be changed to give the operator an approximation of the accuracy of this printing rate. Table 1 shows the relationship between the printing rate, DATRAT, and the resulting percent error. If a Character Request signal cannot be generated by the 332 DATA SET ADAPTER the error, NO REPLY ON OUTPUT will be generated; however this does not mean that a wrong value of DATRAT is the only way that this error may be created. If DATRAT is to be changed it should be adjusted in either of the first two sections, until its lowest operational value is found.

4. CODE - This parameter is used in section 1 as two 8-bit words for output to the remote station. Prestored as two ASCII bell codes, 0707_{16}, the operator may change its value to allow the option of sending any single character or any two characters.

TABLE 1. CONVERSION OF TELETYPE WORDS PER MINUTE TO THE PARAMETER DATRAT

Words Per Minute	Characters Per Second 1	Response Time Per Character 2	Datrat 3		Percent 4 Error
			Base 10	Base 16	
100	10	.10	18	0012	+9.8
			17	0011	+3.7
			16	0010	-2.4
			15	000F	-8.5
150	15	.067	13	000D	+18.9
			12	000C	+9.7
			11	000B	+ .6
			10	000A	-8.5
			9	0009	-17.6

- Based upon six characters per word.
- Reciprocal of characters per second.
- DATRAT is computed by the following formula:

  DATRAT equals response time per character divided by the output loop time of the program. The output loop time is 6.1 milliseconds.
- A plus percent means that the teletype is slow.

  A negative percent means that the teletype is fast.

D. MESSAGES AND AQ DISPLAYS

1. Normal Messages

   a. REMOTE CTT TEST 45, IA = XXXX
   MAKE PHONE CONNECTION

   This message occurs at the start of the test; the initial address is XXXX.

b. START SECTION YYYY

At the start of each section this message is typed; YYYY is the section number.

c. REPEAT SECTION

Every time a section is repeated this message is typed.

d. END TEST

4524 XXXX 00YY ZZZZ

This message is typed after each completion of the test.
4524 is the identification word.
XXXX is the Stop/Jump parameter.
00YY is the pass number.
ZZZZ is the return address.

2. Error Messages - Four basic error formats, their error codes and error type outs are shown in the following:

Error Code		Type Out
01	-	INTERNAL REJECT TRYING TO OUTPUT DATA
02	-	EXTERNAL REJECT TRYING TO OUTPUT DATA

FORMAT:

4538 XXXX SSNN ZZZZ MMMM VVVV PWYY PTTT
4538 is the identification word.
XXXX is the Stop/Jump parameter.
SS is the section number.
NN is the error code.
ZZZZ is the return address.
MMMM is the output data in A at the time of the reject.
VVVV is the command code in Q at the time of the reject.
P is C_{16} if the reject is internal or it is 8_{16} if the reject is external.
W is the status of the 332 Data Set Adapter.
YY is the data in the 332 DSA at the time of the reject.
TTT is the 1749 CTC status at the time of the reject.

Error Code		Type Out
03	-	CHARACTER REQUEST PRESENT WITH EXTRA STATUS. This error will occur on output if the status of the Data Set Adapter contains status bits other than the request bit.

Error Code		Type Out
04	-	332 AND 1749 DIFFER ON CHARACTER REQUEST BIT. This error will occur when the 332 DSA has a Character Request bit set and the 1749 CTC does not have a Character Request bit set.
05	-	NO REPLY ON OUTPUT. This error will occur on output if the 332 DSA status bit-Character Request - is not set. The response time of Table 1 is the maximum time allowed for the request bit to be set before this error occurs.
06	-	NO REPLY ON INPUT. This error will occur on input if the 332 DSA status bit-character ready is not set. A 1 minute limit is allowed for the ready bit to be set before the error occurs.

FORMAT:

4528 XXXX SSNN ZZZZ OWYY OTTT
4528 is the identification word.
XXXX is the Stop/Jump parameter.
SS is the section number.
NN is the error code.
ZZZZ is the return address.
W is the status of the 332 Data Set Adapter.
YY is the data in the 332 DSA at the time of error.
TTT is the status of the 1749 CTC.

Error Code		Type Out
07	-	WRONG STATUS BITS PRESENT WITH INPUT DATA. This error can be caused by a break or lost data condition in the 332 Data Set Adapter. This error may also occur when the 332 DSA has a character ready bit set and the 1749 CTC does not have the character ready bit set.

FORMAT:

4528 XXXX SSNN ZZZZ YYYY VVVV

4528 is the identification word.

XXXX is the Stop/Jump parameter.

SS is the section number.

NN is the error code.

ZZZZ is the address of the input word that has the error.

YYYY is formatted as follows:

Bit		Meaning
0-7	-	332 Data Set Adapter data.
8	-	332 DSA status for break.
9	-	332 DSA status for Character Lost.
10	-	332 DSA status for Character Request.
11	-	332 DSA status for Character Ready.
12	-	1749 CTC status for Status Bit 0 or 1 set.
13	-	1749 CTC status for Character Request.
14	-	1749 CTC status for Character Ready.
15	-	always set to indicate error.

VVVV is the number of the data word or character. This number can vary from 0 to $C7_{16}$ depending upon the number of characters sent by the remote TTY station.

Error Code		Type Out
08	-	PARITY ERROR ON INPUT DATA. This error is caused by a parity error in the input data; incoming data is checked for even parity.

FORMAT:

0528 XXXX SSNN ZZZZ YYYY VVVV

0528 is the identification word.

XXXX is the Stop/Jump parameter.

SS is the section number.

NN is the error code.

ZZZZ is the address of the input word that has the error. The stored word will have corrected parity.

YYYY is the word as it was received with incorrect parity. Only the lower seven bits are taken as data. The eighth bit is the parity bit.

VVVV is the number of the data word or character received. This number can vary from 0 to $C7_{16}$ depending upon the number of characters sent by the remote TTY station.

II. DESCRIPTION

A. INITIALIZATION

1. Calculate bias value.
2. Transfer last word address of the test to SMM.
3. Type out test title.
4. Set up restart address (initial address).
5. Return control to SMM.

B. SECTION 0; OUTPUT CHECK

1. The status of the 332 Data Set Adapter is checked. The 332 DSA Character Request, Ready and Lost bits should be set after the initial phone connection; an error will occur if these are not set or if character break is set. An error will also occur if the 1749 CTC Character Request bit is not set and the 332 DSA Character Request bit is set.
2. An ASCII message and a diagonal pattern is sent to the teletype when the 332 DSA Character Request bit is set. The 332 Data Set Adapter Character Request bit should set after each character is sent; an error will occur if this bit does not set within the response time of Table 1. If any other status bits are set or if the 1749 CTC Character Request bit is not set, an error will be generated.

C. SECTION 1; OUTPUT CHECK

1. If this is the very first section to run then paragraph II. B. 1. applies; otherwise, the status of the 332 DSA will be checked for the following errors. The Character Request bit should be set; it is an error if it is not set or if any other status bits are set. An error will be generated if the 1749 CTC Character Request bit is not set each time the 332 DSA Character Request bit is set.

2. The two ASCII characters, stored in the parameter CODE, are sent alternately, ten times each, to the remote station. The status of the 332 Data Set Adapter is checked for the following conditions. The Character Request bit should be set, within the response time allowed, after a single character is set. An error will occur if any other status bits are set or if the 1749 CTC Character Request bit is not set when the 332 DSA Character Request Bit is set.

D. SECTION 2; INPUT CHECK

1. If this is the only section to run, then paragraph II. C. 1. applies.

2. Instructions are sent to the remote operator telling him to send no more than 200 random characters and type the word END when finished. This output is checked character by character according to paragraph II. B. 2.

3. The 332 Data Set Adapter is checked for incoming status and data; an error is generated if the Character Ready bit is not set at least every minute after the instructions of paragraph II. D. 2. are sent to the remote operator. This bit should be set everytime a new character is received, which must occur at least once a minute until the input is terminated.

4. Incoming data is checked for the following three terminating conditions. (1) The word END is received, (2) 200 characters are received, (3) Data is not received every minute. After the input has been terminated, all of the received data is checked for proper status and parity. An error will be generated if both the 332 DSA Character Ready and Character Request bits were not set with each character or if any other 332 DSA status bits were set. An error will also be generated if the 1749 CTC Character Ready bit was not set with each character.

   Parity is regenerated and compared with the received data for each character, and a parity error will occur if the even parity is wrong. After the parity is checked the received data is retransmitted to the remote station so the remote operator may compare it to the data that was actually sent. The retransmitted data is checked for proper output status according to paragraph II. B. 2.

E. MISCELLANEOUS EXPLANATIONS

1. REPEAT CONDITION ON OUTPUT

   If repeat condition bits are not set and an output error occurs, the program will try to output the data. If repeat condition bits are set the same error condition will repeat itself until stopped or corrected.

2. REPEAT CONDITION ON INPUT

If the repeat condition bit is set in section 2 and no input data is reserved, an error typeout can occur every minute until stopped or the data is received. If the Repeat Condition bit is not set the test will end when data is not received every minute.

3. FUNCTION CODES

Function code keys such as WRU and RUB OUT may be tested in section 2; however some caution is needed. If the desired key generates an automatic reply an error condition could arise. For example, if the remote operator sends a WRU, the 1704 will receive this data and then transmit it to the same station. Upon receiving the WRU code the teletype will generate its reply; therefore, this station may be trying to receive and send at the same time depending upon what follows the WRU code. If the remote operator sends WRU as the last character and waits 1 minute the proper message should be typed out with the station's reply to the WRU as the last message; however, the error NO REPLY ON INPUT will be generated at the 1704. If the WRU is not the last character, the remote station will be trying to send and receive at the same time and non-meaningful data may be typed out, after the WRU is received. This condition may also cause wrong 332 DSA status bits to be set, creating an error the next time a character is sent or received.

EOT may also be tested, but the phone connection must be restored if the data is to be sent back. If EOT is tested in this manner, an error may occur because the 332 DSA status bits Character Ready, Character Request, and Character Lost will be generated each time a phone connection is made. If these three status bits are set it is an error, unless it is the initial connection. The sending of the EOT by the 1704 CTC will also disconnect the phone. Errors may occur when the connection is restored.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIREMENTS

1538_{10} or $5F3_{16}$ locations.

B. TIMING

Approximately 2.5 minutes.

C. EQUIPMENT CONFIGURATION

1. 1704 Computer with 4K memory.
2. 1749 Communications Terminal Controller.
3. 332 Data Set Adapter.
4. Two 103 Data Sets.
5. One Remote Teletype Station.

IV. REFERENCES

A. Control Data 1749 Communications Terminal Controller Reference Manual; Pub. No. 36827100, Rev. C

B. Control Data 332 Data Set Adapter Reference Manual; Pub. No. 13798200, Rev. A.

TELETYPE TEST SECTION 0
ABCDEFGHIJKLMNOPQRSTUVWXYZ

```
!
 "#
   $%
     &'
       ( )
         *+
           ,-
             ./
               01
                 23
                   45
                     67
                       89
                         :;
                           < =
                             > ?
                               @A
                                 BC
                                   DE
                                     FG
                                       HI
                                         JK
                                           LM
                                             NO
                                               PQ
                                                 RS
                                                   TU
                                                     VW
                                                       XY
                                                         Z[
                                                           /]
                                                             ↑←
```

SECTION 1
SECTION 2
TYPE A MESSAGE OF UP TO 200 RANDOM ALPHA-NUMERIC CHARACTERS. WHEN FINISHED TYPE THE WORD END. THE TELETYPE WILL REPEAT MESSAGE.

PLEASE REPEAT THIS MESSAGE. NOW IS THE TIME FOR ALL GOOD MEN TO COME TO THE AID OF THEIR COUNTRY. END

PLEASE REPEAT THIS MESSAGE. NOW IS THE TIME FOR ALL GOOD MEN TO COME TO THE AID OF THEIR COUNTRY. END

TELETYPE TEST SECTION 0
ABCDEFGHIJKLMNOPQRSTUVWXYZ
!
 '#
  $%
   &'
    ( )
     *+
      ,-
       ./
        01
         23
          45
           67
            89
             :;
              < =
               > ?
                @A
                 BC
                  DE
                   FG
                    HI
                     JK
                      LM
                       NO
                        PQ
                         RS
                          TU
                           VW
                            XY
                             Z[
                              /]
                               ↑ ←
SECTION 1
SECTION 2
TYPE A MESSAGE OF UP TO 200 RANDOM ALPHA-NUMERIC CHARACTERS. WHEN FINISHED TYPE THE WORD END. THE TELETYPE WILL REPEAT MESSAGE.
PLEASE TYPE THE FOLLOWING
ABCDEFGHIJKLMNOPQRSTUVWXYZ 1234567890:-!"#$%&'()*=
END
PLEASE TYPE THE FOLLOWING
ABCDEFGHIJKLMNOPQRSTUVWXYZ 1234567890:-!"#$%&'()*=
END

QSE 8249, HIGH SPEED DATA SET CONTROLLER

(HCAA24 Test No. 24)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

1. Cautions to User

   a. Section 6 tries to transmit and receive a record of synchronizing characters. However, the synchronizing character is an option on the SCA-2, and consequently it can be different on the transmit and receive logic. If this is the situation, transmit synchronizing characters will appear as data to the receive logic when echoed. Under this condition, this section should not be used.

   b. The program may stop unexpectedly with the A register = 8000. This means a table containing the addresses of data records, which have been transferred to and from the high speed data set controller but not yet processed, has overrun. The program has been partially destroyed and must be reloaded if valid results are to be expected.

   c. Errors will result in Section 1 if a 1716 or 1706 has an equipment number 3. The program checks the W=0 decoding of the HSDSC and a reply from a 1716 or 1706 with equipment number 3 will cause an illegal reply error.

   d. There must be 8K available to run the program.

B. LOADING PROCEDURES

1. The test operates under control of 1700 System Maintenance Reference Manual (SMM17).
2. The calling sequence is that specified by SMM17.
3. The test can be restarted at initial address.

C. PARAMETERS

1. Normal operation requires no parameters. The following sections will be run under this condition.

   a. Section 1
   b. Section 2
   c. Section 4

d. Section 5
e. Section 6
f. Section 8
g. Section 9
h. Section 10
i. Section 11

For the sections to run, it is assumed the Data mode is ASCII.

2. To alter the parameters, follow the directions stated in SMM17 Reference Manual. Bit zero is used to indicate a request for altering parameters. If this bit is set, a set of parameter stops will be made. The parameter words displayed during a parameter stop are as follows:

a. First Stop:

A = 2451
Q = Stop/Jump Parameter

b. Second Stop:

A = Selected Sections (Prestored as 07BB)
Bit 00 = Section 1 - Quiescent Operation
Bit 01 = Section 2 - Functions
Bit 02 = Section 3 - Functions-Operator Intervention
Bit 03 = Section 4 - Direct Storage Access and Adder
Bit 04 = Section 5 - Terminate Buffer
Bit 05 = Section 6 - Illegal Data
Bit 06 = Section 7 - Data in Universal Mode
Bit 07 = Section 8 - Data in ASCII Mode
Bit 08 = Section 9 - Data in ASCII Transparent Mode
Bit 09 = Section 10 - Odd Character Feature
Bit 10 = Section 11 - Odd Character Feature, Transparent Data
Bit 11 = Section 12 - Half Duplex

Q = Selectable Options with the following bits used:
Bit 01 = ASCII Mode
Bit 02 = Universal Mode
Bit 03 = No Parity
Bit 04 = Odd Parity
Bit 05 = Even Parity
Bit 06 = Parity Bit Enabled
Bit 07 = Frequency Range, 1.8-25 kHz

Bit 08 = Data Set 203
Bit 09 = Frequency Range, 25-230,4 kHz
Bit 10 = Test Mode
Bit 11 = Data Set Simulator
Bit 12 = Resync Option

c. Third Stop:

A = Receive Interrupt Line (prestored as line 4 with only bit 4 set in A)

Q = Transmit Interrupt Line (prestored as line 6 with only bit 6 set in A)

d. Fourth Stop:

A = Equipment Number (prestored as 4)

Q = Equipment Number not used by the system peripherals (prestored as 2)

e. Fifth Stop:

A = Synchronizing Character (prestored as 0016)

Q = 0000

f. Parameter Entry Cautions

If parameters are incorrectly entered, a parameter error will occur and the test will return to the initial parameter stop. Before the test will begin execution, parameters must be correct.

During the second stop, the selectable options must be selected in the following manner:

1) Only one data mode.
2) Only one parity mode.
3) Only one frequency range.
4) Either test mode or data set simulator selected. With the simulator selected, an appropriate data set in echo mode can also be used for testing.

During the third stop, interrupt lines 0 and 1 cannot be used. The receive interrupt line and transmit interrupt line must be different.

During the fourth stop, the equipment number cannot be zero and the W field and director field must be zero.

During the fifth stop, the synchronizing character cannot be zero and must be loaded into the lower seven bits.

g. Messages

1) Typeouts or Alarms

a) Normal Program Typeouts

(1) High Speed Data Set Controller identification during test initialization.

HIGH SPEED DATA SET CONTROLLER TEST 24
IA = XXXX

(2) End of Test

A	Q	A	Q
2424	Stop/Jump Parameter	Pass Number	Return Address

b) Error Alarms

All information shown is displayed after General Display Format.

General Display Format:

A	Q	A	Q
Information Word	Stop/Jump Parameter	Section/ Error Code	Return Address

c) Error Codes

Error messages will follow the standard SMM17 error message reporting technique of generating an error identification number for each specific error type. Error codes and additional appropriate data will be displayed for the following errors.

(1) Input/Output Errors

Error Code	Description
28	Internal reject on a function A = Q at the time of reject Q = Rejected command
27	External reject on a function A = Q at the time of reject Q = Rejected command A = Status II at the time of reject Q = Status I at the time of reject
2A	Internal reject after a status A = Q at the time of reject Q = Not significant
29	External reject after a status A = Q at the time of reject Q = Not significant
30	Internal reject after an Illegal command A = Q at the time of reject Q = 0, during an input operation or Q ≠ 0, during an output operation
31	External reject after an Illegal command A = Q at the time of reject Q = 0, during an input operation Q ≠ 0, during an output operation
36	Reply after an Illegal command Same error display as error 30.

(2) Parameter Entry Errors

Error Code	Description
01	Test mode-data set simulator entry
02	Frequency entry
03	No parity selected

Error Code	Description
04	More than one parity selected
05	Data mode entry
06	Interrupt lines entry
07	Equipment number entry
08	Synchronizing character entry
0A	Unused equipment number entry

(3) Test Errors

Error Code	Description
0B	An interrupt occurred, but the periodic, transmit, and receive interrupt status bits were all zero. A = Status I at the time of interrupt Q = Status II at the time of interrupt A = Exit value of interrupt Q = Not significant
0C	Periodic interrupt did not clear. Same error display as error 0B.
0D	Receive end of operation interrupt did not clear. Same error display as error 0B.
0E	Receive alarm interrupt did not clear. Same error display as error 0B.
0F	Transmit alarm interrupt did not clear. Same error display as error 0B.
10	Transmit end of operation interrupt did not clear. Same error display as error 0B.
13	Unexpected periodic interrupt. A = Status I at the time of the interrupt Q = Status II at the time of the interrupt

Error Code	Description
14	Interrupt status bit did not set after an interrupt. Same error display as error 13.
16	Receive alarm interrupt but no alarm status. Same error display as error 13.
17	Unexpected receive memory parity error interrupt. Same error display as error 13.
18	Unexpected program protect fault interrupt. Same error display as error 13.
19	Unexpected ring indicator interrupt. Same error display as error 13.
1A	Unexpected receive data set ready alarm interrupt. Same error display as error 13.
1B	Unexpected carrier on interrupt. Same error display as error 13.
1C	Receive interrupt but no alarm or end of operation status. Same error display as error 13.
1D	Unexpected receive end of operation interrupt. Same error display as error 13.
1E	Either transmit interrupt but no alarm or end of operation status. Same error display as error 13.
20	Transmit alarm interrupt but no alarm status. Same error display as error 13.
21	Unexpected transmit data set ready. Alarm interrupt. Same error display as error 13.

Error Code	Description
22	Unexpected transmit memory parity error interrupt. Same error display as error 13.
23	Unexpected transmit end of operation interrupt. Same error display as error 13.
24	Error in Status I after a program clear A = Actual status Q = Expected status
2D	Status error A = Expected status Q = Actual status A = Q at the time of status Q = Not significant, except when Q = FFFF. Then the error message refers exclusively to a resync error. This will only occur in Section 2.
2E	Data Compare error A = First word address for the record containing the expected data Q = First word address for the record containing the actual data A = Expected data Q = Actual data A = Word in error Q = Record length

Error Code	Description
32	Transmit current word address register error. A = Actual status Q = Expected status A = Q at the time of status Q = Not significant
33	Receive current word address register error. A = Actual status Q = Expected status A = Q at the time of status Q = Not significant
3E	Function error A = Status indicating the error Q = Function in error A = Q at the time of error Q = Not significant
40	A parity error condition was forced by sending illegal data. The hardware failed to recognize a parity error. A = Output data Q = Not significant
41	DSA address error, data was sent to the wrong address A = Actual first word address Q = Actual last word address A = Not significant Q = Q at the last output A = Expected first word address Q = Expected last word address
44	A buffered data transfer was initiated but the current word address counter did not increment

Error Code	Description
	A = Actual status Q = Expected status A = Q at the time of status Q = Q at the last data initiation A = Last first word address transmitted Q = Last last word address +1 transmitted
45	A terminate buffer command did not terminate the data transfer. Same error display as error 44.
47	Transmit current word address counter failed to increment during a data transfer. A = Actual status Q = Expected status A = Q at the time of status Q = Q at the last data initiation A = First word address at last data initiation Q = Last word address +1 at last data initiation
48	Receive current word address counter incremented during a record whose data was synchronizing characters. Same error display as error 47.
49	Transmit current word address counter does not equal LWA+1 after a transmit end of operation interrupt. Same error display as error 47.
4A	Receive current word address counter incremented during a record whose data was synchronizing characters. The check is made at the end of the transmit record. Same error display as error 47.
4C	Data received in error when synchronizing characters transmitted as data.

Error Code	Description
	A = Actual data Q = Expected data A = Word in error Q = Q at the last data initiation A = First word address at last data initiation Q = Last word address +1 at last data initiation
50	Time out error A = Type of time out error 0001 = Carrier on interrupt 0002 = Periodic interrupt 0003 = End of operation interrupt Q = Not significant
51	Bad quiescent status. For Status I this means a lost data, parity error, and/or no ready status. For Status II this means either carrier on = 0 or Test mode = 0 and sync established = 0. A = Actual status Q = Q at the time of status
55	A lost data condition was forced but no lost data status was received. A = Actual status Q = Q at the time of error
56	Transmit current word counter did not increment during a data transfer. A = Transmit current word address Q = Not significant

II. DESCRIPTION

A. METHOD

1. Section 1 - Quiescent Operation

a. Input Primary Status

1) Ready should be present.
2) No other status should be present.

b. Check the test mode of request send function depending on the param eters.

1) Output the function.
2) Timeout for synchronizing characters.
3) Input secondary status for test mode or carrier on.

c. Load the transmit and receive address registers with various patterns, retrieve and verify the data using the following (hex) patterns.

1) FFFF
2) 0000
3) 5555
4) Sliding One
5) Sliding Zero

d. Check the reply and reject circuitry.

1) Output two transmit and receive first word address with the first output replied to and the second rejected.
2) Status using an unused equipment number and expect an internal reject.
3) With W = 0C, output and input and expect internal rejects.
4) Output unused commands and expect external rejects.

2. Section 2 - Functions

a. Initiate the following functions.

1) Connect/Disconnect
2) Test Mode
3) Reverse Channel Receive
4) Clear Communication Adapter
5) Clear Parity
6) Clear Interrupt

b. Activate the periodic interrupt and verify it does operate.

c. Start an output operation and verify that it terminates properly.

d. Force a lost data condition checking the lost data status.

e. Issue a resync command if the resync option is not enabled, and in either case verify that a resync took place.

f. Output and input the entire buffer area to check counters.

g. Force a parity error and status for the parity error bit.

3. Section 3 - Functions With Operator Intervention

a. All protect bits are cleared.

b. Typewriter prints "PROTECT" and operator should place the 1700 PROTECT switch in Protect mode and HSDSC PROTECT switch in Protect mode.

c. An unprotected status should not be rejected.

d. An unprotected command should be rejected.

e. Typewriter prints "UNPROTECT" and the operator should place the 1700 PROTECT switch in Unprotected mode.

f. Core protect bits are set to a one.

g. Typewriter prints "PROTECT" and operator should place the 1700 PROTECT switch in Protect mode.

h. A Program Protect fault should be generated.

i. Typewriter prints "UNPROTECT" and operator places both 1700 and HSDSC PROTECT switches to Unprotect position.

j. Protect fault interrupt and status verify hardware operation.

k. Typewriter prints "DIAL DATA SET". This is used for checking automatic answering. This is done by actually dialing the data set or by throwing a switch in the HSDSC which causes the HSDSC to think there is an incoming call.

l. During a data transfer, the Data Set Ready alarm is forced to verify it is operational.

4. Section 4-- DSA and Adder Test

a. The ability of the hardware to read from and write into core at the proper location.

b. All of the buffer area is set to zero.

c. The first word in the buffer area is set to a 0617 pattern and output.

d. This location is set to zero.

e. Data is input to ensure that is reached the correct location. The data is not checked for errors.

f. The location is set to zero.

g. Steps b-f are repeated for each location in the buffer area.

h. If data is sent to the wrong location, the program searches the buffer area for the data.

5. Section 5 - Terminate Buffer

   a. A data transfer is started and a check is made to ensure a transfer has started.

   b. A terminate command is issued and an end-of-operation interrupt is expected.

   c. Steps a and b are repeated for various buffer lengths.

6. Section 6 - Sync Character I/O

   a. A data pattern of sync characters is output to the HSDSC.

   b. The program attempts to input the sync characters as data but the hardware should not allow any of them to be input.

7. Section 7 - Data Transfer in Universal Mode

   a. Using variable length buffers and variable data patterns, output data in Universal mode.

   b. Input the data and verify proper data, correct parity, proper status, and correct interrupts.

   c. Steps a and b are repeated for each data pattern.

8. Section 8 - Data Transfer in ASCII Mode

   a. Using variable length buffers, output data in ASCII mode.

   b. The data pattern output is formatted with ASCII control characters.

   c. The data patterns are varied according to a pattern generator.

   d. Input data is verified for accuracy, proper parity, proper status, and correct interrupts.

   e. Steps a-d are repeated for each data pattern and buffer length.

9. Section 9 - Data Transfer in ASCII Transparent Mode

   a. Using variable length buffers, data is output in ASCII Transparent mode.

   b. The data pattern output is formatted with ASCII control character which places the HSCSC in Transparent mode.

   c. The data patterns are varied according to a pattern generator.

   d. Input data is verified for accuracy, proper parity, proper status, and correct interrupts.

   e. Steps a-d are repeated for each data pattern and buffer length.

10. Section 10 - Data Transfer in Either Universal or ASCII Mode Using the HSDSC Odd Character Feature

   a. Using variable length buffers, data is sent to the HSDSC in either ASCII or Universal mode. However, the buffers are set up to have an odd character which the hardware should recognize.

   b. The data pattern is sent in either ASCII or Universal mode.

   c. The data patterns are varied according to a pattern generator.

   d. Input data is verified for accuracy, proper parity, proper status, correct interrupts, and correct odd character handling.

   e. Repeat steps a-d for each data pattern and buffer length.

11. Section 11 - Data Transfer in ASCII Transparent Mode Using the HSDSC Odd Character Feature

   a. Using variable length buffers, data is transmitted in ASCII Transparent mode with the buffer set up to have an odd character.

   b. The data patterns are varied according to a pattern generator.

   c. Input data is verified for accuracy, proper parity, proper status, and correct odd character handling.

   d. Repeat steps a-c for each data pattern and buffer length.

12. Section 12 - Data Transfer in Half Duplex From an External Source

   a. On entering the section, a stop is made for entering a record length.

   b. The HSDSC is set up to receive data in Half-Duplex mode.

   c. On reception of data, the transmit record is sent to the HSDSC and back to the sending station.

d. The data is not checked but correct status and interrupts are checked.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

The test needs a minimum of 3200 memory locations and thus requires an 8K system.

B. TIMING (Test Running Alone, No Errors)

It is impossible to give an accurate indication of how long each section will run because the SCA-2 clock's range is from 1.8 kHz to 230.4 kHz.

1. Section 0 = 4 to 16 Seconds
2. Section 2 =
3. Section 3 =
4. Section 4 =
5. Section 5 =
6. Section 6 =
7. Section 7 =
8. Section 8 =
9. Section 9 =
10. Section 10 =
11. Section 11 =
12. Section 12 =

C. EQUIPMENT CONFIGURATION

1. 1704 computer with 8K of memory
2. 1705 Interrupt Data Channel
3. QSE 8249 - High Speed Data Set Controller

QSE 6340 FV219 PLOTTER CONTROLLER TEST
(PLT039 Test No. 39)

I. IDENTIFICATION:

A. Test number - 39

B. Mnemonic - PLT

C. Equipment - 17x4 Computer
17x5 Data Channel
FV219 (500 Series)

D. SCOPE

The diagnostic exercises the functions available in QSE 6340 for 500 series mode operation. All of its parameters are accepted and displayed at the A/Q registers. By parameter selection, a 12 inch or 30 inch plotter parameter can be selected to provide a pattern size to exercise the plotting area. If a TTY is present, the end of test sections as well as errors will be given on the printer. Test No. 39 contains three sections called Test 1, Test 2, and Test 3 which exercises the different functions as follows:

Test 1:

1. Loads count for 12 or 30 inch plotter.
2. Centers pen in plotting area.
3. Executes consecutive pen up's and down's.

Test 2:

1. Executes an operation and checks busy status.
2. Executes an operation and processes interrupt on EOP.

Test 3:

1. Visual test of all direction pattern.
2. Pattern is executed three times for exact retrace.

II. OPERATIONAL PROCEDURE:

A. RESTRICTIONS:

1. This test will exercise the 500 series mode of the controller using the 1705 A/Q Data Channel. This test will not operate in 700 series mode or on the 1706 BDC.

B. LOADING PROCEDURE:

1. Manually load in magnetic tape boot strap.
2. Set P register to initial address of boot strap. Set SELECTIVE SKIP and SELECTIVE STOP switch and run.
3. First stop will be A=SMM parameter and Q=Stop/Jump parameter. See 1700 SMM Reference Manual.
4. Second stop will be for calling in external test. Set A=39YY, Q=Equipment no. of plotter. YY is the number of passes requested.
5. Drop SELECTIVE SKIP and run.

C. Test No. 39 will load into memory and check for parameter stop. If bit 0 of the SMM Stop/Jump parameter is set at the start of the test, a parameter will occur.

1. Selective Stops

a. Parameters for Test No. 39.

1) First stop will be A = 3941, Q = Stop/Jump parameter. The Stop/Jump parameter may be changed if desired.

2) Second stop will be A = 00FF (do not change) Q = 0007 (selected test sections). Bit 0 corresponds to Test 1, bit 1 to Test 2, and bit 2 to Test 3. Test 1 must be selected to establish plotter parameters. Test 2 and Test 3 are optional.

3) Third stop will be *A = Lost data interrupt line, *Q = RNB interrupt line. Set the bit corresponding to the external interrupt line (bit 4 is for interrupt line 4).

4) Fourth stop will be *A = EOP interrupt line (as above) Q = select plotter size. Bit 0 = 1 for 12 inch plotter and bit 0 = 0 for 30 inch plotter.

---

*The same bit will be set for all three interrupt conditions since a common external interrupt line is used.

b. End of Section:

1) A = 3922
   Q = Stop/Jump parameter

2) A = 0X00 (X = section number)
   Q = Return address

c. End of Test

   A = 3924
   Q = Return address

d. Error (see Section D-2)

D. MESSAGES:

1. Normal Program Typeouts

a. Initialization of test: FV219-A02 PLT Test 39 IA = XXXX

b. After passing each section:

   End Test 1
   End Test 2
   End Test 3

c. End of pass through diagnostic

A	Q	A	Q
3924	Stop/Jump	Pass Count	Return Address

2. Error Typeouts

Error typeouts will be as follows:

A	Q	A	Q	A	Q
3938	Stop/Jump	*XXEE	Return Add	Contents of A Register	Contents of Q Register

a. Sense Test Errors

   01 Unit not ready at start
   02 Did not receive interrupt on RNB status
   03 Did not receive busy status

b. Interrupt Error

   50 EOP interrupt not received
   Lost data interrupt will appear as SMM interrupt error.

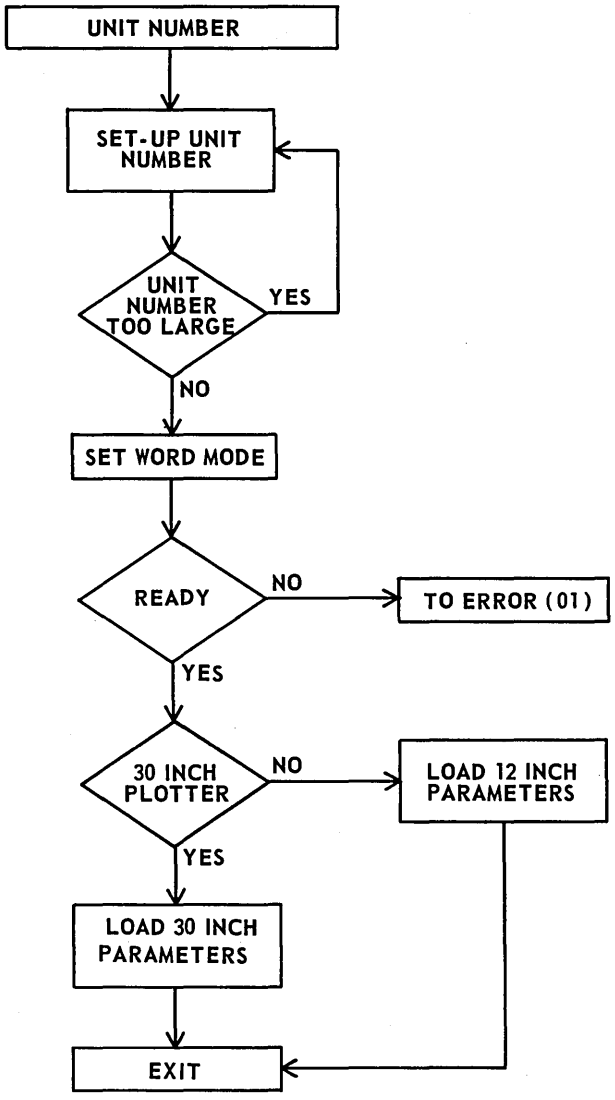
c. Reject Errors:

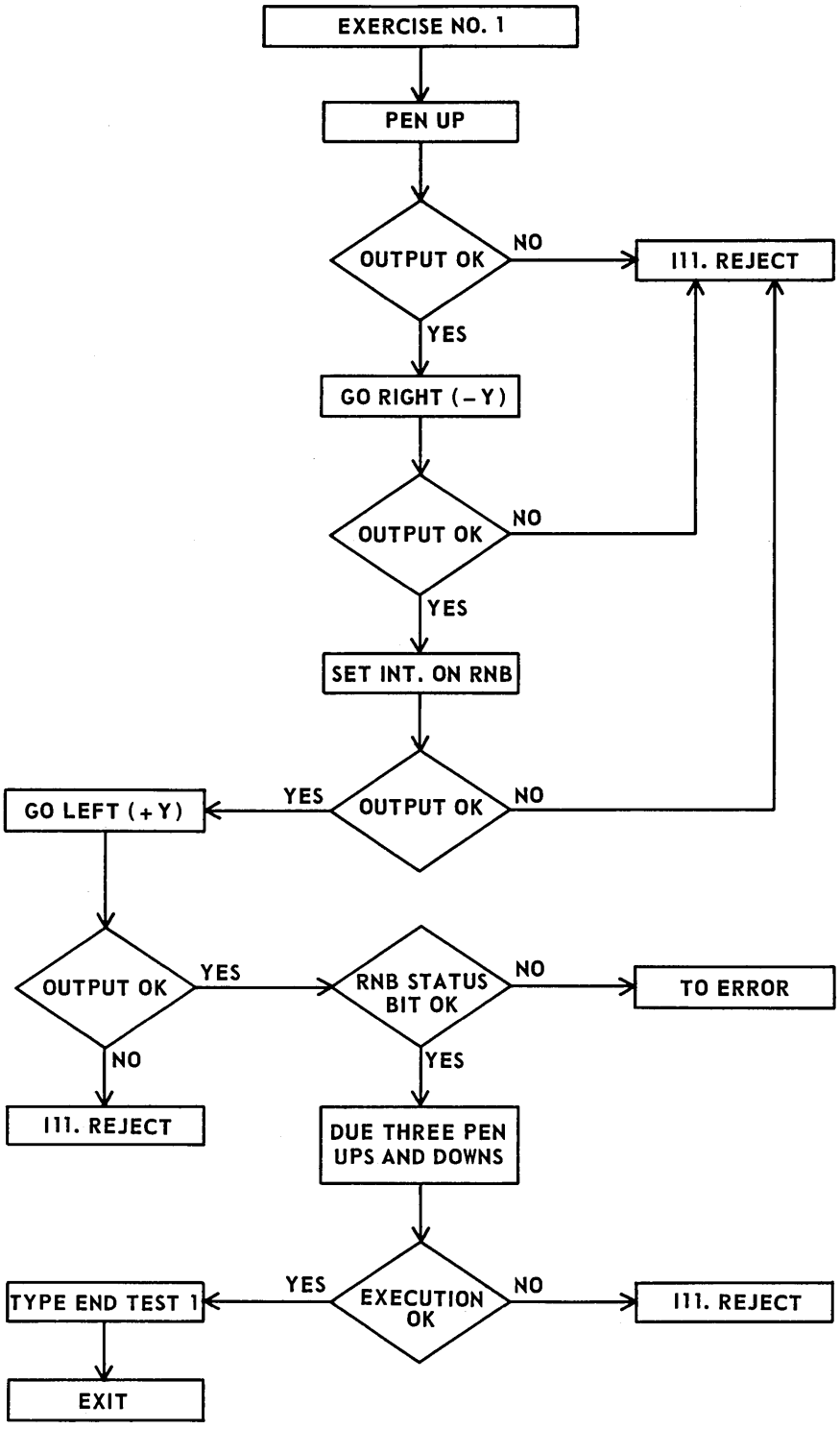
7E Internal reject

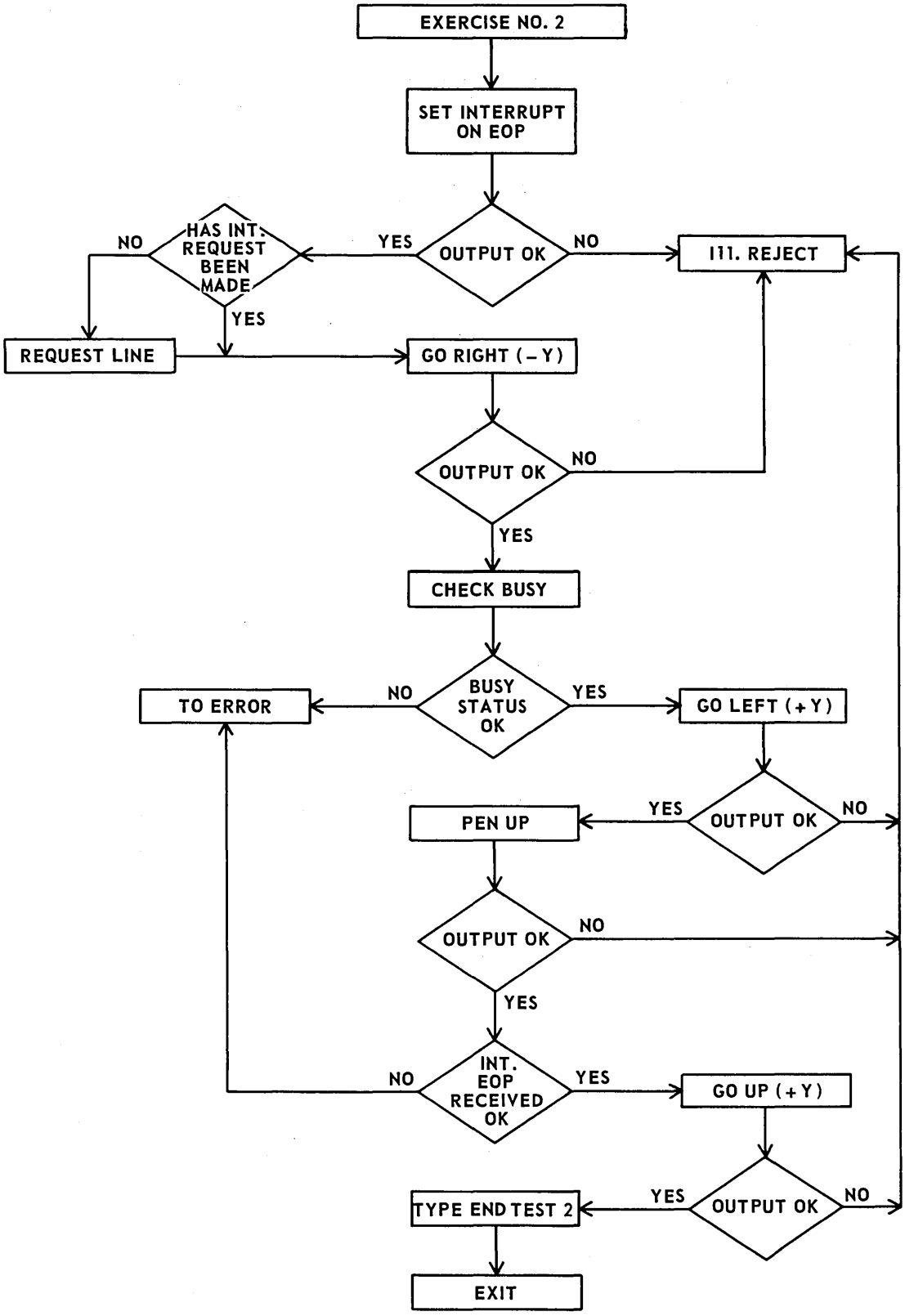
7F External reject

NOTE

XX is section number. EE is the error number.

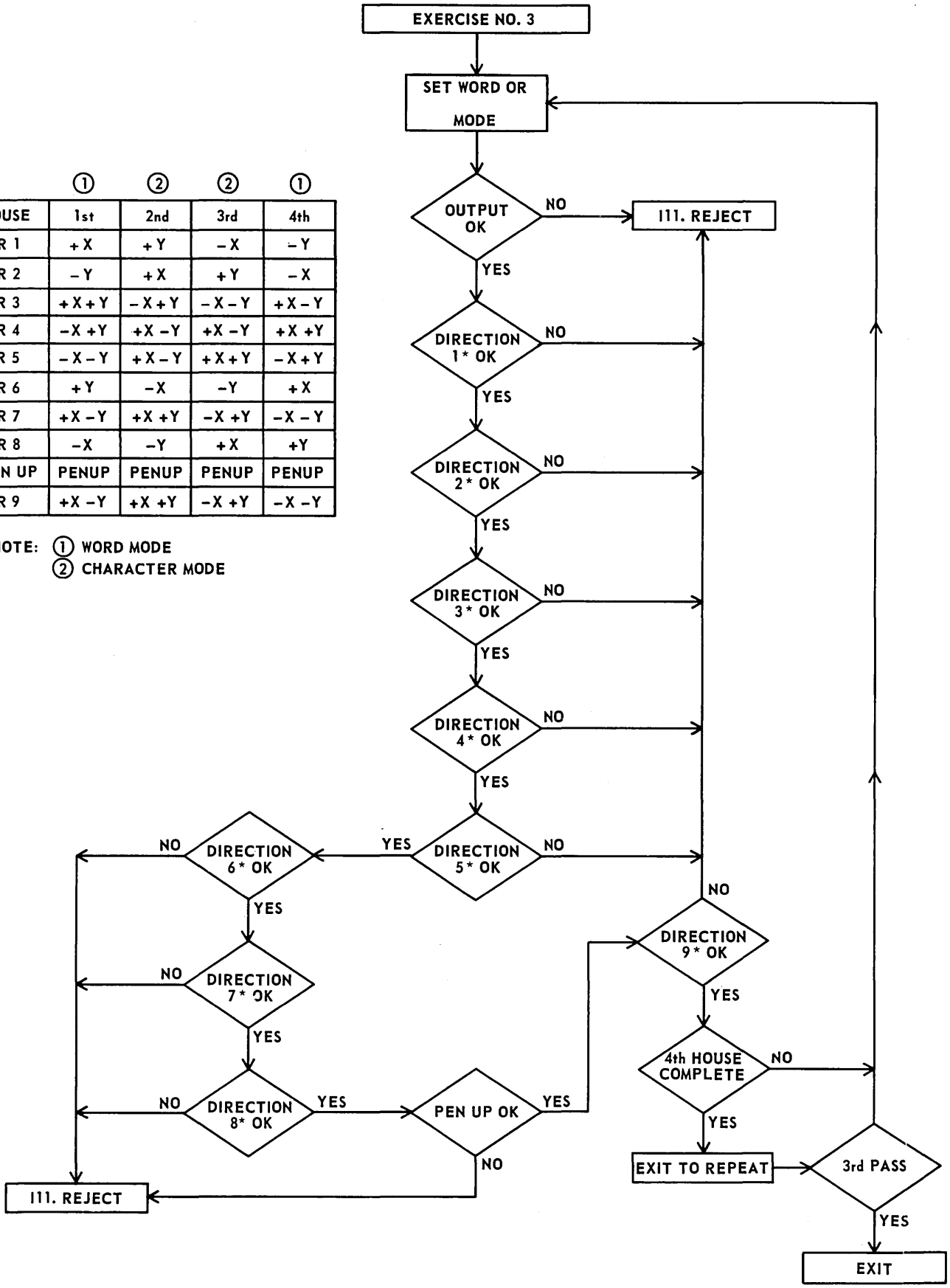



EXERCISE NO. 1
PEN UP
OUTPUT OK
NO
111. REJECT
YES
GO RIGHT (-Y)
OUTPUT OK
NO
YES
SET INT. ON RNB
GO LEFT (+Y)
YES
OUTPUT OK
NO
OUTPUT OK
YES
RNB STATUS BIT OK
NO
TO ERROR
NO
YES
111. REJECT
DUE THREE PEN UPS AND DOWNS
TYPE END TEST 1
YES
EXECUTION OK
NO
111. REJECT
EXIT


EXERCISE NO. 2
SET INTERRUPT ON EOP
OUTPUT OK
NO
111. REJECT
YES
HAS INT. REQUEST BEEN MADE
NO
YES
REQUEST LINE
GO RIGHT (-Y)
OUTPUT OK
NO
YES
CHECK BUSY
BUSY STATUS OK
NO
TO ERROR
YES
GO LEFT (+Y)
OUTPUT OK
YES
NO
PEN UP
OUTPUT OK
NO
YES
INT. EOP RECEIVED OK
NO
YES
GO UP (+Y)
OUTPUT OK
YES
NO
TYPE END TEST 2
EXIT

	①	②	②	①
HOUSE	1st	2nd	3rd	4th
DIR 1	+X	+Y	−X	−Y
DIR 2	−Y	+X	+Y	−X
DIR 3	+X+Y	−X+Y	−X−Y	+X−Y
DIR 4	−X+Y	+X−Y	+X−Y	+X+Y
DIR 5	−X−Y	+X−Y	+X+Y	−X+Y
DIR 6	+Y	−X	−Y	+X
DIR 7	+X−Y	+X+Y	−X+Y	−X−Y
DIR 8	−X	−Y	+X	+Y
PEN UP	PENUP	PENUP	PENUP	PENUP
DIR 9	+X−Y	+X+Y	−X+Y	−X−Y

NOTE: ① WORD MODE
② CHARACTER MODE

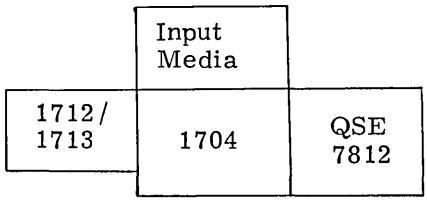


QSE 7812 OPERAND BANK TEST
(QOBA3A Test No. 3A)

I. GENERAL

This specification is for a 32K Operand Bank (QSE 7812) diagnostic test that is designed to operate under SMM17 (1700 Maintenance Monitor System). The installation and operation of the diagnostic is in accordance with the standard procedures as defined in the SMM17 Reference Manual. Information necessary to the interpretation of the diagnostic is contained within this specification.

II. EQUIPMENT



Equipment necessary to the test:

A. One 1704 Computer

B. One QSE 7812

C. One 1712/1713 Teletype

D. One of the following input media:

1. 1731 Magnetic Tape
2. 1721 Paper Tape Reader
3. 1738 Disk Pack Controller
4. 1712/13 Teletype

III. SOFTWARE DEPENDENCIES

A. The QSE 7812 diagnostic is designed to operate under SMM17.

B. Interface between the system and the diagnostic is through programs that are considered within SMM17.

IV. LIMITATIONS

A. Core residence for the test is 1250 decimal locations. Total residence (SMM17 + QSE 7812 diagnostic) is 2750 locations.

B. This diagnostic is not intended to be a memory test. It will only verify that the special NOP instructions used to READ and WRITE into the upper 32K are working correctly. If diagnostic errors are reported that resemble memory errors, it is suggested that the QSE 7812 be switched to 32K upper mode and the standard SMM17 Memory Diagnostic be run.

V. OPERATING CHARACTERISTICS

A. LOADING PROCEDURE

1. The test will be loaded under the control of SMM17.
2. Before the diagnostic is to be loaded, the operator must place the switch on the control panel to 65K mode.

B. PARAMETERS

1. If bit 0 of the Stop/Jump word is not set, the test will be run using prestored parameters. The prestored parameters are as follows:
   a. 1700 main memory consists of 4K of core.
   b. QSE 7812 operand bank consists of 4K of core.
   c. Test No.'s 1, 2, 4 are preselected.

NOTE

If the prestored parameters do not fit a particular site's configuration they may be changed by following the procedures in the SMM17 Edit Routine.

2. If bit 0 of the Stop/Jump word is set, the program will make four stops for test parameter display and/or entry.

   a. First Stop

      Displays the identification word (3A41) in A and the Stop/Jump word in Q.

   b. Second Stop

      A register is used for test section selection and for entering the amount of core in the 1700 Main Memory (M) and the QSE 7812 Operand Bank (OB). When stop is made A = 3421 (Figure 1).

      If Section 3 of the test is selected, the Q register must be entered with the core location to be checked. See VI.C.

   The next two stops are only necessary if Section 3 has been selected.

   c. Third Stop

      A register must be entered with the instruction to be tested.

      Q register must be entered with the operand to be used.

   d. Fourth Stop

      A register must be entered with the contents of the Index register when the instruction is to be executed.

      Q register must be entered with what Q is to be set to when the instruction is executed.

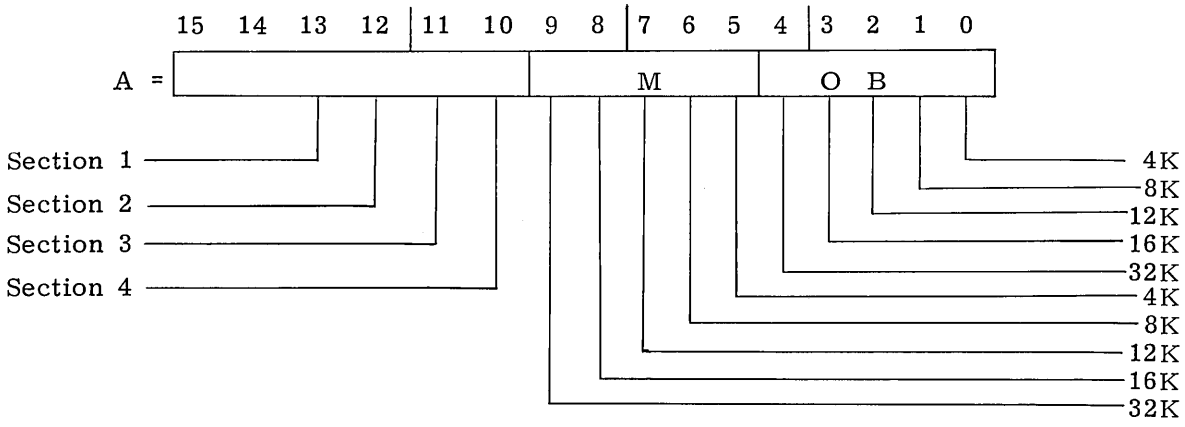


Figure 1

C. MESSAGES

No typeouts occur if bit 8 of the Stop/Jump parameter is set.

1. Normal Program Display

   a. Test identification typeout at start of test

      Operand Bank Test

      IA = XXXX
      (XXXX = Starting Address of Test)

   b. End of Test Typeout

A	Q	A	Q
3A24	Stop/Jump Word	Pass Number	Return Address

2. Error Display

   Error stops 1 and 2 are displayed according to the format described by SMM17.

   Additional stops will be made to display information related to a specific error. See Section VII.

VI. DESCRIPTION

This diagnostic verifies that the special NOP instructions used in addressing the Operand Bank are working correctly. Sections 1 and 2 of the diagnostic will use these instructions with all addressing modes.

A. SECTION 1

This section will perform three functions.

1. It will verify that the normal NOP instruction will not address the Operand Bank.
2. It will verify that Operand Bank can be completely cleared.
3. It will verify that each location can be set to all ones.

B. SECTION 2

This section will verify that each location can be set with its own and the complement of its own address.

C. SECTION 3

If Section 3 is to be run, it must be selected during parameter entry. This section will use only the load and store versions of the instruction given during parameter entry. The operand used, core location, and addressing modes are all selectable.

D. SECTION 4

This section verifies the program protect system in the Operand Bank is working correctly. This is done by setting all of the protect bits in the main memory and the Operand Bank. The diagnostic then tries to store zeros in each location of the Operand Bank using a non-protected store.

VII. ERROR CODES

Error Code	Explanation
01	An error has been made in parameter entry. The test will ask for new parameters.
02	An NOP instruction (0B00-0B7F) failed. It performed as a Load A. Third Error Stop A = Contents of location it read. Q = NOP instruction that failed. This is also the location it read up.
03	An NOP instruction (0B00-0B7F) failed. It performed a Store A. Third Stop A = NOP instruction that failed. This is also the location it stored into. Q = The location specified by A before the store. Fourth Stop A = The current contents of the location specified by the third stop. Q = Disregard.
04	Could not clear the specified location. Third Stop A = Contents of location that failed. Q = Instruction that failed. Fourth Stop A = Location that failed. Q = Index register. Fifth Stop A = Q register. Q = Disregard.

Error Code	Explanation
05	Could not set the specified location to all ones. Error stops are the same as in Error 04.
06	Could not store the specified location with its own address. Error stops are the same as in Error 04.
07	Error in Section 3, operand stored, and pattern loaded differs. Third Stop A = Operand read. Q = Operand selected.
08	Protect interrupt was expected but did not occur. A = Location which should have generated the interrupt. Q = Disregard.
09	Protect interrupt occurred which did not set the protect fault indicator within the computer.
0A	Unexpected interrupt on line 0. A = Address where interrupt occurred. Q = Disregard.
0B	Could not store the specified location with the complement of its own address. Error stops are the same as in Error 04.

QSE 7698 1745-1746/210 DISPLAY STATION TEST
(DDD046 Test No. 46)

I. INTRODUCTION

A. IDENTIFICATION

1. Type of Program

   Diagnostic test under 1700 System Maintenance Monitor (SMM17)

2. Computer

   CONTROL DATA® 1700

B. PURPOSE

The Display Station Test operates under the control of the 1700 System Maintenance Monitor to verify all of the operating features and data handling capabilities of either the 1745 or 1746 Controller.

NOTE

It does not check any features pertaining to the typewriter.

C. CAUTIONS TO USER

The timing is done by counting the number of returns to SMM17. All wait times were calculated by the 1745-1746/210 Test running alone. Therefore, when operating in a system mode these times can be greatly increased.

II. PARAMETER ENTRY

Each time the test is entered, either during the initialization or on restart, the test will identify itself by typing:

1745-1746/210

After this typeout, the computer will halt four times.

A. STOP 1

Displays in A the test number and in Q the Stop/Jump parameter.

B. STOP 2

Enters into the A register the equipment address necessary for a direct input or output (i.e. W=O, 2,7, or C; E=equipment address; S=O; and D=O). Enter into the Q register the interrupt line (i.e. bit 7 implies the 1745/1746 is on interrupt line 7).

C. STOP 3

Enters into the A register the subtest to be executed, i.e. bit 3 implies execute test 3. See Section III.

NOTE

If QSE 7698 (null character) is installed select Test 8 if you wish to run Test 4.

Enter into Q the stations to be tested (i.e. bits 1 and 2 imply stations 1 and 2 are to be tested).

D. STOP 4

Enter into the A register

0050_{16} If the screen size is 13 x 80 or

0032_{16} If the screen size is 20 x 50

Enter into the Q register

$000D_{16}$ If the screen size is 13 x 80 or

0014_{16} If the screen size is 20 x 50

E. STOP/JUMP WORD

Bit 00 must be set to enter parameters.

Bit 02 must be set to stop at end of test.

Bit 03 must be set to type out errors.

III. SUBTEST EXPLANATION

If the multi-station controller (1745) and more than one station is being tested, the station is started with the highest station number (i.e. stations 1 and 2 defined for testing, station 2 will be functioned, then station 1).

The timing is done by counting the number of returns to SMM17. All wait times were calculated by the 1745-1746/210 test running alone. Therefore, when operating in a systems mode these times can be greatly increased.

A. TEST 0 REJECT

1. Purpose

This test verifies the various reject no-reject capabilities of the display subsystem.

The "Reject Code" defines the sequence of operations in which an error was found. See Section V for error typeouts.

2. Method

Reject Code	Procedure	Expected Result
0	Copy status. Check protect status.	Error No 2E if protected. Error No 2D if not protected.
0	Select all possible stations (station numbers 1 through 15). Deselect all stations.	Type station numbers that could be selected. See error code 2F.
1	Issue director function of 3.	Internal reject.
2	Set A = 0. Issue director function of 2.	No reject.
3	Select station.	No reject.
4	Select station. Set active.	No reject.
5	Select station. Clear active.	No reject.
6	Deselect station.	No reject.
7	Deselect station. Set active.	No reject.
8	Deselect station. Clear active.	No reject.
9	Clear A. Issue director function of 1.	No reject.
A	Select end of operation interrupt.	No reject.
B	Select station interrupt.	No reject.
C	Deselect station alert.	External reject.

Reject Code	Procedure	Expected Result
D	Select end of print interrupt.	No reject.
E	Clear interrupt enables.	No reject.
F	Deselect station. Clear screen. Wait for not busy.	External reject.
10	Deselect station. Reset. Wait for not busy.	External reject.
11	Select station. Set active. Alert.	No reject.
12	Select station. Set active. Reset. Wait for not busy.	No reject.
13	Select station. Set active. Clear screen. Wait for not busy.	No reject.
4	Clear controller.	No reject.

B. TEST 1 STATION SELECT

1. Purpose

This test assures that the station selected is the one that data will be transmitted to.

2. Method

a. Clear controller.

b. Reset all stations selected for testing.

c. Select station.

d. Set active.

e. Write screen (full screen each character position containing the station number). Wait a minimum of 2 seconds.

f. Repeat steps 3 through 5 for all defined stations.

g. Reset all stations.

h. Select station.

i. Read full screen. Wait a minimum of 2 seconds.

j. Verify data.

k. Repeat steps 5 through 10 for all defined stations.

l. Clear screen for all stations.

C. TEST 2 END OF OPERATION INTERRUPT ON END OF MESSAGE

1. Purpose

This test verifies that the end of operation interrupt will be generated when the end of message character is read.

2. Method

a. Clear controller.

b. Reset all defined stations.

c. Select station.

d. Set active.

e. Write the end of message character.

f. Deselect station.

g. Repeat steps 3 through 6 for all defined stations.

h. Reset all defined stations.

i. Select station.

j. Set active.

k. Enable end of operation interrupt.

l. Read data.

m. Wait a minimum of 50 milliseconds for interrupt.

n. Verify interrupt status.

o. Deselect station.

p. Verify data.

q. Repeat steps i through p for all defined stations.

r. Steps b through q are repeated until the end of message character has been written in all screen positions starting with the last character and ending with the first (total of 1000 outputs for the 20 x 50 option or 1040 outputs for the 13 x 80 option).

D. TEST 3 PATTERN TEST

1. Purpose

This test verifies that the delay line will accept various bit patterns without losing or retaining bits.

2. Method

a. Clear controller.

b. Reset all defined stations.

c. Select station.

d. Set active.

e. Write full screen. Wait a minimum of 2 seconds.

f. Clear active.

g. Deselect station.

h. Repeat steps b through g for all defined stations.

i. Reset all defined stations.

j. Select station.

k. Set active.

l. Read full screen. Wait a minimum of 2 seconds.

m. Deselect station.

n. Clear active.

o. Verify data.

p. Repeat steps d through o for all defined stations.

q. Clear screen for all defined stations.

r. Repeat steps b through q until all patterns are written, read, and verified.

Patterms Used in Testing

Pattern Number	ASCII Characters	Octal Codes	Expected Displayed Data
1	2041	0001	bA
2	3F3E	7776	?
3	2020	0000	bb
4	3F3F	7777	??
5	4747	0707	GG
6	3838	7070	88
7	5555	2525	UU
8	2A2A	5252	**

E. TEST 4 ALL CHARACTERS IN ALL POSITIONS

1. Purpose

This test verifies that all characters can be written in each screen position (the carriage return (OD) is not used and null character 5B is not used if Qse 7698 is selected). The test further verifies that all illegal characters are transformed into delete codes (7F). All 256 ASCII characters are outputted for all screen positions, as defined by Figure 1.

2. Method

a. Clear controller.

b. Reset all defined stations.

c. Select station.

d. Set active.

e. Write full screen.

f. Clear active.

g. Deselect station.

h. Repeat steps c through g for all defined stations.

i. Reset all defined stations.

j. Select station.

k. Set active.

l. Read full screen.

m. Clear active.

n. Deselect station.

o. Verify data.

p. Repeat steps j through o for all defined stations.

q. Repeat steps b through p until all characters have been written, read, and verified for all screen positions. Steps b through p are repeated a total of 256 times thereby using the complete ASCII symbol set.

Line \ Character Position	1	2	3	4	5	6	7	8
1	00	01	02	03	04	05	06	07
2	01	02	03	04	05	06	07	08
3	02	03	04	05	06	07	08	09
4	03	04	05	06	07	08	09	0A
5	04	05	06	07	08	09	0A	0B

First Output

Line \ Character Position	1	2	3	4	5	6	7	8
1	01	02	03	04	05	06	07	08
2	02	03	04	05	06	07	08	09
3	03	04	05	06	07	08	09	0A
4	04	05	06	07	08	09	0A	0B
5	05	06	07	08	09	0A	0B	0C

Second Output

Figure 1. ASCII Symbols Outputted

F. TEST 5 CARRIAGE RETURN

1. Purpose

This test verifies that carriage returns can be written, properly interpreted, read, and written over. Carriage is implied by * and blank is implied by b. The pattern used is:

LINE 1 LINE 2 LINE 4 LINE 7 LINE 11b*

2. Method

a. Clear controller.

b. Reset all defined stations.

c. Select station.

d. Set active.

e. Write full screen of periods. Wait a minimum of 2 seconds.

f. Clear active.

g. Deselect station.

h. Repeat steps c through g for all defined stations.

i. Reset all defined stations.

j. Select station.

k. Set active.

l. Write pattern (21 words). Wait a minimum of 2 seconds.

m. Clear active.

n. Deselect station.

o. Repeat steps d through n for all defined stations.

p. Reset all defined stations.

q. Select station.

r. Set active.

s. Read data (21 words). Wait a minimum of 2 seconds.

t. Clear active.

u. Deselect station.

v. Verify data.

w. Repeat steps q through v for all defined stations.

x. Reset all defined stations.

y. Select station.

z. Set active.

aa. Write full screen of apostrophies. Wait a minimum of 2 seconds.

bb. Clear active.

cc. Deselect station.

dd. Repeat steps y through cc for all defined stations.

ee. Reset all defined stations.

ff. Select station.

gg. Set active.

hh. Read full screen. Wait a minimum of 2 seconds.

ii. Clear active.

jj. Deselect station.

kk. Verify data.

ll. Repeat steps ff through kk for all defined stations.

G. TEST 6 READY AND NOT BUSY INTERRUPT

1. Purpose

This test verifies that the ready and not busy interrupt will be returned for a reset, clear screen, read, and write.

2. Method

a. Clear controller.

b. Select section.

c. Sect active.

d. Issue reset.

e. Select ready and not busy interrupt.

f. Wait a minimum of 50 milliseconds.

g. Verify interrupt status.

h. Write 1 word (AB).

i. Select ready and not busy interrupt.

j. Wait a minimum of 50 milliseconds.

k. Verify status.

l. Repeat steps h through k until the full screen has been outputted.

m. Issue reset and clear loop count.

n. Select ready and not busy interrupt.

o. Wait a minimum of 50 milliseconds.

p. Verify status.

q. Read full screen minus loop count.

r. Select ready and not busy interrupt.

s. Wait a minumum of 50 milliseconds.

t. Verify status.

u. Verify data.

v. Increment loop count.

w. Repeat steps q through u until loop count equals number of words necessary to fill the screen.

x. Repeat steps b through w for all defined stations.

y. Select station.

z. Set active.

aa. Select clear screen.

bb. Select ready and not busy interrupt.

cc. Wait a minimum of 50 milliseconds.

dd. Verify status.

ee. Clear active.

ff. Deselect station.

gg. Repeat steps y through ff for all defined stations.

H. TEST 7 STATION INTERRUPT

1. Purpose

   This test verifies that the station interrupt will occur for each defined station.

2. Method

   a. Clear controller.

   b. Select station.

   c. Set active.

   d. Enable end of operation interrupt.

   e. Select clear screen.

   f. Wait for interrupt.

   g. Read full screen.

   h. Verify.

   i. Clear active.

   j. Deselect station.

   k. Repeat steps b through j for all defined stations.

   l. Select station.

   m. Set active.

   n. Write the message:

      CLEAR

      ENTER MESSAGE

      SEND

   o. Clear active.

   p. Deselect station.

   q. Repeat steps l through p for all defined stations.

   r. Enable station interrupt.

   s. Wait for station to interrupt (5 minutes minimum).

   t. When the interrupt is received, verify interrupt status.

   u. Select station.

v. Set active.

w. Read screen.

x. Clear active.

y. Deselect station.

z. Search input buffer for EOM.

aa. Place station number directly behind EOM.

bb. Select station.

cc. Set active.

dd. Write message (number of words to first EOM).

ee. Clear active.

ff. Deselect stations.

gg. Repeat steps r to ff until all defined stations have been accounted for.

CAUTION

If the multi-station controller (1745) and more than one station is being tested, the error "send request status not cleared after a read" (Error 27) may be generated if two or more stations interrupted (send request) at about the same time.

I. TEST 8 NULL CHARACTER CHECK

1. Purpose

This test verifies the delay line will not recognize a null character (5B) and is only to be selected if QSE 7698 is installed in the controller.

2. Method

a. Clear controller.

h. Build output buffer.

c. Reset all defined stations (DDRSET).

d. Select station (DDSLSN).

e. Set active (DDSACT).

f. Write full screen. Wait a minimum of 2 seconds (DDWRIT).

g. Clear active (DDCLAC).

h. Deselect station (DDDSSN).

i. Repeat steps d through h for all defined stations.

j. Modify output buffer for read verify.

k. Reset all defined stations (DDRSET).

l. Select station (DDSLSN).

m. Set active (DDSACT).

n. Read full screen. Wait a minimum of 2 seconds (DDREAD).

o. Deselect station (DDDSSN).

p. Clear active (DDCLAC).

q. Verify data.

r. Repeat steps l through q for all defined stations.

s. Clear screen for all defined stations (DDCLSC).

Pattern used for full screen write:

ASCII Characters	Screen Character
2A2A	* - *
5B2A	null - *
5B5B	null - null
2A5B	* - null

J. END OF TEST

1. Purpose

This is not a test and cannot be selected or deselected by the operator. Its purpose is to write the message

END OF TEST

on the screen of each station. Any errors encountered in this test will be indicated as belonging to test 9.

2. Method

a. Clear controller.

b. Clear screen (no verify).

c. Select station.

d. Set active.

e. Write the message.

f. Deselect station.

g. Repeat steps c through g for all defined stations.

h. Go to SMM to check for end of test stop.

i. Go back and repeat all selected subtests.

IV. ROUTINES USED BY TEST

The following is a list of routines common to all subtests. They are presented so that the user may follow the sequence of operation of each subtest.

A. CLEAR ACTIVE ROUTINES

1. Purpose

   This routine attempts to clear the station active condition.

2. Methods

   a. Issue the clear active function.

   b. Check status for no active bit.

B. CLEAR SCREEN ROUTINE

1. Purpose

   This routine issues a clear screen function specifying the end of operation interrupt.

2. Method

   a. Select station.

   b. Set active.

   c. Select end of operation interrupt.

   d. Wait for interrupt (minimum of 50 milliseconds).

   e. Verify interrupt status.

   f. Read and verify full screen, if not end of test. See Section I.

   g. Repeat steps a through f for all stations defined.

C. Deselect Station

1. Purpose

This routine attempts to deselect a previously selected station.

2. Method

a. Issue a deselect station function.

b. Check status for no active bit.

D. FUNCTION ROUTINES

1. Purpose

These routines issue either a director code 1 or director code 2. Any rejects that are detected are immediately typed, control is then returned without reissuing the command.

E. NON REAL-TIME INTERRUPT PROCESSOR

1. Purpose

This routine processes all non-real-time interrupts. It verifies the status received against the status expected.

2. Method: (See flow chart)

F. NON REAL-TIME STATUS ROUTINE

1. Purpose

This routine inputs and stores both director status 1 and director status 2. If any rejects occur, either internal or external, an error message will be typed along with the contents of A and Q when the reject occurred. After the error has been typed, the routine will attempt to input the status again and will continue to do so until the reject condition disappears.

2. Method

a. Input director status 1.

b. Input director status 2.

c. If no rejects, return.

d. If rejects, type error and repeat steps a through c.

G. READ ROUTINE

1. Purpose

This routine is used to input data from the selected station. The read routine will maintain maximum input rate provided it is not interrupted. Any internal rejects that occur will be typed immediately. Any external rejects will be allowed to continue for approximately 25 milliseconds. When an external reject has been continuous for 25 milliseconds, the status is sensed to see if active has dropped. If active has dropped, an error message will be typed. Active will be enabled. If active has not dropped, an external reject error message will be typed.

In the event a reject error message, internal, active dropped, or external, inputting will continue with the pair of characters in which the reject occurred.

H. REAL-TIME INTERRUPT PROCESSOR

1. Purpose

This routine attempts to clear all interrupts while in an interrupt state condition.

2. Method

1. Input and save status 1 and 2.
2. Issue a clear interrupt function.
3. Input and save status 1 and 2.
4. If the interrupt did not clear, disable the mask bit from both the interrupt save area and from SMM enable interrupt mask word.
5. Return to SMM interrupt processor.

I. REAL-TIME STATUS ROUTINE

1. Purpose

This routine inputs status 1 and status 2 while in an interrupt state condition. Any rejects that occur are flagged so that they may be processed non real-time. If a reject occurs, status 1 is set up to show an interrupt is present and status 2 is set to zero.

J. RESET ENTRY MARKER

1. Purpose

This routine issues a reset function, specifying the end of operation interrupt.

2. Method

a. Select station.

b. Set active.

c. Select end of operation interrupt.

d. Issue reset.

e. Wait for interrupt (minimum of 50 milliseconds).

f. Verify interrupt status.

g. Repeat steps a through f for all defined stations.

K. SET ACTIVE ROUTINE

1. Purpose

This routine attempts to activate a selected station.

2. Method

a. Issue the set active function.

b. Check status for active bit.

L. VERIFY ROUTINE

1. Purpose

To verify the data inputted against that expected.

2. Method: (See flow chart)

M. WRITE ROUTINE

1. Purpose

This routine is used to output data from the selected station. The write routine will maintain maximum output rate, provided it is not interrupted. Any internal rejects that occur will be typed immediately. Any external rejects will be allowed to continue for approximately 25 milliseconds. When an external reject has been continuous for 25 milliseconds, the status is sensed to see if active has dropped. If active has dropped, an error

message will be typed, the station selected and active reenabled. If active has not dropped, an external reject error message will be typed.

In the event a reject error message, internal active dropped, or external, the outputting will continue with the pair of characters in which the reject occurred.

Director Status 1

Bit	Purpose
00	Ready
01	Busy
02	Interrupt
03	Ready and Not Busy
04	End of operation Interrupt
05	Not Used
06	Not Used
07	Protected
08	Not Used
09	Station Print Request
10	Station Printing
11	End of Message
12	Active
13	Send Request
14	Printer Printing
15	Print Complete Interrupt

Director Status 2

Bits 6 through 9 indicate the station that issued the send request interrupt. All other bits are not used.

V. ERROR TYPEOUTS

1745-1746/210

TEST t STN ss ERROR ee

ST1 _ _ _ _ ST2 _ _ _ _

AAAA BBBB CCCC DDDD*

Where:

t is the subtest number.

ss is the station number in which the error occurred.

ee is the error code.

ST1 is director status 1.

ST2 is director status 2.

* This contains additional information about the error. See the error code table for the information contained.

Error Number	Explanation	Additional Information
00	No end of operation interrupt on a clear screen function. Minimum wait time 50 milliseconds	None
01	External reject on director status 1	AAAA contents of the A register BBBB contents of the Q register CCCC see reject code, if error occurred in Test 0, for sequence leading to the error
02	Internal reject on director status 1	See error code 01
03	External reject on director status 2	See error code 01
04	Internal reject on director status 2	See error code 01
05	External reject on director function 1	See error code 01
06	Internal reject on director function 1	See error code 01
07	External reject on director function 2	See error code 01
08	Internal reject on director function 2	See error code 01
09	External reject on output of data, the reject has been continuous for more than 25 milliseconds	AAAA = contents of A on reject BBBB = contents of Q on reject
0A	Internal reject on input of data	See error code 09
0B	External reject on input of data, the reject has been continuous for more than 25 milliseconds	See error code 09
0C	Internal reject on input of data	See error code 09
0D	An internal reject was expected but none occurred	See error code 01

Error Number	Explanation	Additional Information
0E	An external reject was expected but none occurred	See error code 01
0F	An unexpected external reject was defected (Test 0 only)	See error code 01
10	An unexpected internal reject was defected (Test 0 only)	See error code 01
11	The active status bit is not set following a set active command. (The station has previously been selected)	None
12	Data verify error The alarm will be turned on for the station that is in error and will remain on for a period of not less than 30 seconds following the verification of the data read from the last station. If no error occurred, the information will be displayed for a period of not less than 2 seconds.	AAAA = Expected data (lower 8 bits) BBBB = Data received (lower 8 bits) CCCC = The line in which the error occurred (starting with line 1) DDDD = The character which is in error (starting with character 1) Up to 7 such errors will be typed until it is assumed that the data block is bad. At this point, the verify will be aborted. This is signified by typing AAAA = FFFF BBBB = FFFF CCCC = blank DDDD = blank
13	The interrupt status bit is still set following a clear interrupt command	None
14	The station active bit is set following a clear active command	None
15	The end of operation status bit is not set following an end of operation interrupt	None

Error Number	Explanation	Additional Information
16	The controller has been busy for more than 50 milliseconds	None
17	No end of operation interrupt has occurred for a reset command, minimum wait time 50 milliseconds	None
18	No end of operation interrupt has occurred for a data input containing an end of message character. Minimum wait time 50 milliseconds	None
19	Active status dropped while outputting data (continuous external rejects for 25 milliseconds before status is checked)	None
1A	Unexpected end of message status has been detected	None
1B	Active status dropped while inputting data (continuous external rejects for 25 milliseconds before status is checked)	None
1C	Unexpected end of operation status has been defected	None
1D	No end of message status is detected following the end operation interrupt for an end of message character minimum wait time 50 milliseconds	None
1E	An unexpected send request interrupt has been detected. Bits 6 through 9 of director status 2 contain a station address that was not defined in parameter entry	AAAA = The station address that gave the unexpected interrupt BBBB = 0
1F	A send request interrupt has been detected from a station that has already given a send request interrupt	See error code 1E

Error Number	Explanation	Additional Information
20	No end of message character can be found in the input buffer following a read on send request interrupt	None
21	No send interrupt(s) have been detected in the past 5 minutes (minimum time)	AAAA = the bits represent the stations that have not replied with a send interrupt
22	An unidentified interrupt has occurred	AAAA = Interrupt that was expected 00 = End of operation on clear screen 17 = End of operation on reset 18 = End of operation on end of message 21 = Send interrupt
23	Director status 2, bits 6 through 9 are zero following a send request interrupt	None
24	Not used	
25	Send request status is present when no send interrupt is expected	None
26	The send request status is not present for an expected send interrupt	None
27	Send request status not cleared after a read. Also see caution for Test 7 (Section H)	None
28	No ready and not busy interrupt after a write. Minimum wait time 50 milliseconds	None
29	Ready and not busy status is not present on a ready and not busy interrupt	None
2A	The ready and not busy interrupt did not occur after a read. Minimum wait time 50 milliseconds	None

Error Number	Explanation	Additional Information
2B	The ready and not busy interrupt did not occur after a reset minimum wait time of 50 milliseconds	None
2C	The ready and not busy interrupt did not occur after a clear screen. Minimum wait time 50 milliseconds	None
2D	This is not an error condition. It defines the position of the PROTECT switch through the status. The PROTECT switch is not on. Also see Test 0 (Section A)	AAAA Not used BBBB Not used CCCC Zero
2E	This is not an error condition. It defines the position of the PROTECT switch. The PROTECT switch is on. Also see Test 0 (Section A)	See 2D
2F	This is not an error condition. It defines the stations that could be selected	AAAA Not used BBBB Not used CCCC Zero DDDD Contains the stations that could be selected (i.e. bit 2 set implies station 2 could be selected), also see Test 0 (Section A)

DC215 DATA TRANSFER BUFFER/415 CARD PUNCH TEST (QSE)

(CP4A2E Test No. 2E)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

This test requires a 1700 computer having 8K (or more) core. This test should be run alone.

B. PHYSICAL REQUIREMENTS

1. Storage requirements - approximately 2500_{10} locations.
2. Timing - variable, depending on length of test deck.
3. Equipment configuration:
   a. 1704 computer with 8K memory
   b. 1705 Interrupt Data Channel
   c. DC215 Data Transfer Buffer/415 Card Punch

C. LOADING PROCEDURE

This test operates as a subprogram under control of the 1700 System Maintenance Monitor (SMM17). The calling sequence is that specified by SMM17. This test is number 2E (hexadecimal).

D. PARAMETER STOPS

At the beginning of the test, the parameter stop below will occur if stop 1 (bit 0) of the Stop/Jump parameter has been selected. The parameter stop is a three-stop set.

First Stop:
A = ID word
Q = Stop/Jump parameter

Second Stop:
A = Select special conditions (bits 1-10 preset)
Clear A for complete test

Bit 0 Cycle Section. Setting this bit will cause the section chosen to be cycled. If this bit is set, only one section may be selected.

Bits 1-10 Select the sections to be tested. Any combination of sections may be selected unless bit 0 is set. Only one section may be selected.

Bit 1 - A Bit 6 - F
Bit 2 - B Bit 7 - G
Bit 3 - C Bit 8 - H
Bit 4 - D Bit 9 - I
Bit 5 - E Bit 10 - J

Bit 12 Cycle Specific Card. If the cycle card bit is set, also select the section containing that card in bits 1-10. That section will be punched up to the specified card. Then that card will be cycled until the test is stopped.

Q = Number of Card to be Cycled. Preset to -0. Set to pattern number desired. (See QSE Test No. 2F, Figure 1 for the card pattern numbers).

Third Stop:

A = Equipment Number. Preset to 0300 (hex). If the DTB is not equipment no. 6, set correct equipment number in bits 7-10.

Q = Interrupt Line. Preset to 0040 (hex). Change if equipment is not on line 6. Bit 0 = line 0, bit 1 = line 1, etc.

E. MESSAGES

1. Title Typeout
   CP4A2E, DTB/415 CARD PUNCH TEST
   IA = XXXX
   where XXXX is the initial address

2. End Typeout
   END DTB/415 TEST

F. ERROR STOPS

An error stop will occur if an error condition is found and if stop 8 (bit 3) of the Stop/Jump parameter is set. This is a three-stop set.

First Stop: A = ID word
Q = Stop/Jump parameter

Second Stop: A = Error code
Q = Return address

Third Stop: A = 415 status if error code = $A, = data or function if error code = $13, = DTB status if error code = $19, otherwise = 0

Q = Equipment code if error code = $13, otherwise = 0

G. ERROR CODES (all errors will terminate the program except error numbers $A, $B, $C)

01 Internal reject when clearing DTB. Q = equipment code+1, A = 3, Output instruction.

02 External reject when clearing DTB.

03 Internal reject - status function to 415. Q = equipment code+2, A = $620 Output instruction.

04 External reject - status function to 415.

05 End of operation interrupt from status function to 415 did not occur within 46.2 microseconds.

06 Internal reject - Input request to DTB. A = 0, Q = equipment code+$C, Output instruction.

07 External reject - input request to DTB.

08 Internal reject - input data (415 status) from DTB. A = 0, Q = equipment code, input request.

09 External reject - input data (415 status) from DTB.

0A Incorrect 415 status bit set.

0B 415 status - not ready.

0C 415 status - MS switch in 1604 position.

0D Internal reject - feed card function. A = $602, Q = equipment code+2, Output instruction.

0E External reject - feed card function.

0F Internal reject - output data to DTB-415. A = data, Q = equipment code+$A, Output instruction.

10 External reject - output data to DTB/415.

11 Internal reject - input DTB status. A = 0, Q = equipment code+1, input instruction.

12 External reject-input DTB status.

13 End of operation interrupt did not occur.

14 Internal reject - clear DTB function in interrupt state.

15 External reject - clear DTB function in interrupt state.

16 Interrupt occurred but DTB status bit (bit 2) not set.

17 Internal reject - input DTB status in interrupt state.

18 External reject - input DTB status in interrupt state.

19 DTB status bit set after a Clear Controller function.

II. DESCRIPTION

This test checks the proper operation of the 415 Card Punch attached to the DC215 Data Transfer Buffer using the AQ channel of the 1700 computer.

A. INITIALIZATION SECTION

1. Checks the proper connection of the DTB and the 415 Card Punch to the computer.
2. Status the 415 Card Punch for proper status at the beginning of the test.
3. Checks if interrupt from DTB at end of status function occurs correctly.

B. TEST SECTIONS

1. This test punches a deck which will be read by the 405 Card Reader under SMM17 Test 2F. (See description for Test No. 2F for explanation of the deck.) The user has the option to choose any combination of the test sections described. Also any single section may be chosen and cycled until the computer is manually stopped. Any single card may be cycled until the computer is stopped. These options are chosen at the parameter stop.
2. Each section sets up the cards, described in Test No. 2F in an 80-word buffer. The lower 12 bits of each word represent one column of a card (bit 0 = row 9, . . . , bit 11 = row 12). When the card is set up, the output routine is called. At the end of each section EOF routine is called. It will punch two end of file cards.

C. OUTPUT ROUTINE

1. The output routine transforms the 80-word column buffer to an 84 word row matrix. The row matrix consists of 12 sets of 7 words, where bits 11-0 of the first 6 words and bits 11-4 of the 7th word are the columns for that row. (See Reference/Instruction Manual for 170 Card Punch Controller, Figure 2-2.)

2. The routine then issues a Feed Card External function to the DTB. When this function has been accepted (End of Operation interrupt occurs) the 84 words of data are outputted. After each word of data is passed the routine waits until the end of operation interrupt occurs before passing the next word. For Section A the actual interrupt is checked. For Section B-J the M register is cleared so the interrupt does not come in. However, the DTB interrupt status bit (bit 2) is checked to see if the interrupt did occur.

3. Cycling Card

   After the card is punched, bit 12 of the test parameter is checked to see if a card is to be cycled. If so, the pattern number to be cycled is compared to the current card number. If they match, the card is cycled until the computer is stopped.

4. Repeating a Card

   If the card is not to be cycled, a counter is checked to see if the card is to be repeated a specific number of times. If it is to be repeated, the counter is decremented and the card is punched again. When punching of the current card pattern is complete, control is returned to the section which called the output routine.

D. INTERRUPTS

The test checks if interrupts from the DTB are working correctly in the initialization section when it inputs the 415 Card Punch status and when punching cards in Section A. When the interrupt comes in, the DTB interrupt status bit (bit 2) is checked and the interrupt is cleared. Control is returned to the test at the instruction where the interrupt occurred.

PONYA PARKING LOT DATA ACQUISITION AND REVENUE CONTROL SYSTEM (PNYA1A TEST NO. 1A)

I. INTRODUCTION

A. PURPOSE

This program was prepared as an off-line diagnostic for a Parking Lot Data Acquisition and Revenue Control System. The primary customer and immediate application is part of New York Authority contract. Specifically, this off-line program will be used for the following:

1. Prove the operation of all CDC supplied hardware for factory (Hopkins) test acceptance by the PONYA engineer. The external inputs and outputs to the 0202 terminal shall be via a CDC supplied simulator box. The remote TTY's will be wired directly to the 332-2 terminal adapter since the Bell 103F's will not be available.
2. Prove the hardware arrived in New York undamaged. This will involve exercising the complete system in the PONYA computer room without phone lines and using the simulator box.
3. Prove the terminals operate in the exit booths with the computer hardware system using phone line but still hooked to the simulator box.
4. Operate the exit lane per the off-line diagnostic program with the terminals connected to the lane hardware furnished by others. This will constitute hardware acceptance by PONYA and start the 30-day warranty period.
5. As a maintenance aid for the CDC customer engineer.

The test procedure and software program for 1, 2, and 3 above are identical. The only change is the physical location of the equipment. Items 2 and 3 can be handled somewhat less formally and are only required as a logical progression to item 4. The test procedure for item 4 will require changes because of the exit land hardware replacing the simulator box. Since CDC has no direct knowlege of the operation of the exit land hardware supplied by others, it is not CDC responsibility to formally revise the test procedure or provide a new procedure for this final test.

NOTE

For additional information on the remote terminal and its operational definition refer to the 0202 Reference Manual, Publication No. 65739900.

B. STANDARD COMPUTER EQUIPMENT

1. Memory Test, see SMM Reference Manual, Publication No. 60182000.
2. Random Protect Test, see SMM Reference Manual.
3. 1713 Teletype Test, see SMM Reference Manual.
4. Magnetic Tape Test, see SMM Reference Manual.
5. Buffer Data Channel Test see SMM Reference Manual.

C. LOCAL EQUIPMENT

1. Alarm Terminal Unit

   The Alarm Terminal Unit (ATU) has three alarm conditions and a clear function. All of these four functions are controllable by typing on the TTY or entering the appropriate parameter bits. All the program does is send the selected function. These functions are listed in Section C.

2. Time Emitter

   The Time Emitter makes time available to the computer. The following checks are made on the clock whenever the program is running:

   a. Time is brought in every interrupt. If minutes have changed, the new time will be processed and used as current computer time.

      1) If the time does not change in less than 2 minutes, a clock error is declared.

      2) If the time changes by more than 1 minute, except from 23:59 to 00:00, a clock error is declared.

D. REMOTE EQUIPMENT

The demonstration program consists of the following operations. The messages are defined below and they will be typed out on the selected TTY, either local or remote or both.

1. Request Keyin
2. Request Keyout
3. Request a fee from either the card reader or keyboard.

These operations may be changed for the purpose of the demonstration. The change occurs either by typing the appropriate information on the TTY or by entering the appropriate parameters at the entry stop at load time. The other operations that can be selected are:

1.	Request Lane Count	The response may be typed if the TTY is enabled.
2.	Request Status	The response may be typed.
3.	Send Lot Full	
4.	Send Clear Lot Full	
5.	Send Manual	
6.	Send Repeat	
7.	Send Terminal Master Clear	
8.	Send System Master Clear	
9.	Send System Ready	
10.	Send Fee Message	Retransmitted fee may be typed out on TTY.
11.	Send Display	Status message may be typed out on TTY.
12.	Send Data Poll	Response may be typed out on TTY.

II. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

Load SMM in the normal manner called out on page 90-1 of the SMM Reference Manual (Part III: Tests).

1. At Stop 1, enter bits into the A and Q registers as desired.
2. At Stop 2, enter into the A register "1A01". This represents the test number ("1A") and the frequency number ("01"). Enter into the Q register the 1749 equipment number, using bits 7 through 10.
3. Lower the SELECT JUMP switch. Place the RUN/STEP switch on RUN. The test will be called from the SMM tape.

B. ENTERING PARAMETERS

After the program has been loaded from the SMM tape, the program will stop (if selective stop bit 1 was set in SMM). At this point, parameters may be entered. See SMM Reference Manual, Parameter Stop. Parameters displayed are:

1. First Stop
   - A = Mux address for the selected remote terminal. Only the lower four bits are used.
   - Q = Mux equipment no. This is the same number as step A.2 above.
2. Second Stop
   - A = Mux address for the remote TTY.
   - Q = TAC. Refer to the PONYA list of addresses for the appropriate address.
3. Third Stop
   - A = Time, the time in binary form. This will be 12:00 (noon) at the beginning and will be updated by the system clock.
   - Q = Date, the date in binary form. This can be from 1 to 365.
4. Fourth Stop
   - A = First 16 bits of parameters.
   - Q = Second 16 bits of parameters.
5. Fifth Stop
   - A = Third 16 bits of parameters.
   - Q = Zero, nothing.
6. Sixth, Seventh, Eighth, Ninth, and Tenth, Stop
   - A and Q display TAC's for the nine possible terminals. These are the addresses that are polled, but the response is not processed.

After all the parameters are entered, cycle the RUN switch. The program will do whatever the parameters are set up for.

C. DEFINITION OF OPERATING PARAMETERS

The following operations can be set by changing the parameters at step C.2. above when the specified bit is set ("1"), or by entering the appropriate information on the TTY. The TTY format is "XX.", where "XX" equals any number from 01 to 99. The program will ignore any number outside the range of 01 to 99 and will ignore any unused number within that range. Typing a given number

will set a bit; typing that number plus one will clear the bit. For example, typing "01." will cause all messages to be typed; typing "02." will cause the typing to stop. If an error occurs, type a slash ("/") and start over.

1. A register bit "0" Type 01.

   Type all responses from remote other than EOT. Characters will be typed as a 2 hexadecimal digit representation.

2. A register bit "1" Type 03.

   Type all messages on local, 1711, 1712, or 1713 TTY.

3. A register bit "2" Type 05.

   Allow a normal polling sequence. This bit has to be = "0" before any other type, 21 or greater, operation can be performed.

4. A register bit "3". Type 07.

   Allow System Ready to be returned in response to a Keyin message from the remote terminal.

5. A register bit "4" Type 09.

   Allow Terminal Master Clear to be returned in response to a Keyout request from a remote terminal.

6. A register bit "5" Type 11.

   Allow a Fee Message to be returned in response to a Fee Request from a remote terminal.

7. A register bit "6" Type 13.

   Allow Display Fee to be sent in response to a Retransmitted Fee from a remote terminal

8. A register bit "7" Type 15.

   Loop on sending Fee Message. See note 1.

9. A register bit "S" Type 17.

   Loop on Fee Message, display sequence. See note 1.

10. A register bit "9" Type 19.

    Loop on Display Fee message. See note 1.

The following operations will occur only if polling is not allowed, bit "2" = 0 (clear) except as noted.

11. A register bit "10" Type 21.

    Request status from remote terminal.

12. A register bit "11" Type 23.

    Send Lot Full message to remote terminal.

13. A register bit "12" Type 25.

    Send Clear Lot Full message to remote terminal.

14. A register bit "13" Type 27.

    Send Manual Operate message to remote terminal.

15. A register bit "14" Type 29.

    Request Lane Count from remote terminal.

16. A register bit "15" Type 31.

    When doing an operation that inputs data, each message is compared to the previous message. If they do not compare, the message will be typed out.

17. Q register bit "0" Type 33.

    Send Repeat message to remote terminal.

18. Q register bit "1" Type 35.

    Send Terminal Master Clear message to remote terminal.

19. Q register bit "2" Type 37.

    Send System Master Clear message to remote terminal.

20. Q register bit "3" Type 39.

    Send System Ready message to remote terminal.

21. Q register bit "4" Type 41.

    Send Fee message to remote terminal.

22. Q register bit "5" Type 43.

    Send Display Fee message to remote terminal.

23. Q register bit "6" Type 45.

    Send Data Poll to remote terminal, do not process response.

24. Q register bit "7" Type 47.

    Set Power alarm at ATU.

25. Q register bit "8" Type 49.

    Set System alarm at ATU.

26. Q register bit "9" Type 51.

    Clear all alarms in ATU.

27. Q register bit "10" Type 53.

    Service Stall alarm every interrupt.

28. Q register bit "11" Type 55.

    Type Message Counter, used in conjunction with A register bit "15".

29. Q register bit "12" Type 57.

    Type Retransmitted Fee Error.

30. Q register bit "13" Type 59.

    Increment fee by $111.11 when not in Demo mode and A register bit "2" is set. If this bit is cleared, the fee will be increased by 1 instead.

D. MEANING OF TYPEOUTS

X = Character
CR = Carriage Return
LF = Line Feed

1. "CR, LF, KEYIN X.....X". X = data from badge readers, can be up to 22 characters or capital "B" for bypass.

   Definition: A keyin request was received from the remote terminal. The message was checked for character parity and message parity and no errors were found. System Ready was sent to the remote terminal. Status was requested from the remote terminal, and the "Ready" bit was set.

2. "CR, LF, KEYOUT X.....X". X = data from badge reader, can be up to 22 characters or capital "B" for bypass.

   Definition: Same requirements as for keyin except that Keyout FCC was received from the remote terminal, Terminal Master Clear was sent to the remote terminal, and the status bit for "Ready" was cleared.

3. "CR, LF, F.R. "X.....X". X = data from badge reader or bypass and keyboard or card reader can be up to 45 characters.

Definition: A fee request has been received from the remote terminal without BCC or parity error, date and time. The retransmitted fee has been received and compared with the fee with no errors detected.

4. "CR, LF, FEE $XXX.XX". X = 5 digit fee that was sent to remote terminal.

   Definition: This message occurs just after fee request message. Display fee has been sent to the remote terminal, the returned status bit checked, and the "Display" bit present. This fee sequence is complete.

5. "CR, LF, INCORRECT DAY"

   Definition: The date from the fee request was later than current date.

6. "CR, LF, INCORRECT TIME"

   Definition: The date from the fee request is the same as the computer date, but the time is later than the current computer time.

7. "CR, LF, TIME BAD"

   Definition: Time from the fee request was greater than 2359.

8. "CR, LF, DATE BAD"

   Definition: Date from the fee request was either zero or greater than 365.

9. "CR, LF, RETRANSMITTED FEE DID NOT COMPARE"

   Definition: The retransmitted fee did not compare with the fee sent to the remote terminal.

10. "CR, LF, CHAR. PARITY"

    Definition: A parity error was detected on a message received from the remote terminal.

11. "CR, LF, BCC-MESSAGE PARITY"

    Definition: The BCC character did not check with the data received from the remote terminal.

12. "CR, LF, LANECOUNTER XXXX XXXX XXXX XXXX"

    Definition: The lane count was requested from the remote terminal and has been received without BCC or parity error and 16 date characters were received. The message is then grouped into blocks of 4 digits for typeout.

13. "CR, LF, INCORRECT MESSAGE FORMAT"

    Definition: A message was received from the remote terminal that should have contained STX and ETX but did not.

14. "CR, LF, STATUS
    CR, LF, DISPLAY
    CR, LF, TEMP. FAULT
    CR, LF, LOT FULL
    CR, LF, MAINTENANCE
    CR, LF, MANUAL
    CR, LF, READY

    Definition: Status was requested from the remote terminal and this status character was received. Only those bits present in the status character will have their meaning typed out as part of the status message.

15. "CR, LF, INCORRECT MESSAGE LENGTH"

    Definition: Incorrect amount of data characters between STX and ETX.

16. "CR, LF, CLOCK ERROR"

    Definition: Either the clock did not advance in a 2 minute time period or advance by more than 1 minute.

17. "CR, LF, TIME XX:XX"

    Definition: X = correct time in the computer.

18. "CR, LF, OPER XX, XX, etc.

    Definition: XX, = the number typed on the TTY to set the selected parameter bits. The list of TTY numbers is elsewhere in this writeup.

E. PARITY ERROR

If a character has parity error, it will be followed by an arrow up instead of a space or blank. If BCC is found to be bad, a bracket will follow the BCC character.

F. CODE

TTY code is standard ASCII. The six FCC's possible from a remote terminal are special ASCII characters for this system:

61 Keyin
62 Keyout
63 Keyboard Fee Request
64 Card Reader Fee Request
65 Lane Counter Date
66 Retransmitted Fee

Status always has the status character first and can look like an FCC. In the status character, bit 2^6 will always be a "1".

G. CHECKOUT MODE TYPEOUT EXAMPLE

This is what a typical keyin would look like: "61 C1 86 02 C2 83 C1 04". These are the eight bits received from the remote terminal including parity and breakdown as follows:

61 FCC
C1 TAC
86 ACK
02 STX
C2 Date, capital "B" for bypass
03 ETX
C1 BCC
04 EOT

II. REMOTE TTY DIAGNOSTIC TYPEOUTS

A. NORMAL TTY MESSAGE

1. PONYA Remote TTY Diagnostic.
2. Sliding pattern, 10 lines.
3. Two lines of worst case pattern "U*".
4. Two lines of worst case pattern "F=".
5. Type in random data. Type slash to repeat section. Type period to end section.
6. Read in and type out answer back drum.
7. TTY SW. TEST X Exercise remote TTY switch.
8. End of test.

B. ERROR MESSAGES TYPED ON LOCAL TTY

1. Unexpected Character Lost
2. Unexpected Break
3. No Character Required

4. Unexpected Character Ready
5. Input Reject
6. Output Reject

III. FLOW CHARTS

A. The program flow chart is as follows:

The first task is all the various initialization steps. After initialization, the program will start cycling, using the various parameters entered during initialization to direct its operations.

1. IDLE is where the spare time between interrupts is spent. When an interrupt occurs, the program will go to INTERR.
2. INTERR communicates with the Mux addresses for input and output as appropriate. This includes inputting or outputting to the remote TTY's, outputting to the ATU as appropriate, and bringing in time from the clock. Control is then passed to PROC.
3. PROC is an executive routine of sorts; it controls whether to go ahead with the next operation or wait until the present operation is complete. Exits from PROC can be to: IDLE if an operation is still in progress; PROCTT (4) if there is a message from the TTY to process; EXCTWO (9) if normal polling is not allowed; TTXFER (12) if there is a message to type on the TTY and if in Checkout mode; BIT0 (a regular POLL) is to occur next; or PROCME (5). The clock is processed via a return jump if minutes have changed.
4. PROCTT takes the input message from the TTY, analyzes it, ignores it if illegal, or jumps to the subroutine specified by that request. TTYTAB is a table of addresses to various subroutines, the numbers can range from 01 to 99 decimal.
5. PROCME determines what kind of information was received from the remote terminal and passes control to that routine. If 10 consecutive messages are received that have an illegal FCC, a Terminal Master Clear will be sent to that terminal.
6. KEYIN sends a System Ready to the terminal and if in Demo mode. It also checks status to see that the station did in fact become Ready.
7. KEYOUT is about the same as KEYIN, except that it is a keyout.

8. FEEREQ processes either a Card Reader or Keyboard Fee request. The date format has to be the same for both. If in Checkout mode, the fee will be incremented by $.01 or $111.11 as appropriate. The fee sequence is executed with no date/time validation or status checking at all. If in the Demo mode, all messages are checked for character parity and BCC as appropriate. Fee request data/time are checked, a fee is computed and sent to the terminal, the retransmitted fee is checked, a Display is sent, and Status is checked to ensure there is a display. Errors detected cause a Repeat to be sent to the terminal and an appropriate error message to be typed on the TTY. If a Fee request is valid, the Fee request data from the remote terminal and the fee will be typed on the TTY.

9. EXCTWO is the part of the program which allows individually controllable messages to be sent to the terminal. These operations are controlled by the bits set in OPMASK, OPMASA, and OPMASI.

10. COMPAR is a subroutine which compares an input message to the previous message and if any bits have changed, the whole message and message number can be typed. This routine is useful when checking the consistency of a message.

11. XFER transfers a message from its place in core to the output bin for the terminal. Parity and BCC are generated during the transfer as appropriate Also, a fee message can be manipulated to cause errors if desired.

12. TTXFER takes an input message from a terminal and breaks each character up into two hexadecimal characters for the TTY. Each character is checked for odd parity and whether or not there is a parity error instead of a blank or space following the two hexadecimal character representation. If so, an arrow up will be inserted. If a BCC error is detected, a bracket will be inserted after the BCC character instead of the blank or arrow up.

13. POLALL is entered from the IDLE routine once each interrupt, if there is time. This routine issues a poll to all addresses in the Mux cabinet, except the one which is in use by the rest of the program. About once a second or slightly more often, each address in the Mux will be polled. If a Mux address will not accept a poll, the program will go on to the next address. No use is made of the response to the poll.

14. PTT01 through PTT99 are various requests that can be made via the TTY. Most of these routines only set or clear bits in OPMASK, OPMASA, or OPMASI. OPMASK, OPMASA, and OPMASI are parameter words where each bit has its own meaning.

15. CPARITY checks character parity for Demo mode.

16. BCCCK checks BCC for error when in Demo mode.

17. PROCLK processes the new time from the clock. Time is checked for the following three items.

    a. When it advances, it advances by only 1 minute.

    b. If time should decrement, it travels from 23:59 to 00:00 only.

    c. Minutes advance at least once each elapsed minute.

    If any of the above are found to be in error, a message is typed on the TTY.

B. REMOTE TTY DIAGNOSTIC

1. TTYD is the remote TTY diagnostic.

    a. The first operation is to type the heading on the local and then the remote TTY.

    b. Status of the remote is checked about 32000 times.

    c. Ten lines of sliding pattern are typed.

    d. Two lines of worst case pattern "U*" are typed.

    e. Two lines of worst case pattern "F=" are typed.

    f. Type lines with increasing number of spaces followed by "CR".

    g. Request input of random data. Input till either a ".", "/", or 1 minute. Type data inputted. If there was a "/", repeat section.

    h. Request answer back drum.

    i. Type answer back drum information.

    j. Do the above operations on the other remote TTY.

    k. Cause switch to other remote TTY and type switch message.

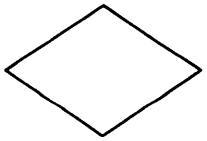
    l. Type END OF TEST on both remote TTY's.

    m. Return to polling remote parking lot terminal program. A clock error may occur but it is not an actual clock error.

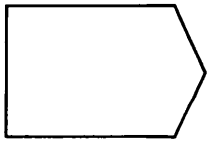
SYMBOL MEANING TABLE

AN OPERATION

DECISION

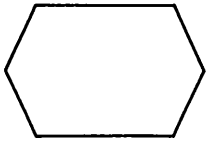


PROGRAM MODIFICATION

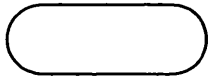


LOGIC CONNECTOR OFF PAGE

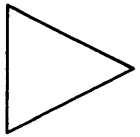
RETURN JUMP TO A SUBROUTINE



SUBROUTINE



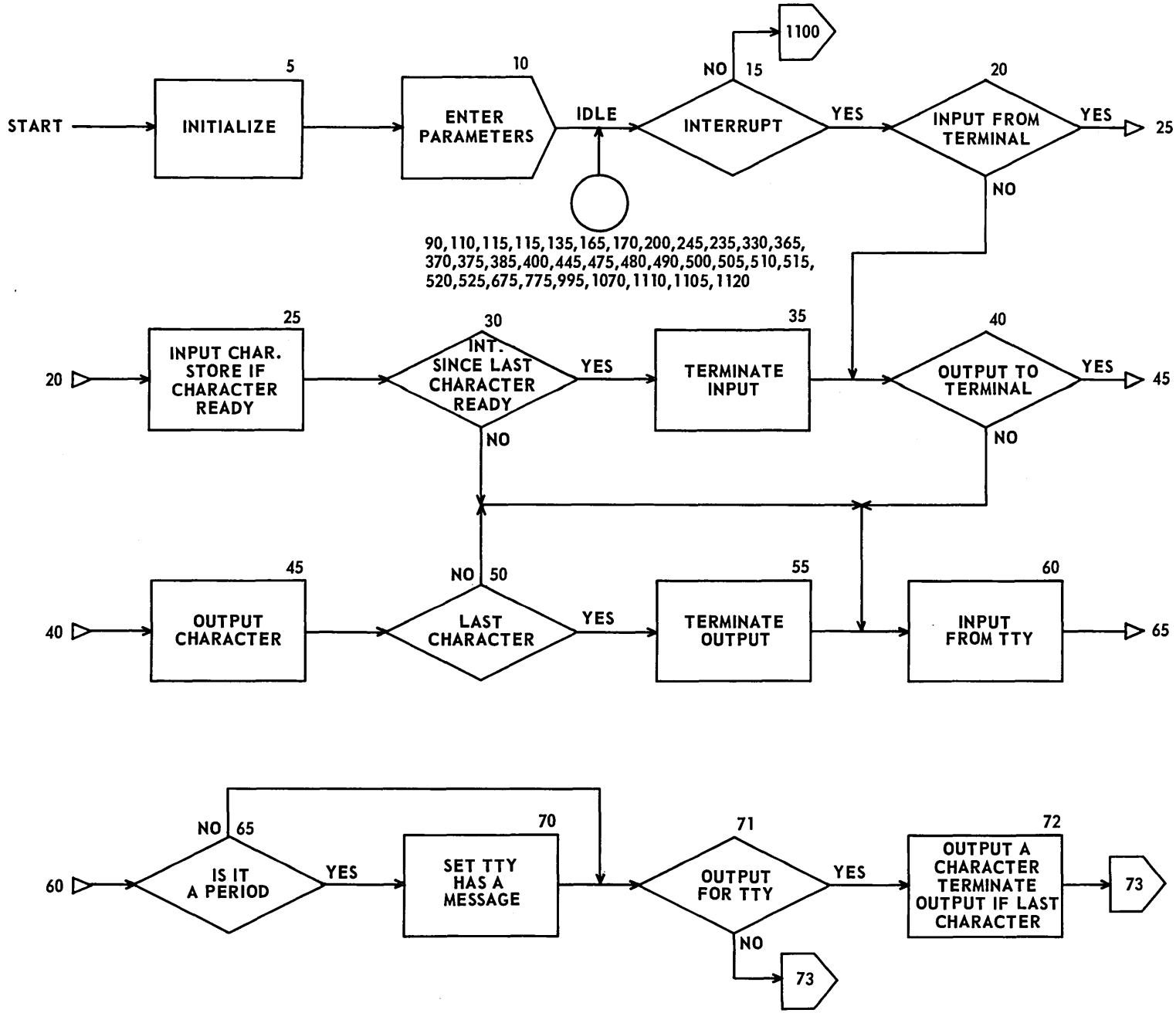
JUMP TO A SUBROUTINE

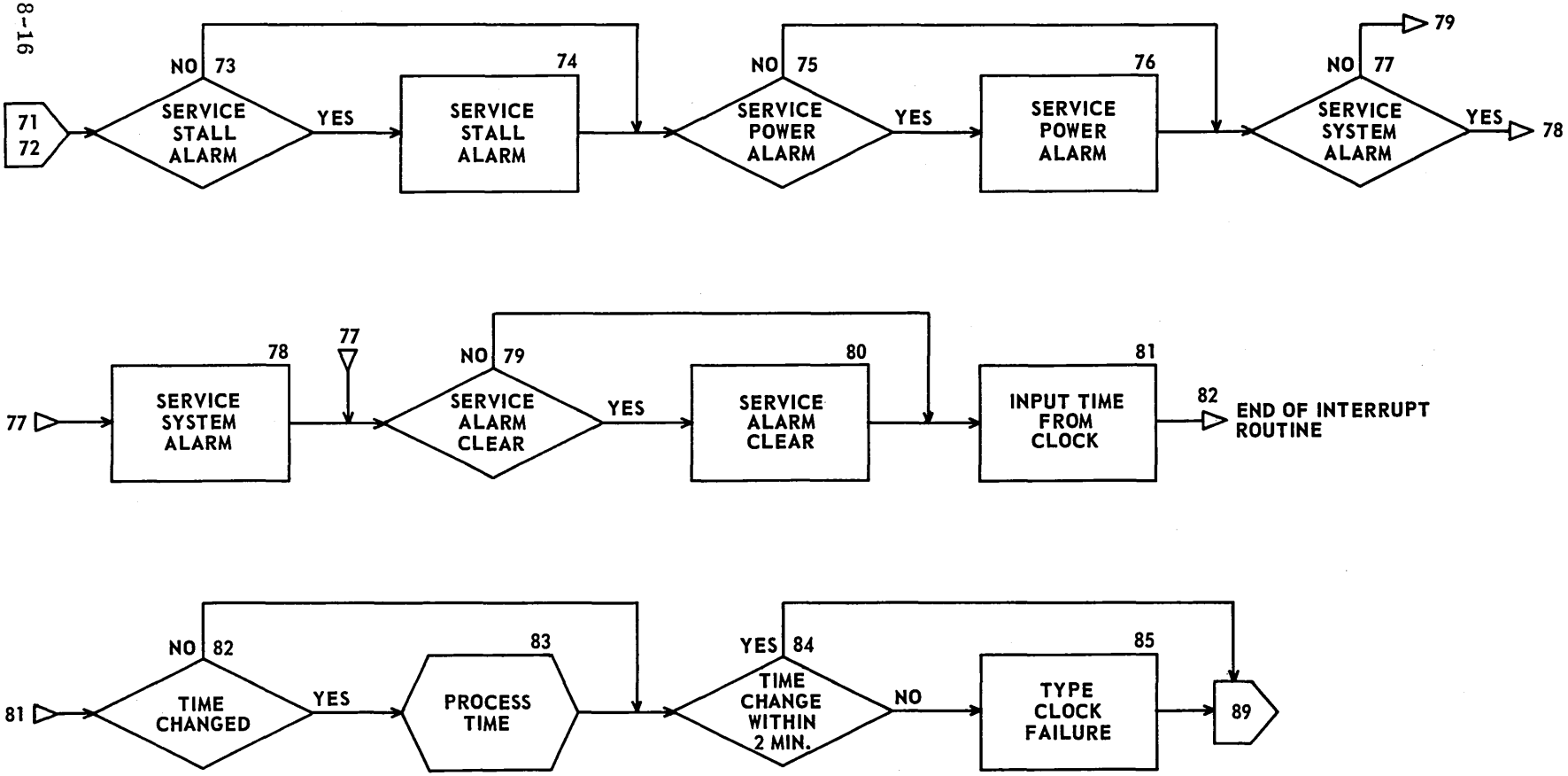


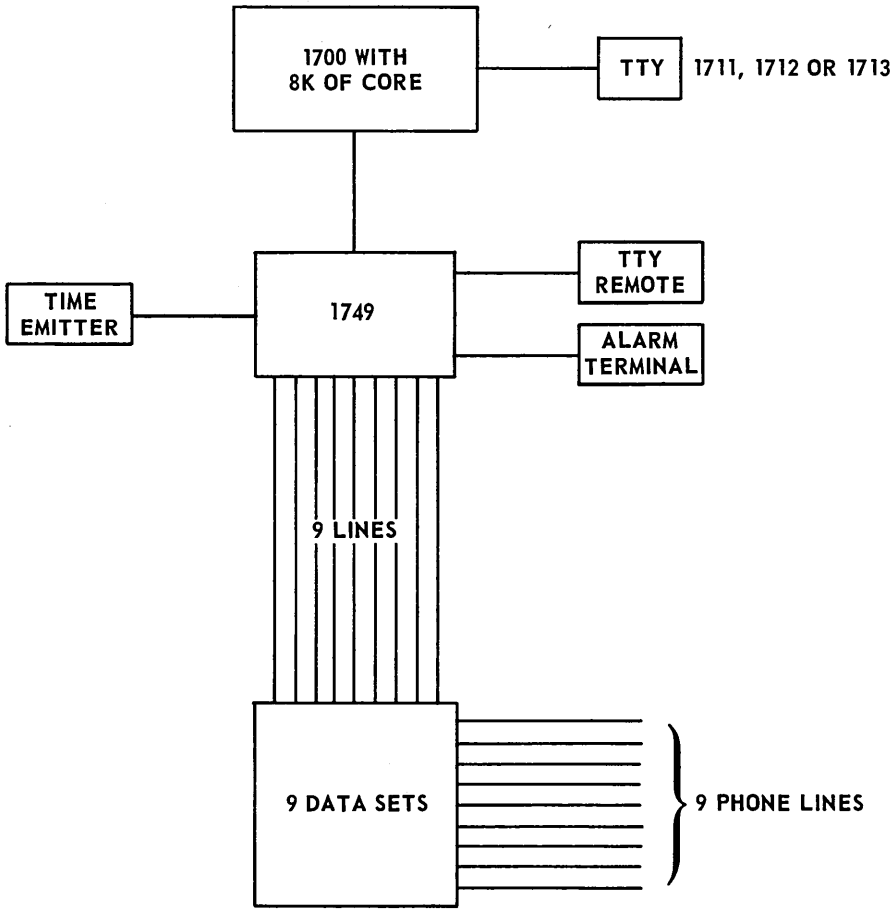
OFF PAGE CONNECTOR

LINE CONNECTORS

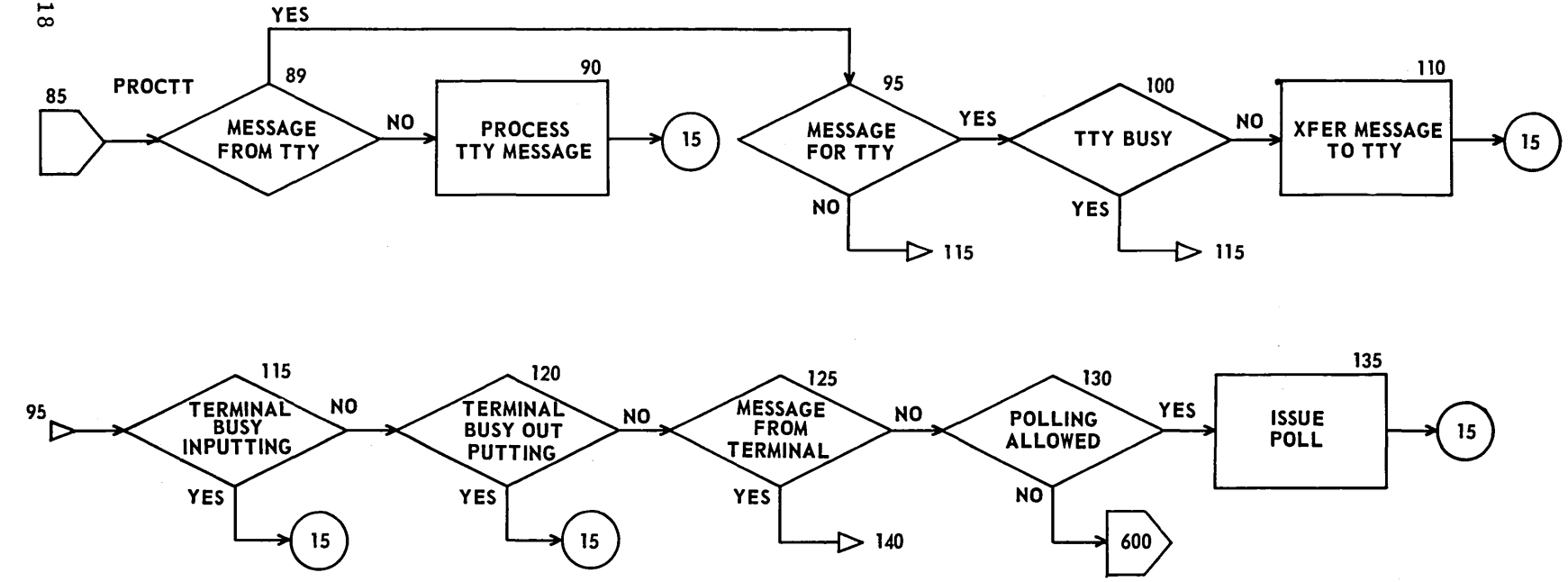
PROGRAM FLOW IS FROM TOP TO BOTTOM, LEFT TO RIGHT UNLESS OTHERWISE NOTED.


START
INITIALIZE
5
ENTER PARAMETERS
10
IDLE
INTERRUPT
15
NO
1100
YES
INPUT FROM TERMINAL
20
YES
25
NO
90,110,115,115,135,165,170,200,245,235,330,365,
370,375,385,400,445,475,480,490,500,505,510,515,
520,525,675,775,995,1070,1110,1105,1120
20
INPUT CHAR. STORE IF CHARACTER READY
25
INT. SINCE LAST CHARACTER READY
30
YES
TERMINATE INPUT
35
OUTPUT TO TERMINAL
40
YES
45
NO
NO
40
OUTPUT CHARACTER
45
LAST CHARACTER
50
NO
YES
TERMINATE OUTPUT
55
INPUT FROM TTY
60
65
60
IS IT A PERIOD
65
NO
YES
SET TTY HAS A MESSAGE
70
OUTPUT FOR TTY
71
YES
NO
73
OUTPUT A CHARACTER TERMINATE OUTPUT IF LAST CHARACTER
72
73

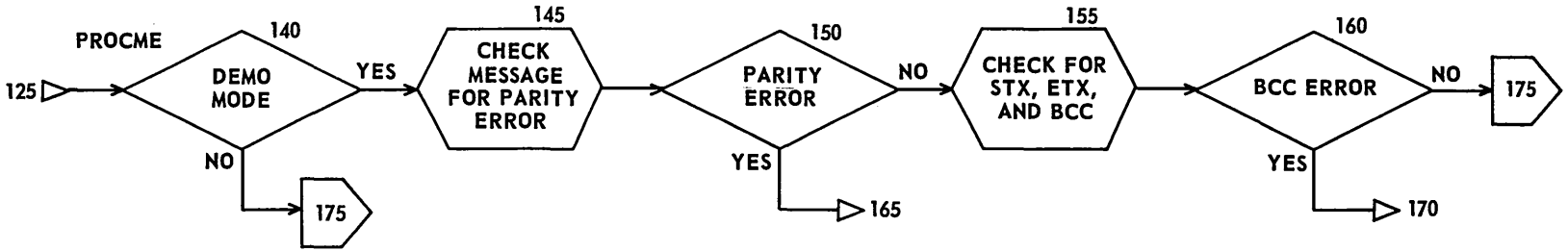

71
72
NO
73
SERVICE STALL ALARM
YES
74
SERVICE STALL ALARM
NO
75
SERVICE POWER ALARM
YES
76
SERVICE POWER ALARM
NO
77
SERVICE SYSTEM ALARM
YES
78
79
77
78
SERVICE SYSTEM ALARM
77
NO
79
SERVICE ALARM CLEAR
YES
80
SERVICE ALARM CLEAR
81
INPUT TIME FROM CLOCK
82
END OF INTERRUPT ROUTINE
81
NO
82
TIME CHANGED
YES
83
PROCESS TIME
YES
84
TIME CHANGE WITHIN 2 MIN.
NO
85
TYPE CLOCK FAILURE
89



MINIMUM SYSTEM THAT THE PROGRAM WAS WRITTEN FOR. THE PROGRAM WILL OPERATE WITH SOME COMPONENTS REMOVED, SUCH AS: TIME EMITTER, REMOTE OR LOCAL TTY, 8 MODEM ADAPTERS AND THE ATU.

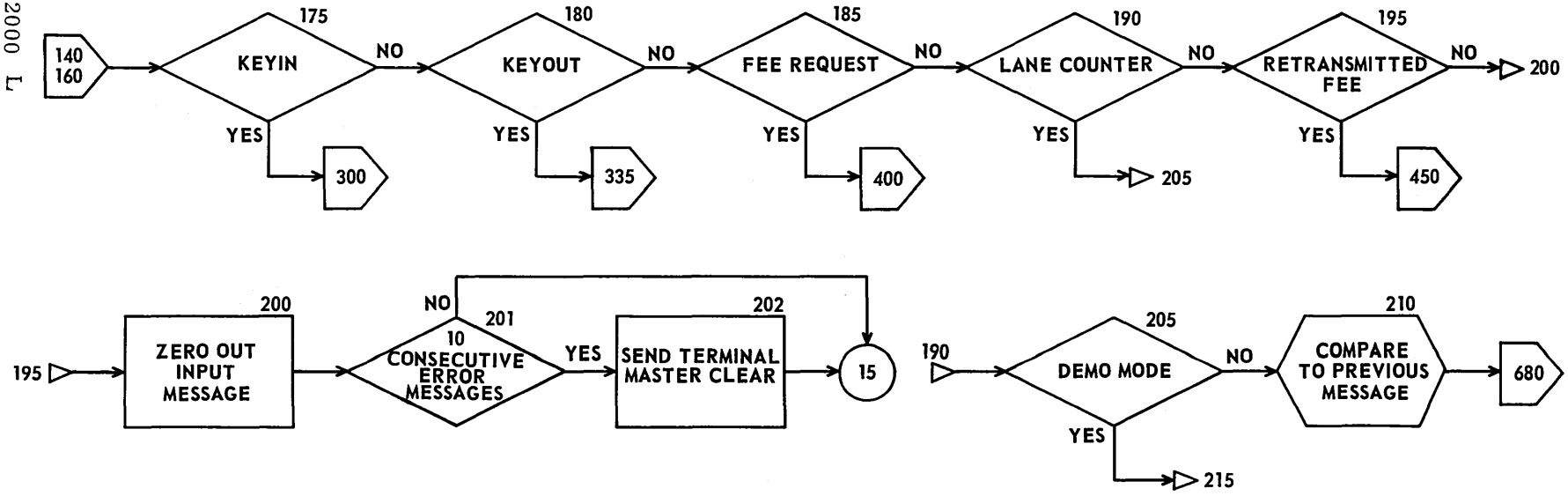

PROCTT
85
89
MESSAGE FROM TTY
NO
90
PROCESS TTY MESSAGE
15
YES
95
MESSAGE FOR TTY
YES
100
TTY BUSY
NO
110
XFER MESSAGE TO TTY
15
NO
115
YES
115

95
115
TERMINAL BUSY INPUTTING
NO
120
TERMINAL BUSY OUT PUTTING
NO
125
MESSAGE FROM TERMINAL
NO
130
POLLING ALLOWED
YES
135
ISSUE POLL
15
YES
15
YES
15
YES
140
NO
600

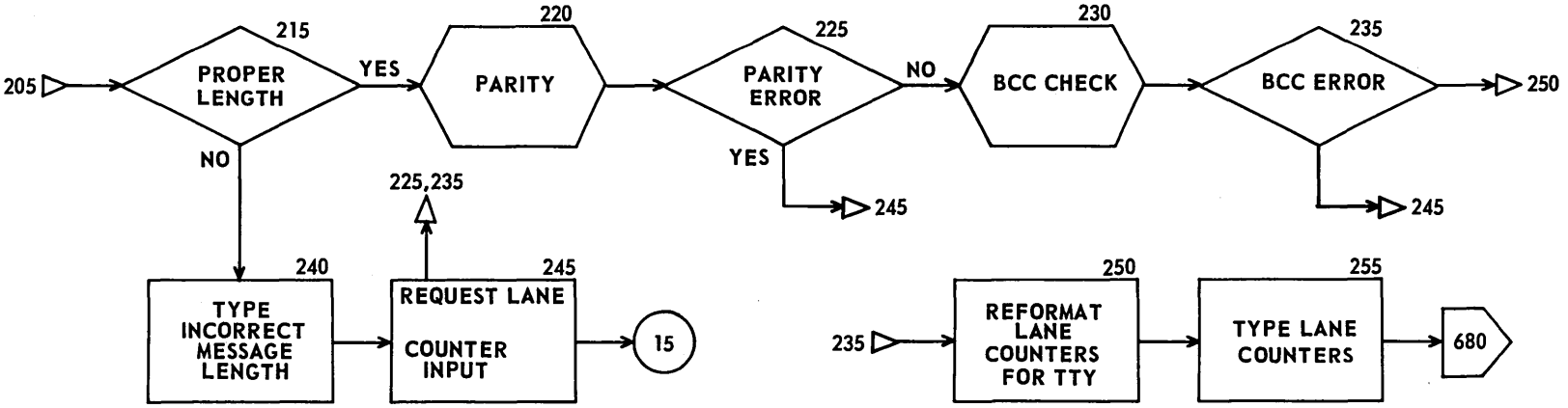

PROCME
125
140
DEMO MODE
YES
145
CHECK MESSAGE FOR PARITY ERROR
150
PARITY ERROR
NO
155
CHECK FOR STX, ETX, AND BCC
160
BCC ERROR
NO
175
NO
175
YES
165
YES
170

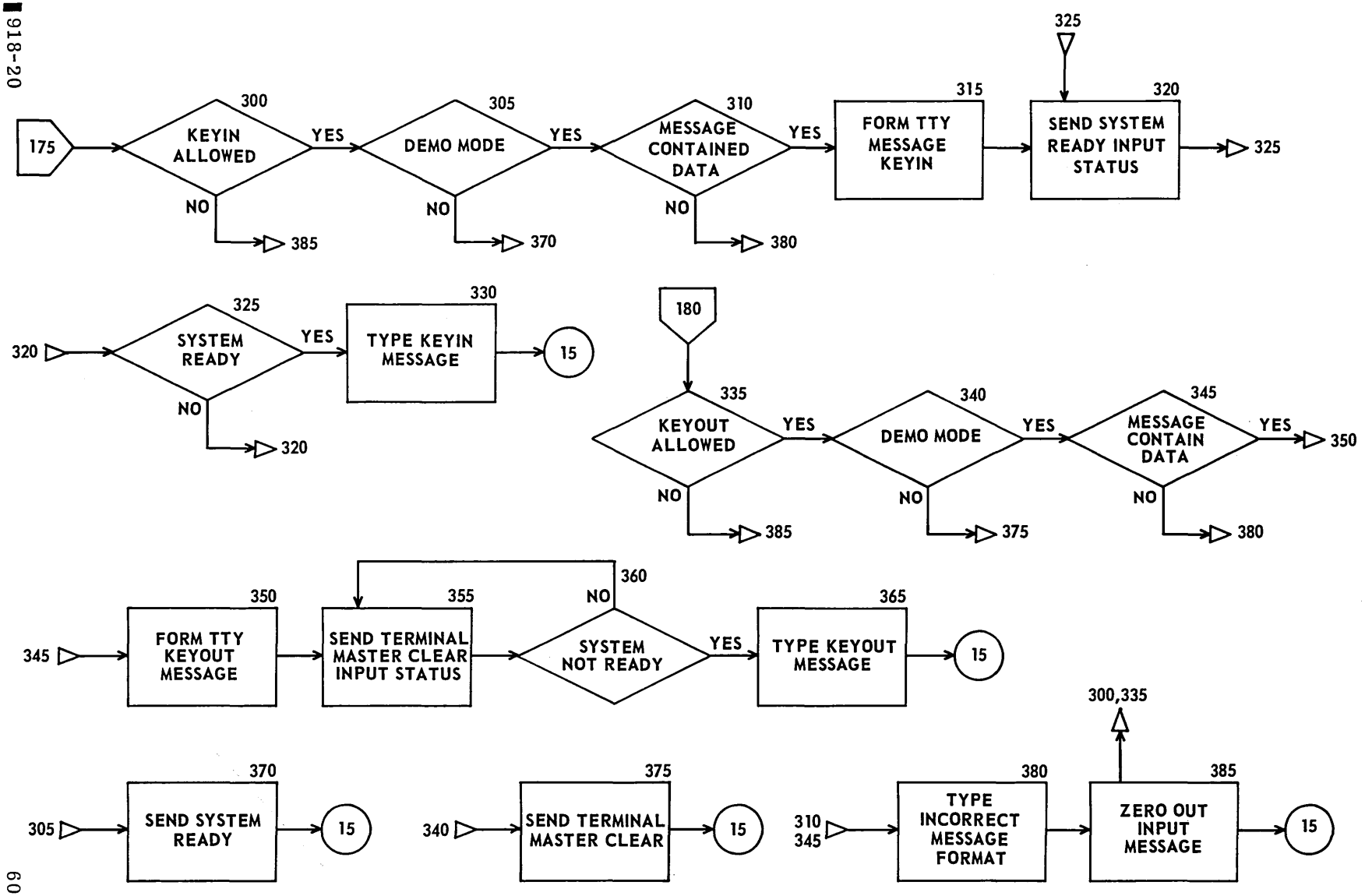
150
165
TYPE CHARACTER PARITY
15
160
170
TYPE BCC-MESSAGE PARITY
15

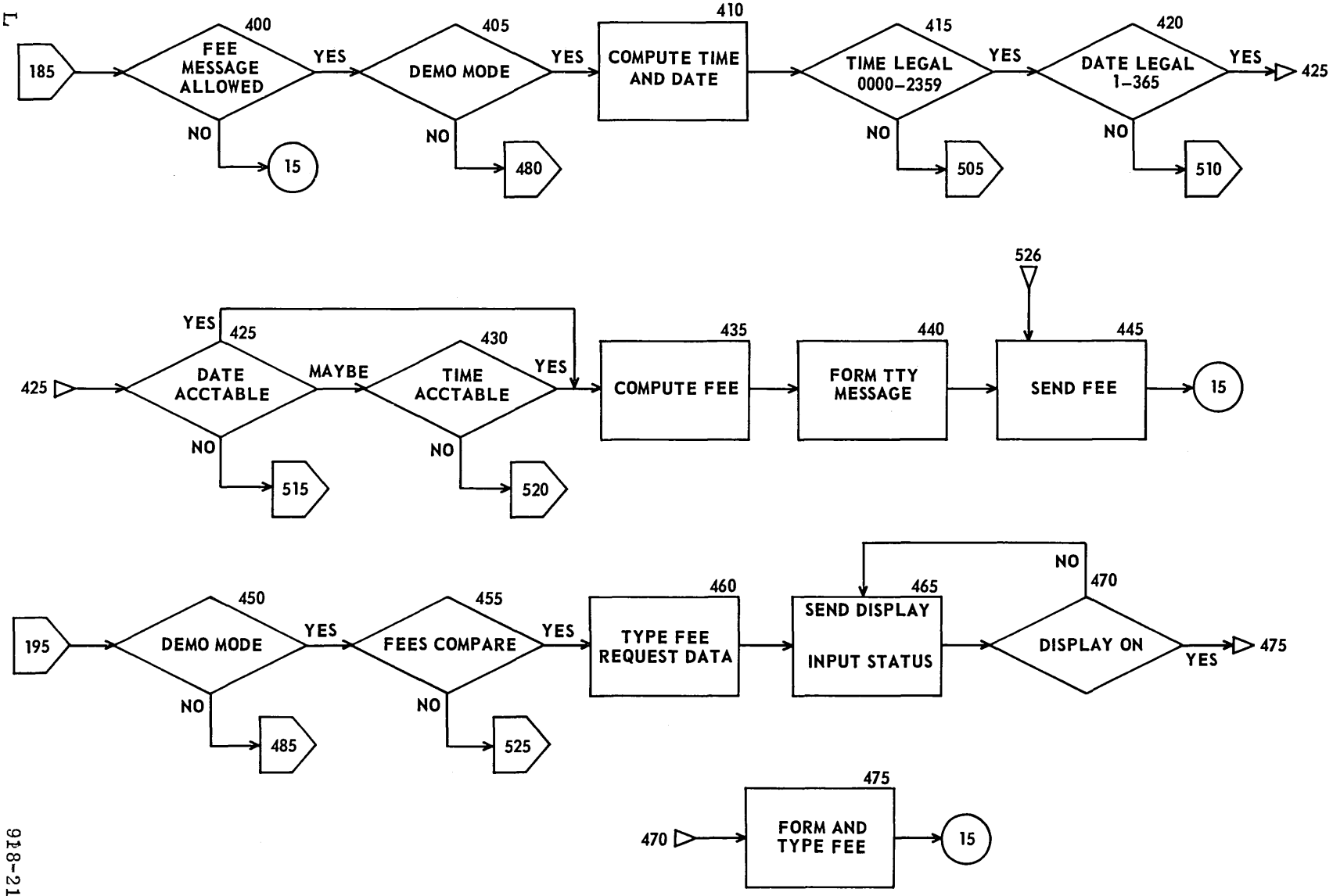
60182000 L

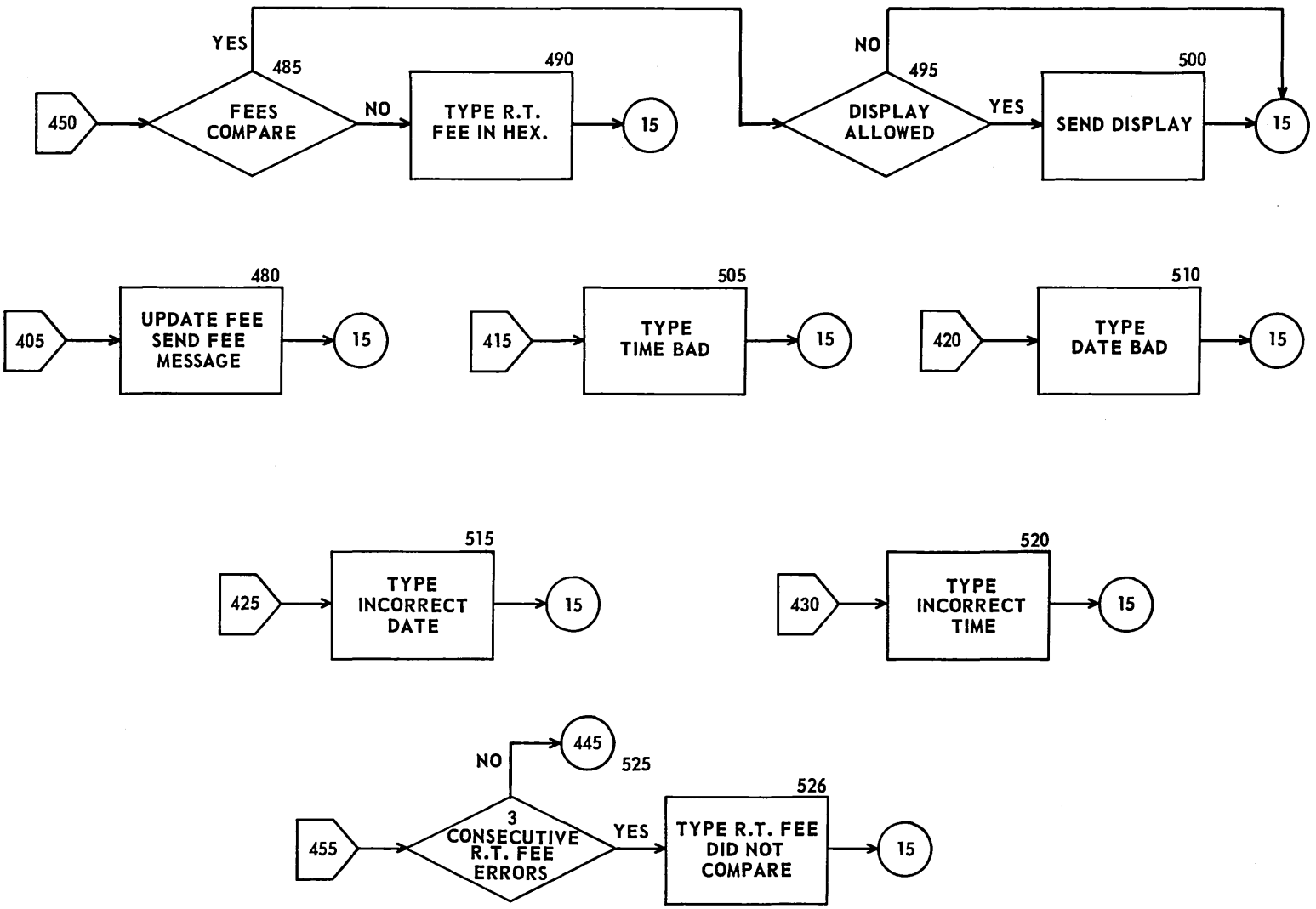

140
160
175
KEYIN
NO
YES
300
180
KEYOUT
NO
YES
335
185
FEE REQUEST
NO
YES
400
190
LANE COUNTER
NO
YES
205
195
RETRANSMITTED FEE
NO
200
YES
450

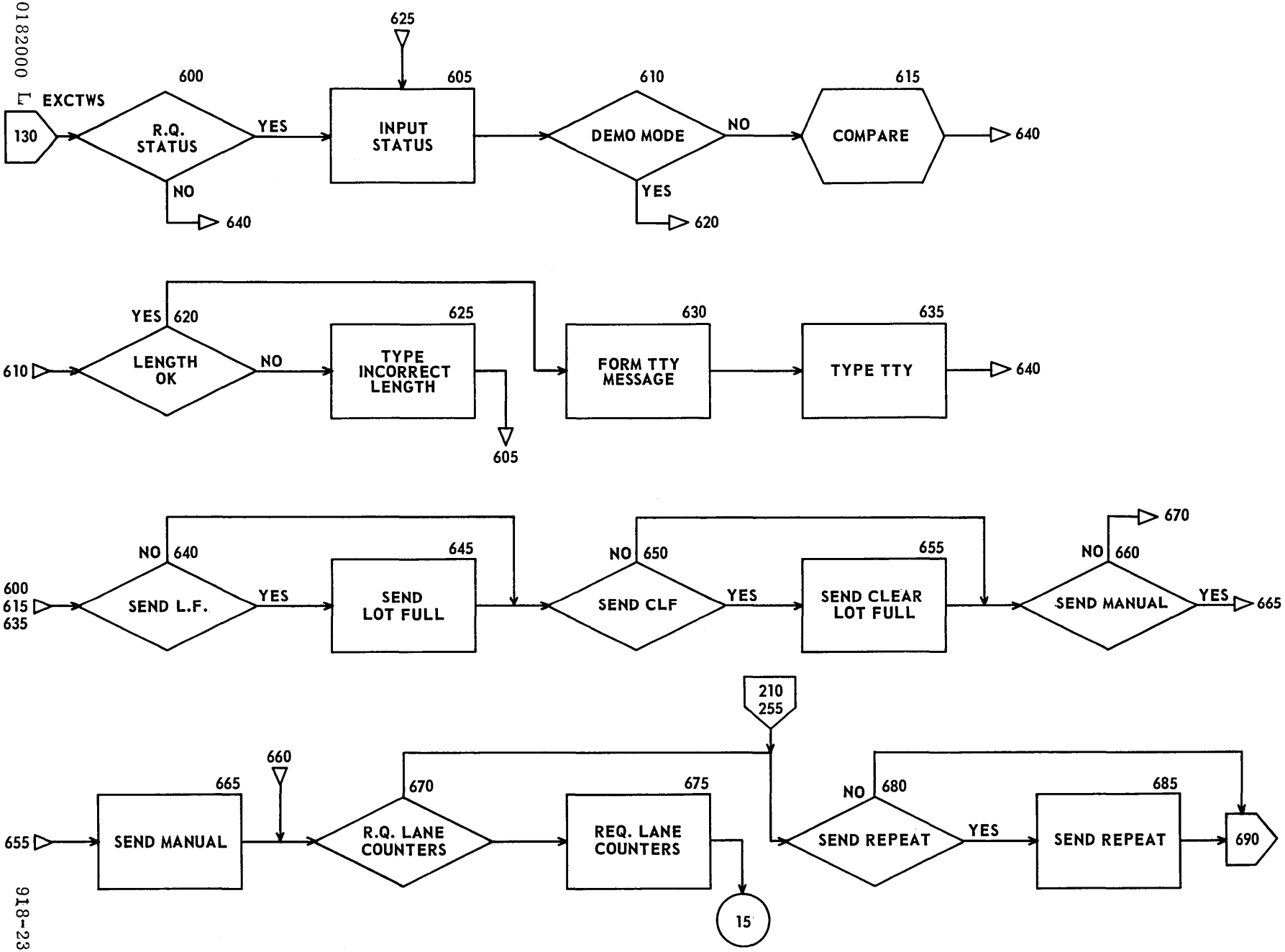
195
200
ZERO OUT INPUT MESSAGE
NO
201
10 CONSECUTIVE ERROR MESSAGES
YES
202
SEND TERMINAL MASTER CLEAR
15
190
205
DEMO MODE
NO
YES
215
210
COMPARE TO PREVIOUS MESSAGE
680

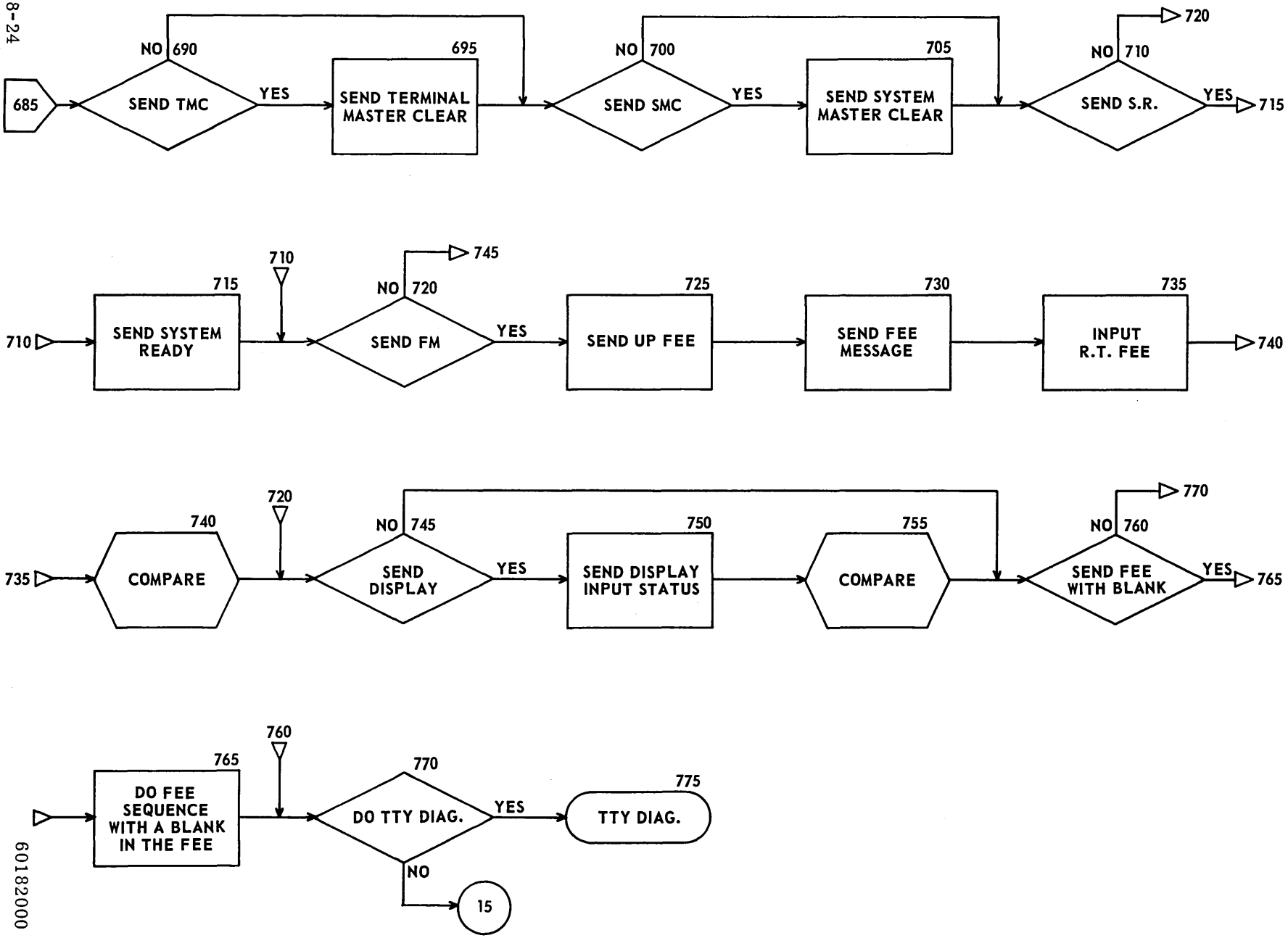

205
215
PROPER LENGTH
YES
NO
220
PARITY
225
PARITY ERROR
NO
YES
245
230
BCC CHECK
235
BCC ERROR
250
245
225,235
240
TYPE INCORRECT MESSAGE LENGTH
245
REQUEST LANE COUNTER INPUT
15
235
250
REFORMAT LANE COUNTERS FOR TTY
255
TYPE LANE COUNTERS
680


175
300
KEYIN ALLOWED
YES
NO
385
305
DEMO MODE
YES
NO
370
310
MESSAGE CONTAINED DATA
YES
NO
380
315
FORM TTY MESSAGE KEYIN
325
320
SEND SYSTEM READY INPUT STATUS
325
320
325
SYSTEM READY
YES
NO
320
330
TYPE KEYIN MESSAGE
15
180
335
KEYOUT ALLOWED
YES
NO
385
340
DEMO MODE
YES
NO
375
345
MESSAGE CONTAIN DATA
YES
NO
380
350
345
350
FORM TTY KEYOUT MESSAGE
355
SEND TERMINAL MASTER CLEAR INPUT STATUS
360
NO
SYSTEM NOT READY
YES
365
TYPE KEYOUT MESSAGE
15
300,335
305
370
SEND SYSTEM READY
15
340
375
SEND TERMINAL MASTER CLEAR
15
310
345
380
TYPE INCORRECT MESSAGE FORMAT
385
ZERO OUT INPUT MESSAGE
15

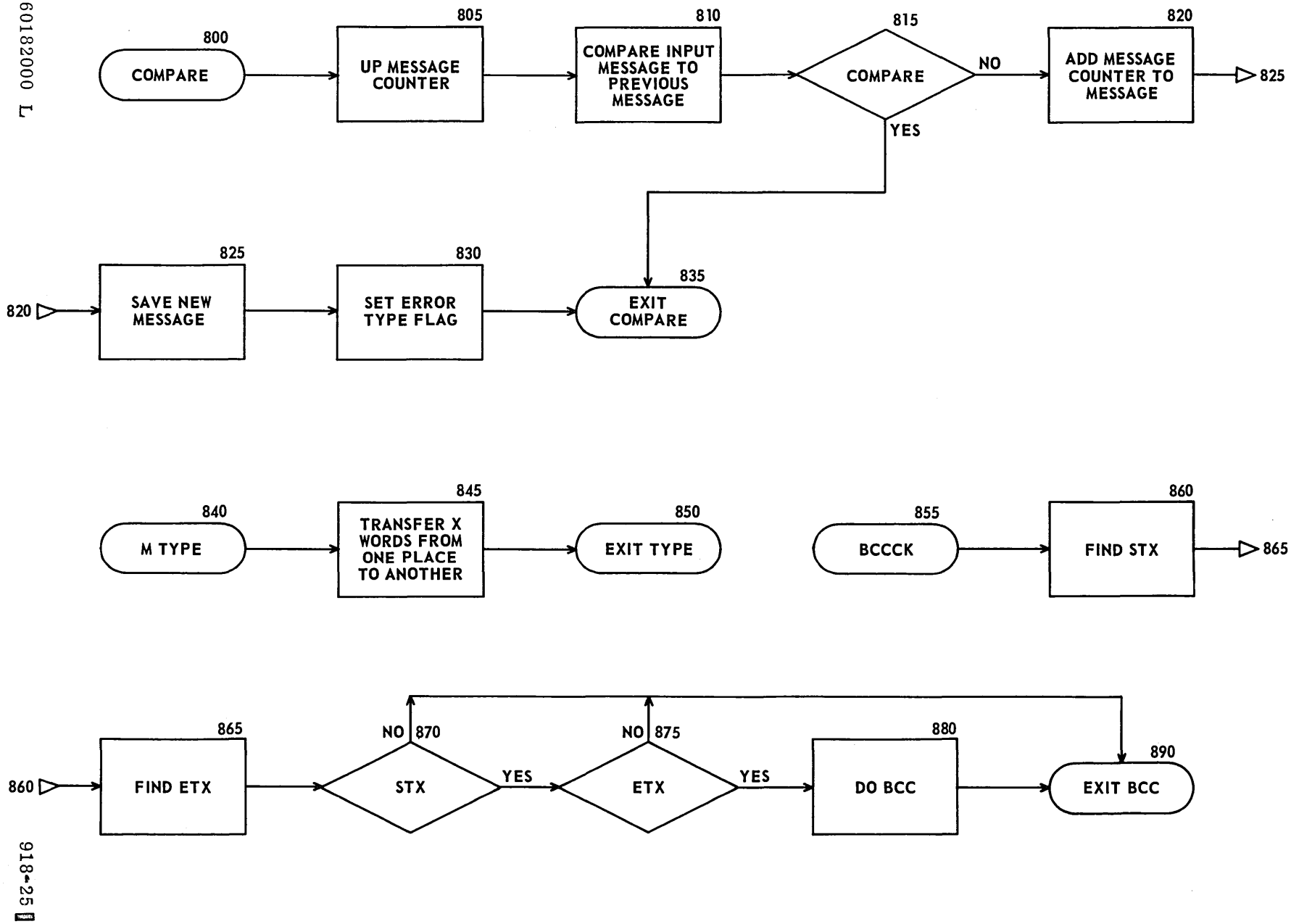

185
400
FEE MESSAGE ALLOWED
YES
NO
15
405
DEMO MODE
YES
NO
480
410
COMPUTE TIME AND DATE
415
TIME LEGAL 0000–2359
YES
NO
505
420
DATE LEGAL 1–365
YES
425
NO
510
526
425
425
DATE ACCTABLE
YES
MAYBE
NO
515
430
TIME ACCTABLE
YES
NO
520
435
COMPUTE FEE
440
FORM TTY MESSAGE
445
SEND FEE
15
195
450
DEMO MODE
YES
NO
485
455
FEES COMPARE
YES
NO
525
460
TYPE FEE REQUEST DATA
465
SEND DISPLAY INPUT STATUS
NO
470
DISPLAY ON
YES
475
470
475
FORM AND TYPE FEE
15


450
485
FEES COMPARE
YES
NO
490
TYPE R.T. FEE IN HEX.
15
NO
495
DISPLAY ALLOWED
YES
500
SEND DISPLAY
15
405
480
UPDATE FEE SEND FEE MESSAGE
15
415
505
TYPE TIME BAD
15
420
510
TYPE DATE BAD
15
425
515
TYPE INCORRECT DATE
15
430
520
TYPE INCORRECT TIME
15
455
3 CONSECUTIVE R.T. FEE ERRORS
NO
445
525
YES
526
TYPE R.T. FEE DID NOT COMPARE
15

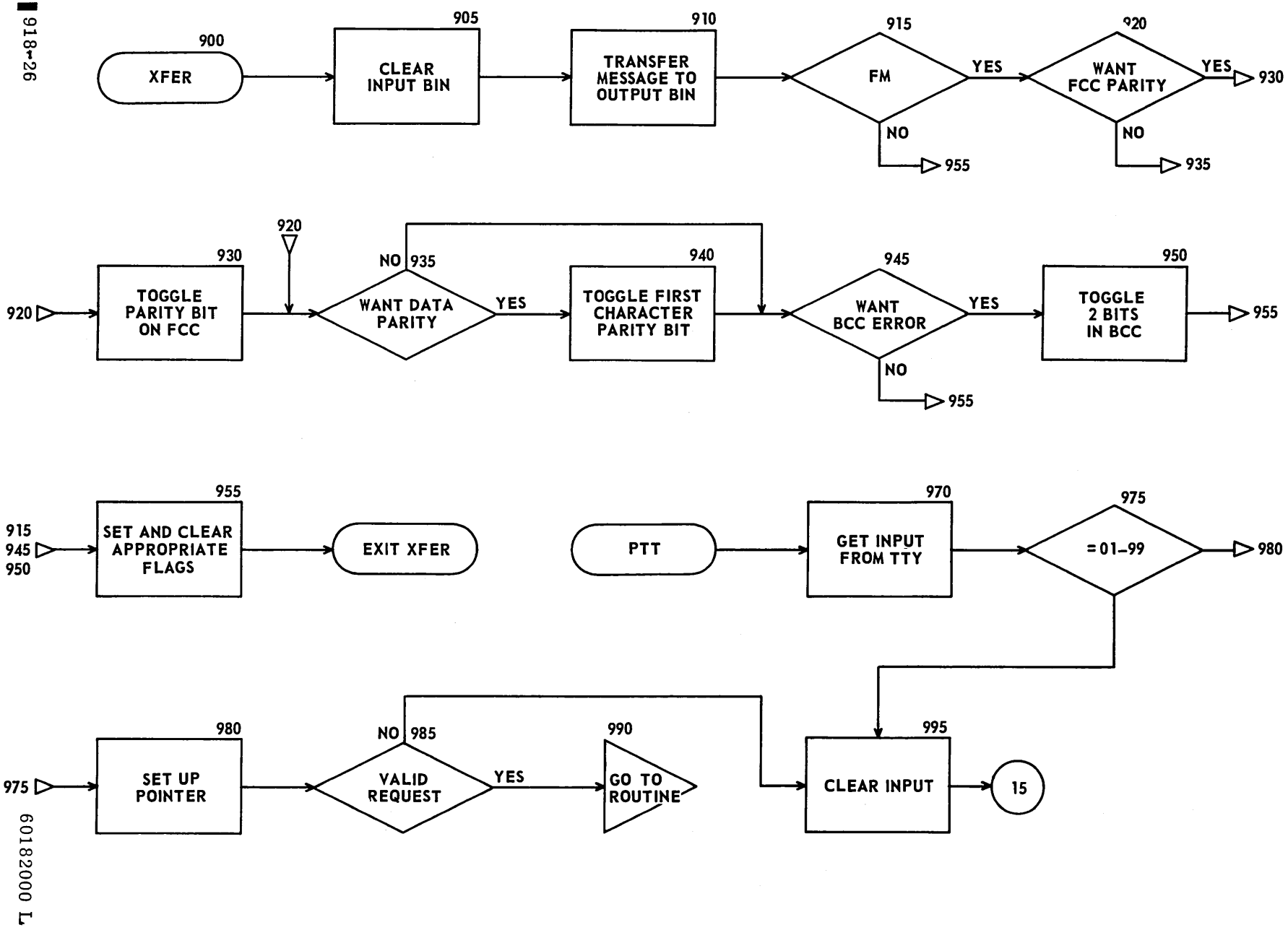

625
600
605
610
615
EXCTWS
130
R.Q. STATUS
YES
INPUT STATUS
DEMO MODE
NO
COMPARE
640
NO
YES
620
640
YES 620
625
630
635
610
LENGTH OK
NO
TYPE INCORRECT LENGTH
FORM TTY MESSAGE
TYPE TTY
640
605
NO 640
645
650
655
660
670
600
615
635
SEND L.F.
YES
SEND LOT FULL
NO 650
SEND CLF
YES
SEND CLEAR LOT FULL
NO 660
SEND MANUAL
YES
665
210
255
660
665
670
675
680
685
655
SEND MANUAL
R.Q. LANE COUNTERS
REQ. LANE COUNTERS
NO 680
SEND REPEAT
YES
SEND REPEAT
690
15

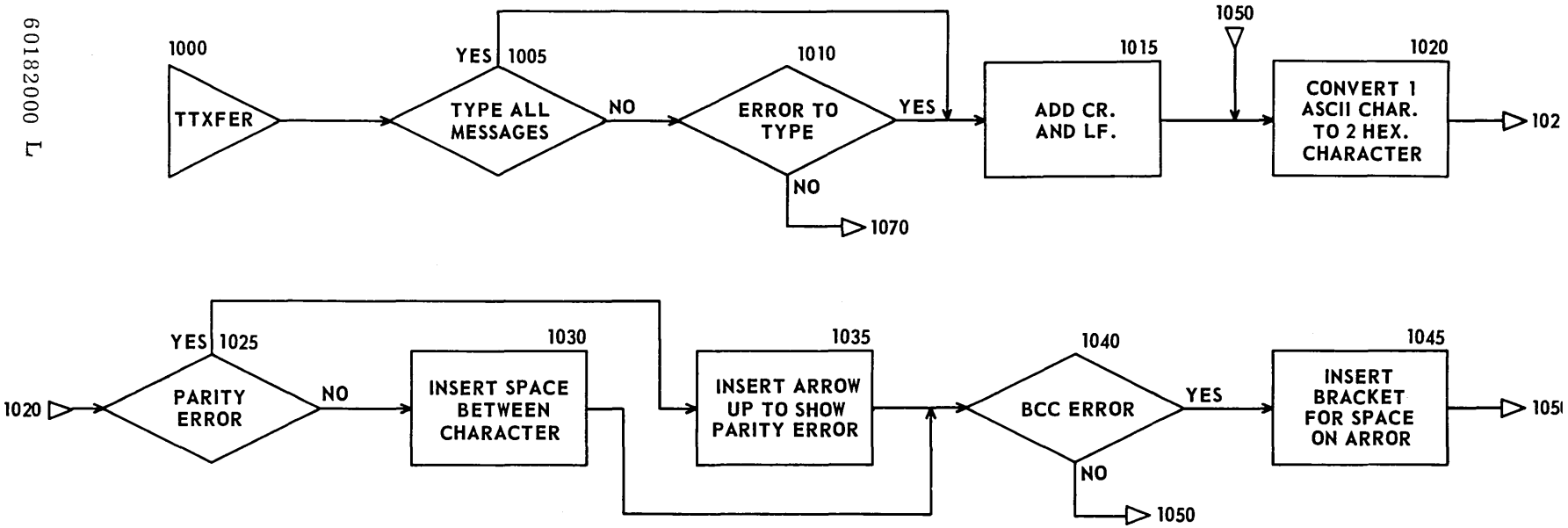

685
690
NO
SEND TMC
YES
695
SEND TERMINAL MASTER CLEAR
700
NO
SEND SMC
YES
705
SEND SYSTEM MASTER CLEAR
720
710
NO
SEND S.R.
YES
715
710
715
SEND SYSTEM READY
710
745
720
NO
SEND FM
YES
725
SEND UP FEE
730
SEND FEE MESSAGE
735
INPUT R.T. FEE
740
735
740
COMPARE
720
745
NO
SEND DISPLAY
YES
750
SEND DISPLAY INPUT STATUS
755
COMPARE
770
760
NO
SEND FEE WITH BLANK
YES
765
760
765
DO FEE SEQUENCE WITH A BLANK IN THE FEE
770
DO TTY DIAG.
YES
775
TTY DIAG.
NO
15

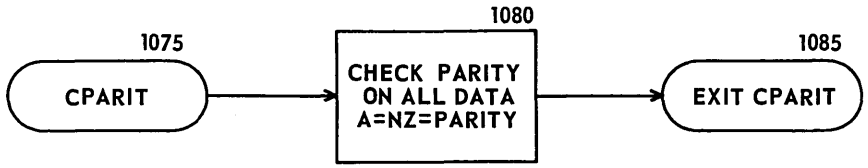
60182000 L

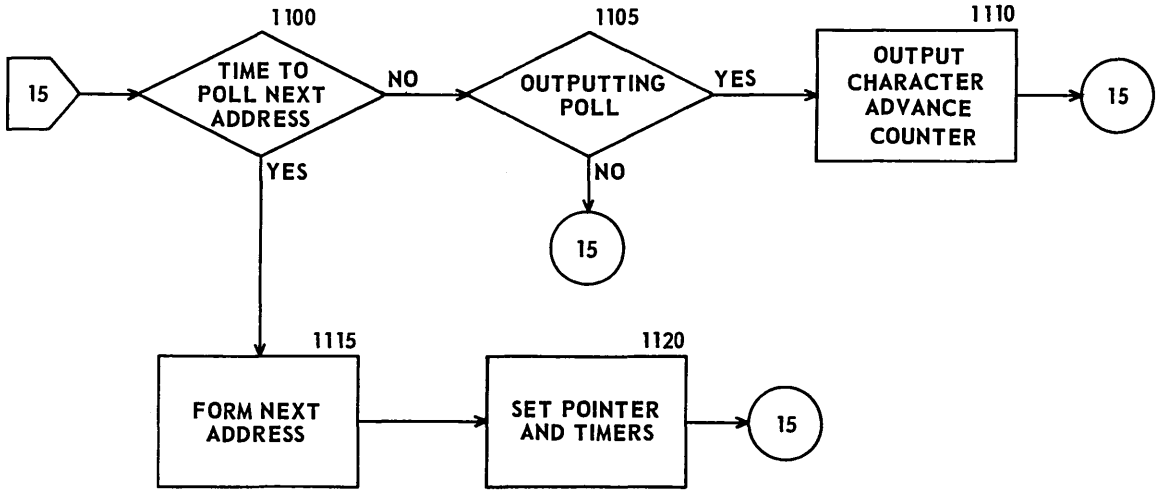


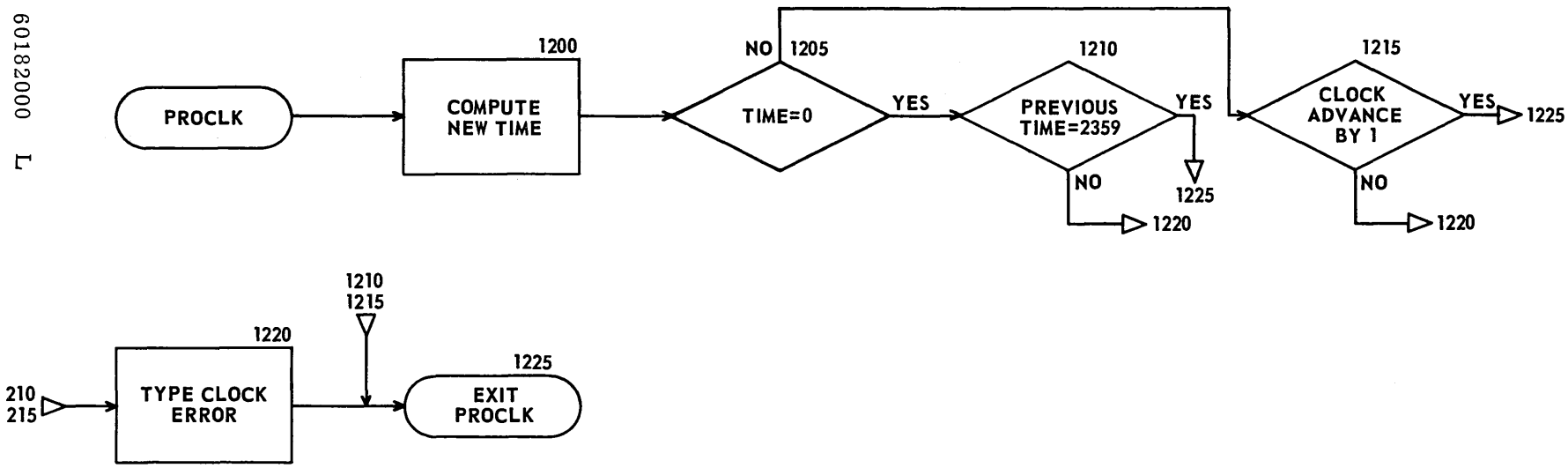
918-25


900
XFER
905
CLEAR INPUT BIN
910
TRANSFER MESSAGE TO OUTPUT BIN
915
FM
YES
NO
955
920
WANT FCC PARITY
YES
930
NO
935
920
930
TOGGLE PARITY BIT ON FCC
NO
935
WANT DATA PARITY
YES
940
TOGGLE FIRST CHARACTER PARITY BIT
945
WANT BCC ERROR
YES
NO
955
950
TOGGLE 2 BITS IN BCC
955
915
945
950
SET AND CLEAR APPROPRIATE FLAGS
EXIT XFER
PTT
970
GET INPUT FROM TTY
975
=01-99
980
980
975
SET UP POINTER
NO
985
VALID REQUEST
YES
990
GO TO ROUTINE
995
CLEAR INPUT
15

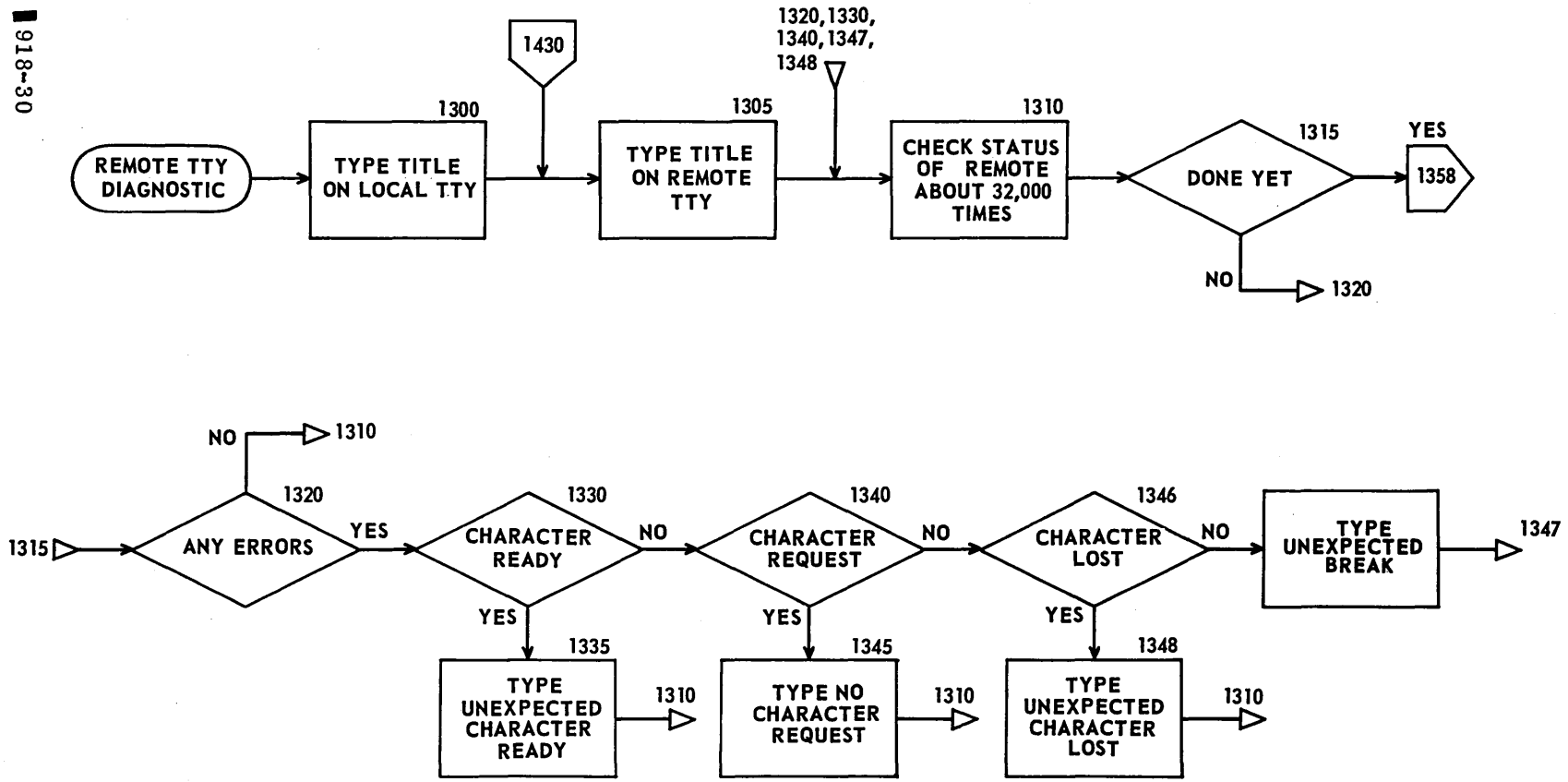

1000
TTXFER
YES 1005
TYPE ALL MESSAGES
NO
1010
ERROR TO TYPE
YES
NO
1070
1015
ADD CR. AND LF.
1050
1020
CONVERT 1 ASCII CHAR. TO 2 HEX. CHARACTER
102
1020
YES 1025
PARITY ERROR
NO
1030
INSERT SPACE BETWEEN CHARACTER
1035
INSERT ARROW UP TO SHOW PARITY ERROR
1040
BCC ERROR
YES
NO
1050
1045
INSERT BRACKET FOR SPACE ON ARROR
105
1040
1045
NO 1050
1020
ALL TRANSFERRED
YES
NO 1055
1070
XFER ERROR COUNTER
YES
NO 1060
1070
ERROR COUNTER TO XFER
YES
1065
XFER ERROR COUNTER
1010, 1055, 1060
1070
CLEAR INPUT BIN
15


1075
CPARIT
1080
CHECK PARITY ON ALL DATA A=NZ=PARITY
1085
EXIT CPARIT

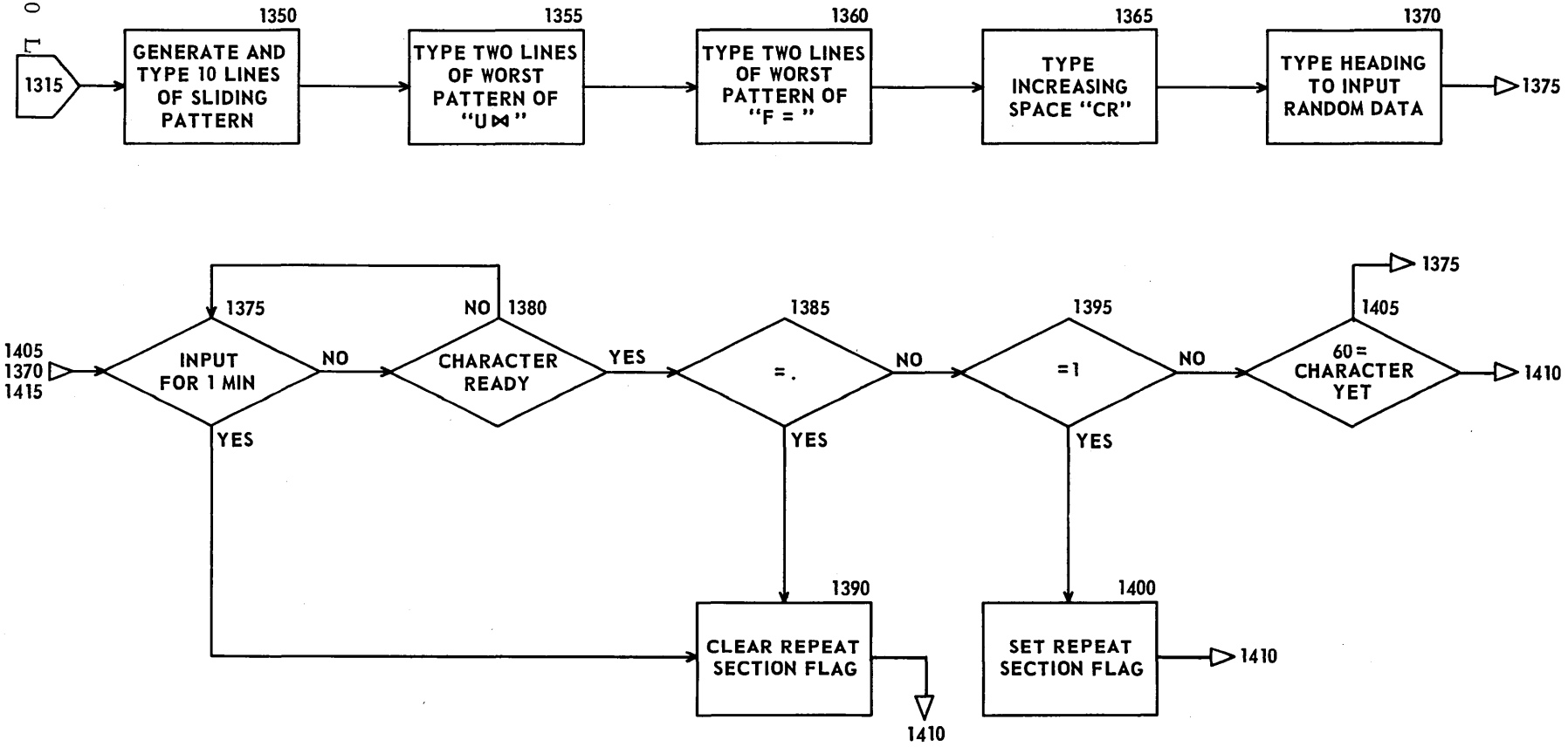

1100
TIME TO POLL NEXT ADDRESS
15
NO
1105
OUTPUTTING POLL
YES
1110
OUTPUT CHARACTER ADVANCE COUNTER
15
YES
NO
15
1115
FORM NEXT ADDRESS
1120
SET POINTER AND TIMERS
15

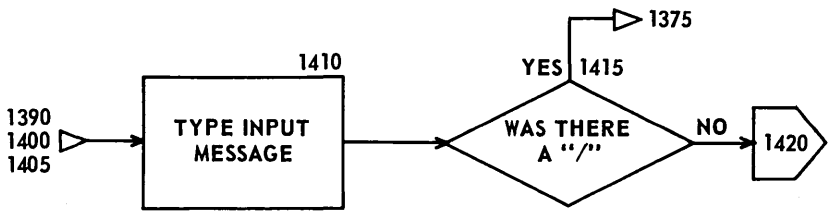

PROCLK
1200
COMPUTE NEW TIME
NO
1205
TIME=0
YES
1210
PREVIOUS TIME=2359
YES
NO
1225
1220
1215
CLOCK ADVANCE BY 1
YES
1225
NO
1220

1210
1215
1220
TYPE CLOCK ERROR
1225
EXIT PROCLK
210
215

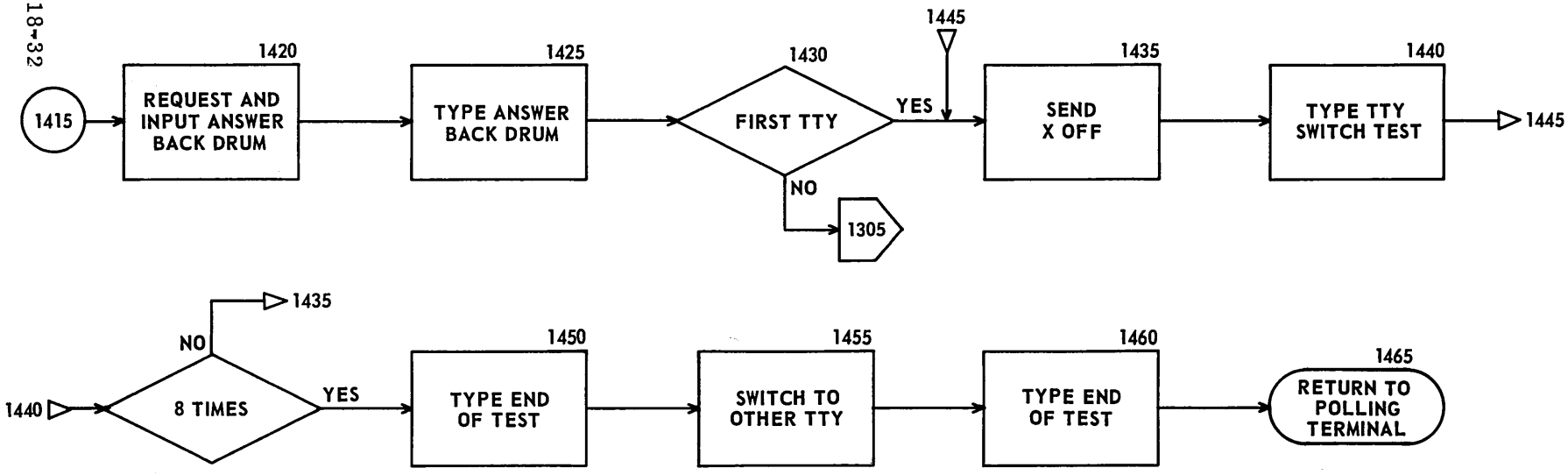

REMOTE TTY DIAGNOSTIC
1300
TYPE TITLE ON LOCAL TTY
1430
1305
TYPE TITLE ON REMOTE TTY
1320,1330, 1340,1347, 1348
1310
CHECK STATUS OF REMOTE ABOUT 32,000 TIMES
1315
DONE YET
YES
1358
NO
1320
NO
1310
1315
1320
ANY ERRORS
YES
1330
CHARACTER READY
NO
1340
CHARACTER REQUEST
NO
1346
CHARACTER LOST
NO
TYPE UNEXPECTED BREAK
1347
YES
1335
TYPE UNEXPECTED CHARACTER READY
1310
YES
1345
TYPE NO CHARACTER REQUEST
1310
YES
1348
TYPE UNEXPECTED CHARACTER LOST
1310

60182000 L





918-31


1415
1420
REQUEST AND INPUT ANSWER BACK DRUM
1425
TYPE ANSWER BACK DRUM
1430
FIRST TTY
YES
NO
1305
1445
1435
SEND X OFF
1440
TYPE TTY SWITCH TEST
1445
1435
NO
1440
8 TIMES
YES
1450
TYPE END OF TEST
1455
SWITCH TO OTHER TTY
1460
TYPE END OF TEST
1465
RETURN TO POLLING TERMINAL

DC 216A/3555/512 PRINTER TEST

(LPXA5A Test No. 5A)
(CP=03)

I. OPERATING PROCEDURE

A. RESTRICTIONS

1. This test must be run alone.
2. This test assumes a format tape has already been installed and punched as shown in Table 1.
3. Bits 2 and 3 of the SMM parameter word must specify the correct machine type.

B. LOADING PROCEDURE

1. This test is called through normal procedure from SMM17.
2. Parameter Stops

   First Stop: A = Indent Word Q = Stop/Jump Word

   Second Stop: A = Section Select Bit - Bit 0 corresponds to Section 0. Bit 1 corresponds to Section 1, etc.

   Q = Train Select Set Q = 0000 for 63 character train. Set Q = 8000 for 48AN Train Set Q = Any positive number for 48HN Train.

Section Select Assignments

Bit	Section	Title
0	0	Status Check
1	1	Spacing Test
2	2	Interrupt Status
3	3	Ripple Left Test
4	4	Ripple Right Test
5	5	Hammer Clarity
6	6	On Character in Alternating Position
7	7	Variable Buffer
8	8	Buffer Memory Test
9	9	Format Level Test
10	A	Image Memory Test
11	B	Random Pattern Test

II. MESSAGES

A. NORMAL MESSAGES

1. Title of Test: 1700/512 test IA = XXXX. XXXX = Initial address of test.
   CP03, VER. 3.1

TABLE 1. FORMAT TAPE CONFIGURATION TO BE USED WITH 3555/512 TESTS

Frame	Levels to be Punched												Frame	Levels to be Punched										
	1	2	3	4	5	6	7	8	9	10	11	12		1	2	3	4	5	6	7	8	9	10	11	12
0 - 66	X	X	X	X	X	X	X	X	X	X	X		33 - 99			X						X		X	
1 - 67											X		34 - 100		X									X	
2 - 68		X									X		35 - 101					X		X				X	
3 - 69			X						X		X		36 - 102		X	X	X		X			X		X	
4 - 70		X		X							X		37 - 103											X	
5 - 71					X						X		38 - 104		X									X	
6 - 72		X	X			X			X		X		39 - 105			X						X		X	
7 - 73							X				X		40 - 106		X		X	X			X		X	X	
8 - 74		X		X				X			X		41 - 107											X	
9 - 75			X						X		X		42 - 108		X	X			X	X		X		X	
10 - 76		X			X					X	X		43 - 109											X	
11 - 77											X		44 - 110		X		X							X	
12 - 78		X	X	X		X			X		X		45 - 111			X		X				X		X	
13 - 79											X		46 - 112		X									X	
14 - 80		X					X				X		47 - 113											X	
15 - 81			X		X				X		X		48 - 114		X	X	X		X		X	X		X	
16 - 82		X		X				X			X		49 - 115							X				X	
17 - 83											X		50 - 116		X			X					X	X	
18 - 84		X	X			X			X		X		51 - 117			X						X		X	
19 - 85											X		52 - 118		X		X							X	
20 - 86		X		X	X					X	X		53 - 119											X	
21 - 87			X				X		X		X		54 - 120		X	X			X			X		X	
22 - 88		X									X		55 - 121					X						X	
23 - 89											X		56 - 122		X		X			X	X			X	
24 - 90		X	X	X		X		X	X		X		57 - 123			X						X		X	
25 - 91					X						X		58 - 124		X									X	
26 - 92		X									X		59 - 125											X	
27 - 93			X						X		X		60 - 126		X	X	X	X	X			X	X	X	
28 - 94		X		X			X				X		61 - 127											X	
29 - 95											X		62 - 128		X									X	
30 - 96		X	X		X	X			X	X	X		63 - 129			X				X		X		X	X
31 - 97											X		64 - 130												
32 - 98		X		X				X			X		65 - 131												

Cut the tape on the line at Frame *132 and glue together. After the tape is glued into a loop be sure to repunch the holes in the last two frames.

NOTE

A prepunched format tape (P/N 50370401) with this format is available from CEM. This format may be punched using a punch (P/N 12209491) and tape (P/N 44713800), also available from CEM.

B. ERROR STOPS

1. All error stops are set up like normal SMM17 errors.

First Stop: A = Ident Word
Q = Stop/Jump Word

Second Stop: A = XYWW
X = Section
Y = Subsection
WW = Error Code
Q = Return Address (Biased)

If there are more than two stops, an explanation will be given in the description of the error.

Error Code	Description
01	Printer not ready
02	False busy status
03	No busy status when there should be
04	No reject on illegal function. A third stop will be: A = illegal function code Q = 0000
05	No last line of form status
06	False last line of form status
08	No End of Operation interrupt. The third stop will be: A = status Q = 0000
0B	Unexpected interrupt. A third stop will show: A = status Q = 0000
11	False memory busy. A third stop will show: A = status Q = 0000
12	No alarm interrupt. A third stop will show: A = status Q = 0000
16	No compare error when expected
17	No print error when expected
1	Busy too long. If busy status did not drop within 750 milliseconds after a print operation, paper motion, or error memory read, this error is given

Error Code	Description
1E	External reject on output. A third stop will show: A = status Q = 0000
1F	External reject on input
20	Internal reject on output. A third stop will show: A = status Q = 0000
21	Internal reject on input
22	No end of error memory read status. A third stop will show: A = status Q = 0000
23, 2A	False end of error memory read status
24	6/8 coincident status never came up after status checks on at least four consecutive lines of print.
25	Interrupt bit not set on interrupt. A third stop will show: A = status Q = 0000
27	End of operation bit not set on EOP. A third stop will show: A = status Q = 0000
28	Alarm bit not set on alarm interrupt. A third stop will show: A = status Q = 0000
29	Abnormal End of Operation bit not set on alarm interrupt. A third stop will show: A = status Q = 0000

III. SECTION DESCRIPTIONS

A. SECTION 0

1. Ready Status
   a. Perform a clear printer function.
   b. Check for ready status.
   c. Repeat steps a through b 50 times. If not ready error 1 (printer not ready).
2. Busy Status - During No Operation
   a. Perform a clear printer.
   b. Check for busy status. If busy, error 2 (false busy status).
   c. Repeat steps a through b 50 times.

3. Busy Status - During and After Print Operation

   a. Perform a clear printer.

   b. Check for busy status. If busy, error 2 (false busy status).

   c. Print "During and after the printing of this data status responses are being checked".

   d. Check busy status. If not busy, error 3 (no busy status when there should be).

   e. Wait for busy to drop. If not dropped by 750 milliseconds, error 1D (busy too long).

   f. Repeat steps c through e 10 times.

4. Illegal Function Code Test

   a. Select the following illegal function codes one at a time and verify the reject. If no reject, error 4 (no reject on illegal function code).

B. SECTION 1

1. Single Space Six Lines Per Inch

   a. Advance to top of form and print: "Single space six lines per inch".

   b. Single space, suppress space, print: "Function Code 01 is for single spacing".

   c. Repeat step b 25 times.

2. Single Space Eight Lines Per Inch

   a. Advance to top of form and print: "Single space eight lines per inch".

   b. Find 6/8 lines coincident.

   c. Select eight lines per inch.

   d. Suppress space, print: "Function code 01 is for single spacing", single space.

   e. Repeat step d 25 times.

3. Double Space Six Lines Per Inch

   a. Advance to top of form and print: "Double space six lines per inch".

   b. Double space.

   c. Suppress space, print: "Function code 02 is for double spacing", double space.

   c. Repeat step c 25 times.

4. Double Space Eight Lines Per Inch

   a. Advance to top of form and print: "Double space eight lines per inch".

   b. Find 6/8 lines coincidence.

   c. Select eight lines per inch. Double space.

   d. Suppress space/print: "Function code 02 is for double spacing", double space.

   e. Repeat step d 25 times.

5. Last Line of Form

   a. Advance to last line of form. Print "Last line of form".

   b. Check status. If no last line of form status, error 5 (no last line of form).

   c. Single space.

   d. Check last line of form status. If last line of form status, error 6 (false last line of form).

   e. Repeat step a through d three times.

6. Top of Form

   a. Function last line of form.

   b. Print "Last line of form".

   c. Advance to top of form. Suppress space and print "top of form".

   d. Repeat c two times, each time addressing another TOF message. The first TOF message will be printed over itself three times, the second one two times, and the third one once.

7. Page Eject.

   a. Function page eject.

   b. Print "Top of form".

   c. Repeat a through b three times.

8. 6/8 Line Coincident Status Test - 6 L. P. I.

   a. Perform a clear printer. Page eject.

   b. Check status. If 6/8 coincident, print: This is a coincident line. If not coincident, print: This is not a coincident line.

   c. Repeat step b 65 times.

9. 6/8 Line Coincident Status Test - 8 L. P. I. (Same as 7 only in 8 lines per inch).

C. SECTION 2

1. Interrupt on End of Operation - Print Operation

   a. Perform a clear printer.

   b. Start printing "Checking End of Operation Interrupt Print Operation".

   c. Function EOP interrupt.

   d. Wait for busy status to drop.

   e. Verify EOP interrupt. If no interrupt, error 08 (no EOP interrupt).

   f. Check Interrupt bit. If not set, error 25 (interrupt bit not set on interrupt).

   g. Check EOP bit. If not set, error 27 (end of operation bit not set on end of operation).

   h. Check memory busy bit. If set, error 11 (false memory busy).

   i. Repeat steps b through h 25 times.

2. Interrupt on End of Operation - Paper Motion

   a. Same as subsection 2 with the exception of step b. Step b is replaced with a double space function. This test is repeated 10 times.

3. Interrupt on End of Operation - Error Memory Read

   a. Perform clear printer.

   b. Output 10 illegal codes.

   c. Function print

   d. Wait until busy status drops.

   e. Function Read Error Memory.

   f. Wait 2 milliseconds, time enough for error memory to be scanned.

   g. Function EOP interrupt.

   h. Input 1 error location.

   i. Check End of Error Memory Read status. If set, error 23 or 2A (false end of error memory read).

   j. Repeat steps i through j 10 times.

   k. After all 10 error memory locations have been read, check end of error memory read status. If not set, error 22 (no end of Error Memory Read status).

   l. Verify EOP occurred. If no EOP interrupt, error 8 (no end of operation interrupt).

   m. Check interrupt bit. If not set, error 25 (interrupt bit not set on interrupt).

   n. Check EOP bit. If not set, error 27 (end of operation bit not set).

   o. Check memory busy bit. If set, error 11 (false memory busy).

   p. Repeat steps a through o 10 times.

4. Check Clear End of Operation Interrupt

   a. Function EOP interrupt.

   b. Function clear EOP interrupt.

   c. Start printing "Checking Clear End of Operation Interrupt Function".

   d. Wait for busy status to drop.

   e. If interrupt is received, error 0B (unexpected interrupt).

   f. Repeat steps a through e 10 times.

5. Check Alarm Interrupt

   a. Function Alarm interrupt.

   b. Output 10 illegal codes.

   c. Function print.

   d. Wait for busy to drop.

   e. Verify interrupt. No interrupt, error 12 (no alarm interrupt).

   f. Check Interrupt bit. If not set, error 25 (interrupt bit not set on interrupt).

   g. Check memory busy bit. If set, error 11 (false memory busy).

   h. Check alarm bit. If not set, error 28 (alarm bit not set on alarm interrupt).

   i. Check abnormal EOP bit. If not set, error 29 (abnormal EOP bit not set on alarm interrupt).

   j. Repeat steps a through i 10 times.

6. Check Clear Alarm Interrupt

   a. Function clear printer.

   b. Function alarm interrupt.

   c. Function clear alarm interrupt.

   d. Output 10 illegal codes.

   e. Function print.

   f. Verify no interrupt. If interrupt occurs, error 0B (unexpected interrupt).

D. SECTION 3

1. Ripple Left - six lines per inch

   a. Print one line of all characters on train.

   b. Shift line one character left for each line of print.

   c. Print 136 lines.

2. Ripple Left - eight lines per inch

   a. Same as subsection 1 at only eight lines per inch.

E. SECTION 4

1. Ripple Right - six lines per inch

   a. Print one line of all characters on train.

   b. Shift line one character left for each line of print.

   c. Print 136 lines.

2. Ripple Right - eight lines per inch

   a. Same as subsection 1 only at eight lines per inch.

F. SECTION 5

1. Hammer Adjustment and Clarity - six lines per inch

   a. Print 14 lines of the letter H in even columns.

   b. Print 14 lines of the letter H in odd columns.

   c. Alternate rows of M and W are printed, 28 lines.

2. Hammer Adjustment and Clarity - eight lines per inch

   a. Same as subsection 1 only in eight lines per inch.

G. SECTION 6

1. Print One Character Alternating With a Space - six lines per inch

   a. Print five lines of a character alternating with a space.

   b. Single space between each five line group.

   c. Repeat a and b for each character on train.

2. Print One Character Alternating With a Space - eight lines per inch

   a. Same as subsection 1 only in eight lines per inch.

H. SECTION 7

1. Variable Buffer - six lines per inch

   a. Print one line of one word (two characters).

   b. Increase each successive line by one word until one full line is printed.

   c. Decrease each successive line by one word until one word is left.

2. Variable Buffer - eight lines per inch

   a. Same as subsection 1 only at eight lines per inch.

I. SECTION 8

1. Buffer Memory Test - six lines per inch

a. Change image code for 4 to $CC.

b. Print one full line of 3 and 4.

c. Repeat a and b 32 times.

d. Print one full line of 4 and 3.

e. Repeat d 32 times.

J. SECTION 9

1. Format Tape Level Test (pre-print levels)

a. All pre-print levels are selected in such an order as to show a double space between each printed line. Each line that is printed gives the pre-print level that was selected. All lines are double spaced except the last line, level 12. The following is the order in which the pre-print levels were selected.

1	2	4
2	6	2
4	2	8
6	4	10
8	9	4
10	8	6
3	2	7
7	6	2
8	2	5
9	5	2
5	7	12

2. Format Tape Level Test (post print levels)

a. Same as subsection 1 except post print levels are selected and print out says "Post Print Level XX".

K. SECTION A

1. Image Memory Test

a. The first 48 locations are filled with a parity pattern (Figure 1). The remaining locations are loaded with a $33 code.

b. The first 48 locations of the buffer memory are filled with the same pattern. The remaining locations are space codes.

c. Print one line.

d. Shift parity pattern one location to the right. A $33 code replaces the location just shifted.

e. Repeat c through d until pattern has been shifted through all 288 locations. Double space between every 10 lines.

Figure 1. Parity Pattern For Section A

1.	01	13.	07	25.	0D	37.	13
2.	FE	14.	F8	26.	F2	38.	EC
3.	02	15.	08	27.	0E	39.	14
4.	FD	16.	F7	28.	F1	40.	EB
5.	03	17.	09	29.	0F	41.	15
6.	FC	18.	F6	30.	F0	42.	EA
7.	04	19.	0A	31.	10	43.	16
8.	FB	20.	F5	32.	EF	44.	E9
9.	05	21.	0B	33.	11	45.	17
10.	FA	22.	F4	34.	EE	46.	E8
11.	06	23.	0C	35.	12	47.	18
12.	F9	24.	F3	36.	ED	48.	E7

L. SECTION B

1. Random Pattern Test

a. Image memory is reloaded with codes 0 through 3E.

b. One full line of random characters is generated.

c. Step b is repeated 132 times. If a print error occurs, an alarm interrupt will be received.
An error 0B (unexpected interrupt) will be received.

Function Codes	
0000	Clear Printer
0001	Single Space
0002	Double Space
0003	Advanced to Last Line
0004	Page Eject
0005	Auto Page Eject

0006	Suppress Space
0007	Conditional Clear Format
0008	Eight Line Select
0009	Six Line Select
000A	Fill Image Memory
000F	Print
0012	Select Interrupt on End of Operation
0013	Clear Interrupt on End of Operation
0014	Select Interrupt on Alarm
0015	Clear Interrupt on Alarm
0016	Enable Error Memory Read
0018	Clear Format Selections/Post Print Spacing Mode
0019-0024	Select Format Tape Levels 1-12 (Post Print Spacing)
0028	Preprint Spacing Mode
0029-0034	Select Format Levels 1-12 (Pre-Print Spacing)

Status Codes

XXX1	Ready
XXX2	Busy
XXX4	Interrupt
XXIX	End of Operation
XX2X	Alarm
XX4X	Abnormal End of Operation
XX8X	Protected
XX1X	Compare Fault
X2XX	Paper Fault
X4XX	Last Line of Form
X8XX	Format Tape Level 9
1XXX	Memory Busy

2XXX	Memory Busy
4XXX	6/8 Line Coincident
8XXX	End of Error Memory Read

ASCII CODES FOR EACH CHARACTER ON THE TRAIN

Codes	63	AN	HN
20	Space	Space	Space
24	$	$	$
25	%	None	'
28	(	%	(
29	)	¤	)
2A	*	*	*
2B	+	&	+
2C	, (Comma)	,	,
2D	-	-	-
2E	.	.	.
2F	/	/	/
30	0	0	0
31	1	1	1
32	2	2	2
33	3	3	3
34	4	4	4
35	5	5	5
36	6	6	6
37	7	7	7
38	8	8	8
39	9	9	9
3A	:	None	None
3B	;	None	None
3C	< (Less)	None	None
3D	=	#	=
3E	> (Greater)	None	None
41	A	A	A
42	B	B	B
43	C	C	C
44	D	D	D
45	E	E	E

Codes	63	AN	HN
46	F	F	F
47	G	G	G
48	H	H	H
49	I	I	I
4A	J	J	J
4B	K	K	K
4C	L	L	L
4D	M	M	M
4E	N	N	N
4F	O	O	O
50	P	P	P
51	Q	Q	Q
52	R	R	R
53	S	S	S
54	T	T	T
55	U	U	U
56	V	V	V
57	W	W	W
58	X	X	X
59	Y	Y	Y
5A	Z	Z	Z
5B	[	None	None
5D	]	None	None
5E	∧	None	None
61	≠	@	None
62	≤	None	None
63	≥	None	None
64	∨	None	None
65	↑	None	None
66	↓	None	None
67	↱	None	None
68	≡	None	None
7C	—	+	&

NOTE

Normally codes 61 through 68 are used for small letters a through h of the alphabet. However, in this test those codes will be used as indicated above.

	Train Set							
Order	63-1	63-2	63-3	63-4	63-5	63-6	AN	HN
1	0	0	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1
3	2	2	2	2	2	2	2	2
4	3	3	3	3	3	3	3	3
5	4	4	4	4	4	4	4	4
6	5	5	5	5	5	5	5	5
7	6	6	6	6	6	6	6	6
8	7	7	7	7	7	7	7	7
9	B	$	J	V	$	(	8	8
10	Z	↱	K	W	↱	G	9	9
11	,	≠	Q	X	≠	H	G	G
12	/	=	*	Y	=	)	H	H
13	8	8	8	8	8	8	+	+
14	9	9	9	9	9	9	-	-
15	A	A	A	A	A	A	.	.
16	C	C	C	C	C	C	E	E
17	(	B	≤	J	V	≤	A	A
18	G	Z	≥	K	W	≥	B	B
19	H	,	<	Q	X	<	C	C
20	)	/	>	*	Y	>	D	D
21	R	R	R	R	R	R	R	R
22	I	I	I	I	I	I	I	I
23	F	F	F	F	F	F	F	F
24	L	L	L	L	L	L	L	L
25	M	M	M	M	M	M	M	M
26	N	N	N	N	N	N	N	N
27	O	O	O	O	O	O	O	O
28	P	P	P	P	P	P	P	P
29	[	(	B	[	J	V	J	J
30	%	G	Z	%	K	W	K	K
31	¬	H	,	¬	Q	X	Q	Q
32	]	)	/	]	*	Y	*	*
33	D	D	D	D	D	D	/	/
34	U	U	U	U	U	U	S	S
35	S	S	S	S	S	S	T	T
36	T	T	T	T	T	T	U	U

Train Set

Order	63-1	63-2	63-3	63-4	63-5	63-6	AN	HN
37	V	↑	(	B	↑	J	V	V
38	W	↓	G	Z	↓	K	W	W
39	X	^	H	,	^	Q	X	X
40	Y	v	)	/	v	*	Y	Y
41	+	O	+	+	+	+	$	$
42	-	-	-	-	-	-	&	&
43	.	.	.	.	.	.	,	,
44	E	E	E	E	E	E	Z	Z
45	J	V	:	(	B	:	¤	(
46	K	W	;	G	Z	;	#	=
47	Q	X	≡	H	,	≡	@	'
48	*	Y	=	)	/	=	%	)

HOUSE OF REPRESENTATIVES VOTE STATION EXERCISER
(VSDA4D Test No. 4D)

I INTRODUCTION

This exerciser reads card data and buttons pushed on the electronic vote stations. This information is displayed on cathode ray tube (CRT), teletype (TTY), or Tally printer.

II REQUIREMENTS

The exerciser runs under control of SMM17.

III OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The exerciser is loaded using standard SMM17 loading procedure.

B. PARAMETERS

A2	Q2	A3	Q3	A4	Q4
VOTU	VOTUA	PFLAG	PRU	TALTU	DISTU

VOTU = Logical unit number of vote station to test
PFLAG = Output device, O = TTY, 1 = Tally printer, 2 = CRT
PRU = Printer logical unit number
TALTU = Tally printer logical unit number
DISTU = Display logical unit number

IV OPERATOR COMMUNICATION

After parameters are entered, no other operator action is necessary.

V DESCRIPTIONS

VSDA4D accepts cards and button data and displays what occurred on the selected output device. After parameters are entered, no other operator action is necessary. Output is in the form:

XX YYYYYYYY ZZZZ

Where XX = The station address of the electronic vote station (EVS)
YYYYYYYY = The ID card data
ZZZZ = "Yea", "Nay" or "Present"

QSE 14735 BUFFERED DATA CHANNEL TEST

(BDL085 Test No. 85)

OPERATIONAL PROCEDURE

A. RESTRICTIONS

Sections 3, 4, 5, and 6 do not select density on the MT units. However, it is recommended that 200 BPI be selected to allow greater accuracy in testing the CWA register.

B. LOADING PROCEDURE

1. The test operates under control of 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17.
3. The test can be restarted after loading from Initial address.

C. PARAMETERS

1. If bit 0 of the Stop/Jump word is set, the program will have one monitor stop displaying $8531 in the A register and the Stop/Jump word in the Q register. Two additional stops with the test parameters displayed in the A and Q registers are defined as follows:

Stop 2	A = WE01,	where the W field is bits 15-11 and defines the BDC to be tested. Enter 2, 7, or C for the BDC numbers 1, 2, or 3 respectively. The E field is bits 10-7. Bits 9 through 7 specify the equipment number of the 1731/1732 Magnetic Tape Controller. Bit 10 specifies the BDC Unit Select group.
	Q = 000U,	where U specifies the 601/608/609 Tape Unit which will be used for I/O.
Stop 3	A = XXXX,	the End of Operation interrupt line for the BDC. Only 1 bit is set in this word which must indicate the interrupt line. For example if the End of Operation interrupts are to be received on line 5, Bit 5 would be set.
	Q = XXXX,	the sections of the BDC test to run. Bit 0 of Q will select Section 1 to be run, etc. There are six sections in all. If all six sections were to be run, Q would be set to 003F.
Stop 4	A = XXXX,	illegal equipment (enter into A an equipment address that is unused on your system. This equipment address is used to check internal rejects) E field bits 7-10.
	Q = XXXX,	unused (prestored as 0001)

2. If bit 0 of the Stop/Jump word is not set, the test will be run using the prestored parameters. These parameters assume the following:

   a. BDC number 1 is to be tested and the tape controller is number 3. (WE01 = 1181)

   b. Tape unit 7 is the tape to use for I/O.

   c. The interrupts on End of Operation from the BDC are received on line 3.

   d. All six sections of the test will be run.

3. A typeout of selected parameters will occur after last stop.

D. SELECTIVE SKIP AND STOP SETTINGS

1. STOP - must be set for running of SMM17.

2. SKIP - when the Stop/Jump word is displayed in Q.

E. MESSAGES

1. Typeouts or Alarms

   a. Normal Program Typeouts

      1) Test identification at start of test
         BDL085, BUFFERED DATA CHANNEL TEST VR. 3.1
         IA=XXXX, FC=XX

      2) End of test typeout

A	Q	A	Q
8524	S/J	Pass No.	Return Address

   b. Error Alarms

      1) The following is typed out:

         a) Identification word

         b) Stop/Jump parameter

         c) Section/Error number

         d) Return address

         e) Information dependent upon specific error

         f) Information dependent upon specific error

2. Error Codes

   An error code is displayed in the lower two digits of the A register on the second stop of all error stop sequences. A description of the error codes used and the data displayed in the A and Q registers of the third stop is listed as follows:

Error 01 - Incorrect equipment parameter was entered. Program will make another parameter stop if placed in Run.

A = the equipment parameter entered
Q = 0000

Error 02 - External reject on input of BDC status. If the error condition is not repeated (Bit 4 of Stop/Jump word set) the test will be terminated.

A = the contents of Q when the input instruction was executed
Q = 0000

Error 03 - Internal reject on input of BDC status. If the error condition is not repeated, the test is terminated.

Error 04 - Ready not set on BDC status. If the condition is not repeated, the test is terminated.

A = BDC status
Q = 0000

Error 05 - External reject on input of BDC current address.

A = contents of Q when the input instruction was executed
Q = 0000

Error 06 - Internal reject on input of BDC current address.

A = contents of Q when the input instruction was executed
Q = 0000

Error 07 = External reject on Terminate Buffer.

A = contents of Q when the input instruction was executed
Q = 0000

Error 08 = Internal reject on Terminate Buffer.

A = contents of Q when the input instruction was executed
Q = 0000

Error 09 = External reject on attempt to output a function to the BDC.

A = contents of Q when output was attempted
Q = contents of A when output was attempted

Error 0A - Internal reject on attempt to output a function to the BDC.

A = contents of Q when output was attempted
Q = contents of A when output was attempted

Error 0B - External reject on direct output of a function to the 1731/1732 Tape Controller.

A = contents of A when output was executed
Q = contents of Q when output was executed

Error 0C - Internal reject on direct output of a function to the 1731/1732 Tape Controller.

A = contents of A when output was executed
Q = contents of Q when output was executed

Error 0D - External reject on input of status 1 of the 1731/1732 Tape Controller.

A = the contents of Q when the input was executed
Q = 0000

Error 0E - Internal reject on input of status 1 of the 1731/1732 Tape Controller.

A = the contents of Q when the input was executed
Q = 0000

Error 0F - External reject on input of status 2 of the 1731/1732 Tape Controller.

A = the contents of Q when the input was executed
Q = 0000

Error 10 - Internal reject on input of status 2 of the 1731/1732 Tape Controller.

A = the contents of Q when the input was executed
Q = 0000

Error 11 - No write ring in selected tape unit. If this error condition is not repeated, the test is terminated.

A = the selected tape unit
Q = status 2 of the selected tape unit

Error 12 - The selected tape unit is protected. If this error condition is not repeated, the test will be terminated.

A = the selected tape unit
Q = status 1 of the selected tape unit

Error 13 - External reject on attempt to initiate buffered output to tape.

A = the first word address minus 1 of the buffer area
Q = contents of Q when the output instruction was executed

Error 14 - Internal reject on attempt to initiate buffered output to tape.

A = the first word address minus 1 of the buffer area
Q = contents of Q when the output instruction was executed

Error 15 - External reject on the attempt to initiate a buffered input from tape.

A = the first word address minus 1 of the buffer area
Q = the contents of Q when the output instruction was executed

Error 16 - Internal reject on the attempt to initiate a buffered input from tape.

A = the first word address minus one of the buffer area
Q = the contents of Q when the output instruction was executed

Error 17 - Busy bit (bit 1) of the BDC status was not set after initiating a buffered output.

A = BDC status
Q = 0000

Error 18 - Busy bit (bit 1) of the BDC status was not set after initiating a buffered input.

A = BDC status
Q = 0000

Error 19 - Reply bit (bit 9) of the BDC status was not set after initiating a buffered output.

A = BDC status
Q = 0000

Error 20 - Reply bit (bit 9) of the BDC status was not set after initiating a buffered input.

A = BDC status
Q = 0000

Error 21 - Reject bit (bit 8) of the BDC status was never set (over an arbitrary length of time) after initiating a buffered output.

A = BDC status
Q = 0000

Error 22 - Reject bit (bit 8) of the BDC status was never set (over an arbitrary length of time) after initiating a buffered input.

A = BDC status
Q = 0000

Error 23 - End of Operation bit (bit 4) of the BDC status is set at the same time as the Busy bit.

A = BDC status
Q = 0000

Error 24 - End of Operation bit (bit 4) of the BDC status is not set after the Busy cleared at the end of a buffered output.

A = BDC status
Q = 0000

Error 25 - End of Operation bit (bit 4) of the BDC status is not set after the Busy cleared at the end of a buffered input.

A = BDC status
Q = 0000

Error 26 - External reject still received from the BDC when attempting a tape status when the BDC was Busy after 16 attempts.

A = BDC status
Q = 0000

Error 27 - No interrupt received from the BDC on End of Operation (buffered output).

A = BDC status
Q = 0000

Error 28 - Alarm bit set in tape status 1 after a buffered output was complete.

A = Tape status 1
Q = 0000

Error 29 - No interrupt received from the BDC on End of Operation (buffered input).

A = BDC status
Q = 0000

Error 2A - Interrupt bit (bit 2) of the BDC status was not set after an End of Operation interrupt occurred.

A = BDC status when interrupted
Q = 0000

Error 2B - Data error

A = Data read
Q = Expected value
A = Failing address
Q = 0000

Error 2D - The current address which was input from the BDC was neither the same as or up to two greater than the previous current address input.

A = Previous current address
Q = Current address
A = BDC status at CA failure
Q = 0000

Error 2E - End of Operation status bit (bit 4) was not set in the BDC status when an Interrupt on End of Operation occurred.

A = BDC status
Q = 0000

Error 2F - Buffer terminated at incorrect address.

A3 = Actual address buffer terminated at
Q3 = Expected last word address, at EOP

Error 33 - Incorrect status after initiating buffer to non-existent equipment (parameter A4) on this BDC.

A3 = Expected channel status after initiating a buffer
Q3 = Actual channel status after initiating a buffer
A4 = Expected address register status
Q4 = Actual address register status
A5 = Equipment address when error occurred
Q5 = Iteration count (range = FFFC-0003)

Error 34 - Current word address was not greater than FWA-1 after initiating a buffer to illegal equipment on BDC, 1 for READ, 2 for WRITE.

A3 = Expected channel status
Q3 = Actual channel status
A4 = FWA-1 output to BDC to initiate buffer
Q4 = CWA of BDC on terminate buffer command
A5 = Equipment address when error occurred
Q5 = Iteration count

Error 35 - Internal reject on clear controlled direct through BDC

A3 = BDC expected status
Q3 = BDC actual status
A4 = Equipment expected status
Q4 = Equipment actual status
A5 = Equipment address when error detected
Q5 = Not available

Error 36 - External reject on clear controller

Same as error 35

Error 37 - Channel busy or not ready

A3 = 0000
Q3 = BDC actual status
A4 = 0000
Q4 = 0000
A5 = Equipment address when error occurred
Q5

Error 38 - Unit/Equipment busy

A3 = 0000
Q3 = BDC actual status
A4 = 0000
Q4 = Unit status
A5 = Equipment address when error occurred
Q5 = Iteration count

Error 39 - Buffer terminated before programmed LWA+1

A3 = Not available
Q3 = BDC status
A4 = Actual CWA status at EOP
Q4 = Expected CWA status at EOP
A5 = Equipment address when error occurred
Q5

Error 3A - Buffer did not terminate at LWA+1

A3 = Not available
Q3 = BDC status
A4 = Current word address when buffer was terminated
Q4 = Expected LWA register

Error 3C - BDC not busy before CWA=LWA+1

A3 = Expected BDC status
Q3 = Actual BDC status
A4 = CWA register status
Q4 = LWA+1 sent to BDC
A5 = Equipment address when error occurred
Q5

Error 3D - BDC buffer hung before CWA=LWA+1 when doing buffered equipment status inputs or buffered clear controller outputs.

A3 = Expected status of BDC
Q3 = Actual status of BDC
A4 = CWA register status of hung buffer
Q4 = Expected LWA+1 of buffer
A5 = Equipment address when error occurred
Q5 = Iteration count

Error 3E - Look ahead, no interrupt is on EOP at end of first buffer.

A = BDC status
Q = 0000

Error 3F - Look ahead, interrupt is on EOP at end of first buffer.

A = BDC status
Q = 0000

Error 40 - Look ahead, ready is set after BDC accepted the second buffered I/O command.

A = BDC status
Q = 0000

Error 41 - Look ahead, busy is not set after first buffer terminated, second buffer did not start.

A = BDC status
Q = 0000

Error 42 - Internal reject, while attempting direct I/O while BDC is busy doing buffered I/O.

A = BDC status
Q = 0000

Error 43 - Internal reject is on second buffered I/O command.

A = FWA-1 of buffer area
Q = Contents at output time

Error 44 - External reject is on second buffered I/O command.

A = FWA-1 of buffer area
Q = Contents at output time

Error 69 - Busy hung, BDC or controller busy is set too long or hung.

A = BDC status
Q = Tape status 1

3. Error Stops

Error stops will occur if bit 3 of the Stop/Jump word is set and an error occurs in the test.

II. DESCRIPTION

A. INITIALIZATION (UNIT)

1. Convert bias value and frequency count to ASCII and store in typeout routine.
2. Type out test title, initial address, and frequency count.

3. Set up return address (IA+5).

4. Parameter entry stop.

5. Check for correct W field in equipment code. Error stop if incorrect.

7. Exit to SMM.

B. SECTION ONE (S1)

This section checks static conditions of BDC then proceeds to check the CWA register, LWA register, adder, buffer read capabilities, and buffer write capabilities.

1. Check status for ready.

2. Input current address; no Reject expected.

3. Execute terminate buffer and input current address to

   a. No Reject expected.

4. Check EOP interrupt select and clear.

5. Attempt buffer output to non-existent equipment on channel.

   a. Start with FWA-1=0. Expect BDC to hang with CWA two greater than FWA-1. Expect status to be busy.

   b. Do until FWA-1 = $7FFF.

   c. Do a and b three times

6. Attempt buffer input from non-existent equipment on channel (same as 5).

7. Do direct FCN clear controller to selected Equipment Expect Reply.

8. Do 500_{10} word buffer after A clear controller function.

   a. Monitor CWA. Expect termination when CWA=LWA+1.

   b. Monitor BDC status. Expect busy until CWA=LWA+1.

   c. Do 100_{10} times.

9. Do direct input status 1 of selected equipments. Save for use in next step. Expect reply.

10. Do 500_{10} word buffer input of status 1 from selected device.

    a. Same as 8a and 8b.

    b. Compare data from step 9 and report errors.

    c. Do 100_{10} times.

C. SECTION TWO (S2)

This section checks static conditions on the BDC, tape controller, and tape unit.

1. Connect selected tape unit.
2. Check for write enable. Error if not present.
3. Check for tape unit unprotected. Error if protected.
4. Rewind tape.
5. Exit section two.

D. SECTION THREE (S3)

This section does a 500-word buffered Write and Read.

1. Request interrupt line from SMM.
2. Select tape unit and rewind it.
3. Select binary mode.
4. Initiate a 500-word buffered write.
5. Check BDC status for Busy. Repeat from item 2 if Not Busy.
6. Check BDC status for Reply. Should be set.
7. Check BDC status for Reject during output. Should be set.
8. Exit to SMM until buffer is complete.

9. Rewind tape.
10. Repeat from item 4 for a 500-word read.
11. Clear interrupt request in SMM.
12. Exit section three.

E. SECTION FOUR (S4)

This section writes and reads ten 500-word records for each of fifteen patterns. End of Operation interrupt is checked after each record.

1. Request interrupt line from SMM.
2. Select tape.
3. Pick up current data pattern.
4. Select binary mode if pattern number is Odd. Select BCD mode if pattern number is Even.
5. Clear interrupt flag.
6. Select EOP interrupt on BDC.
7. Initiate 500-word buffered write.
8. Check for reject during buffered operation.
9. Exit to SMM until buffer is complete.
10. Check for EOP interrupt. Error if not present.
11. Check tape status for EOT, Parity, Lost Data, and Alarm.
12. Repeat from item 5 for 10 records.
13. Update data pattern.
14. Repeat from item 2 for 15 patterns.
15. Rewind tape.
16. Blank out storage data.
17. Repeat from item 5 using a Read instead of a Write. Data is checked for each record.
18. Exit section four.

F. SECTION FIVE (S5)

This section tests the current word address.

1. Request interrupt line from SMM.
2. Rewind tape, select binary mode.
3. Initiate buffered output. Word Count = $7FFE_{16}$-LOCSEX.
4. Input current address to A. Address should be one greater than the CWA.
5. Store current address.
6. Input current address to A. This address should be equal to or up to two greater than previous address. Error if not one of these two conditions.
7. If current address is one greater than previous address, repeat from item 4.
8. If current address equals previous address, check BDC status for EOP. Loop to item 4 if not set.
9. Check tape status for EOT, Parity, Lost Data, and Alarm. Error if any of these are set.
10. Clear interrupt request.
11. Exit section five.

G. SECTION SIX (S6)

This section tests the look ahead feature.

1. Request interrupt line from SMM.
2. Select tape unit and check for write ring.
3. Read status and check if tape unit is protected.
4. Rewind tape.
5. Select interrupt on EOP.
6. Start first buffer ($7F words) output.
7. Check if BDC is busy; error if not.
8. Check if BDC is ready; error if not.
9. Start second buffer output ($7F words).
10. Check if BDC is ready; error if it is.
11. Terminate first buffer.

12. Check if interrupt EOP occurred; error if not.
13. Check if BDC is busy; error if not.
14. Wait till BDC is not busy.
15. Check if interrupt EOP occurred; error if it did.
16. Clear SMM interrupt request.
17. Exit Section 6.

III. PHYSICAL REQUIREMENTS

A. SPACE REQUIRED

Approximately 2000 locations.

B. INPUT AND OUTPUT TAPE MOUNTINGS

The 601/608/609 Tape Unit selected for I/O must have a write ring and must be ready.

C. TIMING - approximately 1 minute 15 seconds.

D. EQUIPMENT CONFIGURATION

1. 1784 Computer
2. 17X5 Interrupt Data Channel
3. QSE 14735 Buffer Data Channel
4. 1731/1732 Magnetic Tape Controller
5. 601/608/609 Magnetic Tape Unit

ECHO DATA TO 6X00 TEST RT3
(GTC07C Test No. 7C)

I. PARAMETERS

A. 1700

A1 = I/O word

Q1 = STJP

A2 = Sections, preset to 0003 (Set bit 15 to repeat any pattern.)
Q2 = Word count, preset to $0140 (500) (8)

A3 = Starting pattern, preset to $FFF
Q3 = Data type (0 = fixed, 1 = random), preset to $0000 (Fixed data = every buffer different but all words are the same pattern.)

B. RT3 SECTION 6

1500 = 0002	Stop on error only
1501 = 6000	Repeat test and repeat section
1502 = CHEQ	MUX address
1503 = 000X	X = MUX DSC number
1507 = 000X	X = MUX DSC number
1510 = 0040	Section 6 only

NOTE

Start Section 6 of RT3 first and then start this test.

II. ERROR CODES

All error conditions return test back to Section 0 transmit.

8 = Transmit Time-Out

A3 = Current word address
Q3 = Address of last reference address

A4 = Status
Q4 = Equipment number

9= Bad Status after Transmit

A3 = Actual status

Q3 = Unexpected status bits

A4 = 0000

Q4 = 0000

A= Receiver Time-Out

A3 = Current word address

Q3 = Address of last referenced address

A4 = Status

Q4 = Equipment number

B= Bad Receive Status

A3 = Actual status

Q3 = Equipment number

A4 = 0000

Q4 = 0000

C= Data Error

A3 = Actual data

Q3 = Expected data

A4 = Difference (EOR of input/output data)

Q4 = Failing word of buffer

COMMENT SHEET

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