CONTROL DATA® 1700 Computer System
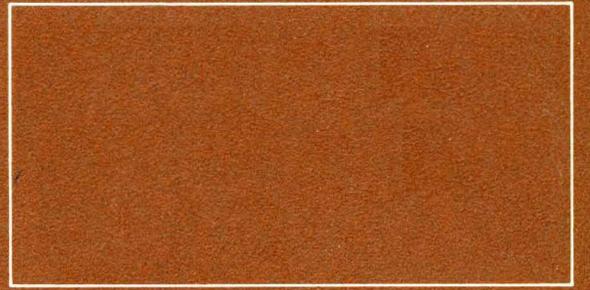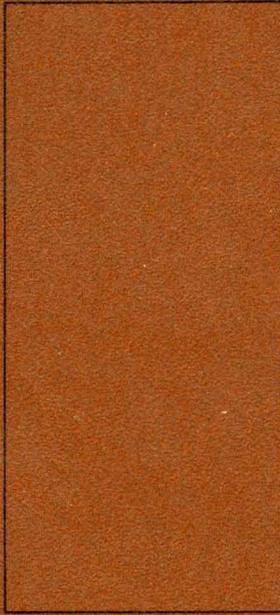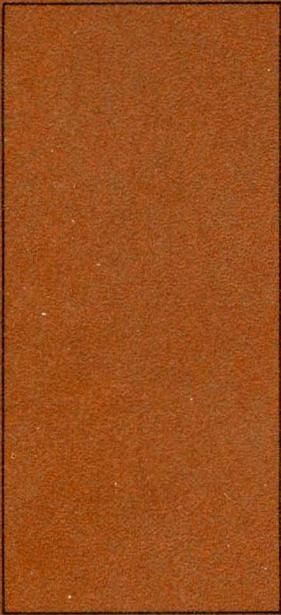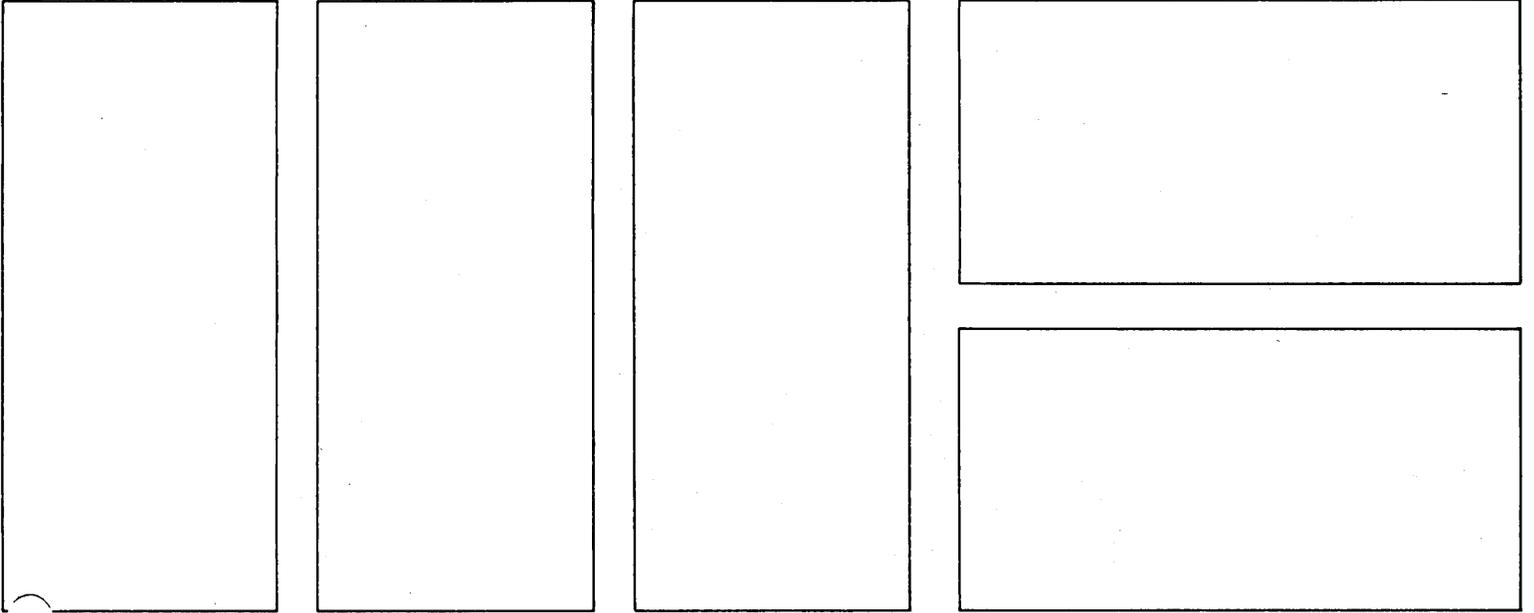
STANDARD PERIPHERAL REFERENCE MANUAL

CONTROL DATA® 1700 Computer System

STANDARD PERIPHERAL REFERENCE MANUAL

RECORD of REVISIONS

REVISION	NOTES
A	Initial Printing. Final Edition.
(10-14-66)	
B	Publications Change Order 15110 which adds 1738-A/B Disk Drive Controller to Mass Storage
(11-8-66)	Equipment Section.
C	Publications Change Order 15448 which adds 1718-A Satellite Coupler to Interface Equipment
(12-23-66)	Section.
D	Publications Change Order 15582 which adds 1716-A Coupling Data Channel to Interface Equipment
(1-13-67)	Section.
E	Publications Change Order 17487 which adds 1742-A/B Line Printer Controller to Part 5, Visual
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F	Publications Change Order 18309 which adds 1732-A/B Magnetic Tape Controller to Magnetic Tape
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	8, 9, 11 and 12 of 1731-A/B Magnetic Tape Controller, Magnetic Tape Equipment Section; pages 10,
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G	Publications Change Order 19029 which adds 1728-A/B Card Reader/Punch Controller to Part 4,
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H	Publications Change Order 18706 which revises page 13 of 1732-A/B Magnetic Tape Controller in
(5-25-68)	Part 3, Magnetic Tape Equipment.
J	Publications Change Order 19529 which adds 1726 Card Reader Controller to Part 4, Card
(5-25-68)	Equipment Section.
K	Publications Change Order 19545 which adds 1740 Line Printer Controller to Part 5, Visual
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L	Engineering Change Order 19932. Pages 10 and 20 revised of the 1738 section.
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(7-31-68)	10, 19 and 20, 1731 pages 14 and 15, 1732 pages 1, 10 and 17, 1742 section revised.
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	(pages i, ii and 1 thru 16), General v changed.
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FOREWORD

Input to A and Output from A, the two 1704 input/output instructions, are the key to all computer communication with its peripheral equipment. These instructions alone do not specify all information necessary to control a device. The programmer, therefore, must select a device, request status, specify operating conditions, and initiate data transfer via these instructions together with the 1700 register contents.

As suggested by the name A/Q Channel, the equipment has access to the information in the A and Q registers. The contents of these two registers (32 total bits available), combined with the two I/O instructions, can specify all the information needed to operate the peripheral equipment. The Q register specifies addresses and operations, while the A register further specifies or directs the operation, receives information, or is available for input or output data.

Logically, if the A register is to be used to supply a control or data word, A must be loaded with that word. Executing an Output from A instruction presents this 16-bit word to the equipment. The Q register directs the controller how to use this word; e.g., as the first word address minus one for a buffered operation, for interrupt selection, or as data. Similarly, if information is to be brought into the A register, an Input to A instruction is used and (Q)* specify the type of information to be brought into A (e.g., status or data).

The reader may notice two paradoxes when examining a table of codes for a 1700 peripheral equipment:

1) The same value in Q may be used for two distinct operations.

2) An input operation using the Direct Storage Access Bus (i.e., a buffered input) is initiated by an Output from A instruction.

The effects of the two 1704 I/O instructions readily explain these paradoxes. In the first case, the OUT instruction and (Q) or the INP instruction and (Q) do indeed uniquely define an operation. In the second case, the A register initially holds the address the converter needs to specify the buffer area. Executing the Output from A instruction sends this address to the converter, whereupon the input buffer operation can begin.

As indicated in the preceding paragraphs, the 1704 I/O instructions do not necessarily transfer data in the usual sense of the word data. These instructions can transfer a word between the A register and the peripheral equipment which is either data or a control word. They directly control the input/ output of a single word to/from the A register. Once they have been used to send the proper control words to the device, the transfer of data to or from memory may occur, not under control of the 1704 instructions but under control of the converter and the Direct Storage Access Bus.

This manual supplies to the programmer the codes for the A and Q registers which are used in conjunction with the two 1704 I/O instructions to operate the 1700 peripheral equipments. It presents a brief physical description of these equipments, the relationship of the equipment to the computer system, definitions of programming operations, special programming considerations, and instructions for manual operation. It assumes the programmer is familiar with the 1704 instructions and procedures. It does not supply information on the basic peripherals. For these devices and further information on input and output, refer to the 1700 Computer System Reference Manual, Pub. No. 60153100.

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* Parentheses around a letter are used to indicate the contents of a register.

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FIGURES

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1706-A BUFFERED DATA CHANNEL

INTRODUCTION

This section describes the CONTROL DATA* 1706-A Buffered Data Channel (BDC), its physical system, and programming information. There is no operating information since the 1706 has no indicators or manual controls.

FUNCTIONAL DESCRIPTION

System Relationship

The 1706 provides a 16-bit, bidirectional, buffered input/output path between the 1704 Computer with a 1705 Interrupt Data Channel (IDC) and up to eight peripheral equipments.
Figure 1 shows the connections between the 1706 and other equipments. The circled numbers indicate the number of connecting cables.

A maximum of three 1706 BDC's may be attached to the 1705 IDC. A 1716 Coupling Data Channel may replace any or all of the 1706's.

Since the 1706 contains no indicators or manual controls, all operations must be initiated by the computer. In response to any I/O instructions and the contents of the Q register, the 1706 connects the computer to one of the external controllers and sends the appropriate Read or Write signal. The 1706 then controls the Read or Write operation. If the contents of the Q register specify a buffered operation, the 1706 obtains access to storage via the Direct Storage Access Bus (DSA) when necessary to fetch or store information. If the (Q) specify a direct input or output, a 16-bit word is transferred from the selected peripheral device to the A register of the 1704 or vice versa.
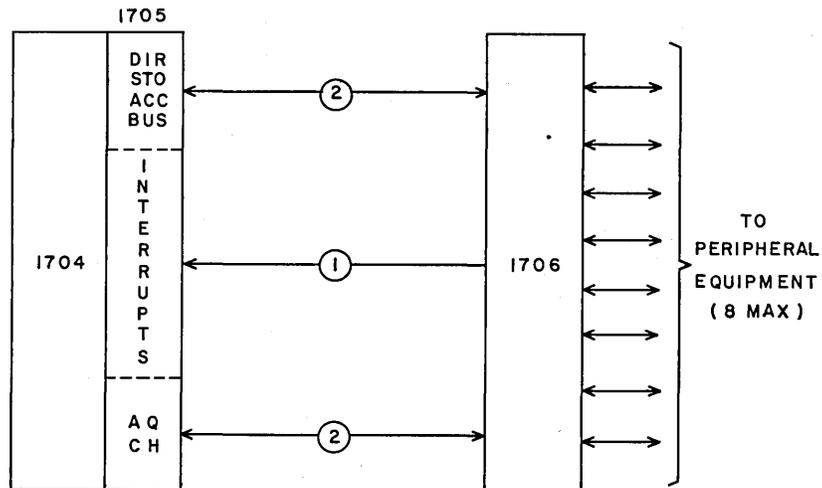

Figure 1. Typical 1704/1705/1706 Configuration.

* Registered trademark of Control Data Corporation

Interrupt

An interrupt to the computer can be generated when the 1706 terminates a buffered transfer, i.e., upon end of operation. This interrupt is enabled by an Output from A instruction with the W field (bits 11-15) of the Q register selecting a function to the 1706, and bits 15 and 00 of the A register set. It is disabled by a function to the 1706 and bit 15 of A clear, bit 00 of A set.

An interrupt itself from the 1706 is cleared by a function to the 1706 with bit 00 of A set. Thus, either reselecting or disabling the interrupt selection also clears the interrupt.

Program Protection

The 1706 rejects non-protected Status, Terminate Buffer, Function, and Current Address instructions during a buffer operation that is initiated by a protected instruction. The 1706 has no program protect switch; the program protect feature of a 1700 System is governed by the PROTECT switches on the 1704 and the specific device connected to the 1706. However, if a program protect fault occurs, a status bit is set in the 1706 status reply word.

Reply/Reject

The 1706 responds to an Input or Output instruction within 4 microseconds with either a Reply or Reject signal. The 1706 returns a Reply whenever it can perform the requested operation. Three conditions will cause a Reject to be returned to the computer:

1) The 1706 is Busy when a request for a buffered transfer, a direct input, or a direct output is received;

2) A program protect fault occurs (also see Program Protection);

3) A device returns a Reject upon a direct input/output request.

If for some reason the computer receives no response (for example, the 1706 addressed does not exist in the system), the computer will generate an Internal Reject.

PROGRAMMING

Summary of Programming Information

Tables 1, 2 and 3 are a synopsis of the information necessary to program the 1706. Explanations of the information presented here can be found in the sections following. These tables are intended as a quick reference for the experienced programmer, a preview for the reader studying the following material, and a summary for the reader interested in the general programming capabilities of the 1706.

TABLE 1. 1706 ADDRESSES AND OPERATIONS

W*			COMPUTER INSTRUCTION	
1706 No. 3	1706 No. 2	1706 No. 1	Input to A	Output from A
0C	07	02	Direct Input	Direct Output
0D	08	03	Terminate Buffer; 1706 Current Address	Function (See 1706 Function Table)
0E	09	04	1706 Status	Buffered Output
0F	0A	05	1706 Current Address	Buffered Input

* The left digit is binary, the right digit hexadecimal.

TABLE 2. 1706 FUNCTIONS

Bit in A Register	Meaning
A15 $\begin{cases} = 1 \\ \\ = 0 \end{cases}$	Set condition for ones in bits A14 - A00
	Clear condition for ones in bits A14 - A00
A14 - A01	(Not defined)
A00	Enable Interrupt on 1706 End of Operation

Addresses

Bits 11-15 of the Q register, called W, are used to select the desired 1706. Bits 00-10 of Q are used to select the peripheral device. The 1706 provides a W=0 signal to devices connected to it. Bit 15, the continue bit, is ordinarily zero when using the 1706. However, this bit may be used by:

1) Addressing the device with the correct code and Q15 set to "0".

2) Using Q15 = 1 for all succeeding addresses to this device.

3) Using Q15 = 0 and a new address to access a different device.

The 1706 interprets an access attempt with Q15 = 1 as a direct input following an Input to A instruction and as a direct output following an Output from A instruction.

Operations

Besides selecting a particular 1706, the W field of Q, combined with a 1704 Input or Output instruction, specifies an operation. The function operation may be further modified by the contents of the A register. Tables 1 and 2 list the addresses, the operations, and the functions. Because W is a 5-bit field and the upper bit (the Continue bit) has a separate use, W is written as two digits; the left digit is binary, the right digit is hexadecimal.

Operations Defined by W and Input to A

Direct Input: Whenever the computer executes an Input instruction to a 1706 with the W field of Q selecting direct input, (Q) is stored in the 1706 and presented to the devices attached to the 1706, and one 16-bit word is transferred into the A register from the selected device. The word may be a data word or the status of the device on the 1706. This mode of operation is identical in every way to that on the AQ channel. The Continue bit (Q15) functions as described under Addresses and in connection with the device being used. If an attempt is made to execute a direct input when the 1706 is busy, the 1706 responds with a Reject. For this reason, it is impossible to determine the status of a device connected to the 1706 during a buffer operation.

Terminate Buffer, 1706 Current Address: This code terminates a buffered operation and loads into the A register the address of the current word being transferred. The Terminate Buffer operation is intended primarily to terminate hung-up input buffers and in this case the A register contains the address of the next word to have been transferred. Otherwise, the current address may be the address of the last word transferred or of the next word to be transferred, depending on when the Terminate Buffer reaches the 1706 with respect to the timing of the data transfer of the peripheral device. A buffered operation initiated by a protected instruction cannot be terminated by a nonprotected Terminate Buffer instruction.

1706 Status: This code is a status request which loads into the A register a status reply word showing the current operating conditions of the 1706. A non-protected status request is rejected during a buffer operation initiated by a protected instruction.

1706 Current Address: This code is a status request which loads into the A register the address of the current word being transferred. A non-protected request for the current address is rejected during a buffer operation initiated by a protected instruction.

Operations Defined by W and Output from A

Direct Output: Whenever the computer executes an Output instruction to a 1706 with the W field of Q selecting a direct output, (Q) is stored in the 1706 and presented to the devices attached to the 1706, and one 16-bit word is transferred from the A register to the selected device. This mode of operation is identical in every way to that on the AQ Data Channel. The Continue bit (Q15) functions as described under Addresses and in connection with the device being used. If an attempt is made to do a direct output when the 1706 is busy, the 1706 responds with a Reject.

Function: This code enables and disables Interrupt on End of Operation and clears the interrupt condition, depending upon the contents of the A register. If A15 and A00 = 1, the interrupt is enabled. If A15 = 0, A00 = 1, the interrupt is disabled. When a function is executed with A00 = 1, the interrupt condition is cleared. Thus either reselecting (enabling) the interrupt or disabling the interrupt clears this interrupt condition. A non-protected function instruction is rejected during a buffer operation initiated by a protected instruction.

Buffered Output on the 1706: A buffered output is initiated when the computer executes an Output instruction and the W field of Q selects a buffered output. (Q) is stored in the 1706, then placed on the 1706 channel and the contents of A are transferred to the 1706. The contents of A specifies the first word address minus 1 (FWA-1) of the block to be transferred. The contents of location FWA-1 specifies the last word address plus one (LWA+1) of the block to be transferred. The 1706 begins the data transfer by raising the Write signal to the device. The device responds within 4 μsec by raising the Reply signal to the 1706. The 1706 then advances to the next data word, repeating this cycle until the block of data has been transferred. If the 1706 receives a Reject, it indefinitely repeats the transfer of the word until the word is accepted. The address is not reissued to storage. The 1706 does not generate an Internal Reject. If an attempt is made to establish a buffered output when the 1706 is Busy, the 1706 responds with a Reject.

Buffered Input on the 1706: A buffered input is initiated when the computer executes an Output instruction and the W field of Q selects a buffered input. (Q) is stored in the 1706, then placed on the 1706 channel and the contents of A is transferred to the 1706. The contents of A specifies the location of the first word address minus one (FWA-1) of the block where data is to be stored. The contents of location FWA-1 specifies the last word address plus 1 (LWA+1) of this block. The 1706 begins the data transfer by raising the Read signal to the device. The device responds within 4 μsec by raising the Reply signal to the 1706. The 1706 then advances to the next data word and repeats this cycle until the block of data has been transferred. If the 1706 receives a Reject from the device, it repeats the transfer of the word indefinitely until the word is accepted. The 1706 does not generate an Internal Reject. If an attempt is made to establish a buffered input when the 1706 is Busy, the 1706 will respond with a Reject.

Status Response

1706 Operating Status

Table 3 lists the bits which may be set in the A register following a status request for 1706 operating conditions. The information following Table 3 defines these bits.

TABLE 3. 1706 STATUS RESPONSE BITS

Bit Set In A Register	Meaning
0	Ready
1	Busy
2	Interrupt
3	(Not used)
4	End of Operation
5	(Not used)
6	Program Protect Fault
7	(Not used)
8	Device Reject
9	Device Reply
10 - 15	(Not used)

Ready (Bit 0 = 1) - This bit is set when power is on.

Busy (Bit 1 = 1) - This bit is set from the time the 1706 accepts an output word from the computer initiating a block transfer until the block transfer is terminated, or during a direct operation.

Interrupt (Bit 2 = 1) - An End of Operation Interrupt is being sent to the computer from the 1706.

End of Operation (Bit 4 = 1) - A buffer transfer input or output has been completed.

Program Protect Fault (Bit 6 = 1) - A reference to computer storage caused a program protect fault. The 1700 Reference Manual defines the conditions causing a program protect fault in its Interrupt Section.

Device Reject (Bit 8 = 1) - This bit, if set, means the peripheral device rejected the last word transfer attempted from the 1706.

Device Reply (Bit 9 = 1) - This bit, if set, means the peripheral device accepted the last word transfer attempted from the 1706.

1706 Current Address

This status shows the address of the current word being transferred. It is loaded into the A register following a Terminate Buffer or a 1706 Current Address operation.

Programming Considerations

1704 Instruction	Q Register	Step	Action
LDQ	Selected 1706 Status Request	1)	Initiate operating status check of desired 1706
INP		2)	A register now contains the operating status of the desired 1706
		3)	Check status in A for Ready and Not Busy
LDQ	W = Direct Input on selected 1706, Bits 0-10 specify status request for equipment	4)	Initiate status check of equipment to be used
INP		5)	A register now contains the equipment status
		6)	Check equipment status for desired conditions.
		7)	Repeat 4-6 for station and unit, if necessary.
LDQ	Selected 1706 Function	8)	Initiate selection or clearing of Interrupt on End of Operation.
LDA		9)	Load A with desired operation
OUT		10)	Interrupt on End of Operation is now enabled or disabled. Any existing interrupt is cleared.
LDQ	W = Direct Output on selected 1706. Bits 0-10 specify an operation on the equipment or station.	11)	Initiate selection of peripheral equipment operating conditions and interrupts.
LDA		12)	If necessary, load A with the code further specifying the operation indicated by (Q).
OUT		13)	Execute Output from A instruction
		14)	Repeat 11-13 until all desired operating conditions are specified.
	For a Direct Input or Output of Data		
LDQ	W = Direct Input or Direct Output on selected 1706. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	15D)*	Select desired type of I/O.
LDA		16D)	If doing a direct output, load the data into A; if direct input, skip this step.

* D indicates a step for the direct transfer of data.

1704 Instruction	Q Register	Step	Action
INP or OUT		17D)	Execute 1704 Input to A or Output from A, depending on desired direction of data transfer.
		18D)	Skip to 19)
For a Buffered Transfer of Data			
LDQ	W = Buffered Input or Buffered Output on selected 1706. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	15B)*	Select desired type of buffered I/O.
LDA		16B)	Load A with the FWA-1 of the buffer area. The contents of memory at this address must contain the LWA + 1 of the buffer area.
OUT		17B)	The buffered transfer is now initiated and under control of the 1706.
		18B)	Go to step 19).
		19)	Status the converter (as in steps 1-3, checking for desired conditions, or by using the 1706 current address status) or proceed with the main program until an interrupt occurs. Using interrupts takes advantage of the capabilities of the buffered data channel to do I/O without hanging up the computer. It is not possible to status a device connected to the 1706 as long as the 1706 is Busy.

*B indicates a step for the buffered transfer of data.

COMMENTS

If a buffered operation becomes hung up, LDQ with W selecting Terminate Buffer for the appropriate 1706, and execute an INP instruction. The buffered operation is terminated and the current address is sent to A. The program can check this address and take the desired action.

One method of determining if the 1706 is hung up is to select the device's Interrupt on End of Operation. When the interrupt is recognized, check the operating status of the 1706. If the 1706 is still Busy, the buffered operation is hung up. Do a status check of the 1706 current address. If the current address does not equal the LWA + 1, the equipment is hung up.

A second method is to do a status check of the 1706 current address. Then wait until at least one more word should have been transferred and again check the current address. If it is unchanged, the buffered operation is hung up. This method requires knowing instruction execution times and the rate of data transfer.

If an INP or OUT instruction results in a Reject, the program proceeds as described in connection with these instructions in the computer reference manual.

1706
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CONTENTS

1716 COUPLING DATA CHANNEL

INTRODUCTION

This section describes the CONTROL DATA* 1716-A Coupling Data Channel, its physical system and programming information. There is no operating information, as there are no controls or indicators on the 1716 other than the Program Protect Switches, which are covered under Program Protection.

FUNCTIONAL DESCRIPTION

System Relationship

The 1716 provides a bidirectional 16-bit data path between two 1704 Computers, each with a 1705 Interrupt Data Channel. It also provides a Buffered Data Channel to which may be attached up to eight peripheral equipments, with a maximum word transfer rate of 900 kc. Figure 1 shows the relationship between the 1716 and other equipments.
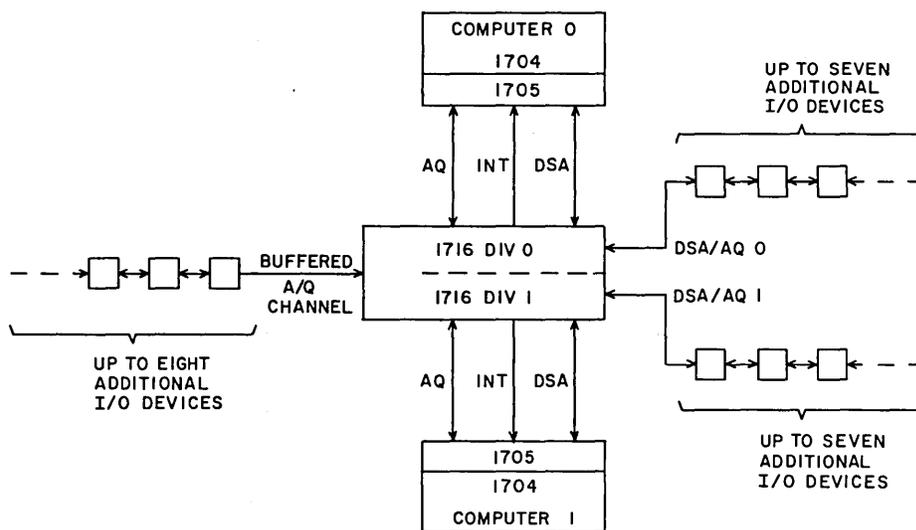
Figure 1. Typical 1716 Configuration

The 1716 is divided into two sections, called division 0 and division 1. Each of these sections is connected to a 1705 Interrupt Data Channel and a 1704 computer. The computer attached to division 0 will be called computer 0, the one on division one, computer 1. A maximum of three 1716's may be connected to a 1705 Interrupt Data channel. A 1706 Buffered Data Channel may replace any or all of the 1716's.

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With the exception of the Program Protect switches, the 1716 is controlled entirely by the Input to A and Output from A instructions from the 1704. The operations for the 1716 are the same as those for the 1706 BDC, with the addition of a Buffered Transfer operation. This operation allows the sending of data directly between the storage of the two connected computers, or from one portion of one computer's storage to another portion of the same computer's storage. In response to an I/O instruction from either computer (and the contents of the respective Q registers) the 1716 connects the computer to the other computer, or to one of the peripheral equipments, and sends the appropriate Read or Write signal; it then controls the transfer of the information. On buffered operations, the 1716 obtains access to storage through the Direct Storage Access Bus of either computer.

Interrupt

The 1716 has one interrupt line to each computer. The interrupts are generated by End of Operation (if enabled) or by matching conditions in the flag and mask bits. The End of Operation interrupt is sent to the computer that initiated the operation. The Flag/Mask interrupt is sent to the computer having a mask bit matching the corresponding flag bit. The flags are shared while each computer has its own mask bits. Use of the interrupt conditions is explained in detail under the Function operation.

Program Protection

The 1716 has two Program Protect switches, one associated with each division. When a switch is ON, only those I/O instructions having a "1" on the protect line will be recognized. An instruction not having a "1" on the protect line will be rejected. The Function instruction will not be rejected; it will be ignored. When the switch is OFF, protected and unprotected instructions will be recognized.

Reply/Reject

The 1716 responds within 4 microseconds to an Input to A or Output from A instruction with either a Reply or a Reject signal. A Reply will be sent whenever the computer can perform the requested operation. The following conditions will cause a Reject to be sent:

1) a program protect violation

2) the 1716 is Busy (if attempting a direct or buffered operation)

3) a device returns a Reject (direct output or input)

If the computer receives no response, it will generate an internal Reject. Function is not rejected on a program protect violation.

PROGRAMMING

Summary of Programming Information

Tables 1, 2, and 3 are a summary of the information necessary to program the 1716. Explanations of the information presented here can be found in the following sections. The tables here are intended as a quick reference for the experienced programmer, and a summary for the reader interested in the general programming capabilities of the 1716.

TABLE 1. 1716 ADDRESSES AND OPERATIONS

W*			COMPUTER INSTRUCTION	
1716 #3	1716 #2	1716 #1	INPUT TO A	OUTPUT FROM A
0B	06	01		Buffered Transfer
0C	07	02	Direct Input	Direct Output
0D	08	03	Terminate Buffer 1716 Current Address	Function (See 1716 Function Table)
0E	09	04	1716 Status	Buffered Output
0F	0A	05	1716 Current Address	Buffered Input

*The left digit is binary, the right digit hexidecimal.

TABLE 2. 1716 FUNCTIONS

BIT IN A REGISTER	MEANING
A15=1	Set condition for ones in A14-A00*
A15=0	Clear condition for ones in A14-A00*
A14	Flag 4
A13	Flag 3
A12	Flag 2
A11	Flag 1
A10	Flag 0
A09	Mask 4
A08	Mask 3
A07	Mask 2
A06	Mask 1
A05	Mask 0
A04	(Not defined)
A03	Reserve flag
A02	(Not defined)
A01	(Not defined)
A00	Interrupt on 1716 End of Operation*

*Functions also used in the 1706.

TABLE 3. 1716 STATUS BITS

BIT SET IN A REGISTER	MEANING
15	(Not used)
14	Flag 4
13	Flag 3
12	Flag 2
11	Flag 1
10	Flag 0
9	Device Reply*
8	Device Reject*
7	(Not used)
6	Program Protect Fault*
5	(Not used)
4	End of Operation*
3	Reserve Flag
2	Interrupt*
1	Busy*
0	Ready*

*Status also used in the 1706.
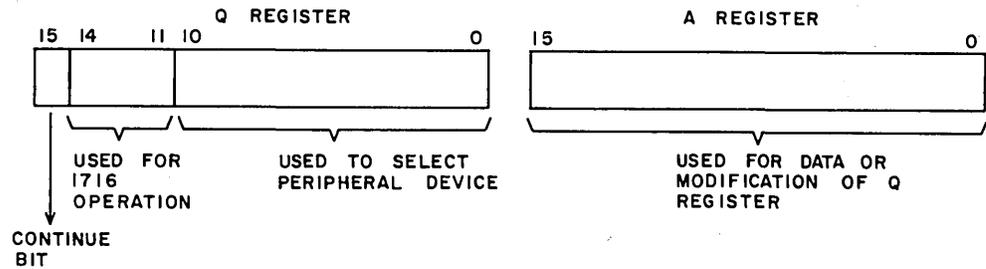
Figure 2. 1700 Q and A Registers

Bits 11-15 of the Q register are used to select the desired 1716 operation, while bits 00-10 are used to select the desired peripheral device. (See Figure 2). The 1716 provides a W = 0 signal to devices connected to it. Bits 11-14 are used to define 1716 operations (see Table 1) and bit 15 is the continue bit, * used as follows:

1) Address the device with Q15 = 0 and the remainder of Q set to select that device; the device is then connected.

2) All succeeding addresses with Q15 = 1 will be recognized by this device. Thus 15 bits of addressing are available to the device.

3) The next address with Q15 = 0 will disconnect the device unless it is the address of that device.

The 1716 will interpret an address with Q15 = 1 as a direct input on an Input to A instruction, and as a direct output on an Output from A instruction.

Operations

Besides selecting a particular 1716, the W field of Q, combined with a 1704 Input to A or Output from A instruction, specifies an operation. The Function operation may be further modified by the contents of the A register. Tables 1 and 2 list the addresses, operations, and functions. Because W is a 5-bit field and bit 15 is used as a Continue bit, W is expressed as a 2-digit number: the right digit is hexadecimal (4 bits), the left digit binary (1 bit).

Operations Defined by W and Input to A

Direct Input: Whenever the computer executes an Input to A instruction to a 1716 with the W field of Q selecting a direct input, Q is stored in the 1716 and presented to the devices attached to the 1716 and one 16-bit word is transferred into the A register from the selected device. The word may be a data word or the status of a device on the 1716. This mode of operation is in every way identical to that of the AQ channel. The Continue bit functions as described previously. If an attempt is made to do a direct input when the 1716 is busy, the 1716 will respond with a Reject. It is therefore impossible to status a device on the 1716 during a buffered operation.

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*This only on certain devices. The 1718 is one such device.

<u>Terminate Buffer, 1716 Current Address:</u> This terminates a buffered opera-
tion and loads the current address of the word being transferred into the A
register. This instruction is intended to terminate hung-up input buffers,
and in this case the A register will contain the address of the next word to be
transferred. Otherwise, the address sent may be either that of the last
word or the next word. Which one will depend on the timing of the 1704/1716
device; i. e. , when the instruction reaches the 1716.

<u>1716 Status:</u> This operation will load the status word from the 1716 into the
A Register of the computer. Table 3 lists the bits in the status word. The
following list explains their meaning.

Flag 4 (Bit 14 = 1) - Shared flag 4 is set. *
Flag 3 (Bit 13 = 1) - Shared flag 3 is set.
Flag 2 (Bit 12 = 1) - Shared flag 2 is set.
Flag 1 (Bit 11 = 1) - Shared flag 1 is set.
Flag 0 (Bit 10 - 1) - Shared flag 0 is set.

Device Reply (Bit 9 = 1) - The peripheral device accepted the last word
transfer attempted from the 1716.

Device Reject (Bit 8 = 1) - The peripheral device rejected the last word
transfer attempted from the 1716.

Program Protect Fault (Bit 6 = 1) - A reference to computer storage has
caused a program protect violation.

End Of Operation (Bit 4 = 1) - A buffered input, output, or transfer has
been completed.

Reserve Flag (Bit 3 = 1) - The reserve flag for this computer is set. This
indicates that the other computer is not using the 1716.

Interrupt (Bit 2 = 1) - An interrupt has been sent from the 1716 to the
computer.

Busy (Bit 1 = 1) - This bit is set from the time the 1716 accepts an output
word from the computer initiating a block transfer until the transfer is
completed, or during a direct input or output operation.

Ready (Bit 0 = 1) - The power is on.

<u>1716 Current Address:</u> This code will cause the address of the current word
being transferred on a buffered operation to be loaded into the A register of
the computer requesting the status. This same word is also loaded into the
A register following a Terminate Buffer operation.

<div align="center">NOTE</div>

Status requests are never rejected on the 1716
unless a program protect violation has occurred.

---

*Flags are explained in more detail under 1716 Function.

Operations Defined by W and Output from A

Direct Output: Whenever the computer executes an Output from A instruction with W selecting direct output, Q is stored in the 1716 and sent to the attached peripheral devices, and one 16-bit word is transferred from the A register to the selected device. This mode of operation is identical in every way to that of the AQ Channel. The Continue bit functions as described before. If an attempt is made to do a direct output when the 1716 is busy, the 1716 responds with a Reject.

Function: This code transmits the function word to the 1716. Table 2 lists the bits in the word. The following list explains their meaning.

(Bit 15 = 1) - If bit 15 is a "1", those conditions indicated by "1's" in bits 0 through 14 will be set in the 1716. Bits not set will not be affected by bit 15.

(Bit 15 = 0) - If bit 15 is a "0", those conditions indicated by "1's" in bits 0 through 14 will be cleared in the 1716. Bits not set will not be affected by bit 15.

```
Flag 4  (Bit 14 = 1) ⎤   The flag and mask bits are used to send interrupts
Flag 3  (Bit 13 = 1) │   between the two computers. The five flag bits are
Flag 2  (Bit 12 = 1) │   shared by both computers. Each computer has its
Flag 1  (Bit 11 = 1) │   own set of mask bits. If a mask bit and its correspond-
Flag 0  (Bit 10 = 1) ⎦   ing flag bit are both set (for example mask 1 and flag 1)
Mask 4  (Bit 9 = 1)  ⎤   an interrupt will be sent to the computer whose mask
Mask 3  (Bit 8 = 1)  │   bit is set. The interrupt will be cleared by the End
Mask 2  (Bit 7 = 1)  │   of Operation interrupt, or if the flag or mask bit
Mask 1  (Bit 6 = 1)  │   causing it is cleared.
Mask 0  (Bit 5 = 1)  ⎦
```

Reserve flag (Bit 4 = 1) - One reserve flag bit is associated with each computer; it is set and cleared in the same manner as the other flag bits. The two reserve flags cannot be set at the same time; that is, when one is set, the other will not respond to a function signal intended to set it. The function will not be rejected. The reserve flag can be cleared by a function from the computer that set the flag, or by a Master Clear or Terminate Buffer operation from either computer. The intended purpose of the reserve flag bit is to indicate to the computer whether or not the other computer is using the 1716. Before issuing instructions to move data, a function to set the reserve flag should be executed, followed by a status instruction. If the reserve flag is set, it indicates the other computer is not using the 1716; i.e., its flag is not set.

Interrupt on End of Operation (Bit 0 = 1) - An interrupt will be sent at the end of a buffered operation. The interrupt will be sent to the computer that initiated the operation. Clearing this bit will also clear the interrupt.
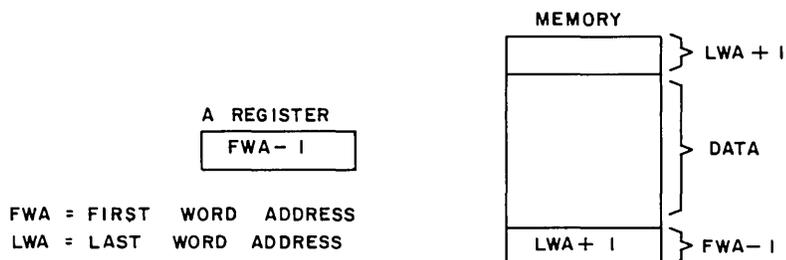
NOTE

Function requests are never
rejected by the 1716.

```
                                         MEMORY
                                      ┌──────────┐ ⎫
                                      │          │ ⎬ LWA + I
                  A REGISTER          ├──────────┤ ⎭
                 ┌───────────┐        │          │ ⎫
                 │  FWA- I   │        │          │ ⎪
                 └───────────┘        │          │ ⎬ DATA
                                      │          │ ⎪
    FWA = FIRST  WORD  ADDRESS        │          │ ⎭
    LWA = LAST   WORD  ADDRESS        ├──────────┤
                                      │  LWA+ I  │ ⎬ FWA- I
                                      └──────────┘
```

Figure 3. Address Arrangement for Buffered Input and Output

Buffered Output: A buffered output is initiated when the computer executes
an Output from A instruction and the W field of Q selects a buffered output.
(See Figure 3.) Q is stored in the 1716, then placed on the 1716 channel,
and the contents of A is transferred to the 1716. The contents of A specifies
the first word address minus one (FWA-1) of the block to be transferred.
The contents of location FWA-1 specifies the last word address plus one
(LWA+1) of the block to be transferred. The 1716 begins the data transfer
by raising the Write signal to the device. The device responds within four
microseconds by raising the Reply signal to the 1716. The 1716 then advances
to the next data word, repeating this cycle until the block of data has been
transferred.

If the 1716 receives a Reject, it indefinitely repeats the transfer of the word
until the word is accepted. The address is not reissued to storage. The
1716 does not generate an internal reject. If an attempt is made to establish
a buffered output when the 1716 is busy, the 1716 responds with a Reject.

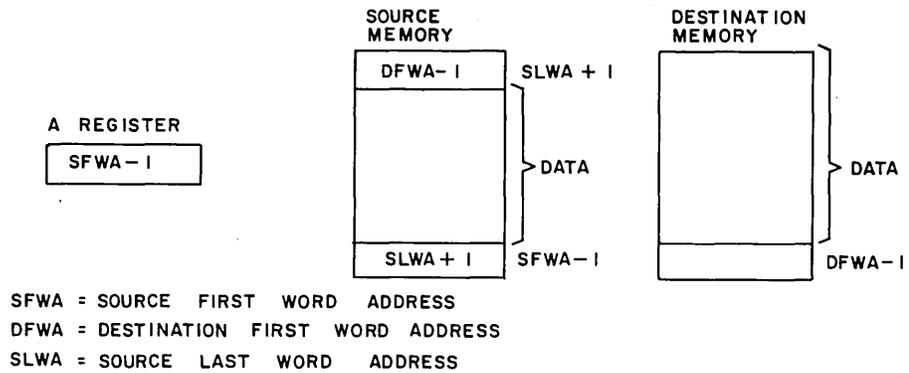Buffered Input: A buffered input is initiated when the computer executes
an Output from A instruction and the W field of Q selects a buffered input.
(See Figure 3.) Q is stored in the 1716, then placed on the 1716 channel
and the contents of A is transferred to the 1716. The contents of A specifies
the location of the first word address minus one (FWA-1) of the block where
the data is to be stored. The contents of the location FWA-1 specifies the
last word address plus one (LWA+1) of this block. The 1716 begins the data
transfer by raising the Read signal to the device. The device responds within four
microseconds by raising the Reply signal to the 1716. The 1716 then advances
to the next data word and repeats this cycle until the block of data has been
transferred.

If the 1716 receives a Reject from the device, it repeats the transfer of the
word indefinitely until the word is accepted. The 1716 does not generate an
internal reject. If an attempt is made to establish a buffered input when the
1716 is busy, the 1716 will respond with a Reject.

```
                        SOURCE                    DESTINATION
                        MEMORY                    MEMORY
                     ┌──────────┐                ┌──────────┐
                     │  DFWA- I │  SLWA + I    ╮ │          │ ╮
    A  REGISTER      ├──────────┤            ╮  │          │  │
  ┌──────────────┐   │          │            │  │          │  │
  │   SFWA- I    │   │          │ ╮DATA       ╮DATA        │  ╮DATA
  └──────────────┘   │          │ │            │          │  │
                     │          │ ╯            │          │  │
                     ├──────────┤            ╯  │          │ ╯
                     │  SLWA + I│  SFWA- I    ╯ ├──────────┤
                     └──────────┘                │          │  DFWA- I
                                                 └──────────┘
```

SFWA = SOURCE FIRST WORD ADDRESS
DFWA = DESTINATION FIRST WORD ADDRESS
SLWA = SOURCE LAST WORD ADDRESS

Figure 4. Address Arrangement for Buffered Transfer

Buffered Transfer: In this mode, data is transferred directly to/from computer core storage via the 1716 (see Figure 4).   The transfer is initiated by one computer executing an Output from A instruction with the W field of Q selecting a buffered transfer (see Table 4).   The transfer is accomplished by defining the bounds of the source data and the FWA-1 of the destination location.   The output to the 1716 initiates the buffer transfer and sends via the A register the source data FWA-1 (SFWA-1).   The contents of SFWA-1 is the source data LWA+1 (SLWA+1).   The contents of SLWA+1 is the destination data FWA-1 (DFWA-1).   Bit 15 of all these addresses refers to the "other" computer if it is set; "this" computer if not set.   It is thus possible to make a block transfer within a single computer's core storage.   All flag, mask, and status functions of the 1716 are available in the buffer transfer mode.

NOTE

On all buffered operations,
bit 15 of the address is used
to determine which computer
is to send or receive the data.
If bit 15 is a "1", it means the
"other" computer; if bit 15 is
a "0", it means "this" computer.

Care should be taken to keep
the starting and ending addresses
of blocks of data to be transferred
within the following limits:

0000 - 7FFF, or
8000 - FFFF

If, during the transfer, the range
of addresses crosses either of
the above boundaries (7FFF to
8000, or FFFF to 0000), bit 15
will change value and data may be
sent to or received by the wrong
computer.

**Programming
Considerations**

1704 Instruction	Q Register	Step	Action
LDQ	Selected 1716 Status Request	1)	Initiate operating status check of desired 1716.
INP		2)	A register now contains the operating status of the desired 1716.
		3)	Check status in A for Ready and Not Busy.
LDQ	Selected 1716 Function	4)	Initiate setting of reserve flag.
LDA		5)	Set reserve flag.
OUT		6)	If reserve flag is available, it will be set.
		7)	Repeat 1-3 to check for reserve flag set. If not set, wait and repeat 1-6.
LDQ	W = Direct Input on selected 1716, Bits 0-10 specify status request for equipment	8)	Initiate status check of equipment to be used.
INP		9)	A register now contains the equipment status.
		10)	Check equipment status for desired conditions.
		11)	Repeat 8-10 for station and unit, if necessary.
LDQ	Selected 1716 Function	12)	Initiate selection or clearing of Interrupt on End of Operation.
LDA		13)	Load A with desired operation.
OUT		14)	Interrupt on End of Operation is now enabled or disabled. Any existing interrupt is cleared.
LDQ	W = Direct Output on selected 1716. Bits 0-10 specify an operation on the equipment or station.	15)	Initiate selection of peripheral equipment operating conditions and interrupts.
LDA		16)	If necessary, load A with the code further specifying the operation indicated by (Q).
OUT		17)	Execute Output from A instruction
		18)	Repeat 15-17 until all desired operating conditions are specified.

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1704 Instruction	Q Register	Step	Action
		For a Direct Input or Output of Data	
LDQ	W = Direct Input or Direct Output on selected 1716. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	19D*)	Select desired type of I/O.
LDA		20D)	If doing a direct output, load the data into A; if direct input, skip this step.
INP or OUT		21D)	Execute 1704 Input to A or Output from A, depending on desired direction of data transfer.
		22D)	Skip to 22B.
		For a Buffered Input or Output of Data	
LDQ	W = Buffered Input or Buffered Output on selected 1716. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	19B†)	Select desired type of buffered I/O.
LDA		20B)	Load A with the FWA-1 of the buffer area. The contents of memory at this address must contain the LWA + 1 of the buffer area.
OUT		21B)	The buffered transfer is now initiated and under control of the 1716.
		22B)	Status the converter (as in steps 1-3, checking for desired conditions, or by using the 1716 current address status) or proceed with the main program until an interrupt occurs. Using interrupts takes advantage of the capabilities of the buffered data channel to do I/O without hanging up the computer. It is not possible to status a device connected to the 1716 as long as the 1716 is Busy.

* D indicates a step for the direct transfer of data.

† B indicates a step for the buffered input or output of data.

Buffered Transfer

The buffered transfer is programmed in much the same way as the buffered input or buffered output. There are four basic transfers:

1) "this" computer to "this" computer
2) "this" computer to "other" computer
3) "other" computer to "this" computer
4) "other" computer to "other" computer

Bit 15 of the 3-address word determines the type of transfer.

1) this to this   - Bit 15 of SFWA*, SLWA+1, and DFWA-1 is zero. This transfer can be used to relocate data in memory.

Computer 1   Computer 2

Q = W For Buffer XFER
A = | O | SFWA-11 |
INSTR = OUT

SFWA-1 | O | SLWA+1 |
       | DATA |
       | OUT |

SLWA+1 | O | DFWA-1 |

DFWA | DATA |
       | IN |
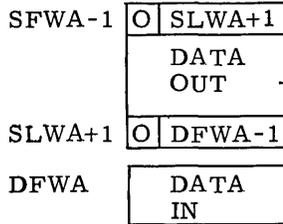
2) this to other   - Bit 15 of SFWA-1, SLWA+1 is zero. Bit 15 of DFWA-1 is one. This will transfer data to the other computer and store it beginning at DFWA.

Computer 1   Computer 2

Q = W For Buffer XFER
A = | O | SFWA-1 |
INSTR = OUT

SFWA-1 | O | SLWA+1 |
       | DATA | DFWA | DATA |
       | OUT | | IN |

SLWA+1 | 1 | DFWA-1 |
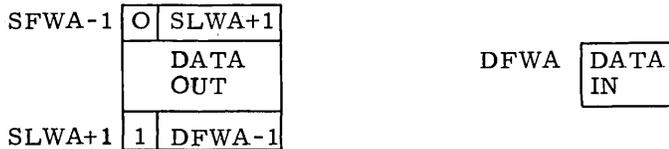
3) other to this   - Bit 15 of SFWA-1 is a one, SLWA+1 is a zero. Bit 15 of DFWA-1 is one. This will move data from the other computer and store it in this computer, beginning at DFWA. Use of this transfer requires some prearranged programming so this computer knows where in the other computer the data to be transferred is located.

Computer 1   Computer 2

Q = W For Buffer XFER
A = | 1 | SFWA-1 |
INSTR = OUT

```
DFWA │DATA│                          SFWA-1 │O│ SLWA+1│
     │IN  │                                 │  DATA  │
                                            │  OUT   │
                                    SLWA+1  │1│ DFWA-1│
```

4) other to other   -   Bit 15 of SFWA-1 is a one, SLWA+1 is a zero. Bit 15 of DFWA-1 is a zero. This transfer will move data in the other computer's memory. This requires some prearranged programming so this computer knows where the other computer's data is initially

```
Computer 1                          Computer 2

Q = W For Buffer XFER               SFWA-1 │O│ SLWA+1│
  A =│1│ SFWA-1│                            │  DATA  │
INSTR = OUT                                 │  OUT   │
    THIS                            SLWA+1  │O│ DFWA-1│

                                    DFWA    │ DATA   │
                                    OTHER   │ IN     │
```

Because of the dependence of the buffered transfer on the system programming, no attempt is made to give a specific sample program. Cases 3 and 4 will not be discussed further because of the special programming required to execute such transfers.

Case 1: "This to this" requires no particular programming effort other than properly establishing the addresses, all with bit 15 equal to zero.

Case 2: "This to other" may be done without any special preparation by merely sending the data at any time to the other computer. It is preferable to send some control or identification word as part of the data to allow the other computer to determine its origin.

If some notification or communication is desired, the flags and masks may be used; this computer can send an interrupt to the other using the flag/mask interrupt, or the other computer can status the flags. Both methods require some prearranged meaning for the flag and mask bits. All mask, flag, and status functions are available to both computers during a buffered transfer.

* SFWA = Source First Word Address
  SLWA = Source Last Word Address
  DFWA = Destination First Word Address

COMMENTS

If a buffered operation becomes hung up, LDQ with W selecting Terminate Buffer for the appropriate 1716, and execute an INP instruction. The buffered operation is terminated and the current address is sent to A. The program can check this address and take the desired action.

One method of determining if the 1716 is hung up is to select the device's Interrupt on End of Operation. When the interrupt is recognized, check the operating status of the 1716. If the 1716 is still Busy, the buffered operation is hung up. Do a status check of the 1716 current address. If the current address does not equal the LWA + 1, the equipment is hung up.

A second method is to do a status check of the 1716 current address. Then wait until at least one more word should have been transferred and again check the current address. If it is unchanged, the buffered operation is hung up. This method requires knowing instruction execution times and the rate of data transfer.

If an INP or OUT instruction results in a Reject, the program proceeds as described in connection with these instructions in the computer reference manual.

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1718-A SATELLITE COUPLER

INTRODUCTION

The CONTROL DATA* 1718-A Satellite Coupler acts as a data path between a Control Data 3000 Series computer I/O channel and a Control Data 1704 Computer I/O channel (1705, 1706, or 1716). The 1718 receives and transfers 12-bit data words between a 3000 Series and a 1704 Computer. The data is not converted, but data bit positions can be reformatted.

A CONTROL DATA 1716 Coupling Data Channel may serve as an interface between the 1718 and 1704 (Figure 1, c); in this case, the 1718 can establish a communication path with two 1704 Computers (one at a time). 1704 programming determines which 1704 Computer will receive data from or send data to the 3000 Series computer during a given operation.

The 1718 coupler contains the circuitry necessary to transfer data, check parity, receive and transmit control signals and interrupt either computer program.

This section contains the description, operating details, and programming information for the 1718 Satellite Coupler.

FUNCTIONAL DESCRIPTION

The 1718 provides a bi-directional path for data transfer between the 3000 Series computer and a 1704 Computer. The coupler consists of two divisions. Division A receives information from and transmits information to the 3000 Series computer. Division B serves the 1704 in the same manner (Figure 1, a).

To transfer data from the 3000 Series computer to the 1704, division A writes into the Data register and division B reads from the Data register. The data travels from the 3000 Series computer to division A, from division A to division B, and from division B to the 1700 channel (1705, 1706, or 1716). To transfer data from the 1704 to the 3000 Series computer, division B writes into the Data register and division A reads from the Data register. Data travels in the same path but in the opposite direction.

The operation performed by each division corresponds directly to the operation which the associated computer performs. If the 3000 Series computer performs a Write operation in conjunction with the 1718, then division A performs a Write operation. If the 1704 performs a Write operation in conjunction with the 1718, then division B performs a Write operation. Conversely when the 3000 Series computer and division A perform a Write operation, the 1704 and division B perform a Read operation. Division A sends an End of Record signal to the 3000 Series computer when the 1704 terminates a division B Write operation.

---

*Registered trademark of Control Data Corporation

1
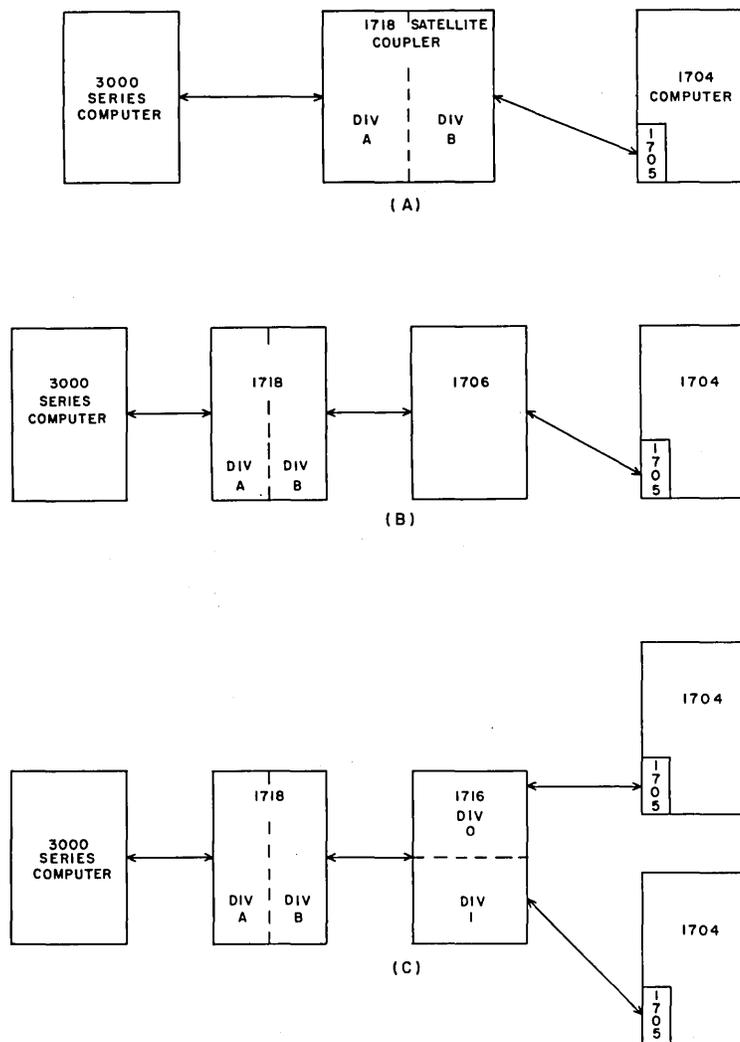
Figure 1. 1718 System Relationship

Each division contains an 8-bit Mask register and shares an 8-bit Flag register. Function codes from the 3000 Series computer set/clear bits in Mask A and function codes from the 1704 set/clear bits in Mask B. The Flag register can be set or cleared by function codes from either computer.

The Flag register is a means of communicating between a 3000 Series and a 1704 Computer. Either computer can use the Flag register to indicate to the other computer that an input or output operation has been initiated, a data transmission has finished, or some other condition exists. The designated use of each flag bit is defined by the specific program being used.

The Flag and Mask registers may act as an interrupt device. Together they allow either computer to initiate an operation and inform the second computer that the first wants to transfer data. A "1", formed by 1 of the 8 bits in the Mask and the corresponding bit position in the Flag, sends an interrupt to the computer associated with the Mask which combined to form the "1" (Figure 2).
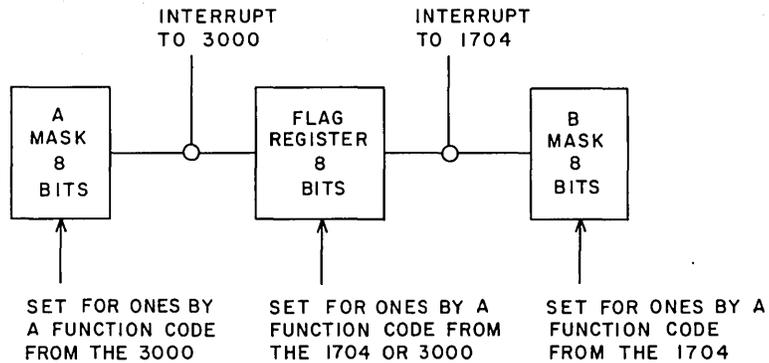
Figure 2. Mask-Flag Relationship

The Flag register may be used independently if the interrupt method of communication is not desired. By setting the Flag register for "1's" from one computer and checking status from the other, the Flag register can be used to communicate a condition from one computer to the other. The function codes and status conditions are described in detail in the Programming section.

8-Bit Character Mode

The transfer of 12-bit data word blocks between the 3000 Series and 1704 computers takes place with no conversion of the data. However, the 8-Bit Character mode function code (described in the Programming section) from the 1704 changes the data path for the bit positions in the 1704 I/O cable. If division A is writing and the Character mode is in effect, bits 0-5 from the 3000 Series computer pass to bits 0-5 of the 1704; bits 6-11 from the 3000 Series computer pass to bit positions 8-13 of the 1704 I/O cable. The reverse is true if division B is writing and division A is reading. If the 8-Bit Character mode is not in effect, data travels from bit positions 0-11 to 0-11 (Figure 3).
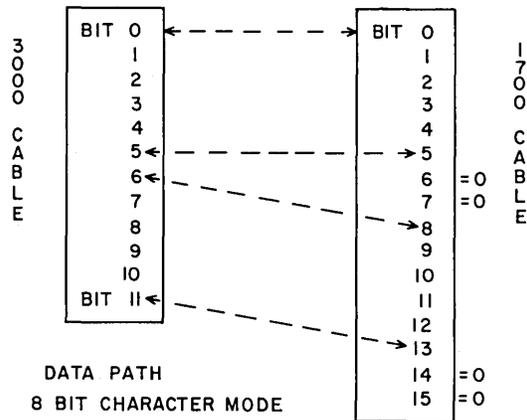
Figure 3. Data Path for 8-Bit Character Mode

The Character mode facilitates the transfer of 6-bit (0-5 and 6-11) character codes in the 3000 Series computer to an 8-bit format in the 1700 cable. The upper 2 bits of each 8-bit character (bits 6, 7, 14, and 15 on Figure 3) are "0's".

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Parity Error

A parity checker in division A checks for odd parity on all data, function codes, and connect codes sent from the 3000 Series computer. A parity bit accompanies data received by division A from the 3000 Series computer. If the state of the parity bit is incorrect as determined by the parity checker, the parity error status bit sets in both division B and division A status, and the PARITY ERROR indicator lights on the computer and the 1718.

A parity error during transmission of the connect code disables the Reply and no connection is made. A parity error on a function code prohibits execution of the code.

Program Protection

The 1718 contains a PROGRAM PROTECT switch. The PROTECTED position of the switch conditions division B to recognize and accept only those I/O instructions from the 1704 which have a "1" on the protect line. The 1718 rejects unrecognized instructions if the switch is in the PROTECTED position. If the switch is in the UNPROTECTED position, the 1718 recognizes both protected and unprotected instructions. The status of the 1718 can always be read, regardless of the PROGRAM PROTECT switch setting.

PROGRAMMING DIVISION A

The 3000 Series computer program controls division A of the 1718 coupler. The computer can initiate a Read or Write operation in division A by following the order of events listed below.

1) Clear
2) Connect
3) Check status
4) Function
5) Read/Write
6) Clear Flags and interrupts if they serve no further purpose

Clear

The 3000 Series computer can generate three types of clears in the 1718 coupler.

Power-On Master Clear - This clears all Flags and Masks and controls in both division A and B when power is applied to the coupler.

Master Clear - The 3000 Series computer physically attached to the 1718 can clear division A of all interrupt conditions with a Master Clear.

Function clears - 3000 Series computer function code clear bits set for "1's" in the Flag register and division A Mask register. Division A must be connected to perform the function clear.

Write

Division A performs a Write operation when the 3000 Series computer transfers data to the 1704. Division A cannot continue writing if division B drops the Read signal.

Read

Division A performs a Read operation when the 3000 Series computer receives data from the 1704. Division A sends an End of Record signal to the 3000 Series computer at the finish of 1704 transmission.

Division A Codes

Connect

To connect division A, the 3000 Series computer channel transmits a 12-Bit Connect code to the 1718. Division A must be connected before a data path is established between the computers and the connect code must match the switch setting on division A. Bits 9-11 are the significant bits in the connect code; bits 0-8 are not used (Figure 4).
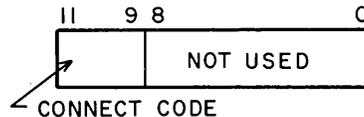
```
  II   9 8                    O
 ┌──┬──┬───────────────────────┐
 │  │7 │       NOT USED        │
 └──┴──┴───────────────────────┘
  CONNECT CODE
```

Figure 4. Connect Code

Division A generates a Reply to the 3000 Series computer channel upon completion of the connection. A parity error during the transmission of the connect code disables the Reply and returns a Parity Error signal which lights the indicators on the computer and 1718.

Status

Following the connection of division A, the 3000 Series computer may check the 12 status lines (Table 1).

TABLE 1. STATUS BITS

BIT NO.	DEFINITION (IF BIT = 1)
0	Flag 0
1	Flag 1
2	Flag 2
3	Flag 3
4	Flag 4
5	Flag 5
6	Flag 6
7	Flag 7
8	Division B Computer Running
9	Division B Read
10	Division B Write
11	Not Used

Flag 0-7 (Bits 0-7) - These 8 status bits show the state of the Flag register; e.g., if the flag bit is set, the status bit is "1".

Computer Running (Bit 8) - This status bit indicates that the 1704 Computer is running. If the 1718 is attached to a 1716, the computer running status bit applies only to the 1704 attached to division 1 of the 1716.

Division B Read (Bit 9) - This status bit indicates that division B is reading. The status bit becomes a "1" when division B executes a Start Input Data Transfer function or initiates a 1706/16 Buffer Input. The status bit drops when a Stop Data Transfer or Clear function is executed in division B or, if division B is connected to a 1706/16, when the Buffer Active signal drops.

Division B Write (Bit 10) - This status bit indicates that division B is writing. The status bit becomes a "1" when the 1704 attempts a Data Output to the 1718 or initiates a 1716/06 Buffer Output. The status bit drops when division B executes a Stop Data Transfer or clear function or, if division B is connected to a 1706/16, when the Buffer Active signal drops.

Division A Function Codes

When division A has been connected, a 12-bit function code from the 3000 Series computer may set up operating conditions defined in Table 2. The 12-bit function code is diagrammed in Figure 5.
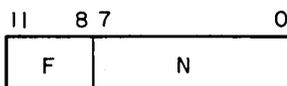
Figure 5. Format of the Function Code

A parity error on a function code cancels the code, disables the Reply and Reject signals, and sends a Parity Error signal to the 3000 Series computer channel, lighting the PARITY ERROR indicators on the 3000 Series computer and the 1718.

TABLE 2. DIVISION A FUNCTION CODES

F	N	DESCRIPTION
0001	XXXXXXXX	Set Flags for "1's" in N.
0010	XXXXXXXX	Clear Flags for "1's" in N.
0100	XXXXXXXX	Set Mask register for "1's" in N.
1000	XXXXXXXX	Clear Mask register for "1's" in N.
0000	00000001	Select interrupt if other computer is not running.
0000	00000010	Clear conditions set up by F = 0000, N = 00000001.
0000	00000100	Select interrupt if other computer reads or writes.
0000	00001000	Clear condition set up by F = 0000, N = 00000100.

PROGRAMMING DIVISION B

The contents of the 1704 A and Q registers define instructions going to division B from the 1704. The two operations possible in division B, Read and Write, correspond directly to the 1704 instructions, output from A and input to A. The Q register determines whether data or a function code will be output from A or whether data or status will be input to A.

The Q register contains 16 bits which are divided into three distinct sections. Figure 6 shows the format of the Q register.
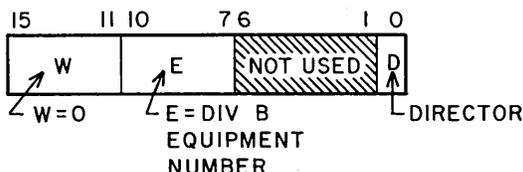
Figure 6. Q Register Format

The W portion (bits 11-15) of the Q register must equal zero* when programming the 1718; this portion is not sent to division B, but a W = 0 signal is sent.

The E portion (bits 7-10) of the Q register contains the equipment number of division B. Table 3 lists the values of E required to select division B with a given equipment number setting.

TABLE 3. DIVISION B SELECT CODES

E (BITS 10-7 OF Q)	EQUIPMENT NUMBER
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

The Director (D) portion (bit 0) determines whether data or a function code will be output from A or whether data or status will be input to A. Table 4 outlines the use of D.

TABLE 4. DIRECTOR USES

D	1704 INSTRUCTION	DIVISION B OPERATION
0	Output from A	Write Data
0	Input to A	Read Data
1	Output from A	Write Function Code
1	Input to A	Read Status

From the table it can be seen that if D equals 0, the contents of the A register is treated as data; if D equals 1, the contents of the A register is treated as a function code or as status information.

Division B Function Codes

Function codes transmitted to division B are 12 bits in length. Figure 7 shows the format of the function code in the A register.
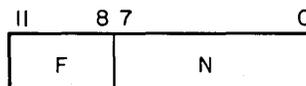
Figure 7. Format of the Function Code

---

*A 1718 attached to a converter (1706/16) receives the W = 0 signal from the converter. The W portion will, in fact, equal the code for the converter.

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TABLE 5. DIVISION B FUNCTION CODES

F	N	DESCRIPTION
0001	XXXXXXXX	Set Flags for "1's" in N
0010	XXXXXXXX	Clear Flags for "1's" in N
0100	XXXXXXXX	Set Mask for "1's" in N
1000	XXXXXXXX	Clear Mask for "1's" in N
0000	XXXXXXX1	Clear
0000	XXXXXX1X	Clear Interrupt and 8-Bit Character Mode
0000	XXXXX1XX	Data Interrupt Request
0000	XXXX1XXX	End of Operation Interrupt Request
0000	XXX1XXXX	Alarm Interrupt Request
0000	XX1XXXXX	Start Input Data Transfer
0000	X1XXXXXX	Stop Data Transfer
0000	1XXXXXXX	Set 8-Bit Character Mode

Set Flags
F = 0001

The Flag register is set where there are "1's" in bit positions 0 through 7 of the function code.

Clear Flags
F = 0010

The Flag register is cleared where there are "1's" in bit positions 0 through 7 of the function code.

Set Mask
F = 0100

The Mask register is set where there are "1's" in bit positions 0 through 7 of the function code.

Clear Mask
F = 1000

The Mask register is cleared where there are "1's" in bit positions 0 through 7 of the function code.

Clear
F = 0000 and Bit 0

This bit clears all interrupt requests, responses, and other logic which may be cleared in division B including the Mask register. A function code in which bit 0 equals 1 and any of bits 2-7 equal 1 will first clear all previous functions and then immediately set the function conditions where bits 2-7 equal 1.

Clear Interrupt and 8-Bit Character Mode
F = 0000 and Bit 1

This bit clears interrupt request selections, responses, and the 8-Bit Character mode. A function code in which bit 1 equals 1 and any of bits 2-7 equal 1 will first clear all previous functions and then immediately set the function conditions where bits 2-7 equal 1.

Data Interrupt Request
F = 0000 and Bit 2

This bit will cause an interrupt to be generated when an information transfer can occur. The interrupt response will be cleared by the Reply to a data transfer.

End of Operation Interrupt Request
F = 0000 and Bit 3

This bit will cause an interrupt to be generated when a data transfer terminates.

Alarm Interrupt Request
F = 0000 and Bit 4

This bit will cause an interrupt to be generated when division A has a transmission parity error or if division A computer is not running.

Start Input Data Transfer
F = 0000 and Bit 5

This bit may be used to signal division A that division B is about to Read. This code is used only when the 1718 operates from the 1705 channel. See division A status and interrupt selection.

Stop Data Transfer
F = 0000 and Bit 6

This bit may be used to signal division A that a data transfer is terminated. This code is used only when the 1718 operates directly from the 1705 channel. See Division A Status, B Read (Bit 9).

Set 8-Bit Character Mode
F = 0000 and Bit 7

This bit conditions the 1718 to change the bit position of bits 6-11. In this mode, bits 6-11 from the 3000 Series I/O cable go to bit positions 8-13 in the 1700 I/O cable (see page 3).

Status

Division B transmits status information to the A register where D (bit 0 of the Q register) equals a "1" and an Input to A instruction is executed. The status bit definition is shown in Table 6.

TABLE 6. STATUS BIT DEFINITION

BIT NO.	MEANING (STATUS IF BIT = 1)
0	Division A Read
1	Division A Write
2	Interrupt
3	Data
4	End of operation
5	Division A transmission parity error
6	Division A computer running
7	Protected
8-15	Flag register

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Division A Read (Bit 0)

This bit indicates that the computer attached to division A is attempting an input.

Division A Write (Bit 1)

This bit indicates that the computer attached to division A is attempting an output.

Interrupt (Bit 2)

This bit indicates that an interrupt has occurred from the 1718.

Data (Bit 3)

This bit indicates that the 1718 is ready to perform a data transfer.

End of Operation (Bit 4)

This bit indicates the end of a data transfer has occurred. It becomes a "1" when division A or B write drops and the Buffer register is empty or if division A or B read drops. This bit becomes a "0" when a new transfer is initiated from division B.

Division A Transmission Parity Error (Bit 5)

This bit indicates that division A has detected incorrect parity on the 3000 Series data channel.

Division A Computer Running (Bit 6)

This bit indicates that the computer attached to division A is running.

Protected (Bit 7)

This bit indicates that the PROGRAM PROTECT switch is in the PROTECTED position.

Bits 8 through 15 copy the condition of the Flag register. Bit 8 corresponds to flag 0, bit 9 to flag 1, etc.

Programming Considerations

Note that the 1718 may be directly attached to the 1705 Interrupt Data Channel or may be attached to the 1706 Buffered Data Channel or the 1716 Coupled Data Channel. Programming the 1718 from the 1705 or 1706/16 must be treated as two distinct cases.

To send a block of data from the 1718 to memory via the 1705, Start Input Data Transfer and Stop Data Transfer function codes are used to define the beginning and the end of the block of data read by the 1705. These two codes are used only by the 1705 program. The Stop Data Transfer function code sets the end of operation status bit in the 1718.

When sending a block of data from memory to the 1718 via the 1705, the Stop Data Transfer function code defines the end of the block. The beginning of the block is defined by the first data output to the 1718.

Data blocks sent to or from memory via the 1705 tie up the 1705 A and Q registers; the operation requires more instructions and is slower than the 1706/16 data transfer. The example has been preceded by necessary functions and selection preparatory to a data transfer.

<div align="center">1705 Output</div>

LDQ	Address 1718 for data
ENA	Clear A
STA	Clear memory index
→ LDA (memory index)	Next data word to A
OUT	Send data
RAO	Increment memory index for next data word
ENA	Count; count equals number of words in the block
ADD	Memory index to A
SAN	Skip back if A ≠ 0

test for end of data block

LDQ	
LDA	Function 1718 with Stop Data Transfer
OUT	

When the 1718 is attached to the 1706/16, the block of data sent to or from the 1706/16 is defined by the channel Buffer Active signal. When the Buffer Active signal drops and the Data register is empty, the end of operation status bit sets in the 1718.

The 1706 and 1716 provide direct access to computer storage, require fewer instructions for input and output to or from the 1718, and transfer data faster than the 1705.

The brevity of the Buffered I/O Instruction sequence for a 1706 or 1716 program is illustrated in the example below. The example has been preceded by necessary functions and selection preparatory to a data transfer.

<div align="center">1706 Buffered Output</div>

LDQ	Selects Buffered Output mode, 1718 equipment number, and bit 0 equals 0 for a data transfer.
LDA	Load A with FWA-1 of the buffer area. The contents of memory at this address must contain the LWA+1 of the buffer area.
OUT	The buffer transfer is now initiated under the control of the 1706.

The 1716 Buffered Input or Output operation is equally as brief. See the appropriate manual for detailed programming information on the 1705, 1706, or 1716.

Division B Operations The D field of the Q register is combined with a 1704 input or output instruction to specify a division B operation (Table 4). The following paragraphs define these operations.

Operations Defined by D and Output from A

Write Data: To perform a Write data operation, load Q with W equal to 00*, E equal to the division B equipment number, and D (bit zero) equal to 0. An Output from A instruction initiates the transfer of data to division B. Division B transfers these 12 bits to division A which sends it to the 3000 Series computer.

Division B Function: To send a function code from the A register to division B, load Q with W equal to 00*, E equal to the equipment number, and D equal to 1. An Output from A instruction initiates the transfer of the function code to division B.

Operations Defined by D and Input to A Instruction

Read Data: To perform a Read data operation, load Q with W equal to 00*, E equal to the equipment number, and D equal to 0. An Input to A instruction initiates data transfer from division A to division B, which sends it to the A register.

Read Status: To perform a Read Status operation, load Q with W equal to 00*, E equal to the equipment number, and D equal to 1. An Input to A instruction initiates transfer of 16 status bits from division B to the A register. Termination of either the Read or Write data operation status bit.

Interrupts Division B will interrupt the 1704 program on the following four conditions:

Interrupt on Data

A "1" from bit 2 of the function code sets this interrupt request and a "1" from bit 0 or 1 of the function code clears the request and response. During a Read operation, the interrupt response will occur when data can be loaded into the register. The next data transfer in the 1718 clears the interrupt response. This interrupt applies only when the 1718 and 1705 are attached directly.

Interrupt on End of Operation

A "1" from bit 3 of the function code sets this interrupt request; a "1" from bit 0 or 1 of the function code clears the request and response. An operation may or may not be in progress at the time of the selection but the interrupt will not respond to an operation which ended before the selection was made. The End of Operation condition results when any data transfer operation terminates.

---

*W is written as two digits; the left is binary and the right is hexadecimal. If the 1718 is connected to the 1704 via a converter (1706/16), W equals the appropriate converter code. The converter will send a W = 0 signal to the 1718. See the appropriate converter reference material.

Interrupt on Alarm

A "1" from bit 4 of the function code sets this interrupt request; a "1" from bit 0 or 1 of the function code clears the request and response. A response to this request results from a transmission parity error or a division A Computer Not Running signal.

These three interrupt conditions can be cleared by a "1" from bit 0 or 1 of the function code. However, these function clear bits are subordinate to bits 2-7 of the function code, so to clear interrupt requests or responses, a function code must be sent with only bit 1 or bit 2 set. A function code sent with a clear bit set and an interrupt bit set will first clear the initial conditions and then set the interrupt.

Mask/Flag Interrupt

A "1" formed by bits in the B Mask and Flag register will also interrupt the 1704 program. See the functional description of the Mask and Flag register.

A Master Clear clears all interrupt requests and responses.

Data Rates

Because of the large number of variables in determining the data rates of the 1718, a few typical examples are given. These can be used as a guide in estimating the data rates of other configurations. The programs used are included because they can influence the data rates. Table 7 contains data rate examples for 1706/3806. Table 8 contains data rate examples for the 1706/3206. It should be noted that the 3200 Series program ran in one memory bank and the data was in a different memory bank to eliminate program interference with the data transfer.

Sample Programs

The following sample programs (Tables 7 and 8) illustrate 1706 output and 3206/3806 input data rates.

TABLE 7. DATA RATE EXAMPLES FOR 1706/3806

3806 PROGRAM TO INPUT 16 (BASE 10) 48-BIT WORDS					
ADDRESS	INSTRUCTION				COMMENTS
10000	740	10000	010	07000	Connect
10001	742	10000	010	10003	Input
10002	750	10000	000	00000	Repeat, wait first
10003	300	00020	000	10004	

1706 PROGRAM TO OUTPUT 64 (BASE 10) 12-BIT WORDS			
ADDRESS	INSTRUCTION		COMMENTS
	MNE CODE	HEX CODE	
1000	LDQ	E000	Prepare 1706 address
1001		2300	
1002	LDA	C000	Prepare 1706 buffer address
1003		1006	
1004	OUT	03FA	Start Output Buffer
1005	JMP	18FA	Repeat, wait first
1006		1046	Buffer LWA + 1
1007		0000	Buffer FWA

```
+------+        +------+        +------+        +------+
| 3806 |<--A--->| 1718 |<--B--->| 1706 |<--C--->| 1705 |
+------+        +------+        +------+        +------+
```

DATA RATE* (microseconds/word)	LENGTH A (feet)	LENGTH B (feet)	LENGTH C (feet)
2.3	60	3	60
2.3	60	100	60
3.0	160	3	60
3.2	60	200	60

*These rates are for 1706 to 3806 transfers. The rates for 3806 to 1706 are virtually identical.

TABLE 8. DATA RATE EXAMPLES 1706/3206

3206 PROGRAM TO INPUT 32 (BASE 10) 24-BIT WORDS		
ADDRESS	INSTRUCTION	COMMENTS
00000	770 16000	Connect
00001	010 00000	
00002	740 60041	Input
00003	100 60000	
00004	010 00002	
00005	010 00000	Jump to beginning

1706 program to output 64 (base 10) 12-bit words is the same program as in Table 7.

3206	←—A—→	1718	←—B—→	1706	←—C—→	1705

DATA RATE* (microseconds/word)		LENGTH A (feet)	LENGTH B (feet)	LENGTH C (feet)
3206 to 1706	1706 to 3206			
4.3	2.8	100	10	10
4.3	2.9	130	10	10
4.3	2.9	130	100	10
4.5	3.0	200	10	10

*Data rates are very sensitive to actual program conditions. For example, a slightly different program yielded a 3.4 microsecond/ word data rate for the 3206 to 1706 instead of 4.3. The listed data rates are an approximation only.

MANUAL OPERATION

Switches and Indicators

The following switches and indicators (Figure 8) on the 1718 are located on the chassis and can be found by opening the front door of the cabinet in which it is housed.
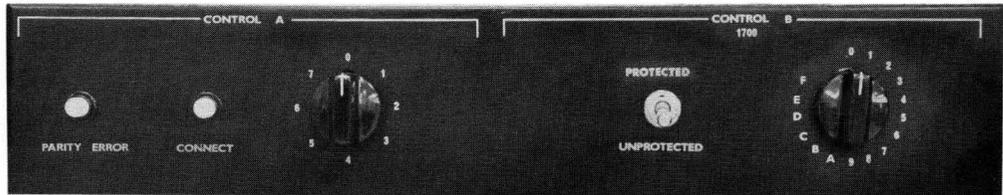
Figure 8. 1718 Switches and Indicators

Equipment Number Switch (Division A) - This 8-position switch selects the address number of division A of the coupler.

CONNECT Indicator - This lights when the 3000 Series computer connects with division A.

PARITY ERROR Indicator - This lights if division A detects a transmission parity error.

Equipment Number Switch (Division B) - This 16-position switch selects the address number of division B. This switch is numbered hexadecimally zero through F.

PROGRAM PROTECT Switch - This switch has two positions, PROTECTED and UNPROTECTED. The PROTECTED position provides for the program protection feature described in the Functional Description section.

CONTENTS

FIGURES

TABLES

CONTROL DATA 1738-B DISK DRIVE CONTROLLER

1738-A/B DISK DRIVE CONTROLLER

INTRODUCTION

The Control Data 1700 Disk Storage Subsystem consists of a CONTROL DATA* 1738 Disk Drive Controller, one or two CONTROL DATA 853/854 Disk Storage Drive Units, and any number of CONTROL DATA 850 Disk Packs. The system provides medium capacity, on-line, random access disk storage. The removable disk pack allows an infinite amount of off-line storage. A complete system is illustrated in Figure 1.

The 1738 Disk Drive Controller contains the circuitry necessary to transfer data, generate control signals, and interpret computer function codes between the disk storage drive units and a 1704 Computer.

This section contains specific description, operation, and programming information for the 1738 Controller. General information is provided for the disk storage subsystem.
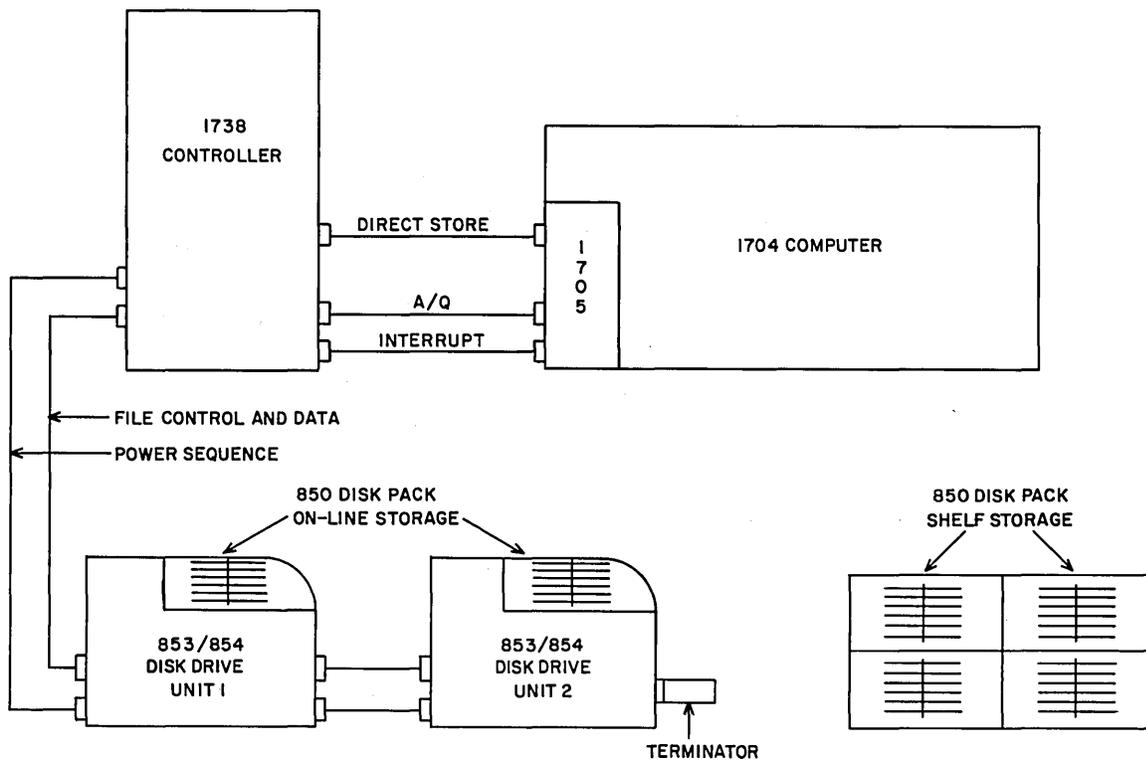
Figure 1. 1700 Disk Storage System - Functional Block Diagram

———————————

*Registered trademark of Control Data Corporation

Physical Description

1738 Disk Drive Controller

The controller logic is constructed of 3000-type logic cards on a standard chassis. The chassis may be mounted in a 3000 Type A cabinet (designated 1738-A) or a 1700 vertical cabinet (designated 1738-B).

853/854 Disk Storage Drive

The drive unit is a free-standing cabinet which contains the drive mechanism, a logic chassis, and a power supply which provides the necessary power.

The track spacing of data provided by the 853 is different from that provided by the 854. Therefore, data transfer is only possible between systems having the same type of disk drive.

850 Disk Pack

Each disk pack is a portable stack of six recording disks approximately 14 inches in diameter mounted on a common vertical axis. Each disk is coated with magnetic oxide recording medium, although data is recorded on only ten of the twelve surfaces. The outer surfaces of the top and bottom disks are not used for recording.

Specifications

Refer to Table 1 for a list of disk storage drive unit specifications.

TABLE 1. DISK STORAGE DRIVE UNIT SPECIFICATIONS

STORAGE CHARACTERISTICS:

Data format: 16 bits per word
          96 words per sector
          16 sectors per track
          10 tracks per cylinder
      100 cylinders (for the 853 File)
      203 cylinders (for the 854 File)

Data capacity: 1,536 bits per sector   (96 words per sector)
      24,576 bits per track   (1,536 words per track)
    245,760 bits per cylinder (15,360 words per cylinder)
  24,576,000 bits per 853 File (1,536,000 words per file)
  49,889,280 bits per 854 File (3,118,080 words per file)

ACCESS TIME:	
Head positioning time	165 milliseconds (maximum)
Cylinder-to-cylinder positioning time	30 milliseconds
Latency time	25 milliseconds (maximum)

TRANSFER RATE:	
Data rate	12.8 usec per 16-bit word
Bit rate	0.8 usec per bit

FUNCTIONAL
DESCRIPTION

1738 Disk Drive Controller

The controller serves as an interface between the computer and the disk storage drive unit. It translates function codes issued by the computer to control disk storage drive operations. The controller ignores any function code which is not accompanied by the equipment number.

The controller buffers data between the computer and the disk storage drive unit. It accepts data (16 bits per word) from the computer in a parallel format and disassembles and transfers the data serially to the drive unit. Similarly, the controller accepts data serially from the drive unit, assembles it into 16-bit bytes, and transfers it in parallel to the computer.

All communications with the controller are through three interfaces. Two of these interfaces serve as communication channels between the computer and the controller. The third interface serves as a communication channel between the controller and the file (disk storage drive unit). The following gives the name and use of each interface:

1) A/Q Interface - This interface is used to transmit function codes and address information to the controller and status and address information to the computer.

2) Direct Storage Interface - This interface is used for all data transfer to or from the computer. It is also used to transfer the last word address plus one (LWA + 1) of the buffer areas to be used.

3) Controller/File Interface - This interface is used for selecting the file, track, and cylinder, and for transferring the difference count. It is also used for transferring serial data to and from the file.

Addressing

Addressing of the records is under program control from the computer. Records within the file are accessed by a 16-bit word sent from the computer to the controller. This word is called the Sector Record Address word, and contains the sector number, the head (or surface) number, and the cylinder number. The least significant four bits of the Sector Record Address word identify the sector within a track (1 of 16_{10}). The next higher four bits identify the head within a cylinder (1 of 10_{10}). Head numbers 10_{10} through 15_{10} are illegal. The upper eight bits identify the cylinder within the file (1 of 100_{10} on the 853, and 1 of 203_{10} on the 854). Cylinder address numbers above 99_{10} on the 853 and above 202_{10} on the 854 are illegal. The sector record address word is illustrated in Figure 2.
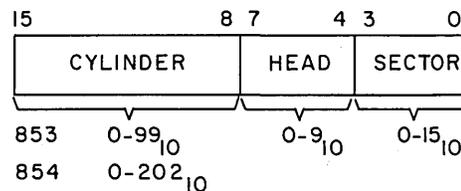

Figure 2. Sector Record Address Word

The file, cylinder, track, and sector are defined as follows:

1) File - The file is defined as all the recording surface under all the heads on all the cylinders.

2) Cylinder - The cylinder is defined as all the recording surface under all the heads at a given position.

3) Track - The track is defined as the recording surface under one read/write (R/W) head at a given cylinder position.

4) Sector - The sector is defined as the smallest subdivision of the file. There are 16 separate and distinct sectors within each track.

The actual positioning of the R/W heads during addressing is determined by a difference count generated by the controller. The sector record address which is loaded into the A register of the computer is sent to the File Address register of the controller. The cylinder number of this address is then compared to current cylinder number (the current position of the R/W heads). The controller determines the difference of these two cylinder numbers and transfers the difference count to the drive unit. The difference count causes the head positioner to seek forward or seek reverse. If the address from the A register is greater than the current cylinder address, the controller initiates a Seek Forward operation. If the address from the A register is less than the current cylinder address, the controller initiates a Seek Reverse operation.

Write Address

Each sector record within the file is assigned a unique identifying address. The Write Address function allows the record address tags to be written onto the disks. The address tags constitute a portion of the sector format illustrated in Figure 3.
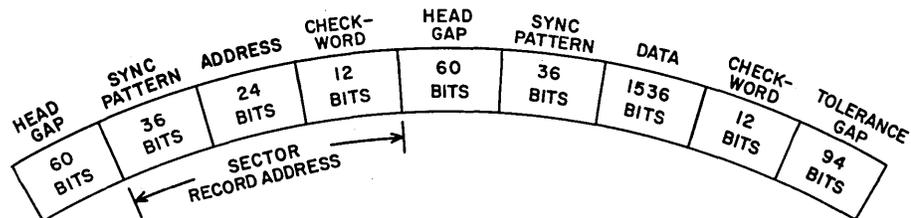
Figure 3. Sector Format

The Write Address function requires that the program send the function code and the address for each track of 16 sector address tags written. It is also necessary that the ADDRESS WRITE switch be enabled when writing the tags. (This switch is located inside the controller cabinet.) The address tags are written sequentially from 0 through 15_{10} starting from the index mark. The writing of information onto the disks during a Write Address function is carried out in the following sequence:

1) Head Gap - Sixty bits are required for the head gap due to the physical characteristics of the drive unit head assembly.

2) Sync Pattern - The sync pattern (36 bits) is written as all zeros except for the least significant bit which is a "1". A "1" denotes the end of the pattern. The sync pattern enables the controller to recognize the significance of the serial data bits from the file.

3) Address - The address (24 bits) contains the Good Track bit, the cylinder number, head number, and sector number. Figure 4 illustrates the bit positioning of the address.
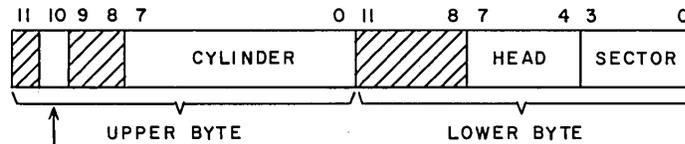
Good Track Bit - This bit, when set, indicates that this sector is in a track which has been checked and is usable. If, during the life of the disk pack, some part of the track becomes defective, then all the address tags on that track are rewritten and a "0" is written into the Good Track bit position. It is then impossible for the programmer to access this track for Read, Write, or Compare operations.

Figure 4.   Bit Positioning of the Address Tag

4) Checkword - The disk system automatically writes a checkword (12 bits) at the end of each address written on the disk. (A checkword is also written at the end of each data record.) This checkword is used to verify the accuracy of each address when it is read from the disk. If, during a Read operation, the address or data record being read does not agree with that which was written, the Checkword Error status bit will set.

The manner in which the addresses are assigned reduces positioning time and access time. All R/W heads move simultaneously and therefore data is written in cylinders (from disk to disk) throughout the pack. Figure 5 indicates sector, surface, and cylinder organization of the disk pack. Table 2 is a guide for the assignment of address tags.

TABLE 2.   GUIDE TO ASSIGNMENT OF SECTOR RECORD ADDRESS TAGS

Address	Sector	Surface	Cylinder
00000 - 00015	00 - 15	0	00
00016 - 00031	00 - 15	1	00
00032 - 00047	00 - 15	2	00
00048 - 00063	00 - 15	3	00
-	-	-	-
-	-	-	-
00144 - 00159	00 - 15	9	00
00160 - 00175	00 - 15	0	01
00176 - 00191	00 - 15	1	01
-	-	-	-
-	-	-	-
01596 - 15982	00 - 15	8	99
15983 - 15999	00 - 15	9	99

NOTES

From one specific sector address to the corresponding sector address on the next surface, the address is incremented by 16. For example, sector 01, surface 0, cylinder 0 (address 00016) to sector 00, surface 2, cylinder 0; 00016 + 16 = 00032.

From one sector address in a cylinder to the corresponding sector address in the next cylinder, the address is incremented by 160. For example, sector 00, surface 1, cylinder 00 (address 00016) to sector 00, surface 1, cylinder 01; 00016 + 160 = 00176.
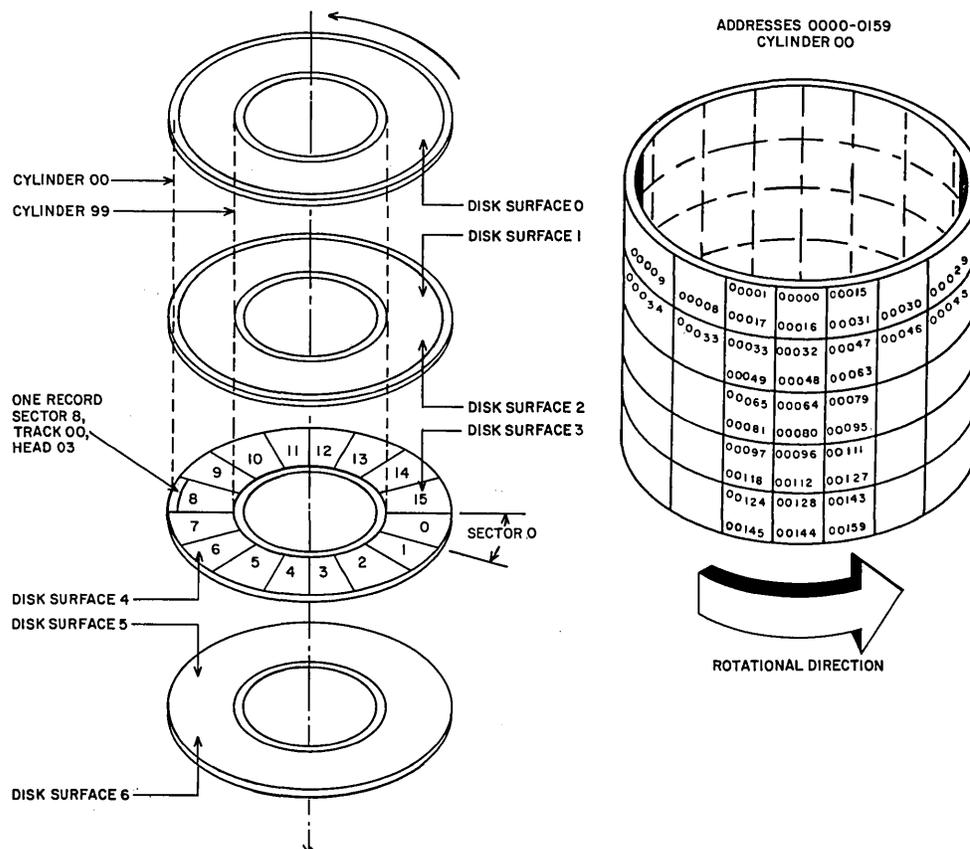
Figure 5. Sector, Surface, and Cylinder Organization of a Disk Pack

Addressing Core Storage

The controller has direct access to the computer's core storage and thus contains the necessary logic for holding and incrementing core addresses. The last word address plus one (LWA + 1) is loaded into the controller as data. This address is held in a Storage Address register to be compared with the current address. The current address initially is the first word address minus one (FWA -1) and is loaded into the controller via the A/Q interface upon programmed instructions. The current address is then incremented by the controller. When the current address compares with the LWA + 1, the controller sets the End of Operation status bit. The setting of this bit signals the computer that the specified operation has been completed.

**Summary of
Programming
Information**

The information necessary to program the 1738 Controller is summarized
at the beginning of this section to aid the experienced programmer. Tables
are also provided for quick reference. Table 2 lists the input and output
function codes, and Table 3 lists the status response bits. Figure 6
shows the Q register format used for all 1738 input or output functions. A
detailed description of each function code and status response bit follows
the summary.

TABLE 3. FUNCTION CODES

Value Set in Q (Bits 02-00)	Output From A	Input to A
001	Director Function	Director Status
010	Load Address	Address Register Status
011	Write	
100	Read	
101	Compare	
110	Checkword Check	
111	Write Address	

TABLE 4. STATUS RESPONSE BITS

Bit Set in A	Title	Bit Set in A	Title
A0=1	Ready	A8=1	Checkword Error
A1=1	Busy	A9=1	Lost Data
A2=1	Interrupt	A10=1	Seek Error
A3=1	On Cylinder	A11=1	Address Error
A4=1	End of Operation	A12=1	Defective Track
A5=1	Alarm	A13=1	Storage Parity Error
A6=1	No Compare	A14=1	Protect Fault
A7=1	Protected	A15=1	Not Used
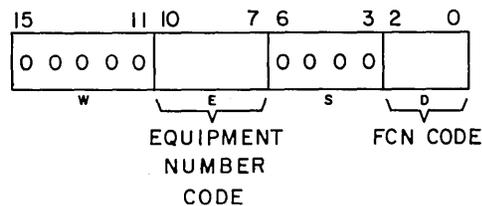
Figure 6. Q Register Format

Summary of Output from A Operations

Director Function (001): For this output function, the bits in the A register
are available for the selection of interrupts and the drive unit. See
Figure 7.
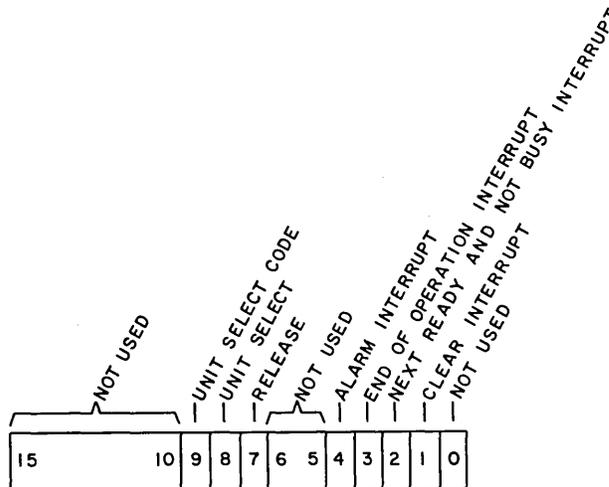
Figure 7. Selectable Bits in A Register

Load Address (010), Checkword Check (110), or Write Address (111): For these output functions, the A register contains the Sector Record Address word. See Figure 8.
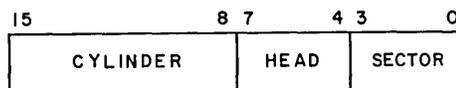
Figure 8. A Register During Load Address, Checkword Check, or Write Address Output Function

Write (011), Read (100), or Compare (101): For these output functions, the A register contains the first word address minus 1 of the buffer area to be used. See Figure 9.
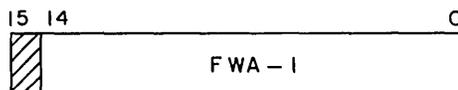

Figure 9. A Register During Write, Read, or Compare Output Function

NOTE

The core storage location specified by the FWA-1 contains the LWA + 1 of the buffer area to be used.

Summary of Input to A Operations

Director Status (001): For this input function, the A register receives the status condition of the controller and disk storage drive unit. The status response bits are illustrated in Figure 10.
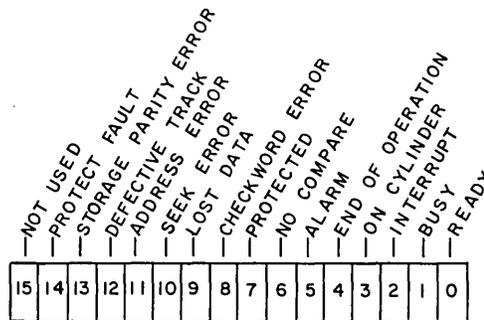
Figure 10. A Register During Director Status Function

Address Register Status (010): For this input function, the A register receives the File Address Register status of the controller. The File Address register contains the Sector Record Address. See Figure 11.

15	8	7	4	3	0
CYLINDER		HEAD		SECTOR	
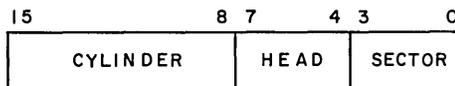
Figure 11. A Register During Address Status Function

Operations

The programmer-operator selects the controller and the drive unit by performing a Director function. The Director function code (001) and the equipment number code are loaded into the D and E fields of the Q register (refer to Figure 6). The required equipment number is determined by the setting of the Equipment Number switch located inside the controller cabinet. Selection of the drive unit (1 of 2) is determined by the value of bit 09 in the A register. If A9 = 0, drive unit 0 is selected. If A9 = 1, drive unit 1 is selected.

All computer operations are initiated by Output from A instructions. The function code for the operation is located in bit positions 02 through 00 of the Q register. Additional control information is transferred to the controller from the A register. The significance of the contents of the A register varies with the operation specified.

The computer checks the status of operation via the Input to A instruction. The function code in the Q register determines the status information to be transferred to the A register.

During either Input to A or Output from A instructions, the Q register must contain the 1738 equipment number in bit positions 10 through 07. All other bits in Q except the function code must be zeros. All unassigned function codes are illegal and will be rejected.

Description of Output Function Codes

Director Function (001): This function prepares the controller for a data transfer or addressing operation. The contents of the A register during this operation determines which conditions will be set in the controller. A list of the selectable conditions for each bit position in the A register is given on the following page.

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A0	Not used.
A1 = 1	Clear Interrupt request - Selecting this request causes all interrupt selections to be cleared.
A2 = 1	Next Ready and Not Busy Interrupt request - Selecting this request causes the interrupt line to become active when the controller becomes Ready and Not Busy.
A3 = 1	End of Controller Operation Interrupt request - Selecting this request causes the interrupt line to become active when the End of Operation status bit is set.
A4 = 1	Alarm Interrupt request - Selecting this request causes the interrupt line to become active when the Alarm status bit is set.
A5	Not used.
A6	Not used.
A7 = 1	Release - This bit is used by a protected program to allow system control to pass to an unprotected program. The protected status is cleared by this bit.
A8 = 1	Unit Select - This bit allows the program to change the drive unit selection. The drive unit selected is determined by bit A9.
A9=X	Unit Select Code - This bit in conjunction with A8 and the Unit Select Code Switch (SW6) determines what unit the system is connected to.

A9=0	Unit Select Code Switch = Normal	Unit Selected = 0
A9=0	Unit Select Code Switch = Reverse	Unit Selected = 1
A9=1	Unit Select Code Switch = Normal	Unit Selected = 1
A9=1	Unit Select Code Switch = Reverse	Unit Selected = 0

A10
thru A15   Not used.

The Director function is accepted if the controller is Not Busy and if the protect conditions are met. (See Programming Considerations.) Acceptance of this function clears all status bits except Ready, On Cylinder, and Protected. If this function selects another unit, these status bits will depend on the conditions of the new unit.

NOTE

The Busy status reflects controller and/or device operation. The controller will accept this function if the Busy status simply indicates that the selected drive unit is in the process of positioning, i.e., not On Cylinder.

Load Address (010): This function causes the controller to load the data from the A register (the Sector Record address) into the controller File Address register. The controller then determines the difference between the present file cylinder address and the new cylinder address. It then transfers this difference and the new cylinder address to the drive unit. The controller then initiates the movement of the head positioner.

The controller will accept this function if it is Ready, Not Busy, and On Cylinder, and if the protect conditions are met. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon accepting the function and remains busy until it completes the movement of the head positioner, at which time it becomes Not Busy. The End of Operation status bit is set when the controller completes the transfer of control information to the file. The On Cylinder status bit is cleared when the controller initiates the positioning and remains cleared until the head positioner reaches its new position.

If the controller receives an address from the computer which is illegal it will set the Address Error, End of Operation, and Alarm status bits. The controller will not initiate a cylinder movement.

Write (011): This function causes the controller to transfer data from computer core storage to file storage. The starting address of file storage is determined by a previous Load Address, or any previous Write, Read, or Compare operation. The addresses in core storage are determined in the following manner.

The A register, during this function transfer, contains the first word address minus one (FWA - 1) of the buffer area to be used. This address is loaded into the controller's current Address register. The content of this storage location is the last word address plus one (LWA + 1) of the buffer area to be used. After loading the current Address register, the controller reads the location it specifies into the LWA + 1 register. It then increments the current Address register and is ready to start the Output operation. During the Write operation the current address is incremented after each word transferred. When the current address equals LWA + 1, the controller ends the data transfer from computer storage. If data transfer stops within a sector, the controller pads out the remainder of the sector with zeros and then writes the checkword. If data transfer extends beyond the last sector in a cylinder, the controller will move the head positioner to the next cylinder and continue the transfer there. If transfer is attempted beyond the last cylinder in a file an Address Error will occur.

The controller will accept this function if it is Ready, Not Busy, and On Cylinder, and if the protect conditions are met. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the last sector operated on. The End of Operation status bit is set when the Busy status bit is cleared. The File Address status at the completion of this operation is that of the last sector written plus one.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end as soon as possible, i.e., immediately or at the end of the sector presently operated on. The abnormal conditions are:

1) Lost Data,

2) Address Error,

3) Seek Error,

4) Defective Track, and

5) Storage Parity Error.

Detection of any of these abnormal conditions causes the corresponding status bit and the Alarm status bit to be set.

Read (100): This function causes the controller to transfer data from file storage to computer core storage. The method for obtaining the starting addresses and the buffer length are the same as for the Write function. If data transfer to the computer stops within a sector, the controller continues reading the data until the end of the sector and determines if the checkword is correct.

The controller will accept this function if it is Ready, Not Busy, and On Cylinder, and if the protect conditions are met. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the last sector operated on. The End of Operation status bit is set when the Busy status bit is cleared. The File Address status at the completion of this operation is that of the last sector read plus one.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end as soon as possible, i.e., immediately or at the end of the sector presently operated on. The abnormal conditions are:

1) Lost Data,
2) Address Error,
3) Seek Error,
4) Protect Fault,
5) Defective Track,
6) Checkword Error, and
7) Storage Parity Error.

Detection of any of the abnormal conditions causes the corresponding status bit and the Alarm bit to be set.

Compare (101): This function causes the controller to compare data from computer core storage with data read from file storage. Addressing is the same as that for the Write operation. The comparison stops when the computer buffer limits are reached, but the controller will read to the end of the last sector compared. If the data does not compare, the No Compare status bit will be set.

The controller will accept this function if it is Ready, Not Busy, and On Cylinder, and if the protect conditions are met. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the last sector operated on. The End of Operation status bit is set when the Busy status bit is cleared. The File Address status at the completion of this operation is that of the last sector read plus one.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end as soon as possible, i.e., immediately or at the end of the sector presently operated on. The abnormal conditions are:

1) Lost Data,
2) Address Error,
3) Seek Error,
4) Defective Track,
5) Checkword Error, and
6) Storage Parity Error.

Checkword Check (110): This function causes the controller to read all of the sectors in the track specified by the contents of the A register. No data is transferred to or from computer core storage. Data is simply read from the 16 sectors into the checkword logic to be checked. The controller will accept this function if it is Ready, Not Busy, and On Cylinder, and if the protect conditions are met. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the 16th sector checked. The End of Operation status bit is set when the Busy status bit is cleared. The File Address status at the completion of this operation is that of the last sector read plus one. Normally this would be the first sector on the next consecutive track.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end as soon as possible. In this case it will be immediately or at the end of the last sector read. The abnormal conditions are:

  1) Address Error,

  2) Seek Error,

  3) Defective Track, and

  4) Checkword Error.

Detection of any of the abnormal conditions causes the corresponding status bit and Alarm bit to be set.

Write Address (111): This function, in conjunction with the ADDRESS WRITE switch on the operator's panel, causes the controller to write the address tags of all the sectors in the track specified by the contents of the A register. No data is transferred to or from core storage.

If the ADDRESS WRITE switch on the operator's panel is in the Bad Track position, the tags written will not contain the Good Track bit. When the controller encounters these tags during Write, Read, Compare, and Checkword Check operations, it will set the Defective Track status bit and End of Operation status bit.

The controller will accept this function if it is Ready, Not Busy, and On Cylinder if the protect conditions are met and if the ADDRESS WRITE switch is enabled. Acceptance of this function causes the clearing of all status bits except Ready, On Cylinder, and Protected.

The controller becomes Busy upon acceptance of this function and remains Busy until the 16th address tag is written. The End of Operation status is set when the Busy status is cleared.

The File Address status at the completion of the operation is that of the last address tag written plus one. This is the first sector address of the next consecutive track.

Two abnormal conditions, Address Error and Seek Error, can develop during this operation. Detection of these conditions by the controller causes the operation to end as soon as possible. In this case it will be immediately. Detection of either of the abnormal conditions causes the corresponding status bit and the Alarm bit to be set.

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Description of Input Function Codes

Director Status (001): This function is used to monitor the controller operating status. The status information is loaded into the A register. The controller will accept this function at any time. The acceptance of this function causes no changes in the status of the controller.

Address Status (010): This function is used to monitor the controller File Address. The address information is loaded into the computer A register by the controller. The address bits are arranged in the same format used to transfer the Sector Record Address word to the controller. This function will be accepted at any time by the controller.

When the controller is Busy, the Address status represents the sector being operated in. When the controller is Not Busy, it represents the sector last operated in plus one.

Description of Status Response Bits

Ready (A0 = 1): This status bit indicates that the selected unit is available and ready to operate. The unit becomes Not Ready for the following reasons:

1) Disk pack not in drive unit

2) Disk drive motor not up to operating speed (2400 rpm)

3) Read/write heads not in operating position

4) A fault condition develops in the selected unit (See Programming Considerations)

This status condition will be affected by the operating program only if it selects a non-existing device or a device which is Not Ready. Normally, this status bit indicates that manual intervention is required at the selected drive unit.

Busy (A1 = 1): This status bit indicates that the controller and/or the drive unit is presently involved in the performance of an operation. This bit is set by the acceptance of a Load Address, Write, Read, Compare, Checkword Check, or Write Address function.

This bit will be cleared when the controller and/or drive unit has completed its operation, or an abnormal condition is detected which aborts the operation. Once initiated, the computer cannot clear the Busy condition.

Interrupt (A2 = 1): This status bit indicates that a selected interrupt condition has occurred. This bit will be cleared by the acceptance of any output function.

On Cylinder (A3 = 1): This status bit will be set when the selected drive unit positioner is On Cylinder. This bit will be cleared if the drive unit is presently positioning or if a Seek Error is detected.

End of Operation (A4 = 1): This status bit will be set whenever the controller portion of an operation is complete. (The Busy status may remain set if the selected unit is positioning.) This bit will be cleared by any output function.

Alarm (A5 = 1): This status bit indicates that one of the following abnormal conditions occurred:

1) Not Ready
2) Checkword Error
3) Lost Data
4) Seek Error
5) Address Error
6) Defective Track
7) Storage Parity Error
8) Protect Fault

This bit will be cleared by any output function. The Not Ready condition can be changed by selecting another drive unit or by manual intervention at the selected drive unit.

No Compare (A6 = 1): This bit indicates that the data received from computer core storage does not compare with data read from file storage during a Compare operation. This bit is cleared by any output function.

Protected (A7 = 1): This bit indicates that a selected drive unit is protected and may only be accessed by protected computer instructions. If this bit is set, it can be cleared by a protected Director Function which has the Release bit set in A.

Checkword Error (A8 = 1): This status bit indicates that the controller logic has detected an incorrect checkword in data read from file storage during a Read, Compare, or Checkword Check operation. This bit is cleared by any output function.

Lost Data (A9 = 1): This bit indicates that the computer's direct access bus has not been able to keep up to the file data transfer rate during a Write, Read, or Compare operation. This bit is cleared by any output function.

Seek Error (A10 = 1): This bit indicates that the drive unit has detected a head positioner which has moved beyond the legal limits of the device during a Load Address, Write, Read, Compare, Checkword Check, or Write Address function.

This bit also indicates that the controller has been unable to obtain the sector record address selected during a Write, Read, Compare, and Checkword Check operation. This bit will be cleared by any function which sets the Busy status bit.

Address Error (A11 = 1): This bit indicates that the controller has detected an illegal file address received from the computer or that the controller has advanced the sector record address beyond the limits of file storage. This bit is cleared by any output function.

Defective Track (A12 = 1): This bit indicates that the controller has attempted to access a file storage address which had previously been labeled as being in a defective track. This bit will be cleared by any output function.

Storage Parity Error (A13 = 1): This bit indicates that the controller has received a parity error signal from the direct storage bus while receiving data or control information. If the error is detected during control information transfer, the operation will end immediately. If the error is detected during data transfer, the operation will end at the end of the current sector. This bit will be cleared by any output function.

Protect Fault (A14 = 1): This bit indicates that an unprotected controller operation attempts to write into a protected computer storage area. When the error is detected while transferring data to storage, the operation will cease at the end of the current sector. This bit will be cleared by any output function.

Interrupts

The controller can interrupt the computer when certain status conditions develop. The status conditions which can enable the interrupt line are Next Ready and Not Busy, End of Operation, and Alarm. The interrupt is enabled only if selected by the Director function. To clear an interrupt, the program is required to initiate any acceptacle output function.

Next Ready and Not Busy Interrupt

This interrupt should be used in one of two situations:

1) if the program requires an interrupt to inform it that manual intervention on the selected unit (changing a disk pack) has been completed and the system is now ready.

2) if a Load Address operation has been initiated and the program requires an interrupt to inform it that the controller portion (the difference calculation and the seek initiation) and the drive unit portion (head positioning) are both complete.

End of Operation Interrupt

This interrupt should be used when the program requires an interrupt to inform it that a Write, Read, Compare, Checkword Check, or Write Address operation has been completed. This interrupt should also be used on a Load Address operation if the program requires an interrupt after the controller portion of the operation is complete. (See Programming Considerations, Overlap Seek.)

Alarm Interrupt

This interrupt should be used if the program requires an interrupt when an Alarm condition develops.

Normal Programming Sequence

There are basically only three operations that the programmer-operator wishes to perform; Write, Read, and Compare. The Load Address function is a preliminary part of the basic operations, while the Checkword Check and Write Address functions are primarily maintenance operations.

When performing these three basic operations, the following sequence is recommended:

1) Perform a Director Function
   a) Select the drive unit
   b) Select the interrupt conditions.

2) Perform a Director Status function to check for Ready, On Cylinder, and Protected.

3) Perform a Load Address function with the Write, Read, or Compare starting address contained in the A register of the computer.

4) Return to main program if interrupts are used, otherwise start checking status immediately.

5) Perform a Director Status function to check for Not Busy and Alarm status. If the Alarm status bit is set, branch to an abnormal analysis routine (see Programming Considerations).

6) Load the buffer area upper limit (LWA + 1). This is simply moving the LWA + 1 to its proper position in core storage so that the controller can access it when performing the Read, Write, or Compare operation.

7) Perform a Director Function. Select the interrupt conditions.

8) Perform the desired operation (Write, Read, or Compare) with the FWA - 1 in the A register.

9) Return to main program if interrupts are used, otherwise start checking status immediately.

10) Perform a Director Status function.

 a) Check for End of Operation and Alarm status.

 b) If the Alarm status is set, branch to an abnormal condition analysis routine.

 c) If the Alarm status bit is not set, the operation has been completed normally.

Programming Considerations

File Protection

The 1700 Disk Storage Subsystem allows a protected program to maintain exclusive control of the system if a protected drive unit has been selected. Once a protected program gains control of the system it will maintain control until it does a Director function with the release bit set in A or selects an unprotected drive unit. Unless the controller is released, all unprotected output functions are rejected.

A drive unit is protected by setting the UNIT PROTECT switch for the drive unit to the ON position. When a drive unit is protected any program may select it, but only protected instructions can operate on it; all others are rejected.

When a protected drive unit is selected, the Protected status bit is set.

Abnormal Conditions

The Alarm status bit indicates a malfunction during the performance of an operation. Upon detection of the malfunction the program should determine what action can be taken.

If the alarm is caused by a Checkword Error, Lost Data Error, Seek Error, or Storage parity error, the program should repeat the operation at least 10 times before aborting. Repetition of an operation includes the loading of the address.

If the alarm is caused by Address Error, Defective Track, or Protect fault, a programming error has been detected and a change in the program must be made before continuing.

If the alarm is caused by the drive unit becoming Not Ready during an operation, the operation should be aborted immediately since manual intervention is required at the selected drive unit.

File Fault: The File Fault line is enabled by the selected drive unit when it detects one of the following conditions:

    1)   More than one head selected.

    2)   Select read and write simultaneously.

    3)   Select read and erase simultaneously.

    4)   Erase and no write selected.

    5)   Erase and both write drivers on.

    6)   Either one or both write drivers on and no erase.

    7)   More than one unit selected.

When the controller detects a file fault the system becomes Not Ready.

Overlap Seek

It is possible to have both disk storage drive units positioning at the same time. This feature reduces overall access time and is called Overlap Seek. To perform this operation, the following sequence should be used:

    1)   Perform a Director Function

        a)   Select the first drive unit

        b)   Select the interrupt conditions if desired (End of Operation and Alarm interrupts).

    2)   Perform a Director Status function to check for Ready, On Cylinder, and Protected status.

    3)   Perform a Load Address function with the starting address of the first drive unit in the A register.

    4)   Return to main program if interrupts are used, otherwise start checking status immediately.

    5)   Perform a Director Status function to check for End of Operation or Alarm status.

    6)   Perform a Director Function

        a)   Select the second drive unit

        b)   Select the End of Operation or Alarm interrupt.

    7)   Perform a Director Status function to check for Ready, On Cylinder, and Protected status.

    8)   Perform a Load Address function with the starting address of the second drive unit in the A register.

    9)   Return to main program if interrupts are used, otherwise start checking status immediately.

   10)   Perform a Director Status function to check for End of Operation or Alarm status.

11) The program may now scan both units using the Director Function and the Director Status until one unit becomes Not Busy. The program may also select either unit and the Next Ready and Not Busy interrupt and return to the main program to wait for this interrupt.

12) Perform a Director Status function to check for End of Operation or Alarm status.

13) Initiate the operation (Write, Read, or Compare). This includes the Load Address function.

MANUAL OPERATION

Switches and Indicators

The switches and indicators on the controller monitor panel and the controller operators panel are illustrated in Figures 12 and 13.
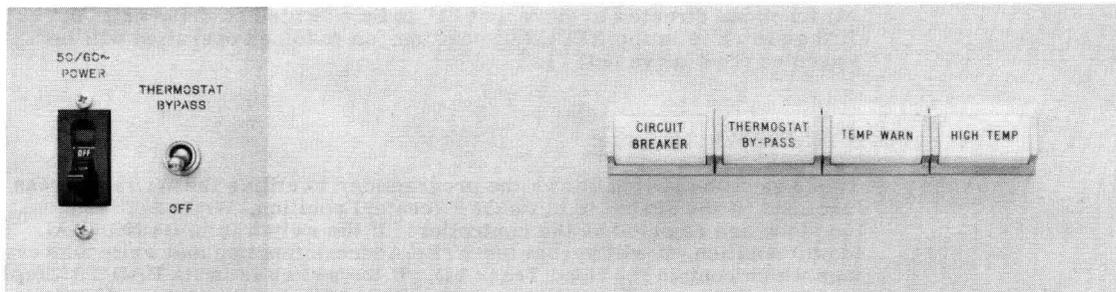
Figure 12. Controller Monitor Panel

50/60 ~ POWER Switch

This switch causes 50/60 cycle power to be applied to the controller when in the ON (up) position. This switch is of the circuit-breaker type and will disengage if the controller power supply becomes overloaded.

THERMOSTAT BYPASS Switch

When this switch is in the up position, the controller thermostat is by-passed. This switch allows the controller to be operated at above normal temperature; its use is recommended for maintenance personnel only.

CIRCUIT BREAKER Indicator

This indicator lights when the controller circuit breaker becomes disengaged.

THERMOSTAT BYPASS Indicator

This indicator lights when the THERMOSTAT BYPASS switch is enabled.

TEMP WARN Indicator

This indicator lights when the operating (AMBIENT AIR) temperature approaches the maximum safe operating limit.

HIGH TEMP Indicator

This indicator lights if the operating temperature of the controller exceeds 110° F.

AUTO LOAD Switch

This is a momentary contact switch on the controller operator's panel. Operation of this switch causes the controller to read data from the 16 sectors of track 0, cylinder 0, of drive unit "0" or drive unit "1" depending on the position of the Unit Select Code Switch. This data will be loaded into the first 1,536 addresses of computer storage. If the Unit Select Code Switch is in the NORMAL position, the autoload will take place from drive unit "0" and if the switch is in the REVERSE position, it will autoload from disk drive unit "1."

UNIT SELECT CODE Switch

This is a two-position switch which, when placed in the NORMAL position, will allow all functions directed to drive unit "0" to be executed on drive unit "0," and all functions directed to drive unit "1" to be executed on drive unit "1." When the switch is placed int the REVERSE position, the unit select lines will be reversed to the drives. This will cause all functions directed to drive unit "0" to be executed on drive unit "1" and all functions directed to drive unit "1" to be executed on drive unit "0." If the switch is in the REVERSE position, an Autoload operation will be executed from drive unit "1."

ADDRESS WRITE Switch

This 3-position switch allows the programmer to utilize the Write Address function. If the switch is in its OFF (center) position, Write Address functions are rejected by the controller. If the switch is in its NORMAL (down) position, it will accept the Write Address function and write address tags which contain the Good Track bit. If the switch is in its BAD TRK (up) position, the controller will accept the Write Address function and write address tags which do not contain the Good Track bit. When the switch is in either the NORMAL or BAD TRK position, an indicator above the switch will be on. The ADDRESS WRITE switch does not directly affect any system function except the Write Address function.

NOTE

The controller will not transfer data to or from any sector which does not contain a "1" in the Good Track bit position of its address tag. The Defective Track status bit will set when the controller encounters any sector which does not contain a Good Track bit.

UNIT PROTECT Switch

There are two UNIT PROTECT switches on the operator's panel, one for each drive unit. If either switch is in the ON position, the corresponding drive unit can only be accessed by protected programs. If both switches are in the ON position, both drive units can only be accessed by protected programs.

NOT AVAILABLE AT THIS TIME

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Figure 13.   Controller Operator's Panel

EQUIPMENT CODE Switch

The EQUIPMENT CODE switch is a 16-position switch (0 through 9 and A through F) which assigns an equipment number to the 1738 Controller. Any communication with the controller via the A/Q interface must be accompanied by an equipment code equal to the setting on this switch.

READY Indicator

This indicator lights if the selected drive unit is available and ready to operate.

BUSY Indicator

This indicator lights if either the controller or the drive unit is Busy.

END OF OPERATION Indicator

This indicator lights when the controller completes its specified operation.

ALARM Indicator

This indicator lights when one of the following abnormal conditions occurs:

1) Not Ready
2) Checkword Error
3) Lost Data
4) Seek Error
5) Address Error
6) Defective Track
7) Storage Parity Error
8) Protect Fault

ON CYLINDER Indicator

This indicator lights when the drive unit heads are on the selected cylinder.

DIRECT STORE CONT Switch (Not Shown)

When performing maintenance operations and for initial installation of the controller, the Direct Storage Control switch may be operated. This is a 5-position switch mounted on the bottom row of the controller chassis. The five positions are as follows:

1) MID
2) FIRST
3) LAST
4) ONE
5) OUT

These names reflect the controller's position within the Direct Storage Bus and varies with each system. For example, if the controller is the first equipment on the Direct Storage Bus, the DIRECT STORE CONT switch is set to the FIRST position. The OUT position is used when performing maintenance so that the controller cannot affect the operating system.
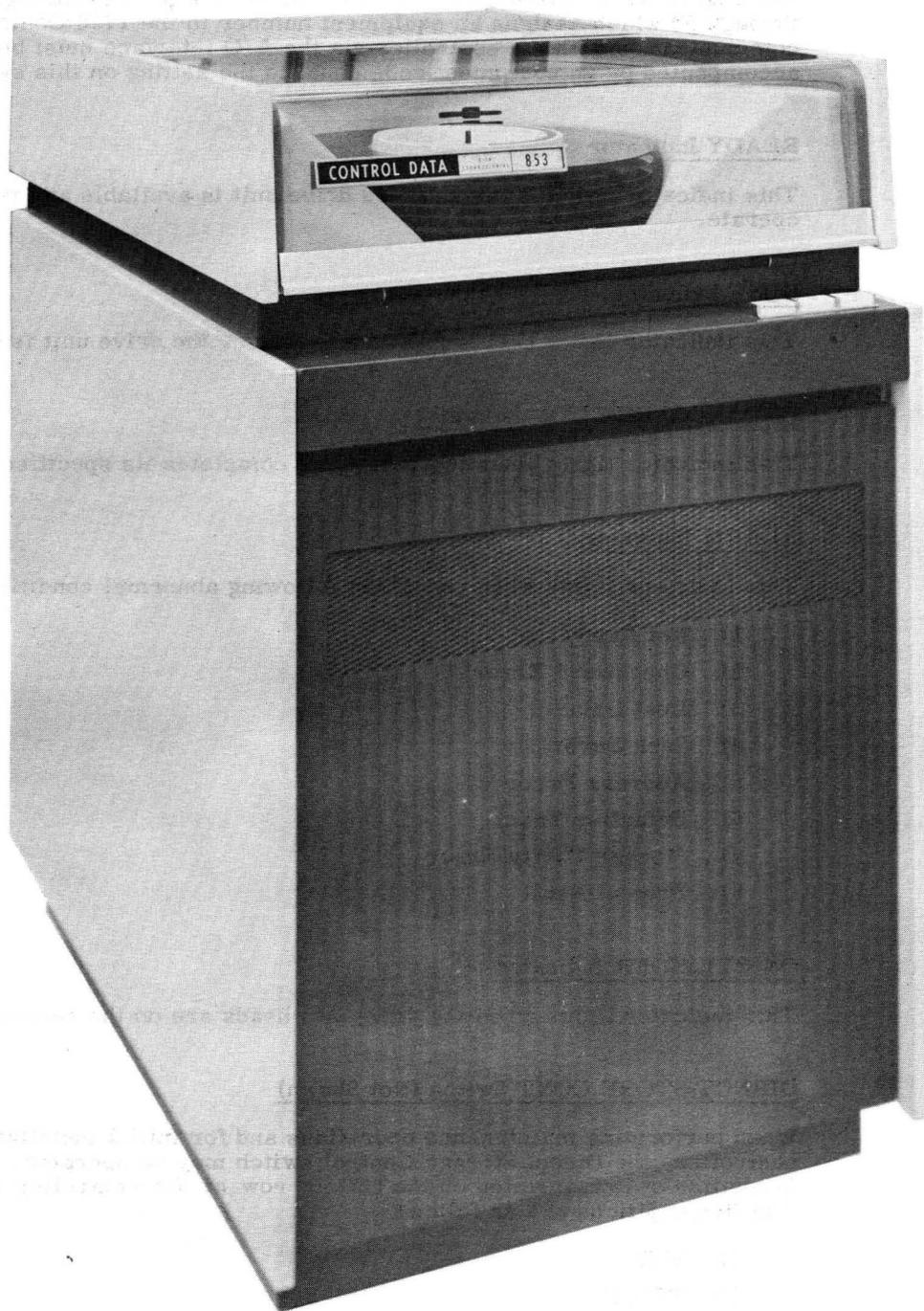
Figure 14. Disk Storage Drive Unit and Disk Pack

Operating Procedures   Operation of the subsystem is normally under program control except for a few manual operations. This section provides information for performing the manual operations on the controller, disk storage drive unit (Figure 14), and loading and unloading instructions of the disk pack.

Initial Power

When power is first applied to the subsystem (or controller), an automatic Master Clear is performed on the controller circuits. The 50-/60-cycle circuit breaker switch, located on the controller monitor panel, is normally used to turn the controller On or Off.

When the subsystem is brought up from a dead start (no power on), each drive unit requires approximately 30 seconds to come up to operating speed and load the R/W heads. As soon as the disk drive units become operable (R/W heads loaded), the Unit Designation indicator lights and operation may begin. However, a 15-minute warmup period is recommended when commencing from a cold start. The disk storage drive unit exterior switch and indicators are illustrated in Figure 15.
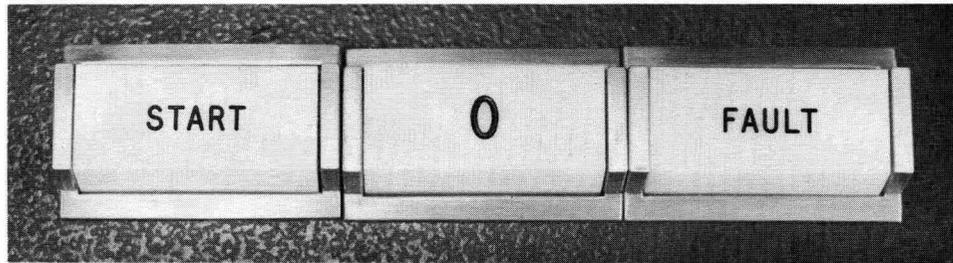
Figure 15. Disk Storage Drive Unit Exterior Switch and Indicators

Disk Pack Loading and Unloading Instructions

The disk pack is loaded and unloaded from the drive unit as follows:

  1) If the unit is operating, turn power Off by pressing the START switch located on the front of the drive unit. Wait for the spindle to stop rotating.

  2) Lift the unit cover upward as far as possible to provide maximum loading clearance.

  3) Load or unload the pack.

Loading: Place the pack onto the spindle and turn the cover handle clockwise to a full stop position. The pack should now be tight on the spindle and the cover will lift off.

Unloading: Engage the cover over the disk pack and rotate the cover three times in a counterclockwise direction. The pack will release from the spindle and can be lifted from the drive unit.

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1731-A/B MAGNETIC TAPE CONTROLLER

INTRODUCTION

The CONTROL DATA 1731 Magnetic Tape Controller synchronizes data transfer between a 1700 Computer System and up to eight 601 Tape Transports. This section describes the physical system, the programming information, and the operating procedures for the 1731 and 601.

FUNCTIONAL DESCRIPTION

System Relationship

The 1731 is used with 601 Tape Transports to control data transfer from 7-track tape on which data is recorded at 200 or 556 bits per inch (bpi). The 1731 controller is mounted in the back of one of the tape transports it controls. Figure 1 shows two possible ways the 1731 may be linked to the computer system.

The address of the controller (0 through F) is selected by the Equipment Number switch on the controller. The program protect feature of the 1700 I/O system is enabled for a specific tape transport via the switches on the controller. Any one of the eight possible tape transports connected to the controller may be selected.

Magnetic Tape

Magnetic tape provides a high-speed, nonvolatile storage medium. The tape has a plastic base and is coated on one side with a magnetic oxide. Information is recorded on this coating. Extreme care is taken to eliminate imperfections which could cause errors.

Information is read (detected) or written (stored) by passing the oxide side of the tape over read/write heads. Information may be written on any of seven independent tracks of the tape. During a Read or Write operation, the tape passes over seven evenly aligned heads; therefore, seven bits may be simultaneously recorded, one bit on each track.

A 7-track non-return-to-zero (change-on-ones) recording scheme is used. In this system, magnetic particles on the tape are aligned in either the positive or negative direction. A binary "1" is recorded by reversing the alignment (polarity); no polarity reversal indicates a "0". Thus, each track of the tape is fully magnetized and the polarity is reversed as each "1" bit is recorded.

Tape Format

Table 1 and Figure 2 describe the data format of magnetic tape. A line or frame of tape data consists of a 6-bit character and a parity (check) bit. Tracks 0 through 5 specify the character while track 6 holds the parity.

1

DIR STO ACC BUS

I N T E R R U P T S

A Q C H

1704

1731

TO
601 TAPE
TRANSPORTS
(8 MAX)

1705

DIR STO ACC BUS

I N T E R R U P T S

A Q C H

1704
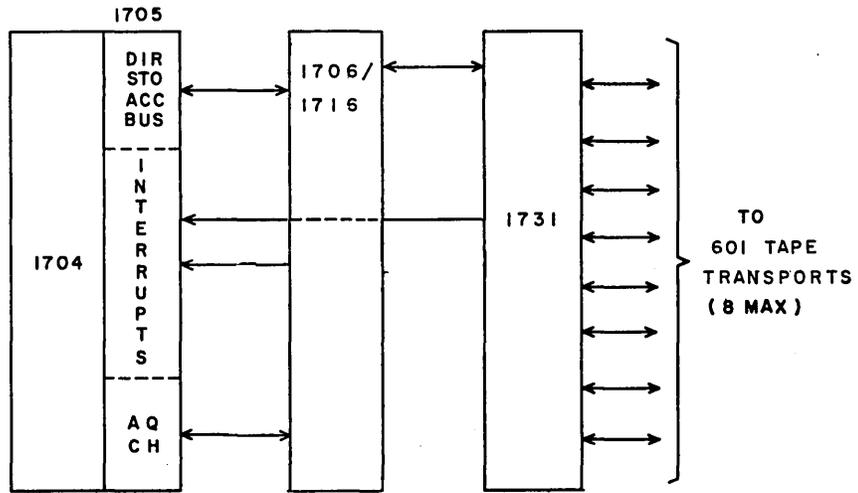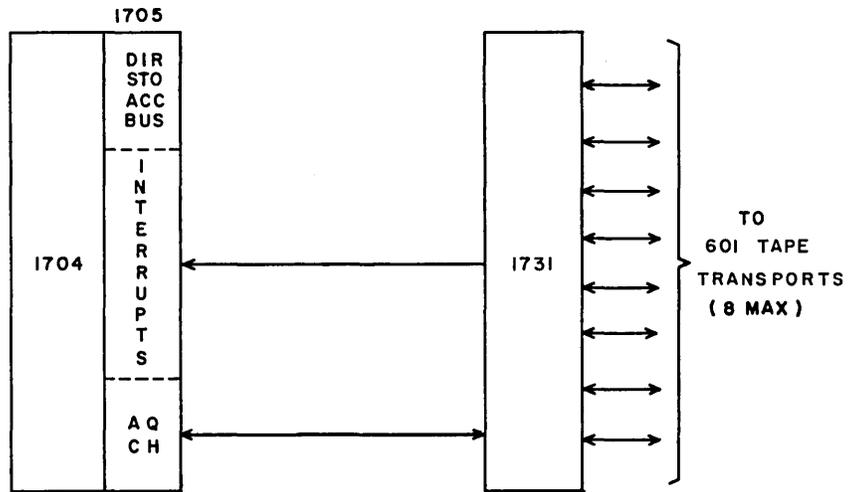
1706/ 1716

1731

TO
601 TAPE
TRANSPORTS
(8 MAX)

Figure 1. Typical Configurations

Density

The controller may be selected to synchronize data at a rate of 200 or 556 bits per inch on tape moving at 37-1/2 inches per second.

Mode

Data may be recorded in one of two modes, binary or BCD. The lower six bits comprise the data as transmitted from or received by the computer. If the mode is binary, the parity is odd. If the mode is BCD, the parity is even.

TABLE 1. 601 TAPE FORMAT

Tracks	Seven
Tape Speed	37-1/2 inches per second
Density	200 or 556 bpi
Parity	Odd (binary) or even (BCD); placed in seventh track
Longitudinal Parity	Even parity check character spaced 4 frames from last data character.
File Mark	A BCD 17_8 six inches from last record. The file mark is followed by a longitudinal check character of BCD 17_8.
Initial Gap	3.0 inches for write, 0.5 inches for read.
Record Gap	0.687 inches minimum 0.960 inches maximum
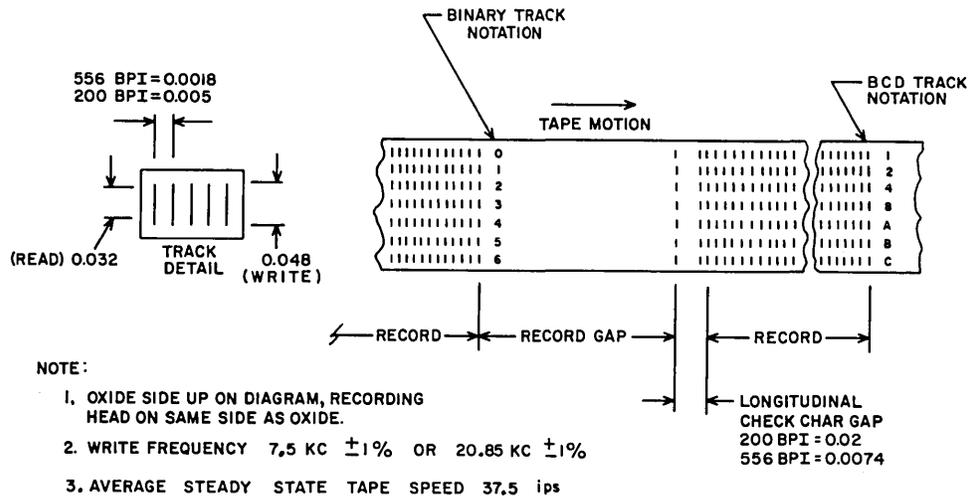
Figure 2. Tape Format

Records and Files

Data recorded on the tape is arranged in groups called records and files. A record consists of consecutive frames of information. A minimum of one frame of information constitutes a record. Adjacent records are separated by a 3/4 inch unrecorded area (record gap). A longitudinal parity check character is recorded at the end of each record; the number of "1's" in each record track is made even. A file consists of a group of records. Adjacent files are separated by recording an end-of-file marker six inches from the last record in the file.

Load Point

The load point is a reflective marker indicating the beginning of the usable portion of the tape. It is located at least 10 feet from the beginning of the tape.

End-of-Tape Marker

The end-of-tape marker is a reflective marker placed not less than 18 feet
from the end of the tape. This provides approximately 10 feet of tape
trailer and enough tape to hold a record of 96,000 characters after the end-
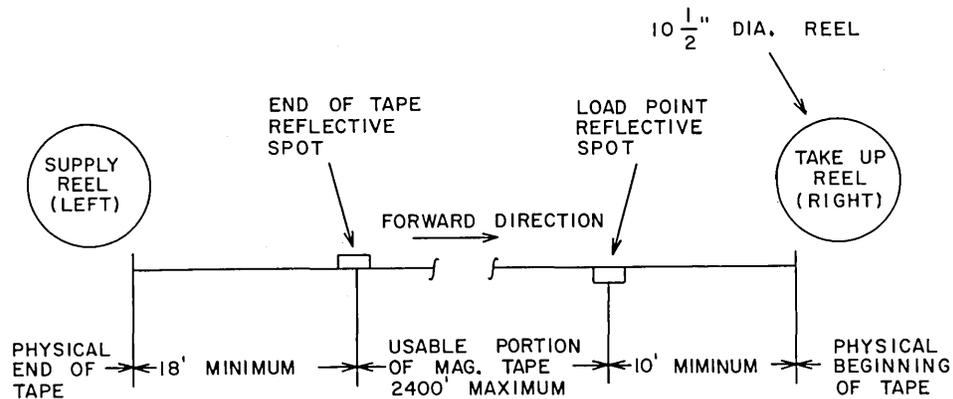of-tape marker is sensed. See Figure 3.

Figure 3. Physical Layout of Tape

Parity

The controller may be selected to operate with even (BCD) vertical parity
or with odd (binary) vertical parity. The controller generates an even
longitudinal parity check character for each physical record.

During a Write, the read heads of the tape transport transfer the newly
written character to the controller. The controller performs a parity
check and sets the Parity Error status bit if an error has occurred. If the
Alarm interrupt has been selected, an interrupt occurs.

During a Read, the parity bit recorded on the tape is checked against the
character. The Parity Error status bit sets if an error occurs. If the
Alarm interrupt has been selected, an interrupt occurs.

Master Clear

Pressing the 1704 Computer CLEAR switch clears all interrupt selections
and error conditions of a connected 1731. It clears a BCD selection, but
does not clear a connection.

Reply/Reject

The Reply signal indicates an operation requested is possible. It is
returned to the computer or converter within 4 usec and at least 0.2 usec
after the request is initiated. A Reject signal indicates the operation
requested cannot or should not be performed at that time. If neither a
Reply nor a Reject is received for 4.0 usec, the computer generates an
Internal Reject.

File Protection

The back of a tape reel has a slot near the hub for a plastic file protection
ring (Figure 4). Writing on a tape is possible only when the reel contains
a file protection ring. Reading from the tape is possible with or without
the ring. Removal of the file protection ring after writing avoids loss of
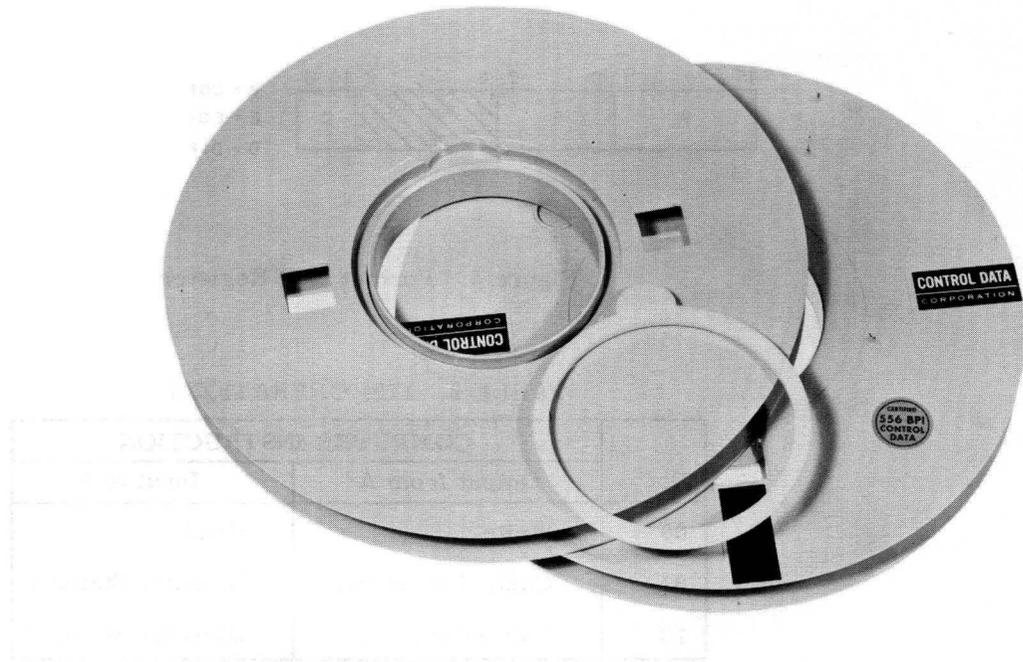valuable records due to accidental rewriting.

Figure 4. File Protection Ring

Program Protection

The 1700 I/O System has a program protect feature which reserves protected equipment for use by protected programs. A 601 Tape Transport is protected by setting the PROGRAM PROTECT switch on the 1731 controller chassis which corresponds to the setting of its Unit Select switch. When its PROGRAM PROTECT switch is set, all instructions for that tape transport (except the two status requests) are rejected if their Program Protect bit is not set or the 1704 protect system is not enabled. To explain in more detail:

1) A protected program may select any unit that is physically in the system, loaded, under external control, and Not Busy.

2) An unprotected program cannot select a tape unit whose switch is in the protected position.

After an attempt by an unprotected program to select a protected transport, the status is:

1) Not Ready, Protected - No tape transport is selected and the requested transport is protected. Any previously selected controller is unprotected and is now deselected.

2) Ready, Protected - The previously selected tape transport is still selected. Once selected, a protected transport can be broken only by using an Output from A instruction whose Program Protect bit is set to initiate either a Deselect Tape Unit function or a new Select Tape Unit function.

PROGRAMMING

Summary of Programming Information

Tables 2 through 5 and Figures 5, 6, and 7 provide the experienced programmer with the information necessary to program the 1731. The following paragraphs further define this information.
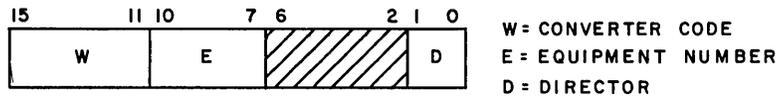
5

1731
Rev. A

```
15        11 10    7 6        2 1  0
┌──────┬──────┬──────────────┬────┐
│  W   │  E   │//////////////│ D  │
└──────┴──────┴──────────────┴────┘
```

W = CONVERTER CODE
E = EQUIPMENT NUMBER
D = DIRECTOR

Figure 5. Format of Q Register

TABLE 2. 1731 OPERATIONS

D	COMPUTER INSTRUCTION	
	Output from A	Input to A
00	Write	Read
01	Control Function	Director Status 1
10	Unit Select	Director Status 2
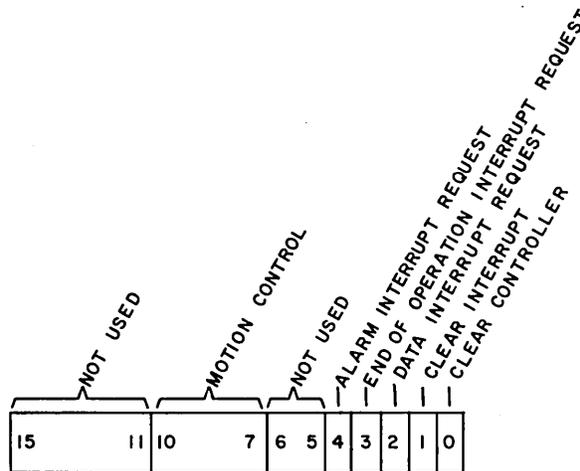
Figure 6. (A) for Control Function

TABLE 3. MOTION CONTROL

Bits 10-7 of A	Motion Function
0001	Write Motion
0010	Read Motion
0011	Backspace
0101	Write File Mark
1000	Rewind Load
1100	Rewind Unload
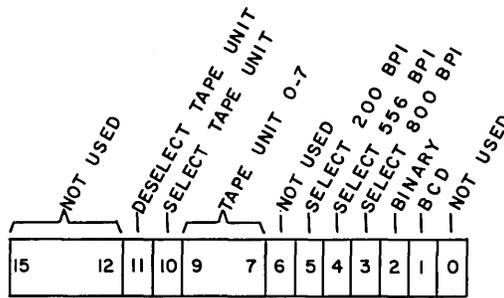
Figure 7. (A) for Unit Select

TABLE 4. DIRECTOR STATUS 1 RESPONSE BITS

BIT SET IN A REGISTER	MEANING
0	Ready
1	Busy
2	Interrupt
3	Data
4	End of Operation
5	Alarm
6	Lost Data
7	Protected
8	Parity Error
9	End of Tape
10	Load Point
11	File Mark
12	Controller Active
13-15	(Not Used)

TABLE 5. DIRECTOR STATUS 2 RESPONSE BITS

BIT SET IN A REGISTER	MEANING
0	556 bpi
1	800 bpi
2	(Not Used)
3	Seven Track
4	Write Enable
5-15	(Not Used)

Addresses

The W = 0 signal plus bits 10-7 of the Q register are used to select the desired 1731. If the 1731 is connected via the A/Q Channel, the W field of Q is always loaded with zeros. If the 1731 is connected to a converter, the converter code is placed in the W field, but the converter supplies the W = 0 signal to the controller. Bits 0-1 of Q are used to specify a command. Figure 5 illustrates the format of the Q register. Table 6 lists the values of E required to select a controller with a given equipment number setting.

TABLE 6. CONTROLLER SELECT CODES

E (BITS 10-7 OF Q)	EQUIPMENT NUMBER	E (BITS 10-7 OF Q)	EQUIPMENT NUMBER
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

Bits 10-7 of the A register are used along with the contents of Q and Output from A to select a tape transport. (See Unit Select.)

Operations

The D field of Q is combined with a 1704 Input from A or Output from A instruction to specify an operation (see Table 2). The operations initiated by an Output from A may be further modified by the contents of the A register. See Table 3, Figure 6, and Figure 7. The following paragraphs define these operations.

Operations Defined by Q and Output from A

Write: A Write transfers data from the computer to the controller which generates a parity bit and writes the data plus parity bit on the tape. To perform a Write, load Q with W = 00*, E = equipment number setting of desired 1731 controller and D = 00. An Output from A instruction initiates the transfer of the lower 6 bits of the A register to the tape.** Any number of consecutive characters sent to the tape are written (along with a parity bit) on the tape as a single record. Whenever the computer breaks the continuity of the character outputs, the controller initiates an End of Record sequence. The End of Record sequence leaves three blank character spaces, writes the longitudinal parity check character, and leaves a 3/4-inch gap.

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* W is written as two digits; the left, binary; the right, hexadecimal. If the 1731 is connected to the computer via a converter, W equals the appropriate converter code. See the reference material for that converter.

** If the output is a buffered output via the converter, the Output from A instruction supplies address information to the converter. The converter controls the buffered operation and the lower 6 bits of each word in the buffer area are written on tape.

If no new Control Function is received from the computer, tape motion stops. A Write is rejected if Not Ready or Write Motion has not been initiated.

Control Function: The Control Function operation specifies operating conditions for the selected controller and transport and initiates tape motion. To perform a Control Function, load Q with W = 00, E = equipment number, and D = 01. Load A according to Figure 6 and Table 3. Execute an Output from A. *With the exception of the Clear codes, Control Function is rejected if Not Ready, Busy, or an illegal code exists in bits 7-10 of A. Clear Controller and Clear Interrupt may be executed while the selected tape transport is Not Ready.

Table 3 lists the legal motion control codes. One motion control plus any or all clears and interrupt selections may be selected simultaneously or individually. The requests are honored in this order: clears, interrupt selections, motion control. The following describes these codes:

1) Clear Controller (A0 = 1) - directs the clearing of all interrupts, interrupt selections, errors, and File Mark status. All other select codes coded with it will also be honored. For example, A = 0011 would clear the controller and the select interrupt on end of operation.

2) Clear Interrupt (A1 = 1) - clears all interrupts and interrupt requests. If an interrupt request is coded along with a Clear Interrupt, that selection is honored, but any previous selections are cleared.

3) Data Interrupt Request (A2 = 1) - causes an interrupt to be generated when an information transfer may occur. The interrupt response is cleared by the Reply to the data transfer. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

4) End of Operation Interrupt Request (A3 = 1) - causes an interrupt to be generated at the end of an operation. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

5) Alarm Interrupt Request (A4 = 1) - causes an interrupt to be generated upon a condition which warrants program or operator attention. The Alarm interrupt is generated by any of the following conditions:

    a) End of tape,

    b) Parity error,

    c) Lost data,

    d) File mark, or

    e) When a change in Ready status is sensed at a time other than a Unit Select operation.

6) Write Motion (A10-7 = 0001) - initiates write motion. A direct or buffered output must follow for data transfer to occur. If the tape is at load point, the first word is written 3 inches after load point. All data requests (Write, Read, Write Motion, Read Motion, Backspace, Write File Mark, Rewind, Rewind Unload) are rejected while the unit is Busy and before End of Operation status. A non-stop Write operation may be done by initiating a new Write Motion function or a Write File Mark function within 4 ms after End of Operation status/interrupt.

7)   Read Motion (A10-7 = 0010) - initiates read motion. A direct or buffered input must follow for data transfer to occur. If the tape is at load point, data can be read within 0.5 inch. Control Data tape does not have information this close to the load point, but other formats do. All data requests are rejected while the unit is Busy and before End of Operation status. Read motion terminates by absence of data from the data handler for three frames. If the computer (or converter) stops requesting characters, data transfer stops but the tape continues to move to the end of the record. A non-stop Read may be done by initiating a new Read Motion function within 4 ms after End of Operation status/interrupt.

If a data transfer request is not received by the controller in time to properly complete the transfer, a lockout prevents further transfers from that block and all subsequent data transfer requests are rejected. When data is read but is not accepted by the computer, the Lost Data status bit is set.

8)   Backspace (A10-7 = 0011) - moves tape backward one record. Backspace from load point and non-stop backspace are possible.

9)   Write File Mark (A10-7 = 0101) - moves tape forward approximately 6 inches and writes a 1-character word of 17_8 with even parity. The normal End of Operation sequence is then performed, writing the longitudinal check character, 17_8. If the controller is in odd parity mode (binary) when a file mark is written or read, a parity error occurs.

10) Rewind Load (A10-7 = 1000) - rewinds tape at high speed to load point. The controller remains Busy until tape is positioned at load point and End of Operation status/interrupt occurs.

11) Rewind Unload (A10-7 = 1100) - rewinds tape to load point. The tape transport becomes Not Ready upon acceptance of the command. Manual intervention is required to reload the tape and place the transport in a Ready condition.

Unit Select: A Unit Select selects a tape transport and its operating conditions or deselects a transport. To perform a Unit Select, load Q with W = 00, E = equipment number, D = 10. Load A according to Figure 7 and Table 7, and do an Output from A. Tape unit, density, and mode (BCD or binary) can be selected simultaneously or individually. Unit Select is rejected if Controller Active or a program protect fault occurs or if an illegal code is selected (for example, two densities chosen).

TABLE 7. TAPE UNIT SELECT CODES

BITS 9-7 OF A	UNIT SELECT SWITCH SETTING
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

1)   BCD (A1 = 1) - Data is read or written in even parity.

2)   Binary (A2 = 1) - Data is read or written in odd parity.

3)   800 bpi (A3 = 1) - Data is recorded at a density of 800 bits per inch. *

4)   Select 556 bpi (A4 = 1) - Data is recorded at a density of 556 bits per inch.

5)   Select 200 bpi (A5 = 1) - Data is recorded at a density of 200 bits per inch.

6)   Tape Unit 0-7 (A9-7) - This code matches the Unit Select setting of the desired transport.

7)   Select Tape Unit (A10 = 1) - This code and bits 9-7 of A select a tape transport.

8)   Deselect Tape Unit (A11 = 1) - The purpose of this function is to disconnect a tape transport that is selected and protected, thus allowing an unprotected program access to the controller. Deselect Tape Unit must be a singular type function.

Operations Defined by Q and Input to A

Read: A Read operation transfers data from tape to the computer and checks parity. To perform a Read, load Q with W = 00, E = equipment number, and D = 00. An Input to A initiates the transfer of one 6-bit character to the lower six bits of A.** Bits 6 and 7 of A are cleared. The upper 8 bits are not changed.

The controller transfers characters to the computer until the computer (or converter) stops requesting characters, or until the controller senses the end of a record. If the computer stops requesting characters, data transfer to the computer stops, but tape motion continues until the end of the record. If a new Read Motion function is received by the controller before tape motion stops at the end of a record, motion continues in a non-stop read.

Director Status 1: Director Status 1 is a status request which loads into the A register a status reply word showing the current operating conditions of the 1731. The request is initiated by loading Q with W = 00, E = equipment number, D = 01, and executing an Input to A. Table 4 describes the contents of A register following the execution of this function. The Status Response section defines these bits.

Director Status 2: Director Status 2 is a status request which loads the A register a status reply word showing the static operating conditions of the 1731. The request is initiated by loading Q with W = 00, E = equipment number, D = 10, and executing an Input to A. Table 5 describes the contents of A register following the execution of this function. The Status Response section defines these bits.

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*Not used with 601 Tape Transport.

**If the input is a buffered input via the converter, an Output from A supplies address information to the converter. The converter controls the buffered operation and the lower 6 bits of each word in the buffer area are loaded with the characters from the tape.

Director Status 1

Table 4 lists the meaning of bits set in the A register following a status request for operating conditions. These bits are further defined below.

Ready (A0 = 1): The tape transport is connected to the equipment and the tape system can perform on command.

Busy (A1 = 1): Equipment is in operation. The 1731 becomes Busy before a Reply is returned if a function can be performed.

Interrupt (A2 = 1): An interrupt condition exists and interrupt upon this condition has been selected. This bit is cleared when the interrupt is cleared.

Data (A3 = 1): A read/write data transfer can now be performed. It is cleared by a data transfer request.

End of Operation (A4 = 1): A new tape function can now be accepted. This bit sets at the completion of all tape motion functions except Rewind Unload. During Read and Write, End of Operation signifies that parity status is valid.

Alarm (A5 = 1): This status bit monitors those conditions requiring the attention of the program or the operator. The following conditions set this bit as well as their own status bit:

1) End of tape,

2) Parity error,

3) Lost data,

4) Ready, i.e., change in Ready status is sensed at a time other than a Unit Select operation, or

5) File mark.

Lost Data (A6 = 1): The Data Transfer register was not empty when a new frame of data was received from the tape transport. This status bit sets only during a Read operation. A Lost Data condition causes all further data requests to be rejected and the Data interrupt to be disabled. Parity status is valid at the end of operation. A new Control Function can be used to clear the Lost Data condition.

Protected (A7 = 1): The PROGRAM PROTECT switch of the tape transport is enabled.

Parity Error (A8 = 1): An error was detected during data transfer or the controller has written a file mark or done a Read operation in the wrong mode. The parity check is complete and Parity Error status is valid at end of operation. Parity is not checked on backspace.

End of Tape (A9 = 1): An end of tape marker has been sensed.

Load Point (A10 = 1): A load point marker has been sensed.

File Mark (A11 = 1): A file mark has been sensed.

Controller Active (A12 = 1): Controller is Active controlling tape motion. Controller Active remains set approximately 4 ms after End of Operation following a Write, Write File Mark, or Read operation and approximately 11 ms after End of Operation following a backspace.

Director Status 2

Table 5 lists the meaning of bits set in the A register following a status request for static operating conditions. These bits are further defined below.

556 bpi (A0 = 1): The selected tape unit is set to operate at a density of 556 bits per inch.

800 bpi (A1 = 1): The selected tape unit is set to operate at a density of 800 bits per inch. This status bit should never be set when the 601 Tape Transport is connected to the 1731, but if bits 1 and 2 of A are clear, the tape is selected to operate at a density of 200 bits per inch.

Seven Track (A3 = 1): The selected tape unit is in 7-track mode. This bit should always be set when a 601 is selected.

Write Enable (A4 = 1): The file protect ring is in the supply reel and the tape has been loaded. Write operations may now be performed.

Interrupts

Interrupts are selected by the Control Function. They may be cleared by:

1) Issuing an Interrupt Clear which clears both the interrupt request and the interrupt.
2) Re-issuing the interrupt request except for the Alarm interrupt when the Alarm condition still exists, i.e., end of tape.
3) Issuing a Clear Controller.
4) Transferring data in the case of the Data interrupt.

Programming Example

This sample program performs the following:

1) Connects Equipment 1, Unit 1.
2) Selects Binary mode, 556 bpi.
3) Writes a 200-word record of all "1's".
4) As soon as Busy drops, backspaces one record.
5) Reads the 200-word record and stores the data in 200 successive memory locations.

SAMPLE PROGRAM

Hexa-decimal Address		Machine Code	Assembly Language		Comments	Step
0000	P	E000	A	LDQ =N$0082	Connect Equipment 1	00001
0001	P	O082				
0002	P	C000		LDA =N$0494	Select Unit 1, 556 bpi, Binary Mode	00002
0003	P	0494				
0004	P	0302		OUT A1-*-1		00003
0005	P	1804		JMP* A2	Reply	00004
0006	P	0000		INTERNAL REJECT	*******UNDSYM	00005
0007	P	0000	A1	EXTERNAL REJECT	Connect Reject *******UNDSYM	00006
0008	P	18F7		JMP* A	Try Again to Connect	00007
0009	P	E000	A2	LDQ =N$0081	Equipment 1	00008
000A	P	0081				
000B	P	C000		LDA =N$0080	Select Write Function	00009
000C	P	0080				
000D	P	0302		OUT A3-*-1		00010
000E	P	1804		JMP* A4	Reply	00011
000F	P	0000		INTERNAL REJECT	*******UNDSYM	00012
0010	P	0000	A3	EXTERNAL REJECT	Function Reject *******UNDSYM	00013
0011	P	18F7		JMP* A2	Reselect Write Function	00014
0012	P	C000	A4	LDA =N-200	200-Word Counter	00015
0013	P	FF37				
0014	P	60FF		STA- I		00016
0015	P	E000	A5	LDQ =N$0080	Equipment 1	00017
0016	P	0080				
0017	P	C000		LDA =N$FF	Pattern of All 1's	00018
0018	P	00FF				
0019	P	0305		OUT A6-*-1	Write 200-Word Record	00019
001A	P	D0FF		RAO- I		00020
001B	P	C0FF		LDA- I	Check Counter	00021
001C	P	0104		SAZ A7-*-1		00022
001D	P	18F7		JMP* A5		00023
001E	P	0000		INTERNAL REJECT	*******UNDSYM	00024
001F	P	0000	A6	EXTERNAL REJECT	*******UNDSYM	00025
0020	P	18F4	JMP* A5			00026
0021	P	E000	A7	LDQ =N$0081	Equipment 1	00027
0022	P	0081				
0023	P	0205		INP A8-*-1	Input Status	00028
0024	P	A000		AND =N$2	Check Busy	00029
0025	P	0002				
0026	P	0104		SAZ A9-*-1	Not Busy	00030
0027	P	18F9		JMP* A7	Loop On Busy	00031
0028	P	0000		INTERNAL REJECT	*******UNDSYM	00032
0029	P	0000	A8	EXTERNAL REJECT	*******UNDSYM	00033

SAMPLE PROGRAM (Cont'd)

Hexa-decimal Address	Machine Code		Assembly Language		Comments	Step
002A P	18F6		JMP*	A7	Re-Status	00034
002B P	E000	A9	LDQ	=N$0081	Equipment 1	00035
002C P	0081					
002D P	C000		LDA	=N$0180	Backspace	00036
002E P	0180					
002F P	0302		OUT	A10-*-1		00037
0030 P	1804		JMP*	A11	Reply	00038
0031 P	0000		INTERNAL REJECT		*******UNDSYM	00039
0032 P	0000	A10	EXTERNAL REJECT		*******UNDSYM	00040
0033 P	18F7		JMP*	A9	Re-Function	00041
0034 P	E000	A11	LDQ	=N$0081	Equipment 1	00042
0035 P	0081					
0036 P	C000		LDA	=N$0100	Select Read Function	00043
0037 P	O100					
0038 P	0302		OUT	A12-*-1		00044
0039 P	1804		JMP*	A13	Reply	00045
003A P	0000		INTERNAL REJECT		*******UNDSYM	00046
003B P	0000	A12	EXTERNAL REJECT		*******UNDSYM	00047
003C P	18F7		JMP*	A11	Reselect Read Function	00048
003D P	C000	A13	LDA	=N-200	200-Word Counter	00049
003E P	FF37					
003F P	60FF		STA-	I		00050
0040 P	E000	A14	LDQ	=N$0080	Equipment 1	00051
0041 P	0080					
0042 P	0207		INP	A15-*-1	Input Data to A	00052
0043 P	6900		STA	DATA+200,I	Store Data at Data Block	00053
0044 P	00D1					
0045 P	D0FF		RAO-	I		00054
0046 P	C0FF		LDA-	I	Check Counter	00055
0047 P	0104		SAZ	A16-*-1		00056
0048 P	18F7		JMP*	A14		00057
0049 P	0000		INTERNAL REJECT		*******UNDSYM	00058
004A P	0000	A15	EXTERNAL REJECT		*******UNDSYM	00059
004B P	18F4		JMP*	A14		00060
004C P	0000	A16	SLS		STOP *******UNDSYM	00061
004D P	00C8		BZS	DATA (200)	Data Block	00062
			END			00063

SYMBOL TABLE

A10	0032 P	A11	0034 P	A12	0038 P	A13	003D P	A14	0040 P	A15	004A P	A16	004C P
A1	0007 P	A2	0009 P	A3	0010 P	A4	0012 P	A5	0015 P	A6	001F P	A7	0021 P
A8	0029 P	A9	002B P	A	0000 P	DATA	004D P	I	00FF				

1731 Switches and Indicators

Equipment Number Switch: This 16-position switch selects the address
number of the controller. It is located on the controller chassis and can be
found by opening the back door of the tape transport in which the controller
is mounted.

PROGRAM PROTECT Switches: These eight toggle switches, one for each
tape transport, select the Program Protect condition for that transport.*
These switches are located beside the Equipment Number switch.

Controller Power On Switch: This switch, located on the power supply,
applies power to the controller power supply and blower.

CONNECT Indicator: This indicator lights when the controller is connected.
It is located on the front indicator panel of the tape transport containing the
controller.

PROTECT Indicator: This indicator lights when a protected tape transport
is selected.

BCD/PE Indicator: The BCD half of this indicator lights when BCD (even
parity) is selected. The PE half lights when a parity error occurs.

601 Switches and Indicators

Power On Switch: This switch applies initial energizing power to the tape
transport. It is located on the maintenance panel and can be found by open-
ing the lower front door of the tape transport.

POWER/WRITE ENABLE Switch/Indicator: The POWER switch/indicator
lights when power is available. Pressing the switch removes power. The
WRITE ENABLE indicator lights when the file protection ring is in place
in the supply reel.

CONNECT	PROTECT	BCD	PE	POWER	WRITE ENABLE	READY	REWIND	CLEAR	LOAD	DENSITY HI	DENSITY LO
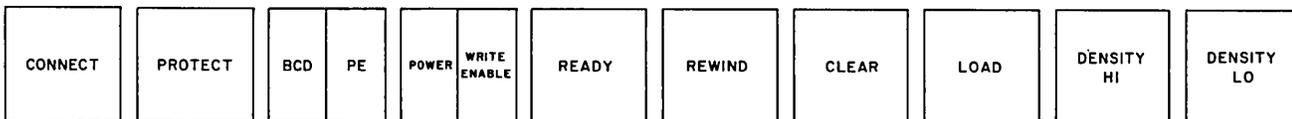
Figure 8. Switches and Indicators

_____

* See Program Protection, page 5.

READY Switch/Indicator: READY switch places the tape transport under program control. The indicator is lighted when the tape transport is under program control.

REWIND Switch/Indicator: REWIND rewinds the tape to load point at high speed. It is lighted during this operation.

CLEAR Switch: This switch Master Clears the tape transport and places it under manual control. It stops tape motion immediately.

LOAD Switch/Indicator: LOAD moves tape forward to load point. It is lighted when the tape is at load point.

DENSITY HI Switch/Indicator: DENSITY HI selects a density rate of 556 bpi and is lit if 556 bpi has been selected.

DENSITY LO Switch/Indicator: DENSITY LO selects a density rate of 200 bpi and is lit if 200 bpi has been selected.

Unit Select Switch: This eight position dial selects the unit number of the tape transport.
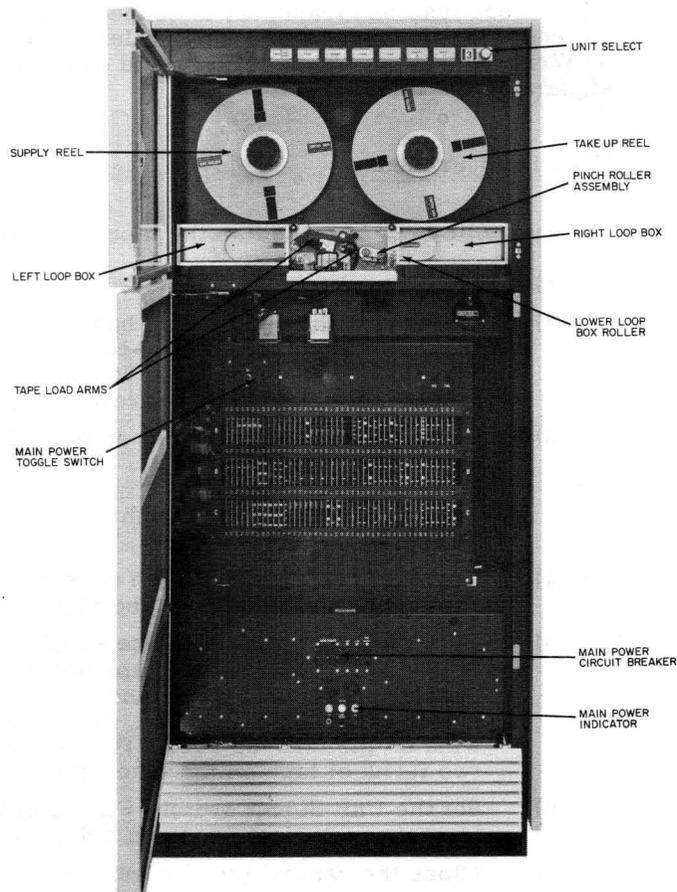
Figure 9. 601 Tape Transport

Application of Power to Tape Transport

The tape transport is initially energized as follows:

1) Open the lower door on the front of the cabinet (Figure 9).

2) Place the MAIN POWER circuit breaker in the ON position. The MAIN POWER indicator will light.

3) Place the remaining power supply circuit breakers in the ON position.

4) Hold the maintenance panel Power On switch in the ON position for approximately two seconds, then release.

5) Observe illumination of the POWER indicator on the operator panel. If the indicator fails to illuminate, repeat the procedure.

6) Close the lower front door.

The POWER switch on the operator control panel is used only to remove power from the unit. Once this switch is pushed, steps 4 and 5 must be repeated to apply primary power.

When more than one transport is connected to a single tape control unit, do not energize or deenergize a unit while a second unit is performing a Read or Write operation. This action could cause data loss due to extraneous signals on the line.

Tape Load Procedure

The magnetic tape is loaded on the tape transport as follows:

1) Open the observation window.

2) Check that the supply reel has been file-protected if necessary. If the installed supply reel contains a file protection ring, the WRITE ENABLE indicator lights when the tape unit is loaded, indicating that a Write operation may be performed.

3) Mount the tape supply reel on the left-hand hub (Figure 9) and tighten the hub knob.

   For proper alignment, push the reel firmly against the hub stop before tightening the knob.

4) Open the center door which covers the read/write heads and capstan assembly. Open the right loop box door.

5) Pull sufficient tape from the supply reel to reach the take-up (right) reel. Thread the tape under the left load arm roller, between members of the pinch roller assembly, under the lower roller of the right loop box, inside the upper idler roller, and wind on the take-up reel. Provide sufficient tape slack to allow two turns of tape on the take-up reel.

6) Set the Unit Select switch (Figure 9) to one of eight (0-7) positions to assign a logical program selection number.

7) Close the central (head cover) door. Close the right loop box door.

8) Press the LOAD switch on the operator control panel. This causes the tape loops to be pulled into the loop boxes, and the load arms to move down to position the tape over the read/write heads and into the tape guide channels.

9) The magnetic tape moves forward, stopping at the load point marker. If the tape continues to move forward for more than 3 or 4 seconds, no load point marker was placed on the tape leader area or the operator has wound the marker onto the take-up reel while performing step 5. Press the CLEAR switch to stop motion. Press the REWIND switch and wait until the tape has stopped at the load point.

10) If the unit is to be externally controlled, press the READY switch at the upper control panel. If the tape transport is to be manually operated, and the READY switch has been pressed (indicator illuminated), press the CLEAR switch.

11) Close the observation window.

Tape Unload Procedure

1) Press the CLEAR switch on the operator's control panel to remove the Ready condition.

2) Press the REWIND switch on the operator's control panel. The REWIND indicator will light and the tape will be drawn from the loop boxes before the tape transport goes into high speed rewind. Motion stops when the load point is detected.

3) With the transport stopped on the load point, press the REWIND and CLEAR switches. This drops the vacuum in the loop boxes, and the load arm rises to disengage the tape.

4) Open the observation window and manually wind the remaining tape onto the supply reel.

5) Loosen the supply reel hub knob and remove the supply reel.

NOTE

The vacuum may be dropped at any point on the tape by pressing the REWIND and CLEAR switches simultaneously.

6) Close the observation window.

Application of Reflective Marker

Reflective markers are required near the beginning of the tape (load point marker) and near the end of the tape (end-of-tape marker). These markers are plastic strips coated on one side with vaporized aluminum and on the other with adhesive, and should be 1 inch long and 3/16 inch wide. They are placed on the uncoated side of the tape.

Positioning: The load point marker is placed at least 10 feet from the beginning of the tape with the 1-inch dimension parallel to and not more than 1/32 inch from the track 0 edge of the tape (the edge nearer the operator when the reel is mounted).

The end-of-tape marker is placed at least 18 feet from the end of the tape when the tape is on the take-up reel. The 1-inch dimension should be parallel to and not more than 1/32 inch from the track 6 edge of the tape (the edge nearer the unit when the reel is mounted).

Procedure:

1) Avoid tape contamination and/or damage.

2) Perform work on a flat stationary surface.

3) Align marker properly.

4) Remove all air bubbles and excess adhesive.

CONTENTS

CONTROL DATA 1732 -A/B MAGNETIC TAPE CONTROLLER

1732-A/B MAGNETIC TAPE CONTROLLER

INTRODUCTION

The CONTROL DATA® 1732 Magnetic Tape Controller synchronizes data transfer between a 1700 Computer System and up to eight 608 or 609 Tape Transports. This section describes the physical system, the programming information, and the operating procedures for the 1732 and 608/609.

FUNCTIONAL DESCRIPTION

System Relationship

As Figure 1 illustrates, the 1732 may be attached directly to the AQ Channel or it may be attached to a 1706 or 1716 converter. The tape transports with which the 1732 is associated are the 7-track 608 and 9-track 609. These may be intermixed on the system as the user desires.

The equipment number switch, located on the controller, designates the controller address (0 through F hexadecimal). Any one of the eight tape transports attached to the controller may be selected.

Character-Assembly/Disassembly Operating Modes

The 1732 operates in either Character mode or Assembly/Disassembly mode. In Character mode the 1732 sends data bits 0-5 or 0-7 to the tape transport (depending upon whether the tape unit is 7 or 9 track). The upper 8 or 10 bits are ignored by the controller. Likewise, when the computer reads data from the tape via the 1732 in Character mode, each tape word is sent to the computer in bit positions 0-5 (or 0-7); the remaining bits are ignored by the computer.

However, in A/D mode each computer word sent to the tape via the 1732 is disassembled into two sections before being sent to the tape unit. If the computer is sending data to a 7-track 608 tape unit, data bits 8-13 comprise the first tape word and data bits 0-5 comprise the alternate tape word. Bits 6, 7, 14 and 15 are ignored.

If the computer is sending data to a 9-track 609 tape unit, data bits 8-15 comprise the first tape word and data bits 0-7 comprise the alternate tape word.

If the controller, operating in A/D mode, reads an odd number of tape words, the lower bits of the last assembled word will be filled with zeroes. The FILL status bit will set to indicate that this portion of the assembled word is not a tape word.
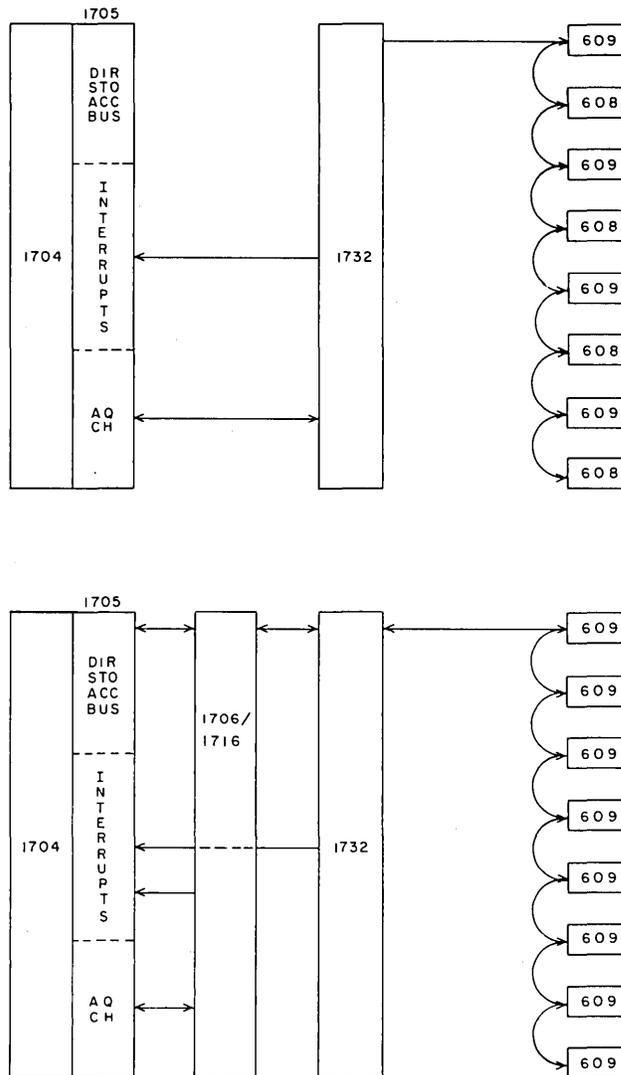
Figure 1. Typical Configurations

Magnetic Tape   Magnetic tape provides a high-speed, nonvolatile storage medium. The tape has a plastic base and is coated on one side with a magnetic oxide. Information is recorded on this coating. Extreme care is taken to prevent error-causing imperfections.

Information is read (detected) or written (stored) by passing the oxide side of the tape over read/write heads. Information may be written on any or all of the tape tracks. During a Read or Write operation, the tape passes over seven or nine evenly aligned heads; therefore, all bits of the tape word may be simultaneously recorded, one bit on each track.

A non-return-to-zero (change-on-ones) recording scheme is used. In this system, magnetic particles on the tape are aligned in either the positive or negative direction. A binary "1" is recorded by reversing the alignment (polarity); no polarity reversal indicates a "0". Thus, each track of the tape is fully magnetized and the polarity is reversed as each "1" bit is recorded.

Tape Format   Table 1 and Figure 2 describe the data format of magnetic tape. A line or frame of tape data consists of a 6-bit or 8-bit tape word and a parity bit. In a 608, tracks 0 through 5 contain the data bits and track 6 holds the parity bit. In a 609, tracks 0 through 7 contain the data bits, and track 8 holds the parity bit.

Density

The controller, when connected to the 608 tape transport, may be selected to synchronize data at a rate of 200, 556 or 800 bits per inch. When the controller is connected to a 609 tape, 800 bpi is the only possible density selection. The tape speed in both tape handlers is 37-1/2 inches per second.

Mode

The 608 tape transport records data in either of two modes: Binary mode, which uses odd parity; or BCD mode, which uses even parity. Since there is no BCD conversion in the 1732, the BCD "zero" character is illegal and should not be used.

BCD can not be used with the 609 tape transport.

TABLE 1. TAPE FORMAT

	608	609
Tracks	seven	nine
Tape Speed	37 1/2 ips	same
Density (bpi)	200 556 800	800
Parity		
Vertical	Binary-odd BCD-even placed in seventh track	odd - placed in ninth track
Longitudinal	even parity check character spaced 4 frames from last data character.	even parity check character spaced 4 frames from the CRC code word.
Cyclic Redundancy Code Word	none	spaced 4 frames from last data character
File Mark	A BCD 17_8 six inches from last record. The file mark is followed by a longitudinal check character of BCD 17_8.	none
Tape Mark	none	A 23_8 6 inches from the last record. It is followed by an ident- ical check character.
Initial Gap	3.0 inches minimum for write 0.5 inches for read	same
Record Gap	0.687 inches minimum 0.960 inches maximum 0.750 inches nominal	0.50 inches minimum 0.75 " maximum 0.60 " nominal
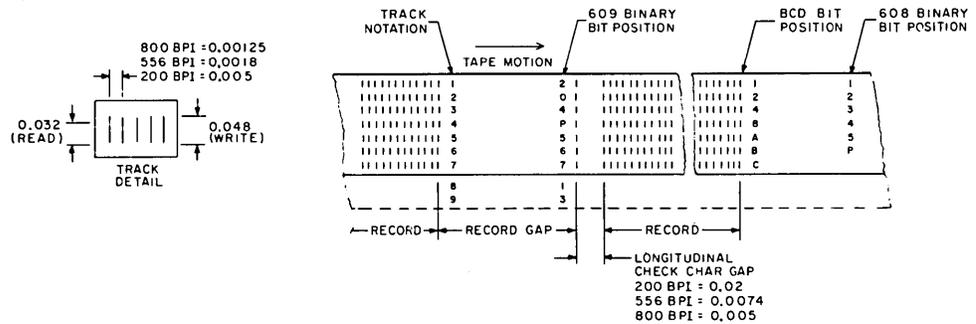
NOTES:
1. OXIDE SIDE UP ON DIAGRAM, RECORDING HEAD ON SAME SIDE AS OXIDE.
2. WRITE FREQUENCY 7.5 KC ±1%, 20.85 KC ±1%, OR 30 KC ±1%.
3. AVERAGE STEADY STATE TAPE SPEED 37.5 ips.

Figure 2. Tape Format

Records and Files

Data recorded on the tape is arranged in groups called records and files. A record consists of consecutive frames of information. A minimum of one frame of information constitutes a record. Adjacent records are separated by a 0.6 inch (609) or 3/4 inch (608) unrecorded area called a record gap. In a 609 tape transport a cyclic code word and a longitudinal parity check character are recorded at the end of each record. In a 608 tape transport the cyclic code word is not present. A file consists of a group of records. Adjacent files are separated by recording an end-of-file marker six inches from the last record in the file. In the 608 the end-of-file marker is called File Mark; in the 609 the end-of-file marker is called Tape Mark.

Load Point

The load point is a reflective marker indicating the beginning of the usable portion of the tape. It is located at least 10 feet from the beginning of the tape.

End-of-Tape Marker

The end-of-tape marker is a reflective marker placed not less than 18 feet from the end of the tape. This provides approximately 10 feet of tape trailer and enough tape to hold a record of 96,000 characters after the end-of-tape marker is sensed. See Figure 3.

Figure 3. Physical Layout of Tape

Parity

The controller may be selected to operate with even (BCD) vertical parity or with odd (binary) vertical parity. The controller generates an even longitudinal parity check character for each physical record.

During a Write, the read heads of the tape transport transfer the newly written character to the controller. The controller performs a parity check and sets the Parity Error status bit if an error has occurred. If the Alarm interrupt has been selected, an interrupt occurs.

During a Read, the parity bit recorded on the tape is checked against the character. The Parity Error status bit sets if an error occurs. If the Alarm interrupt has been selected, an interrupt occurs.

Cyclic Redundancy Check (CRC)

The Cyclic Redundancy feature is an additional check of the accuracy of data transmission and reception between the controller and the tape unit. The CRC, used by the 1732 only in conjunction with the 609, is accomplished by writing a cyclic code word at the end of each record. When the record is read by the controller, the code word should toggle the CRC register to an all clear condition if the data is correct. If the CRC determines that the data is incorrect, a parity error is indicated via the Parity Error light and via a parity error status response. Note that if the number of data characters in a record is even, the parity bit of the Cyclic code word will be odd; if the number of data characters is odd, the parity bit of the code word will be even.

Master Clear

Pressing the 1704 Computer CLEAR switch clears all interrupt selections and error conditions of a connected 1732. It clears a BCD selection and A/D mode selection, but does not clear a connection.

Reply/Reject

The Reply signal indicates an operation requested is possible. It is returned to the computer or converter within 4 μsec and at least 0.2 μsec after the request is initiated. A Reject signal indicates the operation requested cannot or should not be performed at that time. If neither a Reply nor a Reject is received for 4.0 μsec, the computer generates an Internal Reject.

File Protection   The back of a tape reel has a slot near the hub for a plastic file protection ring (Figure 4). Writing on a tape is possible only when the reel contains a file protection ring. Reading from the tape is possible with or without the ring. Removal of the file protection ring after writing avoids loss of valuable records due to accidental rewriting.

Figure 4. File Protection Ring

Program Protection   The 1700 I/O system has a program protect feature which reserves protected equipment for use by protected programs. A 608 or 609 Tape Transport is protected by setting the PROGRAM PROTECT switch on the 1732 controller chassis which corresponds to the setting of its Unit Select switch. When its PROGRAM PROTECT switch is set, all instructions for that tape transport (except the two status requests) are rejected if their Program Protect bit is not set or the 1704 protect system is not enabled. To explain in more detail:

1) A protected program may select any unit that is physically in the system, loaded, under external control, and Not Busy.

2) An unprotected program cannot select a tape unit whose switch is in the protected position.

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After an attempt by an unprotected program to select a protected transport, the status is:

1) Not Ready, Protected - No tape transport is selected and the requested transport is protected. Any previously selected transport is unprotected and is now deselected.

2) Ready, Protected - The previously selected tape transport is still selected. Once selected, a protected transport can be deselected only by using an Output from A instruction whose Program Protect bit is set to initiate either a Deselect Tape Unit function or a new Select Tape Unit function.

PROGRAMMING

Summary of Programming Information

Tables 2 through 5 and Figures 5, 6, and 7 provide the experienced programmer with the information necessary to program the 1732. The following paragraphs further define this information.
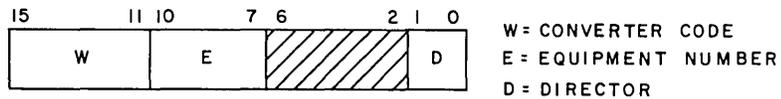
Figure 5. Format of Q Register

TABLE 2. 1732 OPERATIONS

D	COMPUTER INSTRUCTION	
	Output from A	Input to A
00	Write	Read
01	Control Function	Director Status 1
10	Unit Select	Director Status 2
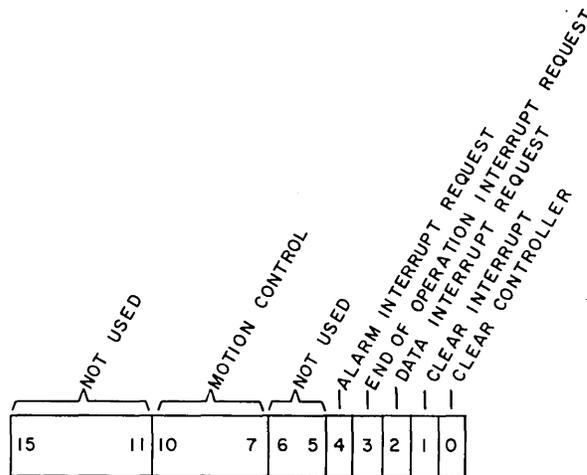
Figure 6. (A) for Control Function

TABLE 3. MOTION CONTROL

BITS 10-7 OF A	MOTION FUNCTION
0001	Write Motion
0010	Read Motion
0011	Backspace
0101	Write File Mark/Tape Mark
0110	Search File Mark/Tape Mark Forward
0111	Search File Mark/Tape Mark Backward
1000	Rewind Load
1100	Rewind Unload

Figure 7. (A) for Unit Select

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TABLE 4. DIRECTOR STATUS 1 RESPONSE BITS

BIT SET IN A REGISTER	MEANING
0	Ready
1	Busy
2	Interrupt
3	Data
4	End of Operation
5	Alarm
6	Lost Data
7	Protected
8	Parity Error
9	End of Tape
10	Load Point
11	File Mark
12	Controller Active
13	Fill
14 - 15	(Not Used)

TABLE 5. DIRECTOR STATUS 2 RESPONSE BITS

BIT SET IN A REGISTER	MEANING
0	556 bpi
1	800 bpi
2	(Not Used)
3	Seven Track
4	Write Enable
5-15	(Not Used)

Addresses

The W = 0 signal plus bits 10-7 of the Q register are used to select the desired 1732. If the 1732 is connected via the A/Q Channel, the W field of Q is always loaded with zeros. If the 1732 is connected to a converter, the converter code is placed in the W field, but the converter supplies the W = 0 signal to the controller. Bits 0-1 of Q are used to specify an operation. Figure 5 illustrates the format of the Q Register. Table 6 lists the values of E required to select a controller with a given equipment number setting.

TABLE 6. CONTROLLER SELECT CODES

E (BITS 10-7 OF Q)	EQUIPMENT NUMBER	E (BITS 10-7 OF Q)	EQUIPMENT NUMBER
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

Bits 10-7 of the A register are used along with the contents of Q and Output from A to select a tape transport. (See Unit Select.)

Operations

The D field of Q is combined with a 1704 Input from A or Output from A instruction to specify an operation (see Table 2). The operations initiated by an Output from A may be further modified by the contents of the A register. See Table 3, Figure 6, and Figure 7. The following paragraphs define these operations.

Operations Defined by Q and Output from A

Write: A Write transfers data from the computer to the controller which generates a parity bit and writes the data plus parity bit on the tape. To perform a Write, load Q with W = 00*, E = equipment number setting of desired 1732 controller and D = 00. An Output from A instruction initiates the transfer of the computer word to the tape.** Any number of consecutive characters sent to the tape are written (along with a parity bit) on the tape as a single record. Whenever the computer breaks the continuity of the computer word outputs, the controller initiates an End of Record sequence. The End of Record sequence leaves three blank character spaces, writes the cyclic code word, leaves three more spaces, writes the longitudinal parity check character, and leaves a record gap.

---

*W is written as two digits; the left, binary; the right, hexadecimal. If the 1732 is connected to the computer via a converter, W equals the appropriate converter code. See the reference material for that converter.

**If the Output is a buffered output via the converter, the Output from A instruction supplies address information to the converter. The converter controls the buffered operation.

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If no new Control Function is received from the computer, tape motion stops. A Write is rejected if Not Ready or Write Motion has not been initiated.

Control Function: The Control Function operation specifies operating conditions for the selected controller and transport and initiates tape motion. To perform a Control Function, load Q with W = 00, E = equipment number, and D = 01. Load A according to Figure 6 and Table 3. Execute an Output from A.

The controller rejects control functions if it is Not Ready, the End of Operation status condition is not present, an illegal code exists in bits 7-10 of A, or if the tape transport is Busy and Rewind or Rewind Unload function is selected.

Table 3 lists the legal motion control codes. One motion control plus any or all clears and interrupt selections may be selected simultaneously or individually. The requests are honored in this order: clears, interrupt selections, motion control. The following describes these codes:

1) Clear Controller (A0 = 1) - directs the clearing of all interrupts, interrupt selections, errors, and File Mark/Tape Mark status. All other select codes coded with it will also be honored. For example, A = 0011 would clear the controller and the select interrupt on end of operation.

2) Clear Interrupt (A1 = 1) - clears all interrupts and interrupt requests. If an interrupt request is coded along with a Clear Interrupt, that selection is honored, but any previous selections are cleared.

3) Data Interrupt Request (A2 = 1) - causes an interrupt to be generated when an information transfer may occur. The interrupt response is cleared by the Reply to the data transfer. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

4) End of Operation Interrupt Request (A3 = 1) - causes an interrupt to be generated at the end of an operation. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

5) Alarm Interrupt Request (A4 = 1) - causes an interrupt to be generated upon a condition which warrants program or operator attention. The Alarm interrupt is generated by any of the following conditions:

   a)   End of tape

   b)   Parity error

   c)   Lost data

d) File mark/tape mark, or

e) The transport goes to Not Ready during an operation.

6) Write Motion (A10-7 = 0001) - initiates write motion. A direct or buffered output must follow for data transfer to occur. If the tape is at load point, the first word is written 3 inches after load point. All data requests are rejected while the unit is Busy and before End of Operation status. For a non-stop Write, initiates a Write Motion or Write File Mark function within 5 ms after End of Operation status/interrupt.

If Write Motion is selected and no data transfer follows, the controller locks out and terminates the Write Motion function when it is time to write the first character on tape. Forward drops to the selected transport and the transport goes Not Busy after 4 ms but no End of Operation is generated. To recover from this error condition, a Unit Select or Clear Controller function can be issued to accept another motion function. An External Master Clear from the 1700 console will also reset End of Operation.

7) Read Motion (A10-7 = 0010) - initiates read motion. A direct or buffered input must follow for data transfer to occur. If the tape is at load point, data can be read within 0.5 inch. CDC tape does not have information this close to the load point, but other formats do. All data requests are rejected while the unit is Busy and before End of Operation status. Read motion terminates by absence of data from the data handler for three frames. If the computer (or converter) stops requesting characters, data transfer stops, but the tape continues to move to the end of the record. For a non-stop Read, initiate a Read Motion within 4 ms after End of Operation status/interrupt. If a data transfer request is not received by the controller in time to complete the transfer properly, a lockout prevents further transfers from the block and all subsequent data transfer requests are rejected. When data is read but not accepted by the computer, the Lost Data status bit is set if Data Request is late and data overlaps in O register.

8) Backspace (A10-7 = 0011) - moves tape backward one record. Backspace from load point and non-stop backspace and possible.

9) Write File Mark/Tape Mark (A10-7 = 0101) - moves tape forward approximately 6 inches and writes a 1-character word of 17_8 (File Mark) in a 608 or a 23_8 (Tape Mark) in a 609. The normal End of Operation sequence follows the Tape Mark/File Mark, writing the longitudinal check character. When the transport is operating in binary mode, the File Mark registers a parity error.

10) Search File Mark/Tape Mark Forward (0110) - moves tape forward until a File Mark or Tape Mark is detected; an end of operation is generated and tape motion stops.

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11) Search File Mark/Tape Mark Backward (0111) - moves tape backward until a File Mark or Tape Mark is detected. When it has been detected, an end of operation is generated, and tape motion stops. If no file mark or tape mark is detected, an end of operation will be generated and motion will stop at load point.

12) Rewind Load (A10-7 = 1000) - rewinds tape at high speed to load point. The controller remains Busy until tape is positioned at load point and End of Operation status/interrupt occurs.

13) Rewind Unload (A10-7 = 1100) - rewinds tape to load point. The tape transport becomes Not Ready upon acceptance of the command. Manual intervention is required to reload the tape and place the transport in a Ready condition.

Unit Select: A Unit Select selects a tape transport and its operating conditions or deselects a transport. To perform a Unit Select, load Q with W = 00, E = equipment number, D = 10. Load A according to Figure 7 and Table 7, and do an Output from A. Tape unit, density, and mode (BCD or binary) can be selected simultaneously or individually. Unit Select is rejected if Controller Active or a program protect fault occurs or if an illegal code is selected (for example, two densities chosen).

TABLE 7. TAPE UNIT SELECT CODES

BITS 9-7 OF A	UNIT SELECT SWITCH SETTING
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

1) Character Mode (A0 = 1) - In this mode the computer word consists of the lower 6 or 8 bits only.

2) BCD (A1 = 1) - Data is read or written in even parity (608).

3) Binary (A2 = 1) - Data is read or written in odd parity.

4) 800 bpi (A3 = 1) - Data is recorded at a density of 800 bits per inch.

5) Select 556 bpi (A4 = 1) - Data is recorded at a density of 556 bits per inch.*

6) Select 200 bpi (A5 = 1) - Data is recorded at a density of 200 bits per inch.*

7) Assembly/Disassembly Mode (A6 = 1) - In this mode the computer word consists of 12 or 16 bits which, during a write, are disassembled into two 6-or 8-bit tape words. During a Read, the tape words are assembled into the original computer word.

8) Tape Unit 0-7 (A9 - 7) - This code matches the Unit Select setting of the desired transport.

9) Select Tape Unit (A10 = 1) - This code and bits 9-7 of A select a tape transport.

10) Deselect Tape Unit (A11 = 1) - This bit disconnects a tape transport that is selected and protected, thus allowing an unprotected program access to the controller. Deselect Tape Unit must be a singular type function.

Operations Defined by Q and Input to A

Read: A Read operation transfers data from tape to the computer and checks parity. To perform a Read, load Q with W = 00, E = equipment number, and D = 00. An Input to A initiates the transfer of one 6-, 8-, 12- or 16-bit character to the lower bits of A.**

The controller transfers characters to the computer until the computer (or converter) stops requesting characters, or until the controller senses the end of a record. If the computer stops requesting characters, data transfer to the computer stops, but tape motion continues until the end of the record. If a new Read Motion function is received by the controller before tape motion stops at the end of a record, motion continues in a non-stop read.

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*Not used with 609 Tape Transport.

**If the input is a buffered input via the converter, an Output from A supplies address information to the converter. The converter controls the buffered operation. The controller loads each tape word into the buffer area.

Director Status 1:   Director status 1 is a status request which loads into the A register a status reply word showing the current operating conditions of the 1732.   The request is initiated by loading Q with W = 00, E = equipment number, D = 01, and executing an Input to A.   Table 4 describes the contents of A register following the execution of this function.   The Status Response section defines these bits.

Director Status 2:   Director Status 2 is a status request which loads the A register a status reply word showing the static operating conditions of the 1732.   The request is initiated by loading Q with W =00, E = equipment number, D = 10, and executing an Input to A.   Table 5 describes the contents of A register following the execution of this function.   The Status Response section defines these bits.

Status Response

Director Status 1

Table 4 lists the meaning of bits set in the A register following a status requset for operating conditions.   These bits are further defined below.

Ready (A0 = 1):   The tape transport is connected to the equipment and the tape system can perform on command.

Busy (A1 = 1):   Equipment is in operation.   The 1732 becomes Busy before a Reply is returned if a function can be performed.

Interrupt (A2 = 1):   An interrupt condition exists and interrupt upon this condition has been selected.   This bit is cleared when the interrupt is cleared.

Data (A3 = 1):   A read/write data transfer can now be performed.   It is cleared by a data transfer request.

End of Operation (A4 = 1):   A new tape function can now be accepted.   This bit sets at the completion of all tape motion functions except Rewind Unload. During Read and Write, End of Operation signifies that parity status is valid.

Alarm (A5 = 1): This status bit monitors those conditions requiring the attention of the program or the operator. The following conditions set this bit as well as their own status bit:

1) End of Tape,

2) Parity Error,

3) Lost data,

4) Ready, i.e., change in Ready status is sensed at a time other than a Unit Select operation, or

5) File mark/Tape mark.

Lost Data (A6 = 1): The Data Transfer register was not empty when a new frame of data was received from the tape transport. This status bit sets only during a Read operation. A Lost Data condition causes all further data requests to be rejected and the Data interrupt to be disabled. Parity status is valid at the end of operation. A new Control Function or a new Unit Selection can be used to clear the Lost Data condition.

Protected (A7 = 1): The PROGRAM PROTECT switch of the selected tape transport is enabled.

Parity Error (A8 = 1): An error was detected during data transfer or the controller has written a file mark or done a Read operation in the wrong mode. The parity check is complete and Parity Error status is valid at end of operation. Parity is not checked on backspace. This condition responds to transverse, longitudinal, and cyclic redundancy parity errors.

End of Tape (A9 = 1): An end of tape marker has been sensed.

Load Point (A10 = 1): The tape load point has been sensed.

File Mark/Tape Mark (A11 = 1): A file mark or tape mark has been sensed.

Controller Active (A12 = 1): 1732 is Active controlling tape motion. Controller remains active approximately 5.5 ms after End of Operation following a Write or Write File Mark/Tape Mark operation, approximately 4 ms after an End of Operation following a Read or a Search File Mark/Tape Mark operation, and approximately 6 ms (609) or 9.5 ms (608) after an End of Operation following a backspace or Search File Mark/Tape Mark backward.

Fill (A13=1): If an odd number of tape words is read, this status will be set to indicate that the lower portion of the word read is not a tape word. It clears on New Function Clear, Clear Controller, Master Clear or Unit Clear.

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Director Status 2

Table 5 lists the meaning of bits set in the A register following a status request for static operating conditions. These bits are further defined below.

556 bpi (A0 = 1):   The selected tape unit is set to operate at a density of 556 bits per inch.

800 bpi (A1 = 1):   The selected tape unit is set to operate at a density of 800 bits per inch. If bits 0 and 1 of A are "0", the tape is selected to operate at a density of 200 bits per inch.

Seven Track (A3 = 1):   The selected tape unit is in 7-track mode. This bit should always be set when a 608 is selected and never be set when the 609 is selected.

Write Enable (A4 = 1):   The file protect ring is in the supply reel and the tape has been loaded. Write operations may now be performed.

Interrupts

Interrupts are selected by the Control Function. They may be cleared by:

1) Issuing an Interrupt Clear which clears both the interrupt request and the interrupt.

2) Re-issuing the interrupt request except for the Alarm interrupt when the Alarm condition still exists, e.g., end of tape.

3) Issuing a Clear Controller.

4) Transferring data in the case of the data interrupt.

5) Reselecting a unit.

Programming Example

This sample program performs the following:

1) Connects Equipment 1, Unit 1.

2) Selects Binary mode, 556 bpi.

3) Writes a 200-word record of all "1's".

4) As soon as Busy drops, backspaces one record.

5) Reads the 200-word record and stores the data in 200 successive memory locations.

SAMPLE PROGRAM

Hexa-decimal Address		Machine Code	Assembly Language			Comments	Step
0000	P	E000	A	LDQ	=N$0082	Connect Equipment 1	00001
0001	P	0082					
0002	P	C000		LDA	=N$04D4	Select Unit 1, 556 bpi, Binary Mode, Assembly/ Disassembly	00002
0003	P	04D4					
0004	P	0302		OUT	A1-*-1		00003
0005	P	1804		JMP*	A2	Reply	00004
0006	P	0000				INTERNAL REJECT	00005
0007	P	0000	A1			EXTERNAL REJECT	00006
0008	P	18F7		JMP*	A	Try Again to Connect	00007
0009	P	E000	A2	LDQ	=N$0081	Equipment 1	00008
000A	P	0081					
000B	P	C000		LDA	=N$0080	Select Write Function	00009
000C	P	0080					
000D	P	0302		OUT	A3-*-1		00010
000E	P	1804		JMP*	A4	Reply	00011
000F	P	0000				INTERNAL REJECT	00012
0010	P	0000	A3			EXTERNAL REJECT	00013
0011	P	18F7		JMP*	A2	Reselect Write Function	00014
0012	P	C000	A4	LDA	=N-200	200-Word Counter	00015
0013	P	FF37					
0014	P	60FF		STA-	I		00016
0015	P	E000	A5	LDQ	=N$0080	Equipment 1	00017
0016	P	0080					
0017	P	C000		LDA	=N$FFFF	Pattern of All 1's	00018
0018	P	FFFF					
0019	P	0305		OUT	A6-*-1	Write 200-Word Record	00019
001A	P	D0FF		RAO-	I		00020
001B	P	C0FF		LDA-	I	Check Counter	00021
001C	P	0104		SAZ	A7-*-1		00022
001D	P	18F7		JMP*	A5		00023
001E	P	0000				INTERNAL REJECT	00024
001F	P	0000				EXTERNAL REJECT	00025
0020	P	18F4		JMP*	A5		00026
0021	P	18F4	A7	LDQ	=N$0081	Equipment 1	00027
0022	P	0081					
0023	P	0205		INP	A8-*-1	Input Status	00028
0024	P	A000		AND	=N$2	Check Busy	00029
0025	P	0002					

Hexa-decimal Address		Machine Code	Assembly Language			Comments	Step
0026	P	0104		SAZ	A9-*-1	Not Busy	00030
0027	P	18F9		JMP*	A7	Loop On Busy	00031
0028	P	0000				INTERNAL REJECT	00032
0029	P	0000	A8			EXTERNAL REJECT	00033
002A	P	18F6		JMP*	A7	Re-Status	00034
002B	P	E000	A9	LDQ	=N$0081	Equiment 1	00035
002C	P	0081					
002D	P	C000		LDA	=N$0180	Backspace	00036
002E	P	0180					
002F	P	0302		OUT	A10-*-1		00037
0030	P	1804		JMP*	A11	Reply	00038
0031	P	0000				INTERNAL REJECT	00039
0032	P	0000	A10			EXTERNAL REJECT	00040
0033	P	18F7		JMP*	A9	Re-Function	00041
0034	P	E000	A11	LDQ	=N$0081	Equipment 1	00042
0035	P	0081					
0036	P	C000		LDA	=N$0100	Select Read Function	00043
0038	P	0302		OUT	A12-*-1		00044
0039	P	1804		JMP*	A13	Reply	00045
003A	P	0000				INTERNAL REJECT	00046
003B	P	0000				EXTERNAL REJECT	00047
003C	P	18F7		JMP*	A11	Reselect Read Function	00048
003D	P	C000	A13	LDA	=N-200	200-Word Counter	00049
003E	P	FF37					
003F	P	60FF		STA-	I		00050
0040	P	E000	A14	LDQ	=N$0080	Equipment 1	00051
0041	P	0080					
0042	P	0207		INP	A13-*-	Input Data to A	00052
0043	P	6900		STA	DATA+200, I	Store Data at Data Block	00053
0044	P	00D1					
0045	P	D0FF		RAO-	I		00054
0046	P	C0FF	LDA-	I		Check Counter	00055
0047	P	0104		SAZ	A16-*-1		00056
0048	P	18F7		JMP*	A14		00057
0049	P	0000				INTERNAL REJECT	00058
004A	P	0000				EXTERNAL REJECT	00059
004B	P	18F4		JMP*	A14		00060
004C	P	0000	A16	SLS	O	STOP	00061
004D	P	00C8		BZS	DATA (200)	Data Block	00062
				END			00063

A10	0032	P	A11	0034	P	A12	0038	P	A13	003D	P	A14	0040	P	A15	004A	P	A16	004C	P
A1	0007	P	A2	0009	P	A3	0010	P	A4	0012	P	A5	0015	P	A6	001F	P	A7	0021	P
A8	0029	P	A9	002B	P	A	0000	P	DATA	004D	P	I	00FF							

MANUAL OPERATION

Switches and Indicators

1732 Switches and Indicators

Equipment Number Switch: This 16-position switch selects the address number of the controller. It is located on the controller chassis and can be found by opening the back door of the controller cabinet.

PROGRAM PROTECT Switches: These eight toggle switches, one for each tape transport, select the Program Protect condition for that transport. *
These switches are located beside the Equipment Number switch.

TEST MODE Switch: This switch, located on the controller chassis beside the PROGRAM PROTECT switches, activates the controller test mode.
Test mode provides the means for checking the hardware which generates the cyclic redundancy character. This feature is intended for checkout and diagnostic purposes only, and care should be taken to deactivate the TEST MODE switch (down position) before attempting normal operation.

Controller Power On Switch: This switch, located on the power supply, applies power to the controller power supply and blower.

CONNECT Indicator: This indicator lights when the controller is connected and has selected a tape unit. It is located on the front indicator panel of the controller cabinet.

PROTECT Indicator: This indicator lights when a protected tape transport is selected.

*See Program Protection.

BCD/PE Indicator: The BCD half of this indicator lights when BCD (even parity) is selected. The PE half lights when a parity error occurs.

608/609 Switches and Indicators

The Operator Control Panel Contains the following switches and indicators.

POWER Switch: Applies/removes power from all tape transport components. When lighted, power is on.

WRITE ENABLE Indicator: This indicator lights when write ring is installed in tape reel.

READY Switch/Indicator: This switch places the tape transport under external control. It is lighted when under external control.

CLEAR Switch/Indicator: CLEAR master clears all previous tape transport settings and conditions. When lighted, it indicates a clear or fault condition.

LOAD Switch/Indicator: The LOAD switch loads tape into loop box vacuum columns and moves tape forward until the load point marker is sensed. The indicator shows that tape is at the load point.

REWIND Switch/Indicator: This switch moves tape in reverse at high speed (150 ips) until load point marker is sensed. It lights during the high speed tape movement.

200 Switch/Indicator*: This switch selects density of 200 bpi, and indicator shows this density is selected.

556 Switch/Indicator*: This switch selects density of 556 bpi, and indicator shows this density is selected.

---

*608 Tape Transport only.

800 Switch/Indicator: This switch selects density of 800 bpi and lights to show that this density is selected.

UNIT SELECT Switch: This switch assigns an address designation to the tape transport for external control.

The Maintenance Panels (front and rear) contain the following.

FORWARD Switch: FORWARD moves tape forward at normal speed of 37-1/2 inches per second.

CLEAR Switch: This switch master clears all previous tape transport settings and conditions.

REVERSE Switch: REVERSE moves tape in reverse at normal speed.

LEVEL Switch: (rear maintenance panel only) This switch increases or decreases read clipping level voltage by percentage shown at various switch positions.

The following are found on the Power Supply Panel.

COOLING FAN Circuit Breaker: This provides overload protection for the cooling blower motor.

CAPSTAN MOTOR Circuit Breaker: This provides overload protection for the capstan and rewind motors.

MAIN POWER Circuit Breaker: This protects the power supply from overload.

MAIN POWER Indicator: This shows that line power is supplied to the power supply.

-20 and +20 Circuit Breakers: These provide overload protection for the respective dc circuits.

PNEUMATIC MOTORS Circuit Breaker: These provide overload protection for the rotary pump motor and loop box vacuum pump.

-20, +20 and GRD Test Jacks: These are connection points for monitoring the respective dc voltages.

Operating Procedures

Power Application

1)   Open the rear door of tape transport.

2)   Turn on all circuit breakers.

3)   Close rear door of tape transport.

4)   Check that Unit Select switch on operator control panel is in desired position.

5)   Press POWER switch on operator control panel.

Tape Loading Procedure

1)   Press down on top of window assembly to open.

2)   Check that the reverse reel (supply reel) has a write ring if a Write operation is to be performed.   Remove the ring for a Read operation.

<div align="center">

CAUTION

Make sure that valuable information has not been stored on the reel before using it for Write operation.

</div>

3)   Place the reverse reel on the reel hub.   Press the reel against the hub stop and close the reel knob latch.

4)   Check that the pad is not under the head assembly.   If necessary, press down on the shield arm assembly handle until it latches.

5)   Unwind about 4 feet of tape from the reverse reel.   Thread tape along the tape path as follows:

a) Place the tape under the tape guide that is located near the reverse reel and then over the top of the head assembly.

CAUTION

The first few feet of tape become extremely dirty due to repeated handling. Avoid contamination of the head assembly by keeping this portion of the tape away from the head assembly.

b) Place the tape under the tape guide that is located near the forward reel and then thread onto the forward reel.

c) Hold the end of the tape in place and turn the forward reel clockwise until tape-to-tape contact is made on the forward reel. Continue winding a few more feet of tape onto the forward reel.

NOTE

Wind sufficient tape onto the forward reel to allow for loading the vacuum column. Do not allow the load point reflective marker to move beyond the sensor.

d) Slide the tape under the head assembly.

e) Take up the tape slack by turning the forward reel clockwise.

6) Press the shield arm assembly release lever. The pad should move up, contacting the tape and the head assembly.

7) Close the window assembly.

8) Press the LOAD switch on the operator control panel. If a write ring is installed in the reverse reel, the WRITE ENABLE indicator on the operator control panel should light. Tape should be drawn into the vacuum columns and move forward until the load point reflective marker is sensed. When tape stops at load point, the LOAD indicator on the operator control panel should light.

Local Operation

1) Apply power and load tape.

2) Press the FORWARD switch on either the front or rear maintenance panel. Tape should move forward.

3) Press the REVERSE switch on either the front or rear maintenance panel to move tape in reverse.

4) Press the CLEAR switch on either the front or rear maintenance panel or the operator control panel to stop forward or reverse tape motion.

External Operation

1) Apply power and load tape.

2) Press the READY switch on the operator control panel. The READY indicator on the operator control panel should light. The tape transport is now under external control.

Unload Tape Procedure

1) Press either CLEAR switch to stop tape motion and to remove the Ready Condition.

2) Press the REWIND switch on the operator control panel. The RE-WIND indicator on the operator control panel should light and tape should move in reverse at high speed until it stops at load point.

3) Again press the REWIND switch. Tape should completely unwind from the forward reel and drop into the vacuum column.

4) Open the window assembly. Manually wind the remaining tape onto the reverse reel.

5) Raise the reel knob latch and remove the reverse reel.

6) Remove the write ring from the tape reel if recorded information is to be preserved. Label the tape reel to ensure that information is not destroyed.

Power Removal

1) Press the POWER OFF switch on the operator control panel. The POWER indicator should go out.

2) Open the rear door of the tape transport. Turn off the MAIN POWER circuit breaker.

Application of Reflective Marker

Reflective markers are required near the beginning of the tape (load point marker) and near the end of the tape (end-of-tape marker). These markers

are plastic strips coated on one side with vaporized aluminum and on the other with adhesive, and should be 1 inch long and 3/16 inch wide. They are placed on the uncoated side of the tape.

Positioning: The load point marker is placed at least 10 feet from the beginning of the tape with the 1-inch dimension parallel to and not more than 1/32 inch from the track 0 edge of the tape (the edge nearer the operator when the reel is mounted).

The end-of-tape marker is placed at least 18 feet from the end of the tape when the tape is on the take-up reel.   The 1-inch dimension should be parallel to and not more than 1/32 inch from the track 6 (608) edge of the tape (the edge nearer the unit when the reel is mounted).

Precautions:

    1)   Avoid tape contamination and/or damage.

    2)   Perform work on a flat stationary surface.

    3)   Align marker properly.

    4)   Remove all air bubbles and excess adhesive.

CONTENTS

FIGURES

TABLES

CONTROL DATA 430 CARD READER/PUNCH WITH 1728-A/B CONTROLLER

2601

1728-A/B CARD READER/PUNCH CONTROLLER

INTRODUCTION

The CONTROL DATA® 1728-A/B Card Reader/Punch Controller operates with a CONTROL DATA® 430 Card Reader/Punch. The controller contains eleven 50-PAKS; six for control and interface, and five for operating the Card Reader/Punch mechanism. The controller interfaces with one 1700 Data Channel, either normal or buffered. Function codes transmitted via the data channel initiate and control the reading and punching of cards, and they enable the generation of interrupts when the specified conditions exist. The Card Reader/Punch mechanism is a non-buffered, column-oriented, punched-card, read-punch device with no code conversion. It contains a hopper, stacker, and power supply.

FUNCTIONAL DESCRIPTION

System Relationship

The controller may interface with the 1706 Data Channel for buffered communication or the 1705 Data Channel for normal (non-buffered) communication. Typical configurations are shown in Figure 1. The interface logic in the controller provides access to the card reader via station one, and to the punch via station two of the selected equipment. Data is transferred to and from the Card Reader/Punch in 16-bit computer words with the lower 12 bits containing the information in one card column (data bit 00 corresponds to card row 9). The Q register in the computer designates the use of the A register bits in the 16-line address cable. Bits of the Q register define the equipment number and whether communication is to be with the reader or punch. With a Read or Write signal, they also define A register bits as function codes, status, or data.
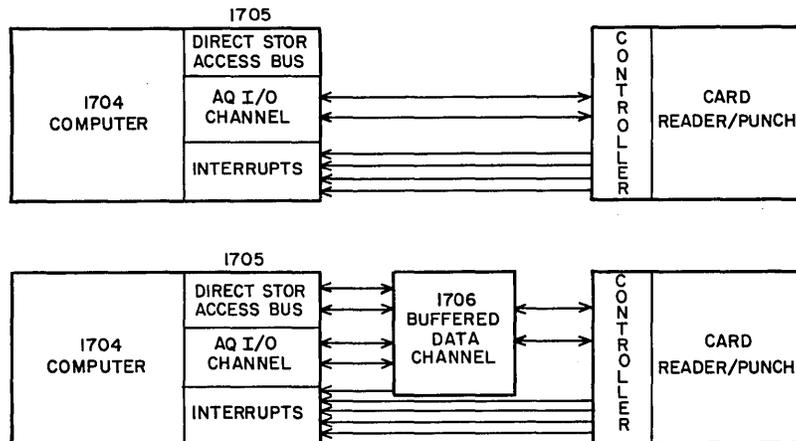
Figure 1. Typical Configurations

Capabilities

The maximum operating rate of the Card Reader/Punch is 500 cards per minute while reading, and 100 cards per minute while punching all card columns. The punching rate is dependent on the number of columns sequenced for punching, with a maximum rate of 476 cards per minute if only the first column is punched. The capacity of the input hopper is 1,200 cards and the capacity of the output stacker is 1,300 cards.

Functional Stations

Refer to Table 1 for a description and to Figure 2 for a diagram of the seven functional stations in the Card Reader/Punch.

TABLE 1. DESCRIPTION OF FUNCTIONAL STATIONS

STATION NUMBER	STATION	DESCRIPTION
1	Hopper	Holds a supply of cards and feeds them to the read ready station.
2	Read Ready	Retains each card as it is fed from the hopper.
3	Read	Examines the cards and presents one column of data on the 12 lines to the logic.
4	Punch Ready	Receives the card as it leaves the read station and indexes it in preparation for punch column one.
5	Punch	Perforates one column of a card for each step as directed by the data lines.
6	Routing	Receives cards as they leave the punch and enables the 3/8 inch offset if directed by the controller.
7	Stacker	Holds the funished card to maintain original card sequence.
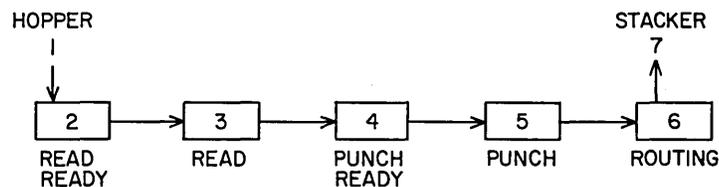
HOPPER   STACKER
1   7

2	→	3	→	4	→	5	→	6
READ READY		READ		PUNCH READY		PUNCH		ROUTING

Figure 2. Functional Stations

Timing

Timing intervals for various operations are as follows:

Feed Timing

A card may be fed at intervals of 120 ms for a maximum 500 card-per-minute rate. While operating at this rate, a maximum of 35 ms will be available after reading card column 80 before the controller need issue its decision to feed the next card. A feed cycle may be initiated at any time while punching.

Read Timing

The read time for card columns 1 through 80 is 57.275 ms. The average time for reading a card column is 725 usec. Column one will be present for reading approximately 18 ms after the initiation of a feed cycle from a static position with the motor running, or 60 ms after feed-cycle initiation from a column 80 position.

Punch Timing

The punch time for columns 1 through 80 is 474 ms. A card column may be punched at intervals of 6 ms for a maximum rate or at any slower rate required. A card is ready for punching approximately 120 ms after the feed cycle is initiated.

Offset Timing

A card will be offset in the stacker if an Offset command is issued any time after reading column 40, and before 10 ms have elapsed of the card cycle in which the card is moving to the routing station.

Definitions of Conditions and Operations

Various conditions and operations in the Card Reader/Punch are defined as follows:

Ready

A Ready condition exists when the Card Reader/Punch is capable of performing all its functions. Pressing the READY switch causes the equipment to become ready if the power supply is in operation, cards are in the input hopper, the stacker is not full, there is no jam condition, the chip box is in place and not full, and the top lid interlock is closed.

Reader Busy

The reader becomes busy when a feed cycle is initiated and remains busy until the completion of a card (81st column time), or until lost data occurs.

Punch Busy

The punch becomes busy when a Reply is sent for the first data output and remains busy until a Feed command is issued or the completion of a card (81st column time).

Read Operation

A Read operation is the time between the acceptance of a Feed command to station 1, and the completion of a card (81st column time) or the time lost data occured.

NOTE

In this equipment, reader and punch operations are
not allowed to overlap.

Punch Operation

A Punch operation is the time between the acceptance of the first data word to station 2 and the completion of a card (81st column time).

NOTE

If the Read or Punch operation is terminated before the 81st column time with a Feed command, no end of operation status or interrupt is issued.

Alarm

An alarm indicates the presence of an abnormal condition. Two types of abnormal conditions can occur; those which require the Card Reader/Punch to go Not Ready, and require operation intervention, and those which allow the Ready status to remain, and do not require operator intervention.

Alarm with Not Ready: This Alarm condition is caused by a condition which causes the Card Reader/Punch to become Not Ready. These conditions are the chip box full, chip box not in place, hopper empty, stacker full, feed alert, or open interlock on the top lid. The alarm is cleared upon correction of the cause for the Not Ready condition.

Alarm with Ready: This Alarm condition is caused by lost data or a punch or read error. The alarm may be cleared by a Master Clear or a Clear Card Reader/Punch director function code.

Error Indications

Not Ready

The absence of any one of the following Ready conditions results in a Not Ready error condition.

    a.   Power supply in operation.

    b.   Cards in the input hopper.

    c.   Card stacker not full.

    d.   No card jam condition.

    e.   Chip box in place and not full.

    f.   Top lid interlock closed.

Pre-read Error

This error occurs if all read amplifiers are not on during a light check, or if the amplifiers are not off during a dark check.

Punch Error

This error occurs when a faulty signal is detected in the area of the punch solenoid and echo amplifier circuits during echo checks.

Alarm

The presence of any abnormal condition results in an Alarm error. An alarm can cause the equipment to go Not Ready or it can exist and allow the Ready state to remain. Conditions causing a Not Ready are:

a. Chip box full or out of place.

b. Hopper empty.

c. Stacker full.

d. FEED ALERT indicator lighted.

e. Open top lid interlock.

Conditions allowing the Ready state to remain are:

a. Lost data.

b. READ ALERT or PUNCH ALERT indicators lighted.

Feed Alert

This error occurs when there has been a failure in the transport of a card. This may be due to a card failing to feed, or a jam occuring in the read, punch, or stacker area.

PROGRAMMING   Table 2 and Figures 3 through 8 provide programming information.

A description of the codes follows the figures.

TABLE 2. SUMMARY OF Q REGISTER FUNCTIONS

Q REGISTER		DESCRIPTION
FORMAT	SYMBOL	
CONVERTER CODE	(W)	W=0 must be present for all Card Reader/Punch operations.
EQUIPMENT CODE	(E)	Set Equipment Select switches - positions 0 thru F (An Equipment Code setting must be present for all operations).
STATION CODE	(S)	Select station (Q05, Q06) For reader, Q05=1 and Q06=0 with Read signal. For punch, Q05=0 and Q06=1 with Write signal.
DIRECTOR CODE	(D)	Defines operation (Q00, Q01) For data, Q00=0 Reader, Q05=1, Q06=0 with Read signal. Punch, Q05=0, Q06=1 with Write signal. For function, Q00=1 with Write"out" signal and Station code. For status, Q00=1, with a Read "in" signal, and the following: for Level 1, Q01=0 for Level 2, Q01=1
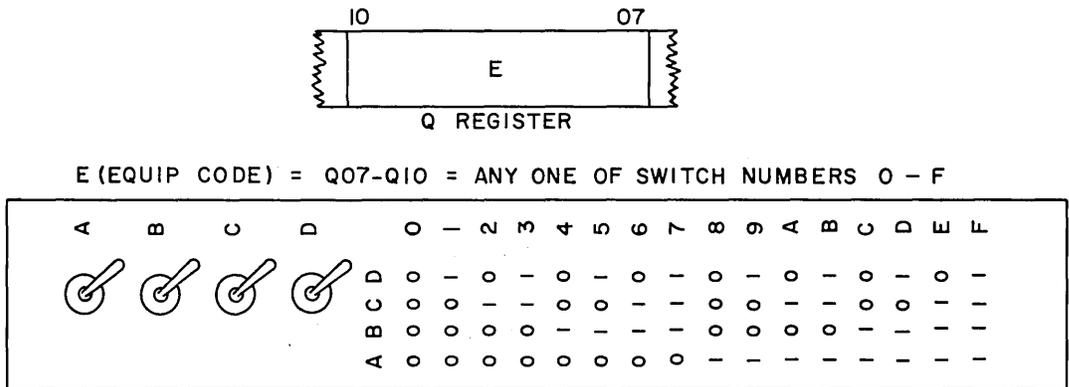
Figure 3. Equipment Select Switches
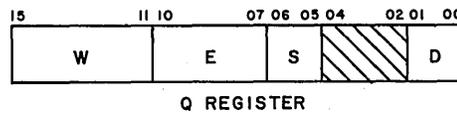
E (EQUIP CODE) = Q07-Q10 = ANY ONE OF SWITCH NUMBERS 0 - F

Figure 4. Q Register Format
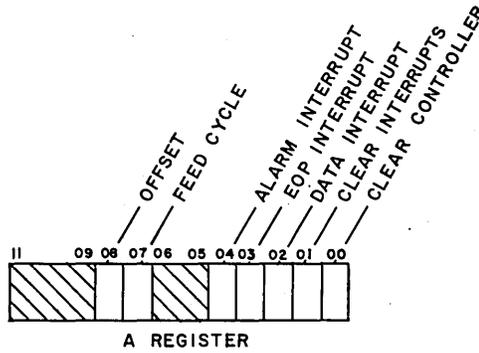
Figure 5. Function Code Format
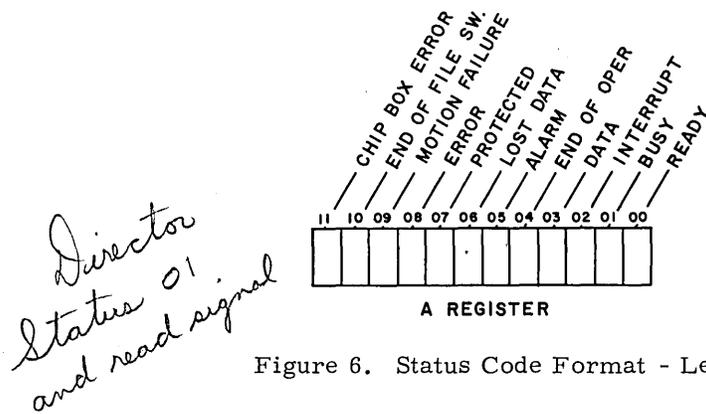
Figure 6. Status Code Format - Level 1

Director Status 01 and read signal

See table 2 Pg 5

Director Status
01 or 11 and
no read signal

INTERLOCK
PUNCH INHIBIT
MANUAL
PUNCH ERROR
PRE-READ ERROR
STACKER AREA JAM
PUNCH AREA JAM
READER AREA JAM
FAIL TO FEED
STACKER FULL
HOPPER EMPTY

11 10 09 08 07 06 05 04 03 02 01 00
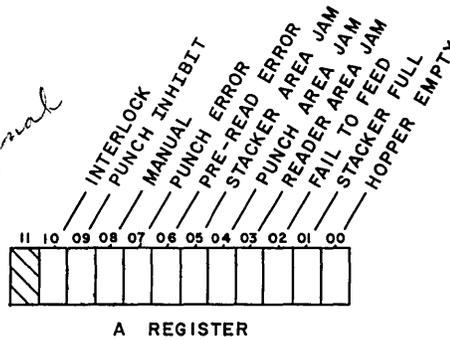
A REGISTER

see table 2 page 5

Figure 7.   Status Code Format - Level 2

WRITE DATA (Q00 = 0, WRITE)
11   00

A REGISTER

READ DATA (Q00 = 0, READ)
11   00

ADDRESS CABLE
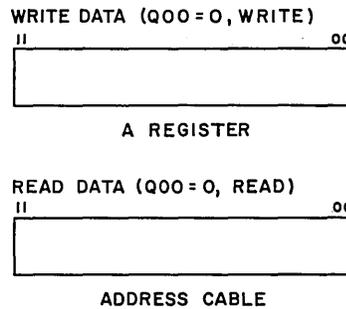
Figure 8.   Data Transfer Format

CODES

Converter

The W portion of the Q register (Q11-Q15) must be all "0's" for all Card Reader/Punch operations.

Equipment

The E portion of the Q register (Q07-Q10) defines the Card Reader/Punch equipment code.   The code is set up by the switches shown in Figure 3. If the switch settings match bits 07-10 of Q, the equipment responds.

Command

When accompanied by an equipment code and either a Read or Write signal, a command code defines the operation to be performed.   The command code consists of a station (S) code and a director (D) code.   Only bits 05 and 06 of the S code are used.   When Q5=1 and Q6=0, the station being communicated with is the reader.   When Q5=0 and Q6=1, the station being communicated with is the punch.   The D portion of Q (Q00 and Q01) defines the word being sent as data, or director function or status codes.

see figure 4

S = 2 = reader
S = 1 = punch
S = 0 or 3 = error

NOTE

If both Q5 and Q6=1, or if both Q5 and Q6=0, the Card Reader/Punch will not accept the word being sent, and will not send a Reply or Reject signal.

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DATA TRANSFER

Read Data (Q00=0, Q01=0, Q05=1, Q06=0)

When bit Q05 is a "1" and bits Q00, Q01 and Q06 are "0", the 16 lines of the data cable (A) are directed to perform a data transfer as specified by the Read signal. A Reject condition will occur if the data cannot be transferred. The card reader will reject data when:

    a.   The Card Reader/Punch is not ready.

    b.   The computer attempts to input data at a rate that exceeds the capabilities of the Card Reader/Punch.

    c.   The 80th column has been read or a feed command has been accepted and a new card has not been registered in the read station.

Write Data (Q00=0, Q01=0, Q05=0, Q06=1)

When bit Q06 is a "1" and bits Q00, Q01, and Q05 are "0", the 16 lines of the data cable (A) are directed to perform a data transfer as specified by the Write signal. A Reject will occur if data cannot be accepted. The punch will reject data when:

    a.   The Card Reader/Punch is Not Ready.

    b.   The computer attemps to output data at a rate that exceeds the capabilities of the Card Reader/Punch.

    c.   The 80th column has been punched and a new card has not yet been registered in the punch station.

DIRECTOR FUNCTIONS (Q00=1, Q01=0)

When Q00 is "1" and Q01 is "0", and they are accompanied by an equipment and station code, together with a Write signal, the 16 lines of the data cable (A) will direct the Card Reader/Punch to perform the following operations. Director functions may be stacked (two or more functions sent simultaneously).

Clear Card Reader/Punch (A00=1)

This function directs the clearing of all interrupt requests and responses, motion requests, errors, and other logic which may be cleared. This bit is subordinate to bits A02 through A08.

NOTE

    The Card Reader/Punch will execute and reply to this function if it is Not Ready, provided that no other director bit, except A01, is transmitted with it (bits A02 through A08 must be zero). Care should be exercised in using this function while the Card Reader/Punch is busy.

Clear Interrupts (A01=1)

This function directs that all Interrupt Requests and their responses be cleared. It is subordinate to the interrupt request bits A02 through A04.

NOTE

The Card Reader/Punch will execute and reply to
this function if it is Not Ready, provided that no
other director bit, except A00, is transmitted with
it (bits A02 through A08 must be zero).

Data Interrupt Request (A02=1) $0000\ 0000\ 0000\ 0100$

This function causes the data Interrupt Request FF to be set. This causes an
interrupt to be generated when an information transfer may occur. The
interrupt will be cleared by a reply to a data transfer. Interrupt request
and response is cleared by bit A00 or A01. Interrupt request takes preced-
ence over function clears. Each station (punch or reader) has a data inter-
rupt request.

Interrupt on End of Operation (A03=1) $0000\ 0000\ 0000\ 1000$

The purpose of this interrupt is to notify the computer that the unit is
finished with an operation or that some condition existed at the end of the
last data transfer which will prevent any further data transfers. Interrupt
request and response is cleared by bit A00 or A01. Interrupt request takes
precedence over function clears. Each station has an End of Operation
interrupt request.

The interrupt may be selected before or during the operation. An interrupt
response will not occur for an operation which was ended before the selection
was made.

Alarm Interrupt Request (A04=1) $0000\ 0000\ 0001\ 0000$

This function enables the generation of an interrupt when an Alarm condition
exists. These conditions are listed in the Alarm section. An Alarm con-
dition that exists at the time of the interrupt request will immediately pro-
vide a response. If the Alarm condition does not exist at the time of the
interrupt request, the interrupt response will be provided as soon as the
Alarm condition is detected.

The Alarm Interrupt Request may be cleared by a Master Clear or by either
A00=1 or A01=1 with A04=0.

The interrupt response may be cleared by a Master Clear or by either
A00=1 or A01=1. When the interrupt response is cleared by Director
Function A00=1 or A01=1, the interrupt request may be reset with the same
operation if A04=1.

Director functions A05 and A06 are not used.

Feed Request (A07=1)

This function directs the Card Reader/Punch to initiate a feed cycle and to
advance the next card.

    a.   Feed and Read - When a Feed Request is initiated with Q05=1 and
           Q06=0 (Read Station Code), the pre-read checks are made on the
           light detection circuits. Lost data error will be detected, if
           present.

b.   Feed and Punch - When a Feed Request is initiated with Q05=0 and Q06=1 (Punch Station Code), the pre-read and lost data checks are not made. The logic regards this as a Feed Request for punching only. Reading may not be done.

Offset Request (A08=1)

This function directs the Card Reader/Punch to initiate an offset operation. This operation shall cause the existing card to be offset approximately 3/8 inch (column 80 end protruding) from the stacker card deck.

Director functions A09 through A15 are not used.

DIRECTOR STATUS (Q00=1, Q01=0), LEVEL 1

When Q00 is a 1 and Q01 is a 0, and a Read signal is present, Level 1 status information is gated to the computer.

Ready (A00=1)

This bit indicates that a Ready condition exists. The requirements are as follows:

a.   Power supply in operation.

b.   Cards present in input hopper.

c.   Stacker not full.

d.   No jam condition present.

e.   Chip box in place and not full.

f.   Top lid interlock closed.

A Ready ceases to exist when any of the above conditions are not met or when the Card Reader/Punch READY switch is pressed when the Card Reader/Punch is in the Ready Condition.

Busy (A01=1)

This bit indicates that the Card Reader/Punch is busy. The card reader becomes busy when a feed cycle is initiated and remains busy until an End of Operation occurs. The punch becomes busy when a Reply is sent for the first data output and remains busy until a Feed command is issued or an End of Operation occurs.

Interrupt (A02=1)

This bit indicates that an interrupt response was generated by the Card Reader/Punch. The other status bits must be monitored to determine the cause of the interrupt.

Data (A03=1)

This bit indicates that a data transfer may occur.

a. Reader Data - The Reader register contains information ready for transfer to the computer. The status and interrupt will drop upon completion of the transfer.

b. Punch Data - The Punch register is empty and an unpunched column is under the punch head. The status and interrupt will drop upon transfer of data to the Punch register.

End of Operation (A04=1)

This bit indicates that the Card Reader/Punch has completed an operation. This can be either a Read or Punch operation which are described in the Definitions of Conditions and Operations section.

Bit A05 is not used. *see page 6 (alarm?)*

Lost Data (A06=1)

This bit indicates that data was not transferred out of the Read register before the next column of a card being read appeared. The status drops when a clear (A00=1) is sent to the controller.

NOTE

When lost data occurs, no further transfers will occur from that card, and an End of Operation status will be generated.

Protected (A07=1)

This bit indicates that the Protect switch on the Card Reader/Punch is in the PROTECT position. When the switch is in the PROTECT position, the Card Reader/Punch will accept only those instructions having a "1" on the program protect line. All other instructions will be rejected. A protected instruction can be used with either a protected or unprotected Card Reader/Punch.

Error (A08=1)

This bit indicates that either a pre-read or punch error has occurred. Level 2 status may be check to determine which of these two errors, or both, have caused the error status.

Feed Alert (A09=1)

This bit indicates that sometime during a card cycle there was a failure in the transport of the card. This can be caused by:

a. Failure to feed the card.

b. Read area jam.

c. Punch area jam.

d. Stacker area jam.

End of File (A10=1)

This bit indicates that the End of File switch is on and that the End of File condition is present. This allows reading or punching the remaining cards still in the transport after the hopper goes empty.

Chip Box (A11=1)

This bit indicates that the chip box is full or not in position. Emptying the chip box and replacing it will cause the status to drop.

Bits A12 through A15 are not used.

DIRECTOR STATUS (Q00=1, Q01=1 or 0), LEVEL 2

When Q00 and Q01 are 1's, and a Read signal is present, Level 2 status information is gated to the computer.

Hopper Empty (A00=1)

This bit indicates that this status is up while the input feed hopper is out of cards.

Stacker Full (A01=1)

This bit indicates this status is present while the output stacker is filled to capacity.

Fail to Feed (A02=1)

This bit indicates that this status will be present if the Read Ready area fails to contain a card after a feed cycle has occurred, and if the input hopper contains cards.

Read Area Jam (A03=1)

This bit indicates that a card transport failure has occurred in the Read area.

Punch Area Jam (A04=1)

This bit indicates that a card transport failure has occurred in the Punch area.

Stacker Area Jam (A05=1)

This bit indicates that a card transport failure has occurred in the Stacker area.

Pre-read Error (A06=1)

This bit indicates that an amplifier failure in the read head was detected.

Punch Error (A07=1)

This bit indicates that the results of the punch echo check do not agree with the requested punch information.

Manual (A08=1)

This bit indicates that the maintenance panel FEED switch is on, placing the Card Reader/Punch under manual control.

Punch Inhibit (A09=1)

This bit indicates that the PUNCH INHIBIT switch on the control panel is on.

Interlock (A10=1)

This bit indicates that the door interlock switch is de-energized. This occurs when the cabinet doors are open.

Bits A11 through A15 are not used.

MANUAL OPERATION

Switches and Indicators

The switches and indicators shown in Figure 9 are located on the main control panel next to the output stacker. They are described as follows:

POWER Switch and Indicator

Pressing this alternate action switch causes power to be applied to, or removed from, all motors, fans, and power supplies in the proper sequence. The indicator lights to indicate that power is applied to the Card Reader/Punch.

READY Switch and Indicator

Pressing this momentary contact switch causes a card to be fed from the hopper to the Read Ready station if this station is not already holding a card, and if all Not Ready conditions have been resolved satisfactorily. Operation of the switch will also clear the following indications: fail to feed, read alert, and punch alert.

The READY indicator lights if the Card Reader/Punch is ready. When the READY indicator is lighted, pressing and releasing this switch will make the Card Reader/Punch Not Ready and stop any further operations from the computer after the operation in progress is completed.

SINGLE CYCLE Switch

Pressing this momentary contact switch causes a card cycle to occur only if the Card Reader/Punch is in a Not Ready condition. A card cycle occurs regardless of which condition is causing the Not Ready.

NOTE

If the FEED ALERT indicator is lighted, make certain that the card path is clear of possible jam conditions before pressing the SINGLE CYCLE switch.
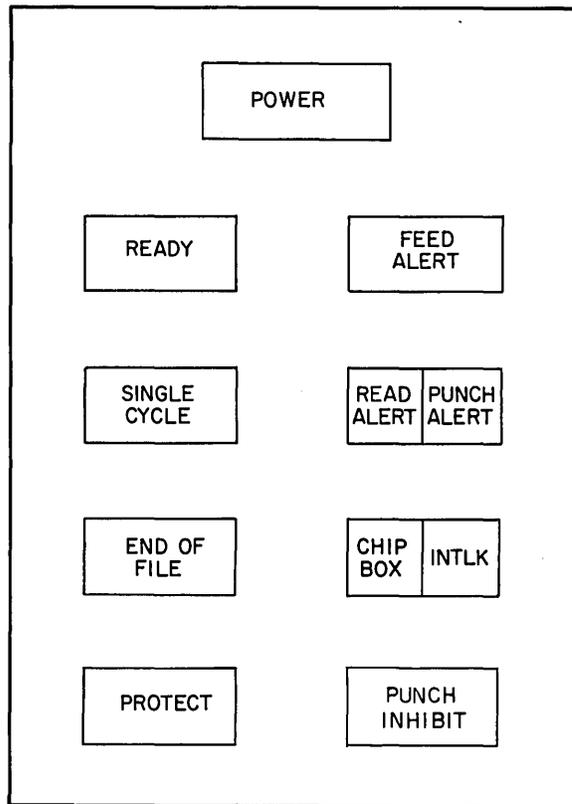
Figure 9. Main Control Panel

END OF FILE Switch and Indicator

Pressing this switch will establish the End of File condition, light the indicator, and generate an End of File status. Pressing the switch again will remove the End of File condition and turn the indicator light off.

The End of File condition allows the Card Reader/Punch to remain Ready after the hopper is empty and there are cards remaining in the transport. This allows reading or punching of the last card in the deck.

PROTECT Switch and Indicator

This alternate action switch, when pressed, places the Card Reader/Punch in the Protected condition, or it can be used to remove the Protected condition. The indicator will be lighted when the Card Reader/Punch is protected. When the switch is on, only protected instructions will be accepted from the computer.

FEED ALERT Indicator

Lights to indicate that sometime during the card cycle there was a failure in the transport of a card. This may be due to:

    a.   Failure to feed the card.

    b.   Read area jam.

c.　Punch area jam.

d.　Stacker area jam.

This indicator can be cleared by pressing the SINGLE CYCLE OR READY switch.

READ ALERT/PUNCH ALERT Indicator

If a Read Alert occurs, the READ ALERT portion of this divided lens indicator lights. If a Punch Alert occurs, the PUNCH ALERT portion lights. Read and Punch Alerts are defined as follows:

a.　Read Alert - The read control logic performs a check on the operational capabilities of the read circuits prior to reading each card. This consists of detecting that all amplifiers are on when the light detection circuits are all uncovered (light check) and of detecting that the amplifiers are all off when the light detection circuits are all covered (dark check). Any error found by these checks will be a pre-read error and it will light the READ ALERT indicator.

b.　Punch Alert - Each punch solenoid has an associated echo amplifier which receives an input from the solenoid each time its respective punch has been active. A check of these signals (echo) is made to determine if the data punched was the same as the data required to be punched. Any error found by this check will be a Punch error and it will light the PUNCH ALERT indicator.

CHIP BOX/INTLK Indicator

If a chip box warning (chip box full, or out of place) occurs, the CHIP BOX portion of this divided lens indicator will light. If the top lid interlock is open, the INTLK portion will light.

PUNCH INHIBIT Switch and Indicator

This alternate action switch inhibits all program-controlled (computer-directed) punching. The indicator will be lighted for the Inhibit condition. This switch does not affect the operation of the switches on the maintenance panel.

Equipment Select Switches

Refer to the Programming section for a description of these switches.

Maintenance Switches

The maintenance switch panel, Figure 10, contains ten switches which allow the Card Reader/Punch to be adjusted and checked off-line. This switch panel is located on the lower right side of the logic chassis.
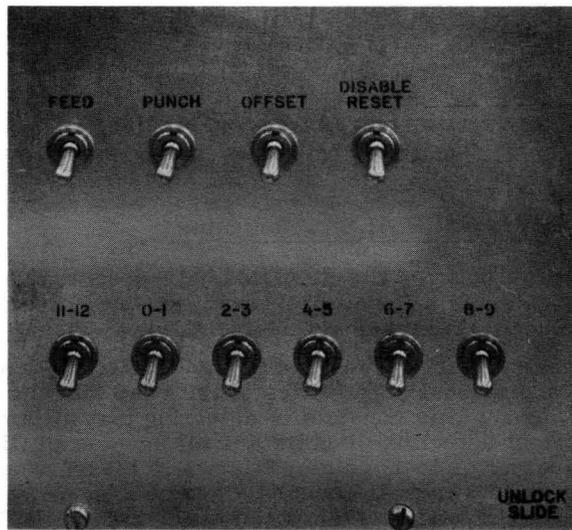
Figure 10. Maintenance Switch Panel

Bit Switches

There are six bit switches on the maintenance panel. Each switch controls the punching of two rows on a card.

FEED Switch

This switch feeds cards at maximum card rate, allowing checks to be made on the reader control logic.

NOTE

The Card Reader/Punch must be ready for the
FEED switch to operate. Therefore, sequence
switches as follows. Set the FEED switch to
separate the Card Reader/Punch from the com-
puter. Use the READY switch on the main con-
trol panel to start and stop feeding of cards.

PUNCH Switch

This toggle switch allows the punching of solid rows of holes on a card. The particular pairs of rows to be punched can be controlled by the bit switches.

NOTE

The FEED switch must be on for the PUNCH switch
to operate.

OFFSET Switch

This switch allows checking the operation of the offset stacker feature.

NOTE

Since the OFFSET switch is not controlled by the
FEED switch, it must be turned off when the Card
Reader/Punch is on-line.

DISABLE RESET Switch

This switch disables the automatic reset feature in the card reader control logic.

NOTE

The FEED switch must be on for this switch to operate.

Operation   Prepare the Card Reader/Punch for operation as follows:

a.   Turn on power by pressing the POWER switch, Figure 9.

b.   Load a deck of cards, face down, with the 9 edge toward the inside of the hopper.

c.   Press the READY switch to single-cycle a card into the Read Ready area.

CONTENTS

FIGURES

TABLES

CONTROL DATA 1729-2 CARD READER SUBSYSTEM

1729-2 CARD READER SUBSYSTEM

INTRODUCTION

The CONTROL DATA® 1729-2 Card Reader Subsystem consists of a reader mechanism, power supply, and controller which contains eight 50-PAKs: five for control and interface and three for operating the Card Reader mechanism. The controller interfaces with one 1700 Data Channel, either normal or buffered. Function codes transmitted via the data channel initiate and control the reading of cards and enable the generation of interrupts when the specified conditions exist. The Card Reader mechanism is a non-buffered, column-oriented, punched card, read device, with no code conversion; it contains a hopper, stacker, and power supply.

FUNCTIONAL DESCRIPTION

System Relationship

The controller may interface with the 17061 Data Channel for buffered communication or the 1705 Data Channel for normal (non-buffered) communication. Typical configurations are shown in Figure 1. The interface logic in the controller provides access to the card reader of the selected equipment. Data is transferred to and from the Card Reader in 16-bit computer words with the lower 12 bits containing the information in one card column (data bit 00 corresponds to card row 9). The Q register in the computer designates the use of the A register bits in the 16-line address cable. Bits of the Q register define the equipment number; and with a Read or Write signal, they define incoming A register bits as function codes, status, or data.
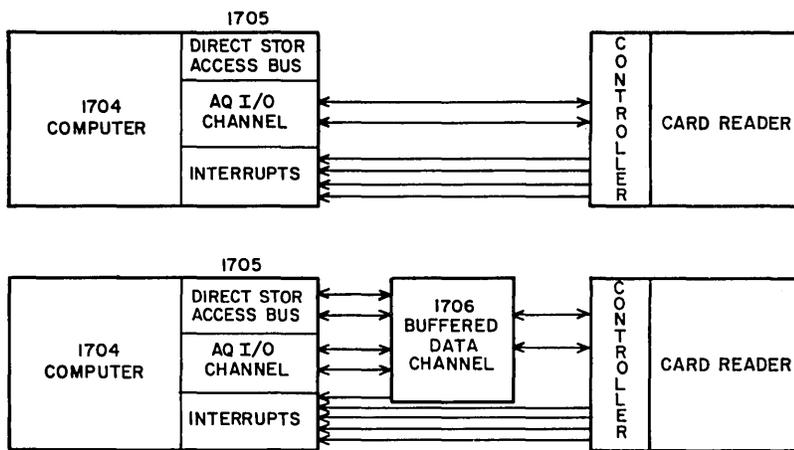
Figure 1. Typical Configurations

Capabilities

The maximum operating rate of the Card Reader is 330 cards per minute. The capacity of the input hopper is 1,200 cards and the capacity of the output stacker is 1,300 cards.

Functional Stations

Refer to Table 1 for a description and to Figure 2 for a diagram of the six functional stations in the Card Reader.

TABLE 1. DESCRIPTION OF FUNCTIONAL STATIONS

STATION NUMBER	STATION	DESCRIPTION
1	Hopper	Holds a supply of cards and feeds them to the read ready station.
2	Ready	Retains each card as it is fed from the hopper.
3	Read	Examines the cards and presents one column of data on the 12 lines to the logic.
4	Post Read	Holds cards from read station prior to routing.
5	Routing	Receives cards as they leave the reader and enables the 3/8 inch offset if directed by the controller.
6	Stacker	Holds the finished card to maintain original card sequence.
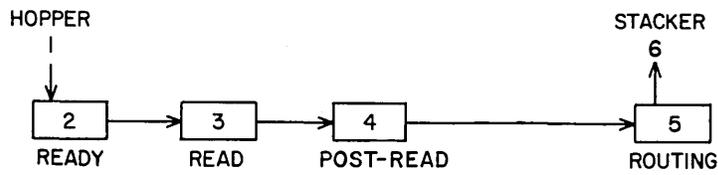
Figure 2. Functional Stations

Timing

Timing intervals for various operations are as follows:

Feed Timing

A card may be fed at intervals of 181 ms for a maximum 330 card-per-minute rate. While operating at this rate, a maximum of 56.5 ms is available after reading card column 80 before the controller need issue its decision to feed the next card.

Read Timing

The read time for card columns 1 through 80 is 86.7 ms. The average time between card columns is 1.08 ms. Column 1 is present for reading approximately 32.6 ms after the initiation of a feed cycle from a static position with the motor running, or 93.5 ms after feed-cycle initiation from a column 80 position.

Offset Timing

A card being read is offset in the stacker if an Offset command is issued any time after reading column 1, and before 15 ms have elapsed of the card cycle in which the card is moving to the routing station.

**Definition of
Conditions and
Operations**

Various conditions and operations in the Card Reader are defined as follows:

Ready

A Ready condition exists when the Card Reader is capable of performing all its functions. Pressing the READY switch causes the equipment to become ready if the power supply is in operation, cards are in the input hopper, the stacker is not full, there is no jam condition, and the top lid interlock is closed.

A Ready ceases to exist when any of the above conditions are not met or when the READY switch is pressed when the Card Reader is in the Ready state.

Reader Busy

The reader becomes busy when a feed cycle is initiated; it remains busy until the completion of a card (81st column time), or until lost data occurs.

NOTE

If the Read operation is terminated before the 81st column time, with a Feed, no End-of-Operation status or interrupt is issued.

Read Operation

A Read operation is in effect between the acceptance of a Feed command to station 1, and the completion of a card (81st column time) or the time lost data occurred.

Alarm

An alarm indicates the presence of an abnormal condition. Two types of abnormal conditions can occur: those which require the Card Reader to go Not Ready and require operator intervention and those which allow the Ready status to remain and do not require operator intervention.

Alarm with Not Ready

This alarm occurs when the Card Reader is affected by a Not Ready condition: hopper empty, stacker full, feed alert, or open interlock on the top lid. The alarm is cleared upon correction of the cause for the Not Ready condition.

Alarm with Ready

This Alarm condition is caused by lost data or a read alert. The alarm is cleared by a Master Clear or a Clear Card Reader director function code.

Error Indications

Not Ready
_____

The absence of any one of the following Ready conditions results in a Not Ready error condition.

    a.   Power supply in operation.

    b.   Cards in the input hopper.

    c.   Card stacker not full.

    d.   No card jam condition.

    e.   Top lid interlock closed.

Pre-read error
_____

This error occurs if all read amplifiers are not on during a light check, or if the amplifiers are not off during a dark check.

Alarm
_____

The presence of any abnormal condition results in an Alarm error. An alarm can cause the equipment to go Not Ready or it can exist and allow the Ready state to remain. Conditions causing a Not Ready are:

    a.   Hopper empty.

    b.   Stacker full.

    c.   FEED ALERT indicator lit.

    d.   Open top lid interlock.

Conditions allowing the Ready state to remain are:

    a.   Lost data.

    b.   READ ALERT indicator lit.

Feed Alert
_____

This error occurs when there has been a failure in the transport of a card which may be due to a card failing to feed, or a jam occurring in the read, post read, or stacker area.

PROGRAMMING   Table 2 and Figures 3 through 8 provide programming information. A description of the codes follows the figures.

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TABLE 2. SUMMARY OF Q REGISTER FUNCTIONS

Q REGISTER		DESCRIPTION
FORMAT	SYMBOL	
CONVERTER CODE	(W)	W =0 must be present for all Card Reader operations.
EQUIPMENT CODE	(E)	Set Equipment Select Switches - positions 0 thru F (an Equipment Code setting must be present for all operations).
STATION CODE	(S)	Select station (Q05, Q06). For Status and data, Q05 must be a 1 and Q06 must be a 0 with a Read signal. For functions, Q05 must be a 1 and Q06 must be a 0 with a Write signal.

DIRECTOR CODE	(D)	Defines operation (Q00, Q01). For data, Q00 = 0 with a Read signal.
		For functions, Q00 = 1 with a Write signal.
		For status, Q00 = 1, Q01 = 0 with a Read signal.
		    Level 1, Q01 = 0
		    Level 2, Q01 = 1

Q REGISTER

E (EQUIP CODE) = Q07-Q10 = ANY ONE OF SWITCH NUMBERS 0 - F
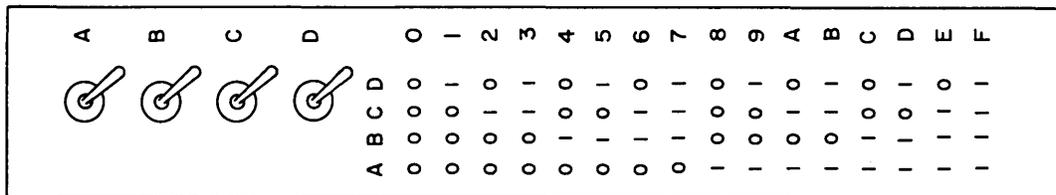
Figure 3. Equipment Select Switches
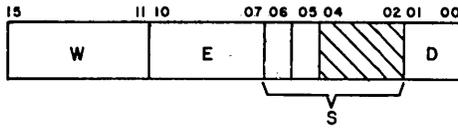
Figure 4. Q Register Format
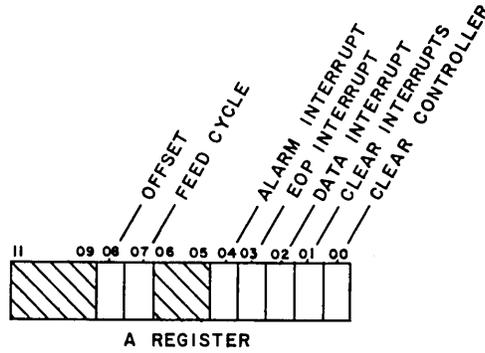
Figure 5. Function Code Format
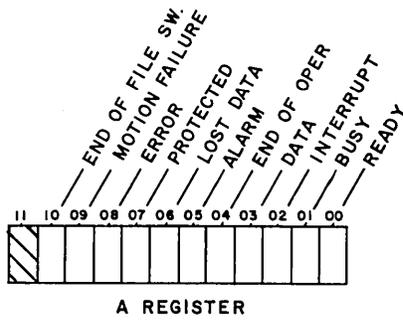
Figure 6. Status Code Format - Level 1
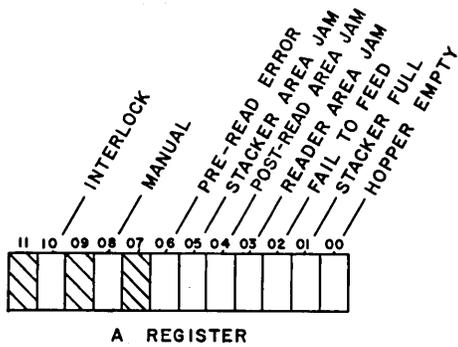
Figure 7. Status Code Format - Level 2
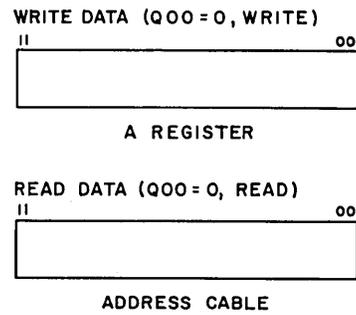
Figure 8. Data Transfer Format

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CODES

Converter

The W portion of the Q register (Q11-Q15) must be all 0's for all Card Reader operations.

Equipment

The E portion of the Q register (Q07-Q10) defines the Card Reader equipment code. The code is set up by the switches shown in Figure 3. If the switch settings match bits 07-10 of Q, the equipment responds.

Command

When accompanied by an equipment code and either a Read or Write signal, a command code defines the operation to be performed. The command code consists of a station (S) code and a director (D) code. Bit 05 of the S code and the D portion of Q (Q00 and Q01) define the word being sent as data, or director function or status codes.

DATA TRANSFER

Read Data (Q00 = 0, Q01 = 0, Q05 = 1)

When bits Q00 and Q01 are 0, and Q05 = 1, the 16 lines of the data cable (A) are directed to perform a data transfer as specified by the Read signal. A Reject occurs if there is no data to be transferred. The Card Reader rejects when:

    a.   The Card Reader is not ready.

    b.   The computer attempts to input data at a rate that exceeds the capabilities of the Card Reader.

    c.   The 80th column is read, or a feed command is accepted and a new card is not registered in the read station.

DIRECTOR FUNCTIONS (Q00 = 1, Q01 = 0, Q05 = 1)

When Q00 and Q05 are 1's, and Q01 is a 0, and they are accompanied by an equipment code and a Write signal, the 16 lines of the data cable (A) direct the Card Reader to perform the following operations. Director functions may be stacked (i.e., two or more functions sent simultaneously).

NOTE

The Card Reader executes and replies to the Clear function if it is Not Ready, provided that no other director bit (except A01) is transmitted with it (bits A02 through A08 must be zero). Care should be exercised in using this function while the Card Reader is busy.

Clear Card Reader (A00 = 1)

This function directs the clearing of all interrupt requests and responses, motion requests, errors, and other logic which may be cleared. This bit is subordinate to bits A02 through A08.

The Card Reader will execute and reply to the Clear
Interrupts function if it is Not Ready, provided that
no other director bit (except A00) is transmitted with
it (bits A02 through A08 must be zero).

Clear Interrupts (A01 = 1)

This function directs that all interrupt requests and their responses be
cleared; it is subordinate to the interrupt request bits A02 through A04.

Data Interrupt Request (A02 = 1)

This function sets the Data Interrupt Request FF which causes an interrupt
to be generated when information is available. The interrupt is cleared by
a reply to a data transfer. The interrupt request and response is cleared
by bit A00 or A01. Interrupt Request takes precedence over function clears.

Interrupt on End of Operation (A03 = 1)

The purpose of this interrupt is to notify the computer that the unit is
finished with an operation or that some condition existed at the end of the
last data transfer which prevents any further data transfers. The Interrupt
Request and Response is cleared by bit A00 or A01. Interrupt Request
takes precedence over function clears.

The interrupt may be selected before or during the operation. An interrupt
response does not occur for an operation which terminated before the se-
lection was made.

Alarm Interrupt Request (A04 = 1)

This function enables the generation of an interrupt when an Alarm condition
exists. These conditions are listed in the Alarm section. An Alarm
condition that exists at the time of the interrupt request immediately provides
a response; if the Alarm condition does not exist at the time of the interrupt
request, the interrupt response is provided as soon as the Alarm condition
is detected.

The Alarm Interrupt Request function is cleared by a Master Clear or when
A00 = 1, or A01 = 1 with A04 = 0.

The interrupt response is cleared by a Master Clear or when A00 = 1 or
A01 = 1. When the interrupt response is cleared by Director Function
A00 = 1 or A01 = 1, the interrupt request may be reset with the same
operation if A04 = 1.

Director functions A05 and A06 are not used.

Feed Request (A07 = 1)

This function directs the Card Reader to initiate a feed cycle and to advance
the next card.

- Feed and Read - When a Feed Request is initiated, pre-read
  checks are made on the light detection circuits and lost data is
  detected (if present).

Offset Request (A08 = 1)

This function directs the Card Reader to initiate an Offset operation which causes the existing card to be offset approximately 3/8 inch (column 80 end protruding) from the stacker card deck.

Director functions A09 through A15 are not used.

DIRECTOR STATUS (Q00 =1, Q01 = 0), LEVEL 1

When Q00 is a 1 and Q01 is a 0, and a Read signal is present, the computer is requesting Level 1 status.

Ready (A00 = 1)

This bit indicates that a Ready condition exists. The requirements are as follows:

    a.   Power supply in operation.

    b.   Cards present in input hopper.

    c.   Stacker not full.

    d.   No jam condition present.

    e.   Top lid interlock closed.

A Ready ceases to exist when any of the above conditions are not met or when the Card Reader READY switch is pressed when the Card Reader is in the Ready state.

Busy (A01 = 1)

This bit indicates that the Card Reader is busy. The Card Reader becomes busy when a feed cycle is initiated and remains busy until an End of Operation occurs.

Interrupt (A02 = 1)

This bit indicates that an interrupt response was generated by the Card Reader. The other status bits must be monitored to determine the cause of the interrupt.

Data (A03 = 1)

This bit indicates that a data transfer may occur.

- Reader Data - The Reader register contains information ready for transfer to the computer. The status and interrupt drop upon completion of the transfer.

End of Operation (A04 = 1)

This bit indicates that the Card Reader completed an operation.

Alarm (A05 = 1)

This bit indicates the presence of an alarm condition.

NOTE

When lost data occurs, no further transfers occur from
that card, and an End-of-Operation status is generated.

Lost Data (A06 = 1)

This bit indicates that data was not transferred out of the Read register
before the next column of a card being read appeared. The status drops
when a clear (A00 = 1) is sent to the controller.

Protected (A07 = 1)

This bit indicates that the PROTECT switch on the Card Reader is in the
Protect position. When the switch is in the Protect position, the Card
Reader accepts only those instructions having "1" on the Program Protect
line. All other instructions are rejected. A protected instruction can be
used with either a protected or unprotected Card Reader.

Error (A08 =1)

This bit indicates that a pre-read error has occurred.

Feed Alert (A09 = 1)

This bit indicates that sometime during a card cycle there was a failure
in the transport of the card. This can be caused by:

    a.   Failure to feed the card.

    b.   Read area jam.

    c.   Post-Read area jam.

    d.   Stacker area jam.

End of File (A10 = 1)

This bit indicates that the END OF FILE switch is on and that the End of
File condition is present. This allows reading the remaining cards in the
transport after the hopper is empty.

Bits A11 through A15 are not used.

DIRECTOR STATUS (Q00 = 1, Q01 = 1), LEVEL 2

When Q00 and Q01 are 1's, and a Read signal is present, the computer is
requesting Level 2 status.

Hopper Empty (A00 = 1)

This bit indicates this status is present while the input hopper is out of
cards.

Stacker Full (A01 = 1)

This bit indicates this status is present while the output stacker is filled to capacity.

Fail to Feed (A02 = 1)

This bit indicates this status is present if the Ready area fails to contain a card after a feed cycle occurred, and if the input hopper contains cards.

Read Area Jam (A03 = 1)

This bit indicates that a card transport failure occurred in the Read area.

Post Read Area Jam (A04 = 1)

This bit indicates that a card transport failure occurred when the card left the Read area.

Stacker Area Jam (A05 = 1)

This bit indicates that a card transport failure occurred in the Stacker area.

Pre-Read Error (A06 = 1)

This bit indicates than an amplifier failure in the read-head was detected.

Bit A07 is not used.

Manual (A08 = 1)

This bit indicates that the maintenance panel FEED switch is on, placing the Card Reader under manual control.

Bit A09 is not used.

Interlock (A10 = 1)

This bit indicates the door interlock switch is de-energized. This occurs when the cabinet doors are open.

Bits A11 through A15 are not used.

MANUAL OPERATION

Switches and Indicators

The switches and indicators shown in Figure 9 are located on the main control panel next to the output stacker. They are described as follows:

POWER Switch and Indicator

Pressing this alternate action switch causes power to be applied to or removed from all motors, fans, and power supplies in the proper sequence. The indicator lights to indicate that power is applied to the Card Reader.

READY Switch and Indicator

Pressing this momentary contact switch causes a card to be fed from the hopper to the Ready station if this station is not already holding a card, and if all Not Ready conditions are resolved satisfactorily. Operation of the switch also clears the following indications: fail to feed and read alert.

The READY indicator lights if the Card Reader is ready. When the READY indicator lights, pressing and releasing this switch makes the Card Reader Not Ready and stops any further operations from the computer after the operation in progress is completed.

CAUTION

If the FEED ALERT indicator is lit, make certain the card path is clear of possible jam conditions before pressing the SINGLE CYCLE switch.

SINGLE CYCLE Switch

Pressing this monentary contact switch causes a card cycle to occur only if the Card Reader is in a Not Ready condition. A card cycle occurs regardless of which condition is causing the Not Ready.
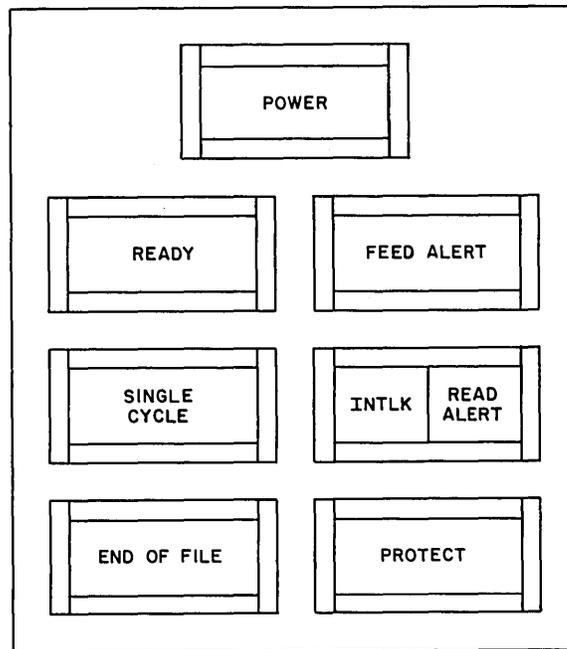
Figure 9. Main Control Panel

END OF FILE Switch and Indicator

Pressing this switch establishes the End of File condition, lights the indicator, and generates an End of File status. Pressing the switch again removes the End of File condition and turns the indicator light off.

The End of File condition allows the Card Reader to remain Ready after the hopper is empty and there are cards remaining in the transport. This allows the last card in the deck to be read.

FEED ALERT Indicator

This indicator lights to indicate that sometime during the card cycle there was a failure in the transport of a card. This may be due to:

    a. Failure to feed the card.

    b. Read area jam.

    c. Post-Read area jam.

    d. Stacker area jam.

This indicator is cleared by pressing the SINGLE CYCLE or READY switch.

READ ALERT Indicator

If a Read Alert occurs, the READ ALERT indicator lights.

- Read Alert - The read control logic performs a check on the operational capabilities of the read interrogation and amplifier circuits prior to reading each card. This consists of detecting that all amplifiers are on when the light detection circuits are all uncovered (light check) and of detecting that the amplifiers are all off when the light detection circuits are all covered (dark check). Any error found by these checks is a pre-read error and lights the READ ALERT indicator.

INTLK Indicator

If the top lid interlock is open, the INTLK indicator lights.

PROTECT Switch and Indicator

This alternate action switch (when pressed) places the Card Reader in the Protected condition, or it can be used to remove the Protected condition. The indicator lights when the Card Reader is protected. When the switch is on, only protected instructions are accepted from the computer.

**Equipment
Select Switches**

Refer to the Programming section for a description of these switches.

**Maintenance
Switches**

The maintenance switch panel (Figure 10) contains three switches which allow the Card Reader to be adjusted and checked off-line. This switch panel is located on the lower right side of the logic chassis.
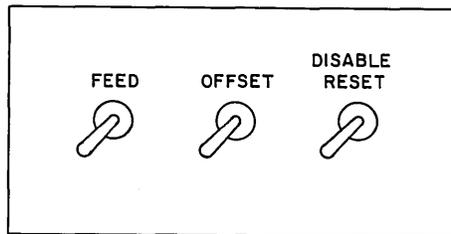

Figure 10. Maintenance Switch Panel

NOTE

The Card Reader must be ready for the FEED switch to operate; therefore, sequence switches as follows: Set the FEED switch to separate the Card Reader from the computer. Use the READY switch on the main control panel to start and stop the feeding of cards.

FEED Switch

This switch feeds cards at a maximum card rate, allowing checks to be made on the reader control logic.

NOTE

Since the OFFSET switch is not controlled by the FEED switch, it must be turned off when the Card Reader is on-line.

OFFSET Switch

This switch allows checking the operation of the offset stacker feature.

NOTE

The FEED switch must be on for the DISABLE RESET switch to operate.

DISABLE RESET Switch

This switch disables the automatic reset feature in the card reader control logic.

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Operation   Prepare the Card Reader for operation as follows:

a.   Turn on power by pressing the POWER switch, Figure 9.

b.   Load a deck of cards, face down, with the 9 edge toward the inside
     of the hopper.

c.   Press the READY switch to single-cycle a card into the
     Ready area.

CONTENTS

FIGURES

TABLES

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CONTROL DATA 405 CARD READER WITH 1726 CARD READER CONTROLLER

2685

1726 CARD READER CONTROLLER

INTRODUCTION

The CONTROL DATA® 1726 Card Reader Controller operates with a CONTROL DATA® 405 Card Reader to transfer punched card information to the 1704 Computer. The controller is mounted inside the card reader on chassis 1 and 2. Chassis 1, located in the front of the card reader, contains the controller memory, its associated logic, and some control logic. Chassis 2, located in the rear of the card reader, contains channel control logic and the controller switches.

The rates and capacities of the card reader are as follows:

Reading rate — 1200 80-column cards/minute
1600 51-column cards/minute

Card capacity — Input tray, 4000 cards
Primary output tray, 4000 cards
Secondary output tray, 240 cards

Data transfer rate — 384 microseconds for an 80-column card
245 microseconds for a 51-column card

**FUNCTIONAL
DESCRIPTION**

System Relationship

The controller interfaces the card reader directly to the AQ channel of the 1705 Interrupt/Data Channel for unbuffered communication or to the 1706 Buffered Data Channel (BDC) for buffered communication. The 1706 BDC provides direct access to storage in the 1704 Computer. The 1716 Coupling Data Channel may be used in applications involving two computers and several peripheral units. Some typical configurations are shown in Figure 1. The controller is a single-channel device which transfers data read from punched cards to the computer. The controller receives and interprets function codes sent by program control via the data channel. The function codes initiate and control card reading, gate status information, and enable interrupts when certain conditions exist.
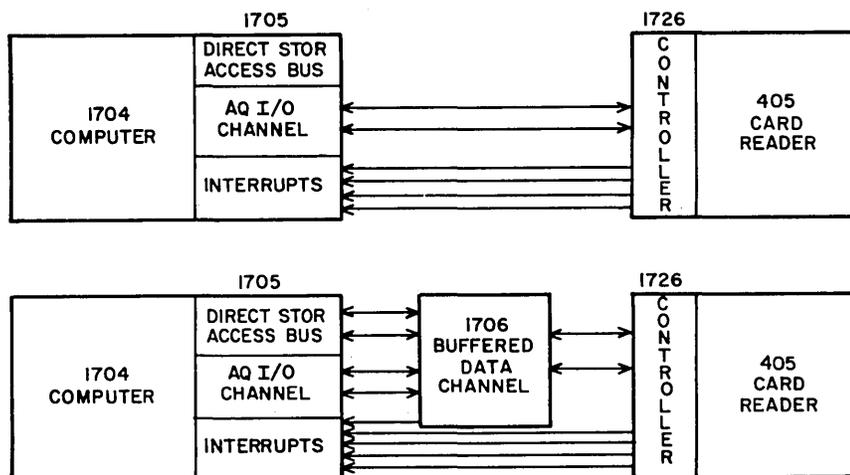
Figure 1. Typical Configuration

Card Format

A punched card contains 51 or 80 12-bit columns, and a punch in any bit position is a "1". Cards may be in either Hollerith or binary format. In Hollerith format, each column contains a combination of punches that specifies one alphanumeric character. In binary format, each card column is a 12-bit binary quantity. Refer to Table 1 for a listing of Hollerith and ASCII card codes.

TABLE 1. HOLLERITH TO ASCII CODE CONVERSIONS

HOLLERITH CODE (PUNCH)	BCD CODE	ASCII CODE (HEX)	ASCII CODE CHARACTER
No Punch	60	20	Space
11-8-2 or 11,0	52	21	!
8-7	17	22	"
12-8-7	37	23	#
11-8-3	53	24	$
0-8-5	75	25	%
8-2	12	26	&
8-4	14	27	'
0-8-4	74	28	(
12-8-4	34	29	)
11-8-4	54	2A	*
12	20	2B	+
0-8-3	73	2C	,
11	40	2D	-
12-8-3	33	2E	.
0-1	61	2F	/
0	00	30	0
1	01	31	1
2	02	32	2
3	03	33	3
4	04	34	4
5	05	35	5
6	06	36	6
7	07	37	7
8	10	38	8
9	11	39	9
8-5	15	3A	:

TABLE 1. HOLLERITH TO ASCII CODE CONVERSIONS (Cont'd)

HOLLERITH CODE (PUNCH)	BCD CODE	ASCII CODE (HEX)	ASCII CODE CHARACTER
11-8-6	56	3B	;
12-8-6	36	3C	<
8-3	12	3D	=
8-6	16	3E	>
12-8-2 or 12,0	32	3F	?
0-8-7	77	40	@
12-1	21	41	A
12-2	22	42	B
12-3	23	43	C
12-4	24	44	D
12-5	25	45	E
12-6	26	46	F
12-7	27	47	G
12-8	30	48	H
12-9	31	49	I
11-1	41	4A	J
11-2	42	4B	K
11-3	43	4C	L
11-4	44	4D	M
11-5	45	4E	N
11-6	46	4F	O
11-7	47	50	P
11-8	50	51	Q
11-9	51	52	R
0-2	62	53	S
0-3	63	54	T
0-4	64	55	U
0-5	65	56	V
0-6	66	57	W
0-7	67	58	X
0-8	70	59	Y
0-9	71	5A	Z
12-8-5	35	5B	[
0-8-2	72	5C	\
11-8-5	55	5D	]
11-7-8	57	5E	†
0-8-6	76	5F	←

Memory Timing

Forty milliseconds are required to advance the first card. If it is not the first card of a new deck, 20 ms are required to advance the card from a stopped position to reading the first column.

The time required to load an 80-column card into the memory is approximately 32 ms, or 400 μsec per column. For a 51-column card, load memory time is approximately 20.4 ms.

After the data from a card has been entered into memory, the memory must be unloaded within 1.5 ms or card motion stops. To gate this card into the secondary stacker, a Gate Card function must be executed. Unloading the memory requires a minimum of 384 μsec for an 80-column card and 245 μsec for a 51-column card.

Read Sequence

The read head assembly consists of two banks of 12 photo diodes which are used for sensing the information holes. The two banks are spaced one card column distance apart. Column one is first read by the primary station

and stored. Four hundred microseconds later column one is read at the second read station and compared to the reading at the first station. Each column on the card is checked in this manner, and any error in reading is transmitted to the computer via the alarm and error status lines.

Cards are routed to the primary stacker unless specifically gated to the secondary stacker. The original sequence and orientation of the card deck is maintained. Cards may be directed to the secondary stacker by a Gate Card function which must be issued for each card.

Before reading each card, the primary read station is checked for light and dark conditions. This check is accomplished by first checking that all the primary read photo diodes are active before the card enters the read station. Then the diodes are checked to ensure that they are inactive when they are covered by the leading edge of the card. Any error occuring during this check is also transmitted to the computer via the alarm and error status lines.

Alarm

An alarm indicates the presence of an abnormal condition which causes the card reader to become Not Ready and which requires operator intervention. These conditions are Compare or Pre-read error, stacker full or jammed, input tray empty, feed failure, or if the AUTO/MAN switch is in the MAN position. The reading of a separator card from buffer memory provides an Alarm status, but does not cause the card reader to become Not Ready.

Program Protection

When the PROTECTED/UNPROTECTED switch on the controller logic chassis is in the PROTECTED position, only those I/O instructions having a "1" on the protect line are recognized. When the switch is in the UNPROTECTED position, both protected and unprotected instructions are recognized.

Data Code Conversion

When reading a Hollerith Card (rows 7 and 9 in column 1 not punched) in the Hollerith to ASCII mode, the 16-bit computer word contains two 7-bit ASCII codes with bit positions 7 and 15 containing zeros. Each card column is converted to one 7-bit ASCII code. When reading a Hollerith card with Negate Hollerith to ASCII selected, or when reading a binary card (rows 7 and 9 punched in column 1), the 16-bit computer word consists of one card column in the lower 12 bit positions with the upper 4 bit positions containing zeros.

Cards are placed in the reader (face in) with the first column forward. All information on the card is read twice and checked. The information may be transferred to the computer as read or, in the case of Hollerith coded cards, converted to ASCII. In converting Hollerith codes to ASCII codes, correct translation is ensured only for the 64 characters represented by BCD codes. If less than a full card of information is required, a Reload Memory function may be executed after inputting less than a card of information.

PROGRAMMING

Programming Summary

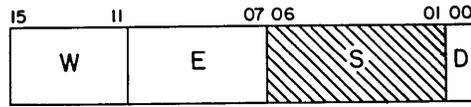Figures 2 through 5 provide programming information. A description of the formats follows the figures.
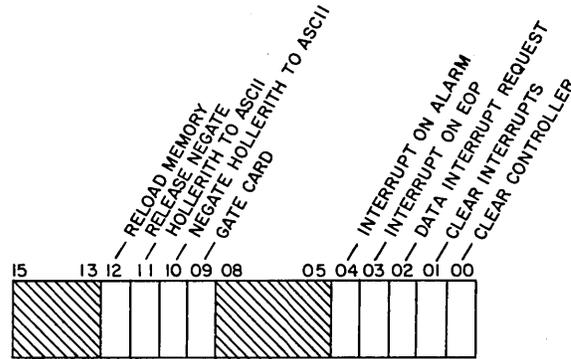
Figure 2. Q Register Format
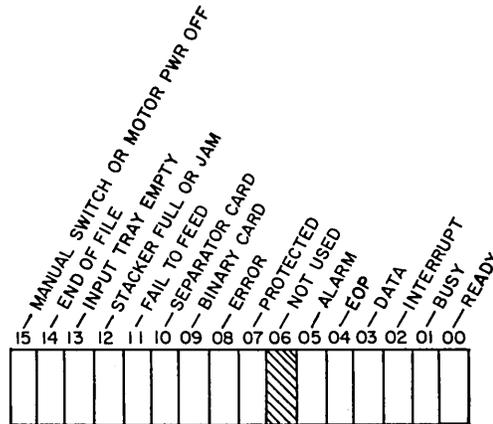

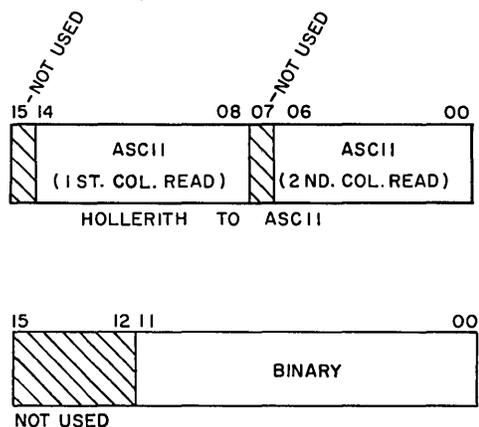Figure 3. Function Code Format

Figure 4. Status Code Format

Figure 5. Data Word Format
(A Register - Data Cable)

Programming Considerations

The Programmer should make certain that the desired function, either Negate Hollerith to ASCII or Release Negate Hollerith to ASCII, has been executed prior to the initiation of a card read. Failure to do this will cause the cards to be read under whatever mode was previously selected.

CODES

Converter

The W portion of the Q register (Q11-Q15) in Figure 2 must be all zeros for all card reader operations.

Equipment

The E portion of the Q register (Q07-Q10) defines the card reader equipment code. The code is set up by the rotary switch shown in Figure 6. If the switch setting matches bits 07-10 of Q, the equipment responds.

Command

When accompanied by an equipment code and either a Read or Write signal, a command code defines the operation to be performed. The command code consists of a station (S) code and a director (D) code. The S code is not used. The D portion of the command code consists of bit Q00 only which, together with a Read or Write signal, defines the word being set as director function, director status, or data transfer codes.

DIRECTOR FUNCTIONS

When bit Q00 is a "1" and a Write signal is present, the 16 lines of data cable (A) direct the card reader to perform the following operations. Director functions may be stacked (two or more functions sent simultaneously).

Clear Controller (A00 = 1)

This bit directs the clearing of all interrupt requests, motion requests, errors, and other logic which may be cleared. Care should be exercised in using this function while the controller is Busy. This bit is subordinate to bits A02 through A04 and bits A09 through A12.

Clear Interrupts (A01 = 1)

This bit directs that all interrupt requests and their responses be cleared. This bit is subordinate to the interrupt request bits A02 through A04.

Data Interrupt Request (A02 = 1)

This bit directs the Data Interrupt request to be set which causes an interrupt to be generated when an information transfer may occur. The interrupt is cleared by a Reply to a data transfer. Interrupt request or response is cleared by A00 or A01 unless bit A02 is a "1".

Interrupt on End of Operation (A03 = 1)

This bit directs an End of Operation Interrupt request to be set which causes an interrupt to be sent to the computer when the last card column has been read from memory or a Reload Memory function is performed. The interrupt request or response is cleared by A00 or A01. Request bit A03 takes precedence over bits A00 or A01.

Interrupt on Alarm (A04 = 1)

This bit directs an Alarm Interrupt request to be set which causes an interrupt when any of the conditions listed occurs. The interrupt request is cleared by bits A00 or A01. The interrupt request takes precedence over function clears.

The Alarm interrupt may indicate any of the following conditions, each determinable by status check:

1. Compare or Pre-read error
2. Stacker full or jam
3. Input tray empty
4. Fail to feed
5. Separator card is read into computer memory.
6. AUTO/MAN switch is in the MAN position.

Director function bits A05 through A08 are not used.

Gate Card (A09 = 1)

This bit gates the card being read to the secondary stacker. This function must be performed during the 1.5 ms following the input of the last card column to the buffer memory.

Negate Hollerith to ASCII (A10 = 1)

When bit A10 is selected, 7 and 9 punch positions in column 1 are ignored and all information (binary or Hollerith) is read as binary. Bit A10 is subordinate to bit A11. Bit A10 is rejected if the controller is Busy.

NOTE

Before beginning a new operation, make certain that bit A10 and the following bit, A11, are appropriately selected. If this is not done, the cards will be read in the mode or state that the card reader was in during the previous operation.

Release Negate Hollerith to ASCII (A11 = 1)

When bit A11 is selected, the 7 and 9 punch positions in column 1 determine whether the card information is to be transferred in ASCII code or in binary form. The Release Negate Hollerith to ASCII function takes precedence over the select Negate Hollerith to ASCII function, and it is rejected if the controller is Busy. See Note.

Reload Memory (A12 = 1)

This bit directs the controller to initiate a card feed thereby reloading the controller memory with the data from the next card in the card reader. The data that has not been transmitted from the memory to the computer is lost when Reload Memory is executed. A Reload Memory is required only if less than a full card of information is desired. Bit A12 is rejected if the controller is Busy.

Director function bits A13 through A15 are not used.

DIRECTOR STATUS

When Q00 is a "1" and a Read signal is present, the computer is requesting status.

Ready (A00 = 1)

The presence of this bit indicates that the card reader is ready for operation.

Busy (A01 = 1)

The controller is Busy whenever a card is being entered into the buffer memory.

Interrupt (A02 = 1)

The interrupt status is available if one or more of the selected interrupts has occurred. Other bits must be monitored to determine the condition causing the interrupt.

Data (A03 = 1)

This status bit indicates that data is ready to be transferred to the computer.

End of Operation (A04 = 1)

This status bit indicates that the last card column has been read from the buffer memory, or a Reload Memory function has been sent. This bit remains a "1" until a Reply signal is sent, or a Clear Controller function or Master Clear is issued.

Alarm (A05 = 1)

The bit remains a "1" until whatever caused the Alarm condition is removed. This status bit indicates that one or more of the following conditions has occurred:

1.   Compare or Pre-read error
2.   Stacker full or jam
3.   Input tray empty
4.   Fail to feed
5.   A separator card has been transferred to the computer memory.
6.   The AUTO/MAN switch is in the MAN position.

Status bit A06 is not used.

Protected (A07 = 1)

This status bit indicates that the controller recognizes only the I/O instructions that have the protect bit present.   This status bit is a "1" when the PROTECTED/UNPROTECTED switch is in the PROTECTED position.

Error (A08 = 1)

This bit indicates that a Pre-read or Compare error has occurred.

Binary Card (A09 = 1)

This bit is present when the contents of the first card column have been transferred to the computer memory and a binary card (rows 7 and 9 punched in first column) was detected, or the Negate Hollerith to ASCII function was selected.   This bit remains a "1" until a Clear Controller or Master Clear function is issued, or a Reply is sent when a card is read under the following conditions:

1.   The card is not a binary or a separator card.
2.   The Release Negate Hollerith to ASCII function is selected.

Separator Card (A10 = 1)

This bit is present when the contents of the first card column have been transferred to computer memory and a separator card (rows 6, 7, 8, and 9 punched in first column) was detected.   This bit remains a "1" until a Reply is sent when a card is read that is not a separator card, or until a Master Clear or Clear Controller function is executed.

Fail to Feed (A11 = 1)

This bit is a "1" if another card is not detected at the primary read station 500 ms after the previous card has cleared the secondary read station.

Stacker Full or Jam (A12 = 1)

This bit is a "1" when the stacker is full of cards or when the cards have jammed.

Input Tray Empty (A13 = 1)

This bit is a "1" when the input tray is empty.

<u>End of File (A14 = 1)</u>

This status bit becomes a "1" when the input tray is empty, the buffer memory is unloaded, and the END OF FILE switch is on. When the input tray does not contain the last card of a file, the switch should be off to inhibit this status bit.

<u>Manual (A15 = 1)</u>

This status bit is a "1" when the AUTO/MAN switch is in the MAN position or the MOTOR POWER switch is off.

DATA TRANSFER

When bit Q00 is a "0" and a Read or Write signal is present, the 16 lines of the data cable (A) are directed to perform a data transfer. Data transfers are terminated by sending either a Reply or Reject signal which drops either the Read or Write signal. This in turn drops the Reply or Reject. A Reject occurs if the data cannot be transferred.

<u>Write Data</u>

A reject will be returned to terminate all Write Data requests since this is a read only device.

<u>Read Data</u>

If the controller has data ready for transfer to the computer at the time a Read Data request is recognized, a Reply is returned which sequentially initiates the transfer. If no data is available when a Read Data request is recognized, a Reject is returned which sequentially terminates the transfer.

MANUAL OPERATION

Controller Switches

<u>Equipment Select Switch</u>

This 16-position rotary switch (0-F hexadecimal) is used to set up the controller equipment code. If the switch setting matches bits 07-10 of the Q register, the equipment responds. It is located on chassis 2 in the rear of the card reader. Refer to Figure 6.

<u>PROTECTED/UNPROTECTED Switch</u>

When in the PROTECTED position, this chassis 2 toggle switch causes the controller to recognize only protected instructions. If the switch is in the UNPROTECTED position, the controller recognizes all instructions. Refer to Figure 6.

Card Reader Switches and Indicators

All operator switches on the top panel of the card reader are alternate action, i.e., press to turn on, press again to turn off. A self-contained indicator lights when the switch is on. Refer to Figure 7.

MAIN POWER Switch/Indicator

This switch is the master power control for the card reader and the controller. It controls the power supplies, cooling fans, and logic.

MOTOR POWER Switch/Indicator

This switch controls power to the drive motors, vacuum pump, compressor, and hopper-stacker vibrators.

AUTO/MAN Switch/Indicator

This 2-position switch selects manual or program-controlled modes of operation. Changing the switch position to MAN drops the Ready status bit. This switch must be in the AUTO position when the card reader is used for a computer input operation.
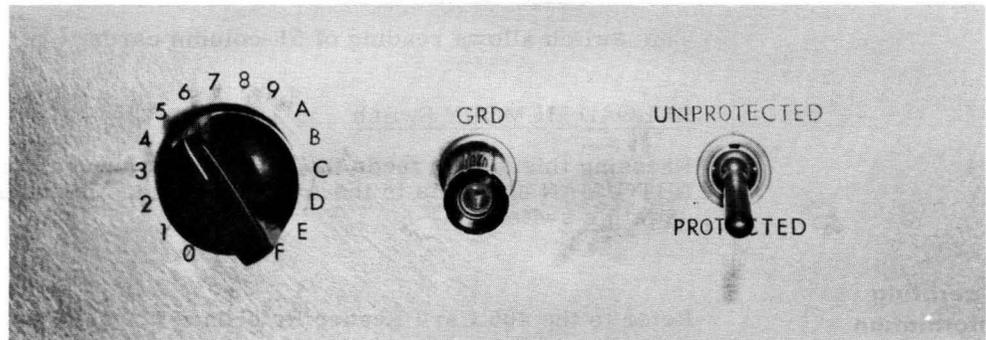
Figure 6. Controller Switches
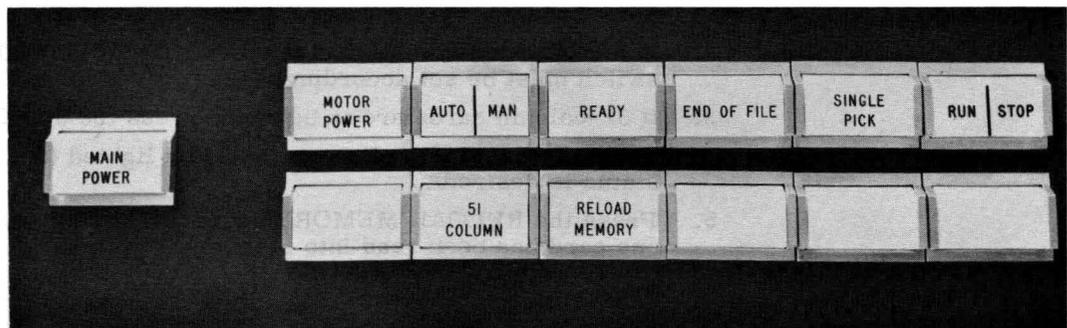
Figure 7. Card Reader Switches/Indicators

READY Switch/Indicator

This switch causes the card reader to become Ready if:

1. The input tray is not empty.
2. The primary and secondary stackers are not full.
3. No error conditions exist in the unit.

END OF FILE Switch/Indicator

This switch enables the controller to generate an End of File status bit after the last card in the input tray is read.

SINGLE PICK Switch

This switch allows a single card to be cycled through the card reader when the AUTO/MAN switch is in the MAN position. There is no indicator associated with this switch.

RUN/STOP Switch/Indicator

This switch allows manual control of card feed when the AUTO/MAN switch is in the MAN position.

51 COLUMN Switch/Indicator

This switch allows reading of 51-column cards.

RELOAD MEMORY Switch

Pressing this switch feeds the data from a new card into memory when the AUTO/MAN switch is in the AUTO position. There is no indicator associated with this switch.

Operating Information

Refer to the 405 Card Reader Reference Manual (Mod A, B, and D) for operation of the card reader. After applying power, be sure that the following controller related switches are set as follows:

1. The Equipment Select switch must be set to match the equipment specified by program control (bits 07 - 10 of Q).

2. If any instructions are protected, the PROTECTED/UNPROTECTED switch must be set accordingly.

3. If 51-column cards are to be read, press the 51 COLUMN switch.

4. The END OF FILE indicator should be lighted (if the End of File status is desired).

5. Press the RELOAD MEMORY switch, if necessary, to ensure that one card has been read into memory.

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FIGURES

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CONTROL DATA 1742-A/B LINE PRINTER

1742-A/B LINE PRINTER

INTRODUCTION

The CONTROL DATA® 1742-A/B Line Printer consists of a controller and a 300 lines-per-minute (LPM) drum printer. The controller consists of ten 50-PAKs; seven for control, three for memory. It interfaces with one data channel, either normal or buffered. The controller receives and interprets function codes from this channel to initiate the print cycle, control paper motion, and enable interrupts when specified conditions arise. The controller includes a buffer memory that is capable of storing one line of print.

Specifications

The specifications and characteristics of the printer are as follows:

Printing rate	- 300 LPM (single line = 136 columns, 64 different characters)
Data Transfer rate	- accepts 16-bit data word every 15 μsec.
Drum speed	- 360 rpm
Paper spacing time	- single line: $T = 25$ ms
	- multiple line: $T = 25 + 8.4 (N-1)$ ms

Memory capable of storing one line of print

Line Spacing - either 6 or 8 lines per inch

Forms

The printer will handle continuous forms punched on both margins about one fourth inch from the edge. These margin holes should be one half inch apart. Other characteristics are as follows:

Width - The printer is capable of handling forms from 3-1/2 inches wide to 20-5/8 inches wide.

Length - The length of an individual form runs up to a maximum of 22 inches Form length is directly related to format tape length.

Single copy paper - For best quality print, paper should be at least 15 lb bond.

Multiple copy paper - A good quality print may be obtained from up to a six-part form. Multiple copy paper includes single sheet carbons.

Stacking - The stacking basket supplied with the printer handles forms up to 11 inches wide. Forms of greater width must be stacked behind the printer.

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FUNCTIONAL
DESCRIPTION

System Relationship   The controller interfaces the printer with a 16-bit bidirectional channel. It may interface with:

   a.   The 1706 or 1716 Data Channels for buffered communication

   b.   The 1705 for non-buffered communication
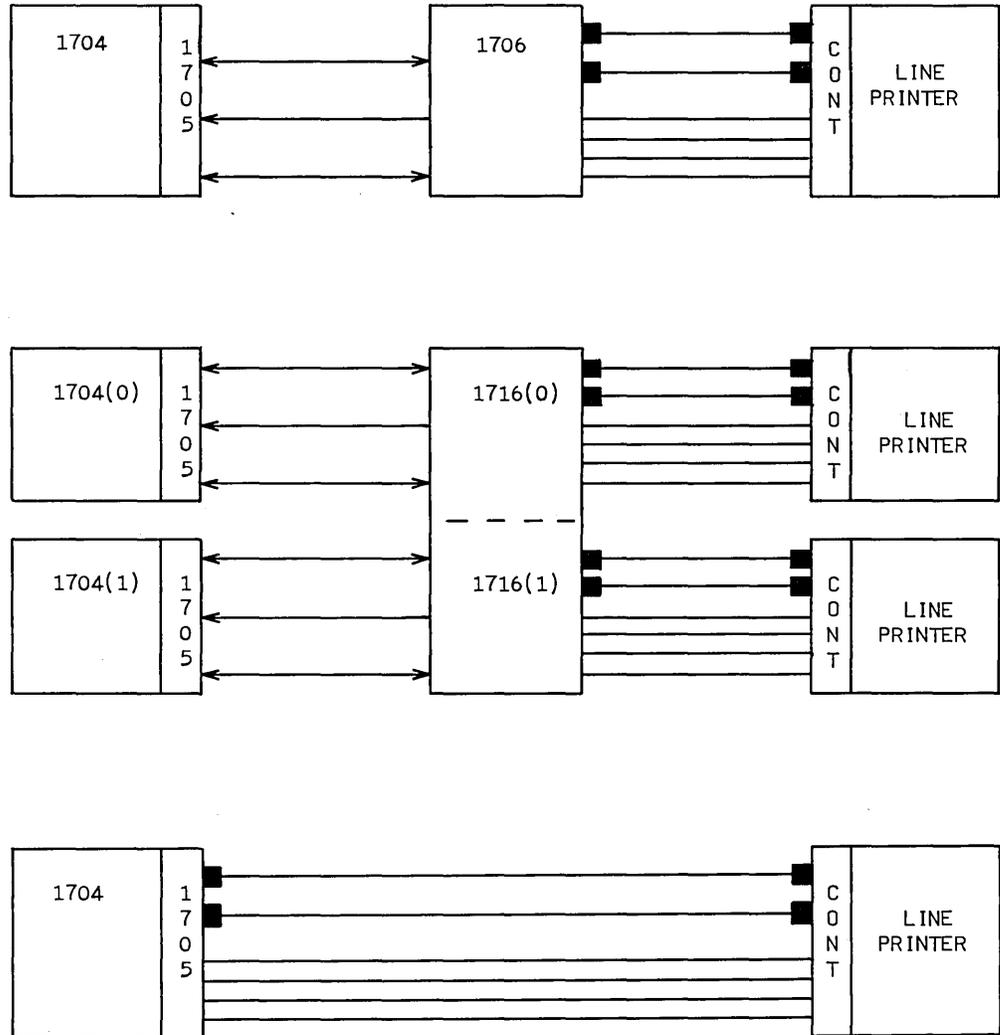
Typical configurations are shown in Fig. 1.

Figure 1.   Typical Configurations

The address of the printer and controller is selected by four double-pole, double-throw toggle switches. See Figure 2. Any of 16 different equipment codes may be set up by these switches.
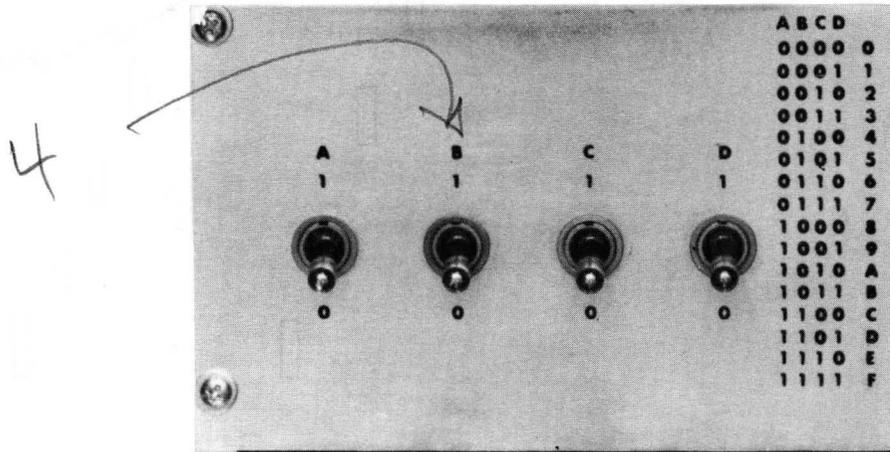

Figure 2. Equipment Select Switches

Data Word Format

A single data word which occupies the A register consists of two 7-bit character codes. The two character codes occupy bit positions A00 - A06 and A08 - A14.

Print-out Format

In the print-out, a total of 136 columns or print locations per line are possible. Sixty-four different characters are available as listed in the ASCII 1967 Code. See Table 2. Detection of an illegal character code generates an alarm status.

Buffer Memory

The buffer memory is a 320-word (4-bits per word) memory with a cycle time of about 2.0 μsec. The controller causes the buffer memory to function as a 136-word (8-bits per word) memory, giving the printer the capability of storing one line of print. Data transferred in excess of one line will be rejected by the printer.

Ribbon

The inked ribbon runs at an angle across the print drum. It continually advances when the printer is in operation, and automatically reverses when it approaches the end. The ribbon assembly consists of the ribbon and the two spools on which it rides. Each spool is driven by an individual motor.
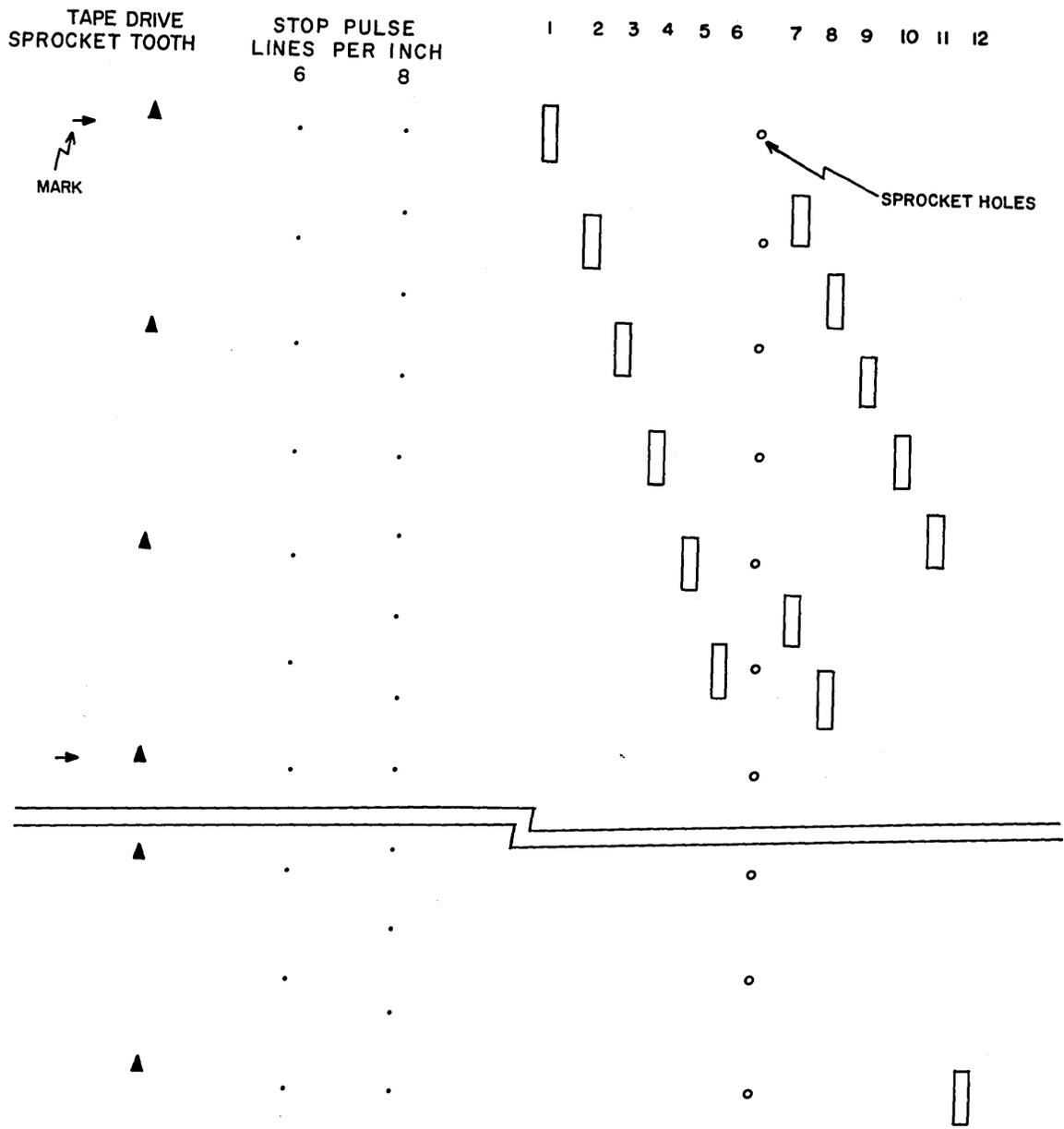
1742
Rev M

Figure 3. Format Tape

Format Tape	The format tape, Figure 3, is a 12-level tape with center-punched sprocket holes for pin feeding. The format tape is joined in a continuous loop and advances through the reader at the rate of one frame for each line of paper advance. The sprocket hole positions correspond to the frame positions for 6 lines-per-inch paper spacing.

Format Tape Levels	The operator should take care when switching from one type of spacing to the other. When the tape is punched for 6 lines-per-inch and the program selects 8 lines-per-inch under format control, irregular spacing may result. See Figure 3.

1. Format Tape Level 1 should always correspond to the Top of Form position. Pressing the TOP OF FORM switch will advance paper and move the format tape until a hole in Level 1 is under the brushes.

2. Format Tape Level 12 should always be used to indicate the last line of form. This hole is used in the Single Cycle operation. A punch in this level is required for each page that is represented on the format tape.

Alarm	An Alarm indicates the presence of an abnormal condition. The abnormal conditions are divided into two types.

1. Those which cause the printer to go Not Ready, requiring operator intervention. These conditions are paper out, paper tear, fuse alarm, and an open interlock. The alarm is cleared upon correction of the cause for the Not Ready condition followed by a Clear Printer, Print Director Function, or a Master Clear.

2. A condition allowing Ready status to remain. This condition occurs when an illegal character code is transferred into memory. This alarm may be cleared by a Clear Printer or a Print Director Function, or a Master Clear.

Flag Bits	The flag bits are added to each character code (one per character code) loaded into the buffer memory, and they are used during a Print operation. A flag bit changes from "1" to "0" when the associated character is printed. When all flag bits are "0" after one pass though memory, the Print operation has ended.

Program Protection	When the PROTECT switch on the printer is on, only those I/O, instructions having a "1" on the protect line will be recognized.

When the PROTECT switch is off, either protected or unprotected instructions will be recognized.

Reply/Reject

Within approximately 4 μsec, the printer always responds to an Input-to-A or an Output-from-A instruction with either a Reply or a Reject signal.

A Reply signal is sent by the printer if it can accept the Director Function of the Data Transfer instruction.

A Reject signal is sent by the printer if it cannot perform the function or transfer instruction. Three conditions that will cause this Reject signal to be returned are:

1. The printer is Busy.

2. A program-protection fault occurs.

3. The printer is Not Ready.

PROGRAMMING

Program Summary

Table 1 and Figures 4 through 8 provide programming information. A description follows the figures.

TABLE 1. TRANSLATION OF LOWER Q BITS

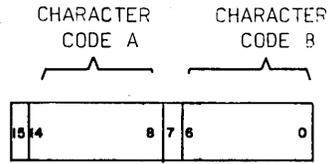| Q BITS 01-00 (D)	OUTPUT FROM A	INPUT TO A
0 0	Data Transfer	
0 1	Director Function 1	
1 1	Director Function 2	Director Status

Figure 4. Q Register Format
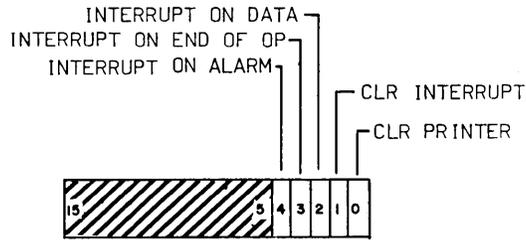
Figure 5. Data Transfer
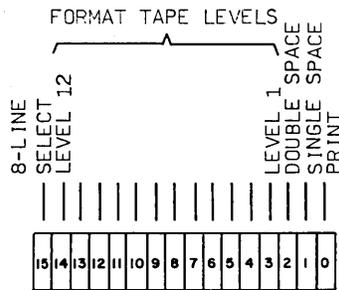

Figure 6. Director Function 1
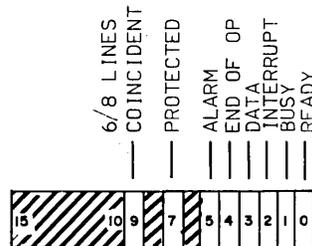

Figure 7. Director Function 2

Figure 8. Director Status

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CODES   Equipment Codes and Command Codes are described as follows:

Equipment   The E portion of the Q register (Q07-Q10) defines the printer's equipment code. (The W portion, Q11-Q15 of Q must be all zeros.) This code is set up by the four Equipment Select Switches shown in Figure 2.

Command   A command code is needed to direct and define an operation to be performed. Bits Q00-Q06 of the Q register defines a command code which, when accompanied by an equipment code and either a Read or Write signal, defines the operation to be performed by the printer. Only bits Q00 and Q01, the D portion of Q, are sampled in the check for a command code. See Table 1. Two general types of operations are selected by the command code: Data Transfer and Director Functions.

DATA TRANSFER (Q00=0, Q01=0)

When Q00 and Q01=0, the 16 lines of the data cable (A) are directed to perform a data transfer. Data will be accepted unless one or more of the following reject conditions is present: The printer is Not Ready, the buffer memory is full, data is transmitted at an output rate exceeding printer capabilities, or the printer is Busy with a Print operation.

A flag bit (A07 and A15) is added to each Character Code (A00-A06 and A08-A14) loaded into memory. The flag bit is used only during the Print operation. Each time a character from memory is printed the flag bit is changed from "1" to "0". Printer control senses these flag bits and when they are all "0", all characters in memory have been printed.

DIRECTOR FUNCTIONS (FUNCTION 1 Q00=1, Q01=0)

When Q00=1 and Q01=0, and it is accompanied by both an equipment code and Write signal, the data cable (A) will direct the printer to perform Function 1. All the functions in this group will be accepted and replied to when the printer is Ready and either Busy or Not Busy, except Clear Printer (A00=1).

Clear Printer (A00=1)

This function will initiate a Clear pulse with a duration of 0.1 μsec clearing control, interrupt requests, interrupt responses, and alarm conditions. It is subordinate to all other bits in this group, and therefore the printer must be Ready and Not Busy to execute this function.

Clear Interrupt (A01=1)

This function will initiate a pulse of 0.1 μsec which will clear all interrupt requests and interrupt responses. It is subordinate to all interrupt request bits coming in so it cannot prevent the setting of new interrupts.

NOTE

Each of the following three interrupt responses, A02, A03, and A04 is transmitted to the computer on a different cable. A fourth cable, Common interrupt, will carry a "1" signal to the computer whenever A02, A03 or A04 is a "1".

Interrupt on Data (A02=1)

This function will set the Data Interrupt FF. This, in turn, enables the generation of an interrupt indicating data transfer to the printer can commence. The interrupt request may be cleared by a Master Clear or by either A00=1 or A01=1 with A02=0.

The interrupt response may be cleared by clearing the interrupt request as stated above. Before a Data Transfer to the printer, this interrupt may be requested and the response will signal the computer that the printer is ready to receive another data transfer. Without reselecting or clearing this interrupt response, the data transfer can take place. During this data transfer, interrupt response will be removed until the printer is ready to receive another data transfer.

Interrupt on End of Operation (A03=1)

This function enables the generation of an interrupt upon the completion of an operation. The interrupt may be selected before or during the operation. An interrupt response will not occur for an operation which was ended before the selection was made. The interrupt request may be cleared by the Master Clear or by either A00=1 or A01=1 with A03=0.

The interrupt response may be cleared by a Master Clear or by either A00=1 or A01=1. When the response is cleared by A00=1 or A01=1, the request may be reset in one operation if A03=1.

Interrupt on Alarm (A04=1)

This function enables the generation of an interrupt when an Alarm condition exists. An Alarm condition that exists at the time this interrupt request is made will immediately provide a response. If the Alarm condition does not exist at the time of the interrupt request, the interrupt response will be provided as soon as an Alarm condition is detected. These conditions are listed in the Alarm section. The interrupt request may be cleared by Master Clear or by either A00=1 or A01=1 with A04=0. The register bits A05 through A15 in this group are not used.

The interrupt response may be cleared by a Master Clear or by either A00=1 or A01=1. When the interrupt response is cleared by A00=1 or A01=1, the interrupt request may be reset with the same operation if A04=1.

The functions in this group may be stacked; that is, two or more functions may be given at the same time. It should be noted that when A00=1 and/or A01=1 are used with stacking, the Clear pulse will take place first, followed by any stacked functions.

DIRECTOR FUNCTIONS (FUNCTION 2 Q00=1, Q01=1)

When Q00=1 and Q01=1, and it is accompanied by both an equipment code and Write signal, the data cable (A) will direct the printer to perform Function 2. All the functions in this group will be accepted and replied to only when the printer is Ready and Not Busy, otherwise they will be rejected.

Print (A00=1)

This function directs the printer to initiate a Print operation. A Print operation is the time between acceptance of a Print Director Function and completion of a line of print. During a Print operation, the Data Director Status will be "0".

Single Space (A01=1)

This function directs the printer to space the paper one line.

Double Space (A02=1)

This function directs the printer to space the paper two lines.

Format Tape Level 1 (A03=1) Through Format Tape Level 12 (A14=1)

Functions A03 through A14 direct the printer to initiate paper motion and to terminate it upon the detection of a hole in the selected Format Tape Level. Tape Levels 1 and 12 are assigned to Top of Form and Last Line of Form, respectively.

8 Line Select (A15=1)

This function directs the printer to space paper using a vertical line pitch of 8 lines per inch. Once 8 line-per-inch pitch is selected, it will stay selected until cleared by a Master Clear or by a Clear Printer.

NOTE

When stacking the functions in the above group, some program restriction will be in effect. For these program restrictions, see Programming Considerations.

DIRECTOR STATUS

The printer always replies to a status request signal. It therefore replies when Q00=1 and it is accompanied by an equipment code and a Read signal. Eight lines of the 16-line data cable (A) transfer the status responses to the computer. The status responses are described below.

Ready (A00=1)

Indicates that a Ready condition exists. The Ready condition must be existing before the printer can operate, and the absence of any one of several requirements can prevent this. The requirements are as follows:

1. All power supplies are operating.

2. Fuses are intact

3. Paper is present

4. Brush reader interlock is in closed position

5. Drum arm is in printing position

6. The READY switch has been pressed

Busy (A01=1)

Indicates that the printer is Busy. The printer becomes Busy:
1. During transfer and storage of each character
2. After the initiation of a print cycle and until all the characters in memory have been printed
3. When any paper motion is initiated and until it stops

Interrupt (A02=1)

Indicates that an interrupt response was generated by the printer. The other status bits must be monitored to determine the cause of the interrupt.

Data (A03=1)

Indicates that the printer is ready to receive data. If Interrupt on Data has been selected, this status will also indicate that this interrupt has occurred. During the loading of the buffer memory, this status signal will follow the Not Busy status signal with each 16-bit word until memory is full. When memory is full, the Not Busy status signal will go back up but the Data status signal will stay down and the data will be rejected.

End of Operation (A04=1)

Indicates that the printer has completed an operation. If Interrupt on End of Operation has been selected, this status bit will also indicate this interrupt has occurred.

Alarm (A05=1)

Indicates that an Alarm condition is present. (For definition of Alarm, see Alarm section.)

Director Status bit A06 is not used.

Protected (A07=1)

Indicates that the PROTECT switch on the printer is on (lighted). In this position, the printer will accept only those instructions having a "1" on the Program Protect line. All other instructions will be rejected. The protect bit is ignored when the printer PROTECT switch is off.

6/8 Line Coincident (A09=1)

Indicates that, at this time, the changing from 6 to 8 lines per inch, or vice versa, can be made without introducing a spacing error.

Director Status bits A10 through A15 are not used.

Character

The following table contains the character code list for ASCII, and it should be noted that Control Data refers to the lowest bit of this 7-bit code as bit zero. In the ASCII listing the lowest bit of a character code is called bit 1.

See also Pg 10-34 of MSOS 2.1

TABLE 2. CHARACTER CODES

ASCII CODE HEXADECIMAL	7-BIT CODE b_6------b_0	DRUM ROW	CHARACTER	SYMBOL
20	010 0000	1	Space	Character is not printed. Used only for balance.
21	010 0001	2	Exclamation Point	!
22	010 0010	3	Quotation Mark	"
23	010 0011	4	Number Sign	#
24	010 0100	5	Dollar Sign	$
25	010 0101	6	Percent	%
26	010 0110	7	Ampersand	&
27	010 0111	8	Apostrophe	'
28	0101000	9	Opening Parenthesis	(
29	010 1001	10	Closing Parenthesis	)
2A	010 1010	11	Asterisk	*
2B	010 1011	12	Plus	+
2C	010 1100	13	Comma	,
2D	010 1101	14	Hyphen	-
2E	010 1110	15	Period	.
2F	010 1111	16	Slant	/
30	011 0000	17	Zero	0
31	011 0001	18	One	1
32	011 0010	19	Two	2

TABLE 2. (Cont'd.)

ASCII CODE HEXADECIMAL	7-BIT CODE b_6------b_0	DRUM ROW	CHARACTER	SYMBOL
33	011 0011	20	Three	3
34	011 0100	21	Four	4
35	011 0101	22	Five	5
36	011 0110	23	Six	6
37	011 0111	24	Seven	7
38	011 1000	25	Eight	8
39	011 1001	26	Nine	9
3A	011 1010	27	Colon	:
3B	011 1011	28	Semicolon	;
3C	011 1100	29	Less than	
3D	011 1101	30	Equals	=
3E	011 1110	31	Greater than	
3F	011 1111	32	Question Mark	?
40	100 0000	33	At Sign	
41	100 0001	34	Letter	A
42	100 0010	35	Letter	B
43	100 0011	36	Letter	C
44	100 0100	37	Letter	D
45	100 0101	38	Letter	E
46	100 0110	39	Letter	F
47	100 0111	40	Letter	G
48	100 1000	41	Letter	H
49	100 1001	42	Letter	I
4A	100 1010	43	Letter	J
4B	100 1011	44	Letter	K
4C	100 1100	45	Letter	L
4D	100 1101	46	Letter	M
4E	100 1110	47	Letter	N
4F	100 1111	48	Letter	O
50	101 0000	49	Letter	P

TABLE 2. (Cont'd.)

ASCII CODE HEXADECIMAL	7-BIT CODE $b_6 \text{------} b_0$	DRUM ROW	CHARACTER	SYMBOL
51	101 0001	50	Letter	Q
52	101 0010	51	Letter	R
53	101 0011	52	Letter	S
54	101 0100	53	Letter	T
55	101 0101	54	Letter	U
56	101 0110	55	Letter	V
57	101 0111	56	Letter	W
58	101 1000	57	Letter	X
59	101 1001	58	Letter	Y
5A	101 1010	59	Letter	Z
5B	101 1011	60	Opening Bracket	
5C	101 1100	61	Reversed Slash	
5D	101 1101	62	Closing Bracket	
5E	101 1110	63	Circumflex	
5F	101 1111	64	Underline	_

PROGRAMMING CONSIDERATIONS

Format Tape Synchronization

The Format Tape Reader restricts the location of the holes in the tape. Two holes may not be adjacent in either the longitudinal or the transverse direction. To make effective use of the 6/8 lines-per-inch spacing feature, the format tape must be installed so that the STP (Stop Paper Pulse) signals for both 6 and 8 line-per-inch spacing are present when a hole is detected in Format Tape Level 1 (Top of Form). This condition will be satisfied when the tape is installed so that the hole in Format Tape Level 1 is lined up with one of the four marks on the tape sprocket. See Figure 3.

Restrictions

Stacking of Director Functions with Q00=1 and Q01=1

It is not advisable to stack the functions in this group. When a print function is stacked with any paper motion function, both printing and paper motion will start at the same time. If two or more paper motion functions are stacked, the paper will stop at the hole that was the farthest from the brushes when the paper motion was started.

<u>Output Limitations</u>

It is possible to program the printer so that its capabilities are exceeded.

EXAMPLE: A solid line of all one character is printed, the paper is single
space, memory is loaded during this paper motion with another
(second) line of all one character which will be in print position
25 ms after the first line was printed. The second line is then
printed. If this operation is repeated, the power supply will
not recover. This type of operation is illegal, and it must be
avoided.

MANUAL OPERATION

**Switches and
Indicators**

<u>Switches and Indicators</u>

The switches and indicators on the front panel of the printer are illustrated
in Figure 9 and are described on page 18.

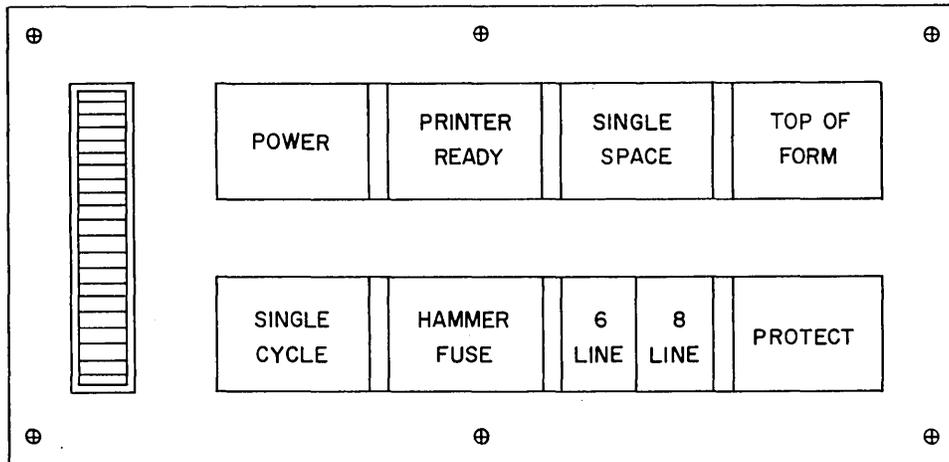| POWER | PRINTER READY | SINGLE SPACE | TOP OF FORM |
| SINGLE CYCLE | HAMMER FUSE | 6 LINE | 8 LINE | PROTECT |

Figure 9. Control Panel

POWER Switch and Indicator

Pressing this alternate action switch causes power to be applied to or removed from all motors, fans, and power supplies in the proper sequence to prevent spurious print-out or paper advance. The indicator lights to indicate that power is applied to the equipment.

PRINTER READY Switch and Indicator

Pressing this momentary contact switch results in the equipment becoming Ready if the required conditions exist in the printer. When the printer is ready, the indicator is lighted. Re-pressing this switch turns off the indicator light and causes the printer to become Not Ready, stopping any further operation after the operation in progress is completed.

> NOTE
>
> If the equipment fails to become Ready when the PRINTER READY switch is pressed, the operator should make certain that the printer is loaded with paper, the print drum latch (interlock) is firmly closed, and that the format-tape brush-reader interlock is engaged before checking for other conditions which can cause a Not Ready.

SINGLE SPACE Switch

Pressing this momentary contact switch causes the paper to advance one line. This switch does not require a Ready condition to be operable.

TOP OF FORM Switch

This momentary contact switch causes the paper to advance to the top of form position, and is controlled by Tape Format Level 1. This operation first requires that the format-tape brush-reader interlocks be closed.

SINGLE CYCLE Switch

This momentary contact switch can be pressed to allow the printing of one additional line if an out-of-paper condition exists. The switch can be pressed again to print additional lines as necessary to complete the form being printed, until the Last Line of Form hole in the printer tape is sensed.

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HAMMER FUSE Indicator

This indicator is lighted when one or more hammer drivers have open fuses.

6-LINE/8-LINE Indicator

This divided lens indicator will show white or red light depending on program selection of 6 or 8 inch line spacing, respectively, in the printer.

PROTECT Switch and Indicator

This alternate action switch, when pressed, places the printer in the Protected condition, or it can be used to remove the printer from the Protected condition. The indicator will be lighted when the printer is protected.

NOTE

The controls described above which do not have any switches, but indicate only, are under Director Function Control.

Character Phasing Control

The Control knob (wheel) provides vertical adjustment of the coverage of printed characters. The adjustment range is plus or minus half a character.

Maintenance Switches

The nine maintenance toggle switches are located in the upper right-hand part of the controller Logic Chassis. These switches provide for adjusting and checking the printer. The switches are shown in Figure 10.

Bit Switches

The seven bit-switches enable setting any one of the character codes.

Run Switch

Use of this switch enables the device to print. If the printer is not off-line it is necessary to avoid interruption by the computer which may be running. Therefore the printer's controller will go Not Ready while this switch is in the Run position. However, a computer Master Clear can still clear the operation; therefore, it is better to disconnect the printer from the system taking if off-line for maintenance.

<u>Clear Switch</u>

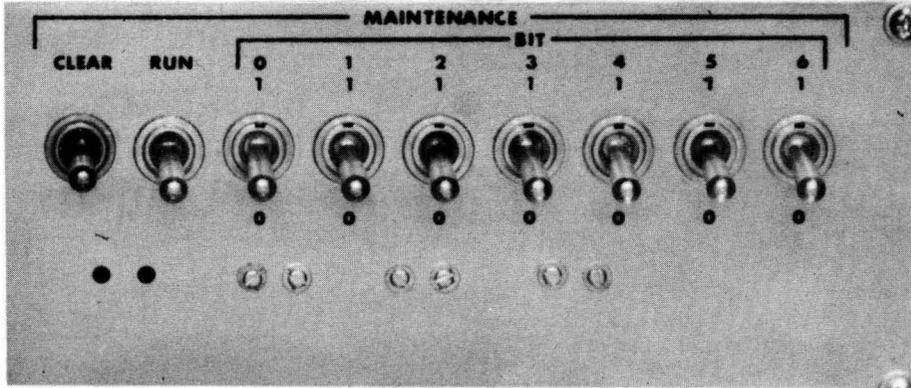This switch sends a Clear signal to the controller.
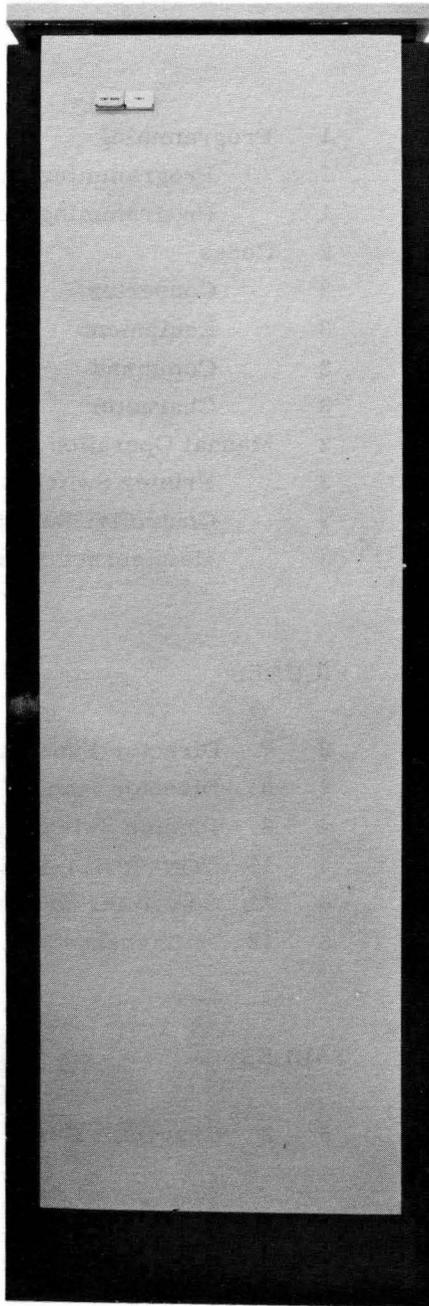

Figure 10.   Maintenance Switches

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FIGURES

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Rev K

CONTROL DATA 1740 LINE PRINTER CONTROLLER

1740 LINE PRINTER CONTROLLER

INTRODUCTION

The CONTROL DATA ® 1740 Line Printer Controller interfaces a CONTROL DATA® 501 or 505 Line Printer and one data channel, either normal or buffered. The controller receives and interprets function codes from the data channel to initiate the print cycle, control paper motion, and enable interrupts when the specified conditions arise. The controller contains a buffer memory that is capable of storing one line of print.

The specifications and characteristics of the equipment are as follows:

501 printing rate	- Nominally 1000 lpm (single space, 136 columns, 48 adjacent characters)
505 printing rate	- 500 lpm
Data transfer rate	- Accepts 16-bit data word every μsec
501 drum speed	- 1000 rpm
505 drum speed	- 500 rpm
Paper spacing time	- Single space: $T = 15$ ms
	- Multiple space: $T = 15 + 6(N-1)$ ms
Line spacing	- Six lines per inch

Memory capable of storing one line of print

FUNCTIONAL DESCRIPTION

System Relationship

The controller interfaces the printer with a 16-bit bidirectional channel. It may interface with the 1706 or 1716 Data Channel for buffered communication or the 1705 for non-buffered communication. Some typical configurations are shown in Figure 1.

The address of the printer and controller is selected by four double-pole, double-throw toggle switches (Figure 2). Any one of 16 different equipment codes may be set up by these switches.
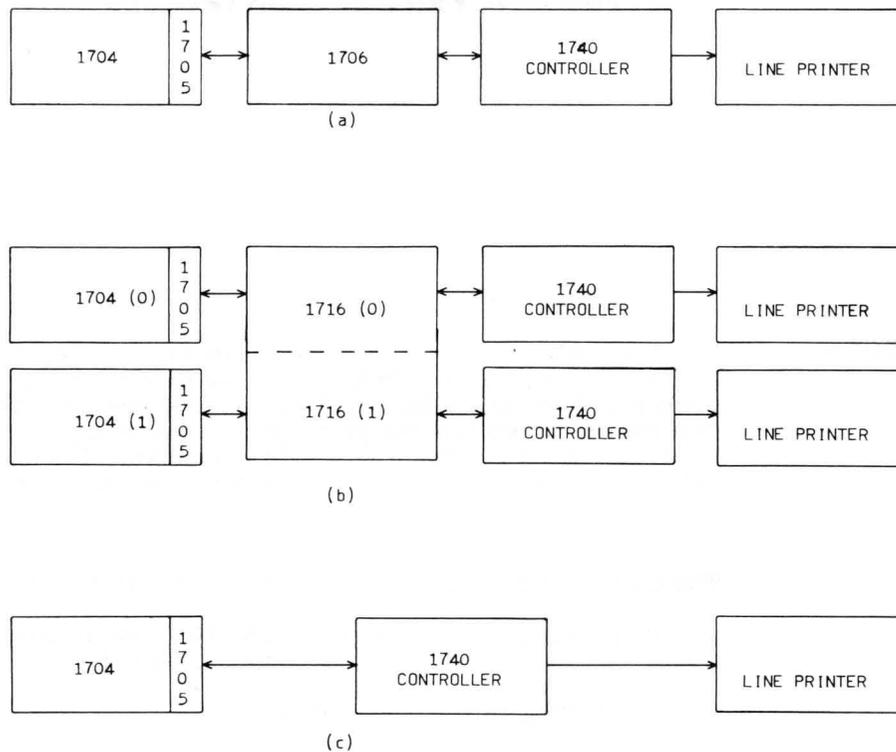
Figure 1.   Typical Configuration
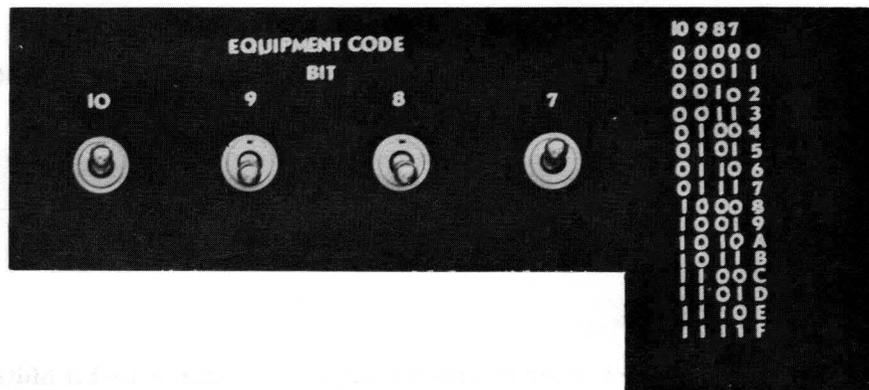
Figure 2.   Equipment Select Switches

Data Word Format

A single data word which occupies the A register consists of two 7-bit character codes.   The two character codes occupy bit positions A00 - A06 and A08 - A14.

Print-out Format

In the print-out, a total of 136 columns or print locations per line are possible.   Sixty-four different characters are available as listed in the ASCII 1967 Code.   See Table 2.   Detection of an illegal character code generates an alarm status.

Buffer Memory

The buffer memory has a capacity of 80 14-bit words but is never loaded with more than 68 words. Data transferred in excess of one line will be rejected by the printer.

Format Tape

The format tape (Figure 3) is an 8-level tape consisting of Levels 1 through 7 and Level 12, with sprocket holes for pin feeding. The format tape is joined in a continuous loop and advances through the reader at the rate of one frame for each line of paper advance. The sprocket hole positions correspond to the frame positions for 6 lines-per-inch paper spacing.

Format Tape Levels

Format Tape Level 1 should always correspond to the Top of Form position. Pressing the PAGE EJECT switch advances paper and moves the format tape until a hole in Level 1 is under the photocells.

Format Tape Level 12 should always be used to indicate the last line of form. This hole is used in the Single Cycle operation. A punch in this level is required for each page that is represented on the format tape.

Alarm

An alarm indicates the presence of an abnormal condition. The abnormal conditions are divided into two types:

1. Those which cause the printer to go Not Ready, requiring operator intervention. These conditions are paper out, paper tear, and fuse alarm. The alarm is cleared upon correction of the cause for the Not Ready condition followed by a Clear Printer, Print Director function, or a Master Clear.

2. A condition which allows Ready status to remain. This condition occurs when an illegal character code is transferred into memory. This alarm may be cleared by a Clear Printer, Print Director function, or a Master Clear.

Flag Bits

The flag bits are added to each character code (one per character code) loaded into the buffer memory and are used during a print operation. A flag bit changes from "1" to "0" when the associated character is printed. When all flag bits are "0", the print operation terminates.

Program Protection

When the PROTECT switch on the printer is on, only those I/O instructions having a "1" on the protect line are recognized. When the PROTECT switch is off, both protected or unprotected instructions are recognized.

Reply/Reject

The controller responds to an Input-to-A or an Output-from-A instruction with either a Reply or a Reject signal within approximately 4 μsec.

A Reply signal is sent by the controller if it can accept the director function of the Output-from-A instruction.

A Reject signal is sent by the controller if it cannot perform the function or transfer instruction. Three conditions that cause the Reject signal to be returned are:

1. The printer is Busy.

2. A program-protection fault occurs.

3. The printer is Not Ready.

Figure 3. Format Tape Levels

PROGRAMMING

**Programming
Summary**

Table 1 and Figures 4 through 8 provide programming information. A description of the codes follows the figures.

TABLE 1. DIRECTOR CODE (D) BIT FUNCTIONS

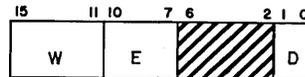| D (Q BITS 01-00)	INSTRUCTION	OPERATION
00	Output From A	Data Transfer
01	Output From A	Director Function 1
11	Output From A	Director Function 2
11	Input From A	Director Status

Figure 4. Q Register Format

**Programming
Considerations**

Stacking of Director Function 2 Codes

It is not advisable to stack the functions in this group. When a print function is stacked with any paper motion function, both printing and paper motion start at the same time. If two or more paper motion functions are stacked, the paper stops at the hole that was the farthest from the photocells when the paper motion was started.

Output Limiations

It is possible to program the printer so that its capabilities are exceeded.

EXAMPLE: A solid line of all one character is printed, the paper is single spaced, memory is loaded during this paper motion with another (second) line of all one character which will be in print position 15 ms after the first line was printed. The second line is then printed. If this operation is repeated, the power supply will not recover. This type of operation is illegal and must be avoided.
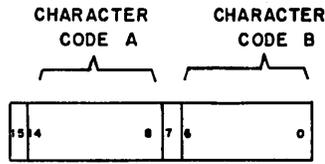
CHARACTER CODE A CHARACTER CODE B

15 14   8 | 7 6   0

Figure 5. Data Transfer

INTERRUPT ON DATA
INTERRUPT ON END OF OP
INTERRUPT ON ALARM
CLR INTERRUPT
CLR PRINTER

15   5 4 3 2 1 0

Figure 6. Director Function I

LEVEL 12
LEVEL 7
6 5 4 3 2
LEVEL 1
DOUBLE SPACE
SINGLE SPACE
PRINT

15 14 13   10 9 8 7 6 5 4 3 2 1 0

Figure 7. Director Function II

PROTECTED
ALARM
END OF OP
DATA
INTERRUPT
BUSY
READY

15   9 7 5 4 3 2 1 0
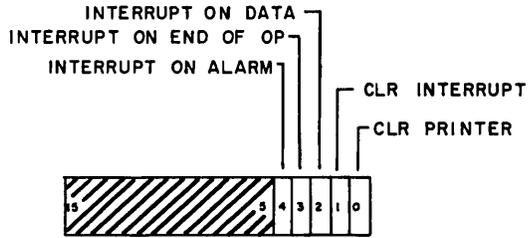
Figure 8. Director Status

CODES

Converter

The W portion of the Q register (Q11-Q15) must be zero for all printer operations.

Equipment

The E portion of the Q register (Q07-Q10) defines the printer's equipment code. This code is set up by the four Equipment Select switches shown in Figure 2.

Command

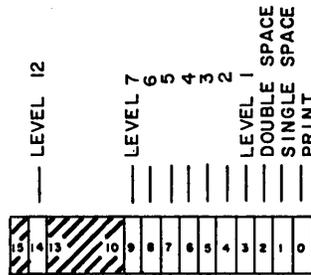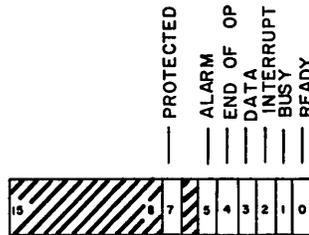A command code is needed to direct and define an operation to be performed. Bits Q00-Q06 of the Q register define a command code which, when accompanied by an equipment code and either a Read or Write signal, defines the operation to be performed by the printer. Only bits Q00 and Q01, the D portion of Q, are sampled in the check for a command code (see Table 1). Bits Q00 and Q01 define the word being transferred as data, director function (two levels), or director status. Bits Q02 through Q06 are not used.

DATA TRANSFER

When Q00 and Q01 equal "0", the 16 lines of the data cable (A) are directed to perform a data transfer. A Reject occurs if data cannot be accepted when:

1. The printer is Not Ready.
2. The buffer memory is full.
3. The data is transmitted at an output rate exceeding the capabilities of the printer.
4. The printer is Busy because a print cycle is in progress.

The controller adds a flag bit (A07 and A15) to each character code (A00-A06 and A08-A14) and loads them into the controller memory. The flag bit is used only during the print operation. Each time a character from memory is printed the flag bit is changed from "1" to "0". The controller senses these flag bits and when they are all "0", an End of Print operation is indicated.

DIRECTOR FUNCTION 1 (Q00=1, Q01=0)

Director Function 1 initiates operations in the controller. All functions, except Clear Printer (A00=1), in this group will be accepted and replied to when the printer subsystem is Ready and either Busy or Not Busy. The register bits A05 through A15 are not used for Director Function 1 codes.

The functions in this group may be stacked (two or more functions may be given at the same time). When A00=1/A01=1 are stacked with other function codes, the Clear pulse first occurs followed by whatever other functions are stacked.

The controller can be directed to interrupt on three conditions: Interrupt on Data, Interrupt on End of Operation, and Interrupt on Alarm. Each interrupt responds to the computer via a separate cable. A fourth interrupt cable carries an interrupt response to the computer if any one of the interrupt conditions is met.

All interrupt requests and responses can be cleared by a Master Clear, Clear Printer function, or Clear Interrupt function.

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Clear Printer (A00=1)

This function initiates a 0.5-μsec Clear pulse which clears control, interrupt requests, interrupt responses, and alarm conditions in the controller. It is subordinate to all other bits in this group, and therefore the printer must be Ready and Not Busy to execute this function.

Clear Interrupt (A01=1)

This function initiates a pulse of 0.5 μsec which clears all interrupt requests and interrupt responses. It is subordinate to all interrupt request bits; it cannot prevent the setting of new interrupts.

Interrupt on Data (A02=1)

This function sets the Data Interrupt Request FF in the controller. This, in turn, enables the generation of an interrupt indicating data transfer to the controller can begin. If A02=0 the interrupt request may be cleared by a Master Clear, Clear Printer function, or Clear Interrupt function.

The interrupt response may be cleared by clearing the interrupt request as stated above. Before a data transfer to the controller, this interrupt may be requested and the response will signal the computer that the controller is ready to receive another data transfer. Without reselecting or clearing this interrupt response, the data transfer can take place. During this data transfer, interrupt response is removed until the controller is ready to receive another data transfer.

Interrupt on End of Operation (A03=1)

This function enables the generation of an interrupt upon the completion of an operation. The interrupt may be selected before or during the operation. An interrupt response will not occur for an operation which was ended before the selection was made. If A03=0 the interrupt request may be cleared by the Master Clear, Clear Printer function, or Clear Interrupt function.

The interrupt response may be cleared by a Master Clear, Clear Printer function, or Clear Interrupt function. When the response is cleared by Clear Printer or Clear Interrupt, the request may be reset in one operation if A03=1.

Interrupt on Alarm (A04=1)

This function enables the generation of an interrupt when an Alarm condition exists. An Alarm condition that exists at the time this interrupt request is made, will immediately provide a response. If the Alarm condition does not exist at the time of the interrupt request, the interrupt response will be provided as soon as an Alarm condition is detected. These conditions are listed in the Alarm section. The interrupt request may be cleared by Master Clear, Clear Printer function, or Clear Interrupt function.

The interrupt response may be cleared by a Master Clear or by either Clear Printer or Clear Interrupt functions. When the interrupt response is cleared by Clear Printer or Clear Interrupt, the interrupt request may be reset with the same operation if A04=1.

DIRECTOR FUNCTION 2 (Q00=1, Q01=1)

Director Function 2 controls operations in the printer. All the functions in this group are accepted and replied to only when the printer is Ready and Not Busy.

Print (A00=1)

This function directs the printer to initiate a print operation. A print operation is the time between acceptance of a Print Director function and completion of a line of print. During a print operation, the Data Director status will be "0".

Single Space (A01=1)

This function directs the printer to space the paper one line.

Double Space (A02=1)

This function directs the printer to space the paper two lines.

Format Tape Level 1 (A03=1) Through Format Tape Level 7 (A09=1) And Format Level 12 (A14=1)

These functions direct the printer to initiate paper motion and to terminate it upon the detection of the selected tape level. Tape Levels 1 and 12 are assigned to top of form and last line of form, respectively.

NOTE

The functions in the above group should not be stacked. For an explanation, see Programming Considerations.

DIRECTOR STATUS (Q00=1)

The controller always replies to a status request signal. It replies when Q00=1 and it is accompanied by an equipment code and a Read signal. Seven lines of the 16-line data cable (A) transfer status signals to the computer. The status responses are described in the following paragraphs.

Ready (A00=1)

Indicates that a Ready condition exists. The controller must be Ready before the printer can operate, and the absence of any one of the following will make the printer/controller Not Ready:

1. All power supplies are operating.
2. Fuses are intact.
3. Paper is present.
4. The READY switch has been pressed.

Busy (A01=1)

Indicates that the controller is Busy. The controller becomes Busy:

1. During transfer and storage of each character.

2. After the initiation of a print cycle and until all the characters in memory have been printed.

3. When any paper motion is initiated and until it stops.

Interrupt (A02=1)

Indicates that an interrupt response was generated by the controller. The other status bits must be monitored to determine the cause of the interrupt.

Data (A03=1)

Indicates that the controller is ready to receive data. If Interrupt on Data has been selected, this status also indicates that this interrupt has occurred. During the loading of the buffer memory, this status signal follows the Not Busy status signal with each 16-bit word until memory is full. When memory is full, the controller will be Not Busy, the Data status bit will equal "0", and the data will be rejected.

End of Operation (A04=1)

Indicates that the printer has completed an operation. If Interrupt on End of Operation has been selected, this status bit indicates whether the operation has ended.

Alarm (A05=1)

Indicates that an Alarm condition is present. (For definition of Alarm, see Alarm section.)

Director status bit A06 is not used.

Protected (A07=1)

Indicates that the PROTECT switch on the controller is in the PROTECT position. In this position, the controller accepts only those instructions having a "1" on the Program Protect line. All other instructions are rejected. A protected instruction can be used with either a protected or unprotected controller, because a controller in the Not Protected condition ignores all instructions with a "1" on the Program Protect line.

Director status bits A08 through A15 are not used.

Character

The controller is designed to use a line printer with ASCII characters on its drum. It is required that the programmer use the ASCII code which matches these characters. However, it is possible to substitute a standard BCD drum on the printer and to use it with ASCII code. The two drums have identical characters in all but 10 cases. These characters are noted in the following table:

TABLE 2. CHARACTER CODES

ASCII CODE HEXADECIMAL	7 BIT CODE $b_6 ------ b_0$	DRUM ROW	CHARACTER	ASCII SYMBOL	BCD SYMBOL
30	011 0000	1	Zero	0	
31	011 0001	2	One	1	
32	011 0010	3	Two	2	
33	011 0011	4	Three	3	
34	011 0100	5	Four	4	
35	011 0101	6	Five	5	
36	011 0110	7	Six	6	
37	011 0111	8	Seven	7	
38	011 1000	9	Eight	8	
39	011 1001	10	Nine	9	
41	100 0001	11	Letter	A	
42	100 0010	12	Letter	B	
43	100 0011	13	Letter	C	
44	100 0100	14	Letter	D	
45	100 0101	15	Letter	E	
46	100 0110	16	Letter	F	
47	100 0111	17	Letter	G	
48	100 1000	18	Letter	H	
49	100 1001	19	Letter	I	
4A	100 1010	20	Letter	J	
4B	100 1011	21	Letter	K	
4C	100 1100	22	Letter	L	
4D	100 1101	23	Letter	M	
4E	100 1110	24	Letter	N	
4F	100 1111	25	Letter	O	
50	101 0000	26	Letter	P	
51	101 0001	27	Letter	Q	
52	101 0010	28	Letter	R	
53	101 0011	29	Letter	S	
54	101 0100	30	Letter	T	
55	101 0101	31	Letter	U	
56	101 0110	32	Letter	V	
57	101 0111	33	Letter	W	
58	101 1000	34	Letter	X	
59	101 1001	35	Letter	Y	
5A	101 1010	36	Letter	Z	
2E	101 1110	37	Period	.	
2D	101 1101	38	Hyphen	-	
2B	010 1011	39	Plus	+	
3D	011 1101	40	Equals	=	

TABLE 2. CHARACTER CODES (Cont'd)

ASCII CODE HEXIDECIMAL	7 BIT CODE b_6 ------ b_0	DRUM ROW	CHARACTER	ASCII SYMBOL	BCD SYMBOL
28	010 1000	41	Opening Parenthesis	(	
29	010 1001	42	Closing Parenthesis	)	
2F	010 1111	43	Slant	/	
2A	010 1010	44	Asterisk	*	
2C	010 1100	45	Comma	,	
27	010 0111	46	Apostrophe	'	
			(Not Equal)		$\neq$
24	010 0100	47	Dollar Sign	$	
3A	011 1010	48	Colon	:	
26	010 0110	49	Ampersand	&	
			(Less than or Equal)		$\leq$
25	010 0101	50	Percent	%	
5B	101 1011	51	Open Bracket	[	
5D	101 1101	52	Close Bracket	]	
40	100 0000	53	At Sign	@	
			(Arrow Right)		$\rightarrow$
5F	101 1111	54	Underline	—	
			(Identity		$=$
3F	011 1111	55	Question Mark	?	
			(Logical AND)		$\wedge$
21	010 0001	56	Exclamation Point	!	
			(Logical OR)		$\backslash$
22	010 0010	57	Quotation Mark	"	
			(Logical NOT)		—
23	010 0011	58	Number Sign	#	
			(Arrow Up)		$\uparrow$
5C	101 1100	59	Reversed Slash	\	
			(Arrow Down)		$\downarrow$
3E	011 1110	60	Greater Than	>	
3C	011 1100	61	Less Than	<	
5E	101 1110	62	Circumflex	$\wedge$	
			(Greater Than or Equal)		$\geq$
3B	011 1011	63	Semicolon	;	
20	010 0000	64	Space	Character is not printed. Used only for balance.	

MANUAL OPERATION

**Printer Switches
and Indicators**

POWER ON	START	SINGLE SPACE	PAPER OUT

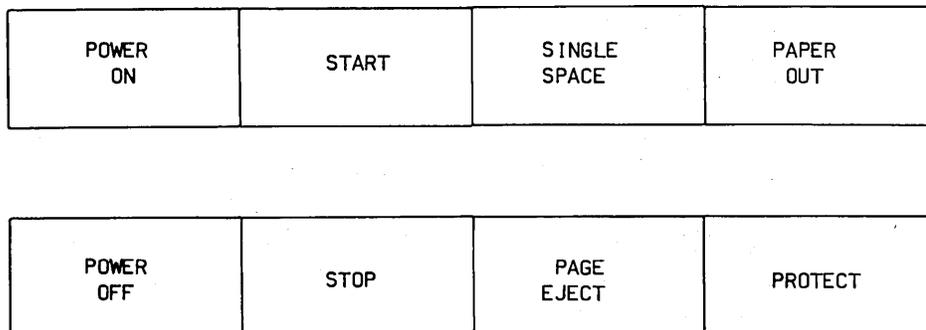| POWER OFF	STOP	PAGE EJECT	PROTECT

Figure 9. Printer Switches/Indicators

POWER ON Switch/Indicator

Pressing this alternate action switch causes power to be applied to all motors, fans, and power supplies in the proper sequence to prevent spurious print-out or paper advance. The indicator lights when power is applied to the equipment.

POWER OFF Switch

This momentary action switch, when pressed, removes power from the power supplies, motor, and fans.

START Switch/Indicator

Pressing this switch under normal conditions causes the printer to become Ready. When the printer is Ready the indicator lights.

This switch is also used during a Single Cycle operation. In this case, the switch allows the printer to print one additional line if a Paper Fault condition exists. This operation may be repeated until a punched hole is detected in Level 12 of the Format Tape, allowing the operator to complete the form which is being printed. After this, the Single Cycle operation is disabled until the Last Line of Form condition is corrected. If the Paper Fault condition results because of torn paper or a paper jam, the Single Cycle operation should not be used.

STOP Switch/Indicator

Pressing this switch causes the printer to become Not Ready. Pressing this switch during a print operation will inhibit printing after the line being printed is completed. The indicator lights when the printer is Not Ready.

SINGLE SPACE Switch

Pressing this switch causes the paper to advance one line.

Figure 10. CONTROL DATA 501 Line Printer

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PAGE EJECT Switch

Pressing this switch causes the paper to move to the top of the next form.

PAPER OUT Indicator

Lights to indicate a Paper Fault condition exists.

PROTECT Switch/Indicator

When this switch is pressed and the indicator is lighted, the printer is in the Protected condition.

Auxiliary Switches

The following auxiliary switches are located on the left rear side next to the paper exit. These are duplicate switches located for operator convenience.

    START

    STOP

    SPACE (SINGLE SPACE)

    PAGE (PAGE EJECT)

Controller Switches and Indicators

The controller switches and indicators (Figure 11) are located on a panel inside the cabinet.

START	STOP	SINGLE SPACE	PAGE EJECT	PROTECT

Figure 11. Controller Switches/Indicators

START Switch/Indicator

Pressing this switch under normal conditions causes the printer to become Ready. When the printer is Ready the indicator lights.

STOP Switch/ Indicator

Pressing this switch causes the printer to become Not Ready. Pressing this switch during a print operation inhibits printing after the line being printed is completed. The indicator lights when the printer is Not Ready.

SINGLE SPACE Switch

Pressing this switch causes the paper to advance one line.

PAGE EJECT Switch

Pressing this switch causes the paper to move to the top of the next form.

PROTECT Switch/Indicator

This indicator lights when the controller is in the protected condition. The protected or unprotected condition changes each time the switch is pressed.

Equipment Select Switches

The equipment number is selected by using these four double-pole, double-throw toggle switches. With these switches any one of 16 equipment codes may be selected for this unit (see Figure 2).

Maintenance Switches

The maintenance switches are nine toggle switches (Figure 12) which allow off-line adjustment and checking of the printer.
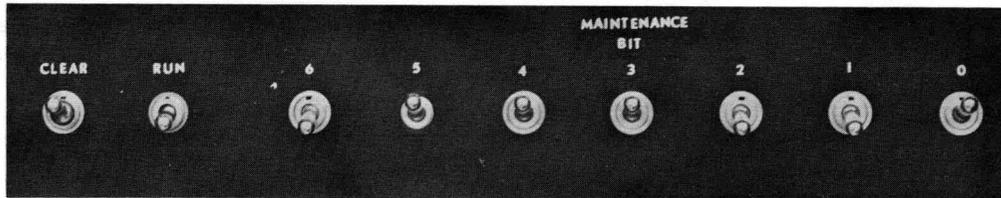
Figure 12. Maintenance Switches

BIT switches

By setting these seven toggle switches any one of the logical character codes may be selected.

RUN switch

This toggle switch may be used to select to print solid lines of the character selected by the BIT switches. The individual lines will be separated by a single space. With this switch in the Run position, the START and STOP switches are used to control the operation. The controller is logically separated from the computer when this switch is in the Run position.

CLEAR Switch

This is a spring loaded toggle switch which, when operated, sends a Master Clear to the controller logic. Operation of this switch causes the controller to clear and any operation in process is terminated.

COMMENT SHEET

MANUAL TITLE ___CONTROL DATA 1700 COMPUTER SYSTEM___

___Standard Peripheral Reference Manual___

PUBLICATION NO. ___60182700___ REVISION _____

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STAPLE   STAPLE

FOLD   FOLD
- -

FOLD   FOLD
- -

CUT ALONG LINE