CONTROL DATA® 1750

DATA AND CONTROL TERMINAL (DCT)

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
THEORY OF OPERATION
MAINTENANCE
DIAGRAMS AND PARTS LIST
WIRE LIST

CONTROL DATA
CORPORATION

HARDWARE REFERENCE/
CUSTOMER ENGINEERING MANUAL

1750 DATA AND CONTROL TERMINAL (DCT)

HARDWARE REFERENCE/
CUSTOMER ENGINEERING MANUAL

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INTRODUCTION

This manual contains logic diagrams, circuit descriptions, and programming information for the CONTROL DATA® * 1750 Data and Control Terminal (DCT). References are made in the text to Control Data manuals which describe invididual equipments in greater detail. Following is a list of Control Data publications that are applicable to the DCT.

1700 MAIN FRAME MANUALS

	Publication NO.
Input/Output Specification Manual	60165800
Computer Reference Manual	60153100
System Manual	60152900

1500 SERIES/MISCELLANEOUS PERIPHERAL MANUALS

1572 Programmable Sample Rate Generator	39070900
1573 Line Synchronized Timing Generator	39071000
1574 Sequential Addressing Unit	39073200
1577 Stall Alarm	84781600
DTL Intebrid® Logic	84785000

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Section One
GENERAL DESCRIPTION

1.1 GENERAL

The CONTROL DATA 1750 Data and Control Terminal (DCT) provides the control and interface to allow communication between the computer and CONTROL DATA® 1500 Series I/O Peripheral Equipment. If optional devices, such as the CONTROL DATA® 1574 Sequential Addressing Unit, 1572 Programmable Sample Rate Unit, 1573 Line Synchronized Timing Generator, and the 1577 Stall Alarm are used in the system, they are contained in the DCT module rack. Following are brief functional descriptions of these optional devices. Complete descriptions of the optional equipment can be found in their respective manuals. The remainder of this manual describes the DCT in detail.

1.2 OPERATIONAL DESCRIPTION

The Data and Control Terminal connects to a CONTROL DATA® 1705 Interrupt/Data Channel and provides a specialized interface for attaching industrial control and data acquisition equipment (see Figure 1.1). The DCT simplifies the logical decoding task of all devices attached to it by providing the following features which are time shared by all devices attached to the Data and Control Bus (DCB).

a. Computer Interface. The DCT provides party-line transmitters and receivers for all lines to the 1705 Interrupt/Data Channel, including transmitters for all 15 interrupt lines. (Refer to publication NO. 84785000 for details on party lines.)

b. Responses. All responses to Read and Write signals from the computer are predetermined by the DCT. No response is sent (resulting in an internal reject within the computer after a preset delay time of 4 microseconds) if the addressed device is not in the system or if it is too slow in acknowledging a data transfer. A Reject is sent if the addressed device is not ready. A Reply is sent only when the operation has been executed successfully.

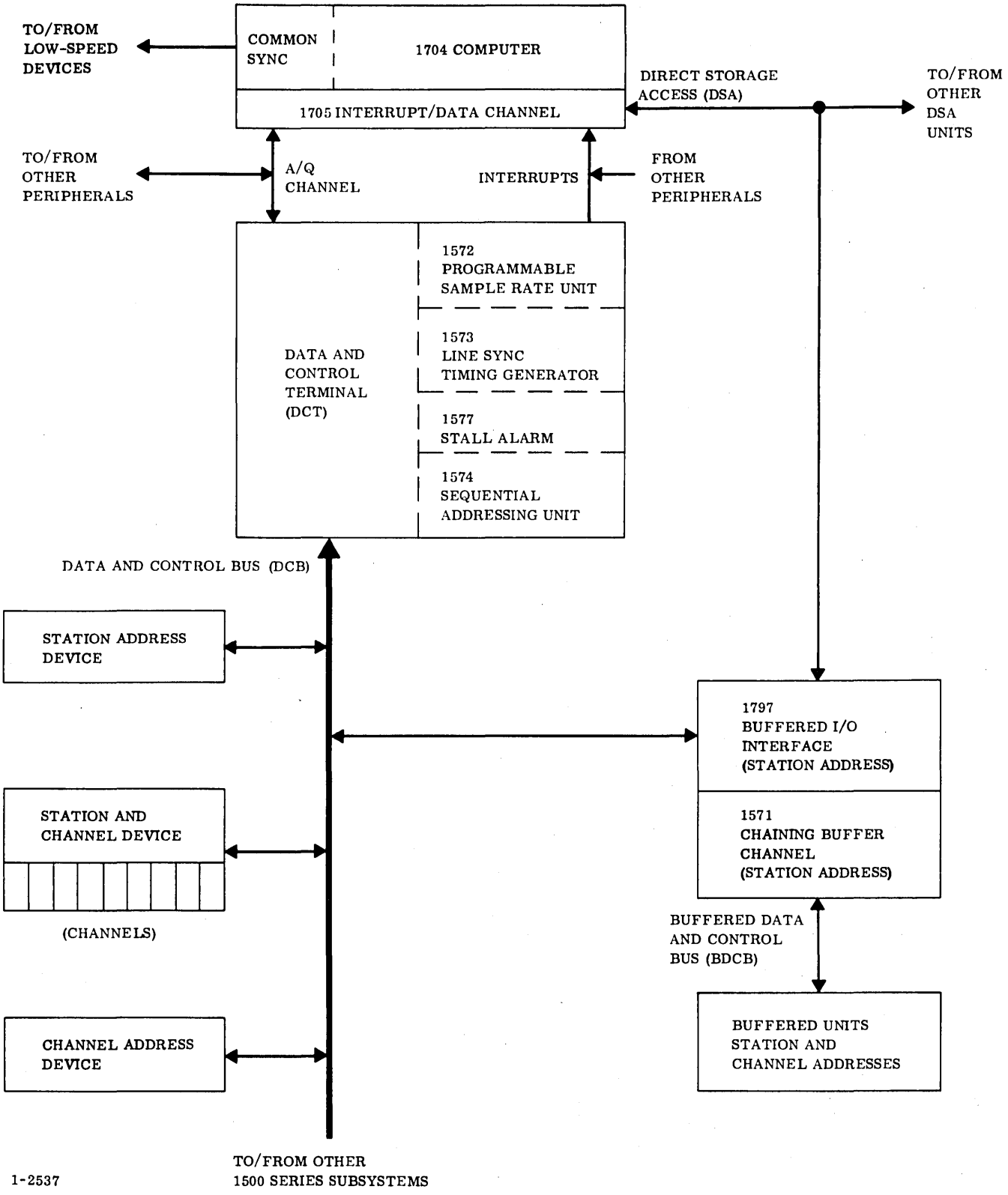


FIGURE 1.1. SYSTEM BLOCK DIAGRAM

1.2.1 Connect/Addressing Requirements

The DCT must be assigned an equipment number, usually Equipment NO. 8 or NO. 9. Equipment NO. 8 is for DCT NO. 1; Equipment NO. 9 is for DCT NO. 2. The DCT is also assigned station addresses (0 and 1). Each device attached to the DCT is assigned a station address and/or channel addresses. A Connect command, which includes the equipment number and a station address, must be sent by the computer. A Continue command is sent for channel addresses. Following are brief descriptions of an equipment, station, channel, Connect command, and Continue command.

a. Equipment. An equipment is any device which occupies a position on the 1705 from the CONTROL DATA® 1700 Computer. A maximum of eight equipments can be attached. A maximum of 16 addresses (0 through F) are available. (Refer to Table 1.1 for recommended equipment codes.)

b. Station. A station is contained within an equipment. Up to 128 station addresses are possible within the DCT. (Refer to Table 1.2 for recommended station assignments.)

c. Channel. A channel is contained within an equipment. (Refer to Table 1.3 for channel assignments.)

d. Connect command. Execution of the Connect command allows addressing of a specific equipment and a station within that equipment.

e. Continue command. Execution of Continue commands allows channel Read and Write instructions to be issued to channels within a specific equipment. (Refer to Section Two for Connect and Continue command formats.)

NOTE

The station and channel assignments in the following tables are recommended only.

The standard addresses listed in Tables 1.2 and 1.3 allow for a system equal to or less than the maximum listed in Table 1.4. Hardware restrictions may prevent these maximums from being realized. For systems exceeding the maximum in one or more areas, it is

TABLE 1.1. EQUIPMENT CODE ASSIGNMENTS

HEXADECIMAL EQUIPMENT CODES	DESCRIPTION
0	Unassigned
1	Low-Speed I/O Equipment (e.g., 1711, 1713, 1721, 1729)
2	1731 Magnetic Tape Controller
3	1751 Drum Interface/1738 Disk Pack Controller
4	1742 Line Printer
5	1749 Communications Terminal Controller
6	Remote I/O Controller NO. 2
7	Remote I/O Controller NO. 1
8	DCT NO. 1
9	DCT NO. 2
A	
B	
C	
D	
E	
F	

TABLE 1.2. DCT STATION ADDRESSES

STATION ADDRESS	EQUIPMENT ASSIGNED	INPUT COMMAND	OUTPUT COMMAND
00 (Fixed Address)	DCT	1750 Status	1750 Function
01 (Fixed Address)	DCT	System Status	Acknowledge Interrupt from 1573
02 (Fixed Address)	1572 Programmable Sample Rate Unit (1 device)		
03 (Fixed Address)	1572 Programmable Sample Rate Unit (1 device)		
04			
05			
06			
07			
08			
09	1577 Stall Alarm	Status	Function
0A	1575 Limit Comparison Unit (1 device)		
0B	1575 Limit Comparison Unit (1 device)		
0C	1575 Limit Comparison Unit (1 device)		
0D	1575 Limit Comparison Unit (1 device)		
0E			
0F			
10	1549 Interrupt Interface NO. 1 (00-15)	Status	Acknowledge Interrupt
11	1549 Interrupt Interface NO. 2 (00-15)	Status	Acknowledge Interrupt
12	1549 Interrupt Interface NO. 3 (00-15)	Status	Acknowledge Interrupt
13	1549 Interrupt Interface NO. 4 (00-15)	Status	Acknowledge Interrupt
14	1549 Interrupt Interface NO. 1 (00-15)	--	Set Mask
15	1549 Interrupt Interface NO. 2 (00-15)	--	Set Mask
16	1549 Interrupt Interface NO. 3 (00-15)	--	Set Mask
17	1549 Interrupt Interface NO. 4 (00-15)	--	Set Mask
18	1549 Interrupt Interface NO. 5 (00-15)	Status	Acknowledge Interrupt
19	1549 Interrupt Interface NO. 6 (00-15)	Status	Acknowledge Interrupt
1A	1549 Interrupt Interface NO. 7 (00-15)	Status	Acknowledge Interrupt
1B	1549 Interrupt Interface NO. 8 (00-15)	Status	Acknowledge Interrupt
1C	1549 Interrupt Interface NO. 5 (00-15)	--	Set Mask
1D	1549 Interrupt Interface NO. 6 (00-15)	--	Set Mask
1E	1549 Interrupt Interface NO. 7 (00-15)	--	Set Mask
1F	1549 Interrupt Interface NO. 8 (00-15)	--	Set Mask
20	1547 Event Counter Interface NO. 1 (0-F)	Status	Acknowledge Interrupt
21	1547 Event Counter Interface NO. 1 (0-F)	--	Set Mask
22	1547 Event Counter Interface NO. 2 (0-F)	Status	Acknowledge Interrupt
23	1547 Event Counter Interface NO. 2 (0-F)	--	Set Mask
24	1547 Event Counter Interface NO. 3 (0-F)	Status	Acknowledge Interrupt
25	1547 Event Counter Interface NO. 3 (0-F)	--	Set Mask
26	1547 Event Counter Interface NO. 4 (0-F)	Status	Acknowledge Interrupt
27	1547 Event Counter Interface NO. 4 (0-F)	--	Set Mask
28	1547 Event Counter Interface NO. 5 (0-F)	Status	Acknowledge Interrupt
29	1547 Event Counter Interface NO. 5 (0-F)	--	Set Mask

TABLE 1.2. DCT STATION ADDRESSES (Continued)

STATION ADDRESS	EQUIPMENT ASSIGNED	INPUT COMMAND	OUTPUT COMMAND
2A	1547 Event Counter Interface NO. 6 (0-F)	Status	Acknowledge Interrupt
2B	1547 Event Counter Interface NO. 6 (0-F)	--	Set Mask
2C	1547 Event Counter Interface NO. 7 (0-F)	Status	Acknowledge Interrupt
2D	1547 Event Counter Interface NO. 7 (0-F)	--	Set Mask
2E	1547 Event Counter Interface NO. 8 (0-F)	Status	Acknowledge Interrupt
2F	1547 Event Counter Interface NO. 8 (0-F)	--	Set Mask
30	1581/1583 Typewriter Interface NO. 1	Data	Data
31	1581/1583 Typewriter Interface NO. 1	Status	Function
32	1581/1583 Typewriter Interface NO. 2	Data	Data
33	1581/1583 Typewriter Interface NO. 2	Status	Function
34	1581/1583 Typewriter Interface NO. 3	Data	Data
35	1581/1583 Typewriter Interface NO. 3	Status	Function
36	1581/1583 Typewriter Interface NO. 4	Data	Data
37	1581/1583 Typewriter Interface NO. 4	Status	Function
38	1581/1583 Typewriter Interface NO. 5	Data	Data
39	1581/1583 Typewriter Interface NO. 5	Status	Function
3A	1581/1583 Typewriter Interface NO. 6	Data	Data
3B	1581/1583 Typewriter Interface NO. 6	Status	Function
3C	1581/1583 Typewriter Interface NO. 7	Data	Data
3D	1581/1583 Typewriter Interface NO. 7	Status	Function
3E	1581/1583 Typewriter Interface NO. 8	Data	Data
3F	1581/1583 Typewriter Interface NO. 8	Status	Function
40	1581/1583 Typewriter Interface NO. 9	Data	Data
41	1581/1583 Typewriter Interface NO. 9	Status	Function
42	1581/1583 Typewriter Interface NO. 10	Data	Data
43	1581/1583 Typewriter Interface NO. 10	Status	Function
44	1581/1583 Typewriter Interface NO. 11	Data	Data
45	1581/1583 Typewriter Interface NO. 11	Status	Function
46	1581/1583 Typewriter Interface NO. 12	Data	Data
47	1581/1583 Typewriter Interface NO. 12	Status	Function
48	1558 Latching Relay Output Interface (1024)	Status	Function
49	1558 Latching Relay Output Interface (1024)	Status	Function
4A	1558 Latching Relay Output Interface (1024)	Status	Function
4B	1558 Latching Relay Output Interface (1024)	Status	Function
4C	1558 Latching Relay Output Interface (1024)	Status	Function
4D	1558 Latching Relay Output Interface (1024)	Status	Function
4E	1538 High-Speed, High-Level Analog Input Interface NO. 1	Status	Function
4F	1538 High-Speed, High-Level Analog Input Interface NO. 2	Status	Function

TABLE 1.2. DCT STATION ADDRESSES (Continued)

STATION ADDRESS	EQUIPMENT ASSIGNED	INPUT COMMAND	OUTPUT COMMAND
50	1538 High-Speed, High-Level Analog Input Interface NO. 3	Status	Function
51	1538 High-Speed, High-Level Analog Input Interface NO. 4	Status	Function
52	1561 High-Speed Analog Output Interface NO. 1	Status	Function
53	1561 High-Speed Analog Output Interface NO. 2	Status	Function
54	1561 High-Speed Analog Output Interface NO. 3	Status	Function
55	1561 High-Speed Analog Output Interface NO. 4	Status	Function
56	1530A, 1530B, or 1534 NO. 1 Analog Input Interface (1024/256)	Status	Function
57	1530A, 1530B, or 1534 NO. 2 Analog Input Interface (1024/256)	Status	Function
58	1530A, 1530B, or 1534 NO. 3 Analog Input Interface (1024/256)	Status	Function
59	1530A, 1530B, or 1534 NO. 3 Analog Input Interface (1024/256)	Status	Function
5A	160A I/O Channel NO. 1	Status	Function
5B	160A I/O Channel NO. 2	Status	Function
5C			
5D			
5E			
5F			
60	1797 Buffered I/O Interface NO. 1	Status	Start
61	1797 Buffered I/O Interface NO. 2	Status	Start
62	1797 Buffered I/O Interface NO. 3	Status	Start
63	1797 Buffered I/O Interface NO. 4	Status	Start
64	1797 Buffered I/O Interface NO. 5	Status	Start
65	1797 Buffered I/O Interface NO. 6	Status	Start
66	1797 Buffered I/O Interface NO. 7	Status	Start
67	1797 Buffered I/O Interface NO. 8	Status	Start
68	1797 Buffered I/O Interface NO. 1	Next Address	Function
69	1797 Buffered I/O Interface NO. 2	Next Address	Function
6A	1797 Buffered I/O Interface NO. 3	Next Address	Function
6B	1797 Buffered I/O Interface NO. 4	Next Address	Function
6C	1797 Buffered I/O Interface NO. 5	Next Address	Function
6D	1797 Buffered I/O Interface NO. 6	Next Address	Function
6E	1797 Buffered I/O Interface NO. 7	Next Address	Function
6F	1797 Buffered I/O Interface NO. 8	Next Address	Function
70 ↕ 7F	No Address Commands ↕ No Address Commands		

TABLE 1.3. CHANNEL ADDRESSES

CHANNEL ADDRESS	EQUIPMENT ASSIGNED
	DIGITAL
000-OFF (R)	1544 Digital Input Interface: 256 words (16 controllers with 16 words each) = 4096 bits
000-07F (W)	1553 External Register Output Interface: 128 words (8 words per controller) = 128 DAC's or 2048 contact closure outputs less 2 words for each digital display
080-1FF (W)	1558 Latching Relay Output Interface: 384 words (64 words per controller) = 384 DAC's or 6144 contact closure outputs. Each DAC relay module (16 DAC's) requires 16 words, and each contact closure relay module (128 contact closures) requires 8 words even if the modules are partially filled. Assign the least significant addresses to the DAC's.
200-27F (R & W)	1547 Event Counter Interface: 16 counters per controller for 8 controllers = 128 counters
3FE	Not Assigned
3FF (R & W)	160A I/O Channel
100-1FF (R)	Not Assigned (256)
280-3FD (R & W)	Not Assigned (382)

TABLE 1.3. CHANNEL ADDRESSES (Continued)

CHANNEL ADDRESS	EQUIPMENT ASSIGNED
	LOW-SPEED ANALOG
800-BFF	1530A, 1530B, or 1534 Analog Input Interface NO. 1: (1024 points) 256 or 1024 per controller
C00-FFF	1530A, 1530B, or 1534 Analog Input Interface NO. 2: (1024 points) 256 or 1024 per controller
	HIGH-SPEED ANALOG
400-7FF (R)	1538 High-Speed, High-Level Analog Input Interface: (1024 points) 256 per controller
400-7FF (W)	1561 High-Speed Analog Output Interface: (1024 points) 256 per controller for 4 controllers = 1024

TABLE 1.4. MAXIMUM DCT STATION AND CHANNEL ASSIGNMENTS

QUANTITY	EQUIPMENT
4096	Digital inputs
6144	Latching contact closure outputs or 384 latching DAC outputs or a combination
2048	External register relay outputs or 128 DAC outputs less two words/digital display or a combination
128	Event counters
128	External interrupts
12	I/O typewriters
2048	Analog input relay multiplexer channels
1024	1538 High-Speed, High-Level Analog Input Interface channels
1024	1561 High-Speed DAC Output Interfaces
1	1577 Stall Alarm
1	1573 Limit Comparison Unit (optional)
1	1572 Programmable Sample Rate Unit (optional)
1	1797 Buffered I/O Interface
2	160A I/O Channels
10	Unassigned station addresses
382	Unassigned channel addresses

recommended that additional devices be assigned in the unassigned areas, even though addresses for a particular class of equipment may not be contiguous.

All responses to Read or Write signals from the computer through the 1705/DCT interface are controlled by the response control logic of the DCT. Conditions existing either at the DCT or at devices connected to the Data and Control Bus (DCB), determine the response to the Read or Write signal. The response conditions are arranged in Table 1.5 in order of precedence. The condition with the highest order of precedence determines the response, and all lower precedence conditions are ignored.

A device must be installed in the system (Here) and available (Ready) at the time of receipt of a Read or Write command. If either of these conditions is not established at the start of a Read or Write pulse or if a protect fault exists, the command is not executed. The device acknowledges receipt of the Read or Write execute signal from the DCT by dropping its ready line. If the ready line does not drop within 2 microseconds after the leading edge of the Read or Write pulse, no response is sent to the computer.

If the computer receives a Reply or a Reject or if no response has been received prior to the end of the Internal Reject delay time, the computer drops the Read or Write Ready input to the DCT and the response logic is cleared allowing the response control logic of the DCT to reset to the Ready state for the next input/output command. Timing of responses is determined by fixed delays with the response control logic. The basic response timing is summarized in Figure 1.2.

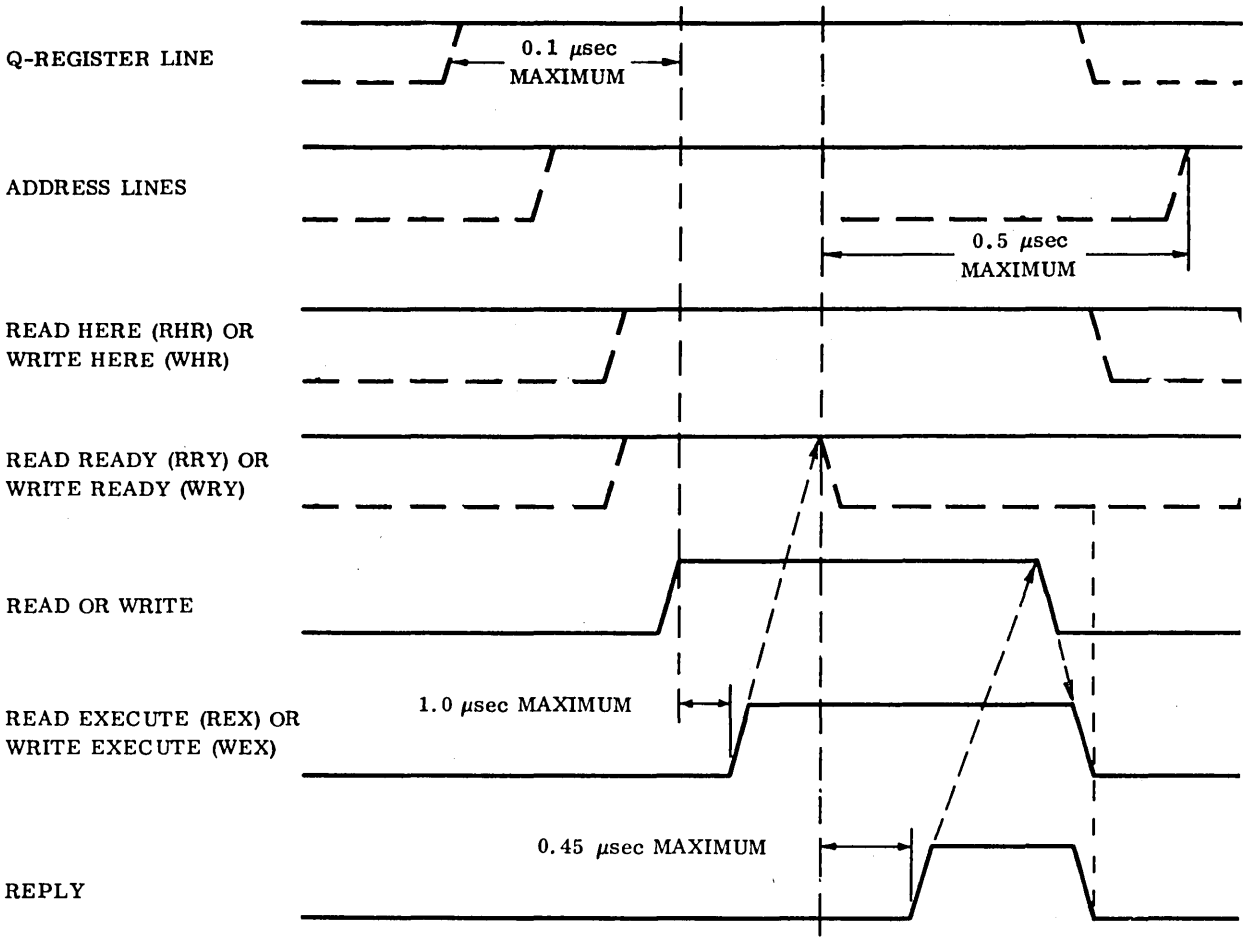
1.2.2 Addressing

All addresses are partially decoded in the DCT for easy recognition by connected devices. The Address Decoder is designed to decode the least significant bits (Q0 through Q11) of the address; this is done by binary decoding of the bits, two at a time, to form four addressing signals for each two bits. If the 1574 Sequential Addressing Unit is installed, the Address Decoder (Card 22) must be removed. The 1574 can be instructed to increment the address

TABLE 1.5 RESPONSE CONDITIONS

PRECEDENCE	CONDITION	RESPONSE
1	Not connected and not a Connect command	None
2a	Unprotected command and PROTECT switch in position 2	Reject
2b	Unprotected command and PROTECT switch in position 3	Reply and Interrupt
3a	Addressed device Here and Ready:	
	Generate REX or WEX and wait 2 μsec from leading edge of Read or Write, then:	
	If Ready drops in time and RJT is false	Reply
	If Ready drops in time and RJT is true	Reject
	If Ready does not drop in time	None
3b	Addressed device Here but not Ready	Reject
3c	Addressed device not Here	None
4	1574 Sequential Addressing Unit not in system:	
	Sequential Setup or Sequential Status command	None
	Random Address command in mode 2 or 3	Reject
	Any No-Address command	Reject
5a	Station Address 00 and Write (set DCT functions)	Reply
5b	Station Address 00 and Read (present DCT status)	Reply
5c	Station Address 01 and Write (1573 Line Synchronized Timing Generator):	
	If 1573 not in system	None
	If 1573 interrupt sent	Reply
	If 1573 interrupt not sent	Reject
5d	Station Address 01 and Read (present system status)	Reply

NOTE: Cases 4 and 5 are special cases of 3.



NOTES:

A REJECT IS SENT INSTEAD OF A REPLY IF RJT IS TRUE WHEN READY DROPS.

A REJECT IS SENT INSTEAD OF AN EXECUTE IF THE ADDRESSED DEVICE IS HERE AND NOT READY.

NO RESPONSE IS SENT IF THE ADDRESSED DEVICE IS NOT HERE.

NO RESPONSE IS SENT IF READY DOES NOT DROP IN TIME (WITHIN 4.0 μSEC OF READ OR WRITE).

ADDRESS BEING INCREMENTED FOR SEQUENTIAL OPERATION (NO-ADDRESS COMMAND ONLY).

1-1347B

FIGURE 1.2. RESPONSE TIMING DIAGRAM

after each data transfer and to cycle repeatedly between programmed first and last addresses. The CONTROL DATA® 1797 Buffered I/O Interface/1571 Chaining Buffer Channel system (optional equipment) contains its own incrementing logic. A brief description of these options can be found at the end of this section.

1.2.3 Interrupt Lines

Fifteen interrupt lines are available for use by the DCT and all devices connected to the DCB. The priority of the interrupt lines is controlled by the computer program by use of the interrupt mask. The interrupt line(s) of any device can be connected to any interrupt line (01 through 15) by proper installation of jumpers on the interrupt plugboard of the device. No control or inhibit of the interrupts from devices connected to the DCB is maintained by the DCT, except for the interrupt status of the DCT. Provision for jumpering interrupts from options housed in the DCT module (refer to Section Three) is available on card position 5.

The basic 1705 Interrupt/Data Channel transfers the address information to the DCT on the Q-register lines and inputs or outputs data on the A-register lines. Data is input or output upon Read or Write commands issued by the computer on the A-Read or A-Write lines, respectively.

Table 1.6 lists the recommended line assignments. These assignments may be changed to meet particular system requirements.

1.2.4 Program Protect

The DCT and all other devices connected to the DCT contain a three-position PROTECT switch. The switch positions are labeled and function as follows:

a. OFF (Position 1). The Program Protect bit is ignored, no protect faults are recognized, and the Program Protect status bit is false.

b. REJECT (Position 2). A Reject signal is transmitted if the command is not protected, and the faulting command is not executed.

TABLE 1.6. INTERRUPT LINE ASSIGNMENTS

INTERRUPT LINE NUMBER	EQUIPMENT
0	Memory Protect/Parity
1	Low-Speed I/O
2	1573 Line Synchronized Timing Generator
3	1731 Magnetic Tape Controller
4	1751 Drum Interface/1738 Disk Pack Controller
5	1749 Communications Terminal Controller
6	1584 I/O Typewriter
7	1545 Digital Input Sync Unit
8	1530/1534 Analog Input Interface
9	1558 Latching Relay Output Interface
10	1547 Event Counter Interface
11	Unassigned
12	Unassigned
13	Unassigned
14	Unassigned
15	Unassigned

c. INTERRUPT (Position 3). A Reply signal is transmitted if the command is not protected, but the faulting command is not executed, and the interrupt output becomes true.

1.3 OPTIONS

The DCT module provides space for the addition of up to three optional units. While these do not form a part of the DCT itself, they occupy the same module as the DCT. The units are the 1574 Sequential Addressing Unit, 1572 Programmable Sample Rate Unit, 1573 Line Synchronized Timing Generator, and the 1577 Stall Alarm.

1.3.1 1574 Sequential Addressing Unit

This unit provides automatic scanning of channel addressing and is an alternate replacement unit for the Address Decoder. The 1574 and the Address Decoder are controlled by common signals and perform similar, but not identical, functions; they cannot both be used with the same DCT. The 1574 must be provided with a first channel address (FCA) and a last channel address plus one (LCA), which are specified by the program. A counter in the 1574 starts at the first channel address and is successively incremented until the last channel address is reached. The counter then recycles, starting again at the first channel address.

Random Address commands can be executed to sample a single address without disturbing the sequence, and a sequence can be modified to skip or repeat a group of channels at any time under the program control.

1.3.2 1572 Programmable Sample Rate Unit

The 1572 Programmable Sample Rate Unit can be operated either as an elapsed-time accumulator or as an interval generator. In the Elapsed-Time mode, it accumulates counts from a time base, and the counter is examined under program control. In the Interval mode, the program specifies a count value, and the 1572 accumulates the time base until the specified count value is reached; at this point an interrupt is generated.

A timing signal is also generated and distributed to the peripherals via the DCB. The 1572 obtains its time base from the 1573 Line Synchronized Timing Generator, a self-contained oscillator, or an external source.

1.3.3 1573 Line Synchronized Timing Generator

The 1573 Line Synchronized Timing Generator provides a timing pulse output and interrupts at selectable frequencies between 60 Hz and 7680 Hz that are multiples of and synchronous with the 60 Hz power line. The interrupt can be used to initiate computer programs. The timing pulse can be used by the 1572 Programmable Sample Rate Unit or by other peripheral devices.

1.3.4 1577 Stall Alarm

The 1577 Stall Alarm detects system malfunctions caused by nonterminating loops or similar errors in the computer program; it also detects power failures. The stall alarm contains a "watchdog timer" that must be periodically reset by the computer program by means of a function command. If the program fails to reset the timer within a given period, the 1577 produces a Stall condition. A Stall condition causes a computer interrupt, actuates an audible alarm, produces a contact closure for controlling external equipment, and may inhibit further data transfers to some of the I/O systems. In the case of a power failure, the 1577 causes an interrupt to inform the computer of the failure.

1.4 SYSTEM OPTIONS

The 1571 Chaining Buffer Channel is a system option that is used in conjunction with the 1797 Buffered I/O Interface. The 1571 is similar to the 1574 Sequential Addressing Unit in that it also provides automatic sequential channel addressing. The 1571, however, can be operated in a Buffered or Nonbuffered mode. The Buffered mode is via the Direct Storage Access (DSA) bus, and the Nonbuffered mode is via the A/Q channel and the DCB. If a 1571 is used in the system, a 1574 is not used.

1.5 PHYSICAL DESCRIPTION

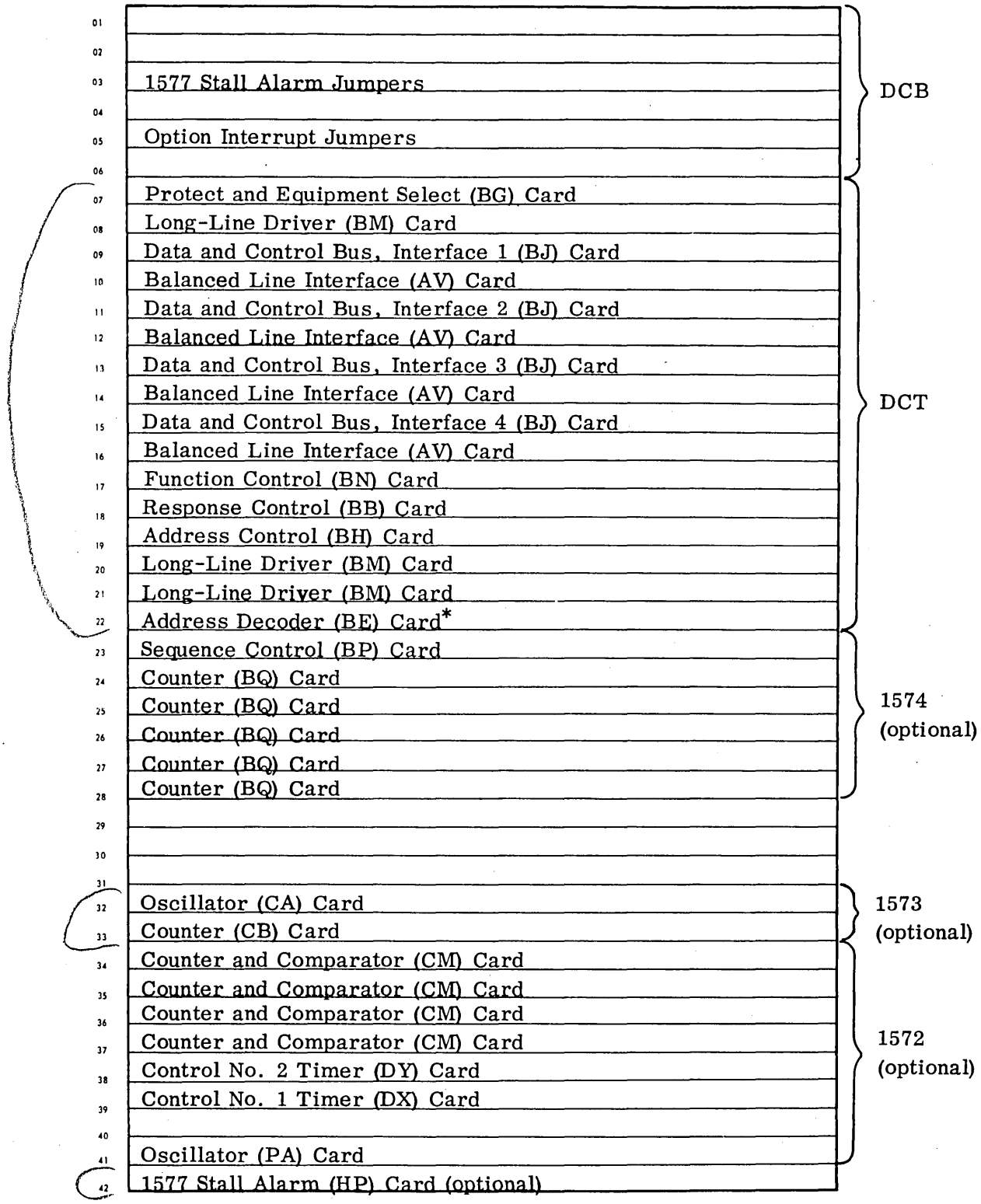
1.5.1 General

The DCT is contained within a standard Control Data 19-inch module. The module provides connectors and card guides for the DCT and for the following additional logic units (see Figure 1.3 for a card position diagram):

a. Address Decoder (standard for the DCT).
b. 1572 Programmable Sample Rate Unit.
c. 1573 Line Synchronized Timing Generator.
d. 1574 Sequential Addressing Unit.
e. 1577 Stall Alarm.

The card connectors are numbered from left to right, 01-42, as viewed from the front of the module. The connector pins are numbered from top to bottom, 01-50. Assignment and wiring of the connectors for the units listed above are as follows:

a. Connectors 02, 04, 06	Used as cable connectors for the DCT (DCB).
b. Connector 05	Used to jumper interrupts from within DCT module to desired interrupt lines.
c. Connectors 07-21	Contain the DCT logic cards.
d. Connector 22	Contains the Address Decoder card (if used).
e. Connectors 23-28	Contain the 1574 Sequential Addressing Unit (if used).
f. Connectors 29-31	Spare connectors.
g. Connectors 32-33	Contain the 1573 Line Synchronized Timing Generator (if used).
h. Connectors 34-39	Contain the 1572 Programmable Sample Rate Unit (if used).
i. Connector 40	Spare connector.
j. Connector 41	Oscillator card (1572).
k. Connector 42	Contains stall alarm logic.



* Remove Card 22 before installing a 1574 unit.

FIGURE 1.3. CARD LOCATION DIAGRAM

1.5.2 Dimensions

Width	Standard 19-inch RETMA relay rack mounting
Height	Standard 7-inch RETMA relay panel
Depth	16 inches
Weight	35 pounds

1.5.3 Cooling

Cooling for the module is provided by fans mounted in the rack. All operating specifications are met with an ambient air temperature of 40°F. to 120°F. and a relative humidity of 0 percent to 95 percent excluding conditions where condensation takes place in and on the equipment in the form of water and/or frost.

1.6 ELECTRICAL REQUIREMENTS

1.6.1 Power

Two integral power supplies are included in the module. Primary power to these supplies is 208V, 3-phase, 400-Hz which is provided by a self-contained MG set or is customer supplied. Power supplied to the printed circuit cards is ground, +6 volts, and -6 volts. The +6 VDC and ground lines are distributed by bus bars. The -6 VDC is wired from connector to connector using wire-wrap techniques. The back plane (chassis) is also used for ground, and pins 2 and 50 of each connector are connected directly to the ground plane. Supplied by a cable from the computer is ±20 volt terminator power for the computer interface.

1.6.2 Logic Levels

Logic levels within the DCT are as follows:

False or "0" = +0.9 to +1.1 VDC

True or "1" = +1.8 to +3.0 VDC (nominal)

Section Two
OPERATION AND PROGRAMMING

2.1 GENERAL

The Data and Control Terminal is programmed using the Input-to-A and Output-from-A commands. For the programming descriptions following, it is assumed that the programmer is familiar with CONTROL DATA 1700 Computer System programming formats and all general 1700 programming procedures. For further information on programming, refer to the CONTROL DATA 1700 Computer Reference Manual and System Manual.

2.2 DATA TRANSFER OPERATIONS

There are four types of data transfer operations: digital output, digital input, analog output, and analog input. Any of these can be executed using Random Address commands or, if the 1574 Sequential Addressing Unit is present, No Address commands can be used.

2.2.1 Digital Output

A digital output consists of transferring one 16-bit word which can be used as a binary quantity, in the form of 16 discrete "0" or "1" values or any combination thereof. The combination is determined only by the output's use by equipment external to this system. The 16 bits are usually stored in flip-flops or relays in a digital output unit or in external equipment.

2.2.2 Digital Input

A digital input can be any combination of binary values and discrete bits making up the 16-bit word. Each bit or group of bits meaning is determined only by the source of information.

2.2.3 Analog Output

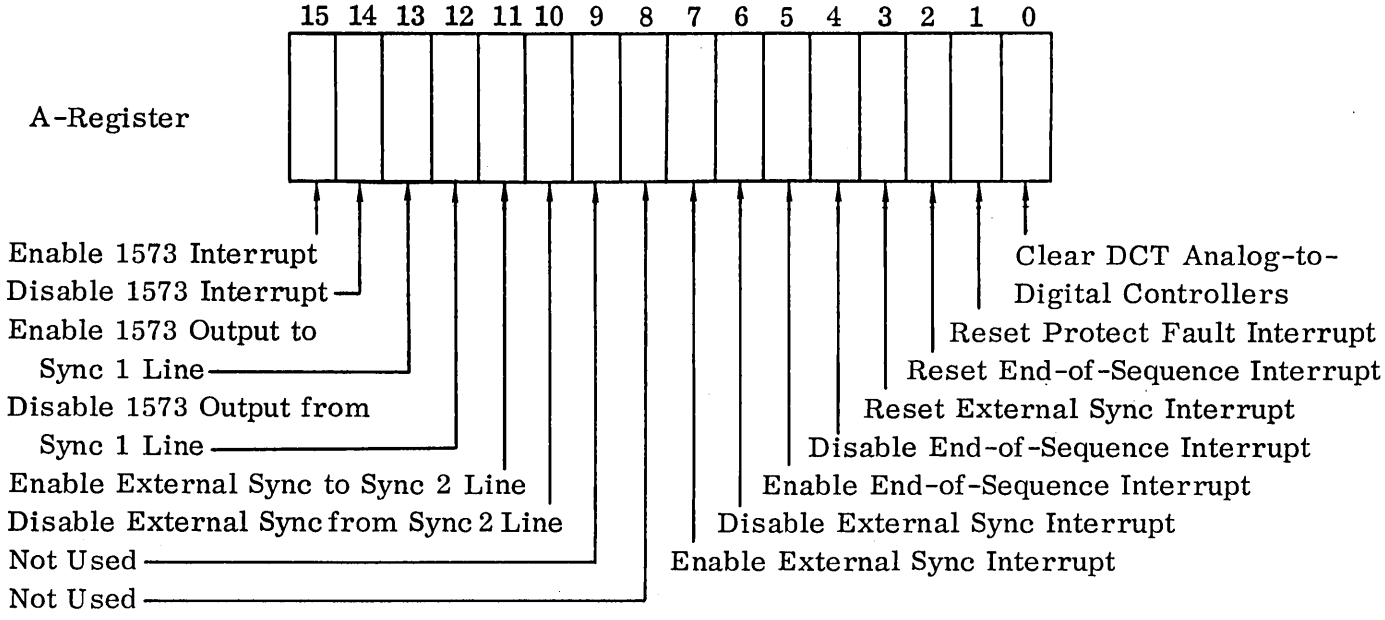
An analog output is similar to a digital output, except that the significant bits are stored in the holding register of a digital-to-analog converter. The command is rejected if a conversion is in progress at the time.

2.2.4 Analog Input

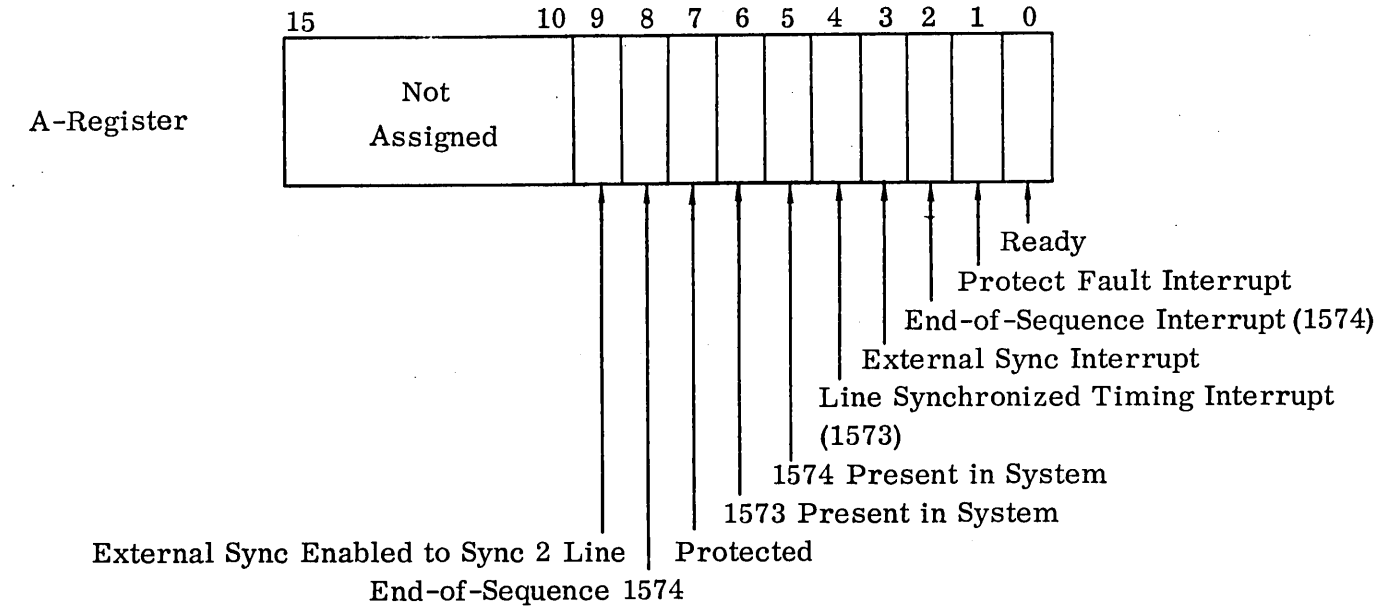
Analog input operations require more sophisticated programming techniques because an analog-to-digital (A/D) conversion takes longer than the 4 microseconds allowed by the computer. The data transferred when an analog input command is executed is the result of the previous A/D conversion. The command is rejected if a conversion is in progress at the time. Another A/D conversion is started at the specified address except when the input command is a Random Address command with mode equal to "0" or a No-Address command with a "1" in bit 0.

2.3 COMMAND FORMATS

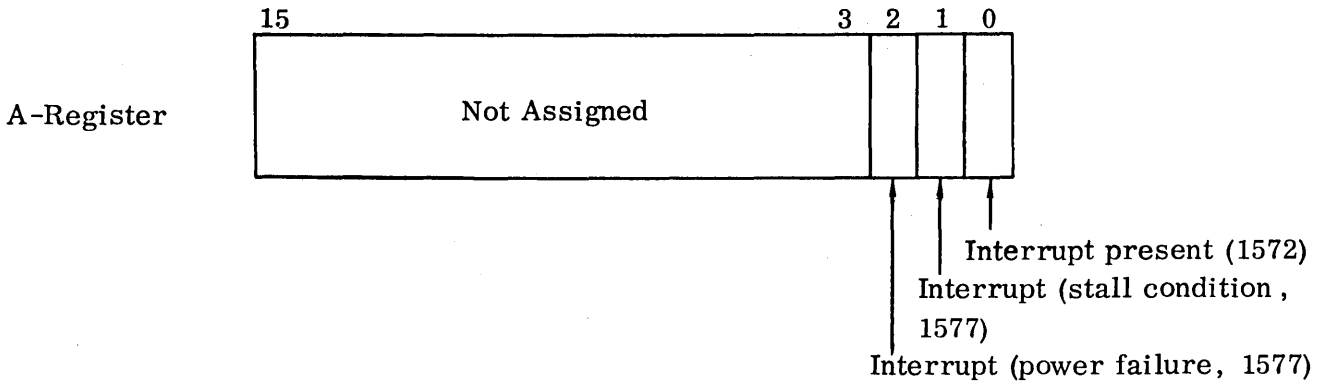
In general, command formats recognized by the DCT are analogous to those used by other equipments connected to the computer (refer to the Computer Reference Manual). Accordingly, four command formats are possible on the A/Q channel, i.e., Connect/Function, Status and Connect, Data Transfer, and Sequential Operations. The function and status bit assignments for the DCT and associated equipment are summarized below.



FUNCTION WORD BIT ASSIGNMENTS (STATION 00 OUTPUT)



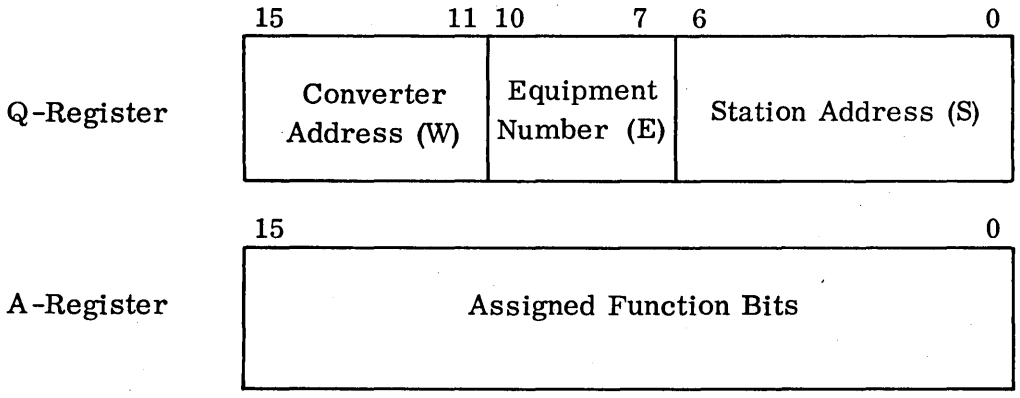
STATUS WORD BIT ASSIGNMENTS (STATION 00 INPUT)



STATUS WORD BIT ASSIGNMENTS (STATION 01 INPUT)

2.3.1 Connect/Function Commands

When the contents of the Q-register conform to the format for a Connect command as shown below, the contents of the A-register control the functions of the DCT. For Function and Connect commands, the W-field must be "0", and the station address must be "0" to address the DCT. The E-field must contain the equipment number of the DCT. The DCT contains a thumbwheel switch for setting the equipment number (usually set to equipment NO. 8 for DCT NO. 1 and equipment NO. 9 for DCT NO. 2). When an Output-from-A command is executed under these conditions, Function and Connect command is executed.



CONNECT/FUNCTION COMMAND FORMAT

When the Connect/Function command is executed, the equipment number in the E-field sets the Connect flip-flop in the DCT and connects the DCT to the computer. A data transfer cannot take place unless the DCT is connected. The Connect flip-flop stays set regardless of the number of new Connect commands as long as the E-field contains the equipment number of the DCT (8 or 9) and the station address is for the DCT or one of the attached devices. The Connect flip-flop is reset by any Connect command addressed to an equipment other than the DCT. The Connect flip-flop is not reset by a clear function.

When the computer executes the Output-from-A instruction, the bits in the A-register control the functions of the addressed station. Refer to the appropriate module manuals for function bit assignments.

STATION ADDRESSES

Bits 0 through 6 of a Connect command are defined as a station address. Station addresses are used to communicate with subsystem interfaces and other devices connected directly to the DCT. Station address 00 is reserved for commands (function and status) directed to the DCT itself.

Execution of an input to station 01 is used to input status from the 1572 and 1577. Execution of an output to station address 01 is used to acknowledge an interrupt from the 1573. The A-register is not used for this operation. No response is sent if the 1573 is not present. A Reply is sent if the 1573 is present, has sent an interrupt, and the interrupt is reset. A Reject is sent if the 1573 is present but has not sent an interrupt.

Station addresses 02 and 03 are reserved for use by the 1572 option within the DCT module. Station addresses 60 through 6F (hexadecimal) are reserved for use by devices connected to the 1797 Buffered I/O Interface.

The values 70 through 7F are not allowed as station addresses because of the restriction that a command with a "1" in bits 4, 5, and 6 is a No Address Data Transfer command.

The remaining 92 station addresses, 04 through 5F (hexadecimal), are reserved for assignment to individual stations connected to the DCT.

FUNCTION CODES

Clear DCT Analog-to-Digital Subsystems Controller (A0 = "1")

This code clears all interrupt selections and signals, error indications, and other clearable conditions. It cannot be used in conjunction with other function codes. This is the same as a Master Clear, except that the DCT is connected.

Clear Protect Fault Interrupt (A1 = "1")

This code clears the interrupt signal generated by a protect fault. The code can be used in conjunction with other function codes. This interrupt can also be reset by clearing the controller or by a Master Clear.

Clear End-of-Sequence Interrupt (A2 = "1")

This code clears the interrupt signal generated by the completion of a sequential addressing operation by the 1574 option. This interrupt can also be reset by clearing the controller or by a Master Clear.

Clear External Sync Interrupt (A3 = "1")

This code clears the interrupt received from an external synchronizing source.

Disable End-of-Sequence Interrupt (A4 = "1")

This code disables the interrupt sent by the 1574 upon completion of an addressing sequence. The interrupt is prevented from reaching the computer, but bit 8 of the DCT status is set by End of Sequence.

Enable End-of-Sequence Interrupt (A5 = "1")

This code enables the interrupt sent by the 1574 at the end of a sequence. The interrupt is sent to the computer, and bits 2 and 8 of the DCT status are set.

Disable External Synchronizing Interrupt (A6 = "1")

This code disables the interrupt sent by an external synchronizing source. The interrupt is prevented from reaching the computer, but bit 3 of the DCT status is set.

Enable External Synchronizing Interrupt (A7 = "1")

This code enables the interrupt generated by an external synchronizing source. The interrupt is sent to the computer, bit 3 of the DCT status is set, and a signal may or may not be sent on the SYNC2 line of the DCB depending on whether or not that signal is enabled or disabled.

Disable External SYNC from SYNC2 Line (A10 = "1")

This code prevents the transmission of a signal received from an external synchronizing source to the SYNC2 line of the DCB.

Enable External SYNC to SYNC2 Line (A11 = "1")

This code enables an external sync signal to be transmitted on the SYNC2 line of the DCB.

Disable 1573 Output from SYNC1 Line (A12 = "1")

This code prevents the transmission of a signal received from a 1573 Line Synchronized Timing Generator to the SYNC1 line of the DCB.

Enable 1573 Output to SYNC1 Line (A13 = "1")

This code enables the signal from a 1573 to be transmitted on the SYNC1 line of the DCB.

Disable 1573 Interrupt (A14 = "1")

This code disables the interrupt sent by the 1573. The interrupt is prevented from reaching the computer, but bit 4 of the DCT status is set.

Enable 1573 Interrupt (A15 = "1")

This code enables the interrupt sent by the 1573. The interrupt is sent to the computer, and bit 4 of the DCT status is set.

2.3.2 Status and Connect

When the contents of the Q-register conform to the format for Function and Connect commands, the status of the DCT is loaded into the A-register when an Input-to-A command is executed. For Status and Connect commands, the W-field must be 00, the station must be 00, and the E-field must contain the equipment number of the DCT.

Execution of this command connects the DCT to the computer.

If station address bits are present when the computer executes the Input-to-A instruction, the status of the addressed station is loaded into the A-register. Refer to the appropriate manuals for status word bit assignments for particular units (stations).

STATUS CODES (STATION 00)

DCT Ready (A0 = "1")

The DCT is always Ready, i.e., any allowable operation can be performed on request, except while being reset by a Master Clear. Thus, this bit is always set in the status word except when the MASTER CLEAR button on the DCT is depressed.

Protect Fault Interrupt (A1 = "1")

Bit A1 is set whenever an unprotected I/O command is received by the DCT and the PROTECT switch is in position 3. An interrupt is generated and a Reply is sent; however, no other action is taken. This bit is cleared when the interrupt signal is cleared.

End-of-Sequence Interrupt (A2 = "1")

Bit A2 is set when the 1574 has generated an interrupt upon completion of an addressing sequence, the interrupt was enabled, and the interrupt has not been acknowledged.

External Sync Interrupt (A3 = "1")

Bit A3 is set when a synchronizing interrupt has been received by the DCT from an external sync source. Bits in the station 00 function word enable an external sync signal to cause an interrupt and/or cause the signal to be transmitted on the SYNC2 line of the DCB. The station 00 function word is also used to reset these interrupts.

Line Synchronized Timing Interrupt (A4 = "1")

Bit A4 is set when a synchronizing interrupt has been received by the DCT from the 1573 Line Synchronized Timing Generator. Bits in the DCT station 00 function word enable the 1573 to send interrupts and/or send a signal on the SYNC1 line of the DCB. A Write command at DCT station address 01 is used to acknowledge an interrupt from the 1573. (Bit A4 is present as a status bit regardless of whether the interrupt is enabled or disabled.)

1574 in the System (A5 = "1")

Bit A5 is set whenever a 1574 is connected to the DCT.

1573 in the System (A6 = "1")

Bit A6 is set whenever a 1573 is connected to the DCT.

Protected (A7 = "1")

This bit is set whenever the DCT's PROTECT switch is in position 2 or 3.

End of Sequence (A8 = "1")

Bit A8 is set when the 1574 is precisely at the end of an addressing sequence.

External Sync Enabled to SYNC2 Line (A9 = "1")

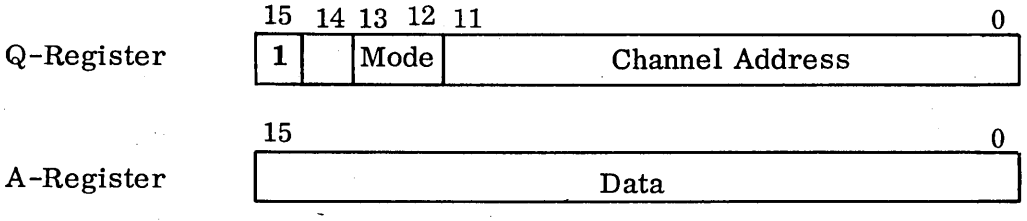
Bit A9 is set when the external synchronizing input has been connected to the SYNC2 line of the DCB. This bit is reset when the external sync is disabled from the SYNC2 line.

2.3.3 Data Transfer Commands

Data Transfer commands are used for Read or Write operations at specified channel addresses. The channel address may be specified in the command (Random Address) or it may have been previously set up (No Address commands) if a 1574 Sequential Addressing Unit is in the system.

DATA TRANSFER COMMAND FORMAT

The general format for data transfer commands is shown below. In Data Transfer command the Q-register contains a "1" in bit 15 and an Input-to-A or Output-from-A command is executed indicating the "connected" flip-flop of the DCT is set. If a Connect command has not been previously executed, the DCT does not respond and the computer generates an Internal Reject.



CHANNEL DATA TRANSFER COMMAND FORMAT

RANDOM ADDRESS COMMANDS

Random Address commands are Data Transfer commands with a "0" in bit 14. The channel address is always specified by bits 0 through 11 of the Q-register. Bits 12 and 13 specify 1 of 4 operating modes as follows:

a. Random Address Read Only (Mode = 00). This mode causes data to be read from the indicated channel without starting another conversion. The sequence of a sequential operation using the 1574 is not affected. No execute signal is generated in this mode.

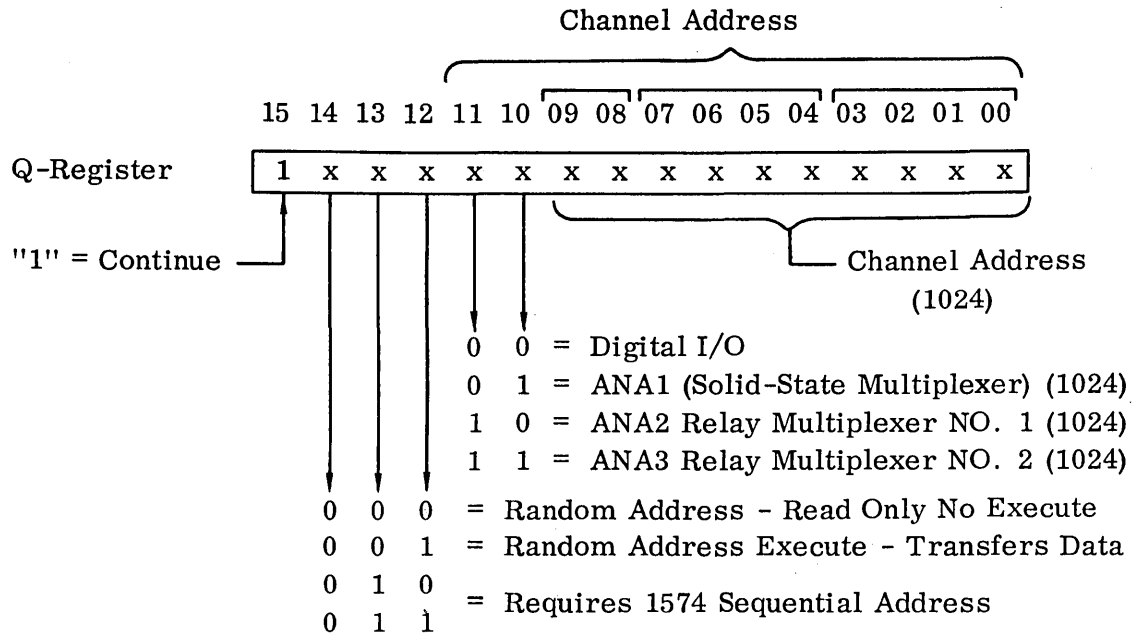
b. Random Address Execute (Mode = 01). This mode causes a data transfer to be executed at the specified channel. The sequence of a sequential operation using the 1574 is not affected.

c. Random Address and Lockup (Mode = 02). This mode is rejected if the 1574 is not present in the system. A data transfer is executed at the specified channel address and the next address in the sequence is set equal to the specified address.

d. Random Address and Increment (Mode = 03). This mode is rejected if the 1574 is not present in the system. A data transfer is executed at the specified channel address and the next address in the sequence is set equal to one greater than the specified address.

CHANNEL ADDRESSES

Bits 0 through 11 of a Data Transfer command are defined as a channel address. Channel addresses are used to communicate with units connected to the stations. Bits 10 and 11 of the channel address select the type of unit to be addressed as illustrated below.

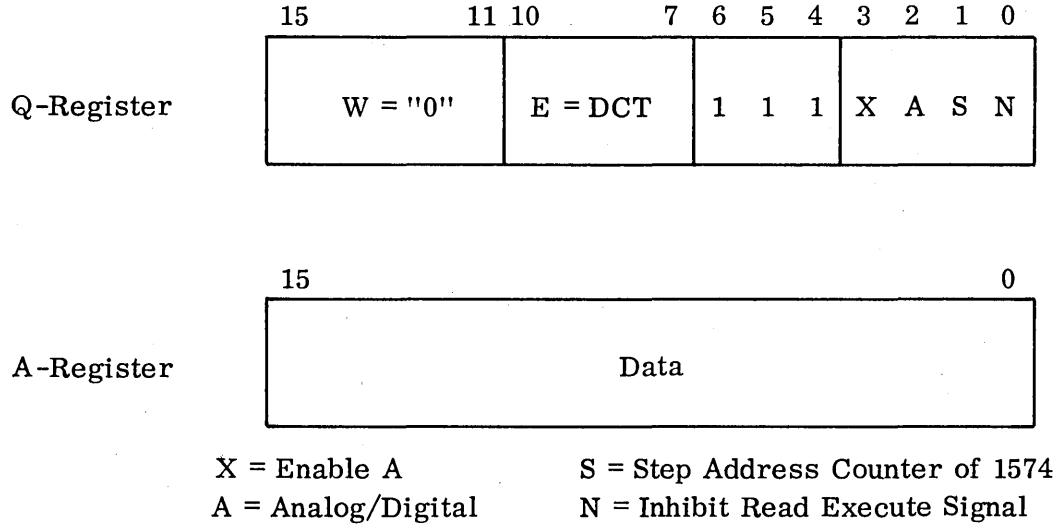


CHANNEL ADDRESS UNIT TYPE BIT ASSIGNMENTS

Unique channel addresses (bits 0-9) must be assigned to all channels connected to stations of the same type.

NO ADDRESS COMMANDS

As No Address command is a command with "1's" in bits 4, 5, and 6 as shown below.



NO ADDRESS DATA TRANSFER COMMAND FORMAT

Bits 0 through 3 specify special operating conditions. The channel address for sequential operations is controlled by the 1574 Sequential Addressing Unit; No Address commands are rejected if the 1574 is not in the system.

Bits 2 and 3 can be used to change from an analog channel to a digital channel of the same address or vice versa. No change is made if bit 3 is "0;" however, if bit 3 is "1," bit 2 is temporarily substituted for bit 10 of the address previously set up if bit 11 of that address is "0."

A "1" in bit 1 causes the channel address to be incremented after the data transfer.

Bit 0 indicates that the Read Execute signal should be inhibited. A No Address input command with a "1" in bit 0 may be used to read the result of an analog-to-digital conversion without starting another conversion. No response is sent to a No Address output command with a "1" in bit 0.

2.3.4 Sequential Operation Commands

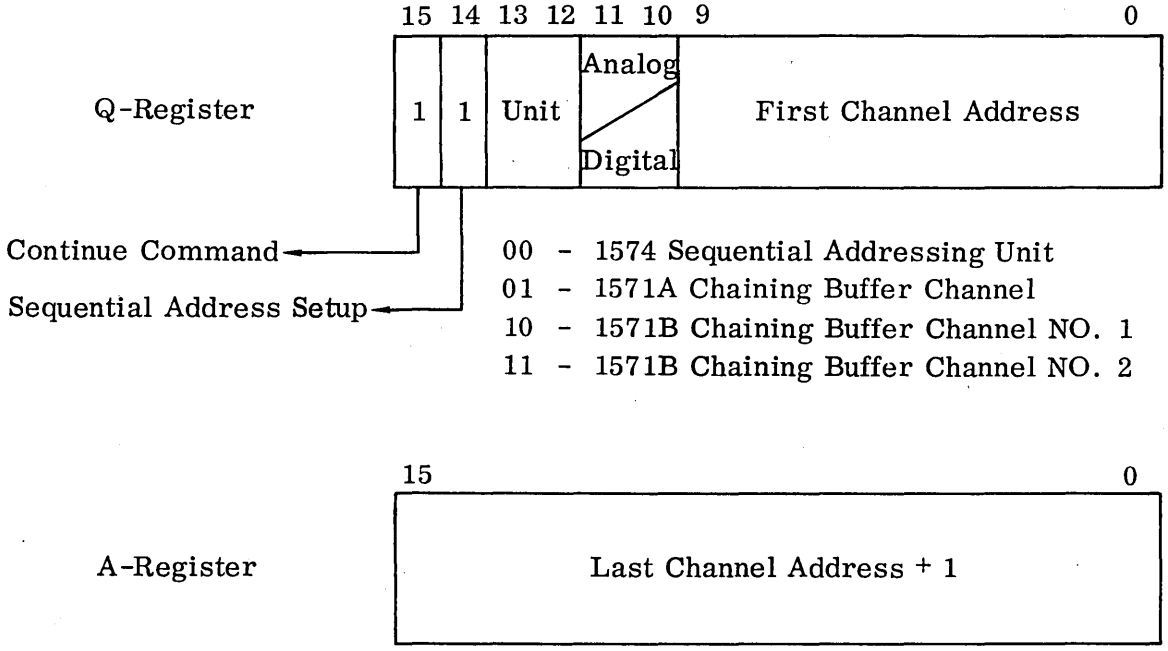
Sequential addressing operations are made possible by the 1574 Sequential Addressing Unit or the 1571 Chaining Buffer Channel. A reject is sent from the DCT when Sequential Operation commands are executed if a 1574 or 1571 is not in the system. The A-register is used for addresses instead of for function or status bits when Sequential Address commands are executed.

Sequential operations for data transfer are executed in the Direct mode using No Address commands (1574 only). The channel address may be incremented (for the 1574) on each data transfer or at selected times as desired. Incrementing of channel addresses using the 1571 is automatic after initial setup. Bits 10 and 11 of the channel address are never incremented since they are used to select the type of unit instead of for channel selection.

Random Address operations can be executed in modes zero or one without disturbing the sequence of a sequential operation. Random Address operations in modes two or three are used only by the 1574 and can be used to change the sequence at any time.

SEQUENTIAL SETUP

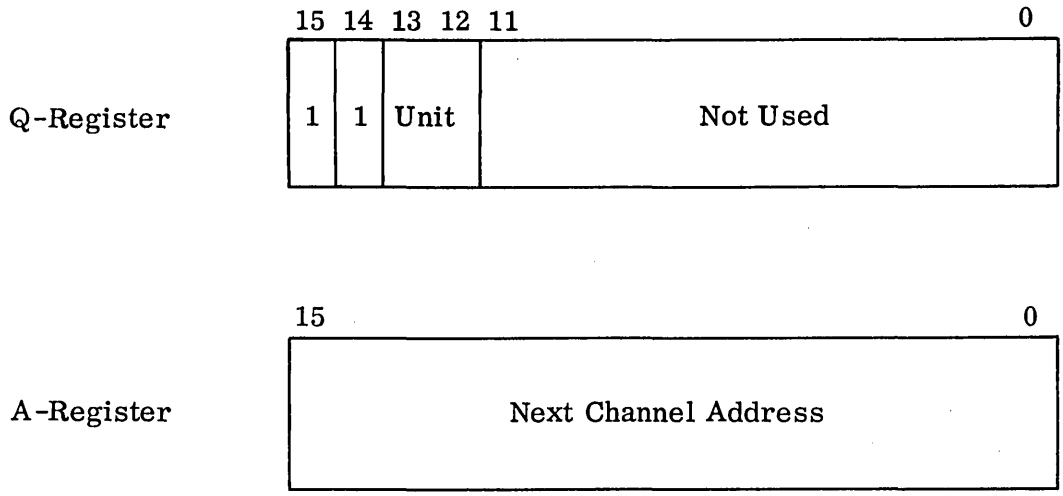
The A- and Q-register formats for Sequential Operation Setup commands are shown below. Sequential setup is accomplished when bit 14 and bit 15 are "1's," the registers are loaded as indicated, and the computer executes an Output-from-A command. Bit 15 indicates the channel address; bit 14 indicates a sequential address setup. Since setup commands are in the form of a Data Transfer command, the DCT must have been connected previously.



SEQUENTIAL OPERATION SETUP COMMAND FORMATS

SEQUENTIAL STATUS

The A- and Q-register formats for Sequential Operation Status commands are shown below. When the Q-register is loaded as indicated and the computer executes an Input-to-A command, the A-register receives the next channel address from the 1574 in bits 0 through 11. The same word as used for a Sequential Setup may be left in the Q-register, since bits 0 through 11 are ignored. This status command can be executed while a sequential operation is in progress to determine how much of a block has been transferred.



SEQUENTIAL OPERATION STATUS COMMAND FORMATS

Table 2.1 summarizes all allowable DCT commands.

2.4 INTERRUPTS USAGE

Refer to Appendix A for a discussion of DCT interrupts usage.

TABLE 2.1. DCT COMMAND STRUCTURE

	OPERATION	INPUT OR OUTPUT	TO/FROM A-REGISTER														FROM Q-REGISTER													
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Function	Out	Functions																W = "0"					E = E_c				Station Address*					
2	Device Status	In	Device Status																W = "0"					E = E_c				Station Address*					
3	Start**	Out	Starting Memory Address																W = "0"									Station Address*					
4	Next Memory Address**	In	Next Memory Address																W = "0"									Station Address*					
5	Direct I/O No Address	I/O	Data																W = "0"					E = E_c				1	1	1	X***	A***	S*** N***
6	Random Address Read Only	In	Data																1000				Channel Address											
7	Random Address Execute	I/O	Data																1001				Channel Address											
8	Random Address Lock Up	I/O	Data																1010				Channel Address											
9	Random Address Increment	I/O	Data																1011				Channel Address											
10	Sequential Setup	Out 1574B						Last Channel Address											1100				First Channel Address											
11	Sequential Setup	Out 1571 (1)						Last Channel Address											1101				First Channel Address											
12	Sequential Status	In 1571 (1)					Next Channel Address												1101				Ignored											
13	Sequential Setup	Out 1571 (2)						Last Channel Address											1110				First Channel Address											
14	Sequential Status	In 1571 (2)					Next Channel Address												1110				Ignored											
15	Sequential Setup	Out 1571 (3)						Last Channel Address											1111				First Channel Address											
16	Sequential Status	In 1571 (3)					Next Channel Address												1111				Ignored											

* Station addresses zero and one are used by the DCT; station addresses 60 through 6F are reserved for the 1797; station addresses 70 through 7F are No Address data transfer.

** Used by buffered devices connected to 1797.

*** Definitions: X = enable A; A = analog/digital: S = step address counter after data transfer; N = inhibit execute signal. No Address commands apply only to modules with sequential channel addressing capability (1574 or 1571).

Section Three

THEORY OF OPERATION

GLOSSARY OF TERMS

SIGNAL NAME	INPUT/OUTPUT	DEFINITION
	INPUT SIGNALS TO DCT FROM 1705	
Q0-Q15	7,9,11,13,15,18,19	Q-Register Inputs
A0-A15	10,12,14,16	A-Register Inputs
WEZ	7	W-Field Equals Zero
MCL	7	Master Clear
PRO	7	Program Protect Bit
READ	18	Read Command
WRITE	18	Write Command
	OUTPUT SIGNALS TO 1705 FROM DCT	
	15	Character Input
RPY	18	Reply
RJT	18	Reject
NT01-NT15	9,11,13,15	Interrupt Lines 01-15
A00-A15	10,12,14,16	A-Register Outputs
S1771	---------	1573 Grounds This Signal
S1785	23-28	1574 Grounds This Signal
S1788	---------	1572 Grounds This Signal
Q00A-Q15B	7,9,11,13,15, 19,22,25,26,28	Condition Q-Register Bits
ADD1A	19	Add "1" to 1574 Register (Q12 · Q14 · Q15)
WHR	19	Write Here
SYN1	9, 13	Sync Source NO. 1
SYN2	9, 17	Sync Source NO. 2
FNCT	7, 20	Function
PRØT	2, 7, 42	Protect
MCL	7	Master Clear
REX	19	Read Execute

SIGNAL NAME	INPUT/OUTPUT	DEFINITION
	INTERNAL CONTROL SIGNALS (Continued)	
WEX	17, 19	Write Execute
ADD1B	9, 19	Add "1" to 1574 Register (No Address · Q01)
NAD	19	No Address
SRS	19	Status Read
PRØ2	7, 18	PROTECT Switch in Position 2
PRØ3	7, 18	PROTECT Switch in Position 3
CNCT	7	Connect
CØNR	7	Reset
	ADDRESS DECODER SIGNALS	
CSA0-CSA3	20, 22	Decoded Address Bits 8,9
CSB0-CSB3	8, 17, 21, 22	Decoded Address Bits 6,7
CSC0-CSC3	8, 17, 21, 22	Decoded Address Bits 4,5
CSD0-CSD3	8, 17, 21, 22	Decoded Address Bits 2,3
CSE0-CSE3	8, 17, 21, 22	Decoded Address Bits 0,1
DIGT	22	Digital Input or Output (Address 0XX)
ANA1	22	Analog 1 (Address 4XX)
ANA2	22	Analog 2 (Address 8XX)
ANA3	22	Analog 3 (Address CXX)
EØS	22	End of Sequence (Grounded by This Card)
DDT	18, 22	Disable Data Transfer EDT (NAD + RAL)
RDT	22	Reject Data Transfer EDT (NAD + RAL)
EDT	22	Enable Data Transfer (Grounded by Cards 23-28)

GLOSSARY OF TERMS (Continued)

SIGNAL NAME	INPUT/OUTPUT	DEFINITION
1574 SEQUENTIAL ADDRESSING UNIT SIGNALS		
CØMP	23-28	Compare
SASS		Sequential Address and Setup
SAM1		Sequential Address Module 1
SAM2		Sequential Address Module 2
NAD		No Address
NLK		1574 Interlock
RAL		Random Address and Lockup
EØS		End of Sequence
NA		Next Address Register
PA		Present Address Register
FA		First Address Register
LA		Last Address Register
CARY		Carry from Preceding Stage of Register
RNA		Read Next Address Register
NAPA		Copy Next Address to Present Address Register
FAPA		Copy First Address to Present Address Register
PANA		Copy Present Address into Next Address Register and Add "1"
QTPA		Copy Q-Register Bits into Present Address Register
RNAR	23-28	Read Next Address Register

SIGNAL NAME	INPUT/OUTPUT	DEFINITION
DCT INPUT AND OUTPUT LINES		
CHL	20	Channel Address
STA	20	Station Address
EØS	23	End of Sequence
SAM1	20, 42	Sequential Addressing Module 1
SAM2	20, 42	Sequential Addressing Module 2
REX	20	Read Execute
WEX	20	Write Execute
PRØ	20	Protected Command
UNPF	20	Unprotected (False)
SYN1	20	Sync NO. 1
SYN2	17	Sync NO. 2
MCL	7	Master Clear
CINF	15	Character Input (False)
RJTF	18	Reject Unconditionally (False)
RHRF	18	Read Here (False)
RRYF	18	Read Ready (False)
WHRF	18	Write Here (False)
WRYF	18	Write Ready (False)
CSA0-CSE3	20, 21	Decoded Address Lines
DIG	20	Digital
ANA1	20	Analog NO. 1
ANA2	20	Analog NO. 2
ANA3	20	Analog NO. 3
AR00F-AR15F	9, 11, 13, 15	A-Read Lines 00-15 (False)
ST00F-ST15F	9, 10, 11, 13, 15	Status Lines 00-15 (False)
AW00-AW15	8	A-Write Lines 00-15
NT01F-NT15F	9, 11, 13, 15	Interrupt Lines 01-15 (False)
PRØSF	7	PROTECT Switch in DCT Off

3.1 GENERAL

The 1750 Data and Control Terminal receives function and addressing information in the form of line-to-line differential voltages of the order of 0.5 volts with a complete voltage reversal distinguishing a "1" from a "0."

For a logical "0," the odd numbered line of the pair (e.g., A1) is at +0.25V and the even numbered line of the pair (e.g., A2) is at -0.25V. For a logical "1," these voltages reverse so that the even numbered line is at +0.25V and the odd numbered line is at -0.25V.

The Q-register and the A-register configurations of the 1700 Computer are transmitted to the DCT with the Q-register containing the W-field, the equipment number in the E-field, and the address (if applicable) in the lower order 7 bits. The A-register contains either the function code or the address. Table 2.1 defines the configuration of the A- and Q-registers during input/output operations.

In addition to the A- and Q-register transfers, inputs are provided for 15 interrupt lines. These interrupts can be generated within the DCT or within any of the devices connected to the DCT.

3.2 TYPICAL DATA AND CONTROL BUS INPUT AND OUTPUT CONFIGURATIONS

3.2.1 Input Configuration

Figure 3.1 shows the typical configuration of input lines from devices connected to the DCT. Each input line forms a continuous AND gate because of the connection of the input signals through the output diodes of the line drivers within the devices. Since inverted logic levels are provided for the output signals from the devices, the net effect is the formation of a continuous OR. The gate implemented by this configuration performs an OR operation on the incoming signals from the devices, and the output of the receiver within the DCT is the logical sum of all the input signals. This output is a "1" if the output from any device is a "0" state signal.

3.2.2 Output Configuration

Figure 3.2 shows the typical configuration of the output line connections for devices connected to the DCT. Each DCT line output driver is capable of driving 40 diode input loads. An isolation diode must be provided for each signal line within each device connected to the DCT. A maximum of two loads are used within any device for each input signal.

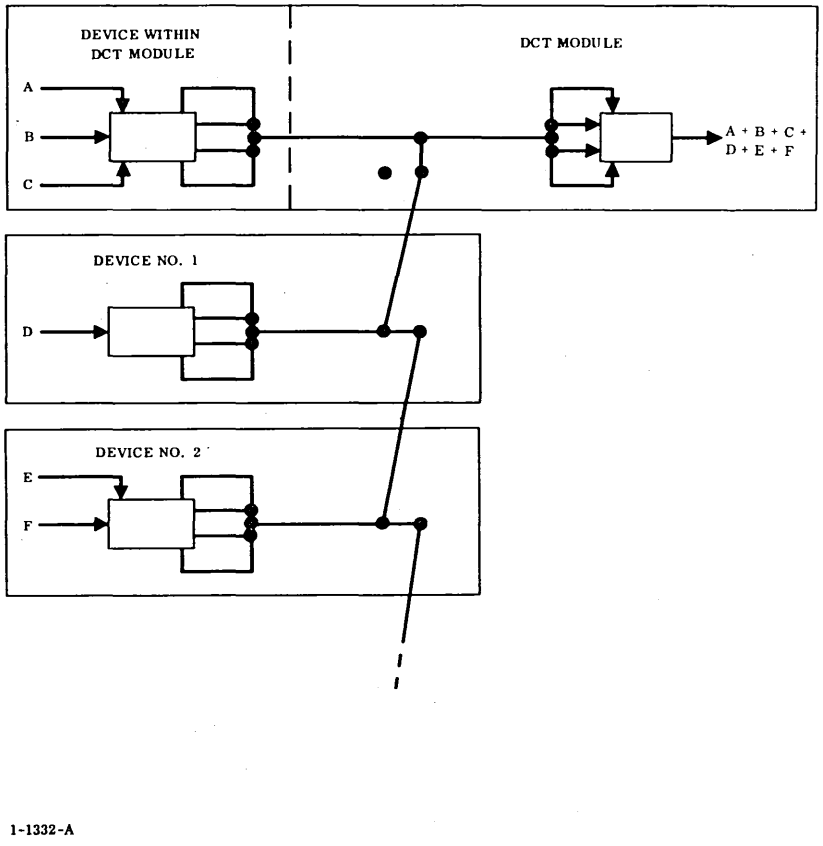


FIGURE 3.1. TYPICAL DCB INPUT CONFIGURATION

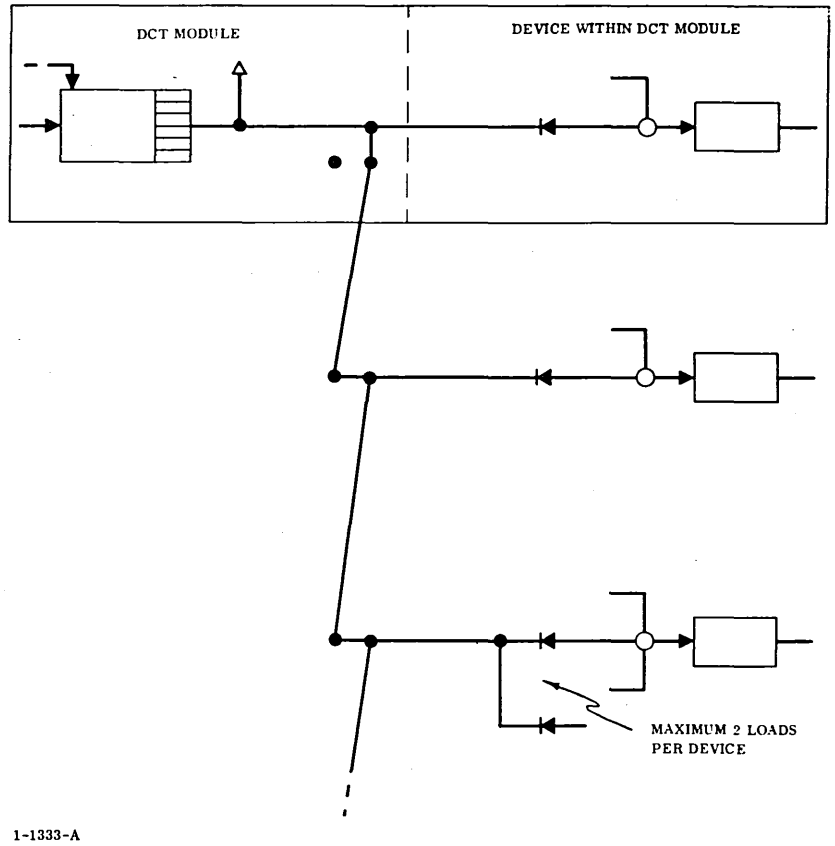


FIGURE 3.2. TYPICAL DCB OUTPUT CONFIGURATION

3.3 FUNCTIONAL DESCRIPTION

Information received by the DCT is handled by the A-register interface, the Q-register receivers (Address Control), and the PROTECT and EQUIPMENT NUMBER switch logic. Control of information flow during input/output information transfers is maintained by the function control and response control logic. Addressing of devices connected to the DCT is established by either the Address Decoder or the 1574 Sequential Addressing Unit. These are mutually exclusive options and only one should be installed in any DCT. If both or parts of both are accidentally installed, a logical interlock system inhibits data transfers until the duplication is eliminated. The interrupts from the DCT and its connected devices are transmitted to the 1705 by the interrupt line transmitters. The function of each of the logic blocks shown in Figure 3.3 is briefly described in the following paragraphs.

3.3.1 A-Register Interface

The A-register interface logic provides an interface for all data and status information between the 1705 and the stations and channels connected to the DCT. The bipolar inputs are received from the A-register transmitters of the 1705, changed to logic levels (0 volts = "0," +3 volts = "1") for transmission to the devices connected to the DCT. Signals originating at the stations are received by line terminators, changed to bipolar levels by the transmitters, and transmitted to the 1705. Control of this information flow is maintained by the DCT function and response control logic with initiation of control by the computer Read/Write signals.

3.3.2 Q-Register Receivers

Q-register bits Q00 through Q06 and Q11 through Q15 are received by this logic block, changed to logic level signals, and output to the Address Decoder, the 1574, and the PROTECT and EQUIPMENT NUMBER switch logic. These bits provide the basic connect and addressing configuration which are decoded to form the various basic control signals.

3.3.3 PROTECT and EQUIPMENT NUMBER Switches

The remaining Q-register bits, the Master Clear, W = "0," and the Program Protect bits are received by this logic block, changed to logic level signals, and compared to the switch settings to originate control signals used by the function and response control logic blocks.

3.3.4 Response Control Logic

This block of logic receives the Read or Write command from the 1705 and the Here, Ready, and Character Input signals from the DCB. The bipolar signals received from the stations connected to the DCB are received as logic levels, and, in some cases, AND'ed with control signals from the function control logic, then changed to bipolar signals and transmitted to the 1705. This block provides the final response to be transmitted to the computer. In cases where no execution of the instruction has occurred, a response is simulated.

3.3.5 Function Control Logic

This logic controls the basic functions of the DCT for transmission, generation, and retrieval of information. Inputs are received from all other logic blocks and from the DCB. The inputs are decoded, interpreted, and combined to control the flow of information to and from the devices connected to the DCT. Decisions regarding disposition of all information transfers are made in this block, with the control information from all other blocks.

3.3.6 Interrupt Interface

The interrupt interface provides line terminators for interrupts generated at the stations or the DCT and transmitters to change these inputs to bipolar signals for transmission to the computer.

3.3.7 A-Write Line Drivers

This block receives the logic level outputs of the A-register interface block and transmits the A-register configuration to the stations continually except during transmission of A-read or status information to the 1705.

3.3.8 A-Read and Status Terminators

This block of logic receives the logic level inputs from the stations which are gated by control signals into the A-register interface block.

3.3.9 C/S Line Drivers

This is a block of line drivers which receives the C/S (Channel/Station Address) inputs from either the Address Decoder or the 1574 and transmits the address control signals to the stations.

3.3.10 End of Sequence

A single line driver is provided for the End-of-Sequence signal from the 1574. This driver is located on a 1574 card and is not used if the 1574 is not installed.

3.3.11 Control Line Drivers

This block of drivers provides amplification for the control signals transmitted to the stations. The inputs to this block are provided by the function control and Address Decoder logic blocks. The input control signals are received, in some cases inverted, and amplified for transmission on the DCB lines.

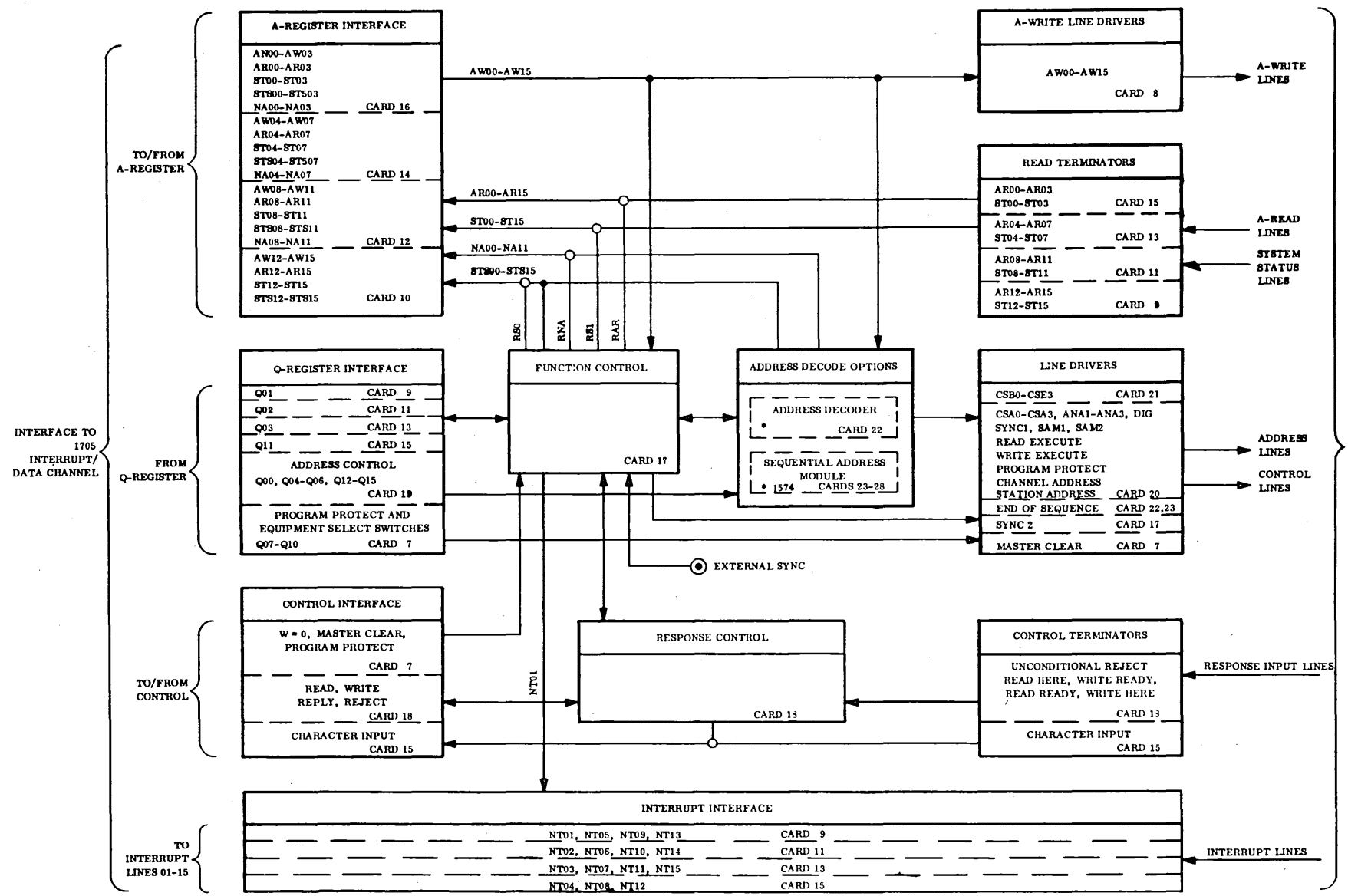
3.3.12 Address Decoder

This block provides decoding for the lower bits of the Q-register. The bits are decoded two at a time to provide four control outputs for each two bits. These outputs are labeled CSA0 through CSE3, with CSE0 through CSE3 decoded from the two lowest order bits of the Q-register.

Q11 is also decoded for special functions within this block. This block and the 1574 are mutually exclusive, and if the 1574 is installed, this block, which is implemented by Card 22, should be removed.

3.3.13 1574 Sequential Addressing Unit

This is an alternate option to the Address Decoder and is used instead of, but not in addition to, the Address Decoder. The 1574 is implemented on cards in positions 23 through 28, all of which must be removed if the 1574 is not used. The 1574 provides a group of four interconnected registers to retain the addresses during sequential addressing operations. The four 8-bit registers are labeled Last Address register, First Address register, Next Address register, and Present Address register.



*CARD 22 IS REMOVED IF THE 1574 MODULE IS INSTALLED.

FIGURE 3.3. DATA AND CONTROL TERMINAL BLOCK DIAGRAM

3.4 DATA AND CONTROL BUS

All communications to and from the computer are via the A/Q cables connected to the DCT. Each interrupt is cabled separately from the DCT to the computer. (See Table 3.1 for DCT pin assignments and Figure 3.4 for DCT cabling.) All communication between the DCT and 1500 Series Peripherals is via the Data and Control Bus (DCB) which originates at the DCT.

The DCB is a two-way communication bus that originates at the DCT in card positions 2, 4, and 6. The DCB is connected to each cabinet rack that contains a controller and is connected from controller to controller in a serial fashion by 50-pin wired connectors (see Figure 3.5). Terminator boards are installed in card positions 2, 4, and 6 of the last controller rack of the serial string.

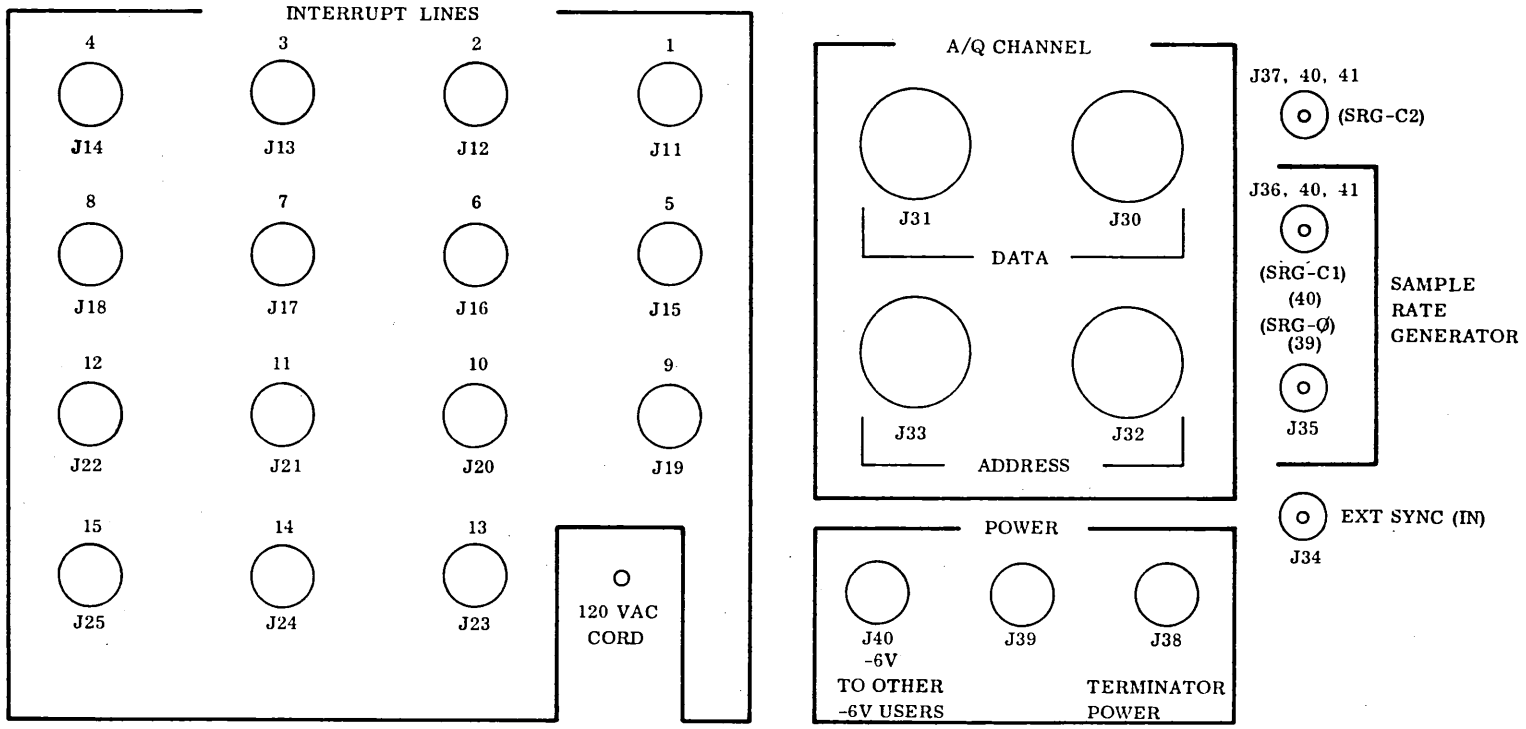
Figures 3.6 through 3.10 list the signal and pin assignments for the DCB connectors that are in card positions 2 through 6. Master Clear (MCL) originates from four parallel diodes of a standard logic element in the DCT and appears in true orientation on the DCB. All other signals originate from four parallel diodes of standard logic elements in devices on the DCB; these signals appear in inverted orientation on the DCB. Card position 3 contains the jumpering for the 1577 Stall Alarm channel/station lines, interrupts, and status. Card position 5 contains the jumpering for signals and interrupts for other optional equipment.

All of the channel/station lines (CSAX, CSBX, CSCX, CSDX, and CSEX) are jumpered from various card positions in the controller module rack to the required DCB lines. (Refer to individual controller manuals for station/channel selection examples and jumpering positions.) Interrupts and multiplexer assignments are jumpered to the DCB lines in the same manner. All other signals are back-plane wired to the DCB lines.

TABLE 3.1. DCT SIGNAL AND PIN ASSIGNMENTS

DATA CABLE SIGNAL		PIN	ADDRESS CABLE SIGNAL	
Data Bit 00		A1, 2	Address Bit 00	
01		3, 4	01	
02		5, 6	02	
03		7, 8	03	
04		9, 10	04	
05		B1, 2	05	
06		3, 4	06	
07		5, 6	07	
08	To/From	7, 8	08	From
09	A-Register	9, 10	09	Q-Register
10		C1, 2	10	
11		3, 4	11	
12		5, 6	12	
13		7, 8	13	W
14		9, 10	14	
Data Bit 15		D1, 2	Address Bit 15	
Reply		3, 4	Read	
Reject		5, 6	Write	
Character Input		7, 8	Master Clear	
Priority*		9, 10	Program Protect	
		E1, 2	Buffer Active*	
		3, 4	Timing Pulse	
		5, 6	Spare	
		7, 8	Spare	
Not Defined		9, 10	Not Defined	
		F1, 2	Not Defined	
		3, 4	Not Defined	
		5, 6	Not Defined	
		7, 8	W = 0	
Termination Power		9, 10	Termination Power	

* These signals exist in the cables from a BDC only and are for use with devices which use the BDC channel exclusively.



J11-J25:
CONNECTOR RECEPTACLE
17896900

J30-J33:
30 TWISTED-PAIR WIRE CONNECTOR
38956900

J38-J40:
CONNECTOR RECEPTACLE
38925500

EITHER ONE OF THE DATA, ADDRESS, AND TERMINATOR POWER CONNECTOR PAIRS CAN BE USED FOR IN OR OUT WHEN THE LCA IS PART OF A CHAIN ON THE 1700 COMPUTER.

IF THE LCA IS THE LAST UNIT ON 1700 PARTY LINES, VACANT RECEPTACLES J30 OR J31 AND J32 OR J33 MUST HAVE A RESISTIVE TERMINATOR PLUG (NO. 30001201) INSTALLED.

FIGURE 3.4. DCT CABLING

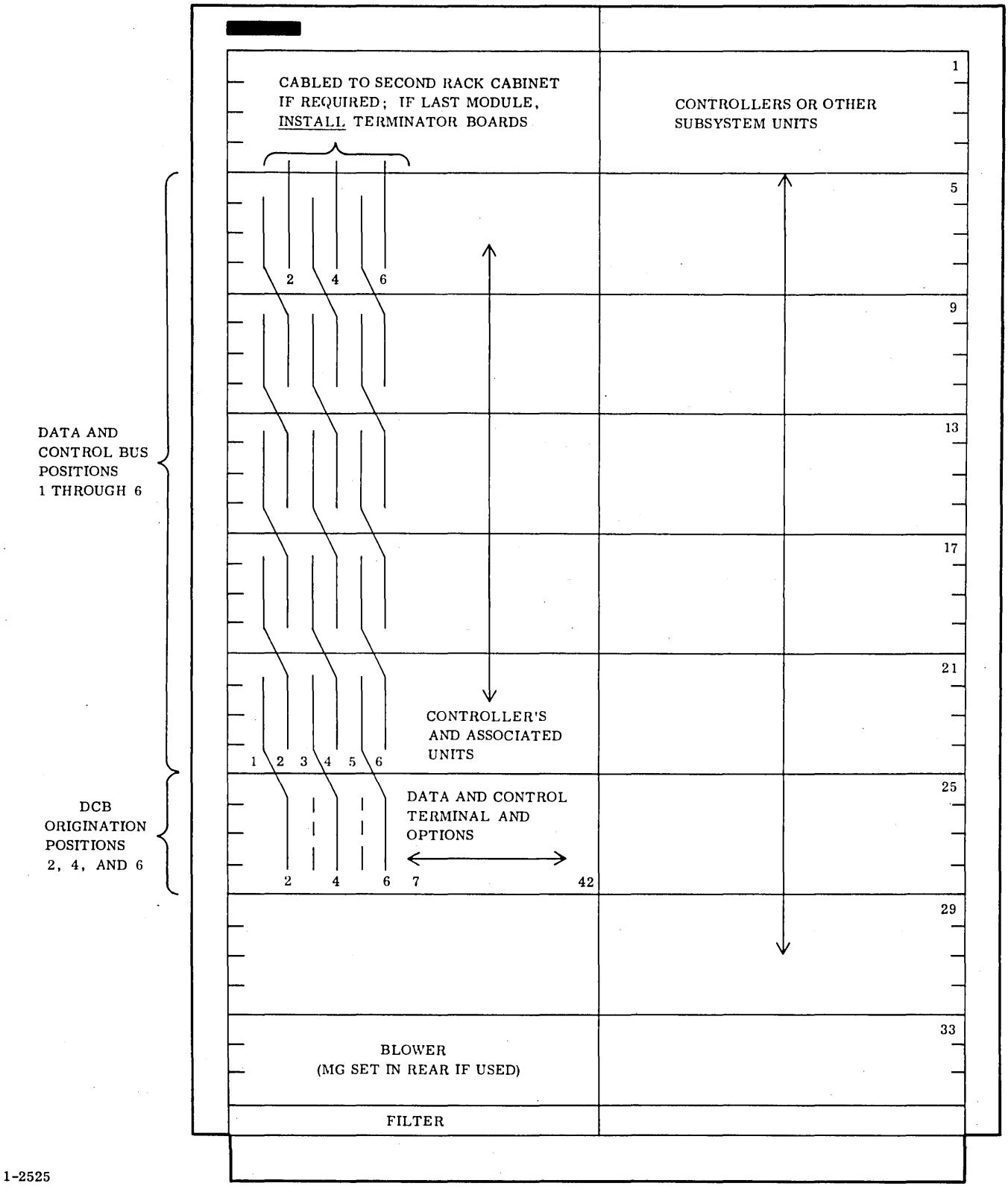


FIGURE 3.5. DATA AND CONTROL BUS

PIN	SIGNAL	TO CARDS	FROM CARDS
1	GROUND		
3	CSA0		
5	CSA1		20
7	CSA2		
9	CSA3		
11	CSB0	17, 3	
13	CSB1	3	
15	CSB2		
17	CSB3		
19	CSC0	17, 3	
21	CSC1	3	
23	CSC2	3	
25	CSC3	3	21
27	CSD0	17, 3	
29	CSD1	3	
31	CSD2	3	
33	CSD3	3	
35	CSE0	17, 3	
37	CSE1	17, 3	
39	CSE2	39, 3	
41	CSE3	39, 3	
43	CHL		20
45	STA	17, 18, 18, 42	20
47	EØS		23, 22
49	GROUND		

PIN	SIGNAL	TO CARDS	FROM CARDS
2	GROUND		
4	DIG		
6	ANA1		
8	ANA2		
10	ANA3		
12	SAM1	23	20
14	SAM2	23	
16	REX	17,18,24,38	
18	WEX	17,23,32,39,42	
20	PRØ		
22	SYN1		
24	SYN2		17
26	MCL	27, 42	7
28	PRØSF	2	7
30	STALL	42	42
32			
34			
36			
38			
40			
42			
44			
46	CINF	15	
48	RJTF	18	
50	GROUND		

NOTE: Pins 28, 32, and 34 are spare pins for signals originating in the DCT; pins 38, 40, 42 and 44 are spare pins for signals originating outside the DCT; pin 36 is used for EØPF in the 1571.

FIGURE 3.6. DCB CONNECTOR (CARD POSITION 2)

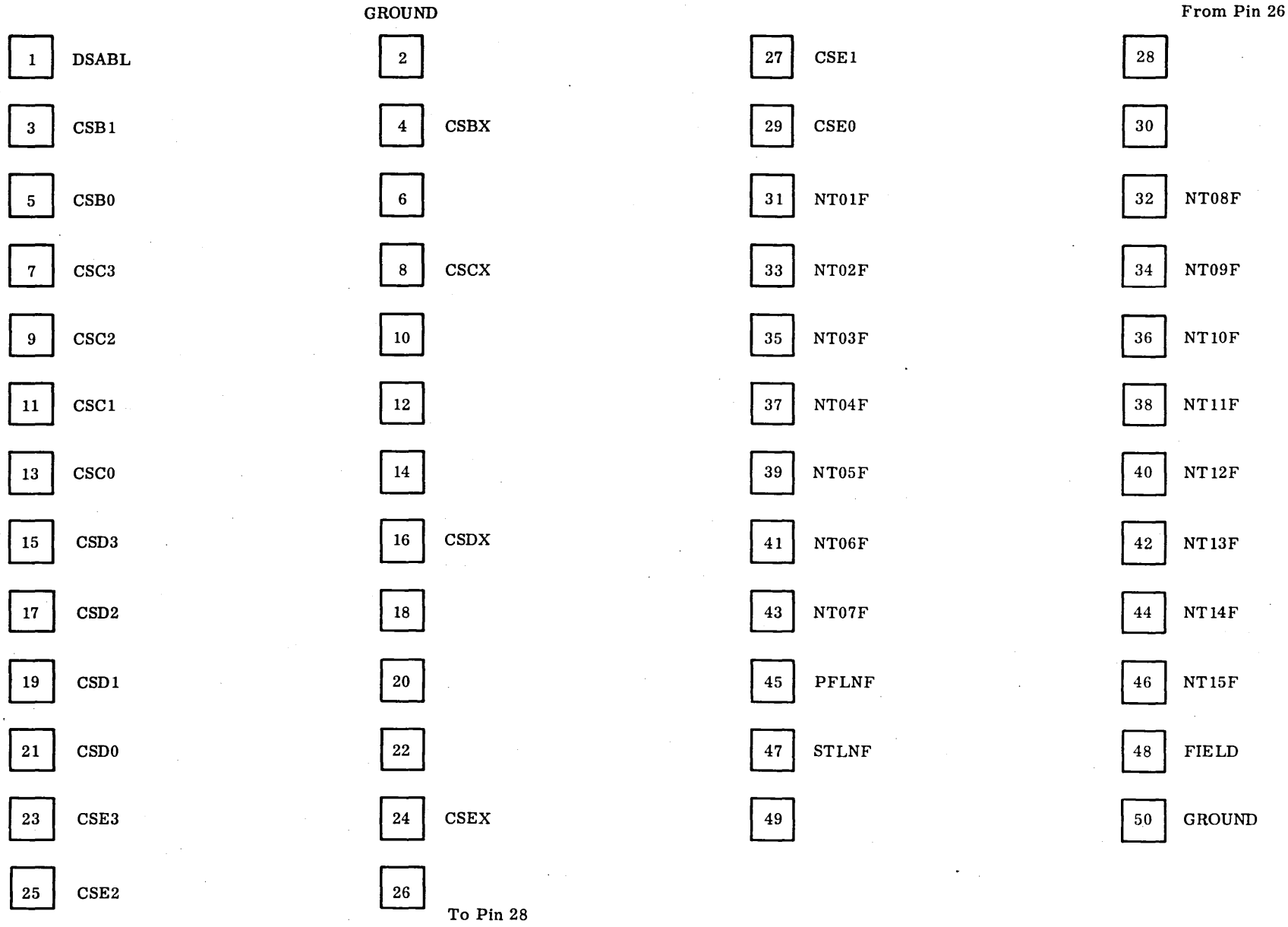


FIGURE 3.7. DCB CONNECTOR (CARD POSITION 3)

PIN	SIGNAL	TO CARDS	FROM CARDS
1	GROUND		
3	AR00F	15	37
5	AR01F		
7	AR02F		
9	AR03F		
11	AR04F	13	36
13	AR05F		
15	AR06F		
17	AR07F		
19	AR08F	11	35
21	AR09F		
23	AR10F		
25	AR11F		
27	AR12F	9	34
29	AR13F		
31	AR14F		
33	AR15F		
35	RHRF	18	13
37	RRYF	18	11
39			
41			
43			
45			
47			
49	GROUND		

PIN	SIGNAL	TO CARDS	FROM CARDS
2	GROUND		
4	AW00	37, 39, 42	8
6	AW01	37, 39	
8	AW02	37	
10	AW03	37	
12	AW04	36	
14	AW05	36	
16	AW06	36, 39	
18	AW07	36, 39	
20	AW08	35, 39	
22	AW09	35, 39	
24	AW10	35, 39	
26	AW11	35, 39	
28	AW12	32, 34, 39	
30	AW13	32, 34, 39	
32	AW14	32, 34, 39	
34	AW15	32, 34, 39	
36	WHRF	18	9
38	WRYF	18, 42	19
40			
42			
44			
46			
48			
50	GROUND		

NOTE: Pins 39 through 48 are not continuous in the DCB Connector.

FIGURE 3.8. DCB CONNECTOR (CARD POSITION 4)

PIN	SIGNAL	TO CARDS	FROM CARDS
1			
3			
5			
7	EØSNF	5	23
9	LSCNF	5	32
11	SRGNF	5	39
13	EXSNF	5	17
15	EØSNF		5
17	LSCNF		5
19	SRGNF		5
21	EXSNF		5
23			
25			
27			
29			
31			
33			
35			
37			
39			
41			
43			
45			
47			
49			

PIN	SIGNAL	TO CARDS	FROM CARDS
2			
4			
6	NT01F	3, 6, 9	Jumpered from signals on pins at left
8	NT02F	3, 6, 11	
10	NT03F	3, 6, 13	
12	NT04F	3, 6, 15	
14	NT05F	3, 6, 9	
16	NT06F	3, 6, 11	
18	NT07F	3, 6, 13	
20	NT08F	3, 6, 15	
22	NT09F	3, 6, 9	
24	NT10F	3, 6, 11	
26	NT11F	3, 6, 13	
28	NT12F	3, 6, 15	
30	NT13F	3, 6, 9	
32	NT14F	3, 6, 11	Jumpered from signals on pins at left
34	NT15F	3, 6, 13	
36			
38			
40			
42			
44			
46			
48			
50	GROUND		

NOTE: For standard interrupt line assignments, insert jumpers as follows: Line Sync Clock (LSC) pin 8 to pin 9 (line 2).

FIGURE 3.9. DCB CONNECTOR (CARD POSITION 5)

PIN	SIGNAL	TO CARDS	FROM CARDS
1	GROUND		
3	UNPF	11	15
5	NT01F	9	
7	NT02F	11	
9	NT03F	13	
11	NT04F	15	
13	NT05F	9	
15	NT06F	11	
17	NT07F	13	
19	NT08F	15	5
21	NT09F	9	
23	NT10F	11	
25	NT11F	13	
27	NT12F	15	
29	NT13F	9	
31	NT14F	11	
33	NT15F	13	
35			
37			
39			
41			
43			
45			
47			
49	GROUND		

PIN	SIGNAL	TO CARDS	FROM CARDS
2	GROUND		
4	ST00F		39
6	ST01F	15	42
8	ST02F		42
10	ST03F		
12	ST04F		
14	ST05F	13	
16	ST06F		
18	ST07F		
20	ST08F		
22	ST09F	11	
24	ST10F		
26	ST11F		
28	ST12F		
30	ST13F	9	
32	ST14F		
34	ST15F		
36			
38			
40			
42			
44			
46			
48			
50	GROUND		

NOTE: Pins 35 through 48 are not continuous in the DCB Connector.

FIGURE 3.10. DCB CONNECTOR (CARD POSITION 6)

3.5 PROGRAM PROTECT AND EQUIPMENT NUMBER SWITCH LOGIC (CARD 7)

This block of logic is implemented by the printed circuit card at card position 7 (see Figure 3.11), which contains a hexadecimally-coded thumbwheel switch (EQUIPMENT NUMBER), a three-position rotary switch (PROTECT), and logic elements for decoding Q7 through Q10, W = "0," Program Protect, and the Master Clear signal to provide control signals.

3.5.1 EQUIPMENT NUMBER Switch

The Q-register bits Q7 through Q10 are received, changed to logic levels for output to other logic blocks within the DCT module, and decoded by the equipment select logic to provide a Connect (CNCT) output. When the setting of the hexadecimal thumbwheel switch matches the E-field (Q7 through Q10) and the W = "0" signal is true, the Connect (CNCT) output is true.

The "C" and "$\overline{C}$" contacts of the EQUIPMENT NUMBER switch are mutually exclusive and provide selection of the output of Q7 through Q10, either as they appear on the output of the receivers or inverted, but not both. When the Q7 through Q10 configurations, and the EQUIPMENT NUMBER switch setting are identical, only "1" state signals are connected to the output. These signals are AND'ed with the W = "0" signal to form the Connect (CNCT) output.

When the switch setting does not match the E-field identically or when the W-field is not "0," the DCT is not connected to the 1705, and the instruction and address is ignored, unless the DCT was connected by a previous operation and bit 15 of the Q-register is a "1" (Continue commands).

3.5.2 PROTECT Switch

The PROTECT switch is a three-position rotary switch used to select the Program Protect response to an unprotected command.

The Program Protect bit is received, changed to a logic level signal, and provided as an output (PRØT) to other blocks of logic. The output of the receiver is also connected to the common pin of the PROTECT switch. The three positions of the switch provide control and status signals as descrived below.

a. OFF (Position 1)

In this position the Program Protect bit is ignored, no protect faults occur, and the Program Protect status bit (STS07, indicating switch positions 2 and 3) is false. The output to the DCT (PRØSF) is true when the switch is in this position.

b. REJECT (Position 2)

In this position the PRØ2 output is the protect bit of the command, the PRØ3 output is true, and the PRØSF output is false. When PRØ2 is false, a protect fault exists, and the faulting command is rejected. For further explanation of this mode, refer to paragraph 3.10.

c. INTERRUPT (Position 3)

In this position the PRØ3 output is the protect bit of the command, the PRØ2 output is true, and the PRØSF output is false. When PRØ3 is false, a protect fault exists, and the response is a Reply and Interrupt transmission to the computer. The faulting command is not executed. For further explanation, refer to paragraph 3.10.

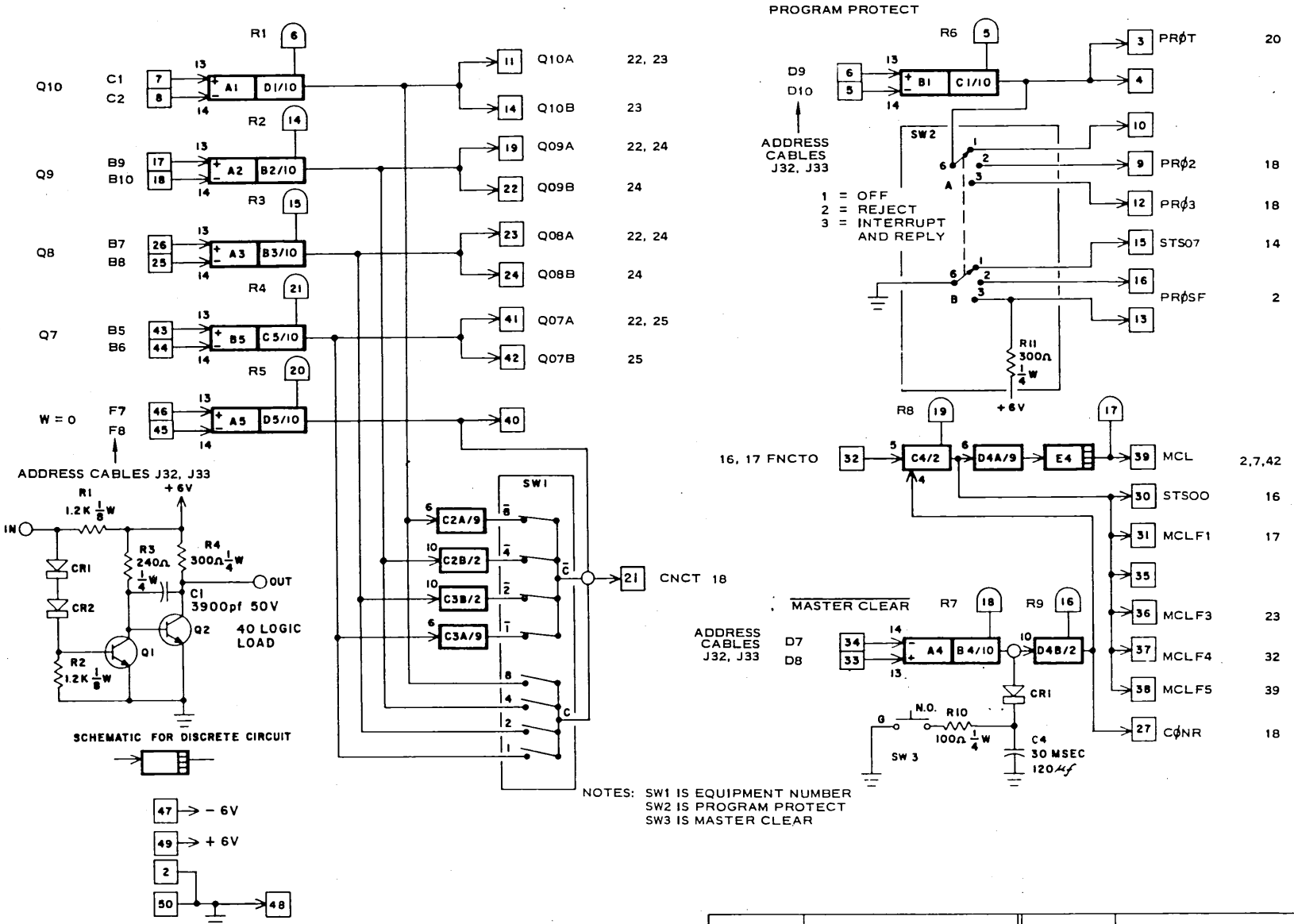
3.5.3 Clear and Master Clear

The Master Clear signal is received in inverted form, changed to a logic level signal, and provided as an input to the AND gate at the input to inverter D4B. The MASTER CLEAR pushbutton provides another input to the AND gate. The manual switch discharges the capacitor, providing a 30-millisecond Clear signal. A 30-millisecond signal is also provided when power is turned on.

When either the Master Clear from the computer or the switch goes false, the input to D4B is false, and the Connect flip-flop reset (CØNR) is true. The Connect reset provides a reset pulse for the Connect flip-flop and an input to inverter C4.

When either CØNR is true or the Clear signal (FNCT AND'ed with A00 and provided as input FNCT0) is true, the output of inverter C4 is false. The output of C4 provides control outputs MCLF1 through MCLF5 and a false signal for status bit 00 (STS00, which indicates a Ready state if true).

The output of C4 is inverted by D4A, which provides an input to the line driver A. The output of line driver A provides a Master Clear signal for other devices connected to the DCT. Figure 3.11 is a diagram of the PROTECT and EQUIPMENT NUMBER switch logic.



	A	B	C	D	E
1	R01A	R01A	R01B	R01B	
2	R01A	R01B	D24		
3	R01A	R01B	D24		
4	R01A	R01B	I48	D24	DCKT
5	R01A	R01A	R01B	R01B	

CARD TYPE: BG
CARD TITLE: Protect and Equipment Select
CARD DRAWING NO.: 38882400
LOGIC DRAWING NO.: 38952600, Sheet 7

PRO3	PROTECT Switch in Position 3	Q0-Q15	Q-Register Inputs
STS00-STS15	Local Status Bits 00-15	Q00A-Q15B	Condition Q-Register Bits
PROSF	PROTECT Switch in DCT Off	FUNCT0	Function at Station Address Zero
MCL	Master Clear	CNCT	Connect
CONR	Reset	PROT	Protect
		PRO2	PROTECT Switch in Position 2

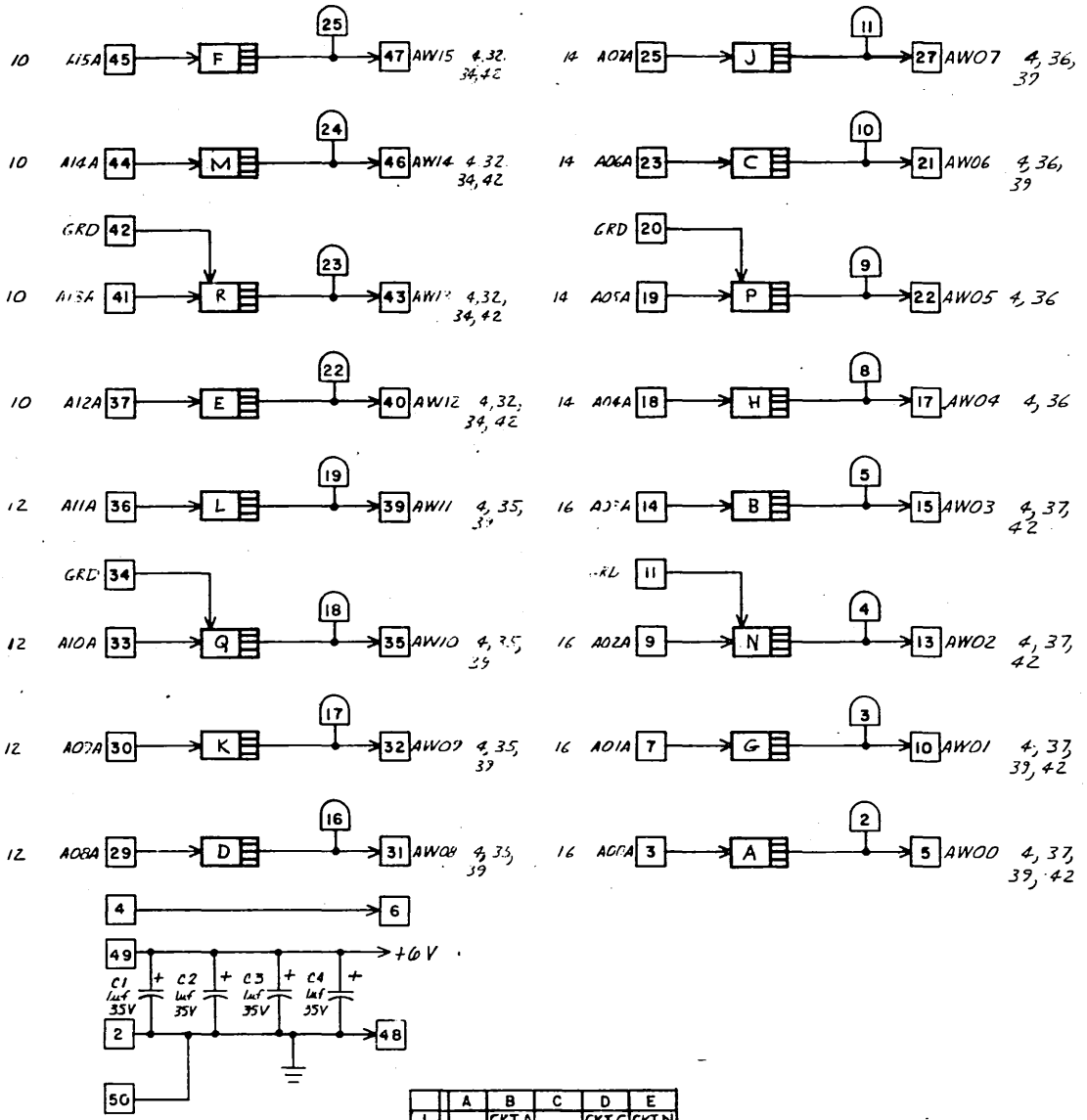
FIGURE 3.11. PROTECT AND EQUIPMENT NUMBER SWITCH LOGIC (CARD 7)

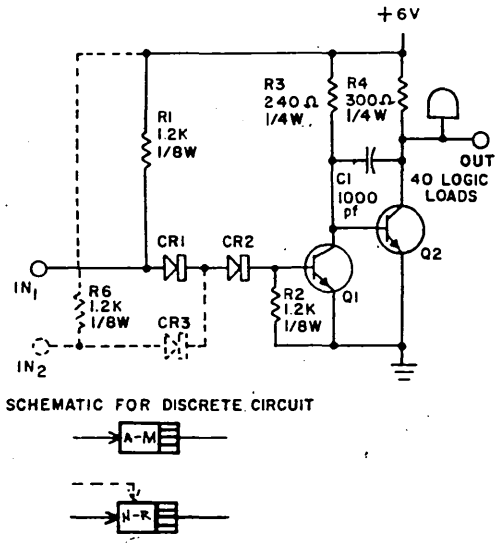
3.6 A-WRITE LINE DRIVERS (CARD 8)

The logic elements contained on the printed circuit card at position 8 (Figure 3.12) provide line drivers for the A-write outputs to the DCT. Each of the noninverting amplifiers contained in this block can drive up to 40 loads. Inputs to these amplifiers are provided by one of the outputs from the A-register interface logic.

The inputs to this card exactly duplicate the configuration of the computer A-register except during the time required for transmission of data or status information to the computer.

The outputs of the amplifiers are connected directly to the connectors to the DCT, and the AW lines are output directly to modules connected to the DCT.





SCHEMATIC FOR DISCRETE CIRCUIT

	A	B	C	D	E
1		CKT A		CKT G	CKT N
2		CKT B		CKT H	CKT P
3		CKT C		CKT J	
4		CKT D		CKT K	CKT Q
5		CKT E		CKT L	CKT R
6		CKT F		CKT M	

CARD TYPE: BM
CARD TITLE: Long Line Drivers
CARD DRAWING NO.: 38897100
LOGIC DRAWING NO.: 38952600, Sheet 8

A00-A15 AW00-AW15	A-Register Inputs A-Write Lines 00-15	

FIGURE 3.12. A-WRITE LINE DRIVERS (CARD 8)

3.7 LINE TERMINATORS (CARD 9)

The printed circuit cards located in card positions 9, 11, 13, and 15 provide line terminators for the A-read lines (AR00 through AR15), system status lines (ST00 through ST15), and interrupt lines (NT01 through NT15). The remainder of the logic elements on these cards are used for miscellaneous functions as described below.

3.7.1 A-Read Lines

The A-read signals received from stations on the DCB are inverted by the line terminators to provide inputs to AND gates located on the A-register interface cards. The A-read line signals are AND'ed with control signals from the function control logic, which controls the data transmission to the 1705.

3.7.2 Status Lines

The System Status signals received from the stations on the DCB are gated to the A-register interface transmitters by the function control logic as described above.

3.7.3 Interrupt Lines

Interrupt lines 02 through 15 are received from the DCB stations, inverted, and transmitted directly to the 1705 interrupt inputs.

Interrupt line NT01 is used for interrupts within the DCT module and for stations on the Decoded Data Channel. When an interrupt occurs either within the DCT or within a station connected to this line, the interrupt is transmitted to the 1705 interrupt input as described above.

3.7.4 Q-Register Receivers

Receivers are provided for Q-register bits Q1, Q2, Q3, and Q11 on the logic cards in locations 9, 11, 13, and 15. The Q-register signals are received, converted to logic level signals, and provided as outputs to the address decoding and/or function control logic blocks.

Q01 is also used for the ADD1B output to the 1574 logic when the 1574 is used. The ADD1B signal is used to increment the Present Address and Next Address registers of the 1574.

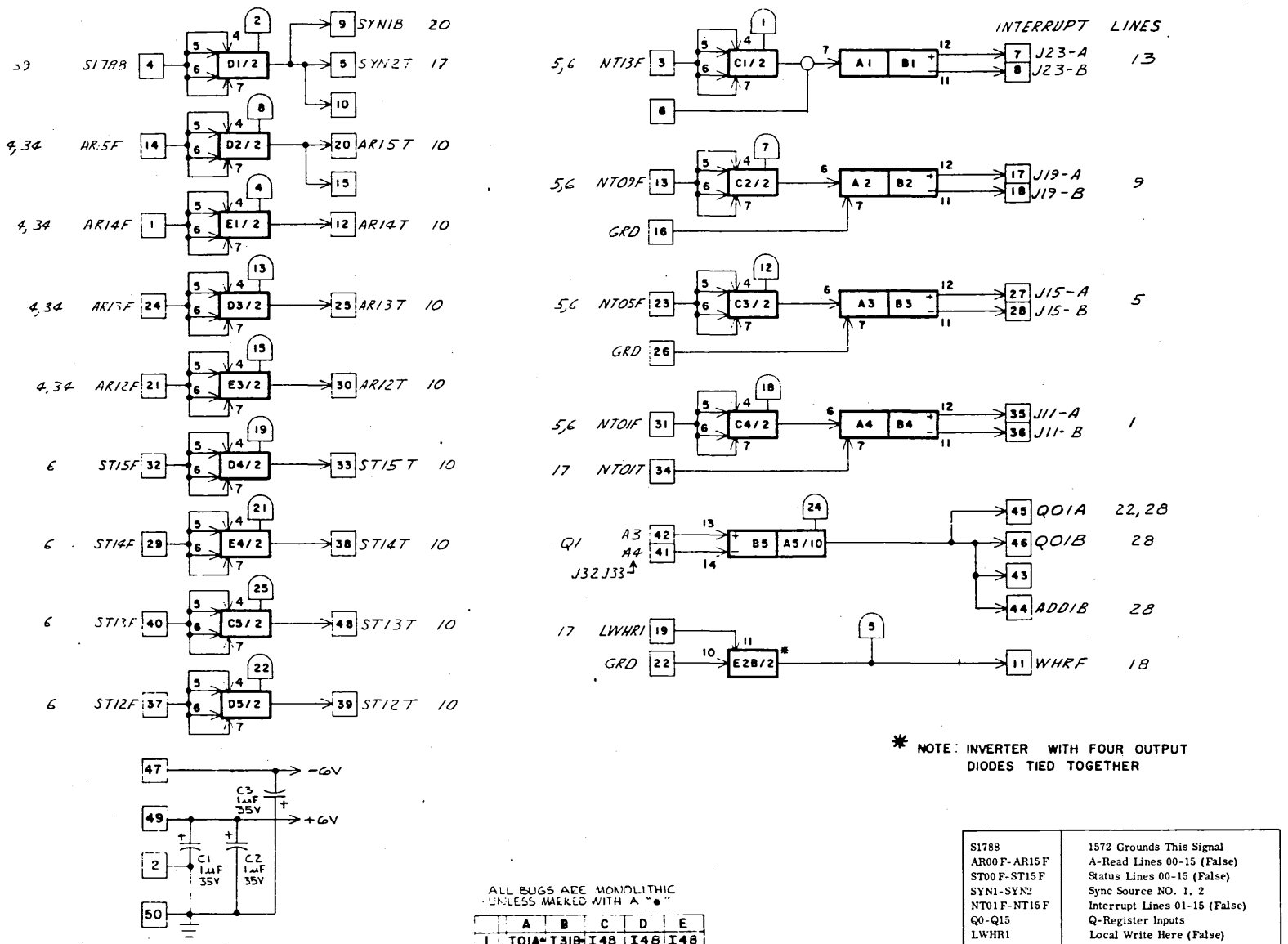
3.7.5 Miscellaneous Logic Elements (Card 9)

S1788

This input is generated by the Sample Rate Generator (Card 9) when this option is installed (see Figure 3.13). The 1788 input is inverted and provided as an input to the function control logic (SYN2T) and as an output to the DCT line drivers (SYN1B).

LOCAL WRITE HERE (LWHR1)

An inverter is provided for the LWHR1 input, from the function control logic, providing an input (WHRF) to the response control logic.



* NOTE: INVERTER WITH FOUR OUTPUT DIODES TIED TOGETHER

ALL BUGS ARE MONOLITHIC UNLESS MARKED WITH A "•"

	A	B	C	D	E
1	T01A•	T31B•	I48	I48	I48
2	T01A•	T31B•	I48	I48	D24
3	T01A•	T31B•	I48	I48	I48
4	T01A•	T31B•	I46	I46	I46
5	R01B•	R01A•	I48	I48	

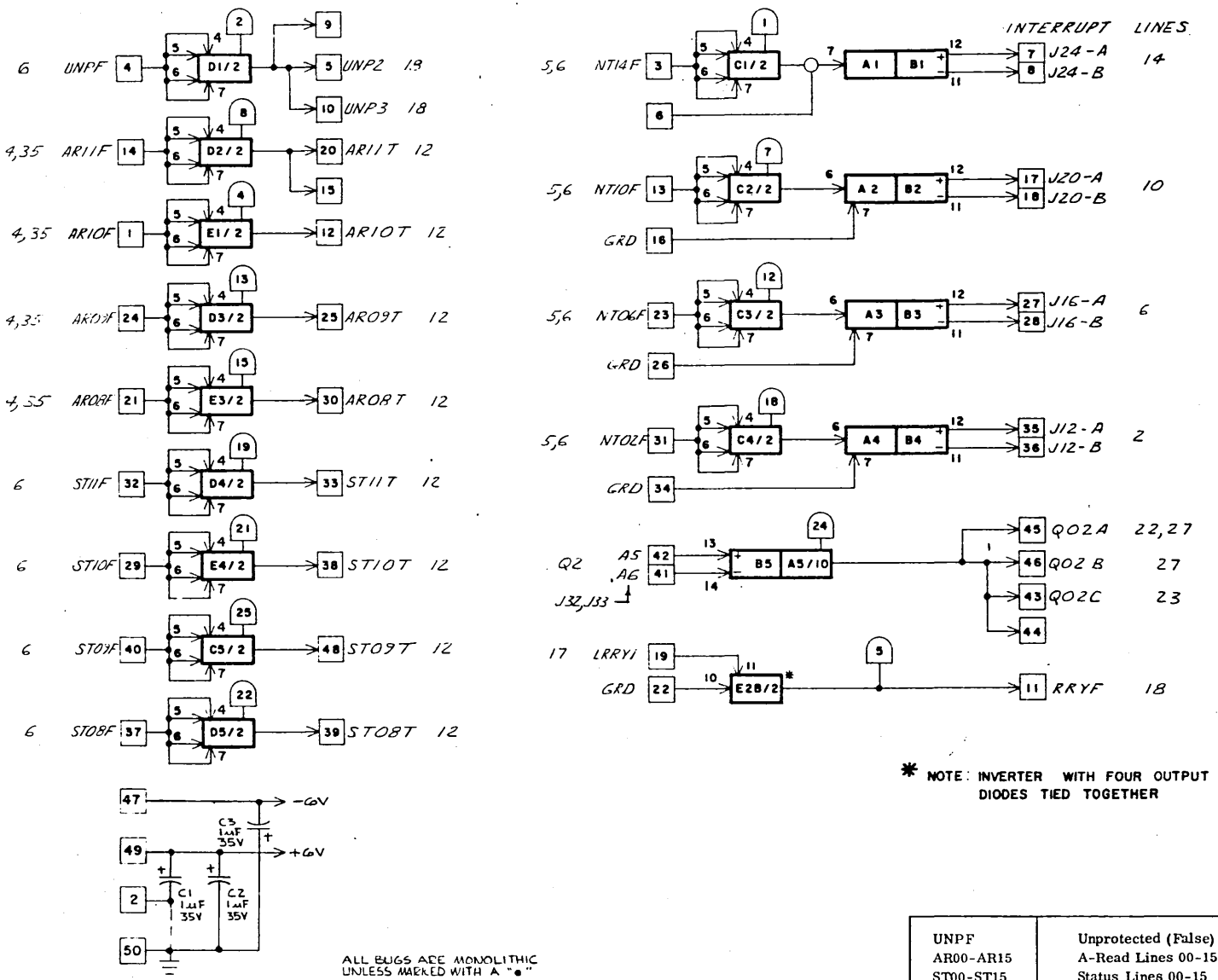
CARD TYPE: BJ
CARD TITLE: Daisy Chain Interface
CARD DRAWING NO.: 38897000
LOGIC DRAWING NO.: 38952600. Sheet 9

S1788	1572 Grounds This Signal
AR00F-AR15F	A-Read Lines 00-15 (False)
ST00F-ST15F	Status Lines 00-15 (False)
SYN1-SYN2	Sync Source NO. 1, 2
NT01F-NT15F	Interrupt Lines 01-15 (False)
Q0-Q15	Q-Register Inputs
LWHR1	Local Write Here (False)
Q00A-Q15B	Condition Q-register Bits
ADD1B	Add "1" to 1574 Register (No Address - Q01)
WHR	Write Here (False)

FIGURE 3.13. DATA AND CONTROL BUS, INTERFACE 1 (CARD 9)

3.7.6 Miscellaneous Logic Elements (Card 11)

In addition to the elements described in the preceding descriptions, Card 11 (Figure 3.14) provides circuit elements for the following signals: (1) UNPF is received from the DCB stations and inverted to provide output signals UNP2 and UNP3, which are used by the response control logic; and (2) LRRY1 is received from the function control logic, inverted, and provided as an output to the response control logic block.



* NOTE: INVERTER WITH FOUR OUTPUT DIODES TIED TOGETHER

ALL BUGS ARE MONOLITHIC UNLESS MARKED WITH A "•"

	A	B	C	D	E
1	TOIA-	T3IB-	I48	I48	I48
2	TOIA-	T3IB-	I48	I48	D24
3	TOIA-	T3IB-	I48	I48	I48
4	TOIA-	T3IB-	I48	I48	I48
5	ROIB-	ROIA-	I48	I48	

CARD TYPE: BJ
CARD TITLE: Daisy Chain Interface
CARD DRAWING NO.: 38897000
LOGIC DRAWING NO.: 38952600, Sheet 11

UNPF	Unprotected (False)
AR00-AR15	A-Read Lines 00-15
ST00-ST15	Status Lines 00-15
NT01-NT15	Interrupt Lines 01-15
Q0-Q15	Q-Register Inputs
LRRY	Local Read Ready
Q00A-Q15B	Condition Q-Register Bits
RRYF	Read Ready (False)

FIGURE 3.14. DATA AND CONTROL BUS, INTERFACE 2 (CARD 11)

3.7.7 Miscellaneous Logic Elements (Card 13)

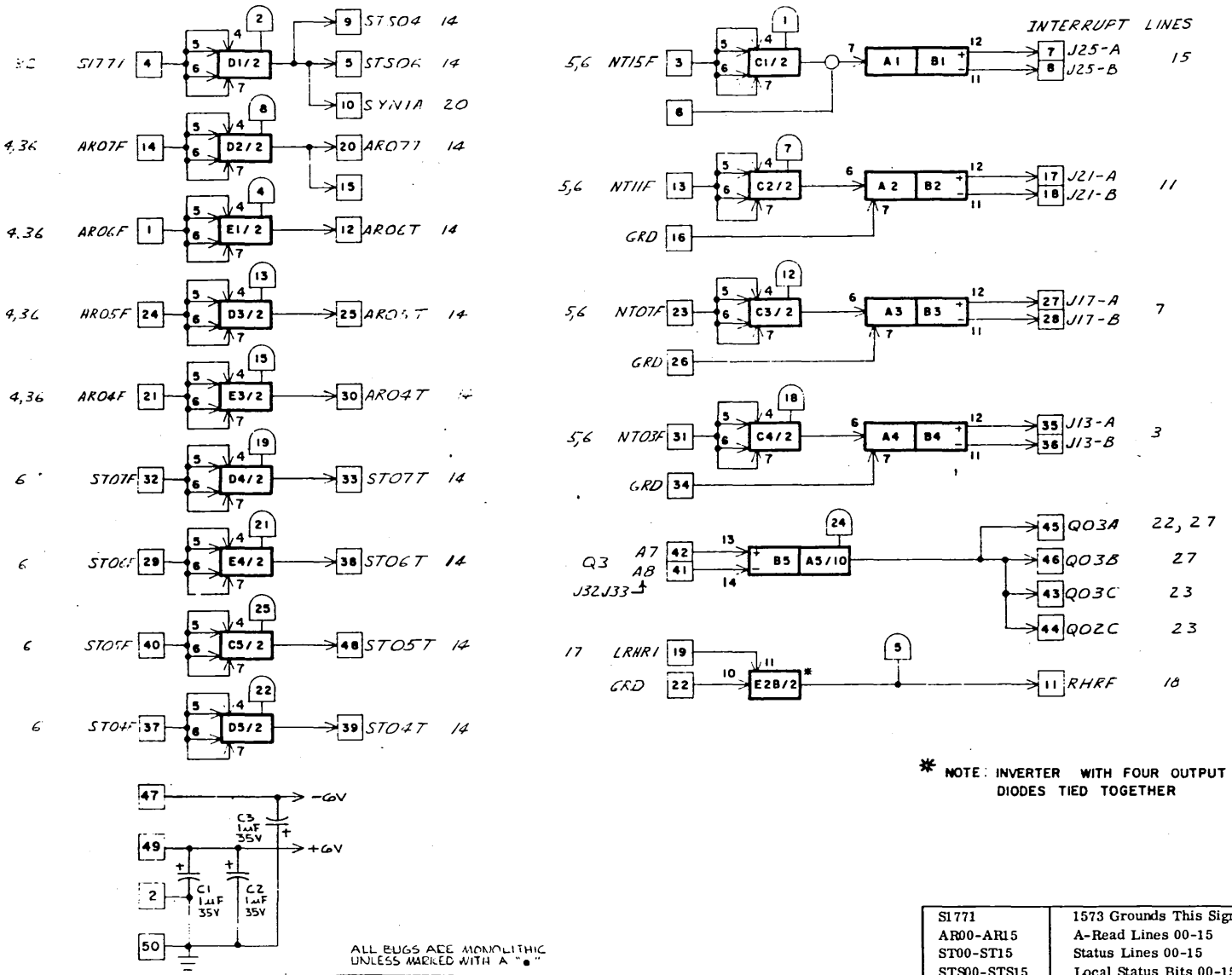
In addition to the elements described in the preceding description, Card 13 (Figure 3.15) provides circuit elements for the following signals.

S1771

This signal is received from the 1573 Line Synchronized Timing Generator, if installed, and is inverted and provided as an output signal to the status transmitters (STS04 and STS06) and as an input to the DCT (SYN1A). STS04 is the status bit 04, indicating a line sync interrupt when true. STS06 is the status bit 06, indicating that the 1573 module is present in the system.

LRHR1

This signal is received from the Function Control logic and inverted for use by the response control logic.



	A	B	C	D	E
1	TOIA•	T3IB•	I48	I48	I48
2	TOIA•	T3IB•	I48	I48	D24
3	TOIA•	T3IB•	I48	I48	I48
4	TOIA•	T3IB•	I48	I48	I48
5	ROIB•	ROIA•	I48	I48	

CARD TYPE: BJ
CARD TITLE: Daisy Chain Interface
CARD DRAWING NO.: 38897000
LOGIC DRAWING NO.: 38952600, Sheet 13

S1771	1573 Grounds This Signal
AR00-AR15	A-Read Lines 00-15
ST00-ST15	Status Lines 00-15
STS00-STS15	Local Status Bits 00-15
SYN1	Sync Source NO. 1
NT01-NT15	Interrupt Lines 01-15
LRHR	Local Read Here
Q00A-Q15B	Condition Q-Register Bits
RHRF	Read Here (False)

FIGURE 3.15. DATA AND CONTROL BUS, INTERFACE 3 (CARD 13)

3.7.8 Miscellaneous Logic Elements (Card 15)

In addition to the elements described in the preceding sections, Card 15 (Figure 3.16) provides circuit elements for the following signals.

NLK5

NLK5 (Interlock 5) is received from the 1574 Sequential Addressing Unit, inverted, and provided as status output signals as follows.

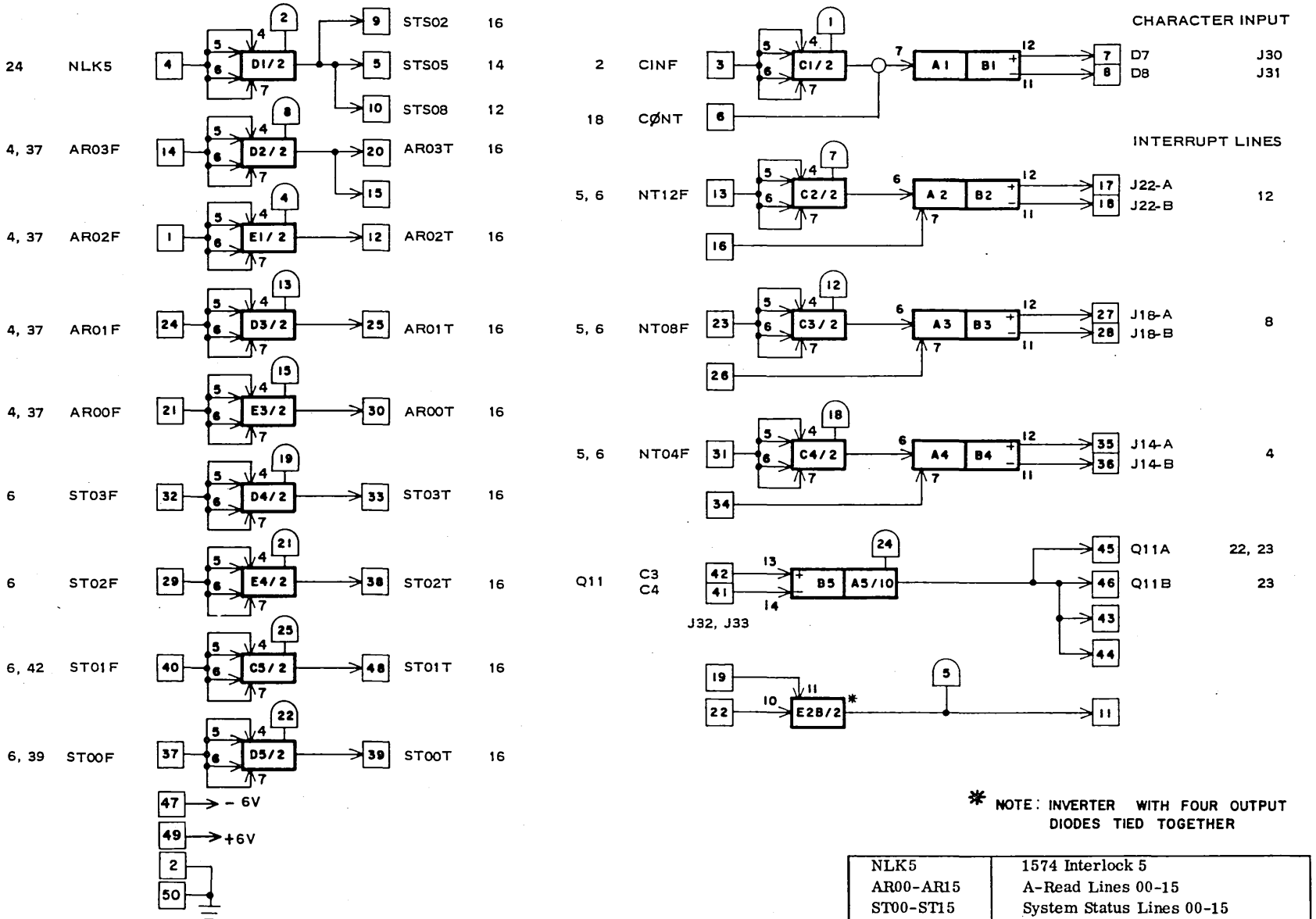
a. STS02 is the 1574 Sequential Addressing Unit interrupt bit.

b. STS05 is the status bit indicating that the 1574 Sequential Addressing Unit is present in the system.

c. STS08 is the status bit that indicates the end of sequence for the 1574.

CINF

The CINF (Character Input) signal is received from the DCB stations, inverted, and AND'ed with the CØNT (Connect) signal to provide an input to the character input transmitter to the 1705. The Character Input signal, when true, indicates that the information being transmitted is a character and not a word of input data.



	A	B	C	D	E
1	T01A	T31B	I45	I45	I45
2	T01A	T31B	I45	I45	D24
3	T01A	T31B	I45	I45	I45
4	T01A	T31B	I45	I45	I45
5	R01B	R01A	I45	I45	

CARD TYPE: BJ
CARD TITLE: Daisy Chain Interface
CARD DRAWING NO.: 38897000
LOGIC DRAWING NO.: 38952600, Sheet 15

* NOTE: INVERTER WITH FOUR OUTPUT DIODES TIED TOGETHER

NLK5	1574 Interlock 5
AR00-AR15	A-Read Lines 00-15
ST00-ST15	System Status Lines 00-15
STS00-STS15	Local Status Bits 00-15
CINF	Character Input (False)
CONT	Connect Signal
NT01-NT15	Interrupt Lines 01-15
Q0-Q15	Q-Register Inputs
Q00A-Q15B	Condition Q-Register Bits

FIGURE 3.16. DATA AND CONTROL BUS, INTERFACE 4 (CARD 15)

3.8 A-REGISTER INTERFACE

The A-register interface is implemented by circuit cards in card positions 10, 12, 14, and 16 (see Figures 3.17 through 3.20). These cards contain both transmitters and receivers for all A-register interfacing.

3.8.1 Receivers

The information is received from the 1705 in the form of bipolar differential signals. The receivers accept the 16A-register bits, change the bipolar signals to logic levels, provide the logic level outputs for use by the DCT logic, and provide inputs to the A-write line drivers (Card 8). The receivers are constantly accepting the A-register contents except during transmission of information from any device on the DCB.

3.8.2 Transmitters

Information transmissions to/from the DCT occur as described below.

The transmitters receive information from the DCB, the 1574, and the DCT. Control of the transmission is maintained by the function control logic (Card 17), the response control logic (Card 18), and the sequential address control (Card 23) if the 1574 is installed.

LOCAL STATUS (STS00-STS15)

Local Status information, from the DCT or devices contained within the DCT module, will be transmitted when the Read-Station-Zero command is executed. During this command the RS0F1 through RS0F4 inputs to the A-register interface cards will be false. The input to the E3 inverter (RS0FX) is false, the output of E3 is true, and the STS00 - STS15 input gates are enabled. If the STS input to the gates are true, a "1" will be transmitted to the 1705.

SYSTEM STATUS (ST00T - ST15T)

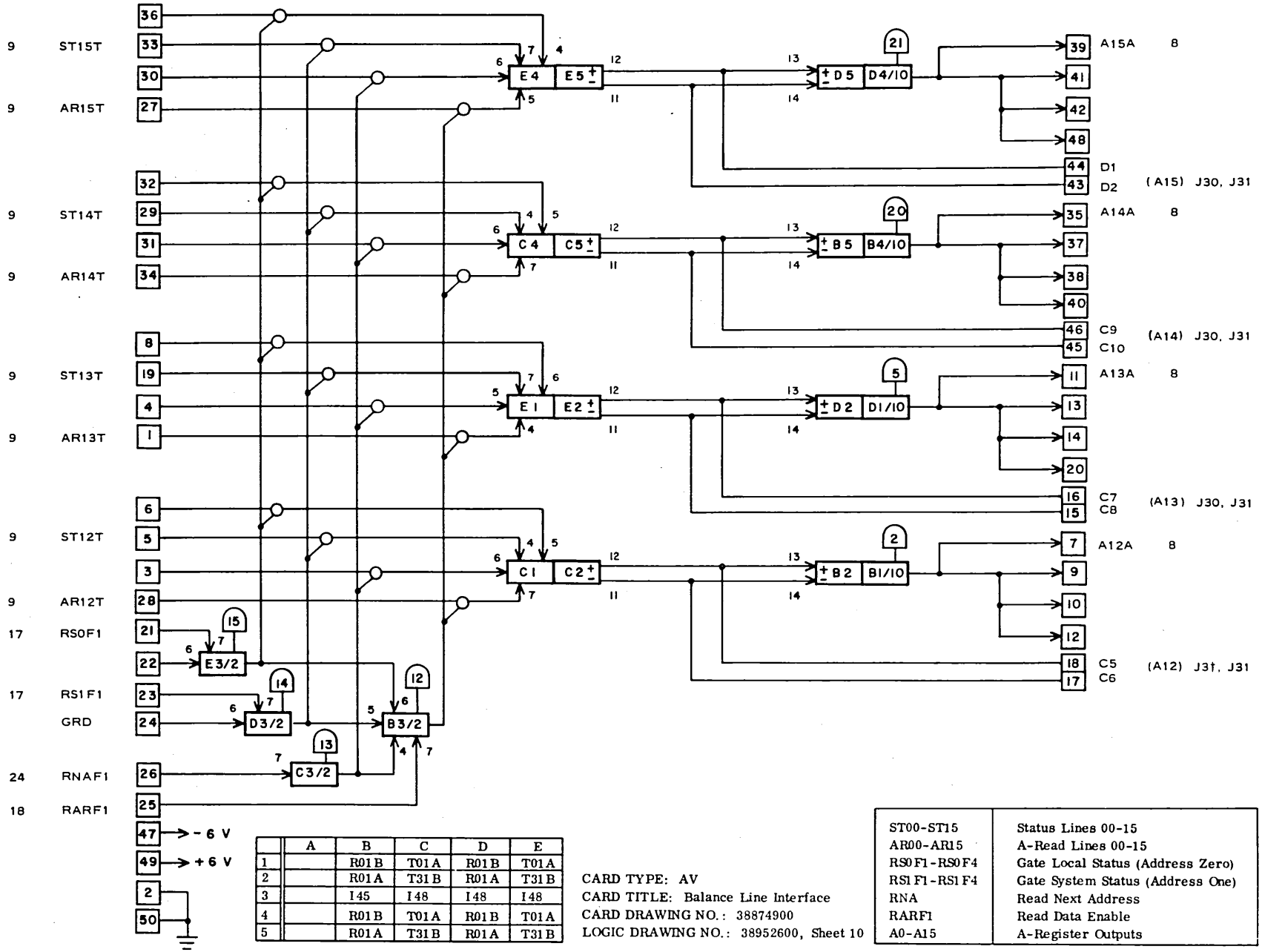
System Status information, received from stations connected to the DCB, will be transmitted when the Read-Station-One command is executed. During this command the RS1F1 through RS1F4 inputs will be false, the outputs of the D3 inverters will be true, and the ST00T - ST15T input gates will be enabled. If the STXXT input is true, a "1" will be transmitted to the 1705.

A-READ LINE INFORMATION (AR00T - AR15T)

Input information, received from the DCB, will be transmitted when a Read command with the appropriate station or channel address is executed. During these commands the RARF1 - RARF4 inputs to the A-register interface will be false. If the other inputs to the B3 inverters (RS0FX, RS1FX, and RNAFX) are also all false, the output of the B3 inverters will be true and the ARXXT input gates are enabled. If the ARXXT input is true, a "1" will be transmitted to the DCT. If one or more of the other inputs to the B3 inverters is true, the ARXXT lines will not be transmitted.

SEQUENTIAL ADDRESSING UNIT NEXT ADDRESS REGISTER (NA00 - NA11)

If the 1574 Sequential Addressing Unit is installed in the DCT package replacing the Address Decoder, the NA00 - NA11 information (contents of the Next Address register of the 1574) is transmitted when a Read-Sequential-Status command is executed. During this command the RNAF1 - RNAF4 inputs to the A-register interface are false, the output of the C3 inverters is true, and the NAXX input gates are enabled. If the NAXX input is true, a "1" is transmitted to the 1705.

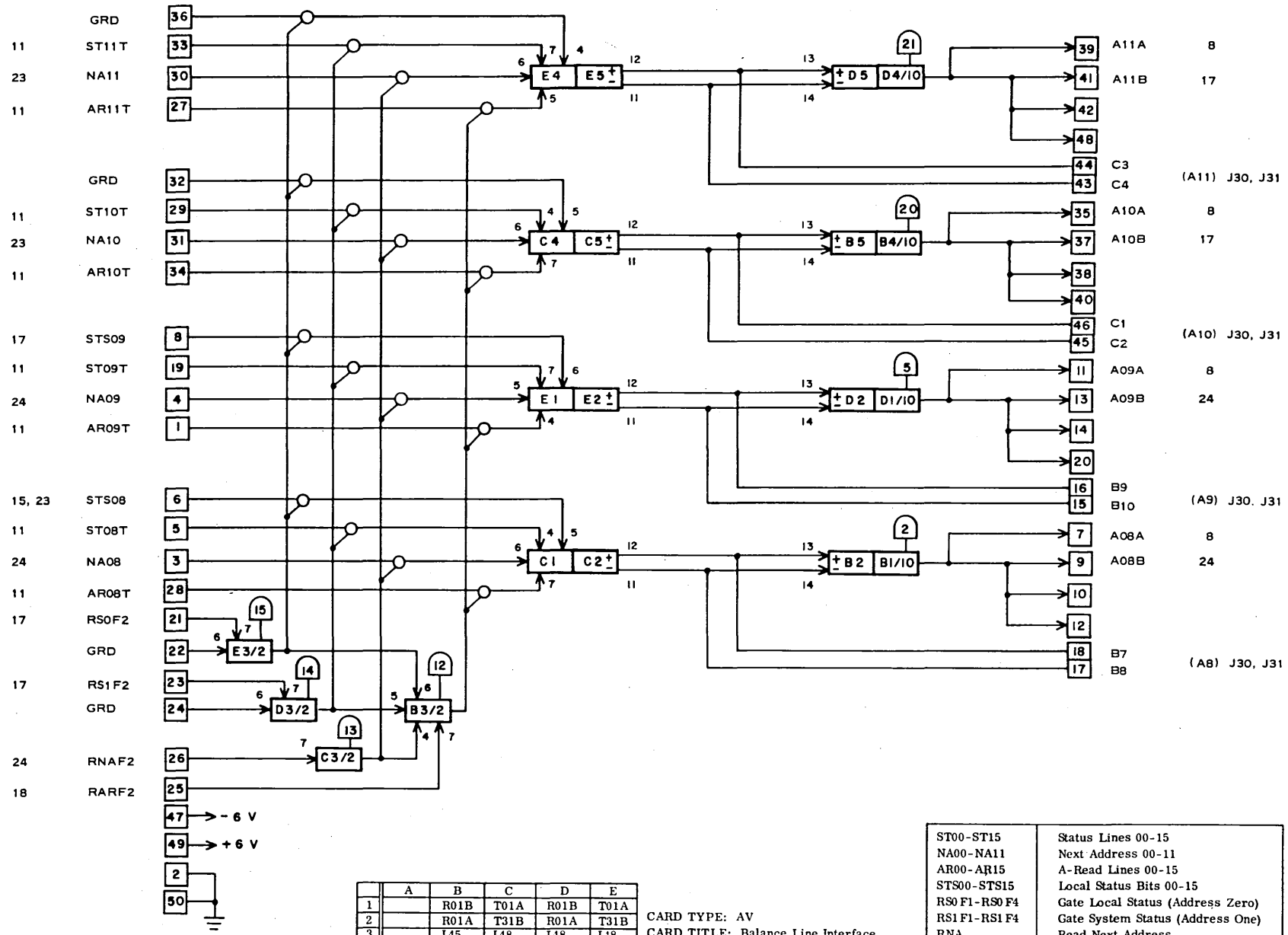


	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I45	I48	I48	I48
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B

CARD TYPE: AV
CARD TITLE: Balance Line Interface
CARD DRAWING NO.: 38874900
LOGIC DRAWING NO.: 38952600, Sheet 10

ST00-ST15	Status Lines 00-15
AR00-AR15	A-Read Lines 00-15
RS0F1-RS0F4	Gate Local Status (Address Zero)
RS1F1-RS1F4	Gate System Status (Address One)
RNA	Read Next Address
RARF1	Read Data Enable
A0-A15	A-Register Outputs

FIGURE 3.17. A-REGISTER INTERFACE: BITS 12-15 (CARD 10)

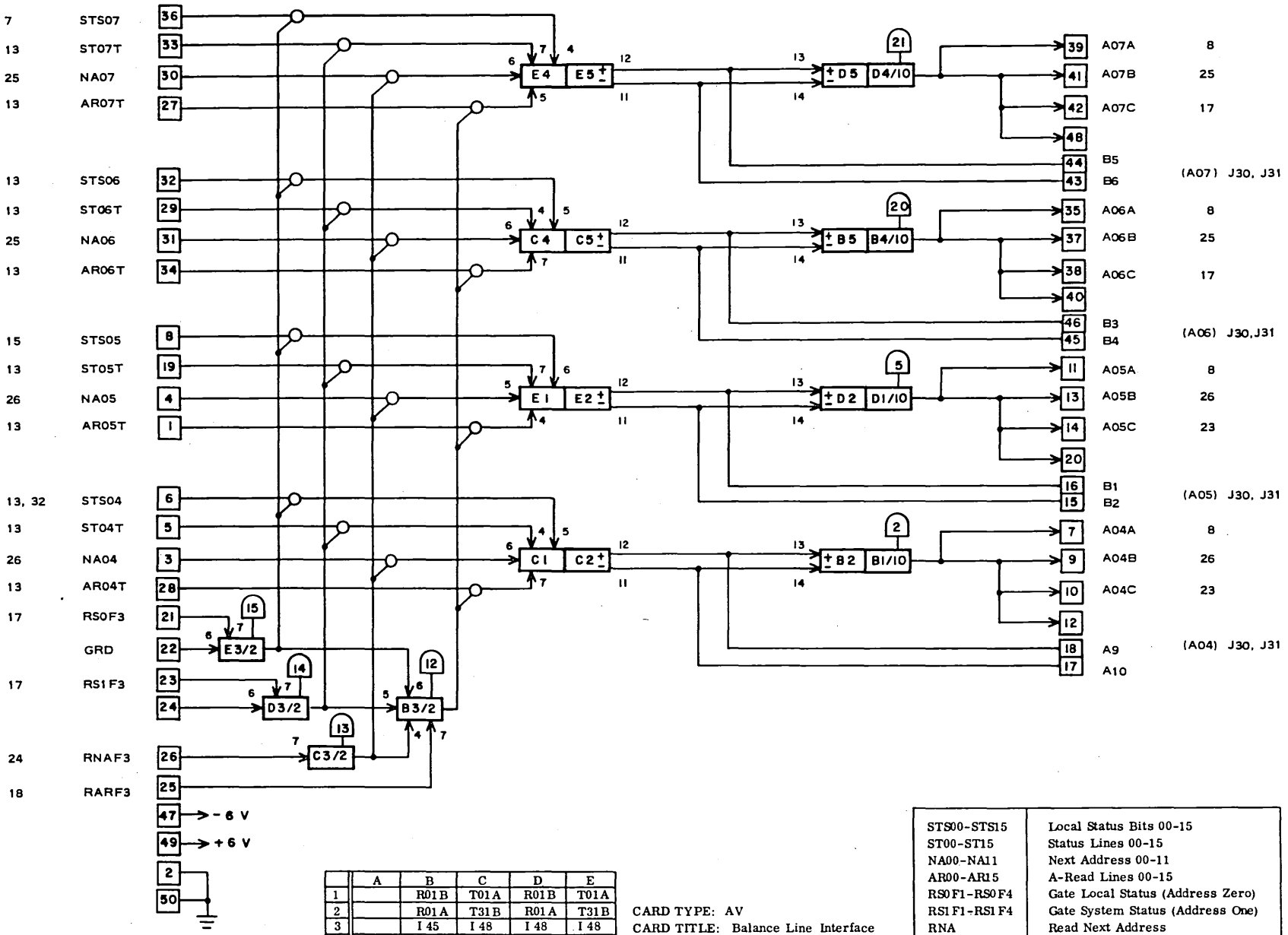


	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I45	I48	I48	I48
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B

CARD TYPE: AV
CARD TITLE: Balance Line Interface
CARD DRAWING NO.: 38874900
LOGIC DRAWING NO.: 38952600, Sheet 12

ST00-ST15	Status Lines 00-15
NA00-NA11	Next Address 00-11
AR00-AR15	A-Read Lines 00-15
STS00-STS15	Local Status Bits 00-15
RS0F1-RS0F4	Gate Local Status (Address Zero)
RS1F1-RS1F4	Gate System Status (Address One)
RNA	Read Next Address
RARF2	Read Data Enable
A00-A15	A-Register Outputs

FIGURE 3.18. A-REGISTER INTERFACE: BITS 8-11 (CARD 12)

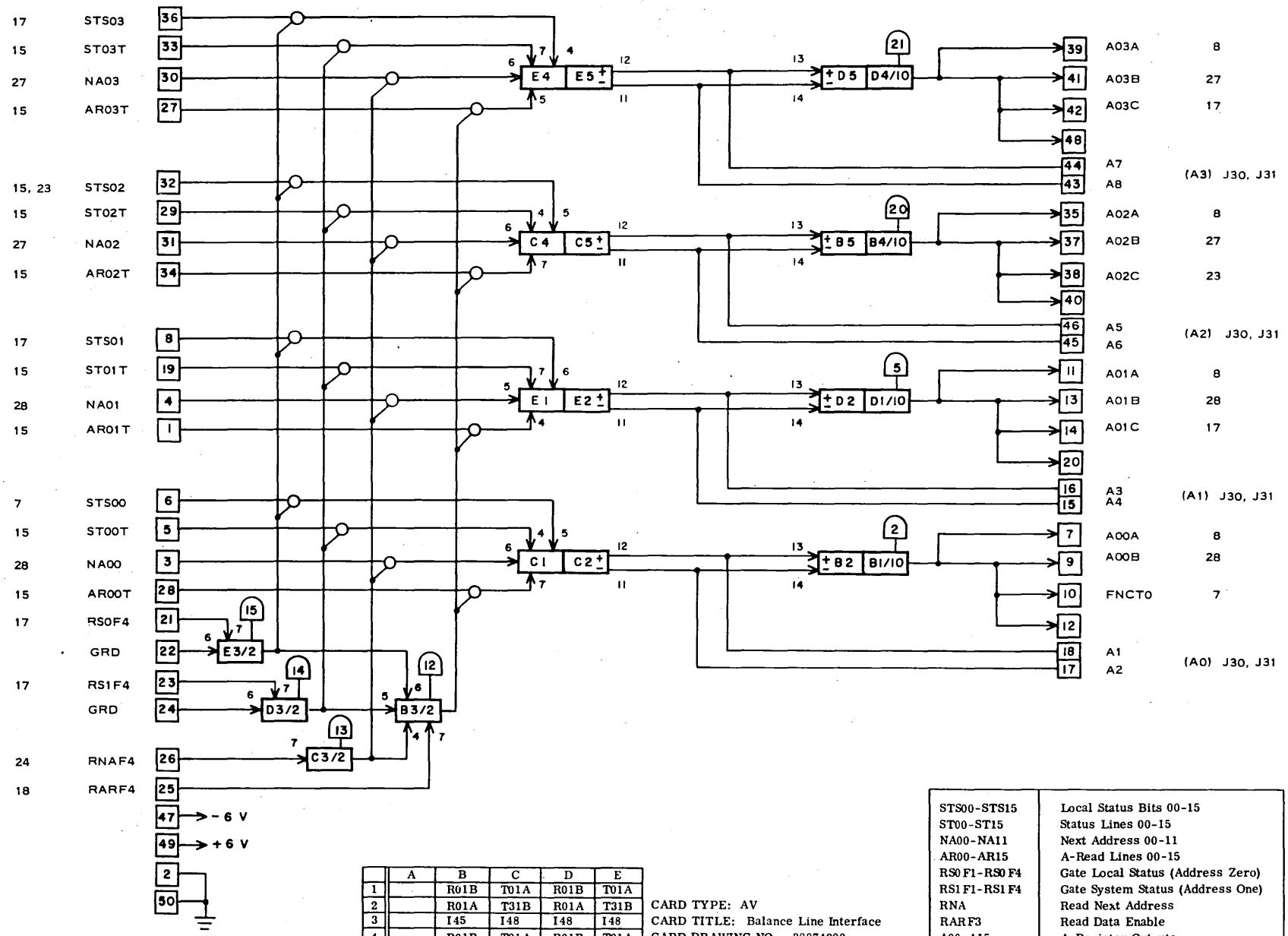


	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I 45	I 48	I 48	I 48
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B

CARD TYPE: AV
CARD TITLE: Balance Line Interface
CARD DRAWING NO.: 38874900
LOGIC DRAWING NO.: 38952600, Sheet 14

STS00-STS15	Local Status Bits 00-15
ST00-ST15	Status Lines 00-15
NA00-NA11	Next Address 00-11
AR00-AR15	A-Read Lines 00-15
RS0F1-RS0F4	Gate Local Status (Address Zero)
RS1F1-RS1F4	Gate System Status (Address One)
RNA	Read Next Address
RARF4	Read Data Enable
A00-A15	A-Register Outputs

FIGURE 3.19. A-REGISTER INTERFACE: BITS 4-7 (CARD 14)



	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I45	I48	I48	I48
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B

CARD TYPE: AV
CARD TITLE: Balance Line Interface
CARD DRAWING NO.: 38874900
LOGIC DRAWING NO.: 38952600, Sheet 16

STS00-STS15	Local Status Bits 00-15
ST00-ST15	Status Lines 00-15
NA00-NA11	Next Address 00-11
AR00-AR15	A-Read Lines 00-15
RS0F1-RS0F4	Gate Local Status (Address Zero)
RS1F1-RS1F4	Gate System Status (Address One)
RNA	Read Next Address
RARF3	Read Data Enable
A00-A15	A-Register Outputs
FNCT0	Function at Station Address Zero

FIGURE 3.20. A-REGISTER INTERFACE: BITS 0-3 (CARD 16)

3.9 FUNCTION CONTROL LOGIC (CARD 17)

The function control logic is implemented by the circuit card in position 17 (see Figure 3.21). Inverters and drivers incidental to function control are located on other cards and described in other sections. The "L" prefix used in this description implies a local control signal (station addresses 0-3), pertaining to devices located within the DCT module package, and includes the DCT logic and the Sequential Setup and Sequential Status commands. The functional descriptions are divided into sections based on the function being described. These sections are not mutually exclusive, but descriptions are carried only as far as required to describe adequately each function.

3.9.1 Local Station False (LSTAF)

This output, when false, indicates that the station address being used is addressing a local station. When a station is addressed (STA true) and when the address is less than 04 (CSB0, CSC0, and CSD0 all true), the input to inverter E1B is true and the E1B output is false. LSTAF is used in the false state to control station addresses 02 and 03. If the device address is not a station (STA false) or if the address is larger than 04 (one or more of the CSB0, CSC0, or CSD0 inputs are false), the input to inverter E1B is false and the output is true. LSTAF in the true state indicates that a local station is not being addressed.

3.9.2 Station Addresses "0" and "1"

If the LSTAF output is false, the input to inverter E1A is false and the output of E1A is true, which enables the input gates to inverters C2A and D2A. When the address is "0" (CSE0 true), the input to D2A is true and the output of D2A is false. If the address is "1" (CSE1 true), the input to C2A is true and the output of C2A is false. When the address is either "0" or "1," a false input is provided for the input gates of inverters C3A, C3B, and D3A. These inverters provide read or write control outputs for stations within the DCT module; read is controlled by the Read Execute (REX), and write is controlled by the Write Execute (WEX), as described below.

READ STATION ADDRESS "0"

When the address is "0," D2B provides a true output to enable the input gate to inverter A2. If the command is a Read command, Read Execute (REX) is true, and the input to A2 is true and the output of A2 is false. The output of A2 provides RS0F1 through RS0F4 outputs (these are used in the false state to gate local status information to the A-read line drivers and transmitters) and provides an input to inverter D3B. The output of inverter D3B provides a true input for the input gate to D3A. The delay input to the D3A gate provides a time delay which is fixed to provide a true Local Read Ready (LRRY1) output for 1.0 microsecond after the leading edge of the Time-to-Execute pulse (REX is timed by TEX). This timing insures sufficient time for transmission of information, and the Ready signal drops at the end of this timed delay and remains false until REX goes false.

READ STATION ADDRESS "1"

The sequence for address "1" is the same as described above for address "0," except for the inverters used. The outputs RS1F1 through RS1F4 are false as described for RS0F1 through RS0F4. The RS1F1 through RS1F4 outputs are used in the false state to gate System Status (status of devices connected to the DCT) to the transmitters. The status word bit assignments for station addresses "0" and "1" are listed below.

a. Input at Station Address "0" (DCT Status).

A-Register Bit	Function (and source if not DCT)
0	Ready
1	Protect Fault Interrupt
2	End-of-Sequence Interrupt (1574)
3	External Sync Interrupt
4	Line Sync Clock Interrupt (1573)
5	1574 Present in System
6	1573 Present in System
7	Protected (PROTECT switch in position 2 or 3)
8	End of Sequence (1574)
9	External Sync Enabled to Sync Line 2
10	
11	
12	
13	
14	
15	

b. Input at Station Address "1" is used to read the system status lines on the DCB.

WRITE STATION ADDRESS "0"

When the station address is "0," the false output of inverter D2A starts at the local read or write cycles (outputs LRRY, LRHR, and LWHR become true), and the LWRY output gate and the A5B inverter input gate are enabled. The output of A5A is normally true; therefore, LWRY goes true at this time. When the Write Execute (WEX) input goes true, the input to A5B is true and the output of A5B is false. The A5B false output provides the FNTF1 through FNTF3 outputs (used in the False state to indicate a Function (Write) for devices within the DCT) and provides a false input to inverter A4. The true output of A4 enables the input gates to the sync and Interrupt flip-flops, provides an input to the A5A gate, and provides the FNCT0 (Function at station 0 address) output. The time delay input to the A5A gate provides a 1.5-microsecond delay and causes the A5A inverter to remain true for 1.5 microseconds after WEX comes true. This delay allows time for the function to be executed. When the 1.5-microsecond delay time elapses, the LWRY output goes false and remains false until WEX goes false. The functions at station address "0" are as listed in the table below.

Output at Station Address "0" (DCT Functions)

A-Register Bit	Function
0	Clear DCT
1	Reset Protect Fault Interrupt
2	Reset End-of-Sequence Interrupt
3	Reset External Sync Interrupt
4	Disable End-of-Sequence Interrupt
5	Enable End-of-Sequence Interrupt
6	Disable External Sync Interrupt
7	Enable External Sync Interrupt
8	
9	
10	Disable External Sync from Sync 2 Line
11	Enable External Sync to Sync 2 Line
12	Disable 1573 Output from Sync 1 Line
13	Enable 1573 Output to Sync 1 Line
14	Disable 1573 Interrupt
15	Enable 1573 Interrupt

EXTERNAL SYNC CONTROL, EXTERNAL SYNC, AND PROTECT FAULT INTERRUPT CONTROL

The functions performed with station address "0" include control of four flip-flops used for External Sync Enable (B4), External Sync Interrupt Enable (C4), External Sync Interrupt (D4), and the Protect Fault Interrupt. Various control signals and A-register bits are used for these control functions, as described below. For these functions, the station address must be "0" and WEX must come true as described above. The following descriptions assume that these conditions have been met and that the FNCT0 (Function at Station Address "0") output is true. Input gates to all the flip-flops are enabled by the FNCT0 signal.

Master Clear

The Master Clear Input (MCLF1, used in the False state to indicate a Master Clear) when false, provides a false input to inverter E5B. The output of E5B goes true and clears (resets) all four flip-flops.

Sync Enable Flip-Flop

a. Set

When FNCT0 is true and the A11B input is true (A-register bit 11), flip-flop B4 is set. The set side of B4, when in the True state, enables the input gate to line driver A and provides a true output for status bit 09 (STS09). STS09, when true, indicates that the External Sync is connected to SYN2. When the EXTSN (External Sync Input) goes true, all inputs to the AND gate at the input to the SYN2 line driver are true (C5A output is normally true), and the SYN2 output goes true. After 300 nanoseconds the output of C5A goes false, and the SYN2 output goes false.

b. Reset

When FNCT0 is true and the A10B input is true (A-register bit 10) or MCLF1 is false as described above, flip-flop B4 resets and remains reset until set again with a FNCT0 command.

When set, the C4 flip-flop provides a true set output which enables the input gate to the C5B line driver. This line driver provides an output to the interrupt lines and can be OR'ed with one or more other interrupt outputs. With the input gate enabled, the input to C5B goes true whenever an External Sync Interrupt occurs (flip-flop D4 set) and remains true until D4 and/or C4 is reset by a FNCT0 command as described above.

External Sync Interrupt Flip-Flop

a. Set

When the EXTSN (External Sync Input) input goes true, flip-flop D4 is set (C5A output is normally true), and a true input is provided for the input gate to inverter C5A. C5A acts as a leading edge detector to provide a sync pulse for a period of 300 nanoseconds. At the end of the 300-nanosecond period, the input to C5A goes true and the C5A output goes false. C5A thus produces a 300-nanosecond, positive-going pulse at the leading edge of the EXTSN pulse. When true, the set side of the D4 flip-flop provides a true input to the line driver C5B. If the input gate of C5B is enabled (enable flip-flop C4 is set), the input to C5B goes true and remains true until D4 and/or C4 is reset.

b. Reset

When FNCT0 is true and the A03C input comes true (A-register bit 03) or when the MCLF1 input goes false as described above, the External Sync Interrupt flip-flop D4 resets and remains reset until the next EXTSN pulse occurs.

Protect Fault Interrupt Flip-Flop

a. Set

When a protect fault interrupt occurs (in other words, the PFNS input is true), flip-flop E4 sets. Flip-flop E4 remains set until it is reset as described in the following paragraph. The set output provides a true output for the protect fault status bit which is STS01.

b. Reset

When FNCT0 is true and the A01C input is true (A-register bit 01), or MCLF1 is false as described above, flip-flop E4 resets and remains set until it is set by PFNS as described above.

During the set state of E4, the reset output provides a false output to inverter E5A. E5A provides a true output connected to interrupt line 01 and may be OR'ed with one or more other NT01 inverter outputs. The input to E5A remains true as long as E4 is set.

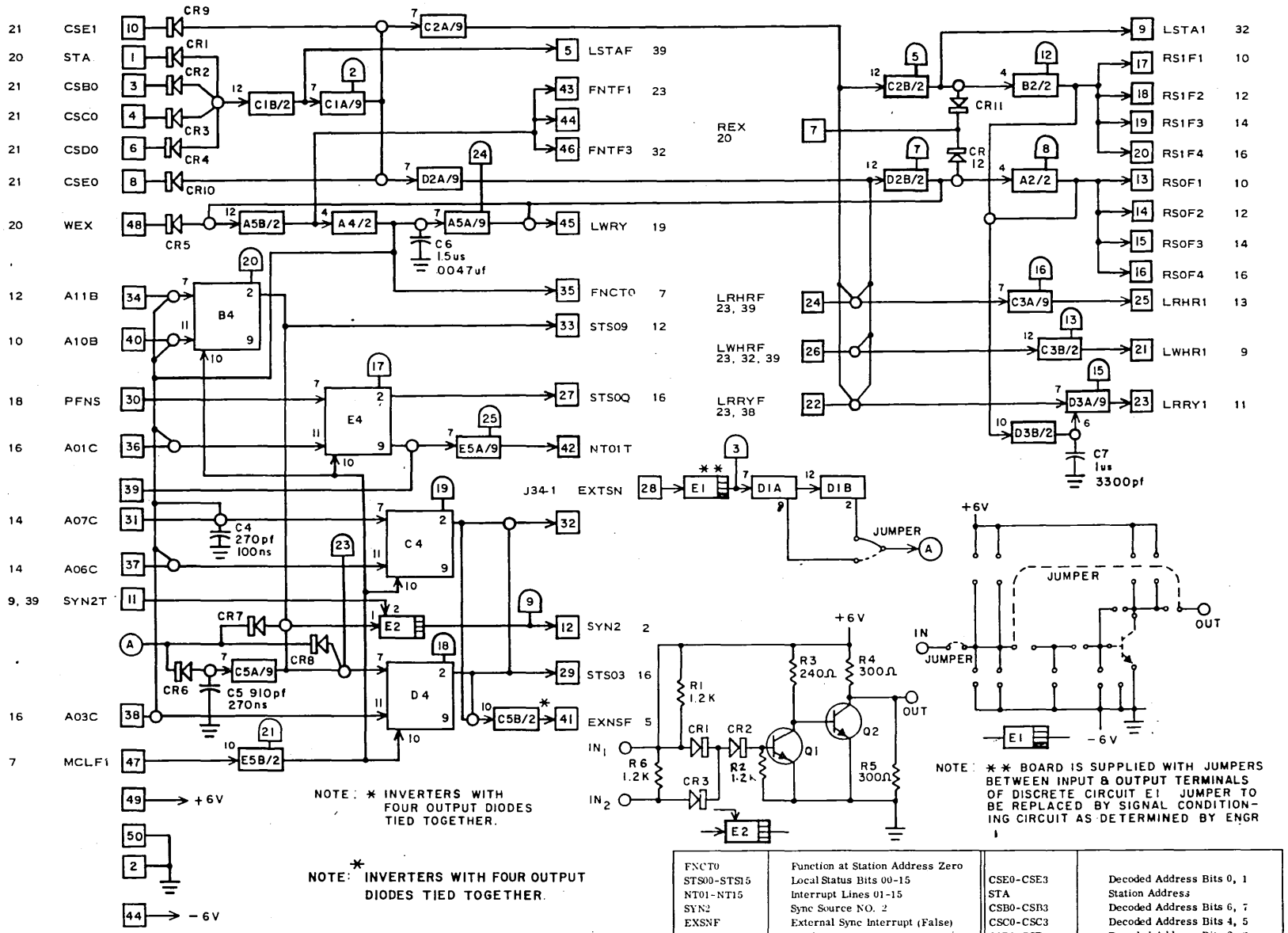
Provision is made to OR another input to E5A via pin 39. When false, the input on pin 39 also provides a true output on NT01T as long as it remains false. As pin 39 is not currently connected to any input, it can be disregarded but should not be tied to ground.

WRITE STATION ADDRESS "1"

When the station address is "1," both inputs to the gate at C2A are true, the input to C2A is true, and the C2A output is false. This false output provides an input for the local Read and Write controls as described above; it also provides false input to C2B.

The output of C2B is true, providing the LST41 output. This command is used to acknowledge an interrupt from the 1573 Line Synchronized Timing Generator. The A-register is not used for this operation.

No response is sent if the 1573 is not present. A Reply is sent if the 1573 is present and has sent an interrupt, and the interrupt is reset. A Reject is sent if the 1573 is present but has not sent an interrupt.



NOTE: * INVERTERS WITH FOUR OUTPUT DIODES TIED TOGETHER.

	A	B	C	D	E
1					D24
2	I48	I48	D24	D24	DCKT
3			D24	D24	
4	I48	F24	F24	F24	F24
5	D34		D24		D24

CARD TYPE: BN
CARD TITLE: Function Control
CARD DRAWING NO.: 38905500
LOGIC DRAWING NO.: 38952600, Sheet 17

FNCT0	Function at Station Address Zero	CSE0-CSE3	Decoded Address Bits 0, 1
STS00-STS15	Local Status Bits 00-15	STA	Station Address
NT01-NT15	Interrupt Lines 01-15	CSB0-CSB3	Decoded Address Bits 6, 7
SYN2	Sync Source NO. 2	CSC0-CSC3	Decoded Address Bits 4, 5
EXSNF	External Sync Interrupt (False)	CSD0-CSD3	Decoded Address Bits 2, 3
REX	Read Execute	WEX	Write Execute
LRHR	Local Read Here	A10B-A07C	A-Register Bits
LWHR	Local Write Here	PFNS	Protect Fault Interrupt Status
LRRY	Local Read Ready	MCLF1	Master Clear Input
EXTSN	External Sync Input	LSTAF	Local Station (False)
LSTA1	Local Station Address NO. 1	LWRY	Local Write Ready
RS0F1-RS0F4	Gate Local Status (Address Zero)	FNTF1, FNTF2	Function False 1, 2
RS1F1-RS1F4	Gate System Status (Address One)		

FIGURE 3.21. FUNCTION CONTROL LOGIC (CARD 17)

3.10 RESPONSE CONTROL LOGIC (CARD 18)

The response control logic (Card 18), with the function control logic, maintains control of the responses sent to the computer. These responses include data inputs and the Reply, Reject, Character Input, and the Interrupt signal used by the DCT module. Table 3.2 lists the responses in order of precedence. The condition with the highest precedence determines the response; all other conditions are ignored.

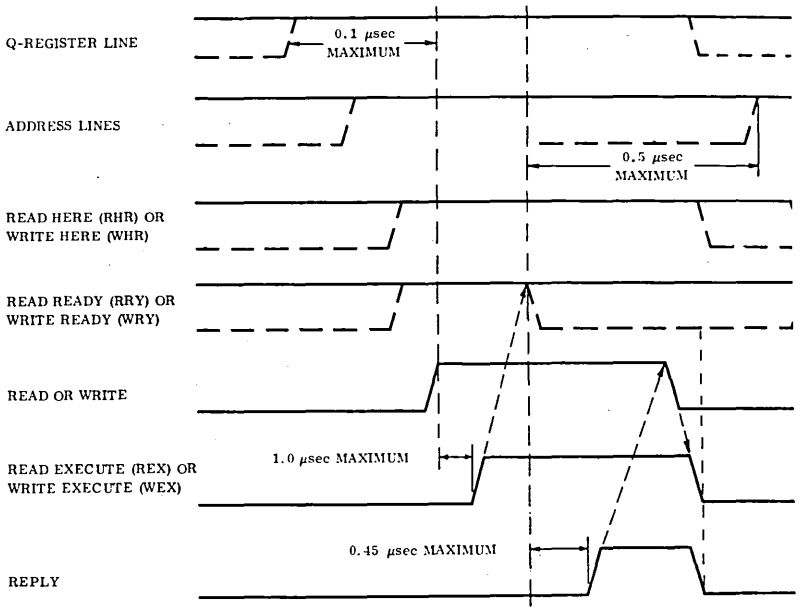
TABLE 3.2. RESPONSE PRIORITIES

PRECEDENCE	CONDITION	RESPONSE
1	Not connected and not a Connect command	None
2a	Unprotected command and PROTECT switch in position 2	Reject
2b	Unprotected command and PROTECT switch in position 3	Reply and Interrupt
3a	Addressed device Here and Ready:	
	Generate REX or WEX and wait 2 μsec from leading edge of Read or Write, then:	
	If Ready drops in time and RJT is false	Reply
	If Ready drops in time and RJT is true	Reject
	If Ready does not drop in time	None
3b	Addressed device Here but not Ready	Reject
3c	Addressed device not Here	None
4	1574 Sequential Addressing Unit not in system:	
	Sequential Setup or Sequential Status command	None
	Random Address command in mode 2 or 3	Reject
	Any No-Address command	Reject
5a	Station Address 00 and Write (set DCT functions)	Reply
5b	Station Address 00 and Read (present DCT status)	Reply
5c	Station Address 01 and Write (1573 Line Synchronized Timing Generator):	
	If 1573 not in system	None
	If 1573 interrupt sent	Reply
	If 1573 interrupt not sent	Reject
5d	Station Address 01 and Read (present system status)	Reply

NOTE: Cases 4 and 5 are special cases of 3.

3.10.1 Basic Response Timing

When a device is addressed, a response [Read Here (RHR) or Write Here (WHR)] is transmitted to the DCT. The addressed device transmits a Read Ready (RRY) or Write Ready (WRY) if ready to perform the specified operation. Upon receipts of a Read or Write command from the computer, the DCT examines the RHR, WHR, RRY, and WRY lines. If the device is both Here and Ready, a Read Execute (REX) or Write Execute (WEX) is transmitted to the device. The device acknowledges the Execute signal by dropping the Ready line, and a Reply (RPY) is transmitted to the computer. This description assumes the DCT is connected, no protect fault exist, and a Reject is not generated by the device. See Figure 3.22 for basic response timing.



NOTES:

A REJECT IS SENT INSTEAD OF A REPLY IF RJT IS TRUE WHEN READY DROPS.

A REJECT IS SENT INSTEAD OF AN EXECUTE IF THE ADDRESSED DEVICE IS HERE AND NOT READY.

NO RESPONSE IS SENT IF THE ADDRESSED DEVICE IS NOT HERE.

NO RESPONSE IS SENT IF READY DOES NOT DROP IN TIME (WITHIN 4.0 μSEC OF READ OR WRITE).

ADDRESS BEING INCREMENTED FOR SEQUENTIAL OPERATION (NO-ADDRESS COMMAND ONLY).

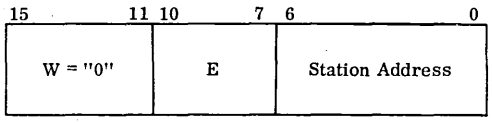
1-1347B

FIGURE 3.22. RESPONSE TIMING DIAGRAM

3.10.2 Command Formats

CONNECT

The format for Connect commands is shown below. A Connect command is defined as any command whose W-field is "0" and whose E-field matches the equipment number of the DCT. When any command is executed, a flip-flop in the DCT is set which allows Continue commands to be recognized. This "connected" flip-flop is reset by any command addressed to another equipment or by a Master Clear. It is not reset by a clear function.



CONNECT COMMAND FORMAT

Connect Flip-Flop

a. Set

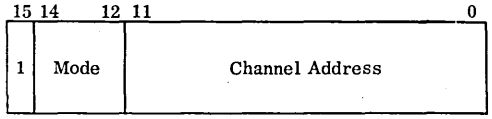
When the Connect (CNCT) input is true, the output of inverter B1A is false to inhibit resetting the connected flip-flop (E1). The input to inverter B1B is false, the output of B1B is true, and if a Read or Write input is true, the connected flip-flop is set. When true, the set output of E1 provides an enable input to the C1A inverter gate and provides the connect (CØNT) output. This output is used on Card 15 to enable the Character Input transmitter gate. The reset output of E1 provides a false signal for one input to the E2 inverter.

b. Reset

If the Connect (CNCT) input is false and the Q15F input (Not Continue) is true, or if the Connect Reset (CØNR) input is true, the Connected flip-flop is reset and remains reset until set as described above.

CONTINUE

The general format for Continue commands is shown below. A Continue command is defined as any command with a "1" in bit 15 when the connected flip-flop is set. The mode field is used by the 1574 Sequential Addressing Unit and 1571 Chaining Buffer Channel and must be "0" or "1" if the 1574 is not present in the system.



CONTINUE COMMAND FORMAT

3.10.3 Normal Response Sequence

During this sequence it is assumed that the DCT is connected, the device is Here and Ready, and no protect faults occur. When the Read or Write pulse goes true, the output of the Read or Write receivers goes true, providing one true input to inverter E5B. A true input is also provided to enable the input gates to inverter E4B (Device Response). The Read Ready or Write Ready signals provide another true input to the E4B gate, and the output of E4B goes false and remains false until the Read or Write Ready line is dropped.

E5B provides a false input to the TEX inverter (B3). The output of the E5B inverter also provides a false input to E4A (Read or Write) and the output of E4A comes true to start the 500-nanosecond Read or Write pulse delay and to start the 3.4-microsecond Internal Reject Delay at the input to the E4B inverter. Inverter D2A provides the 500-nanosecond Read or Write delay. The Read or Write pulse is delayed 500 nanoseconds after the leading edge of the Read or Write command pulse; then the output of D2A goes false, the output of D2B goes true and provides the input to start the Read or Write pulse at the input to E2, and the time-to-execute delay at the input to inverter C1A.

When the E2 inverter output comes true, the reset input gates to the Device-Not-Ready flip-flop (D3) are enabled. Since the device is both Here and Ready, all inputs to either the Read gate or the Write gate are true and the Device-Not-Ready (D3) flip-flop is reset.

The Read or Write pulse output of E2 remains true for 60 nanoseconds, as determined by the delay, and drops false after the delay time has elapsed.

When the output of D2B goes true, the input to C1A is delayed for 250 nanoseconds, as determined by the delay, and the output of C1A remains true during the 250-nanosecond delay time to inhibit the Time-to-Execute (TEX) inverter B3.

Inverter B3 acts as an inverted AND gate for the output of E5B (false at this time) and the output of C1A, which goes false at the end of the 250-nanosecond delay. When both of these inputs are false, the output of B3 comes true, providing a true state TEX (Time-to-Execute pulse), which is transmitted to the device.

Since the Device-Not-Ready reset output enabled the WEXT and REXT gates, and the Read Here or Write Here inputs provided a true input to these gates, the Write Execute (WEXT) or Read Execute (REXT) ouput comes true at the leading edge of the Time-to-Execute pulse, and TEX, WEXT or REXT remain true until the ready line is dropped by the device.

The response control logic of the DCT now waits for the addressed device to drop the Read Ready (RRYF comes true) or the Write Ready (WRYF comes true) line. When the ready line drops, the input to the Device Response inverter (E4B) goes false and the output of E4B becomes true, providing a true input to set the Reply (E3) flip-flop. The delay at the input of the set gate provides a 50-nanosecond delay which acts as a noise filter for the Reply flip-flop. When the set output of the Reply flip-flop comes true and the Reject flip-flop has not been set, a 450-nanosecond delay at the input to the Reply transmitter (D4 and C4) is started to allow the Reply flip-flop to settle. After the 200-nanosecond delay time has elapsed, the input to the Reply transmitter comes true and the reply is transmitted to the computer.

After the computer receives the reply, the Read or Write command line is dropped, causing the output of E5B to go true dropping TEX and WEXT or REXT, and resetting the Reply flip-flop.

E5B also provides a true input to E4A, the false output of E4A provides an input to D2A. The true output of D2A sets the Device-Not-Ready (D3) flip-flop, which disables the REXT and WEXT output gates. The D2A output is coming true and also provides a true input to D2B, and the output of D2B goes false. The DCT is now in the Ready state for the next command.

3.10.4 Device Protect Sequence

The unprotect false (UNPF) line of the decoded data channel is used to inhibit the normal use of the DCT PROTECT switch. When this input is false (0 volts), the addressed station accepts all commands with the proper station address.

If the device has a Program Protect switch, the switch controls the protect responses. If the device has no switch and accepts unprotected commands, the UNPF line is false when the device is addressed.

If the UNPF line is true when a station is addressed, the station is protected against protect faults by the PROTECT switch in the DCT. The UNPF line, when false, provides the response control logic inputs (UNP2 and UNP3). Both these inputs are true when the UNPF line is false.

If the UNP2 and UNP3 inputs are true and the device addressed is a station, the AND gate inputs to inverters C1B and E5A are both true. The outputs of these inverters provide false inputs for the Execute Enable inverter (D1B). Since the DDT input is normally false, the output of D1B is true. The result of this is that the PROTECT switch on the DCT (providing inputs PRØ2 and PRØ3) is ignored, and the Enable Execute is true regardless of the state of the Program Protect bit during the present command.

When the UNPF input is in the true state, the addressed device is protected by the PROTECT switch of the DCT. If the UNPF line is true, UNP2 and UNP3 are false, and the AND gate inputs to inverters C1B and E5A are disabled. In this condition the response depends upon the setting of the DCT PROTECT switch as described below, with normal responses occurring unless there is a protect fault.

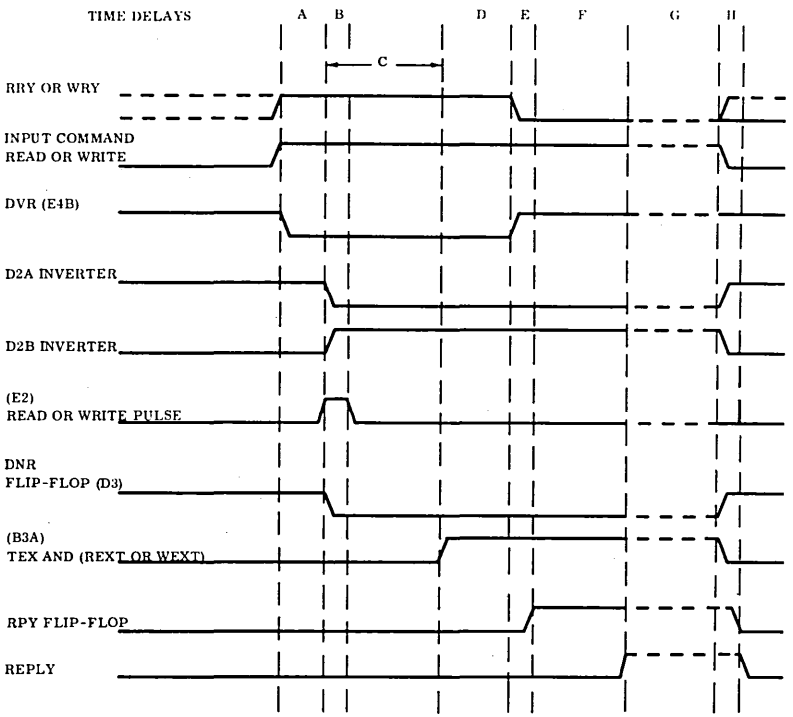
DEVICE PROTECTED WHEN AN UNPROTECTED COMMAND OCCURS

PROTECT Switch in Position 2

With the PROTECT switch in position 2, the input to inverter C1B (the Program Protect bit of the command PR02) is false, and the output of C1B is true, disabling the D1B inverter (Disables Execute) and enabling the input gate to the reject transmitter. This allows a Reject to be transmitted directly during Time-to-Execute (TEX). During this response cycle, the Ready lines from the device, and the state of the Device Ready inverter (E4B) are ignored, the Device-Not-Ready flip-flop (D3) is not reset, and the response cycle proceeds normally, except for these alterations: the Reply and Reject flip-flops are not set and the Reject signal is transmitted during TEX time. The computer responds by dropping the Read or Write command and the DCT cycles out, resetting the response logic to the Ready state for the next command.

PROTECT Switch in Position 3

With the PROTECT switch in position 3, the response cycle proceeds as described above except that the output of inverter E5A provides a true signal to enable the set input of the Reply flip-flop and to enable the Protect Fault Interrupt (PFNS) output gate. When the Read or Write pulse comes true, the Reply flip-flop is set, and the Protect Fault Interrupt output comes true and is transmitted to the computer. The Reject flip-flop (C3) is not set during this cycle, so the input gate to the Reply transmitter is enabled. When the Reply flip-flop set output comes true and after the 200-nanosecond delay time has elapsed, a Reply is sent to the computer. The computer responds by dropping the Read or Write command, and the DCT cycles out to the Ready state for the next command. Figure 3.24 shows the timing of both sequences described above.



TIME DELAY DESCRIPTIONS

A	500 ηs	ALLOWS CONNECT FLIP-FLOP TO SETTLE.
B	60 ηs	LEADING EDGE DETECTOR PULSE USED AS STROBE .
C	250 ηs	COMBINED WITH TIME DELAY B, ALLOWS 250 ηs FOR DNR FLIP-FLOP TO SETTLE.
D	0-2 μsec	WAITING FOR RESPONSE.
E	50 ηs	NOISE FILTER FOR REPLY.
F	200 ηs	ALLOWS RPY FLIP-FLOP TO SETTLE.
G	INDETERMINATE	COMPUTER RESPONSE TIME TO DROP READ OR WRITE.
H	≈20 ηs	REPLY (F) DELAY DISCHARGE.

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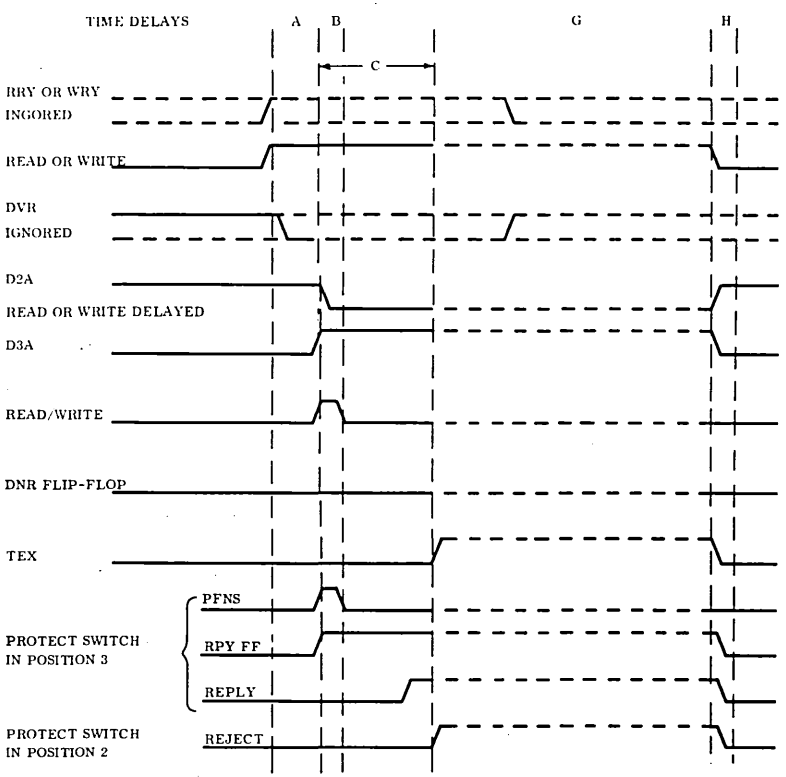
FIGURE 3.23. NORMAL RESPONSE CYCLE



TIME DELAY DESCRIPTIONS

A	500 ηs	ALLOWS CONNECT FLIP-FLOP TO SETTLE.
B	60 ηs	LEADING EDGE DETECTOR PULSE USED AS STROBE.
C	250 ηs	COMBINED WITH TIME DELAY B, ALLOWS 250 ηs FOR DNR FLIP-FLOP TO SETTLE.
D	0-2 μsec	WAITING FOR RESPONSE.
E	50 ηs	NOISE FILTER FOR REPLY.
F	200 ηs	ALLOWS RPY FLIP-FLOP TO SETTLE.
G	INDETERMINATE	COMPUTER RESPONSE TIME TO DROP READ OR WRITE.
H	≈20 ηs	REPLY (F) DELAY DISCHARGE.

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FIGURE 3.24. DEVICE PROTECT CYCLE

3.10.5 Internal Reject Sequence

If the addressed device responds as Here and Ready, the Device Ready inverter (E4B) output goes false as described in the normal response sequence, and the timing sequence proceeds as in the normal sequence. A Read or Write pulse is generated, the Device-Not-Ready flip-flop is reset, and the REX and WEXT or REXT outputs come true.

The DCT is then waiting for the device to drop the ready line to acknowledge execution of the command. If the device never drops the ready line during the 2-microsecond interval specified, the Device Ready inverter (E4B) remains inhibited by the 3.4-microsecond delay. The output of E4B never comes true, the Reply flip-flop is never set, and the computer does not receive a response.

After the time delay set for Internal Reject within the computer, the computer generates an Internal Reject signal for use by the program for recognition of the fault, and the computer drops the Read or Write command. The Response logic then cycles out to the Ready state, as described in the normal response sequence. Figure 3.25 shows the timing of this internal reject sequence described above.

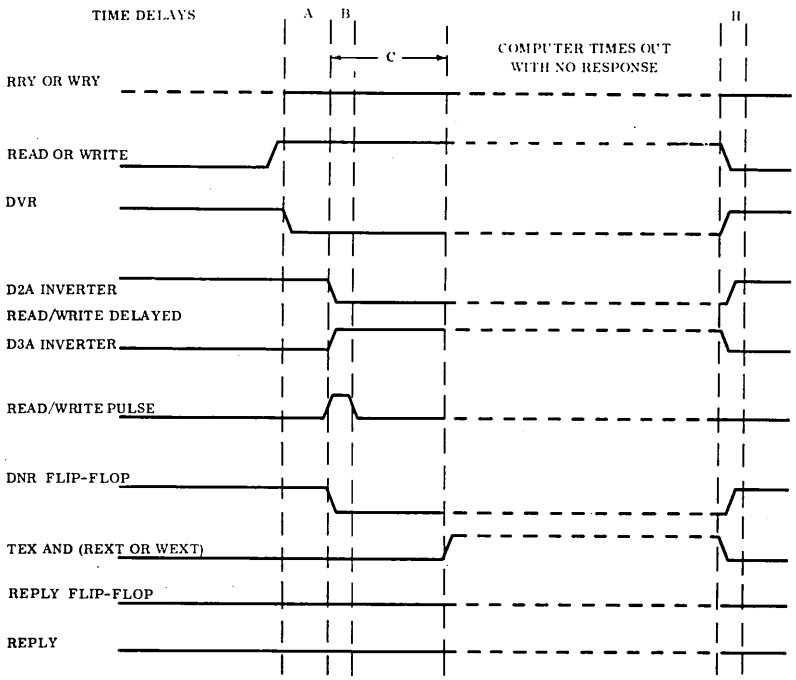


FIGURE 3.25. INTERNAL REJECT CYCLE

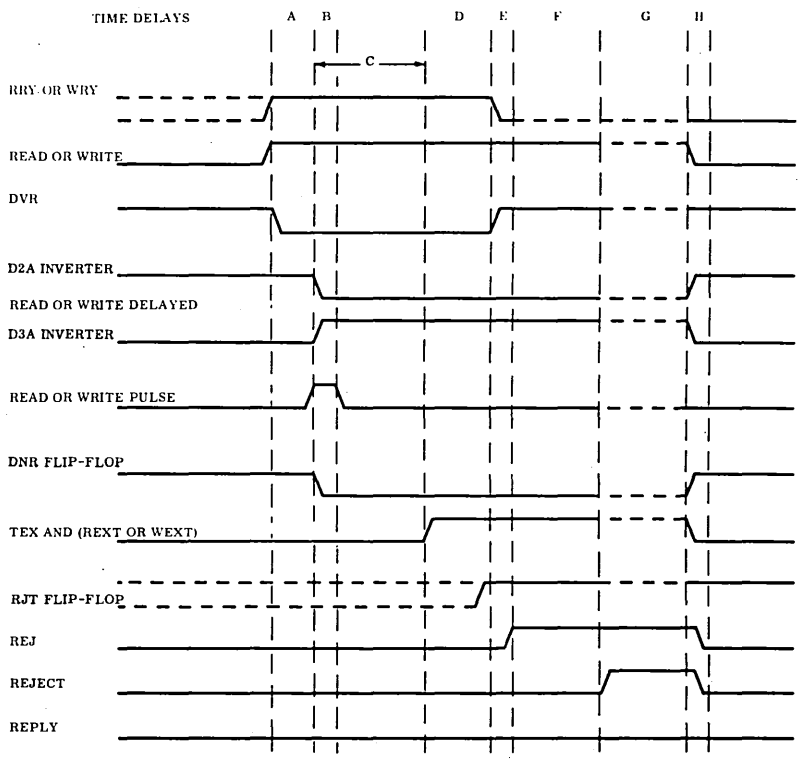
3.10.6 Device Rejects Execution Command Sequence

Stations can inhibit execution of commands by the Reject False (RJTF) input. When the RJTF input is false (indicating of execution), the output of the Reject inverter (D1A) is true, enabling the set input gate to the Reject flip-flop (C3).

The first portions of the timing cycle are normal, but when the TEX (time-to-execute) signal comes true, the Reject false input goes true in the device and is transmitted to the DCT. The output of D1A, now true, is AND'ed with the output of E4B (Device Response) and the reset output of the Device-Not-Ready flip-flop (D3), setting the Reject flip-flop.

The Reject flip-flop reset output (now false) inhibits the Reply transmitter input gate, and the set output starts a 200-nanosecond delay/reject at the input of the transmitter, to allow the Reject flip-flop to settle. When the delay time has elapsed, the Reject signal is transmitted to the computer, and the computer responds by dropping the Read or Write command as described in the normal sequence description.

Figure 3.26 shows the timing during the device reject sequence described above.



1-1327A

NOTE: FOR TIME DELAY DESCRIPTIONS, SEE FIGURE 3.24.

FIGURE 3.26. DEVICE REJECT CYCLE

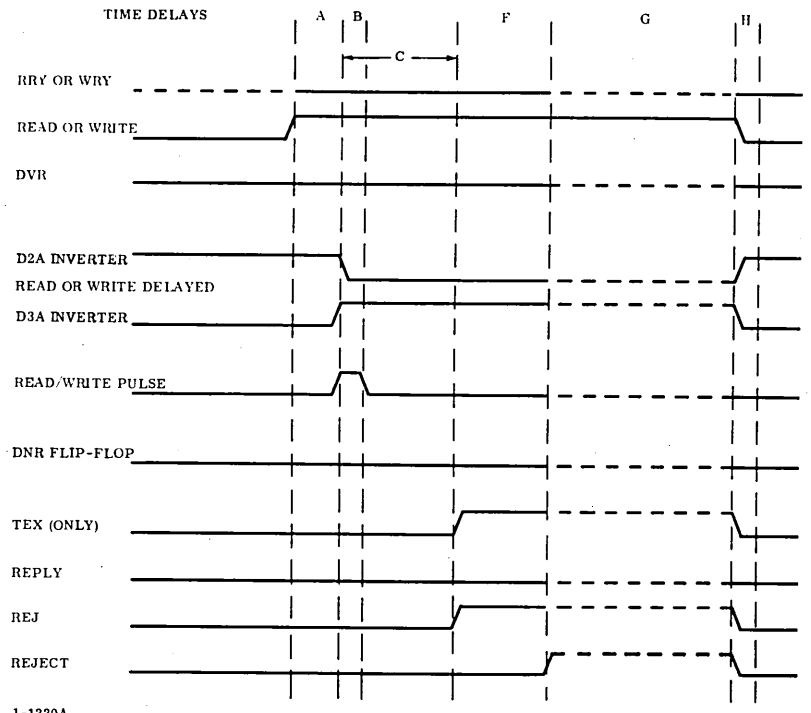
3.10.7 Device Here But Not Ready Sequence

If the addressed device is Here But Not Ready, the RRYF input (Read Ready false) remains true and the output of inverters D5A (Write Ready) or D5B (Read Ready) remains false causing the Device Ready inverter (E4B) output to remain true.

The Read or Write pulse is generated as in the normal sequence, and the Time-to-Execute (TEX) output comes true, but the WEXT or REXT gates are not enabled (since the Device-Not-Ready flip-flop was not reset), and the WEXT or REXT outputs remain false.

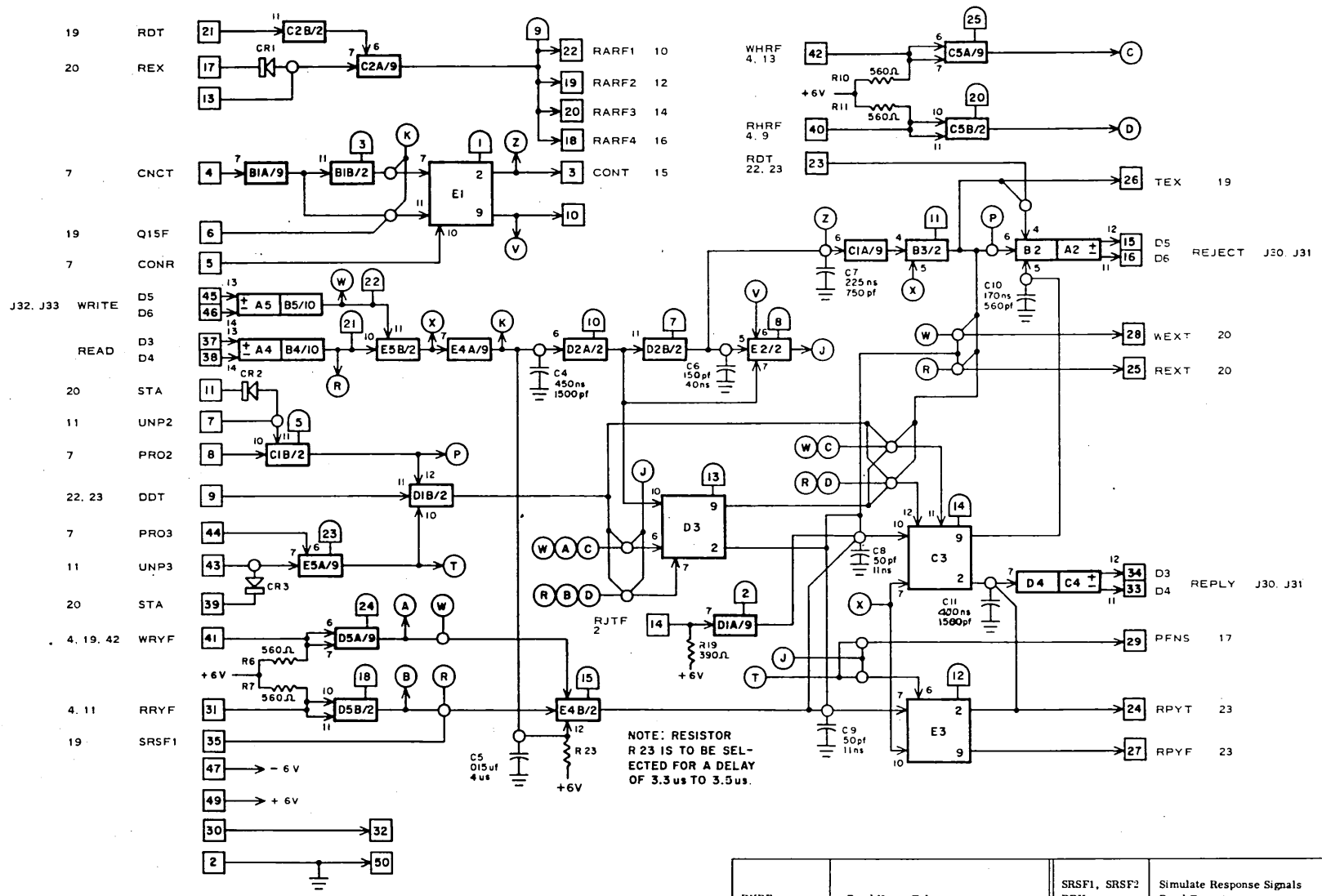
With the Device-Not-Ready flip-flop still set and the Device Here inverter, Read Here (C5A) or Write Here (C5B) output true, the Reject flip-flop set input gate is enabled, and the flip-flop is set when TEX comes true. The Reply is inhibited by the reset side of the Reject flip-flop (now false), and the set side starts the delay at the input to the reject transmitter. After the delay time, the Reject signal is transmitted and the computer responds by dropping the Read of Write command. The response logic cycles out to the Ready state as described in the normal sequence. Figure 3.27 shows the timing of the device here and not ready sequence described above.

Figure 3.28 is a logic diagram of Card 18.



NOTE: FOR TIME DELAY DESCRIPTIONS, SEE FIGURE 3.24.

FIGURE 3.27. DEVICE HERE BUT NOT READY CYCLE



	A	B	C	D	E
1		D24	D24	D34	F24
2	T31B	T01A	D24	D24	I48
3		I48	F34	F24	F24
4	R01A	R01B	T31B	T01A	D34
5	R01A	R01B	D24	D24	D24

CARD TYPE: BB
CARD TITLE: Response Control
CARD DRAWING NO.: 38896800
LOGIC DRAWING NO.: 38952600, Sheet 18

		SRSF1, SRSF2	Simulate Response Signals
RHRF	Read Here (False)	REX	Read Execute
WHRF	Write Here (False	CNCT	Connect
RARF1-RARF4	Read Data Enable	Q0-Q15	Q-Register Inputs
CONT	Connect Signal	CONR	Reset
RDT	Reject Data Transfer EDT	UNP2, UNP3	Unprotected
	(NAD + RAL)	PRO2, PRO3	PROTECT Switch in Positions 2, 3
TEX	Time-to-Execute Pulse	DDT	Disable Data Transfer EDT
WEX	Write Execute		(NAD + RAL)
PFNS	Protect Fault Interrupt Status	WRYF	Write Ready (False)
RPYT, RPYF	Reply True, False	RRYF	Read Ready (False)

FIGURE 3.28. RESPONSE CONTROL LOGIC (CARD 18)

3.11 ADDRESS CONTROL LOGIC (CARD 19)

The address control logic is implemented by the printed circuit card in position 19 (see Figure 3.29) and provides decoding for Q00, Q04 through Q06, and Q12 through Q15. These inputs from the Q-register of the computer are combined in various ways described below to form the control signals to determine the addressing modes.

3.11.1 No-Address (NAD)

When Q04, Q05, and Q06 are all true and Q15 is false, the input to inverter C4B is true. The output of C4B, when false, disables the input gates to C4A, and the STAT output gate. The output of C4A is inverted by D5A to provide a true NAD output and to enable the input gate to E3A. The NAD output, when true, specifies a No-Address data transfer command used for direct I/O with no address.

3.11.2 Station Address (STAT)

The Station Address true (STAT) output is true if the NAD output is false and Q15 is false. This output indicates that the device being addressed is a station and is true only during Function and Connect or Status and Connect commands. The STAT output is transmitted on the DCB and is also used to enable the inhibit gate for the protect fault reject logic on Card 18.

3.11.3 Channel Address (CHLT)

The Channel Address True (CHLT) output indicates that a channel is being addressed and is true for direct I/O commands and all random-addressing commands.

The output of inverter C4B provides a false input to both gates of inverter C4A whenever the direct I/O commands are used. This makes the CHLT output true during these commands.

When Q15 is true, the output of inverter E4 is false, providing a false input to one of the gates to C4A. If Q14 is false, which it is during Random Address commands, the output of the Q14 receiver provides a false input to the other gate of C4A. With both input gates having false signals, the output of C4A (CHLT) is true.

3.11.4 Write Ready (WRYF)

The Write Ready False (WRYF) output is normally true. A Local Write Ready signal (LWRY going true or LWRYF going false) creates a Write Ready condition causing WRYF to go false. It is necessary for Write Ready to drop (WRYF going true) to cause a response. This is inhibited if the output of inverter D4B is true. The output of D4B is true for any Read Only command, as determined by the inputs to E3A, NAD (No-Address) AND'ed with Q0 (Inhibit Execute) and Random Address Read only (Q15 set and Q12, Q13, and Q14 reset).

3.11.5 Q07A

This output is connected with the output of another inverter at the input of logic cards in positions 22 (Address Decoder) and 25 (1574 Sequential Addressing Unit). The two inputs to these cards (Q15 and Q07) are AND'ed to form the final input signal.

When Q15 is false, the Q07 input to the cards is inhibited from the decoding logic. Since a station address consists only of bits Q00 through Q06, the Q07 bit is only inhibited during those commands associated with station addresses. When the address is a channel, the Q07 bit is used in the address decoding.

3.11.6 Q15F

For this output Q15 is inverted and is provided as an output to the response control logic (Card 18). Q15F in the True state enables the reset input gate to the Connect flip-flop, allowing the Connect flip-flop to be reset. Q15F in the False state inhibits the reset gate of the Connect flip-flop, and thus specifies a Continue command, as Q15F is false only during those commands when Q15 is true (Random Addressing and Sequential Addressing).

3.11.7 Read Execute (REXT) and Write Execute (WEXT)

The Read Execute (REXT) and Write Execute (WEXT) outputs are used for all data transfers, unless inhibited, and are false only during direct I/O commands with Q00 false or during Random Address Read Only commands. In all other cases either REXT or WEXT is true for a time specified by the response control logic. They will come true at the leading edge of the Time-to-Execute (TEX) pulse, unless inhibited by a Read Only command.

The conditions creating a false output for these signals are described above in the WRYF descriptions.

3.11.8 Q00A and Q00B

The Q00 outputs are true whenever the Q-register bit 00 is true. They are used to inhibit execution of commands in the No-Address mode as described above and also to provide outputs used by the Address Decoder and the 1574 Sequential Addressing Unit.

When the Address Decoder is installed, Q00 is combined with Q01 to form the CSE0-CSE3 addressing outputs. When the 1574 is installed, Q00 is used as the set input to the least significant bit of the address registers.

3.11.9 Simulate Response

The Simulate Response signals (SRSF1 and SRSF2) are normally true, enabling the normal responses described above. However, for any Read Only command, WEXT and REXT outputs are inhibited. Therefore, the addressed device does not respond by dropping its Ready signal (RRY or WRY going false). The input gate to D4B (Read Only and TEX) causes SRSF1 and SRSF2 to go false when the Time-to-Execute (TEX) pulse occurs. The SRSF1 and SRSF2 outputs go to Card 18 to cause the AR lines to be gated to the A-read line transmitters and to provide inputs to simulate the RRYF output to go true (Read Ready dropping).

This group of control signals is used for all sequential addressing modules.

3.11.10 Sequential Address Setup or Status (SASS)

This control signal is used when a sequential address module is being addressed. It is used by the 1574 as well as by other sequential addressing modules external to the DCT package (e.g., 1797/1571).

When both Q14 and Q15 are true, the inputs to E2B and E4 inverters are true, and the outputs provide false inputs to inverter E3B. With both these inputs false, the output (SASS) is true. When Q15 is true and Q14 is false (during Random Address mode commands), the SASS output is false.

3.11.11 SAM1T and SAM2T

These two signals are used for control of special sequential addressing modules other than the 1574 (1797/1571). Commands controlling these modules are programmed in the Sequential Setup and Sequential Status formats, which are defined as commands having both Q14 and Q15 set ("1's"). When both Q14 and Q15 are true, the outputs of inverters E2B and E4 (both false at this time) provide inputs to inverter E3B, which acts as an inverted AND gate for False State signals and provides a true output (SASS). The Sequential Address or Setup (SASS) output enables the output gates for SAM1T and SAM2T. If Q12 is true, the SAM1T output is true, and if Q13 is true, the SAM2T output is true.

3.11.12 Random Address and Lockup (RAL)

During the Random Address and Lockup commands, which are rejected if the 1574 Sequential Addressing Unit is not installed, a data transfer is executed at the specified address and the next address is set equal to the address specified by the current command.

During the Random Address and Increment commands, also rejected if the 1574 is not installed, a data transfer is executed at the specified channel address and the next address is set to one greater than the address specified by the current command.

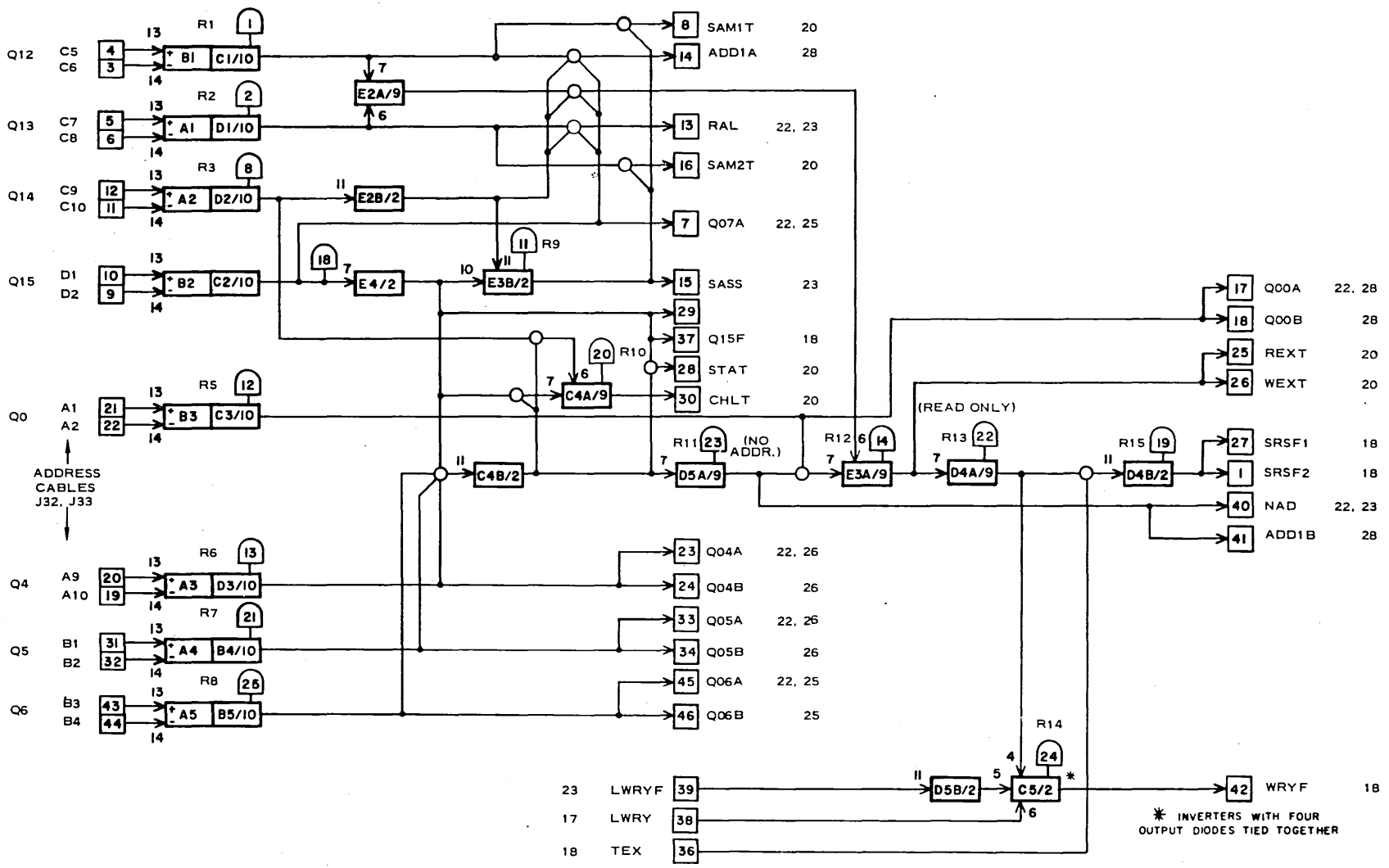
The RAL signal is gated by the Address Decoder logic (Card 18) to cause a Reject Data Transfer (RDT) and a Disable Data Transfer (DDT) if the Address Decoder is installed in addition to the 1574.

The RAL output is decoded from Q13, Q14, and Q15. When Q13 is true, Q14 is false, and Q15 is true, all three inputs to the RAL gate are true, and the RAL signal is available for gating on other logic cards. If any one or more of the inputs is false, the RAL output is disabled.

3.11.13 ADD1A and ADD1B

These outputs are used to increment the Address register of the 1574 during the RAL commands described above. ADD1A is true during Random Address commands when Q12 is true and increments the Next Address register during RAL commands (Random Address and Increment).

ADD1B and Q01 are AND'ed at the input to the 1574 (Card 27) and increment the Next Address register when Q01 is true during a No Address command.



	A	B	C	D	E
1	R01A	R01A	R01B	R01B	
2	R01A	R01A	R01B	R01B	D24
3	R01A	R01A	R01B	R01B	D24
4	R01A	R01B	D24	D24	I48
5	R01A	R01B	I45	D24	

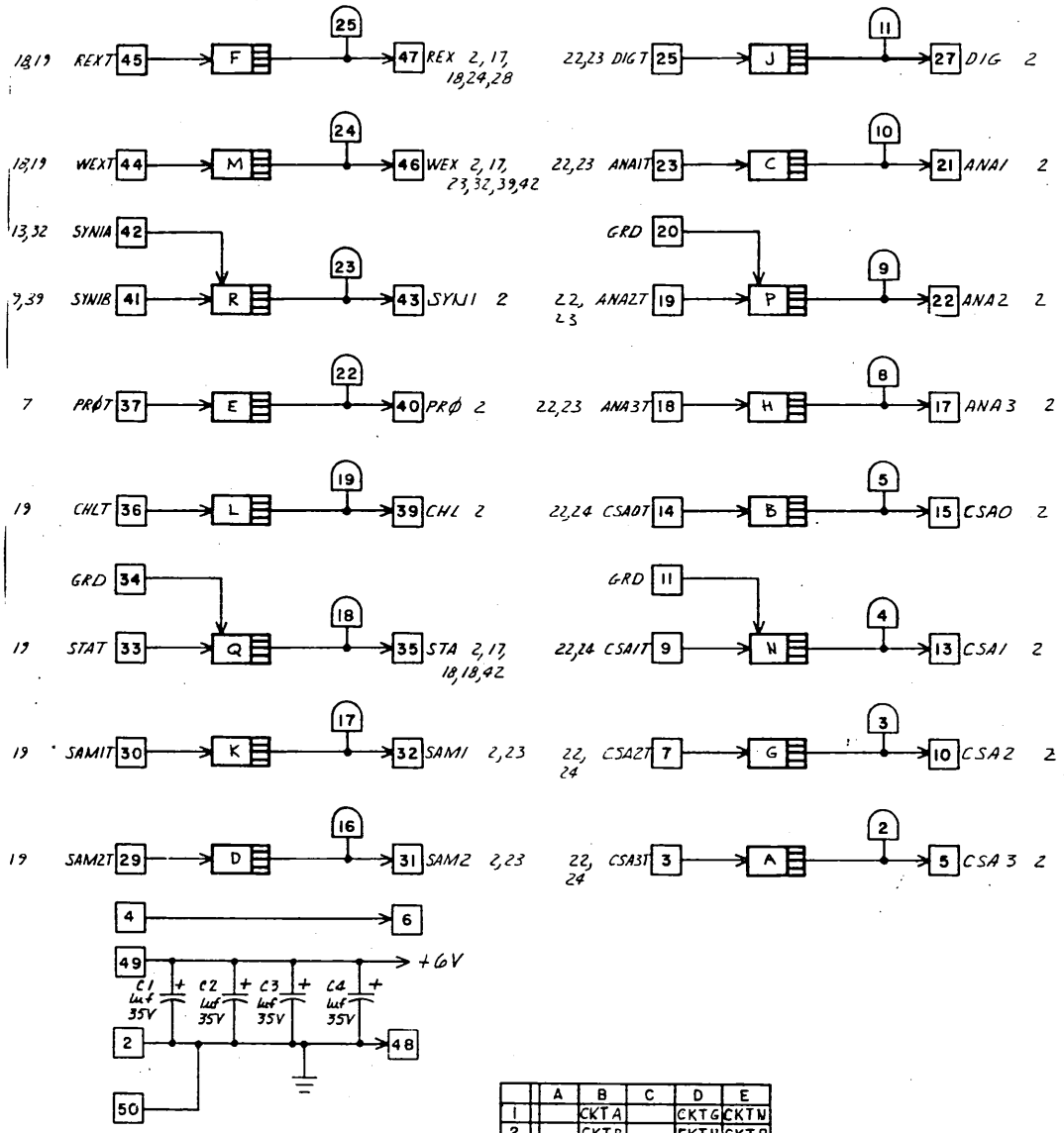
CARD TYPE: BH
CARD TITLE: Address Control
CARD DRAWING NO.: 38896900
LOGIC DRAWING NO.: 38952600, Sheet 19

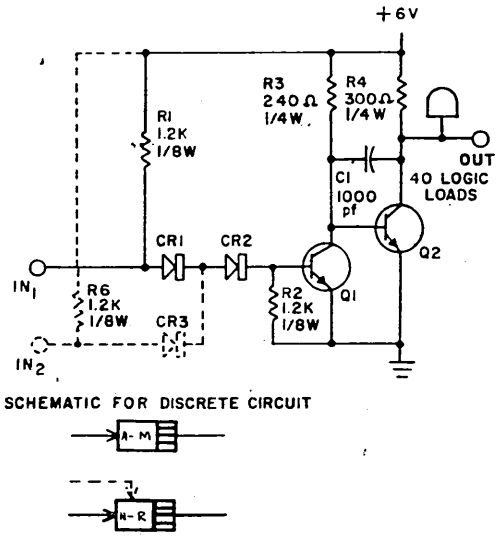
SAM1T	Sequential Address Module 1	STA	Station Address
ADD1A	Add "1" to 1574 Register (Q12 · Q14 · Q15)	CHL	Channel Address
		NAD	No Address
Q0-Q15	Q-Register Inputs	ADD1B	Add "1" to 1574 Register (No Address · Q01)
RAL	Random Address and Lockup		
SAM2T	Sequential Address Module 2	LWRY	Last Address Write Ready
Q00A-Q15B	Condition Q-register Bits	SRSF1, 2	Simulate Response Signals
SASS	Sequential Address and Setup	WRYF	Write Ready (False)

FIGURE 3.29. ADDRESS CONTROL LOGIC (CARD 19)

3.12 LONG-LINE DRIVERS (CARDS 20 AND 21)

The line drivers provided on the printed circuit cards in card positions 20 and 21 provide noninverting amplification of the signals connected to the Data and Control Bus. Figures 3.30 and 3.31 are logic diagrams of the Long-Line Drivers (Cards 20 and 21). The line drivers provide sufficient amplification for driving 40 normal loads. An isolation diode must be provided for each load on each line.





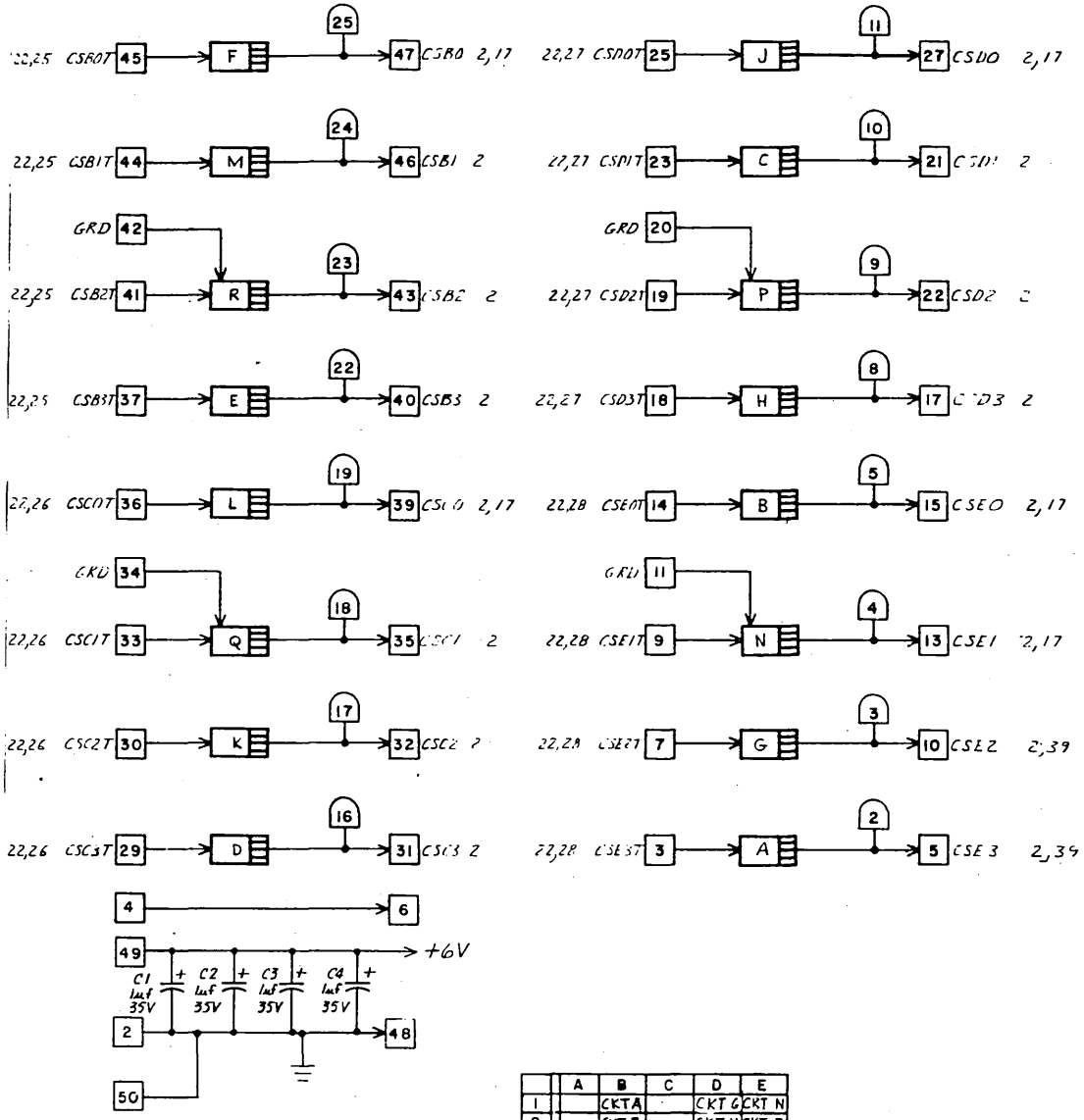
SCHEMATIC FOR DISCRETE CIRCUIT

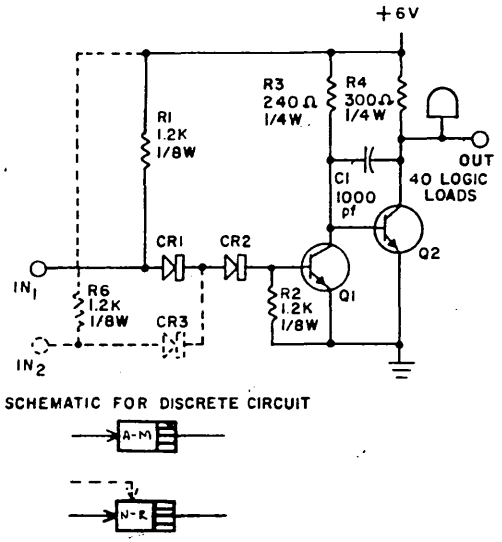
	A	B	C	D	E
1		CKTA		CKTG	CKTN
2		CKTB		CKTH	CKTP
3		CKTC		CKTJ	
4		CKTD		CKTK	CKTQ
5		CKTE		CKTL	CKTR
6		CKTF		CKTM	

CARD TYPE: BM
CARD TITLE: Long Line Drivers
CARD DRAWING NO.: 38897100
LOGIC DRAWING NO.: 38952600, Sheet 20

REX	Read Execute
WEX	Write Execute
SYN1	Sync Source NO. 1
PRO	Protected Command
CHL	Channel Address
STA	Station Address
SAM1-SAM2	Sequential Addressing Module 1, 2
DIG	Digital Input or Output (Address 0XX)
ANA1-ANA3	Analog NO. 1, 2, 3
CSA0-CSA3	Decoded Address Bits 8, 9

FIGURE 3.30. LONG-LINE DRIVERS (CARD 20)





SCHEMATIC FOR DISCRETE CIRCUIT

	A	B	C	D	E
1		CKT A		CKT G	CKT N
2		CKT B		CKT H	CKT P
3		CKT C		CKT J	
4		CKT D		CKT K	CKT Q
5		CKT E		CKT L	CKT R
6		CKT F		CKT M	

CARD TYPE: BM
CARD TITLE: Long Line Drivers
CARD DRAWING NO.: 38897100
LOGIC DRAWING NO.: 38952600, Sheet 21

CSB0-CSB3	Decoded Address Bits 6, 7
CSC0-CSC3	Decoded Address Bits 4, 5
CSD0-CSD3	Decoded Address Bits 2, 3
CSE0-CSE3	Decoded Address Bits 0, 1

FIGURE 3.31. LONG-LINE DRIVERS (CARD 21)

3.13 ADDRESS DECODER (CARD 22)

The Address Decoder (Card 22) provides inverters and gates for partially decoding the Q-register inputs; these inputs have, in some cases, terms AND'ed for additional control features and are not the actual A-Register contents. Each set of four inverters decodes two input bits in straight binary fashion as shown in Table 3.3.

TABLE 3.3. TYPICAL TRUTH TABLES

Q01A	Q00A	TRUE OUTPUT	COMBINATION	Q11A	Q10A	TRUE OUTPUT	COMBINATION
0	0	CSE0T	$\overline{Q01A}\ \overline{Q00A}$	0	0	DIGT	$\overline{Q11A}\ \overline{Q10A}$
0	1	CSE1T	$\overline{Q01A}$ Q00A	0	1	ANA1T	$\overline{Q11A}$ Q10A
1	0	CSE2T	Q01A $\overline{Q00A}$	1	0	ANA2T	Q11A $\overline{Q10A}$
1	1	CSE3T	Q01A Q00A	1	1	ANA3T	Q11A Q10A

Two additional inverters and several input and output pins are used to provide interlocking controls for the Address Decoder (see Figure 3.32).

3.13.1 No Address

The NAD input (No Address is decoded from the Q-register bits to indicate a direct I/O command with no address associated with the command.

3.13.2 Enable Data Transfer

The EDT (Enable Data Transfer) is a pin which is grounded by each card of the 1574, thus providing a false signal input to the Address Decoder when the 1574 is also installed.

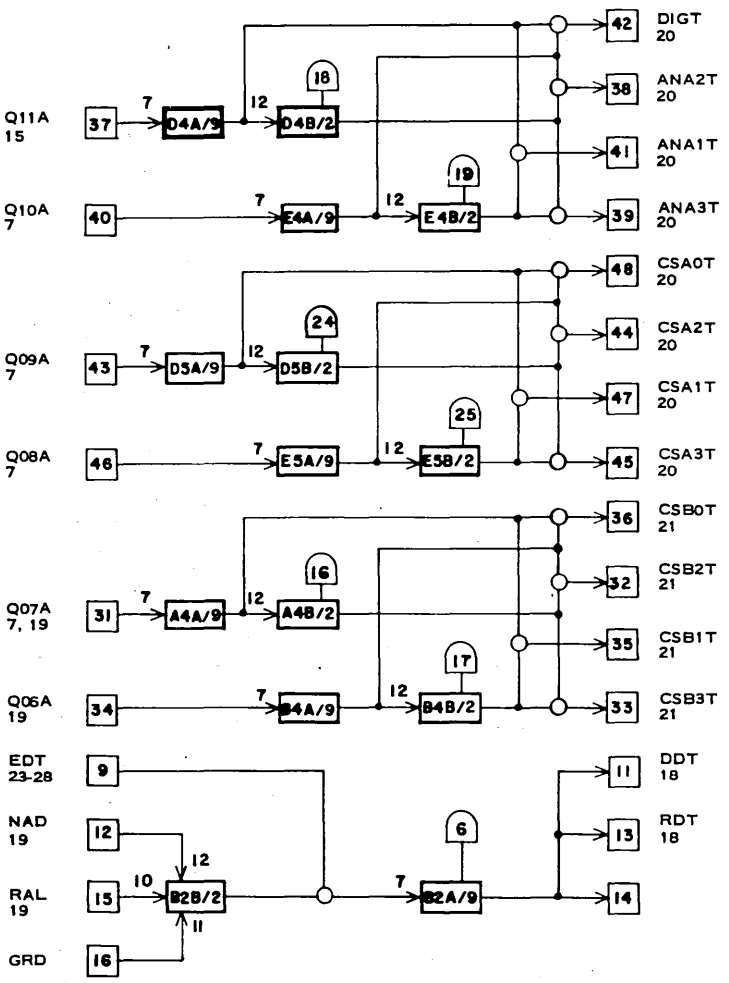
3.13.3 Random Access Lockup

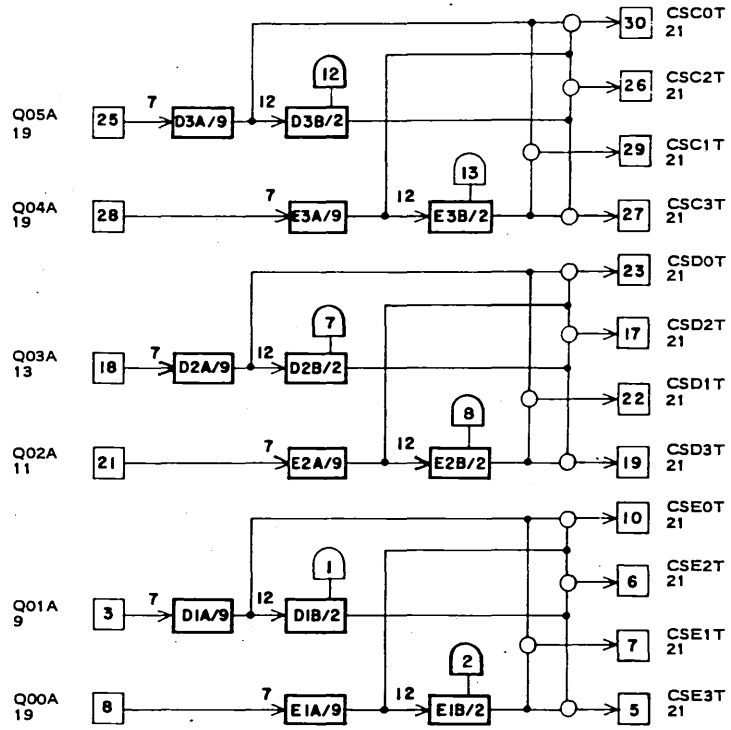
The RAL input is the Random Access Lockup signal used for the 1574 and is not used in the Address Decoder. The B2A inverter acts as a NOR gate for the EDT, NAD, and RAL inputs.

If RAL or NAD come true or if the EDT input is held at ground by any of the 1574 cards installed, the DDT (Disable Data Transfer) and the RDT (Reject Data Transfer) outputs of the card are true, thus disabling and rejecting any transfer of data. This interlocking system provides protection for misplacement of hardware and programming errors.

3.13.4 End of Sequence

The EØS output pin is grounded by the Address Decoder to provide a continuously false EØS output when the Address Decoder is installed. This output and DDT and RDT outputs disable the 1574 if the Address Decoder is installed. This provides bilateral protection for both the Address Decoder and the 1574.





NOTE: THIS CARD IS REMOVED WHEN THE SEQUENTIAL ADDRESSING OPTION IS ADDED TO THE 1750.

	A	B	C	D	E
1				D34	D34
2		D34		D34	D34
3				D34	D34
4	D34	D34		D34	D34
5				D34	D34

CARD TYPE: BE
CARD TITLE: Address Decoder
CARD DRAWING NO.: 38882200
LOGIC DRAWING NO.: 38925600, Sheet 22

Q00A-Q15B	Condition Q-Register Bits	CSB0T-CSB3T	Decoded Address Bits 6, 7 (True)
EDT	Enable Data Transfer (Grounded by Cards 23-28)	DDT	Disable Data Transfer EDT (NAD + RAL)
NAD	No-Address	RDT	Reject Data Transfer EDT (NAD + RAL)
RAL	Random Address and Lockup		
DIGT	Digital Input or Output (Address 0XX)	CSC0T-CSC3T	Decoded Address Bits 4, 5 (True)
ANA1T	Analog 1 (Address 4XX) (True)	CSD0T-CSD3T	Decoded Address Bits 2, 3 (True)
ANA2T	Analog 2 (Address 8XX) (True)	CSE0T-CSE3T	Decoded Address Bits 0, 1 (True)
ANA3T	Analog 3 (Address CXX) (True)	EOS	End of Sequence (Grounded by this card)
CSA0T-CSA3T	Decoded Address Bits 8, 9 (True)		

FIGURE 3.32. ADDRESS DECODER (CARD 22)

Section Four
MAINTENANCE

4.1 GENERAL

Corrective maintenance procedures, parts removal, and parts replacement can be found in Control Data publication NO. 84785000. This section provides only fundamental preventive maintenance instructions and procedures. Since the DCT is located in a cabinet that includes other modules, some maintenance procedures include the other modules as well as the DCT.

4.2 PREVENTIVE MAINTENANCE PROCEDURES

Preventive maintenance includes two basic procedures:

a. Inspect modular cabinet MG air filters and clean as necessary every two to three weeks.

b. Check output of MG power supply at least once a month. The MG power supply contains a variac with which the output voltage can be varied to compensate for additional module loading. Whenever modules are added or deleted, check output voltage and adjust the variac for 208 volts output.

4.3 TROUBLESHOOTING PROCEDURES

There are no normal troubleshooting procedures besides chasing "1's" and "0's." The response control Card 18 (Figure 3.28) contains the response delay for the Reply signal. Resistor R23 is selected to adjust for a nominal response delay of from 3.3 to 3.5 microseconds.

4.4 PREVENTIVE MAINTENANCE INDEX

TIME EST. MINS.	LEVEL	ITEM	PREVENTIVE MAINTENANCE
5	Monthly	1.1	Clean Air Filter
5	Monthly	1.2	Check Cooling
2	Monthly	1.3	Check Power Supplies
40	Bi-Monthly	2.1	Voltage Margins

"This PMI is the recommended frequency of performing preventive maintenance on this equipment. Scheduling of this preventive maintenance is a site responsibility. Scheduling may include variations in the recommended frequency due to individual site conditions (e.g., usage, environment, time, etc.)."

CLEAN AIR FILTER

CHECK/Conditions

1. 60 Hz power off.
2. Snap plate at front bottom of cabinet removed

Action

1. Vacuum both sides of filter element thoroughly.
   a. If filters are very dirty, wash them in a mild detergent-water solution.
   b. Place filters vertically while drying to avoid damage.

CHECK COOLING

CHECK/Condition	Action
1. 60 Hz power off. CHECK: Is the red light on at the bottom of the cabinet?	
Yes ↓	No → 1. Check operation of vane switch. 2. Check for presence of 60 Hz or 400 Hz on either side of lamp. 400 Hz on one side turns on the lamp, while 60 Hz at the other side keeps it off.
2. 60 Hz power turned on. CHECK: Does air circulate upwards through entire cabinet?	
Yes ↓	No → 1. Verify blower is operating. 2. Check for any unnatural obstructions. 3. Verify there is a proper allowance for air to move under cabinet, through filters and up.
Next Item	

CHECK POWER SUPPLIES

CHECK/Condition	Action
1. Verify power supplies are creating +6 VDC and -6 VDC.	

CHECK: Is the proper voltage present?

Yes

No → 1. Check fuse.
2. Check 400 Hz supplied to power supply.
3. Check for any wiring shorts.

2. Verify termination power (±20 VDC) is supplied to the module.

RUN VOLTAGE MARGINS

CHECK/Condition	Action
1. Insure system is configured for running of appropriate diagnostic for equipment on 1750. (Interrupts equipment number, proper inputs or outputs for diagnostic used, . . .)	
2. Optional testing could be performed to verify operation of master clear button, equipment number switch and protect switch depending on whether customer desires to use these features as variables.	
3. Run the diagnostic and shock test the 1750 module*	

CHECK: Are there any errors?

No

Yes → 1. Isolate and/or replace shock sensitive card or component.

4. Re-run the diagnostic at ±10% power supply margins.

CHECK: Are there any errors:

No

Yes → 1. Isolate and/or replace marginal card or component.

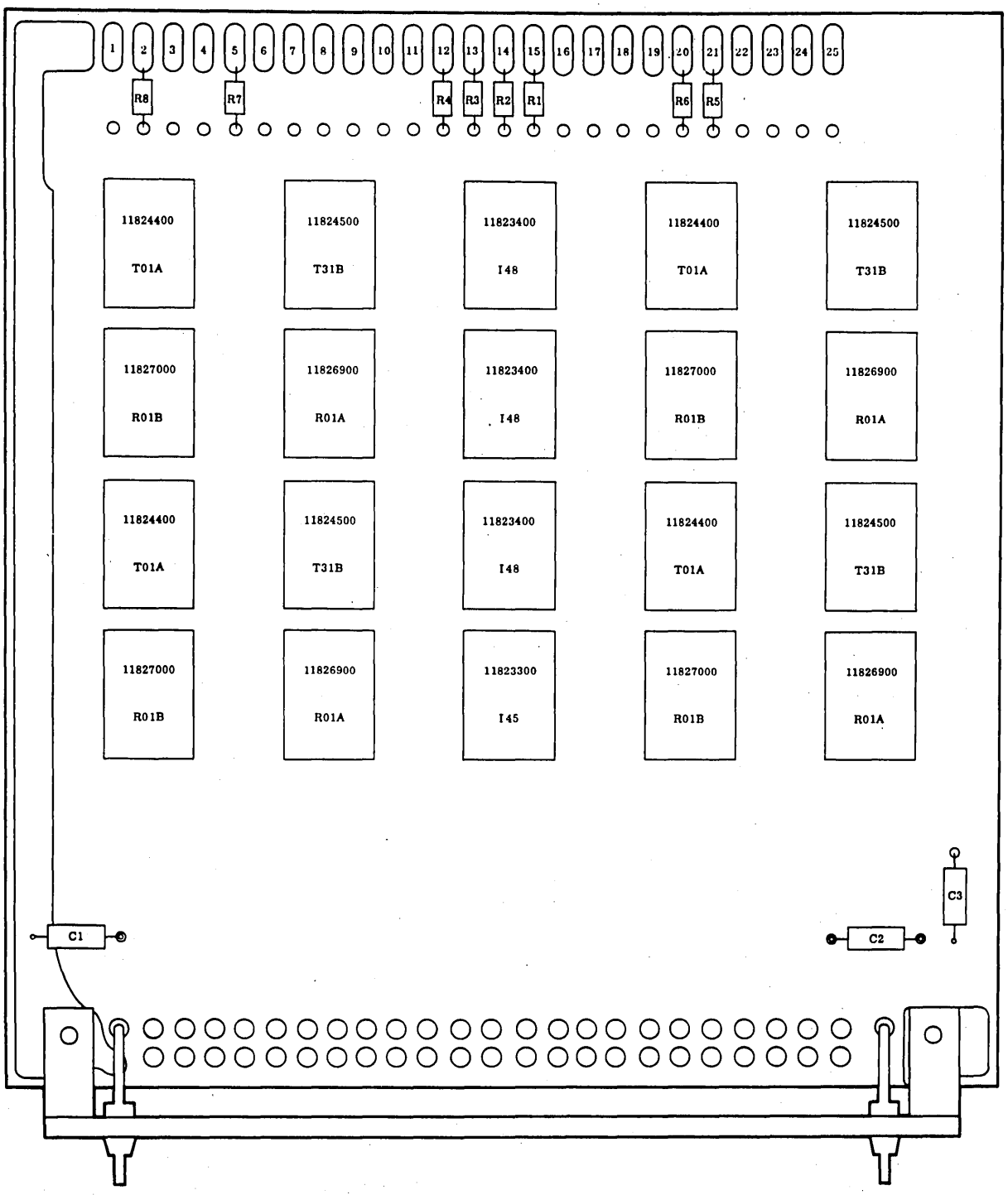
End of PMP

*Equipment that has not been shock tested regularly, should be approached with caution as large scale failures are possible in older modules.

Section Five
DIAGRAMS AND PARTS LIST

5.1 GENERAL

Included in this section are board layout diagrams for all cards in the DCT (see Figures 5.1 through 5.9). These diagrams illustrate the positions of the components on each board. Following each diagram is a parts list for that board. Table 5.10 is a module assembly parts list.



1-8827

FIGURE 5.1 BALANCED LINE INTERFACE (AV) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY
BALANCED LINE INTERFACE
AV

PRODUCT 1500

PL 38874900 RE E

SHEET 1 OF 2

REVISION STATUS OF SHEETS

1	2
A	—
B	B
C	B
D	D
E	D

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	—	RELEASED	
B	11277	FIND # 8 WAS 24505217. ADDED FIND NO. 11 & 12	
C	11455	SEE C.O.	
D	12463	SEE C.O.	
E	DDC	FIN 6 WAS P/N 11823400, QTY 3; DELETED FIN 7; FIN 8 WAS P/N 38901000 (ECR 2553)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED - 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
1	38827200	1		PW BOARD	
2	11827000	4		PARTY LINE RECEIVER	R01B
3	11824400	4		PARTY LINE TRANSMITTER	T01A
4	11826900	4		PARTY LINE RECEIVER	R01A
5	11824500	4		PARTY LINE TRANSMITTER	T31B
6	11848500	4		INVERTER	I48M
7					
8	24505229	3		CAPACITOR CER 10%	C1-C3
9	38996100	REF		LOGIC DIAGRAM	

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BY [illegible] DATE 2-3-66 GBB DATE 2-10-66 APPD. DATE

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

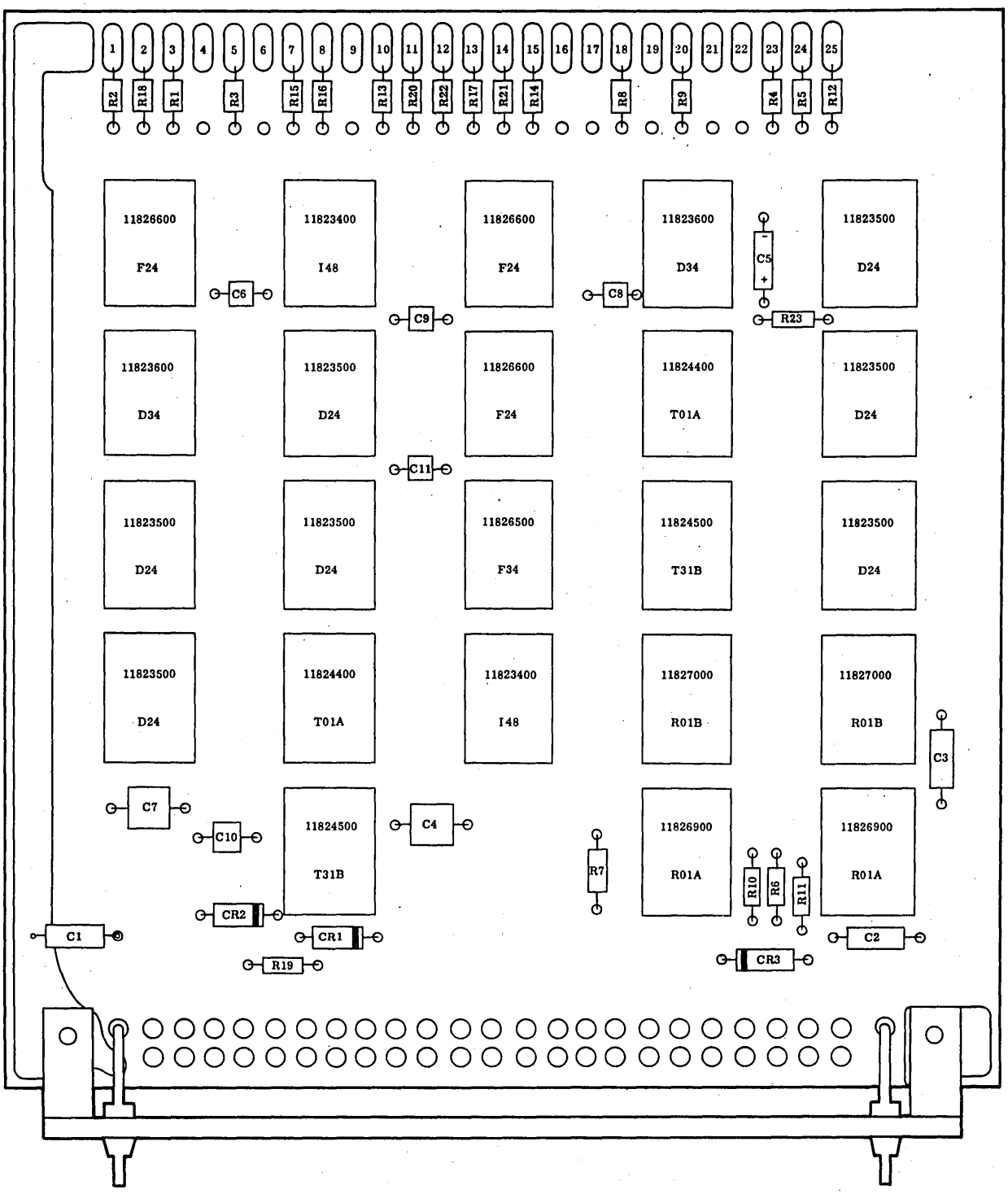
TITLE PRINTED WIRING ASSY
BALANCED LINE INTERFACE
AV

PRODUCT 1500

PL 38874900 REV. D

SHEET 2 OF

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS.	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
10					
11	29563033	8		RES. COMP 1.2K 1/8W 5%	R1 THRU R8
12	38958502	1		TEST JACK	
13	38817200	1		HEADER, PRINTED WIRING	BD
14	84717500	2		RIVET, UNIV HD, AL	1/16 DIA x 1/4 LG



NOTE: BAND DENOTES CATHODE END OF DIODE.
2 R23 IS A SELECT ON TEST RESISTOR (1/4W, 5%)

1-2528A

FIGURE 5.2. RESPONSE CONTROL (BB) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY
RESPONSE CONTROL
BB

PRODUCT 1500

PL 38896800

REV M

SHEET 1 OF 4

REVISION STATUS OF SHEETS

SEE SHT 4 FOR ADDITIONAL REVISIONS

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	/	RELEASED	3/1/66
B	11316	SEE CO	
C	11957	SEE CO	
D	11536	SEE CO	
F	DDC	QUANITY OF FIND NO. 19 WAS 20	
H	12463	SEE CO	
J	DDC	F/N 15 WAS 24510430, #16 WAS 24510445, #17 WAS 24510433 #18 WAS 24510448, #22 WAS 24510437 ECR 2137 RAR	
K	12805	FN 16 QTY WAS 2, DELETED C11. FN 17 QTY WAS 1, ADDED C11. KN	
L	DDC	FIN2 WAS QTY2, FIN3 WAS QTY3, FIN6 WAS QTY2, FIN11 WAS QTY7; ADDED FIN'S 28, 29, 30, 31; FIN 13 WAS PIN 38901000. (ECR2557)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
1	38850800	1		PW BOARD	
2	11823600	1		DOUBLE INVERTER	D34
3	11826600	2		FLIP FLOP	F24
4	11826500	1		FLIP FLOP	F34
5	38958502	1		TEST JACK	
6	11823400	1		INVERTER	I48
7	11826900	2		PARTY LINE RECEIVER	R01A
8	11827000	2		PARTY LINE RECEIVER	R01B
9	11824400	2		PARTY LINE TRANSMITTER	T01A

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DRAWN B. Johnson DATE 3-11-66

CHKD G.B.B. DATE 3-14-66

APPD G.B.B. DATE 3/14/66

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY- RESPONSE CONTROL BB

PRODUCT 1500

PL 38896800 REV. M

SHEET 2 OF

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS.	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
10	11824500	2		PARTY LINE TRANSMITTER	T31B
11	11823501	2		DOUBLE INVERTER	D24
12	25175800	3		DIODE	CR1 THRU CR3
13	24505229	3		CAP. TANT 1uf 35V 10%	C1 THRU C3
14	24505207	1		CAP. TA .015 uf 35V 10%	C5
15	84996708	2		CAP. CER 50pf 100V 10%	C8 AND C9
16	84996723	1		CAP. CER 560pf 100V 10%	C10
17	84996731	2		CAP. CER 1500pf 100V 10%	C4 & C11
18	84996726	1		CAP. CER 750pf 100V 10%	C7
19	24563033	17		RES. COMP 1.2K $\frac{1}{8}$W 5%	R1-5, 8,9, 12-18, 20-22
20	38927100	REF		LOGIC DIAGRAM	
21					
22	84996715	1		CAP. CER 150pf 100V 10%	C6
23	24500057	4		RES. COMP 560 Ω $\frac{1}{4}$W 5%	R6, 7, 10 & 11
24	24500053	1		RES. COMP 390 Ω $\frac{1}{4}$W 5%	R19
25	245000XX	1		RES. COMP $\frac{1}{4}$W 5%	R23 S.O.T.
26	84717500	2		RIVET, UNIV HD, AL	1/16 DIA x 1/4 LG
27	38917200	1		HEADER, PRINTED WIRING	BD
28	52301300	1		DOUBLE INVERTER	D34M

CSD 291

N

CONTROL DATA CORPORATION

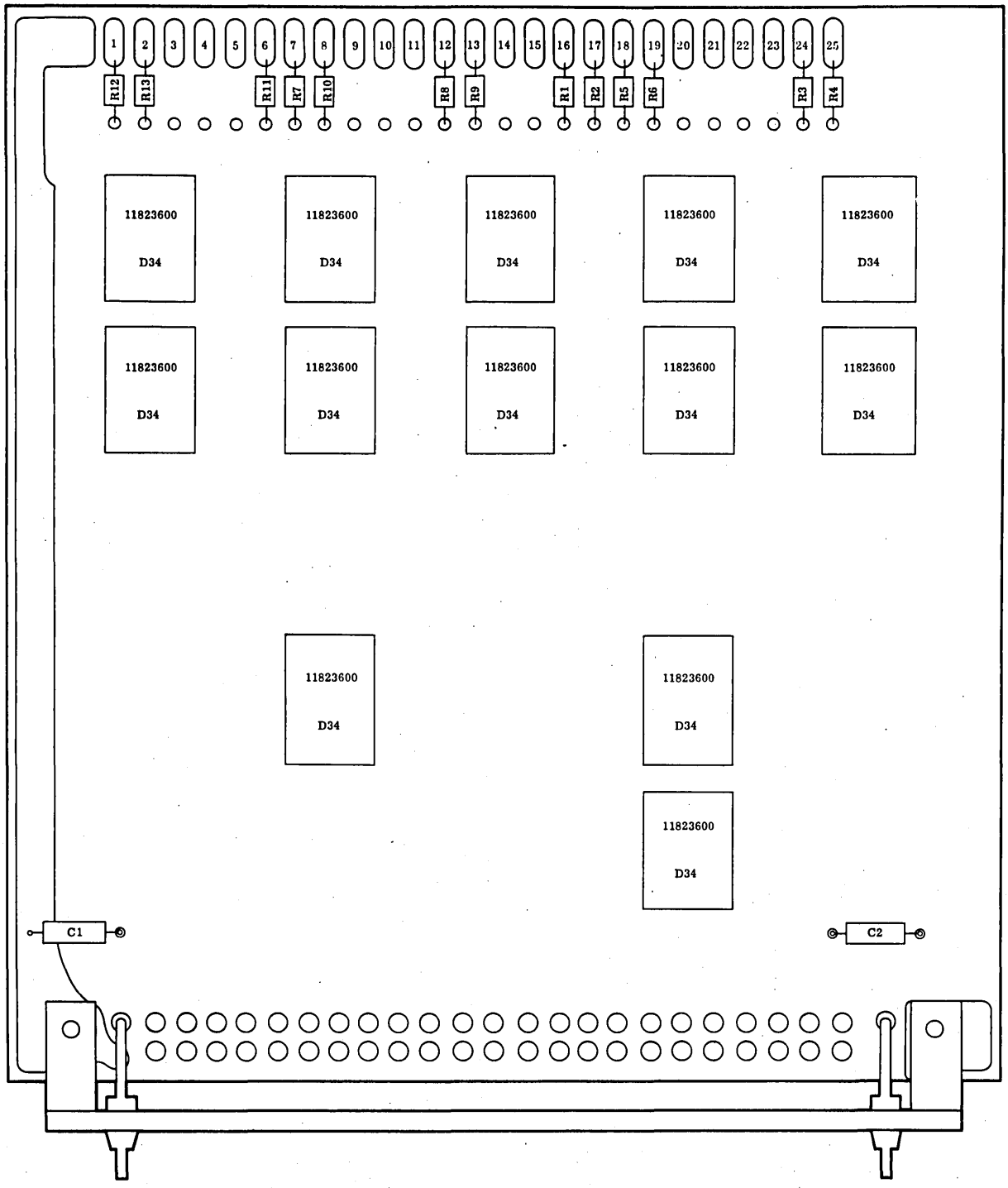
TITLE PRINTED WIRING ASSEMBLY-
RESPONSE CONTROL
BB

PRODUCT

PL 38896800 | REV L

3

ITEM	PART NUMBER	QUANTITY REQUIRED										UNIT OF MEAS.		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
29	11848700	1												FLIP FLOP	F24M
30	11848500	1												INVERTER	I48M
31	11848600	5												DOUBLE INVERTER	D24M



1-2529

FIGURE 5.3. ADDRESS DECODER (BE) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY-
ADDRESS DECODER
BE

PRODUCT
1500

PL 38882200 REV E

SHEET 1 OF 1

REVISION STATUS OF SHEETS

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	/	RELEASED	
B	11116	REVISED PER C.O. GBB 3-30-66	
C	11304	ADDED FIND NO. 7	
D	12463	ADDED F/N 8 & 9 PER CO	
E	DDC	F/N 2 WAS P/N 11823600, F/N 3 WAS P/N 38901000 (ECR 2557)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED - 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
1	38839000	1		PW BOARD	
2	52301300	13		DOUBLE INVERTER	D34M
3	24505229	2		CAP. TANT 1.0 μf 35V 10%	C1 AND C2
4	24563033	13		RES. COMP 1.2K 1/8W 5%	R1 THRU R13
5	84514800	REF		LOGIC DIAGRAM	
6					
7	38958502	1		TEST JACK	
8	38817200	1		HEADER, PRINTED WIRING BD	
9	84717500	2		RIVET, UNI HD, AL	1/16 DIA x 1/4 LG

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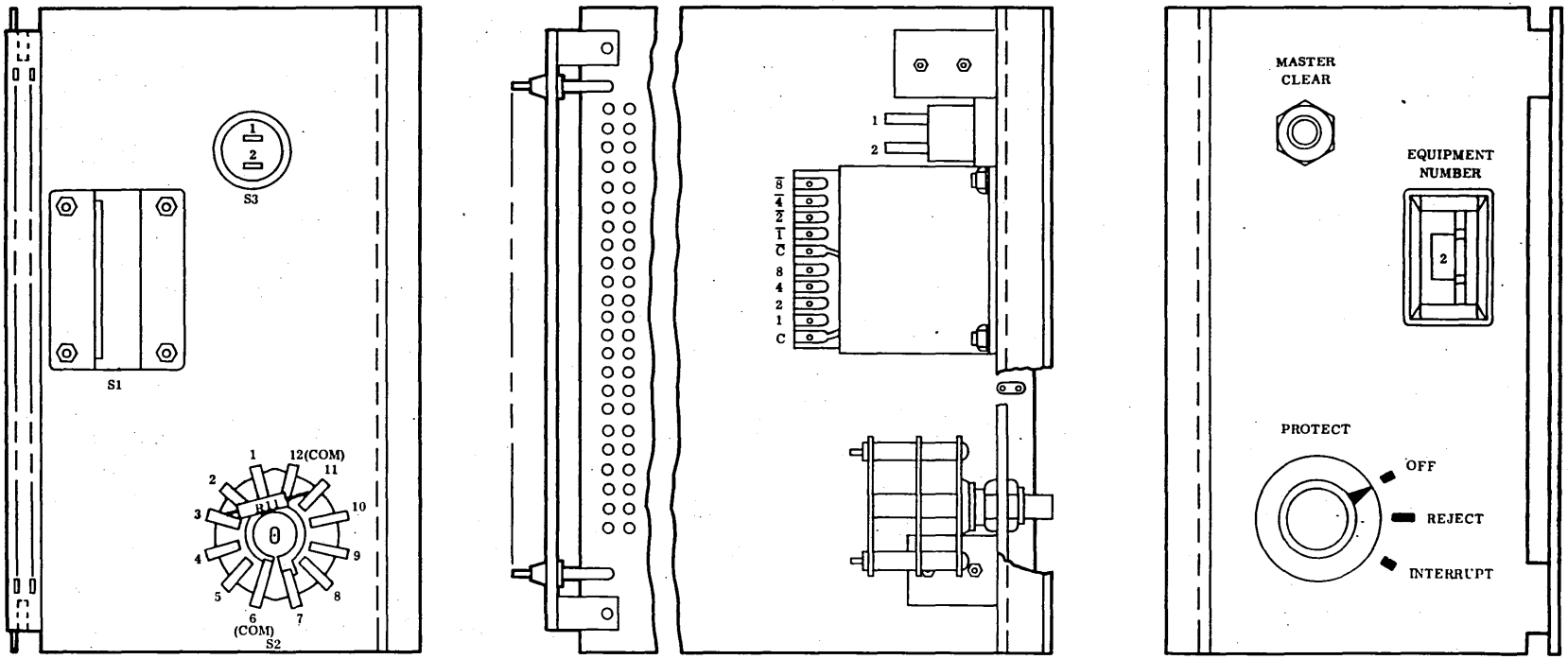
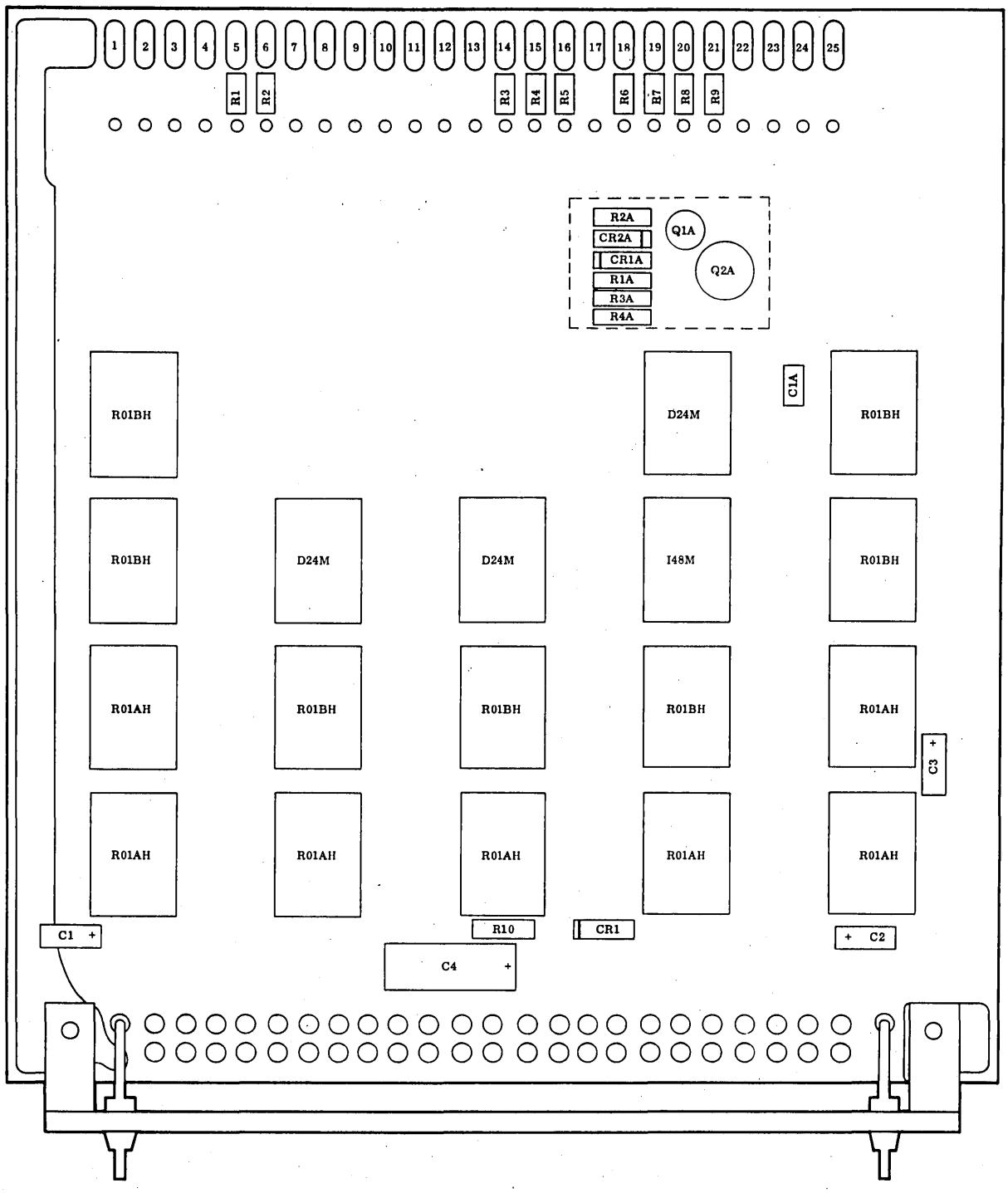


FIGURE 5.4. PROTECT AND EQUIPMENT SELECT (BG) CARD, PANEL ASSEMBLY

TABLE 5.4. PARTS LIST
PROTECT AND EQUIPMENT SELECT (BG) PANEL ASSEMBLY

PART NO.	QTY.	DESCRIPTION
24523001	1	Switch, Push, SPST (S3)
38923002	1	Switch, Rotary (S2)
38851400	1	Switch, Hexadecimal (S1)
24500050	1	Resistor, Composite, 300Ω, 1/4w, 5% (R11)



1-3503BG

FIGURE 5.5. PROTECT AND EQUIPMENT SELECT (BG) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY - PROTECT & EQUIPMENT SELECT

PRODUCT 1500

PL 38882400 REV H

SHEET 1 OF 2

REVISION STATUS OF SHEETS

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	/	RELEASED	
B	11271	REVISED PER CO	
C	11352	SEE CO	
D	11597	FIND NO. 13 WAS 24551300 3-26-66	
E	11734	ADDED FIND NO. 16, FIND NO. 15 QTY WAS 2. 11-14	
F	12463	ADDED FIND NO. 17 AND 18 2-13-68	
G	DDC	FIND NO. 16 WAS 24510458 (ECR 2417)	
H	DDC	F/N 4 WAS P/N 11823500 F/N 6 WAS P/N 11823400 F/N 8 WAS P/N 38901000 F/N 10 WAS QTY 11 ADDED F/N 19 (ECR 2557)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED - 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
1	38860100	1		PW BOARD	
2	11827000	7		PARTY LINE RECIEVER	R01B
3	11826900	7		PARTY LINE RECIEVER	R01A
4	11848600	3		DOUBLE INVERTER	D24M
5	38958502	1		TEST JACK	
6	11848500	1		INVERTER	I48M
7	25175800	3		DIODE	CR1, CR1A, CR2A
8	24505229	3		CAP. TANT 1.0uf 35V 10%	C1 THRU C3
9	17706725	1		CAP. TA 120uf 10V 10%	C4

COPIES TO

BY [signature] DATE 2-16-66 CHKD [signature] DATE 4-1-66 APPD. [signature] DATE

CONTROL DATA CORPORATION

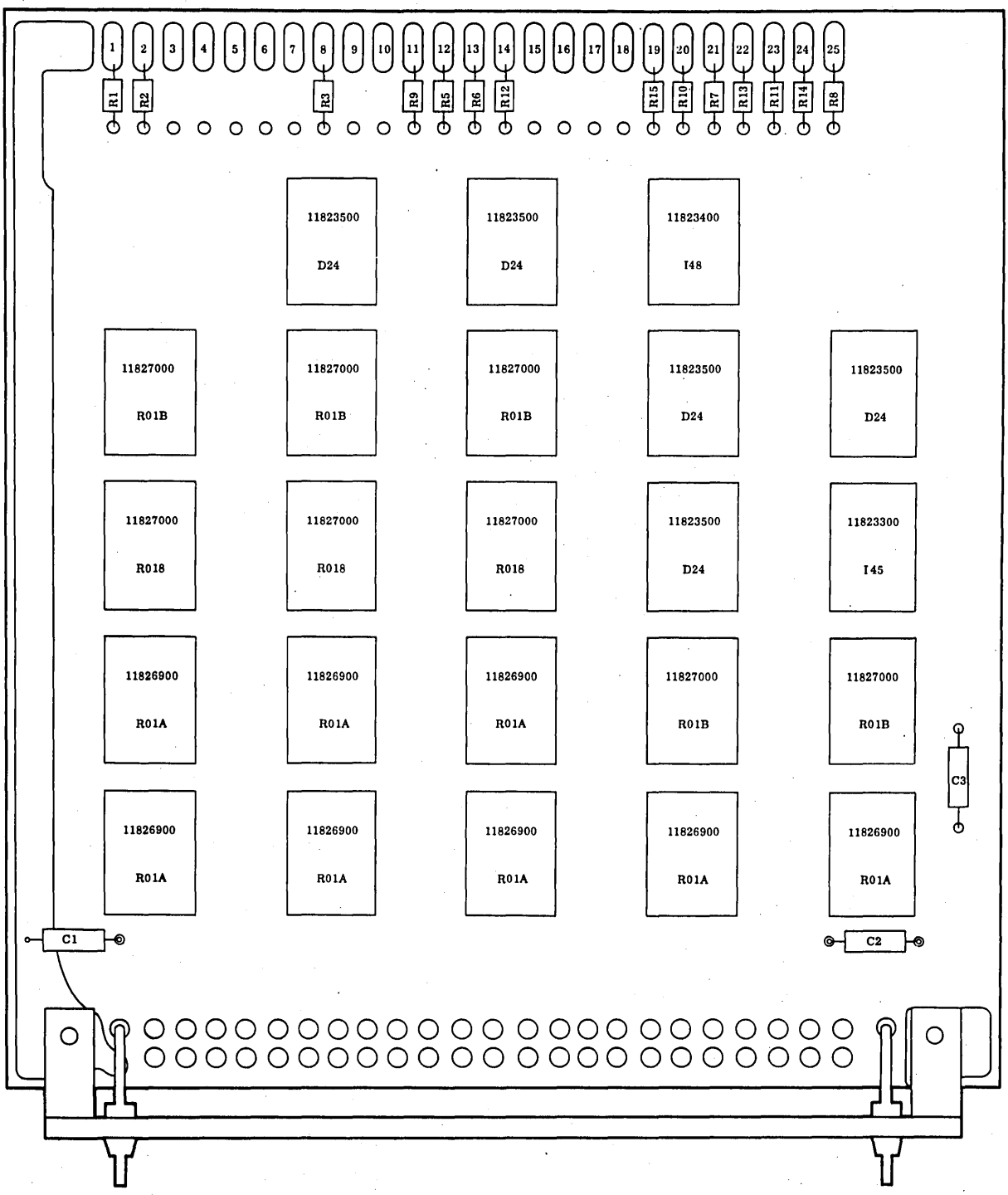
TITLE PRINTED WIRING ASSY-
PROTECT & EQUIPMENT SELECT

PRODUCT 1500 · 38882400 H

2

ITEM NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00										UNIT OF MEAS.		DESCRIPTION	REFERENCE DESIGNATIONS NOTES OR SPECIAL
10	24563033	9												RES. COMP 1.2K $\frac{1}{8}$W 5%	R1-R9
11	24500039	1												RES. COMP 100 ~ $\frac{1}{8}$W 5%	R10
12	24562100	1												TRANSISTOR	Q1A
13	39034800	1												TRANSISTOR	Q2A
14	24500048	1												RES. COMP 240 ~ $\frac{1}{4}$W 5%	R3A
15	24500050	1												RES. COMP 300 ~ $\frac{1}{4}$W 5%	R4A
16	24976737	1												CAP. CER 5400PF 100V 10%	C1A
17	38817200	1												HEADER, PRINTED WIRING BOARD	
18	84717500	2												RIVET, UNIV HD, AL	1/16 DIA X 1/4 LG
19	24500065	2												RES COMP, 1.2K 1/4W 5%	R1A, R2A

CSD 291



1-2531

FIGURE 5.6. ADDRESS CONTROL (BH) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY
ADDRESS CONTROL
BH

PRODUCT
1500

PL 38896900 F

SHEET 1 OF 2

REVISION STATUS OF SHEETS

1	2										
A	-										
B	-										
C	C										
D	C										
E	E										
F	E										

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	/	RELEASED	
B	11228	SEE CO & RELEASED	
C	11264	ADDED FIND NO. 11	
D	11463	SEE CO	
E	12463	ADDED FN 12 & 13. GBB	
F	DDC	FIN14 WAS 11823400 QTY 1, DELETED FIN5, FIN6 WAS P/N 11823500, FIN7 WAS P/N 38901000 (ECR 2557)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS NOTES OR MATERIAL
1	38860900	1		PW BOARD	
2	11826900	8		PARTY LINE RECEIVER	R01A
3	11827000	8		PARTY LINE RECEIVER	R01B
4	11848500	2		INVERTER	I48M
5					
6	11848600	5		DOUBLE INVERTER	D24M
7	24505229	3		CAP. TANT 1.0 uF 35V 10%	C1 THRU C3
8	24563033	14		RES. COMP 1.2K 1/8W 5%	R1 - R14
9	38996400	REF		LOGIC DIAGRAM	

DRF				DATE			APPD		DATE
				3-11-66		GBB	3-14-66		3-

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY-
ADDRESS CONTROL
BH

PRODUCT
1500

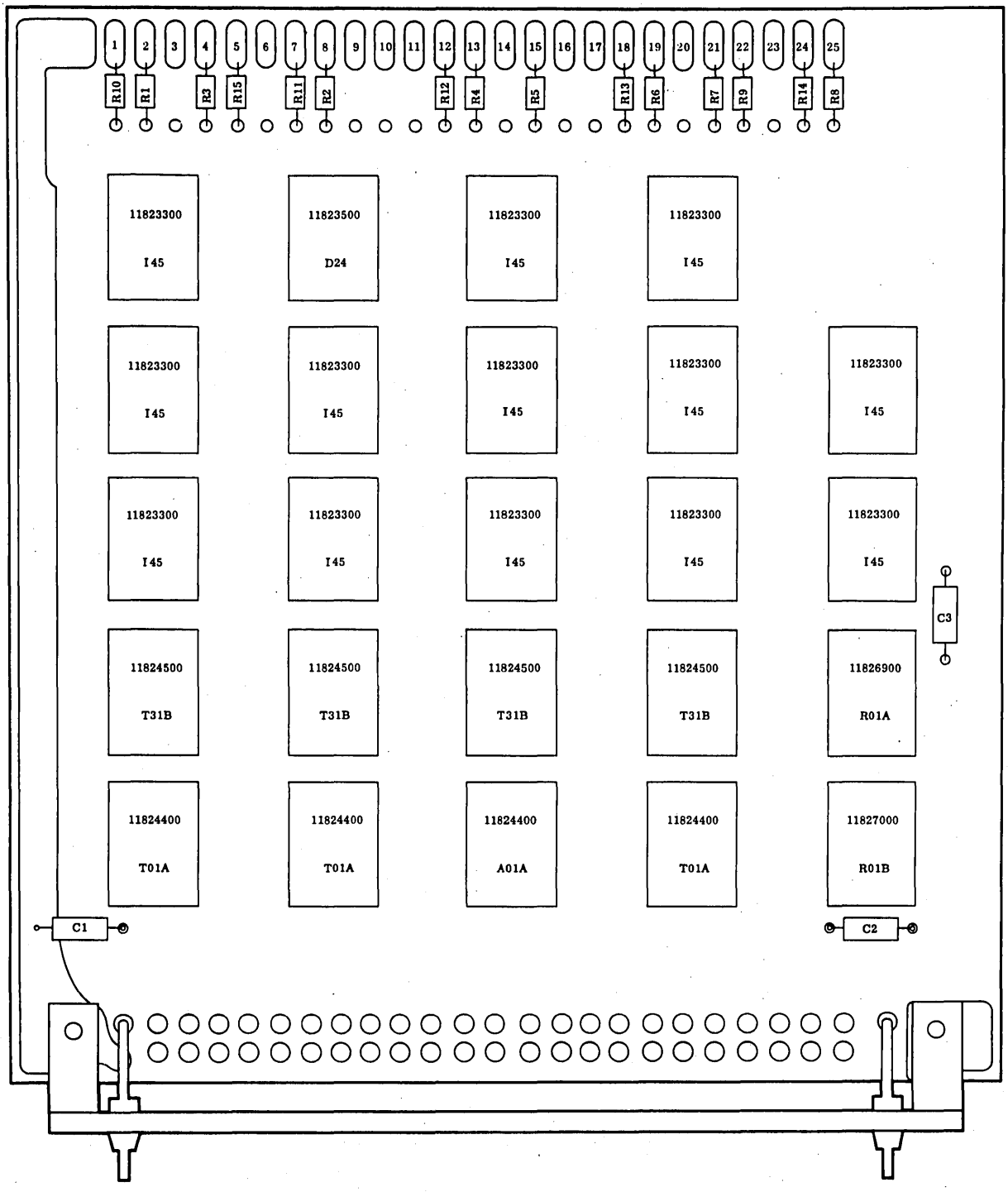
PL 38896900

REV. E

SHEET 2 OF

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS.	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
10					
11	38958502	1		TEST JACK	
12	38817200	1		HEADER PRINTED WIRING BD.	
13	84717500	2		RIVET, UNIV HD, AL,	1/16 DIA x 1/4 LG.

CSD 291



1-2532

FIGURE 5.7. DATA AND CONTROL BUS INTERFACE (BJ) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY-
DAISY CHAIN INTERFACE
BJ

PRODUCT
1500

PL 38897000 E

SHEET 1 OF 2

REVISION STATUS OF SHEETS

	1										

REVISIONS

REV	ECO	DESCRIPTION	APPD
A	/	RELEASED	
B	11305	SEE CO	
C	11451	SEE CO	
E	DDC	F/N 4 WAS P/N 11823300 F/N 5 WAS P/N 11823500 F/N 8 WAS P/N 38901000 (ECR 2557)	

F/ND NO	PART IDENTIFICATION	QUANTITY REQUIRED - 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS NOTES OR MATERIAL
1	38862700	1		PW BOARD	
2	11824400	4		PARTY LINE TRANSMITTER	T01A
3	11824500	4		PARTY LINE TRANSMITTER	T31B
4	11848500	13		INVERTER	I48M
5	11848600	1		DOUBLE INVERTER	D24M
6	11826900	1		PARTY LINE RECEIVER	R01A
7	11827000	1		PARTY LINE RECEIVER	R01B
8	24505229	3		CAP. TANT 1.0uf 35V 10%	C1 THRU C3
9	24563033	15		RES. COMP 1.2K 1/8 W 5%	R1 THRU R15

SCALE | DATE 3-14-66 | APPD | DATE

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSY - DAISY CHAIN INTERFACE BJ

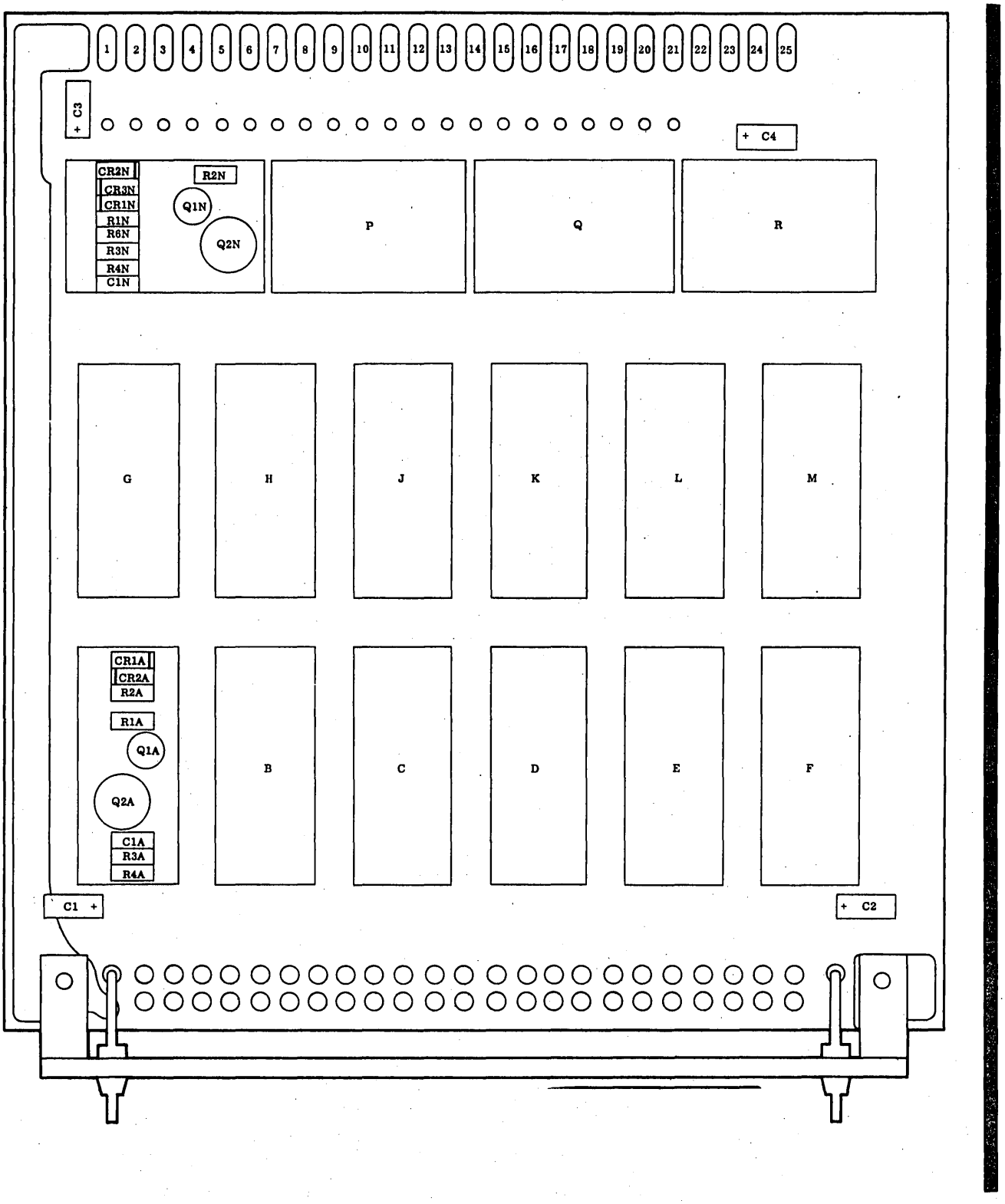
PRODUCT 1500

PL 38897000 RF 1

SHEET 2 OF

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS.	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
10	38995700	REF		LOGIC DIAGRAM	
11					
12	38958502	1		TEST JACK	
13	38817200	1		HEADER, PRINTED WIRING BD	
14	84717500	2		RIVET, UNIV HD, AL	1/16 DIA x 1/8 LG

CSD 291



1-3030

FIGURE 5.8. LONG-LINE DRIVERS (BM) CARD, BOARD LAYOUT

DWN	B. JOHNSON	3-15-6	CONTROL DATA	TITLE PW ASSY- LONG LINE DRIVERS BM	PREFIX PL	DOCUMENT NO. 38897100	REV K
CHKD	G. BRIEN	3-15-6					
ENG			ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037				
MFG							
APPR	A. FRITTS	3-15-6	CODE IDENT 09132	FIRST USED ON		SHEET 1 OF 2	

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
J	12932	F/N 4 WAS 38501000 ⚠1 F/N 12 WAS 38980700			
K	DDC	F/N 11 WAS 24563033 (1.2K 1/8W RES) (ECR 2701)			

NOTES: ⚠1 REDRAWN AT 'J' REVISION, ORIGINAL VELLUM LOST.

DETACHED LISTS

CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 2	PL	DOCUMENT NO 38897100	REV. K

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	38866800	1			PW BOARD	
2	24500048	16			RES COMP 240Ω 1/4W 5%	R3A-R3R
3	24500050	16			RES COMP 300Ω 1/4W 5%	R4A-R4R
4	24505229	4			CAP TANT 1μF 35V 10%	C1-C4
5	39064900	REF			LOGIC DIAG	
6						
7	38958502	1			TEST JACK	
8	24562100	16			TRANSISTOR (2N3014)	Q1A-Q1R
9	39034800	16			TRANSISTOR (2N3252)	Q2A-Q2R
10	25175800	36			DIODE (1N914)	CR1A-CR2M CR1N-CR3R
11	24500065	36			RES COMP 1.2K 1/4W 5%	R1A-R2R, R6N-R6R
12	84996729	16			CAP CER 1000Pf 100V 10%	C1A-C1R
13	38817200	1			HEADER PWB	
14	84717500	2			RIVET UNIV HD ALUM	1/16 DIA X 1/4 LG.

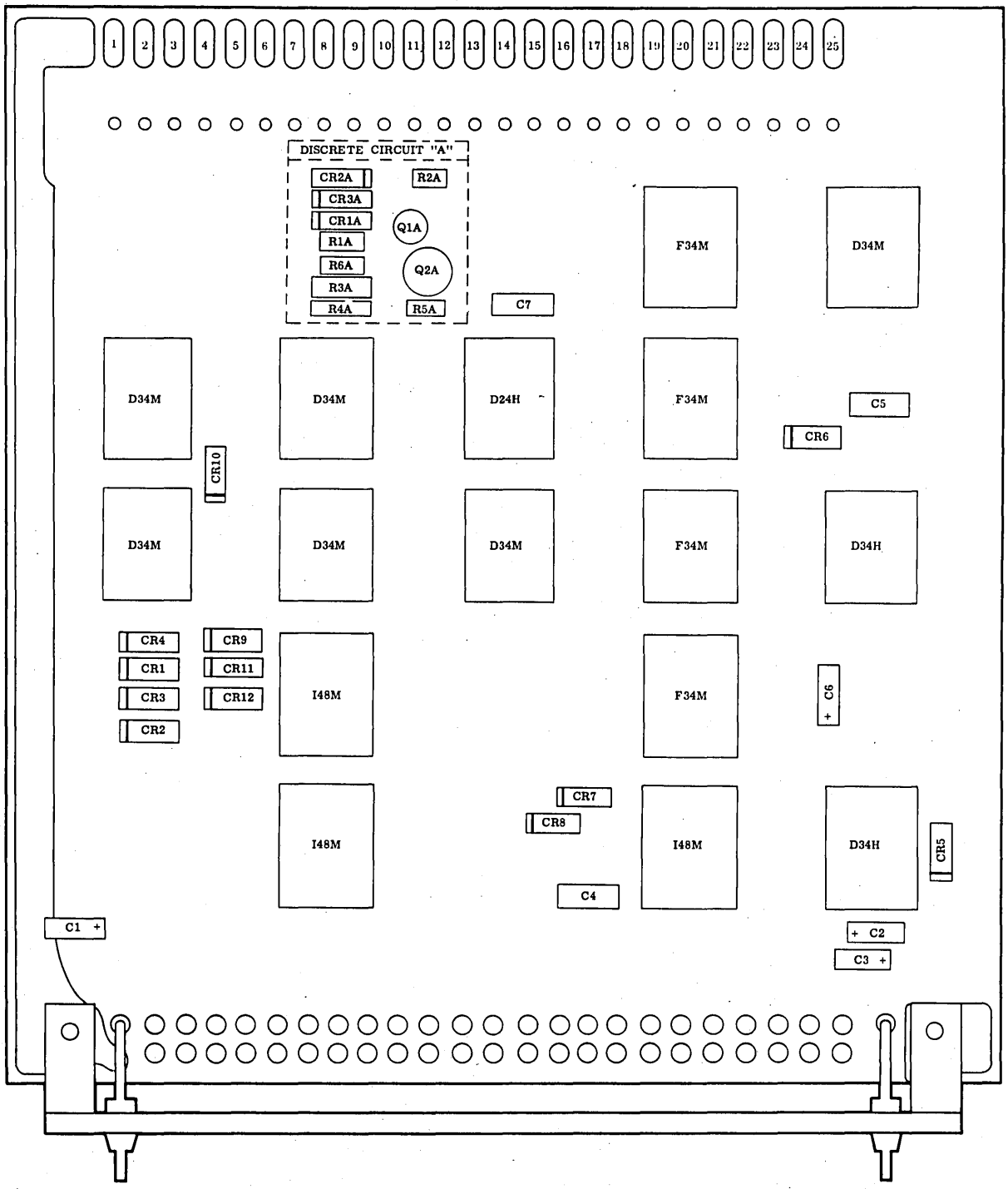


FIGURE 5.9. FUNCTION CONTROL (BN) CARD, BOARD LAYOUT

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSEMBLY-
FUNCTION CONTROL
BN

PRODUCT
1500

PL 38905500

REV L

SHEET 1 OF 2

REVISION STATUS OF SHEETS

REVISIONS

REV	ECO	DESCRIPTION	APPD
J	12622	REDRAWN, SEE C.O.	
K	DDC	F/N 8 WAS 24510440, #9 WAS 24510450, #10 WAS 24510457 (ECP 2137)	
L	DDC	F/N 12 WAS 38901000, F/N 16 WAS 11823400, F/N 18 WAS QTY 8, F/N 19 WAS 11826500, ADDED F/N 22. (ECR 2557)	

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED - 00	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
1	38867800	1		P.W. BOARD	
2	38817200	1		HEADER, P.W.B.	
3	84717500	2		RIVET, UNIV. HD., AL.	1/16DIA. x 1/4 LG
4	38958502	1		TEST JACK	
5	24500048	1		RES., COMP., 240Ω, 1/4W, 5%	R3A
6	24500050	2		RES., COMP., 300Ω, 1/4W, 5%	R4A, R5A
7	24500065	3		RES., COMP., 1.2K, 1/4W, 5%	R1A, R2A, R6A
8	84996718	1		CAP., CER., 270PF, 100V, 10%	C4
9	84996728	1		CAP., CER., 910 PF, 100V, 10%	C5

COPIES TO

BY WDH DATE 10-4-7 CHKD. G.B.B. DATE 10-13-7 APPD. DATE

CONTROL DATA CORPORATION
CONTROL SYSTEMS DIVISION

TITLE PRINTED WIRING ASSEMBLY - FUNCTION CONTROL BN

PRODUCT

PL 38905500 REV. L.

SHEET 2 OF

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	UNIT OF MEAS.	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES OR MATERIAL
10	84996736	1		CAP.,CER.,3300 PF,100 V,10%	C7
11	24505201	1		CAP.,TAN.,.0047uf,35V,10%	C6
12	24505229	3		CAP.,TAN., 1.0uF 35V 10%	C1-C3
13	25175800	15		DIODE	CR1-CR12, CR1A-CR3A
14	24562100	1		TRANSISTOR	Q1A
15	39034800	1		TRANSISTOR	Q2A
16	11848500	3		INVERTER	I48M
17	11823500	1		DOUBLE INVERTER	D24
18	11823600	2		DOUBLE INVERTER	D34
19	52301400	4		FLIP FLOP	F34M
20	25195043	A/R		WIRE,#26AWG,INSUL.	
21	39028800	REF.		LOGIC DIAGRAM	
22	52301300	6		DOUBLE INVERTER	D34M

5.19A

CSD 201

TABLE 5.10. MODULE ASSEMBLY PARTS LIST

PART NO.	QTY.	DESCRIPTION
38898700	1	Connector Plate Assembly (J06)
38969800	2	Transformer (T1, T2)
39004603	2	Terminal Strip (TB01, TB06)
24507230	2	Capacitor, Tantalum, 50 μf, 100V, Foil (C1, C2)
38969401	1	Connector, Taper Block, Red (TB02)
38969405	1	Connector, Taper Block, Blue (TB03)
38969409	1	Connector, Taper Block, Black (TB04)
38948600	1	Cable (P01)
17849500	6	Cable, Service, 18 ga (W01)
17896900	15	Connector Receptacle
38956900	4	Connector, Wired, 30 Twisted-Pair (J30-J33)
24535100	4	Connector Receptacle (J34-J37)
38925500	3	Connector Receptacle (J38-J40)

Section Six
WIRE LIST

6.1 GENERAL

This section contains the wire list for the 1750 Data and Control Terminal.

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DOT

```
*    D= LITES              *
*                          *
*    ON SPECIAL NOTES      *
****************************
*                          *
*                          *
*    K= RELAYS             *
*    X= CABLE CONNECTORS   *
*                          *
*    SS= COAX CABLE        *
*                          *
*                          *
*    S= TWISTED PAIR       *
*    S= SWITCHES           *
*    THIS IS A TEST COMMENT *
*                          *
****************************
*    GRDCH= 16GA WIRE      *
```

EXTSN	X34-001	17-028
PWR1	42-005	T2-003
PWR2	42-006	T2-005
SRGC1	X36-001	41-005
SRGC2	X37-001	41-007
SRGO	X35-001	39-006
TR1	32-033	T1-003
TR2	32-043	T1-004
TR3	32-039	T1-005
V+20	TB5-002	TR2-009

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		OCT
V+20	X30- F9	T82-003		
V+20	X31- F9	T82-004		
V+20	X32- F9	T82-005		
V+20	X33- F9	T82-006		
V+20	X38- A	T82-002		
V+20	X39- A	T82-008		
V-20	TB5-003	T83-009		
V-20	X30- F0	T83-003		
V-20	X31- F0	T83-004		
V-20	X32- F0	T83-005		
V-20	X33- F0	T83-006		
V-20	X38- B	T83-002		
V-20	X39- B	T83-008		
V-6	POS-TER	V-6- PS	NEG-TER V+6- PS	14 GA
V-6	X40- A	41-019		
V-6	X40- A		NEG-TER V-6- PS	14 GA
V-6RT	X40- B		POS-TER V-6- PS	14 GA
117AC	TB1-001	P01-001		
117AC	TB1-001	T1-001		

117AC	TB1-002	T1-002		
117AC	TB1-002	P01-002		
117PD	TB6-001	W01-001		
117PD	TB6-001	T2-001		
117PD	TB6-002	T2-002		
117PD	TB6-002	W01-002		
$A0	X30- A1	16-018	X30- A2	16-017
$A0	X31- A1	16-018	X31- A2	16-017
$A04	X30- A9	14-018	X30- A0	14-017

SIGNAL LIST

NAME		DRAWING #		REV.	DATE	TITLE
1750		38925400		AA		DCT
$A04	X31- A9	14-018	X31- A0	14-017		
$A05	X30- B1	14-016	X30- B2	14-015		
$A05	X31- B1	14-016	X31- B2	14-015		
$A06	X30- B3	14-046	X30- B4	14-045		
$A06	X31- B3	14-046	X31- B4	14-045		
$A07	X30- B5	14-044	X30- B6	14-043		
$A07	X31- B5	14-044	X31- B6	14-043		
$A1	X30- A3	16-016	X30- A4	16-015		
$A1	X31- A3	16-016	X31- A4	16-015		
$A10	X30- C1	12-046	X30- C2	12-045		
$A10	X31- C1	12-046	X31- C2	12-045		
$A11	X30- C3	12-044	X30- C4	12-043		
$A11	X31- C3	12-044	X31- C4	12-043		
$A12	X30- C5	10-018	X30- C6	10-017		
$A12	X31- C5	10-018	X31- C6	10-017		
$A13	X30- C7	10-016	X30- C8	10-015		
$A13	X31- C7	10-016	X31- C8	10-015		
$A14	X30- C9	10-046	X30- C0	10-045		

$A14	X31= C9	10=046	X31= C0	10=045
$A15	X31= D1	10=044	X30= D2	10=043
$A15	X31= D1	10=044	X31= D2	10=043
$A2	X30= A5	16=046	X30= A6	16=045
$A2	X31= A5	16=046	X31= A6	16=045
$A3	X30= A7	16=044	X30= A8	16=043
$A3	X31= A7	16=044	X31= A8	16=043
$A8	X30= B7	12=018	X30= B8	12=017
$A8	X31= B7	12=018	X31= B8	12=017
$A9	X30= B9	12=016	X30= B0	12=015

SIGNAL LIST

NAME		DRAWING #		REV.	DATE	TITLE
1750		38925A00		AA		DCT
$A9	X31- A9	12-016	X31- B9	12-015		
$CINT	X30- D7	15-007	X30- D8	15-008		
$CINT	X31- D7	15-007	X31- D8	15-008		
$MCLT	X32- D7	07-034	X32- D8	07-033		
$MCLT	X33- D7	07-034	X33- D8	07-033		
$PGPT	X32- D9	07-006	X32- D0	07-005		
$PGPT	X33- D9	07-006	X33- D0	07-005		
$Q0	X32- A1	19-021	X32- A2	19-022		
$Q0	X33- A1	19-021	X33- A2	19-022		
$Q1	X32- A3	09-042	X32- A4	09-041		
$Q1	X33- A3	09-042	X33- A4	09-041		
$Q10	X32- C1	07-007	X32- C2	07-008		
$Q10	X33- C1	07-007	X33- C2	07-008		
$Q11	X32- C3	15-042	X32- C4	15-041		
$Q11	X33- C3	15-042	X33- C4	15-041		
$Q12	X32- C5	19-004	X32- C6	19-003		
$Q12	X33- C5	19-004	X33- C6	19-003		
$Q13	X32- C7	19-005	X32- C8	19-006		
$Q13	X33- C7	19-005	X33- C8	19-006		

$Q14	X32- C9	19-012	X32- C0	19-011
$Q14	X33- C9	19-012	X33- C0	19-011
$Q15	X32- D1	19-010	X32- D2	19-009
$Q15	X33- D1	19-010	X33- D2	19-009
$Q2	X32- A5	11-042	X32- A6	11-041
$Q2	X33- A5	11-042	X33- A6	11-041
$Q3	X32- A7	13-042	X32- A8	13-041
$Q3	X33- A7	13-042	X33- A8	13-041
$Q4	X32- A9	19-020	X32- A0	19-019

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3R925400	AA		DCT
$Q4	X33- A9	19-020	X33- A0	19-019
$Q5	X32- A1	19-031	X32- A2	19-032
$Q5	X33- A1	19-031	X33- A2	19-032
$Q6	X32- A3	19-043	X32- A4	19-044
$Q6	X33- A3	19-043	X33- A4	19-044
$Q7	X32- A5	07-043	X32- A6	07-044
$Q7	X33- A5	07-043	X33- A6	07-044
$Q8	X32- A7	07-026	X32- A8	07-025
$Q8	X33- A7	07-026	X33- A8	07-025
$Q9	X32- A9	07-017	X32- A0	07-018
$Q9	X33- A9	07-017	X33- A0	07-018
$READ	X32- D3	18-037	X32- D4	18-038
$READ	X33- D3	18-037	X33- D4	18-038
$REJEC	X30- D5	18-015	X30- D6	18-016
$REJEC	X31- D5	18-015	X31- D6	18-016
$RFPLY	X30- D3	18-034	X30- D4	18-033
$RFPLY	X31- D3	18-034	X31- D4	18-033
$SPA01	X30- D9	X31- D9	X30- D0	X31- D0
$SPA02	X30- E1	X31- E1	X30- E2	X31- E2

$SPA03	X3 - F3	X31- F3	X30- F4	X31- F4
$SPA04	X3 - F5	X31- F5	X30- F6	X31- F6
$SPA05	X3 - F7	X31- F7	X30- F8	X31- F8
$SPA06	X3 - F9	X31- F9	X30- F0	X31- F0
$SPA07	X3 - F1	X31- F1	X30- F2	X31- F2
$SPA08	X3 - F3	X31- F3	X30- F4	X31- F4
$SPA09	X3 - F5	X31- F5	X30- F6	X31- F6
$SPA10	X3 - F7	X31- F7	X30- F8	X31- F8
$SPA11	X32- F1	X33- F1	X32- F2	X33- F2

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3R925400	AA		DCT

$SPA12	X32- E3	X33- E3	X32- E4	X33- E4
$SPA13	X32- E5	X33- E5	X32- E6	X33- E6
$SPA14	X32- E7	X33- E7	X32- E8	X33- E8
$SPA15	X32- E9	X33- E9	X32- E0	X33- E0
$SPA16	X32- F1	X33- F1	X32- F2	X33- F2
$SPA17	X32- F3	X33- F3	X32- F4	X33- F4
$SPA18	X32- F5	X33- F5	X32- F6	X33- F6
$W=0	X32- F7	07-046	X32- F8	07-045
$W=0	X33- F7	07-046	X33- F8	07-045
$WRITE	X32- D5	18-045	X32- D6	18-046
$WRITE	X33- D5	18-045	X33- D6	18-046
$1+	TB5-006	09-035		
$1+	X11- A	TB5-006		
$1-	TB5-004	09-036		
$1-	X11- B	TB5-004		
$10+	TB5-045	11-017		
$10+	X2[illegible]- A	TB5-045		
$10-	TB5-043	11-018		
$10-	X2[illegible]- B	TB5-043		

$11+	TP5-012	13-017
$11+	X21- A	TP5-012
$11-	TP5-010	13-018
$11-	X21- B	TP5-010
$12+	TP5-021	15-017
$12+	X22- A	TP5-021
$12-	TP5-019	15-018
$12-	X22- B	TP5-019
$13+	TP5-030	09-007

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		OCT
$13+	X23- A	TB5-030		
$13-	TB5-028	09-008		
$13-	X23- B	TB5-028		
$14+	TB5-039	11-007		
$14+	X24- A	TB5-039		
$14-	TB5-037	11-008		
$14-	X24- B	TB5-037		
$15+	TB5-048	13-007		
$15+	X25- A	TB5-048		
$15-	TB5-046	13-008		
$15-	X25- B	TB5-046		
$2+	TB5-015	11-035		
$2+	X12- A	TB5-015		
$2-	TB5-013	11-036		
$2-	X12- B	TB5-013		
$3+	TB5-024	13-035		
$3+	X13- A	TB5-024		
$3-	TB5-022	13-036		
$3-	X13- B	TB5-022		

$4+	T85-033	15-035
$4+	X14- A	T85-033
$4-	T85-031	15-036
$4-	X14- B	T85-031
$5+	T85-042	09-027
$5+	X15- A	T85-042
$5-	T85-040	09-028
$5-	X15- B	T85-040
$6+	T85-009	11-027

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
17L0	38925400	AA	OCT	
$6+	X16- A	T85-009		
$6-	T85-007	11-028		
$6-	X16- B	T85-007		
$7+	T85-018	13-027		
$7+	X17- A	T85-018		
$7-	T85-016	13-028		
$7-	X17- B	T85-016		
$8+	T85-027	15-027		
$8+	X18- A	T85-027		
$8-	T85-025	15-028		
$8-	X18- B	T85-025		
$9+	T85-036	09-017		
$9+	X19- A	T85-036		
$9-	T85-034	09-018		
$9-	X19- B	T85-034		
ADD1A	19-014	28-048		
	08.5			
ADD1B	09-044	19-041	28-047	
	05.5	05.5		
ANA1	02-006	20-021		

	09.5		
ANA1T	2[illegible]-23	23-027	22-041
	03.0	03.0	
ANA2	22-[illegible]08	20-022	
	10.0		
ANA2T	20-019	23-025	22-038
	03.0	03.0	
ANA3	22-[illegible]10	20-017	
	09.0		

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3R925400	AA	OCT	

ANA3T	20-018	23-029	22-039
	03.5	02.5	
AR00F	04-003	15-021	37-039
	07.5	12.0	
AR00T	15-030	16-028	
	02.0		
AR01F	04-005	15-024	37-047
	07.5	12.0	
AR01T	15-025	16-001	
	04.0		
AR02F	04-007	15-001	37-043
	06.5	14.5	
AR02T	15-012	16-034	
	04.0		
AR03F	04-009	15-014	37-045
	06.5	13.0	
AR03T	15-020	16-027	
	02.0		
AR04F	04-011	13-021	36-039
	06.0	12.5	
AR04T	13-030	14-028	

	02.0		
AR05F	04-013	13-024	36-047
	06.0	12.5	
AR05T	13-025	14-001	
	04.0		
AR06F	04-015	13-001	36-043
	06.5	14.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
AR06T	13-012	14-034		
	04.0			
AR07F	04-017	13-014	36-045	
	05.5	13.5		
AR07T	13-020	14-027		
	02.0			
AR08F	04-019	11-021	35-039	
	04.5	12.5		
AR08T	11-030	12-028		
	02.0			
AR09F	04-021	11-024	35-047	
	04.5	13.0		
AR09T	11-025	12-001		
	04.0			
AR10F	04-023	11-001	35-043	
	06.5	15.0		
AR10T	11-012	12-034		
	04.0			
AR11F	04-025	11-014	35-045	
	05.5	13.5		
AR11T	11-020	12-027		
	02.0			
AR12F	04-027	09-021	34-039	

	14.0	13.0	
AR12T	[illegible]	10-028	
	12.0		
AR13F	[illegible]	03-024	34-047
	14.0	13.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DCT
AR13T	09-025	10-001		
	04.0			
AR14F	04-031	09-001	34-043	
	06.5	15.5		
AR14T	09-012	10-034		
	04.0			
AR15F	04-033	09-014	34-045	
	05.5	14.0		
AR15T	09-020	10-027		
	02.0			
AW00	04-004	08-005	37-011	39-010	42-033
	02.5	13.5	02.5	04.5	
AW01	04-006	08-010	37-009	39-039	42-041
	03.5	12.5	05.0	02.5	
AW02	04-008	08-013	37-013	42-022	
	03.0	13.0	04.5		
AW03	04-010	08-015	37-015	42-003	
	03.0	13.0	04.5		
AW04	04-012	08-017	36-011		
	03.0	13.0			
AW05	04-014	08-022	36-009		
	03.5	13.5			

AW06	04-016	08-021	36-013	39-026
	13.0	13.5	03.5	
AW07	04-018	08-027	36-015	39-014
	13.5	13.5	02.5	
AW08	04-020	08-031	35-011	39-013
	03.5	14.0	03.0	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE		TITLE
17-0	3R925400	AA		OCT	
AW09	04-022	08-032	35-009	39-011	
	04.0	14.0	03.0		
AW10	04-024	08-035	35-013	39-026	
	03.5	14.5	04.5		
AW11	04-026	08-039	35-015	39-028	
	04.0	14.5	04.5		
AW12	04-028	08-040	32-015	34-011	39-033 42-024
	04.0	13.0	02.5	05.5	03.0
AW12C	42-025	X06-012			
	50.6				
AW13	04-030	08-043	32-017	34-009	39-019 42-026
	04.0	13.5	03.0	04.5	03.5
AW13C	42-027	X06-014			
	50.6				
AW14	04-032	08-046	32-019	34-013	39-027 42-028
	04.5	13.5	02.5	04.5	02.5
AW14C	42-029	X06-016			
	55.6				
AW15	04-034	08-047	32-025	34-015	39-025 42-030
	04.0	13.0	03.0	04.5	03.0
AW15C	42-031	X06-018			
	55.6				

A00A	[illegible]-003	16-007
	05.0	
A00B	16-[illegible]09	28-009
	06.0	
A01A	08-107	16-011
	05.0	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DCT
A01B	16-013	28-005		
	07.0			
A01C	16-014	17-036		
	04.0			
A02A	08-009	16-035		
	07.0			
A02B	16-037	27-009		
	08.5			
A02C	16-038	23-033		
	04.5			
A03A	08-014	16-039		
	06.5			
A03B	16-041	27-005		
	09.5			
A03C	16-042	17-038		
	02.0			
A04A	08-018	14-007		
	04.5			
A04B	14-009	25-009		
	06.0			
A04C	14-010	23-047		
	08.5			

A05A	18-019	14-011
	04.5	
A05B	14-013	26-005
	07.0	
A05C	14-014	23-041
	07.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
A06A	08-023	14-035		
	05.0			
A06B	14-037	25-009		
	08.5			
A06C	14-038	17-037		
	02.5			
A07A	08-025	14-039		
	05.0			
A07B	14-041	25-005		
	09.5			
A07C	14-042	17-031		
	03.5			
A08A	08-029	12-007		
	05.0			
A08B	12-009	24-009		
	06.0			
A09A	08-030	12-011		
	04.5			
A09B	12-013	24-005		
	07.0			
A10A	08-033	12-035		
	03.0			

A10B 12= 37 17=040

03.5

A11A 08=036 12=039

03.0

A11B 12= 41 17=034

04.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DCT
A12A	08-037	10-007		
	05.0			
A13A	08-041	10-011		
	05.0			
A14A	08-044	10-035		
	02.5			
A15A	08-045	10-039		
	02.5			
CARA	36-037	37-035		
	02.0			
CARB	35-037	36-035		
	02.0			
CARC	34-037	35-035		
	02.0			
CARY1	27-048	28-012		
	05.5			
CARY2	26-048	27-012		
	05.5			
CARY3	25-048	26-012		
	05.5			
CARY4	24-048	25-012		
	05.5			

CDIN1 37-127 38-004

04.0

CDIN2 36-127 37-028

02.0

CDIN3 35- 27 36-028

02.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3A925400	AA	OCT	

CDIN4	34-027	35-028						
	02.0							
CDIN5	34-028	39-016						
	04.5							
CD60	32-031	33-047						
	03.5							
CD60F	32-029	33-045						
	03.5							
CFLAF	23-017	24-025	25-025	26-025	27-025	28-025	28-004	27-004
	02.5	01.5	01.5	01.5	01.5	03.0	01.5	
	27-006	26-006	25-006	24-006				
	01.5	01.5	01.5					
CHL	02-043	20-039						
	09.0							
CHLT	19-030	20-036						
	02.5							
CINF	02-046	15-003						
	10.5							
CLAL1	38-005	39-022						
	03.5							
CLAL2	38-031	39-005						
	04.5							

CLRAF 37=010 38=024

13.0

CLRBF 36=010 38=025

03.5

CLRCF 35=010 38=026

04.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
CLRDF	34-010	38-027		
	04.5			
CL2AF	37-031	38-014		
	03.5			
CL2BF	36-031	38-015		
	03.5			
CL2CF	35-031	38-016		
	04.0			
CL2DF	34-031	38-017		
	04.5			
CMP	38-013	39-033		
	03.5			
CMPAF	37-004	38-007		
	01.5			
CMPBF	36-004	38-010		
	02.5			
CMPCF	35-004	38-009		
	02.5			
CMPDF	34-004	38-011		
	03.5			
CMPF	38-006	39-007		
	01.5			

CNCT 17-021 18-004

17.5

COMP 23-043 24-004 25-004 26-004 27-004 28-004

15.5 01.5 01.5 01.5 01.5

CONR 32-005 33-021

03.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DST
CONI	32-008	33-019		
	02.5			
CONR	27-027	18-005		
	08.0			
CONS	32-006	33-017		
	02.5			
CONT	15-006	18-003		
	02.5			
CSA0	02-003	20-015		
	09.5			
CSA0T	20-014	24-039	22-048	
	05.0	03.0		
CSA1	02-005	20-013		
	09.5			
CSA1T	20-009	24-020	22-047	
	04.0	04.5		
CSA2	02-007	20-010		
	09.0			
CSA2T	20-007	24-022	22-044	
	04.5	04.5		
CSA3	02-009	20-005		
	09.0			

CSA3T	23-003	24-019	22-045	
	04.5	04.5		
CSRX	03-004	42-010		
	17.5			
CSR0	02-011	03-005	17-003	21-047
	02.5	07.0	07.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	

CSB0T	21-045	22-036	25-039	
	02.5	02.5		
CSB1	02-013	03-003	21-046	
	02.5	13.0		
CSB1T	21-044	22-035	25-020	
	02.5	04.0		
CSB2	02-015	21-043		
	11.5			
CSB2T	21-041	22-032	25-022	
	02.5	03.5		
CSB3	02-017	21-040		
	11.5			
CSB3T	21-037	22-033	25-019	
	02.0	04.0		
CSCX	03-008	42-011		
	17.0			
CSC0	02-019	03-013	17-004	21-039
	02.5	08.0	06.0	
CSC0T	21-036	22-030	26-039	
	02.5	03.5		
CSC1	02-021	03-011	21-035	
	02.5	11.0		

CSC1T	21-033	22-029	26-020
	02.0	04.0	
CSC2	02-023	03-009	21-032
	03.0	11.0	
CSC2T	21-030	22-026	26-022
	02.0	03.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3R925400	AA	OCT	
CSC3	02-025	03-007	21-031	
	03.5	11.0		
CSC3T	21-029	22-027	26-019	
	02.0	03.5		
CSDX	03-016	42-013		
	17.0			
CSD0	02-027	03-021	17-006	21-027
	02.5	08.5	04.5	
CSD0T	21-025	22-023	27-039	
	02.0	05.0		
CSD1	02-029	03-019	21-021	
	02.5	08.5		
CSD1T	21-023	22-022	27-020	
	02.0	03.5		
CSD2	02-031	03-017	21-022	
	03.0	09.0		
CSD2T	21-019	22-017	27-022	
	02.0	04.0		
CSD3	02-033	03-015	21-017	
	03.5	08.5		
CSD3T	21-018	22-019	27-019	
	01.5	03.5		
CSEX	03-024	42-015		

17.5

CSEn 02-035 03-029 17-008 21-015

02.5 09.0 03.5

CSEnT 21-014 22-010 28-039

02.0 06.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3892540D	AA		DCT
CSE1	02-037	03-027	17-010	21-013
	02.5	08.5	03.0	
CSE1T	21-009	22-007	28-020	
	02.0	05.0		
CSE2	02-039	03-025	21-010	39-031
	03.0	10.0	10.5	
CSE2T	21-007	22-006	28-022	
	02.0	05.5		
CSE3	02-041	03-023	21-005	39-029
	03.5	10.5	11.0	
CSE3T	21-003	22-005	28-019	
	02.0	05.0		
C1771	32-003	33-004		
	02.0			
DDT	18-009	22-011	23-003	
	03.0	02.5		
DIG	02-004	20-027		
	10.5			
DIGT	20-025	23-030	22-042	
	03.0	03.0		
DSABL	03-001	X06-005	42-021	
	13.0	14.5		

EDT	22-009	24-038	25-038	26-038	27-038	28-038	33-048
	05.0	01.5	01.5	01.5	01.5	04.5	
EOS	12-047	23-044	22-004				
	10.0	05.5					
EOSNF	05-007	05-015	23-046				
	02.0	11.5					

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
ETC	38-001	39-004		
	02.0			
EXSNF	05-013	05-021	17-041	
	02.0	08.0		
FAPA	23-032	26-011		
	04.5			
FIELD	03-048	42-043	X06-003	
	17.0	16.5		
FNCTO	07-032	17-035	16-010	
	05.5	04.5		
FNTF1	17-043	23-045		
	04.0			
FNTF3	17-046	32-011		
	10.5			
FPAF1	24-035	26-014		
	04.5			
FPAF2	25-035	26-015		
	03.5			
FPAF3	26-016	26-035		
	03.0			
FPAF4	26-017	27-035		
	03.5			

FPAF5	26-018	28-036
	03.5	
GRD	02-001	02-002
	01.0	
	02-049	02-050
	01.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		PCT

04-001 04-002
01.0

04-049 04-050
01.5

06-001 06-002
01.0

06-049 06-050
01.5

08-002 08-011 08-020
02.5 02.5

08-034 08-042 08-050
02.0 02.0

09-002 09-016 09-022
02.5 02.0

09-026 09-050
03.5

10-002 10-003 10-004 10-006 10-008 10-022 10-024
01.5 01.5 01.5 01.5 02.5 01.5

10-030 10-031 10-032 10-036 10-058
01.5 01.5 01.5 02.5

11-002 11-016 11-022
02.5 02.0

11-026	11-034	11-050
12.0	03.0	
12-022	12-022	12-024
03.5	01.5	
12-032	12-036	12-050
01.5	02.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	

13-002	13-016	13-022
02.5	02.0	
13-026	13-034	13-050
02.0	03.0	
14-002	14-022	14-024
03.5	01.5	
15-002	15-016	
02.5		
15-026	15-034	15-050
02.0	03.0	
16-002	16-022	16-024
03.5	01.5	
20-002	20-011	20-020
02.5	02.5	
20-034	20-050	
03.0		
21-002	21-011	21-020
02.5	02.5	
21-034	21-042	21-050
02.0	02.0	
22-002	22-016	22-024
02.5	02.0	
24-047	24-050	

01.5

25-'47 25-050

01.5

26-'47 26-050

01.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
17+0	38925400	AA		DCT
	27-047 27-050			
	01.5			
	38-034 38-050			
	03.0			
	39-034 39-050			
	03.0			
	41-048 41-050			
	01.5			
	X06-001 X06-040 27-002			
	03.5 11.0			
GRDC	T2-004 42-050			
GRDC	TB1-003 P01-003			
GRDC	TB4-002 38-050			
GRDC	TB5-001 TB4-009			
GRDC	X11- C TB5-005			
GRDC	X12- C TB5-014			
GRDC	X13- C TB5-023			
GRDC	X14- C TB5-032			
GRDC	X15- C TB5-041			
GRDC	X16- C TB5-008			

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GRDC                    X17=  C     T85=017

GRDC                    X18=  C     T85=026

GRDC                    X19=  C     T85=035

GRDC                    X20=  C     T85=044

GRDC                    X21=  C     T85=011

GRDC                    X22=  C     T85=020

GRDC                    X23=  C     T85=029

GRDC                    X24=  C     T85=038
```

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		OCT

GRDC X25= C T85-047

GRDC X30= CT T84-003

GRDC X31= CT T84-004

GRDC X32= CT T84-005

GRDC X33= CT T84-006

GRDC X37-002 X36-002 X35-002 X34-002 T84-007

INPF 38-003 39-012
02.5

LDRAF 37-119 38-018
02.0

LDRBF 36-019 38-019
02.0

LDRCF 35-019 38-020
02.5

LDRDF 34-019 39-021
03.0

LFLAF 23-115 24-003 25-003 26-003 27-003 28-003 29-032 30-032
03.0 01.5 01.5 01.5 01.5 04.0 01.5

27-032 26-032 25-032 24-032
01.5 01.5 01.5

LRHBF 17-124 23-007 39-042
05.0 11.5

LRHR1 13-19 17-025

03.5

LRRYF 17-022 23-009 38-041

04.5 10.5

LRRY1 11-019 17-023

04.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3R925400	AA	OCT	

LSCNF	05-009	05-017	32-024	
	02.0	13.0		
LSTAF	17-005	39-035		
	13.0			
LSTA1	17-009	32-023		
	08.5			
LWHRF	17-026	23-008	32-027	39-040
	05.5	06.5	05.5	
LWHR1	09-019	17-021		
	04.5			
LWRY	17-045	19-038		
	03.0			
LWRYF	19-039	23-010	32-026	39-038
	06.0	06.5	05.5	
MANLF	42-023	X06-009		
	14.5			
MCL	02-026	07-039	42-045	
	04.5	16.0		
MCLF1	17-031	17-047		
	07.0			
MCLF3	07-036	23-042		
	08.5			

MCLF4	[illegible]-037	32-012	
	14.0		
MCLF5	[illegible]-038	39-008	
	17.0		
NAD	19-040	23-034	22-012
	03.5	04.0	

...TONAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1/50	38925400	AA		DCT
NAPA	23-023	25-011		
	03.5			
NA00	16-003	28-031		
	09.0			
NA01	16-004	28-021		
	07.5			
NA02	16-031	27-031		
	05.5			
NA03	16-030	27-021		
	06.5			
NA04	14-003	26-031		
	09.0			
NA05	14-004	26-021		
	07.5			
NA06	14-031	25-031		
	05.5			
NA07	14-030	25-021		
	06.5			
NA08	12-003	24-031		
	09.0			
NA09	12-004	24-021		
	07.5			
NA10	12-031	23-019		

97.0

NA11 12-030 23-021

06.5

NLK1 27-034 28-036

02.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
NLK2	26-034	27-036		
	02.0			
NLK3	25-034	26-036		
	02.0			
NLK4	24-034	25-036		
	02.0			
NLK5	15-004	23-006	24-036	
	04.5	04.5		
NPAF1	24-037	25-014		
	04.0			
NPAF2	25-015	25-037		
	03.5			
NPAF3	25-016	26-037		
	03.5			
NPAF4	25-017	27-037		
	04.0			
NPAF5	25-018	28-037		
	04.0			
NT01F	03-031	09-031	06-005	05-006
	03.5	05.0	02.0	
NT01T	09-034	17-042		
	05.5			

NT02F	03-033	11-031	06-007	05-008
	04.5	05.5	02.0	
NT03F	03-035	05-010	06-009	13-031
	04.5	01.5	06.5	
NT04F	03-037	05-012	06-011	15-031
	04.5	01.5	07.0	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
LIST	33925400	AA	OCT	
NT05F	03-039	05-014	06-013	09-023
	04.5	01.5	03.5	
NT06F	03-041	05-016	06-015	11-023
	04.5	01.5	04.0	
NT07F	03-043	05-018	06-017	13-023
	04.5	01.5	04.5	
NT08F	03-032	05-020	06-019	15-023
	03.5	01.5	05.5	
NT09F	03-034	05-022	06-021	09-013
	03.5	01.5	03.5	
NT10F	03-036	05-024	06-023	11-013
	03.5	01.5	04.5	
NT11F	03-038	05-026	06-025	13-013
	03.5	01.5	05.5	
NT12F	03-040	05-028	06-027	15-013
	03.5	01.5	06.5	
NT13F	03-042	05-030	06-029	09-003
	03.5	01.5	05.0	
NT14F	03-044	05-032	06-031	11-003
	03.5	01.5	06.0	
NT15F	03-046	05-034	06-033	13-003
	03.5	01.5	07.0	
OSC	32-048	33-007		

15.5

PANA 23-16 27-011

25.0

PFLNF 23-45 42-019

19.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		OCT
PFNS	17-030	18-029		
	01.5			
PNAF1	24-041	27-014		
	05.5			
PNAF2	25-041	27-015		
	04.5			
PNAF3	26-041	27-016		
	04.5			
PNAF4	27-017	27-041		
	03.5			
PNAF5	27-018	28-041		
	03.5			
PR0	02-020	20-040		
	10.5			
PR0SF	02-028	07-016	07-013	
	04.5	01.5		
PR0T	07-303	20-037		
	10.0			
PR02	07-009	18-008		
	06.0			
PR03	07-012	18-044		
	09.0			

QTpAF	23=031	24=044	25=044	26=044	27=044	28=044
	03.0	01.5	01.5	01.5	01.5	
QDDA	19=017	22=008	28=042			
	13.5	07.0				
QDDB	19=018	28=023				
	05.0					

SIGNAL LIST

	NAME	DRAWING #	REV.	DATE	TITLE
	1750	38925400	AA	OCT	
Q01A	09-045	28-029	22-003		
	10.5	06.5			
Q01B	09-046	28-026			
	11.0				
Q02A	11-045	22-021	27-042		
	08.0	05.5			
Q02B	11-046	27-023			
	09.5				
Q02C	11-043	13-044	23-022		
	12.5	07.5			
Q03A	13-045	22-018	27-029		
	07.5	04.0			
Q03B	13-046	27-026			
	09.0				
Q03C	13-043	23-018			
	08.0				
Q04A	19-023	22-028	26-042		
	03.0	04.5			
Q04B	19-024	26-023			
	04.0				
Q05A	19-033	22-025	26-029		
	03.5	03.5			
Q05B	19-034	26-026			

15.0

Q06A 19=45 22=034 25=042

13.5 03.5

Q06B 19=46 25=023

05.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		DCT
Q07A	07-041	22-031	25-029	19-007
	08.5	02.5	06.0	
Q07B	07-042	25-026		
	10.0			
Q08A	07-023	22-046	24-042	
	09.5	02.5		
Q08B	07-024	24-023		
	08.0			
Q09A	07-019	24-029	22-043	
	09.0	03.5		
Q09B	07-022	24-026		
	08.5			
Q10A	07-011	23-028	22-040	
	09.5	03.0		
Q10B	07-014	23-020		
	08.5			
Q11A	15-045	22-037	23-026	
	05.0	03.0		
Q11B	15-046	23-024		
	06.5			
Q15F	18-006	19-037		
	14.5			

RAL	19- 13	22-015	23-038
	12.5	04.0	
RARE1	10-025	18-022	
	05.0		
RARE2	12-025	18-019	
	04.5		

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	

RARF3	14-025	18-020				
	03.5					
RARF4	14-025	18-018				
	03.0					
RDT	18-023	22-013	23-004			
	04.0	02.5				
RENAF	37-021	38-045				
	04.0					
RENBF	36-021	38-046				
	04.5					
RENCF	35-021	38-047				
	05.0					
RENDF	34-021	38-048				
	05.5					
REX	02-016	18-017	17-007	24-008	20-047	38-042
	07.5	02.5	04.5	06.5	08.5	
REXT	18-025	19-025	20-045			
	01.5	03.5				
RHRF	04-035	13-011	18-040			
	07.5	06.5				
RJTF	12-048	18-014				
	11.0					
RNAF	23-014	24-013				

11.5

RNAF1 10- 26 24-014

08.0

RNAF2 12-026 24-015

07.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	
RNAF3	14-026	24-016		
	06.5			
RNAF4	16-026	24-017		
	05.0			
RNAT	23-016	24-011		
	02.0			
RPYF	18-027	23-035		
	04.0			
RPYT	18-024	23-037		
	04.5			
RRYF	04-037	11-011	18-031	
	06.5	06.0		
RS0F1	10-021	17-013		
	05.0			
RS0F2	12-021	17-014		
	04.0			
RS0F3	14-021	17-015		
	03.0			
RS0F4	16-021	17-016		
	02.5			
RS1F1	10-023	17-017		
	04.5			

RS1F2 12-123 17-018

04.0

RS1F3 14-123 17-019

03.0

RS1F4 14-123 17-020

02.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1/50	38925400	AA		DCT
SAM1	02-012	23-011	20-032	
	09.5	04.5		
SAM1T	19-008	20-030		
	04.0			
SAM2	02-014	23-012	20-031	
	10.0	04.0		
SAM2T	19-016	20-029		
	02.5			
SASS	19-015	23-005		
	04.0			
SRGC1	40-005	41-005		
	01.5			
SRGC2	40-007	41-007		
	01.5			
SRGI1	39-017	40-024	41-024	41-006	40-006
	02.5	01.5	03.0	01.5	
SRGI2	39-015	40-008	41-008	41-038	40-038
	02.5	01.5	04.5	01.5	
SRGNF	05-011	05-019	39-032		
	02.0	16.5			
SRG1	38-012	39-023			
	02.5				
SRG2	38-034	39-024			

12.5

SRSF1 18-35 19-027

12.5

SRSF2 19-21 19-001

13.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA	OCT	

STA	02-045	18-039	20-035	18-011	17-001	42-009
	18.5	02.5	04.5	02.5	12.5	
STALL	02-030	42-047				
	18.5					
STAT	19-028	20-033				
	02.0					
STLCF	42-035	X06-007				
	16.0					
STLNF	03-047	42-007				
	21.0					
STNA1	38-043	39-045				
	02.0					
STNA2	38-044	39-046				
	02.0					
STS00	07-030	16-006				
	07.5					
STS01	16-008	17-027				
	03.5					
STS02	15-009	16-032	23-040			
	04.0	05.0				
STS03	16-036	17-029				
	02.0					

STS04 13-009 14-006 32-007

02.0 08.5

STS05 14-008 15-005

01.5

STS06 13-005 14-032

04.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925600	AA		DCT
STS07	07-015	14-036		
	06.5			
STS08	12-006	15-010	23-039	
	03.0	07.0		
STS09	12-008	17-033		
	05.5			
ST00F	06-004	15-037	39-036	
	08.0	11.0		
ST00T	15-039	16-005		
	05.0			
ST01F	06-006	15-040	42-037	
	08.5	12.0		
ST01T	15-048	16-019		
	04.5			
ST02F	06-008	15-029	42-039	
	06.5	13.0		
ST02T	15-038	16-029		
	02.5			
ST03F	06-010	15-032		
	07.0			
ST03T	15-033	16-033		
	01.5			
ST04F	06-012	13-037		

16.5

ST04T 13-39 14-005

05.0

ST05F 06-14 13-040

06.5

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	38925400	AA		OCT
ST05T	13-148	14-019		
	04.5			
ST06F	06-016	13-029		
	05.0			
ST06T	13-038	14-029		
	02.5			
ST07F	06-018	13-032		
	05.5			
ST07T	13-033	14-033		
	01.5			
ST08F	06-020	11-037		
	04.5			
ST08T	11-039	12-005		
	05.0			
ST09F	06-022	11-040		
	05.0			
ST09T	11-148	12-019		
	04.5			
ST10F	06-024	11-029		
	03.5			
ST10T	11-138	12-029		
	02.5			

ST11F	10=026	11=032
	04.0	
ST11T	11=033	12=033
	01.5	
ST12F	06=028	09=037
	03.0	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
1750	3P925400	AA	OCT	
ST12T	09-039	10-005		
	05.0			
ST13F	06-030	09-040		
	03.5			
ST13T	09-048	10-019		
	04.5			
ST14F	06-032	09-029		
	02.5			
ST14T	09-038	10-029		
	02.5			
ST15F	06-034	09-032		
	02.5			
ST15T	09-033	10-033		
	01.5			
SYNU	32-010	39-021		
	05.0			
SYN1	02-022	20-043		
	10.5			
SYN1A	13-010	20-042	32-009	
	07.5	09.0		
SYN1B	09-009	20-041	39-009	
	09.0	12.0		
SYN2	02-024	17-012		

18.5

SYNOP 09-005 17-011 39-003

05.0 11.0

S1771 13-004 32-004

09.0

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
17=0	38925400	AA		DCT
S17AA	39-004	39-018		
	14.5			
TEX	19-026	19-036		
	02.5			
T1AF	37-033	38-022		
	03.0			
T1BF	36-033	38-023		
	03.0			
T1CF	35-033	38-029		
	03.0			
T1DF	34-033	38-030		
	03.5			
T2A	37-003	38-037		
	05.0			
T2B	36-003	38-038		
	05.5			
T2C	35-003	38-039		
	06.0			
T2D	34-003	38-033		
	06.0			
UNPF	06-003	11-004		
	03.5			

UNP2	11=[illegible]05	18=007						
	14.5							
UNP3	11=[illegible]16	18=043						
	07.0							
V*6	40=[illegible]35	41=035	41=045	41=046	41=049	40=049	X46=036	X46=035
	01.5	02.5	01.5	01.5	01.5	16.5	01.5	

SIGNAL LIST

NAME	DRAWING #	REV.	DATE	TITLE
[illegible]	38925400	AA	OCT	

V=6

07-047 09-047 10-047 11-047 12-047 13-047 14-047 15-047
02.0 01.5 01.5 01.5 01.5 01.5 01.5

15-047 16-047 18-047 19-047 17-044 32-047 40-019 41-019
11.5 02.0 01.5 02.5 07.5 07.5 01.5

X06-032 X06-031
14.0 01.5

WEX

12-018 23-013 32-021 39-041 42-048 20-046 17-049
10.0 05.5 06.0 06.0 14.0 02.5

WEXB

38-032 39-043
02.5

WEXT

18-028 19-026 20-044
02.0 03.5

WHRF

04-036 09-011 18-042 42-017
05.5 08.0 13.0

WNLKF

38-036 39-044
02.5

WRT

38-035 39-037
02.0

WRYF

04-038 18-041 19-042 42-028
07.0 02.0 12.5

WXA1F

34-038 39-047
03.5

WXA2F

38-040 39-048
02.5

Appendix A
INTERRUPT USAGE IN THE 1700 OPERATING SYSTEM

The 1700 Operating System provides multi-priority-level programming. When a 1705 Interrupt/Data Channel is installed, interrupting of programs from external devices becomes a major source of priority control. Interrupted and scheduled programs are held in "stacks." At the same time, active interrupts which operate at priority levels lower than the current operating level are masked so they cannot interrupt the current programs. The computer executes the highest priority program. This program runs to completion unless interrupted by another program of higher priority.

Up to 16 interrupt levels are available. The 15 external interrupts can be expanded to handle a maximum of 64 interrupt conditions by use of a 1549 Interrupt Interface. The interrupts are fanned into the 15 DCB interrupt lines. Determination of which interrupt activated the interrupt line requires additional software and is not discussed here.

INTERRUPTING CONDITIONS

There are 15 external and 1 internal hardware interrupt lines. In addition, scheduling a program of higher priority (jump to a higher priority program) uses some of the mechanics of processing a hardware interrupt.

INTERNAL HARDWARE

Three internal errors activate the same interrupt line (line 0):

a. Incorrect storage of information in core (parity error).

b. An erroneous attempt to store into or execute from protected core information by nonprotected programs (Protect Fault).

c. A power failure.

In all cases line 0, which normally is assigned priority 15 (highest of any interrupt line), interrupts the running program.

EXTERNAL HARDWARE

Fifteen external interrupt lines are provided; any of the lines can interrupt a running program of lower priority. When this interrupt occurs, the running program parameters are stored and the program associated with the interrupt line is executed. When the interrupting program is completed (barring further interrupts), control of the computer is returned to the first program. The interrupt line may be associated with the running program (e.g., an analog-to-digital input word is requested at higher priority and is now ready in the I/O unit) or with a more important program (e.g., arithmetic operations of low priority are interrupted by a process control device of high priority).

NOTE

Interrupt lines may be disabled or masked.

Disabling takes place when the unit attached to the interrupt line is directed not to send the interrupt under any conditions. The unit internal conditions, which cause the interrupt, occur but that unit's interrupt flip-flop does not set. The interrupt line remains inactive at all times.

Masking takes place via the Operating System Interrupt Mask Table. If a program A is operating at priority level P, all interrupt lines with priority levels $\leq P$ are masked. An interrupt line of priority $Q \leq P$ becomes active but it is not processed until the priority level is lowered to Q (or lower). For example, assume that programs A, B, C, D, E, and F have priority levels 10, 8, 8, 8, 7, and 4, respectively, and program Z has priority level 2. Parameters for programs A through F are held in the interrupt or scheduler stacks or they are programs associated with active hardware interrupt lines which have not been processed because they are masked at the current operating level. All these programs are executed before the priority level is

lowered to level 2 (or lower). Only then is the level 2 interrupt processed and the associated program executed.

Higher Priority Program Request

Running program A can request program B of higher priority than its own. Program A parameters are placed in the interrupt stack and program B is executed. After execution (barring further interrupts), control of the computer is returned to program A.

The following examples indicate the type of programming which requires scheduling a higher priority program.

EXAMPLE 1

Program A requests a message to be printed. The Operating System saves the request parameters, schedules the driver for the message output device, and then returns to the requester (program A). Program A then continues at its normal priority level. However, because the driver for the output device normally runs at a higher priority than program A, program A is saved first on the interrupt stack and the driver is initiated. Only after the driver exits to the dispatchers (e.g., after output of the first character of the message) is the return to program A made. (See Dispatcher Operation, below.)

EXAMPLE 2

Program A is normally interruptable by program B, which is of higher priority. If program A must set up data for use by program B, it may be illegal for program B to interrupt program A while this data is being changed. To prevent this occurrence, interrupts may be inhibited for this portion of program A. Alternatively, program A may schedule a subprogram to a level equal to or greater than the level of program B. This allows the subprogram to set up the desired data and then exit to the dispatcher. Program A then continues at its normal level.

NOTE

Every effort should be made to set up the system so that only short, fast programs are assigned high priority level.

Lower Priority Program Request

If program A requests program B of the same or lower priority level, program B is added to the scheduler stack. Execution of program A is then completed. Any other programs of higher priority than program B are then executed. Program B is called according to its scheduled priority.

PROGRAM PRIORITY CONTROL

Priority control is accomplished by means of the interrupt and scheduler stacks and the interrupt mask. The scheduler stack is a list of requested programs with priority equal to or lower than the current program. The scheduler stack threads the address and significant parameters of such programs to be processed when those programs are requested by other programs of the same or higher priority. The interrupt stack is a list of programs which have been interrupted by programs of a higher priority. This stack holds the address and significant parameters of programs which have been interrupted after starting execution.

The interrupt mask corresponds to the priority level of the running program. It prevents the running programs from being interrupted by a program of equal or lower priority.

Scheduler Stack

Scheduler stack (see Figure 1) entries are threaded together in two or more threads. The full thread links the entries of all scheduled programs; the entry thread joins unused entries. (A timer thread may also be present.) Each entry requires four consecutive locations in core. The entries contain

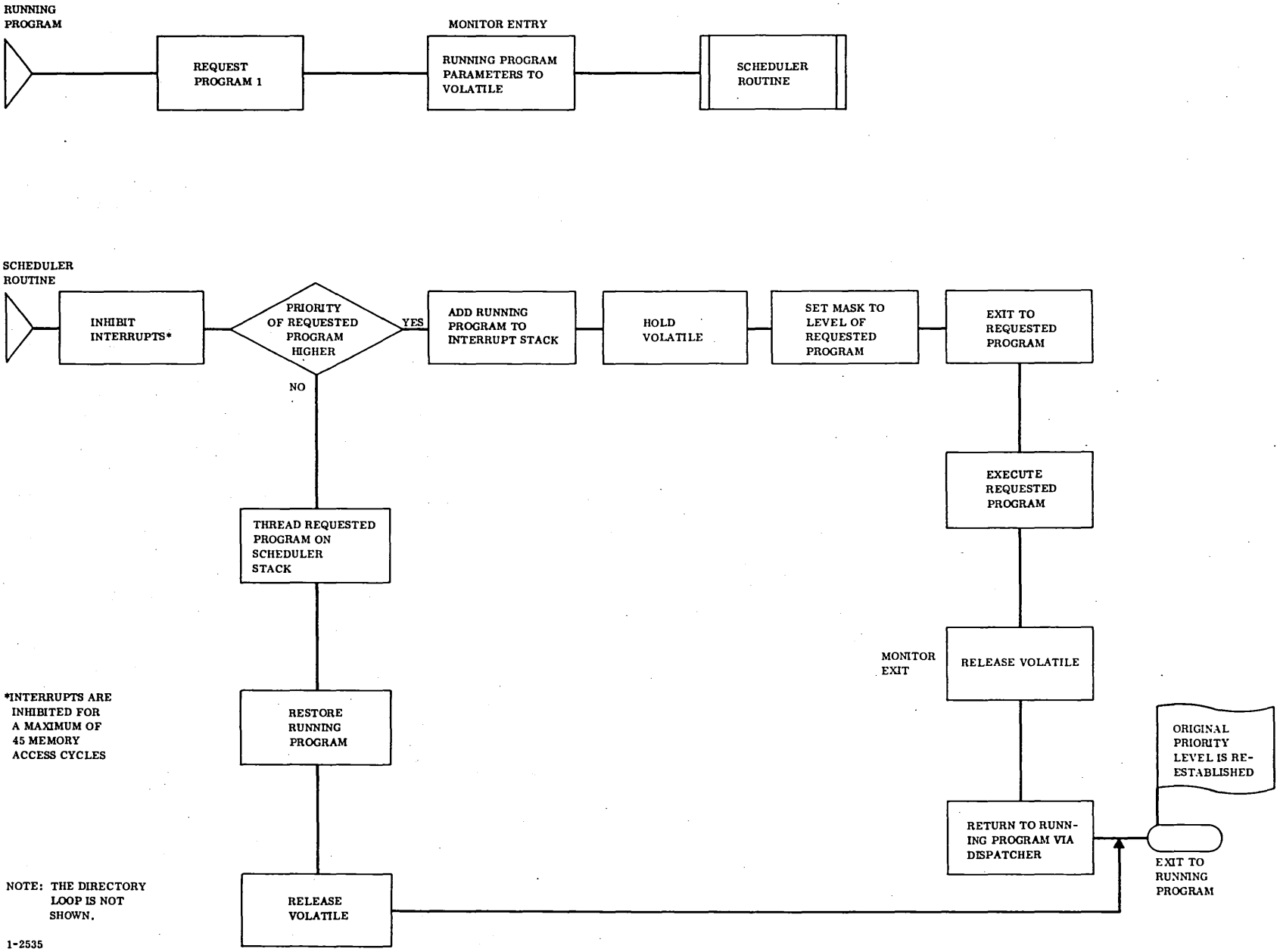


FIGURE 1. SIMPLIFIED FLOWCHART FOR SCHEDULING A REQUESTED PROGRAM

a. Parameters to be passed to the program.

b. Request code.

c. Completion priority of the program.

d. Program address.

e. A pointer to the next entry on the thread.

Programs are threaded in order of increasing priority so that the top entry on the full thread holds the highest priority program. If two or more programs have the same priority level, programs in this priority level are threaded on a first-come, first-served basis. When a program in the scheduler stack is removed to be executed, the thread entry point is added to the list of entries on the empty thread. If a program is requested when no entries remain on the empty thread (i.e., the stack is full), Q is set negative on the return to the requester and the request is ignored.

The scheduler stack is built when the Operating System is assembled. The length should be four times the number of timer calls and scheduler requests that may be active at any one time. As a rule of thumb, $4 \times 25_{10}$ or 100_{10} usually provides an adequate scheduler stack. The form of the stack is shown on pages A.13 and A.14.

While the scheduler is determining whether to put a requested entry in the scheduler stack or to put the running program in the interrupt stack, interrupts are inhibited and the running program parameters are assigned to volatile. Volatile is a specified area of the system table region designated at assembly time. It is used by re-entrant program for storage of necessary parameters and intermediate results. If the requested program is of higher priority, the running program parameters are transferred to the interrupt stack and the requested program is executed. If the requested program is of the same or lower priority, the entry parameters are threaded on the scheduler stack. After the determination is made, the interrupts are re-enabled and the interrupt mask is set to correspond to the current running priority level. The chosen program is then put into execution.

Interrupt Stack, Interrupt Trap, and Interrupt Mask

The interrupt stack (see Figure 2) consists of up to 16 five-word entries. Each entry holds data pointers for programs that have been interrupted. The stack is a push-down, pop-up type. The top-of-the-stack pointer is located at location $B8. It points to the first word of the next available entry.

The size of the interrupt stack should be the number of interrupt lines used (N) times 5. Normally this is 16_{10} x 5, or 90_{10} locations. The stack size is determined at operating program assembly time. A stack smaller than the full number of interrupt lines times five is subject to overflow.

When the interrupt stack entry is due to scheduling up in priority, some parameters from the interrupted program are saved in the volatile area. The I-register entry in the interrupt stack holds the address of that portion of volatile which has the remaining program parameters.

Volatile is not released until the higher priority program is terminated and the requesting program is resumed. The new priority level is established as in the hardware interrupt case. The interrupt mask is set to the new priority level before entering the requested program.

The interrupt mask allows only interrupts of higher priority than the running programs to be processed. All other interrupt lines are suppressed. The suppressed interrupt lines remain activated until the mask is reset to the priority level of the interrupt line (or lower).

Dispatcher Operation to Find Next Program

As higher priority programs are completed, they exit to the dispatcher. The next program is picked off the top of the interrupt or scheduler stack (see Figure 3). The priority level is lowered by the dispatcher to the level of the proposed program to be executed and the Mask register is reset.

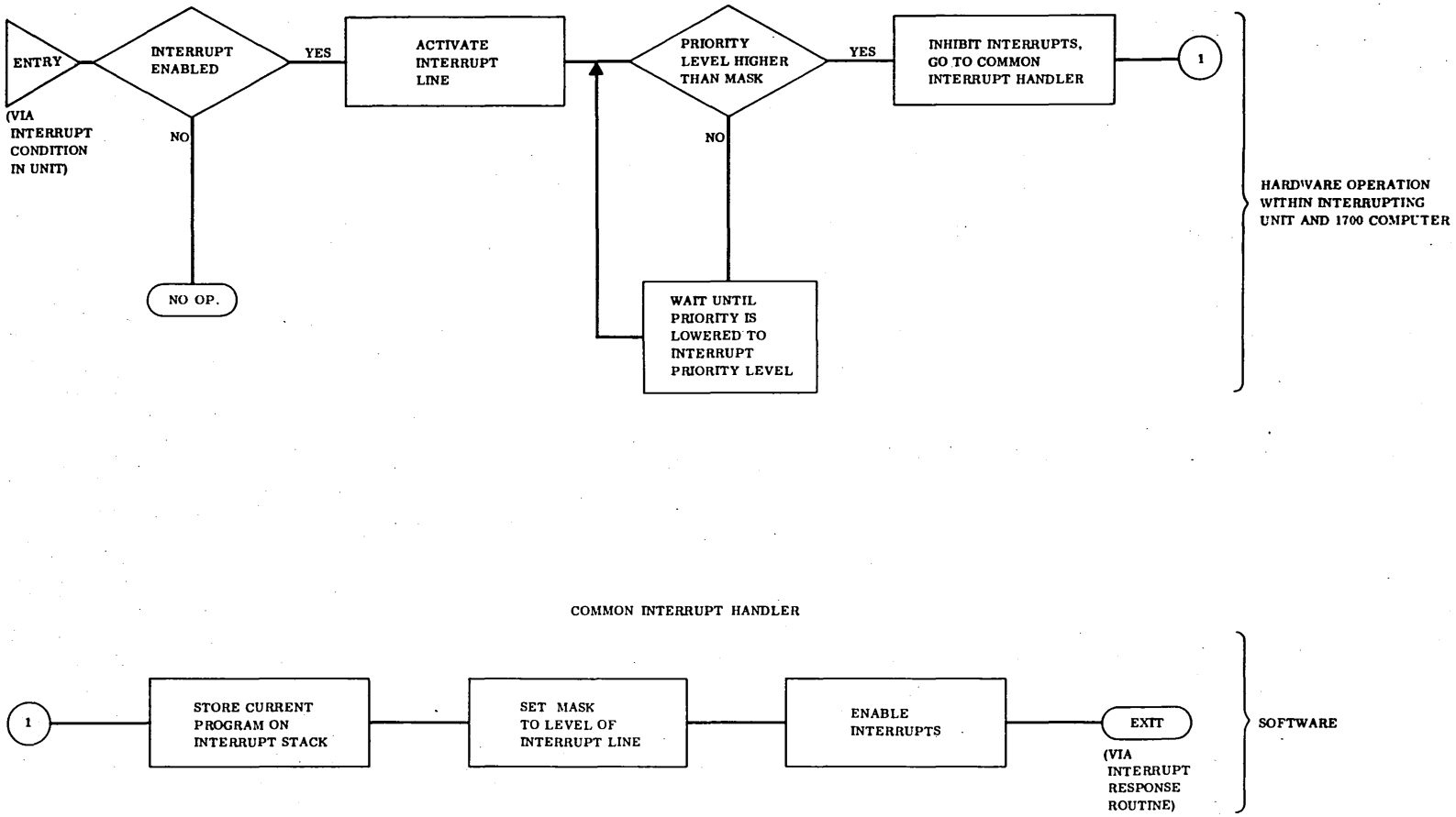
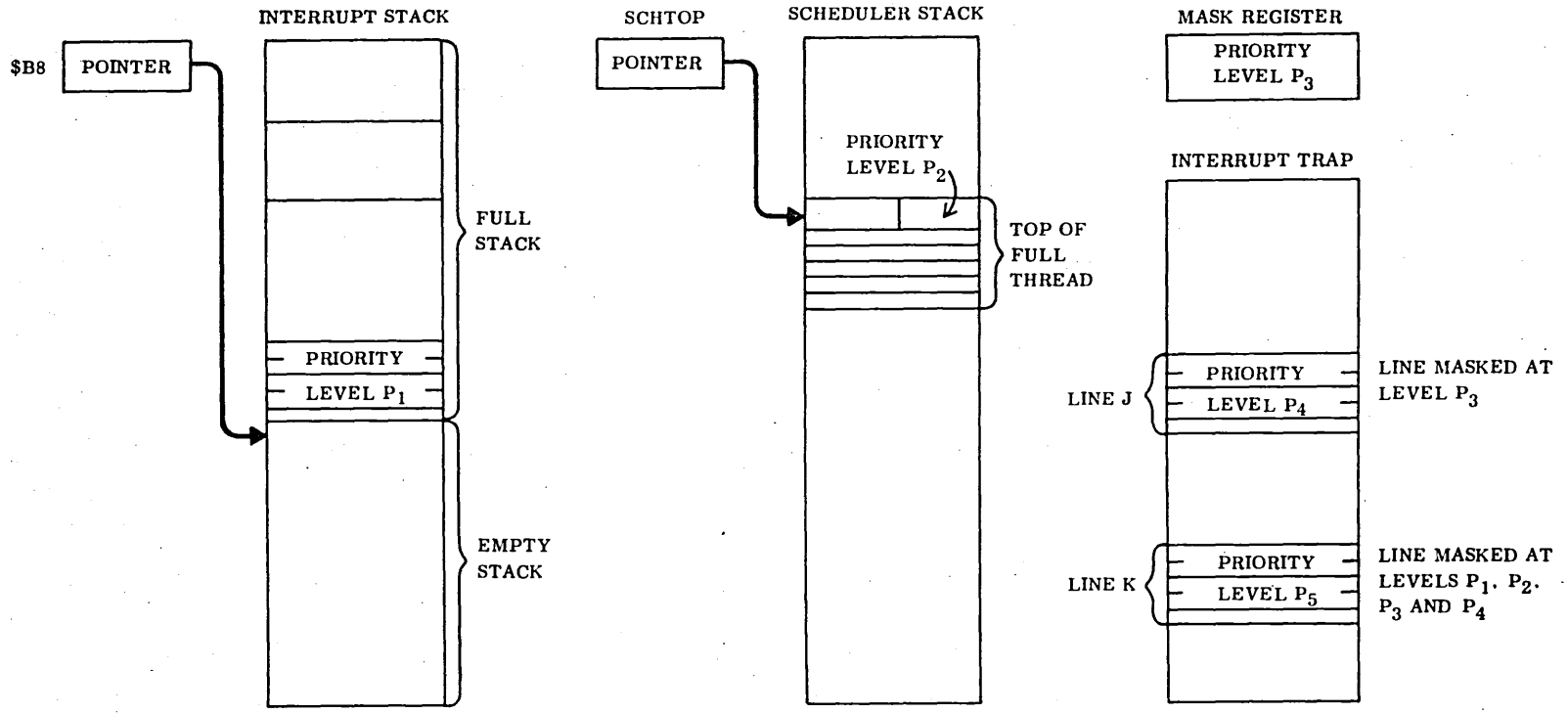


FIGURE 2. SIMPLIFIED INTERRUPT LINE PROCESSING FLOW DIAGRAM



PRIORITIES SHOWN AT THE END OF THE PREVIOUS PROGRAM. PREVIOUS PROGRAM RAN AT LEVEL $P_3 > (P_1, P_2, P_4, \text{OR } P_5)$.

SELECTION OF NEXT PROGRAM PROCEEDS IN TWO STAGES:

a. COMPARE P_1 TO P_2. IF $P_1 \geq P_2$, NEXT PROGRAM 1 COMES FROM P_1; OTHERWISE PROGRAM COMES FROM P_2.

b. CHANGE MASK LEVEL AND CHECK INTERRUPTS AT NEW LEVEL.

   LOWER MASK TO NEW LEVEL (P_1 OR P_2).

   IF $P_4 \geq$ NEW LEVEL, LINE J INTERRUPTS PUTS NEXT PROGRAM 1 ONTO THE INTERRUPT STACK, THE INTERRUPT LINE IS ACKNOWLEDGED, THE MASK IS SET TO P_4 LEVEL, AND THE PROGRAM ASSOCIATED WITH P_4 IS EXECUTED. IF $P_4 <$ NEW PRIORITY LEVEL, LINE J REMAINS MASKED. LINE K REMAINS MASKED IN ALL CASES SINCE $P_5 < (P_1, P_2, P_3, \text{OR } P_4)$.

1-2538

FIGURE 3. SELECTION OF NEXT PROGRAM WHEN PREVIOUS PROGRAM IS COMPLETED

NOTE

When the mask is reset, it may include one or more active interrupt lines. Those lines are processed. The proposed next program is moved to the interrupt stack and the program associated with the interrupting line is put into execution.

INTERRUPT LINE PRIORITY ASSIGNMENT

For maximum efficiency, the used interrupt lines should be assigned priorities on a scale of decreasing order of importance, i.e., line n + 1's priority ≤ line n's priority. Assignment is made this way because interrupting lines which have been masked are processed in line number order when several active lines are unmasked at the same time. In other words, an interrupt on line 0 is processed before an interrupt on line 1, which in turn is processed before an interrupt on line 2, etc., when all these active interrupt lines are unmasked at the same time. Assume, for example, a program operating at priority level 9 ends and the next highest entry in either interrupt or scheduler stack is priority 3. At the same time, three interrupt lines are active:

Line	Priority
5	4
6	7
10	8

In this case, the program with priority 3 becomes the next scheduled. The mask is set to priority level 3. As soon as interrupts are enabled, all three lines are capable of interrupting. Line 5 is processed first. Interrupts are inhibited, the associated priority 4 program is scheduled, the next scheduled program is transferred to the interrupt stack, the mask is set to level 4, and the interrupts are enabled. The same processes are repeated for line 6. Line 6 interrupts, interrupts are inhibited; the level 4 program goes to the interrupt stack, and the mask is raised to level 7. When the interrupts are again enabled, the process is repeated. Line 10 interrupts, interrupts are inhibited, the level 7 program is added to the interrupt stack, the mask is raised to level 8, and interrupts are again enabled. This program is the next to be executed.

Two disadvantages to this type of interrupt line assignment are apparent:

a. Each interrupt processing cycle requires 40 to 50 microseconds.

b. The interrupt stack is unnecessarily filled with programs that might have as well remained masked.

If, in the example given, the lines were assigned priority on a decreasing scale of priorities, the first interrupt would have been line 5 at priority 8, and the associated program would have been executed as soon as the interrupt mask was reset.

STACK ORGANIZATION

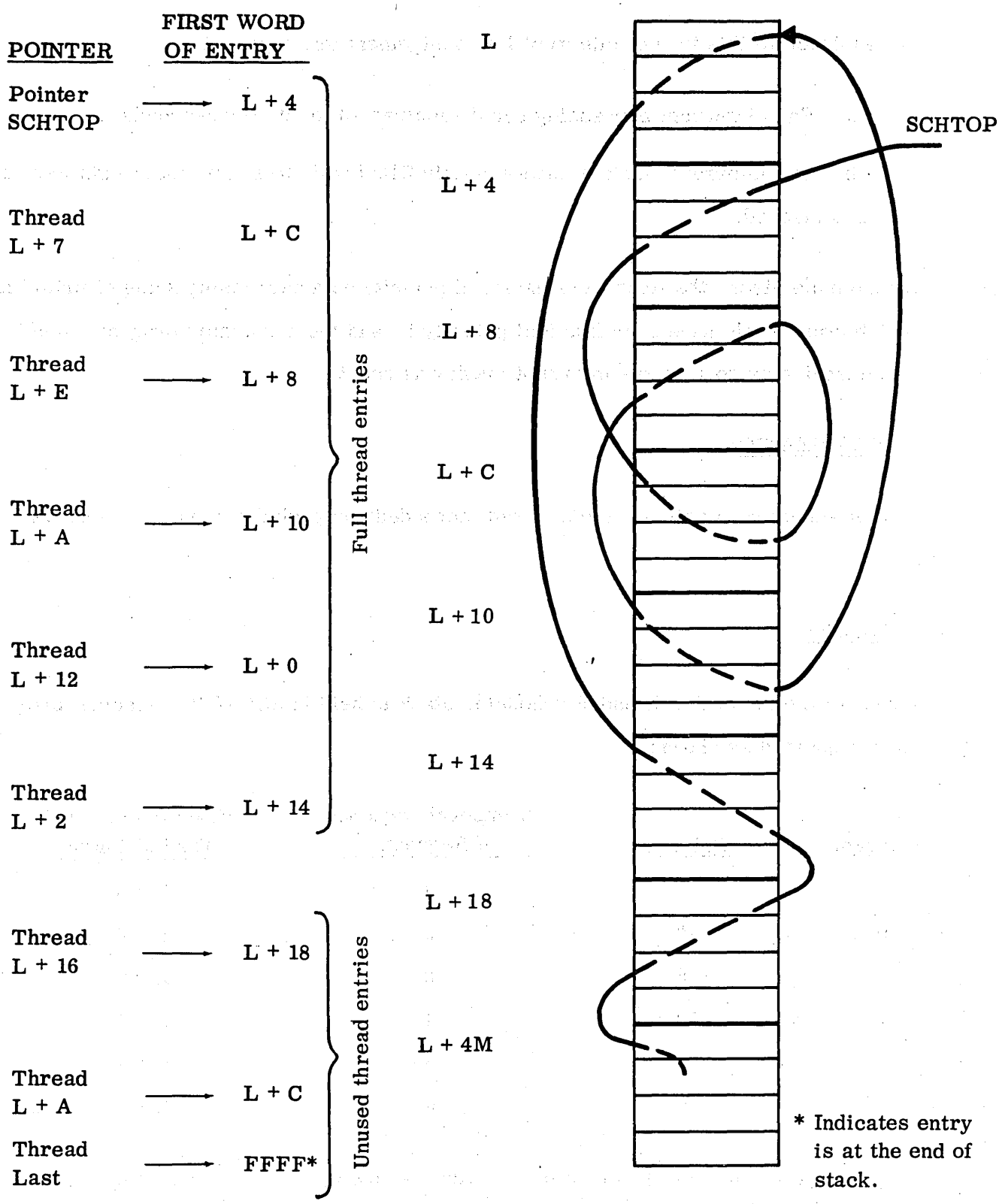
Two types of stack organization are discussed, threaded and push down/pop up. Both are described below.

Threaded Stacks

The address of the top of the threaded scheduler stack is held in SCHTOP. Assume programs are requested as shown:

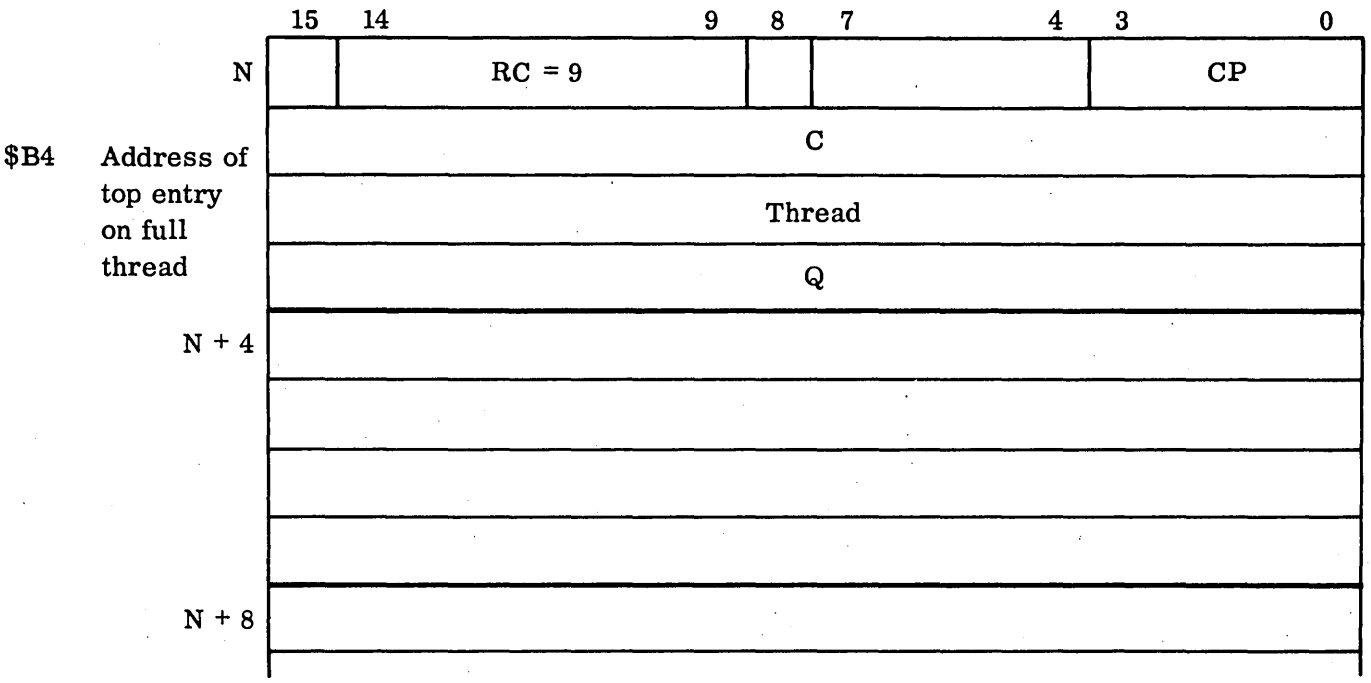
Program	Priority	Temporal Sequence of Requests	Location of First Word of Entry
A	6	1	L + 0
B	10	2	L + 4
C	9	3	L + 8
D	10	4	L + C
E	8	5	L + 10
F	6	6	L + 14

The programs are loaded into the stack in the order of column 3 with the top of each entry shown in column 4. They are threaded as follows:



As programs are removed from the stack the pointer ($B4) is moved consecutively through L + 4 → L + C → L + 8 → L + 12 → L + 0 → L + 14. It can then be reinitialized to L + 0 awaiting a new schedule of programs.

The form of the scheduler stack is shown below:



CP = Completion priority (level at which this entry runs).

Thread = Points to address of first word of next less important entry.

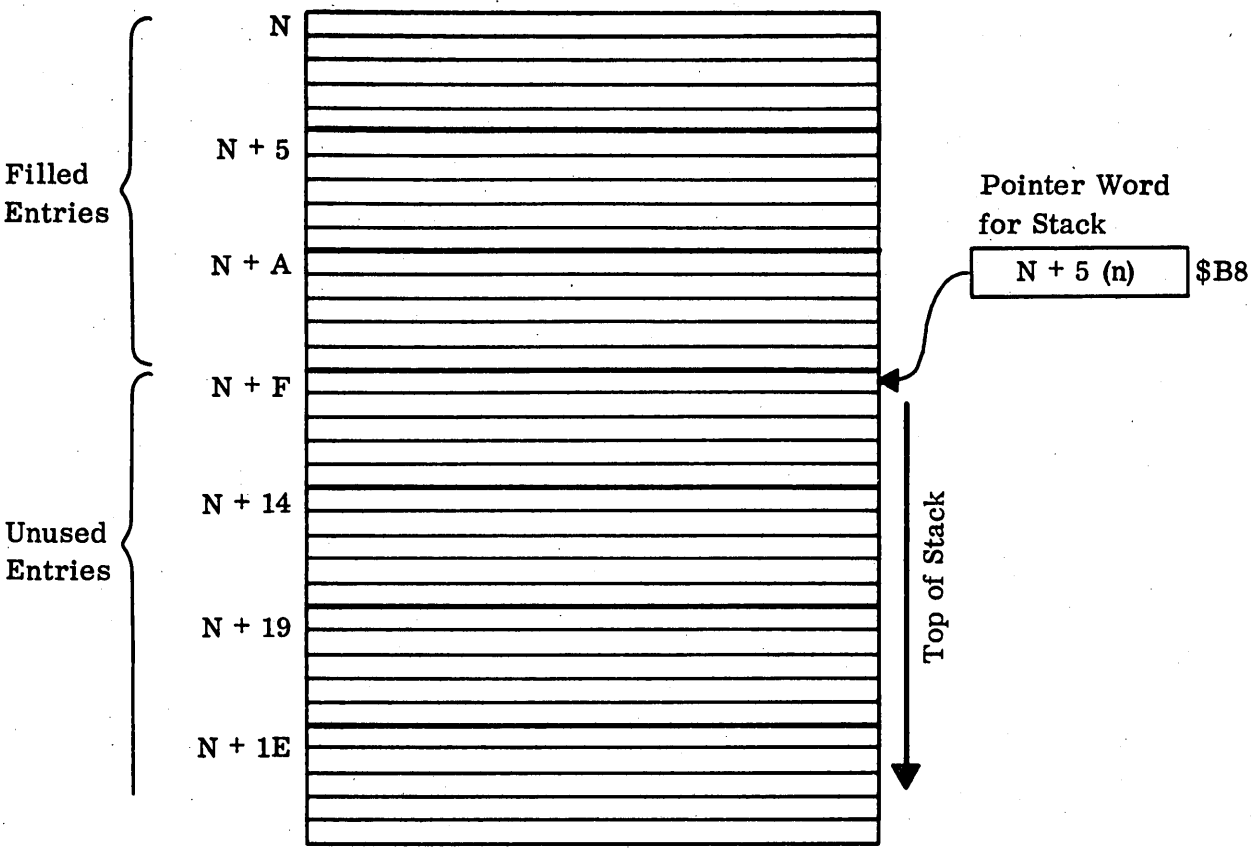
RC = 9 = Request code 9 (schedule) (refer to Control Data Publication No. 60170400, Paragraph 3.2.5)

Q = Contents of the Q-register at the time of request.

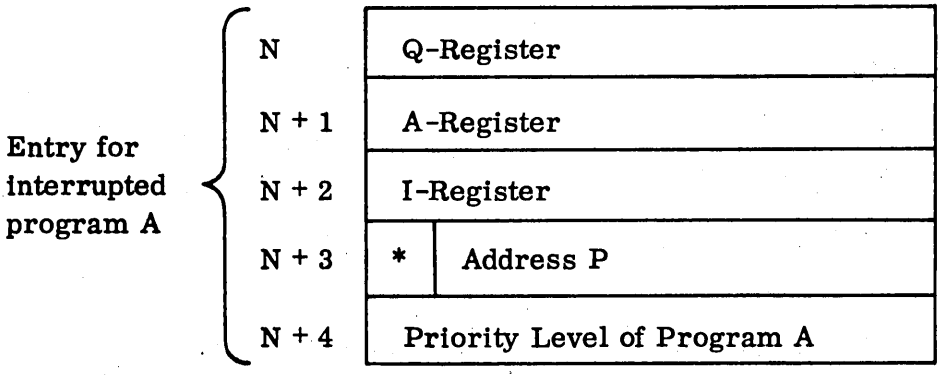
C = Program address.

Push-Down, Pop-Up Stacks

In the push-down, pop-up interrupt stack, entries are added to the top of the stack and the pointer is moved to the next available entry. When an entry is removed, it is always the top (last) entry and the pointer is moved back five words.



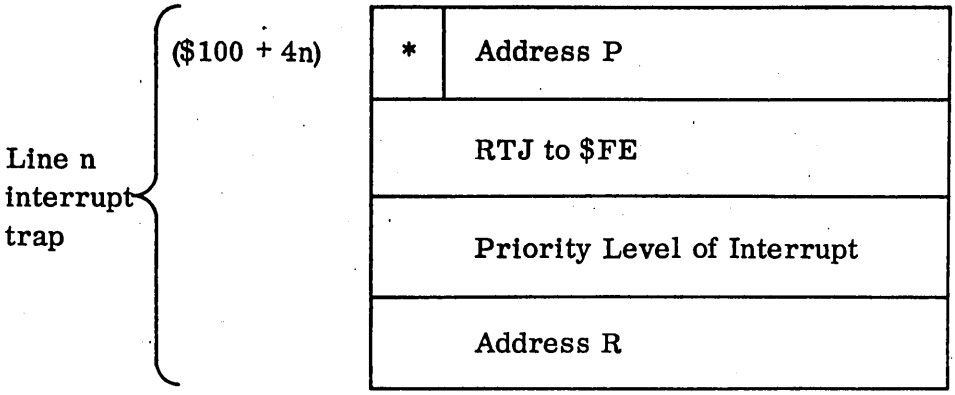
The structure of an entry is shown below:



P = Execution address when program A was interrupted

* Overflow indicator (bit 15)

The structure of the interrupt trap is



R = Address of the program that responds to the interrupt.

* Overflow indicator (bit 15)

Significant parameters and tables are

$FE Address of Common Interrupt Handler

MASKT

Priority Level	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 ← Internal Line Number
-1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1
0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1
+1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1
+2	0	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1
+3	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	1
+4	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	1
+5	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
+6	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
+7	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
+8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
+9	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
+10	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
+11	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
+12	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
+13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
+14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
+15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINE/PRIORITY LEVEL

LINE	PRIORITY LEVEL	
0	15	
1	13	
2	13	
3	8	
4	8	
5	8	
6	MASKED	LINES CAN NEVER BE PROCESSED
7	MASKED	
8	MASKED	
9	MASKED	
10	MASKED	
11	5	
12	5	
13	3	
14	3	
15	2	

MASK REGISTER

Entry from MASKT table corresponding the current priority level

$B8

Address of highest priority entry on the interrupt stack

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