Input/Output Specifications

CONTROL DATA® 1604-C COMPUTER

CONTROL DATA CORPORATION

Input/Output Specifications

CONTROL DATA®
1604-C COMPUTER

60003000	**Record of Revisions**
REVISION	NOTES
C (3-25-65)	This printing obsoletes all previous editions. The Product Designation for this equipment was previously the 1604 Computer.

Pub. No. 60003000
March, 1965

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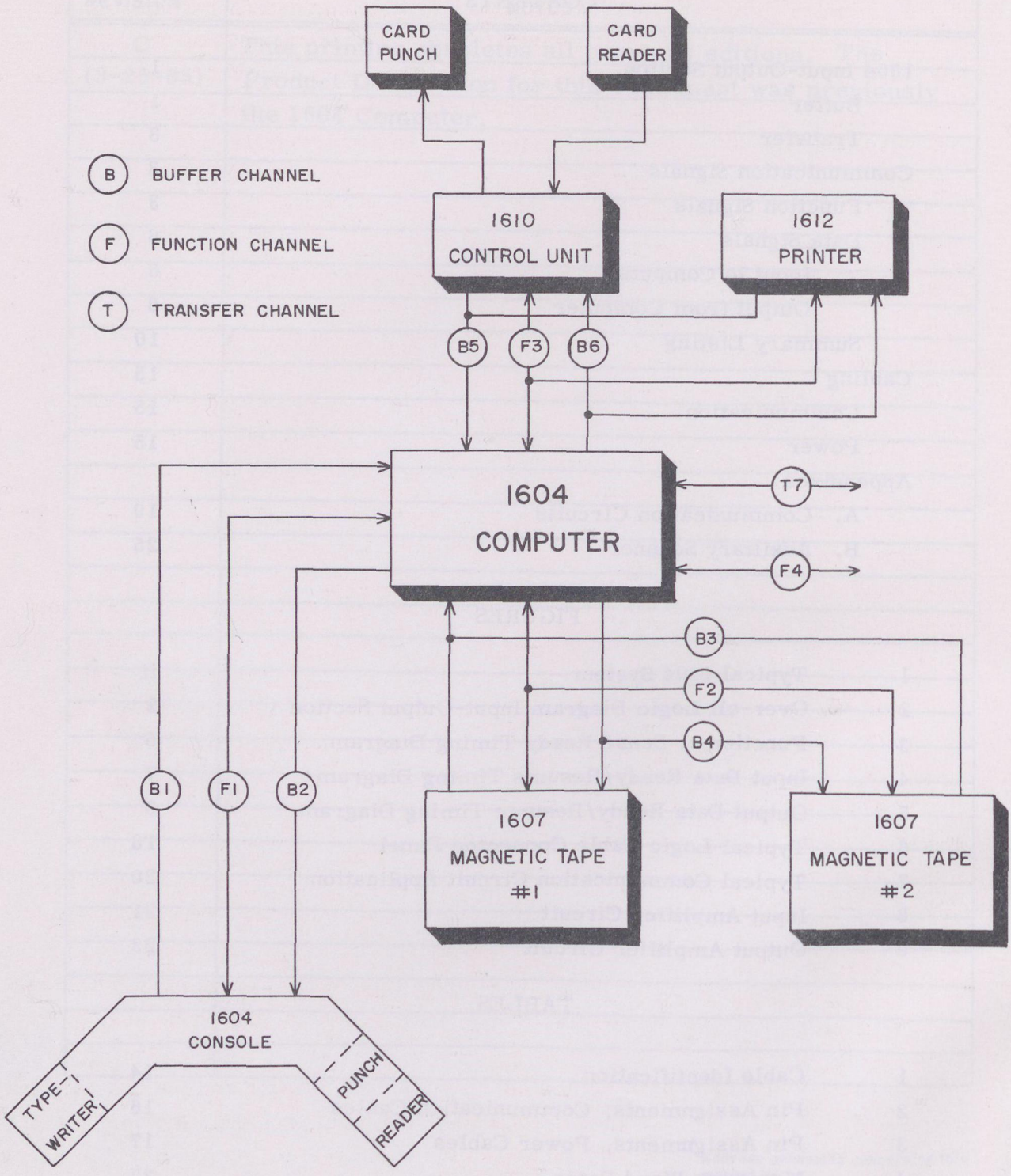


Figure 1. Typical 1604 System

This specification contains information necessary to attach an external equipment to the 1604 computer, either directly or indirectly, through such devices as the 1607 magnetic tape system, 1608 control unit, 1610 card control or the 1612 printer. This specification is written to allow a minimum data exchange time consistent with accepted engineering practices and moderate hardware requirements.

A typical 1604 system is shown in figure 1.

1604 INPUT-OUTPUT SECTION

The 1604 computer communicates with external equipment via six buffer channels and a single transfer channel. The buffer channels provide for the normal exchange of data with several equipments simultaneously. Exchange of data on buffer channels is program initiated but is carried out under control that is independent of the program. The transfer channel provides for very high speed exchange of data under direct program control.

BUFFER

Buffer operation is initiated by the main computer program and continues until finished at a rate determined by the external equipment (see Appendix B). The 1604 can perform a buffer with three input devices and three output devices concurrently. Each device determines the rate of its own data transmission and provides its own means of internal control. Buffer operations are started by the External Function (EXF 74) instruction.

Input buffer channels are numbered 1, 3 and 5; output buffer channels are 2, 4 and 6. Within the I/O section of the computer (figure 2) the three input buffer channels connect to the I^0 inverter rank which transmits the data to the X register. Each output channel is associated with a specific register. Data is held on the line until the external equipment has received and acknowledged receipt of the information. Each external equipment has an output register for sending information to one of the computer input channels.

The 1604 storage section is connected to both the arithmetic section and the I/O section, but it can be used by only one at a time. The buffer and main program, including transfer, must time share the storage section of the computer.

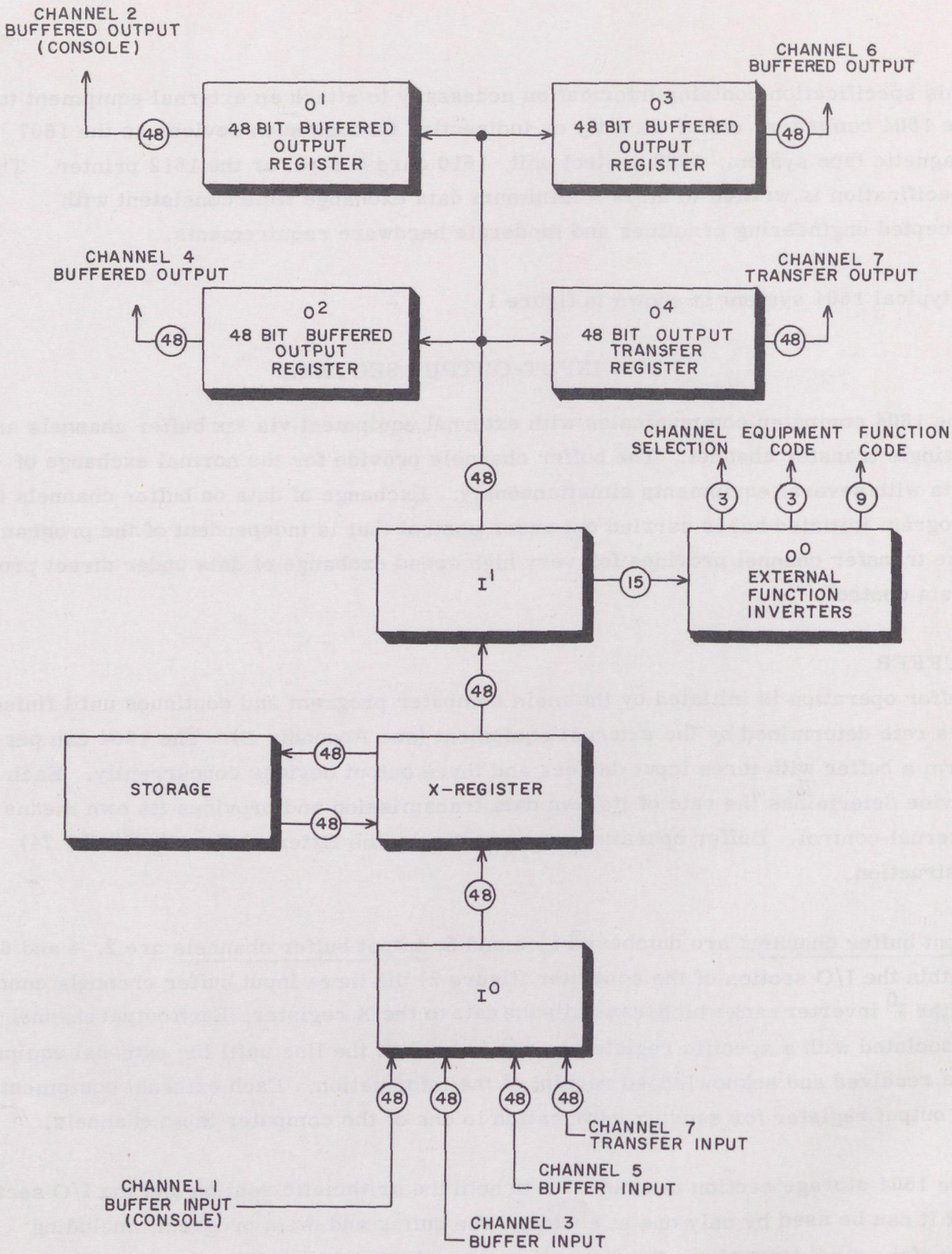


Figure 2. Over-all Logic Diagram Input-Output Section

Buffer channels are grouped for connecting to external equipment as follows:

Channel 1 - Buffer input
2 - Buffer output

3 - Buffer input
4 - Buffer output

5 - Buffer input
6 - Buffer output

TRANSFER

The transfer mode of communication is initiated and carried out by instructions in the main program. Information is transmitted in blocks of words by repetitive action, one repetition per word. The next program instruction is executed only after the last word of the block has been transmitted. (Buffer mode can occur concurrently with a transfer instruction if the buffer is initiated before the transfer instruction.) Input transfer of a block of information is performed by instruction 62, output transfer by instruction 63.

The maximum transfer rate is approximately one word every 5 usec. The transfer channel, consisting of input lines and output lines, connects to the X register as though it were a pair of buffer channels.

COMMUNICATION SIGNALS

Communication with external equipment is established with function signals and data signals. Function signals select an external equipment and direct it to perform some operation. Data signals carry the information to be exchanged. All function and data signals are voltage levels representing a binary "1" or "0". Pulse representation is used internally in the computer but not on the input-output lines.

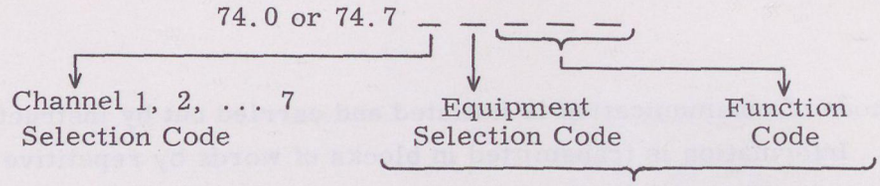
FUNCTION SIGNALS

The number of equipments with which the 1604 can communicate is limited by electrical considerations rather than by the number of I/O channels available. Several equipments can be linked to the computer by connecting jumper cables from one external equipment to another (figure 1). Each equipment is assigned an equipment selection code which it recognizes as a request for action; all other equipment selection codes are ignored. The codes are in the low order 12 bits of the EXF instruction.

EXF 74.0 ----- Selects an external equipment and places it in a mode of operation.

EXF 74.7 ----- Senses conditions such as ready or error in an external equipment.

The five octal digits of the base execution address are interpreted as shown below:



The external function lines carry the four low-order octal digits to the external equipment when an EXF Select or Sense instruction is programmed. The 1604 I/O control translates the channel selection digit and sends one of the following control signals to all equipments on the designated channel to allow each to sample the code.

Select (74.0)	Sense (74.7)
Signals	Signals
Input Function Ready	Input Sense Ready
Output Function Ready	Output Sense Ready

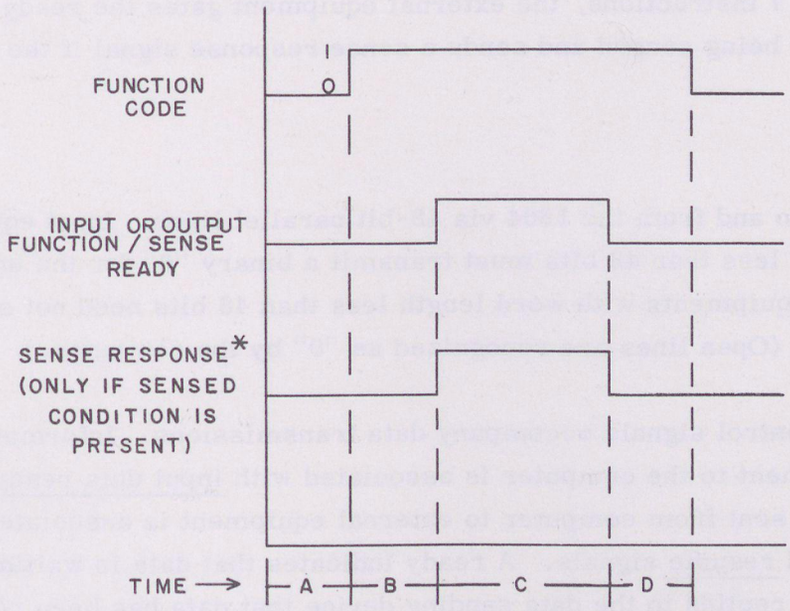
The selected equipment does not send a resume to the computer after an EXF select (74.0) instruction.

For EXF sense (74.7) instructions, the external equipment returns a sense response signal to the computer if the sensed condition is present.

Control circuits of all external equipments on channel X are cleared by an EXF 74.0X0000 (channel clear) code.

All external equipments must adequately resynchronize all control signals (signals other than data).

The control signal sequence for select and sense operations is (figure 3):



Time A - Time before EXF 74.0 (Select) or 74.7 (Sense) instruction

B - 4.5 usec

C - 6 usec

D - Varies with computer instruction sequence.

Figure 3. Function or Sense Ready Timing Diagram

*A logical "1" indicates presence of the exit condition specified by the sense code if the lowest bit of the sense code is a 0. A logical "0" indicates presence of the exit condition if the lowest bit of the sense code is a 1.

1) The computer executes an EXF 74.0 or 74.7 instruction to select or sense an external equipment and its operation.
2) The computer sends the input or output function/sense ready to allow the external equipment to sample the function lines.
3) For EXF 74.7 instructions, the external equipment gates the ready signal with the condition being sensed and sends a sense response signal if the condition is present.

DATA SIGNALS

Data is transmitted to and from the 1604 via 48-bit parallel lines. Input equipment with a word length of less than 48 bits must transmit a binary "0" for the unused higher-order bits. Output equipments with word length less than 48 bits need not sense the unused signal lines. (Open lines are recognized as "0" by the computer.)

Ready and resume control signals accompany data transmissions. Information sent from external equipment to the computer is associated with input data ready and resume signals; information sent from computer to external equipment is associated with output data ready and resume signals. A ready indicates that data is waiting to be sampled. A resume replies to the data sending device that data has been received and should be removed from the line.

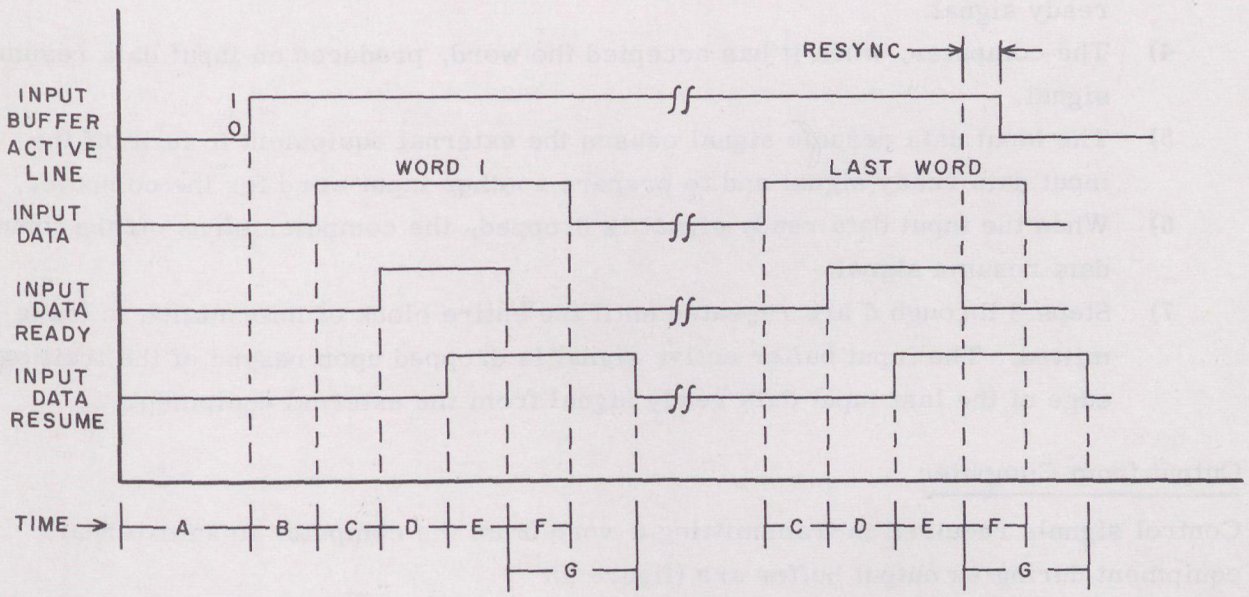
All data lines are stable before the information is sampled. A minimum fixed time of 2.6 usec elapses the instant the data appears on the output line until the accompanying output data ready signal is generated.

Labeling of input and output registers is referred to the pertinent external equipment. For example, data originating in the paper tape reader passes through the reader's output register and is sent to the computer's input register along with an input data ready. Upon receipt of the input data ready the computer stores the information and sends out an input data resume.

Input to Computer

Control signals required in transmitting a word from an external equipment to the computer during an input buffer are as follows (figure 4):

1) The computer, by the correct combination of external select codes, establishes the external equipment from which it is to take information.



Note: All signal timings refer to occurrences at the computer end of all transfers.

Time A - Time before input channel is active

B - Determined by input equipment

C - Determined by input equipment (input data and input data ready signals may be turned on at same time)

D - Minimum time 11.2 usec, maximum time 200 usec

E - Determined by input equipment

F - Determined by input equipment (input data and input data ready signals may be turned off at same time)

G - Minimum time 1.6 usec, maximum time 2.8 usec

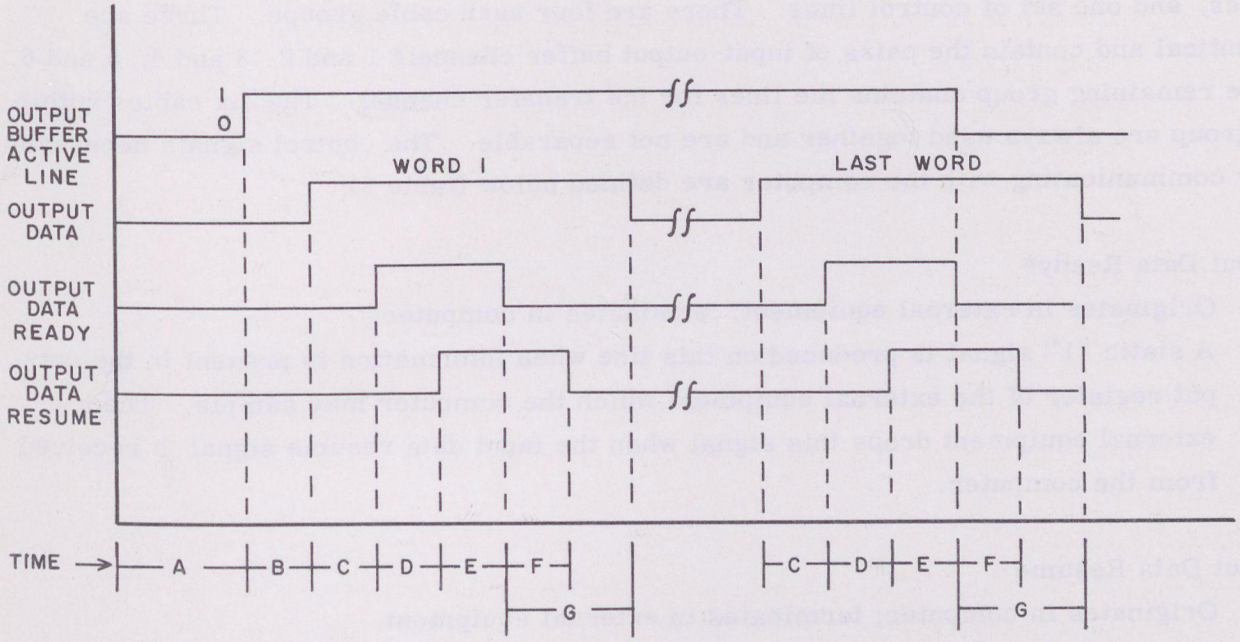
Figure 4. Input Data Ready/Resume Timing Diagram

2) The computer activates the input buffer active line to signal readiness to start data transfer.
3) The external equipment places a word on the lines and produces an input data ready signal.
4) The computer, when it has accepted the word, produces an input data resume signal.
5) The input data resume signal causes the external equipment to turn off the input data ready signal and to prepare another input word for the computer.
6) When the input data ready signal is dropped, the computer turns off the input data resume signal.
7) Steps 3 through 6 are repeated until the entire block of information is transmitted. The input buffer active signal is dropped upon resync of the trailing edge of the last input data ready signal from the external equipment.

Output from Computer

Control signals required in transmitting a word from the computer to an external equipment during an output buffer are (figure 5):

1) The computer, through the correct combination of external select and sense codes, establishes the equipment to which information is to be sent.
2) The computer activates the output buffer active line to indicate readiness to start data transfer.
3) The computer places a word in the associated output register. This energizes all data lines in parallel.
4) When all data lines are stable, the computer generates an output data ready signal which indicates to the external equipment that data is available on the lines in a stable steady-state form.
5) The external equipment accepts the output data ready signal and the information at its own rate and produces an output data resume signal which it returns to the computer after it has accepted the data.
6) The computer accepts the output data resume signal and turns off the output data ready signal.
7) When the output data ready signal is dropped by the computer, the output data resume signal is terminated within the external equipment.
8) Steps 3 through 7 are repeated until the entire block of information is transmitted. The output buffer active signal is dropped upon resync of the leading edge of the last resume from the external equipment.



Note: All signal timings refer to occurrences at the computer end of all transfers.

Time A - Time before output channel is active

B - Minimum time 6.2 usec, maximum time 83 usec

C - Minimum time 2.6 usec, maximum time 5.6 usec

D - Determined by output equipment

E - Minimum time 1.4 usec, maximum time 2.8 usec

F - Determined by output equipment

G - Varies with computer instruction sequence

Figure 5. Output Data Ready/Resume Timing Diagram

SUMMARY LISTING

Each cable group contains one input channel, one output channel, one set of function lines, and one set of control lines. There are four such cable groups. Three are identical and contain the pairs of input-output buffer channels 1 and 2, 3 and 4, 5 and 6. The remaining group contains the lines for the transfer channel. The six cables within a group are always used together and are not separable. The control signals necessary for communicating with the computer are defined below (table 2):

Input Data Ready*

Originates in external equipment; terminates in computer.

A static "1" signal is produced on this line when information is present in the output register of the external equipment which the computer may sample. The external equipment drops this signal when the input data resume signal is received from the computer.

Input Data Resume

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line by the computer when it accepts the input word. When an input data resume signal is received from the computer, the input data ready signal is terminated in the external equipment. Dropping the input data ready signal from the external equipment turns off the input data resume signal at the computer.

Output Data Ready**

Originates in computer; terminates in external equipment.

A static "1" signal on this line accompanies each word of output information. This signal is turned off by the output data resume signal from the external equipment.

Output Data Resume**

Originates in external equipment; terminates in computer.

A static "1" signal on this line indicates that the external equipment has accepted the word of information and will turn off the output data ready signal at the computer; this causes the external equipment to drop the output data resume.

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*Buffer channel Input Data Ready/Resume signals are designated Input Transfer Ready/Resume on Transfer Channel.

**Buffer channel Output Data Ready/Resume signals are designated Output Transfer Ready/Resume on Transfer Channel.

Input Buffer Active*

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever the input buffer channel of the cable group is activated. The signal remains on until the final word of the block is entered in computer storage and resynchronization of the input data ready occurs.

Output Buffer Active**

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever the output buffer channel of the cable group is activated. This signal remains on until the final word of the block is buffered to the external equipment and the output data resume signal is resynchronized by the computer.

External Master Clear

Originates in computer; terminates in external equipment.

A static "1" signal appears on this line whenever the clear switch at the 1604 console is moved to up position. This signal clears the control functions of all external equipment attached to the cable group.

Interrupt

Originates in external equipment; terminates in computer.

A static "1" signal is produced on this line whenever the external equipment has assumed an interrupt condition previously selected by the computer. When the signal appears, the computer interrupts the main program and enters a special subroutine which determines the cause of the interruption, takes appropriate action, and returns to the main program. The interrupt line must remain energized until the computer removes the interrupt selection or the interrupt condition by: (1) a new EXF select, (2) an EXF select channel X clear (74.0X0000) or (3) a master clear.

---

*Not used on Transfer Channel

**Buffer channel Output Buffer Active signal is designated Output Transfer Active on Transfer Channel.

Input Function Ready*

Originates in computer; terminates in external equipment.
A static "1" signal is produced on this line when an external function code is present on the external function lines for translation by the external equipment. A signal on this line selects input conditions within the external equipments. This signal is automatically dropped after 6 microseconds.

Input Sense Ready*

Originates in computer; terminates in external equipment.
A static "1" signal is produced on this line whenever the computer is ready to sense the existence of an input condition within the external equipment. The signal is automatically dropped after 6 microseconds.

Output Function Ready

Originates in computer; terminates in external equipment.
A static "1" signal is produced on this line whenever an external function code is present on the external function lines for translation by the external equipment. This line selects output conditions within the external equipment. This signal is automatically dropped after 6 microseconds.

Output Sense Ready

Originates in computer; terminates in external equipment.
A static "1" signal is produced whenever an external function code is present on the line to sense the existence of an output condition within the external equipment. This signal is automatically dropped after 6 microseconds.

Sense Response

Originates in external equipment; terminates in computer.
A static "1" signal on this line indicates to the computer the presence of the condition specified by the upper 11 bits of the 12-bit code sent to external equipment on external function lines. The sense response line is sampled by the computer at the end of the input-output sense ready signal (the computer interprets the inverse of the sense response received from the external equipment when it sends a code with a "1" in the low order bit position to the external equipment).

*Not used on Transfer Channel

External Function Lines

These lines originate in the computer and must be continuously monitored by the external equipment. Only the presence of the proper function or sense ready signal enables the sampling of these lines by the external equipment as an external function code.

TABLE 1. CABLE IDENTIFICATION

Cable Group One	A/7J2* Ch. 1	Cable Group Three	A/7M2 Ch. 5
	B/7K1 Ch. 1		B/7N1 Ch. 5
	C/7K2 Ch. 1		C/7N2 Ch. 5
	D/8J2 Ch. 2		D/8M2 Ch. 6
	E/8K1 Ch. 2		E/8N1 Ch. 6
	F/8K2 Ch. 2		F/8N2 Ch. 6
Cable Group Two	A/7L1 Ch. 3	Cable Group Four	A/7O1 Ch. 7
	B/7L2 Ch. 3		B/7O2 Ch. 7
	C/7M1 Ch. 3		C/7P1 Ch. 7
	D/8L1 Ch. 4		D/8O1 Ch. 7
	E/8L2 Ch. 4		E/8O2 Ch. 7
	F/8M1 Ch. 4		F/8P1 Ch. 7

Group 1
- channel 1 - buffer input
- channel 2 - buffer output

Group 2
- channel 3 - buffer input
- channel 4 - buffer output

Group 3
- channel 5 - buffer input
- channel 6 - buffer output

Group 4
- channel 7 - transfer input and output

* Cable tag identifies connection point in computer. For example, A/7J2 indicates cable A of group one connects to chassis 10700 at location J2.

CABLING

External equipment is connected to the 1604 computer system by communication cables and power cables.

COMMUNICATION

Communication cables are supplied by Control Data Corporation. An equipment may be tied directly to the computer via one of four cable groups which terminate in the computer, or may be indirectly connected to the computer via jumper receptacles (figure 6) provided for this purpose on each of the cabinets in a computer system. The jumper receptacles are duplicates of those which connect the cable groups to the computer. Each group contains 6 cables. Table 1 identifies the cable groups.

External equipment to be tied into the computer system without intermediary devices must be equipped with 12 cable receptacles placed so that cables will enter from beneath the floor. Side entry is not used in the 1604 system. Connector pin assignments are listed in table 2.

General specifications for communication cables:

Length - 50 feet maximum (total for all equipment on one channel).

Connectors - Cable: Amphenol 67-06P-18-24P (or equivalent) each end of cable.
Chassis: Amphenol 67-02E-18-24S (or equivalent).

Conductors - 48 conductors (24 twisted pairs). Conductors are #24 stranded. All plug connections are covered by 3/4 inch #14 clear vinyl tubing.

Grounding - Pin b carries signal ground. One wire of each twisted pair is connected to this ground at each end of the cable through a ground ring of #20 solid wire. The d-c resistance of the cable ground does not exceed 0.5 ohm.

Poting - Plug connections are potted per Control Data Specification #1100.

POWER

Power for the 1604 computer system is derived from a 208 vac, 60 cps, 4 wire primary service. This service is converted to regulated 208 vac, 400 cps, 4 wire service by a motor generator set. The 400 cps and 60 cps power are routed to separate circuit breaker panels at the computer installation and cabled from there to all equipment. Each equipment has separate 400 cps and 60 cps circuit breakers as required.

TABLE 1. CABLE IDENTIFICATION

Cable Group One	A/7J2* Ch. 1	Cable Group Three	A/7M2 Ch. 5
	B/7K1 Ch. 1		B/7N1 Ch. 5
	C/7K2 Ch. 1		C/7N2 Ch. 5
	D/8J2 Ch. 2		D/8M2 Ch. 6
	E/8K1 Ch. 2		E/8N1 Ch. 6
	F/8K2 Ch. 2		F/8N2 Ch. 6
Cable Group Two	A/7L1 Ch. 3	Cable Group Four	A/7O1 Ch. 7
	B/7L2 Ch. 3		B/7O2 Ch. 7
	C/7M1 Ch. 3		C/7P1 Ch. 7
	D/8L1 Ch. 4		D/8O1 Ch. 7
	E/8L2 Ch. 4		E/8O2 Ch. 7
	F/8M1 Ch. 4		F/8P1 Ch. 7

Group 1
- channel 1 - buffer input
- channel 2 - buffer output

Group 2
- channel 3 - buffer input
- channel 4 - buffer output

Group 3
- channel 5 - buffer input
- channel 6 - buffer output

Group 4
- channel 7 - transfer input and output

* Cable tag identifies connection point in computer. For example, A/7J2 indicates cable A of group one connects to chassis 10700 at location J2.

CABLING

External equipment is connected to the 1604 computer system by communication cables and power cables.

COMMUNICATION

Communication cables are supplied by Control Data Corporation. An equipment may be tied directly to the computer via one of four cable groups which terminate in the computer, or may be indirectly connected to the computer via jumper receptacles (figure 6) provided for this purpose on each of the cabinets in a computer system. The jumper receptacles are duplicates of those which connect the cable groups to the computer. Each group contains 6 cables. Table 1 identifies the cable groups.

External equipment to be tied into the computer system without intermediary devices must be equipped with 12 cable receptacles placed so that cables will enter from beneath the floor. Side entry is not used in the 1604 system. Connector pin assignments are listed in table 2.

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Conductors - 48 conductors (24 twisted pairs). Conductors are #24 stranded. All plug connections are covered by 3/4 inch #14 clear vinyl tubing.

Grounding - Pin b carries signal ground. One wire of each twisted pair is connected to this ground at each end of the cable through a ground ring of #20 solid wire. The d-c resistance of the cable ground does not exceed 0.5 ohm.

Poting - Plug connections are potted per Control Data Specification #1100.

POWER

Power for the 1604 computer system is derived from a 208 vac, 60 cps, 4 wire primary service. This service is converted to regulated 208 vac, 400 cps, 4 wire service by a motor generator set. The 400 cps and 60 cps power are routed to separate circuit breaker panels at the computer installation and cabled from there to all equipment. Each equipment has separate 400 cps and 60 cps circuit breakers as required.

TABLE 2. PIN ASSIGNMENTS, COMMUNICATION CABLES

Wire Color (NEMA)	Pin No.	Input Buffer or Transfer Channel			Output Buffer or Transfer Channel		
		Cable A	Cable B	Cable C	Cable D	Cable E	Cable F
0	A	bit 47	bit 24	bit 01	bit 00	bit 23	bit 46
2	B	46	23	00	01	24	47
4	C	45	22	Input Data Ready [3]	02	25	Output Data Ready [3]
5	D	44	21	Input Data Resume [3]	03	26	Output Data Resume [3]
6	E	43	20	Input Buffer Active [1]	04	27	Interrupt
90	F	42	19	External Master Clear	05	28	Input Function Ready [1]
91	H	41	18	NU	06	29	Input Sense Ready [1]
92	J	40	17	NU	07	30	Output Function Ready
93	K	39	16	NU	08	31	Output Sense Ready
94	L	38	15	NU	09	32	Sense Response
95	M	37	14	NU	10	33	Output Buffer Active [2]
96	N	36	13	NU	11	34	Function Bit 00
97	P	35	12	NU	12	35	01
98	R	34	11	NU	13	36	02
900	S	33	10	NU	14	37	03
910	T	32	09	NU	15	38	04
920	U	31	08	NU	16	39	05
930	V	30	07	NU	17	40	06
940	W	29	06	NU	18	41	07
950	X	28	05	NU	19	42	08
960	Y	27	04	NU	20	43	09
970	Z	26	03	NU	21	44	10
980	a	25	02	NU	22	45	11
990	b	gnd	gnd	gnd	gnd	gnd	gnd

1. Buffer cable only, unused in transfer. 2. Output Buffer Active signal designated Output Transfer Active in Transfer Channel.
3. Input/Output Data Ready/Resume signals designated Input/Output Transfer Ready/Resume in Transfer Channel

Power cables are supplied by the manufacturer of the external equipment. Separate 400 cps and 60 cps cables carry power from the circuit breaker panels to the external equipment. Cables are wired directly to the circuit breakers and no connector is required. Cables may be permanently wired to the equipment or equipped with connectors.

Table 3 lists pin assignments for the two power cables. The 400 cps cable carries a ground that is common to all equipment in the computer system and each cable carries an interlock wire. In each equipment, the interlock wires are connected (as required) across a termperature sensing device which reacts to an overheat condition, and/or a door interlock circuit. Each circuit must provide continuity to the two wires for overheat or open-door condition. The 1604 computer normally senses a short on the two wires. An audible alarm is sounded if the line opens during operation; the 400 cps power to the entire system is dropped after three minutes if the condition causing the alarm is not corrected. Temperature sensing devices should be normally closed and automatic.

General specifications for power cables:

Length - 100 feet maximum (dictated by installation).
Connectors - (as required, 5-pin).
60 cps - Cable: Amphenol MS3106B18-11SX (or equivalent).
Chassis: Amphenol MS3102A18-11PX (or equivalent).
400 cps - Cable: Amphenol MS3106B18-11S (or equivalent).
Chassis: Amphenol MS3102A18-11P (or equivalent).
Conductors - 5 stranded (wire size related to current requirements of equipment) encased in Neoprene jacket. Cable rated at 600 volts. (Bronco 66, Type SO or equivalent).

TABLE 3. PIN ASSIGNMENTS, POWER CABLES

60 cps			400 cps		
Wire Color	Pin No.	Signal	Wire Color	Pin No.	Signal
Black	A	60 cps, ϕA	Black	A	400 cps, ϕA
Red	B	60 cps, ϕB	Red	B	400 cps, ϕB
Orange	C	60 cps, ϕC	Orange	C	400 cps, ϕC
White	D	60 cps, Neutral	Green	D	Equipment Ground
Green	E	Interlock B	White	E	Interlock A

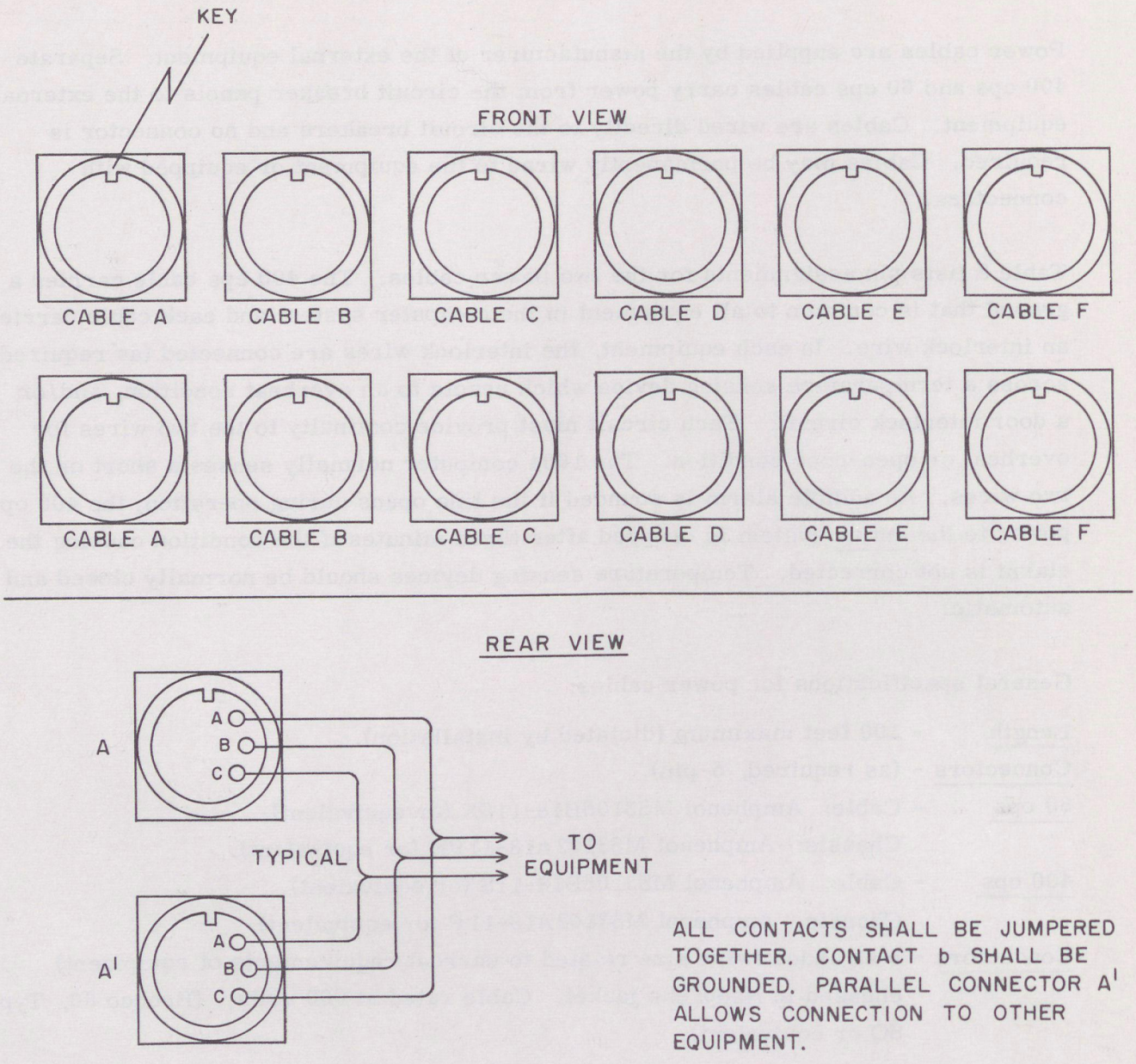

Figure 6. Typical Logic Cable Connector Panel

APPENDIX A

COMMUNICATION CIRCUITS

SIGNAL LEVELS AND TOLERANCES

In communicating with external devices the computer signals undergo a level change to minimize effects of cable impedance. The computer signals are referred to as logic levels, the cable signals as line levels. The binary representation for the two levels are:

Logic	"1"	-3.0v (+0.25v)
	"0"	-0.5v (+0.25v)
Line	"1"	-0.5v (+0.25v)*
	"0"	-16v (+2.5v)

Both line and logic levels are encountered in the input and output amplifier cards. All external equipment control signals are resynchronized upon entering the computer.

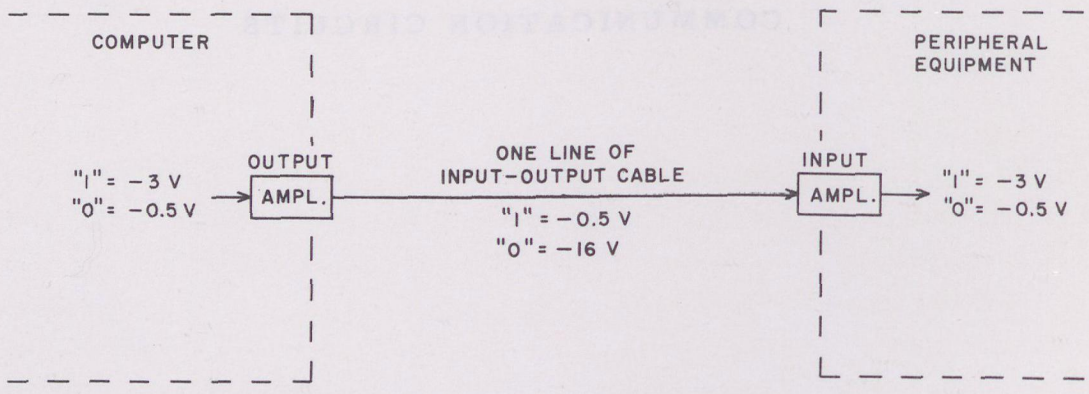

Figure 7. Typical Application

NOTES:

1. Total Line Capacitance, 0.002 uf max.
2. DC Resistance of Ground Return, 0.5 ohm max.
3. Input and Output amplifiers each perform a 180^{o} electrical phase shift; however, they do not invert logic signals.

* Tolerances given are for Control Data equipment. When other equipment is connected to Control Data computers, the following variation may be tolerated on the "1" line level: +0.5v, -2.5v

INPUT AMPLIFIER

The input amplifier (figure 8) converts inputs received from the signal line to outputs suitable for use by logic circuits. A-0.5v "1" is converted to a -3v "1", and a -16v "0" is converted to a -0.5v "0". Forward drive current is provided by the -20v supply through resistor R01. If the input pin is left open, the transistors are driven to the conduction state, producing a -0.5v "0" output. If the input is grounded, the output is held at -3.0v "1".

Approximately 10 ma of current is required at the input in order to prevent the transistors from switching to the conduction state. This requirement may be satisfied by providing a low-impedance path from the input tpin to ground. In this condition, the forward drive current which would otherwise be drawn through transistor Q01 is supplied externally through the input pin. The transistors remain in a state of minimum conduction producing a circuit output of -3.0v "1"; however, they are held out of cutoff by the feedback connection through diode CR01.

If the circuit input is opened or allowed to "float", current flow will increase through the biasing network of resistors R01, R02, R06, R07, and R08. However, the voltage across R07 is clamped by the sum of the base-emitter junction drops of Q01 and Q02, which is approximately 0.6v. Thus, as the input goes negative, the voltage drop across R07 is clamped at approximately 20.6v so that current through it does not increase beyond about 0.9ma. Therefore as the input becomes more negative, forward drive current is drawn through transistors Q01 and Q02, causing them to switch to a state of high conduction. The circuit output becomes -0.5v "0"; however the transistors are held out of deep saturation by diode CR04.

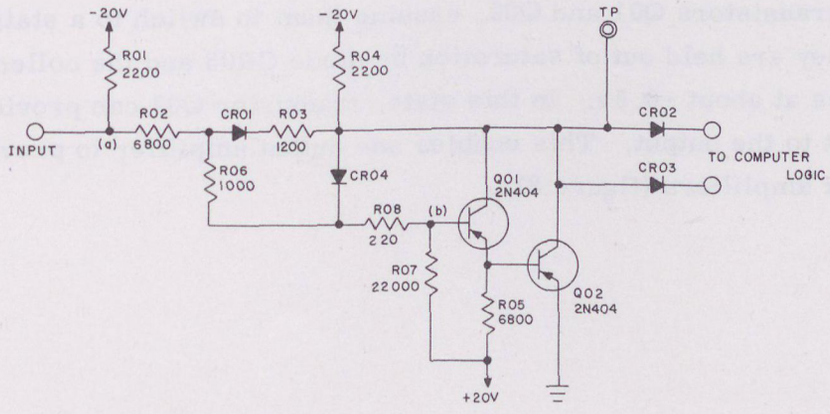

Figure 8. Input Amplifier Circuit

OUTPUT AMPLIFIER

The output amplifier (figure 9) converts logic-level inputs to outputs suitable for transmission over an input-output cable. A -3v "1" is converted to a -0.5v "1", and a -0.5v "0" is converted to a -16v "0". Each input acts as a single-way AND, with forward drive current provided by the -20v source through resistor R01. An open input allows the transistors to be driven to the conduction state, producing a -0.5v "1" output. If all inputs are grounded, the output is held at a -16v "0".

The output amplifier operates as an electronic switch, so that its output is either essentially grounded or floating. The circuit will drive five standard input amplifiers of the type shown in figure 14. Transition time of the signal waveform from the output amplifier circuit is 2 usec minimum, 4 usec maximum. Voltage level rise and fall rates are 8 volts per usec.

A positive-going input causes transistors Q01 and Q02 to switch to a state of minimum conduction. When the input reaches -0.5v "0", the base of Q01 will be about +0.8v. This results in approximately +0.5v on the base of Q02, so that it is well into the cutoff region. In this state, the circuit output is approximately "floating" and rises toward -20v; however the drop across R07 and the input impedance of the driven load limit the output to about -16v.

As the circuit input goes negative, conduction increases through the AND resistor R01 and diode CR01, and the biasing network of resistors R03, R05, and R06. The voltage across R05 is clamped by the base-emitter junction drops of Q01 and Q02, which is clamped at approximately 20.6v so that current through it does not increase beyond 0.9ma. Therefore as the input becomes more negative, forward drive current is drawn through transistors Q01 and Q02, causing them to switch to a state of heavy conduction. They are held out of saturation by diode CR03 and the collector voltage of Q02 stabilizes at about -0.5v. In this state, transistor Q02 can provide 50ma of positive current to the output. This enables one output amplifier to provide a -0.5v "1" input for 5 input amplifiers (figure 8).

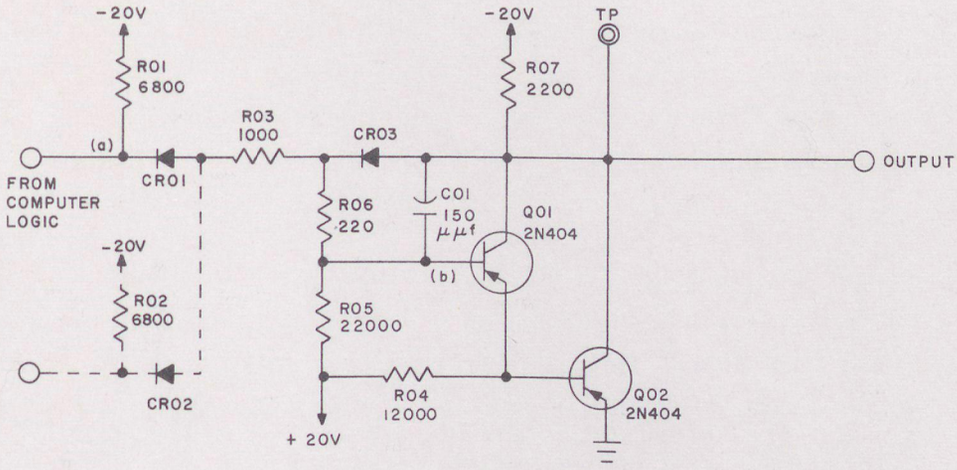

Figure 9. Output Amplifier Circuit

APPENDIX B

AUXILIARY SCANNER

AUXILIARY SCANNER

The auxiliary scanner which controls the input-output buffer interrogates the six buffer channels, the interrupt line, and the real-time clock for action requests.* Under no-request conditions, each is interrogated once every 3.2 microseconds. The order of scan is: real-time clock, channel 1, channel 3, channel 2, channel 6, interrupt, channel 5, channel 4. This sequence runs simultaneously with the main computer program and does not interfere with it. When an action request occurs, execution of the next instruction in the main program is temporarily witheld to permit the exchange of the input-output data word. After completion of the exchange the main program continues.

Action requests from the eight sources may momentarily block execution of main-program instructions. Once the scanner recognizes an action request and input-output action is initiated, a request for action in any of the four successive positions of the scanner will be honored before the main program will be permitted to continue. The one exception is an interrupt request; control is always returned to the main program for at least one instruction. (This is a jump instruction in the lower half of address 00007.) If the real-time clock initiates the request for action and stops the scanner, any of the next seven successive requests occurring in the action interval will be honored before control is returned to the main program.

The main computer program can be locked out indefinitely under one unusual circumstance. This occurs when communication is on but two channels occupying opposite positions on the scanner (3 and 5, 2 and 4) and transmitting information at 37.5 kc rate. This rate is sufficient to show an action request every half-scan of the scanner.

The slowest maximum transmission rate per channel, 5 kc, assumes requests on all six channels, a rise and fall time of 9 microseconds for the ready and resume lines, and a divide instruction when the scanner requests the storage section.

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* For detailed information on the scanner and other control portions of the computer, refer to the 1604 Instruction Book.

The fastest rate of transmission occurs with only one channel activated and instructions occurring in the computer of 5 usec average duration. An average word rate of 52 kc can be obtained, although successive data ready signals can be sent at intervals of 15.4 usec.

In table 4, peak loads are based on main computer programming of divide instructions at the critical time, an interrupt request, and a real-time clock request. Minimum loads are based on main computer programming of 5 usec duration instructions, no interrupt, no clock request.

TABLE 4. MAXIMUM WORD RATES ALL CHANNELS

Number of Channels Used	Peak Load	Time in usec	Minimum Load	Time in usec
1	11 kc	91	52 kc	19
2	8 kc	125	37.5 kc	26
3	7 kc	143	24.5 kc	41
4	6.3 kc	158	18.1 kc	55
5	5.6 kc	178	14.3 kc	70
6	5 kc	200	11.9 kc	84

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