CONTROL DATA
1604-A COMPUTER

INPUT/OUTPUT SPECIFICATIONS

1604-A COMPUTER

Input/Output Specifications

1. The following pages of this publication contain errors and should be corrected as indicated:

Page 7 -- Change time intervals D and G to:

D - Minimum time 7.4 μsec, maximum time 50.8 μsec

G - Minimum time 1.4 μsec, maximum time 2.8 μsec

Page 9 -- Change time interval B and E to:

B - Minimum time 5.8 μsec, maximum time 49.2 μsec

E - Minimum time 1.4 μsec, maximum time 2.8 μsec

2. Page B-1 of this publication has been revised and supersedes the original page B-1.

3. This change should be recorded on the change sheet near the front of the publication.

APPENDIX B
BUFFER CONTROL

After a buffer operation is initiated by the main program, the actual word-at-a-time transfer of data is regulated by buffer control.

The heart of buffer control is the auxiliary scanner which ensures that no one buffer channel can monopolize the I/O section. The scanner probes the six buffer channels in search of action requests.* The order in which the channels are scanned is 1-3-2-6-4-5. When an action request is detected, the scanner stops and initiates a buffer operation. After one word is transferred, the scanner probes all other channels before returning to transfer the second word. Up to six buffer channels may be active at the same time, each taking its turn at transferring a word.

Although program operations may continue while buffer operations take place, program and I/O operations must time-share storage. Buffer operations have priority.

Table B-1 shows maximum word rates for any number of buffer channels in use at one time. These are maximum possible word rates; the actual word rates are determined by the speed of external equipment. The "worst condition" rate assumes that the program is able to make one storage reference for each cycle of the scanner. For only one channel active one program storage reference may be made between each word buffered. When two or more channels are active they may monopolize storage time and prevent the program from referencing storage until the buffering is completed.

Most I/O equipment is slower than the times shown in table B-1 and actual speed of buffer operations is governed by the external equipment. Therefore, except when magnetic tape units are used, there is little conflict for storage time.

TABLE B-1. MAXIMUM WORD RATES

Number of Channels Active	Best Conditions	Worst Conditions
1	1 word/7.4 μsec	1 word/13.8 μsec
2	1 word/14.8 μsec (each chnl.)	1 word/21.2 μsec (each chnl.)
3	1 word/22.2 μsec (each chnl.)	1 word/28.6 μsec (each chnl.)
4	1 word/29.6 μsec (each chnl.)	1 word/36.0 μsec (each chnl.)
5	1 word/37.0 μsec (each chnl.)	1 word/43.4 μsec (each chnl.)
6	1 word/44.4 μsec (each chnl.)	1 word/50.8 μsec (each chnl.)

*An action request indicates that the program has asked for a buffer operation and that the external equipment is ready to transfer a word.

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RECORD OF CHANGE NOTICES				
C. N. NO.	DATE ORIGINATED	DATE ENTERED	INITIALS	REMARKS

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Figure 1.   Typical 1604-A System

This specification contains information necessary to attach external equipment to the CONTROL DATA* 1604-A computer either directly or indirectly (through such devices as the 1615 magnetic tape adapter, 1608 control unit or 1610 card control unit). A typical 1604-A system is shown in figure 1.

1604-A INPUT/OUTPUT SECTION

The 1604-A computer communicates with external equipment via six buffer channels and a single transfer channel. The buffer channels provide for the normal exchange of data with several equipments concurrently. Exchange of data on buffer channels is program initiated but is carried out independently by the buffer control section. The transfer channel provides for very high speed exchange of data under direct program control.

BUFFER

Buffer operation is initiated by the main computer program and continues at a rate determined by the external equipment (see appendix B). The 1604-A can perform buffer operations with three input devices and three output devices concurrently. Each device determines the rate of its own data transmission and provides its own means of internal control. Buffer operations are started by the External Function (EXF 74) instruction.

Input buffer channels are numbered 1, 3 and 5; output buffer channels are 2, 4 and 6. Within the I/O section of the computer (figure 2) the three input buffer channels connect to the I^0 register which transmits the data to the storage section. Each output channel is associated with a specific register. Data is held on the line until the external equipment has received and acknowledged receipt of the information. Each external equipment has an output register for sending information to one of the computer input channels.

The 1604-A storage section is connected to both the arithmetic section and the I/O section, but it can be used by only one at a time. The buffer and main program must time share the storage section of the computer.

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* Registered trademark of Control Data Corporation

1

CHANNEL 2
BUFFERED OUTPUT
(CONSOLE)

O^1
48-BIT BUFFERED
OUTPUT
REGISTER

CHANNEL 6
BUFFERED OUTPUT

O^3
48-BIT BUFFERED
OUTPUT
REGISTER

CHANNEL 4
BUFFERED OUTPUT

O^2
48-BIT BUFFERED
OUTPUT
REGISTER

CHANNEL 7
TRANSFER OUTPUT

O^4
48-BIT OUTPUT
TRANSFER
REGISTER

CHANNEL
SELECTION

EQUIPMENT
CODE

FUNCTION
CODE

O^0
EXTERNAL FUNCTION
INVERTERS

I^1

STORAGE

X REGISTER

CHANNEL 7
TRANSFER INPUT

I^0

CHANNEL 1
BUFFER INPUT
(CONSOLE)

CHANNEL 5
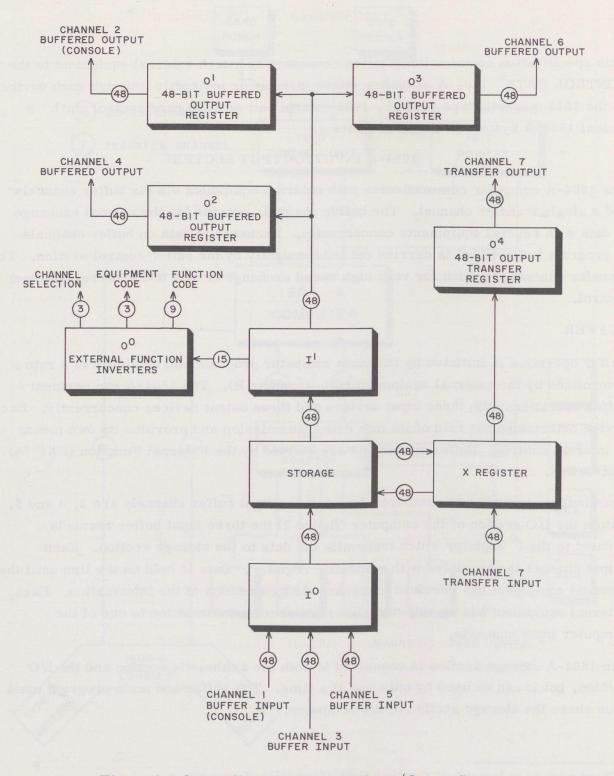BUFFER INPUT

CHANNEL 3
BUFFER INPUT

Figure 2. Over-all Logic Diagram Input/Output Section

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Buffer channels are grouped for connecting to external equipment as follows:

Channel 1 - Buffer input
2 - Buffer output

3 - Buffer input
4 - Buffer output

5 - Buffer input
6 - Buffer output

TRANSFER

The transfer mode of communication is initiated by the program and program operations stop while the transfer takes place. A block of words is transmitted one word at a time and the next program instruction is executed only after the last word of the block has been transmitted. (Buffer mode can occur concurrently with a transfer instruction if the buffer is initiated before the transfer instruction.) Input transfer of a block of information is performed by instruction 62, output transfer by instruction 63.

The maximum transfer rate is approximately one word every 5 μsec. The transfer channel, consisting of input lines and output lines, connects to the X register.

COMMUNICATION SIGNALS

Communication with external equipment is established with function signals and data signals. Function signals select an external equipment and direct it to perform some operation. Data signals carry the information to be exchanged. All function and data signals on the input and output lines are voltage levels representing a binary "1" or "0". Pulse representation is used internally in the computer but not on the input/output lines.
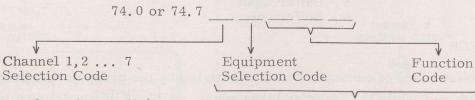
FUNCTION SIGNALS

The number of equipments with which the 1604-A can communicate is limited by electrical considerations rather than by the number of I/O channels available. Several equipments can be linked to the computer on the same I/O channel by connecting jumper cables from one external equipment to another. Each equipment is assigned an equipment selection code which it recognizes as a request for action. The codes are in the low-order 12 bits of the EXF instruction.

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EXF 74.0 ----- Selects an external equipment and places it in
a mode of operation.

EXF 74.7 ----- Senses conditions such as ready or error in an
external equipment.

The five octal digits of the base execution address are interpreted as shown below:

74.0 or 74.7 ___ ___ ___ ___ ___

Channel 1, 2 ... 7   Equipment   Function
Selection Code   Selection Code   Code

(1604-A translates internally)   To equipment on channel designated

The four low-order octal digits are sent on all function channels (buffer and transfer).
The 1604-A buffer control translates the channel selection digit and sends one of the
following control signals to all equipments on the designated channel to allow each to
sample the code.

Select   Sense

Input Function Ready   Input Sense Ready

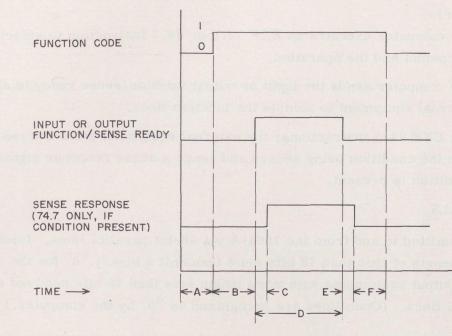Output Function Ready   Output Sense Ready

The selected equipment does not send a resume to the computer after an EXF select
(74.0) instruction.

For EXF sense (74.7) instructions, the external equipment returns a sense response
signal to the computer if the sensed condition is present.

Control circuits of all external equipments on channel X are cleared by an EXF
74.0X0000 (channel clear) code.

All external equipments must adequately resynchronize all control signals (signals
other than data).

The control signal sequence for select and sense operations is shown in figure 3.

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FUNCTION CODE

INPUT OR OUTPUT
FUNCTION/SENSE READY

SENSE RESPONSE
(74.7 ONLY, IF
CONDITION PRESENT)

TIME →

Time A - Time before EXF 74.0 (Select) or 74.7 (Sense) instruction

   B - Minimum time 1.4 μsec, maximum time 3.0 μsec

   C - Determined by external equipment

   D - 12.8 μsec

   E - Determined by external equipment

   F - Varies with computer instruction sequence

Figure 3.   Function or Sense Ready Timing Diagram

The sequence is:

1) The computer executes an EXF 74. 0 or 74. 7 instruction to select an external equipment and the operation.

2) The computer sends the input or output function/sense ready to allow the external equipment to sample the function lines.

3) For EXF 74. 7 instructions, the external equipment gates the ready signal with the condition being sensed and sends a sense response signal if the condition is present.

DATA SIGNALS

Data is transmitted to and from the 1604-A via 48-bit parallel lines. Input equipment with a word length of less than 48 bits must transmit a binary "0" for the unused high-order bits. Output equipments with word length less than 48 bits need not sense the unused signal lines. (Open lines are recognized as "0" by the computer.)

Ready and resume control signals accompany data transmissions. Information sent from external equipment to the computer is associated with input data ready and resume signals; information sent from computer to external equipment is associated with output data ready and resume signals. A ready indicates that data is waiting to be sampled. A resume replies to the data sending device that data has been received and should be removed from the line.
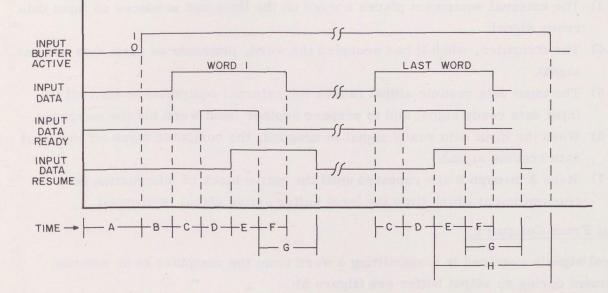
Labeling of input and output registers is referred to the pertinent external equipment. For example, data originating in the paper tape reader passes through the reader's output register and is sent to the computer's input register along with an input data ready. Upon receipt of the input data ready the computer stores the information and sends out an input data resume.

Input to Computer

Control signals required in transmitting a word from an external equipment to the computer during an input buffer are as follows (figure 4):

1) The computer, by the correct combination of external select codes, establishes the external equipment from which it is to take information.

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INPUT
BUFFER
ACTIVE

WORD 1   LAST WORD

INPUT
DATA

INPUT
DATA
READY

INPUT
DATA
RESUME

TIME → ├─ A ─┤─ B ─┤─ C ─┤─ D ─┤─ E ─┤─ F ─┤   ├─ C ─┤─ D ─┤─ E ─┤─ F ─┤
                                            └─ G ─┤   └─ G ─┤
                                                                                    └─ H ─┤

Time A - Time before input channel is active

B - Determined by input equipment

C - Determined by input equipment (input data and input
     data ready signals may be turned on at same time)

D - Minimum time 8.4 μsec, maximum time 44.2 μsec

E - Determined by input equipment

F - Determined by input equipment (input data and input
     data ready signals may be turned off at same time)

G - Minimum time 0.4 μsec, maximum time 1.8 μsec
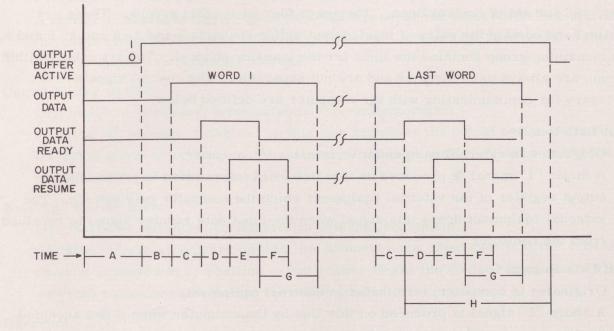
H - Determined by input equipment

Figure 4. Input Data Ready/Resume Timing Diagram

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2) The computer activates the input buffer active line to signal readiness to start data transfer.   This line remains up until the final word of the block is transmitted.

3) The external equipment places a word on the lines and produces an input data ready signal.

4) The computer, when it has accepted the word, produces an input data resume signal.

5) The input data resume signal causes the external equipment to turn off the input data ready signal and to prepare another input word for the computer.

6) When the input data ready signal is dropped, the computer turns off the input data resume signal.

7) Steps 3 through 6 are repeated until the entire block of information is transmitted at which time the input buffer active signal is dropped.

Output From Computer

Control signals required in transmitting a word from the computer to an external equipment during an output buffer are (figure 5):

1) The computer, through the correct combination of external select and sense codes, establishes the equipment to which information is to be sent.

2) The computer activates the output buffer active line to indicate readiness to start data transfer.   This line remains on until the final word of the block is transmitted.

3) The computer places a word in the associated output register.   This energizes all data lines in parallel.

4) When all data lines are stable, the computer generates an output data ready signal which indicates to the external equipment that data is available on the lines in a stable steady-state form.

5) The external equipment accepts the information at its own rate and then sends an output data resume to the computer.

6) The computer accepts the output data resume signal and turns off the output data ready signal.

7) When the output data ready signal is dropped by the computer, the output data resume signal is terminated within the external equipment.

8) Steps 3 through 7 are repeated until the entire block of information is transmitted, at which time the output buffer active signal is dropped.

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Time A - Time before output channel is active

     B - Minimum time 5.8 μsec, maximum time 41.8 μsec

     C - 1.0 μsec

     D - Determined by output equipment

     E - Minimum time 0.4 μsec, maximum time 1.8 μsec

     F - Determined by output equipment

     G - Varies with computer instruction sequence

     H - Determined by output equipment

Figure 5. Output Data Ready/Resume Timing Diagram

SUMMARY LISTING

Each cable group contains one input channel, one output channel, one set of function lines, and one set of control lines. There are four such cable groups. Three are identical and contain the pairs of input/output buffer channels 1 and 2, 3 and 4, 5 and 6. The remaining group contains the lines for the transfer channel. The six cables within a group are always used together and are not separable. The control signals necessary for communicating with the computer are defined below.

Input Data Ready*

Originates in external equipment; terminates in computer.

A static "1" signal is produced on this line when information is present in the output register of the external equipment which the computer may sample. The external equipment drops this signal when the input data resume signal is received from the computer.

Input Data Resume*

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line by the computer when it has accepted the input word. When an input data resume signal is received from the computer, the input data ready signal is terminated in the external equipment. Dropping the input data ready signal from the external equipment turns off the input data resume signal at the computer.

Output Data Ready**

Originates in computer; terminates in external equipment.

A static "1" signal on this line accompanies each word of output information. This signal is turned off by the output data resume signal from the external equipment.

Output Data Resume**

Originates in external equipment; terminates in computer.

A static "1" signal on this line indicates that the external equipment has accepted the word of information. This signal turns off the output data ready signal at the computer; this causes the external equipment to drop the output data resume.

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* Input Data Ready/Resume signals are designated Input Transfer Ready/Resume on Transfer Channel.

** Output Data Ready/Resume signals are designated Output Transfer Ready/Resume on Transfer Channel.

Input Buffer Active*

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever the input buffer channel of the cable group is activated. The signal remains on until the final word of the block is entered in computer storage.

Output Buffer Active*

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever the output buffer channel of the cable group is activated. This signal remains on until the final word of the block is buffered to the external equipment.

External Master Clear

Originates in computer; terminates in external equipment.

A static "1" signal appears on this line whenever the clear switch at the 1604-A console is moved to up position. This signal clears the control functions of all external equipment attached to the cable group.

Interrupt

Originates in external equipment; terminates in computer.

A static "1" signal is produced on this line whenever the external equipment has assumed an interrupt condition previously selected by the computer. When the signal appears, the computer interrupts the main program and enters a special subroutine which determines the cause of the interruption, takes appropriate action, and returns to the main program. The interrupt line remains energized until the computer removes the interrupt selection or the interrupt condition by: (1) a new EXF select and (2) EXF select channel X clear (74.0X0000) or (3) a master clear.

Input Function Ready

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line when an external function code is present on the external function lines for translation by the external equipment. This signal is automatically dropped after 12.8 μsec.

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*Input/Output Buffer Active signals are designated Input/Output Transfer Active on Transfer Channel.

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Input Sense Ready

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever the computer is ready to sense the existence of an input condition within the external equipment. The signal is automatically dropped after 12.8 μsec.

Output Function Ready

Originates in computer; terminates in external equipment.

A static "1" signal is produced on this line whenever an external function code is present on the external function lines for translation by the external equipment. This signal is automatically dropped after 12.8 μsec.

Output Sense Ready

Originates in computer; terminates in external equipment.

A static "1" signal is produced whenever an external function code is present on the line to sense the existence of an output condition within the external equipment. This signal is automatically dropped after 12.8 μsec.

Sense Response

Originates in external equipment; terminates in computer.

A static "1" signal on this line indicates to the computer the presence of the condition specified by the upper 11 bits of the 12-bit code sent to external equipment on external function lines. The sense response line is sampled by the computer at the end of the input/output sense ready signal (the computer interprets the inverse of the sense response received from the external equipment when it sends a code with a "1" in the low-order bit position to the external equipment).

External Function Lines

These lines originate in the computer and must be continuously monitored by the external equipment. Only the presence of the proper function or sense ready signal enables the sampling of these lines by the external equipment as an external function code.

CABLING

External equipment is connected to the 1604-A computer system by communication cables and power cables.

COMMUNICATION

Communication cables are supplied by Control Data Corporation. An equipment may be tied directly to the computer via one of four cable groups which terminate in the computer, or may be indirectly connected to the computer via jumper receptacles provided for this purpose on each of the cabinets in a computer system. The jumper receptacles are wired in parallel with those which connect the cable groups to the computer. Each group contains 6 cables. Table 1 identifies the cable groups.

External equipment to be tied into the computer system without intermediary devices must be equipped with cable receptacles placed so that cables will enter from beneath the floor. Side entry is not used in the 1604-A system. Connector pin assignments are listed in table 2.

General specifications for communication cables:

Length — 50 feet maximum (total for all equipment on one channel).

Connectors — Cable: Amphenol 67-06P-18-24P (or equivalent) each end of cable.
Chassis: Amphenol 67-02E-18-24S (or equivalent).

Conductors — 48 conductors (24 twisted pairs). Conductors are #24 stranded. All plug connections are covered by 3/4 inch #14 clear vinyl tubing.

Grounding — Pin b carries signal ground. One wire of each twisted pair is connected to this ground at each end of the cable through a ground ring of #20 solid wire. The d-c resistance of the cable ground does not exceed 0.5 ohm.

Plotting — Plug connections are potted per Control Data Specification #1100.

POWER

Power for the 1604-A computer system is derived from a 208 vac, 60 cps, 4-wire primary service. This service is converted to regulated 208 vac, 400 cps, 4-wire service by a motor generator set. The 400 cps and 60 cps power are routed to separate circuit breaker panels at the computer installation and cabled from there to all equipment. Each equipment has separate 400 cps and 60 cps circuit breakers as required.

TABLE 1.   CABLE IDENTIFICATION

Cable Group One	A/7J2 *	**Cable Group Three**	A/7M2
	Ch. 1-2		Ch. 5-6
	B/7K1		B/7N1
	Ch. 1-2		Ch. 5-6
	C/7K2		C/7N2
	Ch. 1-2		Ch. 5-6
	D/8J2		D/8M2
	Ch. 1-2		Ch. 5-6
	E/8K1		E/8N1
	Ch. 1-2		Ch. 5-6
	F/8K2		F/8N2
	Ch. 1-2		Ch. 5-6
Cable Group Two	A/7L1	**Cable Group Four**	A/7O1
	Ch. 3-4		Ch. 7
	B/7L2		B/7O2
	Ch. 3-4		Ch. 7
	C/7M1		C/7P1
	Ch. 3-4		Ch. 7
	D/8L1		D/8O1
	Ch. 3-4		Ch. 7
	E/8L2		E/8O2
	Ch. 3-4		Ch. 7
	F/8M1		F/8P1
	Ch. 3-4		Ch. 7

Group 1

   channel 1 - buffer input

   channel 2 - buffer output

Group 2

   channel 3 - buffer input

   channel 4 - buffer output

Group 3

   channel 5 - buffer input

   channel 6 - buffer output

Group 4

   channel 7 - transfer input and output

*Cable tag identifies connection point in computer. For example, A/7J2 indicates that cable A of group one connects to chassis 10700 at location J2.

TABLE 2. PIN ASSIGNMENTS, COMMUNICATION CABLES

Wire Color (Nema)	Pin No.	Input Buffer or Transfer Channel			Output Buffer or Transfer Channel		
		Cable A	Cable B	Cable C	Cable D	Cable E	Cable F
0	A	bit 47	bit 24	bit 01	bit 00	bit 23	bit 46
2	B	46	23	00	01	24	47
4	C	45	22	Input Data Ready**	02	25	Output Data Ready**
5	D	44	21	Input Data Resume**	03	26	Output Data Resume**
6	E	43	20	Input Buffer Active*	04	27	Interrupt
90	F	42	19	External Master Clear	05	28	Input Function Ready*
91	H	41	18	Interrupt	06	29	Input Sense Ready*
92	J	40	17	NU	07	30	Output Function Ready
93	K	39	16	NU	08	31	Output Sense Ready
94	L	38	15	NU	09	32	Sense Response
95	M	37	14	NU	10	33	Output Buffer Active
96	N	36	13	NU	11	34	Function Bit 00
97	P	35	12	NU	12	35	01
98	R	34	11	NU	13	36	02
900	S	33	10	NU	14	37	03
910	T	32	09	NU	15	38	04
920	U	31	08	NU	16	39	05
930	V	30	07	NU	17	40	06
940	W	29	06	NU	18	41	07
950	X	28	05	NU	19	42	08
960	Y	27	04	NU	20	43	09
970	Z	26	03	NU	21	44	10
980	a	25	02	NU	22	45	11
990	b	grd	grd	grd	grd	grd	grd

*Buffer cable only, unused in transfer. Input/Output Buffer Active signals designated Input/Output Transfer Active in Transfer Channel.

**Input/Output Data Ready/Resume signals designated Input/Output Transfer Ready/Resume in Transfer Channel.

Power cables are supplied by the manufacturer of the external equipment. Separate 400 cps and 60 cps cables carry power from the circuit breaker panels to the external equipment. Cables are wired directly to the circuit breakers and no connector is required. Cables may be permanently wired to the equipment or equipped with connectors.

Table 3 lists pin assignments for the two power cables. The 400 cps cable carries a ground that is common to all equipment in the computer system and each cable carries an interlock wire. In each equipment, the interlock wires are connected (as required) across a temperature-sensing device which reacts to an overheat condition, and/or a door interlock circuit. Each circuit must provide continuity to the two wires for overheat or open-door condition. The 1604-A computer normally senses a short on the two wires. An audible alarm is sounded if the line opens during operation; the 400 cps power to the entire system is dropped after three minutes if the condition causing the alarm is not corrected. Temperature-sensing devices should be normally-closed and automatic.

General specifications for power cables:

Length	-	100 feet maximum (dictated by installation).
Connectors	-	(as required, 5-pin).
60 cps	-	Cable: Amphenol MS3106B18-11SX (or equivalent).
		Chassis: Amphenol MS3102A18-11PX (or equivalent).
400 cps	-	Cable: Amphenol MS3106B18-11S (or equivalent).
		Chassis: Amphenol MS3102A18-11P (or equivalent).
Conductors	-	5 stranded (wire size related to current requirements of equipment) encased in Neoprene jacket. Cable rated at 600 volts. Bronco 66, Type SO (or equivalent).

TABLE 3. PIN ASSIGNMENTS, POWER CABLES

60 cps			400 cps		
Wire Color	Pin No.	Signal	Wire Color	Pin No.	Signal
Black	A	60 cps, ØA	Black	A	400 cps, ØA
Red	B	60 cps, ØB	Red	B	400 cps, ØB
Orange	C	60 cps, ØC	Orange	C	400 cps, ØC
White	D	60 cps, Neutral	Green	D	Equipment Ground
Green	E	Interlock B	White	E	Interlock A

APPENDIX A
COMMUNICATION CIRCUITS

An output amplifier circuit (L--- card) in the computer converts the low-level internal logic voltages to high-level voltages necessary for transmission by cable to external equipment. An input amplifier circuit (M___ card) converts the high-level cable voltages to the low-level internal logic voltages. Although each circuit produces a 180° phase shift, it does not function as a logical inverter. A logical "1" (-3.0v) input to an L___ card produces a "1" output (-0.5). A "1" input (-0.5) to an M--- card produces a logical "1" output (-3.0v).
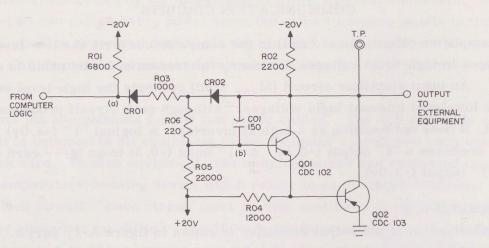
OUTPUT AMPLIFIER

A schematic diagram of the output amplifier is shown in figure A-1, part a. Resistor R01 and the -20v supply hold the input to the circuit (point a) at binary "1" (-3v) when no input signal is applied to the circuit or when no data or control line is tied to the circuit. The collectors of transistors Q01 and Q02 are connected to the base of Q01 through 150 $\mu\mu$f capacitor C01 which integrates the collector signal. Assuming that a binary "1" is supplied to the circuit, Q01 and Q02 turn on placing a low impedance between ground and the output line. The output of the circuit is effectively held to -0.5v. Capacitor C01 tends to oppose the initial conduction of Q01 and Q02 by feeding back a less negative signal than was initially placed on the base. When C01 approaches full charge, Q01 and Q02 approach full conduction and the output rises to -0.5v. Full saturation is prevented by feedback diode CR02. If a binary "0" (-0.5v) is applied to the circuit, the voltage divider action of the circuit causes Q01 and Q02 to turn off. No feedback is applied to prevent cutoff so the output voltage rises toward -20v; the actual voltage is determined by the driven output circuit.

The binary "1" state of the output amplifier circuit is -0.5v (±0.25v)* at the terminals of external equipments or computer under all conditions.
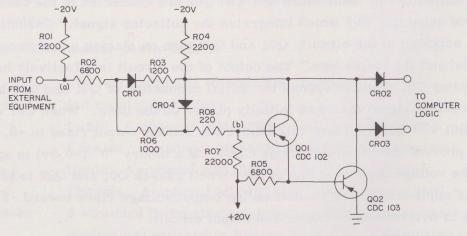
The binary "0" state of the output amplifier is -16v (±2.5v) at the terminals of the external equipments under all conditions.

In the binary "1" or "0" state an output amplifier circuit (whether located in the computer or in an external equipment) need supply no more than 10 ma to any single input amplifier circuit in another equipment.
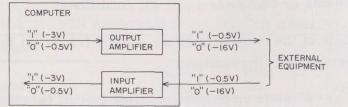
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* Tolerances given are for Control Data equipment. When other equipment is connected to Control Data computers, the following variations may be tolerated for the "1" line level: +0.5v, -2.5v.
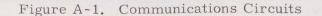
a. OUTPUT AMPLIFIER

b. INPUT AMPLIFIER

c. AMPLIFIER CONVERSIONS

Figure A-1. Communications Circuits

The output amplifier circuit can drive a maximum of five input amplifier circuits (50 ma maximum available current from output amplifier circuit).

Waveform characteristics of the signal from the output amplifier:

    No transition with slope greater than 8v per μsec for a 30 foot cable

    Minimum transition time 2 μsec

    Maximum transition time 4 μsec

The circuit is capable of driving a total wiring capacity which can vary between 0 and 2000 $\mu\mu$f.

INPUT AMPLIFIER

A schematic diagram of the input amplifier circuit used in the computer is given in figure A-1, part b. Resistor R01 and the -20v supply hold the input to the circuit (point a) at binary "0" (-16v) when no input signal is supplied to the circuit or when no data or control line is connected to the circuit. Assuming a binary "1" (-0.5v) input to the circuit, the base of Q01 (point b) rises positive due to the voltage divider action of R02, R06, R07, and R08. The collectors of Q01 and Q02 then move in a negative direction. A feedback network including R03 and CR01 limits the negative potential of the collectors so that a binary "1" (-3v) is presented to the computer logic circuits. Conversely, if a binary "0" (-16v) input is applied to the circuit, the voltage divider action causes the transistors to increase conduction. The feedback network of R08 and CR04 limits conduction so that the output to the computer logic circuits approaches -0.5v or binary "0".

The maximum steady-state current drawn from a line by an input circuit does not exceed 10 ma. The circuit is designed so that if the input wire is disconnected the effect will be as though a binary "0" were present at the input.

The waveshape of the current drawn from a line by an input circuit has a slope which does not exceed 5 ma per μsec.

APPENDIX B
BUFFER CONTROL

After a buffer operation is initiated by the main program, the actual word-at-a-time transfer of data is regulated by buffer control.

The heart of buffer control is the auxiliary scanner which ensures that no one buffer channel can monopolize the I/O section. The scanner probes the six buffer channels in search of action requests.* The order in which the channels are scanned is 1-3-2-6-4-5. When an action request is detected, the scanner stops and initiates a buffer operation. After one word is transferred, the scanner probes all other channels before returning to transfer the second word. Up to six buffer channels may be active at the same time, each taking its turn at transferring a word.

Although program operations may continue while buffer operations take place, program and I/O operations must time-share storage. Buffer operations have priority.

Table B-1 shows maximum word rates for any number of buffer channels in use at one time. These are maximum possible word rates; the actual word rates are determined by speed of external equipment. The "worst condition" rate for one channel active assumes that the main program makes a storage reference between each word buffered. No worst condition times are listed for more than one channel active since it is possible for two or more buffer channels to monopolize storage time.

The speed of most I/O equipment is lower than those shown in table B-1 and actual speed of buffer operations is governed by the external equipment. Therefore, except when magnetic tape units are used, there is little conflict for storage time.

TABLE B-1. MAXIMUM WORD RATES

Number of Channels Active	Best Conditions	Worst Conditions
1	116 KC	68.5 KC
2	67.5 KC	
3	45 KC	
4	33.8 KC	
5	2.7 KC	
6	22.5 KC	

*An action request indicates that the program has asked for a buffer operation and that the external equipment is ready to transfer a word.

CONTROL DATA

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