CONTROL DATA
169
AUXILIARY MEMORY UNIT

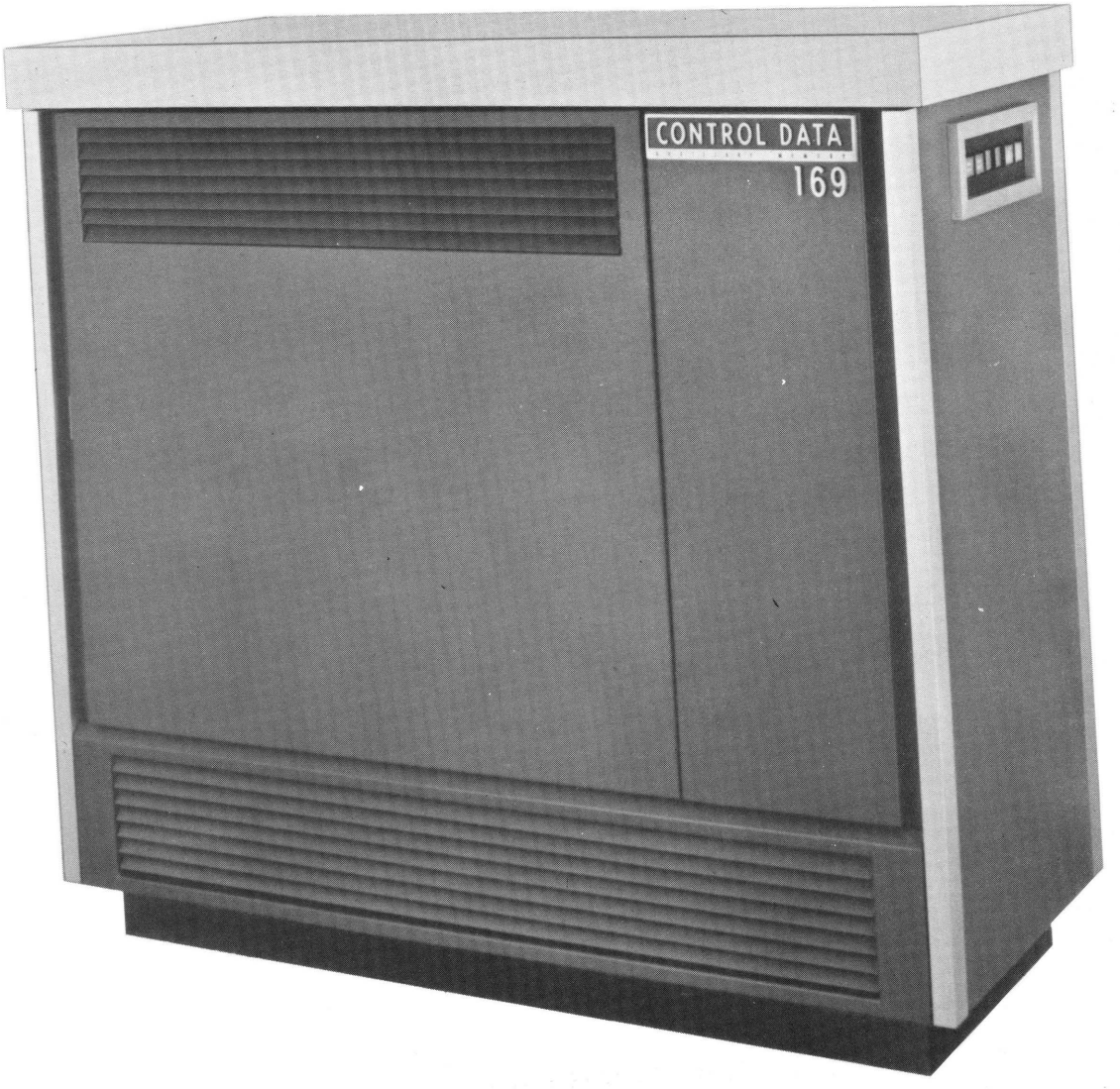
VOLUME 1
DESCRIPTION, OPERATION,
AND MAINTENANCE

CONTROL DATA
169
AUXILIARY MEMORY UNIT

VOLUME 1
DESCRIPTION, OPERATION,
AND MAINTENANCE

144a
REV 8/62

GENERAL CONTENTS


CONTROL DATA
169

CONTENTS

Chapter 1 - Description

Chapter 2 - Operation

Chapter 3 - Principles of Operation

CONTENTS (Cont'd)

Chapter 3 - Principles of Operation (Cont'd)

Chapter 4 - Maintenance

Appendixes

FIGURES

Chapter 1 - Description

Chapter 2 - Operation

Chapter 3 - Principles of Operation

FIGURES (Cont'd)

Chapter 3 - Principles of Operation (Cont'd)

Chapter 4 - Maintenance

TABLES

Chapter 1 - Description

Chapter 2 - Operation

Chapter 4 - Maintenance

CHAPTER 1

DESCRIPTION

The Control Data 169 Auxiliary Memory Unit connects on-line to one or two 160-A computers. The unit increases the storage capacity of the 160-A by 24, 576 words (maximum) and provides the computers with an additional input-output buffer. This buffer, once addressed, operates independent of the computers.

The auxiliary memory unit makes up to five peripheral equipments and six external memory banks available to either computer. Since external buffer and memory circuits function independently, one computer can initiate an external buffer operation while the other uses an external memory module. As long as the computers select separate modules, concurrent external memory references are possible. The 169 resolves multiple requests for a single module on a word-by-word equal-share basis.

EXTERNAL MEMORY CHARACTERISTICS

The 169 cabinet holds one, two, or three external memory modules (figure 1-1). Each module has two 4096 12-bit word banks, identical to those of the 160-A internal memory. A basic 12-bit storage address designates a word location in an internal or external bank. Storage cycle time is 6.4 usec.

The computer storage bank controls specify four functional banks:

relative (for instructions)
direct (for constants)
indirect (for operands)
buffer (for internal buffered I/O data)

Programmed or manual bank selection by the 160-A determines the physical bank to be used (banks 0 and 1 in the 160-A, banks 2 through 7 in the 169). A bank can represent more than one functional bank. Several banks cannot operate concurrently as one functional bank. For example, to have banks 2 and 4 represent the relative bank, the computer must make two bank selections, negating the first before selecting the second.

Independent storage cycles eliminate the need for synchronization between external memory modules.

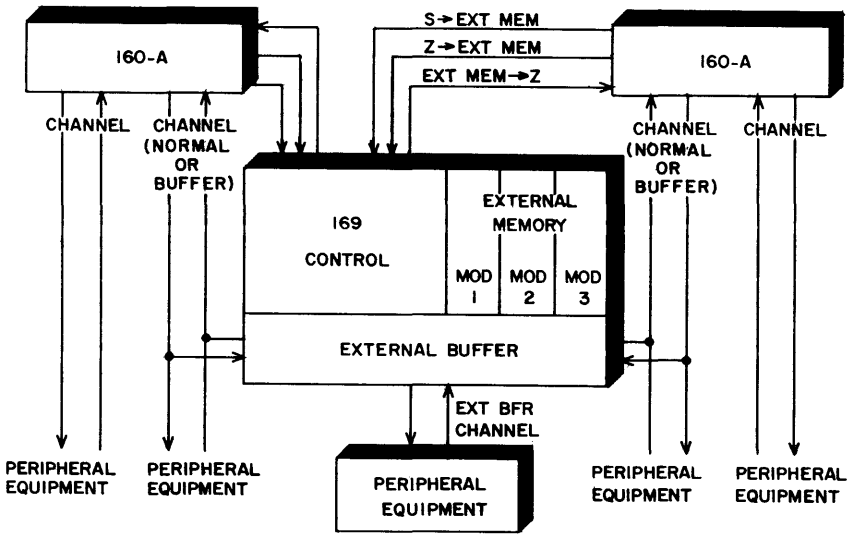


Figure 1-1. System Diagram

The external buffer and computers share access to each external memory module. Each module contains a scanner which continually monitors module access requests from the computers or external buffer. When it detects such a request, the scanner stops and the module storage cycle starts. During the last quarter of this cycle, the scanning resumes. One device cannot monopolize a module. If the computers and the external buffer try to make concurrent storage references in a module, the scanner allows first one, then another, and finally the third device to use the memory. In the most unfavorable case the waiting period between storage cycles cannot exceed 16 usec. In the most favorable case (one device continuously interrogating a particular module), the scanner cycles back during the fourth quarter of the cycle so that there is no delay between storage references.

EXTERNAL BUFFER CHARACTERISTICS

The external buffer is an I/O circuit that transfers information between the external memory and peripheral equipment at rates up to 125 kc. Operation of the external buffer is independent of the computer once the buffer mode has been initiated. During this time the computer can select another equipment or perform internal computation. The 160-A can simultaneously perform input-output operations on the internal buffer channel, external buffer channel (via the 169), and normal input-output channel.

Six external function (EF) codes permit different uses of the external buffer.

Code	Selects	Explanation
4701	Buffer mode	Data is transferred between an external module and a unit of peripheral equipment; rate determined by peripheral equipment.
4702	Clear buffer controls	Master clear of external buffer controls.
4704	Buffer entrance register (BER) read	This code, followed by an INA instruction, transmits the contents of BER (last word buffered address + 1) to computer A register.
4710	Channel extension mode	Computer bypasses buffer circuits to communicate directly with peripheral equipment attached to external buffer.
4720	Clear channel extension mode	Disconnects direct communication between computer and equipment attached to external buffer.
4740	Buffer status	This code, followed by an INA instruction, transmits buffer status information to computer A register.

During the buffer mode selected by code 4701, three interrupt features are available. One notifies the computer of the end of a buffer operation, the second periodically informs the computer of the progress of a non-terminating buffer, and the third interrupts the other computer.

PHYSICAL AND ELECTRICAL CHARACTERISTICS

The 169 has two basic chassis (140100 and 140200), a connector panel, and a power supply (figure 1-2). For 16, 384 word storage capacity, chassis 140400 is added; for

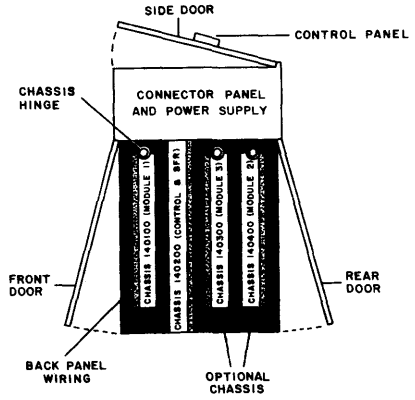


Figure 1-2. Top View, 169 Cabinet Layout

24,576 word storage capacity, chassis 140300 and a second power supply are added. Front and rear doors and swing-out module chassis allow access to both sides of every chassis. A side door permits access to connectors, fuses, and switches.

Printed circuit cards plug into horizontal rows on the chassis. Blower fans at the bottom of the unit cool the components. One or two power supplies provide d-c power for the logic and memory circuits.

TABLE 1-1. TECHNICAL SPECIFICATIONS

Cabinet size	43 inches high x 47 3/4 inches long x 20 1/4 inches deep	
Weight	2 chassis 600 pounds 4 chassis 800 pounds	
60~ Power requirements	Operating: 1380w, 8,192 word memory 365w for each additional 8,192 word memory Standby: 1340w, 8,192 word memory 130w for each additional 8,192 word memory Voltage, 115 vac ± 10%; single phase	
Cooling requirements	4700 BTU/hr 8,192 word memory 5600 BTU/hr 16,384 word memory 6500 BTU/hr 24,576 word memory 80°F room temperature limit	
Data transfer times	160-A	External Buffer
	One 160-A using one module exclusively: 6.4 usec/word	External buffer using one module exclusively: 8 usec/word
	Two 160-A's sharing one module: 14.4 usec/word maximum	One 160-A and external buffer sharing one module: 16 usec/word maximum
	Two 160-A's and external buffer sharing one module: 22.4 usec/word maximum	Two 160-A's and external buffer sharing one module: 24 usec/word maximum
External buffer rate	Operates at rate of peripheral equipment up to 125 kc.	

Note: See appendix C for signal characteristics.

CHAPTER 2

OPERATION

CABINET CONTROLS

The 169 has six indicator switches (figure 2-1, table 2-1). Except for the power switch, these controls allow manual circuit clearing. Timing fault buttons clear the external memory module controls and cannot be programmed. The external buffer can be cleared by the IBA/OBA switch, the Select switch, or EF code 4702.

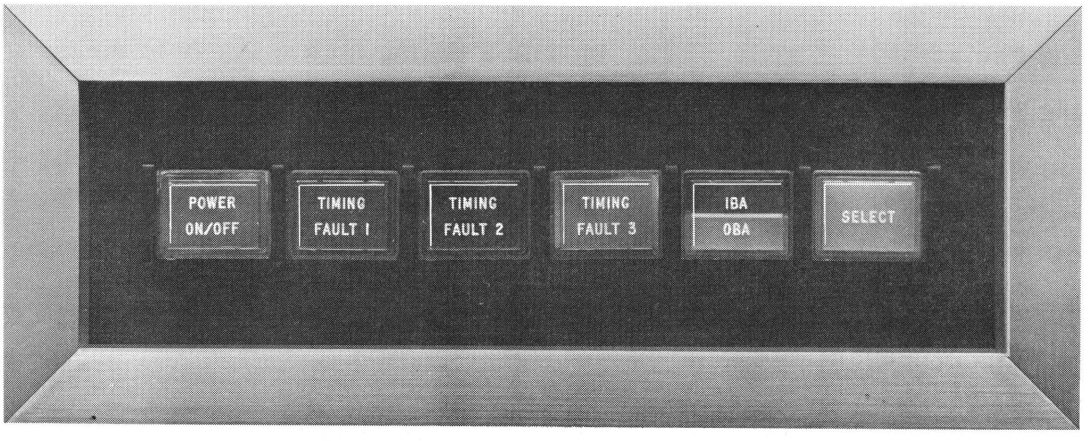


Figure 2-1. Cabinet Controls

STARTING AND CLEARING PROCEDURES

Press the Power On/Off button. A green light indicates that power is on; the three Timing Fault indicators show red. Press each Timing Fault indicator to turn it off and clear the module controls.

If a timing fault occurs in any of the external memory modules during operation, press the indicator involved to clear the circuit. After a clear, the module can be reselected by the computer or the external buffer.

TABLE 2-1. CABINET CONTROLS

Name	Indication	Function
Power On/Off	green	Alternate action switch. Press to supply 115 vac input to power supply. Press again to disconnect power.
Timing Fault 1	red	Module 1 timing fault caused by: initial start condition multiple pulses or dropout of pulse in scanner multiple pulses in module timing chain Press to clear module 1.
Timing Fault 2	red	Module 2 timing fault. Press to clear.
Timing Fault 3	red	Module 3 timing fault. Press to clear.
IBA OBA	blue white	Input buffer (IBA) or output buffer (OBA) is active. Press to clear buffer controls.
Select	white	Buffer is waiting to select peripheral equipment. Press to clear buffer controls.

EXTERNAL MEMORY SELECTIONS

The 160-A uses an external storage bank as it does an internal bank. No external function (EF) codes are needed for external memory operations.

Programmed instructions or manual selections from the 160-A console determine which banks are relative, direct, indirect, and buffer. For an external memory operation, the computer sends bank selection information to the 169. If the external module containing the selected bank is busy, the computer timing chain stops at the end of its first quarter and waits a maximum of 16 usec. When the module becomes available, the 169 completes the selection and restarts the timing chain at the place where it was interrupted. Neither the stopping nor restarting of the computer timing chain is under program control.

EXTERNAL BUFFER SELECTIONS

An EF code selects the external buffer just as an EF code selects any other equipment on the I/O channel (table 2-2). Except for status or BER read information, only one computer can use the external buffer at a time.

The external buffer operates in external buffer and channel extension modes. The first involves a buffered I/O operation; the second, a direct transmission from the computer. Usually, the computer sends a status request to the 169 before either operation. The status request may be repeated by either computer at any time without affecting operation.

TABLE 2-2. EXTERNAL BUFFER EF SELECT CODES

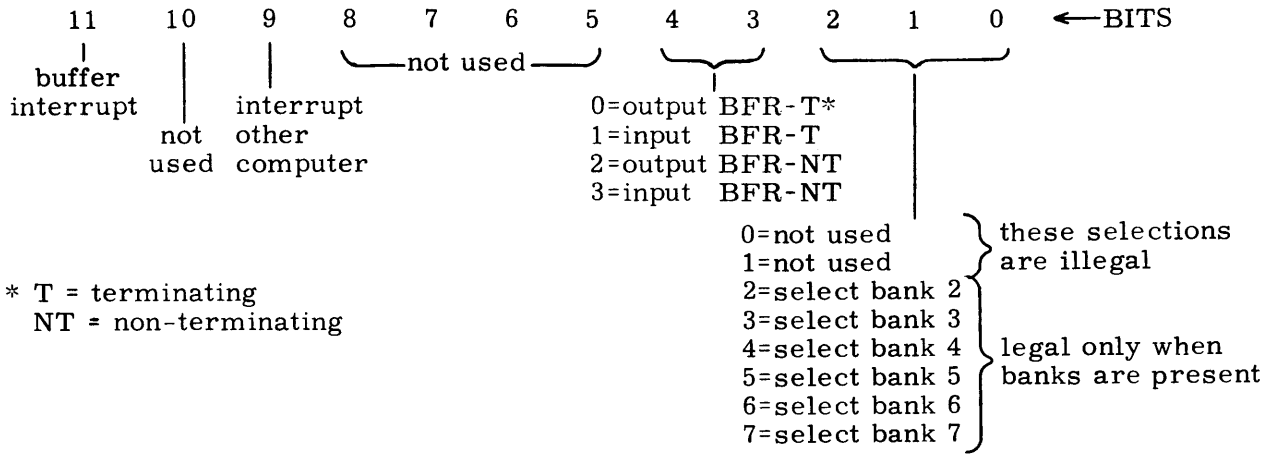
Code	Name
4701	Select External Buffer Mode
4702	Clear External Buffer Controls
4704	Select BER Read
4710	Select Channel Extension Mode
4720	Clear Channel Extension Mode
4740	Select External Buffer Status

BUFFER MODE

The computer selects the 169 buffer mode to transfer data between the external memory and the peripheral equipment at a rate determined by the peripheral equipment. The computer sends four 12-bit control words to the 169 to specify the type and number of buffer operations and the external storage bank. Upon receipt of the fourth word, the 169 buffers data without further computer control. The buffer terminates when the selected block of data is buffered or the buffer circuits are cleared by the 4702 code, IBA/OBA button, or Select button.

CONTROL WORDS

The format for control word 1 is:



Bits 11 and 9 select external buffer interrupts. Bit 3 prepares the external buffer for an input to storage or an output from storage. Bit 4 determines whether the buffer will terminate after transferring a block of data, or continue indefinitely. In the case of an input buffer, an input disconnect will terminate a non-terminating input buffer. Bits 2-0 select one of the six external storage banks for use by the external buffer.

Control word 2 is the address of the first word of the input or output data. Control word 3 is the terminating address (last word + 1) of the input or output data. Control word 3 is not used for a non-terminating buffer operation but must be transmitted to the 169. Control word 4 is the EF code of the peripheral equipment.

PROGRAM EXAMPLES

These programs select the external buffer by using 160-A normal I/O instructions rather than 160-A buffer channel instructions. The first program transmits the control words one at a time, the second uses block transfer.

EXAMPLE 1

Location	F	E	Comment
a	EXF	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read Status
a + 3	NZF	AA	Go if status OK; otherwise jump forward and examine status
a + 4	EXC	00	Select buffer mode
a + 5	47	01	Operand (select buffer)
a + 6	LDC	00	Load control word 1
a + 7	WX	YZ	Word 1 (see control words, above, for WXYZ)
a + 8	OTA		Gate information on the output lines to 169
a + 9	LDC	00	Load control word 2
a + 10	SS	SS	Word 2 (address of first word of input or output data)
a + 11	OTA		Gate information on output lines to 169
a + 12	LDC	00	Load control word 3
a + 13	TT	TT	Word 3 (terminating address of input or output data)
a + 14	OTA		Gate information on the output lines to 169
a + 15	LDC	00	Load control word 4
a + 16	UU	UU	Word 4 (function code of peripheral equipment)
a + 17	OTA		Gate information on the output lines to 169
a + 18	HLT (or continue program)		
AA	subroutine to examine status		

EXAMPLE 2

Location	F	E	Comment
a	EXC	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read status
a + 3	NZF	AA	Go if status OK; otherwise jump forward and examine status
a + 4	EXC	00	Select buffer mode
a + 5	47	01	Operand (select buffer)
a + 6	OUT	XX	Output control words
a + 7	YY	YY	

Location	F	E	Comment
a + 8	HLT (or continue program) Buffer operation is now independent		
XX	FWA		
AA	subroutine to examine status		
FWA	WX	YZ	Control word 1
FWA+1	SS	SS	Control word 2
FWA+2	TT	TT	Control word 3
FWA+3	UU	UU	Control word 4
YYYY	terminating address for output instruction		

INTERRUPTS DURING BUFFER MODE

If bit 11 of control word 1 is a "1", the buffer returns a line 30 interrupt signal when it terminates. For a non-terminating buffer this interrupt occurs each time a buffer cycle is executed at locations 1777_8, 3777_8, 5777_8, and 7777_8. There are 1024_{10} words between each of the above addresses.

Every interrupt sets a status bit in the external buffer so a status check can determine the source of the interrupt. When a computer selects a buffer interrupt, it has priority to use the external buffer until the status response bit, which indicates the buffer complete interrupt, clears.

For a terminating buffer operation, any 169 EF selection clears the buffer interrupt signal. For a non-terminating buffer operation, the periodic buffer interrupt is cleared only by reading the 169 status. For both terminating and non-terminating buffer operation, any EF selection (169 or peripheral), except 169 status, clears the status response bit that indicates buffer interrupt. For a non-terminating buffer, the 169 status must be read before the interrupt status bit can be cleared.

If, at any time while the buffer is inactive, bit 9 of control word 1 is a "1", a line 30 interrupt is transmitted to the other computer. An interrupt from peripheral equipment goes to both computers via the 169.

Buffer interrupt and interrupt other computer should not be selected simultaneously. The IBA/OBA button, Select button, or a clear buffer controls selection by either computer drops all interrupts and the corresponding status bits.

Program Example for Interrupting the Other Computer

This operation signals the other computer. Only bit 9 of control word 1 can be set. The control words 2, 3, and 4 are not sent, and the external buffer is cleared by the clear channel extension code.

Location	F	E	Comments
a	EXC	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read status
a + 3	NZF	AA	Go if status OK, otherwise jump forward and examine status
a + 4	EXC	00	Select buffer mode
a + 5	47	01	Operand (select buffer)
a + 6	LDC	00	Load control word 1
	10	00	Word 1: all bits zero except bit 9 (interrupt other computer)
a + 7	OTA		Gate information on the output lines
a + 8	EXC	00	Select external buffer for clear channel extension
a + 9	47	20	Operand (select clear channel extension)
a + 10	HLT (or continue program)		
AA	subroutine to examine status		

CLEAR EXTERNAL BUFFER CONTROLS

By executing a clear external buffer controls, either computer can clear all 169 selections, interrupts, and any buffering that is in process. No clear is sent to the peripheral equipment. This code should be used with caution for it clears selections by other computer.

SELECT BER READ

The buffer entrance register (BER) read selection can be attempted at any time by either computer. The selection cannot be completed while the other computer is doing a BER read or when BER is advanced during each buffer storage cycle. The waiting periods do not affect program control. When this function code is followed by an INA instruction, the contents of BER are sent to the computer A register. If a buffer operation is in progress, the contents of BER contain the address of the next word to be buffered. If no buffer operation is in progress, the contents of BER contain the effective terminating address (last word address + 1) of the completed buffer.

Program Example

This program uses a BER read to determine the length of an input buffer. The program does an output of the same words that were buffered in.

Location	F	E	Comments
a	EXC	00	Clear buffer controls
a + 1	47	02	Operand (clear buffer controls)
a + 2	EXC	00	Select buffer mode
a + 3	47	01	Operand (select buffer mode)
a + 4	OUT	AA	Send control words for input buffer
a + 5		BB+4	
a + 6	EXC	00	Select 169 status
	47	40	Operand (select 169 status)
a + 7	INA	00	
a + 8	NZB	01	Wait until buffer terminates (zero status means buffer is completed)
a + 9	EXC	00	Select BER read
a + 10	47	04	Operand (select BER read)
a + 11	INA	00	Read effective terminating address of input buffer
a + 12	STF	DD+2	Place above address into output buffer control word 3
a + 13	EXC	00	Select buffer mode
a + 14	47	01	Operand (select buffer mode)
a + 15	OUT	CC	Send control words for output buffer
a + 16		DD+4	
a + 17	EXC	00	Select 169 status
a + 18	47	40	Operand (select 169 status)
a + 19	INA	00	Wait until buffer terminates
a + 20	NZB	01	
a + 21	ZJB	a+2	Repeat program
AA		BB	Location of control word 1 for input buffer
CC		DD	Location of control word 1 for output buffer
BB	00	12	Control word 1 for input buffer (specifies bank 2)
BB+1	10	00	Control word 2 for input buffer (start at loc. 1000)
BB+2	20	00	Control word 3 for input buffer (terminate at loc. 2000)
BB+3	42	20	Control word 4 for input buffer (select typewriter input)

Location	F	E	Comments
DD	00	02	Control word 1 for output buffer (specifies bank 2)
DD+1	10	00	Control word 2 for output buffer (start at loc. 1000)
DD+2	20	00	Control word 3 for output buffer (set by program to (BER))
DD+3	42	10	Control word 4 for output buffer (select typewriter output)

CHANNEL EXTENSION MODE

The EF code that selects channel extension mode connects the 169 I/O lines directly to the 160-A I/O channel. This operation bypasses all external buffer controls. The channel extension mode is cleared by the same computer selecting the buffer mode or executing the clear channel extension function. Either computer can clear the channel extension mode by selecting clear buffer controls.

PROGRAM EXAMPLE

Location	F	E	Comments
a	EXC	00	Select external buffer for status
a + 1	47	40	Operand (request buffer status)
a + 2	INA		Read status
a + 3	NZF	AA	Go if status OK, otherwise jump forward and examine status
a + 4	EXC	00	Select channel extension mode
a + 5	47	10	Operand (select channel extension)
a + 6	EXC	00	Select peripheral equipment for status
a + 7	UU	UU	Operand (request status of peripheral equipment)
a + 8	INA		Read status
a + 9	NZF	BB	Go if status OK, otherwise jump forward and examine status
a + 10	EXC	00	Select peripheral device for output
a + 11	VV	VV	Operand (select code for peripheral equipment)
a + 12	OUT	YY	Transmit output data (YY starting address)
a + 13	WW	WW	(WWWW terminating address of output data)
a + 14	EXC	00	Select clear channel extension
a + 15	47	20	Operand (clear channel extension)
a + 16	HLT or continue program		

Location	F	E	Comments
AA			Subroutine to determine cause of non-zero status response
BB			Subroutine to determine cause of non-zero status response
YY		SS	Starting address
SS			First word of output data

EXTERNAL BUFFER STATUS

Either computer can select status at any time. When an INA instruction follows this function code, a 12-bit status response returns to the computer. The computer subroutine that examines the status response returned by the 169 must check the bit positions (figure 2-2).

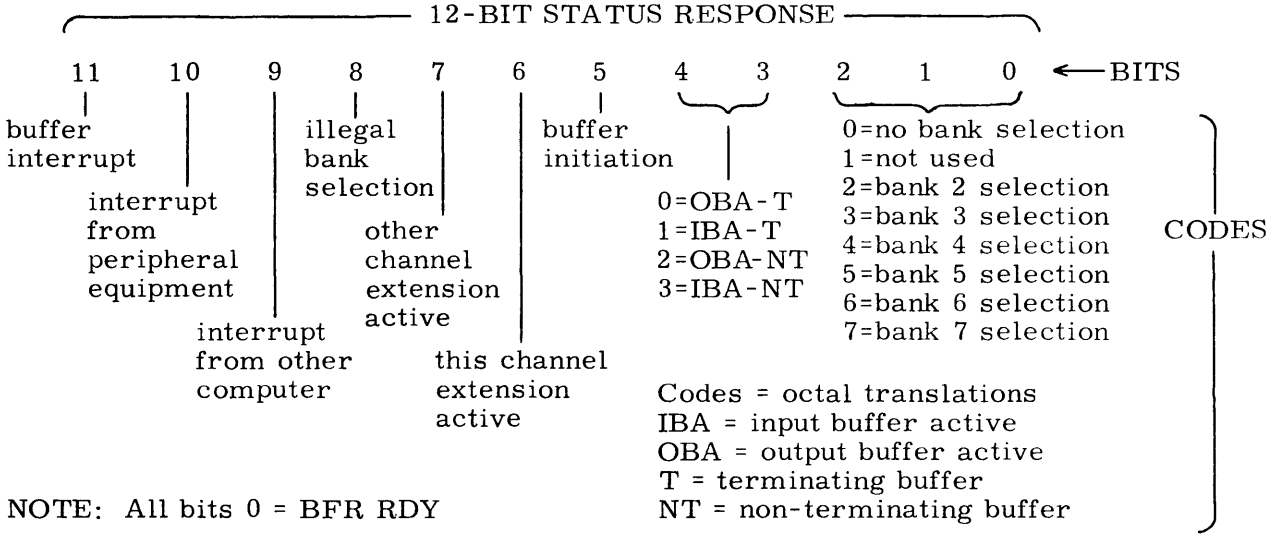


Figure 2-2. Status Response

The status response bits occur in combinations so that one response transmits all status information. In general, the status response bits report on control word 1 selections. Bit 5, buffer initiation, is present between the selection of the buffer mode and the function signal from the peripheral equipment which starts data buffering. If a channel extension is selected, bits 6 and 7 specify which computer made the selection. Bit 8 is a "1" when a 160-A internal storage bank or an external bank not in the 169 is selected. Bit 10 indicates interrupt conditions which did not originate in the 169. All bits are zero when buffer mode and channel extension are inactive and no interrupts exist (buffer ready).

PROGRAM EXAMPLE

This program examines each bit position of the 12-bit status response, starting at the left.

Main Program Exit-Enter Routine

Location	F	E	Comments
30	Main program address		
31	STD	37	Save contents of A register at time of interrupt
32	JPR	00	Jump to status response routine
33	b		Routine location - 1
34	LDD	37	Restore (A) to value at time of interrupt
35	CIL		Clear interrupt lockout
36	JPI	30	Return to main program
37	Temporary storage for A register		

Status Response Routine

Location	F	E	Comments
b - 1	JFI	01	Re-enter above routine
b	XX	XX	
b + 1	EXC	00	Select status request
b + 2	47	40	Operand (select status)
b + 3	INA		Read status
b + 4	PJF	03	If no status bit, continue routine
b + 5	JPR	00	If status bit, jump to buffer interrupt routine
b + 6	c		Routine location - 1
b + 7	LS1		Shift A left 1
b + 8	PJF	03	If no status bit, continue routine
b + 9	JPR	00	If status bit, jump to peripheral equipment interrupt routine
b + 10	d		Routine location - 1
b + 11	LS1		Shift A left 1
b + 12	PJF	03	If no status bit, continue routine
b + 13	JPR	00	If status bit, jump to interrupt from other computer routine
b + 14	e		Routine location - 1
b + 15	LS1		Shift A left 1

Location	F	E	Comments
b + 16	PJF	03	If no status bit, continue routine
.	.		.
.	.		.
.	.		.
Check remaining 9 bit positions in same way			
.	.		.
.	.		.
b + n	JFI	01	Return to main program exit, enter routine
	b - 1		
c - 1	JFI	01	Re-enter status response routine
c	b + 7		
c + 1	--		Buffer interrupt routine
c + n	JFI	01	
	c - 1		Return to status response routine
d - 1	JFI	01	Re-enter status response routine
d	b+11		
d + 1	--		Peripheral equipment interrupt routine
d + n	JFI	01	
	d - 1		Return to status response routine
e - 1	JFI	01	Re-enter status response routine
e	b+15		
e + 1	--		Interrupt from other computer routine
e + n	JFI	01	
	e - 1		Return to status response routine
.	.		.
.	.		.
.	.		.
remaining status subroutines			
.	.		.
.	.		.
.	.		.

CHAPTER 3
PRINCIPLES OF OPERATION

Volume 2, Equipment Diagrams, and volume 3, Equation File, supplement this chapter. The file and diagrams express all logic connections in Boolean algebra. All descriptions require familiarity with the 160-A computer.

INTERNAL AND EXTERNAL 160-A MEMORY AND BUFFER OPERATIONS

All 160-A storage and buffer operations are basically the same whether they occur internally or externally. The block diagram of storage and buffer circuits (figure 3-1) shows only one of the two possible computers and only one of the three possible memory modules. The abbreviations used in this chapter are:

MOD	memory module
BFR	buffer
I^-	inverter
S	storage address register
'	equivalent computer register in external module
( )	equivalent computer register in external buffer
BFR	buffer register
TAR	terminating address register
BER	buffer entrance register
BAR	buffer address register
AHR	address hold register

The block diagram shows four basic operating loops. The two external loops use 169 circuits to accomplish the same operations as the 160-A internal memory and buffer loops.

	INTERNAL	EXTERNAL
MEMORY	S → Mod → Z	S → Z S' → Mod' → Z'
BUFFER	S → Mod → Bfr	BAR → BFR S' → Mod' → Z'

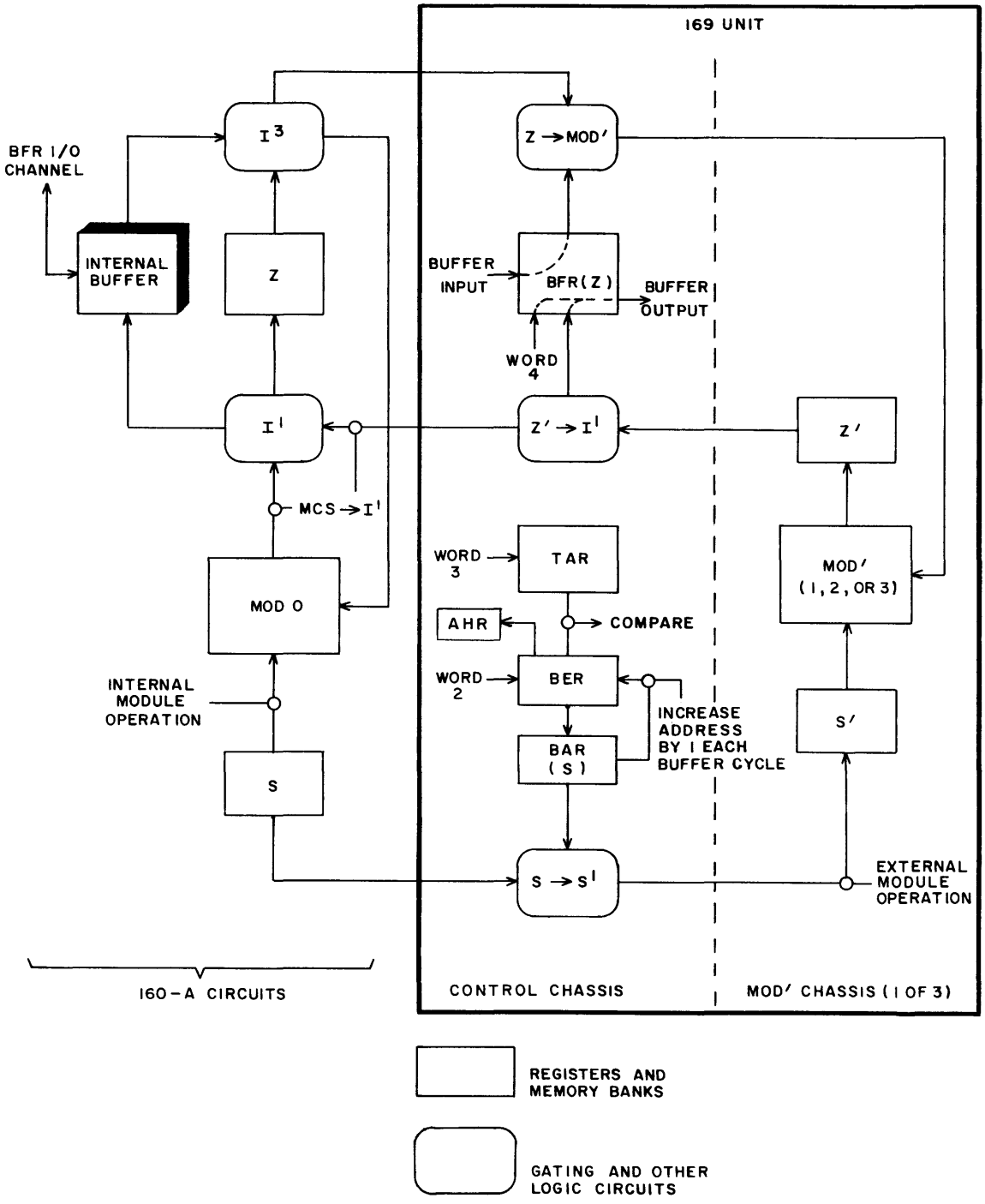


Figure 3-1. 169 Block Diagram

STORAGE SECTION

Each of the six banks (maximum) in the storage section consists of a 4096 word, 12-bit memory using magnetic toroids. The toroids, or cores, have an essentially square hysteresis curve. The memory (storage) cycle is 6.4 usec long. The read phase, which takes 1.8 usec, transfers the information from storage to the storage register (Z'). The information in the selected cores is destroyed, but is automatically restored by rewriting during the write phase, which is initiated 2.8 usec after the start of the module storage cycle and lasts 1.8 usec.

MEMORY PLANES

Each bit of the 12-bit word is represented by a separate plane containing 4096 cores in a 64 x 64 array. The 12 planes are stacked to constitute a storage bank. Two banks (24 planes) form a memory module (figure 3-2). This module is the same as that used in the internal storage of the 160-A computer.

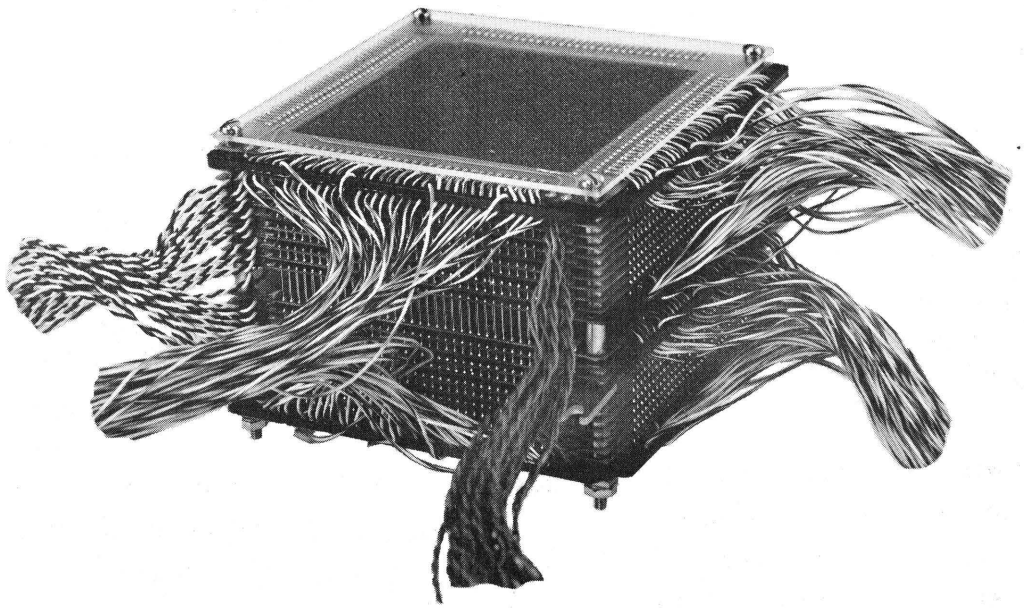


Figure 3-2. Memory Module

Four continuous wires thread each core (figure 3-3). Two of the wires, intersecting the core at right angles to each other, select one of the cores in the array by the vertical and horizontal coordinate system. These wires, called the horizontal and vertical drive lines, transverse each of the 12 planes. In this manner, all 12 bits of one word (the 12 cores at the corresponding coordinate locations in each of the memory planes) are selected simultaneously.

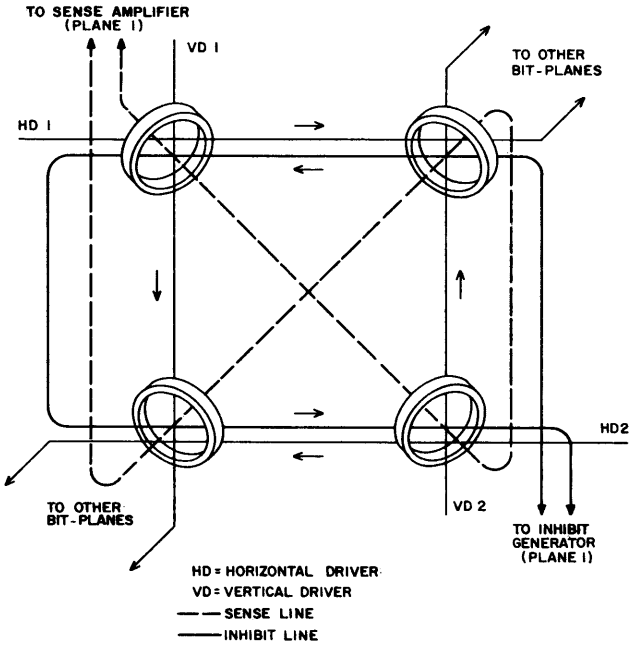


Figure 3-3. Four-Bit Magnetic Core Storage

The drive lines connect to a bi-polar source (read/write drivers) which passes current in the lines in one direction for writing data into the core and in the opposite direction (reversing the state of the core) for reading data from the core. The read pulse switches a core from a "1" to the "0" state, and the write pulse switches the core from a "0" to a "1".

The third wire, the inhibit line, is in parallel juxtaposition with the horizontal drive lines. Since the drive lines influence all 12 cores in a selected word simultaneously, it is necessary to negate the effect of those lines in any bit position which must remain in the "0" state. The 12 inhibit lines connect to 12 inhibit generators which are controlled by the state of a corresponding bit position of Z or bit position of a Buffer Data register. If, for example, Z contains a "0" for bit 04, the correct inhibit generator

is switched. Current in the inhibit line equals that in the H drive line, but is of opposite polarity. As a result, the effect of the write currents acting on the selected core in the inhibited bit-plane is insufficient to change the state of that core from "0" to "1".

The fourth wire, intersecting all cores of one bit-plane, is the sense line. It detects the pulse created when the core in that plane shifts from "1" to "0" during the read phase. The outputs from the sense windings transfer the word to the Z' register, where it is made available to the computers or buffer. Writing information is accomplished by the data sent to the inhibit translators from the computers or the buffer. The 169 makes no distinction between a memory cycle used to read information or one used to write information.

The H and V drive lines thread across the board horizontally and vertically and terminate in tabs at either side of the edge of the phenolic memory plane frame. A wire connected to a front tab on one edge of the frame terminates in a rear tab on the opposite edge. This allows close spacing of the wires. The end of each inhibit wire terminates in a corner of the frame from which connections are made to the inhibit generator. Sense amplifier connections terminate in another corner of the frame.

The 24 memory planes comprising the memory plane assembly, or stack, are held together by bolts passing through the four corners of each, and are separated by tubular aluminum spacers. An aluminum plate at the back and a plexiglass plate at the front protect the stack from physical damage.

PROPERTIES OF THE MAGNETIC CORE

The magnetic properties of a core are represented by its hysteresis diagram (figure 3-4), which plots magnetic flux density (B) as a function of the field intensity (H). If current sufficient to cause a field intensity of $+H_m$ is applied to the drive lines, the flux density increases to saturation ($+B_s$). When current is removed, the flux density drops to the residual positive value ($+B_r$), the "0" state, and remains there. Another pulse of ($+H_m$) would shift the core to ($+B_s$) again; after the pulse is removed, it would drop back to ($+B_r$).

Application of current sufficient to cause a field intensity of $-H_m$ reverses the flux density to $-B_s$ and, when current is removed, the flux density drops to the residual negative value ($-B_r$), the "1" state.

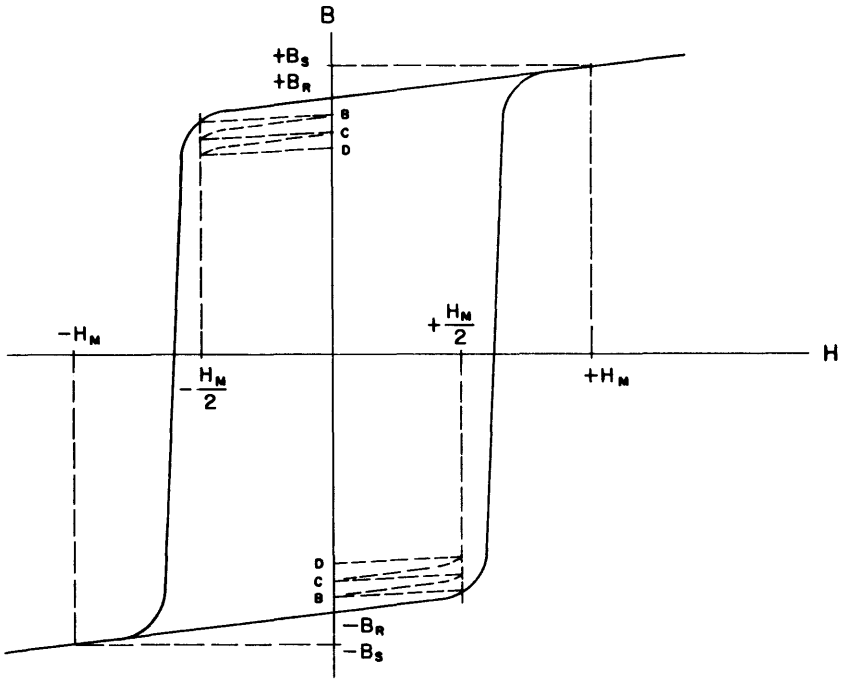
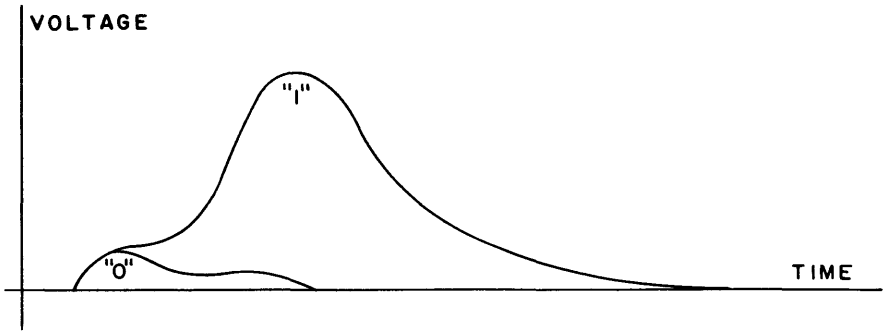


Figure 3-4. Typical Hysteresis Diagram

The basic memory cycle uses half-amplitude pulses capable of producing a field intensity of $H_m/2$. Since a half-amplitude pulse cannot switch the core, the flux density returns to the residual value or slightly lower after the pulse is removed. The coincidence of two half-amplitude pulses, one on the H drive line and the other on the V drive line of a core, produces a net field of H_m sufficient to switch the core. When a half-amplitude pulse drives the flux density toward the knee of the hysteresis loop, the flux travels up or down the knee and then returns to a slightly lower residual value (B). Since the core is operating on a smaller loop, further half pulses reduce this remanent flux again and this effect soon reaches a limit, point D.

Any change in the magnetic state of a core causes a change in the total flux linking the core and winding and produces a voltage output on the sense winding (see drawing). While H is applied, the voltage is sampled to see if the core switches. If a large voltage is sensed, the core was in the "1" state and has switched. If a small voltage is sensed, the core was in the "0" state and has shifted from $+B_r$ to $+B_s$ and back again.



ADDRESS SELECTION

There are 4096 cores in each memory plane, and each core may be addressed by a discrete combination of one of the 64 horizontal and one of the 64 vertical drive lines. The 64 horizontal drive lines connect, in groups of eight, to eight horizontal drivers; the 64 vertical drive lines connect similarly. Current from the drivers is directed or diverted by eight diverter cards to one of the eight associated drive lines. Thus, the combination of eight drivers and eight diverters selects any one of 64 drive lines, horizontal or vertical.

Storage Address Register

The information for selecting one out of 4096 possible cores in each memory plane is in the storage address register at the start of every storage cycle. As shown below, the 12 stages of the S' register form four octal groups. The highest order group controls inputs to translators which select the horizontal read/write driver, the next lower group provides horizontal diverter selection, and the two remaining octal groups provide selection for the vertical read/write driver and vertical diverter.

HORIZONTAL R/W DRIVER			HORIZONTAL DIVERTER			VERTICAL R/W DRIVER			VERTICAL DIVERTER		
11	10	09	08	07	06	05	04	03	02	01	00

Storage Translators

The storage translators interpret the contents of the four octal groups of S' to provide inputs to the correct driver and diverter elements for each H and V selection.

R/W Driver Selection: Each bi-polar read/write driver connects to eight drive lines. The direction of the current in these lines depends on whether the associated driver is in the read or write state, as determined by storage reference control. Electronic Theory of Memory Circuits, appendix B, discusses production of this current.

The R/W drive selection for a given state of the three pertinent stages of the S' register allows a total of three translators to be selected (figure 3-5). Only two of these will be selected at any one time, since one translator depends only on the translation of S'; the other two are also dependent on the read and write phases of the storage cycle. It is the conditional translator which ultimately decides whether the current through the drive line will produce a read or write pulse.

The current source cards provide d-c from which the selected driver draws the read/write current. A current of 400 ma is needed to shift the state of the memory core. Each current source card provides 100 ma of this current. The half current of 200 ma needed for the H or V line is provided by a current step-up ratio of 1:2 delivered by the transformer on the driver card.

The 64 H or V drive lines do not form a continuous progression from 00 to 77 (octal), but are interlaced (figure 3-6). Each even numbered driver has eight drive lines interlaced with those from the successively higher odd numbered driver. This does not affect the selection of any chosen core, but merely makes drive line connections more convenient.

The T1-- translators select the horizontal R/W drivers (G01-); the T0-- cards perform the vertical R/W driver selection (G00-).

Diverter Selection: The diverters determine which of the eight drive lines is to carry the R/W current through the 12-bit planes. Stages $S^{6, 7, 8}$ supply the information used by translators T300 through T305 to determine the horizontal drive line selected; $S^{2,1,0}$ in conjunction with T200 through T205 select the vertical drive line. The eight horizontal (D10-) and eight vertical (D00-) diverters are selected by a translation of the three bits of the S' register for that particular set. A translation choosing diverter four (D-04) is given as an aid to understanding the octal translation (figure 3-6).

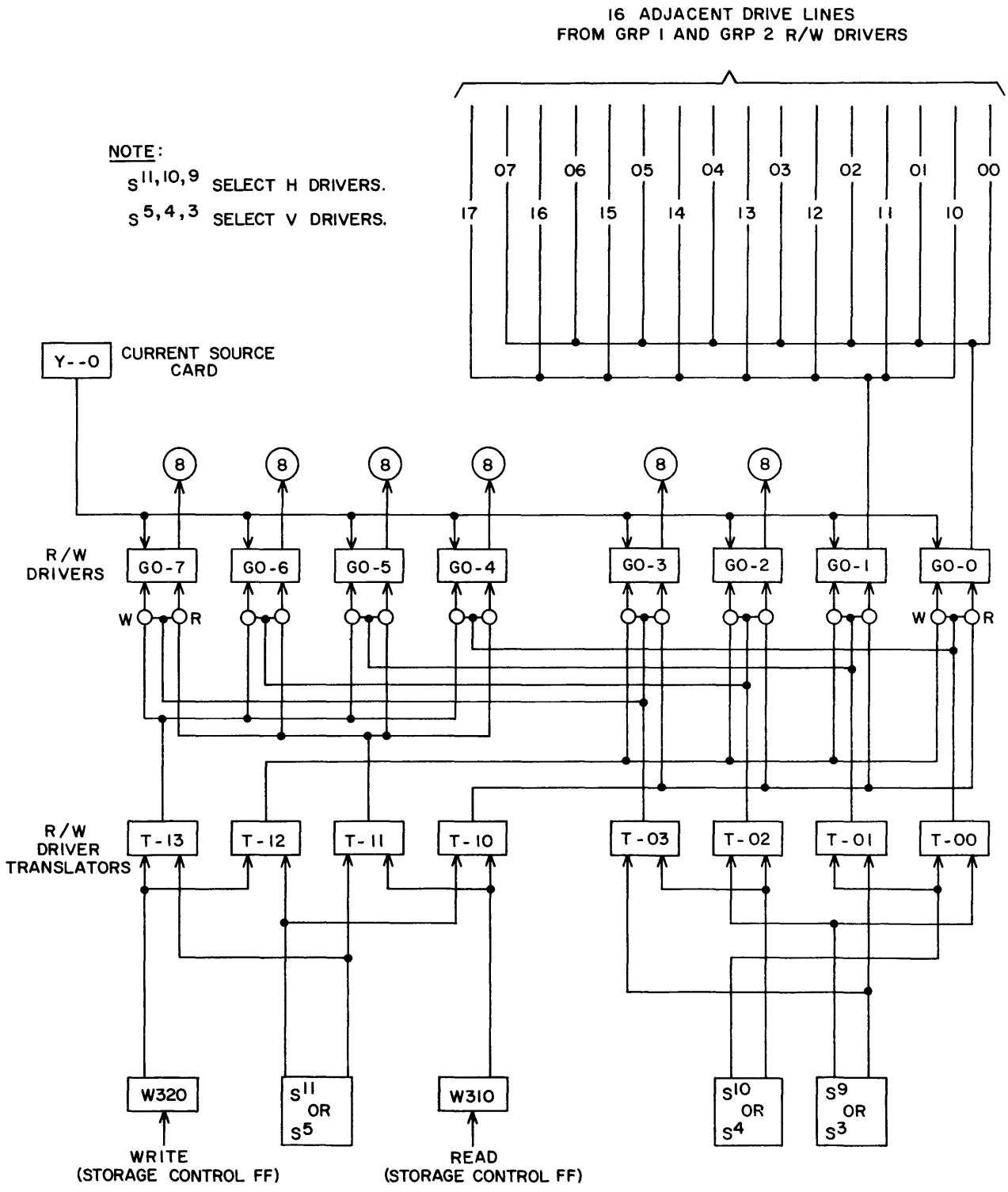


Figure 3-5. R/W Driver Selection

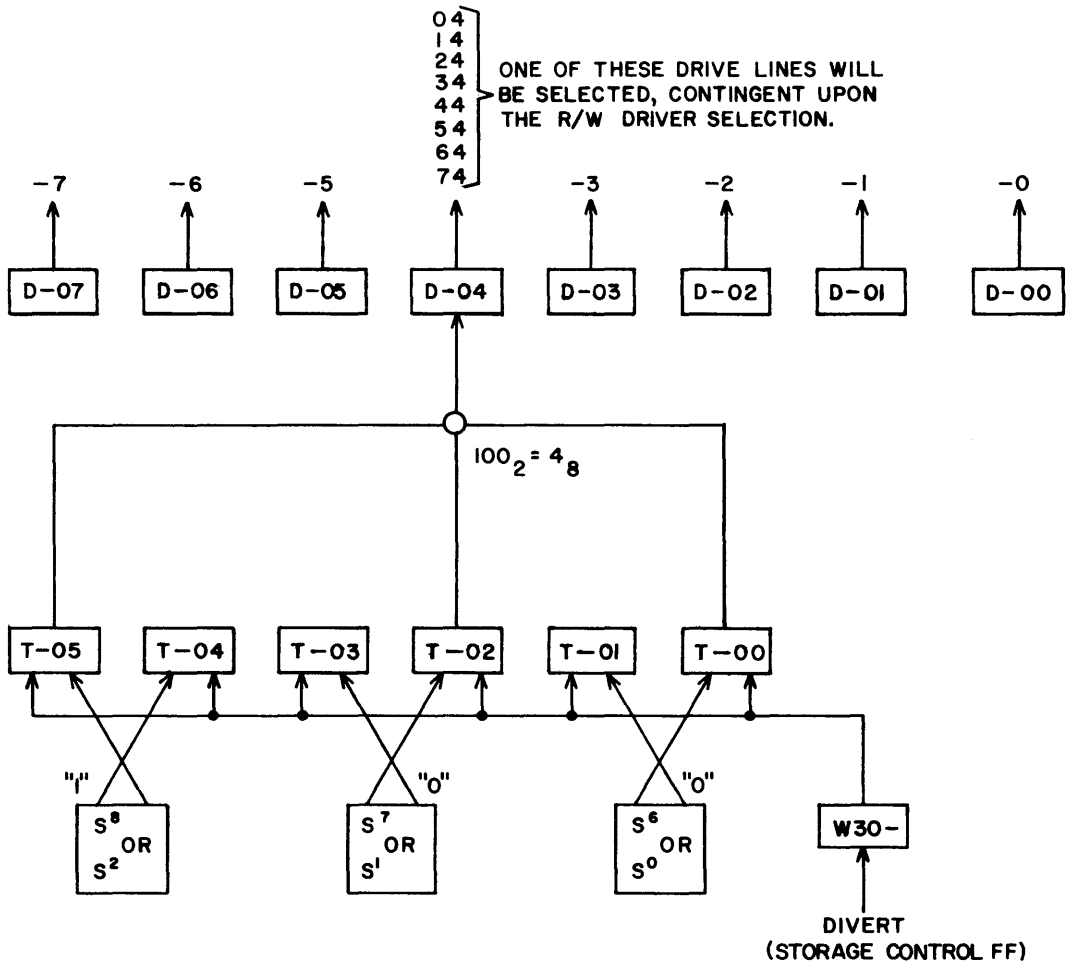


Figure 3-6. Diverter Selection

Inhibit Driver Selection: If the core is not to be forced to a "1" by the write current pulse (figure 3-7), an inhibit driver must hold the selected core in the memory plane in the "0" state. Two parallel current source cards (Y2--, Y3--) provide d-c for the inhibit driver connected to each memory plane. The stage of Z' controlling the inhibit translator must be a "0" to select the translator. A driver must be selected and the storage reference control must be in the inhibit phase before the drive current is generated.

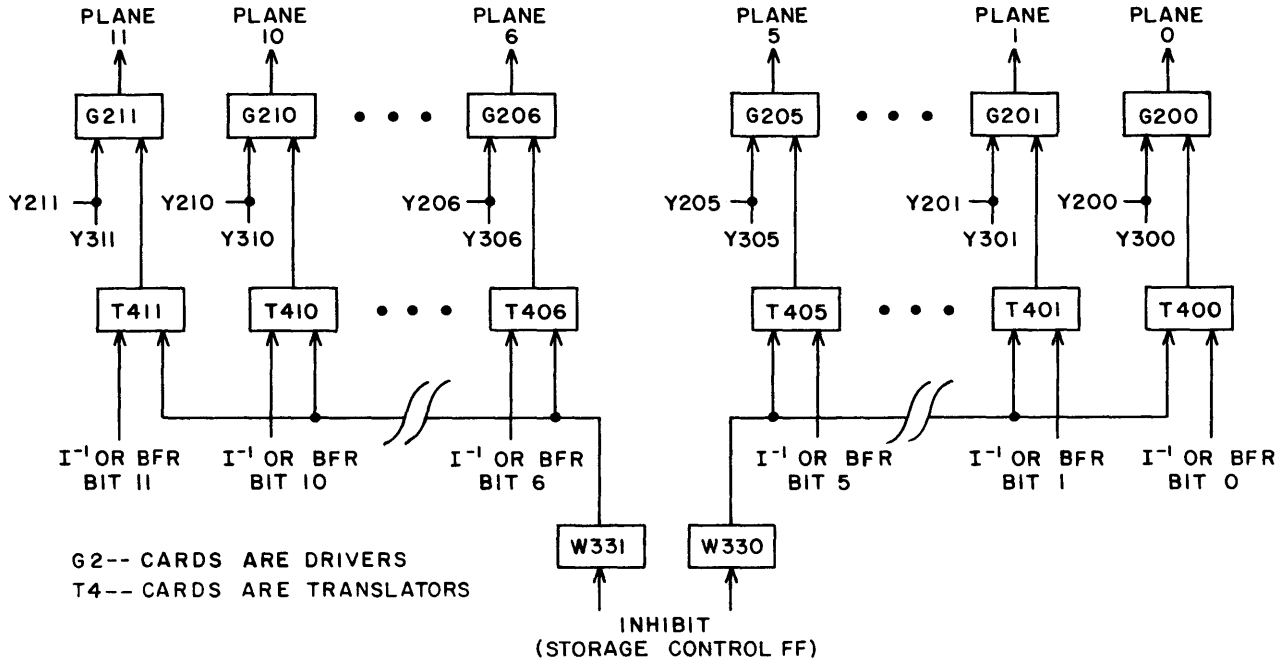
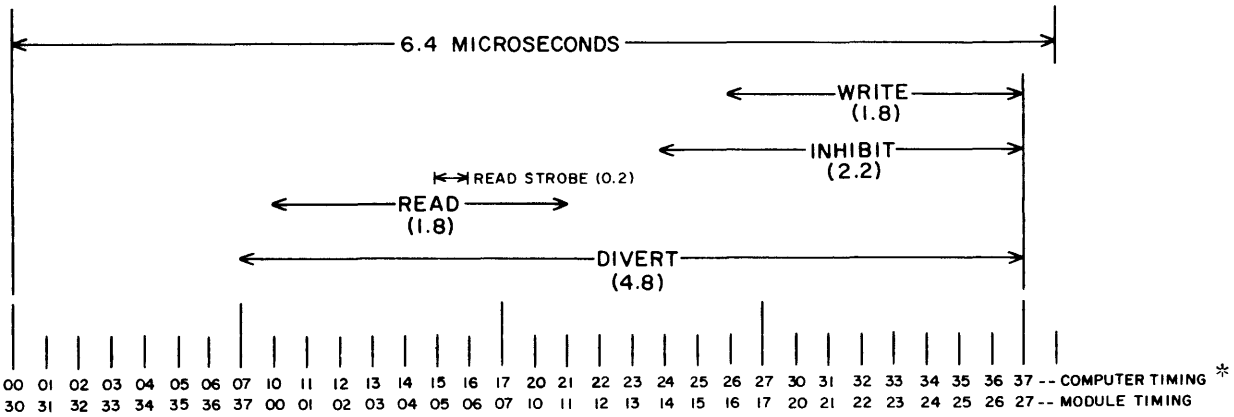


Figure 3-7. Inhibit Driver Selection

STORAGE CYCLE

The storage cycle selects a word from memory or writes a word in memory. The 32-pulse cycle has four overlapping phases: read, write, inhibit, and divert. During the read phase, two drive lines (one H and one V) switch the selected toroids to the "0" state. During the overlapping write and inhibit phases, the drive lines set each of the 12 selected cores to a "1" except where prevented by an inhibit line. The divert operation which permits a final selection of two drive lines out of a possible 128 is necessary because the read/write drivers enable the H and V lines in groups of eight. Since the drive lines remain selected throughout read and write, the divert phase encompasses both of these.



EACH DIVISION REPRESENTS 0.2 MICROSECOND. FIGURES IN PARENTHESES INDICATE ELAPSED TIME (IN μs) FOR THAT PHASE.

* NOTE--EXTERNAL BUFFER TIMING SAME AS COMPUTER TIMING

The above diagram shows when the external module Read, Write, Inhibit, and Divert FFs are set during one storage cycle. When the 160-A uses internal instead of external memory, four similar FFs in the 160-A operate at approximately the same time.

The external memory module controls, which supply storage cycle timing, do not differentiate between 160-A storage cycle types A, B, C or D.

MODULE CONTROL

SELECTION

At the end of the 4th quarter of its storage cycle, the selecting device (160-A or external buffer) sends an external module select code to the 169. If the module is not busy, the 169 returns a resume signal in time to allow the device timing chain to continue without interruption. If the module is busy, the device chain stops after the next quarter cycle. When the resume occurs the device timing chain continues from where it stopped.

When the device enters the first quarter of its storage cycle, the 169 translates the module select code. A scanner assigned to each module continually searches for select signals whenever the module is not in use. This scanner starts within 4 ms after power is turned on. When the recirculating pulse in the scanner loop (figure 3-8) senses a select, an AND circuit is completed to set one of the select FFs and cause the following events:

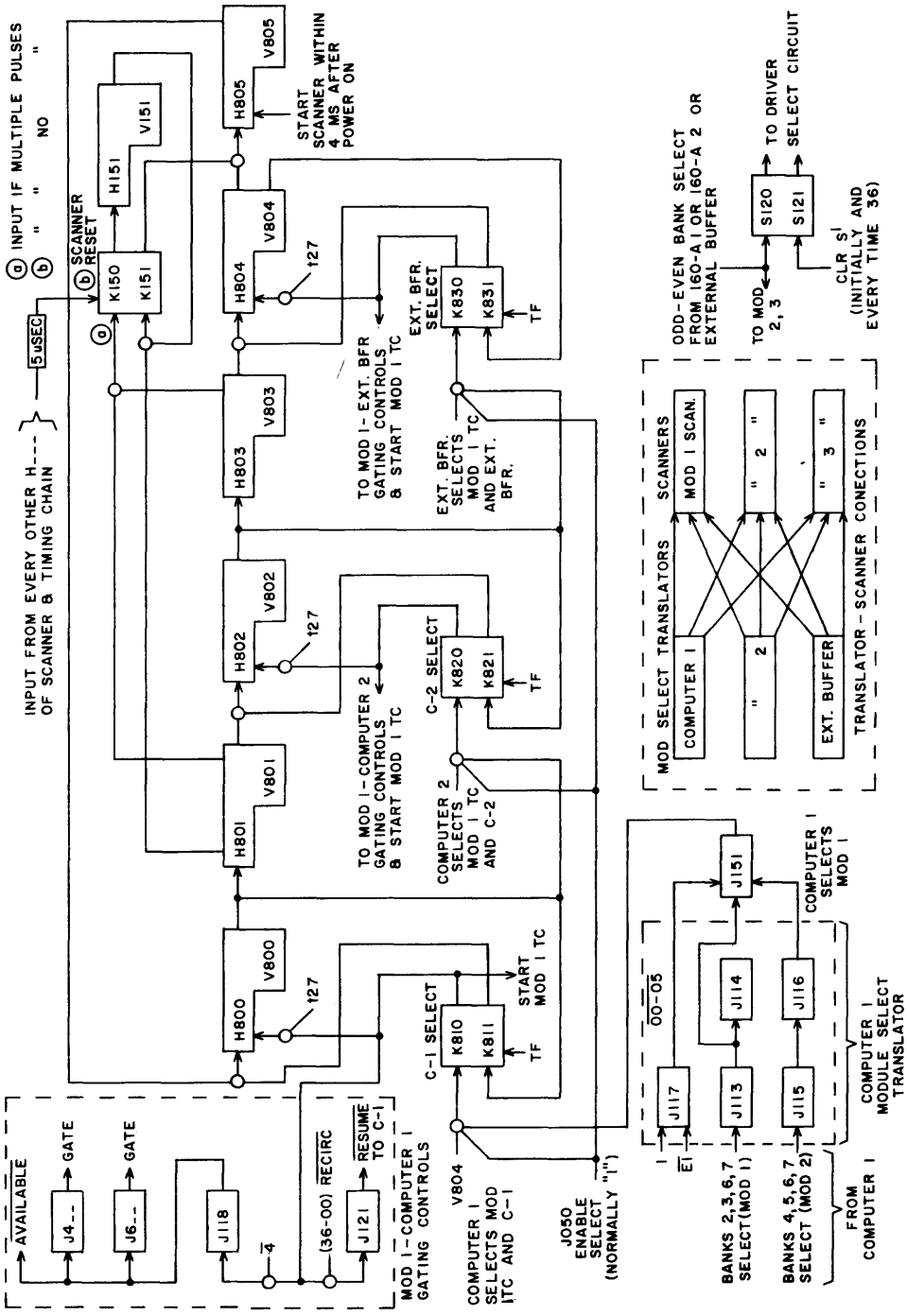


Figure 3-8. Module Selection Control (Scanner)

The scanner stops and locks out all other requests until the external memory operation is over (time 27 of the module timing chain).

The module connects on-line to the device.

An Available signal (0v) is returned to the device. This signal removes the blocking of the device timing chain.

A resume signal (0v) restarts the device timing chain or continues it if it has not yet stopped.

The Scanner Reset FF and H151 eliminate multiple pulses in the scanner when power is turned on. This circuit also indicates a timing fault when it detects scanner pulse duplication or dropout.

Each scanner connects to all three module select translators (figure 3-8). This multiple connection allows both computers and the external buffer to use the external memory unit at the same time if different modules are selected.

TIMING

The memory modules operate independently; each module has a timing chain, quarter counter, quarter translations, and storage control FFs. When selected, a module substitutes its core memory and timing signals for those in the 160-A. The computer cannot sense any difference between internal and external module references.

Two 160-A computers and the external buffer have access to any module according to priority determined by the module scanner. When the scanner stops to complete a selection, the resultant Available signal combines with the next even resync pulse from the selecting device (pulse every 1.6 usec) to start the module timing chain (figure 3-9). The chain starts in clock synchronization with the timing chain of the selecting device but lags by one quarter cycle. All external module storage control signals are adjusted to be available to the 160-A or external buffer at the correct time.

Figure 3-23 at the end of this chapter shows the relationship between the timing chain in the selecting device and that in the selected module. During the last quarter of the 32-pulse module storage cycle, the scanner searches for another request. If a request is not present the module timing chain stops at the end of the cycle.

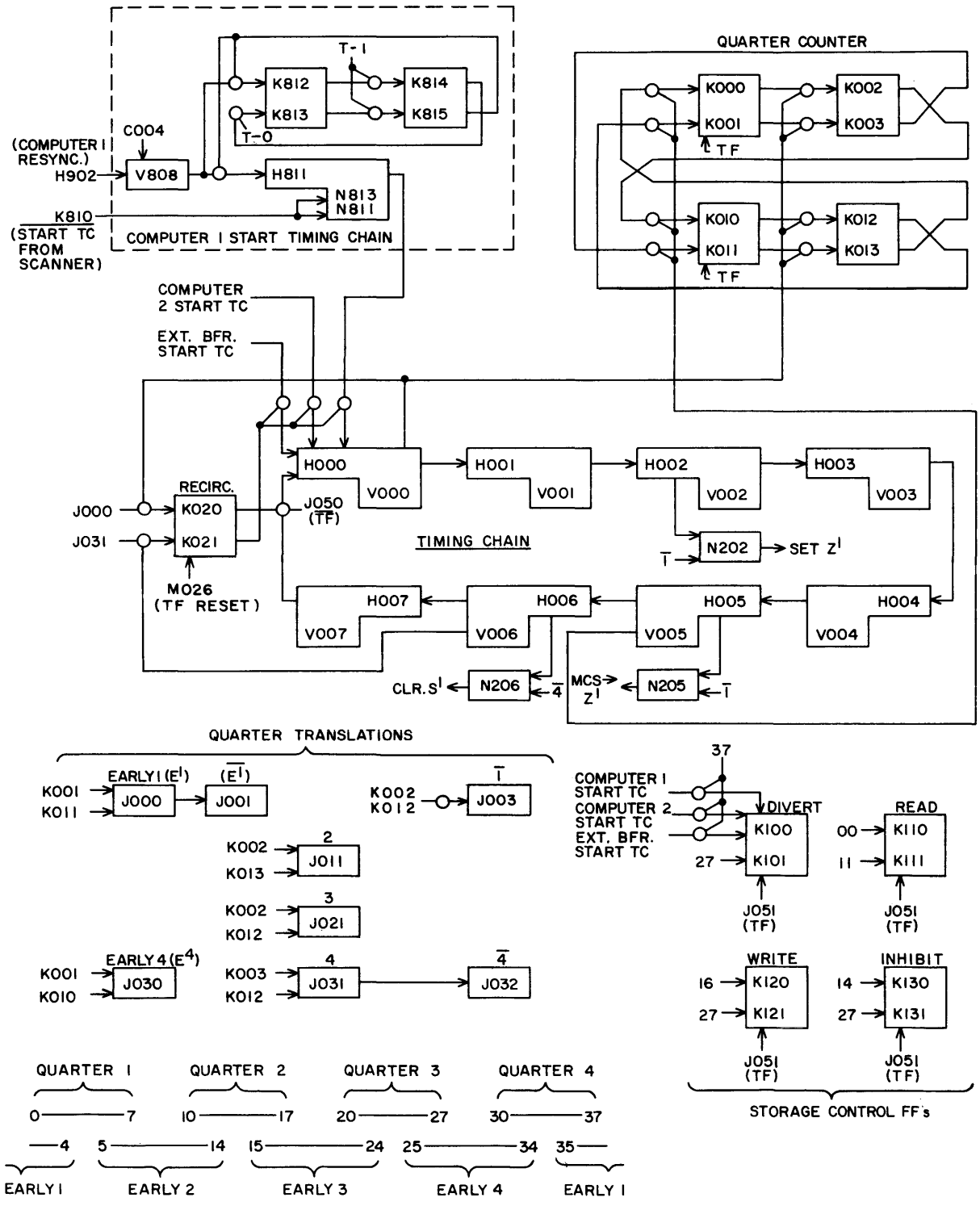


Figure 3-9. Module Timing Control

GATING

Gating inverters determine which paths are gated by external module selections (figure 3-10). The memory modules connect to the external buffer the same as to the 160-A computers.

When the scanner accepts a selection from a 160-A, the selected module replaces the internal module. In general, J4-- and J6-- gating terms are arranged so that the second digit represents the interrogating device, and the third the module interrogated. The external buffer interrogating module 2, for example, could be represented by J432. These terms gate Z'→Z and Z→Mod' for the period starting 0.4 usec before the first quarter of the module timing chain and ending after the third quarter. Although the external module is connected to the device during this time, actual reading and writing are under storage cycle control.

N8-- terms gate the storage address into S' (S→S') 0.2 usec before the first quarter of the module timing chain. The address is, therefore, present in the module Storage Address register during read/write operations.

NON-VOLATILE STORAGE AND RESET CIRCUITS

Decay of memory drive line current after a power interruption or multiple pulses in the timing chain after power application cause accidental destruction (volatilization) of storage. The non-volatile storage circuit (figure 3-11) clears storage controls during these situations.

The pulsating d-c from the bridge rectifier goes to the input pin of a standard input amplifier. With no rectifier output, the voltage divider (two 2.2K resistors) holds point (1) at ground. During the decay of each -20v (peak) pulse, M916 switches between ground and -3v. Due to their brevity and spacing, the negative pulses from M916 cannot pass the 4 ms capacitive delay between M916 and J040. J040 therefore has a "1" output unless power is interrupted.

If power is interrupted (power takes 45 ms to drop), J040 allows J051 to have an output at fourth quarter. This output clears the quarter counter, storage control FFs, and blocks select signals, the module timing chain recirc path, and (through the storage control FFs) current to the memory driver cards.

The same clearing and lockouts occur when power first comes on and when multiple pulses arise in the scanner or timing chain. The Timing Fault light also goes on and S' clears. Press the Timing Fault Reset button to remove the clears and lockouts and to permit another selection of the module.

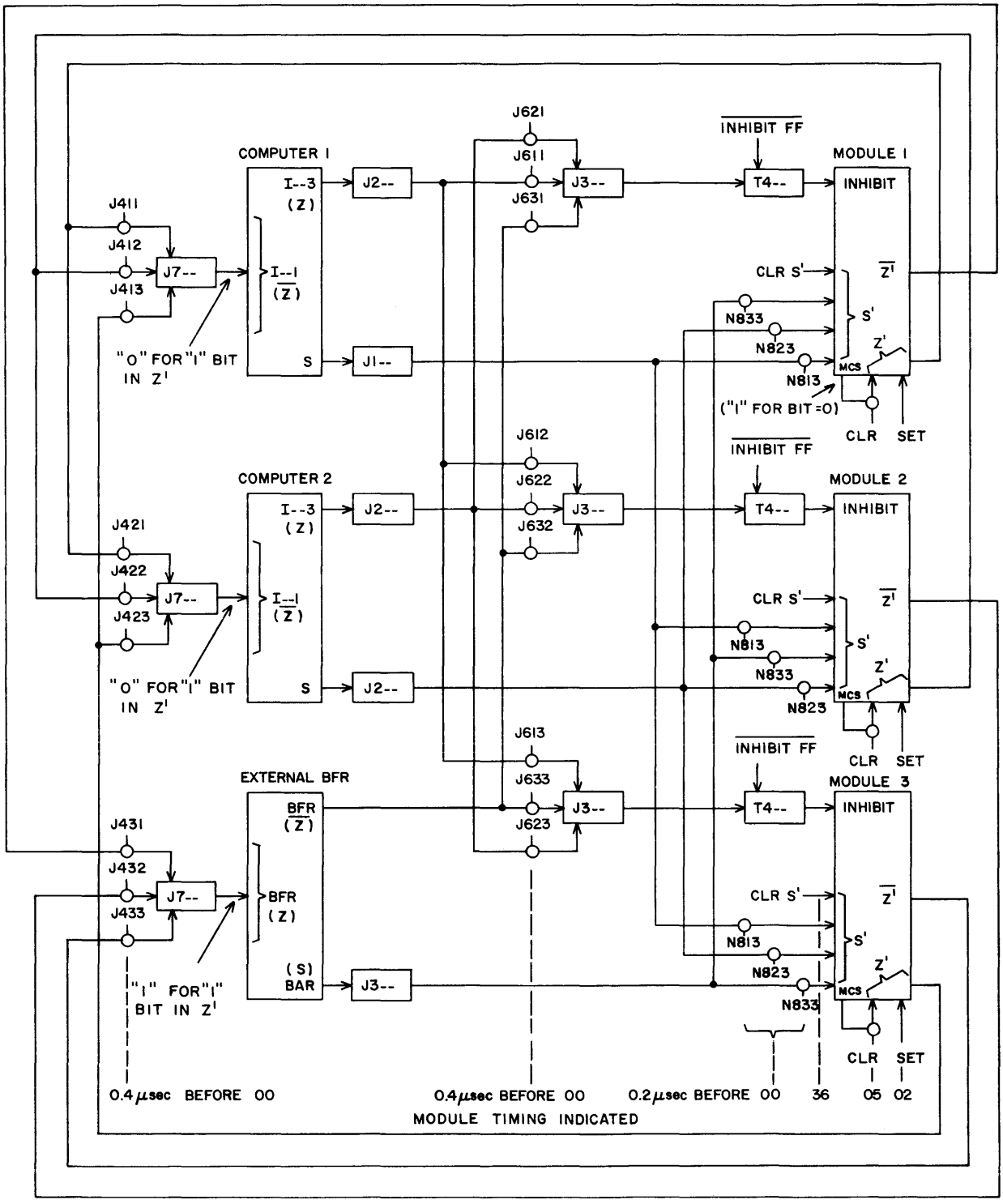


Figure 3-10. Module Gating Control (for 1 bit of 12-bit word)

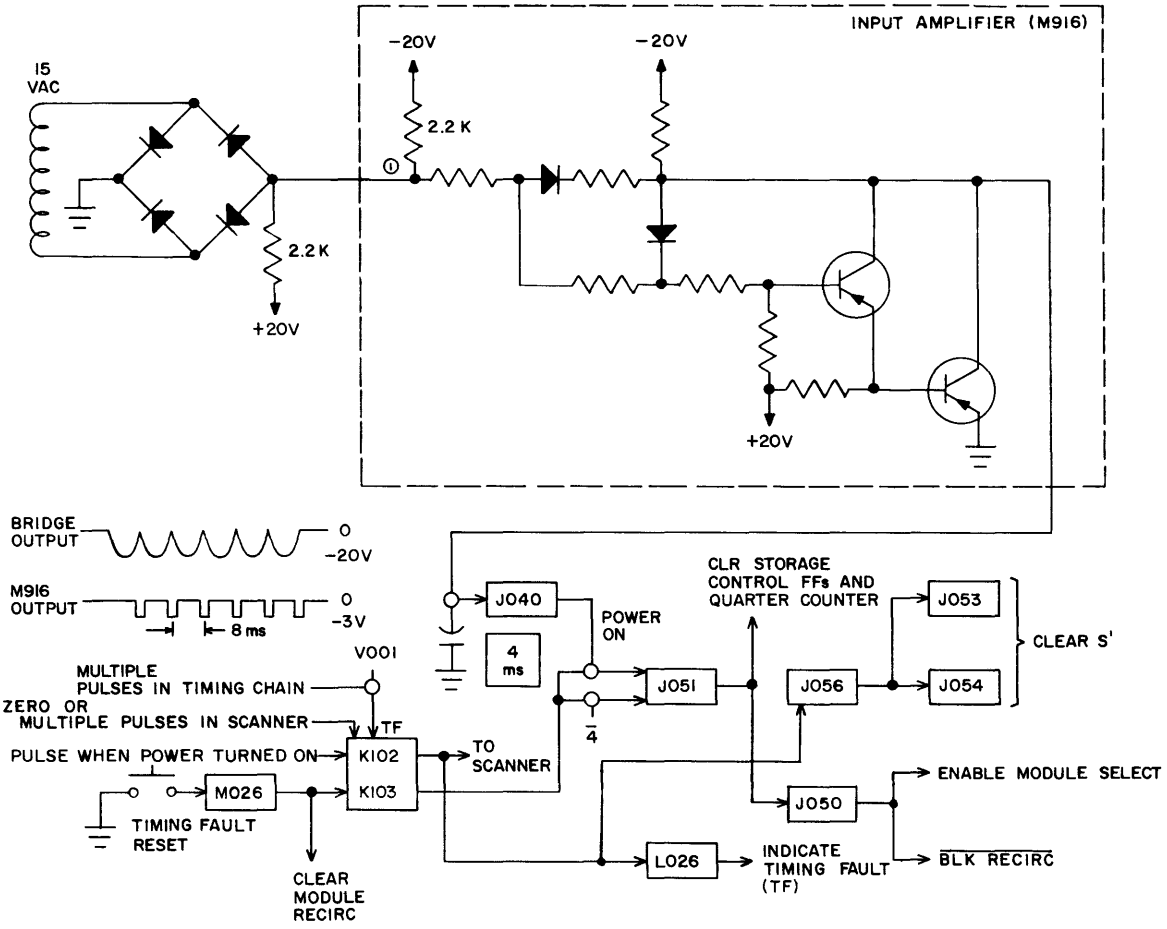


Figure 3-11. Non-Volatile Storage and Timing Fault Circuits

EXTERNAL BUFFER CONTROL

The external buffer is an additional input-output channel. The 160-A selects the I/O operation and section of external memory to be transferred. The external buffer controls generate gating and control signals that transfer data between external memory and peripheral equipment. The external buffer has access to all memory modules except those within the computers.

While the external buffer is operating, the computers are free to perform internal operations, to address other equipments on the normal input-output channel, and to use the regular 160-A buffer channel.

Six EF codes select the external buffer:

Code 4701 selects the buffer mode for an external buffer operation.

Code 4702 clears external buffer controls.

Code 4704 selects BER read to determine the address +1 of the last word buffered.

Code 4710 selects the channel extension mode, allowing the input and output lines to pass through the external buffer without a buffered operation.

Code 4720 clears the channel extension mode.

Code 4740 requests buffer status.

Figure 3-12 shows the transmission paths between 160-A, external buffer, external memory, and peripheral equipment. The second 160-A (not shown) connects to the external buffer in the same way. If two computers are used, they share the buffer unless one computer establishes priority by use of the buffer interrupt. The EF selections described above appear as AND gates in the figure.

If the buffer mode is selected, the 160-A normally sends four control words to the external buffer:

word 1 Information specifying storage bank, input or output operation, terminating or non-terminating buffer, interrupt features.

word 2 Address of first word of data to be transferred.

word 3 Terminating address (last word address + 1) of data to be transferred.

word 4 EF code selecting peripheral equipment.

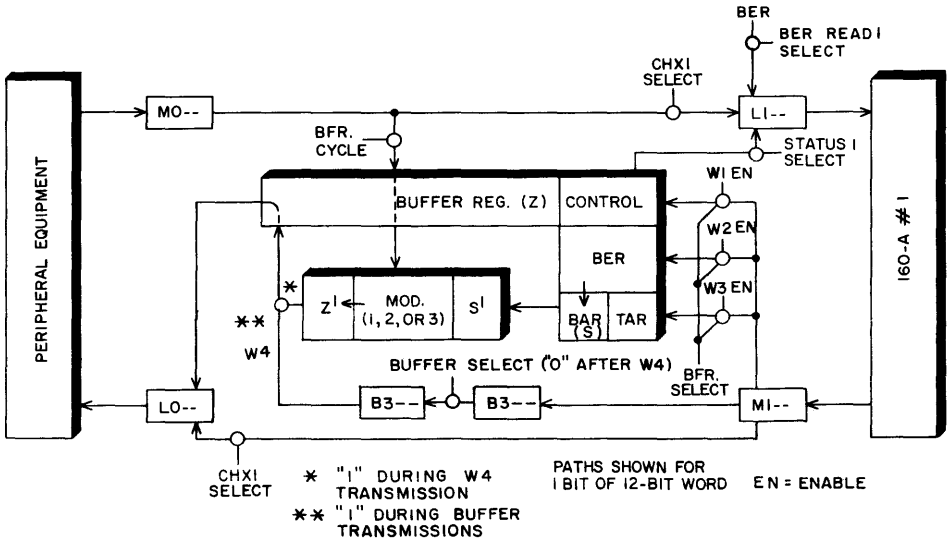


Figure 3-12. External Buffer Transmission Paths

After the four control words enter the external buffer, the buffer controls sequence operations. Because the external memory module reacts to the external buffer as if it were another computer, the Buffer register (BFR) and Buffer Entrance register (BER) replace the computer's Z and S registers for external memory references.

TIMING

For input (peripheral equipment to external memory) and output (external memory to peripheral equipment) operations, the buffer duplicates the computer 6.4 usec timing cycle. Although the buffer timing chain uses only four control delays (figure 3-13), it has the same cycle time as that of the external memory module but, similar to the 160-A, runs one quarter cycle ahead. A free-running resync counter restarts the four-stage buffer timing chain every 1.6 usec. If the buffer mode is selected and the four control words are already processed, the buffer cycle signal starts the quarter counter and provides the quarter translations which condition the timing chain outputs. Counters are reflected binary.

SELECTION

Similar circuits receive selections from computers 1 and 2 (figure 3-14). Resync pulses and interlocks at the input to the select circuits prevent simultaneous selection of both.

When computer 1 selects the external buffer, the function ready signal (FR) waits until resync time to enter select 1 circuit. If computer 2 has just previously (during a time when the buffer was not busy and the select 1 FFs were not set) sent a FR signal, the computer 1 FR signal must wait until that other signal drops.

Status, BER read, and clear buffer controls selections use no delays; other selections use a 1 usec delay (B120 path). Selection through this second path requires that the buffer is not busy and the other computer has not already made a selection. These last two conditions do not hamper status selections or BER read selections which only report on the existing state of the 169 unit and do not change it.

A status or BER read selection causes initial clearing of the Status Select FF and BER Read Select FF. A buffer mode selection or channel extension selection initially clears the Status, BER Read, and Buffer Mode Select FFs.

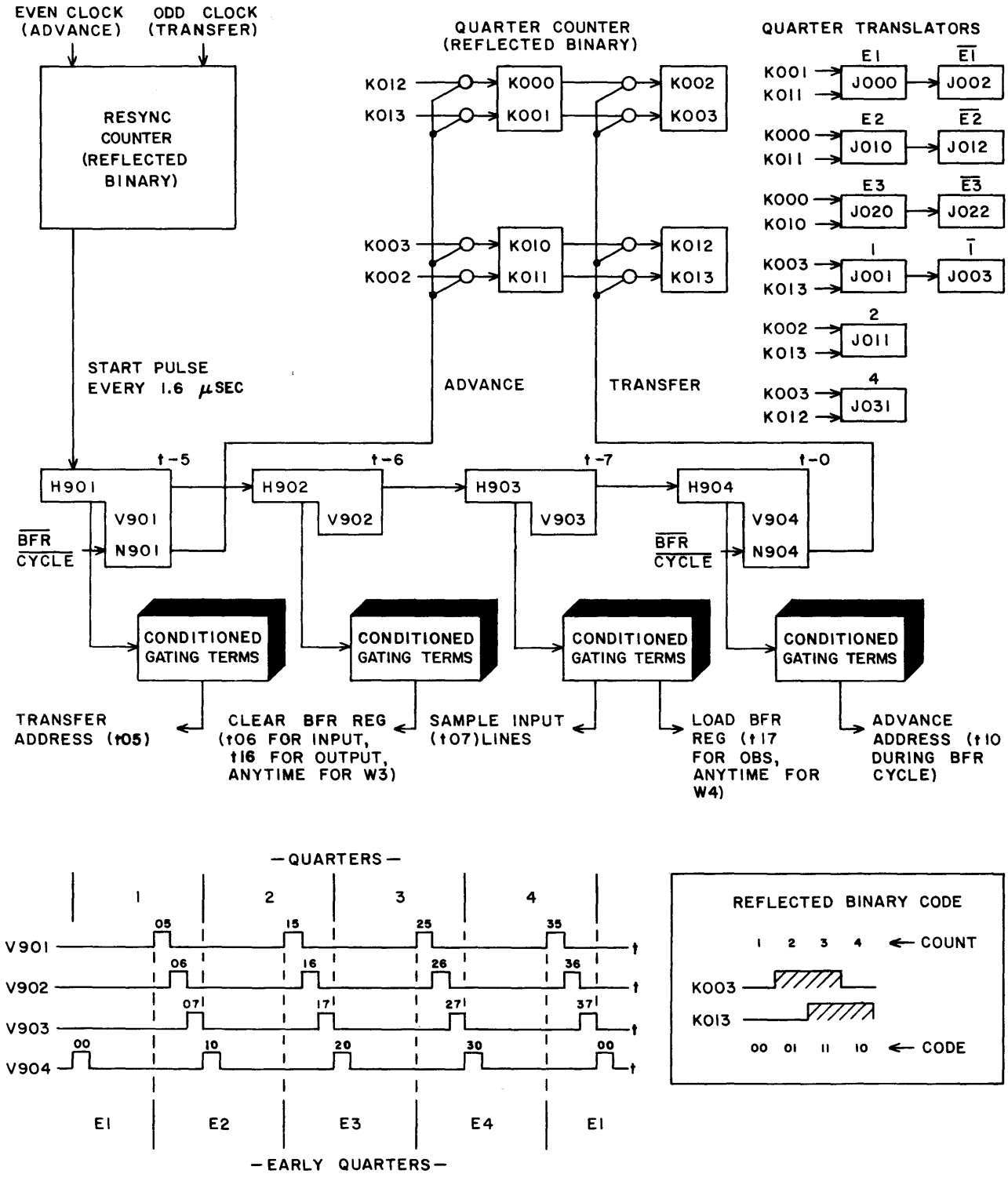


Figure 3-13. External Buffer Timing Controls

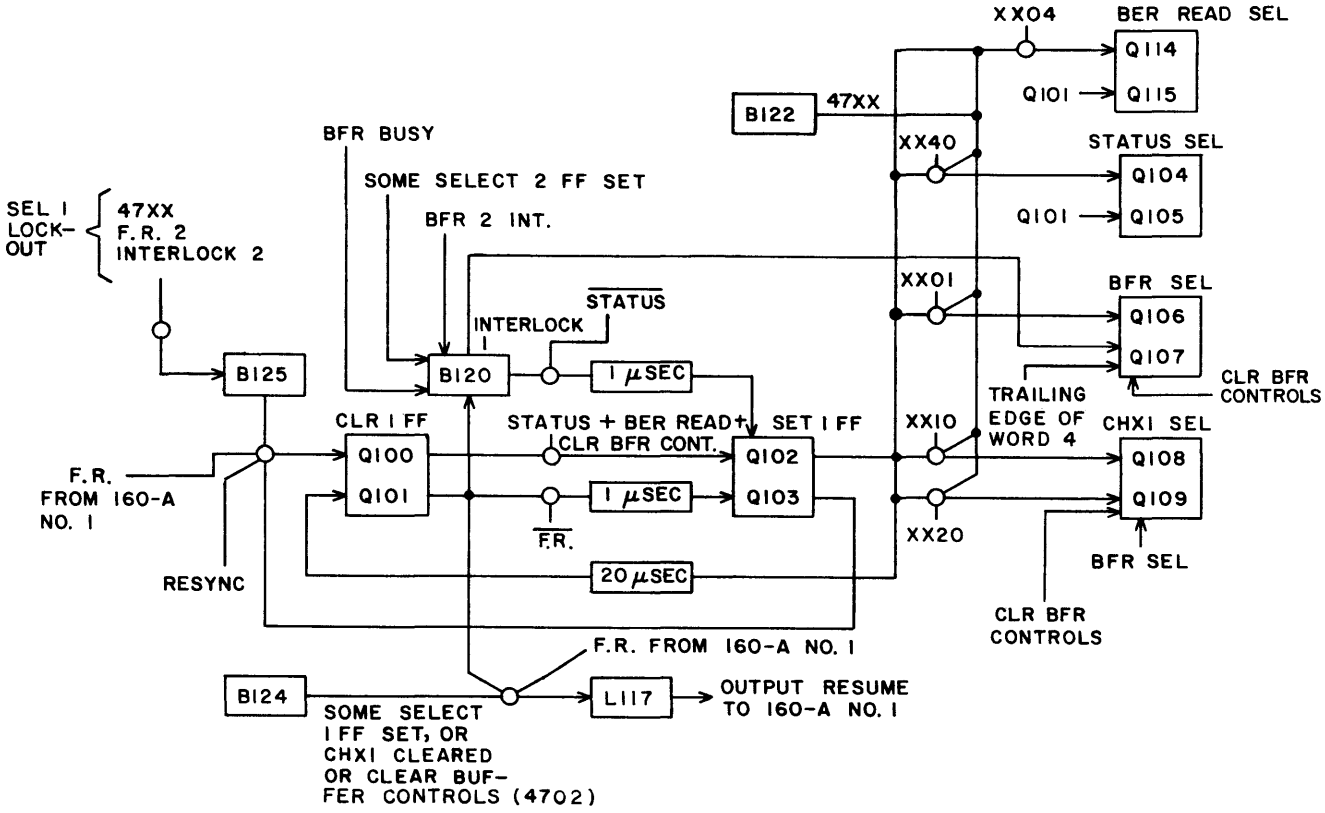


Figure 3-14. External Buffer Select Circuit 1

After a channel extension mode operation, the Channel Extension Select FF (CHX1) requires a special select code or a subsequent buffer mode operation to clear. After a status or BER read operation, the Status or BER Read Select FF remains set until another selection. During a buffer mode operation, the Buffer Select FF clears after the fourth control word prepares the buffer for independent operation.

Twenty usec after a select FF sets, the Clear Select FF clears and an output resume returns to the computer. When the computer drops its function ready indicating that the selection is completed, the circuit can accept another selection.

The clear external buffer controls code is a method of programming the IBA/OBA or Select button. The clear external buffer controls select code does not set a select FF as do the other select codes. Instead, a clear pulse is generated during the interval that function ready and the clear external buffer controls code are present. The duration of this pulse is about 20 usec.

STATUS, BER READ, AND CHANNEL EXTENSION MODE OPERATIONS

Status, BER read, or channel extension selections result in input or output line gating from 169 to 160-A. The status response (figure 3-15) reports control word 1 selections, interrupt conditions, illegal bank selections, and buffer initiation and buffer ready conditions. The channel extension select (figure 3-16) couples external buffer input lines to external buffer output lines so that data bypasses all buffer controls. The clear channel extension select code decouples the lines.

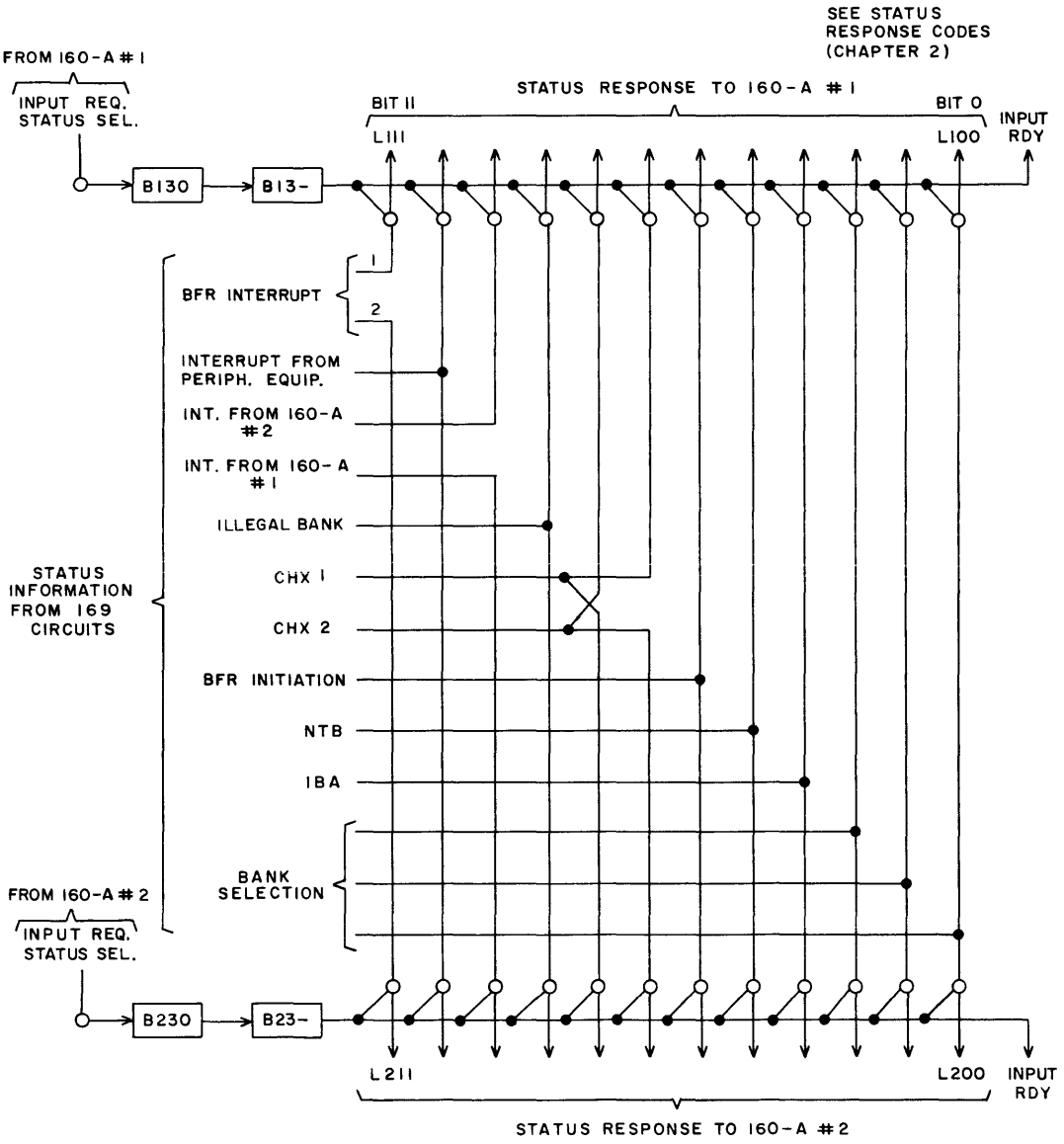


Figure 3-15. Status Response Gating

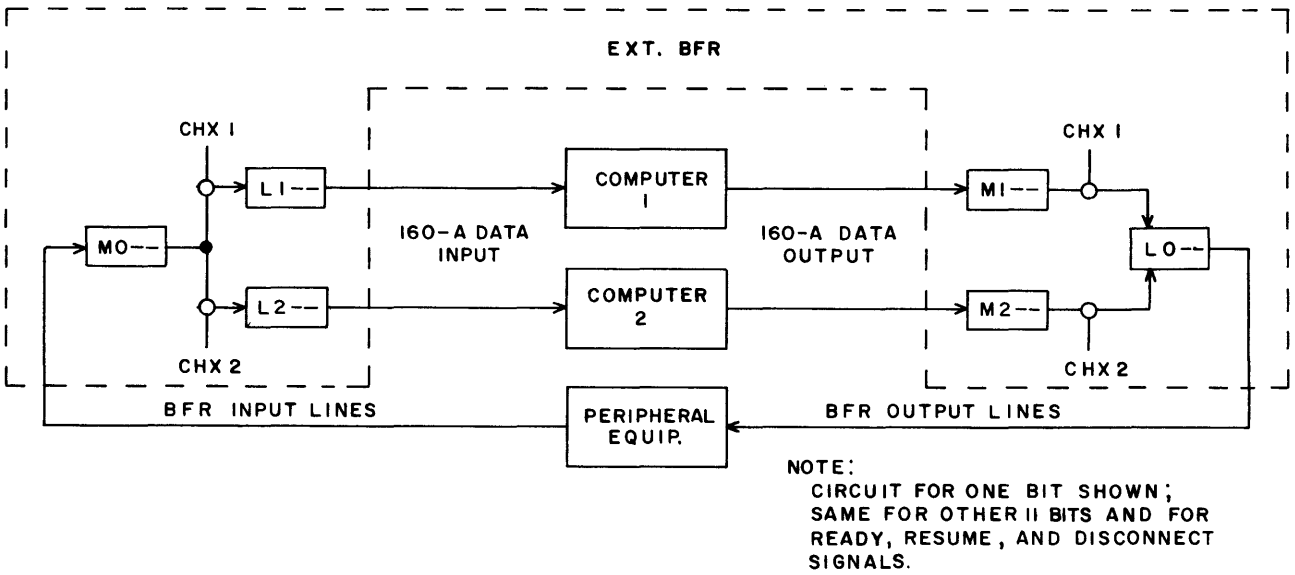


Figure 3-16. Channel Extension Gating

BUFFER MODE OPERATION

Without the 169, only one output or one input equipment can use the 160-A I/O channel at a time. Two equipments can operate simultaneously on one channel if one of them connects via the external buffer. In the buffer mode, the external buffer sequences all buffering. After the 160-A has sent the control words, it can perform further operations as though the 169 were not on the channel.

Control signals select the buffer mode, pass the four control words from the 160-A to the external buffer, and transmit the required number of words between external memory and peripheral equipment (figure 3-17). The ready and resume signals appear as connecting links between the 12-bit parallel transmissions. The equipments are redrawn for each step. Use of this control signal breakdown during the rest of the chapter distinguishes identically-named control signals between the computer and the buffer, and between the peripheral equipment and the buffer.

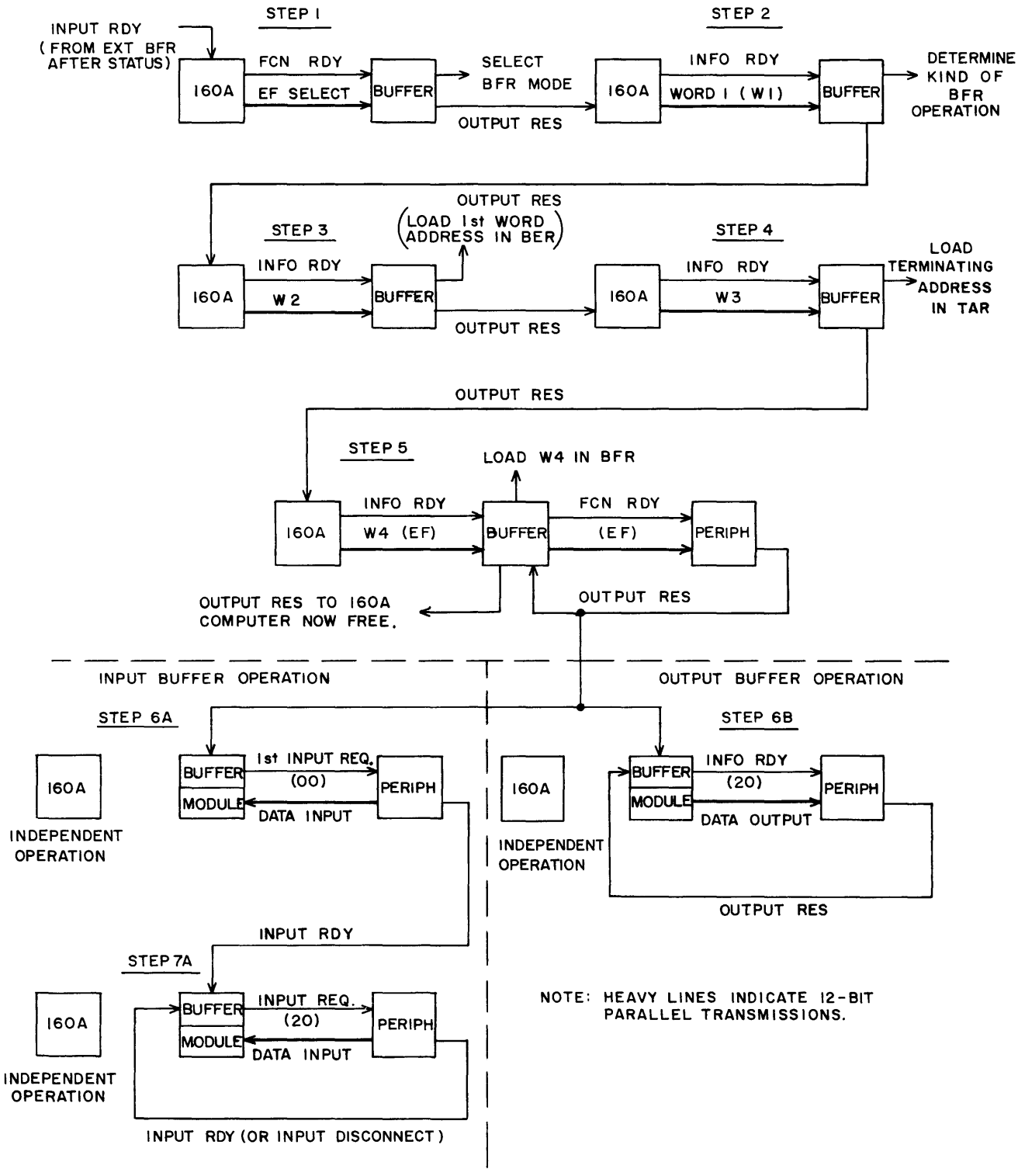


Figure 3-17. Control Signal Sequence for Buffer Mode Operation

CONTROL WORD GATING

The 160-A sends four control words to the external buffer. Inverters B300-B311 (figure 3-18) receive each word. The information ready signal preceding each control word advances a modulus 4 control word counter (WK) which gates the word from the B3-- inverters to the correct registers. The word counter also provides control word circuit clearing signals.

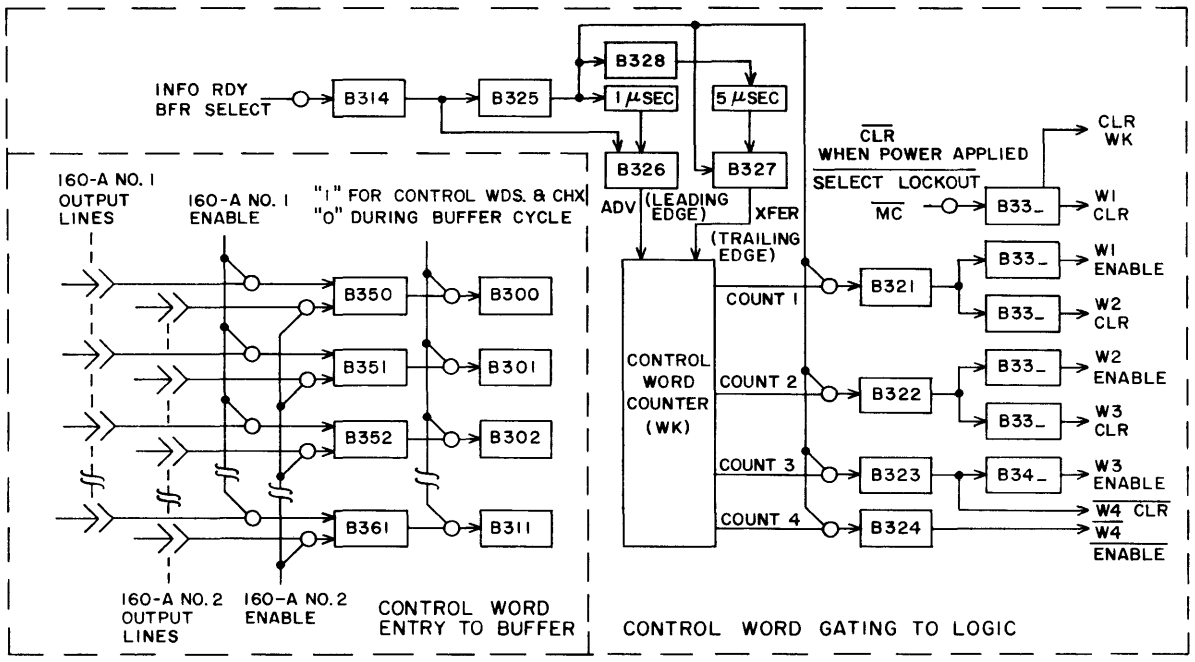
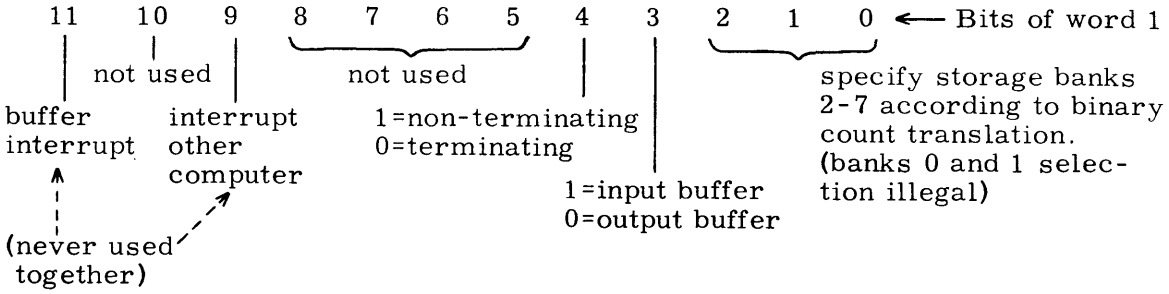


Figure 3-18. Buffer Control Word Gating

WORD 1 CIRCUIT AND INTERRUPT

Control word 1 selects storage bank input or output operation, terminating or non-terminating operation, and interrupt features. The code breakdown for control word 1 is:



Upon receipt of the information ready accompanying word 1, an output resume returns to the computer. At the same time, word 1 sets the FFs of figure 3-19. Outputs from the storage bank FFs go to the external memory. Outputs from the Input Buffer Select (IBS) and Output Buffer Select (OBS) FFs go to the buffer mode data-transfer circuit (figure 3-24) and also generate the buffer busy signal that locks out further selections (figure 3-14). The output from the Non-Terminating Buffer FF (NTB) blocks the comparison of BER and TAR that would terminate the buffer at some specific address.

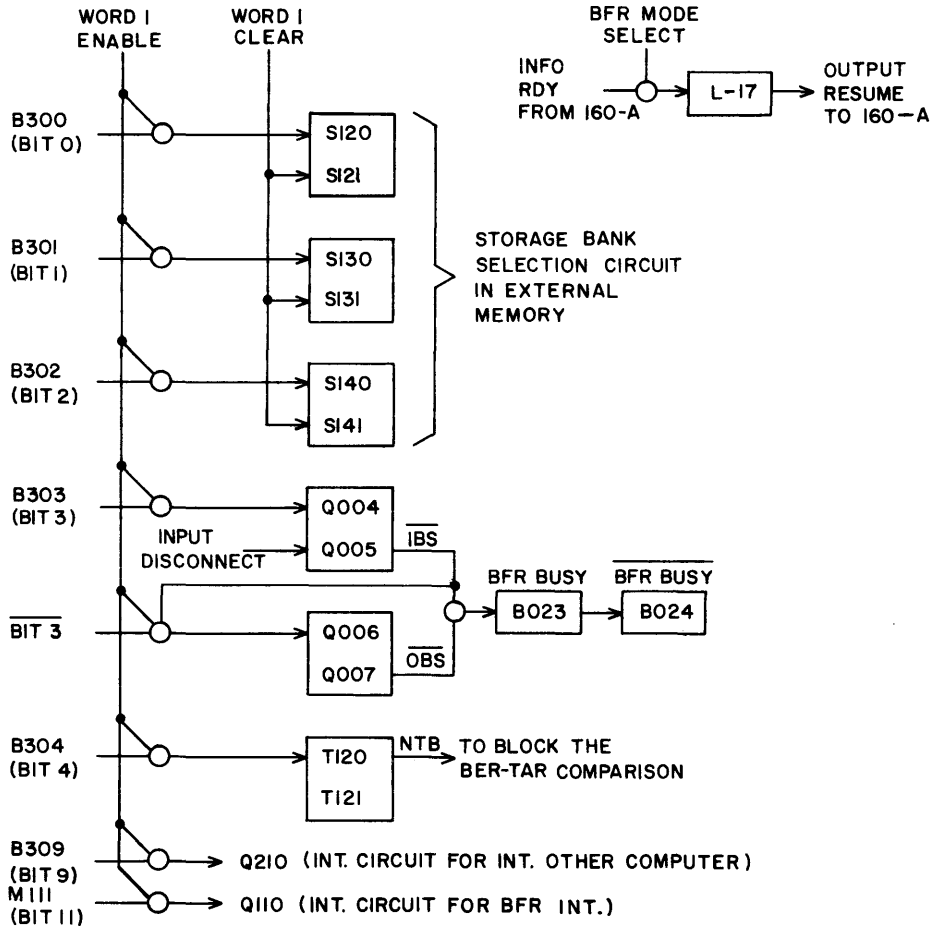
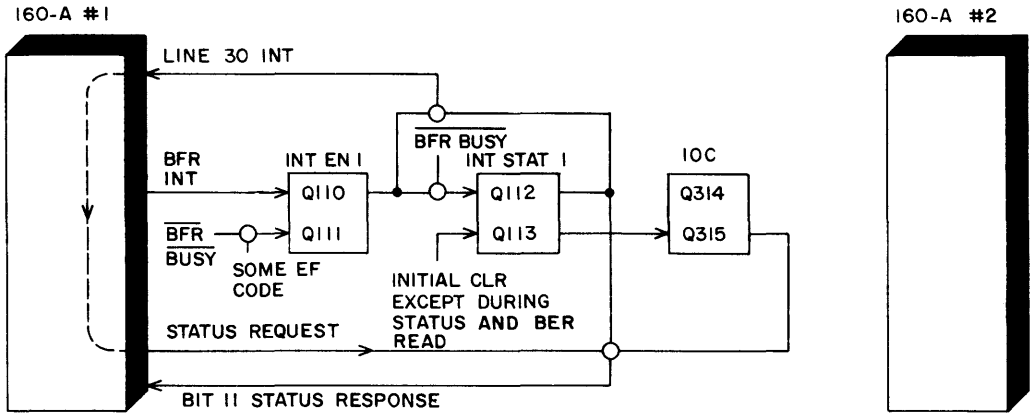
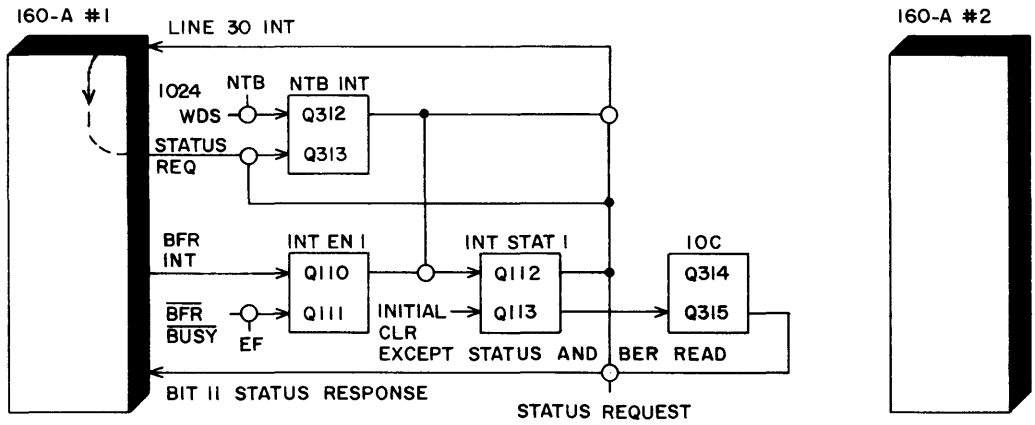


Figure 3-19. Word 1 Circuit

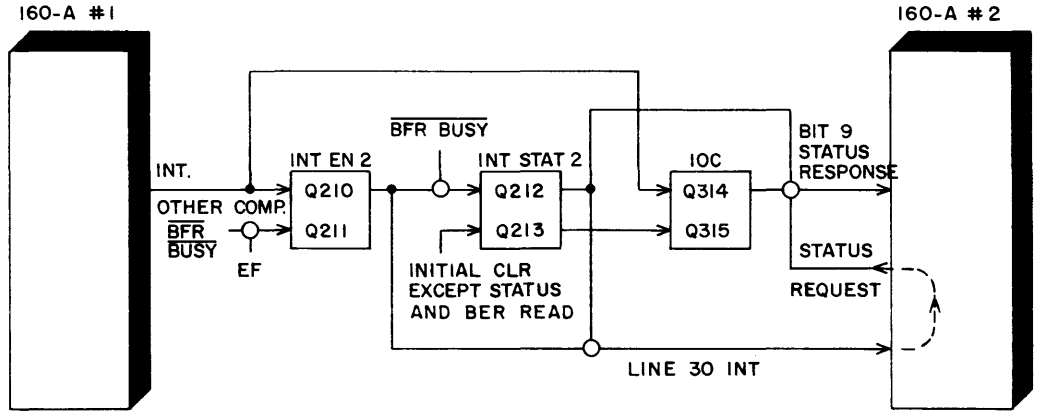
Word 1, bit 11 selects the buffer interrupt. Case 1 (figure 3-20) shows the circuit for this interrupt during a terminating buffer. The Interrupt Status 1 FF waits until the buffer is completed and then returns an interrupt to the computer. The computer can determine the source of the interrupt by a status check.



CASE 1: BFR INTERRUPT, TERM BFR



CASE 2: BFR INTERRUPT, NTB



CASE 3: INTERRUPT OTHER COMPUTER

Figure 3-20. Interrupt Circuits

Case 2 shows the buffer interrupt circuit for a non-terminating buffer. After a block of 1024 words is buffered, the Interrupt Status 1 FF returns an interrupt to the computer. As in case 1, a status check evokes a bit 11 status response.

Word 1, bit 9, selects the interrupt other computer (case 3). The Interrupt Status 2 FF immediately sends an interrupt to the other computer. A status check by that computer results in a bit 9 status response. To interrupt the other computer, only bit 9 in control word 1 should be a "1". The remaining three control words should not be transmitted to the 169. Instead, the external buffer should be cleared by a clear channel extension selection. (See chapter 2 for sample programs.)

WORD 2 AND WORD 3 CIRCUITS AND BER READ

Control word 2 provides the external buffer with the address used for storing the first input word or for reading the first word for output. This word enters the Buffer Entrance register (BER), and passes from there to the Buffer Address register (BAR) and to the S' register of the external memory (figure 3-21). Control word 3, the terminating address (last address + 1) of the data to be buffered, enters the Terminating Address register (TAR). After control word 4 is processed and the buffer operation begins, a BAR→BER transfer advances the count of the word address during each buffer cycle. Unless the non-terminating feature has been selected, the buffer mode operation stops when the bit-for-bit comparison circuit (figure 3-21) finds BER=TAR.

A BER read operation gives the computer the address of the last word buffered + 1. The Address Hold register (AHR, figure 3-22) stores the contents of BER. The BER read enable drops the load input to AHR after a 1 usec delay necessary to complete the AHR feedback loop, and then gates the output of AHR to the computer. This enable is locked out during the critical time 10 when BER is advanced every buffer cycle, or during or immediately following a BER read operation by the other computer.

AHR is loaded for a 1 usec interval during the first quarter (00-07). This prevents error if a read enable occurs prior to the lockout at time 05. Without this special storage of the contents of BER, the 160-A could read an unstable state of BER.

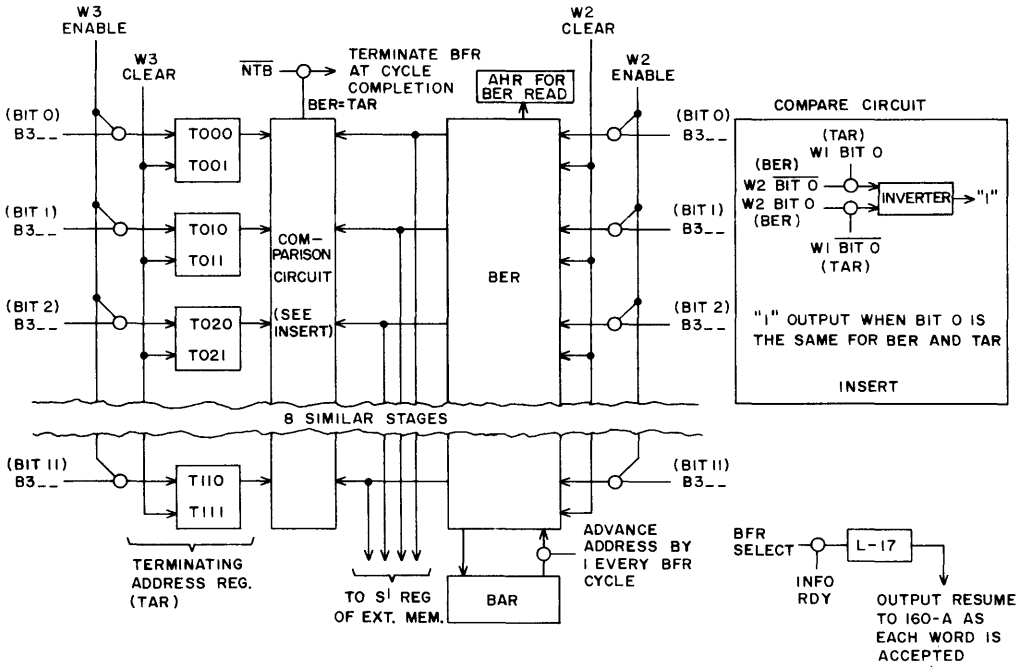


Figure 3-21. Word 2 and 3 Circuits

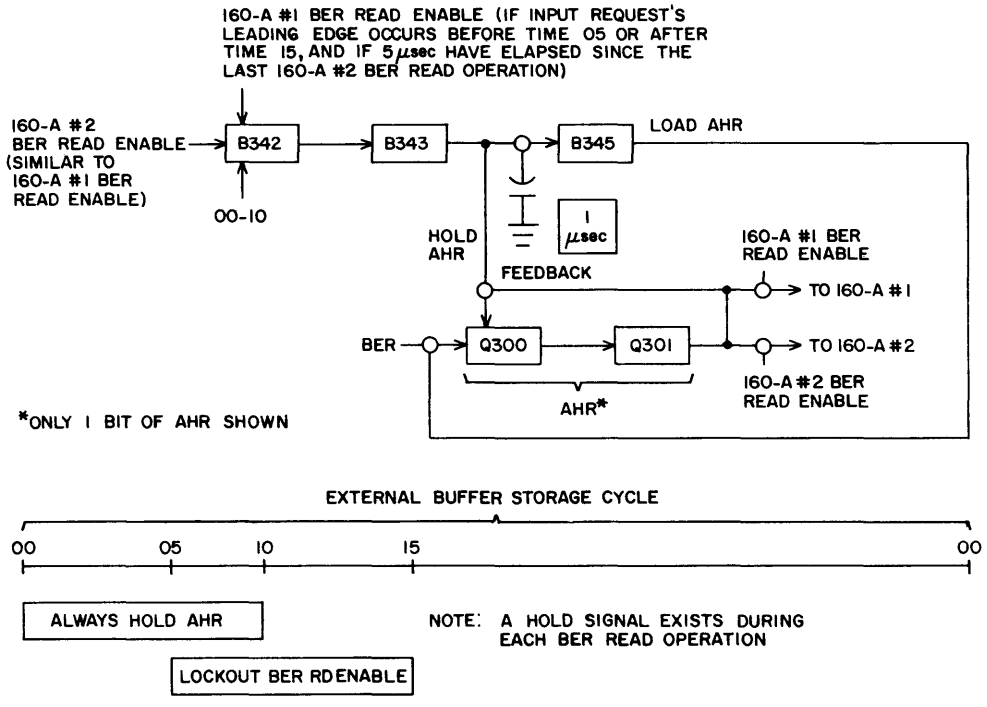


Figure 3-22. BER Read Controls

WORD 4 CIRCUIT

Control word 4 sends the peripheral equipment EF code (figure 3-23) to the Buffer register (BFR). The W4 enable transmits this code and function ready to the peripheral equipment. From this point on, transmissions between external memory and the peripheral equipment through the external buffer are independent of the 160-A. The peripheral equipment returns an output resume to the external buffer resync circuit, starting the buffer sequence and dropping the EF code and function ready.

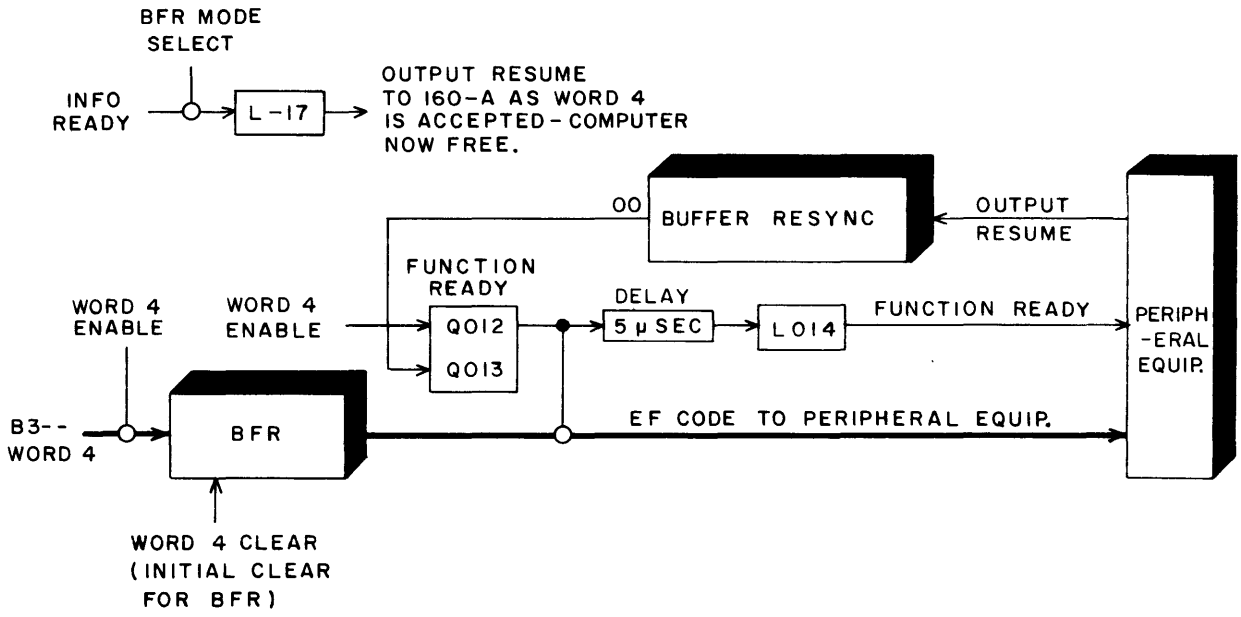


Figure 3-23. Word 4 Circuit

DATA GATING

Before the buffer sequence, the first control word has set the Input Buffer Select FF (IBS) or the Output Buffer Select FF (OBS) selecting input or output circuits (figure 3-24). Either circuit gates the data lines between external memory and peripheral equipment and supplies the information ready (output operation) or input request (input operation).

For a buffer input, the Input Request FF first sets when an output resume is received in response to the function ready (figure 3-24). This FF sends an input request for the first data transmission from peripheral equipment to external memory. At external buffer time 07 the data then transfers to the Buffer register. The next and all subsequent input requests occur at time 20.

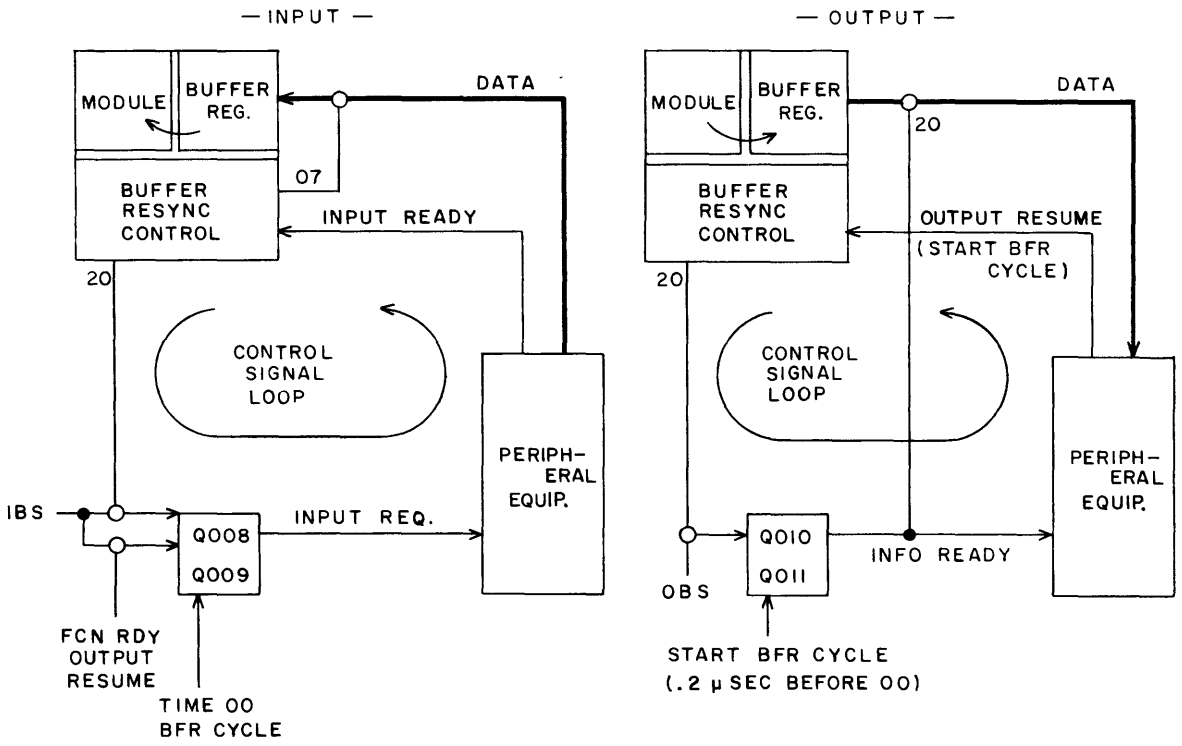


Figure 3-24. Buffer Mode Data Transfer

In the case of a buffer output, all information ready signals occur at the same time because the buffer initiates output data transfer. Data always gates from the external memory via the buffer register to the peripheral equipment at time 20.

The buffer resync circuit receives the ready or resume from the peripheral equipment after each transmission, and initiates a new buffer cycle. This resync circuit continues the control signal loop for both input and output buffer transfers until the sequence is finished.

RESYNC CIRCUIT

The resynchronization circuit (figure 3-25) synchronizes ready or resume signals generated outside the external buffer with the buffer clock.

The Enable FF prevents the same ready or resume from entering the resync circuit twice. This FF is set by the non-active state of the ready, resume, or input disconnect signals from the peripheral equipment. The input disconnect is a ready signal indicating the peripheral equipment has no more data to transmit.

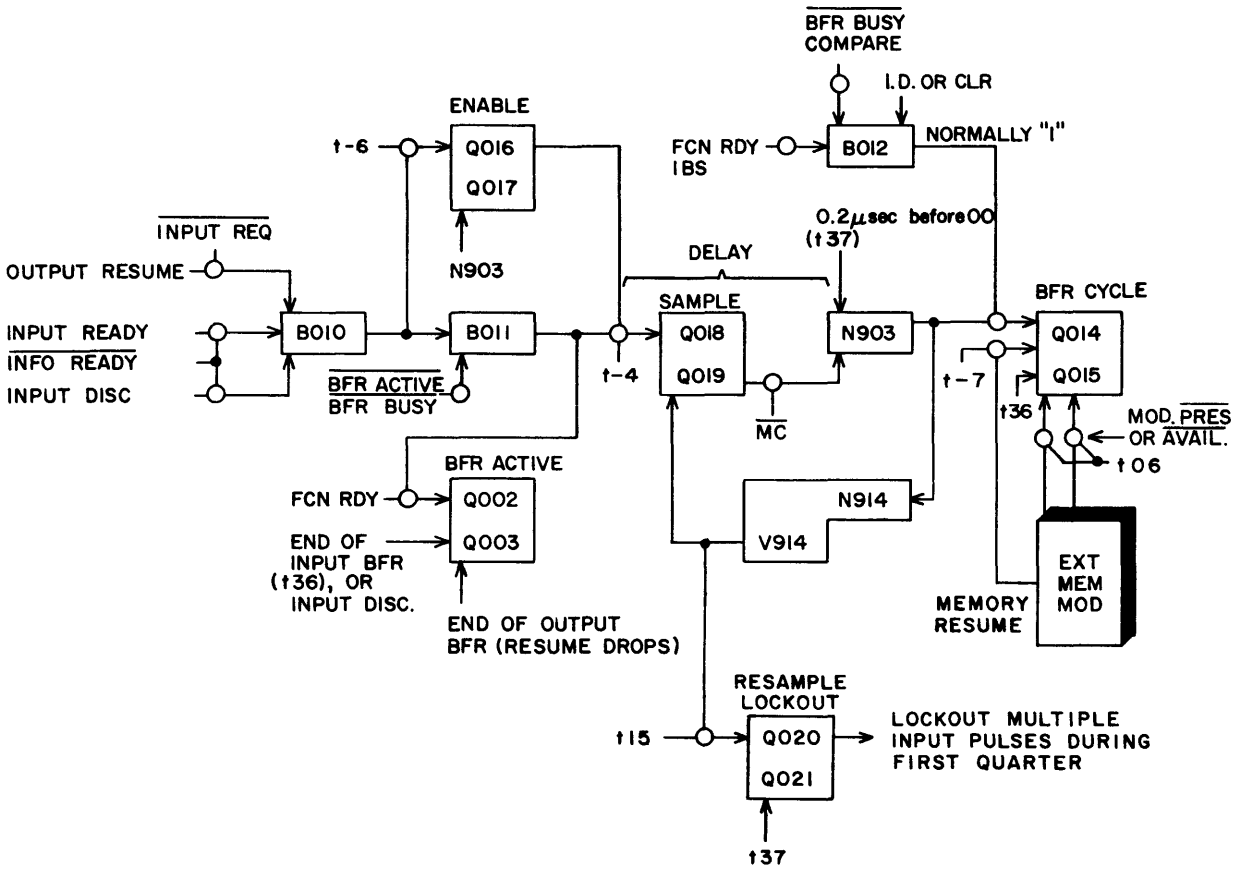


Figure 3-25. External Buffer Resync Circuit

If the Enable FF is set during a buffer mode operation, a ready or resume signal sets the Sample FF at a resync time (every 1.6 usec). After a delay to allow decay of noise and runt pulses, N903 transmits the Sample FF output to set the Buffer Cycle FF which starts the buffer timing chain. This FF normally clears after each word is buffered (time 36).

The Buffer Cycle FF clears at time 06 if the selected external memory module is not present. It also clears at this time if the module is busy, but resets 0.2 usec before time 10 when the module scanner selects the buffer.

The Buffer Active FF sets at the start of a buffer operation and remains set until the operation is completed.

When the Buffer Cycle FF clears due to a busy module, the buffer timing cycle remains in its first quarter but the free running timing chain recycles every 1.6 usec. The Resample Lockout FF sets after the first t-7 input sample pulse generated by the buffer timing chain. This FF locks out all subsequent input sample pulses during the extended first quarter.

MODULE AND EXTERNAL BUFFER RESETS

A timing fault clears the scanner FFs, quarter counter, and four storage control FFs of a module. When a Timing Fault indicator lights, press the indicator to reset (master clear) the timing fault circuits of the external module. A timing fault occurs when:

Power is turned on.

There is no pulse in the scanner and in the timing chain (under normal operation, when the scanner stops, the timing chain starts).

There are multiple pulses in the scanner or timing chain.

The external buffer controls are cleared manually with the 169 IBA/OBA or Select switches. The controls are also cleared by EF code 4702. The clear affects the buffer quarter counter, the Buffer Cycle and Buffer Active FFs, the buffer select circuit, interrupt circuit, and input-output controls. The manual clears, but not the EF code, send a clear to the peripheral equipment.

The 160-A master clear clears the interrupt controls for that computer if the buffer is not busy, and during channel extension operations, sends a master clear to the peripheral equipment.

TIMING

Figure 3-26 gives the major timing signals for the 169. The figure shows all data transfers in their time relationship to the 6.4 usec storage reference cycle. The module timing chain is contrasted with that of the selecting device (160-A computer or external buffer). The example shows an arbitrary 3.2 usec delay between selection of the module by the device and the selection completion by the module available signal.

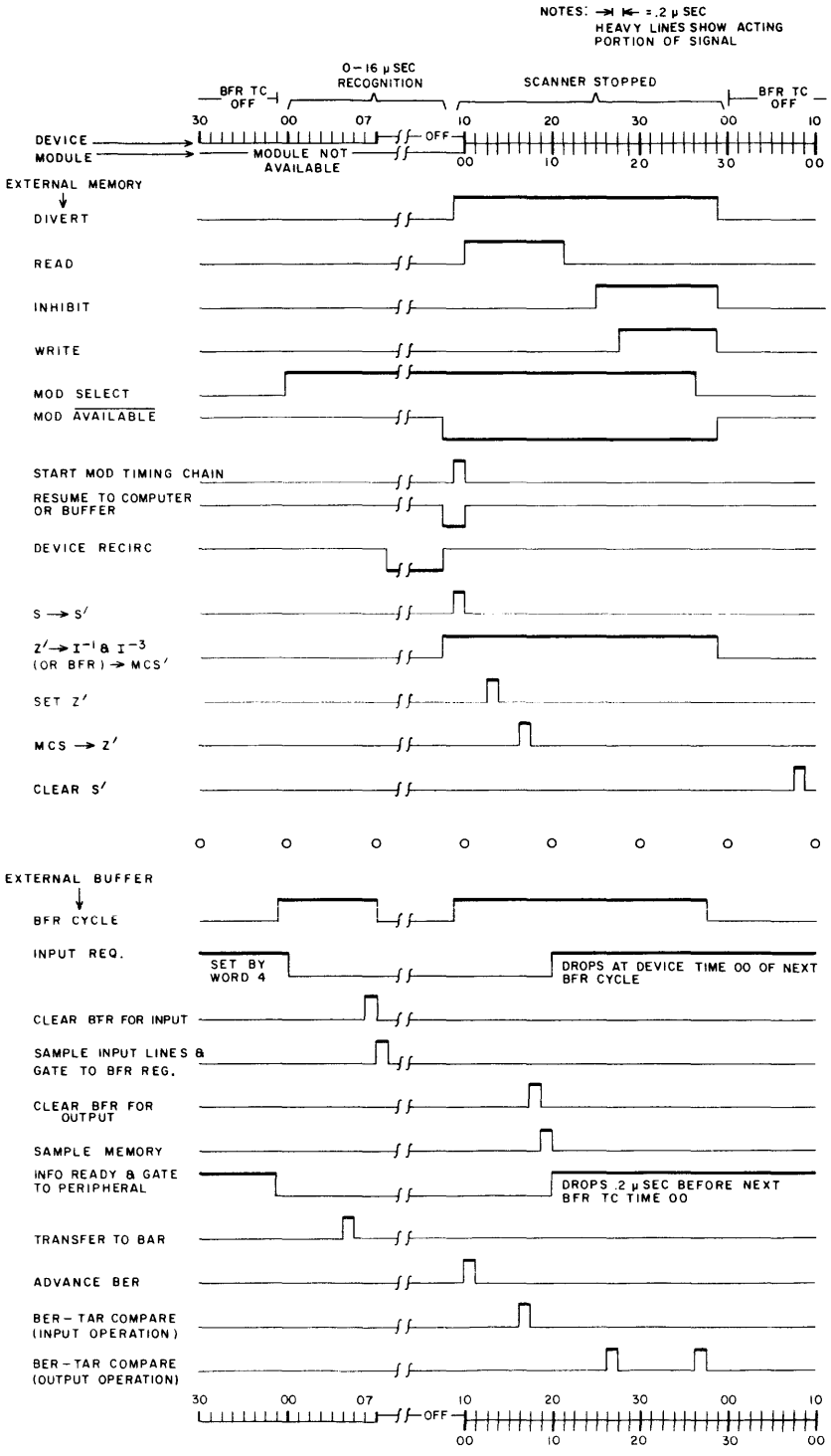


Figure 3-26. 169 Timing Chart

CHAPTER 4

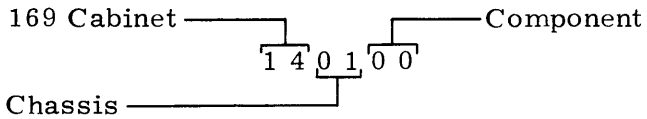
MAINTENANCE

System maintenance requires knowledge of 169 logic, familiarity with 160-A circuit diagnostic techniques, and use of certain maintenance aids.

169 LOGIC	MAINTENANCE AIDS	160-A DIAGNOSTIC TECHNIQUES
Equation File Logic Diagrams Principles of Operation Appendix B (Electronic Memory Cards) 151 Card Tester Manual (logic cards)	Standard VOM Oscilloscope [Tektronix 543 or equivalent with type CA preamplifier or Tektronix 317 with "T" adapter IPC No. 10,000 and two Tektronix 543 probes (010-038)] 151 Card Tester Taper Pin crimping and insertion tools Bulb insertion and extraction tool Microswitch Lamp Tool, Type 15 PA19 Usual hand tools for mechanical and electrical maintenance	Control Data 160-A Computer manual, volume 2: Maintenance 160-A Installation

COMPONENT NUMBERING SYSTEM

The 169 uses the hundred-thousandths system to designate cabinet, chassis and component.



One of the following component identification symbols usually accompanies the component number:

K	Relay	J	Jack
DS	Indicator	B	Blower
S	Switch or thermostat	E	Terminal E strip
F	Fuse	PS	Power supply

When identifying components by means of frame labeling, drawing designations, or photographic call-outs, the shortest designator is used, consistent with clearness. In addition to the full length designation (J140102, for example) two shorthand methods are employed. The first method describes components by prefixing a chassis number to the component designator. This is used where there might be some confusion as to the number of a chassis carrying the particular component: 1J02.

The second shorthand system applies when the chassis to which the component is attached is clearly identifiable. This is used to label component locations on cabinet and chassis frames: J02.

Components such as blowers which are mounted within a cabinet but not on a chassis carry the prefix "0", either expressed or implied: (0)B01.

The 169 cabinet contains nine chassis (figures 4-1 and 4-2):

Chassis No.	Use
140100	Module 1
140200	Control and Buffer
140300	Module 3
140400	Module 2
140500	Power supply for chassis 140100 and 140200 (and 140400 for 16,384 word memory)
140600	Power supply for chassis 140300 and 140400 (24,576 word memory)
140700	Switch panel
140800	Connector panel
140900	Power panel

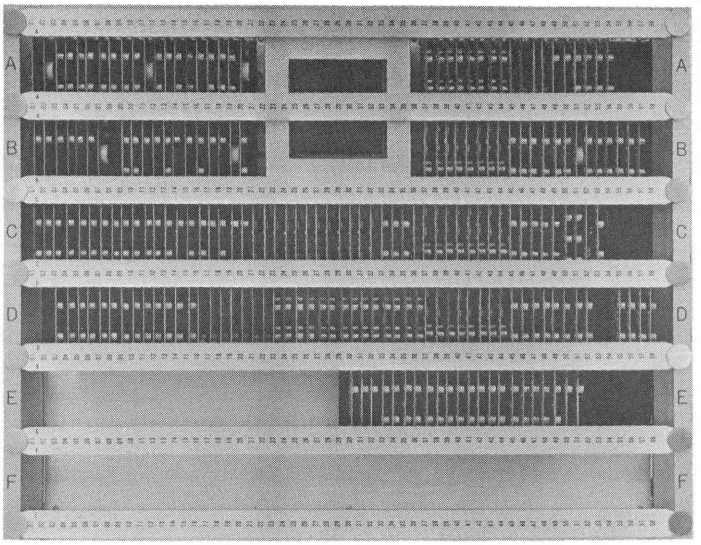


Figure 4-1. Module Chassis

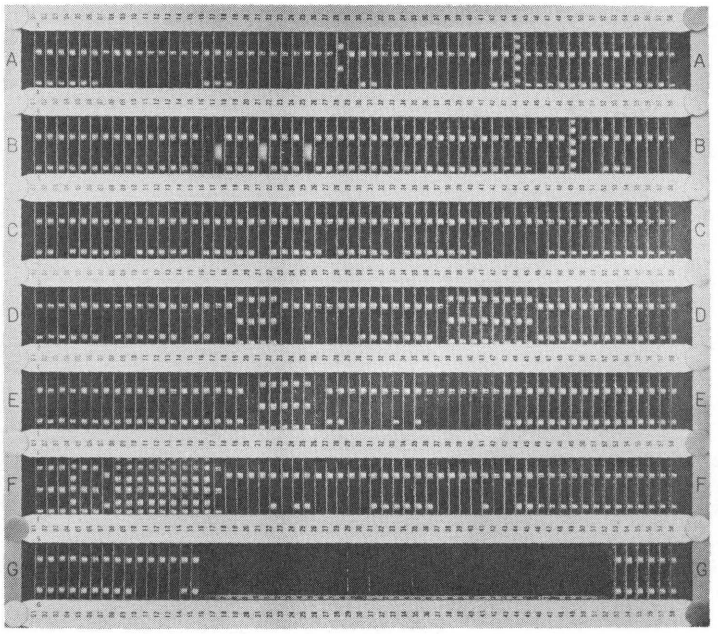


Figure 4-2. Control Chassis

AC POWER DISTRIBUTION*

The a-c power distribution (figure 4-3) uses 115 vac, DPDT relays to turn on the blowers when input power is applied to the d-c power supplies. Power supply number 1 connects to chassis 140100 and 140200. If one additional memory module is used, power supply number 1 also connects to chassis 140400. If two additional memory modules are used, power supply number 2 connects to chassis 140300 and 140400. Two thermostats suspended from the cabinet ceiling turn off all power is overheating occurs.

Power to the 169 may be turned on and off from the computer by connecting the controlled a-c line from the 160-A to the controlled a-c line of the 169 at an external power panel. If this is done, the 169 Power switch must be left in the OFF position, and care must be taken to connect the 160-A and 169 to the same phase of the a-c line.

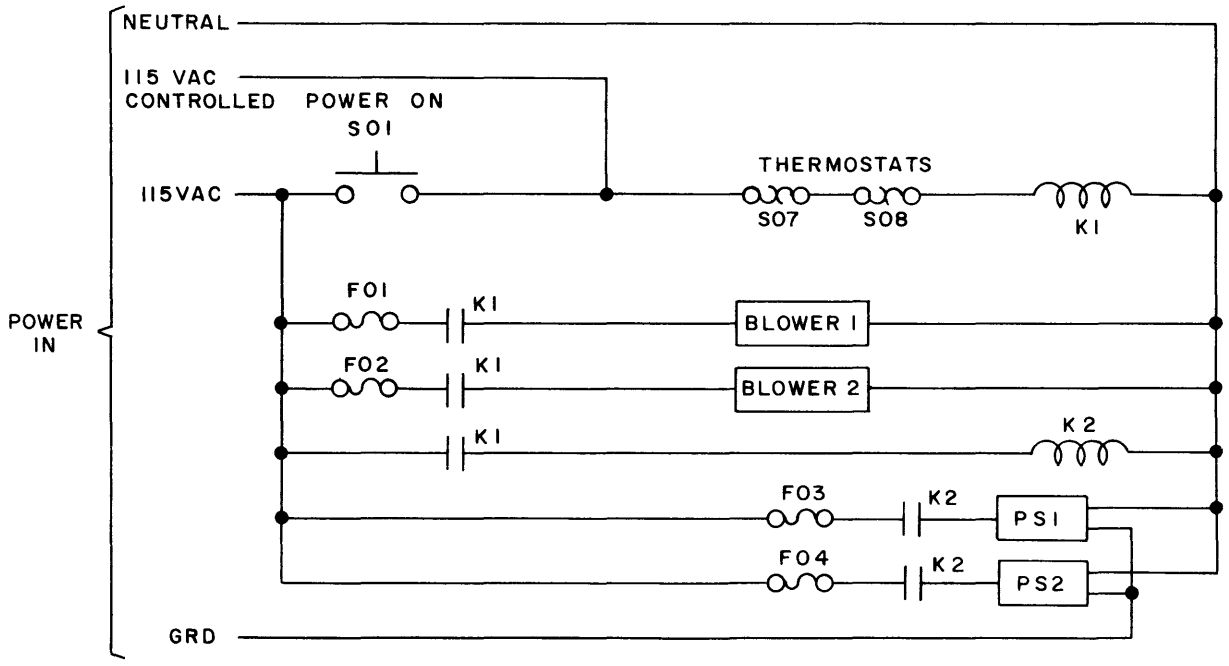


Figure 4-3. AC Power Distribution

* A separate manual describes the d-c power supply.

TABLE 4-1. REPLACEABLE FUSES

NO.	CHASSIS	RATING	TYPE	PROTECTS
F01	140900	2 1/2 amp slo-blo	MDX or 3AG	blower 1
F02	140900	2 1/2 amp slo-blo	MDX or 3AG	blower 2
F03	140900	15 amp	ABC	power supply #1
F04	140900	10 amp	ABC	power supply #2

COOLING

All blowers and fans use grease-sealed ball bearings and require no maintenance for the life of the machine. Clean filters weekly. Total heat generated by the 169 is: 4700 BTU/hr, 8K memory; 5600 BTU/hr, 16K memory; 6500 BTU/hr, 24K memory.

APPENDIX A

CABLE PIN ASSIGNMENTS

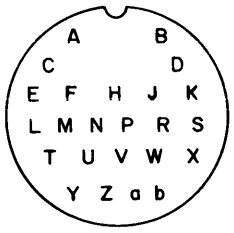
All signal cables are 24 TP (twisted pair) terminated by 24 pin Amphenol connectors. Appendix A gives the signal carried by each pin. If the external buffer is on the 160-A buffer channel, the buffer channel connectors replace the I/O channel connectors. The power cable is 3 wire connecting to 5 pin Amphenol connector.

The 169 uses three basic cable groups:

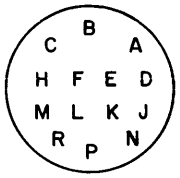
A - cables to module (6 cable types)
B - 160-A memory cables (3 cable types)
C - external buffer cables (2 cable types)

There are 18 cables in group A, 6 cables in group B, and 12 cables in group C. Tables A-1, A-2, and A-3 give the pin assignments.

The pin arrangements for the logic and power connectors are:



24 pin logic connector



(PIN SIDE OF PLUGS WIRING SIDE OF RECEPTACLES)

14 pin power connector

Pin-to-pin jumpering between adjacent connectors permits connection of more than one equipment to the inputs or outputs.

For cable group B, use cables with maximum length of 15 feet, assuming 13.5 microfarad capacitance per cable foot. Interface logic cables can have a maximum length of 75 feet.

TABLE A-1. PIN ASSIGNMENTS, CABLE GROUP A
(CABLE TYPES A-1 TO A-6)

CABLE TYPE A-1 (three cables)			
2J01 ---------- 1J01 2J06 ---------- 4J01 2J13 ---------- 3J01			
PIN	FUNCTION	PIN	FUNCTION
A	resync from 160-A #1	P	resume to 160-A #1
B	resync from 160-A #2	R	resume to 160-A #2
C	resync from ext bfr	S	resume to ext bfr
D	even clock	T	mod $\overline{\text{present}}$ to 160-A #2
E	odd clock	U	mod $\overline{\text{present}}$ to ext bfr
F	MTF	V	mod $\overline{\text{present}}$ to 160-A #1
H	manual reset	W	160-A #2 $\overline{\text{present}}$
J	160-A #1 $\overline{\text{present}}$	X	banks 4, 5, 6, 7 select from ext bfr
K	mod available to 160-A #1	Y	bit 11 $S_2 \rightarrow S'$
L	mod available to 160-A #2	Z	bit 3 $Z' \rightarrow$ BFR
M	mod available to ext bfr	a	bit 11 $Z' \rightarrow$ BFR
N	non-volatile memory	b	ground

TABLE A-1. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE A-2 (three cables)			
2J02 ---------- 1J02 2J07 ---------- 4J02 2J14 ---------- 3J02			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 BER → S'	P	odd bank select from 160-A #1
B	1	R	odd bank select from 160-A #2
C	2	S	odd bank select from ext bfr
D	3	T	$\overline{1}$, E1 from 160-A #1
E	4	U	banks 2, 3, 6, 7 select from 160-A #1
F	5	V	banks 4, 5, 6, 7 select from 160-A #1
H	6	W	$\overline{1}$, E1 from 160-A #2
J	7	X	banks 2, 3, 6, 7 select from 160-A #2
K	8	Y	banks 4, 5, 6, 7 select from 160-A #2
L	9	Z	$\overline{1}$, E1 from ext bfr
M	10	a	banks 2, 3, 6, 7 select from ext bfr
N	11	b	ground

TABLE A-1. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE A-3 (three cables)			
2J03 ---------- 1J03 2J08 ---------- 4J03 2J15 ---------- 3J03			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 S_1 → S'	P	Bit 0 S_2 → S'
B	1	R	1
C	2	S	2
D	3	T	3
E	4	U	4
F	5	V	5
H	6	W	6
J	7	X	7
K	8	Y	8
L	9	Z	9
M	10	a	10
N	11	b	ground

TABLE A-1. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE A-4 (three cables)			
2J04 ---------- 1J04 2J09 ---------- 4J04 2J16 ---------- 3J04			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 Z → Mod'	P	Bit 0 Z' → I^{-1} (160-A #1)
B	1	R	Bit 0 Z' → I^{-1} (160-A #2)
C	2	S	Bit 0 Z' → BFR (ext bfr)
D	3	T	1 (160-A #1)
E	4	U	1 (160-A #2)
F	5	V	1 (ext bfr)
H	6	W	2 (160-A #1)
J	7	X	2 (160-A #2)
K	8	Y	2 (ext bfr)
L	9	Z	3 (160-A #1)
M	10	a	3 (160-A #2)
N	11	b	ground

TABLE A-1. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE A-5 (three cables)			
1J05 ---------- 2J05 4J05 ---------- 2J10 3J05 ---------- 2J17			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 4 $Z' \rightarrow I^{-1}$ (160-A #1)	P	8 (160-A #1)
B	Bit 4 $Z' \rightarrow I^{-1}$ (160-A #2)	R	8 (160-A #2)
C	Bit 4 $Z' \rightarrow$BFR (ext bfr)	S	8 (ext bfr)
D	5 (160-A #1)	T	9 (160-A #1)
E	5 (160-A #2)	U	9 (160-A #2)
F	5 (ext bfr)	V	9 (ext bfr)
H	6 (160-A #1)	W	10 (160-A #1)
J	6 (160-A #2)	X	10 (160-A #2)
K	6 (ext bfr)	Y	10 (ext bfr)
L	7 (160-A #1)	Z	11 (160-A #1)
M	7 (160-A #2)	a	11 (160-A #2)
N	7 (ext bfr)	b	ground

TABLE A-1. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE A-6 (three cables)

Origin (direct wiring)	Terminating Connector
power supply 1	1J06
power supply 1	2J12
power supply 1	(16K-4J06)
power supply 2	4J06 } 24K
power supply 2	3J06 } 24K

PIN	FUNCTION	PIN	FUNCTION
A	-20v	J	+20v
B	-20v	K	+20v sense
C	-20v	L	NVM, 15 vac
D	-20v	M	NVM, 15 vac
E	-20v sense	N	ground
F		P	ground
H	+20v	R	sense ground

TABLE A-2. PIN ASSIGNMENTS, CABLE GROUP B
(CABLE TYPES B-1 TO B-3)

CABLE TYPE B-1 (two cables)			
160-A #1, J12 ---------- 2J27 160-A #2, J12 ---------- 2J30			
PIN	FUNCTION	PIN	FUNCTION
A	0 S → S'	P	odd bank selection
B	1	R	resync to mod 1
C	2	S	resync to mod 2
D	3	T	resync to mod 3
E	4	U	even clock
F	5	V	odd clock
H	6	W	$\overline{\text{resume}}$ to 160-A timing chain
J	7	X	mod 1 $\overline{\text{present}}$
K	8	Y	mod 2 $\overline{\text{present}}$
L	9	Z	mod 3 $\overline{\text{present}}$
M	10	a	
N	11	b	ground

TABLE A-2. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE B-2 (two cables)			
2J28 ---------- 160-A #1, J13 2J31 ---------- 160-A #2, J13			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 $Z' \rightarrow I^{-1}$	P	mod 1 $\overline{\text{available}}$
B	1	R	mod 2 $\overline{\text{available}}$
C	2	S	mod 3 $\overline{\text{available}}$
D	3	T	bank select 2, 3, 6, 7
E	4	U	bank select 4, 5, 6, 7
F	5	V	1 (computer)
H	6	W	$\overline{\text{E1}}$ (computer)
J	7	X	
K	8	Y	
L	9	Z	
M	10	a	
N	11	b	ground

TABLE A-2. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE B-3 (two cables)			
160-A #1, J14 ---------- 2J29 160-A #2, J14 ---------- 2J32			
PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 I^{-3} → MCS'	P	
B	1	R	
C	2	S	
D	3	T	
E	4	U	
F	5	V	
H	6	W	
J	7	X	
K	8	Y	
L	9	Z	
M	10	a	
N	11	b	ground

TABLE A-3. PIN ASSIGNMENTS, CABLE GROUP C
(CABLE TYPES C-1 AND C-2)

CABLE TYPE C-1 (six cables)			
	2J33	8J01, 02	160-A #1, J17, 18
	2J35	8J05, 06	160-A #2, J17, 18
	2J37	8J09, 10	input from periph.

PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 (Input Data)	P	
B	1	R	Input Ready
C	2	S	Input Request
D	3	T	
E	4	U	
F	5	V	Input Disconnect
H	6	W	
J	7	X	
K	8	Y	
L	9	Z	
M	10	a	
N	11	b	ground

TABLE A-3. PIN ASSIGNMENTS (Cont'd)

CABLE TYPE C-2 (six cables)			
	2J34	8J03, 04	160-A #1, J19, 20
	2J36	8J07, 08	160-A #2, J19, 20
	2J38	8J11, 12	output to periph.

PIN	FUNCTION	PIN	FUNCTION
A	Bit 0 (EF code or Output Data)	P	
B	1	R	Information Ready
C	2	S	Output Resume
D	3	T	Function Ready
E	4	U	Master Clear
F	5	V	
H	6	W	
J	7	X	
K	8	Y	Interrupt 30
L	9	Z	Interrupt 40
M	10	a	
N	11	b	ground

APPENDIX B

ELECTRONIC THEORY OF MEMORY CIRCUITS

The storage section performs non-logical functions such as amplification, pulse generation and switching. The card types are:

- drive generator (card type 51)
- diverter (card type 52)
- selector (card type 53)
- current source (card type 54)
- inhibit generator (card type 55)
- sense amplifier (card type 57)

DRIVE GENERATOR (TYPE 51)

The drive generator (figure B-1) develops the R/W current which is applied to the selected H and V wires. Two identical channels feed opposite ends of the primary winding of transformer T01. Each channel consists of transistor Q01, connected as an emitter-follower, and transistors Q02 and Q03, connected in parallel as amplifiers. The input signal is an AND combination of two selector outputs. A -0.5v input results in approximately 0v at the base of Q01. The emitter Q01 is clamped to ground by CR03, so neither Q02 or Q03 conduct. Consequently, no current flows in the primary of T01.

A -12v input signal causes Q01 to conduct; however, the conduction is held below saturation by feedback diode CR01. The negative voltage developed across R06 is applied to the bases of Q02 and Q03, causing these transistors to conduct. Current flows from the current sources through the emitters of Q02 and Q03 to the collectors, through the primary of T01, to the current sources. The current pulse from the secondary of T01, amplified by the step-down action of T01, is applied to the H and V wires of the memory plane assembly. It then flows through the selected diverter card and back to the secondary of T01.

The polarity of the output current from T01 is determined by the direction of the current flow in the primary. The direction of current flow, in turn, is determined by the selected channel. For example, if channel A receives a -12v input, a read pulse is generated; a channel C input generates a write pulse. The CR02, R05 combination clamps the collectors so the voltage does not exceed 25v.

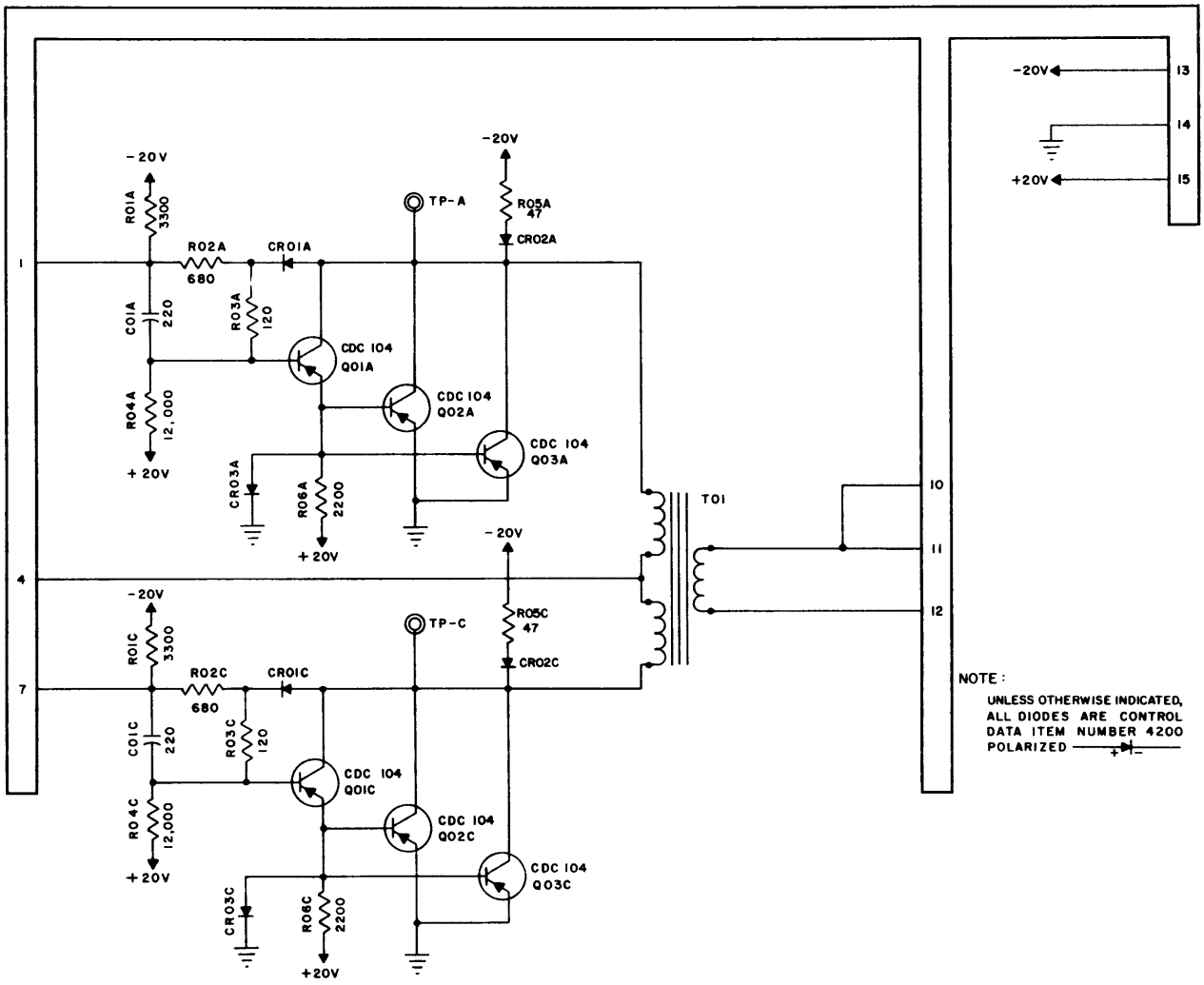


Figure B-1. R/W Driver (51)

DIVERTER (TYPE 52A)

The diverter circuit (figure B-2) serves as an electronic switch for bi-polar current in series with an H or V wire of the memory plane assembly. The diverter consists of transistor Q01, connected as an emitter follower, and transistors Q02 and Q03. One or the other of these transistors passes the current pulse on the H or V wire to which the diverter is connected, depending on the polarity of that pulse.

A positive pulse passes one of the pairs of diodes CR03 and CR04, CR07 and CR08, CR11 and CR12, etc., depending upon the driver selection, and through Q02. A negative pulse passes through Q02 and one of the pairs of diodes CR01 and CR02, CR05 and CR06, etc. In either case, the current pulse is returned to the R/W driver through a common bus to which pin 12 is connected. The bleeder networks of all the diverters are connected in parallel via terminal 11.

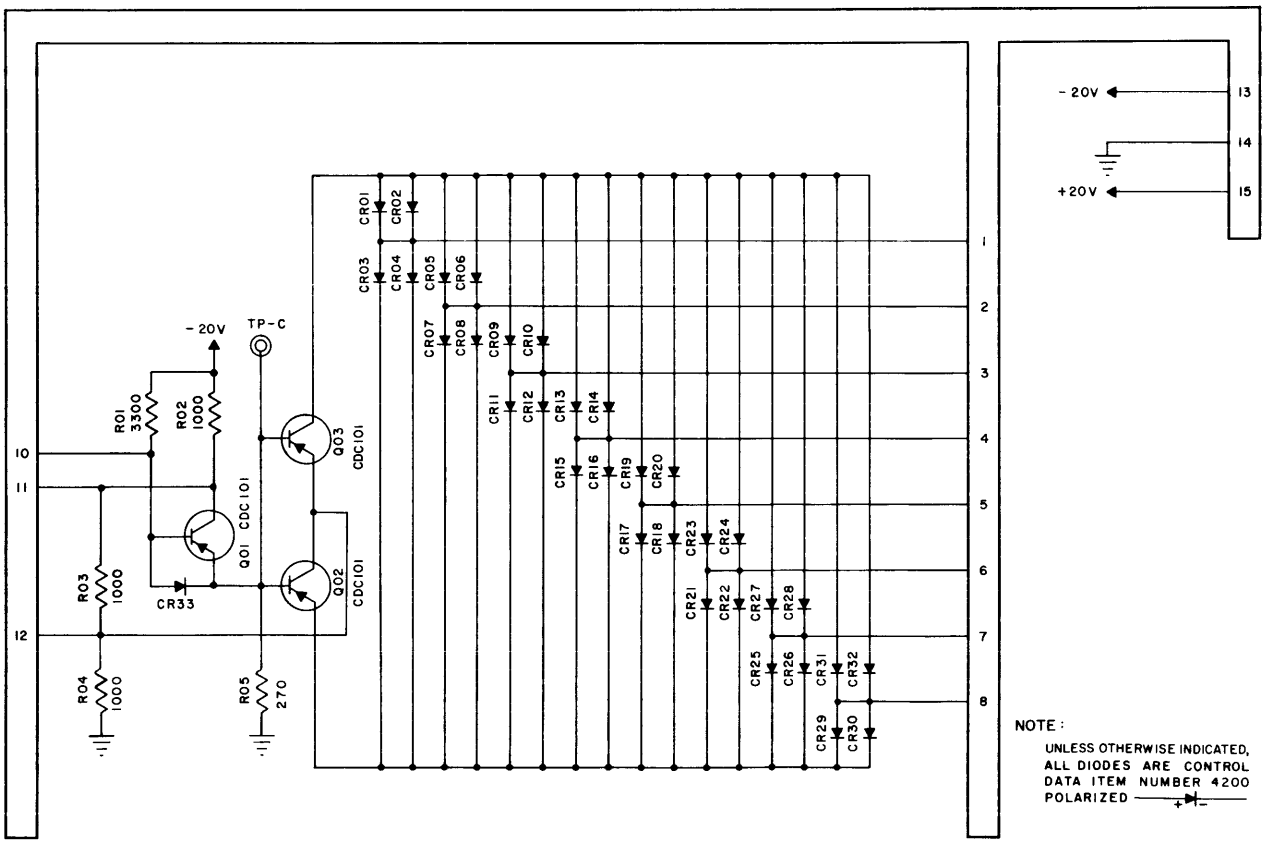


Figure B-2. Diverter (52A)

SELECTOR (TYPE 53)

The storage translators drive type 51, 52, and 55 cards, each of which presents a different impedance level input than the standard logic card. For this reason, all storage translators employ the type 53 card. Each selector card consists of two identical selector circuits. A selector circuit (figure B-3) is similar to the standard inverter except that the resistance results in output signal levels of -0.5v and -12v. Each selector circuit has two input diodes (CR01 and CR02) and four output diodes (CR09, CR10, CR11 and CR12).

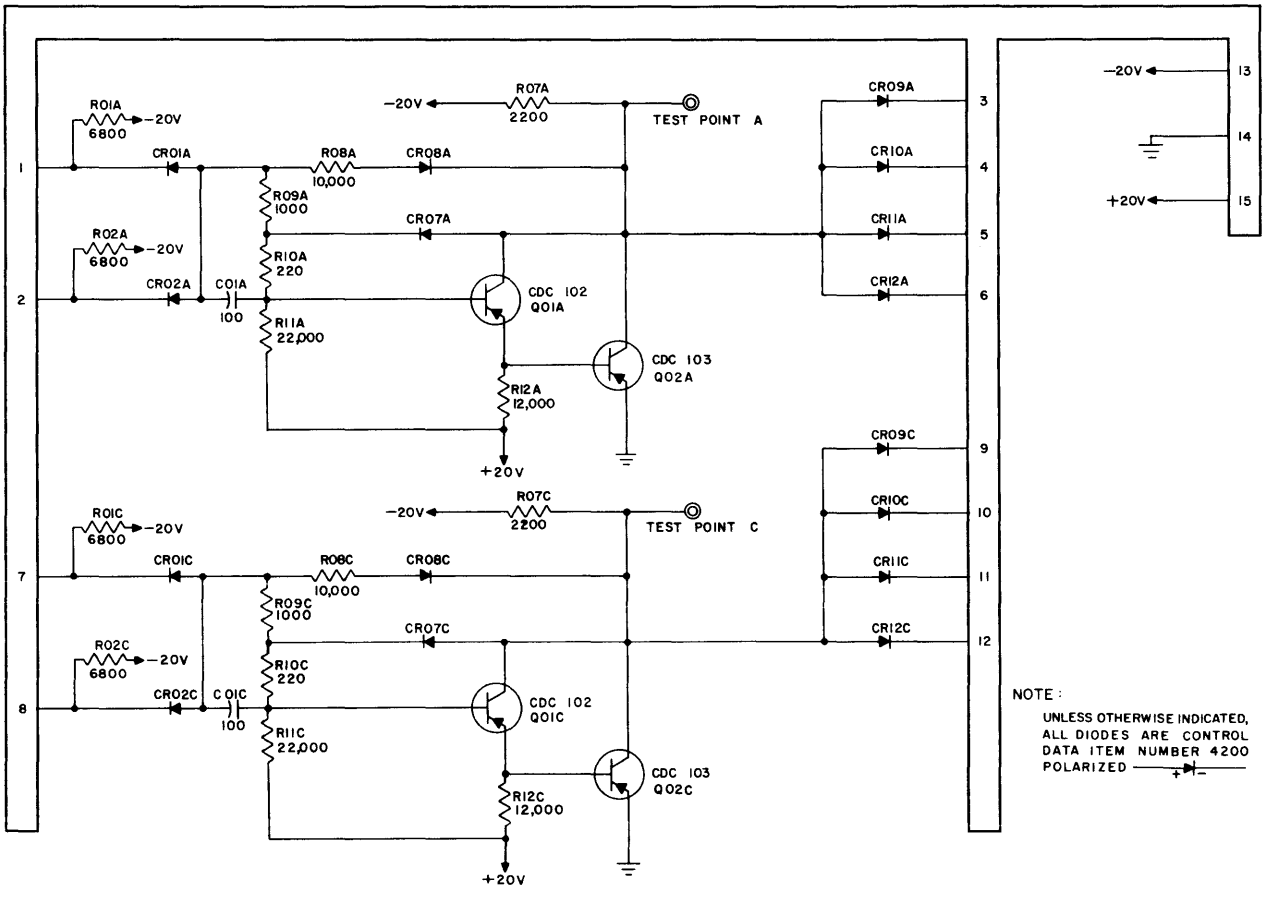


Figure B-3. Selector (53)

CURRENT SOURCE (TYPE 54)

The current source card (figure B-4) consists of five banks of parallel resistors. The effective resistance of four banks is 150 ohms each; that of the remaining bank is 303 ohms. One end of each bank is connected to the -20v output of the power supply. The 150-ohm banks supply current to the H, V and inhibit current generators; the 303-ohm banks usually supply current to a dummy load.*

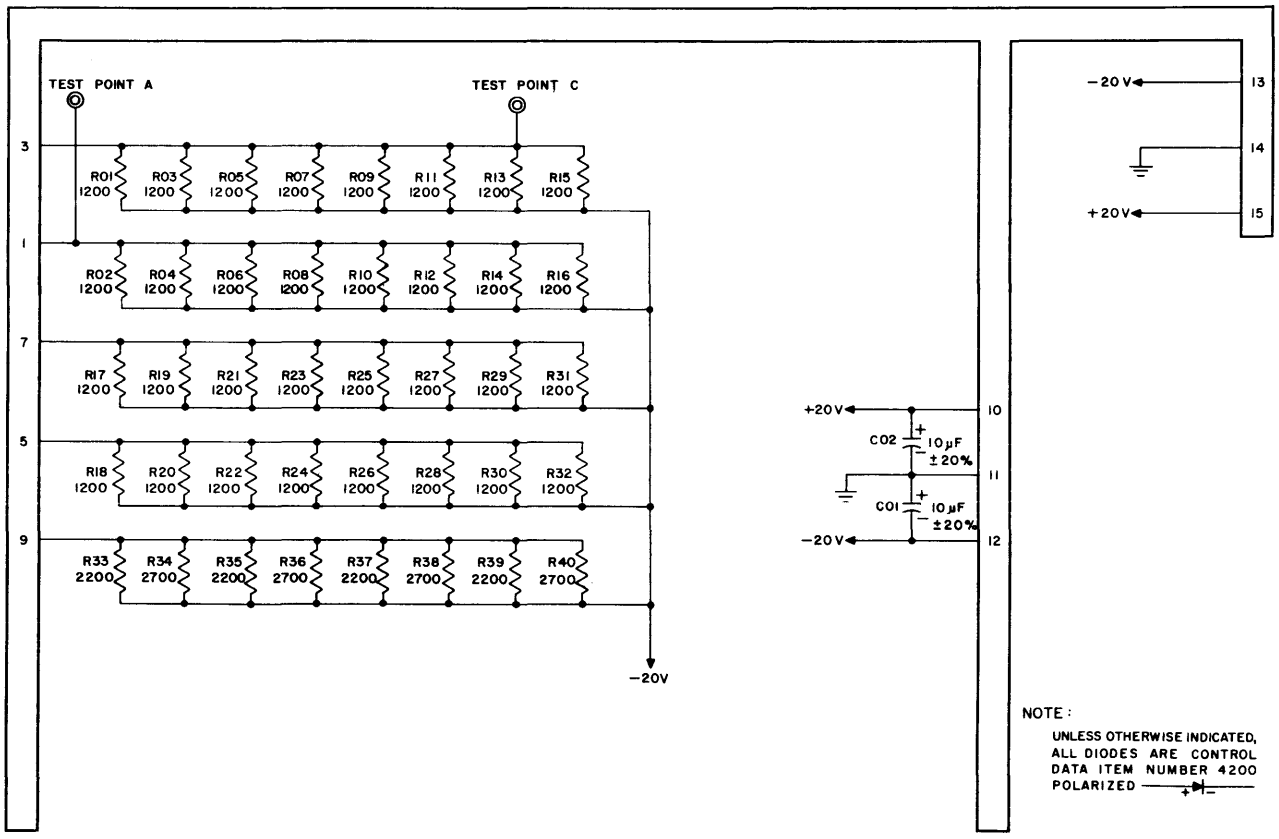


Figure B-4. Current Source (54)

* Cards are standard types for use in various computers. The 169 does not use a dummy load, therefore the 303-ohm banks are not connected.

INHIBIT GENERATOR (TYPE 55)

Each inhibit generator card (figure B-5) has two generator circuits which are similar to the type 51 drive generator channels except for the absence of an output transformer. The output of each channel is independently connected to a terminal of the card.

A -12v input signal to either generator of a type 55 card causes Q01 to conduct and thus enable Q02 and Q03. Current from the external source connects to the generator via terminal 6 or 12 and passes through Q02 and Q03 to ground.

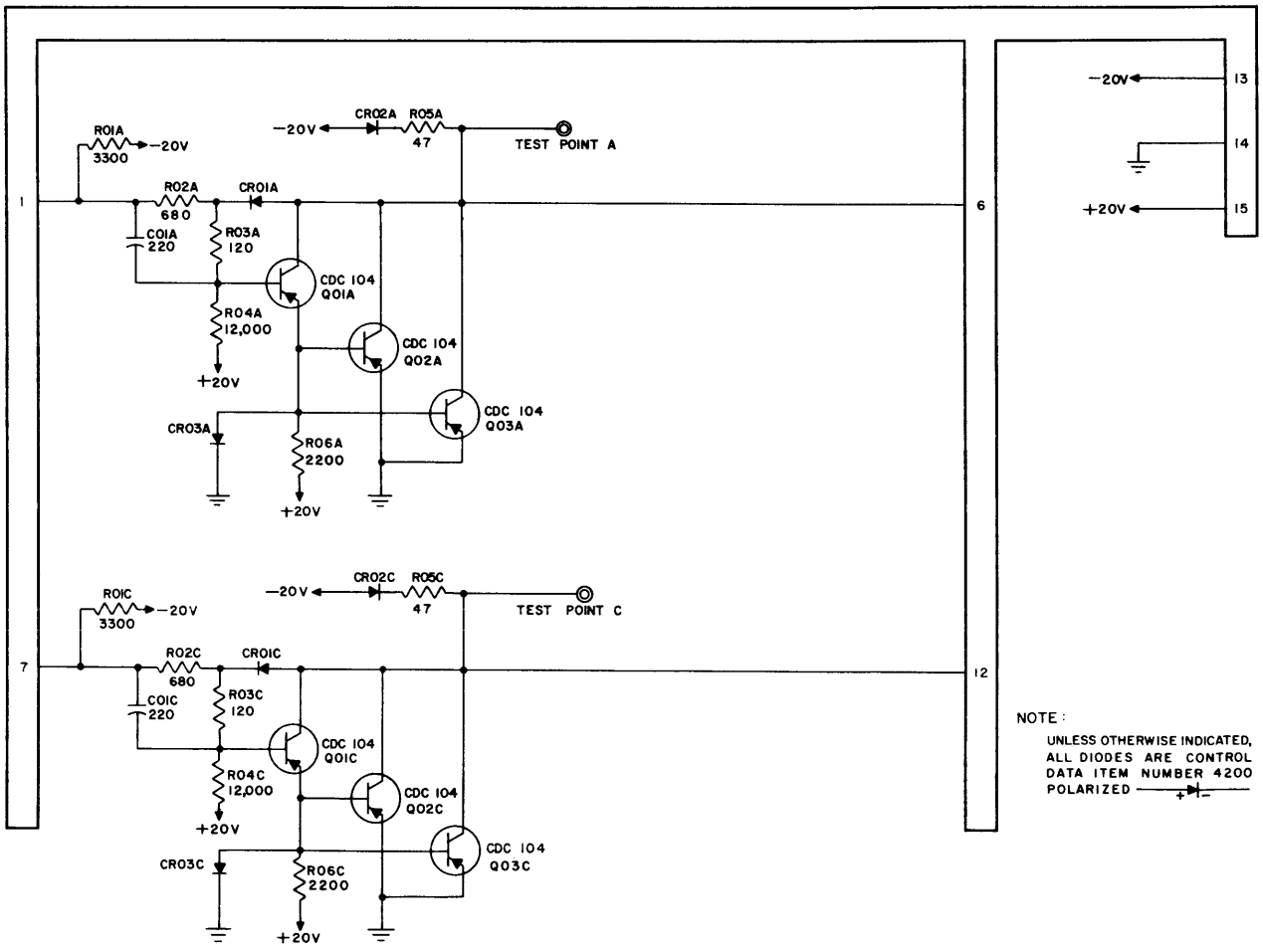


Figure B-5. Inhibit Generator (55)

SENSE AMPLIFIER (TYPE 57)

The sense amplifier (figure B-6) amplifies the signal from a memory plane (pins 2 and 4) as the result of a read pulse. Transistors Q01, Q02, Q03, and Q04 form a differential amplifier which feeds T1 through coupling capacitors C02 and C03. The secondary of T1 is connected to a bridge detector so that the signal polarity at TP-C is always the same. The Q05 network is a standard inverter circuit providing normal output logic levels of -3.0v and -0.5v.

Gain from the differential amplifier for the common mode component of the input signal is about 2; for the differential mode component, across R06 - C01, gain is about 100. Pin 1 is connected to a Margin Test switch when the 57 card is used in the 160-A internal memory. The 169 does not have this switch, consequently, pin 1 is not used. Pin 6 is connected to the diverter bus (-7.0v) to provide bias for input transistors Q01 and Q02. The output from Q05, as the result of a "1" signal on the sense lines, is -0.5v.

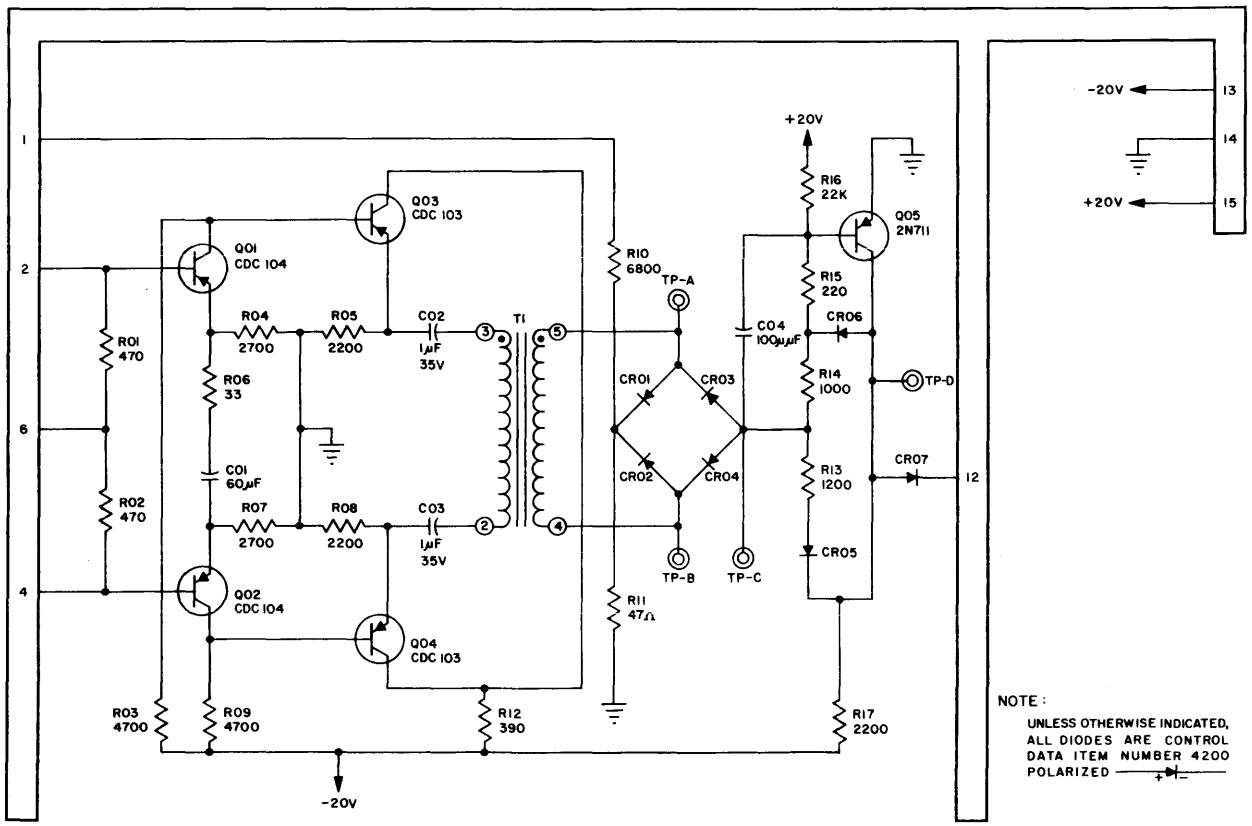


Figure B-6. Sense Amplifier (57)

APPENDIX C

SIGNAL CHARACTERISTICS

TABLE C-1. LOGICAL EXTERNAL BUFFER CABLE SIGNALS

12 bits from 160-A to 169	EF selection, control word (buffer mode), output data word (channel extension).
12 bits from peripheral equipment to 169	Data word for storage (buffer mode) data word for 160-A (channel extension).
12 bits from 169 to 160-A	Status Response, input data word (channel extension), content of BER.
12 bits from 169 to peripheral equipment	Data word from storage (buffer mode), data word from 160-A (channel extension).
Input Ready	169 to 160-A; computer may sample information. Peripheral equipment to 169; 169 (buffer) may sample information.
Input Request	160-A to 169; computer can accept an input (status information). 169 to peripheral equipment; 169 can accept an input.
Input Disconnect	Peripheral equipment to 169; there is no more data to deliver.
Function Ready	160-A to 169; EF code is on the lines. 169 to peripheral equipment; EF code selecting peripheral equipment is on the lines.
Information Ready	160-A to 169; computer is placing output word on the lines. 169 to peripheral equipment; 169 has output word on the lines.
Output Resume	169 to 160-A; 169 has accepted a word. Peripheral equipment to 169; peripheral equipment has accepted a word.
Master Clear	160-A to 169; clears 169 interrupt circuits.
Interrupt 30	From 169 or peripheral equipment via the 169 to 160-A; indicates an interrupt.
Interrupt 40	From peripheral equipment via the 169 to 160-A; indicates an interrupt.

TABLE C-2. LOGICAL MEMORY CABLES TO 160-A SIGNALS

12 bits, S → S'	Storage address transfer at start of module storage cycle.
12 bits, Z' → I^1	Data transfer from external memory to 160-A Z register; lines enabled during first 3 quarters of module storage cycle.
12 bits, I^3 → MCS'	Data transfer from 160-A Z register or External Buffer register (BFR) to module core storage (MCS'); lines enabled during first 3 quarters of module storage cycle.
160-A resync to Mod 1	Pulse every 1.6 usec; synchronizes 160-A and module 1 storage cycles.
160-A resync to mod 2	Pulse every 1.6 usec; synchronizes 160-A and module 2 storage cycles.
160-A resync to mod 3	Pulse every 1.6 usec; synchronizes 160-A and module 3 storage cycles.
Even clock	Even phase of 2.5 megacycle sine wave.
Odd clock	Odd phase of 2.5 megacycle sine wave.
$\overline{\text{Resume}}$ to 160-A	From module scanner to restart the 160-A storage cycle.
Mod 1 $\overline{\text{present}}$	Presence of module 1.
Mod 2 $\overline{\text{present}}$	Presence of module 2.
Mod 3 $\overline{\text{present}}$	Presence of module 3.
Mod 1 $\overline{\text{available}}$	Availability of module 1 to 160-A
Mod 2 $\overline{\text{available}}$	Availability of module 2 to 160-A
Mod 3 $\overline{\text{available}}$	Availability of module 3 to 160-A
Odd-even bank selection	Bit presence indicates odd bank; bit absence indicates even bank.
Bank select 2, 3, 6, 7	Selection indicated by binary translation.
Bank select 4, 5, 6, 7	Selection indicated by binary translation.
First quarter of 160-A storage cycle	160-A timing signals to 169.
$\overline{\text{Early first quarter}}$ of 160-A storage cycle	160-A timing signals to 169.

TABLE C-3. ELECTRICAL SIGNALS

Interface Logic Signals	Signal rise and fall times; 2 usec minimum, 4 usec maximum. Logic zero: -16v (±2.5v) (zero current drain) signal absent Logic one: -0.5v (+0.5v, -2.5v) (10 ma maximum current), signal present
Interface Memory Transfer Signals and Internal Logic Signals	Signal rise and fall times; less than 0.1 usec maximum. Logic one: -3v (±0.25v) signal present Logic zero: -0.5v (±0.25v) signal absent

APPENDIX D

INSTALLATION

The Control Data 169 Auxiliary Memory Unit is designed to provide additional memory facilities for the 160-A computer system. The 169 may be connected to one or two 160-A computers and to a maximum of five units of peripheral equipment. This appendix includes electrical and physical information to aid in the installation of the 169. Tables D-3 and D-4 give the special adjustment procedure which must be completed prior to placing the 169 in service. For special installation information, Control Data Corporation should be consulted.

GENERAL REQUIREMENTS

FLOOR

Cables may be brought in through the cable opening in the bottom of the cabinet or by removing the metal strip located immediately below the control panel door. If the bottom cable opening is used, it is recommended that raceways for the interconnecting cables be built into the floor as described in the installation manual for the 160-A computer system.

TEMPERATURE

Blowers cool the unit by drawing air through reuseable filters at the bottom of the cabinet. Air is exhausted through the louvres in the unit doors.

The unit is designed to operate in an ambient air temperature not exceeding $80^{o}F$. Although it is not critical, the humidity should be maintained at between 40% and 60%.

FIRE PRECAUTIONS

Fire extinguishers should be located near the computer system and normal fire precautions observed.

SPACE AND LAYOUT REQUIREMENTS

The unit should be positioned so the operator may observe the indicators. There should be a minimum three-foot clearance surrounding the unit to facilitate movement of maintenance test equipment. Cabinet dimensions and door swings are given in figure D-1. Dimensions and weight are in table D-1.

TABLE D-1. SPECIFICATIONS

Height	43 inches
Width	47 3/4 inches
Depth	20 1/4 inches
Weight	600 pounds with two chassis, 800 pounds with 4 chassis
BTU/Hour	4700 BTU/hr maximum (upper ambient limit for cooling by internal blowers is 80°F)
Power Requirement	169-1, 12 amp (1380 w) 169-2, 15 amp (1725 w) 169-3, 17 amp (1955 w)

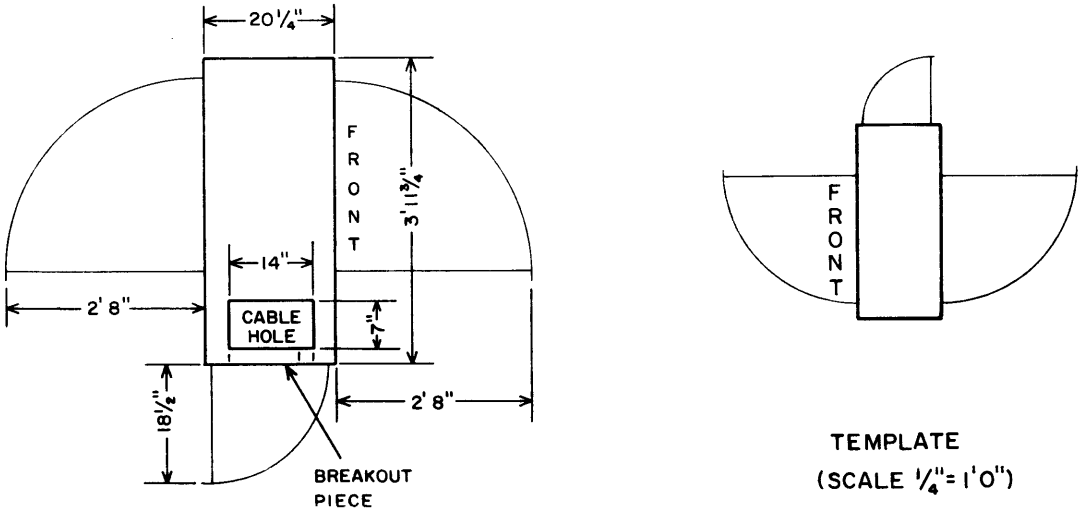


Figure D-1. Space Requirements

POWER REQUIREMENTS

POWER SERVICE

The primary power requirement is 115v, 60 cycle, single phase. Current requirements are listed in table D-1. The unit may be connected to any normal convenience outlet in the computer area. At the customer's option, the single phase power may be derived from one leg of a three phase Y connected source.

Power to the 169 is normally controlled by the On-Off switch on the indicator panel. However, power to the 169 may be controlled from the computer by connecting the controlled a-c line from the 160-A to the controlled a-c line of the 169 at an external power panel. If this is done, the 169 Power switch must be left in the OFF position, and care must be taken to connect the 160-A and 169 to the same phase of the a-c line.

INTERCONNECTING CABLES

INPUT-OUTPUT CABLES

The cables which connect the unit to the computer will be delivered at the time of installation (figure D-2, table D-2). The cables carrying the memory transfer signals may be a maximum of 10 feet long. Interface logic signal cables may be a maximum of 75 feet long.

Control Data Corporation should be advised of any unusual cabling requirements no later than two months prior to shipment. Any unusual cable lengths may be purchased from Control Data Corporation. Sufficient cable length should be allowed to accommodate minor changes in the location of the unit.

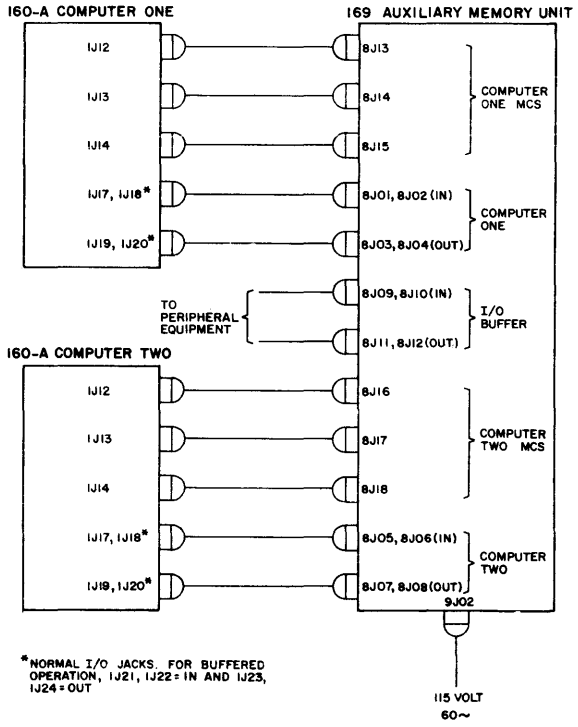


Figure D-2. Cabling Diagram

TABLE D-2. CABLE CONNECTIONS, INPUT-OUTPUT

Function	169 Jack	160-A Jack
60 Cycle Power Input	9J02	
Memory Transfer (coaxial)	8J13	1J12 (computer one)
Memory Transfer (coaxial)	8J14	1J13 (computer one)
Memory Transfer (coaxial)	8J15	1J14 (computer one)
Memory Transfer (coaxial)	8J16	1J12 (computer two)
Memory Transfer (coaxial)	8J17	1J13 (computer two)
Memory Transfer (coaxial)	8J18	1J14 (computer two)
Normal/Buffer Input	8J01-8J02	1J17-1J18 (computer one)
Normal/Buffer Output	8J03-8J04	1J19-1J20 (computer one)
Normal/Buffer Input	8J05-8J06	1J17-1J18 (computer two)
Normal/Buffer Output	8J07-8J08	1J19-1J20 (computer two)
Peripheral Equipment Input	8J09-8J10	
Peripheral Equipment Output	8J11-8J12	

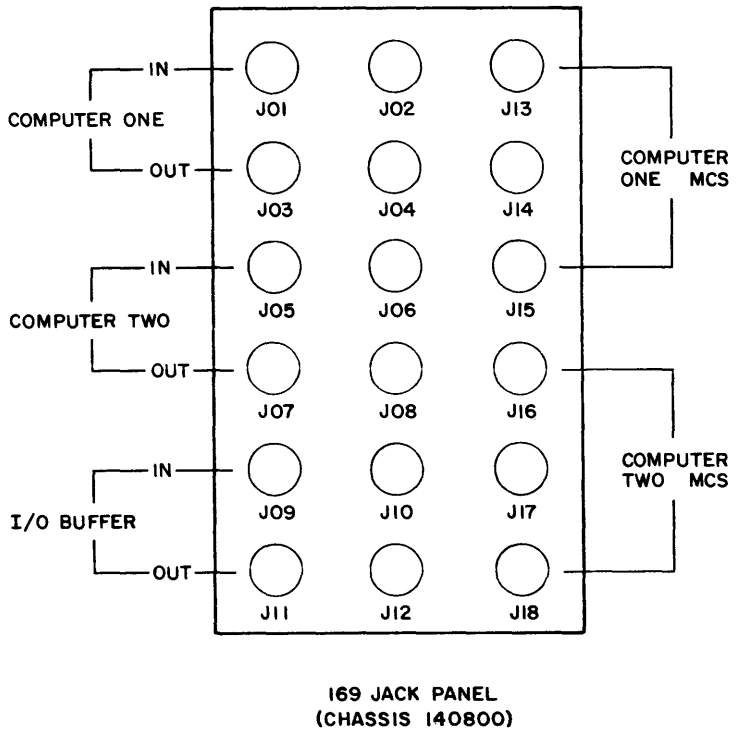


Figure D-3. Cable Connections

INSTALLATION ADJUSTMENT PROCEDURE

The adjustment procedure for the 169 when used with a single computer is given in table D-3. This adjustment must be made to synchronize the master clocks of the 169 and the computer.

When the 169 is shared by two computers, the master clocks of both computers must be synchronized (table D-4). Either computer master clock may be used as a reference standard. In the computer not used as the reference standard, one master clock oscillator card must be changed from a fixed oscillator card (type 01) to a variable oscillator card (type 02). This variable oscillator card provides the adjustment necessary to synchronize the master clocks of the two computers.

An oscilloscope with a differential input and a card extender (Control Data No. 6167) is required for these adjustments. A Tektronix 543A oscilloscope equipped with a type CA plug-in unit and two 10X attenuator probes is recommended.

If an oscilloscope with a differential input is not available, these adjustments may be accomplished with an oscilloscope having a single input. A Tektronix 317 oscilloscope is recommended. In order to use an oscilloscope with a single input, it is necessary to connect two 10X attenuator probes (Tektronix type P6000) to a "T" coaxial adapter (Amphenol type 83-1T, UHF "T" adapter). This "T" coaxial adapter is then attached to the single vertical input of the oscilloscope. With both probes connected to the "T" coaxial adapter, each probe must be frequency compensated.

The 169 adjustment procedures are essentially the same as given in tables D-3 and D-4 except where reference is made to figure D-4 and to channels A and B. Where figure D-4 is referenced, figure D-5 should be consulted. Where channels A and B are referenced, they may be ignored because the attenuator probe may be used interchangeably.

TABLE D-3. SYNCHRONIZATION OF THE 169 AND 160-A

STEP	OPERATION
1	Connect all necessary cables between the unit and the computer as shown in figure D-2. NOTE If two computers are used in the system, the procedure outlined in table D-4 must be completed prior to this adjustment.
2	Remove the clock disconnect card (type 00) at location A41, chassis 140200, of the 169 and replace it with an empty card extender (Control Data No. 6167).
3	Place the oscilloscope controls to the position shown in figure D-4. Make certain the Variable controls are in the fully clockwise or calibrated position.
4	Turn on all units in the system. Allow several hours for the system to stabilize. A preliminary adjustment may be made after ten minutes of warm up time.
5	Connect the oscilloscope vertical input channels to the card extender at pin 1 (channel A) and pin 3 (channel B), using a 10X attenuator probe for each channel. Make certain there is a good ground connection between the oscilloscope and the 169.
6	Adjust the Triggering Level and Stability controls on the oscilloscope to the point where the oscilloscope is sweeping and a stable pattern is obtained.
7	Adjust the master clock variable oscillator card, located at B25, chassis 140200, of the 169 to zero beat (no modulation on the oscilloscope pattern).

TABLE D-3 (Cont'd)

STEP	OPERATION
8	Turn the variable oscillator adjustment (step 7) counterclockwise until the oscilloscope pattern shows one peak per centimeter (see scope pattern on figure D-4). The tolerance on this adjustment is -0%, +100%. This adjustment sets the master clock on the 169 control chassis to between 10kc and 20kc higher than the master clock of the reference computer.
9	Connect channel A of the oscilloscope to pin 2 of the card extender and adjust the variable oscillator card located at A02, chassis 140100, of the 169 following the procedure outlined in steps 7 and 8.
10	(16K and 24K units only) Connect channel A of the oscilloscope to pin 5 of the card extender and adjust the variable oscillator card located at A02, chassis 140400, following the procedure outlined in steps 7 and 8.
11	(24K units only) Connect channel A of the oscilloscope to pin 6 of the card extender and adjust the variable oscillator card located at A02, chassis 140300, following the procedure outlined in steps 7 and 8.
12	Remove the card extender and replace the clock disconnect card at location A41, chassis 140200.
13	Using the oscilloscope, measure the clock amplitude at either test point A or C of the clock disconnect card (location A41, chassis 140200). The waveform should be a 2.5 megacycle sine wave with an amplitude of 15 volts $\pm$ 10%, peak to peak. No detachable modulation should be present.
14	Clear all Timing Faults indicated on the control panel before attempting any operation.

TABLE D-4. SYNCHRONIZATION OF TWO 160-A COMPUTERS

STEP	OPERATION
1	Connect all necessary cables between the 169 and the two computers as shown in figure D-2.
2	In the computer to be synchronized, replace the master clock oscillator card (type 01) located at A05 with a variable oscillator card (type 02).
3	Remove the clock disconnect card at location A41, chassis 140200, of the 169 unit, and replace it with an empty card extender (Control Data No. 6167).
4	Place oscilloscope controls to the positions shown in figure D-4. Make certain the Variable controls are in the fully clockwise or calibrated position.
5	Connect the oscilloscope vertical input channels to the card extender at pin 3 (channel A) and pin 4 (channel B), using a 10X attenuator probe for each channel. Make certain there is a good ground connection between the 169 and the oscilloscope.
6	Turn on both computers and the 169. Allow several hours for the system to stabilize. A preliminary adjustment may be made after ten minutes of warm up.
7	Adjust the Triggering Level and Stability controls on the oscilloscope to the point where the oscilloscope is sweeping and a stable pattern is obtained.
8	Adjust the master clock variable oscillator card (step 2) until the oscilloscope pattern shows no modulation (zero beat).
9	Starting at step 5 of table D-3 continue the adjustment procedure.

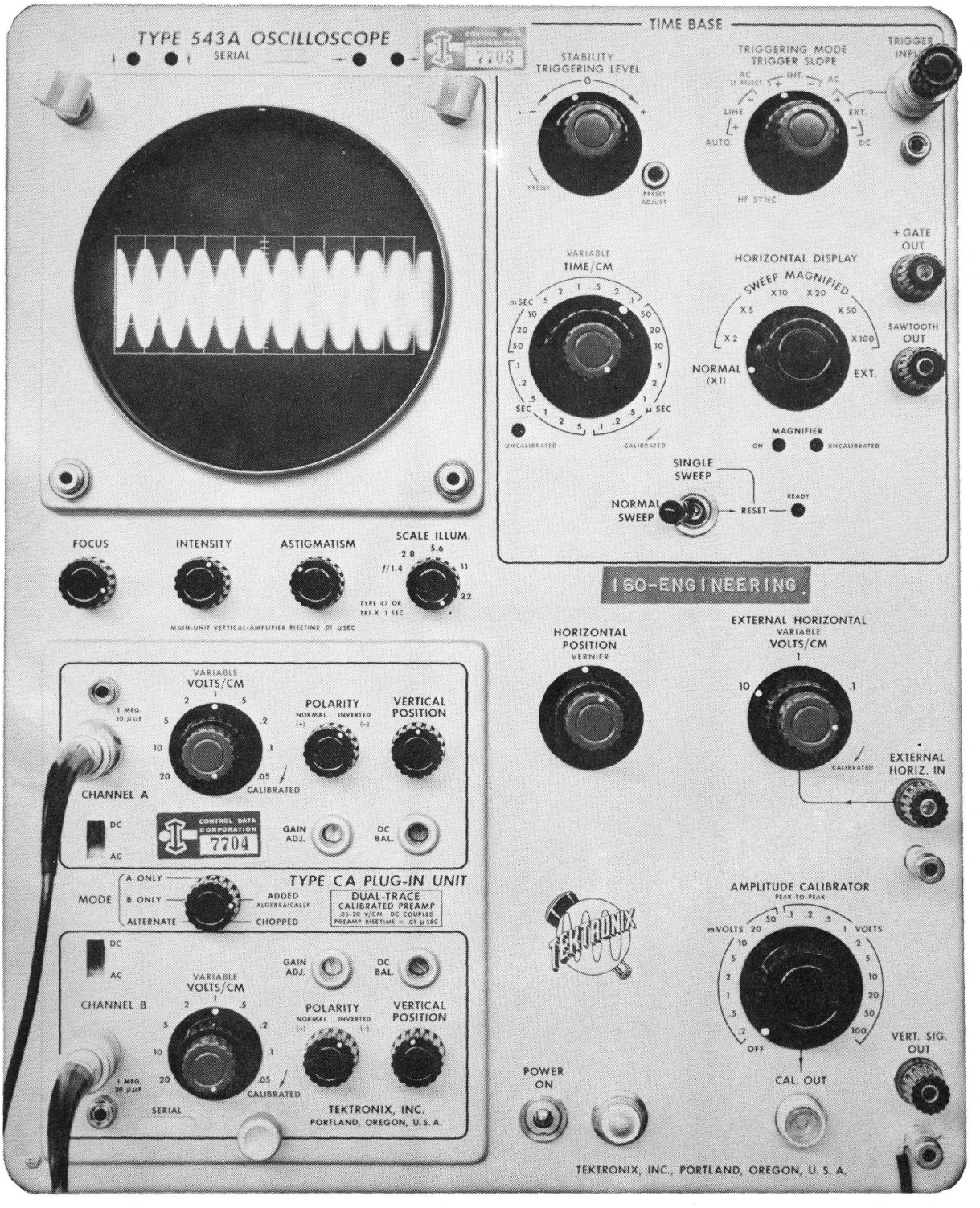


Figure D-4. Oscilloscope Control Positions

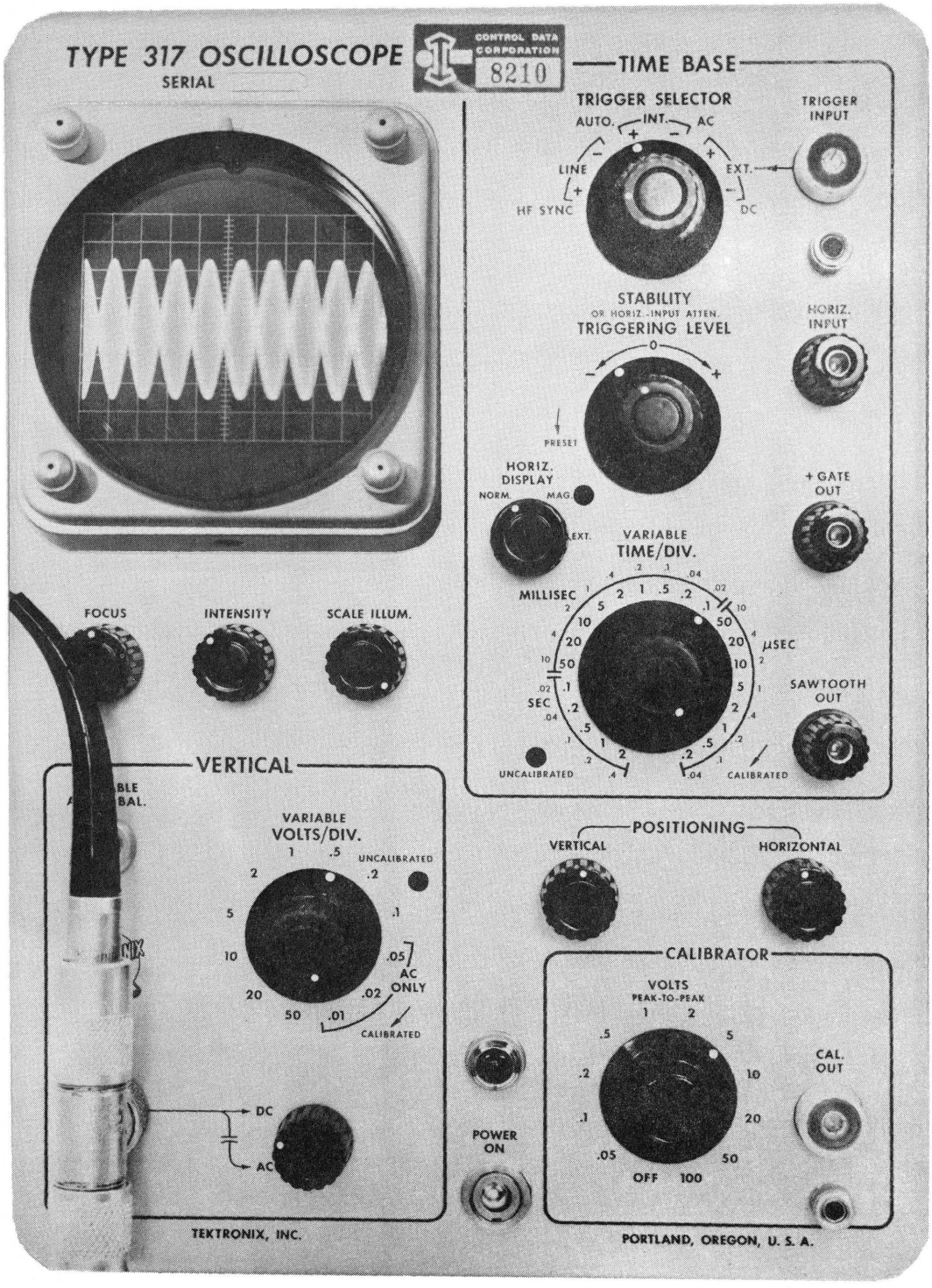


Figure D-5. Alternate Oscilloscope Control Positions

CONTROL DATA

CORPORATION

501 PARK AVENUE, MINNEAPOLIS 15, MINNESOTA • FEDERAL 9-0411