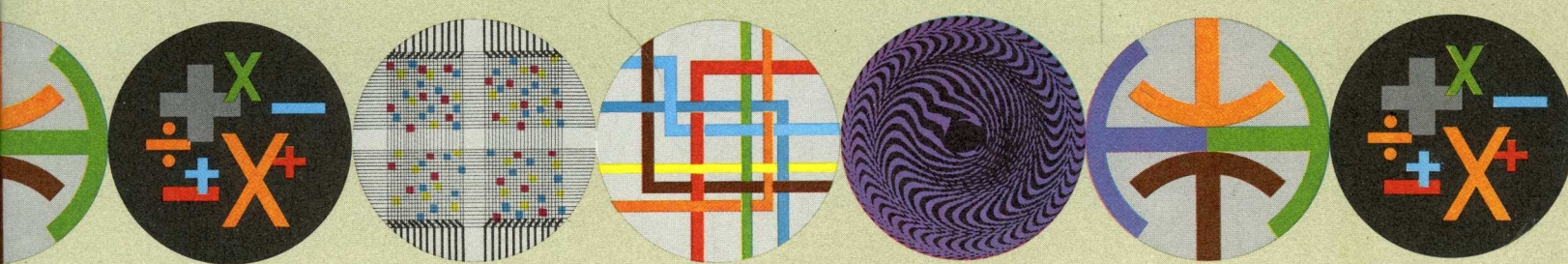
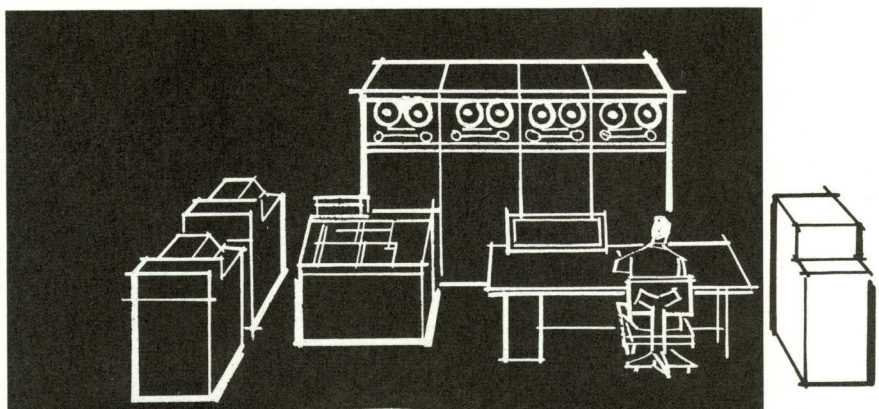
BURROUGHS MILITARIZED D825 MODULAR DATA PROCESSING SYSTEM



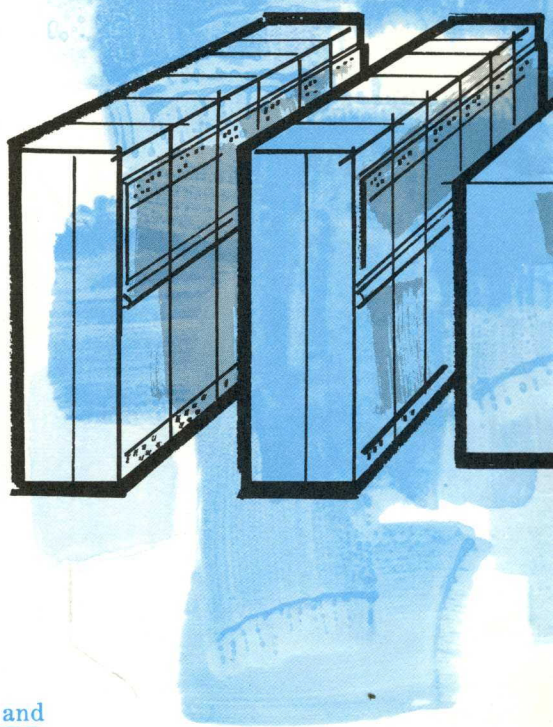
D825 MODULAR DATA PROCESSING SYSTEM

DESIGNED FOR **PRESENT** AND **FUTURE** MILITARY AND SPACE REQUIREMENTS



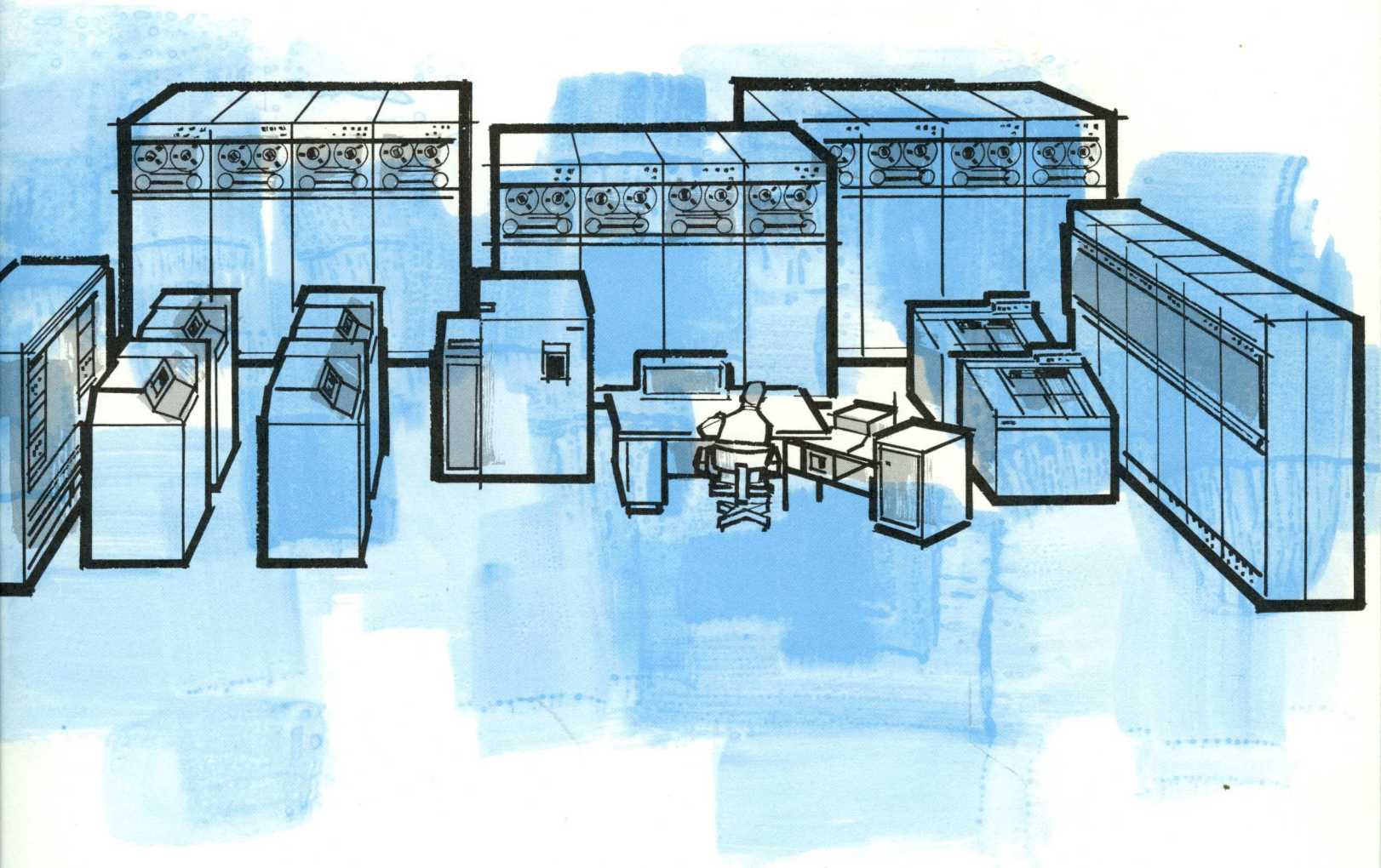
Burroughs Corporation
Defense and Space Systems Marketing, PAOLI, PA.

An extremely reliable, versatile data processing system—featuring high *throughput* speed, *parallel processing*, and economical *expandability*—has long been sought by military and space agencies to resolve their pressing computational needs. ☐ In the absence of a military-oriented computer answering these requirements, military and quasi-military applications in past years have necessarily been implemented with general-purpose commercial equipment. In nearly all cases, these computers have become saturated with mushrooming workloads far in excess of anticipated increases. ☐ Well experienced in the field of military computation, Burroughs Corporation launched an in-house study early in 1959 to



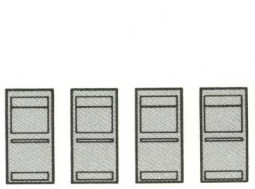
* A non-technical brochure documenting this study and explaining the BURROUGHS MILITARY-ORIENTED D800 SERIES MODULAR DATA PROCESSING CONCEPT is available upon request.

examine and develop techniques for parallel processing and automatic programming . . . a study that sparked the breakthrough revolutionizing the concept of modern electronic computer organization. ✻ The result of this study and developmental program is the D825 Militarized Modular Data Processing System—the *first totally modular* computing system designed expressly for military environments and applications. □ Incorporating advanced techniques proved by Burroughs in previous military applications, the D825's basic organization and built-in growth potential make it particularly well suited for applications such as command, control, and communications systems, air and space surveillance and traffic control systems, and weather data collection and reporting systems. □ The revolutionary feature of this new computer—and key to its unique versatility—is the use of *functionally* independent Computer Modules, Memory Modules, and Input/Output Control Modules, all of which are inter-connected to form a flexible and highly efficient system capable of both multi- and parallel processing. This interconnection is achieved by means of a unique Switching Interlock organization which responds to a permanently stored scheduling program. Therefore, Modules may be added or eliminated as requirements change without affecting existing programs . . . and without time-consuming reprogramming. □ The result is a system which automatically schedules itself, ensures its own maximum efficiency, adapts to real-time influence, and adapts to changes in program priorities and workload (without reprogramming). The system also automatically diagnoses and bypasses its own malfunctions and cannot be totally disabled by a single system element failure. □ The D825 is especially enhanced by its critically high *throughput* capability. Other computation systems may quote faster *raw* speeds, but raw speed is actually not an accurate measurement of a computer's problem-solving capability. Throughput—the speed at which a computer can complete a *total* assignment from problem conception to problem solution—is a far more meaningful performance criterion. D825 throughput —the summation of all technical advancements described in the following pages—is unmatched in military computers today.

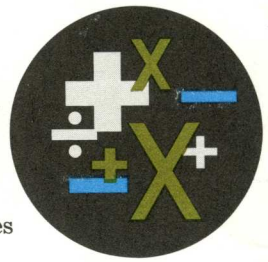


D825 SYSTEM CHARACTERISTICS

Burroughs D825 Modular Data Processor is composed of independent but interconnected, compatible, standard modules —not one rigidly integrated piece of hardware. This is the unique feature which permits system expansion. The size of the system (or number of modules) depends entirely on the application. The user selects the system required to meet the immediate workload; then, as requirements increase, additional modules may be added to expand the total capability. Thus, even though a greatly expanded future workload is anticipated, the user need only install what is required to meet present needs. Because of the basic design of the system, all additional modules may be integrated *without* costly, time-consuming down-time or reprogramming.



1 to 4 Computer Modules

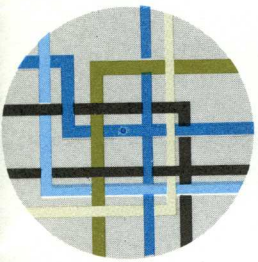


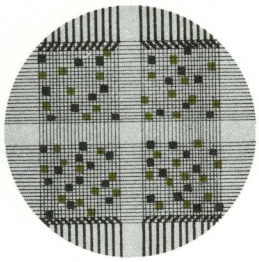
SYSTEM FEATURES

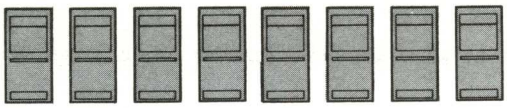
- Military specification design
- Automatic control of intermodule communications
- Simultaneous computing and I/O operations
- Real-time interrupts
- Indirect addressing
- Zero, one, two or three address instructions
- Direct access to totally shared Memory Modules by all Computer Modules and I/O Modules
- Simultaneous operation of as many I/O devices as there are I/O Control Modules in the I/O exchange
- Automatic Computer program re-start after primary power failure
- Highly reliable solid state circuitry

SYSTEM SPECIFICATIONS

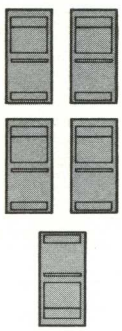
- System Hardware Complement:
  - 1 to 4 Computer Modules
  - 1 to 16 Memory Modules
  - 1 to 10 Input/Output Control Modules (1 to 20 with 3-Computer system)
  - 1 to 64 Input/Output Devices (1 to 128 with 3-Computer system)
- System Software Complement:
  - Advanced Program Compilers, including:
    - —ALGOL
    - —JOVIAL
    - —FORTRAN
  - AOSP (Automatic Operating and Scheduling Program), providing:
    - —Multi- and parallel processing
    - —Automatic self-diagnosis
    - —Automatic bypass of inoperative modules
    - —Operational modularity
    - —Automatic priority determination
    - —Unified system balance
  - Auxiliary routines, including:
    - —Symbolic Assembler
    - —Standard mathematical subroutines
- Clock Rate: 3.0 megacycles
- Ferrite Core Memory:
  - 4,096 words of 48 bits, plus one parity bit in each Memory Module
- Thin-film Memory:
  - 128 words of 12 or 16 bits in each Computer Module
- Index Registers: 15
- Comparison Limit Registers: 15
- I/O Channel Transfer Rate:
  - 250,000 wps, or 2,000,000 cps
- Reliability: The D825 modular organization inherently provides extremely reliable operation. Dynamic scheduling of modules on a priority sensitive basis permits automatic rerouting of problems around failures of individual modules. Addition of a module of each type provides redundancy without duplication of the entire system. The redundant equipment does not remain idle but shares the processing load during normal operation. The failure of any module does not reduce full operational capability. Availability in excess of 99.99% can be obtained in this manner.





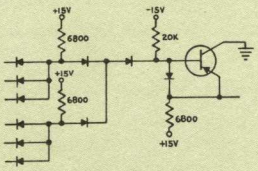


1 to 16 Memory Modules (2 per cabinet)



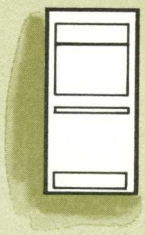
1 to 10 Input/Output Control Modules (2 per cabinet)

LOGIC CIRCUITRY



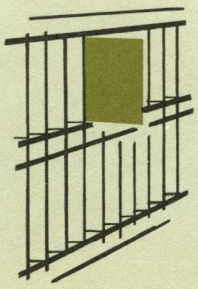
The logic circuitry of the D825 system uses Burroughs proprietary Hybrid Transistor-Diode Logic technique. This circuitry, proved by Burroughs over a wide range of severe military applications, offers optimum use of transistor gain-band width product, noncritical transistor parameters, large fan-in and fan-out capability, and maximum system reliability through a minimum of circuit components. In addition, minimum component cost is ensured through the use of inexpensive diode gates and the employment of transistors as amplifiers.

CABINETS



The Computer, Memory, and I/O Control Modules are housed in identical standard cabinets. Each cabinet has its own power supply. The basic cabinet is front-opening steel weldment designed for maximum radio frequency interference shielding and optimum component accessibility and cooling. Each cabinet is 80″ x 39″ x 24″ and has a volume of 43.3 cubic feet. Each standardized cabinet can accommodate one Computer unit, two Memory units, or two I/O Control units.

PACKAGING



A considerable reduction in the size and cost of the system modules has been achieved through use of miniaturized circuit cards and circuit components. These submodular units are arranged on two identical subassembled racks per cabinet. Each rack is pivoted on a common center to permit easy access to both the card insertion face and the backplane wiring face. Maintenance can be performed on a D825 system module without disconnecting or interrupting system operation.

COMPUTER MODULE

The D825 system accommodates up to four Computer Modules. Each Computer Module is *functionally* divided into three principal areas. The first area, the arithmetic section, is comprised of three registers with associated controls. The second area is a complex series of registers contained in a small thin-film magnetic memory. The third area, the control section, provides indexing, direct address computation, and indirect addressing. Included in the control section are the command and subcommand matrices.

ARITHMETIC AREA

The arithmetic section operates in parallel, but receives data in serial-parallel form. Fixed-point add is executed in 1.33 μs for like signs and 2.00 μs for unlike signs. For floating point and fixed point operations, the A, B, and C registers act as shift registers. The A register is capable of shifting in optimum combinations of 1, 6, and 12 places to the right, or one place to the left.

THIN-FILM MEMORY AREA

The magnetic thin-film storage, operating at a 3-megacycle clock rate, includes a four-word operand stack ("scratch pad" memory) which greatly reduces the number of required accesses to main memory modules. The thin-film area also includes a number of other registers which are described below.

The CENTRAL BUFFER REGISTER is a multipurpose register. To initiate a memory transfer, the memory address is first transferred to this central buffer register. The portion of the address which designates a Memory Module is sent as dc levels to the switching interlock circuitry of the memory trunk. Address data for the Memory Module and information words entering the Computer Module from the Memory Module are transmitted through the central buffer register, 12 bits at a time.

The COMMAND REGISTER is a 12-bit register that holds the operation syllable being executed and provides the dc levels for driving the command and subcommand matrices.

The MULTIPLY/DIVIDE COUNTER controls the number of add or subtract cycles to be executed. The counter also controls the number of shifts to be executed during an instruction.

The five OPERAND REGISTERS include four operand storage registers (thin-film operand stack) and the thin-film C register—used to store the least significant half of a double length product and the remainder of a division. There are also two PROGRAM-STORAGE REGISTERS providing storage for eight instruction syllables and permitting overlapped instruction fetch.

The BASE ADDRESS REGISTER holds the address of the starting location of the data direct-address memory area; the BASE PROGRAM REGISTER holds the starting location of the program address memory area.

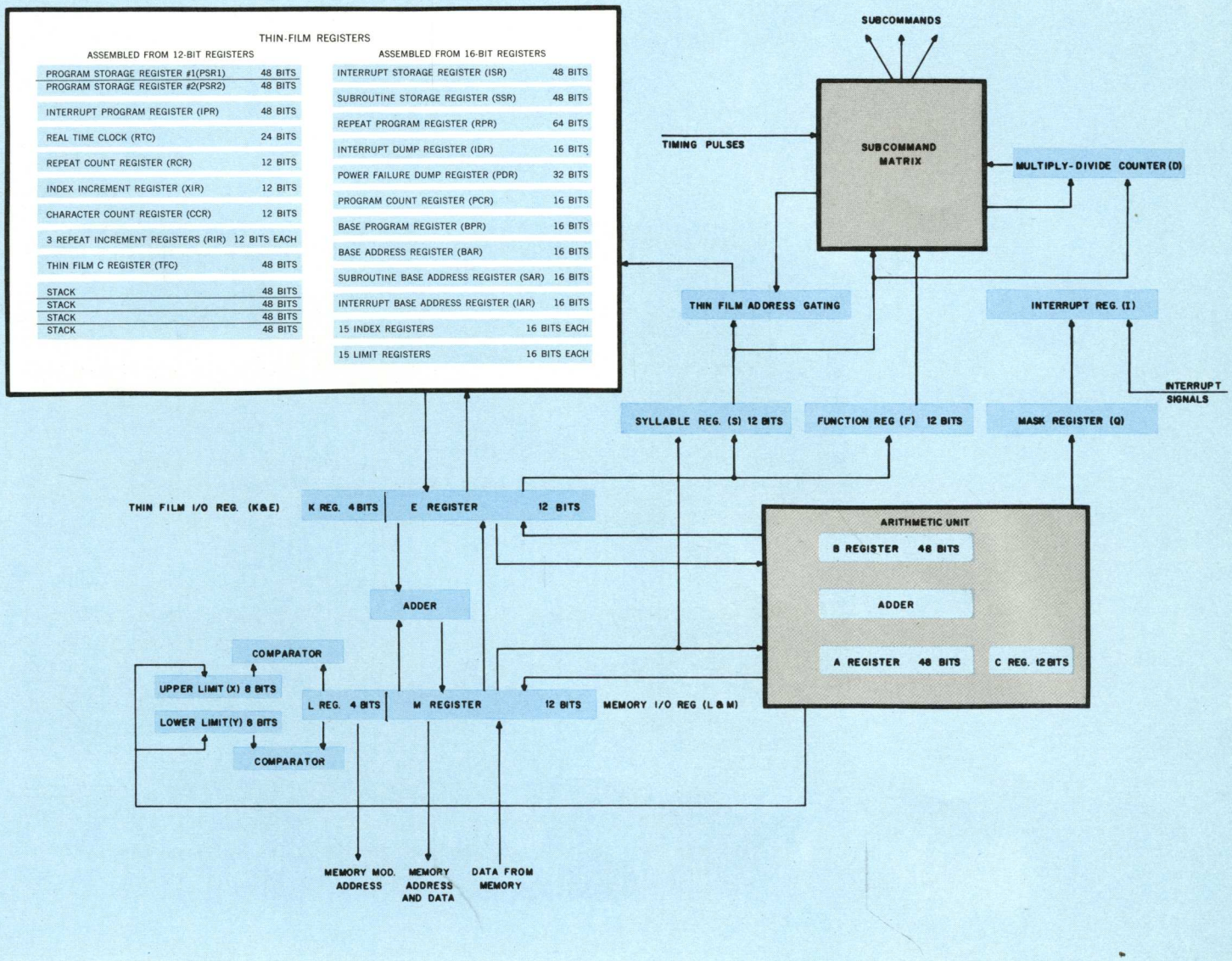
There are 15 INDEX REGISTERS and 15 COMPARISON LIMIT REGISTERS. Any three of the index registers may be addressed by each index address syllable and used to modify each instruction address. The index registers may be incremented, decremented, and compared with the comparison limit registers.

The contents of the REAL-TIME CLOCK REGISTER are automatically read out and decremented every 10 milliseconds. This clock register may be sampled by the program or used to initiate an interrupt when the count reads a ZERO.

The INTERRUPT SYSTEM REGISTERS provide storage for data in the operational registers in the event of an interrupt. (See Pages 14 and 15.)

CONTROL AREA

The control area, responsible for total intra-computer module communication links, provides indirect addressing to an unlimited number of levels. The address obtained as a result of indirect addressing may also be indexed.

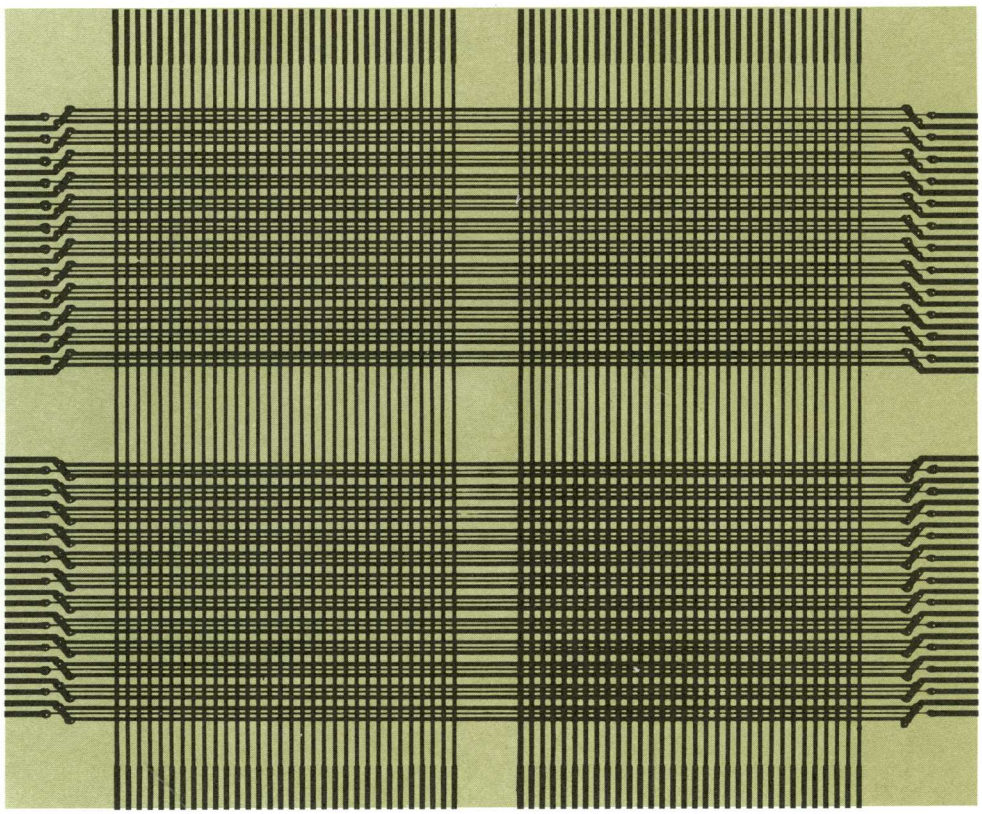


COMPUTER MODULE: THIN FILM MEMORY ...HEART OF HIGH THROUGHPUT SPEED

Within each Computer Module is a thin-film memory which serves as high-speed storage (or "scratch-pad" memory) for control registers and the operand stack. By designing this compact, advanced memory technique into the Computer Module itself, the number of required accesses to main Memory Modules is significantly reduced—thereby contributing immeasurably to the high throughput speed attained by the D825 system.

Each thin-film memory has a capacity of 128 words of 12 or 16 bits each; the read-write cycle time is 0.33 microseconds.

The thin-film memory for the D825 is constructed in a plane of two small plates (each, 64 x 24 bits). These plates have particles of nickel-iron alloy vacuum-deposited on glass substrate. Preferred magnetic orientation of the bits is achieved by performing the deposition process in a magnetic field. Uniformity of electrical characteristics is obtained by extremely precise control of the deposition process.



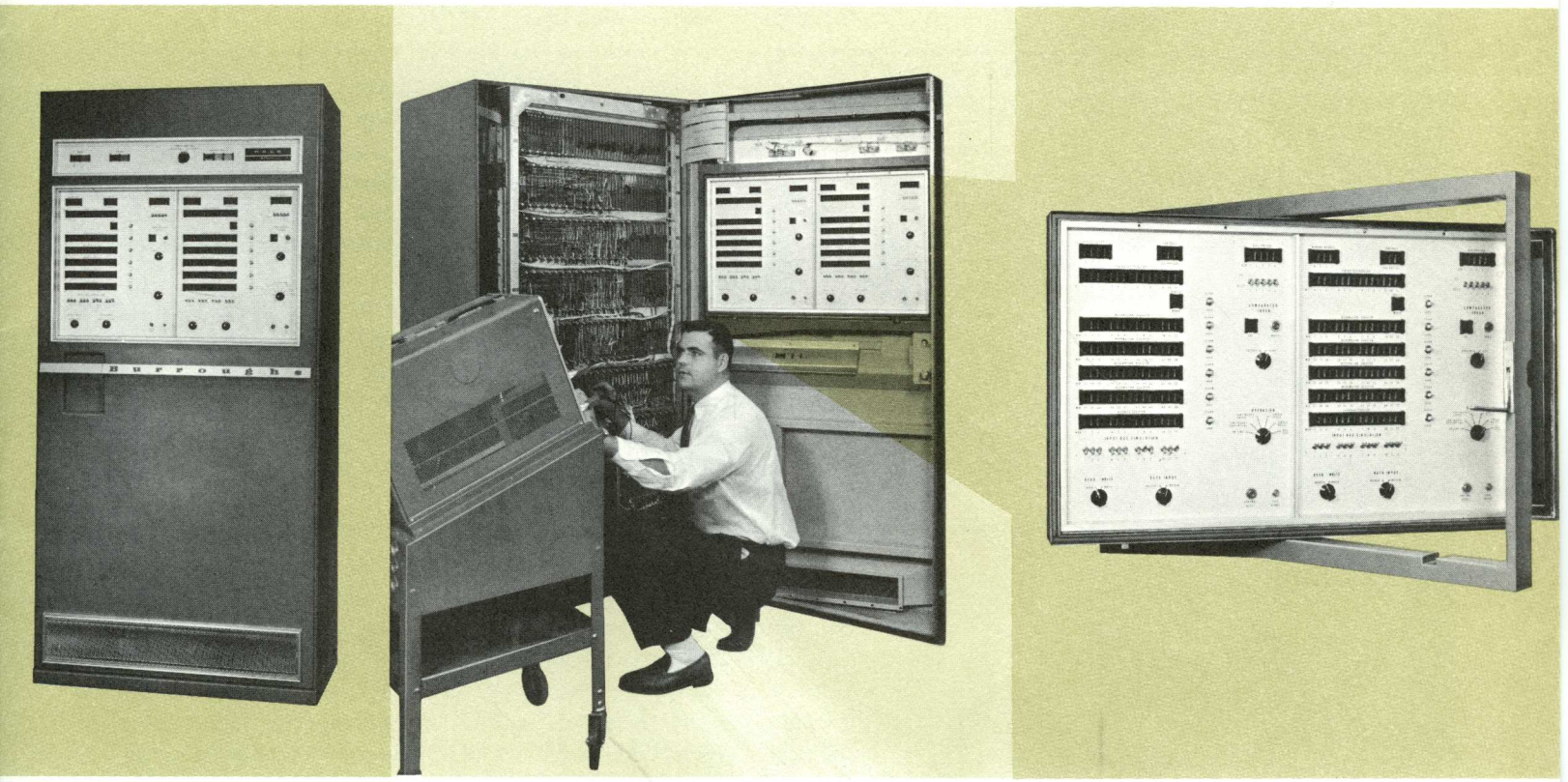
MEMORY MODULE

The D825 Memory Modules are linear-select (word-organized) ferrite-core arrays which operate with a complete read-write cycle time of four microseconds. Access time is one microsecond. Each Memory contains 4,096 words of 48 information bits and one parity bit. A fully expanded system with 16 Memory Modules provides 65,536 words of random-access memory.

Each Memory Module contains independent read, write, and regenerate circuitry as well as necessary addressing circuitry. Read requests are made to a specific Memory Module by transmitting the 12-bit address of the desired word to that module. One microsecond after the completion of this transmission, the desired word is in the module's data register; word regeneration and transmission of the word, 12 bits at a time, proceeds in parallel. The complete cycle is accomplished in four microseconds. Similarly, the complete cycle for writing new information into memory—including the transmission to memory of both the word address and the data—requires but four microseconds.

There are five buses in the basic D825 system capable of exchanging information between the Memory Modules and the Computer and I/O Control Modules. If each bus is exchanging information with a different Memory Module, all buses can simultaneously exchange information with memory at a rate of one 48-bit word per bus per four microseconds, or 250,000 words per second, or 2,000,000 characters per second.

Because of this unique memory-sharing technique, it is conceivable that two or more buses might simultaneously request the same Memory Module. Should this rare short-term conflict develop, it is automatically resolved by a priority scheme based on a predetermined sequence. No delay is longer than four microseconds—the average is 2 microseconds.



INPUT/OUTPUT CONTROL MODULE

The I/O Control Module consists essentially of control and data manipulation registers and associated decoding and timing circuits. Each is capable of controlling all devices in the I/O complement; there can be as many simultaneous I/O operations as there are I/O Control Modules. The I/O exchange automatically connects Control Modules with specific I/O devices on command from Computer Modules. After giving the command, the Processor is free to work on something else at clock rate and no valuable time is lost in waiting for a slow I/O device. Each I/O Control Module can transmit and receive data to and from memory at a rate of two million characters a second. I/O devices with speeds in excess of 500 kc are easily handled.

The D825 system can accommodate up to 10 I/O Control Modules for each memory bus allocated to I/O. The I/O Control Modules are capable of controlling 32 input and 32 output channels or up to 64 external devices (and many more by multiplexing). The execution of a "Transmit to I/O" instruction by a Processor Module causes the transmission of a 48-bit I/O descriptor (I/O instruction word) to the first available I/O Control Module. The instructed Control Module then decodes its descriptor and acts accordingly.

There are two word registers in each I/O Control Module—one for transmission and reception of data to and from memory and one for the packing and unpacking of data to and from I/O device. Sufficient control circuitry for the registration and utilization of the control word is included.

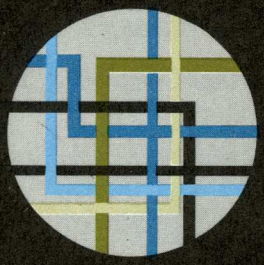
Each time a memory location is transferred, the transfer count is stepped down and the memory location count is stepped up. When an I/O operation is terminated, a result descriptor is generated containing the I/O device designation, the last memory location transferred plus one, the number of locations left to be transferred, the operation being performed, and the reason for the termination.

This result descriptor is made available to the system for further action. An I/O completion interrupt is also set and the system is thus signaled. Appropriate action is then taken by the executive program (Automatic Operating and Scheduling Program).

The communication between an I/O Control Module and external devices proceeds at a rate determined and controlled by the external device.

Each I/O Control Module requests service over the I/O-memory bus for only the actual time (four microseconds) required to transmit a memory address and a data word. Circuitry automatically resolves short-term conflicts between different I/O Control Modules requesting the same bus in a manner analogous to the case of different trunks requesting the same memory module. This conflict resolution, based on a predetermined sequence, is essentially zero-time since the bus is capable of a 250-kilocycle data word rate even when communicating with a number of I/O Control Modules.

SWITCHING INTERLOCK ORGANIZATION

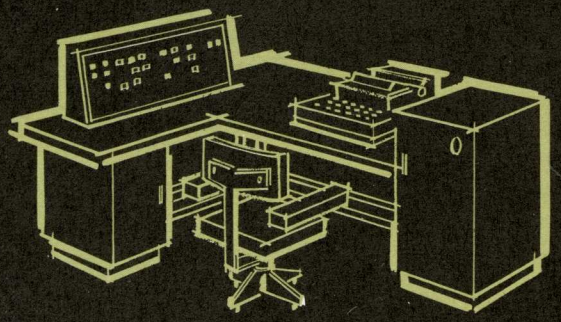


The Switching Interlock is the *organization* of circuitry in the D825 responsible for all data flow. It provides automatic control of intermodule communications and interrupt signals between the Computer Modules, Memory Modules, and Input/Output Control Modules. Primarily a circuitry matrix, it is not, therefore, an integrated piece of hardware. If there is a Switching Interlock failure in any one module, only its function for that unit is impaired. One of the principal features of this unique Interlock system is that it permits totally *parallel* operations. Each Computer Module has exclusive use of a data transfer bus by which it can communicate, via the Switching Interlock, with any Memory Module in the system. The I/O Control Modules of an I/O exchange share a single bus; an additional exchange on a separate bus is available in one-, two-, and three-computer systems.

Memory Modules may be used concurrently by all Computer and I/O Control buses. If two or more buses simultaneously address the same Memory Module, the Switching Interlock automatically resolves the conflict according to priority and queues the lower priority items. One Module gains immediate access while the other is delayed only until completion of the first memory transfer. It resolves communication conflicts, therefore, by *scheduling* rather than by buffering—without the normal buffering delays.

The D825 Switching Interlock Organization, together with other features of this unique system, relieves the operator of many burdensome tasks that complicate operation of conventional computers. The D825 system design and organization require a minimum of instructions and increase the collective capabilities of man and machine.

OPERATOR'S STATUS DISPLAY CONSOLE AND KEYBOARD PRINTER



Through the Keyboard Printer located by the Operator's Status Display Console, queries and interrupts can be effected with little interference of the task in process. The console provides a compact status display and power controls for all modules in the system. The console also houses the system's over/under voltage detector which detects and signals excursions of primary power beyond fixed voltage limits. This signal allows the Computer Module to store necessary information which is automatically fed back into the system when power is restored and the program restarted. The power supplies have time-constants sufficient to protect the hardware, program, and data from all primary power transients and failures and allow continuation of the program when stable primary power is restored.

It is significant to note that the Keyboard Printer is connected to the system through the I/O exchange as are all other I/O devices thus giving simplicity and flexibility to system organization and arrangement.

D825 AUTOMATIC OPERATING

. . . AN EXECUTIVE PROGRAM FUNCTIONALLY COMBINING

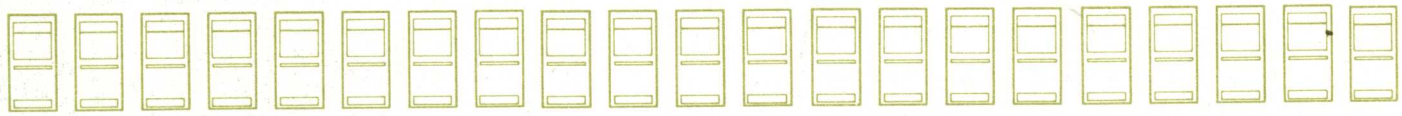
The D825 modularity concept is clearly far more than a geometric concept. Designed to perform multiple and parallel data processing at throughput speeds approaching real time, the modular complex—composed of independent Computer, Memory, and I/O Control Modules—is completely responsive to the changing requirements of military-oriented computer applications. Therefore, unprecedented reliance is placed in the Automatic Operating and Scheduling Program (AOSP). The D825 AOSP is a dynamic executive program with a multitude of critical responsibilities—not just a package of passive utility routines. It has three primary functions. First, it provides operational modularity to modular hardware. Second, it provides system unity for real-time response. And third, the AOSP coordinates modules without the vulnerability associated with systems in which coordination is performed by a unit of hardware.

OPERATIONAL MODULARITY

Since real-time applications are so important, the D825 system as a whole was designed to function even though individual modules might malfunction. In the event of unexpected module shutdown, programs are transferred automatically to other modules in accordance with established priorities. Basic design further permits identical programs to be run on separate D825 systems with the same or different module configurations. Built-in flexibility is also achieved by use of identical modules which can be easily added or excluded without system interruption and without costly reprogramming.

To provide this operational modularity, AOSP:

- Maintains records of current system configuration
- Receives, decodes, and processes external requests to modify system configuration records
- Selects available Computer Module, memory space, I/O device, and secondary storage for each specific program
- Furnishes adaptations which link different programs and data blocks with separately allocated memory locations
- Maintains records of memory space available for allocation to new run requests
- Maintains a program of routine confidence testing of hardware modules to anticipate possible malfunctions



AND SCHEDULING PROGRAM

HARDWARE AND SOFTWARE FOR REAL-TIME APPLICATIONS

UNIFIED SYSTEM BALANCE

The D825 functions as a unified system even though it is composed of individual modules. External requests are not addressed to particular Computer, Memory, or I/O Control Modules—they are presented to the system as a whole. The request states the program, the data, and the priority; then the entire system, under the guidance of the AOSP, provides the unified timeliness to the real-time response.

To ensure system unity, AOSP:

- Responds to external request interrupts
- Administers the input and output of messages and data between the system and external stations
- Maintains a system of priorities and selects tasks to be performed on the basis of this priority
- Maintains master files of system facilities such as a library of production programs, service programs, standard subroutine procedures, and permanent data objects; adds and deletes items from master files
- Records data objects and action requests introduced to the system; eliminates them when not needed.
- Administers the use of the system's real-time clocks

MODULE COORDINATION

The basic philosophy and design objective was to make all D825 Computer Modules identical and independent to provide parallel processing, dynamic operation, and flexibility—and to avoid reliance on any one portion of the system. But because each Computer shares all Memory Modules and has equal access to any I/O device, computer operation must be coordinated to avoid duplication of effort. Without direction, each Computer would rush to answer all interrupt signals and do the highest priority jobs as if it were the only Computer in the system.

AOSP furnishes the necessary coordination to prevent this duplication of tasks. Through AOSP control: (1) two or more Computer Modules can without mutual interference simultaneously execute the same program using different data; (2) the same Computer Module can execute two or more incarnations of the same program, reactivating the different versions in turn; (3) parallel operations can be effected when Computer Modules are available, although serial operation will be utilized when Computers are in demand for higher priority tasks; (4) no two Computers will answer the same interrupt signal or run the same program unaware of the other's participation; (5) Computers will not inadvertently write into another's data area; and (6) two or more Computers (or programs) can use the same copy of a common subroutine or refer to data in a common table.

To accomplish this coordination, AOSP:

- Maintains records showing current action on programs, standard subroutines, or tables; prevents multiple usage when necessary
- Responds to program-generated signals to ready a program, subroutine, or data object—bringing it into main memory if desirable
- Establishes a separate data area and working storage area for each requested new use of programs involving new data
- Arranges to save necessary information when a running task is suspended for one of higher priority
- Enlists additional Computer Modules when a branch point is reached in parallel computation
- Maintains necessary records to cause suspension of processing until converging branches are processed
- Assigns and maintains the settings of Computer mask registers to see that desired interrupt lines are monitored by appropriate Computers, prevents duplicate monitoring, and assigns most monitoring to the Computer running the lowest priority task
- Loads memory limit registers of each Computer in accordance with the location in memory of the data area assigned to the Computer's current task so that hardware can prevent that Computer from inadvertently writing outside these limits.

AUTOMATIC INTERRUPT CAPABILITY

One of the most powerful and dynamic features of the D825 is its Interrupt system. This Interrupt system is the built-in electronic facility by which the entire D825 complement can signal the Automatic Operating and Scheduling Program (AOSP) that control of some type is needed or that some element of the system is not operating properly. It provides the facility for interrupting the "normal" data processing mode of operation.

Each D825 Computer Module contains its own interrupt register and mask register. Of the 12 unique interrupt conditions (see below), the first two require neither mask nor interrupt register bits. These two conditions are of the highest priority and lead to the automatic and immediate processing of the interrupt. The other interrupt conditions are handled by the AOSP. The interrupt mask register in each Computer Module is set by the AOSP to indicate which interrupts each module will process.

When a computer is running an object program and senses a ONE in an interrupt register position, it immediately processes the appropriate interrupt as soon as it completes the current instruction.

An interrupt condition causes transfer of control of the interrupted Computer Module from the object program to the AOSP. Decoding the interrupt condition at hand, the AOSP transfers control to the appropriate routine for handling the condition. When the interrupt condition has been satisfied, control is returned to the interrupted object program or to a newly introduced object program.

In the event of a primary power failure, storage circuits maintain dc supply voltages at normal levels for a period following the failure detection. During this time, the contents of all appropriate registers, including all I/O descriptors, are stored automatically for future recall. After power is restored, the object program is automatically restarted.

Interrupt conditions occurring simultaneously are handled in a predetermined sequence; interrupt conditions which occur while an earlier interrupt is being processed are held momentarily.

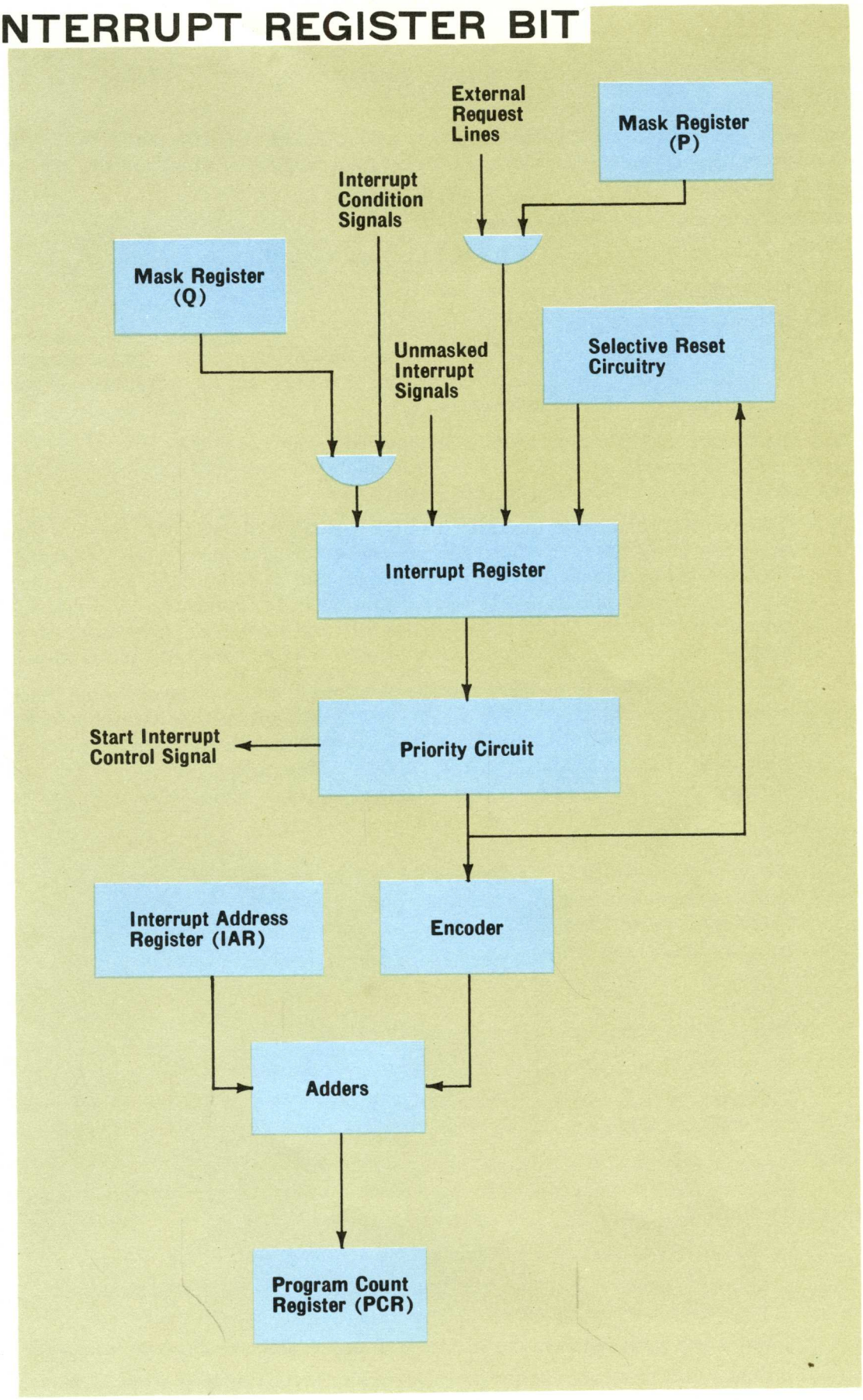
There are 12 specific conditions which can cause an interrupt. The following list shows them in the order of processing priority:

1. **Primary power failure**
2. **Increment real-time clock**
3. **Restart after primary power failure**
4. **16 external requests (all masked)**
5. **I/O termination (masked)**
6. **Interrupt Processor N**
7. **Real-time clock overflow (masked)**
8. **Write out of bounds**
9. **Illegal instruction**
10. **Internal parity error**
11. **Arithmetic overflow (masked)**
12. **Normal mode halt instruction**

Mask registers are "set" in the Processor Modules by the AOSP so that only selected interrupt conditions will be processed by a particular Processor. System interrupt conditions can be assigned to any Processor in the D825 system—depending on the workload and urgency of the request.

The D825 interrupt system provides the means by which total D825 system control responds to the external environment or equipment malfunction.

TYPICAL INTERRUPT REGISTER BIT



D825 PROGRAMMING FEATURES

Burroughs D825 Modular Data Processing system was designed to simplify programming, thereby reducing total throughput time for any given program.

To achieve this capability, compilers for ALGOL-60, JOVIAL, COBOL, and FORTRAN are an integral part of the software complement of the D825. These program languages, which are the link between the user and the system, provide:

- reduced programming time and costs
- reduced compiling time (for ALGOL, JOVIAL, and COBOL)
- efficient object programs
- easy program debugging

For those D825 applications which appear to be best accomplished by machine language programming, the D825 offers a versatile zero-, 1-, 2-, or 3-address feature that offers all the advantages of computers having a single capability, but none of the related drawbacks.

The major features of D825 programming are covered below.

VARIABLE ADDRESS PROGRAMMING

Efficiency is promoted in the D825 with the capability of zero-, one-, two-, or three-address programming according to the needs of a particular instruction. This capability takes advantage of the fact that many fundamental operations involve three factors, and therefore may require three storage locations. The classic example is "add A and B; store the results in C." Single address programming would require three separate instructions: "clear and add A; add B; and store in C." Conversely, in a system with only three-address programming, an unconditional transfer uses only one syllable and wastes the other two.

The object program in memory consists of blocks of 48-bit program words. Each program word consists of four syllables. The advantage of the D825 system instruction lies in the fact that the instructions are considered as "strings of syllables" which vary in length from one to seven syllables per instruction. Also, an instruction can begin at any syllable location in the memory word and end with the same or any succeeding syllable of the memory word or can continue on into as many as two succeeding memory words.

FOUR-LEVEL OPERAND STACK

An important feature of the D825 is the fast access, thin-film operand stack. Operands which are used again and again can be kept in the stack and addressed in a shorter time than would be required to obtain an operand out of memory. The stack is effectively a 4-word circular memory with the top of the stack being an implicit address.

INDEXING

D825 indexing implements two processes:

- The automatic modification of an address by adding the contents of one, two, or three index registers
- The modification, by instruction, of the contents of an index register by comparing with the contents of a specific limit register and transferring program control to the appropriate location

A special feature of the D825 is "multiple indexing"—adding the contents of up to three index registers to the address when necessary to maintain more than one separate index in computing the addresses of operands in an array.

Other features of the D825 indexing system are as follows:

- An ample quantity of index and limit registers (15 each) located in thin film, independent of program or data locations in memory
- Index and limit registers are 16 bits each and contain an absolute memory address
- Contents of index and limit registers are unsigned quantities; if a "negative address modifier" is desired, the two's-complement "positive address modifier" will serve the same purpose

RELATIVE ADDRESSING AND INDIRECT ADDRESSING

The D825 has the capability for infinite levels of indirect addressing followed by indexing at the last level.

Normally, a program for the D825 is contained in a block of contiguous memory locations. The address of this location is placed and retained in a thin film register called the Base Program Register (BPR). Any transfer of control adds the literal specified in the branch syllable to the BPR and places this sum in the Program Count Register, another thin film register. Thus, transfers are specified to locations relative to the beginning of the program block and the program may be loaded and executed in any position in memory with no modifications of branch addresses and no wasted indexing.

Direct handling of card decks and other kinds of input on the part of the central system is made possible by the D825's automatic relative addressing hardware. No matter where a program is put in memory, it can be immediately executed without any Computer first having to perform an address-fixing pass over the program instructions. Relative addresses are converted to proper absolute addresses during instruction execution. To each relative address in the program being executed, the D825 automatically adds the base address found in the base address register (data) or the base program register (branch addresses). These base addresses are set by the AOSP when it readies a program for execution. The D825's automatic relative addressing makes it unnecessary for the user to choose between having address-fixing performed off-line and having it take computer time on-line. There simply is no address-fixing required in the D825. Off-line equipment and use of the main computer for address fixing are both eliminated.

FIELD-DEFINED INSTRUCTIONS

A set of field-defined instructions is provided to facilitate code conversion and multiple use of a memory location. A field is a set of physically adjacent 6-bit characters in fixed locations in a word. The ability to perform simple arithmetic, manipulation, and comparison on such fields is available.

SUBROUTINE CONTROL

The capability to transfer control to a remote subroutine, and to return, is provided in the D825. This transfer of control enters a subroutine indirectly through a list of all subroutine addresses. The list is specified by the Subroutine Base Address Register. This feature eases the bookkeeping required to relocate a subroutine. An index register is set by the computer logic to allow the addressing of constants in the subroutine area. The ability to locate the working-storage area of subroutines is provided by the instruction logic. It is possible to have several computer modules independently and simultaneously execute a subroutine through the use of independent direct address areas.

INSTRUCTION SYLLABLES

There are 18 types of syllables used in D825 machine language programming, including the operator syllable, index syllable, memory address syllables, and special-use syllables. All syllables are 12 bits in length.

Only the OPERATOR syllable is required for every instruction. It identifies any syllables that may follow and any stack usage for the instruction.

The INDEX syllable can be used with any other syllable except the index syllable itself, the operator syllable, or any syllables used in a repeated instruction. In all cases, use of the index syllable is optional. The contents of up to three index registers can be applied to one syllable. When a syllable is indexed, it is immediately preceded by its index syllable. In indexed indirect-addressing, the contents of the index registers are applied to the last-level address only.

The MEMORY ADDRESS SYLLABLE is used to address data words in memory. The relative address is added to the contents of the Base Address Register (BAR) to obtain the effective memory address. Each level of indirect addressing after the first contains an absolute address and therefore is not added to the BAR.

D825 INSTRUCTION EXECUTION TIMES AND TIMING ALGORITHMS

The following times are presented to indicate the speed of the D825. They do not take into consideration the important multi- and parallel-processing features of the D825. Only the primary program operations are shown.

Typical Instruction Execution Times (in Microseconds)

BAD: Binary Add	1.33	—signs alike
	2.00	—signs different
BMU: Binary Multiply	24.00 + 0.67n	—(n = number of 1's in the multiplier excluding 1's in bit positions 1, 12, 24, 36, 48)
BSU: Binary Subtract	1.33	—signs different
	2.00	—signs alike
CBF: Convert Binary Floating Point	1.33 + 0.33n	—(n = number of shifts-left needed to normalize)
	0.33	—if the number is zero
FAD: Floating Add	6.67 + 0.33(n+m)	—(n = number of shifts-right needed in units of 1, 6, 12 bits for lining up the operands and m = number of shifts-left needed to normalize the result)
	2.33	—signs of the exponents of the two operands are different, and the absolute value of the sum of the two exponents is greater than 2,047
FMU: Floating Multiply	21.00 + 0.67n + 1.33	—if normalization of 1 position is necessary (n = number of 1's in the mantissa of the multiplier, excluding 1's in bit positions 1-13, 24, 36, 48)
	1.67	—exponent overflow or underflow has occurred
FSU: Floating Subtract	6.67 + 0.33(n+m)	—same as FAD above
	2.33	—same as FAD above

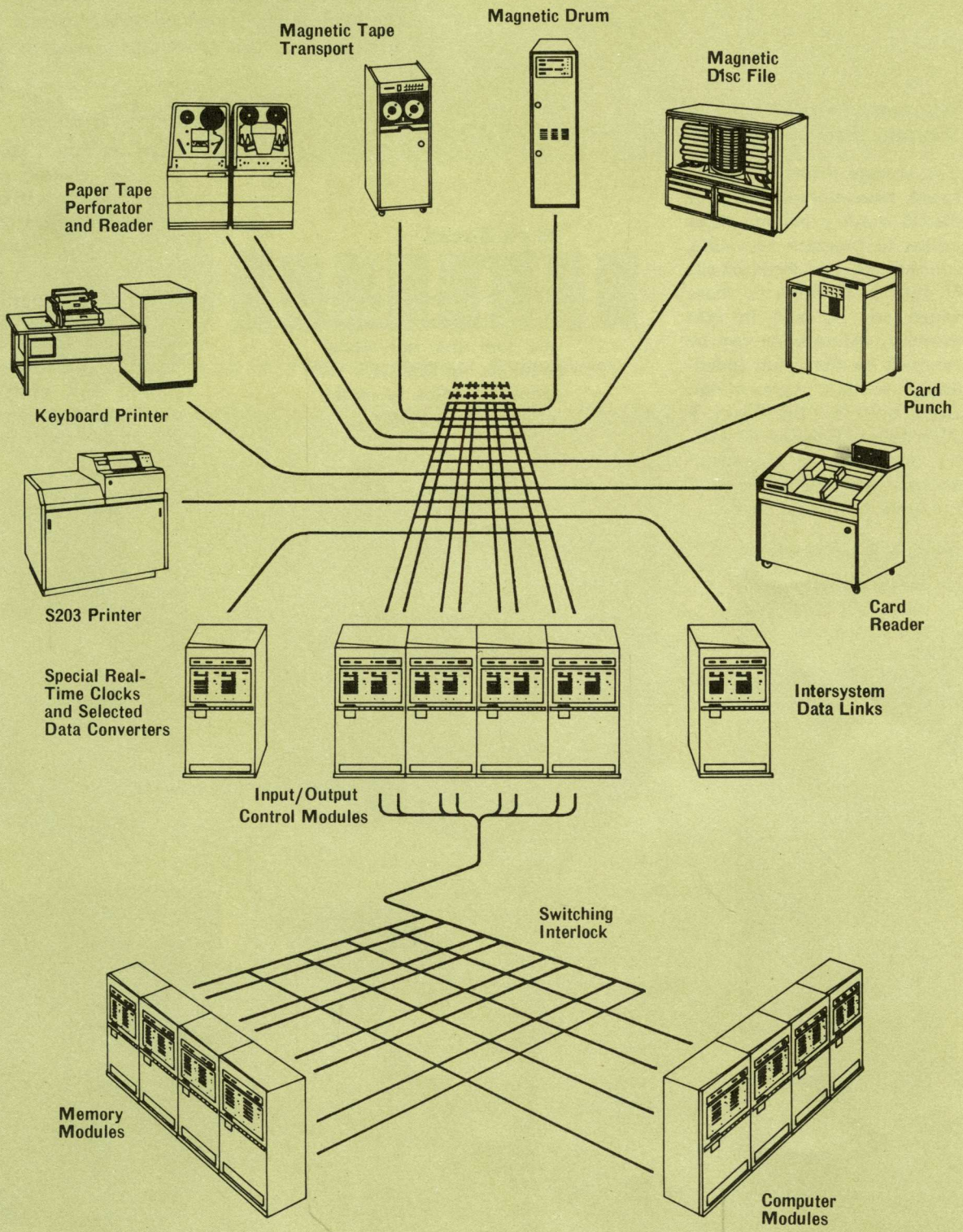
Timing Algorithms (in Microseconds)

+2.00—stack read*
+1.67—stack write
+4.00—level of indirect addressing**
+1.67—per repeated instruction***
+Individual processing time for each type of syllable used:
  1.33—program operator syllable
  5.33—memory syllable (read)
  4.33—memory syllable (write)
  0.33—branch (if executed)
  0.67—branch (if not executed)
  1.67—index syllable
  1.67—other type of syllable
+5.00—program word (fetch**)
−5.00—program word (fetch overlap)
Plus the sum of instruction execution times.

Typical Subroutine Execution Times

Sin X (22-bit accuracy)	=195 microseconds
Sq Rt X (24-bit accuracy)	=212 microseconds
Arc Tan X (26-bit accuracy)	=435 microseconds

*0.33 for a stack read if it follows a stack write of the preceding instruction
**counted only the first time if repeated
***not counted the first time



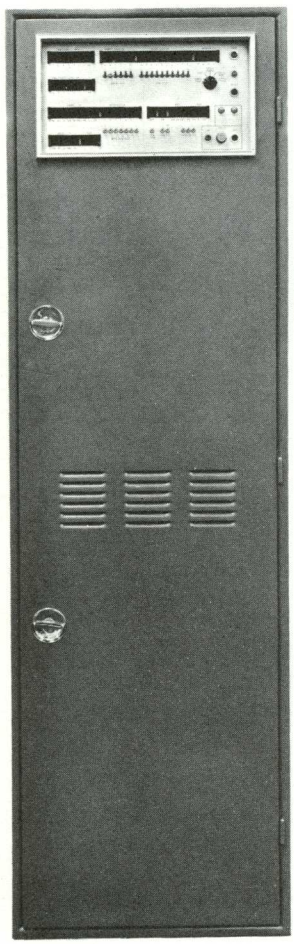
Possible System Organization of Burroughs D825 Modular Data Processing System

INPUT/OUTPUT DEVICE COMPLEMENT

All I/O peripheral equipments are independent of the Computer Modules. They are governed exclusively by the I/O Control Modules, which in turn communicate with the Computer Modules via the Switching Interlock organization. The distinct advantage of this switching arrangement is that the

Magnetic Drum Storage Unit

The storage drum is a high-speed, mass-storage device of 65,536 words providing rapid access to program segments, subroutines, and large blocks of data in addition to those which can be held in core memory. Information can be retained on the drum indefinitely without regeneration. Each word on the drum is addressable. Reading or writing may start at any drum address. Average access time is 8.5 ms in a single band.

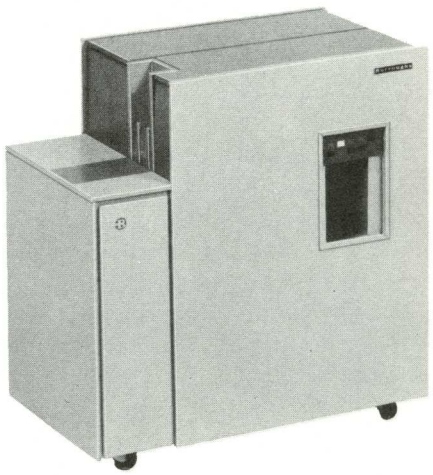


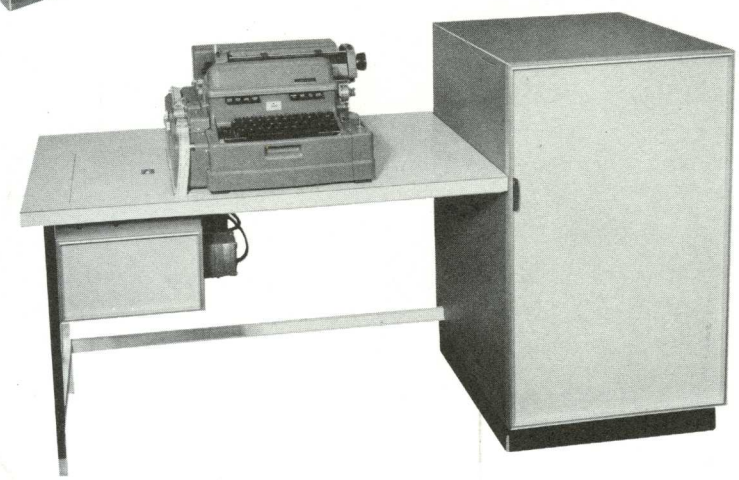
High-Speed Printer

This high-speed printer has 120 print positions per line and full alphanumeric characters. It prints at rates in excess of 600 lines a minute.

Card Punch

The Card Punch Module feeds, punches, checks, and stacks 80-column cards in both standard and postcard thicknesses. Double-punch and blank-column detection units are available in groups of 20 as optional devices. The punch contains a single-panel plugboard for the wiring of double-punch and blank-column checking. Punching speeds are 100 or 300 cards per minute.





Keyboard Printer

This is the medium of communication between operator and the D825 system. The D825 instructs and answers the operator through this printer; the operator initiates inquiries and instructions to the system's Automatic Operating and Scheduling Program through the keyboard and acknowledges instructions.

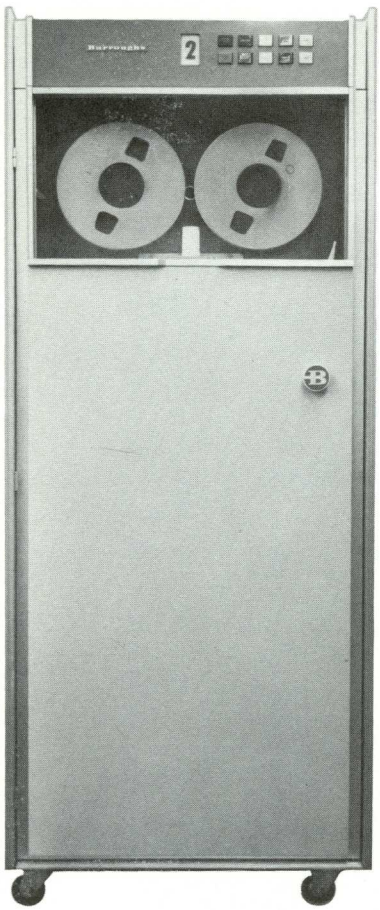
I/O Control Module, operating at system clock rate, can instantaneously channel input or output data at the moment needed. Since the I/O devices, operating at widely divergent rates, are never directly connected with the Computer Modules, I/O delays are avoided.

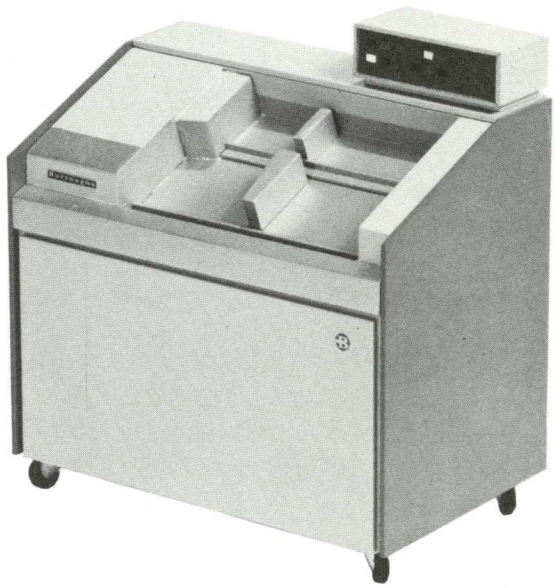
Versatility is another advantage of the unique D825 system design. Any known I/O device can be readily integrated into the system, since total throughput of the D825 is not dependent on any one I/O device. Design of the D825 consequently permits immediate integration of any existing I/O device, up to a maximum of 64, regardless of speed or mode of operation.

Typical Burroughs I/O Devices available for the D825 System are described on the following two pages.

Magnetic Tape Unit

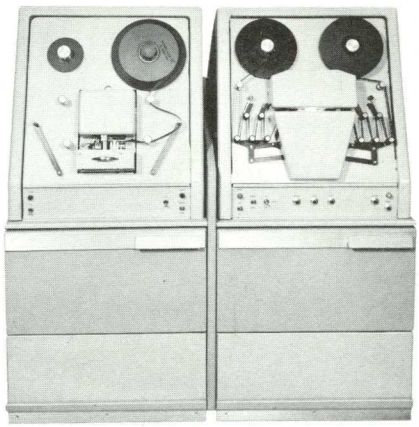
This unit accepts data in either binary or single-frame alphanumeric form. The tape unit operates in either local or remote mode. The tape transfer rate is 66,660 characters per second.





Card Reader

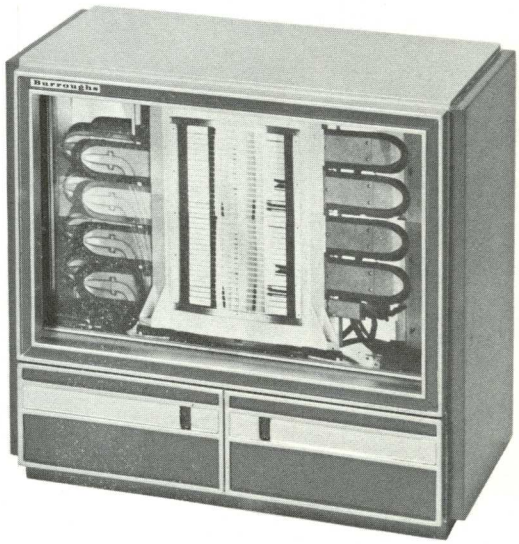
This "end-fed" reader accepts cards of 51, 60, 66, or 80 columns at the rate of 800 cards per minute. Information is read serially, column by column. Card data may be represented in standard tabulating card code or straight binary code. Cards can be added or removed while the reader is operating.



Paper Tape Punch/ Paper Tape Reader

The Paper Tape Punch has the capability of punching standard seven-hole paper tapes at 110 characters a second.

The Paper Tape Reader reads standard seven-hole paper tapes at 1,000 characters a second and can stop on a single character.



Magnetic Disc File

The Magnetic Disc File is a mass storage semi-random device that stores up to three million 48-bit words. Average access time is 158 ms. A similar model that provides three access channels to the file is available.

APPLICATIONS

As the preceding pages have indicated, the Burroughs Military-oriented D825 Modular Data Processing System was conceived, designed, and developed for one specific objective: to fulfill the computational requirements of present and future military and space applications.

A typical example of the growing complexity of tasks computers must perform in military applications is the intricate and diverse problems encountered in a command and control operation. Although command and control missions vary with individual operations, to be sure, certain basic needs are similar to all such missions and can be used as a basis for evaluation.

To readily perform the computing demands of even a routine command or control situation, it is mandatory that:

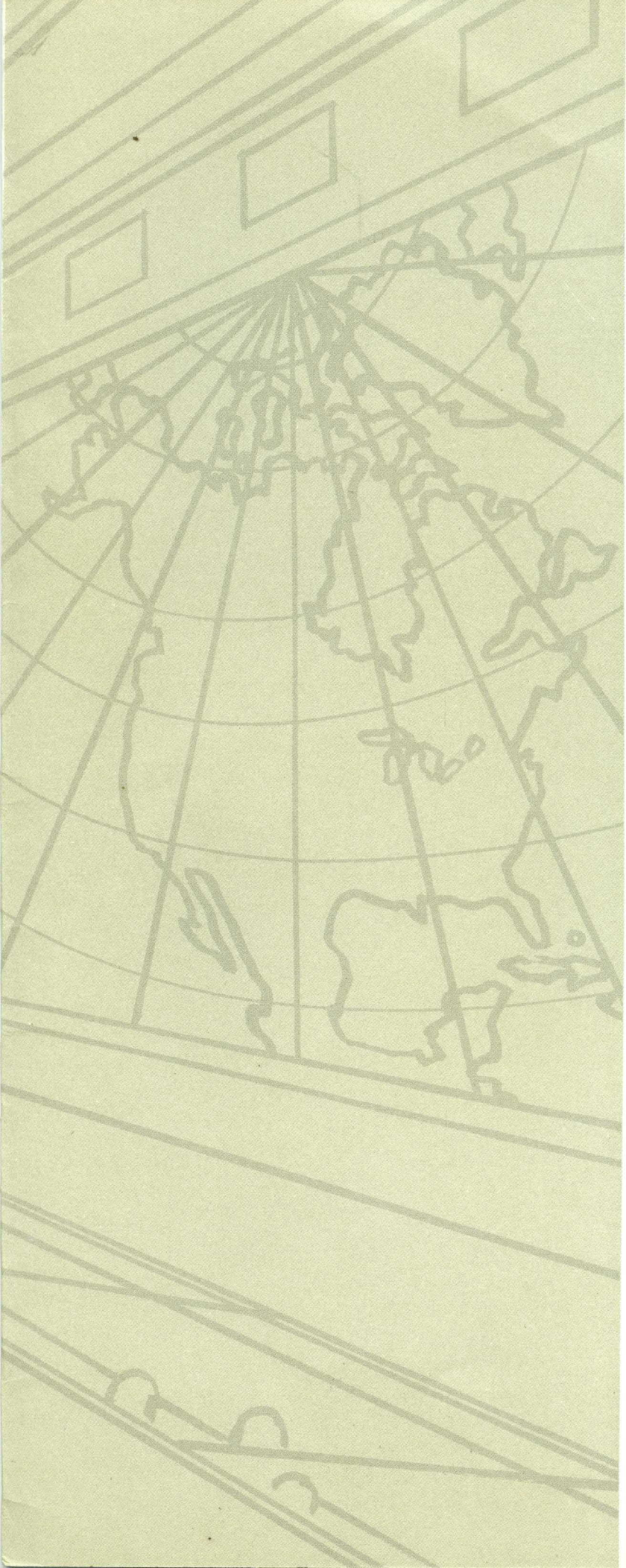
- Hardware be designed to permit system growth as requirements grow —without time-consuming or costly reprogramming.
- Equipment complements and programming languages be compatible with other intra- and inter-service systems.
- Real-time operation be virtually continuous with almost perfect reliability—even in the event of destruction or degradation of some system elements.
- Inter-system flow of sensitive data, either processed or stored, be automatically protected and controlled.
- System hardware be inherently flexible to adapt to a multitude of varying problems and existing systems and devices.
- System hardware never be input/output bound.

The D825—with its tailor-made module configuration, programming ease and versatility, parallel processing, automatic diagnostic routines, high-speed thin-film "scratch pad" memory, and totally shared main Memory Modules—easily fulfills all requirements.

In command *or* control situations, however, there is one more vital factor —the relationship between man and machine. Man-machine compatibility in the D825 is unique and comprehensive. The machine supplements human effort and complements man's capabilities; but man retains sole responsibility for decision-making. The D825 can translate from command to machine language and back to understandable displays.

In addition to the variety of command and control applications, the D825 is ideally suited for scores of other military-related assignments. The D825, for example, can perform such complex tasks as missile guidance, predictions of missile tracks and satellite orbits, or rendezvous interception points. The D825 also can be applied easily to the total supervision of multi-missile and satellite systems. It is also well-suited for scientific applications, communications systems, air and space surveillance and traffic control systems, and weather data collection and reporting systems. Another major application is as a mission and trainer simulator.

The first two customers to receive Burroughs D825 Modular Data Processing systems were the U. S. Naval Research Laboratory—and the U. S. Air Force Systems Command which utilizes D825's as an integral part of the BUIC (Back-Up Interceptor Control) program, an emergency control program for continental air defense.



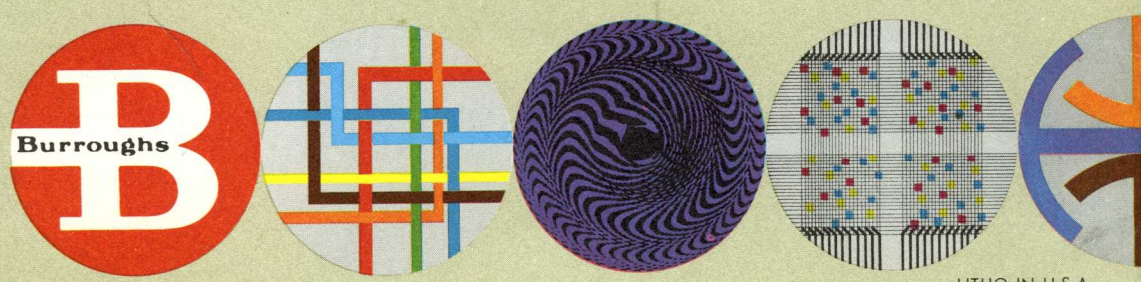
It is assumed this brochure has prompted as many questions as it has attempted to answer . . . questions that would be difficult to predict and answer in a semi-technical brochure of any size.

For additional information—or to make arrangements for a personal inspection and demonstration of the D825—you are invited to contact any Burroughs Defense and Space Systems Marketing representative, or write:

Vice-President
Defense and Space Marketing Division
Burroughs Corporation
Paoli, Pennsylvania

Burroughs Corporation

Defense and Space Systems Marketing, PAOLI, PA.



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