Ł BURRCUGHS CORPORATION 1997 5390 + SYSTEM DEVELOPMENT GROUP PASADENA PLANT **V SERIES INSTRUCTION SET** ł + REV. A COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION PAGE 1 ----______ م م <u>ف م</u> ----

TABLE OF CONTENTS

	1	INTRODUCTION	2
	1_1	PREFACE PAGE 12	2
	1.2	RELATED SPECIFICATIONS	2
	1.3	GENERAL DESCRIPTION	
	2	DATA REPRESENTATION PAGE 13	
		SIGNED NUMERIC FORMAT (SN)	
		UNSIGNED NUMERIC FORMAT (UN)	
		UNSIGNED ALPHA FORMAT (UA)	-
		INSTRUCTION REPRESENTATION	•
	3.1	INSTRUCTION FORMAT	-
	3.2	ADDRESS RESOLUTION PAGE 19	
	3.3	OPERATOR CODE	-
	3.4	FIELD LENGTH PAGE 28	-
	3.5	INSTRUCTION OPERAND OVERLAP DEFINITIONS PAGE 35	
	4	PROCESSOR STATE	-
	4.1	INTERNAL PROCESSOR STATE	
•	4.2	OVERFLOW FLAG.	5
	4.5	COMPARISON FLAGS (COPH, COML)	j.
	4-4	MODE INDICATORS PAGE 43	5
	4.5	MEMORY ERROR REPORT ENABLE	5
	4.6	SNAP FICTURE ENABLE	Ś
	4.7	TASK TINER	7
	4.8	KERNEL MODE	3
	5	TASK ADDRESSING ENVIRONMENT	Ś
	5.1	TASK ADDRESSING CAPABILITIES	
	5_2	REINSTATE LIST	
	5.3	ENVIRONMENT TABLE.	
	5.4	MEMORY AREA TABLE.	
	5.5	MEMORY AREAS	
	5.6	MEMORY AREA STATUS TABLE (MAST)	
1	5.7	LOCATING A MEMORY AREA TABLE ENTRY PAGE 53	-
	5.8	RESOLVING A MEMORY AREA TABLE ENTRY PAGE 5	
		LOADING A MEMORY AREA TABLE	-
			-
	6		-
	6.1	INTERRUPT PROCEDURE (INP)	
	6.2	HARDWARE CALL PROCEDURE (HCP)	
	7	INSTRUCTION SET SUMMARY	
	8	ARITHMETIC; FIXED POINT, VARIABLE FIELD LENGTH . PAGE 82	
	8.1	TWO ADDRESS ADD (INC)/OP=01	
	8.2	THREE ADDRESS ADD (ADD)/OP=02	-
	8.3	TWO ADDRESS SUBTRACT (DEC)/OP=03 PAGE 89	9
	8.4	THREE ADDRESS SUBTRACT (SUB)/OP=04 PAGE 94	4

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BURROUGHS CORPORATION	+	 + 1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION S	SET
CCMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	A PAGE 2

+4

TABLE OF CONTENTS

2.5	MULTIPLY (MPY)/OP=05 PAGE	97
8.6	DIVIDE (DIV)/OP=06	100
9	ARITHMETIC; FIXED POINT, FIXED FIELD LENGTH PAGE	105
9.1	INTEGER LOAD (ILD)/OP=58	107
9.2	INTEGER LOAD (ILD)/OP=58	109
9.3	INTEGER ADD (IAD)/OP=50	111
9.4	INTEGER ADD AND STORE (IAS)/OP=51	
		113
9.5	INTEGER SUBTRACT (ISU)/OP=52	115
8.6	INTEGER SUBTRACT AND STORE (ISS)/OP=53 PAGE	117
9.7	INTEGER MULTIPLY (IMU)/54 PAGE	119
9.8	INTEGER MULTIPLY AND STORE (IMS)/OP=55 PAGE	121
9_9	INTEGER MEMORY INCREMENT (IMI)/OP=57 PAGE	123
10	ARITHMETIC; FLOATING POINT, FIXED FIELD LENGTH . PAGE	125
10.1	REAL LOAD (RLD)/OP=78 PAGE	127
10.2		
10.3		131
10_4		133
10.5	REAL AUD AND SIGKE (KAS//UF-1) AGE	1.3.3
	REAL SUBTRACT (RSU)/OP=72 PAGE	135
14.0	REAL SUBTRACT AND STORE (RSS)/OP=73 PAGE	137
10.7	REAL MULTIPLY (RMU)/OP=74 PAGE	139
	REAL MULTIPLY AND STORE (RMS)/OP=75 PAGE	141
10.9	REAL DIVIDE (RDV)/OP=76 PAGE	143
10.10	REAL DIVIDE AND STORE (RDS)/OP=77 PAGE	145
10_11	ACCUMULATOR MANIPULATE (ACM)/OP=84 PAGE	147
11	ADDRESS BRANCHING	153
11.1	BRANCH/OP=2x	153
12	HALTS DACE	15.6
12.1	HALTS. PAGE HALT BRANCH (HBR)/OP=29. PAGE	157
12.2	HALT BREAKPOINT (HBK)/OP=48.	
13	THE DECENTURY (DEC)/UF-40	158
	ENVIRONMENT CHANGE PAGE	159
15-1	BRANCH COMMUNICATE (BCT)/OP=30 PAGE	159
13 13.1 13.2 13.3	ENTER (NTR)/OP=31	163
13.3		166
13.4	VIRTUAL ENTER (VEN)/OP=35	168
13.5	HYPER CALL CHCLJ/OP=62	172
13_6	RETURN (RET)/OP=63	176
13.7	ADJUST STACK POINTER (ASP)/OP=61 PAGE	181
13.8	INTERRUPT (INT)/OP=90 PAGE	
13.9	VIRTUAL BRANCH REINSTATE (BRV)/OP=93 PAGE	183
14	DATA MOVEMENT	185
	NOVE DATA (MVD)/OP=08	
		185
14.3	MOVE LINKS (MVL)/OP=09	188
1997 - 194 - J an	MOVE ALPHA (MVA)/OP=10	191
		ata-

BURRCUGHS CORPORATION		+				1997 5	390
SYSTEM DEVELOPMENT GRO Pasacena plant	UP	in de la companya de La companya de la comp La companya de la comp	SERIES	INSTRUCT	TION SET		
COPPANY CONFIDENTIAL	SYSTEM	DESIGN	SPECIF	ICATION	REV. A	PAGE	3

TABLE OF CONTENTS

	14.4	MOVE NUMERIC (MVN)/OP=11	N., 199
	14.5	MOVE WORDS (MVW)/OP=12	
	14-6	MOVE WORDS AND CLEAR (MVC)/OP=13 PAGE 208	
	14.7	MOVE REPEAT (MVR)/OP=14	
	14 8	TRANSLATE (TRN)/OP=15	
	14.0	EDIT (EDT)/OF=49	
	15	LOGICAL	
	15 1	SCAN TO DELIMITER - EQUAL (SDE)/OP=16 PAGE 232	
		SCAN TO DELIMITER - UNEQUAL (SDU)/OP=17 PAGE 235	
	15.3	SCAN TO DELIMITER - ZONE EQUAL (SZE)/OP=18 PAGE 238	
		SCAN TO DELIMITER - ZONE UNEQUAL (SZU)/OP=19 PAGE 242	
		SEARCH (SEA)/OP=39	
	15.6	SEARCH LINK LIST (SLL)/OP=37 PAGE 252	
		SEARCH LINK DELINK (SLD)/OP=38 PAGE 257	
		SEARCH LIST (SLT)/OF=64.	,
	15.8	SEARCH TABLE (STB)/OP=66	
		PIT ZERO TEST (BZT)/CP=40 PAGE 274	
	15.10	BIT ONE TEST (BOT)/OF=41 PAGE 276	
		EIT ONE TEST (BOT)/OF=41 PAGE 276 COMPARE ALPHA (CPA)/OP=45 PAGE 278	-
	15.12		-
	15.13	COMPARE NUMERIC (CPN)/OP=46 PAGE 281	
		BIT RESET (BRT)/0P=33	
	15.15	BIT SET (BST)/CP=34	
	15.16	LOGICAL AND (AND)/OP=42	
		LOGICAL OR (ORR)/OP=43	
	15.18	LOGICAL NOT (NOT)/OP=44 PAGE 295	
	16	INPUT/OUTPUT	
	16.1	INITIATE I/O (IIC)/OP=94 PAGE 298	-
	16.2	READ ADDRESS (RAD)/OP=92	
	16.3	SCAN RESULT DESCRIPTOR (SRD)/OP=91 PAGE 301	
	16.4	CONVERT I/O (CIO)/OP=85	
	16.5	I/O COMPLETE (IOC)/OP=98	
. •	17	BINARY/DECIMAL CONVERSION)
	17.1	DECIMAL TO BINARY (D2B)/0P=88)
	17.2	BINARY TO DECIMAL (B2D)/OP=89	2
	18	TIME-OF-DAY TIMER PAGE 31	5
		이 것 같아요. 이 가지 않는 것 같아요. 이 가지 않는 것 같아요. 이 것 같아요. 이 것 같아요. 이 것 같아요.	6
	18.2	READ TIME OF DAY (RDT)/OP=95 PAGE 310 SET TIME OF DAY (STT)/OP=97 PAGE 310 MEASUREMENT	7
	19	MEASUREMENT PAGE 318	8
• • •	19_1	MEASUREMENT OP (MOP)/CP=87	
	20	MISCELLANEOUS	
		ALTER TABLE ENTRY (ATE)/OP=86 PAGE 32	
		LOAD INDEX REGISTERS (LIX)/OP=67 PAGE 330	
	20.3	STORE INDEX REGISTERS (SIX)/OP=68	
	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	STORE INDEA REDISTERS (SIATOF-00	-

1

• 5

---+ 1997 5390 BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT **V** SERIES INSTRUCTION SET 1 +--COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 4 ______ 

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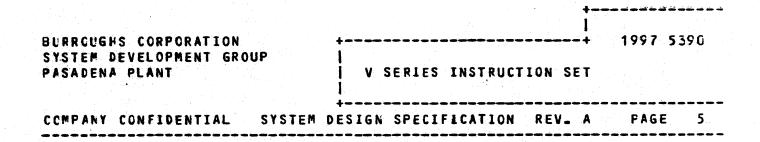
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TABLE OF CONTENTS

	20.4	LOCK/UNLOCK (LOK)/OP=60	PAGE 335	
	20.5	INITIALIZE LOCK/EVENT STRUCTU	RES (ILS)/0P=69 PAGE 348	
	20.6	MOVE LOCK STRTUCTURES (MLS)/0	P=6A PAGE 352	
	20.7	WRITE HARDWARE REGISTERS (WHR	)/OP=65 PAGE 354.	τ
	20.8	SET MODE (SMF)/OP=47		
	20.9	FAIL (BAD)/OP=AB		
	20.10	SYSTEM STATUS (SST)/OP=99.		
	21	STRING INSTRUCTIONS		
	21.1	MOVE STRING (MVS)/OP=A0		
	21.2	COMPARE STRING (CPS)/OP=A1 .	PAGE 369	
	21-3	HASH STRING (HSH)/OP=A2		
	22	RESERVED MEMORY.		
	22.1	KERNEL DATA AREA		
	22.2	RESERVED MEMORY RELATIVE TO T	HE MCP DATA AREA PAGE 377	
		A - COMPATIBILITY NOTES		
	A-01	RELATED SPECIFICATIONS		•
	A.02	CPA		
	A-03	NVA		
	A-04	MVN		
	A.05	BZT, BOT		
	A.06	LSS, EQL, LEQ, GTR, NEQ, GEQ,		
	A.07	MVN, MVC		
	A.08	INC, DEC		
	A.09	ADD, SUB		
	A.10	MPY	PAGE 386	
	A.11	AND, ORR, NOT		
	A.12	SEA	PAGE 388	
	A.13	EQT	PAGE 389	
	A. 14	TRN	PAGE 390	
	A.15	MVR		
	A.16	ARITHMETIC INSTRUCTIONS	••••••••••••••••••••••••••••••••••••••	
	A_17	RAA, RAS, RSU, RSS, RMU, RMS	••••••••••••••••••••••••••••••••••••••	
	A.18	RAA, RAS, RSU, RSS	••••••••••••••••••••••••••••••••••••••	
	A.19	NTR		
	A.20	MVD		
	A_21	MVL	••••••••••••••••••••••••••••••••••••••	
	A.22	MVL. BRT, BST	PAGE 397	
	A.23	SRD	• • • • • • • • • • PAGE 398	
	A.24	COMPATIBILITY		
	A.25		••••••••••••••••••••••••••••••••••••••	
	A-26	SLL/SLD		
	A.27			
	A-28	INVALID LITERALS	• • • • • • • • • • • • • • • • • • •	
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4.



# TABLE OF CONTENTS

A.29	UNDIGITS IN INTERMEDIATE INDIRECT ADDRESSES PAGE 403
A.30	INDEXING ABOVE LIMIT OR BELOW BASE PAGE 403
A.31	MEMORY ERROR REPORT
A.32	BASE INDICANT VALUES
A.33	USER SERVICES MEMORY AREA TABLE ENTRY PAGE 405
A.34	MEMORY AREA TABLE ENTRY FORMATS
A.35	ABSOLUTE ADDRESSES
A.36	TIME OF DAY COUNT RATE
A.37	LOCK/UNLOCK
A.38	REINSTATE LIST ENTRY SPECIFICATIONS PAGE 409
A_40	SST
A.43	DIFFERENT REFERENCES ARE RECALCULATED PAGE 411
A_44	TASK STATE MAINTAINED WITHIN THE PROCESSOR PAGE 411
A.45	TASK TIMER FAULT
A_46	REINSTATE LIST
A_47	MEMORY AREA STATUS TABLE ENTRY
A.48	ENVIRONMENT TABLE ENTRY
A.50	TRACE FAULT DATA
A.51	MEMORY AREA FAULT HARDWARE CALL PROCEDURE PAGE 417
A.52	IMPROPER UNDIGITS IN BRANCH ADDRESS SYLLABLES PAGE 417
A.53	MEMORY ADDRESSABILITY
A.54	HANDLING OF THE SIGN DIGIT IN ILD/IST/RLD/RST PAGE 418

BURRCUGHS CORPORATION	++	997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 6

## OP CODE DIRECTORY BY CODE

OP	Mnemonic	Section	Compatibility Notes
01	INC	8_1	A.08
02	ADD	8-2	A.09
03	DEC	8.3	A_08
04	SUB	8.4	A.09
05	MPY	8.5	A.10
06	DIV	8.6	
08	MVD	14.1	A.20
09	MVL	14.2	A.21
10	MVA	14.3	A.03
11	MVN	14.4	A.04
12	MVW	14.5	A_07
13	MVC	14.6	A.07
14	MVR	14.7	A.15
15	TRN	14.8	A.14
16	SDE	15.1	
17	SDU	15.2	
18	SZE	15.3	
19	SZU	15.4	
20	NOP	11.1	
21	LSS	11.1	A.06
22	EQL	11_1	A.06
23	LEQ	11.1	A.06
24	GTR	11.1	A.06
25	NEQ	11.1	A.06
26	GEQ	11_1	A.06
27	BUN	11.1	
28	OFL	11.1	
29	HBR	12.1	
24	NUL	11.1	A_06
2B	GTN	11.1	A.06
30	BCT	13.1	A.UU
31	NTR	13.2	A.19
32	EXT	13.3	· · · · · · · · · · · · · · · · · · ·
33	BRT	15.14	A-22
34	BST	15.15	A.22
34	VEN	13.4	n an an Anna a Anna an Anna an
37	SLL	15_6	A.26
38		15.7	A.20 A.26
	SLD		
39	SEA	15.5	A.12
40	BZT	15.10	A.05

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 7

# OP CODE DIRECTORY By Code

41       BOT       15.11       A.05         42       AND       15.16       A.11         43       ORR       15.17       A.11         44       NOT       15.18       A.11         45       CPA       15.12       A.02         46       CPN       15.13       A.11         47       SMF       20.8       A.02         46       CPN       15.13       A.13         50       IAD       9.3       A.13         51       IAS       9.4       5         52       ISU       9.5       53         53       ISS       9.6       5         54       IMU       9.7       5         55       IMS       9.8       5         57       IMI       9.9       5         58       ILD       9.1       5         59       IST       9.2       6         61       ASP       13.7       6         62       HCL       13.5       6         63       RET       13.6       6         64       SLT       15.9       6         67       LIX <td< th=""><th>0P</th><th>Mnemonic</th><th>Section</th><th>Compatibility Notes</th></td<>	0P	Mnemonic	Section	Compatibility Notes
42       AND       15.16       A.11         43       ORR       15.17       A.11         44       NOT       15.18       A.11         44       NOT       15.12       A.02         46       CPA       15.12       A.02         46       CPN       15.13       47         47       SMF       20.8       48         48       HBK       12.2       A.25         49       EDT       14.9       A.13         50       IAD       9.3       51         51       IAS       9.4       52         52       ISU       9.5       53         53       ISS       9.6       54         54       IMU       9.7       55         55       IMS       9.8       57         57       IMI       9.9       58         1LD       9.1       59       57         59       IST       9.2       60         10K       20.4       61       ASE         63       RET       13.6       65         64       SLT       15.8       65         65       HRL		BOT	15.11	A.05
43       ORR       15.17       A.11         44       NOT       15.18       A.11         45       CPA       15.12       A.02         46       CPN       15.13			15.16	
44       NOT       15.18       A.11         45       CPA       15.12       A.02         46       CPN       15.13       A.02         46       CPN       15.13       A.02         47       SMF       20.8       A.02         48       HBK       12.2       A.25         49       EDT       14.9       A.13         50       IAD       9.3       S         51       IAS       9.4       S         52       ISU       9.5       S         53       ISS       9.6       S         54       IMU       9.7       S         55       IMS       9.8       S         57       IMI       9.9       S         58       ILD       9.1       S         59       IST       9.2       S         60       LOK       20.4       S         61       ASP       13.7       S         62       HCL       13.5       S         63       RET       13.6       S         64       SLT       20.2       S         67       LIX       20.2				
45       CPA       15.12       A.02         46       CPN       15.13       47         47       SMF       20.8       48         48       HBK       12.2       A.25         49       EDT       14.9       A.13         50       IAD       9.3       51         51       IAS       9.4       52         52       ISU       9.5       53         53       ISS       9.6       54         54       IMU       9.7       55         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         64       MLS       20.6         70       RAA       10.3       A.17, 18 <tr< td=""><td></td><td></td><td></td><td>A_11</td></tr<>				A_11
47       SMF       20.8         48       HBK       12.2       A.25         49       EDT       14.9       A.13         50       IAD       9.3       51         51       IAS       9.4       52         52       ISU       9.5       53         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.5         64       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A		CPA	15.12	A_02
48       HBK       12.2       A.25         49       EDT       14.9       A.13         50       IAD       9.3         51       IAS       9.4         52       ISU       9.5         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.5         64       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.8       A.17			15.13	
49       EDT       14.9       A.13         50       IAD       9.3         51       IAS       9.4         52       ISU       9.5         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.5         64       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         71       RAS       10.6       A.17, 18         73       RSS       10.6       A.17         74       RMU       10.7       A.17	47	SMF	20-8	
50       IAD       9.3         51       IAS       9.4         52       ISU       9.5         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         74	48	HBK		
51       IAS       9.4         52       ISU       9.5         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         73       RSS       10.6       A.17, 18         73       RSS       10.8       A.17         74       RMU       10.7       A.17         75       RMS       10.8       A.17		EDT		A.13
52       ISU       9.5         53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.5         64       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77 <tr td="">       76       RDV       10.1</tr>		IAD		
53       ISS       9.6         54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         71       RAS       10.6       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10<		IAS		·
54       IMU       9.7         55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       ROV       10.9       77         77       RDS       10.10       78         78       RLD </td <td></td> <td></td> <td></td> <td></td>				
55       IMS       9.8         57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79 </td <td></td> <td></td> <td>9-6</td> <td></td>			9-6	
57       IMI       9.9         58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         72       RSU       10.5       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
58       ILD       9.1         59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
59       IST       9.2         60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
60       LOK       20.4         61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
61       ASP       13.7         62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
62       HCL       13.5         63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
63       RET       13.6         64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
64       SLT       15.8         65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         79       RST       10.2				
65       WHR       20.7         66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79				
66       STB       15.9         67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
67       LIX       20.2         68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				· · · ·
68       SIX       20.3         69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17, 18         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10         78       RLD       10.1         79       RST       10.2				
69       ILS       20.5         6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         79       RST       10.2				
6A       MLS       20.6         70       RAA       10.3       A.17, 18         71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         78       RLD       10.1       79         79       RST       10.2				
70RAA10.3A.17, 1871RAS10.4A.17, 1872RSU10.5A.17, 1873RSS10.6A.17, 1874RMU10.7A.1775RMS10.8A.1776RDV10.977RDS10.1078RLD10.179RST10.2				
71       RAS       10.4       A.17, 18         72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       77         77       RDS       10.10       78         79       RST       10.2				A 17 18
72       RSU       10.5       A.17, 18         73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       A.17         77       RDS       10.10       78         79       RST       10.2       A.17				
73       RSS       10.6       A.17, 18         74       RMU       10.7       A.17         75       RMS       10.8       A.17         76       RDV       10.9       A.17         77       RDS       10.10       A.17         78       RLD       10.1       A.17         79       RST       10.2       A.17				
74RMU10.7A.1775RMS10.8A.1776RDV10.977RDS10.1078RLD10.179RST10.2				
75RMS10.8A.1776RDV10.977RDS10.1078RLD10.179RST10.2				
76         RDV         10.9         77         RDS         10.10         78         RLD         10.1         79         RST         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2         10.2				
77         RDS         10.10           78         RLD         10.1           79         RST         10.2				··· • • •
78 RLD 10.1 79 RST 10.2				
79 RST 10.2				

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COMPANY CONFIDENTIAL	SYSTEM DE	SIGN SPECI	FICATION	REV. A	PAGE	8

# OP CODE DIRECTORY By CODE

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OP	Mnemonic	Section	Compatibility Notes
85	CI0	16.4	
86	ATE	20.1	
87	MOP	19_1	
88	D2B	17.1	
89	B2D	17.2	
90	INT	13.8	
91	SRD	16.3	A.23
92	RAD	16.2	
93	BRV	13.9	
94	IIO	16.1	
95	RDT	18.1	
97	STT	18.2	• · · · · · · · ·
98	IOC	16.5	
99	SST	20.10	A.40
AO	MVS	21.1	
A1	CPS	21.2	
AZ	HSH	21.3	
AB	BAD	20-9	

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BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
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CCMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 9

# OP CODE DIRECTORY BY MNEMONIC

Mnemonic	0 P	Section	Compatibility Notes
ACM	84	10.11	
ADD	02	8.2	A.09
AND	42	16.14	A_10
ASP	61	13.7	
ATE	86	20.1	
BAD	AB	20.9	•
BCT	30	13.1	
BOT	41	15.11	A.05
BRT	33	15.14	A.22
BRV	93	13.9	
BST	34	15.15	A.22
BUN	27	11.1	
BZT	40	15.10	A.05
82 D	89	17.2	
CIO	85	16.4	
CPA	45	15.12	A.02
CPN	46	15.13	
CPS	A1	21.2	
DEC	03	8.3	A.08
DIV	06	8.6	
02B	88	17.1	
EDT	49	14.9	A.13
EQL	22	11.1	A.06
EXT	32	13.3	
GEQ	26	11_1	A_06
GTN	28	11.1	A.06
GTR	24	11.1	A.06
нвк	48	12.2	A.25
HBR	29	12.1	
HCL	62 -	13.5	
HSH	A 2	21.3	
IAD	50	9.3	
IAS	51	9_4	
110	94	16.1	
ILD	58	9.1	
ILS	69	20.5	
IMI	57	9.9	
IMS	55	9_8	
IMU	54	9.7	
INC	01	8.1	A.08

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# OP CODE DIRECTORY BY MNEMONIC

Mnemonic	OP	Section	Compatibility Notes
INT	90	13.8	
IOC	98	16.5	
ISS	53	9=6	
IST	59	9-2	
ISU	52	9.5	
LEQ	23	11.1	A.06
LIX	67	20.2	
LOK	60	20.4	
LSS	21	11.1	A_06
MLS	6 A	20.6	
NOP	87	19_1	
MPY	05	8.5	A.10
HVA	10	14-3	A.03
MVC	13	14.6	A.07
MVD	08	14.1	A.20
MVL	09	14.2	A_21
MVN	11	14.4	A_04
AVR	14	15.7	A.15
MVS	AO	21.1	
<b>NVW</b>	12	14.5	A_07
NEQ	25	11.1	A.06
NOP	20	11.1	
NOT	44	15.18 13.2	A.11
NTR	31	13_2	A.19
NUL	2 A .	11.1	A.06
OFL	2.8	11.1	
ORR	43	15_17	A.11
RAA	70	10.3	A.17, 18
RAD	92.	16.2	
RAS	71	10_4	A_17, 18
RDS	7.7	10-10	
RDT	95	18.1	
RDV	76	10.9	
RET	63	13_6	
RLD	78	10.1	
RMS	75	10.8	A.17
RMU	74	10.7	A.17
RSS	73	10.6	A_17, 18
RST	79	10.2	
RSU	72	10.5	A.17, 18

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 11

## OP CODE DIRECTORY BY MNEMONIC

Mnemonic	OP	Section	Compatibility Notes
SDE	16	15.1	
SDU	17	15.2	
SEA	39	15.5	A_12
SIX	68	20.3	
SLD	38	15.7	A.26
SLL	37	15.6	A.26
SLT	64	15.8	
SMF	47	20_8	
SRD	91	16.3	A.23
SST	99	20.10	A . 40
STB	66	15.9	
STT	97	18.2	
SUB	04	8_4	A_09
SZE	18	15.3	
SZU	19	15.4	
TRN	15	14_8	A.14
VEN	35	13_4	
WHR	65	20.7	

BURRCUGHS CORPORATION System development gro Pasadena plant	UP	V SERIES INSTRUCTION SET		1997 5390				
COMPANY CONFIDENTIAL	SYSTEM	I +	SPECTI	ICATION	REV A	PAGE	12	-

1 INTRODUCTION

#### 1.1 PREFACE

This specification defines the instruction set for the V-Series processor family.

Appendix A - Compatibility Notes: Describes the machine dependent variations to the instruction specifications.

1.2 RELATED SPECIFICATIONS

See Appendix A - Compatibility Notes (A.01).

#### 1.3 GENERAL DESCRIPTION

This instruction set consists of powerful, high level variable length instructions of up to three operand addresses each. It has instructions for data manipulation and local program control as well as more complex instructions to address outside of the local program environment and switch program environments. This family of instructions will also permit the system to address memory of greater than five million bytes. Addressing limitations are machine dependent. See Appendix A -Compatibility Notes (A.53).

Operands may be fixed in length, may vary from 1 to 100 units, or may have their lengths defined by a begin/end address pair. In addition, data types may specify unsigned numeric, signed numeric, or unsigned alpha.

BURRCUGHS CORPOR System developme Pasadena plant		V SERIES INSTRUCTION SET	1997 5390
CCMPANY CONFIDEN	TIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 13

DATA REPRESENTATION

2

Conversion between signed and unsigned 4-bit representation and 8-bit representation is accomplished automatically during the execution of instructions.

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2.1 SIGNED NUMERIC FORMAT (SN)

Data is interpreted in units of 4 bits (one digit). The sign is interpreted as a separate and leading 4-bit unit. The 4-bit code is interpreted by the arithmetic units as follows:

4-bit Code	Digit	Sign Code
0000	0	+
0001	1	+
0010	2	+
0011	3	+
0100	4	+
0101	5	+
0110	6	+
0111	7	+
1000	8	+
1001	9	+
1010	A Undefined	* +
1011	B Undefined	
1100	C Undefined	
1101	D Undefined	
1110	E Undefined	
1111	F Undefined	

* Undefined - The hexadecimal digits A through F are hereafter referred to as "undigits". Use of undigits in an arithmetic operand, except for the sign digit, will cause an Invalid Arithmetic Data Fault. See Appendix A - Compatibility Notes (A.16).

BURROUGHS CORPORATION	↓ 	1997 5390	
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET		
	DESIGN SPECIFICATION REV. A		

2.1 SIGNED NUMERIC FORMAT (SN) (Continued)

When the result of an operation is signed, the sign-digit is stored as follows:

+ = 1100 (C) - = 1101 (D)

When the sign digit is interpreted as PLUS, it will compare as HIGH relative to a sign digit interpreted as MINUS.

In the examples that are given at the end of the description of many of the instructions the plus symbol (+) is used to indicate a sign digit value of 0-9, A, B, C, E or F. The symbol also is used to represent a plus sign value that may be stored within the processor. The letter "C" is used to indicate that the processor has written a plus sign into memory. The letter "D" is used to indicate the minus sign except that the minus symbol (-) is used to represent a minus sign value that may be stored within the processor.

2.2 UNSIGNED NUMERIC FORMAT (UN)

Data is interpreted in units of four-bits (one digit). Unsigned data fields are assumed to be positive.

2.3 UNSIGNED ALPHA FORMAT (UA)

Data is interpreted in units of eight bits (one byte or one character).

The internal representation of alpha data is in the Extended Binary Coded Decimal Interchange Code (EBCDIC).

Eight-bit data is considered unsigned except in the case of the Move Alpha (OP = 10), Move Numeric (OP = 11), and Edit (OP = 49) instructions. Additional details are given in the description of these instructions.

Alphanumeric comparisons are binary and thus the (low-to-high) collating sequence for EBCDIC is symbols-alphas-digits.

BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT

V SERIES INSTRUCTION SET

1

1997 5390

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 15

3

# INSTRUCTION REPRESENTATION

"Reserved" or "not specified" bits, digits, or characters must be zero and are reserved for future specification. Ignored bits, digits or characters are not examined and may be any value.

All fields are addressed most significant digit first, unless specifically noted otherwise.

All instructions must start at an even address or cause an Address Error Fault (AEX = 43).

The data fields are called the A-field, the B-field and the C-field. AF and BF generally refer to the lengths of A and B fields respectively The address of each field is called the A, B and C address. The data type of each field is generally defined by the first digit (controller bits) of the A, B and C addresses.

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SYSTEM DEVELOPMENT GROU Pasadena plant	V SERIES INSTRUCTION	SET	
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION RE	V.A PAGE 16	) <b>— —</b>

## 3.1 INSTRUCTION FORMAT

The Processor instructions may vary in length from 4 to 30 digits. An instruction may use a mixture of Extended Address and Non-extended Address formats. Extended format is specified by the value of the second digit of each of the A, B, and C address syllables. An extended address occupies 8 digits whereas a non-extended address occupies 6 digits of an instruction.

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## Non-Extended Format:

Description OP VV OP VVVV CP AAAA OP AAAAAA OP AFBF AAAAAA OP AFBF AAAAAA BBBBBB OP AFBF AAAAAA EEBBBB CCCCCC

#### Extended Format:

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Description OP AAAAAAAA OP AFBF AAAAAAAA OP AFBF AAAAAAAA OP AFBF AAAAAAAA BBBBBBBB OP AFBF AAAAAAAA BBBBBBBBB CCCCCCCC

Where:

- OP = Operator Code
  - V = Variant Digits
- AFBF = A and B-field length variant.

A, B, C = Address of respective data fields

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 17

## 3.1.1 NON-EXTENDED FORMAT

Non-extended direct addressing capability is from 0 through 99,999. In a Branch Instruction, the two address controller bits can be used to extend the address range to 299,998 (See Section 3.5). The non-extended format is shown in Figure 3.1-1.

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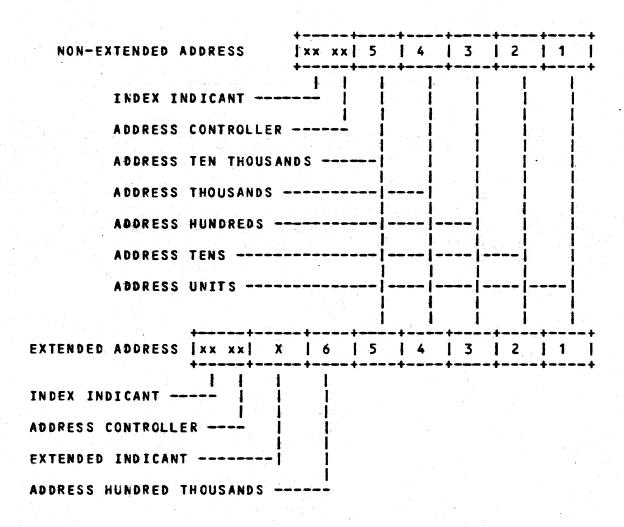
#### 3.1.2 EXTENDED FORMAT

Extended direct addressing capability is from 0 through 999,999.

An Extended Indicant is specified if the two high order bits of the second most significant digit of an address syllable are true. An Extended Indicant signifies that the next six digits contain the address and determines which index registers may be specified for this address. See Section 3.2. The non-extended and extended addressing formats are shown in Figure 3.1-1.

BURROUGHS CORPORATION System development group	• • • • • • • • • • • • • • • • • • •		• • • • • • • • • • • • • • • • • • •	1997 5390	
PASACENA PLANT		V SERIES INSTR	UCTION SET		
CCPPANY CONFIDENTIAL S	YSTEM DES	IGN SPECIFICATI	ON REV. A	PAGE 18	

FIGURE 3.1-1 NON-EXTENDED/EXTENDED ADDRESSING FORMAT



BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYST	EM DESIGN SPECIFICATION REV. A	PAGE 19

#### 3.2 ADDRESS RESOLUTION

Under the MCP for the V Series machines, most of the MCP and all user programs are partitioned into a number of separate memory pieces. Each is defined by its base and limit which are always MOD 1000. All addresses to this memory are relative to one of these base and limits.

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All processes running under the MCP on these machines have accessability to memory via eight base and limit pairs. Base #0 is defined as that process' context (data) area. Base #1 is defined as that process' code area. Non-indexed addresses will refer to base #0 or base #1, depending upon whether the address refers to data or code, respectively. In order to support user programs with only one base and limit (i.e. with the intermixed code and data), both base #0 and base #1 point to the same area of memory.

Processes can also address memory via all 8 base and limit pairs through the use of the base indicant digit in one of the index registers. With non-extended addressing, IX1, IX2, and IX3 can be used. Extended addressing also allows the use of IX4, IX5, IX6, and IX7.

Addresses will be resolved according to the following chart:

EXTENDED INDICANT	INDEX INDICANT	ADDRESSING MODE
None	0	Context Relative
None	1	IX1 w/Base Indicant
None	2	IX2 w/Base Indicant
None	3	IX3 w/Base Indicant
A	0	Address Error
Α.	1	Address Error
A	2	Address Error
A	3	Address Error
В	0	Address Error
В	1	Address Error
B	2 /	Address Error
. <b>B</b>	3	Address Error

BURRQUEHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 20

3.2 ADDRESS RESOLUTION (Continued)

#1)

BURRCUGHS CORFORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 21

## 3.2.1 NON-INDIRECT ADDRESS

A non-indirect context relative address is relative to the Code Base (Base #1) for the following instruction opcodes:

______

0 P	Mnemonic	Name
20	NOP	No-operation
21	LSS	Branch on Less
22	EQL	Branch on Equal
23	LEQ	Branch on Less or Equal
24	GTR	Branch on Greater
25	NEQ	Branch on Not Equal
26	GEQ	Branch on Gtr or Eql
27 [·]	BUN	Branch Unconditional
28	OVF	Branch on Overflow
29	HBR	Halt Branch
2.4	NUL	Branch on Null
28	GTN	Branch on Gtr or Null
31	NTR	Enter
32	EXT	Exit

A non-indirect context relative address is relative to the Data Base (Base #0) for all other instruction opcodes.

Address digits are limited to the decimal values of 0-9. Undigits (A through F) in a resolved final address will cause an Address Error fault.

These specifications define certain absolute address fields, however, some machines require fixed address modifications. See Appendix A - Compatibility Notes (A.35).

BURROUGHS CORPORATION			+ ******	1997 5390
SYSTEM DEVELOPMENT GRO Pasadena plant	DUP	V SERIES	INSTRUCTION SET	
COMPANY CONFIDENTIAL	+- System des	IGN SPECI	FICATION REV. A	PAGE 22

#### 3.2.2 INDIRECT ADDRESS

The referenced address field does not contain the operand data, but contains another address. The latter address may point to data or still another address. This indirect reference may be carried to any depth. The controller of the final (direct) address specifies the format of the operand field to be accessed and must conform to any address controller restrictions for the instruction.

Full generality of indexing is maintained in indirect addressing. Any or all of the indirect addresses in a chain may be indexed. An address is always indexed before the indirect reference is taken.

Extended addressing may be applied to any or all of the indirect addresses in a chain.

All Indirect Addresses in an indirect address chain that are context relative are relative to the Data Base (Base #0). If the indirect address is indexed, the specified Base Indicant from the index register will be used to determine the base. If the indirect address is extended with a "D" and no index register is specified, the address is relative to the Code Base (Base #1).

Undigits in an unresolved intermediate address will produce an Address Error Fault (AEX = 32). See Appendix A - Compatibility Notes (A.29).

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BURRCUGHS CORPORATION System development group	 ++	1997 5390
PASACENA PLANT	V SERIES INSTRUCTION SET	•
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 23

#### 3.2.3 BRANCH ADDRESS

If non-extended address format is used, the branch address in the Address Branch, Halt Branch, Enter and Exit instructions have a maximum address capability of 299,998. To accomplish this the address controller bits carry the following significance:

00 = 0 = Most Significant Digit of Address

- 01 = 1 = Most Significant Digit of Address
- 10 = 2 = Most Significant Digit of Address
- 11 = 3 = Indirect Address

If address extension is used, the address controller in the Branch, Halt Branch, Enter and Exit instructions is only used to indicate an indirect address.

All Indirect Addresses in the indirect address chain that are context relative are relative to the Data Base (Base #0) unless the indirect address is indexed. If the indirect address is indexed, the specified Base Indicant from the index register will be used to determine the Memory Area that contains the indirect address. If the indirect address is extended with a "D" and no index register is specified, the address is relative to the Code Ease (Base #1).

An indexed tranch address should resolve to a Base Indicant value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments.

BURRCUGHS CORPORATION System development group Pasacena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 24

3.2.4 ADDRESS INDEXING

The Index Register Format is defined as:

 SIGN
 BI
 D6
 D5
 D4
 D3
 D2
 D1

 I
 S
 I
 I
 D
 I
 D
 I
 D
 I
 D
 I
 D
 I
 D
 I
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S = Sign digit

I = Base Indicant

D = Decimal digit 0 thru 9

The address of the Index Register points to the sign digit. If indexing is specifed, the Index Register contents (D6 - D1) are added to or subtracted from the address depending on the value of the sign digit.

The value of the Base Indicant indicates which Base/Limit pair is associated with the indexed address. The Base Indicant must accompany the address in all further processing. The specified base is added to the sum of the address and the decimal field of the index register.

Some values of the Base Indicant may be invalid. See Appendix A - Compatibility Notes (A.32).

An attempt to index below the BASE or above the LIMIT (see Section 5.1) will cause an Address Error Fault (AEX = 11). See Appendix A - Compatibility Notes (A.30).

An undigit in the decimal field of an Index Register will cause an Address Error Fault (AEX = 12).

An indexed branch address should resolve to a Base Indicant value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments.



#### 3.2.4 ADDRESS INDEXING (Continued)

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Three Index Registers (IX1, IX2 & IX3) occupy a reserved area of memory, relative to Base #0. They are located at memory addresses 08, 16 and 24 respectively.

These Index Registers may also be loaded with the Load Index Register instruction (OP = 67) and stored with the Store Index Register instruction (OP = 68).

The following instructions and procedures have the ability to change the index registers that are maintained in reserved memory as an implicit operand:

0 P	Mnemonic	Name	
30	BCT	Branch Communicate	(1X3)
31	NTR	Enter	(IX3)
32	EXT	Exit	(IX3)
35	VEN	Virtual Enter	(IX3)
37	SLL	Search Link List	(IX1)
38	SLD	Search Delink	(IX1,IX2)
39	SEA	Search	(IX1)
62	HCL	Hyper Call	(IX3)
63	RET	Return	(IX3)
64	SLT	Search List	(IX1,IX2)
66	STB	Search Table	(1X1)
91	SRD	Scan R/D	(IX1)
	HCP	Hardware Call	(1X3)

BURROUGHS CORFORATION	↓ ★	1997 5390
SYSTEM DEVELOPMENT GROUP Pasacena plant	V SERIES INSTRUCTION SET	
	<b> </b> +	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 26

## 3.2.4 ADDRESS INDEXING (Continued)

The four Mobile Index Registers (IX4, IX5, IX6 & IX7) may be loaded indivually or collectively with a Load Index Register instruction (OP = 67) and stored indivually or collectively with a Store Index Register instruction (OP = 68). The processor must maintain the value of these registers.

The following instructions and procedures set the Mobile Index registers invalid after storing them on a stack:

OP	Mnemonic	Name
-		
30	BCT	Branch Communicate
62	HCL	Hyper Call
	INP	Interrupt Procedure
	HCP	Hardware Call Procedure

The following instructions restore the Mobile Index registers that were stored on a stack.

OP	Mnemonic	Name
-		
63	RET	Return (HCL & HCP variant)
93	BRV	Virtual Branch Reinstatee

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SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 27

#### 3.2.5 ADDRESS CONTROLLER

The two low-order bits of the first digit of the address field provide information that refers to the particular address or to the type of data stored at that address.

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The two bits generally carry the following significance:

00 - Unsigned 4-bit format (UN) 01 - Signed 4-bit format (SN) 10 - Unsigned 8-bit format (UA) 11 - Indirect Address (IA)

Some combinations are prohibited in some instructions and may be variants in other instructions.

The values of the first digit for both the low (controller) and the high order (indexing) bits are shown below.

			UA ++		
I	0	1	2	3	No indexing
ł	4	5		7	IX1 IX4 IX7
1	8	9	A	в	1X2 1X5
1	C I	D	•	FÍ	1X3 1X6
+	+		}+	+	

Examples:

1. A-address = 601000.

From the above table, 6 means UA and IX1. This means add 1000 and the contents of Index Register One to the value of the Base. The data at this address is processed as eight bit units.

2. A-address = F00000.

From the table, F means IA and IX3. This means that the indirect address will be found by adding zero to the contents of IX3 and then adding the base.

BURRCUGHS CORFORATION System development group	 +	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	•
COMPANY CONFIDENTIAL SYST	EM DESIGN SPECIFICATION REV. A	PAGE 28

#### 3.3 OPERATOR CODE

The first two digits of an instruction are used to define the operation. All unassigned operator codes are reserved for expansion. The occurrence of an invalid operator code is an Invalid Instruction Fault (IEX = 01) and will cause a Hardware Call procedure to be executed.

#### 3.4 FIELD LENGTH

The next four digits may be used to define field length. AF and BF generally refer to the data field length of the "A" operand and the "B" operand respectively. Maximum field length of 100 units is indicated when the two digit value is equal to 00.

# 3.4.1 INDIRECT FIELD LENGTH

Indirect Field Length is specified by setting the two high order bits (8 & 4) of the most significant digit True. When Indirect Field Length is specified, a two-digit memory Location relative to the Data Base (Base #0), is addressed. The information at this address specifies the actual field length or another two digit memory location.

The relative address of the Indirect Field Length information is specified by the two low order bits of the most significant digit and the three high order bits of the least significant digit.

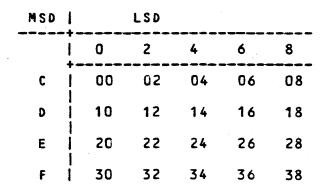
		LSD		
8	1 I	U	I	= Indirect Field Length Flag = 1
4	I I	•	T	= Tens Position of Address + Base
2	T	-	U	= Units Position of Address + Base
	•	-	0	= MUST BE ZERO

BURROUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 29

## 3.4.1 INDIRECT FIELD LENGTH (Continued)

Twenty even numbered indirect addresses ranging from OO to 38, relative to Base #0, are available. The following table decodes the relative address of the indirect field length specified by AF or BF.

-----



Example: If AF=C4 and Base #0 = 1000, the two digit length of the "A" data field or another indirect field length is found at absolute address 1004.

Only the following instructions have Indirect Field Length capability for both AF and BF:

OP	Mnemonic	Name
01	INC	Increment
02	A D D	Add
03	DEC	Decrement
04	SUB	Subtract
05	MPY	Multiply
06	DIV	Divide
08	MVD	Move Data
09	MVL	Move Links
10	MVA	Move Alpha
11	MVN	Move Numeric
12	MVW	Move Words
13	MVC	Move and Clear Words
14	MVR	Move Repeat
15	TRN	Translate

BURROUGHS CORPORATION		1997 5390
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	PAGE 30
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3.4.1 INDIRECT FIELD LENGTH (Continued)

01		Mnemonic	Name
, <b>1</b> 0		SDE	Scan-Equal
17		SDU	Scan-Unequal
13		SZE	Scan-Zone Equal
19		SZU	Scan-Zone Unequal
31		BCT	Communicate
3		NTR	Enter
3.		VEN	Virtual Enter
31		SLL	Search Link List
3	3	SLD	Search Link DeLink
3	9	SEA	Search
4	2	AND	And
4	5	ORR	, takan ang ang ang ang ang ang ang ang ang a
4		NOT	Not
4	5	CPA	Compare Alpha
4	5	CPN	Compare Numeric
4	9	EDT	Edit
6	Di stati di seco	LOK	Lock/Unlock
6	1	ASP	Adjust Stack Pointer
6	2	HCL	Hyper Call
6		SLT	Search List
6	5	WHR	Write Hardware Registers
6	6	STB	Search Table
6	• • • •	LIX	Load Index Registers
6		SIX	Store Index Registers
8	5	CIO	Convert I/O
8	-	ATE	Alter Table Entry
8		MOP	Measurement OP
8		D2B	Decimal to Binary
8		BZD	Binary to Decimal
9		INT	Interrupt
9		SRD	Scan Result Descriptor
9		RAD	Read Address
9	-	IIO	Initiate I/O
9	-	RDT	Read Time of Day
9		STT	Set Time of Day
9	-	IOC	I/O Complete
9	9	SST	System Status
A	-	MVS	Move Strings
A		CPS	Compare Strings
A	2	HSH	Hash Strings

BURROUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasacena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 31

# 3.4.1 INDIRECT FIELD LENGTH (Continued)

The following instructions have Indirect Field Length capability in AF only. BF indirect field length will be ignored.

0 P -	Mnemonic	Name
33	BRT	Bit Reset
34	BST	Bit Set
40	BZT	Bit Zero Test
41	BOT	Bit One Test
48	HBK	Halt Breakpoint

* See Appendix A - Compatibility Notes (A.25).

# 3.4.2 LITERALS (AF ONLY)

The literal capability can only be specified by "Af". An "A" Field Literal is specified by setting the 8 and 2 bits of the most significant digit of AF True and the 4 bit False. The Literal flag indicates that the "A" address syllable of the instruction does not contain an address but does contain the literal data that is to be used by the instruction. The six digits of the "A" address portion of the instruction are the operand itself and not the address index, address controller or the operand address. The Literal is LEFT JUSTIFIED. Literal capability and AF Indirect Field Length cannot be specified at the same time.

			LSD	
	I L			L = Literal Flag = 1
4	1 0	1		0 = Must be Zero
2	I L		U	U = Units of Literal Length
1	I A1	1	U	A = Address controller of Literal

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 32

Bits A1 and AO of "AF" indicate the Literal data type.

	A1	AO	Controller	Unit Length
	O	1 0	Unsigned 4-bit (UN)	1-6 aigits
	C	1 1	Signed 4-bit (SN)	1-5 digits plus sign
	1	1 0	8-bit (UA)	1-3 characters
1	1	1 1	Reserved	+

The following improper useage of Literal will produce an Invalid Instruction Fault (IEX = 22). See Appendix A - Compatibility Notes (A.28).

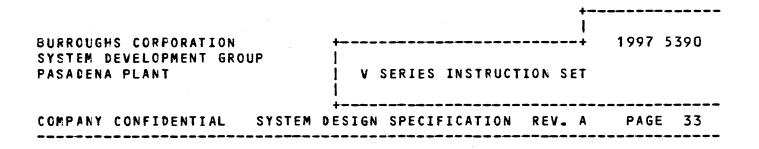
1. Controller = 3 (A1+A0)

2. Controller = 2 (A1 $\pm$ AO/) and length >3

3. Controller = 1 (A1/*AO) and Length >5

4. Controller = 0 (A1/ $\star$ AO/) and length >6

The data itself must be left-justified in the six digit field that would have contained the non-extended A address if it were not literal.



Only the following instructions have literal capability:

0 P	Mnemonic	Name
01		The hone
02	INC	Increment Add
02	AD D	Decrement
	DEC	
04	SUB	Subtract
05	MPY	Multiply
06	DIV	Divide
10	MVA '	Move Alpha
11	MVN	Move Numeric
14	MVR	Move Repeat
16	SDE	Scan-Equal
17	SDU	Scan-Unequal
18	SZE	Scan-Zone Equal
19	SZU	Scan-Zone Unequal
37	SLL	Search Link List
38	SLD	Search Link Delink
39	SEA	Search
*40	8Z T	Bit Zero Test
*41	BOT	Bit One Test
42	AND	And
43	ORR	0 r
44	NOT	Not
45	CPA	Compare Alpha
46	CPN	Compare Numeric
49	EDT	Edit
61	ASP	Acjust Stack Pointer
87	MOP	Measurement OP
88	D2B	Decimal to Binary
89	B2D	Binary to Decimal
94	110	Initiate I/O
-98	IOC	I/O Complete
	<b>▲ ∨ ₩</b>	

*Not recommended for general use

BURRCUGHS CORFORATION	+	 + 1997 5390
SYSTEM DEVELOPMENT GROU Pasadena plant	P   V SERIES INSTRUCTI	ION SET
CCMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION	REV. A PAGE 34

The Literal Flag is invalid in the following instructions and will cause an Invalid Instruction Fault (IEX = 21):

OP	Mnemonic	Name
08	MVD	Move Data
09 .	MVL	Move Links
31	NTR	Enter
33	BRT	Bit Reset
34	BST	Bit Set
64	SL T	Search List
66	STB	Search Table
67	LIX	Load Index Registers
68	SIX	Store Index Registers
85	CIO	Convert I/O
90	INT	Interrupt
92	RAD	Read Address
93	BRV	Virtual Branch Reinstate
95	RDT	Read Time of Day
97	STT	Set Time of Day
99	SST	System Status
AO	MVS	Move Strings
A1	CPS	Compare Strings
A2	HSH	Hash Strings

The Literal Flag is ignored in the following instructions:

OP	Mnemonic	Name
47	SMF	Set Mode
48	HBK	Halt Breakpoint
63	RET	Return
84	ACM	Accumulator Manipulate
91	SRD	Scan Resust Descriptor

BURRCUGHS CORPORATION System development group Pasadena plant	++     V SERIES INSTRUCTION SET	 ⊦ 1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 35

The Virtual Enter (VEN) and Hypercall (HCL) instructions use concatenated AF/BF field lengths or an AF literal. In this case, an AF literal of B1, B2 or B3 will be interpreted as a length of 1, 2 or 3 characters in the "A" location. All other literals are not allowed and will cause an Invalid Instruction fault (IEX = 21).

3.5 INSTRUCTION OPERAND OVERLAP DEFINITIONS

3.5.1 TOTAL OVERLAP

Two operands totally overlap if their addresses, address controllers and field lengths are identical.

3.5.2 PARTIAL OVERLAP

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Two operands partially overlap if at least one digit of each occupy the same memory location and at least one of the following conditions is true.

1) Starting operand addresses are not equal.

- 2) Data types are not equal.
- 3) Field lengths are not equal.

#### 3.5.3 MATCHING TYPE-ADDRESS OVERLAP

A type of partial overlap where the operands addresses are the same and data types are the same, but the field lengths are not the same.

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BURRCUGHS CORPORATION	 ++	1997 5390
SYSTEF DEVELOPMENT GROUP		
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 36

#### COMPANY CONFIDENTIAL STSTEP DESIGN SPECIFICATION REV. A FAGE SU

PROCESSOR STATE

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#### 4.1 INTERNAL PROCESSOR STATE

The V-Series architecture is basically a memory-to-memory computer architecture. However, some processor state is loaded from memory by the processor at specific times, and any succeeding modifications of those fields in main memory has no immediate effect upon the processor operation.

The following list specifies the global state set up in memory by software and loaded within the processor:

- 1. REINSTATE LIST ADDRESS
- 2. MEMORY AREA STATUS TABLE ADDRESS
- 3. SNAP PICTURE ADDRESS
- 4. MEMORY ERROR REPORT ADDRESS
- **** 5.** KERNEL MEMORY AREA TABLE BASE/LIMIT ENTRIES
  - 6. MCP ENVIRONMENT TABLE ADDRESS
  - 7. NUMBER OF ENTRIES IN THE MCP ENVIRONMENT TABLE
  - 8. TIME OF DAY
  - ** Not all processors load this item of processor state. See Appendix A - Compatibility Notes (A.44).

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		The 1	fcllow proce									main	tair	ned with	hin the
		1.	TASK Curre			ELI	ST	POIN	TER	-	poi	nts	to	entry	for
		2.	TASK for c				MEN	TTA	BLE	<b>P</b> 03	INTE	R -	poi	ints to	D ET
		3.	NUMBE	ROF	ENT	RIES	IN	TAS	K US	SER	ENV	IRCN	MENT	TABLE	
		4.	TASK to US		_					REA	TAB	LE P	CINT	TER - p	oints
		5.	NUMBE Table	R OF	ENT	RIES	IN	THE	USI	ER	SER	VICE	S M	IEMORY	AREA
		6 -	MCP D MA fo					BAS	E/L	IMIT	г <b>-</b>	poin	tst	to MCP	DATA
		7.	ACTIV for c				TN	UMBE	R -	act	tive	env	iror	nment n	umber
		8.	PROGR	AM C	OUNT	ER -	pr	ogra	n ac	dri	ess	for	curi	ent ta	s k
		9.	TIME	SLIC	E RE	MAIN	ING								
		10.	ACCUM	ULAT	OR										
-		11.	MEASU	REME	NTR	EGIS	TER								
		12.	INTER	RUPT	MAS	к									
		13.	MOBIL	E IN	DEX	REGI	STE	RS							
		14.	COMPA	RISO	N TO	GGLE	s (	COMS	)						
		15.	OVERF	LOW	TOGG	LE									
		16.	MODE	INDI	CATO	RS									

BUFRCLGHS CORPORATION		1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
CCMPANY CONFIDENTIAL SYST	M DESIGN SPECIFICATION REV. A	PAGE 38

#### 4.2 OVERFLOW FLAG

The Overflow Flag indicates that the result field length of an arithmetic, Move Alphanumeric, or Move Numeric operation is not sufficient to store the result.

-----

The Overflow Flag is not cleared at the beginning of an arithmetic operation, but is preserved. Therefore, it indicates overflow that has occurred any time before or during a series of arithmetic operations or other interspersed non-arithmetic operations.

The Overflow Flag is cleared by the Conditional Branch on Overflow (OP = 28), Edit (OP = 49) and Search (OP = 39) instructions.

The Overflow Flag is stored in memory and reset by the Branch Communicate (OP = 30), Enter (OP = 31), Virtual Enter (OP = 35), and Hyper Call (OP = 62) instructions. The Overflow Flag is also stored in memory and reset by the Interrupt and the Hardware Call procedures.

The Overflow Flag is unconditionally restored from memory by the Return (OP = 63) and Virtual Branch Reinstate (OP = 93) instructions and conditionally restored from memory by the Exit (OP = 32).

The COM and OVF flags field referenced elsewhere in this documentation contain the following information:

	Dig	it	Bit
		<b></b>	
	.0*		3
			2
			1
			0
	1		3
			2
lag			1
Flag			0
		()* 1 1	

* Note: Digit 0 is used as a flag during the EXIT instruction to specify whether to restore the settings of the Overflow and Comparison flags.

BUFRCUGHS CORPORATION System development group PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
CCMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 39

4_2 OVERFLOW FLAG (Continued)

The Overflow Flag is affected by the following instructions and procedures:

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-----

0 P	Mnemonic	Name
01	INC	Fixed Point Arithmetic
02	ADD	
03	DEC	
04	SUB	
06	DIV	
10	MVA	Move Alphanumeric
11	MVN	Move Numeric
28	OFL	Branch on Gverflow
30	BCT	Branch Communicate
31	NTR	Enter
32	EXT	Exit
35	VEN	Virtual Enter
39	SEA	Search
49	EDT	Edit
50	IAD	Integer Arithmetic
51	IAS	-
52	ISU	
53	ISS	
54	IMU	
55	IMS	
57	IMI	
62	HCL	Hyper Call
63	RET	Return
70	RAA	Real Arithmetic
71	RAS	1
72	RSU	
73	RSS	
74	RMU	
75	RMS	
76	RDV	
77	RDS	
84	ACM	Accumulate Manipulate
88	D2B	Decimal to Binary Conversion
89	B2D	Binary to Decimal Conversion
93	BRV	Virtual Branch Reinstate
	INP	Interrupt Procedure
	HCP	Hardware Call Procedure

BURROUGHS CORPORATION	110	+				1997 5	390
PASADENA PLANT		V S	SERIES	INSTRUCT	ION SET		
COMPANY CONFIDENTIAL	SYSTEM D	+	SPECI	ICATION	REV. A	PAGE	40

4.3 COMPARISON FLAGS (COMH, COML)

The states of the Comparison Flags are:

+-	COMI	L -   -	-COMI	1-+	
ł	0	Í	0	1	Null (Clear)
1	0	- P	1	1	Greater or High
1	1	1	0	Ĩ	Less or Low
1	1		1	1	Equal
+					

The Comparison Flags will be stored in memory and reset by the Branch Communicate (OP = 30), Enter (OP = 31), Virtual Enter (OP = 35), and Hyper Call (OP = 62) instructions. They are also stored in memory and reset by the Interrupt and the Hardware Call procedures.

The Comparison Flags are unconditionally restored from memory by the Return (CP = 63) and Virtual Branch Reinstate (OP = 93) instructions and conditionally restored from memory with by the Exit (OP = 32).

The layout of the COM Flags Field is displayed in Section 4.2.

BURRCUGHS CCRPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 41

## 4.3 COMPARISON FLAGS (Continued)

The Comparison Flags are affected by the following instructions and procedures:

.

+-----

OP	Mnemonic	Name
01	INC	Fixed Point Arithmetic
02	ADD	
03	DEC	
04	SUB	
05	MPY	
06	DIV	
10	MVA	Move Alphanumeric
11	MVN	Move Numeric
16	SDE	Scan to Delimiter - Equal
17	SDU	Scan to Delimiter - Unequal
18	SZE	Scan to Delimiter - Zone Equal
19	SZU	Scan to Delimiter - Zone Unequal
30	BCT	Branch Communicate
31	NTR	Enter
32	EXT	Exit
33	BRT	Bit Reset
34	BST	Bit Set
35	VEN	Virtual Enter
37	SLL	Search Link List
38	SLD	Search Link Delink
39	SEA	Search
40	BZT	Bit Zero Test
41	BOT	Bit One Test
42	AND	And
43	OR	Or
44	NOT	Not
45	CPA	Compare Alphanumeric
46	CPN	Compare Numeric
49	EDT	Edit
50	IAD	Integer Arithmetic
51	IAS	
52	ISU	
53	ISS	
54	IMU	
55	IMS	
57	IMI	
58	ILD	
59	IST	
60	LOK	Lock/Unlock

BURROUGHS CORPORATION	+	l + 1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SE	T
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV.	A PAGE 42

4.3 COMPARISON FLAGS (Continued)

	0 P	Mnemonic	Name
	62	HCL	Hyper Call
	63	RET	Return de la companya
	64	SLT	Search List
	66	STB	Search Table
- 11 - 11 - 11	70	RAA	Real Arithmetic
	71	RAS	
	72	RSU	
	73	RSS	
	74	RMU	
	75	RMS	
	76	RDV	
	77	RDS	
	78	RLD	
	79	RST	
	84	ACM	, • · · · · · · · · · · · · · · · · · ·
	88	D2B	Decimal to Binary
	89	B2D	Binary to Decimal
	91	SRD	Scan Result Descriptor
	92	RAD	Read Address Register
	93	BRV	Virtual Branch Reinstate
	94	IIO	Initiate I/O
	A1	CPS	Compare Strings
		INP	Interrupt Procedure
		HCP	Hardware Call Procedure
,			

The Comparison Flags are not altered by conditional or unconditional branching.

BURRCUGHS CORPORATION System development group	  + 	1997 5390	
PASADENA PLANT	V SERIES INSTRUCTION SET		
CCMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 43	
4.4 MODE INDICATORS			

The Mode Indicators are used to specify the operating mode of the processor.

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The Mode Indicators are stored in memory in the following format:

DIGIT	BIT	
0	3	
0	2	
0	1	
0	0	
1	3	
1	2	
1	1	
1	0	
	DIGIT 0 0 0 1 1 1 1 1	DIGIT BIT 0 3 0 2 0 1 0 0 1 3 1 2 1 1 1 0

The Mode Indicators may be changed by the following instructions and procedures:

0P	Mnemonic	Name
	***	
30	BCT	Branch Communicate
62	HCL	Hyper Call
63	RET	Return
93	BRV	Virtual Branch Reinstate
	INP	Interrupt Procedure
	HCP	Hardware Call Procedure

# 4.4.1 SNAP ENABLE INDICATOR

The Snap Enable Indicator must be set in addition to the Snap Picture Enable (See Sec. 4.6) to allow a Snap picture to be taken and stored at the Snap Picture address that has been set with the Write Hardware Register instruction (OP = 65:BF = O1).

BURROUGHS CORPORATION					1997 5390		
System development group				+			
Pasadena plant		V SERIES INSTRUCTION SET		ION SET			
	SYSTEM	1		FICATION		PAGE	44

#### 4.4.2 TRACE INDICATOR

The Trace Indicator enables the Trace function of the processor. The Trace Indicator is either set or reset by the Hyper Call (OP = 62), the Return (OP = 63), or the Virtual Branch Reinstate (OP = 93) instructions or the Hardware Call procedure. The Trace Indicator is always reset by the Interrupt Procedure.

_____

When the Trace function is enabled, a Trace Fault Hardware Call procedure will be executed at the completion of the current instruction except after the Hardware Call Return variant of the Return (OP = 63) instruction. The Hardware Call procedure will store the instruction address of the next instruction to be executed along with some trace parameters on the stack. See Appendix A - Compatibility Notes (A.50).

The Hardware Call Return variant of the Return (OP = 63) instruction will prevent a Hardware Call procedure due to the Trace Indicator until the next instruction has been executed.



#### 4.4.3 PRIVILEGED/USER MODE INDICATOR

The Privileged/User Mode Indicator is used to control the use of certain instructions that may only be executed by the operating system. The system is in Privileged Mode, which allows all instructions to be executed, if the indicator is set. The system is in User Mode if the indicator is reset. An attempt to use a privileged instruction while in User Mode will cause an Invalid Instruction fault (IEX = 02).

The following instructions may only be executed in Privileged Mode:

OP	Mnemonic	Name
60	LOK	Lock
63.	RET	Return (HCL & HCP variant)
65	WHR	Write Hardware Register
85	CIO	Convert I/O
86	ATE	Alter Table Entry
90	INT	Interrupt
91	SRD	Scan Result Descriptor
92	RAD	Read Address
93	BRV	Virtual Branch Reinstate
94	IIO	Initiate I/O
97	STT	Set Time-of-Day Timer
98	IOC	I/O Complete
99	SST	System Status

The Privileged/User Mode Indicator also restricts the use of the MCP Environment Number in certain instructions. In the Virtual Enter (OP = 35), the Virtual Exit variant of Return (OP = 63), the Move String (OP = AO), the Compare String (OP = A1) and the Hash String (OP = A2) instructions, if the most significant digit of the Environment Number is equal to a "D" and the system is not in Privileged Mode cause an Invalid Instruction fault (IEX = 31). In the Move String (OP = A0), Compare String (OP = A1) and Hash String (OP = A2) instructions, if the Environment Number is equal to "zero" and the system is not in Privileged Mode cause an Invalid Instruction fault (IEX = 32).

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4 4 4	SOFT FAULT ENABLE INDICATOR	
••••		
	The Soft Fault Enable Indicator enables the	soft fault
	reporting feature of the V-Series operating s	
	reporting reacure of the voerres operating s	y s c c m e
	When this indicator is set the Branch	Compunicato
	(OP = 30), Hyper Call (OP = 62), Return	
	Virtual Branch Reinstate (OP = 93) instru	
	examine the Soft Fault Pending Flag in the R	
	entry for the current task, and cause a H	
· · · · ·	procedure to be executed if the digit is	not equal to
	zero.	
	a ser a s	
4.5	MEMORY ERROR REPORT ENABLE	
	The Memory Error Report Enable allows one	nemory error
	report to be written into memory.	
•	This indicator affects the contents of	main memory
	specified by the value of the Memory Error R	
	that has been set by the Write Hardwa	
	instruction (OP = $65$ :BF = O2).	
	This enable is set by the Write Hardwa	re Penister
	instruction $(OP = 65:BF = O2)$ and is	
		written into
· ·		written into
	memory.	
1 4	CNAD DIFTUDE ENADLE	
4.6	SNAP PICTURE ENABLE	
	The one produce problem allow and other all	
	The Snap Picture Enable allows one SNAP pi	cture to be
	stored in memory.	
	This enable affects the contents of main memo	
	by the value of the Snap Picture Address that	
	by the Write Hardware Register	instruction
	(OP = 65:BF = 01).	
	This indicator is set by the Write Hardw	are Register
	instruction (OP = $65:BF = C1$ ) and is	turned off
	•	written into
	memory.	
	•	

BURROUGHS CORPORATION	 ++	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 47

#### 4.7 TASK TIMER

The Task Timer is a counter that is used to interrupt a task when its time slice has ended. The maximum timer value is about 100 seconds. The most significant digit of the timer controls the timer interrupt.

If the Timer Interrupt bit is set in the Interrupt Mask, an Interrupt procedure occurs, that stores the address of the next instruction to be executed, whenever the most significant digit of the timer is equal to zero.

If the Timer Interrupt bit is not set in the Interrupt Mask, the timer will continue to decrement at the same rate until an Interrupt procedure is executed for any reason. At that time the value of the Task Timer will be stored in the Reinstate List Entry for the interrupted task and the Task Timer set to its maximum value.

If an interrupt has not occurred before the entire task timer reaches zero, a task timer fault will occur, which will cause a hardware call that will store the address of the next instruction to be executed. See Appendix A -Compatibility Notes (A.45).

The Task Timer is affected by the Virtual Branch Reinstate instruction (OP = 93) and the Interrupt procedure.

The resolution of the Task Timer is machine dependent. See Appendix A - Compatibility Notes (A.36).

BURROUGHS CORPORATION	++ 1997 5390
SYSTEM DEVELOPMENT GROUP	
PASADENA PLANT	V SERIES INSTRUCTION SET
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 48

#### 4.8 KERNEL MODE

Kernel Mode is the special mode the processor is in while executing the MCP Kernel routine. The MCP Kernel is entered with the execution of the Interrupt procedure and is exited with the execution of the Virtual Branch Reinstate instruction (OP = 93).

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An attempt to execute a Hardware Call procedure while in Kernel Mode will cause the system to REDLIGHT halt after storing the fault indicators in absolute memory location 72 - 81.

When a REDLIGHT halt occurs, a SNAP picture is taken (if enabled) and the processor stops. The processor cannot continue from this point as the error that caused the REDLIGHT is in a non-recoverable portion of the system. The error must be cured and the system reinitialized manually.

# 5 TASK ADDRESSING ENVIRONMENT

#### 5.1 TASK ADDRESSING CAPABILITIES

A task may have up to eight different areas of main memory addressable in its local environment at any one time. These local memory areas are located using the following data structures: the Reinstate List, the MCP Environment Table, the User Environment Table, and Memory Area Tables. These tables are described in more detail in later sections. However, the basic linkages between these tables are described briefly below.

Each task has an entry in a system array called the Reinstate List in which the processor and MCP maintain information about that task.

A task may execute instructions from MCP code modules or user program code. All of the code modules for the MCP have entries in the MCP Environment Table. Entry #0 of the Reinstate List contains a pointer to the MCP Environment Table. All of the code modules for a user program have entries in the User Environment Table for that task. The Reinstate List entry for each task contains a pointer to the User Environment Table for that task.

EURROUGHS CORFORATION System development group	 ++ 	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 49

5.1

TASK ADDRESSING CAPABILITIES (Continued)

Each MCP or User Environment Table entry points to a Memory Area Table which describes the local addressing environment for that code. The first eight entries in the Memory Area Table contain the actual base/limit pairs for each memory area or indirect pointers to the actual base/limit pairs.

The smallest allocatable unit of memory is a Memory Area. It may be from 1,000 to 1,000,000 digits in size in increments of 1000 digits.

The following instructions or procedures change the operating environment of the processor by resolving the first eight entries in the specified Memory Area Table and retaining the Base and Limit values for memory access protection. See Appendix A - Compatibility Notes (A.34).

OP	Mnemonic	Name
30	BCT	Branch Communicate
35	VEN	Virtual Enter
62	HCL	Hyper Call
63	RET	Return
86	ATE	Alter Table Entry
93	BRV	Virtual Branch Reinstate
	INP	Interrupt Procedure
	HCP	Hardware Call Procedure

The processor has the ability to reference these eight Memory Areas as the local environment at any point in time (See Section 3.2). The processor also has the ability to reference non-local Memory Areas and provide memory access protection for such Memory Areas as are specified by the Convert I/O (OP = 85), the Alter Table Entry (OP = 86), the Move String (OP = A0), the Compare String (OP = A1), or the Hash String (OP = A2) instructions.

BURROUGHS CORFORATION		+			+	1997 5	390
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CCMPANY CONFIDENTIAL	SYSTEM	+	SPECI	FICATION	REV. A	PAGE	50

5.2 REINSTATE LIST

The Reinstate List is a system array set up by the MCP to control task switching on the processor. Every task has an entry in this table.

The Reinstate List is located in memory with a Write Hardware Register instruction (OP = 65:BF = 00).

Two of the entries have special significance. The entry for task #0 is not assigned a task, because its Environment Table Address field contains the address of the MCP Environment Table. Task #1 is reserved for the MCP Kernel code.

See Appendix A - Compatibility Notes (A.46) for a detailed layout of the entry.

#### 5.3 ENVIRONMENT TABLE

The Environment Tables are system arrays set up by the MCP to inform the processor of the legal addressing environments for a task. A task has access to addressing environments in the MCP Environment Table or that task's USER Environment Table.

The MCP Environment Table is located by the Environment Table Address field in the Reinstate List entry for Task #0. This Environment Table is shared by all tasks.

Every task has its own USER Environment Table, located by the Environment Table Address field in the Reinstate List entry for that task.

See Appendix A - Compatibility Notes (A.48) for a detailed layout of the Environment Table entry.

BURRCUGHS CORPORATION System development group Pasadena plant	+     V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM		

5.4 MEMORY AREA TABLE

A Memory Area Table (MAT) contains 1-100 entries which contain the actual Ease/Limit pairs for a memory area or point indirectly via Copy descriptors to the actual Base/Limit pairs. It may be an executable or non-executable Memory Area Table.

Each environmental table entry of a task contains the address of a Memory Area Table and the number of entries in that table. Each task when running has one of its Memory Area Tables loaded into the hardware. This is called its local addressing environment. A task can have up to eight different memory areas in its local addressing environment at any one time. Its local addressing environment is defined by an executable Memory Area Table. An executable Memory Area Table contains eight entries, of which Base/Limit #1 references a code memory area (i.e., instructions are fetched from this memory area).

A non-executable Memory Area Table does not contain a reference to a code memory area in Base/Limit pair #1. It is used for storage of Memory Area descriptors (Base/Limit pairs).

Every task has a User Services Memory Area Table (USMAT). This non-executable Memory Area Table describes MCP memory areas containing privileged information about that task. To protect these memory areas from user access, this Memory Area Table is located by the Memory Area Table Address field in the USER Environment Table entry #0 for the task. Thus to access any of these memory areas via an instruction, the user must specify an Environment Number of zero, which is illegal except in Privileged Mode.

A Memory Area Table entry can have the following Memory Area Table entries: Original Entry, "C" Copy Entry, "E" Copy Entry, Memory Area Fault Entry, and Unused Entry. See Appendix A - Compatibility Notes (A.34) for a detailed layout of each entry.

Some processors require an ATE to notify it when a MAT entry is modified. See Section 20 on the ATE instruction for details.

BURRCUGHS CORPORATION	++ 1997 1	5 3 9 0
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A PAGE	52

#### 5.5 MEMORY AREAS

The smallest allocatable unit of memory is a Memory Area. It may be from 1,000 to 1,000,000 digits in size in increments of 1000 digits. For example, a software code module that is 57,244 digits in size will be assigned to a 58,000 digit Memory Area. A software code module of only 150 digits will be assigned to a 1,000 digit Memory Area.

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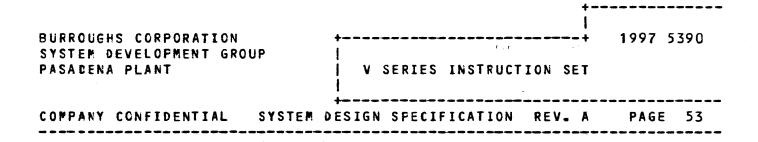
A memory area is located by a Base/Limit pair contained in a Memory Area Table. For references to data or code in the local addressing environment, the base relative memory addresses are added to the selected Base value determine the absolute memory location.

Memory access protection is provided by comparisons of the Base and Limit Values to the address of the requested memory access to insure that the value of the requested address is less than the Limit value but greater than or equal to the Base value. If the address of requested memory access is outside of the specified Memory Area, cause an Address Error fault (AEX = 20-26) and terminate the instruction without storing any further data into memory.

5.6 MEMORY AREA STATUS TABLE (MAST)

The Memory Area Status Table is located in memory with a Write Hardware Register instruction (OP = 65:BF = 03). Each entry in the Memory Area Status Table contains information that is related to a Memory Area that is known to the system.

See Appendix A - Compatibility Notes (A.47) for a detailed layout of the entry.



# 5.7 LOCATING A MEMORY AREA TABLE ENTRY

A Memory Area Table Entry is specified by a Task Number (TN), Environment Number (EN), and a Memory Area Number (MAN).

To locate a Memory Area Table (MAT) or an entry within a MAT, one must traverse the address links through the Reinstate List, the MCP Environment Table or Task User Environment Table, and Memory Area Tables.

The Task Number represents an array subscript into the Reinstate List of 0000 to 9999. (The actual number of possible tasks may be limited by memory constraints.) The address of the Reinstate List is provided by software with a Write Hardware Register instruction (BF = 00). The processor maintains an internal pointer to the Reinstate List entry for the current task, but must recalculate any references to Reinstate List entries for other tasks. The Reinstate List entry for Task #0 contains the MCP Environment Table Address and that table's number of entries rather than information about an actual independent task.

If the first digit of the EN is equal to a "D", then the five least significant digits represent an array subscript into the MCP Environment Table of 00000 to 99999. The Reinstate List entry for Task #0 contains the address of the MCP Environment Table in its Environment Table Address field and the size of the MCP Environment Table in its Number of Entries in the Environment Table Field.

If the first digit of the EN is equal to "O - 9", this six oigit number represents an array subscript into a User Environment Table of 000000 to 999999. (The actual number of environments for a task may be limited by memory constraints.) The Reinstate List entry for a task contains the address of its task's User Environment Table in its Environment Table Address field and the size of its task's User Environment Table in its Number of Entries in the Environment Table field.

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BURROUGHS CORPORATION System development gro Pasadena plant	UP     V SERIES INSTRUCTION SET 	1997 5390
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV. A	PAGE 54

#### 5.7

#### LOCATING A MEMORY AREA TABLE ENTRY (Continued)

If the first digit of the EN is equal to any other value, then cause an Address Error fault (AEX = 52 if the EN came from an Environment Descriptor or AEX = 62 if the EN came from a MAT entry) and terminate the instruction with no further action. If undigits exist in the last five digits of the EN, cause an Address Error fault (AEX = 53 if the EN came from an Environment Descriptor or AEX = 63 if the EN came from a MAT entry) and terminate the instruction with no further action.

If the array subscript portion of the Environment Number is larger than the number in the Number of Entries field for the relevant Environment Table, cause an Address Error fault (AEX = 57 if the EN came from an Environment Descriptor or AEX = 67 if the EN came from a MAT entry) and terminate the instruction with no further action.

If a MAT is being located by an Environment Number contained in user addressable memory (i.e., other than a MAT Copy Type entry or an MCP Function Table entry), then the following additional security check is done:

If the processor is not in Privileged Mode and either the Environment Number equals zero (excluding the special cases of VIRTUAL ENTER and RETURN (VIRTUAL EXIT Variant)) or the first digit of the Environment Number equals "D", then cause an Invalid Instruction fault (AEX = 31) and terminate the instruction with no further action.

The Environment Table entry located above contains the address of the desired Memory Area Table in its Memory Area Table Address field and the size of the MAT in its Number of Entries in the Memory Area Table field. If the Memory Area Number parameter is greater than the value in the Number of Entries in the Memory Area Table field, then cause an Address Error Fault (AEX = 58 if the EN came from an Environment Descriptor or AEX = 68 if the EN came from a MAT entry). If any of the digits of the Memory Area Number contain undigits, then cause an Address Error Fault (AEX = 54 if the EN came from an Environment Descriptor or AEX = 64 if the EN came from a MAT entry).

BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	P     	V SERIES	INSTRUCTI	1 	1997	5 39 0
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COMPANY CONFIDENTIAL	SYSTEM DES	IGN SPECI	ICATION	REV. A	PAGE	55
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#### 5.8 RESOLVING A MEMORY AREA TABLE ENTRY

A Memory Area Table (MAT) entry may contain the following types of entries: an Original Type (the actual Base/Limit of the corresponding Memory Area), an Unused Type (entry is unused), "C" or "E" Copy Types (entry contains a "C" or "E" Copy Descriptor pointing to another MAT entry), or Memory Area Fault Type (the Memory Area is not currently in main memory).

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The algorithm for resolving a MAT entry is generally handled as described below. However, in some instruction algorithms, additional entry type checking is performed which may cause additional error faults. Refer to the particular instruction algorithms for these exceptions.

Copy Type entries provide levels of indirection for MAT entries, so that only one Original Entry may exist for a memory area. One Original Entry may have many Copy Type entries pointing to it. If the MAT entry being resolved is a Copy Type entry, then the information in this entry is used to locate another MAT entry which must then be resolved. If a chain of Copy Type entries exists, then this process will repeat itself until a non-Copy Type entry is found. The handling of this final non-Copy Type entry is described later in this section. The next paragraph explains how to determine the Copy Descriptor parameters needed to locate the next MAT entry in the chain.

If the MAT entry is a "C" Copy Type entry, then the Environment Number and Memory Area Number contained in the MAT entry (along with the current Task Number) are used to locate the next MAT entry to be resolved (See Section 5.7 for details). Since the information in a "C" Copy Type entry may only point to a MCP MAT or a MAT for the current task, it is frequently used by the MCP to gain access to memory areas belonging to whichever task it is currently servicing.

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BURROUGHS CORPORATION	+	1997 5390
SYSTEM DEVELOPMENT GROUP		
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 56

## 5.8

RESOLVING A MEMORY AREA TABLE ENTRY (Continued)

If the MAT entry is an "E" Copy Type entry, then the absolute address of the next MAT entry to be resolved is contained in the MAT entry. However, an "E" Copy Type entry must not point to another Copy Type entry or an Address Error fault (AEX = 69) will occur. The "E" Copy Type entry is typically used when a task wants to gain access to data in a memory area which belongs to antoher task. In this case, the owning task has the Original Entry for the shared memory area in its Memory Area Table and the other tasks point to it via an "E" Copy Type entry.

If the final MAT entry is an Original Type, then the Base/Limit pair contained in this entry is loaded directly into proper processor Base/Limit registers.

If the final MAT entry is a Memory Area Fault Type, then a Hardware Call Procedure reporting either a Soft Memory Area Fault or Hard Memory Area Fault is performed. A Soft Memory Area Fault is performed unless the particular instruction algorithm states otherwise. Note that an attempt to execute a Hardware Call Procedure in Kernel Mode causes a REDLIGHT halt (See Section 4.8).

If the final MAT entry is an Unused Type, then the Base and Limit registers for this entry are set equal to each other. However, since these Base/Limit values are invalid (i.e., Base/Limit = 000/000), any attempt to access memory via an Unused Entry will cause an Address Error fault (AEX = 2n). COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 57

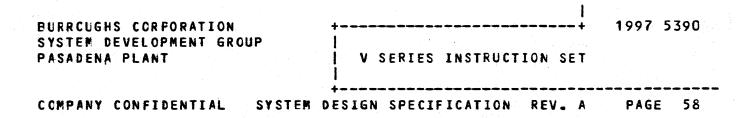
5.9 LOADING A MEMORY AREA TABLE

Loading a Memory Area Table (MAT) consists of locating an eight entry executable MAT, resolving entries 0-7, and, if no error faults were detected, loading the final results into the corresponding processor Base/Limit registers 0-7.

This procedure is performed when a task changes or reloads its local environment during instructions like Hypercall, Branch Communicate, Virtual Enter (non-local variant), Return (Virtual Exit, Hyper Return, and Hardware Return variants), Interrupt, Virtual Branch Reinstate, and Alter Table Entry. It is also used in the Hardware Call Procedure and Interrupt processing.

# 5.10 MCP DATA AREA

Every task has a memory area (located by User Environment Number 0, Memory Area Number 0) called the MCP Data Area in which the MCP maintains information concerning that task. In addition, it contains the "reserved memory" of the MCP routines for that task (See Section 22.2 for a description of the MCP Data Area reserved memory). The MCP Data Area is described by Base/Limit pair #0 when a task is executing MCP code.



INTERRUPT PROCESSING

6

There are two mechanisms for interrupting an instruction stream to start executing the appropriate MCP routines: Interrupt Procedures and Hardware Call Procedures.

1. An Interrupt Procedure is executed as a response to certain instruction interrupts or maskable interrupts to transfer control of the processor to the MCP Kernel routine.

An Interrupt Mask is used to indicate which of the maskable conditions will be allowed to interrupt the current processing. If any interrupt conditions have occurred, and the corresponding bit(s) in the Interrupt Mask is set, then an interrupt procedure is executed. The interrupt condition will be reset during the execution of the Interrupt procedure if the corresponding condition is set in the Interrupt Mask.

The Interrupt Descriptor is as follows:

CONDITION	BIT	CAUSE
Reserved	7	
Instruction	6 -	Instruction-related Interrupt
Overtemp		System Overtemperature
Task Timer	4 -	MSD = 0
Reserved	3	
REAL TIME I/O	2 -	I/O COMPLETE
		Real Time Device.
NORMAL I/O ERROR	1 -	I/O COMPLETE, Exceptions,
		Non-Real Time Device.
NORMAL I/O	0 -	I/O COMPLETE, No Exceptions,
		Non-Real Time Device.

The Instruction Interrupt is not maskable. However, the other Interrupt Descriptor bits are the logical "and" of the pending interrupt conditions and the Interrupt Mask.

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BURROUGHS CORPORATION	! +	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 59

6

INTERRUPT PROCESSING (Continued)

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The definition of the eight bit Interrupt Mask is as follows:

CONDITION	BIT	CAUSE
Reserved Reserved Overtemp	7 6 5 -	System Overtemperature
Task Timer	4 -	MSD = O
Reserved	3	
REAL TIME I/O	2 -	I/O COMPLETE Real Time Device.
I/O ERROR	1 -	I/O COMPLETE, Exceptions, Non-Real Time Device.
NORMAL I/O	0 -	I/O COMPLETE, No Exceptions, Non-Real Time Device.

The interrupt conditions are tested and the interrupt procedure initiated at the end of the current instruction with the address of the next instruction to be executed stored in the Interrupt Frame unless an instruction variant specifies that the address of the instruction that caused the interrupt is to be stored in the Interrupt Frame.

Instruction Interrupts are flagged in the Interrupt Descriptor with the actual Instruction Interrupt condition stored in the Instruction Interrupt Cause Descriptor located in absolute memory locations 32 -33.

BURROUGHS CORPORATION System development group	++	1997 5390
PASACENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 60

6

INTERRUPT PROCESSING (Continued)

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The Instruction Interrupt Cause Descriptor is defined as follows:

VALUE	CAUSE
·	
08-FF	Reserved
07	Failed Virtual Branch Reinstate
0.6	Executed Interrupt Instruction (OP = $90$ )
05	Failed Hardware Call
04	Released Event
03	Released Lock
02	Failed Event
01	Failed Lock
00	Reserved

An Interrupt caused by a failed Hardware Call procedure may store inconsistent values depending upon the cause of the failure.

An over-temperature condition in the system will cause an Interrupt procedure to be executed. After detection of the condition a processor-dependent time delay occurs before a system power-off is initiated.

If an Interrupt condition and a Hardware Call condition exist at the same time, the following algorithm is applied:

- a. If an Instruction Interrupt condition and an instruction-related Hardware Call "error" condition (Invalid Arithmetic Data, Instruction Timeout, Address Error, Uncorrectable Memory Parity Error, Invalid Instruction) occurs at the same time, then the Instruction Interrupt condition is ignored as the instruction did not actually execute correctly.
- b. If the Instruction Interrupt condition is a Failed Lock and the only Hardware Call condition is a Trace Fault, then the Trace Fault condition is ignored.

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 61

# INTERRUPT PROCESSING (Continued)

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c. If any other Fault conditions still remain, then a Hardware Call Procedure is performed.

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- d. If any Instruction Interrupt conditions remain or any maskable interrupt conditions are not masked by the Interrupt Mask (which may have just been loaded by a Hardware Call procedure), then an Interrupt Procedure is performed.
- 2. A Hardware Call procedure is executed as a response to certain processor detected faults. A Hardware Call procedure changes the system environment and transfers control to a software error handling routine.

The Hardware Call procedure stores the "state" of the processor in a Hardware Call Stack Frame on the stack that is associated with the called routine.

The instruction address of the failing instruction is included in the "state" that is stored as a result of the following faults: Address Error; Invalid Instruction; Invalid Arithmetic Data; Invalid Alter Table Entry; Accumulator Trap; Uncorrectable Memory Errors; Instruction Timeout; and certain Memory Area Faults.

The instruction address of the next instruction to be executed (unless one of the faults that require that the address of the failing instruction be stored is also present) is included in the "state" that is stored as a result of the following faults: Trace; Programatic Soft Fault; and other Memory Area Faults.

See the introductory discussion in Section 6 about Interrupt Procedures for a description of the algorithm to be applied when an Interrupt condition and a Hardware Call condition exist at the same time.

BURRCUGHS CORPORATION	 	1997 5	5390
SYSTEM DEVELOPMENT GRO PASADENA PLANT	UP     V SERIES INSTRUCTION SET 		
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV. A	PAGE	

6.1 INTERRUPT PROCEDURE (INP)

The Interrupt procedure is used by the processor hardware to transfer the system environment to the MCP Kernel.

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This procedure is used to enter the MCP Kernel function specified by the six digit address located at memory address 94, relative to the MCP Data Area for Task #1. Processor registers and "state" are stored in the Interrupt frame and control is transferred to the MCP Kernel environment.

The following operations are peformed by this instruction to enter the MCP Kernel environment:

- 1. Store the current value of the Task Timer into the Time Slice Remaining Field of the Reinstate List Entry for the current Task. Set the value of the Task Timer to its maximum numeric value.
- 2. Store the two-digit Interrupt Descriptor into absolute memory locations 21-22.
- 3. Store the machine "state" of the interrupted task into the Interrupt Frame, located in the Reinstate List Entry for the interrupted task.
- 4. Selectively reset the interrupt conditions according to the Interrupt Mask. If the bit in the mask is equal to a "one", reset the corresponding condition. If the bit in the mask is equal to "zero" the corresponding condition will not be changed. Reset the Instruction Interrupt condition.

SET TO

5. Set the machine "state" as follows:

INFORMATION

Kernel Mode	SET
Active Environment Number	000000
Current Task Number	0001
Privileged/User Mode	PRIVILEGED
Trace Mode	NON-TRACING
Snap Enable	DISABLED
Soft Fault Enable	DISABLED
Measurement Register	0000 0000
Comparison & Overflow Flags	RESET

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 63

# 6.1 INTERRUPT PROCEDURE (Continued)

6. Set the MOPOK signal to "O" while the Measurement register is being changed and set it to a "1" at all other times.

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- 7. Set the Interrupt Mask register to zero.
- 8. Store the four digit Task number for Task number one (0001) at absolute memory address 82.
- 9. Locate and load the Kernel Memory Area Table (MAT), which is the MAT pointed to by the first entry in the USER Environment Table for Task #1.
- 10. Execute an unconditional branch to the six-digit address, relative to Base #1, located at memory address 94, relative to Base #0. If any Hardware Call conditions exist, cause a REDLIGHT halt (See Section 4.6) after storing the fault indicators in absolute memory location 72 - 81.

BURRCUGHS CORPORATION System development group Pasadena plant	++ 1997 53 V SERIES INSTRUCTION SET
COMPANY CONFIDENTIAL SYSTEM	M DESIGN SPECIFICATION REV. A PAGE

#### 6.2 HARDWARE CALL PROCEDURE (HCP)

The Hardware Call procedure is used by the processor hardware, when one of the specified faults exist, to enter the routine specified by the Hardware Call Function. The fault indicators are stored in a fixed memory location relative to Base #0 of the called function. Processor "state" is stored in a Hardware Call Stack Frame on a stack that is relative to Base #0 of the specified function. Control is transferred to the Hardware Call Procedure code.

If the processor is in the MCP Kernel environment, an attempt to execute a Hardware Call procedure will cause the processor to REDLIGHT halt (See Section 4.8) after the fault indicators have been stored in absolute memory location 72 - 81.

The following operations are performed by this procedure:

1. Locate the six digit address, relative to the MCP Data Area, of the Hardware Call Function entry in the MCP Function Table at memory address 87 relative to the MCP Data Area.

The Hardware Call Function entry contains the following information:

INFORMATION

DIGITS

_____

Environment Numbe	er	00-05
Next Instruction	Address	06-11
Protection Field	(DD)	12-13
Reserved		14-15
Interrupt Mask		16-17
Mode Indicators		18-19
Houe Indicators		10 17

Note - The lowest memory address = 00

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SFECIFICATION REV. A	PAGE 65

6.2 HARDWARE CALL PROCEDURE (Continued)

If the Protection Field is not equal to "DD", then this Hardware Call Procedure has failed. Perform the following steps:

-------

- a. Write the Fault Indicators into the Failed Hardware Call R/D Area Field of the Reinstate List entry for this task.
- b. Write "05" into the State Indicator field of the same Reinstate List entry.
- c. Perform an Interrupt Procedure, reporting a "05" (Failed Hardware Call) in the Instruction Interrupt Cause Description.
- 2. Load the Memory Area Table specified by the Environment Number contained in the Hardware Call Function Table entry.

If an invalid Environment Number or Memory Area Number is encountered or a Memory Area Fault is found during the loading of the MAT, then this Hardware Call Procedure has failed. Perform the following steps:

- a. Write the Fault Indicators into the Failed Hardware Call R/D Area Field of the Reinstate List entry for this task.
- b. Write "05" into the State Indicator field of the same Reinstate List entry.
- c. Perform an Interrupt Procedure, reporting a "05" (Failed Hardware Call) in the Instruction Interrupt Cause Description.

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MPANY CON	FIDENTIA	L SYSTEM	DESIGN SPECIFICATION R	EV. A	PAGE 66
6.2	HARDWAR	E CALL PRO	CEDURE (Continued)		
	3. St	ore ten di	gits of Fault Indicat	ors into	) memory
	Lo	cation 77	2 - 81, relative to t	he newly	Loaded
	Ba	se #0. The	e Fault Indicators conta	in the 1	following
	in	formation:			
		TH 60001177			
		INFORMATIO		DIGIT	BIL
		Hard Nemo	ry Area Fault	72	3
		Trace		72	Ž
			rithmetic Data (Undigits)	. –	1
			ry Area Fault	72	Ō
		SOIL MEMOR	ry Area Fault	12	0
		Invatid I	nstruction	73	3
		Uncorrect	able Memory Parity Error	73	2
		Address E		73	1
			on Timeout	73	Ō
				12	5
		Stack Ove	rflow	74	3
		Accumulate		74	2
		Snap Pict	•	74	1
		Soft Faul		74	Ó
		0011 1001	•	14	U
		Reserved		75	3
		Reserved		75	2
		Reserved		75	1
		Task Time	n Fault	75	0
	•	IOSK IINC	rauce	<i>, , , ,</i>	U
		Reserved		76-77	ALL
		Address E	rror Extension	78-79	ALL

4. Reset the Fault Condition Indicators.

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OMPANY	CONFIDENTIAL S	STEM DESIGN SPECIFICATION REV. A PAG	E 67
6 3	NADRUADE CAI	PROCEDURE (Continued)	
0.2	MARUWARC LAL	FROCEDORE (CONCINCED)	
	5. Use th	stack pointer, located at address	40
		e to the newly loaded Base #0) as	
		address, relative to Base #0, to store Call Stack Frame.	the
		ware Call Stack Frame is stored on the	stack
	in the	cllowing sequence.	
		INFORMATION D	IGITS
	OLd TOS ==>	Accumulator	00-27
			28-35
			36-37
		Mobile Index Registers	
			70-71
			72-73
			74-79 80-85
	NEW IX3 -=>		86-93
			94-95
			96-10
			02-10
		Fault Task Number ** 1	04-10
		Trace Information ** 1	08-187
	New TOS ==>	•	
		lote - The lowest memory address = 00.	
	* Either	tore the address of the failing instru	ction
		ddress of the next instruction to be exe	
		tack depending upon the type of fault.	

** If the Hardware Call was caused by a Hard or Soft Memory Area fault, store the Environment Number, Memory Area Number and Task Number of the faulted entry as parameters on the stack. See Appendix A -Compatibility Notes (A.51). If in Trace Mode, the trace parameters are passed on the stack in the next 80 digits. See Appendix A - Compatibility Notes (A.50). The space for these parameters is always atlocated whether or not they are actually present.

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OMFANY	CONFIDEN	TIAL S	YSTEM	+ DESIGN	SPECI	FICATION	REV. A	PAGE 68
6.2	HARD	WARE CAL	L PROC	EDURE	(Contin	nued)		
	6.							able staci
								se #0) into
				s 40	(Rela	tive to	the ne	wly loaded
		Base #0	).					•
	7.	Set the	two m	ost si	anifica	ant diai	ts of IX	3 to "CO"
								s of IX3 to
	4							address 41
		(Relati	ve to	the new	wly loa	aded Bas	e #0) plu	s 80.
		TX3 DOH	noint	s to ti	he Nevi	t Instru	ction Add	ress in the
		Stack F						
	8 -	Set the	machi	ne "st	ate" a	s follow	S :	
		INFO	RMATIO	N			S	ET TO
						SS		ion Table
					nt Numl			ion Table
			rrupt		•			ion Table
				ators				ion Table
						user fie	τα) Ο	00000
			arison e Mode		TTLOW	Flags	MAN	RESET -TRACING
		ITAC	e mode				NUN	TRACING
	9.							Measurement
					chan	ged and	set it to	a "one" at
		all oth	er tim	es.				

BURROUGHS CORPORATION	+	1997 5390
SYSTEM DEVELOPMENT GROUP	1	
PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 69

- 6.2 HARDWARE CALL PROCEDURE (Continued)
  - 10. Using the new Base/Limit environment, resolve the next instruction address, relative to Base #1 and execute an unconditional branch to that address.

The use of the Mobile Index Registers or the Accumulator to pass parameters is invalid. The contents are not guaranteed.

The Hardware Call procedure fails if any faults exist at the completion of the Hardware Call procedure. If the Hardware Call procedure fails, store:

- (a) the Fault indicators in the Failed Hardware Call R/D Area Field of the Reinstate List Entry for this task
- (b) "05" into the State Indicator Field of the Reinstate List entry for this task
- (c) "05" into absolute memory location 32 and cause an Instruction Interrupt to the MCP Kernel. The Interrupt procedure may store inconsistent values depending upon the cause of the failure.

BURROUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP		
PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 70

#### 6.2.1 FAULT INDICATORS

The Fault Indicators are described in the following paragraphs.

#### 6.2.1.1 (DIGIT 72 BIT 3) - HARD MEMORY AREA FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because a Memory Area Fault entry was detected while loading a Memory Area Table in certain instructions EHyper Call (OP = 62), Convert I/O (OP = 85), Move String (OP = AO), Compare String (OP = A1), and Hash String (OP = A2)] that require the faulted entry in order to execute the instruction. The Environment Number and Memory Area Number that point to this Memory Area Table entry were also stored as stack parameters.

## 6.2.1.2 (DIGIT 72 BIT 2) - TRACE FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the next instruction to be executed because the system is operating in Trace Mode.

The following information is passed on the stack on each trace fault. See Appendix A - Compatibility Notes (A.50).

- 1. Program address of previous instruction (the one being traced).
- 2. Program address of next instruction.
- 3. Opcode.
- Resolved AF with an indirect flag indication.
- 5. Resolved BF with an indirect flag indication.

6. A address, resolved (including index register used and address controller).

7. B address, resolved (including index register used and address controller).

BURROUGHS CORPORATION + SYSTEM DEVELOPMENT GROUP   PASADENA PLANT   V SERIES	I 1997 5390 S INSTRUCTION SET
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECI	IFICATION REV. A PAGE 71

#### 6.2.1.2 TRACE FAULT (Continued)

- 8. C address, resolved (including index register used and address controller).
- 9. Overflow and Comparison flags.
- 6.2.1.3 (DIGIT 72 BIT 1) INVALID ARITHMETIC DATA FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an undigit other than the sign digit has been detected in an arithmetic operand. See Appendix A - Compatibility Notes (A.16).

A SNAP picture will be taken if enabled by the Snap Enable Indicator (Sec. 4.4.1) and the Snap Picture Enable (Sec. 4.6).

6.2.1.4 (DIGIT 72 BIT 0) - SOFT MEMOPY AREA FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the next instruction to be executed because a Memory Area Fault entry was detected while loading a Memory Area Table in those instructions that do not require the faulted entry in order to execute the instruction. The Environment Number, Memory Area Number and Task Number that point to this Memory Area Table entry were also stored as stack parameters.

6.2.1.5 (DIGIT 73 BIT 3) - INVALID INSTRUCTION FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an Invalid Instruction has been detected. Further detail will also be stored in the Invalid Instruction Extension byte (See Section 6.2.3).

A SNAP picture will be taken if enabled by the Snap Enable Indicator (Sec. 4.4.1) and the Snap Picture Enable (Sec. 4.6). See Section 6.2.3 for those errors classified as Instruction Errors.

BURRCUGHS CORPORATION System development group Pasadena plant	<pre></pre>	1997 5390
	I SYSTEM DESIGN SPECIFICATION REV. A	PAGE 72

#### 6.2.1.6 (DIGIT 73 BIT 2) - UNCORRECTABLE MEMORY PARITY ERROR

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an Uncorrectable "multi-bit" Memory Parity Error has been detected. An Uncorrectable Memory Parity Error during the execution of a processor instruction will terminate the instruction without writing into memory at the Location the error was detected.

#### 6.2.1.7 (DIGIT 73 BIT 1) - ADDRESS ERROR FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an Address Error has been detected. Further detail will also be stored in the Address Error Extension byte (See Section 6.2.2).

A SNAP picture will be taken if enabled by the Snap Enable Indicator (Sec. 4.4.4) and the Snap Picture Enable (Sec. 4.6). See Section 6.2.2 for those errors classified as Address Errors.

#### 6.2.1.8 (DIGIT 73 BIT 0) - INSTRUCTION TIMEOUT FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an instruction has taken longer than a specified processor dependent timeout value. The Instruction Timeout timer value varies from processor to processor. See Appendix A - Compatibility Notes (A.27.4).

A SNAP picture will be taken if enabled by the Snap Enable Indicator (Sec. 4.4.1) and the Snap Picture Enable (Sec. 4.6).

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 73

## 6.2.1.9 (DIGIT 74 BIT 3) - STACK OVERFLOW FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an attempted stack operation would have exceeded the limit of Memory Area "zero". This bit may only be set by the Virtual Enter (OP = 35), the Hyper Call (OP = 62) or the Adjust Stack Pointer (OP = 61) instructions.

6.2.1.10 (DIGIT 74 BIT 2) - ACCUMULATOR TRAP FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the failing instruction because an Accumulator Trap Fault occured.

6.2.1.11 (DIGIT 74 BIT 1) - SNAP PICTURE TAKEN

This fault indicates that a SNAP Picture was stored in memory at a location that has been previously been set with a Write Hardware Register instruction (OP = 65:BF = 01).

6.2.1.12 (DIGIT 74 BIT 0) - SOFT FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the next instruction to be executed because a Soft Fault has been detected. A Soft Fault is detected when Soft Fault Enable is set and the soft fault digit, located in the Reinstate List entry for the current task, is not equal to zero. This indicator may only be set by the Hyper Call (OP = 62), Branch Communicate (OP = 30), Return (OP = 63) and Virtual Branch Reinstate (OP = 93) instructions.

6.2.1.13 (DIGIT 75 BIT 0) - TASK TIMER FAULT

This fault indicates that a Hardware Call procedure was executed that stored the address of the next instruction to be executed because the task timer reached a value of zero. See Appendix A - Compatibility Notes (A.45).

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	DESIGN SPECIFICATION REV.	****
6.2.2 (DIGIT 78-79) - A	ADDRESS ERROR EXTENSION (AEX)	
	Error Fault Indicator is set Address Error Extension byte of error.	
INFORMATI	EON	VALUE
General		00
Inva	alid Address Relationship	01
Нуре	er Call Function Limit Error	02
Odd	Operand Address	03
Inva	alid MAT Entry Type	04

Index Register, General
Invalid Arithmetic
Index Register Contains Undigit
Invalid Base Indicant
Stack Pointer (IX3) is negative
Stack Pointer (IX3) is odd
Base/Limit Error, General
Instruction Fetch
Address Resolution
Operand write
Operand Read
Global Link Address

Instruction retch	21
Address Resolution	22
Operand write	23
Operand Read	24
Global Link Address	25
Address Undigit, General	30
Instruction Fetch	31
Address Resolution	32
Operand Write	33
Operand Read	34
Global Link Address	35
Branch Address, General	40
Address >= Limit	41
Address Contains Undigit	42
Odd Address	43

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 75

# 6.2.2 (DIGIT 78-79) - ADDRESS ERROR EXTENSION (Continued)

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INFORMATION	VALUE
Invalid Environment Descriptor	50
Invalid Environment Number	51
Invalid Most Significant Digit	52
Index Contains Undigit	53
Memory Area Number Contains Undigit	54
Environment Number or Memory Area	
Number Out of Range, General	56
Environment Number Out of Range	e 57
Memory Area Number Out of Range	
Invalid Memory Area Table Entry	60
Invalid Environment Number	61
Invalid Most Significant Digit	62
Index Contains Undigit	63
Memory Area Number Contains Undigit Environment Number or Memory Area	64
Number Out of Range, General	66
Environment Number Out of Rang	e 67
Memory Area Number Out of Rang	
"E" Copy Type Entry points to a Cop	
Type Entry	69

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MPANY CO	NFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A	PAGE 76
nga ship aga seo sin din san sin		
6.2.3	(DIGIT 80-81) - INVALID INSTRUCTION EXTENSION	(IEX)
	When the Invalid Instruction Fault Indicator i Section 6.2.1.5), the Invalid Instruction Ex will further define the type of error.	
	INFORMATION	VALUE
	General	CO
	Invalid Operator Code	<b>C1</b>
	Privileged Mode Violation	02
	Invalid Address Controller	03
· · · ·	Stack Overflow ( $OP = 31$ )	04
	Counter Overflow	05
	Invalid Field Comparison	06
	Invalid Operand Field	07
	Invalid AF or BF	20
	Literal not Allowed	21
	Invalid Literal	22
	Invalid Indirect Field Length	23
	Invalid Variant	24
	Invalid AF Variant	25
	Invalid BF Variant	26
	Invalid Priviliged Primary Access	31
	Invalid Priviliged Secondary Access	32
	Invalid Attempt to Modify Original or	
	Fault Memory Area Table Entry	35
	Copy Protection Violation	36
	Stack Protection Violation	37

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			×									
7		INS	TRUCT	ION SET S	UMMARY	• ·						
				umber of :								
				on-extend						in d	igit	5.
	- Fi			omparison F indirec	and Uve	rtiow ti d	lags ch	ange	a.			
				F indirect								
S				NAME			ADDR'S	LG	LIT	AIN	EIN	FLG
						•						
				IC; Fixed								
	8.1	01	INC	Two-addr Three-addr Two-addr Three-add Multiply	ess Add		2	18	Y	Y	Y	Y
	8.2	02	ADD	Three-ad	dress Ad	d	3	24	Ŷ	Y	Y	Y
	8-3	03	DEC	Two-addr	ess Subt	ract	2	18	Y	Y	Y	Y
	8-4	04	SUB	Three-ad	dress Su	btract	3	24	Y	Y	Ŷ	Y
	85	05	MPY	Multiply Divide			.5	24	₹ °	Ŷ	T T	Y
	0-0	00	DIV	סוערט	,		2	24	T	T	ł	T
	9.	ARI	THMET	IC; Fixed	Point,	Fixed F	iela Le	ngth				
	9.1	58	ILD	Integer	Load		1	8	N N N	N	N	Y
	9.2	59	IST	Integer	Store		1	8	Ν	N	N	Ý
	9.3	50	IAD	Integer	Add		1	8	Ν	Ν	N	Y
	9_4	51	IAS	Integer	Add/Stor	e	1	8	N	N	N	Y
				Integer								
	9.6	53	ISS				1	8	N	N	N	Y
	9.7	54	IMU				1	8	N	N	N	Y
	9-8 9-9	55 57	IMS Imi	Integer Incremen	• •		1	8 8	N N	N N	N N	Y Y
				C; Floati	-		-	-				•
. 1	0.1	78	RLD	Real Loa	d		1	8	N	N	N	Y
	0.2	79	RST	Real Sto			1	8	N	N	N	Ŷ
	0_3	70	RAA	Real Add			1	8	N	N	N	Ŷ
	0.4	71	RAS	Real Add			- 1	8	N	N	N	Ŷ
	0.5	72	RSU	Real Sub			1	8	N	Ν	N	Y
	0.6	73	RSS	Real Sub		ore	1	8	N	N	N	Y
	0.7	74	RMU	Real Mul	• •		1	8	N	N	N	Y
	0.8	75	RMS	Real Mul		ore	1	- 8	N	N	N	Y
	0_9	76	RDV	Real Div			1	8	N	N	N	Y
	0.10		RDS				1	8	N	N	N	Y
4	0.11	X 4	ACM	Accumula	tor Mani	nulate	0	4	N	N	N	Y

BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 78

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7:

INSTRUCTION SET SUMMARY (Continued)

SEC.	OP		NAME			ADDR S	LG	LIT	AIN	BIN	FLG
11.		ESS B	RANCHIN	G						;	
11.1	20	NOP	No Ope	rat	ion	1	8	N	N	N	N
11.1.1	21	LSS	Branch	on	Less Than	1	8	N	N	N	N
11.1	22	EQL	Branch	on	Equal	1	8	N	N.	N	Ň
11.1	23	LEQ	Branch.	on	Less Than						
					or Equal	1	8	N	N	N	N
11.1	24	GTR	Branch	on	Greater Than		8	N	Ň	N	N
		NEQ			Not Equal	1	8	N	Ν	N	Ň
11.1	26	GEQ	Branch	on	Greater Than						
					or Equal		8	N	N	N	Ň
11.1		BUN	Branch	Un	conditional	1	8	N	N	N	N
11.1	28	OFL	Branch	on	Overflow	1	8	N	N	N	N
11.1		NUL	Branch	on	NULL	1	8	N	N	N	Ν
11.1	28	GTN	Branch	on	Greater or Nu	LL 1	8	N	N	N	N
11.1	81	LSS	Branch	on	Less Than	1	8	N	N	N	N
11.1	82	EQL	Branch	on	Equal	1000	8	N	N	N	N
11_1	83	LEQ	Branch	on	Less Than						
					or Equal	. 1	8	N	- N	N	Ν
11.1	84	GTR	Branch	on	Greater Than	1	8	N	N	N	N
11.1	85	NEQ	Branch	on	Not Equal	1	8	N 1	N	N	Ν
11.1	86	GEQ	Branch	on	Greater Than						
					or Equal		8	N	N	N	N
11-1	BA	NUL	Branch	on	Null	1	8	N	N	N	N
11.1	88	GTN	Branch	on	Greater or Nu	LL 1	8	N	N	N	N
11.1	E1	LSS	Branch	on	Less Than	1	8	N	N	N	N
11-1	E2	EQL	Branch	on	Equal	1	8	N	N	N	N
11.1	E3	LEQ	Branch	on	Less Than	•					•.
	•			•	or Equal	1	8	N	N	N	Ν
11.1	E4	GTR	Branch	o.n	Greater Than		8	N	N	N	Ν
11.1	E5	NEQ	Branch	on	Not Equal	1	8	N	N	N	N
11_1	£6	GEQ	Branch	on	Greater Than						
					or Equal	1	8	N	N	N	Ν
11.1	EA	NUL	Branch	on	Null	1	8	N	N	N	N
11.1	EB	GTN	Branch	on	Greater or Nu	ιι 1	8	N	N	N	N

EURROUGHS CORPORATION	MENT GROUP V SERIES INSTRUCTION SET	
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 79

7

INSTRUCTION SET SUMMARY (Continued)

SEC.	0 P		NAME		ADDR"S	LG	LIT	AIN	BIN	FLG
11.		ESS B	RANCHING							
11.1	F1	LSS	Branch or	Less Than	1	8	N	N	N	N
11.1	F2	EQL	Branch or	n Equal	1	8	Ν	N	N	N
11.1	F3	LEQ	Branch or	Less Than					. •	
		•		or Equal	1	8	N	N	N	N
11.1	F4	GTR	Branch or	Greater Than	1	8	N	N	N	N
11_1	F5	NEQ	Branch or	Not Equal	1	8	Ν	N	N	N
11.1	FÓ	GEQ	Branch or	Greater Than						
				or Equal	1	8	N	N	Ν	N
11.1	FA	NUL	Branch or	NULL	1	8	N	Ν	N	N
11.1	FB	GTN	Branch or	n Greater or Nu	LL 1	8	N	N	N	N
12.	HALT	S								
12.1	29	HBR	Halt Bran	nch	1	8	N	N	N	N
12_2	48	HBK	Halt Brea	akpoint	C	6	N	Y	N	N
13.	ENVI	RONME	NT CHANGE							
13.1	30	BCT	Branch Co	ommunicate	0	6	N	Y	Y	Y
13.2	31	NTR	Enter		1	12+	N	Y	Y	Y
13.3	32	EXT	Exit		1	8	N	N	N	Y
13.4	35	VEN	Virtual B	Enter	2 2	18	¥+	Y	Y	Y
13.5	62	HCL	Hyper Cal	.t	2	18	<u>.</u> ¥+	¥ -	Y	Y
13_6	63	RET	Return		C	4	N	Y	Y	Y
13.7	61	ASP		tack Pointer	1	12	Y	Y	Y	N
13.8		INT	Interrupt		1	12	N	Y	Y	N
13.9	93	BRV		Branch Reinstat	e O	4	N	Ŷ	N	Y
	+	- = n	Characters	s (Stack Parame	ters)	follo	w as	spe	cifi	e d

by the instruction (O=<n=<9,999 bytes).

Y+ = Special Literal value.

SYSTE	UGHS C M DEVE ENA PL	LOPM	ENT GI	ROUP	V SERIES	INSTRUCT		 + SET	19	97 5	390
					 +=============					-	
COPPA	NY CON	FIDE	NTIAL	SYSTEM D	ESIGN SPECI	FICATION	REV	- A	P .	AGE	80
·, · 7.		INS	TRUCT	LON SET SUM	MARY (Conti	inued)					•
	SEC.	OP		NAME		ADDR'S	LG	LIT	AIN	BIN	FL
	14.		MOVE	MENT							
	16-1	0.8	MVD	Move Data		3	24	N	Y	¥	N
				Move Links		3	24	N.			
				Move Alpha	numeric	3 3 2	18	Y	Ý	Ŷ	Ϋ́
				Move Numer		Ž	18	Y Y	Ŷ	Y .	Ý
				Move Words		2	18	N	Ý	· Y	Ň
	14.6	13	MVC	Move and C	lear Words	2	18	Ň	· Y	Ŷ	N
	14.7	14	MVR	Move Repea	t	2	18	N N Y	Ŷ	Ŷ	Ņ
				Translate		3	24	Ň	Ŷ	Ŷ	Ň
	14.9					3	24			Y	Y
						n de Maria de Carlos de Carlos Anticipados de Carlos de Carlos					•
	15.	LOGI	CAL				•				
	15.1	16	SDE	Scan-Delim	iter Equal	2	18	Y	Y.	Y	Y
	15.2	17	SDU	Scan-Delim	iter Unequal	2	18	Y	Ŷ	Ŷ	Ý
	15.3	18	SZE	Scan-Zone	iter Equal iter Unequal Equal	2	18	Y	Y	Y .	Ý
	15.4	19	SZU	Scan-Zone	Jnequal	2	18	¥	Y	Y.	Y
	15_5	39	SEA	Search		3	24	Y	Y	Y.	Y
				Search Lin	k List	2	18	Ŷ	Ŷ	Y	Ŷ
	15.7	38	SLD	Search Lin	k Delink			¥			
	15-8	64	SLT	Search Lis		3	24	Ŷ	Y	Ŷ	Ŷ
	15.9	66	STB	Search Tab		3	24	Y	Y	Y	Ŷ
	15.10	40	BZT	Bit Zero T	est	1	12	Y	Y	N	Y
	15.11		BOT	Bit One Te		1	12	Y Y	Y	N	Ŷ
	15-12		CPA	Compare AL		2	18	Y	Y	Y	Ŷ
	15.13		CPN	Compare Nu		2	18	Y.	Y	Ŷ	Ý
	15-14		BRT	Bit Reset		1	12	N	Ý	N	Ý
	15.15		BST	Bit Set		1	12	N	Y.	N	Y
	15.16		AND	Logical An	d	3	24	Y	Ŷ	Ŷ	Ý
	15.17		ORR	Logical Or		3	24	Ŷ	Ŷ	Y	Ý
	15.18		NO T	Logical No		3	24	Ŷ	Y	Ŷ	Ŷ

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				N	+			+   +	19	97 5	 390
	ENA PL			ROUP	V SERIES	ENSTRUCT	ION	SET			
0 M P A	NY CON	IFIDE	NTIAL	SYSTEM D	ESIGN SPECIFI	LCATION	REV	. A	P	AGE	81
7		INS	TRUCT	ION SET SUM	MARY (Contin	nued)					
	SEC.	0 P		NAME		ADDR'S	LG	LIT	AIN	BIN	FLG
		INPU	T/OUT	PUT							
	16.1	94 92	IIO RAD	Initiate I Read addre	/0 ss t Descriptor 0 te	1	12 12	Y N	Y Y	Y Y	Y Y
	16.4	85 98	C I O I O C	Convert I/ I/O Comple	te te	2 2	18 18	N Y	Y Y	Y Y Y	Y Y Y
	17.	BINA	RY/DE	CIMAL CONVE	RSION				•		
				Decimal to Binary to		2 2	18 18	Y Y	Y Y	Y Y	Y Y
	18.	TIME	-0F-D	AY TIMER							
				Read Time Set Time o		1 1	12 12	N N	Y Y	Y Y	N N
	19.	MEAS	UREME	NT							
	19.1	87	MOP	Measuremen	t OP	2	18	N	Y	¥	N
	20.	MISC	ELANE	ous							
	20.1	86 67	ATE LIX	Alter Tabl	e Entry Registers	2	18 12	N	Y Y	Y ¥	N
	20.3	68	SIX		x Registers	1	12	N	Y	Ŷ	N N
	20.4	60	LOK	Lock/Unloc		1	12	N	Ŷ	Ŷ	Y
	20.7	65	WHR		ware Register		12	N	Ŷ	Ŷ	N
	20.8	47	SMF	Set Mode		G	6	N	Ŷ	Ŷ	N
	20.9	AB	BAD	Fail		1	12	N	Ň	N	N
	20.10		SST	System Sta	tus	1	12	N	Y	Ŷ	N
	21.	STRI	NG								
	21.1	AO	MVS	Move Strin	as	2	18	N	Y	Y	Y
	21.2	A1	CPS	Compare St		2	18	N	Ŷ	Ŷ	Ý
	21.3	A2	HSH	Hash Strin		2	18	N	Ŷ	Ŷ	N

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OMPANY C	DNFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 82
8	ARITHMETIC; FIXED POINT, VARIABLE FIELD LENGTH
8.1	TWO ADDRESS ADD (INC)/OP=01
	Format
	++   OP   AF   BF   A   B   ++
	$\mathbf{0P} = 01$
	AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of "OO" is equal to a length of 100 units.
	BF = Length of the "B" field. BF may be indirect. A value of "00" is equal to a length of 100 units.
	A = Address of the addend field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	B = Address of the augend and sum field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	Function
	The Two Address Add instruction adds the contents of one memory location (A) to the contents of a second memory location (B) and stores the sum in the second memory location (B) unless an overflow condition exists. If the number of significant digits in the result is greater than the sum field length, the sum field will be unchanged, the Comparison Flags will be unchanged and the Overflow Flag will be set.

BURROUGHS CORPORATION System development group Pasacena plant	V SERIES INSTRUCTION SET	1997 5390
CCMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 83

### 8.1 TWO-ADDRESS ADD (INC)/OP=01 (Continued)

Store the absolute value of the sum when the sum field data type is unsigned (UN or UA). Store the standard EBCDIC form of the result sign as the first digit of the result when the sum field data type is SN. Fill the zone digit with the EBCDIC numeric subset code (F) when the sum field data type is alphanumeric (UA).

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The sign of a zero is always considered to be positive.

If the addend and the augend are of unequal lengths (AF not equal to BF), the shorter of the two is treated as if it has been left filled with zero's.

Only the numeric digits of an alphanumeric field enter into the operation. Unsigned (UN or UA) operands are assumed to be positive.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison Flags

In all cases except overflow, set the Comparison Flags to indicate whether the sum is greater than (HIGH), equal to (EQUAL), or less than (LOW) zero.

Overlap

"A" and "B" may totally overlap or may have matching type-address overlap (See 4.9.4). Partial overlap of "A" and "B" other than matching type-address overlap, may produce incompatible results. See Appendix A - Compatibility Notes (A.08).

	PORATION		<b>+</b>		 +	1997 5390
STEM DEVELOPMENT GROUP Sacena plant		OUP	V SI	ERIES INS	STRUCTION SET	
PANY CONI	IDENTIAL	SYSTEM	DESIGN	SPECIFIC	ATION REV. A	PAGE 84
8.1	TWO-ADDRE	ESS ADD (1	[NC]/OP=(	J1 (Cor	ntinued)	
	Examples					
	EXAN	IPLE (1)	Add an I	Alpha Fie	eld to a Sign	ed Field
	C	P AF BF	÷ an A		8	
	-	01 02 04,	A FIELD	(UA), B	FIELD (SN)	
				BEFORE	AFTER	
•		A FIELD B FIELD		C1E7 +0257	unchanged C0274	
		COMPARI: Overflow		nn nn	HI GH unchanged	an a
	EXAN	IPLE (2)	Add wit	h Overfl	ow condition	
	landa da Carlos Contra da Carlos	OP AF BF	en de la constante de la const Al constante de la constante de		8	
•	-	1 02 03.	A FIFLD	(UN), B	FIELD (UN)	
				BEFORE	AFTER	
		A FIELD B FIELD		18 985	unchanged unchanged	
· · · ·		COMPARI Overfloi		nn	unchanged ON	

								+	
				,				1	
BURRCUG					+			+	1997 5390
SYSTEM I	DEVE	OPME	NT GRO	UP	1				
PASADENI	A PL	ANT			I V	SERIES I	NSTRUCTIO	N SET	
					1				
					+				
CCMPANY	CON	FIDEN	TIAL	SYSTEM	DESIGN	SPECIFI	CATION F	REV. A	PAGE 85
									***********
8-2		THRE	FADDR	ESS ADD	(ADD)/	0P=02			
002									
		Form	at						
							+	+	
								:	
		+	-+	++		- +	+	+	
			~ ~						
	•	0P =	02						
		A.C	1	6 <b>64 8</b> 6.		iald Ac	move ha	indian	** ** ***
		AF =							ct or may lue of "00"
						h of 100			
			13 EU		a cenyc		unitse		
		BF =	Lenat	h of th	a ngn f	ield. BF	may be i	ndirec	t. A value
·							h of 100		
						<b>-</b>			
		A =	Addres	ss of t	he adde	nd field	. Address	a may b	e indexed,
			indir	ect or	exten	ded. T	he addres	s cont	roller data
			type i	may be	UN, SN,	or UA.			
				_					<b>.</b>
		8 =							e indexed,
							he addres	is cont	roller data
			τγρει	may be i	JN, SN,	OF UA.			
		c =	Addee	ee of t	ho eum	field	Address	may h	e indexed,
									roller data
					UN, SN,				
			-76-			•••••			
		Func	tion						
									ents of one
									cona memory
									ry location
		(0)							e sum field
		the							values. If is greater
					-		the sum		-
									ged and the
					l be se			411 11 011 011	JEA ANA CHE
			1		~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~				

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	S CORFORATION	+		1997 539	
ASACENA	EVELCPMENT GROUP Plant	V SERIES IN	STRUCTION SET	SET	
CMPANY	CONFIDENTIAL SYSTEM	DESIGN SPECIFIC	ATION REV. A	PAGE 8	
8.2	THREE ADDRESS ADD	(100)/08-02 ()	(antinued)		
0	Ince Augress Aug		, une mueur		
	Store the absolute data type is us EBCDIC form of the	nsigned (UN or I	JA). Store th	ie standar	
9	result when the s digit with the EB	sum field data ty CDIC subset code	pe is SN. Fil	l the zon	
	data type is alph	anumeric (UA).			
	The sign of a zero	o sum is always (	positive.		
	If the addend and equal to BF), the	shorter of the	two will be tre		
	it has been left	filled with zero	'S.		
	Only the numeric of into the operation		lphanumeric fi	ield ente	
	Unsigned (UN or U	A) operands are	assumed to be p	ositive.	
	If the operand da sign digit, cau Appendix A - Comp	se an Invalid A	rithmetic Data		
	Comparison Flags				
	In all cases excer indicate whether (EQUAL), or less	the sum is great			
	Overlap				
	"A" and "B" may p may totally ove type-address over	rlap with "C",	or may have		
	Partial overlap matching type-ad results. See Appe	dress overlap,	may produce in	compatibl	

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BURROUGHS (	ORPORATION		+		+	1997 5390
	LOPMENT GROU		1			
PASADENA PL	ANT		I V S	ERIES INS	STRUCTION SET	
COMPANY CON	FIDENTIAL	SYSTEM	DESIGN	SPECIFIC	TION REV. A	PAGE 87
8_2	THREE ADDRI	ESS ADD	{ A D D ) / O	P=02 (.0	Continued)	
	Examples					
	EXAMPL	.E (1)		Unsigned a Signed	Field to a Si Sum	igned Field
	0P	AF BF	A		В	C
				<i></i>		
	02	02 05,	A FIELD	(UN), B	FIELD (SN), (	C FIELD (SN)
		•		BEFORE	AFTER	
		FIELD		20	unchanged	
		B FIELD		+00015		
	(	FIELD		nnnnn	-	
		COMPARIS	SON	nnn	HIGH	
		VERFLOW		nnn		
	EXAMPL	.E (2)			Field to a Sined Alpha Sum	igned Field
		A.F. 0.F		-	_	
	0P 	AF BF	• A		8	C 
	02	02 05,	A FIELD	(UN), B	FIELD (SN), (	FIELD (UA)
				BEFORE	AFTER	
		FIELD		10	unchanged	
		B FIELD		D00050	unchanged	
	(	FIELD	nn	nnnnnnn	FOFOFOF4FO	
		COMPARIS	SON	nnn	LOW	
	· (	DVERFLOW	ł	nnn	unchanged	

BURROUGHS CORPORATION		+	•	1997 5390			
SYSTEM DEVE Pasadena pl	LOPMENT GROUP Ant	   V SERIES 1 	V SERIES INSTRUCTION SET				
OMPANY CON	FIDENTIAL SYSTEM	DESIGN SPECIFI	CATION REV. A	PAGE 88			
8.2	THREE ADDRESS ADD	(ADD)/0P=02	(Continued)				
	EXAMPLE (3)	Add an Alpha I	Field to an Alph	a Field			
	OP AF BF		8	C			
	02 02 02,	A FIELD (UA),	B FIELD (UA), C	FIELD (UA)			
		BEFOR	E AFTER				
	A FIELD	F4 F0	unchanged				
an a	8 FIELD	C1C2	unchanged				
	C FIELD	กกกก	F5F2				
	COMPARIS	ON nnn	HIGH				
	OVERFLOW	nnn	unchanged				
	a de la companya de Esta de la companya de						
		Add two field	s with an Overfl	ou Conditio			
	EAMPLE (4)	NGG LBG IJELU:	S WILH de VVerit	ow condition			
and a gradient of the second	OP AF BF		8				
	02 02 02,	A FIELD (UN),	B FIELD (UN), C	FIELD (SN)			
		BEFORE	AFTER				
		DEFVRE	I AFICK				
	A FIELD	61	unchanged				
	B FIELD	53, 1	unchanged				
	C FIELD	nn	unchanged				
	COMPARIS		unchanged				
	OVERFLOW	nnn	ON				
				an a			
and							

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STEM DEV	CORPORATION +
SADENA P	DNFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 89
8.3	TWO ADDRESS SUBTRACT (DEC)/OP=03
	Format
	++   OP   AF   BF   A   B   ++
x	OP = 03
	AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of "OO" is equal to a length of 100 units.
	BF = Length of the "B" field. BF may be indirect. A value of "OO" is equal to a length 100 units.
	A = Address of the subtrahend field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	B = Address of the minuend/difference field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.

Function

The Two Address Subtract instruction subtracts the contents of memory location (A) from the contents of a second memory location (B) and stores the difference in the second memory location (B) unless an overflow condition exists.

If the number of significant digits in the result is greater than the difference field length, the difference field will be unchanged, the Comparison Flags will be unchanged and the Overflow Flag will be set.

Store the absolute value of the difference when the difference field is unsigned (UN or UA). Store the standard EBCDIC form of the result sign as the first digit of the result when the difference field data type is SN. fill the zone digit with the EBCDIC numeric subset code (F) when the difference field data type is alchanumeric (UA).

	CORPORATION	• • • • • • • •	•		 +	1997 5	390
SYSTEM DE Pasadena	VELOPMENT GRO Plant	UP     	V SERIES	INSTRUCT	LON SET		
COMPANY C	ONFIDENTIAL	+- SYSTEM DES	IGN SPECI	FICATION	REV. A	PAGE	90
8.3	TWO ADDRES	S SUBTRACT	(DEC)/0P=(	03 (Con	tinued)		
		f a zero di				e.	

If the subtramend and minuend are of unequal length (AF not equal to BF), the shorter of the two is treated as if it has been left filled with zero*s.

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Only the numeric digits of an alphanumeric field enter into the operation. Unsigned (UN or UA) operands are assumed to be positive.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison Flags

and a start of the second s The second se The second se

In all cases, except overflow, set the Comparison Flags to indicate whether the difference is greater than (HIGH), equal to (EQUAL), or less than (LOW) zero.

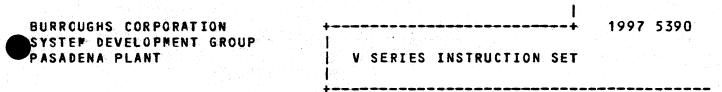
Overlap

"A" and "B" may totally overlap or may have matching type-address overlap (See 4.9.4). Partial overlap of "A" and "B" other than matching type-address overlap, may produce incompatible results. See Appendix A - Compatibility Notes (A.08).

--Burroughs Prior Written Consent Required For Disclosure Of This Data--

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	CORPORATION /ELCPMENT GR PLANT		V SERIES INS	1997 5390	
COMPANY CO	DNFIDENTIAL	+- System des	SIGN SPECIFICA	TION REV. A	PAGE 91
8.3	TWO ADDRE	SS SUBTRACT	(DEC)/0P=03	(Continued)	
	Examples			•	· · · ·
	EXAM	PLE (1) Sul	otract two pos	itive numbers	
	0	P AF BF	A	В	
	0	3 03 03, A I	IELD (SN), B	FIELD (SN)	
			BEFORE	AFTER	
	•	A FIELD B FIELD	+014 +062	unchanged CO48	
		COMPARISON Overflow	nnn	HIGH unchanged	
			en e		
•	EXAM	IPLE (2) Sul	otract two Neg	ative numbers	
	. 0	P AF BF	Α	В	
	0	3 03 03, A	FIELD (SN), B	FIELD (SN)	
			BEFORE	AFTER	
		A FIELD B FIELD	D035 D029	unchanged COO6	
	2. 2. ¹ 8	COMPARISON Overflow	nnn nnn	HIGH unchanged	
			•		
	· ·				



COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 92

8_3 TWO ADDRESS SUBTRACT (DEC)/OP=03 (Continued)

EXAMPLE (3) Subtract Signed Field From Unsigned Field

+-

	03	C2	03, /	A E	IELD	(SN), B	FIELD	(UN)
	0P	AF	BF		. <b>A</b> s		<b>B</b>	
** 15 1 1 1								

BEFORE AFTER

A FIELD	D71	unchanged
8 FIELD	121	192
COMPARISON	nnn	HIGH
Overflow	nnn	unchanged

EXAMPLE (4) Subtract Unsigned Field from Signed Field OP AF BF A B ----

03 G3.03, A FIELD, (UN), B FIELD (SN)

	BEFORE	AFTER
A FIELD B FIELD	259 +138	unchanged D121
COMPARISON	nnn	LOW
OVERFLOW	nnn	unchanged

المدارح وثيرها عوبت الصوحة تتجب

BURROUGHS CORPORATION System development group	  +	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 93

8.3 TWO ADDRESS SUBTRACT (DEC)/OP=03 (Continued)

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EXAMPLE (5) Subtract Two Signed Fields, Overflow Condition

0P	AF	8 F	A		в	
03	03	03,	A FIELD	(SN), E	B FIELD (SN)	

	BEFORE	AFTER
A FIELD	D556	unchanged
B FIELD	+942	unchanged
COMPARISON	nnn	unchanged
OVERFLOW	nnn	ON

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MPANY CON	FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE	9
)		,
8.4	THREE ADDRESS SUBTRACT (SUB)/OP=04	
	Format	
	++++++++	
	OP AF I BF I A I B I C I	
	++++++++++	
	OP = 04	
	AF = Length of the "A" field. AF may be indirect or	
e en	indicate the A-syllable is a literal. A value of " is equal to a length of 100 units.	'00'
	BF = Length of the "B" field. BF may be indirect. A va	itu
	of "00" is equal to a length of 100 units.	
	A = Address of the subtrahend field. Address may	
	indexed, indirect or extended. The addr controller data type may be UN, SN, or UA.	.62
	B = Address of the minuend field. Address may be index	ed
	indirect or extended. The address controller d	
	type may be UN, SN, or UA.	
	C = Address of the difference field. Address may indexed, indirect or extended. The addr	
•	controller data type may be UN, SN, or UA.	
	Function	
	The Three Address Subtract instruction subtracts	
je star i star star star star star star star star	contents of one memory location (A) from the contents of second memory location (B) and stores the difference in	
	third memory location (C) unless an overflow condit	tio
	exists. The difference field length is equal to the lar	ge
	of AF or BF.	
•	If the number of significant digits in the result	
	greater than the difference field length, the differe	
	field will be unchanged, the Comparison Flags will unchanged and the Overflow Flag will be set.	D

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SYSTEM DEVELOPMENT GROUP Pasadena plant		V SERIES INSTRUCTION SET	
MPANY C	ONFIDENTIAL SYSTEM	ESIGN SPECIFICATION REV. A	PAGE 9
8.4	THREE ADDRESS SUBT	ACT (SUE)/OP=04 (Continue	d)
	difference field standard EBCDIC for of the result who Fill the zone digin	value of the differenc is unsigned (UN or UA). m of the result sign as the n the difference field data with the EBCDIC numeric ference field data type is	Store the first digit type is SN. subset code
	The sign of a zero	difference is always positi	ve.
• · ·		nd minuend are of unequal , the shorter field is trea d with zero's.	
	Only the numeric d into the operation	gits of an alphanumeric	field enter
	Unsigned (UN or UA)	fields are assumed to be p	ositive.
	sign digit, caus	contains undigits other t an Invalid Arithmetic Dat ibility Notes (A.16).	
	Comparison Flags		
	indicate whether	t overflow, set the Compari the difference is greater or less than (LOW) zero.	
	Overlap 		
		tially or totally overlap. ap with "C", or may ha p. (See 4.9.4)	
	matching type-add	"A" or "B" with "C", ess overlap, may produce lix A - Compatibility Notes	incompatible

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OMPANY CON	FIDENTIAL SYSTEM DE	SIGN SPECIFIC	ATION REV. A	PAGE 96			
8-4	THREE ADDRESS SUBTRA	CT (SUB)/OP=C	4 (Continued)				
	Examples						
	EXAMPLE (1) Su Fi	btract an Uns eld	igned Field fr	om an Alpha			
	OP AF BF		B	C			
	04 01 05, A	FIELD (UN), E	R FIELD (UA), C	FIELD (SN)			
		BEFORE	AFTER				
	A FIELD B FIELD C FIELD	5 c1c2c3c4c5 nnnnn	unchanged unchanged C12340				
	COMPARISON Overflow	nnn nnn	HIGH unchanged				
	a da serie de la companya de la comp Porte de la companya d						
				and a second			
				94 194 194 194 194 194 194 194 194 194 1			

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ASACENA PL	ANT V SERIES INSTRUCTION SET
COMPANY CON	+
8.5	MULTIPLY (MPY)/OP=05
	Format 
	ttttttt
	0P, = 05
	AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of"00" is equal to a length of 100 units.
•	BF = Length of the "B" field. BF may be indirect. A value of "00" is equal to a length of 100 units.
	A = Address of the multiplier field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	B = Address of the multiplicand field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	C = Address of the product field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	Function
	The multiply instruction multiplies the contents of one memory location (B) by the contents of a second memory location (A) and stores the product in a third memory location (C). The product field length is the sum of AF and BF, and could be as long as 200 units.
	Store the absolute value of the product when the product field data type is unsigned (UN or UA). Store the standard EBCDIC form of the sign as the first digit of the result when the product field data type is SN. Fill the zone digit with the EBCDIC numeric subset code (F) when

the product field data type is alphanumeric (UA).

EURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	     V SERIES INSTRUCTION SET	1997 5390		
CCMPANY CONFIDENTIAL SYST	1 + EM DESIGN SPECIFICATION REV. A	PAGE 98		

8.5 NULTIPLY (MPY)/OP=05 (Continued)

The Overflow Flag is not affected by this instruction.

The sign of a zero product is always positive.

Only the numeric digits of an alphanumeric field (UA) enter into the operation. Unsigned fields are assumed to be positive.

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If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison Flags

In all cases, set the Comparison Flags to indicate whether the product is positive (HIGH), equal to zero (EQUAL) or negative (LOW).

Overlap

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"A" and "B" may partially or totally overlap.

Overlap of "A" and "B" with "C", other than matching type-address overlap, may produce incompatible results. See Appendix A - Compatibility Notes (A.10).

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8.5	MULTI	PLY (I	4P Y.) / 0P:	=05	(Co	ntinue	d)					
	Examp	les										
•		EXAMPI	_E (1)	Multi Field		an Alı	pha Fie	ld <b>þy a</b> n	Unsigi	ned		
		0P	AF BF		A		8		с 			
		05	02 05,	AFIE	LD	(UA), E	B FIELD	(UN), C	FIELD	(SN)		
•						BEFORE		AFTER				
	·											
			A FIELD 3 FIELD			0102 00011		n <b>chan</b> ged n <b>chan</b> ged				
			C FIELD			nnnn		c0000132				
		(	COMPARI	SON		nnn		HIGH				
		EXAMPL	LE (2)	Multi	ply	Two S	igned N	umbers				
		0 P	AF BF		A		В		C			
		05	02 02,	A FIE	LD	(SN), 1	B FIELD	(SN), C	FIELD	(SN)		
				• •		BEFORE	A	FTER				
			A FIELD			D15	unc	hanged				
			B FIELD			D17		hanged 0255				
			C FIELD			nennn	6	0233				
		(	COMPARI	SON		nnn		HIGH				
	• • 0		a na ana taon ing sa sa	* = *		• • •						
			· · · · · · · · · · · · · · · · · · ·			· •	·		•			

BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION BEY A PAGE 100

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 100

8.6 DIVIDE (DIV)/OF=06

- OP = 06
- AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of "00" is equal to a length of 100 units.
- BF = Length of the "B" field. BF may be indirect. A value of "OO" is equal to a length of 100 units.
  - A = Address of the divisor field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
  - B = Address of the dividend/remainder field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
  - C = Address of the quotient field. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.

# Function

The divide instruction divides the contents of one memory Location (B) by the contents of a second memory location (A) storing the remainder in the "B" data field and storing the quotient in a third memory location (C).

The length of the dividend field must be greater than the length of the divisor field (BF greater than AF). The length of the quotient field is the difference in length of the "A" and "B" fields (BF-AF). If the result is too large to fit into the quotient field or if BF is not greater than AF, the division is not performed, the contents of "B" and "C" are unchanged, the Comparison Flags are unchanged, and the Overflow Flag is set.

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 101

#### 8.6 DIVIDE (DIV)/OP=06 (Continued)

If the absolute value of the divisor is not greater than the absolute value of the equivalent number of leading digits of the dividend, the division is not performed and the Overflow Flag is set with the Comparison Flags remaining unchanged. Note that a divisor which is zero will fail this test and the Overflow Flag will be set.

The absolute value of the quotient is stored when the quotient field data type is unsigned (UN or UA). The standard EBCDIC form of the sign is stored as the first digit of the result when the quotient data type is SN. The zone digits are filled with the EBCDIC numeric subset code (F) when the quotient field data type is alphanumeric (UA).

The absolute value of the remainder is stored when the remainder field data type is unsigned (UN or UA). The standard EBCDIC form of the sign is stored as the first digit of the result when the remainder data type is SN. The zone digits are filled with the EBCDIC numeric subset code (F) when the remainder field data type is alphanumeric (UA).

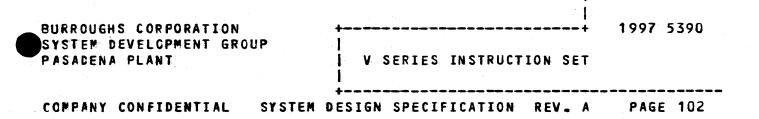
Only the numeric digits of an alphanumeric field (UA) enter into the operation.

Unsigned fields are assumed to be positive.

The sign of the quotient is positive if the sign of the divisor and the dividend are the same or the quotient is zero, otherwise the sign is negative.

If the dividend data type is SN, the sign of the dividend will be left unchanged in memory and will thus become the sign of the remainder. Therefore this final remainder sign could be other than "C" or "D" and a remainder of zero magnitude could have a negative sign.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).



8.6 DIVIDE (DIV)/OP=06 (Continued)

# Comparison Flags

In all cases, except overflow, set the Comparison Flags to indicate whether the quotient is positive (HIGH), equal to zero (EQUAL) or negative (LOW).

## Overlap

Partial overlap of the dividend field (B) and either of the other operands may produce inconsistent results.

If the address of the dividend field is the same as the address of the quotient field (B = C) and the respective address controllers are equal (BC = CC), a result will be produced that consists of the quotient followed by the least significant AF units of the remainder. In the case of SN data, the sign of the quotient will be stored in the first digit of the result followed by the quotient and the least significant AF digits of the remainder.

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# Examples

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EXAMPL	LE (1)	Divide Tu	lo Signe	d Numb	ers	
OP	AF BF	entro de Caracteria de Cara Caracteria de Caracteria de		8		C
06	01 04,		(SN), B Before		(SN) Ter	, C FIELD (SN)
	A FIELD B FIELD C FIELD		+9 +0101 nnnn	+0	ange 002 011	Remainder
	COMPARIS DVERFLOW		ุกกก กกก		IGH ange	d

					+-	4007 5700
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CMPANY (	CONFIDENTIAL	SYSTEM	+ DESIGN	SPECIFI	CATION REV. A	PAGE 103
8.6	DIVIBE (DI	(V)/0P=0	6 (Con	tinued)		
	EXAMF	PLE (2)	Divide	Two Sig	ned Fields, Ne	gative Number
	OF	AF BF	A	·	B	C
	00	5 02 05,	A FIEL	- D (SN), I	B FIELD (SN),	C FIELD (SN)
				BEFORE	AFTER	
		A FIELD B FIELD C FIELD	Í	D12 D00187 nnnn	unchanged D00007 Re C015 Qu	emainder Jotient
		COMPARI: Overfloi		nnn nnn	HIGH unchanged	
	EXAMP	PLE (3)	Divide	Producia	ng Overflow (Lo	ength Problem
	O F	P AF BF	A		8	C
		5 04 03,	A FIEL	- D (SN), I	B FIELD (SN), (	FIELD (SN)
				BEFORE	AFTER	
		A FIELD		01014	unchanged	
		B FIELD			unchanged	
		C FIELD		nnn	unchanged	•
		COMPARIS OVERFLO		កកក កកក	unchanged ON	
	EXAMP	PLE (4)	Divide	Produci	ng Overflow (Da	ata Problem)
•	0 F	AF BF	A		B	C
		5 02 03,	A FIEL	- D (SN), I	B FIELD (SN), (	FIELD (SN)
			Į	BEFORE	AFTER	
	• . *	A FIELD		D11	unchanged	
		8 FIELD		D125	unchanged	
		C FIELD		nnn	unchanged	٢
		COMPARI		nnn	unchanged	、
		OVERFLO	W	nnn	ON	

BURROUGHS CORPORATION System development group Pasadena plant		 ++ 1997 5390     V SERIES INSTRUCTION SET				
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		n -				
	04 40					
8.6 DIVIDE (DIV)/OP=	uo (con	tinued/				
EXAMPLE (5)	Dividé	By Zero	and a second second Second second			
OP AF BF			B	C		
06 02 03	, A FIEL	- D (SN), E	B FIELD (SN),	C FIELD (	SN)	
		BEFORE	AFTER			
A FIEL B FIEL C FIEL	D	+00 D125 D000	un changed un changed un changed			
COMPAR Overfl		nnn nnn	unchanged ON			
EXAMPLE (6)	Total	Overlap (	of "B" & "C".			
OP AF BF	A		B	C		
06 02 04	, A FIEL	D (UN), E	B FIELD (UN),	B FIELD (	UN)	
		BEFORE	AFTER			
A FIEL B FIEL		13 1127	unchanged 8609			
COMPAR Overfl		nnn nnn	HIGH unchanged			

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BURROUGHS CORPORATION System development group	++	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 105

9

## ARITHMETIC; FIXED POINT, FIXED FIELD LENGTH

Fixed field Length arithmetic instructions use a 20 digit accumulator which holds the instruction result within the processor as an operand for a subsequent operation. Every instruction has an implied reference to the accumulator.

The fixed point (integer) format consists of an implied signed exponent field (+08) (of 3 digits) followed by a mantissa field of a single sign digit followed by eight digits of mantissa.

The fixed point instructions operate on the twelve most significant digits of the accumulator. This format is similar to the single Precision format in the Floating Point, Fixed field length instructions (See Section 10.). The same accumulator is used for the Fixed Point and Floating Point instructions.

If the instruction produces a result greater than seven digits, an overflow occurs and the following characteristics apply.

- If the operation specifies a store of the result to memory (IAS, ISS, IMS, IMI), this store is not performed.
- 2. The sign and exponent field is set to +08.
- 3. Set the Overflow Flag and set the Comparison Flags to HIGH.
- 4. The final contents of the accumulator are unspecified.

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COMPANY CON	FIDENTIAL	SYSTEM	DESIGN	SPECI	FICATIO	DN REV.	A	PAGE 1	06
9	ARITHMETIC	; FIXED	POINT,	FIXED	FIELD	LENGTH	( C C	ontinued)	ŀ.

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A trap rault is a software enabled routine that allows the instruction in error to be examined.

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The Trap Fault will be enabled if the two digit key stored at memory address 64, relative to Base #0, is equal to "FF".

If Trap Fault is enabled and a fault occurs, a Hardware Call procedure will be executed with the address of the instruction at fault stored on the stack.

If Trap Fault is not enabled and a fault occurs, the next program instruction will be executed.

BURROUGHS CORPORATION System development group	 ++ 	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 107

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9.1 INTEGER LOAD (ILD)/OP=58

Format -----+

| OP | A |

0P = 58

A = Address of the source data field. Address may be indexed, indirect or extended. The final address controller data type will always be treated as SN.

Function

The integer load instruction loads the accumulator with an 8 digit data field at memory (A). The data field, consisting of a sign and seven digits, is loaded into the 20 digit accumulator as shown below, where "S" is the sign of the data field and "Dn" represents the numeric data. Undigits may be loaded into the mantissa field of the accumulator. The result of loading undigits into the sign digit is machine dependent. See Appendix A - Compatibility Notes (A.54).

i + 0 8 s i G D2 D3 D4 i D5 D6 D7 D8 i 0 0 0 0 i 0 0 0 0 i

Note that the exponent is set to +08 and that the most significent digit as well as the least significant eight digits of the mantissa are set to zero.

Comparison Flags

Set the Comparison Flags HIGH if the result is positive, EQUAL if the result equal to zero, and LOW if the result is negative.

Overflow

The Overflow flag is not affected by this instruction.

URRCUGHS CORPORATION YSTEM DEVELOPMENT GROUP ASADENA PLANT		+ 1997 5:     V SERIES INSTRUCTION SET		
		DESIGN SPECIFICATI		GE 108
9.1	INTEGER LOAD (ILD)	/OP=58 (Continued		
	Examples			
	EXAMPLE (1)	Load Accumulator i	ith Integer	
	0P	An and a second s		
	58 A F	IELD		
		BEFORE	AFTER	•
	A FIELD Accumul		·	5
	COMPARI Overflo		LOW unchanged	a Urtu Maria Aria
	EXAMPLE (2)	Load Accumulator	ith Undigits	
	0P			
	58 A F	 IELD		
		BEFORE	AFTER	
	A FIELD Accumul	DUF1B2E3		3
	COMPARI Overflo	Winn	LOW unchange	€d

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SYSTEM DE PASADENA	VELOPMENT GROUP V SERIES INSTRUCTION SET
COMPANY C	ONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 109
9_2	INTEGER STORE (IST)/OP=59
	Fermat
	OP   A   ++
	OP = 59
	A = Address of the destination field. Address may be indexed, indirect or extended. The final address controller data type will always be treated as SN.
	Function
	The integer store instruction will store into an 8 digit field at memory location (A) the integer and its sign from the accumulator. Undigits may be stored from the mantissa field of the accumulator. The handling of the sign digit is machine dependent. See Appendix A – Compatibility Notes (A_54).
	The accumulator, which is in the form:
•	++   + 0 8 S   D1 D2 D3 D4   D5 D6 D7 D8   D9D10D11D12D13D14D15D16   ++
	is stored in the destination field as:
	++   S D2 D3 D4   D5 D6 D7 D8   ++
	Where "S" indicates the operand sign and "Dn" represents the operand digits. Notice that D1 is dropped. Meaningful results are obtained only when D1 is equal to zero.
	Comparison Flags
	Set the Comparison Flags HIGH if the stored operand is positive, EQUAL if the stored operand is equal to zero, and LOW if the stored operand is negative.
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CMPANY CONFIDENTIAL	SYSTEM DESI	GN SPECIFICATION	REV. A PAGE 11	
9,2 INTEGER STO	DRE (IST)/OF	=59 (Continued)		
Overflow	an a			
The Overflo	ow Flag is r	not affected by t	his instruction.	
Examples	n e su préférie dyna T	an a		
	an Antonia antona antona di		1. 	
EXAMPL	.E (1) Stor	e Accumulator In	teger in Memory	
OP), blatet i se afas it ereit, je fas se it o 				
59	A FIELD		na	
		BEFORE	AFTER	
	FIELD	nnnnnnn +08-09876543 nnnnnnn	D9876543 unchanged	
	COMPARISON	nnn	LOW	
EXAMPL	.E (2) Stor	e Accumulator Im	age in Memory	
0P.	A			
59	A FIELD			
		BEFORE	AFTER	
an an an ann an an an an an an an A	A FIELD ACCUMULATOR	nnnnnnn +08-00f182E3 nnnnnn	DOF1B2E3 unchanged	
an an an an an an an an an Araba an	CMPARISON	NNN	LOW	

BURROUGHS CORPORATION System development group	 ++ 1997 5390 	
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYS	TEM DESIGN SPECIFICATION REV. A PAGE 111	

9.3

INTEGER ADD (IAD)/OP=50

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Fo	) <b>r m</b> a	it		
		-		
+-		+		
1	0P	1	A	
÷				_

0P = 50

A = Address of the Addend field. Address may be indexed, indirect or extended. The data type of the final address controller is ignored and will always be treated as SN.

Function

The integer add instruction adds the number stored in a memory location (A) to the value stored in the accumulator and stores the sum in the accumulator.

The signs of both the accumulator and the addend are considered in the addition and the mantissa sign field is set positive or negative based on the result.

Set the signed exponent field of the accumulator to +08 even in the case of overflow.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison and Overflow Flags

If the addition produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGN. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, the Comparison Flags will be set to EQUAL if the result is zero, HIGH if the result is positive and LOW if the result is negative.

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MPANY C	ONFIDENTIAL SYSTEM	DESIGN SPECIFICA	TION REV. A PA	AGE 1	
9.3	INTEGER ADD (IAD)	/OP=50 (Continue	d)		
	Overlap				
	There are no over	·lap restrictions	for this instructi	ion.	
	Examples				
1	EXAMPLE (1)	Add Integer to A	ccumulator		
	0 <b>P</b>				
•	50 A F	FIELD			
		BEFOR	E AFTER		
	A FIELD Accumul		67 +08+02345678		
	COMPARI Overflo		그 같은 것 같은		

	CORPORATION ++ 1997 5390 VELOPMENT GROUP   PLANT   V SERIES INSTRUCTION SET
COMPANY C	CNFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 113
9.4	INTEGER ADD AND STORE (IAS)/OP=51 Format
	++   OP   A   ++
	0P = 51
	A = Address of the Addend and Sum field. Address may be indexed, indirect or extended. The data type of the final address controller will always be treated as SN.
	Function
	The integer add and store instruction will add the number stored in a memory location (A) to the value stored in the accumulator and store the sum in the accumulator and in the same memory location (A). The store to memory does not take place on overflow.
	The signs of both the accumulator and the addend are considered in the addition and the mantissa sign field is set positive or negative based on the result.
	Set the signed exponent field of the accumulator to +08 even in the case of overflow.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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SYSTEM DEVELOPMENT GROUP PASADENA PLANT		V SERIES INSTRU	UCTION SET
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9.4	INTEGER ADD AND ST	ORE (IAS)/OP=51 (	Continued)
	Comparison and Ove	rflow Flags	
set the Overf HIGH. The Trap Call procedure of the accumul overflow condi EQUAL if the r		Flag and set to ult, if enabled, w to the fault routing or are unspecifie on, the Comparison	eater than 7 digits, he Comparison Flags to ill cause a Hardward e. The final content d. If there is no n Flags will be set to H if the result is gative.
		ap restrictions to	r this instruction.
	Examples		
	EXAMPLE (1)	Add Integer to Acc	umulator and Store
	0.P A		
	51 A FI	ELD	
		BEFORE	AFTER
	A FIELD Accumula	+1111111 TOR +08+01234567 nnnnnnn	C2345678 +08+02345678 00000000
	COMPARIS	ON ANN	HIGH

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SE	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	A PAGE 115

9.5

INTEGER SUBTRACT (ISU)/OP=52

Format

-----+ | OP | A | +----+

OP = 52

A = Address of the subtrahend field. Address may be indexed, indirect or extended. The data type of the final address controller will always be treated as SN.

Function

The integer subtract instruction will subtract the number stored in a memory location (A) from the value stored in the accumulator and store the difference in the accumulator.

The signs of both the accumulator and the subtrahend are considered in the subtraction and the mantissa sign field is set positive or negative based on the result.

The signed exponent field of the accumulator is set to +08 by this instruction even in the case of overflow.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison and Overflow Flags

If the subtraction produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGH. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, set the Comparison Flags to EQUAL if the result is zero, HIGH if the result is positive and LCW if the result is negative.

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OMPANY CO	NFIDENTIAL SYSTEM	DESIGN SPECIFICAT	ION REV. A PAG	E 116
9.5	INTEGER SUBTRACT	(ISU)/OP=52 (Cont	inued)	
	Overlap			
		<ul> <li>A second sec second second sec</li></ul>		
a second se	There are no over	lap restrictions f	or this instructio	<b>n.</b>
	Examples	ж •	• Constant of the second se	
• •				
	EXAMPLE (1)	Subtract Integer	from Accumulator	
	0P	an an an Anna a 📭 an an Anna an		
	 52 A FIE			
	JZ A FIE	LD An Anna Anna Anna Anna Anna Anna Anna		
		BEFORE	AFTER	
	A FIELD		unchanged	
	ACCUMUL	ATOR +08+02345678	+08+03345677	
	and a second	กกกกกกก	00000000	
	COMPARI		HIGH	
	OVERFLO	N DUU	unchanged	
	ang			
	and the second secon			

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COMPANY CONF		DESIGN SPECIFICATION REV.	A PAGE 117
9.6	INTEGER SUBTRACT A	ND STORE (ISS)/OP=53	
	Format		
	OP   A   ++		
	0P = 53	····	
	Address may		extended. The
:	Function		. ·
	stored in a memor the accumulator a accumulator and	ct instruction will subtrac ry location (A) from the va and store the differen in the same memory locat es not take place on overfl	lue stored in ce in the ion (A). The
	considered in the	the accumulator and the su subtraction and the mantis negative based on the resu	sa sign field
	Set the signed expo even in the case of	onent field of the accumul f overflow.	ator to +08
	sign digit, cause	a contains undigits other e an Invalid Arithmetic Da tibility Notes (A.16).	

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 118 --------

9.6 INTEGER SUBTRACT AND STORE (ISS)/OP=53 (Continued)

> Comparison and Overflow Flags

If the subtraction produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGH. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, set the Comparison Flags to EQUAL if the result is zero, HIGH if the result is positive and LOW if the result is negative.

Overlap -----

There are no overlap restrictions for this instruction.

Examples

EXAMPLE (1) Subtract Integer from Accumulator and Store

0P A ------53 A FIELD

	BEFORE	AFTER
A FIELD	D0999999	C 3345677
ACCUMULATOR	+08+02345678	+08+03345677
	որողորո	0000000
COMPARISON	nn n	HIGH
OVERFLOW	nnn .	unchanged

BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 119

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9_7 INTEGER MULTIPLY (IMU)/54

Format

+----+ | OP | A |

0P = 54

A = Address of the multiplier field. Address may be indexed, indirect or extended. The data type of the final address controller will always be treated as SN.

Function

The integer multiply instruction causes the value stored in the accumulator to be multiplied by the number stored in a memory location (A) and the product to be stored in the accumulator.

The signs of both the accumulator and the multiplicand are considered in the multiplication and the mantissa sign field is set positive or negative based on the result.

Set the signed exponent field of the accumulator to +08 even in the case of overflow.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Note, Section A.16.

Comparison and Overflow Flags

If the multiplication produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGH. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, set the Comparison Flags to EQUAL if the result is zero, HIGH if the result is positive and LOW if the result is negative.

OMPANY COL	NFIDENTIAL SYSTE	 + M DESIGN SPE	CIFICATION	REV. A	PAGE 120
9.7	INTEGER MULTIPLY	(IMU)/54 (	Continued)		
	Overlap				
	There are no ove	rlap restric	tions for th	is instru	iction.
	Examples				
	EXAMPLE (1)	Multiply A	ccumulator b	y Integer	• • •
	0 <b>P</b>		andar a san ang san an San ang san ang San ang san ang	an an taon 1990 - Angeland Angeland 1990 - Angeland Angeland	
	54 A FI	ELD			•
			BEFORE	AF	TER
	A FIEL Accumu		0000003 01234567 nnnnnnn	+08+037	anged 103701 100000
	COMPAR Overfl		<b>NNN</b> NNN		IIGH langed

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	S CORPORATION Development group A plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY	CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 121
9 - 8	INTEGER MULTIPLY	AND STORE (IMS)/OP=55	
	Format		

t	-	-	-	-+	******	+
I		0	P		A	L
	-	_	_	-*		1

0P = 55

A = Address of the multiplier and the product field. Address may be indexed, indirect or extended. The data type of the final address controller will always be treated as SN.

Function

The integer multiply and store instruction causes the value stored in the accumulator to be multiplied by the number stored in a memory location (A), the product to be stored in the accumulator and in the same the memory location (A). The store to memory does not take place on overflow.

The signs of both the accumulator and the multiplicand are considered in the multiplication and the mantissa sign field is set positive or negative based on the result.

The signed exponent field of the accumulator is set to +08 by this instruction even in the case of overflow.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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	 +		
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV.	. A:	PAGE 122

9.8 INTEGER MULTIPLY AND STORE (IMS)/0P=55 (Continued)

Comparison and Overflow Flags

If the multiplication produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGH. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, set the Comparison Flags to EQUAL if the result is zero, HIGH if the result is positive and LOW if the result is negative.

Overlap

There are no overlap restrictions for this instruction,

Examples

EXAMPLE (1) Multiply Accumulator by Integer and Store

OP		A
55	A	FIELD

OVERFLOW

	BEFORE	AFTER
A FIELD	+0000003	c3703701
	+08+01234567	+08+03703701 00000000
COMPARISON	nn	HIGH
CUMPARISUN	11111	птен

nnn

unchanged



9.9

INTEGER MEMORY INCREMENT (IMI)/OP=57

Format -----+ | OP | A |

OP = 57

A = Address of the increment field. Address may be indexed, indirect or extended. The final address controller if equal to one (SN) indicates a decrement operation and if equal to zero (UN) indicates an increment operation. Other controller values are reserved.

Function

The integer memory increment instruction, depending on the value of the address controller, increments or decrements a number at a memory location (A) and stores that value in the accumulator and at the same memory location (A).

The signed exponent field of the accumulator is always set to +08 by this instruction.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

Comparison and Overflow Flags

If the increment/decrement produces a result greater than 7 digits, set the Overflow Flag and set the Comparison Flags to HIGH. A Trap Fault, if enabled, will cause a Hardware Call procedure to the fault routine. The final contents of the accumulator are unspecified. If there is no overflow condition, set the Comparison Flags to EQUAL if the result is zero, HIGH if the result is positive and LOW if the result is negative.

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9-9	INTEGER MEMORY I	NCREMENT (I	MI)/OP=57	Continued	)
	Overlap				
	There are no ove	rlap restric		this instr	uction_
	Examples	in an an ann an Anna an			
	EXAMPLE (1)	Memory Ind	crement		
	<u></u>	y a transformation of the second s Second second		n de la companya de l Porte de la companya d	
	57 A FI	ELD (UN)	and the second		
			n an tha she dha ta she Citir a sa sa sa		
an a	an an an Araban ann an Araban a Araban an Araban an A Araban an Araban an A		BEFORE	AF	TER
	A FIEL		+1234567	C123	
e e e e e e e e e e e e e e e e e e e		LATOR nnni	nnnnnnnn	+08+0123 0000	
					Maria di Kasaran da Kas
	COMPAR	ISON	nnn		HIGH
· .	OVERFL	OW	กกก	unc	hanged
		andar Aliante de la composición de la composi Aliante de la composición de la composic	en Alexandre de la companya de la comp Alexandre de la companya de la compa		
•	EXAMPLE (2)	Memory Dec	crement		•
	0.P	A	and and an and a second se	•	
	 57 A FI	ELD (SN)		•	
			BEFORE	A:F	TER
	and a second second Second second second Second second	ling and the set of the set of the set of the set of the set set of the set			
	A FIEL Accumu		+1234567	c123 +08+0123	
1. 1. 1. 1. 1. <del>1.</del> 1.			กกกกกกก	0000	
	COMPAR	ISON	nnn	H	IGH
	OVERFL		nnn		anged

BURRCUGHS CORPORATION System development group	 ++ 1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A PAGE 125

ARITHMETIC; FLOATING POINT, FIXED FIELD LENGTH

Fixed field length arithmetic instructions use a 20-digit accumulator which holds the instruction result within the processor as an operand for the next operation. Every instruction has an implied reference to the accumulator.

The floating point (real) format consists of a signed exponent field followed by a signed mantissa field. The representation of a floating point field is:

S/X, EXP, S/M, MANTISSA

10

Where: S/X is the sign of the exponent (1 digit) EXP is the exponent (2 digits) S/M is the sign of the mantissa (1 digit) Mantissa is the mantissa data (8 or 16 digits)

Example: +01-87654321

The mantissa is a numeric field of two possible lengths; eight digit-Single Precision or sixteen digit-Double Precision. The mantissa is assumed to always have the decimal point to the left of the most significant digit.

The same accumulator is used for Fixed Point and Floating Point instructions.

If all sixteen digits of the accumulator mantissa are equal to zero, the exponent and mantissa sign will be set to -99+.

The Overflow Flag is set and the Comparison Flags are set to HIGH on overflow, to LOW on underflow and to EQUAL on a divide by zero.

OMPANY CO	NFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 120
10	ARITHMETIC FLOATING POINT, FIXED FIELD LENGTH (Continued)
	A Trap Fault is a software enabled routine that allows the instruction in error to be examined.
	The Trap Fault will be enabled if the two digit key stored at memory address 64, relative to Base #0, is equal to "FF".
	If Trap Fault is enabled and a fault occurs, a Hardward Call procedure will be executed with the address of the instruction at fault stored on the stack.
	If Trap Fault is not enabled and a fault occurs, the nex program instruction will be executed.
	A Trap Fault is caused when:
· · · ·	<ol> <li>The resultant normalized mantissa is non-zero and the exponent is greater than +99 (overflow).</li> </ol>
	<ol> <li>The resultant normalized mantissa is non-zero and the exponent is algebraically less than -99 (underflow).</li> </ol>
	3. The most significant digit of the mantissa of the divisor is equal to zero (divide by zero).
	The result is not stored in memory. Division by zero doe not change the contents of the accumulator. For all othe instructions, the final contents of the accumulator will be unspecified.

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BURROUGHS CORPORATION System development group Pasadena plant	I I I V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 127

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10_1 REAL LOAD (RLD)/OP=78

OP = 78

A = Address of the source data field operand. Address may be indexed, indirect or extended. When the final address controller is equal to "0" or "2", the data field will be Single Precision. When the final address controller is equal to "1", the data field will be Double Precision.

Function

The real load instruction loads the accumulator with a floating point data field located in memory (A). The source data field is assumed to be in the form shown below:

SINGLE PRECISION

Sx Ex Sm D1 D2 D3 D4 D5 D6 D7 D8

DOUBLE PRECISION

Sx Ex Sm D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16

Sx is the sign of the exponent (1 digit). Ex is the exponent (2 digits). Sm is the sign of the mantissa (1 digit). D1-D8 is the single precision mantissa (8 digits) D1-D16 is the double precision mantissa (16 digits).

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTE	EM DESIGN SPECIFICATION REV. A	PAGE 128

10_1 REAL LOAD (RLD)/OP=78 (Continued)

When the operation is single precision, only the eight most significant digits of the mantissa are loaded into the accumulator; the least significant eight digits are set to zero. When the operation is double precision all sixteen digits of the mantissa are loaded into the accumulator. The exponent and both signs will be loaded in the form that they appear in memory. Undigits may be loaded into the exponent and the mantissa fields of the accumulator. The result of loading undigits into the sign digit is machine dependent. See Appendix A - Compatibility Notes (A.54). 

> Comparison Flags

> > and and a second se

Set the Comparison Flags to HIGH if the result is positive, EQUAL if the result is zero and LOW if the result is negative.

EXAMPLE (1) Load Accumulator with Floating Point Number

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0 P A -78 A FIELD (UN)

ارد. موجود هم مشاهیهای در این در از این از موجود میچود . موجود این ا

BEFORE

AFTER

A FIELD +07012345678 ACCUMULATOR nnnnnnnnnn DNNNNN LOW

unchanged 407-12345678 00000000

BURROUGHS CORPORATION System development group	++	1,997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 129

10_2 REAL STORE (RST)/OP=79

Format

+----+ | OP | A |

0P = 79

A = Address of the destination field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

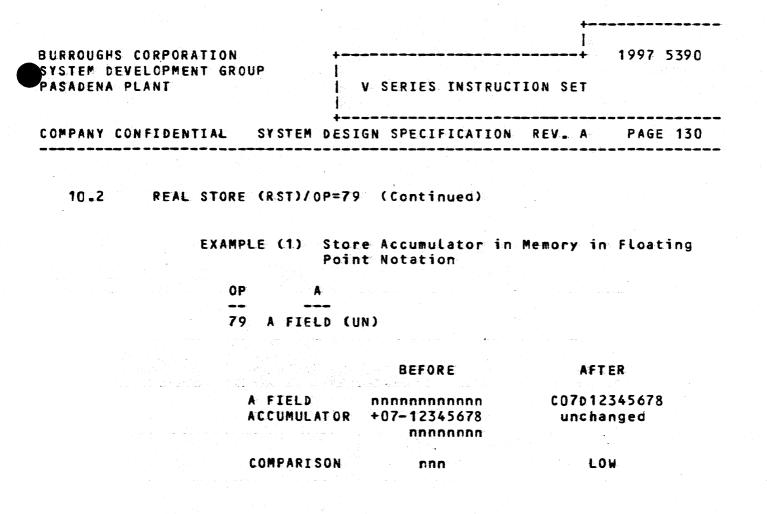
Function

The real store instruction will store in a memory location (A) the contents of the accumulator, including the exponent, its sign and the sign of the mantissa. Undigits may be stored from the exponent and mantissa fields of the accumulator. The handling of the sign digit is machine dependent. See Appendix A - Compatibility Notes (A.54).

If the operation is single precision, the least significant eight digits of the accumulator are ignored.

Comparison Flags

Set the Comparison Flags to HIGH if the result is positive, EQUAL if the result is zero and LOW if the result is negative.





10.3 REAL ADD (RAA)/OP=70

Format		
++-		+
OP	A	1
++-		+

- OP = 70
- A = Address of the Addend field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Dcuble Precision.

Function

The real add instruction adds the floating point number stored in a memory location (A) to the value stored in the accumulator and stores the sum in the accumulator.

The initial and final value of the accumulator and memory will have the same precision.

Different machines may maintain differing number of significant digits while performing the computation, thereby producing slightly different results. See Appendix A - Compatibility Notes (A.18).

Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). The result of the operation will always be normalized.

If the operand data contains undigits other than in the sign digits, cause an Invalid Arithmetic Data. See Appendix A - Compatibility Notes (A.16).

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10.3	REAL ADD (RAA)/OP=70	(Continued)	
	Comparison Flags	and a second	
	Set the Comparison positive, EQUAL if result is negative.	Flags to HIGH the result is	if the result is zero and LOW if the
. 1948 -	Examples	n an an Araban an Ar Araban an Araban an Ar	n an
	EXAMPLE (1) Add	Floating number	to Accumulator
	OP A		
1. 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 19 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1994 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -	70 A FIELD (U	N Data and a second	
an din i		BEFORE	AFTER
	A FIELD Accumulator	+05+22222222 +05+12345678 nnnnnnn	unchanged +05+34567900 0000000
	COMPARISON Overflow	nnn nnn	HIGH unchanged

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 133	BURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
	COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 133

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10.4 REAL ADD AND STORE (RAS)/OP=71

Format

-----+ | OP | A |

- 0P = 71
  - A = Address of the Addend and Sum field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real add and store instruction will add the floating point number stored in a memory location (A) to the value stored in the accumulator and store the sum in the accumulator and in the same memory location (A). The store to memory will not take place on an error condition.

The initial and final value of the accumulator and memory will have the same precision.

Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). The result of the operation will always be normalized.

If the operand data contains undigits other than in the sign digits, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

SYSTEM DEVELOPMENT GROUP 1	BURROUGHS (	ORFORATION	******		19	97 5390
10.4 REAL ADD AND STORE (RAS)/OF=71 (Continued) Comparison Flags Set the Comparison Flags to HIGH if the result i positive, EQUAL if the result is zero and LOW if th result is negative. Examples . EXAMPLE (1) Add Floating Number to Accumulator and Store OP A 71 A FIELD (UN) BEFORE AFTER A FIELD +05+2222222 C05C34567900 ACCUMULATOR +05+12345678 +05+34567900 NORMANNNN 00000000 COMPARISON nnn HIGH OVERFLOW nnn unchanged	EURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT		V SER	IES INSTRUC		
Comparison Flags Set the Comparison Flags to HIGH if the result i positive, EQUAL if the result is zero and LOW if th result is negative. Examples EXAMPLE (1) Add Floating Number to Accumulator and Store OP A 71 A FIELD (UN) BEFORE AFTER A FIELD +05+22222222 C05C34567900 ACCUMULATOR +05+12345678 +05+34567900 nnnnnnn 00000000 COMPARISON nnn HIGH OVERFLOW nnn unchanged	COMPANY CON	FIDENTIAL SYSTEM	DESIGN SP	ECIFICATION	I REV. A P	AGE 134
Comparison Flags Set the Comparison Flags to HIGH if the result i positive, EQUAL if the result is zero and LOW if th result is negative. Examples EXAMPLE (1) Add Floating Number to Accumulator and Store OP A 71 A FIELD (UN) BEFORE AFTER A FIELD +05+2222222 C05C34567900 ACCUMULATOR +05+12345678 +05+34567900 nnnnnnn 00000000 COMPARISON nnn HIGH OVERFLOW nnn Unchanged						
Set the Comparison FLags to HIGH if the result i positive, EQUAL if the result is zero and LOW if th result is negative. Examples 	10.4	REAL ADD AND STOR	E (RAS)/OF	=71 (Conti	inued)	
positive, EQUAL if the result is zero and LOW if th result is negative. Examples 		Comparison Flags				
EXAMPLE (1) Add Floating Number to Accumulator and Store OP A 71 A FIELD (UN) BEFORE AFTER A FIELD +05+2222222 C05C34567900 ACCUMULATOR +05+12345678 +05+34567900 0000000 COMPARISON nnn HIGH Unchanged		positive, EQUAL	if the			
Store OP A 71 A FIELD (UN) BEFORE AFTER A FIELD +05+22222222 C05C34567900 ACCUMULATOR +05+12345678 +05+34567900 00000000 COMPARISON nnn HIGH OVERFLOW nnn Unchanged		Examples		and a start of the second s Second second s		
BEFOREAFTERA FIELD ACCUMULATOR+05+22222222 +05+12345678 nnnnnnnCOSC34567900 +05+34567900 00000000COMPARISON OVERFLOWnnnHIGH unchanged			Store	ing Number	to Accumulato	r and
A FIELD ACCUMULATOR COMPARISON OVERFLOW ACCUMULATOR +05+2222222 +05+34567900 0000000 0000000 HIGH unchanged	· ·	71 A FIE	LD (UN)			
ACCUMULATOR +05+12345678 +05+34567900 nnnnnnn 00000000 COMPARISON nnn HIGH OVERFLOW nnn unchanged	•			BEFORE	AFTER	
OVERFLOW nan unchanged				12345678	+05+3456790	0

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 135

10_5 REAL SUBTRACT (RSU)/OP=72

Format -----+ ! OP | A | +----+

0P = 72

3

A = Address of the subtrahend field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real subtract instruction will subtract the floating point number stored in a memory location (A) from the value stored in the accumulator and store the difference in the accumulator.

The initial and final value of the accumulator and memory will have the same precision.

Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). The result of the operation will always be normalized.

If the operand data contains undigits other than in the sign digits, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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10.5	REAL SUBTRA	CT (RSU)/OF	=72 (Continued)		
	Comparison				
		1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -			
	Set the C positive, result is r	EQUAL if	Flags to HIGH the result is	if the resu zero and LOW	lt is if the
	Examples		andra Article (1990) Article (1990) Article (1990)		
			andre en service de la companya de Esta de la companya d Esta de la companya d	• • • • • • • • • • • • • • • • • • • •	
	EXAMPL		ract Floating Num mulator	ber from the	
	0P	n ger he <b>A</b> aroo aa			
	 72	A FIELD (L			
	na an a				
			BEFORE	AFTER	
			+05+11111111 +05+12345678 nnnnnnn	unchanged +04+12345670 00000000	
		COMPARISON DVERFLOW	nnn nnn	HIGH unchanged	
	<ol> <li>A set of the set of</li></ol>				
		an a	na an ann an Aonaichtean ann an Aon Ann an Aonaichtean ann an Aonaichtean		

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 137

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10.6 REAL SUBTRACT AND STORE (RSS)/OP=73

Format

ŧ		-+-		+
l	OP		A	. 1.
*				

OP = 73

A = Address of the subtrahend and difference field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real subtract and store instruction will subtract the floating point number stored in a memory location (A) from the value stored in the accumulator and store the difference in the accumulator and in the same memory location (A). The store to memory will not take place on an error condition.

The initial and final value of the accumulator and memory will have the same precision.

Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). The result of the operation will always be normalized.

If the operand data contains undigits other than in the sign digits, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

BURRCUGHS CORPORATION System development grou Pasadena plant	+- IP	V SERIES	INSTRUCT	+   ION SET	1997 5390
COMPANY CONFIDENTIAL	SYSTEM DES	IGN SPECIF	ICATION	REV. A	PAGE 138

REAL SUBTRACT AND STORE (RSS)/OP=73 (Continued) 10.6

> Comparison Flags

Set the Comparison Flags to HIGH if the result is positive, EQUAL if the result is zero and LOW if the result is negative.

Examples -----

•

ر د چېده

EXAMPLE (1) Subtract Floating Number from the Accumulator and Store

73	A FIELD	(UN)
OP	A	

BEFORE

AFTER

ι.

 المستعدة فالمعرب ومقرا المتحاد المتحاد والمتحاد والمتحاد والمتحاد والمتحاد والمتحاد والمتحاد والمتحا	والمحاجب والمراجع والمرجع والمعجود	the second second second second
A FIELD +05	+1111111	CO4C12345670
ACCUMULATOR +05	+12345678	+04+12345670
a de la companya de Esta de la companya d Esta de la companya d	กกกกกกก	00000000

COMPARISON	nnn	HIGH
OVERFLOW	nnn	unchanged

	1	
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	+	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 139

10.7 REAL MULTIPLY (RMU)/OP=74

Format		
	<b>■</b> .	
•		
+		+
OP	A	1
+		+

- 0P = 7.4
  - A = Address of the multiplier field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real multiply instruction multiplies the value stored in the accumulator by the floating point number stored in a memory location (A) and stores the product in the accumulator.

The initial and final value of the accumulator will be 16 digits regardless of whether the input was single or double precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). If the input operands are normalized, the result will be normalized, and if they are not normalized, they may not produce a normalized result.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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•					
10.7	REAL MULTI	PLY (RMU)/0	P=74 (Continue	d )	
	Comparison	Flags			
	Set the positive, result is	EQUAL if	Flags to HIG the result i	H if the s zero and	result is LOW if the
	Examples			andar and an	
	EXAMP	LE (1) Mul Num	tiply Accumulat	or by Floati	ng Point
an a	n a ser and by the second s				
	0P 		ter en service de la service de la service Norma de la service de la s ➡Ter en service de la servi		
		A FIEL	D (UN)	•••	•
			BEFORE	AFT	ER
		A FIELD Accumulator	+05+30000000 +05+12345678 nnnnnn	+09+3703	7034
		COMPARISON Overflow	nnn nnn	HI uncha	



10.8 REAL MULTIPLY AND STORE (RMS)/OP=75

Format -----+ | OP | A | +----+

OP = 75

A = Address of the multiplier and product field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real multiply and store instruction multiplies the value stored in the accumulator by the number stored in a memory location (A) and stores the product in the accumulator and in the same memory location (A). The store to memory will not take place on an error condition.

The initial and final value of the accumulator will be 16 digits regardless of whether the input was single or double precision.

The operands need not be normalized, but incompatible results may be produced. See Appendix A - Compatibility Notes (A.17). If the input operands are normalized, the result will be normalized, and if they are not normalized, they may not produce a normalized result.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

	CORPORATION ELOPMENT GROUP LANT	V SER	IES INSTRUCT		1997 5390
OMPANY CO	NFIDENTIAL SYSTEM	DESIGN SP	ECIFICATION	REV. A	PAGE 14
10.8	REAL MULTIPLY AND	STORE (RM	S)/OP=75 ((	Continued	
	Comparison Flags				
	Set the Compar positive, EQUAL result is negativ	if the			
	Examples				· . · · ·
	EXAMPLE (1) OP	Multiply and Store A 	Accumulator	by Float	ing Number
	75 A	FIELD (UN)			
			BEFORE	. A F	TER
	A FIEL Accumui	+05 ATOR +05	+30000000 +12345678 	+09+37	037034 037034 000000
	COMPAR Overfl		nnn nnn		IGH anged
			an a		



10.9 REAL DIVIDE (RDV)/OP=76

- 0P = 76
  - A = Address of the divisor field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "2" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real divide instruction divides the value stored in the accumulator by the floating point number stored in a memory location (A) and stores the quotient in the accumulator.

The initial and final value of the accumulator and memory will have the same precision.

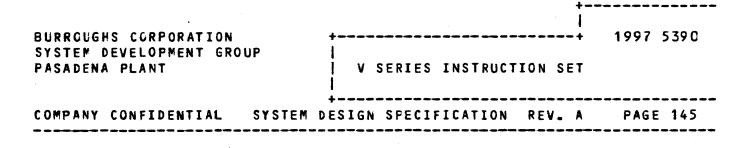
Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands must be normalized.

Operands that are not normalized will be treated as being equal to zero.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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	LON SET	V SERIES INSTRU		ENA PLANT	ASADENA
GE 14	REV. A PAGE	GN SPECIFICATIO	SYSTEM DESI	NY CONFIDENTIAL	OMPANY
		6 (Continued)	DE (RDV)/OP=7	.9 REAL DIVI	10.9
			on Flacs	Compariso	
•		nter en la companya de la companya d La companya de la comp			
et the arison	that will termin Flag, and set et the Compari itive, EQUAL if negative.	the Overflow UAL. Otherwise,	ruction, set on Flags to EG HIGH if 1	the inst Compariso Flags to	
nt	Floating Point	de Accumulator	IPLE (1) Div Numb	EXAM	
	and a second second Second second		)P	an a	
		(UN)	6 A FIELD	- 7	
		na an an Arabana Agus an Arabana an Arabana Arabana an Arabana	han an an ann an Arland an Arland an Arland An <mark>Canadar an Arland an Arland Arland an Arland an A</mark>		
	AFTER	BEFORE			
	unchanged +00+61728390 00000000	+05+20000000 +05+12345678 			
	HIGH	nnn	COMPARISON		
	unchanged	nnn,	OVERFLOW	ا میں ایک	
				a a construction of the second s	.'
	аланан алан алан алан алан алан алан ал	en de la companya de La companya de la comp	n a star anna an anna anna	an a	



1C.10 REAL DIVIDE AND STORE (RDS)/OP=77

- 0P = 77
  - A = Address of the divisor/quotient field operand. Address may be indexed, indirect or extended. A final address controller value of "0" or "1" indicates Single Precision. A final address controller value of "1" indicates Double Precision.

Function

The real divide and store instruction divides the value stored in the accumulator by the floating point number stored in a memory location (A) and stores the quotient in the accumulator and in the same memory location (A). The store to memory will not take place on an error condition.

The initial and final value of the accumulator and memory will have the same precision.

Set the least significant eight digits of the accumulator to zero when the operation is single precision.

The operands must be normalized.

Operands that are not normalized will be treated as being equal to zero.

If the operand data contains undigits other than in the sign digit, cause an Invalid Arithmetic Data fault. See Appendix A - Compatibility Notes (A.16).

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BURROUGHS CORPORATION	++	1997 5390
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 146

1C.10 REAL DIVIDE AND STORE (RDS)/OP=77 (Continued)

Comparison Flags

Division by zero is an error condition that will terminate the instruction, set the Overflow Flag, and set the Comparison Flags to EQUAL. Otherwise, set the Comparison Flags to HIGH if the result is positive, EQUAL if the result is zero and LOW if the result is negative.

EXAMPLE (1) Divide Accumulator by Floating Point Number and Store

77	A	FIELD	(UN)
0 P	. •	, A.	

BEFORE

AFTER

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an in the second se	가슴 물건 가는 것 같아. 이 것 같아. 말 같아. 가지 않는 것 같아.	and the second
A FIELD	+05+20000000	COOC61728390
ACCUMULATOR	+05+12345678	+00+61728390
and a strategy of the	nnnnnn	00000000

COMPARISON	nnn	HIGH
OVERFLOW	nnn	unchanged



10.11 ACCUMULATOR MANIPULATE (ACM)/OP=84

Format

0P = 84

AF = Operation variants.

Function

The accumulator manipulate instruction modifies the contents of the accumulator as specified by the AF variants.

All variants of this instruction reference the entire accumulator without regard to data type or precision.

AF = 0x, Normalize Accumulator (x = unused)

If the most significant digit of the mantissa is zero, the entire mantissa will be shifted left and the exponent will be decremented by one. Continue shifting until the leading digit is non-zero, set the Comparison Flags according to the mantissa sign. If all sixteen digits are zero, set the exponent and mantissa signs to -99+ and set the Comparison Flags to EQUAL. If there are no leading zeros, set the Comparison Flags according to the mantissa sign. If the resulting exponent is smaller than -99, set the Overflow Flag and set the Comparison Flags to LOW (underflow). If an underflow is produced and Trap is enabled, a Trap Fault will occur.

AF = 1x, Convert Floating Point to Fixed Point (x = unused)

The accumulator mantissa is assumed to be normalized.

BURROUGHS CORPORATION	++	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYS	TEM DESIGN SPECIFICATION REV. A	PAGE 148

## 1C_11 ACCUMULATOR MANIPULATE (ACM)/OP=84 (Continued)

The data in the accumulator is converted from floating point to fixed point format. The mantissa is shifted right and the exponent is incremented until equal to +08. Set the Comparison Flags according to the mantissa sign. If the original exponent is equal to or greater than +08, an overflow is produced. The conversion does not take place if it would cause an overflow. If the eight most significant digits are now equal to zero, set the exponent and signs to -99+, set the eight least significant digits to zero, set the Comparison Flags to EQUAL. If an overflow is produced and Trap is enabled, a Trap Fault will occur.

-----------

 $AF = 2x_p$  Set the Mantissa Sign to Plus (+) (x = unused)

Set the mantissa sign to plus. If the mantissa is 0, set the Comparison Flags to EQUAL. If the mantissa is non-zero, set the Comparison Flags to HIGH.

 $AF = 3x_p$  Set the Mantissa Sign to Minus (-) (x = unused)

If the mantissa is non-zero, set the mantissa sign to minus and set the Comparison Flags to LOW. If the mantissa is zero, set the mantissa sign to plus and set the Comparison Flags to EQUAL.

AF = 4x, Complement the Mantissa Sign (x = unused)

If the mantissa is non-zero, complement the mantissa sign. Set the Comparison Flags to HIGH if the sign is set plus and LOW if the sign is set minus. If the mantissa is zero, set the mantissa sign to plus and set the Comparison Flags to EQUAL.

 $AF = 5x_p$  Zero the Accumulator (Set to -99+0) (x = unused)

Set the 16 digit accumulator mantissa to zero. Set the signed exponent field to -99 and set the mantissa sign to plus. Set the Comparison Flags to EQUAL.

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 149

# 10.11 ACCUMULATOR MANIPULATE (ACM)/OP=84 (Continued)

 $AF = 6n_p$  Increment the Exponent by n (n = 0-9)

Increment the exponent by n. Set the Comparison Flags to HIGH if the mantissa sign is plus, LOW if minus and EQUAL if the mantissa is zero. Attempts to increment the exponent beyond +99 will cause an overflow. A Trap Fault will occur if Trap is enabled.

-----------

 $AF = 7n_{p}$  Decrement the Exponent by n (n = 0-9)

Decrement the exponent by n. Set the Comparison Flags to HIGH if the mantissa sign is plus, LOW if minus, and EQUAL if the mantissa is zero. Attempts to decrement the exponent beyond -99 will cause an underflow. A Trap Event will occur if Trap is enabled.

All other variants are reserved and will cause an Invalid Instruction fault (IEX = 25) and terminate the instruction with no change to the accumulator.

Examples

EXAMPLE (1) Normalize Accumulator

۰,	AF	
	00	
	••	

	BEFORE	AFTER
ACCUMULATOR	+05+00123456	+03+12345678
	78901234	90123400
COMPARISON	nnn	HIGH

			+
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YSTEM DEVELOPM Asadena plant	ENT GROUP	V SERIES INSTRUCT	
MPANY CONFIDE	NTIAL SYSTEM DESI	GN SPECIFICATION	REV. A PAGE 150
10.11 ACC	UMULATOR MANIPULATE	(ACM)/0P=84 (Co	ntinued)
	EXAMPLE (2) Conv Poin	ert Floating Poin t Number	t Number to Fixed
	OP AF		
	84 10		
		BEFORE	AFTER
	ACCUMULATOR	+06+12345678 90123456	+08+00123456 00000000
	COMPARISON	nnn	HIGH
	EXAMPLE (3) Set	Mantissa Sign to	Plus
	OP AF		
	84 20		
		BEFORE	AFTER
	ACCUMULATOR	-05-12345678 90123456	-05+12345678 90123456
	COMPARISON	nnn	HIGH
	EXAMPLE (4) Set	Mantissa Sign to	Minus
	OP AF		
	84 30		
		BEFORE	AFTER
	ACCUMULATOR	+05+12345678 90123456	+05-12345678 90123456
	COMPARISON	nnn	LOW
•			

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PANY CONFIDENTIA	L SYSTEM DESI	GN SPECIFICATION	REV. A PAGE 151
		(ACM)/OP=84 (Co Lement Mantissa (	
EA	1.	itement mantissa (	5 I Y II
	0P AF  84 40		
		BEFORE	AFTER
en de la companya de La companya de la comp	ACCUMULATOR	+05-12345678 90123456	+05+12345678 90123456
•	COMPARISON	nnn	HIGH
EX	AMPLE (6) Clea	r Accumulator	
	OP AF		
	84 50		
		BEFORE	AFTER
	ACCUMULATOR	กกกกกกกกกก	-99+00000000 00000000

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MPANY CO	NFIDENTIAL SYSTEM DESIG	N SPECIFICATION	REV. A PAGE 15
10.11	ACCUMULATOR MANIPULATE	(ACM)/0P=84 (Con	itinued)
	EXAMPLE (7) Incre	ment Exponent by	
	OP AF		
	84 64		
n an		BEFORE	AFTER
	ACCUMULATOR	+05-12345678 90123456	+09-12345678 90123456
and a set of the set of the			
			an an an State an St State an State an Stat
	EXAMPLE (8) Decre	ment exponent by	2
	O'P A F	ter i se la construir de la con En la construir de la construir La construir de la construir de	
	84 72		
		BEFORE	AFTER
	ACCUMULATOR	+09+12345678 90123456	+07+12345678 90123456
	COMPARISON	n na star star star star star star star sta	HIGH

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	A PAGE 153

- 11 ADDRESS BRANCHING
- 11_1 BRANCH/OP=2x

#### Format

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ŀ		+-		-+
ļ.	OP	1	A	
ŀ		+		-+

OP = 20, 21, 22, 23, 24, 25, 26, 27, 28, 2A, 2B

A = Branch Address. Address may be indexed, indirect or extended. When not extended the final address controller bits specify the most significant digit of the address. This permits branching to any address up to and including 299,998, relative to Base #1, without indexing or extension. When the address is indexed, the final Base Indicant should resolve to a value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments.

# Function

If the condition specified for the branch is true or if the branch is unconditional, the "A" address is selected as the next program instruction address. If the condition specified is not true or if the instruction is a "NO-OP", the next instruction is fetched with no significant action. The address field of a non-taken branch or a "NOP" must have the same attributes as any address, however, the address does not have to resolve into a valid address. For example, a six digit address may not contain undigit in the extended digit position as this an condition causes the processor to mistakingly treat this address as an eight digit address. An odd address only causes errors if the branch is taken. Undigits in address positions other than the address controller and extended digit may result in incompatible behavior (See Appendix A, Compatibility Notes, A.52). The Comparison and Overflow Flags define the branch conditions.

BURROUGHS CORPO		++ 1997 5390
SYSTEM DEVELOPM Pasadena plant		V SERIES INSTRUCTION SET
COMPANY CONFIDE	NTIAL SYSTEM C	DESIGN SPECIFICATION REV. A PAGE 154
11.1 BRA	NCH (Continued)	
Not	in inco	branch prediction op codes" may result ompatible behavior. See Appendix A, ility Notes (A.O6).
	= 20 (NOP) NO	OPERATION
	This inst	truction performs no significant action.
0P	= 21 (LSS) BR/	ANCH ON LESS THAN CONDITION
	, address	truction causes a branch to the "A if the Comparison Flags are set LO , COMH=O).
OP	= 22 (EQL) BR/	ANCH ON EQUAL CONDITION
	address	truction causes a branch to the "A' if the Comparison Flags are set EQUAN COMH=1).
OP	= 23 (LEQ) BR	ANCH ON LESS THAN OF EQUAL CONDITION
		truction causes a branch to the "A if the Comparison Flags are set LOW o OML=1)_
0 P	= 24 (GTR) BR	ANCH ON GREATER THAN CONDITION
	address	truction causes a branch to the "A if the Comparison Flags are set HIG COMH=1).
0 P	= 25 (NEQ) BR/	ANCH ON NOT EQUAL CONDITION
	address	truction causes a branch to the "A' if the Comparison Flags are not se cleared (COML=0 or COMH=0 ).
0 P	= 26 (GEQ) BR/	ANCH ON GREATER THAN OF EQUAL CONDITION
		truction causes a branch to the "A' if the Comparison Flags are set HIGH of OMH=1).

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BURROUGHS CORPORATION System development group		1997 5390
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PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 155

11.1 BRANCH (Continued)

OP = 27 (BUN) BRANCH UNCONDITIONAL

This instruction always causes a branch to the "A" address.

OP = 28 (OFL) BRANCH ON OVERFLOW CONDITION

This instruction causes a branch to the "A" address if the Overflow Flag is set and resets the Overflow Flag.

OP = 2A (NUL) BRANCH ON NULL CONDITION

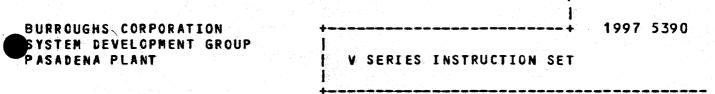
This instruction causes a branch to the "A" address if the Comparison Flags are reset (COML=0 and COMH=0).

**OP = 2B** (GTN) BRANCH ON GREATER OR NULL CONDITION

This instruction causes a branch to the "A" address if the Comparison Flags are reset or set HIGH (COML=0).

Comparison Flags

The Comparison Flags are not altered by these instructions.



COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 156 _____

12 HALTS

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Halt instructions are dependent upon an execution digit located in absolute memory location 48 which determines the course of action as follows:

#### . ACTION

VALUE

Re	served	د. در درمانههای از کامیتان امراک		N - F
Ha	lt is	ignored.		3
la de la companya de	lt is	executed if	not Privileged Mode.	2
	lt is	executed if	Privileged Mode.	14 .
Ha	lt is	executed.		0

If the halt is executed, the processor will enter a WAIT state that requires operator intervention to allow the processor to continue the execution of the instruction.

If the Halt is not executed, no significant action will be performed by the processor.

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 157

12.1 HALT BRANCH (HBR)/OP=29

OP = 29

A = Branch Address. Address may be indexed, indirect or extended. When not extended the final address controller bits specify the most significant digit of the address. This permits branching to any address up to and including 299,998, relative to Base #1, without indexing or extension. When the address is indexed, the final Base Indicant should resolve to a value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments.

Function

The Halt Branch instruction conditionally executes a halt according to the halt digit in absolute address 48. See Appendix A - Compatibility Notes (A.24).

If the halt is to take place, operator intervention is required to continue. Once continued, instruction execution resumes at the final "A" address.

If the halt is to be ignored, instruction execution continues at the final "A" address.

Comparison Flags

The Comparison Flags are not affected by this instruction.



12.2 HALT BREAKPOINT (HBK)/OP=48

Format

+----+ AF | BF |

OP = 48

- AF = Final AF value is ignored, but useful in identifying the specific HBK. May specify Indirect Field Length. However, the specification of an AF indirect field length may produce incompatible results. See Appendix A - Compatibility Notes (A.25).
- BF = Eight bit breakpoint control mask. The field will not be recognized as indirect.

Function

The Halt Breakpoint instruction performs a mask test against a halt character in memory location 46 relative to Base #0. If a bit is set in the halt character that corresponds to a bit set in the mask, the instruction executes a halt according to the halt digit in absolute memory address 48. See Appendix A - Compatibility Notes (A_24).

If there is no correspondence between the bits in the mask and the bits in the breakpoint bit pattern, the next instruction is selected in normal sequence with no other significant action.

Comparison Flags

The Comparison Flags are unchanged.

Overlap

There are no overlap restrictions for this instruction.

BURROUGHS CORPORATION System development group	++ 1	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 159

13 ENVIRONMENT CHANGE

13.1 BRANCH COMMUNICATE (BCT)/OP=30

Format

CP AFBF

OP = 30

AFBF = Function Address consisting of the low order four digits of an address that is relative to the specified Task's MCP Data Area. The high order digits are equal to zero. Indirect Field lengths may be specified.

Function

The Branch Communicate instruction is used to allow a user program to enter a function in the MCP environment. It stores processor state and registers in Hyper Call Stack Frame format on the stack of the called environment and passes control to the specified function.

Its function is similar to the function of the Hyper Call instruction except for the selection of the Function entry and the inability to directly pass parameters.

The following operations are performed by this instruction:

 The four digit Function Address (AFBF) is used as an offset relative to the task's MCP data area to select a Function entry.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT I V SERIES INSTRUCTION SET

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 160

13.1 BRANCH COMMUNICATE (BCT)/OP=30 (Continued)

Each Function entry contains the following information:

INFORMATION DIGITS

Environment Number	00-05
Next Instruction Address	06-11
Protection Field (DD)	12-13
Reserved	14-15
Interrupt Mask	16-17
Mode Indicators	18-19

Note - The lowest memory address = 00

If the Protection Field is not equal to "DD", cause an Invalid Instruction fault (IEX = 37) and terminate the instruction with no further action.

 Resolve the Environment Number, contained in the Function entry, to point to the selected Environment Table entry. However, retain the Active Environment Number so that it may be stored on the stack.

Resolve entry #0 of the Memory Area Table for the new environment from memory and maintain addressability along with Base #0 of the current environment. See Section 5.7 entitled "Resolving a Memory Area Table Entry".

BURROUGHS CORPORATION +-----+ 1997 5390 SYSTEM DEVELOPMENT GROUP | PASADENA PLANT | V SERIES INSTRUCTION SET

13_1

BRANCH COMMUNICATE (BCT)/OP=30 (Continued)

3. The top of stack pointer, located at address 40 (Relative to the new environment's Base #0), is used as the starting address, relative to the new environment's Base #0, to store the Hyper Call Stack frame.

The sum of the top of stack pointer and the size of the Hyper Call Stack Frame (96) and the size of the Hardware Call Stack Frame area (500) is compared to Limit #0. If the sum is equal to or greater than Limit #0, cause a Stack Overflow fault and terminate the instruction with no further action. Otherwise, store the Hyper Call Stack Frame in the following sequence.

#### INFORMATION DIGITS

_____

OLD TOS	==>	Accumulator	00-27
		Measurement Register	28-35
		Interrupt Mask	36-37
		Mobile Index Registers	38-69
		Mode Indicators	70-71
а -		COM & OVF Flags	72-73
		Active Environment Number	74-79
New IX3	==>	Next Instruction Address	80-85
		Saved IX3 Value	86-93
		Stack Frame Indicator (FE)	94-95
		Stack Parameters (O to 9999	bytes)
New TOS	==>		-

Note - The lowest memory address = 00

4. Store the new address of the next available stack location (Relative to the new environment's Base #0), into memory location 40 (Relative to the new environment's Base #0).

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OMPANY	CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 1	16
42 4	BRANCH COMMUNICATE (BCT)/OP=30 (Continued)	
1° J <b>B</b> AR	BRANCH COMMUNICATE COLITION - 50 CCONCINGED	
	5. Set the two most significant digits of IX3 to "(	
	and set the six least significant digits of IX3	
	the initial address specified in memory location	
	(Relative to the new environment*s Base #0) plus 80	Ja
	IX3 will now point to the Next Instruction Address	i
	the Hyper Call Stack Frame.	
	6. Set the machine "state" as follows:	
	INFORMATION SET TO	
	Next Instruction Address Function Table Active Environment Number Function Table	e.
	Active Environment Number Function Table	e
	Interrupt Mask Function Table	e
	Mode Indicators Function Table	e
	Measurement Register (user field) 000000	
	Comparison & Overflow Flags RESET	
	7 Cat the MODOV line to Respect while the Messagers	
	7. Set the MOPOK line to "zero" while the Measureme register is being changed and set it to a "one"	
	all other times.	a
	8. If Soft Fault is now enabled, examine the memo	o r
	location specified by the Reinstate List ent	
	pointer plus 8. If it is not equal to zero, execute	e
	Hardware Call procedure that will store the addre	es
	of the next instruction to be executed.	
	O load the Menory Area Table retained to by the table	<b>.</b>
	9. Load the Memory Area Table pointed to by the Acti Environment Number.	IV
	Ella II Climette Humber .	
	10. Using the new Base/Limit information, resolve 1	th
	next instruction address, relative to Base #1, a	
	execute an unconditional branch to that address.	
	The use of the Mobile Index Registers or the Accumulat	
	to pass parameters is invalid. The contents are r guaranteed.	10
	yuaranıczu.	

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 163

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13.2 ENTER (NTR)/0P=31

# Format

I OP | AFBF | A | PARAMETERS |

0P = 31

- AFBF = Length, in bytes, of the Parameter field. The maximum number of bytes moved is 9,999. A value of 0000 will move no data. AF or BF may specify indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21). See Appendix A - Compatibility Notes (A.19.1).
  - A = Branch Address. Address may be indexed, indirect or extended. When not extended the final address controller bits specify the most significant digit of the address. This permits branching to any address up to and including 299,998, relative to Base #1, without indexing or extension. When the address is indexed, the final Base Indicant should resolve to a value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments. When indexed by IX3, the initial contents of IX3 are used.

PARAMETERS = Data field to be stored in the stack.

Function

The Enter instruction stores control information and parameters into a stack located in memory and executes an unconditional branch to the instruction at the "A" address.

A six digit address containing the stack location, relative to Base #0, is specified in memory location 40 relative to Base #0.

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	V SERIES INSTRUCTION SET		
COMPANY CONFIDENTIAL SYSTEM DI	ESIGN SPECIFICATION REV. A PAGE 164		

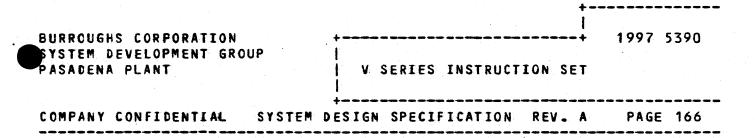
# 13.2 ENTER (NTR)/OP=31 (Continued)

The Enter Stack Frame is stored in the following sequence.

	INFORMATION		DIGITS
OLC TOS ==>	Next Instruction A Saved IX3 Value Reserved COM & OVF Flags	lddress	00-05 06-13 14 15
	Stack Parameters (	0 to 9999 by	
New TOS ==>			
Note - L	owest memory addres	s = 00	
"COM & OVF FLags	" contain the follo	wing inform	ation:
INFORMAT	EON	BIT	
Reserved		32	
Overflow Comparis	Flag on Low Flag	2 1	
	on High Flag	Ô	
Parameters =	AFBF bytes of data address field in t		
the contents o	significant digits f IX3 to the initi 40 relative to Base	al address	"CO". Set specified in
	lue of the next ava se #0, into memory		
digits, cause	o be stored into lo an Invalid Instru Compatibility Note	iction fault	
	and a second second Second second second Second second second Second second second Second second second Second second second Second second second Second second second Second second second Second second		

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BURRCUGHS CORPORATION 1997 5390 SYSTEM DEVELOPMENT GROUP **V** SERIES INSTRUCTION SET PASADENA PLANT SYSTEM DESIGN SPECIFICATION REV. A COMPANY CONFIDENTIAL PAGE 165 ______ 13.2 ENTER (NTR)/OP=31 (Continued) Comparison Flags Reset the Comparison and Overflow Flags. Overlap Undefined results will be produced if the stack area overlaps with the instruction or it's parameters. Examples -----EXAMPLE (1) Enter ADDRESS OP AFBF A PARAMETERS ---------------31 0003 020166 003016 203010 3 BEFORE AFTER NI 003016 020166 IX3 +0000010C0001024 0000040 001024 001046 Top of Stack 0001024 003034 Address Pointer 00000 After Parameters +0000010 IX3 Value O Zero Digit 5 COM & OVF Flags 203010 Parameters COMPARISON HIGH CLEAR **CVERFLOW** ON OFF



13.3 EXIT (EXT)/0P=32

0P = 32

A = Return Address. Address may be indexed, indirect or extended. When not extended the final address controller bits specify the most significant digit of the address. This permits branching to any address up to and including 299,998, relative to Base #1, without indexing or extension. When the address is indexed, the final Base Indicant should resolve to a value of "1". The processor will always treat the resolved address as being relative to Base #1. The processor will not check for improper memory assignments. The normal return address is obtained by setting the "A" address to zero, indexing by IX3 and setting the address is indexed by IX3, the initial contents of IX3 are used.

Function

The Exit instruction reverses the actions of the Enter (OP = 31) instruction, thus accomplishing an exit from the stack.

The instruction restores the settings of the Overflow and Comparison Flags as specified by IX3 plus 15 if the digit at IX3 plus 14 is zero. If the digit at IX3 plus 14 contains a one, the flags will not be restored. All other values (2 to F) are reserved.

Copy the least significant six digits contained in IX3 to memory location 40 relative to Base #0.

Copy the eight digits at the location specified by IX3 plus 6 to IX3.

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13.3	EXIT (EXT	)/OP=32	(Continued)				
	Compariso 	n Flags					
	according	to the		o, set the Com cant 2 bits of r OP = 31).			
	Overlap						
	There are	no overl	an restrictio	ns for this in	struction.		
	EXAM	PLE (1)	Exit the Stac	k			
	0	P A					
	3	2 F00000					
			BEFORE	AFTER			
•		NI	nnnnn	003034			
		IX3	+0001024	+0000010			
		0000040 0001024	001046 003034	001024 unchanged	STACK		
		0001024	+0000010	unchanged	UTAUN .		
			06	unchanged			
			203010	unchanged			
		COMPARIS	0N nnn	LOW			
		OVERFLOW	nnn	ON			
	an an an Araa. Araan			e La constantina de la constantina de la La constantina de la c			
					·		

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OMPANY CON	FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 168
13.4	VIRTUAL ENTER (VEN)/OP=35
	Format
	++ 1 OP   AFBF   A   B
	0F = 35
	AFBF = Length, in bytes, of the Parameter field. The
	maximum number of bytes moved is 9,999. A value of
	0000 will move no data. Indirect field lengths may
	be specified. An AF literal of B1, B2 or B3 will be interpreted as a length of 1, 2 or 3 characters
	in the "A" location. All other literals will cause
	an Invalid Instruction fault (IEX = 22).
	A = Address of the parameter data field operand. Address may be indexed, indirect or extended. The
	final address controller must equal UA or cause an
	Invalid Instruction fault (IEX = 03).
	B = Address of the twenty digit Environment field. Address may be indexed, indirect or extended. The
	final address controller must equal UN or cause an
	Invalid Instruction fault (IEX = 03).
	The Environment field contains the following information:
	INFORMATION DIGITS
	Environment Number 00-05
	Branch Address 06-11
	Reserved 12-19
an di seria di seria Seria di Seria di Seri Seria di Seria	Note - Lowest memory address = 00
	Function
	The Virtual Enter instruction checks the stack limit then
	stores control information and parameters onto the users
	stack, located in memory, and executes an unconditional
	branch to a location specified by the environment field
	(B) using the specified Memory Area Table.

BURROUGHS CORPORATION	 +	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 169

13.4 VIRTUAL ENTER (VEN)/OP=35 (Continued)

The following operations are performed by this instruction.

- Check the Environment field (B) for either of these two cases:
  - a. If the Reserved area of the Environment field is not equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.
  - b. If the Environment Number, contained in the Environment field (B), is equal to zero, store zeroes into the "Active Environment Number" field of the Virtual Enter Stack Frame. Otherwise, store the current Active Environment Number in the Virtual Enter Stack Frame.
- 2. The top of stack pointer, located at memory address 40 (relative to Base #0), is used as the starting address, relative to Base #0 to store the Virtual Enter Stack Frame.

The sum of the top of stack pointer and the size of the Virtual Enter Stack Frame (30) and the amount of parameters (2 x AFBF) and the size of the Hardware Call Stack Frame area (500) is compared to Limit #0. If the sum is equal to or greater than Limit #0, cause a Stack Overflow fault and terminate the instruction with no further action. Otherwise, store the Virtual Enter Stack Frame in the following sequence.

		INFORMATION	DIGITS
OLD TOS	==>	Measurement Register (User Part)	00-05
4 - 14 -		COM & OVF Flags	06-07
		Active Environment Number	08-13
New IX3	==>	Next Instruction Address	14-19
		Saved IX3 Value	20-27
		Stack Frame Indicator ("FF")	28-29
a ¹		Stack Parameters (0 to 9999 byte	es)
New TOS	==>		

Note - Lowest memory address = 00

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COMPANY CONFIDENTIAL SYS	TEM DESIGN SPECI	FICATION	REV. A	PAGE 170			

13.4

VIRTUAL ENTER (VEN)/OP=35 (Continued)

"COM & OVF Flags" contain the following information in the least significant digit. The other digit is reserved for future use and will equal zero.

_____

	INFORMATION	•	BIT
	Reserved	•	3
	Overflow Flag		2
	Comparison Low Flag		1.
	Comparison High Flag		Ũ
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- 3. Move the parameters from a location in memory (A) to the stack.
- 4. Set the two most significant digits of IX3 to "CO", and set the six least significant digits of IX3 to the initial address specified at memory location 40 plus 14, relative to Base #O, to point to the Next Instruction Portion of the Virtual Enter Stack Frame.
- 5. Store the new value of the next available stack Location, relative to Base #0, into memory Location 40, relative to Base #0.
- 6. Reset the Comparison and Overflow Flags.

The Mode Indicators, the Accumulator, the Measurement register, the Moble Index Registers and the Interrupt Mask register are not changed by this instruction.

7. If the Environment Number (B) is equal to zero, then this is a local VEN, which does not require an environment change (i.e., the correct Base/Limit pairs are already resident in the processor). The active Environment Number remains unchanged. Skip the rest of this step.

If the Environment Number (B) is not equal to zero, it replaces the Active Environment Number. Locate and load the Memory Area Table specified by this new Active Environment Number.



#### 13.4 VIRTUAL ENTER (VEN)/OP=35 (Continued)

-

8. Execute an unconditional branch to the address, relative to Base #1, that is contained in the Branch Address portion of the Environment field (B).

The Active Environment Table and the Environment Table being entered must share the same Data Area (Base #0). The processor will not check for improper memory assignments.



13.5

HYPER CALL (HCL)/0P=62

Format

 	·+	 +		- 4
AFBF		Ī	-	I
 -		 		

OP = 62

- AFBF = Length, in bytes, of the Parameter field. The maximum number of bytes moved is 9,999. A value of 0000 will move no data. Indirect field lengths may be specified. An AF Literal of B1, B2 or B3 will be interpreted as a length of 1, 2 or 3 characters in the "A" location. All other literals will cause an Invalid Instruction fault (IEX = 22).
  - A = Address of the parameter data field operand. Address may be indexed, indirect or extended. The final address controller must equal UA or cause an Invalid Instruction fault (IEX = 03).
  - B = Address of the four digit Function Number. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

# Function

The Hyper Call instruction is used to enter a function in the MCP environment. The top of stack limit is checked then the processor registers, state and parameters are stored on the stack of the called environment and control is transferred to the specified function.

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SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 173

#### 13.5 HYPER CALL (HCL)/OP=62 (Continued)

The following operations are peformed by this instruction:

- 1. Locate the six digit address, relative to the Task MCP Data Area, of the Hyper Call Function Table at memory address 87 relative to the Task MCP Data Area.
- 2. The four digit Function Number (B) is used as an array subscript into the Hyper Call Function Table. If the Function Number is not numeric, cause an Address Error fault (AEX = 34) and terminate the instruction with no further action. If the resultant address exceeds the six digit Hyper Call Function Limit, located at memory address 94 relative to the MCP Data Area, cause an Address Error fault (AEX = 02) and terminate the instruction with no further action.

Each Function entry contains the following information:

INFORMATION DIGITS

Environment Number	00-05
Next Instruction Address	06-11
Protection Field (DD)	12-13
Reserved	14-15
Interrupt Mask	16-17
Mode Indicators	18-19

Note - The lowest memory address = 00

If the Protection Field is not equal to "DD", cause an Invalid Instruction fault (IEX = 37) and terminate the instruction with no further action.

3. Resolve the Environment Number, contained in the Function entry, to point to the selected Environment Table entry. However, retain the Active Environment Number so that it may be stored on the stack.

Resolve entry #0 of the Memory Area Table for the new environment from memory and maintain addressability along with Base #0 of the current environment. See Section 5.7 entitled "Resolving a Memory Area Table Entry".

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	0 V 0 T C M		A-7/

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 174 _____

13.5 HYPER CALL (HCL)/OP=62 (Continued)

4. The top of stack pointer, located at address 40 (Relative to the new environment's Base #0), is used as the starting address, relative to the new environment's Base #0, to store the Hyper Call Stack Frame.

The sum of the top of stack pointer and the size of the Hyper Call Stack Frame (96) and the amount of parameters (2 x AFBF) and the size of the Hardware Call Stack Frame area (500) is compared to Limit #0. If the sum is equal to or greater than Limit #0, cause a Stack Overflow fault and terminate the instruction with no further action. Otherwise, store the Hyper Call Stack Frame in the following sequence.

# INFORMATION

DIGITS

OLD TOS	==>	Accumulator	00-27
		Measurement Register	28-35
gen and a second second		Interrupt Mask	36-37
		Mobile Index Registers	38-69
		Mode Indicators	70-71
and the second	a shine tari a	CON & OVF Flags	72-73
		Active Environment Number	74-79
New IX3	==>	Next Instruction Address	80-85
ت بې مېسې د		Saved IX3 Value	86-93
		Stack Frame Indicator (FE)	94-95
		Stack Parameters (O to 9999	bytes)
Nou TOS	>		

New TOS ==>

e e constante

Note - The lowest memory address = 00

- 5. Move the Parameters, if any, from a location in memory (A) to the Hyper Call Stack Frame.
- 6. Store the new address of the next available stack location (Relative to the new environment's Base #0), into memory location 40 (Relative to the new environment*s Base #0).

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13.5	HYPE	RCAL	L (HC	L)/0	P=62	2 (	Con	tin	ued	)								
	7.	Set	the t set															
			initi															
			ative															
		IX3	will	now	poir	nt t	o t	he	Nex	t I	nst	ruc	tic	on A	ddr	ess	in	
		the	Нурег	Cal	LS	tack	Fr	ame	•									
	8-	Set	the m	achi	ne '	'sta	te"	as	fo	110	WS;							
		I	NFORM	ATIO	N									SET	TO			
			ext [.] I									F	und	tio	n T	abl	e	
		A	ctive	Env	iror	nmen	t N	umb	er			F	้นกด	tio:	n T	abl	e	
		· I	nterr	upt	Masl	C								tio:				
			ode I											tio;			e	
			easur															
		C	ompar	ison	8 (	)ver	flo	w F	lag	S				RES	ET			
	9.		the M															
			ster			ing	c h	ang	ed	and	se	t i	t t	o a	"0	ne"	at	
		all	other	tim	es.													
	10.	If S	oft F	ault	is	na	. W	ena	ble	d_	ex	ami	ne	th	e	mem	ory	
			tion															
		poin	ter p	lus	8. 1	lf i	ti	s n	ot	equ	al	to	zer	۰٥,	exe	cut	e a	
		Hard	ware	Cal	l ;	roc	edu	re	tha	t w	iιι	st	ore	e th	e a	ddr	ess	
		of t	he ne	xt i	nsti	ruct	ion	to	be	еx	ecu	ted	• .			•		
	11.	Load	the	Menn	rv /	rea	Та	hle	<b>n</b> 0	int	ed	to	hv	th	6	Act	ive	
	•••		ronme		-					• • • •			-,	• • •				
	12.	Usin	g the	new	Ba	ase/	Lim	it	in	for	mat	ion	,	res	οιν	e	the	
		next	ins	truc	tion	n a	ddr	ess	,	rel	ati	ve	to	Bas	e #	1,	and	
	a	exec	ute a	n un	cond	iti	ona	lb	ran	ch	to	tha	t a	ddr	ess	•		
	The	use o	fthe	Mob	ile	Ind	ex	Reg	ist	ers	or	t	he	Ac	cum	ula	tor	
		pass																
	guar	antee	d.															

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13_6 RETURN (RET)/0P=63

Format -----+ | OP | AF | +----+ OP = 63 AF = Unused and reserved. Function

The Return instruction is a companion instruction to the Hyper Call (OP = 62), and Virtual Enter (OP = 35) instructions and the Hardware Call procedure. It reverses the action of the calling instruction or procedure by loading machine "state" from the current stack, restoring the user environment and executing an unconditional branch to the location specified in the Stack Frame as the Next Program Instruction.

The value of IX3 plus 14 represents the address, relative to Base #0, of the two digit Stack Frame Indicator. The information contained in this field indicates the type of calling procedure that stored the stack frame and the type of Return to be executed.

INFORMATION

INDICATOR

VIRTUAL ENTER/VIRTUAL	EXIT	FF
HYPER CALL(BCT)/HYPER	RETURN	FE
HARDWARE CALL/RETURN		FD

All other the Stack Frame Indicator values are invalid and will cause an Invalid Instruction fault (IEX = 37).

The parameter values stored in the stack are unchanged by this instruction and are not copied into any other area of memory.

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COMPANY CON	FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 177	
13_6_1	VIRTUAL ENTER/VIRTUAL EXIT	
	1. IX3 minus 14 represents the address of the Virtual	
	Enter Stack Frame relative to Base #0. The	
	information in the Virtual Enter Stack Frame is used to replace the respective "state" in the machine.	
	to replace the respective state in the mathine.	
	The Virtual Enter Stack Frame has been stored in the	
	following sequence.	
• • •		
	INFORMATION DIGITS	
	Old TOS ==> Measurement Register (User Part) 00-05	
•		
	COM & OVF Flags U6-U7 Active Environment Number 08-13	
	New IX3 ==> Next Instruction Address 14-19	
	Saved IX3 Value 20-27	
	Stack Frame Indicator ("FF") 28-29	
	Stack Parameters (0 to 9999 bytes)	
	New TOS ==>	
	Note - Lowest memory address = 00	
	2. Replace the address in memory address 40, relative to	
	Base #0, with the value of IX3 minus 14, relative to	
	Base #0. After the "state" is loaded, replace the	
,	contents of IX3 with the value of IX3 in the Virtual	
	Enter Stack Frame.	
	3. The Mode Indicators, the Accumulator, and the	
	Interrupt Mask Register are not changed by this	
	variant.	
	4. If the Environment Number, contained in the stack	
	frame, is equal to zero, the environment being	
	returned to is the same environment that is specified	
and a second s	by the Active Environment Number. Since the correct	
	Base/Limit pairs are already resident within the	
	processor, skip the rest of this step.	
•	If the Environment Number, contained in the stack	
	frame, is not equal to zero, then this instruction is	
	a non-local Virtual Exit, which requires that a new Memory Area Table must be loaded.	
	nemory area laute must de loaded.	

BURROUGHS CORPORATION System development group		1997 5390
PASADENA PLANT COMPANY CONFIDENTIAL SYSTEM	V SERIES INSTRUCTION SET	PAGE 178

## 13.6.1 VIRTUAL ENTER/VIRTUAL EXIT (Continued)

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If the first digit of the Environment Number is equal to a "D" and the processor is not in Privileged Mode, cause an Invalid Instruction fault (IEX = 31) and terminate the instruction with no further action.

Load the Memory Area Table pointed to by the Environment Number in the stack frame.

- 5. Resolve the next instruction address, relative to Base #1, and execute an unconditional branch to that address.
- 6. The current Memory Area Table and the Memory Area Table being entered must share the same Data Area (Base #0). The processor may or may not check for improper memory assignments.

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BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	     V SERIES INSTRUCTION SET 	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 179

# 13.6.2 HYPER CALL/HYPER RETURN HARDWARE CALL/RETURN

- 1. This variant may only be executed in Privileged Mode.
- 2. IX3 minus 80 represents the address of the Hyper Call or Hardware Call Stack Frame, relative to Base #0. The information in the Hyper Call/Hardware Call Stack Frame is used to replace the respective "state" in the machine.

The Hyper Call/Hardware Call Stack Frame has been stored in the following sequence.

		INFORMATION	DIGITS
New TOS	==>	Accumulator	00-27
·		Measurement Register	28-35
		Interrupt Mask	36-37
		Mobile Index Registers	38-69
		Mode Indicators	70-71
		COM & OVF Flags	72-73
		Active Environment Number	74-79
OLD IX3	==>	Next Instruction Address	80-85
		Saved IX3 Value	86-93
		Stack Frame Indicator (FE/FD)	94-95
		Stack Parameters (O to 9999 b	ytes)

0ld TOS ==>

Note - The lowest memory address = 00

- 3. Replace the address in memory address 40, relative to Base #0, with the value of IX3 minus 80, relative to Base #0. After the "state" is loaded, replace the contents of IX3 with the value of IX3 in the Hyper Call/Hardware Call Stack Frame.
- 4. Set the MOPOK line to "zero" while the Measurement register is being changed and set it to a "one" at all other times.
- 5. Load the Memory Area Table pointed to by the Environment Number in the Hyper Call/Hardware Call stack frame.



# 13.6.2 HYPER CALL/HYPER RETURN (Continued) HARDWARE CALL/RETURN

6. Examine the Soft Fault and Trace Mode Fault Condition Indicators to determine if a Hardware Call Procedure should be executed. If Soft Fault is now enabled, examine the Soft Fault Pending Flag in the Reinstate List entry for this task. If it is not equal to zero, then a Soft Fault Condition exists.

If this variant is a Hyper Return (Stack Frame Indicator = FE) and Trace Mode is enabled, then a Trace Fault Condition exists.

> If this variant is a Hardware Return (Stack Frame Indicator = FD), ignore the Trace Mode until the execution of the following instruction is complete.

7. If a Fault Condition has been found, execute a Hardware Call Procedure that will store the address of the next instruction to be executed and report all existing Fault Conditions.

Otherwise using the new Base/Limit information, resolve the next instruction address, relative to Base #1, and execute an unconditional branch to that address.

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13.7	ADJUST STACK POINTER	(ASP)/0P=61	
	Format		
	· · · · · · · · · · · · · · · · · · ·		
	1 OP   AF   BF	•	
	<b>++</b> ++		
	0P = 61	· · · · · · · · · · · · · · · · · · ·	
		(6) must be specified d ld length or a literal.	irectly or as
	BF = Unused and rese	rved. May be specified	as indirect.
	indexed, indir	increment field. Add ect or extended. The be UN or cause an Inval ).	final address
	Function	· · · · · · · · · · · · · · · · · · ·	
	the value of the T address 40, relative	nter instruction is used op of Stack Pointer (loca to Base #0) and to dete e between the Top of Sta	ated at memory rmine if there
	Top of Stack Poi relative to Base #0	ment value (A) and the nter, located at memo and the value of Base #0 Stack Frame area (500)	ry address 40 and the size
	Stack Overflow fau	to or greater than Limit It that stores the a and terminate the instru	ddress of the
		sum of the increment va Top of Stack Pointer to Base #0.	
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COMPANY CO	FIDENTIAL SYSTEM (	DESIGN SPECI	FICATION RI	EV. A	PAGE 182
13.8	INTERRUPT (INT)/OP=	=90			
	Format				
•					
	+++++++++	A 1			
	0P = 90				
	AF = Length of the value of "00" moved. A Li Instruction fa	indicates tl iteral flag	hat there an will caus	re no un	its to be
	BF = Eight bit Kern indirect.	nel Request	code. May I	ce spec	ified as
	A = Address of the indirect or must be UN or (IEX = 03).	extended.	The final a	ddress c	ontrolle
	Function	e de la defensión defensión de la defensión defensión de la defensión de la de	×		
	The Interrupt insti of the system er the information specified.	nvironment to	o the MCP K	ernel an	d to pass
	1. Store "Oó" in	to absolute i	nemory loca	tion 32	- 33.
	2. Store the valu 34 - 35.		absolute	memory	location
	3. If AF does not in absolute me exceeds 40, (IEX = 25).	t equal zero, emory locatio	on 8000. I	f the va	Lue of A
	4. Cause an Inter address of the	rrupt procee e next instru	dure that uction to b	will s e execut	tore the ed.
			xecuted in I		مرامع الع

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PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 183

13.9

VIRTUAL BRANCH REINSTATE (BRV)/OP=93

Format

+----+ | OP | AF | +----+

0P = 93

AF = Unused and reserved.

Function

The Virtual Branch Reinstate instruction is a companion instruction to the Interrupt procedure. The instruction restores the processor registers according to the contents of the Interrupt Frame and transfers control to the task specified by the address of the Reinstate List entry pointer contained in IX1.

The following operations are performed by this instruction to exit the MCP Kernel environment.

- 1. Use IX1 to locate the Reinstate List Entry for the new task to execute. This new task is now referred to as the Current Task.
- 2. Store the Task Number from the Reinstate List Entry for the current task into absolute memory addresses 82-85.
- 3. Reset Kernel Mode.
- 4. Load the Interrupt Frame from the Reinstate List Entry for this task.
- 5. Set the Task Timer to the value located at the Time Slice Remaining field in the Specified Reinstate List Entry.
- 6. Set the MOPOK line to "zero" while the Measurement register is being changed and set it to a "one" at all other times.

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COMPANY CO	INFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 18
13.9	VIRTUAL BRANCH REINSTATE (BRV)/OP=93 (Continued)
	7. If any processor detected faults exist, the Virtua Branch Reinstate has failed. Store:
	(a) the Fault indicators into the Failed Hardwar Call R/D Area Field of the Reinstate List Entr for this task
	(b) "07" into the State Indicator Field in th Reinstate List entry for this task
949) 11. 11.	<pre>(c) "07" into absolute memory location 32 and caus an Instruction Interrupt to the MCP Kernel.</pre>
	8. Load the Memory Area Table pointed to by the "Activ Environment Number", which was loaded from th Interrupt Frame.
	9. Examine the Soft Fault and Trace Fault Conditio Indicators to determine if a Hardware Call Procedur should be executed. If Trace mode is now set, then Trace Fault Condition exists.
	If Soft Fault is now enabled, examine the Soft Faul Pending Flag in the Reinstate List entry for thi task. If it is not equal to zero, then a Soft Faul Condition exists.
	10. If a Fault Condition has been found, execute Hardware Call Procedure that will store the addres of the next instruction to be executed and report al existing Fault Conditions.
and a second sec	Otherwise, use the new Base/Limit information t resolve the next instruction address (Relative t Base #1) and execute an unconditional branch to tha address.
	This instruction may only be executed in Privileged Mode.

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PASADENA PL	ANT	V SERIES INS	TRUCTION SET	
COMPANY CON	FIDENTIAL SYSTEM	DESIGN SPECIFICA	TION REV. A	PAGE 185
14	DATA MOVEMENT			
14_1	MOVE DATA (MVD)/OP	=08		
	Format			· ·
• •	++++++++++	A I B	I C I	
	0P = 08			
	indirect. A Instruction	ard variant. AF herwise, move d literal flag fault (IEX lity Notes (A.20	ata BACKWARD will cause = 21). Se	AF may be an Invalid
	BF = Unused & real indirect field		y be speci	fied as an
	A = Address of the be indexed, controllers a	indirect or ext		
		ress of the d be indexed, in ollers are ignor	direct or ex	· · · · · · · · · · · · · · · · · · ·
	C = End address o may be inde controllers a	xed, indirect		
		difference bet may produce in - Compatibility	compatible	results. See
	the same Me	"C" addresses m mory Area. The r memory assignm	processor wi	

•		
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PASADENA PLANT	V SERIES INSTRUCTION SET	

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 186

14.1

MOVE DATA (MVD)/OP=08 (Continued)

Function

The Move Data instruction moves data from the source data field to the destination data field starting with the "B" address and continuing until the "C" address.

______

Move Forward Variant

--------

If AF = 00, a move forward takes place. The end "C" address must be greater than the starting "B" address, otherwise the instruction has no effect. Source field digits are moved to the destination field in an ascending manner until the "B" address is equal to or greater than the "C" address. No data is moved into the "C" address memory location.

Move Backward Variant

If AF = 01, a move backward takes place. The end "C" address must be less than the starting "B" address, otherwise the instruction has no effect. Source field digits are moved to the destination field in a descending order until the "B" address is equal to or less than the "C" address. No data is moved into the "B" address memory location. No data is moved from the "A" address memory location.

Comparison Flags

The Comparison and Overflow Flags are unchanged by this instruction.

Overlap

Partical overlap of "A" and "B" may produce incompatible results. See Appendix A - Compatibility Notes (A.20.2).

I 1997 5390 BURRCUGHS CORPORATION ---+ SYSTEM DEVELOPMENT GROUP PASACENA PLANT **V** SERIES INSTRUCTION SET COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 187 14.1 MOVE DATA (MVD)/OP=08 (Continued) Examples EXAMPLE (1) Forward Move OP AF BF 8 C A -- -- --08 CO 00 001000 002000 002016 AFTER BEFORE 0001000 0123456789ABCDEF unchanged 0002000 0123456789ABCDEF <u>nnnnnnnnnnnnnnn</u> EXAMPLE (2) Backward Move B OP AF BF A C -----08 01 00 005010 006032 006020

BEFORE

AFTER

 0004098
 9876543210AB
 unchanged

 0006020
 nnnnnnnnn
 9876543210AB

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14.2	MOVE	LINKS	(MVL)/(	)P=09		-			
	Forma	It	a a sana an						
n de la companya de La companya de la comp	I OP	AF	BF	A	•	3	C	+	
	+	+		• • • • • • • • • • • • • • • • • • •				+	
	0P =	09					anti Anti-Anti-Anti-Anti-Anti-Anti-Anti-Anti-		
	8 <b>F</b> =	indir flag See A Unuse	will cau ppendix	eld le ise an A - Co eserved	ngth Inval mpatib , but	may be id Ins ility N	indicat tructio otes (/	ted. on () A_21_1	A litera IEX = 21)
		index contr		lirect	or e	tended	. The	fina	ess may b al addres addres
	<b>B</b> =	index contr		irect	or e	xtended	. The	fina	ess may b al addres addres
		index data	ed, indi type may	irect o y be UN	r exter , SN,	nded. T or UA.	he addı	ress (	ess may b controlle
n an the second seco			ee addre						cause a Appendi

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14-2 MOVE LINKS (MVL)/OP=09 (Continued)

> Function _____

The Move Links instruction moves the number of units specified by AF in the following manner. The "C" field data is saved. The "A" field data is moved to the "C" data field. The "B" field data is moved to the "A" data field. The saved "C" field data is moved to the "B" data field.

*****---

Comparison Flags -----

The Comparison and Overflow Flags are unchanged by this instruction.

Overlap ----

Any total or partial overlap may produce incompatible results. See Appendix A - Compatibility Notes (A.21.2).

Examples -----

AMPLE (1)	Move Num	meric Fie	lds	
OP AF BF	A	•	В	C
09 05 00,	A FIELD	(UN), B	FIELD (UN),	C FIELD (UN)
		BEFORE	AFTER	
A FIELD		12345	67890	
B FIELD		67890	87654	
C FIELD		87654	12345	

EXA

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			************************			6		w ale ale -100 -100 -100 -100		)	
14-2	NOVE	LINKS	(MVL)/	0P=09	( (	Continue	ed)				
		EYANDI	5 (2)	Mova	A 1 -	oha Fiel	de				
			1 an - 1			/11 G [ 1 C ]					
		0P	AF BF		A.:			B 		C.	
		09	03 00,	A FI	ELD	(UA), E	FIE	LD (UA)	, C F	IELD	(UA)
e				· · · · ·		BEFORE	· .	AFTER			
			A FIELD B FIELD C FIELD			XYZ MNO GHI		MNO GHI XYZ			
		EXAMP	LE (3)	Two	Fiel	ld Excha	inge				
	• * ***	0.P	AF BF	н. 19	A		1	<b>B</b> .		С	
		09	04 00,	A FI	ELD	(SN), E	 B FIE	LD (SN)	, B F	IELD	(SN)
								BE	FORE		AFTE
			A FIELD B FIELD			+2386					

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				+							-
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											-

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14.3 MOVE ALPHA (MVA)/OP=10

Fo	0 <b>r m</b> a	at								
+-		-+-		-+-		-+-				+
ľ	0P	ł	AF	1	8 F	1	A	1	8	1

OP = 10

- AF = Length of "A" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "A" address controller). AF may be indirect or may indicate the A-syllable is a literal.
- BF = Length of "B" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "B" address controller). BF may be indirect.
  - A = Address of the source data field. Address may be indexed, indirect or extended. Data type may be UN, SN, or UA.
  - B = Address of the destination data field. Address may be indexed, indirect or extended. Data type may be UN, SN, or UA.

## Function

The Move Alpha instruction moves digits or characters, depending on the address controllers, from one location in memory to another memory location, left justified.

### AF>BF:

If the source data field is longer than the destination field (AF>BF), move the left most BF units from the "A" field to the "B" field, ignoring the remainder of the "A" field data, and set the Overflow Flag.

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 192

14.3

MOVE ALPHA (MVA)/OP=10 (Continued)

AF<BF:

If the source data field is shorter than the destination field (AF<BF), move the data and fill the destination data field with trailing zeros (SN or UN) or blanks (UA).

UA-UA:

When both address controllers specify 8-bit format (UA-UA), move each character.

UN-UN:

When both address controllers specify unsigned 4-bit format (UN-UN), move each digit.

SN-SN:

When both address controllers specify signed 4-bit format (SN-SN), move each digit and set the sign of the destination data field to the standard EBCDIC form (C = positive, D = negative) of the sign of the source data field. (Note: A negative zero remains a negative zero.)

UA-UN:

When the "A" and "B" address controllers specify UA and UN, respectively, only move the low order digit of each character in the source data field to the destination data field.

UA-SN:

When the "A" and "B" address controllers specify UA and SN, respectively, only move the low order digit of each character in the source data field to the destination data field. Set the sign of the destination data field to the standard EBCDIC sign for the interpreted value of the sign located in the most significant digit of the source data field.

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SY	STEM DESIGN SPECIFICATION REV. A	PAGE 193

#### 14.3 MOVE ALPHA (MVA)/OP=10 (Continued)

UN-UA:

When the "A" and "B" address controllers specify UN and UA, respectively, move each digit and set the zone (high order) digit of the character to be stored in the destination data field to the standard EBCDIC numeric subset code (F)_

UN-SN:

When the "A" and "B" address controllers specify UN and SN, respectively, move each digit and set the sign of the destination data field to the standard EBCDIC positive sign code (C).

SN-UN:

When the "A" and "B" address controllers specify SN and UN, respectively, move each digit and ignore the sign of the source data field except for setting the Comparison Flags.

SN-UA:

When the "A" and "B" address controllers specify SN and UA, respectively, move each digit and set the zone (high order digit) digit of the character to be written in the destination data field to the standard EBCDIC numeric subset code (F). The most significant digit of the destination field is set to the standard EBCDIC form of the sign of the source field.

Comparison Flags

Set the Comparison Flags to HIGH if the numeric digits moved from the source data field are non-zero and the sign of the source field is interpreted as positive.

Set the Comparison Flags to EQUAL if the numeric digits moved from the source data field are all zero.

Set the Comparison Flags to LOW if the numeric digits moved from the source data field are non-zero and the sign of the source field is interpreted as negative.



14.3

MOVE ALPHA (MVA)/OP=10 (Continued)

Overlap ----

When the "A" and "B" controllers indicate UA data, the field lengths are equal (AF=BF) and the value of the final "B" address is within the "A" data field (Address "A" to "A"+2 X AF), repeat the source data field between the "A" and "B" addresses throughout the destination data field.

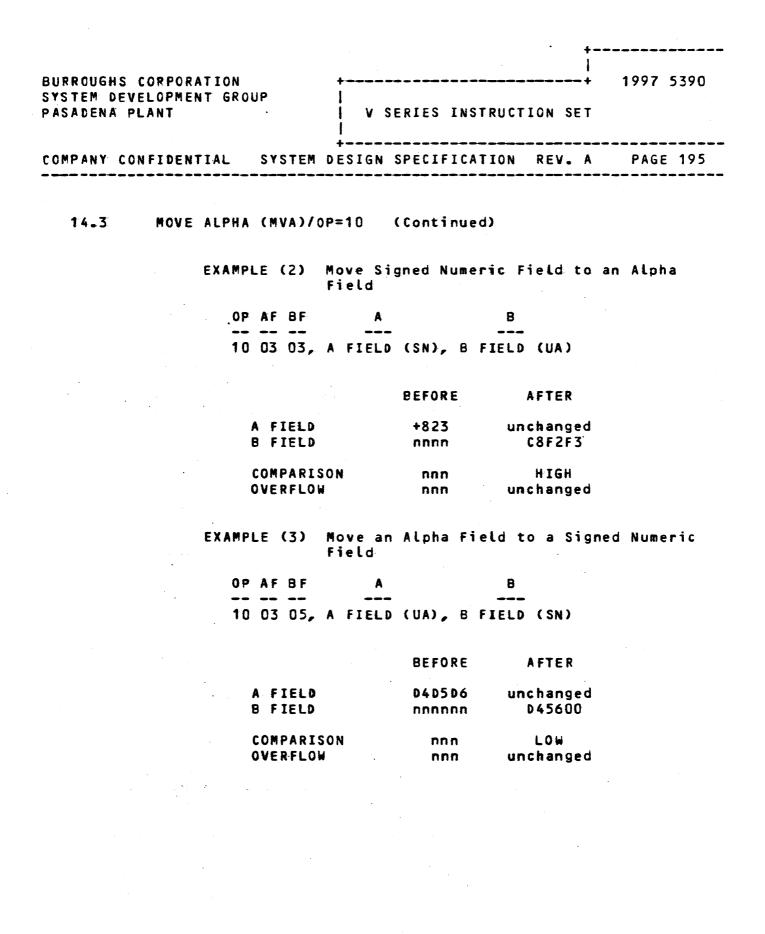
Cases of overlapping "A" and "B", other than described above, may produce incompatible results. See Appendix A - Compatibility Notes (A.03).

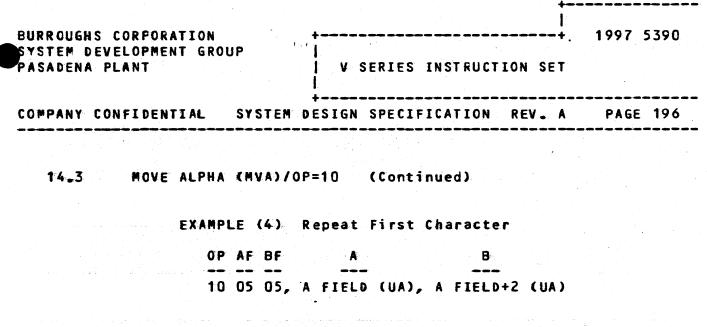
Examples -----

> EXAMPLE (1) Move Numeric Field to a Signed Numeric Field

OP AF BF A B -- -- ---____ 10 05 03, A FIELD (UN), B FIELD (SN)

	BEFORE	AFTER
A FIELD	23511	unchanged
B FIELD	BDDDD	C235
COMPARISON	nnn	HIGH
OVERFLOW	nnn	ON





	BEFORE	AFTER
A FIELD	FOnnnnnnnn	FOFOFOFOFOFO
COMPARISON OVERFLOW	រាពភា ការាក	HIGH unchanged

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CCMPANY CONI	IDENTIAL SYSTEM DESIGN	SPECIFICATION REV.	A PAGE 197
14_4	MOVE NUMERIC (MVN)/OP=11		
	Format		
	++++	++	
	OP   AF   BF   A ++++	B   ++	
	OP = 11		
•	AF = Length of "A" field. Length of 100 u specified by the "A" indirect or may indi	nits (digits or c address controller)	haracters as . AF may be
	BF = Length of "B" field. Length of 100 u specified by the "B" indirect.	nits (digits or c	haracters as
	A = Address of the sourc indexed, indirect SN, or UA.		
	B = Address of the desti be indexed, indire UN, SN, or UA.		
	Function		
	The Move Numeric instruct depending on the address memory to another memory	controllers, from on	e Location in

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BURROUGHS CORPORAT	• 				1997 5390
PASADENA PLANT	i i	V SERIES	INSTRUC	TION SET	

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 198

14.4

MOVE NUMERIC (MVN)/OP=11 (Continued)

AF<BF:

If the source data field is shorter than the destination field (AF<BF), the data is right justified in the destination field and padded with leading zero digits in the cases of UN and SN or zero characters (FD) in the case of UA.

AF>BF:

If the source data field is longer than the destination field (AF>BF), examine the high order numeric digits of the source data field for non-zero content. If these digits are non-zero, set the Overflow Flag and terminate the instruction with no further action. If these digits are zero, left truncate the source field and move the remainder of the field.

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BURRGUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTE	EM DESIGN SPECIFICATION REV. A	PAGE 199

#### 14.4 MOVE NUMERIC (MVN)/OP=11 (Continued)

UA-UA:

When both address controllers specify 8-bit format (UA-UA), move the numeric portion of each character in the source data field to the destination data field with the zone digit set to the standard EBCDIC numeric subset code (F).

UN-UN:

When both address controllers specify unsigned 4-bit format (UN-UN), move each digit.

SN-SN:

When both address controllers specify signed 4-bit format (SN-SN), move each digit and set the sign of the destination data field to the standard EBCDIC form of the sign of source data field (C for positive, D for negative).

UA-UN:

When the "A" and "B" address controllers specify UA and UN, respectively, only move the low order digit of each character in the source data field to the destination data field.

UA-SN:

When the "A" and "B" address controllers specify UA and SN, respectively, only move the low order digit of each character in the source data field to the destination data field. Set the sign of the destination data field to the standard EBCDIC sign for the interpreted value of the sign located in the most significent digit of the source data field.

UN-UA:

When the "A" and "B" address controllers specify UN and -UA, respectively, move each digit and set the zone (high order digit) digit of the character to be written in the destination data field to the standard EBCDIC numeric subset code (F).

BURROUGHS CORPORATION	+	1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 200

14_4 MOVE NUMERIC (MVN)/OP=11 (Continued)

#### UN-SN:

When the "A" and "B" address controllers specify UN and SN, respectively, move each digit and set the sign of the destination data field to the standard EBCDIC positive sign code (C).

# SN-UN:

When the "A" and "B" address controllers specify SN and UN, respectively, move each digit and ignore the sign of the source data field except for setting the Comparison Flags.

SN-UA:

When the "A" and "B" address controllers specify SN and UA, respectively, move each digit and set the zone (high order digit) digit of the character to be written in the destination data field to the standard EBCDIC numeric subset code (F). Set the most significant digit of the destination field to the standard EBCDIC form of the sign of the source data field.

#### Comparison Flags

Set the Comparison Flags to HIGH if the numeric digits moved from the source data field are non-zero and the sign of the source field is interpreted as positive.

Set the Comparison Flags to EQUAL if the numeric digits moved from the source data field are all zero. and the second and the second seco

Set the Comparison Flags to LOW if the numeric digits moved from the source data field are non-zero and the sign of the source data field is interpreted as negative.

Note: Move Numeric UA-UA and UA-UN cause incompatible result in the final comparison flags. See Appendix A - Compatibility Notes (A.04.2).

BURROUGHS CORPORATION System development group	++ I	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	· .
COMPANY CONFIDENTIAL SYS	STEM DESIGN SPECIFICATION REV. A	PAGE 201

14.4 MOVE NUMERIC (MVN)/OP=11 (Continued)

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Overlap

When the "A" and "B" controllers indicate UN data and AF=BF, and the final "B" address one greater than the final "A" address, repeat the first digit of the source data field throughout the destination data field.

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Cases of overlapping "A" and "B", other than described above, may produce incompatible results. See Appendix A - Compatibility Notes (A.04).

Examples

EXAMPLE (1) Move Numeric Field to a Shorter Numeric

OP AF BF A B 11 05 03, A FIELD (UN), B FIELD (UN)

	BEFORE	AFTER
A FIELD	00123	unchanged
B FIELD	nnnn	123
COMPARISON	nnn	HIGH
OVERFLOW	nnn	unchanged

RROUGHS CORPORATION			+-   	1997 5390
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MPANY CONFIDENTIAL SYSTE	+ M DESIGN	SPECIFICA	TION REV. A	PAGE 202
14_4 MOVE NUMERIC (MV	N)/0P=11	(Continu	ued)	
EXAMPLE (2)	Move N Field	umeric fie	ld to a∝Long	er Numeric
OP AF BE	• * * * * * * * * * * * * * * * * * * *		B	
11 03 05	, A FIEL	- D (SN), B I	FIELD (SN)	
	in a proposition Maria a constantia Maria a constantia	BEFORE	AETED	
an an an an Argan an Argan an Argan an Argan an Argan an Argan Argan an Argan an Arg Argan an Argan an Arg				
A FIEL B FIEL	<b>.</b> D	+123 กกกกก	unchanged COO123	
COMPAR Overfl		nnn nnn	HIGH unchanged	
	•			
EXAMPLE (3)	Move a Condit		ield with an	Overflow
OP AF BI	•		8	
11 05 03	S, A FIEL	- D (UN), B 1	FIELD (UN)	
	an a	n an		
	•	BEFORE	AFTER	
A FIEL B FIEL		12300 8888	unchange unchange	
COMPAR Overfl		nnn nnn	unchange ON	<b>1</b>
	ng kalèn kalèn kalèn Kalèn kalèn kal Kalèn kalèn kalè			
	n magina an a	· · · · · · · · · · · · · · · · · · ·		

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SYSTEM DEVELOPMENT GROUP Pasadena plant		V S	V SERIES INSTRUCTION SET			
COMPANY	CONFIDENTI	AL SYSTE	+ M DESIGN	SPECIFICA	TION REV. A	PAGE 203
14-4	MOVE N	UMERIC (MV	N)/0P=11	(Contin	ued)	
	Ē	XAMPLE (4)	Move ar	Alpha Fi	eld to an Alpi	na field
	•	OP AF BF	A		B	
		11 03 03	, A FIELO	(UA), B	FIELD (UA)	
				BEFORE	AFTER	

	BEFORE	AFTER
A FIELD	C2D4E9	unchanged
B FIELD	nnnnn	F2F4F9
COMPARISON	nnn	HIGH
OVERFLOW	nnn	unchanged

EXAMPLE (5) Repeat First Digit

0P	AF	BF		A			8	
	-							
1:1:	05	.05,	A	FIELD	(UN),	A	FIELD+1	(UN)

BEFORE	AFTER
6nnnnn	666666
nnn	HIGH
nnn	unchanged
	6лпппп 

COMPANY CONFIDENTIAL       SYSTEM DESIGN SPECIFICATION REV. A         14.4       MOVE NUMERIC (MVN)/OP=11 (Continued)         EXAMPLE (6) Move ALpha Field to Signed Field         OP AF BF       A         11 03 03, A FIELD (UA), B FIELD (SN)         BEFORE       AFTER         A FIELD       D1COF3       unchanged         B FIELD       nnn       D103         COMPARISON       nnn       LOW         OVERFLOW       nnn       unchanged         EXAMPLE (7) Move Signed Field to Alpha Field       OP AF BF       A         BEFORE       A FIELD (SN), B FIELD (UA)       BEFORE       AFTER         A FIELD       A FIELD (SN), B FIELD (UA)       BEFORE       AFTER	PAGE 204
EXAMPLE (6) Move Alpha Field to Signed Field OP AF BF A B 11 03 03, A FIELD (UA), B FIELD (SN) BEFORE AFTER A FIELD D1COF3 unchanged B FIELD nnnn D103 COMPARISON nnn LOW OVERFLOW nnn unchanged EXAMPLE (7) Move Signed Field to Alpha Field OP AF BF A B 11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	
OP AF 11OF AF BFAB110303, AFIELD (UA), BFIELD (SN)BEFORE B FIELDAFTER D1COF3 nnn D103AFTER D103COMPARISON OVERFLOWnnn nn nnnLOW unchangedEXAMPLE T(7)Move Signed Field to Alpha Field OP AF BF T AB B FIELDOP B F T T T OT D3AFIELD S S S S S 	
11 03 03, A FIELD (UA), B FIELD (SN) BEFORE AFTER A FIELD D1COF3 unchanged B FIELD nnnn D103 COMPARISON nnn LOW OVERFLOW nnn unchanged EXAMPLE (7) Move Signed Field to Alpha Field OP AF BF A B 11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	i
A FIELD B FIELDD1COF3 nnnunchanged D103COMPARISON OVERFLOWnnnLOW unchangedEXAMPLE (7) Move Signed Field to Alpha FieldOP AF BF 11 03 03, A FIELD (SN), B FIELD (UA)BEFOREAFTER +123A FIELD+123unchanged	
B FIELD nnnn D103 COMPARISON nnn LOW OVERFLOW nnn unchanged EXAMPLE (7) Move Signed Field to Alpha Field OP AF BF A B 11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	
OVERFLOW nnn unchanged EXAMPLE (7) Move Signed Field to Alpha Field OP AF BF A B 11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	
OP AF BF A B 11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	
11 03 03, A FIELD (SN), B FIELD (UA) BEFORE AFTER A FIELD +123 unchanged	Ĺ
BEFORE AFTER A FIELD +123 unchanged	
A FIELD +123 unchanged	
	· · · · · · · · · · · · · · · · · · ·
COMPARISON nnn HIGH OVERFLOW nnn unchanged	

EURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 205
14.5 NOVE WORDS (MVW)/	0P=12	

_____

Format

+-		-+-		-+-		-+-		-+
I	0 P	I	AFBF	I	A	1	В	1
+-		- +-		-+		-+		-+

• OP = 12

- AFBF = Length of both operands. A value of "0000" is equal to a length of 10,000 4-digit "words" or 40,000 digits. AF or BF may be indirect. A literal flag will cause an Invalid Instruction fault (IEX = 21). See Appendix A - Compatibility Notes (A.07.1).
  - A = Address of the source data field. Address may be indexed, indirect or extended. Final address controllers are ignored.
  - B = Address of the destination data field. Address may be indexed, indirect or extended. Final address controllers are ignored.
  - Note: Use of non-mod 4 "A" or "B" addresses may produce incompatible results. See Appendix A - Compatibility Notes (A.07.2).

Function

The Move Words instruction moves the number of four digit "words" specified by the concatenation of AF and BF from the source data field in memory to the destination data field in memory.

The contents of the source data field are unchanged (unless "A" and "B" partially overlap).

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROU PASADENA PLANT	IP   V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV. A	PAGE 206

14.5 MOVE WORDS (MVW)/OP=12 (Continued)

Comparison Flags

The Comparison Flags are unchanged by this instruction.

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Overlap

When the final "B" address is less than the final "A" address and the fields partially overlap, the source data field will be shifted by that number of digits to the left. When the "B" data field partially overlaps the "A" data field and "B" is greater than "A", repeat the data from the "A" address to the "B" address throughout the destination data field.

The "B" data field may totally overlap the "A" data field.

EURROUGHS CORPORATION System development group Pasadena plant	+     V SERIES INSTR 	1 1 1997 5390 RUCTION SET
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATI	ON REV. A PAGE 207
14.5 MOVE WORDS (MVW)/	OP=12 (Continued)	
Examples		
EXAMPLE (1)	Move Eight Digits	
OP AFBF	A	8
12 0002	A FIELD, B F	IELD
	BEFORE	AFTER
. A FIELD B FIELD	01020304 	01020304 01020304
COMPARI Overflo		unchanged unchanged
EXAMPLE (2)	Repeat Data Field	
OP AFBF	A	8
12 0002	A FIELD (UN), A FIE	LD+4(UN)
	BEFORE	AFTER
A FIELD	0123nnnnnnn	012301230123
COMPARI Overflo		unchanged unchanged
	Naroda da seconda de la constante de la constant	

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PASADENA PL	ANT	V SER	IES INSTR	UCTION SET	
COMPANY CON	FIDENTIAL SYSTEM	DESIGN SPI	ECIFICATI	ON REV.A	PAGE 208
14.6	MOVE WORDS AND CLE	AR (MVC)/	0P=13		
		•			
	++++	A	B		
• •	OP = 13				
	digits. AF	th of 1 or BF ma an Inval	0,000 4-d y be indi id Instru	igit "word rect. A l ction faul	s" or 40,000 iteral flag t (IEX = 21)
	A = Address of indexed, controllers	indirect	or ext		ess may be nal address
	B = Address of be indexed controllers	, indire	ct or e		Address may inal address
	Note: Use of non- incompatibl A - Compati	.e . r	esults.	See	may produce Appendio
	Function		• • • • • • • • • •		
	The Move Words and four digit "word and BF from the destination data field are set to z	ls" speci source d field.	fied by t ata fiel	he concate d in mem	nation of Al ory to the
	Comparison Flags				
	The Comparison Fla	igs are un	changed b	y this ins	truction.

	SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
CCMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 2	COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 209

14.6

MOVE WORDS AND CLEAR (MVC)/OP=13 (Continued)

Overlap

When the final "B" address is less than the final "A" address and the fields partially overlap, the source data field will be shifted by that number of digits to the left.

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When the "B" data field partially overlaps the "A" data field and "B" is greater than "A", the data from the "A" address to the "B" address will be right justified in the destination data field and filled with leading zeros.

When the "B" data field totally overlaps the "A" data field, the "A" field is rewritten but not cleared.

	ORPORATION LOPMENT GR ANT		V SERIES IN	+- I STRUCTION SET	1997 5390
OPPANY CON	FIDENTIAL	SYSTEM DE	SIGN SPECIFIC	ATION REV. A	PAGE 210
14_6	MOVE WORD	S AND CLEAR	(MVC)/0P=13	(Continued)	
	Examples				
	EXAM		ve Eight Digi eld	ts and Clear t	he Source
		PAFBF	A.	<b>B</b>	
		3 0002 A F	IELD (UN) B	FIELD (UN)	
		•	BEFORE	AFTER	
		A FIELD B FIELD	F1F2F3F4		
		COMPARISON Overflow	<b>nnn</b> <b>nn</b> n	unchanged unchanged	
	EXAN	IPLE (2) Ju	stify Data Fi	eld	
	(	P AFBF		8	
	an a	3 0002, A F	IELD (UN), A	FIELD+4(UN)	
		•	BEFORE	AFTER	
		A FIELD	1605nnnnnn	00000001605	
		COMPARISON Overflow	nnn nnn	unchanged unchanged	
					•
	т на на на на н тр	i i i i i i i i i i i i i i i i i i i	e e e en e	· · · · · · · · · · · · · · · · · · ·	

EURRCUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 211

14.7 MOVE REPEAT (MVR)/OP=14

Format

	+	+	+			+
OP	AF	BF	1	A I	B	ł
	+	+	+			+

0P = 14

- AF = Length of the "A" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "A" address controller). AF may be indirect or may indicate that the A-syllable is a literal.
- BF = Number of repetitions. A value of "00" is equal to 100 repetitions. BF may be indirect.
  - A = Address of the source field. Address may be indexed, indirect or extended. The final address controller data type should specify UN or UA. An SN data type will be treated as UN.
  - B = Address of the destination field. Address may be indexed, indirect or extended. The final address controller data type should specify UN or UA. An SN data type will be treated as UN.

Function

The Move Repeat instruction moves AF number of digits or characters, depending on the address controllers, from the "A" field to the "B" field such that there are BF consecutive copies of the result in the "B" field.

When both address controllers specify 8-bit format (UA), move each character.

When both address controllers specify unsigned 4-bit format (UN), move each digit.

BURROUGHS CORFORATION System development group Pasadena plant		++ 1997 5390				
		V SERIES INSTRUCTION SET				
OPPANY CO	NFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A PAGE 212				
14.7	MOVE REPEAT (MVR)	/OP=14 (Continued)				
	UN, respectively	"B" address controllers specify UA and , only move the low order digit of each source data field to the destination data				
	UA, respectively order digit) digi	"B" address controllers specify UN and , move each digit and set the zone (high t of the character in the destination standard EBCDIC numeric subset code (F).				
antan Marina da	Concention Floor					
	Comparison Flags					
	The Comparison FL	ags are unchanged.				
	Overlap 					
	"A" and "B" may type-address over	totally overlap or may have matching Lap (see 4.9.4).				
	matching type-ad results. See Appe	f the "A" and "B" fields other than dress overlap, may produce imcompatible ndix A - Compatibility Notes (A.15).				
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OMPANY CO	NFIDENTIAL	SYSTEM	DESIGN	SPECIFICAT	ION REV. A	PAGE 213			
14.7	MOVE REPEA	T (MVR)/	0P=14	(Continued	)				
	Examples								
	EXAMP	LE (1)	Repeat 4 Times		Numeric Fiel	Ld			
	0 P	AF BF	A		8				
	14	03 04,	A FIELD	(UN), B F	IELD (UN)				
	•			BEFORE	AFTER				
		A FIELD B FIELD			unchange 057057057				
		COMPARIS Overflow		nnn	unchange unchange				
- ·	EXAMP	LE (2)		a 3 Charac meric Fiel	ter Alpha Fi d	ield Twice			
	0P	AF BF	A		8				
	14	03 02,	A FIELD	(UA), B.F	IELD (UN)				
				BEFORE	AFTER	· · ·			
		A FIELD B FIELD		D4D5D6 nnnnn	D4D5D6 456456				
•		COMPARIS Overflow		nnn nnn	unchangeo unchangeo				
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	99 99 99 99 99 99 99 99 99 99 99 99 99		-			*****	
14.8 TRANSLA	TE (TRN)/OP=	15					
Format							
an a		+		+		+	
• • •	AFBF	A	8		C	 +	
0P =	15				•		
	value of " units. Af or	0000" BF ma n Inva A - C	is e ly be lid In ompati	qual indire struct bility	to a le ct. A ion fau Notes		
an a	address may	be in	dexed,	indir	ect or		
an an an an an an an an Arraigh an an an Arraigh an an an an Arraigh an an an Arraigh an Arraigh an Arraigh an Arraight an Arraight an Arr	controller d	direct ata ty rest	or e pe is rictio	xtende ignor ns on	d. The ed. So this	final address me processors address. See	
	be indexed address cont data type	, ind roller will c	lirect must ause a	or e be UA n Inva	xtended or UN. Lid Ins	e address may The final Use of SI truction fault ibility Notes	
			-				

BURROUGHS CORPORATION System development group Pasadena plant	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTE	4 DESIGN SPECIFICATION REV. A	PAGE 215

14.8 TRANSLATE (TRN)/OP=15 (Continued)

# Function

The Translate instruction substitutes a character from the translate table in the "B" field for each digit or character in the source ("A") field and moves the substituted character or the low order digit of that character to the destination ("C") field.

If the "A" field's data type is UN or SN, assume a EBCDIC numeric subset zone (F) before translation. If SN, the first digit (sign) is ignored.

If the final "C" address controller data type is UN, store only the digit portion of each translated character.

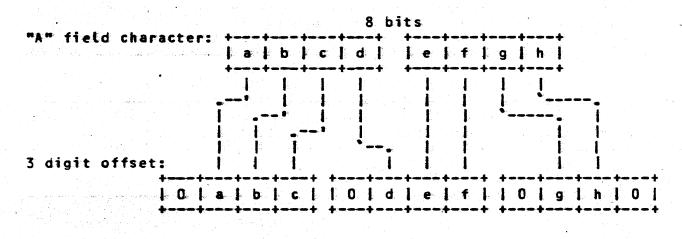
Each "A" field character itself is used to calculate an offset to the "B" address. The character found at "B" + offset is substituted for the "A" field character and moved to the "C" field.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 216

14.8 TRANSLATE (TRN)/OP=15 (Continued)

The offset can be calculated by mapping the bits of the "A" field character to form a 3 digit number as shown in Figure 14.8-1.

Figure 14.8-1 Offset Calculation



Ex. "A" field character "\$" (5B) produces an offset of 266.

A tabulation of offsets for all possible characters is shown in Figure 14.8-2.

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	1	
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 217

**14.8** TRANSLATE (TRN)/OP=15 (Continued)

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# Figure 14.8-2 Offset Tabulation

LSD>	0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F
MSC.																1
0	000	002	004	006	010	012	014	016	020	022	024	026	030	032	034	036
1	040	042	044	046	050	052	054	056	060	062	064	066	070	072	074	076
2	100	102	104	106	110	112	114	116	120	122	124	126	130	132	134	136
3	140	142	144	146	150	152	154	156	160	162	164	166	170	172	174	176
4	200	202	204	206	210	212	214	216	220	222	224	226	230	232	234	236
5	240	242	244	246	250	252	254	256	260	262	264	266	270	272	274	276
6	300	302	304	306	310	312	314	316	320	322	324	326	330	332	334	336
7	340	342	344	346	350	352	354	356	360	362	364	366	370	372	374	376
8	400	402	404	406	410	412	414	416	420	422	424	426	430	432	434	436
9	440	442	444	446	450	452	454	456	460	462	464	466	470	472	474	476
A	1500	502	504	506	510	512	514	516	520	522	524	526	530	532	534	536
В	540	542	544	546	550	552	554	556	560	562	564	566	570	572	574	576
C	600	602	604	606	610	612	614	616	620	622	624	626	630	632	634	636
D	640	642	644	646	650	652	654	656	660	662	664	666	670	672	674	676
E	700	702	704	706	710	712	714	716	720	722	724	726	730	732	734	736
F	740	742	744	746	750	752	754	756	760	762	764	766	770	772	774	776

Note: MSD, LSD is the "A" field character. The corresponding tabulation entry is the offset.

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PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 218

14.8 TRANSLATE (TRN)/OP=15 (Continued)

Overflow/Comparison Flags

The Overflow and Comparison Flags are not changed by this instruction.

# Overlap

If the "A" and "C" data types are both UA or both UN, the "A" and "C" fields may totally overlap. All other forms of overlap may produce incompatible results. See Appendix A - Compatibility Notes (A.14.3).

Examples

EXAMPLE (1) Translate 1 Character OP AF BF A B

		•••		•
-				
- 1	5 00 01	A FIELD (UA)	B FIELD	C FIELD (UA)
		BEFORE		AFTER
	A FIELD	CÓ		C 6
	B ADRS+61	4 7C		70
	C FIELD	nn	4	70
	COMPARISO	No nan		unchanged
	OVERFLOW	nnn		unchanged

С

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COMPANY CON	FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 219
14.9	EDIT (EDT)/OP=49 Format
•	++   OP   AF   BF   A   B   C   ++
	OP = 49 AF = Not used as "A" field length. AF may be indirect or may indicate that the A-syllable is a literal.
	BF = Number of eight bit edit-operators and in line literals in the "B-field". A value of "OO" is equal to a length of 100 characters. BF may be indirect.
	A = Address of the source field to be edited. Address may be indexed, indirect or extended. The address controller data type may be UN, SN, or UA.
	B = Address of the edit-operator field. Address may be indexed, indirect or extended. The final address controller data type is ignored and treated as UA.
· · · · ·	C = Address of the destination field. Address may be indexed, indirect or extended. The final address controller data type must be UN or UA. Use of SN data type will cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.13.1).
	Function
· · · · · · · ·	The Edit instruction moves digits or characters (depending on the "A" address controller) from the "A" field to the "C" field under control of the edit-operators in the "B" field. Characters may be moved, inserted or deleted according to the edit-operators. Data movement and editing are stopped by the exhaustion of edit-operators in the "B" field.
	Unconditionally reset the Overflow Flag.

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BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT I V SERIES INSTRUCTION SET

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 220

# 14.9 EDIT (EDT)/OP=49 (Continued)

The source or "A" field is considered positive for unsigned numeric (UN) format. For unsigned alpha (UA), the most significant digit of the most significant character is interpreted as the sign. For signed numeric (SN), the most significant digit of the field is the sign (which is otherwise ignored).

If the "C" address controller is other than UA, only insert the low order digit of each character in the edit table into the destination data field. Therefore, whenever a blank (40) is specified, a zero will be inserted.

The edit instruction uses an edit table that is located in memory locations 48-63 relative to Base #0. This table may be initialized to any desired set of insertion characters.

The edit-operator field consists of a string of two-digit instructions. Each instruction is of the format MAv. The "M" digit is the operation code portion of the edit-operator. The "Av" digit is the variant position of the edit-operator. The various edit-operators are summarized in Figure 14.9-1 which is followed by a more detailed description. 

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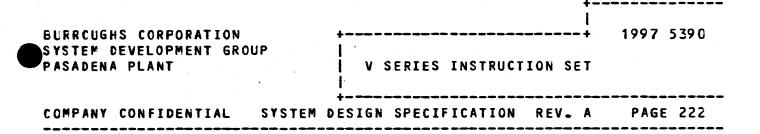
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 SYSTEM DESIGN SPECIFICATION REV. A
 PAGE 221

14.9 EDIT (EDT)/OP=49 (Continued)

Figure 14_9-1 Edit-Operators

+	INSTRUCTION		VARIANT
1 M	NAME	Av	ACTION
	MOVE DIGIT		T<== 1 (SIGNIFICANCE) MOVE Av + 1 DIGITS
1 1	MOVE CHARACTERS	0 thru 9	T<== 1 (SIGNIFICANCE) MOVE Av + 1 CHARACTERS
2	MOVE SUPPRESS	0 thru 9	IF T = 1, M <== 0 IF T = 0, READ EACH A-DIGIT, THEN IF A-DIGIT=0/, M <== 0 IF A-DIGIT=0, THEN IF Q = 0, INSERT BLANK IF Q = 1, INSERT TABLE ENTRY 2
	INSERT UNCONDITIONALLY		INSERT TABLE ENTRY 0 - 7 IF A = +, INSERT TABLE ENTRY 0 IF A = -, INSERT TABLE ENTRY 1 IF A = +, INSERT BLANK IF A = -, INSERT TABLE ENTRY 1 IF A = +, INSERT TABLE ENTRY 0 IS A = -, INSERT BLANK INSERT NEXT B CHARACTER
	INSERT ON PLUS	0 – B	IF A = +, M <== 3 IF A = -, THEN IF Q = 0, INSERT BLANK IF Q = 1, INSERT TABLE ENTRY 2 IF Av = B, SKIP NEXT B CHAR.
	INSERT ON MINUS	0 <b>-</b> B	IF A = -, M <== 3 IF A = +, THEN IF Q = 0, INSERT BLANK IF Q = 1, INSERT TABLE ENTRY 2 IF Av = B, SKIP NEXT B CHAR.



14.9 EDIT (EDT)/OP=49 (Continued)

•	INSTRUCTION		VARIANT
M	NAME	Av	ACTION
6			IF T = 1, M <== 3
			IF T = O, THEN
· 1			IF Q = O, INSERT BLANK
			IF Q = 1, INSERT TABLE ENTRY 2
			IF AV = B, SKIP NEXT B CHAR.
7	INSERT FLOAT	0 — в	IF T = 1, MOVE ONE DIGIT
1			IF AV = B, SKIP NEXT B CHAR.
		l	IF $T = 0$ , READ ONE A-DIGIT, THEN
			IF A-DIGIT=0/, THEN, T <== 1,
	and the second		IF Av = 0 - 7, THEN
		]	INSERT TABLE ENTRY 0 - 7
			MOVE ONE DIGIT
			IF $Av = 8 \pm A = +$ , THEN
			INSERT TABLE ENTRY O,
-			MOVE ONE DIGIT
	•	<b>1</b>	IF $Av = 8 \star A = -$ , THEN
	, <b>,</b>	1	INSERT TABLE ENTRY 1, MOVE ONE DIGIT
1		₿. ∎.	I = IF Av = 9 + A = +, THEN
		Berne (Mexico and Construction) (Construction)	INSERT BLANK,
		1	MOVE ONE DIGIT
. 1		1	IF Av = $9 \pm A = -$ , THEN
		1	INSERT TABLE ENTRY 1,
		• •	MOVE ONE DIGIT
j			IF AV = A + A = +, THEN
		Istantina and a second	INSERT TABLE ENTRY O,
			MOVE ONE DIGIT
	na series de la companya de la comp En la companya de la c		IF AV = $A + A = -$ , THEN
		t l	INSERT BLANK,
- I		1	MOVE ONE DIGIT
.:	a agentication and a second	li de la companya de	IF AV = B, THEN
1		l a construction de la construct	INSERT NEXT B CHAR
	line and the second second	1	MOVE ONE DIGIT
-		t Alexandra de la composición de la com	IF A-DIGIT =0, THEN
1		1	IF $Q = 0$ , INSERT BLANK,
1	1	l	IF Q = 1, INSERT TABLE ENTRY
1			IF AV = B, SKIP NEXT B CHAR.

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BURRCUGHS CORPORATION	 ++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	+ DESIGN SPECIFICATION REV. A	PAGE 223

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14.9 EDIT (EDT)/0P=49 (Continued)

	INSTRUCTION	1	VARIANT
M	NAME	Av.	ACTION
8	I END FLOAT	0 — В     -	IF T = 1, THEN IF AV = B/, NO OPERATION IF AV = B, SKIP NEXT B CHAR. IF T = 0, M <== 3
9	CONTROL     	0   1   2   3	T <== 0   T <== 1   Q <== Q/   SKIP A DIGIT/CHARACTER

"T" denotes a Flag that is set to zero initially and is set to a one (significance) if a digit or character is moved from the source data field to the destination data field or if the CONTROL edit-op (MAv/=/91) is executed. If "T" is equal to one, zero suppression will be inhibited.

"Q" denotes a Flag that is set to zero initially. It is set to a one with the Control edit-op (MAv = 92) if a "check protect" or other character is to be repeated.

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 224

14.9 EDIT (EDT)/OP=49 (Continued)

M = 0, MOVE DIGIT (Av = 0-9):

Set "T" to one (significance).

When the "A" and "C" address controllers both specify 4-bit format (UN or SN), move "Av"+1 digits from the source data field to the destination data field.

When the "A" and "C" address controllers both specify 8-bit format (UA), move the numeric portion of "Av"+1 characters in the source data field to the destination data field and set the zone digit to the EBCDIC numeric subset code (F).

When the "A" and "C" address controllers specify UA and UN respectively, only move the numeric portion of "Av" +1 characters in the source data field to the destination data field.

When the "A" and "C" address controllers specify (UN or SN) and UA respectively, move "Av"+1 digits in the source data field to the destination data field and set the zone digit (high order digit) of each character to be stored to the EBCDIC numeric subset code (F).

H = 1, MOVE CHARACTER (Av = 0-9):

Set "T" to one (significance).

When the "A" and "C" address controllers both specify 4-bit format (UN or SN), move "Av"+1 digits from the source data field to the destination data field.

When the "A" and "C" address controllers both specify 8-bit format (UA), move "Av"+1 characters from the source data field, unchanged, to the destination data field.

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 225

# 14.9 EDIT (EDT)/OP=49 (Continued)

When the "A" and "C" address controllers specify UA and UN respectively, only move the numeric portion of "Av" +1 characters in the source data field to the destination data field.

When the "A" and "C" address controllers specify (UN or SN) and UA respectively, move "Av"+1 digits in the source data field to the destination data field and set the zone digit (high order digit) of each caracter to be stored to the EBCDIC numeric subset code (F).

M = 2, MOVE SUPPRESS (Av = 0-9):

If "T" equals one (significance), perform the operation move digit (M =0).

If "T" equals zero and the first source digit (or the low order digit of the first character) has a value of zero, and "Q" equals zero, insert a blank (40) into the destination data field; if "Q" equals one, insert the edit table value at Base #0+52 into the destination data field. "Av"+1 indicates the number of digits/characters to be examined.

If "T" equals zero and the first source digit (or the low order digit of the first character) has a value other than zero (significance), perform the operation Move Digit (M = 0).

BURRCUGHS CORPORATION	 ++ 1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET
CMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A PAGE 220
14.9 EDIT (EDT)/0P=49	(Continued)
M = 3, INSERT UN	CONDITIONALLY (Av = $0-9$ , A, or B):
If "Av" equa table at B field.	Ls "O-7", insert a character from the editate ase #O+48+2Av into the destination data
field is po Base #0+48 i	ls "8" and the sign of the source dat sitive (+), insert the edit table entry a nto the destination data field.
field is ne	Ls "8" and the sign of the source dat gative (-), insert the edit table entry a ill be inserted into the destination dat
	ls "9" and the sign of the source dat ositive (+), insert a blank (40) into th data field.
field is ne	Ls "9" and the sign of the source dat gative (-), insert the edit table entry a nto the destination data field.
field is po	Ls "A" and the sign of the source dat sitive (+), insert the edit table entry a nto the destination data field.
	ls "A" and the sign of the source data egative (-), insert a blank (40) into the data field.
	Ls "B", insert the next character in the the destination data field.
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BURROUGHS CORPORATION System development group	 ++ 1	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 227

### 14_9 EDIT (EDT)/OP=49 (Continued)

 $M = 4_p$  INSERT ON PLUS (Av = 0-9_ A_p or B):

If the sign of the source data field is positive (+), perform the operation Insert Unconditionally (M = 3).

If the sign of the source data field is negative (-) and "Q" equals zero, insert a blank (40) into the destination data field_

If the sign of the source field is negative (-) and "Q" equals one, insert the edit table entry at Base #0+52 into the destination data field_

If the sign of the source field is negative (-) and if "Av" equals "B", skip the next character in the edit-op field. However, if there are no characters left to skip in the edit-op field, then cause an Invalid Instruction fault (IEX=07).

M = 5, INSERT ON MINUS (Av = 0-9, A, or B):

If the sign of the source data field is negative (-), perform the operation Insert Unconditionally (M = 3).

If the sign of the source data field is positive (+) and "Q" equals zero, insert a blank (40) into the destination data field.

If the sign of the source data field is positive (+) and "Q" equals one, insert the edit table entry at Base #0+52 into the destination data field.

If the sign of the source data field is positive (+) and if "Av" equals "B", skip the next character in the edit-op field. However, if there are no characters left to skip in the edit-op field, then cause an Invalid Instruction fault (IEX=07).

BURRCUGHS CORPORATION 1997 5390 SYSTEM DEVELOPMENT GROUP PASADENA PLANT **V** SERIES INSTRUCTION SET COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 228 14_9 EDIT (EDT)/OP=49 (Continued) M = 6, INSERT SUPPRESS (Av = 0-9 A, or B): If "T" equals one (significance), perform the operation Insert Unconditionally (M = 3). If "T" equals zero and "Q" equals zero, insert a blank (40) into the destination data field. If "T" equals zero and "G" equals one, insert a character from the edit table at Base #0+52 into the destination data field. If "T" equals zero and "Av" equals "B", skip the next character in the edit-op field. However, if there are no characters left to skip in the edit-op field, then cause an Invalid Instruction fault (IEX=07). H = 7, INSERT FLOAT (Av = 0-9, A, or B): If "T" equals one (significance), perform the operation Hove Digit (M = 0, Av = 0). If "T" equals one (significance) and "Av" equals a "B", skip the next character in the in the edit-op field. However, if there are no characters left to skip in the edit-op field, then cause an Invalid Instruction fault (IEX=07). If "T" equals zero and the source digit (AC=SN or UN) or the low order digit of the source character (AC=UA) has a value of zero and "Q" equals zero, insert a blank (40) into the destination data field. If "Q" equals a one, insert the edit table entry at Base #0+52 into the destination data field. If "T" equals zero and the source digit (AC=SN or UN) or the low order digit of the source character (AC=UA) has a value of other than zero, perform the operation Insert Unconditionally (M = 3), set T to one and perform the operation Move Digit (M = 0, Av = 0). If Av = B, skip next character in edit-operator field. However, if there are no characters left to skip in the edit-op field, then cause an Invalid Instruction fault (IEX=07) --Burroughs Prior Written Consent Required For Disclosure Of This Data--

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14.9		EDIT	(EDT)	/0P=49	(Conti	nued)			
		M =	8, EN D	FLOAT	(Av = 0)	-9, A,	or B):		
	,						ance) an erformed		s not equal
				skip tl					equals a the edit-op
•	• 2014	 	If "T" Uncond	equal	s zero Ly (M =	, perf 3).	orm the	operat	ion Insert
		M =	9, CON	TROL (A	v = 0-3	):		•	
				dit-oper varian		erforms	a contr	ol func	tion based
	2000		Varian	it .		Actio	<b>n</b> . -		
	•	•					-		
			1	•		"T" to			
			2			plement			
		•	3			p the So Charac	ource Da ter	ta Field	Digit
					· .				
		Note							the values an Invalid
			In	strucrt	ion fa	ult (I	EX = 07)	. See	Appendix
				-		y Notes	(A.13.2	).	
			•						
· •••	e nor é i	a character		n far			•		
					· · · ·				

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 230

14.9 EDIT (EDT)/OP=49 (Continued)

Overflow/Comparison Flags

Set the Comparison Flags to HIGH if the numeric digits moved from the source data field are non-zero and the sign of the source field is interpreted as positive.

------

Set the Comparison Flags to LOW if the numeric digits moved from the source data field are non-zero and the sign of the source field is interpreted as negative.

Set the Comparison Flags to EQUAL if all the numericsam digits moved from the source data field are equal to zero or if no character or digit is moved from the source data field.

Reset the Overflow flag.

Overlap

Overlap of the "A", "B", or "C" fields in any manner may produce incompatible results. See Appendix A - Compatibility Notes (A_13_3).

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14.9 EDIT (EDT)/0P=49	(Contin	ued	>									
Examples				•								
EXAMPLE (1) Edit			•									
OP AF BF A		8					C					
			-			-		_				
49 00 01, A FIELD (	(UA), 8 F	IEL	D. ()	UA),	, C	FI	ELD	(U)	A )			
A FIELD B FIELD	C1C2C3 02											
C FIELD (AFTER)	F1F2F3											
COMPARISON (AFTER)	HIGH											
EXAMPLE (2) Edit												
OP AF BF	A				<b>8</b> ·					C		
49 00 22, A FIE	ELD (SN),		B	- FIE	 L D 1	CUA	),	(	C FI	LELI	. <u> </u>	IA)
A FIELD									c n	01	30	59
B FIELD				48 85					92	75	64	75
TABLE(48-62)				05	4E			4B	68	5B \$	FO	40
	C1 E8 40 A Y b			5C *	58	F 1	F3	48	F5	F9	40	40
Note: b = Blank							-					
COMPARISON (AFTER)											ш 1	GH

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15	LOGICAL
15.1	SCAN TO DELIMITER - EQUAL (SDE)/OP=16
	Format
	he <del>는 것 같은 것 같은 사</del> 는 사람이 있는 것은 것은 것은 것은 것은 것은 것은 것을 알려갔다. 것은 것은 것은 것은 것은 것은 것은 것을 알려갔다. 것은
	++   OP   AF   BF   A   B
	a na seu de la constant de la consta La CPra≡ 16 de la constant de la cons
	$AF = Length of the "A" field_ A value of "00" is equal to$
	a length of 100 units (digits or characters as specified by the "A" address controller). AF may be
s	indirect or may indicate that the A-syllable is
•	n se la l <b>iteral.</b> No se la segura de la companya de La companya de la comp
	BF = Length of the "B" field. A value of "OO" is equal to
	a length of 100 units (digits or characters a
	<pre>specified by the "B" address controller). Bf may be indirect.</pre>
	A = Address of the delimiter list field. Address may be
	indexed, indirect or extended. The final address
	controller data type may be UN, SN, or UA. An S controller is treated as UN (eg. 7SN = 7UN).
	B = Address of the data field to be scanned. Address ma
	be indexed, indirect or extended. The final address
	controller data type may be UN, SN, or UA. An SI controller is treated as UN (eg. 7SN = 7UN).
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 233

# 15.1 SCAN TO DELIMITER - EQUAL (SDE)/OP=16 (Continued)

# Function

The Scan to Delimiter-Equal instruction scans the "B" field for a character equal to one of the delimiter characters from the "A" field.

_____

The first "B" field character is compared to each delimiter ("A") field character until a match is found. If no match is found, the next "B" field character is compared to each delimiter. Continue this process until a matching delimiter is found or until the "B" field is exhausted.

Note: If a numeric data type (UN/SN) is specified in either field, add the EBCDIC zone digit "F" to each digit to form the character for use in the comparison.

This instruction stores the number of characters in the "B" data field PRECEDING the equal character into memory locations 38-39, relative to Base #0 (accessible with indirect field length). However, if no equal character is found, store the field length of the data field minus one (BF - 1).

Comparison Flags

Set the Comparison Flags to HIGH, if no characters (in the "B" field) were found to be equal to any delimiter (in the "A" field), LOW if the first character was equal to any delimiter and EQUAL if any character but the first was equal to any delimiter.

Overlap

There are no overlap restrictions for this instruction.

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FIDENTIAL SYSTEM	DESIGN :	SPECIFICAT	ION REV. A	PAGE 234	
SCAN TO DELIMITER ·	- EQUAL	(SDE)/OP=	16 (Conti	nued)	
Examples					
		li <b>i ni t</b> ran u <b>F</b> a		diait Faual	
EXAMPLE (I)	Scan ve	Limiter-Ed	ual, rirst	digit Equal	
OP AF BF	A	•	8		
		•	IELD (UA)		
		BEFORE	AFTER	•	
A FIELD		1	unchanged	i.	
		F1C8C4D9	unchanged	l ·	
000038		nn	UU		
COMPARIS	ON	nnn	LOW		
and an					
EXAMPLE (2)	Scan De digit e	limiter-Eq qual	ual, Other	Than First	
OP AF BF	A		B		
T6 01 04	A ETELN		 TELD (11A)		
	N FICLU		IELU (UN)		
	n an	BEFORE	AFTER		
A FIELD		E7	unchanged	l	
B FIELD	•	C1C2E7F5			
	n to date and a second	nn	U2		
		nnn	EQUAL		
and the state of the second state of the state of the second state	n engle produktion	and the second second second second	<ul> <li>A second sec second second sec</li></ul>		
F	SCAN TO DELIMITER Examples EXAMPLE (1) OP AF BF TO 01 04, A FIELD B FIELD 0000038 COMPARIS EXAMPLE (2) OP AF BF TO 01 04, A FIELD B FIELD 0000038	LOPMENT GROUP ANT V SI FIDENTIAL SYSTEM DESIGN S SCAN TO DELIMITER - EQUAL Examples EXAMPLE (1) Scan Del OP AF BF A T6 O1 O4, A FIELD B FIELD OOOOO38 COMPARISON EXAMPLE (2) Scan Del digit ed OP AF BF A T6 O1 O4, A FIELD B FIELD OOOO38	LOPMENT GROUP ANT FIDENTIAL SYSTEM DESIGN SPECIFICAT SCAN TO DELIMITER - EQUAL (SDE)/OP= Examples EXAMPLE (1) Scan Delimiter-Eq OP AF BF A T6 01 04, A FIELD (UN), B F BEFORE A FIELD 1 B FIELD F1C8C4D9 0000038 nn COMPARISON nnn EXAMPLE (2) Scan Delimiter-Eq digit equal OP AF BF A T6 01 04, A FIELD (UA), B F BEFORE A FIELD ET B FIELD C1C2E7F5 Nn	LOPMENT GROUP ANT V SERIES INSTRUCTION SET FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A SCAN TO DELIMITER - EQUAL (SDE)/OP=16 (Conti Examples EXAMPLE (1) Scan Delimiter-Equal, First OP AF BF A B T6 O1 O4, A FIELD (UN), B FIELD (UA) BEFORE AFTER A FIELD 1 unchanged OD00038 nn LOW EXAMPLE (2) Scan Delimiter-Equal, Other digit equal OP AF BF A B T6 O1 O4, A FIELD (UA), B FIELD (UA) EXAMPLE (2) Scan Delimiter-Equal, Other digit equal OP AF BF A B T6 O1 O4, A FIELD (UA), B FIELD (UA) BEFORE AFTER A FIELD ET UNCHANGED BEFORE AFTER A FIELD ET UNCHANGED O000038 nn 02	

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 235

15.2

SCAN TO DELIMITER - UNEQUAL (SDU)/OP=17

Format

+----+---+----+----+----+ OP | AF | BF | A | B | +----+

0P = 17

- AF = Length of the "A" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "A" address controller). AF may be indirect or may indicate that the A-syllable is a literal.
- BF = Length of the "B" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "B" address controller). BF may be indirect.
  - A = Address of the delimiter list field. Address may be indexed, indirect or extended. The final address controller data type may be UN, SN, or UA. An SN controller is treated as UN (eg. 7SN = 7UN).
  - B = Address of the data field to be scanned. Address may be indexed, indirect or extended. The final address controller data type may be UN, SN, or UA. An SN controller is treated as UN (eg. 7SN = 7UN).

Function

The Scan to Delimiter-Unequal instruction scans the "B" field for a character not equal to any of the delimiter characters from the "A" field.

The first "B" field character is compared to each delimiter ("A") field character until a match is found. If a match is found, the next "B" field character is compared to each delimiter. Continue this process until no matching delimiter is found for a given "B" field character or until the "B" field is exhausted.

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COMPANY CONFIDENTIAL	SYSTEM	DESTEN	SPECIFICATION	REV_ A	PAGE 236

### 15.2 SCAN TO DELIMITER - UNEQUAL (SDU)/OP=17 (Continued)

Note: If a numeric data type (UN/SN) is specified in either field, add the EBCDIC zone digit "F" to each digit to form the character for use in the comparison.

This instruction stores the number of characters in the data field PRECEDING the equal character in memory locations 38-39, relative to Base #0 (accessible with indirect field length). However, if no unequal character is found, store the field length of the data field minus one (BF - 1).

Comparison Flags

Set the Comparison Flags to HIGH if all the characters in the data field ("B") are equal to the characters in the delimiter list ("A"), LOW if the first character was not equal to any of the delimiters and EQUAL if some other character is unequal.

Overlap

There are no overlap restrictions for this instruction.

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			•		
15.2	SCAN TO DELIMITER	- UNEQUA	AL (SDU)/	OP=17 (Cont	inued)
	Examples				
		Scan De equal	limiter-U	nequal, First	digit
•	OP AF BF	A L		B	
	17 03 04,	A FIELD	(UN), B	FIELD (UN)	•
			BEFORE	AFTER	
	A FIELD		123	unchanged	
	B FIELD 0000038		6123 nn	unchanged 00	
	COMPARI	SON	nnn	LOW	
	EXAMPLE (2)	Scan Del digit Ui		nequal, Other	Than First °
	OP AF BF	A		в	·
	17 03 04,	A FIELD	(UA), B	FIELD (UA)	
		• • • •	BEFORE	AFTER	
	A FIELD B FIELD 0000038		C1C2C3 C1C2C3C4 nn	unchanged	
	COMPARI	SON	nnn	EQUAL	
1.00	n National States and Stat	an a			

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15.3		SCAN	TO DE		TER -	- ZONE	EQU		ZE)/0f	P=18			· .
		Forma	it -										
		<b>*</b>	+	+					w				
		I OP	I AF	BF		A	<ul> <li>F.</li> </ul>	8	1				
		0P =	18	•			•			÷			
· ·.												equal	
		ang tanàn ang taon an										racter F may	
				ect								lable	
		BF =	Lengt	h of	the	"B" f	ield.	. A: Va	alue d	of "00	" is	equal	t
	• • • •											racter F may	
			indir		Uy	the D		11 633	CONCI	ULLEI	/. Di	r way	U
· · ·		<b>.</b> .	Addre	ss 0.	f th	e deli	miter	liet	fiel	d. Ad	dress	s may	ь
	. ¹ . 1		index	ed,	ind	irect	or	exte	nded.	The	fina	al add	res
		· · · · · ·				ta typ treat						An An	S
		8 =										ddress al add	
			contr	olle	r: da	ta typ	e may	be l	UN, SI	i, or	UA.	. An	S
		· · ·	contr	olle	r is	treat	ed as	S UN (	(eg_ i	'SN =	7UN).	-	
		Funct	ion										
•-		The S	can t	o De	limi	ter-Zo	ne E	qual	inst	ructi	on s	scans	th
		chara	cters	of	th	e "B"	" fie	eld fo	or a c	:harac	ter	hose	zon
						the zo e "A"			of any	of	the	delim	ite
												racter	
												"A") f	
			next									is fo ed to	
		deli	niter!	s zoi	ne.	Contir	nue tl	nis p	rocess	s unti	l a	matc	hin
		deli	iter'	s zo	one	is f	ound	or	until	. the	"B'	' fiel	d i:

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BURROUGHS CORPORATION System development group Pasadena plant

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 239

#### 15_3 SCAN TO DELIMITER - ZONE EQUAL (SZE)/OP=18 (Continued)

•• · ·

Note: If a numeric data type (UN/SN) is specified in either field, the EBCDIC zone digit "F" is used in the comparison.

This instruction stores the number of characters in the data field PRECEDING the zone-equal character in memory locations 38-39, relative to Base #0 (accessible with indirect field length). However, if no zone-equal character is found, store the field length of the data field minus one (BF - 1).

# Comparison Flags

Set the Comparison Flags to HIGH if none of the zones of any of the data field characters are equal to the zone portion of any delimiter list character, LOW if the zone of the first data field character is equal to the zone of any delimiter field character, and EQUAL if the zone of any character but the first were equal.

Overlap

There are no overlap restrictions for this instruction.

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15.3 SCAN TO DELIMITER	- ZONE	EQUAL (SZ	E)/0P=18	(Continued)
Examples		andra an an sua sua sua An serie da Santa San An serie da Santa Sant	para ang ang ang ang ang ang ang ang ang an	
EXAMPLE (1)	Scan Do Equal	elimiter-Z	one Equal,	First Zone
OP AF BF			B	
18 02 03,	A FIEL	- ) (UA), B	FIELD (UA)	
		BEFORE	AFTER	
A FIELD B FIELD			unchanged unchanged	
0000038		nn	00	
COMPARI	SON	nnn	LOW	
EXAMPLE (2)		elimiter-2 Lone Equal		Other Than
OP AF BF	A		B	
18 02 04,	A FIEL	- ) (UA), B	FIELD (UA)	and and a second se
	and a second			
		BEFORE	AFTE	<b>R</b> ¹
A FIELD B FIELD 0000038		C1D1 E6D2C1D4 nn	unchan unchan 01	ged
COMPARI	SON	nnn	EQUA	L

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 241

15.3 SCAN TO DELIMITER - ZONE EQUAL (SZE)/OP=18 (Continued)

EXAMPLE (3) Scan Delimiter-Zone equal, No Zones Equal

_____

 OP AF BF
 A
 B

 18 04 04, A FIELD (UA), B FIELD (UA)

•	BEFORE	AFTER
A FIELD	F160C101	unchanged
8 FIELD	E6E7E8E9	unchanged
0000038	nn	03
COMPARISON	nnn	HIGH

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ONPANY COL	VFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 24
15.4	SCAN TO DELIMITER - ZONE UNEQUAL (SZU)/OP=19
	Format
	++   OP   AF   BF   A   B   ++
	OP = 19
	AF = Length of the "A" field. A value of "00" is equal to a length of 100 units (digits or characters a specified by the "A" address controller). AF may b indirect or may indicate that the A-syllable is literal.
	BF = Length of the "B" field. A value of "OO" is equal to a length of 100 units (digits or characters a specified by the "B" address controller). BF may be indirect.
	A = Address of the delimiter list field. Address may b indexed, indirect or extended. The final addres

controller data type may be UN, SN, or UA. An SN controller is treated as UN (eg. 7SN = 7UN). Э

B = Address of the data field to be scanned. Address may be indexed, indirect or extended. The final address controller data type may be UN, SN, or UA. An SN controller is treated as UN (eg. 7SN = 7UN).

## Function

The Scan to Delimiter-Zone Unequal instruction scans the characters of the "B" field for a character whose zone digit is NOT equal to the zone digit of any of the delimiter characters from the "A" field.

The zone digit of the first "B" field character is compared to the zone digit of each delimeter ("A") field character until a match is found. If a match is found, the next "B" field character's zone is compared to each delimiter's zone. Continue this process until no matching delimiter's zone, is found for a given "B" field character's zone or until the "B" field is exhausted.

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COMPANY CO	ONFIDENTIAL	SYSTEM	DESIGN	SPECIFI	CATION	REV. A	PAGE 243
15.4	SCAN TO	DELIMITER	- ZONE	UNEQUAL	(SZU)/	0P=19	(Continued)

Note: If a numeric data type (UN/SN) is specified in either field, the EBCDIC zone digit "F" is used in the comparison.

-

This instruction stores the number of characters in the data field PRECEDING the zone-unequal character in memory locations 38-39, relative to Base #0 (accessible with indirect field length). However, if no zone-unequal character is found, store the field length of the data field minus one (BF - 1).

Comparison Flags

Set the Comparison Flags to HIGH if every data field zone matches a delimiter character zone, LOW if the zone of the first data field zone is not equal to the zone of any delimiter field character, and EQUAL if some zone, other than the first, in the data field is not equal to the zone of any delimiter list character.

- Overlap

There are no overlap restrictions for this instruction.

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	n an an Anna an Anna Anna An Anna Anna A						
15.4 S	CAN TO DELI	MITER	- ZONE	UNEQUAL (S	ZU)/0P=	19 (C	ontinued)
an an an ann an Aonaichte An ann an Aonaichte an Aonaichte An an Aonaichte an Aonaichte an Aonaichte							
	xamples						
	EXAMPLE	(1)	Scan D Unequa	elimiter-Zo L	ne Unec	ual, Fi	rst Zone
	OP A	FBF		n an an Arrange ann an Arrange ann an Arrange An Arrange ann an Arrange ann an Arrange An Arrange ann an Arrange ann an Arrange	B		
an a		1 04,	A FIEL	- D (UA), B F	IELD (U		
				BEFORE		AFTER	
		FIELD		<b>C</b> 1	L	nchange	d
		FIELD 00038		D1C1C2E nn		nchange 00	
	<b>CO</b>	MPARIS	SON	nan		LOW	
	EXAMPLE	(2)	Scan De first	eLimiter-Zo Zone Unequa	ne Unea L	ual, Ot	her Than
	OP A	FBF	A		В	• 	
	19 0	2 04,	A FIEL	- D (UA), B F	IELD (U		
				BEFORE	,	FTER	
	8	FIELD FIELD		C1D1 C1C2E7C3		hanged hanged	
		00038				02	
	C.O.	MPARIS	SON	nnn	1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -	QUAL	
				•			
	<ul> <li>A start of the sta</li></ul>						

	CORPORATION Velopment group Plant	+     V S	ERIES INSTRU	CTION SET	1997 5390
COMPANY CO	ONFIDENTIAL SY	I + STEM DESIGN	SPECIFICATIO	N REV.A	PAGE 245
15.4	SCAN TO DELIM	ITER - ZONE	UNEQUAL (SZU	)/OP=19	Continued)
	EXAMPLE	(3) Scan De Unequal	limiter-Zone	Unequal, M	lo Zones
	OP AF	BF A		8	
	- 19 02	04, A FIELD	(UA), B FIE	LD (UA)	
			BEFORE	AFTER	
•	•••••	IELD	C1D1	unchanged	
		IELD 0038	C3C4D4D6 nn	unchanged 03	I
	COM	PARISON	nnn	HIGH	

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SYSTEM DEVELOPMENT GROUP Pasadena plant		SERIES I	NSTRUC		ET.	
COMPANY CONFIDENTIAL SYSTEM	+ DESIGN	SPECIFI	CATION	REV.	A PAG	E 240
15.5 SEARCH (SEA)/0P=39			-		 *	
Format						
		an a	2010 1910 1910 - Ali			
++++++++					-+	
+++++++++++++++					-+	
OP = 39				•		
AF = Number of unit						
the two data						
Length of 1	00 un				•	
indicate a li	teral.			•		-
BF = Number of uni						
the "B" addr will be incre						
*00* is equ						
indirect.					en a state de la companya de la comp	
A = Address of the						
indirect or specify the form						
and may be UN,						
B = Address of the	e firs	t table	entry	. Ad	dress ma	ay be
indexed, ind						
same as that final addres					etermine	
incrementatio						
of the Table	•					
must be the s improper memo				will n	ot check	fo
	•	-	he in the		•	
B Address C			Incr	ement	in Digits	; •
	M ) -		r	BF		
01 (S					+1	
10 (U		,		_	x BF	

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BURROUGHS CORPORATION System development group Pasadena plant	I 1997 5390 V SERIES INSTRUCTION SET
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A PAGE 247

15.5 SEARCH (SEA)/OP=39 (Continued)

.

C = Address of the table limit. Address may be indexed, indirect or extended. The final address controller bits specify the type of search to be performed. The Base Indicant of the Table Entry (B) and Table Limit (C) addresses must be the same. The processor will not check for improper memory assignments.

C.	Address Controller	Search Type
	00 (UN) _	Search for Equal
	01 (SN)	Search for Low
	10 (UA)	Search for Lowest

# Function

The Search instruction compares the key field (A) with the first Table Entry (B) in the manner prescribed by the "C" address controller variants, then increments the Table Entry address by the amount specified by BF and the "B" address controller. This new location is compared with the key field (A). Continue this operation of compare and increment until the searched for condition is found or when the Table Entry is equal to or greater than the Table Limit (C), except in the case of "Search Lowest".

The Overflow Flag is reset by this instruction.

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SYSTEM DEVELOPMENT GRO	UP I	
PASADENA PLANT	V SERIES INSTRUCTION SET	f i i i i i i i i i i i i i i i i i i i
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION REV.	PAGE 248

# 15.5 SEARCH (SEA)/OP=39 (Continued)

Search for Equal:

Terminate the search when a Table Entry field equal to the key field (A) is found, or when the Table Limit (C) is reached or exceeded.

If a Table Entry field equal to the key (A) is found, store the address of the Table Entry field, relative to the same base as the "B" operand in IX1 with the same Base Indicant as the resolved "B" operand. Otherwise, IX1 remains unchanged (Search for Equal Condition NOT met).

For SN data, a positive zero does not compare equal to a negative zero.

Search for Low:

Terminate the search when the first Table Entry field less than the key field (A) is found, or when the Table Limit is reached or exceeded.

If a Table Entry field less than the key (A) is found, store the address of that Table Entry field, relative to the same base as the "B" operand, in IX1 with the same Base Indicant as the resolved "B" operand. Otherwise, IX1 remains unchanged (Search for Low Condition NOT met).

For SN data, a negative zero compares less than a positive zero.



15.5 SEARCH (SEA)/OP=39 (Continued)

Search for Lowest:

Terminate the search only when the Table Entry field address reaches or exceeds the Table Limit (C). If any Table Entry fields are found that are less than the key (A), store the first Table Entry field, relative to the same base as the "B" operand, WHICH IS LESS THAN OR EQUAL TO ALL THOSE LESS THAN THE KEY in IX1 with the same Base Indicant as the resolved "B" operand. If NO Table Entry fields are found that are less than the key (A), store the base relative value of the key (A) in IX1 with the two most significant digits of IX1 set to "CO". (Search for Lowest Condition NOT met).

For SN data, a negative zero compares less than a positive zero.

In each type of search, if the Table Entry field being compared to the key (A) overlaps the Table Limit, incompatible results may be produced. See Appendix A - Compatibility Note (A.12)

Comparison Flags

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When the searched for condition is met, set the Comparison Flags to EQUAL. If the searched for condition is NOT met, set the Comparison Flags to HIGH.

## Overlap

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There are no overlap restrictions for this instruction.

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BURROUGHS CORPORATION System development gro Pasadena plant	UP I V SERIES INSTRUC	+ 1997 5390 CTION SET
COMPANY CONFIDENTIAL	SYSTEM DESIGN SPECIFICATION	N REV. A PAGE 250

15.5 SEARCH (SEA)/OP=39 (Continued) 

Examples

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and the second second

EXAMPLE (1) Search Equal

OP AF	BF	A	8		C
39 01	02, A F	EELD (UA),	1000 (1	JA),	1020 (UN)

	BEFORE	AFTER
A FIELD	<b>C1</b>	unchanged
B FIELD	C1F1C2F2C3F3C4F2C5F1	unchanged
IX1	กกุกกุกกุก	+0001000

	COMF	ARISON	nnn	EQUAL
ان پېچېنې اد ود موجه کېږد . در پېچېنې	OVER	FLOW	nnn	OFF
		이 같은 것을 가지?		
9	EXAMPLE	2) Search	Low, Condition	Not Found

	OP AF	BF	A		E	3	(	
	39 01	01, A F		(UN),	1000	(UN),		
							•	

BEFORE AFTER

A FIELD 2	unchanged
B FIELD 3459876345	unchanged
IX1 nnnnnn	unchanged
COMPARISON NAA	HIGH
Overflow naa	OFF
	an a

BURROUGHS CORPORATION System development group Pasadena plant			++ 1997 5390     V SERIES INSTRUCTION SET 			
MPANY	CONFIDENTIAL	+ System de	SIGN SPECIFICATION R	EV. A PAGE 251		
15.5	SEARCH (	SEA)/OP=39	(Continued)			
	EXA	IPLE (3) Se	arch Lowest			
		P AF BF	A B	C		
	•	39 01 01, A	FIELD (UA), 1000 (UA)	, 1020 (UA)		
			BEFORE	AFTER		
		AFIELD	C.5	unchanged		
		B FIELD IX1	C5C2C3C4C9C3C1E2C3C9	unchanged +0001012		
			(Points to Letter A			
		COMPARISON	nnn	EQUAL		
				OFF		

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	ORPORATION Lopment group Ant	<pre>+     V SERIES INSTRUCTIO</pre>	+ 1997 539( N SET
OMPANY CON	FIDENTIAL SYSTEM	ESIGN SPECIFICATION R	
			****
15_6	SEARCH LINK LIST (S	SLL)/0P=37	
	Format		
	<b>*</b>		
	OP   AF   BF	A T B T	
	OP = 37		
		"A" data field. May A value of "OO" is	
	field to be s more to allow of "00" is ed be indirect.	set in units from the " searched. BF is typica for the link address a qual to an offset of ze	lly six digits of t "B". A value
	be compared. extended. The format for bo or UA. If the an Invalid	e key to which the "B" Address may be ind final address controll th the "A" and "B" fiel address controller spe Instruction fault Compatibility Notes (A.	exed, indirect of er specifies the ds and must be U cifies SN, cause (IEX = 03). Set
	may be index not allowed. "A" address bits determine	e first list entry. Th ded or extended. Indir The data format is tha controller. The "B" a the type of compariso	ect addressing is t of the final ddress controller
an a			

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SYSTEM DEVE PASADENA PL	LOPMENT GROUI	P	V SERIES INSTRUCTION SET	r
COMPANY CON	FIDENTIAL	SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 253
15.6	SEARCH LINK	LIST	(SLL)/OP=37 (Continued)	· · ·
	B Address Controller	-	Search Type	
	00 (UN)	=	Search Equal.	
			Set the Comparison Flags to the entire key field is equa data field.	
	01 (SN)		Any Bit Equal.	
	• • • • • • • • •		Set the Comparison Flags to any "one" bit of the key fi to the corresponding bit of 1 field.	ield is equal
	10 (UA)	= (	Less Than or Equal To.	
			Set the Comparison Flags to key field is algebraically ( "B" data field. Set the Compa to EQUAL if the key field is "B" data field.	less than the orison Flags
	11 (IA)		No Bit Equal.	
		1	Logical sums of corresponding "A" and "B" fields are co logical sum is formed for eac "B" field bits are examin logical sums are zero (bit pa or 10) for all pairs, set th Flags to EQUAL.	mpared. The ch pair (all ned). If the airs 00, 01,
	a oo ay			

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PASADENA PLANT		V SI	ERIES	INSTRUCT	ION SET		
COMPANY CONFIDENTIAL	SYSTEM	+	SPECIF	ICATION	REV_ A	PAGE	254

15.6 SEARCH LINK LIST (SLL)/0P=37 (Continued)

Function

The Search Link List instruction compares the key with the data located at "B+BF" or "B+2BF", as specified by the "A" address controller. If the comparison condition is met, set the Comparison Flags, as indicated above, and store the resolved "B" address, with its associated Base Indicant digit, in index register one (IX1). The standard EBCDIC sign is stored in sign digit of IX1. See Appendix A - Compatibility Notes (A.26.1).

The first six digits of "B" contain the address of the next. List entry. In UA format, the address is in the first three characters.

If the conditions are not met, read the next list entry from the "B" data field. This list entry is a link to a new data field which replaces the original "B" data field address, however, the "B" address Base Indicant remains the same as for the resolved "B" data field address. BF is used in the same manner as it was with the original "B" data field. Cotinue this process until the list entry address is zero; at that time set the Comparison flags to HIGH and terminate the instruction without storing into the index register (IX1).

The final "B" address will be checked for undigits (new link-list address will also be checked for undigits).

BURRCUGHS CORPORATION System development group Pasadena plant			++ 1997 5390     V SERIES INSTRUCTION SET 				
OMPANY CO	NFIDENTIAL	SYSTEM	DESIGN	SPECIFICATI	ION REV.A	PAGE 255	
15.6	SEARCH LIN	K LIST (	SLL)/OP:	=37 (Conti	inued)		
	Examples						
					· · · ·		
-	EXAMP	LE (1)	Search B	Equal			
•	OP	AF BF	A		B		
· .		05 06,	A FIELD	(UN), 8-FJ	LELD (UN)		
				· · ·			
				BEFORE	AF	TER	
		A FIELD		12345		anged	
		B FIELD IX1		012345 nnnnnn	unch B-FIELD	anged ADDRESS	
	· · ·	COMPARIS	ON	nnn	EQ	UAL	
	EXAMP	LE (2)	Search /	Any Bit Equ	ual, None F	ound	
-	0P	AF BF	. Ai	•	в		
	37	01 06	A FIELD	(UN), B-F1	(ELD (SN)		
	• • • •			BEFORE	<b>A</b>	FTER	
		A FIELD		6		hanged	
		B FIELD IX1		0000009 nnnnnnn		hanged hanged	
		COMPARIS	ON	nnn .	н	IGH	
	· · · · · · · · · · · · · · · · · · ·	an a		N ² 200 - 1			

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YSTEM DEVELOPMENT G Asadena plant	ROUP	V SERIES INSTI		1777 3370
OMPANY CONFIDENTIAL	SYSTEM DESI	LGN SPECIFICAT	ION REV. A	PAGE 256
15.6 SEARCH L	INK LIST (SLL)	)/0P=37 (Conti	inued)	
EXA	MPLE (3) Sear	rch Less than (	or Equal To	
	OP AF BF		8	
	37 05 06, A FI	(UN), B-F	(UA)	
		BEFORE		FTER
	A FIELD B FIELD IX1	12345 00400012345 nnnnnn	unc	hanged
	COMPARISON	nnn	E	QUAL
EXA	MPLE (4) Seal	rch No Bit Fou	<b>a</b> 1	<u>1</u> - 4 1
	OP AF BF			
· · · · · · · · · · · · · · · · · · ·			B	
· · · · · · · · · · · · · · · · · · ·		••••••••••••••••••••••••••••••••••••••	B	ER
		A [ELD (UN), B-F]	B (ELD (IA)	nged nged
	A FIELD B FIELD	A LELD (UN), B-F1 BEFORE 6 0000009	B [ELD (IA) AFT uncha uncha	nged nged ADDRESS
	37 OT OG A-FI A FIELD B FIELD IX1 COMPARISON	A EELD (UN), B-F1 BEFORE 6 0000009 nnnnnnn nnn	B [ELD (IA) AFT uncha uncha B-FIELD	nged nged ADDRESS
	A FIELD B FIELD IX1 COMPARISON	A [ELD (UN), B-F] BEFORE 6 0000009 nnnnnnn	B [ELD (IA) AFT uncha uncha B-FIELD	nged nged ADDRESS
	A FIELD B FIELD IX1 COMPARISON	A EELD (UN), B-F1 BEFORE 6 0000009 nnnnnnn nnn	B [ELD (IA) AFT uncha uncha B-FIELD	nged nged ADDRESS
	37 OT OG A-FI A FIELD B FIELD IX1 COMPARISON	A LELD (UN), B-FI BEFORE 6 0000009 nannann nnn	B IELD (IA) AFT uncha uncha B-FIELD EQU	nged nged ADDRESS
	A FIELD B FIELD IX1 COMPARISON	A LELD (UN), B-FI BEFORE 6 0000009 nannann nnn	B [ELD (IA) AFT uncha uncha B-FIELD	nged nged ADDRESS

BURROUGHS CORPORATION System development group Pasagena plant	V SERIES INSTRUCTION SET	1997 5390
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 257

15.7 SEARCH LINK DELINK (SLD)/OP=38

Format

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 •		+	•	
		- ·	в	
 +		+	 +	•

0P = 38

- AF = Length of the "A" data field. May be indirect or literal flag. A value of "00" is equal to a length of 100 units.
- BF = Amount of offset in units from the "B" address to the field to be searched. BF is typically six digits or more to allow for the link address at "B". A value of "OO" is equal to an offset of zero units. BF may be indirect.
  - A = Address of the key to which the "B" data field will be compared. Address may be indexed, indirect or extended. The final address controller specifies the format for both the "A" and "B" fields and must be UN or UA. If SN is specified, cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.26.2).
  - B = Address of the first list entry. The initial address may be indexed or extended. Indirect addressing is not allowed. The data format is that of the final "A" address controller. The "B" address controller bits determine the type of comparison to be made:

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					و ورد هر جه چه چه چه چه هو هو هو هو هو هو هو
		~ ~			
15.1	SEAKCH LINK	DELINK (SLU	)/0P=38 (Cont	cinued)	
	B Address				
	Controller		Type		
	a da anti-anti-anti-anti-anti-anti-anti- Anti-anti-anti-anti-anti-anti-anti-anti-a				
	00 (UN)	= Search	Equal.		
		Cat at	· formation 1		CONAL
			e Comparison   ntire "A" key		
			ta field.		
a di seria d		d Department of the second fraction of the second		under state figter	
	01 (SN)	= Any Bi	t Equal.		
	an a	Set th	e Comparison I	lags to	EQUAL when
		any "	one" bit of	the "A"	key field is
		equal data 1	to the correspond	onding b	it of the "B'
	a a substantia de la companya de la	Udla			
	10 (UA)	= Less T	han or Equal	No.	
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		nAn i	e Comparison ey field is a	rlags to Gebraica	LUW IT THE
and the second	atta sugar di se	the "E	" data field.	Set th	e Comparisor
			to EQUAL it		
		equal	to the "B" dat	ta field.	
	11 (IA)	= No Bit	Equal.		
	al an				• • • • • • • • • • • • • • • • • • • •
	ing for the state of the second second		t sums of cori ind "B" field		
			L sum is form		
a Maria da Ar	na sa		ield bits a		
			L sums are zer		
			)) for all pain to EQUAL.		
al sea i printe de la companya de la	- Constrained a result of the result of t				an an an an Araban Margana an Arabana an Arabana Arabana Arabana
				• •	
an a	, in the second seco		n a general de la composition		
			• • • • • • • • • • • • • • • • • • •		an de la companya de La companya de la comp
	and a second and a s A second a se				

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 259

#### 15.7

SEARCH LINK DELINK (SLD)/OP=38 (Continued)

## Function

The Search Link Delink instruction compares the key with the data located at "B+BF" or "B+2BF", as specified by the "A" address controller. If the comparison condition is met, set the Comparison Flags as indicated above. If the condition is met the first time, store the resolved "B" address, with its associated Base Indicant, in both index register one (IX1) and two (IX2). On any other time, store the current "B" address into index register one (IX1) and store the previous "B" address into index register two (IX2). The standard EBCDIC sign is stored in sign digit of IX1 and IX2. See Appendix A - Compatibility Notes (A.26.1).

The first six digits of "B" contain the address of the next list entry. In UA format, the address is in the first three characters.

If the conditions are not met, read the next list entry from the "B" data field. This list entry is a link to a new data field which replaces the original "B" data field address, however, the Base Indicant remains the same as the original "B" data field address. BF is used in the same manner as it was with the original "B" data field. Continue this procedure until the list entry address is zero; at that time set the Comparison Flags to HIGH and terminate the instruction without storing into the index registers (IX1 & IX2).

The final "B" address will be checked for undigits (new tink-list address will also be checked for undigits).

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OMPANY CO	NFIDENTIAL	SYSTEM	DESIGN SPECIF	ICATION	REV. A	PAGE 260
15.7	SEARCH L	INK DELINK	(SLD)/0P=38	(Continu	ed)	
· ,	Examples					
· · · · ·						
	EXA	MDIE (1)	Search Equal		л	
196 - Ale A			Scalen Equat		-	
		OP AF BF	A ===	• B		
		38 05 06	A FIELD (UN)	B FIELD	(UN)	
						•
		an a	BEFOR	E 1	A 1	FTER
	یسی میں در د	A FIELD				nanged
		004000	0040001234		unci 00500	nanged 12345
		**** <b>IX</b> 1******	nnnnn		B-FIEL	ADDRESS
		IX2	nnnnnn	n	8-FIEL	ADDRESS
		COMPARIS	ION nnn	h. Harina an a	E	NUAL
	and a second			•		
	EXA	MPLE (2)	Search Any Bi	t Equal,	None Fou	bur
		OP AF BF	Α	B		
y - 1€ - 1		38 01 06	A FIELD (UN)	B FIELD	(SN)	
			and the second sec		 	
		<ul> <li>A set of second s</li></ul>	BEFOR	E	AFT	ER
		A FIELD		6	unchai	
		B FIELD IX1	000000		unchar unchar	
e Se for e se se se	a di karana k Karana karana k	IX2			unchar	
		COMPARIS	SON nnn		HI	- <b>-</b> -
	5. 		, and a second		<b>Π▲</b> \	
				•		
	•					

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	EVELOPMENT		   V S	SERIES I	NSTRU	CTION	SET	1771 33.
OMPANY	CONFIDENTIA	L SYSTEM	DESIGN	SPECIFI	CATIO	N RE	V_ A	PAGE 2
15.7	SEARCH I	LINK DELIN	K (SLD)/	0P=38	(Cont	inued	)	
	EX	AMPLE (3)	Search	Less Th	an or	Equa	L To	
		OP AF BF	A			8		
		38 05 06	A FIELD	- D (UN)	B FI	ELD (	UA)	
•	· · · · · · · · · · · ·			BEFORE			AF	TER
		A FIELD		12345			unct	anged
		B FIELD		00002345			unch	nanged
		004000 IX1		)0012345 10000000		8.		nanged D ADDRESS
		IX2		nnnnnn				ADDRESS
	•	COMPARI	SON	nnn			EG	DUAL
	EX.	AMPLE (4)	Search	No Bit	Equal		,	
		OP AF BF	A			8		
		38 01 06	A FIEL	D (UN)	B FI	ELD (	IA)	
	•			BEFORE			AFTE	ER
	• • •	A FIELD		BEFORE 6		-		
		B FIELD		6 0040006			unchar unchar	nged nged
		B FIELD 004000		6 0040006 0050009			unchar unchar unchar	nged nged nged
		B FIELD	r r	6 0040006		1	unchar unchar unchar 00004	nged nged nged
· · · · · · · · · · · · · · · · · · ·		8 FIELD 004000 IX1		6 0040006 0050009 nnnnnnn nnnnnnn nnnnnnn		1	unchar unchar unchar 00004 IELD EQU/	nged nged nged 4000 NDDRESS AL
		B FIELD 004000 IX1 IX2		6 0040006 0050009 nnnnnnn nnnnnnn		1	unchar unchar unchar 00004 IELD 4	nged nged nged 4000 NDDRESS AL
		B FIELD 004000 IX1 IX2 Compari	SON	6 0040006 0050009 nnnnnnn nnnnnnn nnnnnnn		1	unchar unchar unchar 00004 IELD EQU/	nged nged nged 4000 NDDRESS AL
•		B FIELD 004000 IX1 IX2 Compari	SON	6 0040006 0050009 nnnnnnn nnnnnnn nnnnnnn		1	unchar unchar unchar 00004 IELD EQU/	nged nged nged 4000 NDDRESS AL
		B FIELD 004000 IX1 IX2 Compari	SON	6 0040006 0050009 nnnnnnn nnnnnnn nnnnnnn		1	unchar unchar unchar 00004 IELD EQU/	nged nged nged 4000 NDDRESS AL

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							49	****	
15_8	SEARCH LIS	T (SLT)/	0P=64						
	Format								
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	field by th	length.	The fi after	ollowi	ng var	riant	s may		ec
	field by th been	length. is field	The fi after	ollowi	ng var	iant ct	s may	be specifi	e
	field by th been	length. is field resolved	The fi after	ollowi	ng var	iant ct	s may Field	be specifi	e
	field by th been FU St	length. is field resolved NCTION ore IX2	The fo after : (Delin	ollowi any k)	ng var	iant ct	s may Field	be specifi	e
	field by th been FU St	length. is field resolved	The fo after : (Delin	ollowi any k)	ng var	iant ct	s may Field MSD	be specifi	ec
	field by th been FU  St No	length. is field resolved NCTION ore IX2	The fo after : (Delini IX1 on	ollowi any k)	ng var	BF	s may Field MSD	be specifi	ec
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	field by th been FU St No CO	length. is field resolved NCTION ore IX2 rmal -	The fo after : (Delini IX1 on	ollowi any k)	ng var	BF	s may Field MSD 4 0	be specifi	ec
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	field by th been FU St No CO  Se Se No An A A A A A	length. is field resolved NCTION ore IX2 rmal - MPARISON arch Low arch Hig Bit Equ y Bit Equ greater Greater Less Tha	The for after CDelini IX1 on IX1 on I	k) Lowi any k) Ly	ng van Indire L to E	BF BF	s may Field MSD 4 0 LSD 9 8 7 6 5 4 3	be specifi	ec
	field by th been FU  St No CO  Se No An A A A A A A A A A A	length. is field resolved NCTION ore IX2 rmal - MPARISON arch Low arch Hig Bit Equ Bit Equ g Bit Equ g Bit Equ Greater Greater Less Tha Less Tha Not Equa	The for after CDelini IX1 on IX1 on I	k) Lowi any k) Ly	ng van Indire L to E	BF BF	s may Field MSD 4 0 LSD 9 8 7 6 5 4 3 2 1	be specifi	ec
	field by th been FU  St No CO  Se Se No An A A A A A A A A A A A A A A A A A A	length. is field resolved NCTION ore IX2 rmal - MPARISON arch Low arch Hig Bit Equ y Bit Equ Greater Greater Less Tha Less Tha Less Tha Less Tha Sot Equa	The for after (Delini IX1 on IX1 on I	r Equa qual to	ng van Indire L to E o B alues	is r	s may Field MSD 4 0 LSD 9 8 7 6 5 4 3 2 1 0 eserve	be specifi Length h d and wi	
	field by th been FU  St No CO  Se Se No An A A A A A A A A A A A A A A A A A A	length. is field resolved NCTION ore IX2 rmal - MPARISON arch Low arch Hig Bit Equ y Bit Equ g Bit Equ g Bit Equ g Bit Equ s Bit Equ g Bit	The for after (Delini IX1 on IX1 on I	r Equa qual to	ng van Indire L to E o B alues	is r	s may Field MSD 4 0 LSD 9 8 7 6 5 4 3 2 1 0 eserve	be specifi Length h d and wi	
	field by th been FU  St No CO  Se Se No An A A A A A A A A A A A A A A A A A A	length. is field resolved NCTION ore IX2 rmal - MPARISON arch Low arch Hig Bit Equ y Bit Equ Greater Greater Less Tha Less Tha Less Tha Less Tha Sot Equa	The for after (Delini IX1 on IX1 on I	r Equa qual to	ng van Indire L to E o B alues	is r	s may Field MSD 4 0 LSD 9 8 7 6 5 4 3 2 1 0 eserve	be specifi Length h d and wi	

BURRCUGHS CORPORATION System development group Pasadena plant	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 263

- 15.8 SEARCH LIST (SLT)/OP=64 (Continued)
  - A = Address of the key field. Address may be indexed, indirect or extended. The final address controller specifies the data type for both the key (A) and the comparison. The address controller must specify UN or UA. An SN controller will cause an Invalid Instruction fault (IEX = 03).
  - B = Address of the list field entry pointer. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03). This six digit field contains an address that is relative to the same memory area as the "B" address. This address is a pointer to the first list to be compared. A value of "EEEEEE" indicates an empty or "NULL" list.
  - C = Address of the list descriptor. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03). The length of this field is always 18 digits and in the following format:

INFORMATION

DIGITS

Link Offset (digits) 00-05 Comparison Offset (digits) 06-11 Key Length (digits) 12-17

Note - The lowest memory address = 00

If any of the list descriptor values are invalid (undigits), cause an Address Error fault (AEX = 34).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 264

### 15.8 SEARCH LIST (SLT)/OP=64 (Continued)

The Search List instruction is a general search instruction for Linked Lists.

If the initial value of the list field entry pointer (B) is equal to "EEEEEE", the list is empty. Store the value "CiEEEEEE", where "i" represents the Base Indicant of the resolved "B" operand, in IX1 and set the Comparison flags to NULL. If the store of IX2 is specified by the most significant digit of "BF", store the address of the List Field Entry pointer (B), relative to the same base as the resolved "B" operand, in IX2.

If the list is not empty, compare the data contained in the key (A), with a length as specified by the Key Length (C 12:6), with the data located in a specified list field. The "B" address specifies a location in memory that contains the six digit address, relative to the same memory area as the resolved "B" operand, of the list field entry pointer in memory. The list field key is found by adding the comparison offset (C 06:6) to the value of the list field entry pointer. The result of the comparison will cause one of two actions.

1. Except in the case of Search Lowest or Search Highest, if the comparison condition, as specified by the Least significant digit of "BF" is met, store the List field entry pointer, relative to the same base as the "B" operand, in IX1.

In the case of Search Lowest or Search Highest, the entire list is examined before storing the address of the entry with the lowest or highest value in IX1.

If the store of IX2 is specified by the most significant digit of "BF" and this is the first comparison, store the address of the List Field Entry pointer, relative to the same base as the resolved "B" operand, in IX2. If it is other than the first comparison, store the address of the previous link address field (list field entry pointer plus the link offset), relative to the same base as the resolved "B" operand, in IX2.

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 265

## 15.8 SEARCH LIST (SLT)/0P=64 (Continued)

2. If the selected comparison condition is not met, use the sum of the list field entry pointer and the Link Offset (C 00:6) as an address to obtain the six digit link address of the next field entry pointer from memory. Repeat this procedure until the compare condition is met or the link address is equal to "EEEEEE".

If the link address is equal to "EEEEEE", store the NULL list value (CiEEEEE) in IX1. If the store of IX2 is specified by the most significant digit of "BF", store the address of the link address field (list field entry point plus the link offset) in the last entry in the list, relative to the same base as the resolved "B" address, in IX2.

ANY BIT EQUAL

"Any Bit Equal" requires that all of the key (A) field be ANDed with all of the comparison field to determine if the the result is equal to zero. If the result is not equal to zero, a match occured.

NO BIT EQUAL

"No Bit Equal" requires that all of the key (A) field be ANDed with all of the comparison field to determine if the result is equal to zero. If the result is equal to zero, a match occured.

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15.8

SEARCH LIST (SLT)/OP=64 (Continued)

SEARCH LOWEST

Terminate a "Search Lowest" only when a NULL Link is reached. Search through the list for the lowest comparison field entry which is also less than key (A). If at least one entry is found, then store the address of the first such entry in IX1 with the same base indicant as the resolved "B" address.

If the store of IX2 is specified by the most significant digit of "BF", store the address of the previous link address field (list field entry point plus the link offset), relative to the same base as the resolved "B" address, in IX2.

If NO entries are found that are less than the key (A), store the NULL list value (CiEEEEE) in IX1. If the store of IX2 is specified by the most significant digit of "BF", store the address of the link address field (list field entry point plus the link offset) in the last entry of the list, relative to the same base as the resolved "B" address, in IX2.

BURROUGHS CORPORATION System development group Pasadena plant	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 267

15.8 SEARCH LIST (SLT)/OP=64 (Continued)

SEARCH HIGHEST

Terminate a "Search Highest" only when a NULL Link is reached. Search through the list for the highest comparison field entry which is also higher than key (A). If at least one entry is found, then store the address of the first such entry in IX1 with the same base indicant as the resolved "B" address.

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If the store of IX2 is specified by the most significant digit of "BF", store the address of the previous link address field (list field entry point plus the link offset), relative to the same base as the resolved "B" address, in IX2.

If NO entries are found that are greater than the key (A), store the NULL list value (CiEEEEEE) in IX1. If the store of IX2 is specified by the most significant digit of "BF", store the address of the link address field (list field entry point plus the link offset) in the last entry of the list, relative to the same base as the resolved "B" address, in IX2.

The relative addresses stored in IX1 and IX2 will be relative to the same base as the resolved "B" address and contain the Base Indicant associated with the resolved "B" address.

The list must reside within one memory area as specified by the Base Indicant associated with the resolved "B" address. The processor will not check for improper memory assignments.

BURRCUGHS CORPORATION System development group Pasadena plant	I 1997 5390 V SERIES INSTRUCTION SET
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A PAGE 268

15.8 SEARCH LIST (SLT)/OP=64 (Continued)

Comparison Flags

If the comparison condition is met on the first entry, set the Comparison Flags to LOW. If the comparison condition is met on other than the first entry, set the Comparison Flags to EQUAL. If the comparison condition is not met, set the Comparison Flags to HIGH.

If the List is empty, set the Comparison Flags to NULL.

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BURROUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTE	FM DESIGN SPECIFICATION REV. A	PAGE 269

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15.9 SEARCH TABLE (STB)/OP=66

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Format

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ŧ	0 P	ŧ	AF	1	8 F	1	A	1	8	1	C	
+-		+-		+-	-	+		+		+		ŀ

= 0P = 66

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- AF = Unused and reserved. AF may be specified as an indirect field length but a literal flag will cause an Invalid Instruction fault (IEX = 21).
- BF = Search Variant and may be specified as an indirect field length. The following variants may be specified by this field after any Indirect Field Length has been resolved:

COMPARISON	BF
Search Lowest	09
Search Highest	08
No Bit Equal	07
Any Bit Equal	06
A Greater Than or Equal to B	05
A Greater Than B	04
A Less Than or Equal to B	03
A Less Than B	02
A Not Equal to B	01
A Equal to B	00

The use of all other BF values is reserved and will cause an Invalid Instruction fault (IEX = 26).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 270

### 15_9 SEARCH TABLE (STB)/OP=66 (Continued)

- A = Address of the key field. Address may be indexed, indirect or extended. The final address controller specifies the data type for both the key (A) and the comparison. The address controller must specify UN or UA_ An SN controller will cause an Invalid Instruction fault (IEX = 03).
- B = Address of the base of the table. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).
- C = Address of the table descriptor. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03). The length of this field is always 24 digits and in the following format:

INFORMATION	nan an <b>san</b> a <b>sayan na</b> an	DIGITS
	(digits)	
Comparison Offset Key Length	(digits) (digits)	
Table Limit	(address)	18-23

Note - The lowest memory address = 00 Invalid table descriptor values will cause an Invalid Instruction fault (IEX = 07).

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 271

15_9 SEARCH TABLE (STB)/OP=66 (Continued)

The Search Table instruction is a general search instruction for Tables. The data contained in the key (A) is compared with the data located in a specified table field. Except for Search Lowest or Search Highest, If the comparison condition, as specified by the least significant digit of "BF" is met, store the address of the table entry in IX1 and set the Comparison Flags. If the selected condition is not met, examine the next table entry. Continue this procedure until the next table entry address is equal to or exceeds the Table Limit address.

In the case of Search Lowest or Search Highest, the entire table is examined before storing the address of the entry with the lowest or highest value in IX1.

Add the value of the Comparison Offset (C 06:6) to the Table Base address (B) to find the first field to be compared.

If the address of the first field to be compared is equal or greater than the Table Limit, the table is empty. Store the value "CiEEEEEE", where "i" represents the Base Indicant of the resolved "B" address, in IX1 and set the Comparison Flags to NULL.

If the comparison condition is not met, the sum of the Table Base address (B) and the Table Entry Length (C 00:6) replaces the Table Base address to point at the next table entry. If the next table entry address is equal to or exceeds the Table Limit address (C 18:6), set the Comparison Flags to HIGH and terminate the instruction. Otherwise, execute another comparison using data from the new table entry.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 272 15.9 SEARCH TABLE (STB)/OP=66 (Continued)

> Except in the case of Search Lowest or Search Highest, if the Table Limit is reached or exceeded, set the Comparison Flags to HIGH and terminate the instruction as indicated above, with IX1 containing "CiEEEEEE".

> The relative address stored in IX1 contains the Base Indicant associated with the resolved "B" address.

The table must reside within one memory area as specified by the Base Indicant associated with the resolved "B" address. The processor will not check for improper memory assignments.

ANY BIT EQUAL

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"Any Bit Equal" requires that all of the key (A) field be logically ANDed with all of the comparison field to determine if the the result is equal to zero. If the result is not equal to zero, a match occured.

NO BIT EQUAL

"No Bit Equal" requires that all of the key (A) field be logically ANDed with all of the comparison field to determine if the result is equal to zero. If the result is equal to zero, a match occured.

SEARCH LOWEST

Terminate a "Search Lowest" only when the Table Limit has been exceeded. If any comparison field entries are found that are less than the key (A), store the Table Entry pointer, relative to the same base as the resolved "B" address, for the FIRST FIELD WHICH IS LESS THAN OR EQUAL TO ALL THOSE FIELDS THAT ARE LESS THAN THE KEY, in IX1 with the same Base Indicant as the resolved "B" address.

If NO entries are found that are less than the key (A), store the NULL list value (CiEEEEEE) in IX1.

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SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	r
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	A PAGE 273

15.9 SEARCH TABLE (STB)/OP=66 (Continued)

SEARCH HIGHEST

Terminate a "Search Highest" only when the Table Limit has been exceeded. If any comparison field entries are found that are greater than the key (A), store the Table Entry pointer, relative to the same base as the resolved "B" address, for the FIRST FIELD WHICH IS GREATER THAN OR EQUAL TO ALL THOSE FIELDS THAT ARE GREATER THAN THE KEY, in IX1 with the same Base Indicant as the resolved "B" address.

If NO entries are found that are greater than the key (A), store the NULL list value (CiEEEEEE) in IX1.

Comparison Flags

If the comparison condition is met on the first compare, set the Comparison Flags to LOW. If the comparison condition is met on other than the first compare, set the Comparison Flags to EQUAL. If the comparison condition is not met, set the Comparison Flags to HIGH.

If the Table is empty, set the Comparison Flags to NULL.

BURROUGHS CORPORATI	ON	++	1997 5390
SYSTEM DEVELOPMENT PASACENA PLANT	GROUP	V SERIES INSTRUCTION SET	

## COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 274

15.10 BIT ZERO TEST (BZT)/OP=40

Format

OP | AF | BF | A |

0P = 40

- AF = Length of the "A" data field. May be indirect or may indicate the A-syllable is a literal. A value of "00" is equal to a length of 100 units.
- BF = Eight bit selection mask. "One" bits in this mask select those bit positions to be tested for "zero" bits within each eight bit group of the "A" data field. "A" through "F" may be used to specify undigits in the mask. The field will not be recognized as indirect.
- A = Address of the data field to be examined. Address may be indexed, indirect or extended. The final address controller type must be UN or UA. Use of SN data type will cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.05).

## Function

The Bit Zero Test instruction tests a data field in memory (A) in eight-bit groups, for "zero" bits in the bit positions selected by the field mask (BF).

If the number of digits accessed is even, the entire eight-bit mask is applied to successive groups of two digits. If the number of digits is odd, the operation is the same until the last digit is accessed. The most significant four bits of the mask are applied to this digit.

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SYSTEM DEVELOPMENT Pasadena plant	GROUP	V SERIES INSTRUCTION SET
COMPANY CONFIDENTI	+- AL SYSTEM DES	IGN SPECIFICATION REV. A PAGE 275
15.10 BIT ZE	RO TEST (BZT)/O	P=40 (Continued)
Compar 	ison Flags	
		ags to EQUAL if any tested bit is all tested bits are "one" bits.
Overla		
Field	overlap is not	applicable to this instruction.
Exampl	es 	
E	XAMPLE (1) Zer	o Test-Zero Found
	OP AF BF	A
	40 04 CO, A F	IELD (UA)
•	DATA	BINARY VALUE
A FIELD	C3C1E77B	11000011110000011110011101111011
MASK Hit Compariso	1	1100000011000001100000011000000 1
	к	
E		o Test-All Ones Found
	OP AF BF	A 
	40 04 CO, A F	IELD (UA)
	DATA	BINARY VALUE
A FIELD	C2D9C1C3	11000010110110011100000111000011
HIT	COCOCOCO (no hit)	11000000110000001100000011000000
COMPARISO	N HIGH	

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COMPANY CONFIDENTIAL S	YSTEM DESIGN SPECIFICATION REV. A	PAGE 276

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15.11

BIT ONE TEST (BOT)/OP=41

Format

÷-	-	+-		+-	-		+	 _		-+
ľ	OP	<b>1</b>	AF	1	B	F	1	A		ł
۰.		•		*-				 	_	- 4

0P = 41

- AF = Length of the "A" data field. May be indirect or may indicate the A-syllable is a Literal. A value of "00" is equal to a length of 100 units.
- BF = Eight bit selection mask. "One" bits in this mask select those bit positions to be tested for "one" bits within each eight bit group of the "A" data field. "A" through "F" may be used to specify undigits in the mask. The field will not be recognized as indirect.
  - A = Address of the data field to be examined. Address may be indexed, indirect or extended. The final address controller data type must be UN or UA. Use of SN data type will cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.05).

Function

The Bit One Test instruction tests a data field in memory (A) in eight-bit groups, for "one" bits in the bit positions selected by the field mask (BF).

If the number of digits accessed is even, the entire eight-bit mask is applied to successive groups of two digits. If the number of digits is odd, the operation is the same until the last digit is accessed. The most significant four bits of the mask are applied to this digit.

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COMPANY CO	NFIDENTIAL	SYSTEM D	+ ESIGN	SPECIFIC	ATION	REV. A	PAGE 277	
15.11	BIT ONE TES	ST (BOT)/	0P=41	(Conti	nued)	•		
	Comparison	Flags						
ء • • • • • • •	Set the Con "one" or to						bit is a bits.	
	Overlap							
	Field over	lap is no	ot appl	licable t	o this	instruct	tion.	
	EXAMPLES		· · · · · · ·					
	EXAMPL	LE (1) (	nes To	est-One F	ound			
		AF BF	A					
	41	03 FO, A	A FIELI	CUN)				
			•	DATA		BINARY	VALUE	
	1	N FIELD Mask HIT		001 FOF 1		0000 000		
		COMPARISC	N	EQUAL				
	EXAMPI	LE (2) (	nes T	est-All Z	eros	Found		
	0 P	AF BF	A					
	41	02 03, /	FIEL	- CUA)				
	andra an	in and an insta-		DATA		BINARY	ALUE	
	an general d	A FIELD Mask HIT		C4C4 0303 (no hit)	(	10001001 000000110		

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MPANY CON	FIDENTIAL SYSTEM	DESIGN SPE	CIFICATION	REV. A	PAGE 27
15.12	COMPARE ALPHA (CPA	)/OP=45			
	•				
	Format				
	OP AF BF	A I	в		
	AF = Length of "A" length of specified by indirect or i	100 uni the "A" ac	ts (digits ddress conti	or char roller). A	acters a F may l
	BF = Length of "B" Length of specified by indirect .	100 unit	ts (digits	or char	acters a
	A = Address of indexed, ind controller da the "B" add Invalid Instr	irect or ta type mi ress cont	extended. ust be UA of troller da	The fin r UN and t ta type o	al addres he same a

- controller data type must be UA or UN and the same as the "A" address controller data type or cause an Invalid Instruction fault (IEX = 03).
- Note: Use of SN data types or mixed UA and UN data types will cause an Invalid Instruction fault (IEX = 03). See Appendix A, Compatibility Notes (A.02).

## Function

The Compare Alpha instruction compares the characters (or digits) in the two data fields in memory according to the binary collating sequence, and sets the Comparison Flags accordingly.

BURROUGHS CORPORATION System development group Pasadena plant	++     V SERIES INSTRUCTION SET	1997 5390
	DESIGN SPECIFICATION REV. A	PAGE 279

## 15.12 COMPARE ALPHA (CPA)/OP=45 (Continued)

If the field lengths are unequal, and the data types are UA, pad the shorter field with trailing blanks (EBCDIC Code 40) to equal the length of the longer field. If the data types are UN, pad the shorter field with trailing zeros.

_____

The values in memory are unchanged.

# Comparison Flags

Set the Comparison Flags to HIGH if the binary value of the "A" data field is greater than that of the "B" data field, EQUAL if the two data fields have exactly the same bit patterns (including trailing blanks or zeros), and LOW if the binary value of the "A" data field is less than that of the "B" data field.

Overlap

There are no field overlap restrictions for this instruction.

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ASADENA PLANT	V SERII	ES INSTRUC	TION SET	1997 2290
CMPANY CONFIDENTIAL SYSTEM	DESIGN SPE	CIFICATION	REV_ A	PAGE 280
15.12 COMPARE ALPHA (CPA	)/OP=45 ((	Continued)		
Examples		an ang san an Ng		
EXAMPLE (1)	Compare Two	Alpha Da	ta Fields	
OP AF BF	n an Anna an A	8		
45 05 03,	A FIFLD (III	A), B ETEL	- D (11A)	
a series and the series and the series of				
	BEI	FORE	AFTER	•
A FIELD	C1 E31	E24040 un	changed	
8 FIELD	C1E3I	E2 un	changed	
COMPARIS	DN	nnn	EQUAL	
		en an earlier an earlier An earlier an earlier a	r r 1 i fean an t-	
EXAMPLE (2)	Compare Two	o Alpha Da	ta Fields	
OP AF BF		ала с <b>В</b>		
45 02 02,	A FIELD (U	A), B FIEL	D (UA)	
	i de la companya de la companya de la com la companya de la comp			
	BEI	FORE	AFTER	
A FIELD B FIELD			changed changed	
	a a ser a			
COMPARIS		nna Statistics	LOW	
a and a star a star a s The star and a star and a star a st	n na san ang na san an Na san ang na san ang na Na san ang na	i ibnai i ainte ainte	na an ann an	•
		an a	· · · · ·	•
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BURRCUGHS CORFORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 281

15.13 COMPARE NUMERIC (CPN)/OP=46

Format

+----+ 1 OP | AF | BF | A | B | +----+

0P = 46

- AF = Length of "A" field. A value of "00" is equal to a length of 100 units (digits or characters as specified by the "A" address controller). AF may be indirect or may indicate the A-syllable is a literal.
- BF = Length of "B" field. A value of "00" is equal to a Length of 100 units (digits or characters as specified by the "B" adoress controller). BF may be indirect.
  - A = Address of the "A" data field. Address may be indexed, indirect or extended. The final address controller data type may be UN, SN, or UA.
  - B = Address of the "B" data field. Address may be indexed, indirect or extended. The final address controller data type may be UN, SN, or UA.

Function

The Compare Numeric instruction algebraically compares the numeric portion of the "A" data field in memory against the numeric portion of the "B" data field in memory.

The numeric portion of a UA data field consists of the least significant digit of each character (i.e. zone digits are ignored).

If the field lengths are unequal, pad the shorter field with leading zeros to equal the length of the longer field. The length does not include the sign digit of a signed numeric (SN) field.

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SYSTEM DEVELOPMENT GRO Pasadena plant	UP	l I V	SERIES INSTRUCT	ION SET	
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COMPANY CONFIDENTIAL	SYSTEM	DESIGN	SPECIFICATION	REV. A	PAGE 282

15.13 COMPARE NUMERIC (CPN)/OP=46 (Continued)

Plus zero compares equal to minus zero. UA and UN fields are assumed to have a positive sign. The values in memory are unchanged.

Comparison Flags

Set the Comparison Flags to HIGH if the algebraic value of the numeric portion of the "A" data field is greater than that of the numeric portion of the "B" data field, EQUAL if the numeric portion of both data fields have exactly the same bit patterns (including leading zeros), and LOW if the algebraic value of the numeric portion of the "A" data field is less than that of the numeric portion of the "B" data field.

Overlap

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There are no field overlap restrictions for this instruction.

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COMPANY CON	NFIDENTIAL	LSYSTEM	DESIGN S	PECIFICA	FION REV. A	PAGE 283
		یہ سے بیٹ روہ خلو کہ جو میں بیوری ہے	, , ,			
15.13	COMPARE	NUMERIC ((	CPN)/OP=4	6 (Con	tinued)	
	Examples	S.				
		-				
	EXAI		Compare a Insigned		Literal Field	with an
	· .	OP AF BF	A		B	
		46 AA 05 0	 20 (SL)	- 8 FI	ELD (UN)	
	•					
				BEFORE	AFTER	
		A FIELD		C20	unchanged	
		B FIELD		00015	unchanged	
		COMPARIS	SON	nnn	HIGH	•
	EXA		Compare a Signed Fi		Literal Field	d with a
		OP AF BF	A		8	
		46 A6 02,	000012 0	NI) - B F	TELD (SN)	
		· .		BEFORE	AFTER	
· · · · ·		A FIELD B FIELD		000012 c25	unchanged unchanged	•
		COMPARIS	SON	nnn	LOW	
	· · · ·					
•	and the second s	•	1	- ·		

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A PAGE 284

15.13 COMPARE NUMERIC (CPN)/OP=46 (Continued)

	46 US US, A FI	ELD (UN), B	FIELD (UA)
an a			
		BEFORE	AFTER
	A FIELD B FIELD	213 · D2C1D4	unchanged unchanged
	COMPARISON	កភា	LOW

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COMPANY	CONFIDENTIAL	SYSTEM	DESIGN	SPECIFIC	ATION	REV.	A	PAGE	285

15.14 BIT RESET (BRT)/OP=33

Format

+-	-	-+-		+-		-+-		-+
1	0P	1	AF	I	BF	1	A	1
+		-+-		+-		-+-		-+

0P = 33

- AF = Length of the "A" data field. May be indirect. A value of "00" is equal to a length of 100 units. A literal will cause an Invalid Instruction fault (IEX = 21). See Appendix A Compatibility Notes (A.22).
- BF = Eight bit selection mask. "One" bits in this mask select those bit positions to be set to "zero" bits within each eight bit group of the "A" data field. "A" through "F" may be used to specify undigits in the mask. The field will not be recognized as indirect.
  - A = Address of the data field operand. Address may be indexed, indirect or extended. The final address controller must be UN or UA. If UN format is specified and the number of digits accessed is even, the entire eight-bit mask is applied to successive groups of two digits. If the number of digits is odd, the operation is the same until the last digit is accessed. The most significant four bits of the mask are applied to this digit. If the controller specifies SN, cause an Invalid Instruction fault (IEX = 03).

Function

The Bit Reset instruction resets bits in a data field in memory (A) in eight-bit groups, according to the bit positions selected by "one" bits in the field mask (BF).

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15.14 1	BIT RESET	(BRT)/0P=33	(Continued)	
	Compariso	n Flags		-
			ags to HIGH if the least significa is a "one"; otherwise, set them	
	Overlap			
	There are	no overlap	restrictions.	
	Examples			
	EXGMPLES	n de la competencia d La competencia de la c		
EXA	NPLE (1)	Bit Reset,	Alpha Field	
	OP AF BF			
	33 03 AO.	A FIELD (UA		
n an	a an an an ar an	DATA	BINARY VALUE	
	IELD		111100011111001011110011	
	K Ult	A0A0A0 515253	101000001010000010100000 0101000101010010	
	PARISON	HIGH		
	FARLJUN	N 7 0 11		
EXA	MPLE (2)	Bit Reset,	Numeric Field	
	OP AF BF			
ు ఈ ఇందిన యాయిత్రం నికి				
	33 05 15,	A FIELD (UN		
<ul> <li>A state of the s</li></ul>		DATA	BINARY VALUE	
۵۵ کار کار کار در دارد. ۲۰۰۰ <b>۸</b> ۹۰ <b>۴</b> ۰	IELD	43105	0100001100010000101	
MAS	K	15151	00010101000101010001	
		42004	0100001000000000100	
RES	ULT	42004		

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 287

15.15 BIT SET (BST)/OP=34

Format

+		+-		+		+		+
ľ	0P	T	AF	1	8 F		A	- I
		+-		+-		+		+

0P = 34

- AF = Length of the "A" data field. May be indirect. A value of "00" is equal to a length of 100 units. A literal will cause an Invalid Instruction fault (IEX = 21). See Appendix A Compatibility Notes (A. 26.1).
- BF = Eight bit selection mask. "One" bits in this mask select those bit positions to be set to "one" bits within each eight bit group of the "A" data field. "A" through "F" may be used to specify undigits in the mask. The field will not be recognized as indirect.
  - A = Address of the data field operand. Address may be indexed, indirect or extended. The final address controller must be UN or UA. If UN format is specified and the number of digits accessed is even, the entire eight-bit mask is applied to successive groups of two digits. If the number of digits is odd, the operation is the same until the last digit is accessed. The most significant four bits of the mask are applied to this digit. If the controller specifies SN, cause an Invalid Instruction fault (IEX = 03).

Function and a second second

The Bit Set instruction sets bits in a data field in memory (A), in eight-bit groups, according to the bit positions selected by "one" bits in the field mask (BF).

BURROUGHS CORPORATION	++ 1997 5390				
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET				
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A PAGE 288				
15.15 BIT SET (BST)/OP=3	34 (Continued)				
Comparison Flags					
Set the Comparison bit of the resu EQUAL.	n Flags to HIGH if the Least significant ult is a "one"; otherwise, set them to				
Overlap					
There are no overl	lap restrictions.				
Examples					
FXANPLE (1)	Bit Set, Alpha Field				
OP AF BF					
34 03 AO,	A FIELD (UA)				
DATA	BINARY VALUE				
A FIELD 515253	010100010101001001010011				
MASK ADADAO Result f1f2f3	10100000101000010100000 111100011111001011110011				
COMPARISON HIGH					
FXAMPLE (2)	Bit Set, Numeric Field				
OP AF BF					
	A FIELD (UN)				
DATA	BINARY VALUE				
A FIELD 94236	10010100001000110110				
MASK F1F1F	11110001111100011111				
RESULT F5F3F	11110101111100111111				
COMPARISON HIGH					

PASADENA PLANT V SERIES INSTRUCTION SET			
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PASADENA PLANT V SERIES INSTRUCTION SET	BURRUUGHS CORFORATION	•	
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	PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 289	T NONDEWN TENNT		
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	COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 289

15.16 LOGICAL AND (AND)/OP=42

Format

· · · ·

0P = 42

- AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of "00" is equal to a length of 100 units.
- BF = Length of the "B" field. BF may be indirect. A value of "OO" is equal to a length of 100 units.
  - A = Address of the "A" source field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
  - B = Address of the "B" source field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
  - C = Address of the result field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
- Note: If the data types are not all UA or not all UN, cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.11.1).

BURROUGHS CORPORATION	 ++	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
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COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 290

15_16 LOGICAL AND (AND)/OP=42 (Continued)

#### Function _____

The Logical And instruction stores the logical product (AND) of two data fields (A & B), located in memory, into a third memory location (C).

The "C" field length is equal to the larger of AF or BF. If the "A" and "B" fields are not of equal length, pad the shorter by adding trailing characters/digits of all zero bits.

Comparison Flags -----

Set the Comparison Flags to HIGH if the least significant bit of the result is a "one"; otherwise, set them to EQUAL 

Overlap -----

Total overlap or matching type-address overlap of any of the fields is allowed. Partial overlap of "A" or "B" with "C" other than matching type-address overlap may produce incompatible results. See Appendix A - Compatibility Notes (A.11.2).

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MPANY CONFIDENTIAL SYSTE	M DESIGN SPE	CIFICATION R	EV. A PAGE 291
15.16 LOGICAL AND (AND	)/OP=42 (C	ontinued)	
Examples			
EXAMPLE (1)	AND Two Nu	meric Fields	
OP AF BF	A	В	С
 42 02 03	A FTELD (III	N). R FTFID (I	JN), C FIELD (UN)
	BEFORE	AFTER	BINARY VALUE
	D F6		
B FIEL C FIEL		unchanged 220	001000110101 001000100000
COMPAR	ISON nnn	EQUAL	
EXAMPLE (2)	AND TWO AL	pha Fields	
OP AF BF	A	8	C.
42 02 03	, A FIELD (U	A), B FIELD (1	JA), C FIELD (UA)
В	EFORE A	FTER	BINARY VALUE
B FIELD D	40801 uncl	hanged 110101	11111101000000000 00110110001101000
C FIELD		· · · ·	1001100100000000
COMPARISON	nnn E	QUAL	

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT		V SERIES INSTRUCTION SET					1997 539(	
OMPANY CONFI	IDENTIAL	SYSTEM D	+	SPECI	FICAT	 I O N	REV. A	PAGE 29
15.17 L	OGICAL OR	(ORR)/OF	=43	•	•			
	Format	• • •		n An An An Anna An An	4 			
	•••••	-		•		•		r .
	0P   AF				8	 +	C ]	
	a si ta ma si sa si si si si si si si s		- 	n n seje	ر. رواند المحاد		s • .	
	DP = 43						-	
	indica		A-sy	Llable	is	a Li	teral.	ect or may A value o
		of the "is equ						ct. A valu
								ess may be
								inal address
		is the ot						must be the types.
and a second								ess may be
								inal address must be the
n an								types.
	C = Addres	e of the	racul	+ + +	A h L	ddeee	e mav	be indexed,
	indire	ct or	extend	ied.	The f	inal	addres	s controlle
								same as the
	other	address	contro	oller	data	types	•	
	Note: If t caus	he data e an Inv	types alid 1	are n Instru	ot al	L UA faul	or n t (IEX	ot all UN, = 03). Sec 1).
and the second				atibil	ity N	otes.	(A.11.	1).
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15.17 LOGICAL OR (ORR)/OP=43 (Continued)

Function

The Logical Or instruction stores the logical sum (OR) of two data fields (A & B), located in memory, into a third memory location (C).

The "C" field length is equal to the larger of AF or BF. If the "A" and "B" fields are not of equal length, pad the shorter by adding trailing characters/digits of all "zero" bits.

Comparison Flags

Set the Comparison Flags to HIGH if the least significant bit of the result is a "one"; otherwise, set them to EQUAL.

Overlap

Total overlap or matching type-address overlap of any of the fields is allowed. Partial overlap of "A" or "B" with "C" other than matching type-address may produce incompatible results. See Appendix A - Compatibility Notes (A.11.2).

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OMPANY CONFIDENTIAL SY	STEM	DESIGN	SPECIFI	CATION	REV.	PAG	E 294
15.17 LOGICAL OR (0	RR)/0	P=43	(Contin	ued)		ni na secondaria.	
Examples			and a state of the				
			enne serie de la serie Sudde de la serie de la serie Transformation de la serie de la s				•
EXAMPLE		OR TWO	Numeric	Fields			
OP AF	BF,	<b></b>	an da an References de la companya de la comp References de la companya de la comp	В		C	
43 02	03	A ETEI	.D (UN),	B FTFID	( LIN )	 C ETEL D	(IIN)
					( UN / ,	C TILLU	V.UN7
an an a' Si Dalah salar tang tang bilan kalan kalan kalan sa		EFORE	ACT	ER	DINAD	/ VA1 05	
	D	EFVRE	AT 1	CN	DINAK	VALUE	
A FIELD	••• •••	.81	uncha	nged	100000	0010000	
8 FIELD C FIELD		223	uncha	nged 3	101000	0100011	
			and an		101000	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
COMPARI		nnn	HI.	GH			
						•	
EXAMPLE			Aloha F		and a second		
- 12 학교 관계로 통하는 것을 같은							
	BF	1999 - 1997 - 19 <b>1</b>		B	etta de la	C	
43 03	02.	A FIEL	D (UA),	B FIELD	(UA),	C FIELD	(UA)
a series and the series of the	en e	in a sta		- 14 A	<ul> <li>The second s</li></ul>		
		0.05			<b>D T N</b> (		-
	BEF		AFTER		BIN	ARY VALU	E
A FIELD	C1C	204	unchange	d 110	000011	0000101	100010
B FIELD	F2		unchange			1100110	
C FIELD	nn	1 S 1 S 1 S 1 S 1	F3F3C4		100111	11100111	100010
COMPARIS			EQUAL				

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BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 295

15.18 LOGICAL NOT (NOT)/OP=44

Format

	+		+-	-	-1		+		+		F
OP	/	\F	1	BF	- [	A	1.	8	1	<b>c</b> 1	
			+ -	-	-+		+		•		ŀ

0P = 44

- AF = Length of the "A" field. AF may be indirect or may indicate the A-syllable is a literal. A value of "00" is equal to a length of 100 units.
- BF = Length of the "B" field. BF may be indirect. A value of "00" is equal to a length of 100 units.
  - A = Address of the "A" source field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
  - B = Address of the "B" source field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
  - C = Address of the result field. Address may be indexed, indirect or extended. The final address controller data type may be UN or UA and must be the same as the other address controller data types.
- Note: If the data types are not all UA or not all UN, cause an Invalid Instruction fault (IEX = 03). See Appendix A - Compatibility Notes (A.11.1).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 296 

15.18 LOGICAL NOT (NOT)/OP=44 (Continued)

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Function

The Logical Not instruction stores the modulo two sum (Exclusive OR) of two data fields (A & B), located in memory, into a third memory location (C).

The "C" field length is equal to the larger of AF or BF. If the "A" and "B" fields are not of equal length, pad the shorter by adding trailing characters/digits of all "one" bits.

Comparison Flags

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Set the Comparison Flags to set HIGH if the least significant bit of the result is a "one"; otherwise, set them to EQUAL.

Overlap

Total overlap or matching type-address overlap of any of the fields is allowed. Partial overlap of "A" or "B" with "C" other than matching type-address overlap may produce incompatible results. See Appendix A - Compatibility Notes (A.11.2).

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					· · · · · · · · · · · · · · · · · · ·	
15.18	LOGICAL NOT (NOT	)/OP=44	(Continued)			
	Examples					
•	EXAMPLE (1)	Exclusiv Function	e OR of Two N	umeric	Fields	
	OP AF BF	A	8		c	
	44 03 03	, A FIELD	(UN), B FIELD	(UN),	C FIELD	(UN)
		BEFORE	AFTER	BINARY	VALUE	
	A FIELD	FFF	unchanged		111111	
	B FIELD C FIELD	6A1 nnn	unchanged 95E	011010 100101		
1 s.	•			100101	011110	
	COMPARISON	nnn	EQUAL			
•			· · · ·	•		
	EXAMPLE (2)	Exclusiv	e OR of Two A	lpha Fi	elas	
·	OP AF BF	A	В		C	
	<u> </u>	A FTFLD	(UA), B FIELD	(liA).	C FTFID	(114.)
					• • • • • • •	
		BEFORE	AFTER	BINARY	VALUE	
	A FIELD	5050	unchanged	010100	00010100	00
	B FIELD	C7D7	unchanged	110001	11110101	11
	C FIELD	nnnn	9787	100101	11100001	11
	COMPARISON	nnn	HIGH			

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COMPANY CONFIDENTIALSYSTEM16INPUT/OUTPUT16.1INITIATE I/O (IIOFormat10P   AF   BF  10P   AF   BF  10P = 94AF = AF may be spif the I/Ogreater thanis unused.BF = Channel numbA = Address of Iindirect orignored. The	)/OP=94 + A   + ecified as i descriptor		REV. A	PAGE 298
16.1 INITIATE I/O (IIO Format I OP   AF   BF   Format OP = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	+ A   + ecified as i descriptor			
16.1 INITIATE I/O (IIO Format I OP   AF   BF   Format OP = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	+ A   + ecified as i descriptor			
16.1 INITIATE I/O (IIO Format I OP   AF   BF   OP = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	+ A   + ecified as i descriptor			
Format I OP   AF   BF   H OP = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	+ A   + ecified as i descriptor			
<pre> I OP   AF   BF   I OP   AF   BF   OP = 94  AF = AF may be sp if the I/0 greater than is unused.  BF = Channel numb A = Address of I indirect or</pre>	ecified as i descriptor			
<pre> I OP   AF   BF   I OP   AF   BF   OP = 94 AF = AF may be sp if the I/0 greater than is unused. BF = Channel numb A = Address of I indirect or</pre>	ecified as i descriptor			
OF = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	ecified as i descriptor	ndirect		
OP = 94 AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	ecified as i descriptor	ndinact o		
AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	descriptor	ndiment of		
AF = AF may be sp if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	descriptor	ndiment of		
if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	descriptor	ndirect of		
if the I/O greater than is unused. BF = Channel numb A = Address of I indirect or	descriptor			
A = Address of I indirect or		does not	require a	a length of
indirect or	er. BF may	be indire	ct.	
	extended. Th	e final ad	ddress con	
Function		· · · · · · · · · · · · · · · · · · ·	· · · ·	
The Initiate I/O				
receive an I/O				
route it to the a A - Compatibility				e Appendix channel is
busy, set the Com				
instruction with	no furthe			
Comparison Flags	to EQUAL.	· ·		
The format of the	I/O descrip	tor is as	follows:	
INFORMATI	ON		DIGITS	
ا از می از می از این			•	•••
Opcode Sy			00-05	
A Address			06-15	
B Add <b>re</b> ss C Field			16-25 26-33	•
	ea Status Nu	mber	34-39	
This instruction				

	4	
BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	  - 1997 5390 
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV.	PAGE 299

16.2 READ ADDRESS (RAD)/OP=92

Format

				•	
+	+	+	+		ŀ
OP	AF	BF	1	A I	
+	+	+	+		ŀ

OP = 92

AF = Operation variant. AF may be indirect, but a literal flag will cause an Invalid Instruction fault (IEX = 21). The following variants may be specified after any indirect field length has been resolved.

VARIANT	OPERATION
09	Store the 10 UN contents of memory
	specified by the "A" address int
	both the begin and the end address
A second seco	of the channel specified by BF.
03	Store up to 4 words (16 digits) o
	the extended R/D for the channe
	specified by BF in memory at th
	location specified by the "A
	address. These words will be left
na series de la companya de la compa	justified in a sixteen digit dat
	field.
02	Store the first two words of th
	extended R/D for the channe
	specified by BF in memory at th
	location specified by the "A
	address.
OT	Store the current end address o
	the channel specified by BF i
	memory as a 10 UN field at th
	location specified by the "A
	address.
	Store the current begin address o
	the channel specified by BF i
	memory as a 10 UN field at th
	Location specified by the "A
· · ·	address.
	AAA1 / 448

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PASADENA PLANT	V SERIES INSTRUCTION SET	
		· •
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 300

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#### 16.2 READ ADDRESS (RAD)/OP=92 (Continued)

- BF = Channel number. BF can be indirect. BF can specify any octal value from "00" to "77", or the non octal value "08". Use of other channel numbers will cause an Invalid Instruction fault (IEX = 26).
- A = Address of the memory operand. The address may be indexed, indirect or extended. The final address controller is ignored. The address must be modulo two or cause an Address Error fault (AEX = 03).

# Function

When BF equals a legal octal channel number from "00" to "77", the Read Address instruction causes the processor to read the specified data from an I/O channel address memory and store the value in a memory location (A) or write the value from a memory location (A) into both the begin and end addresses of the associated channel. See Appendix A - Compatibility Notes (A_24).

Examine the specified I/O channel to determine if it is busy with another I/O function. If it is available, the RAD function will be performed and the Comparison Flags set to EQUAL. If the I/O channel is unavailable, the RAD function will not be performed and the Comparison Flags will be set to HIGH.

A RAD to Channel 8 is treated as a no-op.

This instruction may only be executed in Privileged Mode.

BURRCUGHS CORPORATION System development group Pasadena plant	I I I V SERIES INSTRUCTION SET	1997 5390
	DESIGN SPECIFICATION REV. A	PAGE 301

16.3 SCAN RESULT DESCRIPTOR (SRD)/OP=91

Format

+----+ † OP | AFBF | +----+

0P = 91

AFBF = Low order four digits of an absolute address in memory. The high order three digits are assumed to be zero. Indirect Field Lengths may be specified.

Function

If the resolved "AFBF" is equal to zero, set the Comparison Flags to EQUAL, and terminate the instruction without changing index register one (IX1).

If the resolved "AFBF" is non-zero, then the address formed from the "AFBF" is assumed to point to a sixteen bit result descriptor area. Examine the first bit of this area.

- 1. If it is equal to zero (no result descriptor present), examine the four digits (link address) immediately following the descriptor area.
  - A. If they are equal to "0000", set the Comparison Flags to EQUAL and terminate the instruction (no descriptor found).
  - B. If they are not equal to zero, they replace the original address value and the operation is repeated. The link addresses are assumed to be absolute addresses.
- 2. If it is equal to one (result descriptor present), store a sign and Base Indicant character of "C7" and six digits of the absolute address of the descriptor area into index register one (IX1).

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PASADENA PLANT	V SERIES INSTRUCTION S	ET

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 302 _____ _____

16.3

SCAN RESULT DESCRIPTOR (SRD)/OP=91 (Continued)

----

Examine the next bit. Set the Comparison Flags to HIGH if it is a zero; otherwise, set them to LOW and terminate the instruction.

----

Undigits in the resolved AFBF or in the link addresses will cause an Address Error fault (AEX = 42). See Appendix A - Compatibility Notes (A.23)

This instruction may only be executed in Privileged Mode.

Comparison Flags 

See functional description for details.

Overlap -----

There are no overlap cases for this instruction.

			+	
	CORPORATION ELOPMENT GROUP	+		1997 5390
PASADENA PL		V SERIES INSTRUCT	ION SET	
COMPANY CON	FIDENTIAL SYSTEM	DESIGN SPECIFICATION	REV. A	PAGE 303
16_4	CONVERT I/O (CIO)/	0P=85		
	Format			
	***			
	<b>*</b> ~~~*~~~*~~~*~~			
	OP AF BF			
	<b>*</b> +++	++		
	0P = 85			
· ·				•
		served. May be speci		
		• A literal flag wi ault (IEX = 21).	ll cause a	n Invalid
	Instruction i			
· ·		served, but may be	specifie	d as an
	indirect fiel	d length.		
· •	A = Address of th	e initial descriptor.	Address	may be
		rect or extended.		
	controller m Instruction f	ust specify UN or	cause an	Invalid
		e resultant descripto		
		rect or extended.		
		ust specify UN or ault (IEX = 03).	cause an	Invalid
	The format of	the initial descript	or is as f	ollows:
	INFORMATIO	N	DIGITS	·
	Opcode Syl	lahla	00-05	
	Environmen		06-11	
· .	Memory Are		12-13	
		s (Convert)	14-19	
1997 - A.	"B" Addres "C" Field	s (Convert)	20-25 26-33	
	U TIELU		20 33	
. • .	Note - The Lo	west memory address =	00	

BURROUGHS CORPORATION		++ 1997 5390
SYSTEM DEVELOPMENT GR Pasadena plant	OUP	V SERIES INSTRUCTION SET
COMPANY CONFIDENTIAL	SYSTEM	DESIGN SPECIFICATION REV. A PAGE 304

## 16.4 CONVERT I/O (CIO)/OP=85 (Continued)

The format of the resultant descriptor is as follows:

INFORMATION		DIGITS
Opcode Syllable		00-05
A Address		06-15
B Address		16-25
C Field	с	26-33
Memory Area Status	s Number	34-39

## Function

This instruction converts the relative addresses in the initial descriptor to absolute addresses in the resultant descriptor, verifies that an I/O can be initiated to the specified memory area, and increments the "Number of I/O's in Process" field for that memory area in the Memory Area Status Table.

The initial descriptor (A) is read from memory. If the I/O descriptor "A" and "B" addresses are not mod 2 or contain undigits, or if the "A" address is not less than the "B" address, cause an Address Error fault (AEX = O1) and terminate the instruction with no further action.

Locate and resolve the Memory Area Table (MAT) entry pointed to by the Environment Number and Memory Area Number in the initial descriptor (A). If the resolved MAT entry is a Memory Area Fault Entry, then cause a Hard Memory Area Fault and terminate the instruction. Otherwise, if the resolved MAT entry is not an Original Entry, then cause an Address Error Fault (AEX = 04) and terminate the instruction. Add the base value in the resolved MAT entry to the initial descriptor "A" and "B" addresses and store them in the resultant descriptor "A" and "B" addresses. If the addresses are greater than the associated limit value, cause an Address Error fault (AEX = 24) and terminate the instruction with no further action.



## 16.4 CONVERT I/O (CIO)/OP=85 (Continued)

Move the initial descriptor Opcode Syllable and "C" field to the resultant descriptor. Move the Memory Area Status Table (MAST) Number from the resolved MAT entry to the resultant descriptor. Then use the MAST number as an array subscript into the Memory Area Status Table to locate the MAST entry associated with this memory area. Examine the Status digit of this Memory Area Status Table entry. If the Inhibited I/O Memory Area flag is set, set the Comparison Flags to LOW and terminate the instruction with no further action.

If the Inhibited I/O Memory Area flag is reset, increment the "Number of I/O's in Process" field in the Memory Area Status Table entry. If the result overflows the field, cause an Invalid Instruction fault (IEX = 05) and terminate the instruction with no further action. If no overflow, store the incremented number back in the field and set the comparison flags to EQUAL.

This instruction may only be executed in Privileged Mode.

	CORPORATION ELOPMENT GROUP ANT	+     V SERIES INSTRU	+ 1997 5390 CTION SET
COMPANY CO	NFIDENTIAL SYSTEM D	ESIGN SPECIFICATIO	N REV. A PAGE 300
16.5	I/O COMPLETE (IOC)/	0P=98	
	Format		
	++++   OP   AF   BF   ++++	A B B B	
	OP = 98		
	AF = A length of si an indirect fi		
	length. BF c "77" or the no	an specify any oct n-octal value "08" rs will cause a	an indirect field al value from "00" to . Use of any othe n Invalid Instruction
	Number. Add extended. The	ress may be i final address con	Area Status Table ndexed, indirect of troller must specify on fault (IEX = 03).
	may be index address contr		

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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE ³⁰⁷

16.5 I/O COMPLETE (IOC)/OP=98 (Continued)

Function

The I/O Complete instruction stores the unsigned difference between the I/O buffer begin and end address registers for the specified channel (BF) in memory (B). (The begin address will have been incremented during the I/O operation to show the number of bytes transferred.) This instruction examines the specified Memory Area Status Table entry (A), decrements the "I/Os in Process" field and sets the comparison flags accordingly.

1. If the I/O Channel is busy, set the Comparison Flags to HIGH and terminate the instruction with no further action.

If the I/O Channel is not busy, continue as follows. If the specified channel number is the octal value OO to 77, using the specified channel number, store the difference between the end address and the begin address at the specified memory location (B) If the specified channel number is the non-octal value O8, store zero at the specified memory location (B).

- 2. Use the Memory Area Status Table Number (A) as an array subscript into the Memory Area Status Table to locate the specified entry (See Section 5.6). If the Memory Area Status Table Number (A) is invalid (undigits), cause an Address Error fault (AEX = 34) and terminate the instruction with no further action.
- 3. Examine the "Number of I/0"s in Process" field located in the Memory Area Status Table entry. If it is equal to zero, cause an Invalid Instruction fault (IEX = 05) and terminate the instruction with no further action. Otherwise, decrement the value of this field by one and store the result in the "Number of I/0"s in Process" field of the specified MAST entry.

BURRCUGHS CORPORATION Bystem development group	↓ ++	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYST	EM DESIGN SPECIFICATION REV. A	PAGE 308

## 16.5 I/O COMPLETE (IOC)/OP=98 (Continued)

4. If the value of the "Number of I/O's in Process" field is now equal to zero, examine the Status digit of the Memory Area Status Table entry. If the Inhibited I/O Memory Area flag is set, set the Comparison Flags to LOW and terminate the instruction.

If the Inhibited I/O Memory Area flag is reset or if the value of the "Number of I/O's in Process" field is not equal to zero, set the Comparison Flags to EQUAL and terminate the instruction.

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This instruction may only be executed in Privileged Mode.

SYSTEM DEVI Pasadena pi	CORPORATION ELOPMENT GROUP LANT NFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 309
17	BINARY/DECIMAL CONVERSION
17.1	DECIMAL TO BINARY (D2B)/CP=88
· .	Format 
	++   OP   AF   BF   A   B   ++
	OP = 88
	AF = Length of the source data field. Value may be indirect or a literal. A length of of "OO" is equal to a length of 100.
	BF = Length of the destination data field in units consisting of four binary bits each. Value may be indirect. A value of "00" is equal to a length of 100 units.

- A = Address of the decimal source data field. Address may be indirect, indexed or extended. The final address controller may be UN or UA. When the final controller is UA, the zone digits will be ignored. The final address controller must specify UN or UA or cause an Invalid Instruction fault (IEX = 03). Undigits in this field will cause an Invalid Arithmetic Data fault.
- B = Address of the binary destination data field. Address may be indirect, indexed or extended. The final address controller must specify UN or cause an Invalid Instruction fault (IEX = 03).

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17.1

DECIMAL TO BINARY (D2B)/OP=88 (Continued)

Function

The decimal to binary instruction will read a decimal data field from a memory location (A), convert the entire value to a binary representation and store the binary value in a second memory location (B).

If the converted data length is less than the destination data field (BF), store the converted data "Right Justified" with leading zeros.

If the converted value exceeds the length of the destination data field (BF), set the Overflow and terminate the instruction without storing the result.

Comparison Flags

Set the Comparison Flags to EQUAL if the source data field is equal to zero, otherwise, set them to "HIGH".

Overlap

This instruction has no overlap restrictions.

EXAMPLE: (1) Decimal to Binary

OP	AF	BF	<b>. . .</b>		B	
88	03	02	A FIELD	(UN)	B. FIELD	(UN)
				BE	FORE	AFTER
	IELD IELD		e of an fer and other definition		174 nn	unchanged AE
	PARI Rflo				nn nn	HIGH unchanged

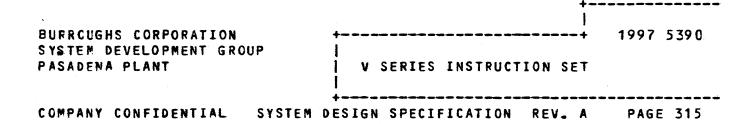
STEM C	HS CORPORATIO Development G A plant		+-	V SERIE:	S INSTRUCTION	+ 1997 5390 SET
MPANY	CONFIDENTIAL	SYSTE	+- M DES	IGN SPEC	LFICATION RE	V. A PAGE 311
17.1	DECIMAL	TO BINAF	Y CD2	8)/0P=88	(Continued)	
	EXAMPLE:	(2) Dec	imal	to Binary	/ - Overflow	Condition
		OP AF	BF	A	B	
		88 03	02	A FIELD	(UN) B FIEL	D (UN)
					BEFORE	AFTER
		A FIEL B FIEL		. <b>.</b> .	374 nn	unchanged unchanged
		COMPAR Overfl			nnn	HIGH ON
	EXAMPLE:	(3) Dec	imal	to Binary	- Mixed Con	trollers
		OP AF	BF	A	8	
	•	88 03	03	A FIELD	(UA) B FIEL	D (UN)

BEFOREAFTERA FIELDF1F7F4unchangedB FIELDnnnOAECOMPARISONnnnHIGHOVERFLOWnnnunchanged

BURRCUGHS CO System devel Pasadena pla	OPMENT GROUP	V SERIES INSTRUCTION SE	1 + 1997 539 T
COMPANY CONI	FIDENTIAL SYSTEM D	ESIGN SPECIFICATION REV.	A PAGE 31
17-2	BINARY TO DECIMAL C	B2D)/OP=89	
	Format		
	OP   AF   BF	A A B B B B A A	
	0P = 89		
	binary bits	source data field in un each. Value may be in ue of "00" is equal to a l	direct or
		destination data field. V value of "00" is equal t	
	be indirect, controller mu	binary source data field. indexed or extended. The st specify UN or cause ult (IEX = 03).	final addres
	Address may final address final control The final addr	he decimal destination be indirect, indexed or controller may be UN or U ler is UA, F zones will ess controller must specif id Instruction fault (IEX	extended_ Th A_ When th be inserted y UN or UA o
	Function		
	field from a memory	al instruction will read a location (A), convert the entation and store the dec ation (B).	entire valu
		ta length is less than the , store the converted ding zeros.	
•			

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PASADENA P	LANT			1	VS	SERIE	SINST	RUCTIO	N SET	
COMPANY CO	NFIDENTIAL	SY	STEM	DES	IGN	SPEC	FICAT	ION RI	EV. A	PAGE 313
•	. *									
17.2	BINARY T	) DEC	IMAL	(82	D)/(	)P=89	(Con	tinued	)	
		ion (	data	fi	eld.	(BF)	, se	t the (	verflow	of the Flag and alt.
	Comparis	on Fla	ags							
	Set the is equal									ata field
	Overlap									
	This inst EXAMPLE:						•	trictio	ons.	
	14 - 1 1	OP	AF	8 F		A		1	3	
	٥	89	02	03						
				0.0	A I	IELD	(UN)	8 FIE	D (UN)	
			ŪĽ	<b>ر</b> ال	~ 1	IELD	(UN) Befori		.D (UN) After	t
			IELD IELD		~ 7	IELD				ged
	•	B F	IELD	SON	^ <b>r</b>	IELD	BEFORI		A FTER unchang	ged I
		B F	IELD IELD Pari:	SON	A 7	IELD	BEFORI AE nnn nnn		AFTER unchang 174 HIGH	ged I
	•	B F	IELD IELD Pari:	SON		IELD	BEFORI AE nnn nnn		AFTER unchang 174 HIGH	ged I
		B F	IELD IELD Pari:	SON	<u> </u>	IELD	BEFORI AE nnn nnn		AFTER unchang 174 HIGH	ged I
		B F	IELD IELD Pari:	SON		IELD	BEFORI AE nnn nnn		AFTER unchang 174 HIGH	ged I
· · · · · · · · · · · · · · · · · · ·		B F	IELD IELD Pari:	SON		IELD	BEFORI AE nnn nnn		AFTER unchang 174 HIGH	ged I

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L SYSTEM I	DESIGN SPECIFICA	TION REV. A	PAGE 314
TO DECIMAL	(B2D)/0P=89 (Cc	intinued)	
• (2) Binar	v to Decimal - 0	verflow Condit	ion
A ETEIN			
8 FIELD			
		ON	
LOMPARIS		<b>U</b> 194	
: (3) Binar	y to Decimal - Z	ero Source Dat	9
OP AF I	BFA	<b>B</b>	
88 12	OT A FIELD (UN)	B FIELD (UN)	
	BEFOR	E AFTE	R
A FIELD B FIELD	0000000 n	)0000 unchan O	ged
OVERFLOW	n († 1997) 1997 - State State († 1997) 1997 - State State († 1997)	n unchan	ged
e: (4) Binary	y to Decimal – M	ixed Controlle	r s.
BF	8		
03 A FIEL	Ø (UN) B FIELD	CUA)	
	EFORE	TER	
			3
la de la companya de			
	GROUP L SYSTEM TO DECIMAL : (2) Binar OP AF 88 O2 A FIELD OVERFLOW COMPARIS : (3) Binar OP AF 88 T2 A FIELD B FIELD COMPARIS OVERFLOW : (4) Binar BF A O3 A FIEL B	GROUP V SERIES INS L SYSTEM DESIGN SPECIFICA TO DECIMAL (B2D)/OP=89 (CC C(2) Binary to Decimal - 0 OP AF BF A 88 02 02 A FIELD (UN) BEFORE A FIELD AE B FIELD AE B FIELD Nn OVERFLOW NN COMPARISON NN COMPARISON NN BEFOR A FIELD CUN B FIELD N COMPARISON NN COMPARISON NN COMP	GROUP V SERIES INSTRUCTION SET SYSTEM DESIGN SPECIFICATION REV. A TO DECIMAL (B2D)/OP=89 (Continued) C (2) Binary to Decimal - Overflow Condit OP AF BF A B 88 02 02 A FIELD (UN) B FIELD (UN) BEFORE AFTER A FIELD AE unchanged OVERFLOW nnn ON COMPARISON nnn HIGH COMPARISON nnn HIGH COMPARISON nnn AIGH B FIELD CUN) B FIELD (UN) BEFORE AFTE A FIELD COOCOOOOOOO unchan B FIELD N OOOOOOOOOO unchan COMPARISON nnn EQUAL OVERFLOW nnn ON COMPARISON NNN B FIELD (UN) BEFORE AFTE A FIELD COOOOOOOOOO unchan COMPARISON NNN EQUAL OVERFLOW NNN EQUAL OVERFLOW NNN EQUAL BEFORE AFTE A FIELD COOOOOOOOOOO Unchan B FIELD COOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO



18 TIME-OF-DAY TIMER

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These instructions concern the operation of the time-of-day timer. The time-of-day timer is a twenty digit counter that counts up at a one microsecond rate. See Appendix A - Compatibility Notes (A.36).

The time-of-day timer has the following format:

INFORMATION	DIGITS		
Year .	00 - 03		
Month	04 - 05		
Day	06 - 07		
Reserved	08		
Microseconds	09 - 19		

Note - The lowest memory address = 00

The time-of-day timer is set (OP = 97) once as a privileged instruction. It may be read (OP = 95) by any user that requires the time-of-day.

At midnight, software will initialize the day, month, year, and microseconds via the STT instruction.

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BURROUGHS C System deve Asadena pl	LOPMENT GROUP
COMPANY CON	FIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 310
1	
18.1	READ TIME of DAY (RDT)/OP=95
	Format
an an ann an Airtean Airtean Airte	
	++   OP   AF   BF   A   ++
• * ** ********************************	OP = 95
ر با با بار ۲۰ همین از بار ۱۹ همان ۲۰ میلود با	<pre>AF = Unused &amp; reserved, but may be specified as an indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21).</pre>
	BF = Unused & reserved, but may be specified as an indirect field length.
	A = Address of the memory location where the twenty digit timer value is to be stored. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).
	Function
	The Read Time of Day instruction will store the twenty digit time-of-day timer at the memory location specified by the "A" address.
	See Appendix A - Compatibility Notes (A.24).
	Comparison FLags
in the second	Not changed.
	Overlap
· .	There are no overlap cases in this instruction.

BURROUGHS CORPORATION System development group	 ++ 	1997 5390
PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 317

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18.2

SET TIME of DAY (STT)/0P=97

Format

ŧ	•					-+			+-	 	 -4	F
1		0P	- 1	Ŀ	AF	: I	В	F	Ľ	A	1	
4	-	-	-4		-	-+			+-	 	 - 4	Ŀ.

0P = 97

- AF = Unused & reserved, but may be specified as an indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21).
- BF = Unused & reserved, but may be specified as an indirect field length.
- A = Address of the memory location where the twenty digit timer value is stored. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

Function

The Set Time of Day instruction will load the time of day timer with the twenty digit value located in memory at "A". If the value is invalid (undigits), cause an Invalid Instruction fault (IXE = 07) and terminate the instruction.

This instruction may only be executed in Privileged Mode.

See Appendix A - Compatibility Notes (A.24).

Comparison Flags

Not changed.

Overlap

There are no overlap cases in this instruction.

SYSTEM DEVEL Pasadena pla	OPMENT GROUP	V SERIES INSTRUCTION SE	a ang ang ang ang ang ang ang ang ang an
PROAVENA PLA		I V SERIES INSTRUCTION SE	

OMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 318

19 MEASUREMENT

전 물건가 물건을 잡고 있는 것이다. 같은 것을 물건하고 있는 것이다. 같은 것은 것을 같은 것은 것이다.

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The Measurement register is an eight digit register with outputs that are made available as external outputs of the processor so that they may be monitored by various hardware monitoring devices.

The format of the Measurement register is:

مانه المروي هو محمد مراجع	and a second	n an anna a' galais ann an
•	INFORMATION	DIGITS
an an ann an Anna an A Anna an Anna an	User	00-05
•	Name	06-07

Note - The Lowest memory address = 00

and the second second

The MOPOK signal, available externally, will be held to "zero" at any time that the Measurement register is being changed and held to a "one" at all other times.

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BURRCUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 319

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19.1 MEASUREMENT OF (MOP)/OP=87

Format

0P = 87

AF = A length of six (6) must be specified directly or as an indirect field length or a literal.

- BF = A length of six (6) must be specified directly or as an indirect field length.
- A = Address of the Setting field. Address may be indexed indirect or extended. The final address controller controller must equal UN or cause an Invalid Instruction fault (IEX = 03).
- B = Address of the Mask field. Address may be indexed indirect or extended. The final address controller controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 320

19_1

MEASUREMENT OP (MOP)/OP=87 (Continued)

Function

The Measurement instruction is used to load the User portion of the Measurement register. The Measurement register is an eight digit register with outputs that are made available as external outputs of the processor so that they may be monitored by various hardware monitoring devices.

The six digit Mask field will be read from a memory Location (B) and used to determine which bits in the Measurement register are capable of being changed by the Setting field which is also located in memory (A).

Each bit in the Mask field that is equal to a "one" will permit the corresponding bit in the Measurement register User field to assume the state of the corresponding bit in the Setting Field (A).

Each bit in the Mask field that is equal to a "zero" will prevent changes to the corresponding bit in the Measurement register User field.

The MOPOK signal, available externally, will be held to "zero" at any time that the Measurement register is being changed and held to a "one" at all other times.

The Measurement register is changed by the Virtual Branch Reinstate (OP = 93), Branch Communicate (OP = 30), Hyper Call (OP = 62), and Return (OP = 63) instructions. It is also changed by the Interrupt and Hardware Call procedures.

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C C M P A N Y	CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 321
20	MISCELLANEOUS
	These instructions facilitate the implementation of the V-Series operating system.
20-1	ALTER TABLE ENTRY (ATE)/OP=86
	Format
	++++++
	OF LAF BF LA B
	0P = 86
•	AF = Unused & reserved, but may be specified as an indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21).
	BF = Variant, may be specified as an indirect field length.
	BF = QO marks the selected Memory Area Table entry as Unused.
	BF = 01 performs a copy of a Memory Area Table entry.
	BF = 02 alters the task's Environment Table entry.
	BF = 03 alters the task's Memory Area Table entry.
	BF = 04 signals the processor that a Memory Area Table entry was modified by a non-ATE instruction.
	The use of all other BF values is reserved and will cause an Invalid Instruction fault (IEX = 26).
	A = Address of the source operand. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

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COMPANY CONFIDENTIAL	SYSTEM	DESIGN	SPECIF	ICATION	REV. A	PAGE	322
							****

2C.1 ALTER TABLE ENTRY (ATE)/OP=86 (Continued)

When BF = 00 or BF = 04, this operand is unused. However, this address must still have valid address syllable attributes.

_____

B = Address of the destination operand. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

When BF = 04, this operand is unused. However, this address must still have valid address syllable • attributes. .

• '

BURROUGHS CORFORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 323

2C.1 ALTER TABLE ENTRY (ATE)/OP=86 (Continued)

Function

## BF = 00 WRITE UNUSED MEMORY AREA TABLE ENTRY

The Write Unused Memory Area Table entry variant is used to store an Unused Entry in the Memory Area Table entry specified by the Environment Number and the Memory Area Number found in the destination operand (B).

The eight digit destination operand contains the following information which is necessary to locate the desired Memory Area Table Entry.

INFORMATION	•	DIGITS
Environment	Number	00-05
Memory Area	Number	06-07

Note - The lowest memory address = 00

If the Destination Write Enable bit in the Environment Table entry associated with the destination operand is set, the destination entry is located using the Environment Number and the Memory Area Number found in the destination operand (B). Otherwise, cause an Invalid Instruction fault (IEX = 36) and terminate the instruction with no further action.

If the Type digit of the destination entry is an Original Entry or a Memory Area Fault Entry, cause an Invalid Instruction fault (IEX = 35) and terminate the instruction with no further action. Otherwise, write an Unused Entry in the specified destination.

Reload the current Memory Area Table using the Active Environment Number.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 324

## 20_1 ALTER TABLE ENTRY (ATE)/OP=86 (Continued)

BF = 01 COPY MEMORY AREA TABLE ENTRY

The Copy Memory Area Table entry variant is used to generate a copy of the source Memory Area Table entry specified by the Environment Number and the Memory Area Number found in the source operand (A) and store the copy in the destination entry location specified by the Environment Number and the Memory Area Number found in the destination operand (B).

Each eight digit operand contains the following information which is necessary to locate the desired Memory Area Table Entry.

INFORMATION		DIGITS
	and the second states and	
Environment	Number	00-05
Memory Area	Number	06-07

Note - The lowest memory address = 00

The following operations are performed by this variant:

- Resolve the destination Memory Area Table entry specified by the Environment Number and the Memory Area Number contained in the destination operand (B). If the Type digit of the resolved destination entry is an Original entry or a Memory Area Fault entry, cause an Invalid Instruction fault (IEX = 35) and terminate the instruction with no further action.
- 2. Resolve the source MAT entry specified by the Environment Number and the Memory Area Number found in the source operand (A). If either the Source Copy Enable bit in the Environment Table entry associated with the source operand or the Destination Write Enable bit in the Environment Table entry associated with the destination operand is not set, cause an Invalid Instruction fault (IEX = 36) and terminate the instruction with no further action.

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COMPANY CO	NFIDENTIAL SYST	EM DESIGN SPEC	IFICATION REV_ A	PAGE 325
20.1	ALTER TABLE ENT	RY (ATE)/OP=86	(Continued)	
	3. If the res	olved sourced	MAT entry belong	s to the

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- current task, then store a "C" Copy descriptor which points to that resolved source MAT entry.
  - If the resolved source MAT entry belongs to another task, then store an "E" Copy descriptor entry, which points to that resolved source MAT entry.

4. Reload the current Memory Area Table using the Active Environment Number.

. . . .

20.1 ALTER TABLE ENTRY (ATE BF = 02 ALTER TASK'S ENT The Alter Task's Envir to alter an existing Environment to) the Environment operand (A). The source operand (A) INFORMATION Environment Nur Task Number The destination operan INFORMATION Environment Nur The destination Envir non-zero value. The valid MCP or USER Envir Number must be a decim The following operatio 1. Locate the source Task number, cont	NVIRONMENT TABLE ENTRY onment Table Entry variant is used nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
20.1 ALTER TABLE ENTRY (ATE BF = 02 ALTER TASK'S ENT The Alter Task's Envir to alter an existing E the destination operant to) the Environment operand (A). The source operand (A) INFORMATION Environment Nur Task Number The destination operant INFORMATION Environment Nur The destination Envir non-zero value. The valid MCP or USER Envir Number must be a decim The following operatio 1. Locate the source Task number, cont	0/OP=86 (Continued) NVIRONMENT TABLE ENTRY onment Table Entry variant is used nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
BF = 02 ALTER TASK'S EN The Alter Task's Envir to alter an existing E the destination operan to) the Environment operand (A). The source operand (A) INFORMATION Environment Nur Task Number The destination operan INFORMATION Environment Nur The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	NVIRONMENT TABLE ENTRY onment Table Entry variant is used nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
BF = 02 ALTER TASK'S E The Alter Task's Envir to alter an existing E the destination operant to) the Environment operand (A). The source operand (A) INFORMATION Environment Nur Task Number The destination operan INFORMATION Environment Nur The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	NVIRONMENT TABLE ENTRY onment Table Entry variant is used nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
The Alter Task's Envir to alter an existing E the destination operan to) the Environment operand (A). The source operand (A) INFORMATION Environment Nur Task Number The destination operan INFORMATION Environment Nur The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	onment Table Entry variant is used nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
to alter an existing E the destination operan to) the Environment operand (A). The source operand (A) INFORMATION Environment Nu Task Number The destination operan INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	nvironment Table entry, specified by d (B), to be a copy of (identical Table entry specified by the source format is: OFFSET mber 00 - 05 06 - 09 d (B) format is: OFFSET
INFORMATION Environment Nu Task Number The destination operan INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	0FFSET mber 00 - 05 06 - 09 d (B) format is: 0FFSET
Environment Nu Task Number The destination operan INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	mber 00 - 05 06 - 09 d (B) format is: OfFSET
Task Number The destination operan INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	06 - 09 d (B) format is: OfFSET
Task Number The destination operan INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	06 - 09 d (B) format is: OfFSET
INFORMATION Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	OFFSET
Environment Nu The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	
The destination Envir non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	
non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	mber 00 - 05
non-zero value. The valid MCP or USER Envi Number must be a decim The following operatio 1. Locate the source Task number, cont	onnant Number suct he a deciral
1. Locate the source Task number, cont	source Environment Number must be a ronment Number. The source Task
Task number, cont	ns are performed by this variant:
	Reinstate List entry by using the ained within the source operand (A), ript into the Reinstate List.
	Environment Table by using the
	address contained within the source try. Use the Environment Number
	the source operand (A) as an array
subscript into th	is Environment Table. If the source
	er is greater than the Number of
	nment Table field, contained within 's Reinstate List Entry, cause an
	lt (AEX = 57) and terminate the
instruction with	
·	no further action.

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DESIGN SPECIFICATION REV.	A PAGE 327
	V SERIES INSTRUCTION SE DESIGN SPECIFICATION REV.

#### 20.1

#### ALTER TABLE ENTRY (ATE)/OP=86 (Continued)

- 3. Locate the destination entry using the Environment Number contained in the destination operand (B) as an array subscript into the appropriate Environment Table. If the first digit of the Environment Number is equal to "0 - 9", this six digit number represents an array subscript into the current User Environment Table of 000000 to 999999. If the Environment Number is equal to or greater than the value of the Number of Entries in the USER Environment Table field (located in the Reinstate List Entry for this Task), cause an Address Error fault (AEX = 57) and terminate the instruction with no further action.
  - If the first digit of the Environment Table is not "0-9", cause Address Error (AEX = 52) and terminate the instruction with no further action.
- 4. Copy the contents of the source Environment Table entry to the destination Environment Table entry.
- 5. Reload the current Memory Area Table using the Active Environment Number.

For proper operation of this variant the following points must be followed. However, these points are not enforced by the hardware.

- 1. The destination EN must never be equal to the currently active EN.
- 2. The source MAT (pointed to by the EN/Task number pair) can never contain copy descriptors because these copy descriptors will not resolve correctly. Any pointers that may be affected by this instruction must be recalculated.

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SYSTEM DEVELOPMENT GROUP Pasadena plant	V SERIES INSTRUCTION SET	

#### 20.1 ALTER TABLE ENTRY (ATE)/0P=86 (Continued)

_____

BF = 03 COPY ALTERNATE TASK'S MEMORY AREA TABLE ENTRY

The Copy Alternate Task's Memory Area Table entry variant is used to generate a copy of the source Nemory Area Table entry, specified by the source operand (A) and store the copy in the current task's destination operand (B). The format of the source and destination operands are defined below.

The source operands (A) format is as follows:

	Information		•	Offset
and a second second Second second	Environment	Number		00 - 05
	Memory Area	Number		06 - 07
	Task Number		1	08 - 11

The destination operands (B) format is (The format is identical to BF = 01 variant of the ATE source and destination operands): 

Information	0	ffset
مرد به در معروفه است. مرد است استوفاع است که در م	and the second	
Environment	Number	00 - 05
Memory Area	Number	06 - 07

The following operations are performed by this variant:

- 1. Locate and resolve the destination MAT entry using the Environment Number and the Memory Area Number contained in the destination operand (B).
  - 2. If the Type digit of the destination entry is an Original Entry or a Memory Area Fault Entry, cause an Invalid Instruction fault (IEX = 35) and terminate the instruction with no further action.

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BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 329

- 20.1 ALTER TABLE ENTRY (ATE)/OP=86 (Continued)
  - 3. Locate and resolve the source MAT entry using the Task Number, Environment Number, and Memory Area Number contained in source operand (A).

- 4. If either the Source Copy Enable bit in the Environment Table entry associated with the resolved source entry OR the Destination Write Enable bit in the Environment Table entry associated with the destination operand are NOT SET, cause an Invalid Instruction fault (IEX = 36) and terminate the instruction with no further action.
- 5. Store an "E" Copy Type Entry, containing the absolute address of the resolved source entry (A), into the destination entry (B).
- 6. Use the Active Environment Number to reload the current Memory Area Table from memory using the Active Environment Number.

BF = 04 NOTIFICATION OF MAT MODIFICATION BY NON-ATE INSTRUCTION

This variant performs no significant operation other than to notify the processor that a Memory Area Table Entry was changed by an instruction other than an ATE instruction.

It is necessary for those processors which cache Memory Area Base/Limit pairs to always be notified by some sort of ATE instruction when a MAT entry is modified.

This instruction may only be executed in Privileged Mode.

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OMPANY CONFID	ENTIAL SYSTEM D	ESIGN SPECIFIC	TION REV_	PAGE 33
20.2 LO	AD INDEX REGISTER	S (LIX)/0P=67		
Fo	rmat			
م <del>یر</del> این این ا این از این				
	+++ OP   AF   BF	-		
•		•		• •
0.P	= 67		n Alexandria Alexandria	
	= Unused. AF may			
میں بار کی جارت ہوئے۔ 1995ء - میں میں میں میں میں میں میں میں اور	cause an Inval	id Instruction	fault (IEC =	= 21).
BF	= Load Variant a	ind may be spe The variants		
		Length has be		
	The least sign			
	the insert of as follows:	f a Base Indica	int value in	to the resul
	VARIANT		BFL	
		int Value #7	7	
		int Value #6 int Value #5	6	
	Base Indica	int Value #4	4	
	Base Indica Base Indica		3	
		int Value #1	1	
		icant Value	0	
	The use of all	other BFL val	es is reserv	ed and wil
	cause an Inval	id Instruction	fault (IEX =	
an an daring sa sayan an Arten Antari ang sa sayan ang sang sa sayan ang sang sa sayan sa sayan sa sayan sa sa Antari ang sang sa sang sa sayan sa sang sa sayan sa	a da de la composición de la composició La composición de la c	e en ar denna de la composición de la c La composición de la c		
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BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 331

# 20.2 LOAD INDEX REGISTERS (LIX)/OP=67 (Continued)

The most significant digit of the BF field specifies the Index Register to be loaded as follows:

VARIANT			BFM	
Load Index	Register	#7		7
Load Index	Register	#6		6
Load Index	Register	#5		-5
Load Index	Register	#4		4
Load Index	Register	#3		3
Load Index	Register	#2		2
Load Index	Register	#1		1
Load Mobil	Index Reg	gisters	(4)	0

The use of all other BFM values is reserved and will cause an Invalid Instruction fault (IEX = 26).

A = Address of the Index Register field. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

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BURROUGHS CORPORATION	++	1997 5390
SYSTEM DEVELOPMENT GROUP Pasacena plant	V SERIES INSTRUCTION SET	
COMPANY CONFIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A	PAGE 332

20.2 LOAD INDEX REGISTERS (LIX)/OP=67 (Continued)

Function

The Load Index Register instruction provides the memory address (A) of the starting location of either an eight digit field that contains the value that is to be loaded into the specified Index Register (BFM) or the starting location of a 32-digit field that contains the values that are to be loaded into the four Mobile Index Registers (IX4, IX5, IX6 & IX7).

Each eight digits represents an index register of the following format:

INFORM	DIGITS	
Sign		00
Base	Indicant	01
Addres	5S	02-07

Note - The lowest memory address = 00

If the load variant (BFM) specifies the load of a single register and if a Base Indicant is specified (BFM = O/), the value contained in the least significant digit of BF is inserted into the Base Indicant digit of the specified Index Register. See Appendix A - Compatibility Notes (A.32) for valid Base Indicant values.

The Mobile Index Registers (IX4, IX5, IX6, & IX7) are registers in the hardware (i.e., not located in main memory). When the remaining Index Registers (IX1, IX2, & IX3) are loaded, the associated memory location (8, 16, & 24 relative to Base #0) will be updated to the value found in the "A" operand.

BURROUGHS	CORPORATION	+	 + 1997 5390
SYSTEM DEV Pasadena P	ELOPMENT GROUP Lant	V SERIES INSTRUCTIO	N SET
COMPANY CO	NFIDENTIAL SYST	EM DESIGN SPECIFICATION R	EV. A PAGE 333
20.3	STORE INDEX REG	ISTERS (SIX)/OP=68	

----

Format

+----+ | OP | AF | BF | A | +----+

0P = 68

- AF = Reserved and unused. AF may be indirect but a literal flag will cause an Invalid Instruction fault (IEX = 21).
- BF = Store Variant and may be specified as an indirect field length. The following variants may be specified by this field after any Indirect Field Length has been resolved:

VARIANT		BFM
* * <del>* * * * *</del> *	• • •	
Store Index Reg	ister #7	7
Store Index Reg	ister #6	6
Store Index Regi	ister #5	5
Store Index Reg	ister #4	4
Store Index Reg	ister #3	3
Store Index Reg	ister #2	2
Store Index Reg	ister #1	1
	ex Registers (4)	0

The use of all other BF values is reserved and will cause an Invalid Instruction fault (IEX = 26).

A = Address of the Index Register field. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

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COMPANY	CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 334
20.3	STORE INDEX REGISTERS (SIX)/OP=68 (Continued)
	Function 
	The Store Index Register instruction provides the memory address (A) of the starting location of either an eight digit field that will be used to store the specified (BFM)

digit field that will be used to store the specified (BFM) Index Register or the starting location of a 32-digit field that will be used to store the the four Mobil Index Registers (IX4, IX5, IX6 & IX7).

Each eight digits represents an index register of the following format:

INFORMATION	DIGIT	S
Sign	00	
Base Indicant	01	
Address	02-0	7

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Note - The Lowest memory address = 00

See Appendix A - Compatibility Notes (A.32) for valid Base Indicant values.

BURRCUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 335

20.4 LOCK/UNLOCK (LOK)/OP=60

Format

ł	-		-	+-			+-	-		+	 -	 	+
I		0 P		ŀ	A	F	I	8	F	I.	A		ł
4	-		-	<b>+</b> -		-	+-	-		+-	 -	 	+

0P = 60

AF = Unused & reserved, but may be specified as an indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21).

BF = Instruction Variant and may be indirect.

VARIANT	FUNCTION
09	Event Cause and Reset
08	Event Reset and Wait
07	Test Happened Status
06	Event Reset
05	Event Wait
04	Event Cause
02	Conditional Lock
01	Unconditional Lock
00	Unlock

All other BF values are reserved and will cause an Invalid Instruction fault (IEX = 26).

A = Address of the Lock/Event structure. Address may be indexed, indirect or extended. The final address controller must equal UN or cause an Invalid Instruction fault (IEX = 03).

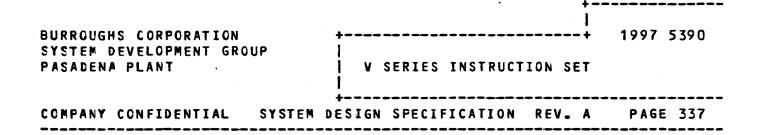
If "BF" has a value of OO-O2, "A" represents a Lock Structure.

If "BF" has a value of 04-09, "A" represents an Event Structure.

JRRCUGHS CORPORATION	+		1997 5390
STEM DEVELOPMENT GROUP Sadena plant	V SERIES INS	TRUCTION SET	
MPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICA	TION REV. A	PAGE 336
20.4 LOCK/UNLOCK (LOK	)/OP=60 (Continue	d)	
The Lock Str	ucture format is	as follows:	
INFORMATI	ON	DIGITS	
Lock Stat	us Field *	00-01	
	r Field	02-05	
	er Link Field	06-09	
	er Field	10-13	
	er Link Field	14-17	
Reserved		18-19	
Note ¹ - Th	e lowest memory a	ddress = 00	
The Event St	ructure format is	as follows:	
INFORMATI	ON	DIGITS	
Event Sta	tus Field *	00-01	
	te Field	02-05	
Event Wai	ter Link Field	06-09	
	ignator Field	10-13	
Event Cou	-	14-19	
Note - Th	e lowest memory a	ddress = 00	• •
* See Appendix	A - Compatibilit	y Notes (A.37)	)
	e Lock/Event Stru cause an Invalid		
Function			
This instruction			
and, according			
	, if necessary, t		
(A) and associa	ted lock fields w		owning or

• • •

contending for the lock or event.



#### 20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

The processor must determine if a lock is owned or available. If the Owner Field of the Lock Structure is equal to zero, the lock is available. If it is not equal to zero, the lock is owned.

The processor must determine if an event has happened. If the Event State Field is all "zeroes", the event has happened. If the Event State Field is all hexadecimal "F"s, the event has not happened. If the Event State Field contains any other value, cause an invalid instruction fault (IEX = 06) and terminate the instruction with no further action.

The machine dependent Lock Status Field of the Lock/Event Structure (A) may also be used to represent the status of the structure with one value representing owned and another representing available. This specification will always refer to the Owner Field of the Lock Structure (A) with the understanding that some systems may incorporate this feature. See Appendix A - Compatibility Notes (A.37).

This instruction may only be executed in Privileged Mode.

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# 20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 00 - UNLOCK

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This variant releases a Lock and, if any task is waiting for this lock, causes an interrupt to the MCP Kernel.

Read the Lock Structure (A) from memory. The value of the "Lock Owner Field" must equal the current Task Number located in absolute memory location 82 or cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

Store zeros into the "Lock Owner Field" of the Lock Structure (A) to indicate that this lock is now available.

Compare the "Lock Number Field" of the Lock Structure (A) with the "MCP Canonical Lock Number" field located in the Reinstate List Entry for the current task. If they are not equal, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

If the number fields are equal, store the contents of the "Lock Number Link Field" of the Lock Structure (A) into the "MCP Canonical Lock Number" field, located in the Reinstate List Entry for the current task.

Examine the "Lock Waiter Field" of the Lock Structure (A). If it is equal to zero, set the Comparison Flags to EQUAL and terminate the instruction.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASADENA PLANT	     V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 339

#### 20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

If the "Lock Waiter Link Field" is not equal to zero, execute the following procedure.

- 1. The Reinstate List pointer has been located with a Write Hardware Register (OP = 65:BF = 00) instruction. The four digit "Lock Waiter Field" of the Lock Structure (A) is used as an array subscript into this table to locate a new Reinstate List Entry. A sign and Base Indicant character of "C7" and six digits of the absolute address of this Reinstate List Entry are stored absolute memory location 24 31 (absolute IX3).
- Store the Released Lock Flag (03) into the Instruction Interrupt Cause Descriptor in absolute memory locations 32 - 33.
- 3. Set the Comparison Flags to HIGH and cause an Interrupt procedure to be executed that stores the address of the next instruction to be executed in the Interrupt Frame.

--Burrough's Prior Written Consent Required For Disclosure Of This Data--

SYSTEM DEVELOPMENT GROUPPASADENA PLANTV SERIES INSTRUCTION SET	BURROUGHS CORPORATION	++ 1997 5	390
PASADENA PLANT V SERIES INSTRUCTION SET	SYSTEM DEVELOPMENT GROUP		
	PASADENA PLANT	V SERIES INSTRUCTION SET	

20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 01 - UNCONDITIONAL LOCK

This variant competes for the lock specified by the Lock Structure (A) and, if the lock is owned, causes an interrupt to the MCP Kernel.

Read the Lock Structure (A) from memory.

Compare the "Lock Number Field" of the Lock Structure (A) with the "MCP Canonical Lock Number" field, located in the Reinstate List Entry for the current task. If the "Lock Number Field" is less than or equal to the "MCP Canonical, Lock Number" field, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

If the Lock is available, store the current task number (4 digits), located in absolute memory location 82, into the "Lock Owner Field" and store zeros into the "Lock Waiter Link Field" of the Lock Structure (A) and execute the following procedure.

- Copy the contents of the "MCP Canonical Lock Number" field, located in the current Reinstate List Entry, into the "Lock Number Link Field" of the Lock Structure (A).
  - 2. Copy The contents of the "Lock Number Field" of the Lock Structure (A) into the "MCP Canonical Lock Number" field, located in the Reinstate List Entry for the current task.

3. Set the Comparison Flags to EQUAL and terminate the instruction.

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V SERIES INSTRUCTION SET

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 341

20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

If the Lock is owned, execute the following procedure.

- Copy the "Lock Owner Field" of the Lock Structure (A) into the "Task Number Owning" field Located in the Reinstate List Entry for the current task.
- Copy the "Lock Waiter Link Field" of the Lock Structure (A) into the "Next Task in List" field Located in the Reinstate List Entry for the current task.
- 3. The four digit "Lock Owner Field" of the Lock Structure (A) is used as an array subscript into the Reinstate List to locate a new entry. A sign and Base Indicant character of "C7" and six digits of the absolute address of this Reinstate List Entry are stored absolute memory location 24 - 31 (absolute IX3).
- 4. Store the current Task number, located at absolute memory location 82, into the "Lock Waiter Link Field" of the Lock Structure (A).
- 5. Store the Waiting Lock flag (01) into the "State Indicator" field located in the Reinstate List Entry for the current task.
- 6. Store the Failed Lock Flag (01) into the Instruction Interrupt Cause Descriptor in absolute memory Locations 32 - 33.
- 7. Ignore the Trace Mode Bit. Even if in trace mode, do not perform a Trace Hardware Call following this instruction.
- 8. Set the Comparison Flags to LOW and cause an Instruction Interrupt to the MCP Kernel that stores the current instruction address in the Interrupt Frame.

BURROUGHS CORPORATION SYSTEM DEVELOPMENT GROUP PASA DENA PLANT	V SERIES INSTRUCTION SET	1997 5390
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20_4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 02 - CONDITIONAL LOCK

This variant attempts to obtain the lock specified by the Lock Structure (A).

If the Lock is available, perform the following:

- Compare the "Lock Number Field" of the Lock Structure (A) with the "MCP Canonical Lock Number" field Located in the Reinstate List Entry for the current task. If the "Lock Number Field" is less than or equal to the "MCP Canonical Lock Number" field, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.
  - 2. If the "Lock Number Field" is greater than the "MCP Canonical Lock Number, store the current task number (4 digits), located in absolute memory location 82, into the "Lock Owner Field" and store zeros into the "Lock Waiter Link Field" of the Lock Structure (A).
  - 3. Copy the contents of the "MCP Canonical Lock Number" field, located in the Reinstate List Entry for the current task, into the "Lock Number Link Field" of the Lock Structure (A).
  - 4. Copy the contents of the "Lock Number Field" of the Lock Structure (A) into the "MCP Canonical Lock Number" field, located in the Reinstate List Entry for the current task.
  - 5. Set the Comparison Flags to EQUAL and terminate the instruction.

If the Lock is owned:

1. If the "Lock Owner Field" equals the Task Number, set the Comparison Flags to LOW and terminate the instruction with no further action. If the owner is not the current task, set the Comparison Flags to HIGH and terminate the instruction with no further action.

BURROUGHS CORPORATION System development group Pasadena plant

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**V** SERIES INSTRUCTION SET

# COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 343

#### 20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 04 - EVENT CAUSE

This variant causes an Event and signals this fact to all tasks that are waiting for this event.

Read the Event Structure (A) from memory. If the "Event Designator Field" is not ecual to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

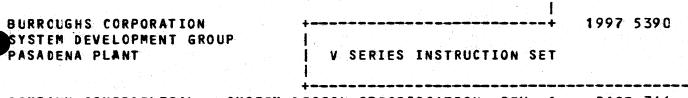
If the Event is in the Happened state, increment the "Event Count Field" by one (if it was originally at the maximum value for the container, set it to zero), set the Comparison Flags to Equal and terminate the instruction with no further action.

If the Event is in the Not Happened state, increment the "Event Count Field" of the Event structure (A) by one (if it was originally at the maximum value, set it to zero, and set the Event State Field to the Happened State.

Examine the "Event Waiter Link Field" of the Event Structure (A). If it is equal to zero, set the Comparison Flags to EQUAL and terminate the instruction with no further action.

If the "Event Waiter Link Field" is not equal to zero, execute the following procedure.

- The four digit "Event Waiter Link Field" of the Event Structure (A) is used as an array subscript into the Reinstate List to locate a new entry. A sign and base indicant character of "C7" and six digits of the absolute address of this Reinstate List Entry are stored at absolute memory locations 24 - 31 (absolute IX3).
- Store the Released Event Flag (04) into the Instruction Interrupt Descriptor in absolute memory locations 32 - 33.
- 3. Set the Comparison Flags to HIGH and cause an Instruction Interrupt to the MCP Kernel that stores the address of the next instruction to be executed in the Interrupt Frame.



### 20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

# BF = OS - EVENT WAIT

This variant will cause the current task to wait (i.e. be suspended) until the specified event is caused, if it is currently in the Not Happened State.

Read the Event Structure (A) from memory. If the "Event Designator Field" is not equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

If the event is in the Happened State, set the Comparison Flags to EQUAL and terminate the instruction with no further action.

If the event is in the Not Happened State, execute the following procedure.

- Copy the "Event Waiter Link Field" of the Event Structure (A) into the "Next Task in List" field located in the Reinstate List Entry for the current task.
- Store the current Task number, located at absolute memory location 82, into the "Event Waiter Link Field" of the Event Structure (A).
- Store the Waiting Event flag (02) into the "State Indicator" field located in the Reinstate List Entry for the current task.
- 4. Store a Failed Event flag (02) into the Instruction Interrupt Cause Descriptor in absolute memory Locations 32 - 33.
- 5. Set the Comparison Flags to LOW and cause an Instruction Interrupt to the MCP Kernel that stores the next instruction address in the Interrupt Frame.

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20.4	LOCK/UNLOCK (LOK)/OP=60 (Continued)
	BF = 06 - EVENT RESET
	This variant resets the Happened State of the event to the Not Happened State.
	Read the Event Structure (A) from memory. If the "Event
	Designator Field" is not equal to zero, cause an Invalid
• • •	Instruction fault (IEX = 06) and terminate the instruction with no further action.
a gaar -	If the event is in the Not Happened State, set the
	Comparison Flags to HIGH and terminate the instruction with no further action.
	If the event is in the Happened State, reset the "Event
	State Field" to the Not Happened State and store zeroes
	into th <del>e</del> "Event Waiter Link Field" of the Event Structure (A).
	Set the Comparison Flags to EQUAL and terminate the
• • • •	instruction.
	BF = 07 - EVENT TEST HAPPENED STATUS
	This variant tests whether or not an Event Happened.
	Read the Event Structure (A) from memory. If the "Event
	Designator Field" is not equal to zero, cause an Invalid
	Instruction fault (IEX = 06) and terminate the instruction with no further action.

If the event is in the Not Happened State, set the Comparison Flags to HIGH and terminate the instruction with no further action.

If the event is in the Happened State, set the Comparison Flags to EQUAL and terminate the instruction with no further action.

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20.4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 08 - EVENT RESET AND WAIT

This variant resets an Event Structure to the Not Happened state and forces the current task to wait (e.g., become suspended) unit the event has been caused.

Read the Event Structure (A) from memory. If the "Event Designator Field" is not equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with not further action.

Reset the Event State Field to the Not Happened State, then execute the following procedure.

- 1. Copy the "Event Waiter Link Field" of the Event Structure (A) into the "Next Task In List" field located in the Reinstate List Entry for the current task.
- 2. Store the Current Task Number located in the current Reinstate List Entry into the "Event Waiter Link Field" of the Event Structure (A).
- 3. Store the Waiting Event flag (02) into the "State Indicator" field located in the Reinstate List Entry for the current task.
- Store the Failed Event flag (02) into the Instruction Interrupt Cause Descriptor in absolute memory locations 32 - 33.
- 5. Set the Comparison Flags to "Low" and cause an Instruction Interrupt to the MCP Kernel that stores the next instruction address in the Interrupt Frame.

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### 20_4 LOCK/UNLOCK (LOK)/OP=60 (Continued)

BF = 09 - EVENT CAUSE AND RESET

This variant causes an Event, allowing any tasks which were waiting for the event to continue processing, and leaves the Event Structure in the Not Happened state.

------

Read the Event Structure (A) from memory. If the "Event Designator Field" is not equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

Increment the "Event Count Field" by one. Reset the Event State Field to the Not Happened state.

Examine the "Event Waiter Link Field" of the Event Structure (A). If it is equal to zero, set the Comparison Flags to "Equal" and terminate the instruction with no further action.

If the "Event Waiter Link Field" is not equal to zero, execute the following procedure.

- The four-digit "Event Waiter Link Field" of the Event Structure (A) is used as an array subscript into the Reinstate List to locate a new entry. A sign and base indicant character of "C7" and six digits of the absolute address of this Reinstate List Entry are stored at absolute memory locations 24 - 31 (absolute IX3).
- Store the Released Event flag (04) into the Instruction Interrupt Descriptor in absolute memory locations 32 - 33.
- 3. Set the Comparison Flags to "High" and cause an Instruction Interrupt to the MCP Kernel that stores the address of the next instruction to be executed to be saved in the Interrupt Frame.

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20.5	INITIALIZE LOCK/EV	ENT STRUCTURES (ILS)/OP=69
	Format	
an a		
	++++ 1 OP   AF   RF	A
	++++	
	OP = 69	
	AF = Length of t	he A operand in digits. AF may be
na da ante ante ante 1917 - Antara Antara da Antara da Antaria. 1919 - Antaria Antaria da Antaria da Antaria da Antaria da Antaria da		indirect or as a literal. Value has to otherwise an Invalid Instruction fault
• • • • • • • • • • • • • • • • • • •		ll be caused.
	BF = Instruction V	ariant and may be indirect.
	Variant F	unction
i na si	02 C	ounted Wait Freate Lock
	00 c	reate Event
		values are reserved and will cause an ouction fault (IEX = 26) if used.
- - 		e initial state data for the Event/Lock
•		alized or used. The address may be rect, or extended. The final address
	controller mu	st be UN or an Invalid Instruction fault
	the address	d (IEX = 03). If "BF" is 00, this is of a Boolean value which determines
		Event Structure being created will in the Happened state or in the Not
	Happened stat	e. If "BF" is 01, this is the address of
and a second s	the canonica	U number for the created Lock Structure.
		, this is the address of the count value determine whether to Wait or not.
	and a second second Second second second Second second	
•		

BURROUGHS CORPORATION System development group Pasadena plant	     V SERIES INSTRUCTION SET	1997 5390
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# 20.5 INITIALIZE LOCK/EVENT STRUCTURES (ILS)/OP=69 (Continued)

B = Address of the Event/Lock Structure being initialized. The address may be indexed, indirect, or extended. The final address controller must be UN or an Invalid Instruction fault will be caused (IEX = 03). If "BF" is 00 or 02, this is the address of an Event Structure. If "BF" is 01, this is the address of a Lock Structure.

#### Function

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This instruction creates and initializes a Lock Structure or an Event Structure in memory, or performs a counted wait on event. This instruction may only be executed in privileged mode.

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### 20.5 INITIALIZE LOCK/EVENT STRUCTURES (ILS)/OP=69 (Continued)

BF = 00 - CREATE EVENT

This variant creates an Event Structure in either the Happened state or the Not Happened State.

If the A Operand is non-zero (Boolean true), create an Event Structure at the B Address in the Happened state. If the A Operand is zero (Boolean false), create the Event Structure in the Not Happened state. All other fields in the event are cleared to zeroes and the comparison flags remain unchanged.

BF = 01 - CREATE LOCK

This variant creates a Lock Structure in the available state with a canonical Lock Number as specified by the A Operand.

If the A Operand is zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action. If it contains undigits, cause an Invalid Instruction fault (IEX = 07) and terminate the instruction with no further action.

Create a Lock Structure in the processor-dependent available state, with the "Lock Number Field" set to the value provided by the A Operand and all other fields cleared to zero.

The comparison flags remain unchanged.

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COMPANY	CONFIDENTIA	L SYSTEM	DESIGN	SPECI	ICATION	REV.	A	PAGE	351	1

# 20.5 INITIALIZE LOCK/EVENT STRUCTURES (ILS)/OP=69 (Continued)

BF = 02 - COUNTED WAIT

This variant uses the count provided by the A Operand as a guard to determine whether to perform the "Wait" function on the Event Structure described by the B Address.

Read the Event Structure (B) from memory. If the "Event Designator Field" is not equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction with no further action.

Read the 6-digit A Operand from memory. If the value of the A Operand is not equal to the "Event Count Field" in the Event Structure (B), set the comparison flags to equal and terminate the instruction with no further action.

If the value of the 6-digit A operand is equal to the "Event Count Field" in the Event Structure (B), examine the processor-dependent state of the Event. If it is in the Happened state, set the comparison flags to EQUAL and terminate the instruction with no further action. If it is in the Not Happened state, execute the following procedure.

- 1. Copy the "Event Waiter Link Field" of the Event Structure (A) into the "Next Task In List" field located in the Reinstate List Entry for the current task.
- 2. Store the Current Task Number located in the current Reinstate List Entry into the "Event Waiter Link Field" of the Event Structure (A).
- 3. Store the Waiting Event flag (02) into the "State Indicator" field located in the Reinstate List Entry for the current task.
- 4. Store a Failed Event flag (02) into the Instruction Interrupt Cause Descriptor in absolute memory locations 32 - 33.
- 5. Set the Comparison Flags to LOW and cause an Instruction Interrupt to the MCP Kernel that stores the next instruction address in the Interrupt Frame.

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20.6 MOVE	LOCK STRTUCTUR	ES (MLS)/OF	9=6A	
Forma	t sa			
•				
1 OP	+++   AF   BF   +++	A b	В	
0P =	6 A			
		d Length.	A literal f	specified as a lag will cause a •
BF =	Instruction Va	riant and m	ay be indir	ect.
	Variant Fu	nction		
	01 Ma 00 Ma	ve Lock Owr		
A =	Address may	be indexed controller	, indirect, must be UN	Event Structure or extended. Th or an Invali X = 03)
	Address of the	receiving	field for	the informatio
	The address ma	ly be indexe less control	ed, indirec ler must be	/Event Structure t, or extended UN or an Invali X = 03).
Funct	ion			
Event an ic	Structure (BF Mentically size	= 00) or a d destinati	Lock Struc	f state from a ture (BF = 01) t This instruction
may (	only be execute	d in privil	.eged mode.	•
	•			

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20.6	MOVE LOCK STRTUCTURES (MLS)/OP=6A (Continued)
	BF = 00 - MOVE EVENT COUNT
	Read the Event Structure (A) from memory. If the "Event
	Designator Field" is not equal to zero, cause an Invalid
	Instruction falult (IEX = 06) and terminate the
	instruction with no further action.
	If the "Event Count Field" contains undigits, cause an
	Invalid Instruction Fault (IEX = 07) and terminate the
	instruction with no further action.
	Mana bla d'Alais Menant Caugh Sialdh Anan bha Suadh
	Move the 6 digit "Event Count Field" from the Event Structure (A) to the 6 digit destination field specified
	by the B Address.
	by the D Address.
	BF = 01 - MOVE LOCK OWNER
	Read the Lock Structure (A) from memory. If the "Lock
	Number Field" is equal to zero, cause an Invalid Instruction fault (IEX = 06) and terminate the instruction
	with no further action. If the "Lock Number Field"
	contains undigits, cause an Invalid Instruction Fault
	(IEX = 07) and terminate the instruction with no further
	action.
	If the "Lock Number Field" is not equal to zero or
	contains no undigits, move the 4 digit Lock Owner Field
	from the Lock Structure (A) to the 4 digit destination
	field specified by the B Address.

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20.7

WRITE HARDWARE REGISTERS (WHR)/OP=65

Format

+----+ OP | AF | BF | A | +----+

0P = 65

AF = Unused & reserved, but may be specified as an indirect field length. A literal flag will cause an Invalid Instruction fault (IEX = 21).

_____

BF = Variant and may be specified as an indirect field length. The following variations may be specified by this field after any Indirect Field Length has been resolved:

**BF = 00 REINSTATE LIST ADDRESS** 

Use the "A" operand to locate the nine digit absolute memory address of the Reinstate List pointer. See Appendix A - Compatibility Notes (A.38). Recalculate any references based on the Reinstate List pointer. See Appendix A - Compatibility Notes (A.43).

**BF = O1** SNAP PICTURE ADDRESS

Use the "A" operand to locate the nine digit absolute memory address of the Snap Picture. Snap Picture Enable will be set to "one".

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20.7	WRITE H	ARDWARE REG	ISTERS	(WHR)/O	P=65 (Ca	ontinued)	
	BF = 02	MEMORY ER	ROR REF	ORT ADD	RESS.		
	men Eri Eri Pro Eri	ror Report ror Report ocessors ha ror Report	ess of Enable Pending ive diff	the Me will be will b erent r	mory Eri set to e set to equirema	ror Repor a "one" o "zero". ents for	t. Memory and Memory
		.31).					
	BF = 0.3	MEMORY AR	EA STAT	US TABL	E ADDRES	5 S -	
	nen		ss of	the M	emory /	Area Sta	t absolute tus Table. inter.
	OTHER BI	F VALUES					
		e use of al ise an Inva					
	ma) add	be inde	exed, i oller m	ind <mark>irec</mark> t iust equ	or ex al UN or	ktended.	e address The final ^S n Invalid
	dat	any of the ta field ror fault (	are inv	alid (u			
		at certain (ecuting th					
		struction a	ay only	be exe	cuted in	n Privile	ged Mode.
					<b>.</b> .		

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20.8 SET MODE (	SMF)/0P=47					
Format						
T OP   A1	+ FBF   +					
OP = 47 AFBF = Uni	used and i	gnored.		a San San San San San San San San San San San San San San San San San San		
Function -	n an an Anna an Anna Anna Anna Anna Ann					

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The Set Mode instruction performs no useful operation. See Appendix A - Compatibility Notes (A.24).

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20.9 FAIL (BAD)/OP=AB

Format

+----+ | OP | AF | BF | A | +----+

OP = AB

AF = Unused and ignored. The literal and indirect field length flags will be ignored.

BF = Unused and ignored. The indirect field length flag will be ignored.

A = Unused and ignored. The indirect, extented and indexed flags will be ignored.

Function

The Fail instruction causes an intentional Invalid Instruction fault (IEX = 01). The instruction will not be examined for any invalid address constraints.

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20.10	SYSTEM STATUS (SST	T)/OP=99	
	Format		
	*****		
anda Antonio antonio antonio Antonio antonio antonio	P AF BF	•	
	0P = 99		ана станция и служная станция станция и При служи служи станция станция При служи станция станц
	field length	eserved. May be speci n. A literal flag wi fault (IEX = 21).	
	BF = Status Variar Length.	nt. May be specified a	s an indirect fiel
	VARIANT	FUNCTION	
	00. 01	STATUS INDICATIORS System I/D	
		ll other BF values is alid Instruction fault	
	indexed, ind controller i	he Status data field. direct or extended. must equal UA or c fault (IEX = 03).	The final address
	Function		
n a se		instruction stores th pecified below, into t	

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20.10	SYSTEM STATUS (SST)/OP=99 (Continued)	
BF = 00	SYSTEM STATUS	
	The System Status is stored in memory in t format:	he following
	INFORMATION BYTE B	IT
		-7 3 2
	Temperature Warning Status 00	1 0
•	Note - The lowest memory address = 00	
8F = 01	<pre>* See Appendix A - Compatibility Note SYSTEM I/D</pre>	S (A.4U).
	The System I/D is stored in memory in t format:	he following
	INFORMATION EBCDIC BYTE	S
	Processor Type 00-09 * Specification Level 10-19 *	
	Shared System Number 20-21 Multiple Processor Number 22-23 Serial Number 24-33 *	
	Memory Size 34-49 Firmware Level 50-97 * Reserved (00 00) 98-99	
	Note - The Lowest memory address = 00	J
	* See Appendix A - Compatibility Note	s (A.40).
	The Firmware Level field of the System I/D m character "FF" to indicate the end of da field.	
	character "FF" to indicate the end of da	

#### 20.10.1 STATUS INDICATORS

17-18-88-94-48.

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The Status Indicators are described in the following paragraphs.

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MEMORY ERROR REPORT STATUS

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This bit is set to indicate that a Memory Error Report has been stored in memory at a location that has been previously been set with a Write Hardware. Register instruction (OP = 65:BF = 02).

VOLTAGE WARNING STATUS

This bit is set to indicate that the System input Voltage is less than a preset value. This condition does not cause a power-off cycle. This bit will be true as long as the warning condition exists.

#### TEMPERATURE WARNING STATUS

This bit is set to indicate that the System Temperature has exceeded a preset value. This condition does not cause a power-off cycle. This bit will be true as long as the warning condition exists.

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 361

21 STRING INSTRUCTIONS 

Service aspects

Search and and

String instructions operate on large data fields that are described by string descriptors that are found in memory at the locations specified by the "A" and "B" instruction addresses. د بالمطالب بالمحاد مستمر بالم

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The format of the string descriptor is as follows:

INFORMATION		DIGITS
Reserved	na an an Anna an Anna An an Anna an An	00-01
Environment Number		02-07
Memory Area Number		08-09
String Begin Address	(SBA)	10-15
String End Address	(SEA)	16-21
Container Begin Address	(CBA)	22-27
	(CEA)	28-33

Note: - the lowest memory address = 00

The "4" bit of the most significant digit of the instruction field length (AF/BF) contains the Memory Area Variant.

If the Memory Area Variant is not set, then the and Environment Number and the Memory Area Number contained in the string descriptor must be resolved to point to the selected Memory Area Table entry.

If the Memory Area Variant is set, then the addresses contained within the string descriptor are relative to the base of the same Memory Area that is specified for the address of the string descriptor.

And Electric If the first digit of the Environment Number is equal to a "D" or if the Environment Number is equal to "O" and the processor is not in Privileged Mode, cause an Invalid Instruction fault (IEX = 32) and terminate the instruction with no further action. Otherwise, resolve the Memory Area Table entry pointed to by the Environment Number and Memory Area Number in the string descriptor.

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21

STRING INSTRUCTIONS (Continued)

If the resolved MAT entry type digit indicates an Original entry, use the Base and Limit addresses contained in the entry to locate the string.

If the resolved MAT entry type digit indicates an Unused entry, cause an Address Error (AEX = 50) fault that will store the instruction address of the String instruction in the resultant Hardware Call procedure and terminate the instruction with no further action.

If the resolved MAT entry type digit indicates a Memory Area Fault entry, cause a Hard Memory Area Fault that will store the address of the next instruction to be executed in the resultant Hardware Call procedure. The Environment Number, Memory Area Number, and Task Number that point to this Memory Area Table entry will be stored as stack parameters in the resultant Hardware Call procedure.

This procedure is repeated for each of the operands.

STRING	- The six	digit address,	relative to the	
BEGIN	specified	memory area, of	the first digit of th	e
ADDRESS	string.		· · ·	

STRING - The six digit address, relative to the END specified memory area, of the first digit beyond ADDRESS the end of the string.

CONTAINER - The six digit address, relative to the specified BEGIN memory area, of the area allocated to contain ADDRESS the specified string.

CONTAINER - The six digit address, relative to the specified END memory area, of the first digit beyond the area ADDRESS allocated to contain the specified string.

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21.1

MOVE STRING (MVS)/OP=A0

Format

OP = AO

AF = Source field variant. AF may be indirect but a
 literal flag will cause an Invalid Instruction fault
 (IEX = 21).

The least significant digit is the Update Variant. A value of "O" indicates that no Update should take place. A value of "1" indicates that an update of the source string begin address should take place. The use of all other AFL values is reserved and will cause an Invalid Instruction fault (IEX = 25).

The most significant digit is the Memory Area Variant. A value of "O" indicates that the Memory Area specified by the Environment Number and the Memory Area Number contained in the source string descriptor (A) is to be used for the addresses contained within the source string descriptor. A value of "4" indicates that the Memory Area specified for the source string descriptor (A) is to be used for the addresses contained within the source string descriptor. The use of all other AFM values is reserved and will cause an Invalid Instruction fault (IEX = 25).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 364

### 21_1 MOVE STRING (MVS)/OP=A0 (Continued)

BF = Destination field variant. BF may be indirect.

The two least significant bits of the most ine two teast significant Dits of the most significant digit of BF contain the Substring Select variant and are coded to select a substring from the destination string. The possible selections are:

	SUB-STRING RAN	GE	VALUE
	Container Begi Reserved	n => Container End	3
	String End String Begin	=> Container End => String End	Ť O

The "4" bit of the most significant digit of BF is the Memory Area Variant. If the variant is equal to "O", the Memory Area specified by the Environment Number and the Memory Area Number contained in the destination string descriptor (B) is to be used for the addresses contained within the destination string descriptor. If the variant is equal to "1", the Nemory Area specified for the destination string descriptor (B) is to be used for the addresses contained within the destination string descriptor.

The least significant digit of BF is the Update Variant. A value of "O" indicates that no update of the destination string begin address should take place. A value of "1" indicates that an update should take place.

The use of all other BF values is reserved and will cause an Invalid Instruction fault (IEX = 26). 

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21_1 MOVE STRING (MVS)	)/OP=AO (Contin	ued)	
controller Instruction	, indirect or ext must specify U fault (IEX = 03)	ended. The fir N or cause a	nal address
final addre variant as f	the destinati y be indexed, i ess controller follows:	ndirect or exte	ended. The
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Pad with No paddir		0 (UN) 1 (SN) 2 (UA)	· • •
n se service de la composition de la co La composition de la c			
്യം പ്രതിനം പ്രതിനം പാലം പ്രതിപ്പോയം തില്ലെക്കാനം ഇതുലായിന് കുത്താനം പ്രതിവ്യാം പ്രതിവ്യാം പാലായിന്നും പോല്യം പ്രതിന്നും പ്രതി	aanat ar totoo a saa ay ahaan ay ahaan ahaan ahaa		

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21.1 MOVE STRING (MVS)/OP=A0 (Continued)

# Function

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The Move String instruction will move the string begin to string end substring from a location specified by the source string descriptor (A) to a location specified by the destination string descriptor (B) and the string select variant (BF). If padding is required in the destination, it will be specified by the Padding variant (BC). Data will not be read from a string end address or written into the string end address or the container end address.

If the source substring begin address is greater than the source substring end address, cause an Address Error fault (AEX = 01) and terminate the instruction with no further action.

If the destination substring begin address is greater than the destination substring end address, cause an Address Error fault (AEX = 01) and terminate the instruction with no further action.

If the Update bit in "AF" is equal to a "zero", the source string descriptor will not be changed.

If the Update bit in "AF" is equal to a "one", the String Begin Address in the source string descriptor is set to point to one digit beyond the last digit moved.

If the Update bit in "BF" is equal to a "zero", the destination string descriptor will not be changed.

If the Update bit in "BF" is equal to a "one", the String End Address in the destination string descriptor is set to point to one digit beyond the last digit written.

If the Update bit in "BF" is equal to a "one" and the Sub-string Select bits are equal to "3" (CBA => CEA), the String Begin Address in the destination string descriptor is set to the same value as the Container Begin Address.

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21.1 NOVE STRING (MVS)/OP=A0 (Continued)

EQUAL LENGTHS

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If the source and destination lengths are equal the source substring will be moved to the destination substring and the Comparison Flags will be set to EQUAL.

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SOURCE LONGER THAN DESTINATION

If the source length is longer than the destination length, then a length corresponding to the destination length will be moved from the left justified source substring to the destination substring and the Comparison flags will be set to NIGH.

SOURCE SHORTER THAN DESTINATION

If the source length is shorter than the destination length, then a length corresponding to the source length will be moved from the source substring to the left justified destination substring. The "B" address controller bits will determine if padding is required and what type of padding is required.

If the "B" address controller is equal to "1", then no padding takes place and the Comparison Flags are set to LOW_

If the "B" address controller is equal to "O", then the remaining digits in the destination string are padded with zeros and the Comparison Flags are set to EQUAL.

If the "B" address controller is equal to "2", then the remaining digits in the destination string are padded with blanks (40) and the Comparison Flags are set to EQUAL. If there are an odd number of digits remaining in the destination string, cause an Invalid Instruction fault (IEX = 07) and terminate the instruction without updating the pointers.

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 368

21.1 MOVE STRING (MVS)/OP=A0 (Continued)

# Null Strings

If the source string is a null (SBA=BEA), then the destination field will be filled with the padding character specified by the "B" address controller. If the destination string is a null, the Comparison flags will be set HIGH and the instruction will terminate with no further action. If both the source string and the destination string are null, the Comparison Flags will be set to EQUAL and the instruction will terminate with no further action.

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Overlap

String containers and descriptors that occupy any of the same memory locations will produce unspecified results that may vary from processor model to processor model.

Fartial overlapping string containers will produce unspecified results that may vary from processor model to processor model.

Partial overlapping descriptors will produce unspecified results that may vary from processor model to processor model.

Total overlap of string containers is permitted.

Total overlap of descriptors (A = B) is permitted. The hardware is restricted to not update the source descriptor before the destination descriptor has been acquired.

Partial overlap of substrings will produce unspecified results unless the destination substring select bits equal "3" (CBA => CEA) and the descriptors totally overlap (A = B), in which case the string is normalized by moving the string to the left and filling the container with the padding characters specified by the "B" address controller.

BURROUGHS CORFORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 369

21.2

### COMPARE STRING (CPS)/OP=A1

Format

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ŧ.	OP	1. J	AF	1	8 F	1	A	ţ.	8	· ].
+-		+		-+-		+		-+		+

OP = A1

- AF = A Memory Area Variant. AF may be indirect but a literal flag will cause an Invalid Instruction fault (IEX = 21). The most significant digit is the Memory Area Variant. A value of "O" indicates that the Memory Area specified by the Environment Number and the Memory Area Number contained in the first string descriptor (A) is to be used for the addresses contained within the first string descriptor. A value of "4" indicates that the Memory Area specified for the first string descriptor (A) is to be used for the addresses contained within the first string descriptor. A value of "4" indicates that the Memory Area specified for the first string descriptor (A) is to be used for the string descriptor. A value of "4" indicates that the Memory Area specified for the first string descriptor (A) is to be used for the addresses contained within the first string descriptor. The use of all other AF values is reserved and will cause an Invalid Instruction fault (IEX = 25).
  - BF = B Memory Area Variant. BF may be indirect. The most significant digit is the Memory Area Variant. A value of "O" indicates that the Memory Area specified by the Environment Number and the Memory Area Number contained in the second string descriptor (B) is to be used for the addresses contained within the second string descriptor. A value of "4" indicates that the Memory Area specified for the second string descriptor (B) is to be used for the second string descriptor. The use of all other BF values is reserved and will cause an Invalid Instruction fault (IEX = 26).

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 370

### 21.2 COMPARE STRING (CPS)/OP=A1 (Continued)

A = Address of the first string descriptor. Address may be indexed, indirect or extended. The final address controller must specify UN or cause an Invalid Instruction fault (IEX = 03).

B = Address of the second string descriptor. Address may be indexed, indirect or extended. The final address controller specifies the padding variant as follows:

PADDING VARIANT	B-CONTROLLER
Pad with zero	0 (UN)
No padding	1 (SN)
Pad with blank (40)	2 (UA)

# Function

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The Compare String instruction will compare the binary values of the substring defined by the String Begin and End Addresses specified by the "A" string descriptor to the substring defined by the String Begin and End Addresses specified by the "B" string descriptor and set the Comparison Flags EQUAL if the strings are identical, HIGH if the "A" string is of greater value than the "B" string, and LOW if the "A" string is of lesser value than the "B" string. No compare will take place on the data located at the string end address.

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21_2	COMPARE STRING (CPS	)/OP=A1 (Co	ntinued)	
	If a String Begin A Address, cause an terminate the instr	Address E	rror fault	(AEX = 01) and
• • • • • • • • • • • • • • • • • • •	The comparison of length) will caus EQUAL_			
	If the source and strings will be co set.			
	If the lengths a dependent on the va			
•	If the "B" address string will be c length of the short of no padding, co set the Comparison	ompared to er string on mparison wit	the shorter ly. However, h a null stri	string for the for this case
	If the "B" address string will be c length of the short longer string wi comparison with a n compared entirely a	ompared to er string th ll be comp ull string,	the shorter en the rema ared against the non-null	string for the inder of the zeros. (For
	If the "B" address string will be c length of the short longer string w characters. (For non-null string w characters.)	ompared to er string the ill be comp comparison ill be comp	the shorter en the rema pared agains with a null ared entirely	string for the inder of the t blank (40) string, the
· · · · · · · · · ·	Overlap			
	Partial overlapping results that may model.			

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21.3

HASH STRING (HSH)/OP=A2

Format

OPIAFIBFIA I BI

OP = A2

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AF = A Memory Area Variant. AF may be indirect but a literal flag will cause an Invalid Instruction fault (IEX = 21). A value of "00" indicates that the Memory Area specified by the Environment Number and the Memory Area Number contained in the source string descriptor (A) is to be used for the addresses contained within the source string descriptor. A value of "40" indicates that the Memory Area specified for the source string descriptor (A) is to be used for the source string descriptor. A value of "40" indicates that the Memory Area specified for the source string descriptor (A) is to be used for the addresses contained within the source string descriptor (A) is to be used for the addresses contained within the source string descriptor. The use of all other AF values is reserved and will cause an Invalid Instruction fault (IEX = 25).

____

BF = Length of the "B" field. A value of "00" is equal to a length of 100 digits. BF may be indirect.

- A = Address of the source string descriptor. Address may be indexed, indirect or extended. The final address controller must specify UN or cause an Invalid Instruction fault (IEX = 03).
- B = Address of the destination hash key field. Address may be indexed, indirect or extended. The final address controller must specify UN or cause an Invalid Instruction fault (IEX = 03).

BURROUGHS CORPORATION System development group Pasadena plant	V SERIES INSTRUCTION SET	1997 5390
COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 373

### 21.3 HASH STRING (HSH)/OP=A2 (Continued)

Function -----

The Hash String instruction will produce a hash key of Begin and End Addresses specified by the "A" string descriptor and store the key in the memory location specified by the "B" address.

Ef the String Begin Address is greater than the String End Address, cause an Address Error fault (AEX = 01) and terminate the instruction with no further action.

If the length of the source string is less than the length of the destination field (BF), the data from the source string will be moved to the destination data field and the remaining destination data field will be filled with trailing zeros.

If the length of the source string is equal to the length of the destination field (BF), the data from the source string will be moved to the destination data field and the instruction will terminate with no further action.

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21.3	HASH STRING (HSH)/OP=A2 (Continued)
	The hashing algorithm requires that successive "BF" amounts of the specified string are Exclusive OR'ed and the result stored in memory. The following steps itlustrate one method of performing this algorithm.
	<ol> <li>Using the String Begin Address as the source address, move "BF" digits from the string to the "B" field in memory.</li> </ol>
	2. Increment the source address by "BF".
<ul> <li>at the of a light grad</li> </ul>	3. Perform an Exclusive OR of "BF" digits specified by the source address and the "B" field in memory.
	4. Store the result in the "B" field in memory.
	5. Increment the source address by "BF" and repeat Steps 3 - 5 until the difference between the source address and the String End Address is zero or less than "BF".
	If the difference is zero the instruction is complete.
	If the difference is less than "BF", then perform the next Exclusive OR with only the difference amount.
	Store the result in the "B" field in memory leaving the remainder of the "B" field as it was previously and terminate the instruction.
	Overlap
	Any overlap of the "B" operand with the descriptor or the string produces unspecified results.
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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 375

- - 22 RESERVED MEMORY

22.1 KERNEL DATA AREA

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The following areas of absolute memory are reserved for the purposes indicated.

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Absolute Memory Address	Purpose
00-39	Indirect Field Length
00-07	Undefined
08-15	Index Register One (IX1)
16-23	Index Register Two (IX2)
24-31	Index Register Three (IX3)
21-22	Interrupts Occured Code
32-33	Instruction Interrupt Cause Descriptor
34-35	MCP Kernel Request Code
38-39	SCAN Result Storage
40-45	Kernel Stack Pointer
46-47	Breakpoint Pattern for Kernel
48	HALT Execution Digit
•	Internal I/O Mask
50-71	Unused
72-81	R/D Storage Area
82-85	Current Task Number
86-93	Reserved
94-99	Kernel Interrupt Branch Address
100-111	Channel "OO" Result Descriptor
	and Link
120-131	Channel "O1" Result Descriptor
	and Link
••••	
an a	
1640-1651	Channel "77" Result Descriptor
na an a	and Link
8000-8039	MCP Kernel Request Data



Figure 20-1 Channel Format

1011021031041051061071081091101111121131141151161171181191201 <----R/D--->|<----LINK--->|<----R/D--->|<----MCP USAGE----->|

Memory address for channel "nn" Result Descriptor and Link equals: 20 x Channel "nn" + 100.

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RESERVED MEMORY RELATIVE TO THE MCP DATA AREA.

Each task has the following areas of its MCP Data Area (Environment #0, Memory Area #0) reserved for the purpose indicated.

Relative	
Memory Address	Purpose
00-39	Indirect Field Length
08-15	Index Register One (IX1)
16-23	Index Register Two (IX2)
24-31	Index Register Three (IX3)
38-39	SCAN Result Storage
40-45	Stack Pointer
46-47	Breakpoint Bit Pattern
48-49	Edit Table Entry O
50-51	Edit Table Entry 1
52-53	Edit Table Entry 2
54-55	Edit Table Entry 3
56-57	Edit Table Entry 4
58-59	Edit Table Entry 5
60-61	Edit Table Entry 6
62-63	Edit Table Entry 7
64-65	Trap Enable (FF)
66-71	Trap Address
72-81	R/D Storage Area
82-85	Task Number
86	Reserved
87-92	Hyper Call Function Table Pointer
93	Reserved
94-99	Hyper Call Function Table Limit



### APPENDIX A - COMPATIBILITY NOTES

### INTRODUCTION

The main body of this specification describes the machine independent behavior of a family of computers built with the V-Series operating system architecture. All members of the family exhibit the operational characteristics described in the main body. Previously supported user programs are still supported by this architecure, however, all of the prior privileged instructions have been changed or modified so that only a V-Series operating system may be executed with the describle instructions.

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The purpose of this appendix is to describe and contrast the machine dependent behavior of various medium systems processors as applied to the specified instructions.

Note: In the descriptions that follow, the phrase "results are unpredictable" means that the instruction may not get the same results from execution to execution due to the parallel access indicated bidding by multiple requesters, the fact that input operands may not be fully buffered before writing, and the requirement that in some cases multiple memory modules must be available for a read.

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#### A_01 RELATED SPECIFICATIONS

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	S 1987				Architecture
ED	S 1983	6915	a a secondaria da secondari	¥300	IOP
ED	s 1990	9431		V300	SNAP

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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 379

APPENDIX A - COMPATIBILITY NOTES (Continued)

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A-02

CPA

"Use of SN data types or mixed UA, UN data types may produce incompatible results."

B4800 - Mixed UN, UA data types:

Each digit of UN field is appended to a zero digit to produce a character of the form Od which is compared against the other operand's character.

SN data type:

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The B4800 treats this exactly as if it were UN (eg. 7 SN is treated as if 7 UN).

B2900 - Both operand data types must be the same, or else B3900 it is treated as an Invalid Instruction. SN is treated as UN.

- B4900 If the data types are not both UA or both UN, execution of the instruction results in a BCT to 94 with Invalid Instruction set in the processor R/D.
- V3 If the data types are not both UA or both UN, execution of the instruction results in a Hardware Call procedure with an Invalid Instruction fault (IEX = 03).



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### A.03

MVA

"When the "A" and "B" controllers indicate UA data, the field lengths are equal (AF=BF), and the final "B" address is within the "A" data field (address "A" to "A" + 2 x AF), the source data field between the "A" and "B" address will be repeated throughout the destination field."

"Cases of overlapping "A" and "B", other than described above, may produce incompatible results."

B4800 - UN-UN or SN-SN:

Source data between "A" and "B" addresses will be replicated in "B". Rules for padding or truncation remain the same.

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UA-UA: UA: 

AF does not have to equal BF for replication.

Mixed data types cause unusual results.

82900 - In all cases, other than the one described, no. B3900 replication will take place. The result field will contain the same data as if there were no overlap.

B4900 - Same as B2900/B3900 except that partial V3 overlapping the literal field will cause the result field to contain the same data as if there were no overlap. were no overlap.

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	APPEN	DIX A - COMPATIBILITY NOTES (Continued)
A_04	MVN	n na sa manggangangangan na sa
<b>#_04.1</b>	"Cases of overla above, may produ	pping "A" and "B", other than described ce incompatible results."
•	84800 - UN-UN, S	N-SN OF UA-UA:
	Source d replicat truncati	ata between "A" and "B" addresses will be ed in "B". Rules for padding or on remain the same.
	Mixed da	ta types cause unusual results.
	B3900 replicat	ases, other than the one described, no ion will take place. The result field tain the same data as if there were no
	"Move Numeric UA the final compar	
	84800 - UA-UA, U 84900 V3	
	If the i zero, t otherwis if the interpre will b	nterpreted value of the source data is the comparison flags will be set to EQUAL, the comparison flags will be set to HIGH first digit of the source data is ted as positive or the comparison flags be set to LOW if the source data is
	82900 - UA-UA, U	ted as negative. A-UN
	B3900	nterpreted value of the source data is he comparison flags will be set to EQUAL, e the comparison flags will be set HIGH.

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MPANY CON	FIDENTIAL SYSTE	M DESIGN SPECIFICATION REV. A PAGE 382
	APPEN	DIX A - COMPATIBILITY NOTES (Continued)
A .05	BZT, BOT	
	"Use of SN data	type may produce incompatible results.
	84800 - Treats a	ll non-UA data types as UN.
	82900 - An SN da 83900 Instruct 84900	
	V3 - An SN da	ta type will cause an Invalid ion fault (IEX = 03).
A_06	LSS, EQL, LEQ, G	TR, NEQ, GEQ, NUL, GTN
	"Use of branch incompatible beh	prediction op codes may result in avior."
		a branch prediction scheme whereby op codes indicate the most probable ath.

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 383

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## APPENDIX A - COMPATIBILITY NOTES (Continued)

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E626(GEQ)Taken (last time not taken)EA2A(NUL)Taken (last time not taken)EB2B(GTN)Taken (last time not taken)F121(LSS)Taken (last time taken)F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)	- 	E4	24(GTR)	Taken (last time not taken)	
EA2A(NUL)Taken (last time not taken)EB2B(GTN)Taken (last time not taken)F121(LSS)Taken (last time taken)F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)		E5	25(NEQ)	Taken (last time not taken)	
EB2B(GTN)Taken (last time not taken)F121(LSS)Taken (last time taken)F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA24(NUL)Taken (last time taken)		EÓ	26(GEQ)	Taken (last time not taken)	
F121(LSS)Taken (last time taken)F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)		EA	2A(NUL)	Taken (last time not taken)	
F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)		EB	2B(GTN)	Taken (last time not taken)	
F222(EQL)Taken (last time taken)F323(LEQ)Taken (last time taken)F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)	an a	5.55 F1	21(LSS)	Taken (last time taken)	
F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)		F2		Taken (last time taken)	
F424(GTR)Taken (last time taken)F525(NEQ)Taken (last time taken)F626(GEQ)Taken (last time taken)FA2A(NUL)Taken (last time taken)		F3			
F5 25(NEQ) Taken (last time taken) F6 26(GEQ) Taken (last time taken) FA 2A(NUL) Taken (last time taken)	• •				
F6 26(GEQ) Taken (last time taken) FA 2A(NUL) Taken (last time taken)					
FA 2A(NUL) Taken (last time taken)	, ··				

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A_C7	IVW, NVC	
A.07.1	'If AF indicates literal, the results may b incompatible."	e
	14800 - Since the field length is AFBF, the normal litera code (e.g. "A6") would indicate a literal of ove 400 digits starting at the instruction' A-syllable.	r
	32900 - Results in an Address Error. 33900	
	14900 - Results in an Invalid Instruction.	
and and a second se	13 - Causes an Invalid Instruction fault (IEX = 21).	
A.07.2	"Use of non-Mod 4 "A" or "B" addresses may produc incompatible results."	e
	14800 - Results in an Address Error_	

B2900 - No mod restrictions on "A" or "B". B 39 00 B 49 00 V 3 B3900

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1997 5390

A-08 INC, DEC

"Partial overlap of "A" or "B" may produce imcompatible results."

B4800 - Results are consistent but undefined.

B2900 - There are no overlap restrictions. The correct B3900 result will be stored in the "B" field.

B4900 - If both the "A" and "B" operands are less than or equal to 10 digits long, the correct answer will V.3 be stored in the result field. If either "A" or "B" operands are greater than 10 digits long and if the "A" address equals the "B" address and their data types are also the same, the correct result will be stored regardless of the values for AF and BF. In all other cases, the results are undefined.

#### A .09 ADD, SUB

"Partial overlap of "A" or "B" with "C" may produce incompatible results_"

B4800 - Results are undefined.

- B2900 Since there are no overlap restrictions, the B3900 correct result will be stored in the "C" field.
- B4900 If both the "A" and "B" operands are less than or W3 equal to 10 digits long, the correct answer will be stored in the result field. If either "A" or "B" operands are greater than 10 digits long and if the "A" or "B" address equals the "C" address and the respective data types are also the same, the correct result will be stored regardless of the values for AF and BF. In all other cases, the results are undefined.

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COMPANY CONF	IDENTIAL	SYSTEM	+ DESIGN	SPECIE	ICATION	REV. A	PAGE 386

A.10	MPY
	"Partial overlap of "A" or "B" with "C" may produce imcompatible results."
an a	B4800 - Results are consistent but undefined.
and a second	B2900 — Since there are no overlap restrictions, the B3900 correct result will be stored in the "C" field.
	B4900 - If both the "A" and "B" operands are less than or V3 equal to 10 digits long, the correct answer will be stored in the result field. If either "A" or "B" operands are greater than 10 digits long and if the "A" or "B" address equals the "C" address and the respective data types are also the same, the correct result will be stored regardless of
	the values for AF and BF. In all other cases, the results are undefined.

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COMPANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. A	PAGE 387

### A_11 AND, ORR, NOT

- A.11.1 "If the data types are not all UA and not all UN, incompatible results may be produced."
  - B4800 Mixed data types produce irregular results. For example, UN-UN-UA case results in characters whose zone digits are zero. In the UN-UA-UN case, the least significant digit of each "B" field character is ignored.
  - B2900 The "A" data type is used for all three fields B3900 ("B" and "C" data types are ignored).
  - B4900 Results in an Invalid Instruction.
  - V3 Cause an Invalid Instruction fault (IEX = 03).
- A_11_2 "Partial overlap of "A" or "B" with "C" may produce incompatible results".
  - B4800 Results are produced from previous intermediate results.
  - B2900 There are no overlap restrictions. The correct B3900 result will be stored in the "C" field.
  - B4900 If both the "A" and "B" operands are less than
    V3 or equal to 10 digits long, the correct answer will be stored in the result field. If either "A" or "B" operands are greater than 10 digits long and if the "A" or "B" address equals the "C" address and the respective data types are also the same, the correct result will be stored regardless of the values for AF and BF. In all other cases, the results are undefined.

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PASADENA PLANT	V SERIES INSTRUCTION SE	T

COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 388

### APPENDIX A - COMPATIBILITY NOTES (Continued)

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### A.12 SEA

"In each type of search, if the "B" field entry being compared to the key overlaps with the "C" address location, incompatible results may be produced."

B4800 - Search for Equal.

84900

V3 The overlapping "B" field entry is always considered Not equal to the key.

Search for Low or Lowest.

Only those units of the "B" field entry up to the "C" address are compared against a corresponding number of units of the "A" field key.

B2900 - If the "B" field overlaps the "C" address and it B3900 is the first comparison (i.e., starting "B" address), then the full "B" field is compared. If the "B" field overlaps the "C" address and it is not the first comparison, no comparison is performed and this "B" field entry is considered not equal to the key.

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	ander ander ander Ander ander ander ander Ander ander and	APPENDIX	A - COMF	PATIBILITY	NOTES ((	Continued)	
A.13	EDT				•		
A_13_1	"Use of an incompatib			the "C"	field 1	ay produce	
	84800 - SN	is treat	ed as if	the C con	troller sp	ecified UN.	
	82900 - SN 83900 In 84900				controlle	er sets	
		data typ walid Ins				er causes an	
A.13.2	Use of und specified					"Av" not	
n na sa	84800 - Re	sults are	undefine	d and may	go undete	ected.	
	82900 - Re 83900 ma 84900					oartial result	
	pa fi	rtial re eld.	sult may	struction have be	fault (IE en stored	EX = 07). A in the "C"	
A.13.3		f "A", "B			in any	manner may	
	82900 - To 83900 - To 91	pected r	esults.	Any oth	er form o		
	84900 ty V3 "E Mc tt	pes are t "field c we Digits	he same, onsist of , and Mov as the	and the f any subs /e Charact B2900/390	edit opera et of Mov ers, the p	and "C" data ators in the ve Suppress, results are other cases	
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		APPENDIX A	- COMPATIBIL	ITY NOTES	(Continued)		
A.14	TRN						
A-14-1	"If AF ind produced."		eral, incomp	atible re	sults may be		
			BF are concat f units will		literal length		
	84900 - Re	sults in an	Invalid Inst	ruction.			
	V3 - Ca	uses an Inv	alid Instruct	ion fault	$(IEX = 21)_{-}$		
A_14_2			s controller may be produc		ype is SN,		
	84800 - SN	is treated	as if it wer	e specifie	d as UN.		
، در به ۲۰۰۵ میلید ۱۹۹۵ - ۲۰۰۹ ۱۹۹۵ - ۲۰۰۹ میلید ۱۹۹۵ - ۲۰۰۹ میلید	82900 - Re 83900 84900	sults in an	Invalid Inst	ruction.			
	V3 - Ca	uses an Inv	alid Instruct	ion fault	(IEX = 03).		
A_14_3	"A" and "C	" fields ma		rlap. All	r both UN, the other forms of		
	B4800 - Re	sults are u	ndefined.				
		sults are u e B4800.	ndefined and	may be dif	ferent than		
		sults are u te)	npredictable.	(See "Int	roduction"		
A.14.4	B Address	restriction	na danasa (140) kijitaté kuadéa So		an a		
	84800 - B	Address mus	t be MOD 1000	<ul> <li>International descent des encont descent des encont descent desc</li></ul>	andra an Andra andra andr Andra andra and		
	82900 - No 83900 84900 V3	address re	strictions.				
	V5						

BURROUGHS CORPORATION System development group Pasadena plant		 ++ 1997 5390     V SERIES INSTRUCTION SET
CMPANY CON	FIDENTIAL SY	STEM DESIGN SPECIFICATION REV. A PAGE 391
	AP	PENDIX A - COMPATIBILITY NOTES (Continued)
A.15	MVR	
	"Partial over imcompatible	lap of the "A" and "B" fields may produce results."
	"B" "	irst move results in the data between "A" and smeared". This result is produced BF times in B" field.
a a a a a a a a a a a a a a a a a a a		
	B2900 - No ov B3900 in th	erlap restrictions. Produces correct result e "B" field.
	V3 data be st	e "A" address = the "B" address and their types are the same, the correct result will ored. In all other cases, the results are ined and depend upon the data types, the

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BURROUGHS CORPORATION YSTEM DEVELOPMENT GROUP ASADENA PLANT COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 392 APPENDIX A - COMPATIBILITY NOTES (Continued)

A.16 ARITHMETIC INSTRUCTIONS

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"If the operand data contains undigits other than in the sign digit, incompatible results may be produced."

- B4800 Undigits in arithmetic data other than the sign or zone digits are not detected as an error.
- B2900 Undigits in arithmetic data other than the sign or B3900 zone digis are detected as errors. The entire field containing the invalid unidgits remains unchanged. The processor reports the address of the instruction in error. The Overflow Flag is always set.
- B4900 Undigits in arithmetic data other than the sign or zone digits are detected as errors. If the operand in error is also written (i.e., INC), the operand may be partially overwritten with the new result but the detected undigits will still be present. The processor reports the address of the instruction in error. The Overflow Flag will not be set.
- V3 Undigits in arithmetic data other than the sign or zone digits are detected as errors. If the operand in error is also written (i.e., INC), the operand may be partially overwritten with the new result but the detected undigits will still be present. The processor will report the address of the instruction in error in the resultant Hardware Call procedure. The Overflow Flag will not be set.

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		APPENDIX	A - COMP	ATIBILITY (	NOTES (Co	ntinued)	
A.17	RAA, RAS, R	SU, RSS,	RMU, RMS	na an a	· · · · · · · · ·		
	If the mant (contains produced.						
	B4800 - The B4900 ope V3 tha	ration,	which may	produce a	less prec		
	82900 - The 83900	data wi	ll be nor	malized pr	ior to the	operation.	
A.18	RAA, RAS, R	SU, RSS					
	Different p significant producing s	digit	s durin	§ the co	omputation		
	V3			ntains 9 si ntains 17.	ignificant	digits;	
	82900 - 215 83900		cant digi	ts are main	ntained.		

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COMPANY CON	IFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 394
	APPENDIX A - COMPATIBILITY NOTES (Continued)
A_19	ele se
A_19_1	"If AF specifies literal, incompatible results may be produced."
-	B4800 - Undefined results.
	B2900 - Results in an Address Error. B3900
ina ing Kabupatèn Ang Ing Kabupatèn Ang	B4900 - Results in an Invalid Instruction.
an An Anna An An Anna Anna An	V3 - Causes an Invalid Instruction fault (IEX = 21).
A.19.2	"If the address to be written into base relative location 000040 exceeds six digits, incompatible results may be produced."
	84800 - Results in an Address Error.
	B2900 - Results in an Invalid Instruction. B3900 B4900
	V3 - Causes an Invalid Instruction fault (IEX = 04).

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		APPENDIX	A —	COMPAT	IBILIT	NOTES	(Cont	inued)	
A.20	MVD								
A.20.1	"Partial ov results."	verlap of	нАн	and "B	" may	produce	inco	mpatible	5
	on tha	lress is	less gro fie ackwa addre	than "I ups of ld with rd and ss; t	B" add four, h smean the "/ he sou	ress, th , are If o A ^m addre urce fi	e sour moved verlap ss is eld di	ce field to the occures greater gits, in	d e s r n
	84900 - Mov V3	ve Forwar	d						
						of 4 di accordi		will be	5
	Hov	e Backwa	rd					2000 1	
an a	and an element	The dif replica		ce bet	ween "/	and	<b>"8</b> "	will be	5
A.20.2	"Use of a l	iteral m	ay pr	oduce	incompa	atible r	esults	i **	
•	84800 - Lit	erals ar	e all	owed.		•	•		
	82900 - Res 83900	sults in	an Ad	dress	Error.				
	84900 - Res	ults in	an In	valid	Instru	ction.			
	V3. – Cau	ises an I	nvali	d Inst	ruction	n fault	(IEX =	21).	
a Salah sa				•				e	

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2 BURROUGHS CORPORATION 1997 5390 -----SYSTEM DEVELOPMENT GROUP PASADENA PLANT V SERIES INSTRUCTION SET COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 396 APPENDIX A - COMPATIBILITY NOTES (Continued) AL21 NVL A.21.1 "A literal may produce incompatible results". **B4800 - Literal is allowed.** B2900 - Literal is allowed but not recommended. B3900 B4900 - Literal will result in an Invalid Instruction. V3 - Literal will cause an Invalid Instruction fault ne di serie (IEX = 21). A.21.2 "Any partial or total overlap may produce incompatible results". 84800 - Total overlap allowed on: B4900 1) Identical B and C field or V3 2) Identical A and B field. No partial overlap is allowed. B2900 - There are no overlap restrictions. A_21.3 "If the three address controllers are not equal, incompatible results may be produced." B4800 - Not detected. "C" address controller used for all three. , where a long of B2900 - Results in an Invalid Instruction. B3900 B4900 V3 - Causes an Invalid Instruction fault (IEX = 03). 

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		APPENDIX	A - COMPAT	IBILITY NO	)TES (Co	ontinued)
A-22	BRT, BST		an a	👷 - n griff an ang	ه است.	
			produce in		e results	, ⁴⁴ •
n A≹Î A Marina Asert	84800 - L ⁴ 82900 83900	iteral is a	allowed.			
			an Invalid			
			nvalid Inst			( = 21).
A .22.2	"If the " may be pro		Ler specifi	ed SN, in	compatabl	e results
· · · · · ·	84800 - SI	treated a	as if UN wa	s specifio	ed 👞	
	83900 84900		an Invalid nvalid Inst		2000 - 2000 2004 - 2000 2004 - 2000	( = 03).
					an a	на устан Парала Парала Парала
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		PPENDIX A - COMPATIBILITY NOTES (C	ontinued)
A-23	SRD		
	"Undigits in results."	AFBF or link address may produce i	ncompatible
	84800 - There 82900 the F 83900	e is no undigit check for AFBF or t R/D area.	he Link in
		gits are checked for AFBF and the s will result in an Address Error.	following
		gits in AFBF and the following e an Address Error fault (AEX = 42)	
A.23.1	SRD	n an Alfred Standard (1997) and a standard and an	
	B4800 - SRD I B2900 B3900 B4900	resets Processor Interrupt.	
		essor Interrupt is not reset by thi ruction.	S
A.24	COMPATIBILITY		
and the states		an an an an an ann an an ann an ann an a	

This instruction is functionally different than the same op code in prior processors. 

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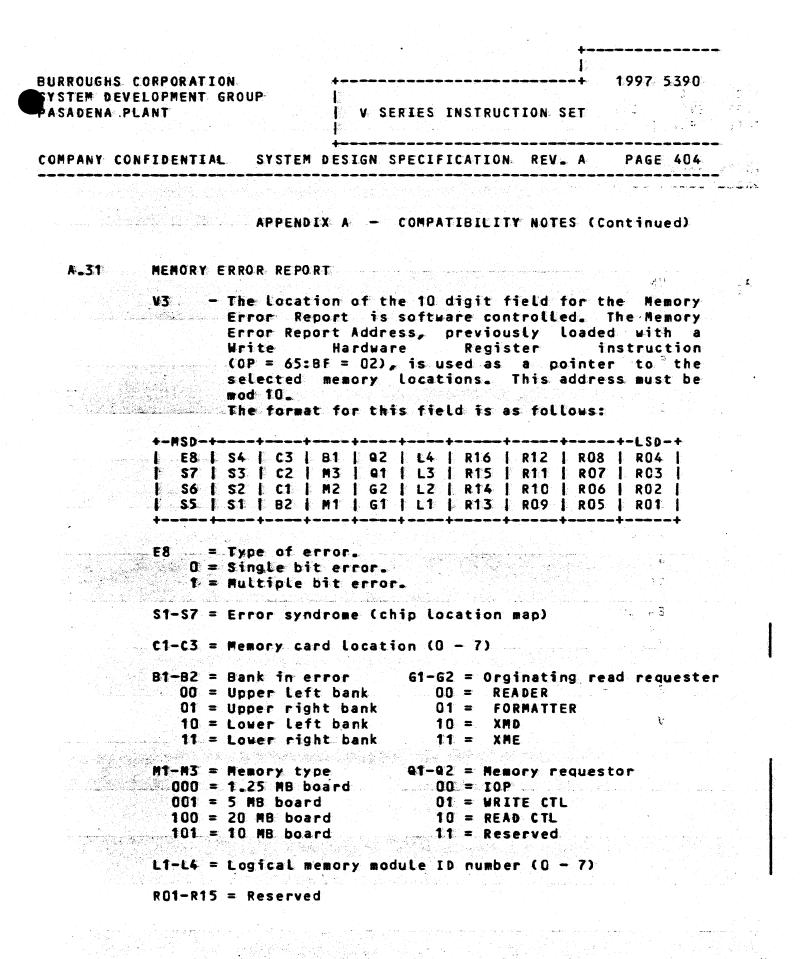
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	APPENDIX A - COMPATIBILITY NOTES (Continued)
A-25	HBK
	"Specification of an AF indirect field length may produce incompatible results."
	B4800 — An AF indirect field length may have many levels of indirection. Due to the indirect field length flag bits, the final AFA value must be in the hexadecimal range D-B. Undigits are allowed in the final AFB value.
•	B2900 - If the original AF does not specify indirect field B3900 length, the AF is valid and unchanged. However, if the indirect field length bits are set, the indirect field length is checked for errors and resolved (only one level of indirection is resolved). The final resolved field may be any value and is ignored.
	<ul> <li>B4900 - Any undigits in the original AF will cause an</li> <li>V3 Invalid Instruction unless contained in a valid indirect field length or literal specification. If the indirect field length bits are set, the indirect field length is checked for errors and resolved (only one level of indirection is resolved). The final resolved field may be any value and is ignored.</li> </ul>
A.25.1	HBK
	84800 - The Halt Digit is located at absolute memory 82900 address 77. 83900 84900

V3 - The Halt Digit is located at absolute memory address 48.

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and and a second se	APPEND	IX A - COMPATIBILITY NOTES	(Continued)
A-26	SLL/SLD		eren er en er e En er en e En er en e
A-26-1		SLL/SLD the sign digit of B ess in SLD) may produce	
		stored in sign digit field D) is neither a "C" or a "D'	
•		EBCDIC sign is stored in IX ⁴	1 (and IX2 in
•		ss controller specifies SN,	incompatible
	B4800 - SN treate	d as if UN was specified.	
	82900 - Results i 83900 84900	n an Invalid Instruction.	
· · ·	V3 - Causes an	Invalid Instruction fault	(IEX = 03).
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	<u>د ا</u>			APPEND	IX A -	COMPAT	IBILITY	NOTES	(Conti	nued)
A_29			ITS I	N INTER	MEDIATE	INDIF	RECT ADDI	RESSES		
	<b>\$</b> 5	"Undi produ	gits ce in	in an compati	unres ble res	olved ults."	intermo	ediate	addres	s may
	っしき きのご ない	B4800	- Th	e undig an add	its wil ress wl	.l not nich wo	be deter ould fet	cted an ch mean	d will ingless	be used data.
				defined an Add			inal add	dress w	ithout	resulting
		B4900	- Re	sults i	n an Ac	Idress	Error.			
		<b>V</b> 3	- Ca	uses an	Addres	s Erro	or fault	(AEX =	32).	
A_30		INDEX	ING A	BOVE LI	MIT OR	BELOW	BASE			
				t to in compati			BASE OI	r above	the LI	MIT may
8.		82900 83900	th th	at the e Base	final a /Limit	iddress will	SE or a wraps   produce causes	back ar e an	ound to unpredi	within ctable
<b>.</b>	* ) <b>? 5</b>	B4900	- Re	sults i	n an Ac	ldress	Error.		•	
		٧3	- Ca	uses an	Addres	s Erro	or fault	(AEX =	11).	
			• • • • • • • • • • • • •	• • • • • • •						
	- <u>.</u>	· · · · ·								



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ANT	•	ES INSTRUCT	ON SET	
FIDENTIAL S	+ YSTEM DESIGN SPI	CIFICATION	REV. A	PAGE 405
	PPENDIX A - COM	PATIBILITY NO	)TES (Co	ntinued)
BASE INDICAN	TVALUES	<u> </u>		
"Some values	of the Base Inc	licant digit	may be i	nvalid"
and and	will cause a			
USER SERVICE	S MEMORY AREA T	BLE ENTRY		
V3 - INFO	RMATION		DIGITS	I
Base	Address		00-04	•
Soft	ware Use		10-19	- - -
Note	- Lowest memory	address = (	)0	•
				Services
Soft	ware must add 1(	,000 to the	desired	Base and
Lini				
	RMATION		DIGITS	
Base	Address		00-05	
SOTE	ware Use		12-13	i
Memo	ry Area Status 1	able Number	14-19	i -
The f	Base and Limit a	ddresses of	the User	Services
Memo requ addr		entry are mo ent to provid	id 1,000 ie absolu	and do not te memory
	A BASE INDICAN "Some values V3 - Base and CAEX USER SERVICE The first en describes th V3 - INFO Base Limi Soft Note The Memo Soft Limi V5 - INFO Base Limi Soft	APPENDIX A - COMP BASE INDICANT VALUES "Some values of the Base Ind V3 - Base Indicant values and will cause a CAEX = 13). USER SERVICES MEMORY AREA TA The first entry in the User describes the environment of V3 - INFORMATION Base Address Limit Address Software Use Note - Lowest memory The Base and Limit a Memory Area Table er Software must add 10 Limit values to prov V5 ¹ - INFORMATION Base Address Limit Address Software Use Memory Area Status T The Base and Limit a	APPENDIX A - COMPATIBILITY NO BASE INDICANT VALUES "Some values of the Base Indicant digit V3 - Base Indicant values of "8 - F" and will cause an Address CAEX = 13). USER SERVICES MEMORY AREA TABLE ENTRY The first entry in the User Services M describes the environment of the MCP Dat V3 - INFORMATION Base Address Limit Address Software Use Note - Lowest memory address = C The Base and Limit addresses of Memory Area Table entry are mod Software must add 10,000 to the Limit values to provide absolute V5 ¹ - INFORMATION Base Address Limit Address Software Use Memory Area Status Table Number The Base and Limit addresses of	<ul> <li>"Some values of the Base Indicant digit may be i</li> <li>V3 - Base Indicant values of "8 - F" are reand will cause an Address Error CAEX = 13).</li> <li>USER SERVICES MEMORY AREA TABLE ENTRY</li> <li>The first entry in the User Services Memory A describes the environment of the MCP Data Area a</li> <li>V3 - INFORMATION DIGITS         <ul> <li>Base Address</li> <li>00-04</li> <li>Limit Address</li> <li>Software Use</li> <li>Note - Lowest memory address = 00</li> <li>The Base and Limit addresses of the User Memory Area Table entry are mod 1,000.</li> <li>Software must add 10,000 to the desired Limit values to provide absolute memory</li> <li>V5 ¹ - INFORMATION DIGITS</li> </ul> </li> </ul>

	an a	
BURRCUGHS CORPORATION	+	1997 5390
YSTEM DEVELOPMENT GROUP		
PASADENA PLANT	V SERIES INSTRUCTION SET	A the Let
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COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 406

APPENDIX A - COMPATIBILITY NOTES (Continued)

A.34 NEMORY AREA TABLE ENTRY FORMATS

V3 — The format of each Original entry is as follows:

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	ر. پېچېرې تاريخ چره استان او استان	INFORMATION	na an a	DIGITS
		Base Address		00-04
	. San and the	Limit Addres	<b>S</b>	05-09
		Software Use		10-13
		Memory Area	Status Table Ni	umber 14-19
an a	ىرىيەتىرىيەتىرىيەتىرىيەت يەرىپىيەت بىركىيەتىرىيەت	n an	الم المراجع الم المراجع الم	

Note - Lowest memory address = 00

Software must add 10,000 to the desired Base and Limit values to provide absolute memory addresses.

VS - INFORMATION DIGITS Base Address 00-05 Limit Address 06-11	Software Use	12-13
이 같은 것 같은 바람들은 것을 가지 않는 것 같은 것 같	Limit Address	06-11
VS - INFORMATION DIGITS	Base Address	00-05
VS - INFORMATION DIGITS	이 영어가 지수는 활동을 물건을 가지 않는 것이 모르는 것이다.	
	VS - INFORMATION	DIGITS

Memory Area Status Table Number 14-19

Note - Lowest memory address = 00

> An Original entry is indicated if the most significant digit of the entry has a value of

The Base and Limit addresses in an Original entry are mod 1,000 and do not require any adjustment to provide absolute memory addresses.

		+
URROUGHS CORPORATION	+	1997 5390
SYSTEM DEVELOPMENT GROUP Asadena plant	V SERIES INST	RUCTION SET
OMPANY CONFIDENTIAL SY	STEM DESIGN SPECIFICAT	ION REV. A PAGE 407
AP	PENDIX A - COMPATIBILI	IY NOTES (Continued)
A.34 MEMORY AREA T	ABLE ENTRY FORMATS (C	ontinued)
an a		
V3, V5 - The foll		y descriptor entry is as
INFO	RMATION	DIGITS
Туре		00a
	rved	01
	ronment Number ry Area Number	02-07 08-09
	ware Use	10-19
Note	- Lowest memory addres	ss = 00
The T "C".	ype digit of a "C" Copy	y entry is equal to
		· · · · ·
V3, V5 - The foll		y descriptor entry is as
INFO	RMATION	DIGITS
Туре		00
	Lute Address of next	
	ined MAT entry ware Use	01-09 10-19
가 있는 것은 가 있는 것이 있다. 이 가 있는 것은 것은 것은 것은 것은 것은 것이 있는 것이 같이 있는 것이 같이	- Lowest memory addres	
"E".	ype digit of a "E" Copy	v entry is equal to
the second s	· · · · · · · · · · · · · · · · · · ·	

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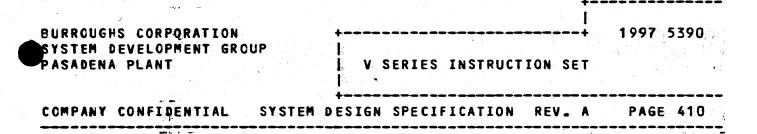
1 BURROUGHS CORPORATION -+ 1997 5390 SYSTEM DEVELOPMENT GROUP ASADENA PLANT **V** SERIES INSTRUCTION SET T. 4 COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A PAGE 408 APPENDIX A - COMPATIBILITY NOTES (Continued) A-34 MEMORY AREA TABLE ENTRY FORMATS (Continued) V3, V5 - The format of each Memory Area Fault entry is as follows: المعياف البيمين المعالم ومعليكي المعظم والمعيان والمجهور المراجع والمعارية INFORMATION DIGITS Туре . 01 Reserved 02-09 Faulted Area Table Address -10-13 Software Use Memory Area Status Table Number 14-19 Note - Lowest memory address = 00 The Type digit of a Memory Area Fault entry is equal to "F". W3, W5 - The format of each Unused entry is as follows: INFORMATION DIGITS Type Reserved (must be zer Software Use 00 Reserved (must be zero) 01-09 10-19 Note - Lowest memory address = 00 The Type digit of an Unused entry is equal to "B". Use of all other Type digit values is reserved and will cause an Invalid Instruction fault (IEX = 50 or 60). 

	S. CORPORATION	<b>4</b>	+   + 1997 5390
PASADENA	DEVELOPMENT GROUP A Plant	V SERIES INSTRUCTI	ON SET
COMPANY	CONFIDENTIAL SYSTE	EM DESIGN SPECIFICATION	REV. A PAGE 409
۰ ۰ ۰ ۰۰۰۰۰۰	APPEN	NDIX A - COMPATIBILITY NO	TES (Continued)
A.35	ABSOLUTE ADDRESS	SES	
	the "Sul	ain absolute address fiel b-Base Zero Memory" (curr en added to each addres	ently 10,000) must
and an annual second second Second second second Second second		digit absolute address of ach Reinstate List Entry.	
	2. The eight of Table in ea	digit absolute address of ach Environment Table Ent	the Memory [®] Area
	3. The Mod 1K Memory Area	Base and Limit fields a Table Entry.	in each original
A_36	TIME OF DAY COUN	NT RATE	
	microse	e of Day timer value is i millisecond rather tha cond and the three least time field will be set to	n by one every significant digits
	every m	e of Day timer value is i icrosecond.	ncremented by one
A_37	LOCK/UNLOCK		
	not be u	k Status Field of the Loc used to determine if the	lock is available.
A-38	REINSTATE LIST	ENTRY SPECIFICATIONS	
		nstate List Entry Size is te List may not exceed o	

Reinstate List may not exceed one million digits in size. The address of the Reinstate list must be mod 1000.

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APPENDIX A - COMPATIBILITY NOTES (Continued)

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35.0

_BF = OO System Status

A.40

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SST

183 - The processor will store, maximum, a one byte status indicator. (No padding is required for the remaining 99 bytes.)

BF = Of System I/D

٧3 - The processor will not store the Serial Number or the Firmware Level. The character string "V310", "V340", or "V380" will be stored tert justified with blank fill in the Processor Type field depending upon the performance level of the machine. The character string "A" will be stored left justified with blank fill in the Specification Level field. operation level field.

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	ELOPMENT GRO		V SERIES	S INSTRUCTI	ON SET	
OMPANY COL	NFIDENTIAL	SYSTEM	DESIGN SPECI	FICATION	REV. A	PAGE 411
		APPENDI	X A - COMPAT	IBILITY NO	TES (Co	ntinued)
		an aga ann				8.8.5
A_43	DIFFERENT	REFERENC	ES ARE RECAL	CULATED		28.3
		e follow	ing referenc	es will be	recaldú	Latedi
			instate List		nter	<u>.</u>
			nment Table Entries in t		ironment	Table.
	(0		nt must be or a Virtua 1.			
A.44	TASK STATE	E MAINTAI	NED WITHIN T	HE PROCESS	OR	
			Base/Limit processor.	entries ar	e not	maintained
			Memory Area ined within			t entries
A.45	TASK TIMER	R FAULT				
. · · · · ·	v3 -	,				
	NC	task ti	ner fault wi	ll occur.		
· · · · · ·			fault will lice expires		999 seco	nds after
		e en			•	

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	EVELOPMENT GROU			SERIES I	NSTRUCT	ION SET	
OMPANY	CONFIDENTIAL	SYSTEM	DESIGN	SPECIFI	CATION	REV A	PAGE 412
	r då dørate att de state att dørate og att de state og att de state att dørate a					ینه هی مزیر می بود می می می می می	
	an a	APPEND	LX A - C	COMPATIB	ELITY N	OTES (Co	ntinued)
A.46	REINSTATE	LIST		n an	an a	an a	
	Each Rein information						following
	<b>V3/V5 - Di</b>	ait	Purpos	5 e:			
				· ·	je se	n an	
	.9.						
		-007				te List E	ntry
	n da se <b>se</b> se al al al al al anticipada de la seconda de	008		ault Pe	nding F	Lag	and a sec
	1.	009 -015	1/0 FL	-		<b>-</b>	
		-015					ent Table ansion Area
		-027		onment T		· · · · · ·	ansion area
	$a = a \cdot c$	-037				R/D Area	н
	028			rocesso			• . • .
		-043		Number O			
	· · ·	-047		ask on I	-		
	048	-049	State	Indicat	0 <b>r</b>		
	1 050	-053	MCP	Canonica	Lock	Number	
	054	-057	User C	Canonica	Lock	Number	
		-061		ting Cla			
		-070		Schedule		ime	
		-076		ait Tim			· · · · ·
	077			ime Slic		• • • •	
		-090		t Time A			ал т - 2. Так
	091					Save Area	
		-101 -105		Software Task Numi			
		-113		fime SLi		ining	
	₹ 106· 114			Interrup:			
	114			-Accumul			
		-149		-Measure		aister	
	.150			Interru		-	ener e energia e e
	152					egisters	
		-185	-	-Mode In	dicator	S	
		-187		-COM & 0			
	188					ment Numb	er
	194	-199	-	-Instruc	tion Ad	dress	

RRCUGHS CORPORATION STEM DEVELOPMENT GROU SADENA PLANT		RIES INSTRUCT	ION SE	+ - <b>™*997**539(</b> 110, <b>**</b> *0, 2= T	]:2.∜
MPANY CONFIDENTIAL	SYSTEM DESIGN SE	PECIFICATION	REV.	A PAGE 41	3 1.84
	APPENDIX A - COM	PATIBILITY N	OTES	(Continued)	
A-46. REINSTATE	IST (Continued)				с 1. <b>1</b> 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.
	te Indicator fiel the following i		nstate		,
Value	Purpo	o s e		an a	
00 01 02 03 04 05 06 07 08-00 00	Runat Waiti Dozir Waiti Failo Kerne Inval Reser Waiti	ing Lock ing Event ng ing Terminati ed Hardware C el Entry Lid Virtual B	all	Reinstate	

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BURROUGHS CORPORATION -+ 199795390 YSTEN DEVELOPMENT GROUP V SERIES INSTRUCTION SET ASA PENA PLANT

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+----COMPANY CONFIDENTIAL SYSTEM DESIGN SPECIFICATION REV. A. PAGE 414 Ye

> APPENDIX A - COMPATIBILITY NOTES (Continued)

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MEMORY AREA STATUS TABLE ENTRY A.47

بالمتحدث والمحج والمحاج والمحاجب والمحاجب

A Memory Area Status Table entry contains the following information. . . .

	Digit	Bit	Purpose
san a sa <b>ra</b> g	00-01	n na Nagi shara w	Hardware Lock (For use by processor)
	02_	3	Memory Area Present
	02	2	To be Rolled Out
and the second second	02	1	Reserved
	02	0	I/O Inhibited Memory Area
	03-05	al de se	Software Usage
ارد. مراجع محمد بروی میرود میرود میرود.	06-09	n na na sana na sana na sana na sana sa	Number of I/O's in Process
	10-13		Task Number of Owner
	14-19		Environment Number of Original
and a second	20-21		Nemory Area Number of Original
	22-25		Memory Area Size
	26-39		Available

Note - The lowest memory address = 00

and the second second

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PANY CONFIDENTIAL SYSTEM	DESIGN SPECIFICATION REV. ALAXTPAGER415 YA
	IX A - COMPATIBILITY NOTES (Continued)
A_48 ENVIRONMENT TABLE	scription is of an Environment sTable
entry.	
	V3, V3
V3 - Digit Bit	
08-09	Memory Area Table Address Number of Entries in the Memory Area Table Reserved
10	Reserved
e statistica in the second	Copy Protection Digit
2	Reserved Source Copy Enable
	Destination Write Enable Reserved
그는 것은 것은 것을 가지 않는 것이 없는 것이 없다.	The Lowest memory address = 00
josesto ed nett≁ i 1.1.199.¥5+tj:Digit n Bil	t Purpose
19546 C F	• • • • • • • • • • • • • • • • • • •
00−08 0010 00−08 00000000000000000000000	Memory Area Table Address Number of Entries in the
5.9 5.9 2	Reserved by bbA a 3
- 273_110 <b>1 1</b> .	Source Copy Enables (195)
12-19	Reserved
Note -	The lowest memory address = 00
•	$\mathcal{T}^{(1)}$ is a transformed parallel of $\mathcal{D}$
	na service and a service se

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CMPANY CONFIDENTIA	SYSTEM O	ESIGN SPECIFICAT	TION REV. A PAGE 416
ι∵εμη ( -\ <b>η C</b>		A — COMPATIBILI	LTY NOTES (Continued)
A-50 TRACE F	AULT DATA		
			i on the stack on trace
V3, V5			
	HARDWARE	DATA FORMAT	DESCRIPTION
1#2. •	- 121	OCOIAAAAAA	Program counter; I = Base Indicant
<b>122</b>		OPAFBFXXXX	OPSYL with final AF/BI (fully resolved)
132	- 141	CXOIAAAAAA	Non-literal data operand ASYL
		LEELLXXXX	Literal ASYL
		OXOIAAAAAA	Branch Address
and a set of the set of	an analysing filling a start and start a	CXOIAAAAAA	BSYL - can be other info depending on OP
			CSYL - can be other info depending on OP
162	- 191		Reserved
sig Fes	nificant two aining bits		lved (the least ne operand data type. The and may contain non-zero
	ues.)		
A = Add	ress digits		*** <b>\$</b> #
	odified lite	ral	
X = Don	't care	an an an an Araba an Araba an Araba an Ar	a and a second

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ASADENA PLANT	ROUP	IES INSTRUCTION SET
OMPANY CONFIDENTIAL	SYSTEM DESIGN SP	ECIFICATION PRÉV. PAISMPAGE 417:3484
	na 1945 - Andrew Stephens, ang setatu ang setatu 1946 - Andrew Stephens, ang setatu ang setatu ang setatu ang setat	
	12) - Enders Alexandri, en	PATIBILITY NOTES (Continued)
A-51 MEMORY	REA FAULT HARDWARE	CALL PROCEDURE
· · · · · · · · · · · · · · · · · · ·	Task Number is alwa	●学校の「「「「「」」」、「「」、「「「「」」、「「」、「「」、「「」、「」、「」、「」
€ 1. VS 1 1 1 +	Task Number is repo	rted accurately: -\Duesde
		NOL 2011 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 -
	UNDIGITS IN BRANCH	ADDRESS SYLLABLES
B2900/-	Undigits in branch	addresses other than the address
B3900	controller or exten cause an address er	ded digit positions will always ror.
		addresses other than the address
		ded digit positions will only he branch is taken.
A.53 MEMORY A	<b>DDRËSSABILITY</b>	
B4800 -		dress 10 million digits. Only physically attached.
82900/- 83900/ 84900	This machine can attached 10 million	address and have physically digits.
¥3 -		dress 100 million digits. Only physically attached.
	640 million digits	dress 1 billion digits. Up to can be physically attached per
	INFORMATION	DIGITS
	Constant-1	00-05
	"A" Absolute Addres	s 06-13
	"B" Absolute Addres Constant-2	s 14-21 22-29
	Note - The lowest m	emory address = 00

BURROUGHS CORP YSTEM DEVELOP Asadena plant	ORATION	I V SERIES INSTRU	
COMPANY CONFID	ENTIAL VSYSTEM	DESIGN SPECIFICATIO	NI REV. A BAGE 418
			in a sense and an
	APPENDI		NOTES (Continued)
A_54 HA	NDLING OF THE SI	GN DIGIT IN ILD/IST	/RLD/RST
		ay be loaded and re he accumulator.	covered from the sign
83 84	900/ accumulato 900/ accumulato / Store inst	or will be stored a or and will be reco	ne sign digit of the is a "C" or "D" in the overed as such via a
	INFORMATIC	) National de la companya	DIGITS
	#A" Addres "B" Addres Constant-2	(Moved) ss (Converted) ss (Converted) (Moved) ea Status Table Numb	14-21 22-29
	Note - The	e lowest memory addr	ess =, 00

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