Burroughs Corporation

ELECTRODATA M & E DIVISION
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CHANGE SHEET

TITLE B5500 PROCESSOR MAINTENANCE TEST ROUTINE SYSTEM

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1 INTRODUCTION

1.1 General

The two major parts of the "MTR System," (1) the Maintenance Test Routines (basic and general), and (2) the MTR Support, are summarized in this specification. Detailed specifications are given in the related documents.

1.2 Related Documents

B5500 Processor Basic MTR Specification, 11187275

B5500 Processor General MTR Specification, 11187283

B5500 Processor MTR Support Specification, 11212818

The first two detailed specifications refer to the testing of processor hardware by the Maintenance Test Routines.

The third detailed specification is concerned with the initial creation and the upkeep of the MTR's themselves. Thus, only the first two documents are of interest for the field engineer.

2 GENERAL DESCRIPTION

2.1 Organization of the MTR System

In this context, the term "MTR System" denotes a combination of two things:

(1) the Maintenance Test Routines (basic and general) and
(2) the MTR Support programs and procedures.

2.2 MTR Objective, Scope, and Approach

The objective of the B5500 Processor Maintenance Test Routines is to effectively aid the user in the initial proving out, in the periodic confidence checkout, and in the corrective maintenance, of the processor hardware.

The overall scope of the maintenance tests is to detect and facilitate the diagnosis of a well-defined set of "common" hardware failures which may occur in a B5500 processor under well-defined "normal" operating conditions.

The approach in the maintenance tests is as follows:

2.2 MTR Objective, Scope, and Approach (Con't.)

(1) Assume the proper working of specific minimum system hardware,

(2) through the execution of the four basic tests, verify the assumptions plus the proper working of further basic logic areas,

(3) relying on the so proven "MTR hardware," verify the correct working of all processor functions through the execution of the general MTR.

2.3 Basic Tests

The four basic test routines are a string of 661 individually devised and carefully sequenced short programs (test cases). The division of the string into four "routines" was dictated solely by memory loading limitations. Each short program may have several exits, one (linked to the next test case) corresponding to no failure, while the others (terminating in error halts) to specific single component failures. Thus, error detection and identification are accomplished together but with the limitation that only single failures are always properly handled.

The basic tests cover 15-20% of the processor logic.

The basic tests are stored at the beginning of the B5500 MTR test tape.

2.4 General Tests

One general control routine (GCR) plus over 15,000 "general" test cases make up the general tests. The functions of GCR are the loading of test case groups and the setting up, execution, evaluation, and error flagging of individual test cases. In performing these functions, GCR uses the previously proven "basic" computer logic. All failure modes route GCR to a common error-handling path. Thus, GCR is capable of detecting and handling even multiple failures. On the other hand, failure diagnosis is apparently less detailed in GCR than in the basic tests. Reasonable diagnostic detail can still be achieved in the general tests through an interplay of man, machine, and documents. The general control routine and its associated test cases are stored on the B5500 Processor MTR test tape, following the basic tests.

2.5 MTR Use, MTR Documentation

A single MTR tape loader (itself loaded from cards) is provided to initiate the execution of all (basic and general) tests. This is the normal use of the MTR's.

2.5 MTR Use, MTR Documentation (Con't.)

Manual loading from tape is possible (using a working I/O channel). This is to be done only if the card reader or the basic processor functions fail.

Loading of each basic test from cards is a back-up provision. The general tests (GCR and test cases) are not available on cards.

One or two processors (with from two to eight consecutive memory modules) can be tested. Test cases not applicable to a particular system configuration are automatically skipped. Tape unit and I/O channel designations are optional. Card reader and supervisory printer are very desirable.

MTR documentation is provided in the specifications and in the three-volume MTR manual. Knowledge of the proper use of the manuals is essential for efficient troubleshooting.

2.6 MTR Support: Objectives, Scope, and Approach

The objectives of the MTR support programs and procedures are partly included in the name. Besides the original development work, these aids are essential in maintaining the test routines in case of logic changes in the processor.

With the exception of logic book manipulation, the scope of MTR Support is limited to the general test area. Within this area, MTR Support is useful in test case development, filing, verification, maintenance, manipulation by contents, sequencing and sorting, allocating (memory), and documentation (with automatic change control).

The approach in test case development includes machine tasks (logic explosion) and manual tasks. Once the test case information is available on cards, its filing, verification, (error flagging) maintenance, manipulation by contents, sequencing and sorting, and memory mapping can be programmatically accomplished (Project Assistance Routine, PAR). Various printed reports can also be obtained through PAR.

The approach in test case documentation is entirely programmatic. The creation of the test case Error Reference Manual (ERM) involves the collecting of changes from the PAR tape files, file splitting, sorting into execution sequence, automatically assigning page numbers (with revision letters), producing the change pages and change indices, and updating the ERM tape files. Creating (updating) of the MTR test tape is accomplished in a final program pass.