

UNISYS

A 12 A 15 Systems

Hardware
Operational
Guide

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Customer Services Engineering
Restricted/Proprietary Data

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UNISYS

**A12, A15
Systems**

**Hardware
Operations
Guide**

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Description

The pages provided with this PCN contain changes to the A 12, A 15 Systems Hardware Operational Guide, form 1192432, dated October, 1986. Locations of changes are indicated by black vertical bars on the replacement pages.

Replace These Pages

Title

4-3

6-7

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3-1 thru 3-37	Original
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4-3	PCN-001
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SECTION 1

CENTRAL PROCESSOR MODULE

PRIMARY MODE OPERATORS

	0	1	2	3	4	5	6	7
8	ADD	SUBT	MULT	DIVD	IDIV	RDIV	NTIA	NTGR
9	LAND	LOR	LNOT	LEQV	SAME	VARI	BSET	DBST
A	BRFL	BRTR	BRUN	EXIT	ICUD	NXLN	INDX	RETN
B	ZERO	ONE	LT8	LT16	PUSH	DLET	EXCH	DUPL
C	SCLF	DSLFL	SCRT	DSRT	SCRS	DSRS	SCRFL	DSRFL
D	TEED	PACD	EXSD	TWSD	TWOD	SISO	SXSN	ROFF
E	TLSD	TGED	TGTD	TLED	TEQD	TNED	TUND	INXA
F	CLSD	CGED	CGTD	CLED	CEQD	CNED	STAD	STAN

	8	9	A	B	C	D	E	F
8	LESS	GREQ	GRTR	LSEQ	EQUL	NEQL	CHSN	MULX
9	FLTR	DFTR	ISOL	DISO	INSR	DINS	BRST	DBRS
A	DBFL	DBTR	DBUN	ENTR	EVAL	NXLV	MKST	STFF
B	STOD	STON	OVRD	OVRN	LODT	LOAD	LT48	MPCW
C	SCRR	DSRR	ICVD	ICVU	SNGT	SNGL	XTND	IMKS
D	TEEU	PACU	EXSU	TWSU	TWOU	EXPU	RTFF	MKSN
E	TLSU	TGEU	TGTU	TLEU	TEQU	TNEU	TUNU	NXVA
F	CLSU	CGEU	CGTU	CLEU	CEQU	CNEU	NOOP	NVLD

VARIANT MODE OPERATORS

	0	1	2	3	4	5	6	7
4	ZIC	RJNI	JOIN	SPLT	IDLE	SINT	EEXI	DEXI
7	UPLD	UPRD	PKUD	PKLD	PKRD	ICRD	ICLD	BCD
8	ASRT	RSNR	RNGT	DRNT	PAUS	OCRX	NTTD	NTGD
9		SEND	REMC	WEMC	REMT	WEMT		
A					WATI			RTOD
B	LOK		UNLK		STAG	RTAG	RSUP	RSDN
D	USND	UPUD	TWFD	TWTD	SWFD	SWTD		TRNS
F	SLED	SGED	SGTD	SLED	SEQD	SNED	DLAY	

	8	9	A	B	C	D	E	F
4		WTOD					WHOI	
7	UPLU	UPRU						DBCD
8	AMIN		AMAX	LOG2	LNMC	LVLC	NORM	
9	RIPS	WIPS	RASD	WASD				CSCP
A		BMS		HASH		EAAE		MVST
B	RPRR	SPFR	RDLK	CBON	LODT	LLLU	SRCH	STOP
D	USNU	UPUU	TWFU	TWTU	SWFU	SWTU	SHOW	HALT
F	SLSU	SGEU	SGTU	SLEU	SEQU	SNEU	NOOP	NVLD

NEW OPERATORS FOR ASD OPERATING SYSTEM

RASD V(9A)
 WASD V(9B)
 EAAE V(AD)
 BMS V(A9)
 HASH V(AB)

DEIMPLEMENTED OPERATORS FOR ASD OPERATING SYSTEM

REMT V(94)
 WEMT V(95)

ASD OPERATING SYSTEM ONLY

LOK V(B0)
 UNLK V(B2)

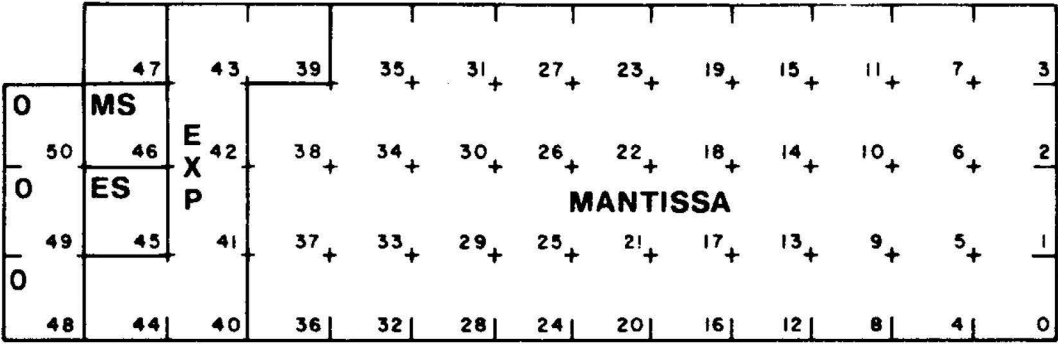
E745J

EDIT MODE OPERATORS

	0	1	2	3	4	5	6	7
D	MINS	MFLT	SFSC	SRSC	RSTF	ENDF	MVNU	MCHR
F								

	8	9	A	B	C	D	E	F
D	INOP	INSG	SFDC	SRDC	INSU	INSC	ENDE	HALT
F							NOOP	NVLD

FOR ASN AND ASD OPERATING SYSTEM SINGLE PRECISION OPERAND

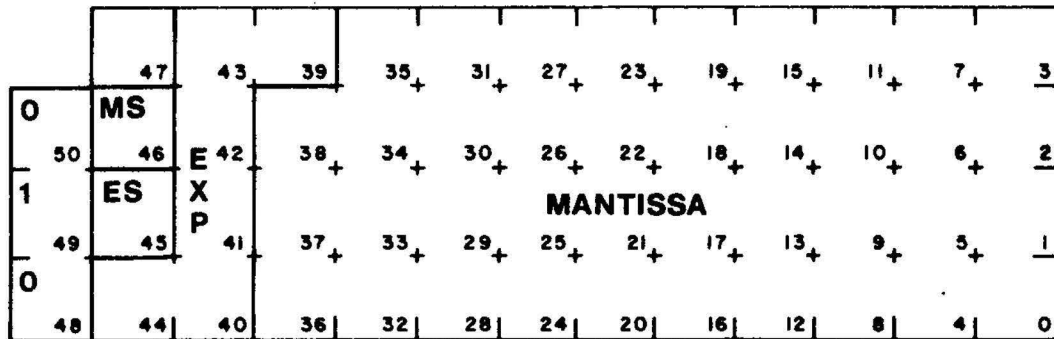


- TAG 50:3 000
- MS 46:1 MANTISSA SIGN (0 POSITIVE, 1 NEGATIVE)
- ES 45:1 EXPONENT SIGN (0 POSITIVE, 1 NEGATIVE)
- EXP 44:6 POWER OF EIGHT TO WHICH THE MANTISSA IS SCALED
- MANTISSA 38:39 MAGNITUDE OF THE NUMBER BEFORE SCALING
NOTE: OCTAL POINT IS AT THE RIGHT OF BIT 0

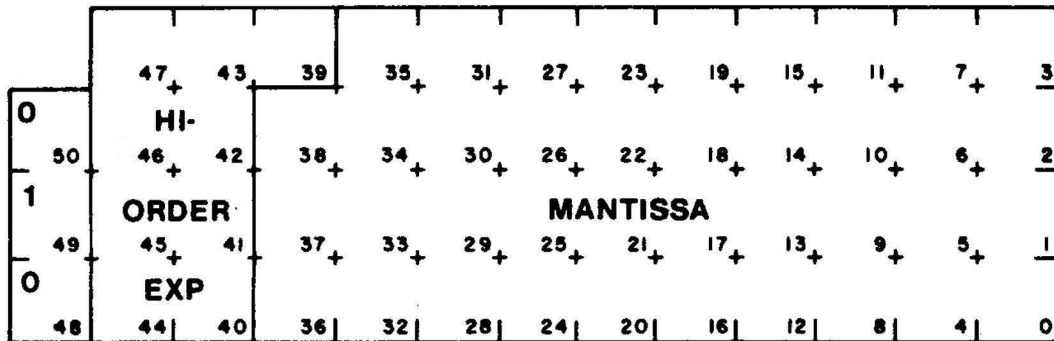
E3318

DOUBLE PRECISION OPERAND

1st WORD



2nd WORD



1st WORD

TAG	50:3	010
MS	46:1	MANTISSA SIGN (0 POSITIVE, 1 NEGATIVE)
ES	45:1	EXPONENT SIGN (0 POSITIVE, 1 NEGATIVE)
EXP	44:6	LOW-ORDER SIX BITS OF THE EXPONENT
MANTISSA	38:39	INTEGRAL PORTION OF THE MANTISSA

2nd WORD:

TAG	50:3	010
HI-ORDER EXP	47:9	HIGH-ORDER NINE BITS OF THE EXPONENT
MANTISSA	38:39	FRACTIONAL PORTION OF THE MANTISSA

E5847

TAG 4 WORD

1	47+	43+	39+	35+	31+	27+	23+	19+	15+	11+	7+	3
50	46+	42+	38+	34+	30+	26+	22+	18+	14+	10+	6+	2
0	(MAY BE INTERPRETED AS A BIT VECTOR)											
49	45+	41+	37+	33+	29+	25+	21+	17+	13+	9+	5+	1
0												
48	44	40	36	32	28	24	20	16	12	8	4	0

E3320

TAG 6 WORD

1	47+	43+	39+	35+	31+	27+	23+	19+	15+	11+	7+	3
50	46+	42+	38+	34+	30+	26+	22+	18+	14+	10+	6+	2
1	(MAY BE INTERPRETED AS A BIT VECTOR)											
49	45+	41+	37+	33+	29+	25+	21+	17+	13+	9+	5+	1
0												
48	44	40	36	32	28	24	20	16	12	8	4	0

E3321

FOR ASN OPERATION SYSTEM UNINDEXED (ORIGINAL OR COPY) DD

	PR	RO											
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE											
	50	46	42	38	34	30	26	22	18	14	10	6	2
0	I	S	LENGTH				ADDRESS						
	49	45	41	37	33	29	25	21	17	13	9	5	1
1	PG	E											
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
PR	47:1	PRESENT BIT (0 = ABSENT, 1 = PRESENT).
C	46:1	COPY BIT (0 = ORIGINAL, 1 = COPY)
I	45:1	INDEXED BIT (0 = UNINDEXED)
PG	44:1	PAGED BIT (0 = NONPAGED, 1 = PAGED)
RO	43:1	READ ONLY BIT (0 = READ-WRITE, 1 = READ ONLY)
ELEMENT SIZE	42:3	TYPE OF ARRAY ELEMENT (0 = SINGLE PRECISION, 1 = DOUBLE PRECISION, 2 = HEX. 4 = EBCDIC, (3,5,6,7) ARE INVALID).
LENGTH	39:20	NUMBER OF ELEMENTS IN THE ARRAY.
ADDRESS	19:20	ADDRESS INTERPRETATIONS ARE: 1. PRESENT, THE NOMINAL ADDRESS OF THE BASE WORD OF THE DATA SEGMENT. 2. ABSENT AND COPY, THE NOMINAL ADDRESS OF THE ASSOCIATED ORIGINAL DESCRIPTOR. 3. ABSENT AND ORIGINAL, ENCODED BY SOFTWARE.

E5323

CODE SEGMENT DESCRIPTOR

	PR											
	47	43	39	35	31	27	23	19	15	11	7	3
0	C					SEG				ADDRESS		
	50	46	42	38	34	30	26	22	18	14	10	6
1						LENGTH						
	49	45	41	37	33	29	25	21	17	13	9	5
1												
	48	44	40	36	32	28	24	20	16	12	8	4
												0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
PR	47:1	PRESENT BIT (0 ABSENT, 1 PRESENT)
C	46:1	COPY BIT (0 ORIGINAL, 1 COPY)
-	45:13	RESERVED FOR SOFTWARE
SEG LENGTH	32:13	NUMBER OF CODE WORDS IN THE SEGMENT.
ADDRESS	19:20	ADDRESS INTERPRETATIONS ARE: 1. PRESENT, THE NOMINAL ADDRESS OF THE BASE WORD OF THE DATA SEGMENT. 2. ABSENT AND COPY, THE NOMINAL ADDRESS OF THE ASSOCIATED ORIGINAL DESCRIPTOR. 3. ABSENT AND ORIGINAL, ENCODED BY SOFTWARE.

E3324

STUFFED INDIRECT REFERENCE WORD

		47	43	39	35	31	27	23	19	15	11	7	3
0									ST			OFFSET	
	50	46	42	38	34	30	26	22	18	14	10	6	2
0	STACK NO				DISPLACEMENT								
	49	45	41	37	33	29	25	21	17	13	9	5	1
1													
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 1.
STACK NO	47:12	IDENTIFICATION OF THE STACK CONTAINING THE REFERENCED LOCATION.
DISPLACEMENT	35:16	DISPLACEMENT FROM THE BASE OF THE STACK TO THE BASE OF THE ACTIVATION RECORD.
	19:1	NOT USED
ST	18:1	STUFFED TYPE BIT. CONSTANT VALUE 1
	17:4	NOT USED
	15:1	RESERVED FOR SOFTWARE USE
OFFSET	12:13	OFFSET FROM THE BASE OF THE ACTIVATION RECORD TO THE REFERENCED LOCATION.

E3326

INDEXED DATA DESCRIPTOR

INDEXED WORD DD (INDEXED WORD DATA DESCRIPTOR)

	PR	RO											
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE											
50	46	42	38	34	30	26	22	18	14	10	6	2	
0	I	SIZE		INDEX					ADDRESS				
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	PG												
48	44	40	36	32	28	24	20	16	12	8	4	0	

POINTER (INDEXED CHARACTER DATA DESCRIPTOR)

	PR	RO	CHAR										
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE	CHAR		WORD								
50	46	42	38	34	30	26	22	18	14	10	6	2	
0	I	SIZE	INDEX		INDEX				ADDRESS				
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	PG												
48	44	40	36	32	28	24	20	16	12	8	4	0	

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
PR	47:1	PRESENT BIT (0 - ABSENT, 1 - PRESENT)
C	46:1	COPY BIT (1:(INDEXED)COPY)
I	45:1	INDEXED BIT (1:INDEXED)
	44:1	MUST BE ZERO
RO	43:1	READ ONLY BIT (0 - READ, WRITE, 1 - READ ONLY)
ELEMENT SIZE	42:3	TYPE OF ARRAY ELEMENT (0 - SINGLE PRECISION, 1 - DOUBLE PRECISION, 2 - HEX, 4 - EBCDIC, AND (3,5,6,7) ARE INVALID VALUES).
INDEX	39:20	USED IF ELEMENT SIZE IS SINGLE OR DOUBLE PRECISION: THE WORD INDEX FROM THE BASE OF THE ARRAY TO THE REFERENCED WORD.
CHAR INDEX	39:4	USED IF ELEMENT SIZE IS EBCDIC OR HEX: THE INDEX WITHIN THE WORD OF THE REFERENCED CHARACTER.
WORD INDEX	35:16	USED IF ELEMENT SIZE IS EBCDIC OR HEX: THE INDEX FROM THE BASE OF THE ARRAY TO THE WORD CONTAINING THE REFERENCED CHARACTER.
ADDRESS	19:20	ADDRESS INTERPRETATIONS ARE: 1. PRESENT, THE NOMINAL MEMORY ADDRESS OF THE BASE WORD OF THE ACTUAL SEGMENT. 2. ABSENT, THE NOMINAL MEMORY ADDRESS OF THE ASSOCIATED ORIGINAL DATA DESCRIPTOR.

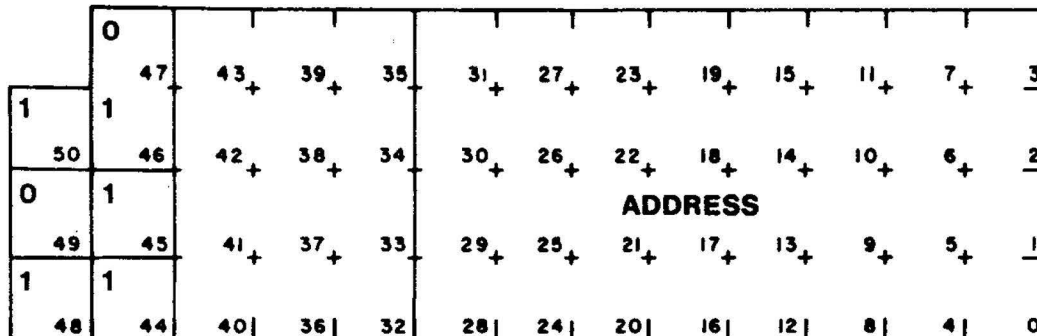
MARK STACK CONTROL WORD

	47	43	39	35	31	27	23	19	LL	15	11	7	3
0	STACK			DISPLACEMENT				E	LL	HISTORY			
50	46	42	38	34	30	26	22	18	14	10	6	2	
1	NUMBER							LL		LINK			
49	45	41	37	33	29	25	21	17	13	9	5	1	
1								LL					
48	44	40	36	32	28	24	20	16	12	8	4	0	

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
STACK NUMBER	47:12	IDENTIFIES THE STACK CONTAINING THE ACTIVATION RECORD TO WHICH THE LEXICAL LINK POINTS.
DISPLACEMENT	35:16	DISPLACEMENT FROM THE BASE OF THE STACK NUMBER STACK TO THE BASE OF THE ACTIVATION RECORD ADDRESSED BY THE LEXICAL LINK STACK.
	19:1	NOT USED
E	18:1	ENTERED BIT (0 = INACTIVE, 1 = ENTERED).
LL	17:4	LEXICAL LEVEL AT WHICH THE ACTIVATION RECORD RUNS.
HISTORY LINK	13:14	DISPLACEMENT DOWN THE CONTAINING STACK FROM THE MSCW TO THE PRIOR MSCW. THE FIRST ENTERED MSCW ON THIS CHAIN DEFINES THE PRIOR TOPMOST (INITIATING) ACTIVATION RECORD.

E3329

FOR ASD OPERATING SYSTEM ABSOLUTE STORE REFERENCE WORD



FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
	47:2	BINARY 01: DENOTES ABSOLUTE ADDRESS CONTAINER
	45:1	1
	44:1	1: DENOTES ASRW.
	31:32	ADDRESS OF MEMORY ITEM

E5848

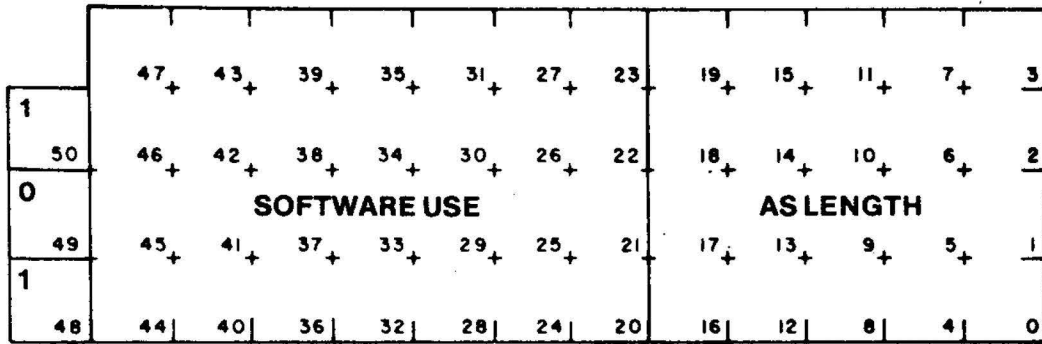
ACTUAL SEGMENT DESCRIPTOR, FIRST WORD

	0	UA																	
		47	43	39		35		31+	27+	23+	19+	15+	11+	7+	3				
1	1		NS				S												
	50	46	42	38		34	O	30+	26+	22+	18+	14+	10+	6+	2				
0	PP	PIO					F												
	49	45	41	37		33	T	29+	25+	21+	17+	13+	9+	5+	1				
1	0	NP																	
	48	44	40	36		32		28	24	20	16	12	8	4	0				

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
	47:2	BINARY 01: DENOTES ABSOLUTE ADDRESS CONTAINER.
PRESENT-TO-PROC	45:1	SEGMENT-IS-PRESENT INDICATOR FOR NON-I/O ACCESS (0 = SEGMENT IS ABSENT, 1 = SEGMENT IS PRESENT)
	44:1	0: DENOTES ASD1
UNALTERED	43:1	ALTERED DATA INDICATOR (0 = ALTERED, 1 = UNALTERED)
NOT STACK	42:1	STACK INDICATOR (0 = STACK, 1 = NOT STACK)
PRESENT-FOR-IO	41:1	SEGMENT-IS-PRESENT INDICATOR FOR USE AS AN I/O BUFFER (0 = SEGMENT IS ABSENT, 1 = SEGMENT IS PRESENT)
NOT-PAGE	40:1	PAGE INDICATOR (0 = PAGE, 1 = NOT PAGE)
ADDRESS	31:32	IF PRESENT-TO-PROC AND PRESENT-FOR-IO ARE BOTH ZERO, THE ADDRESS FIELD IS INTERPRETED BY SOFTWARE; OTHERWISE, IT CONTAINS THE BASE ADDRESS OF THE ACTUAL SEGMENT.

E5849

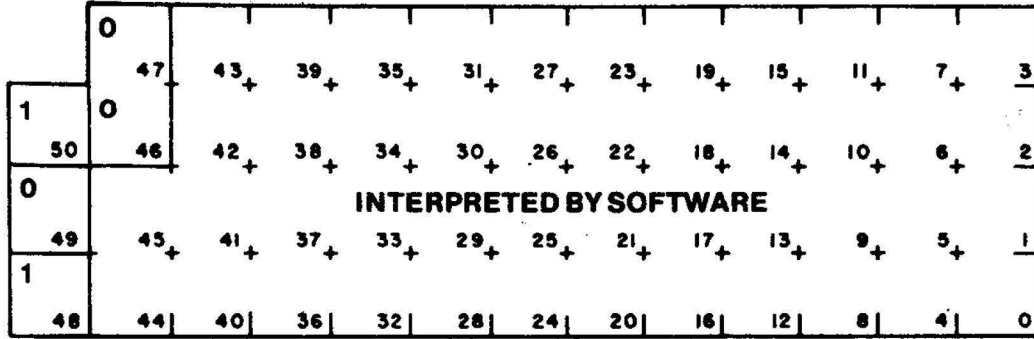
ACTUAL SEGMENT DESCRIPTOR, SECOND WORD



FIELD	BITS	DESCRIPTION
	47:28	RESERVED FOR SOFTWARE USE.
AS LENGTH	19:20	ACTUAL-SEGMENT LENGTH IN WORDS

E5850

UNTOUCHED DD



FIELD	BITS	DESCRIPTION
-------	------	-------------

	47:2	BINARY 00: DENOTES UNTOUCHED DD
--	------	---------------------------------

	45:46	INTERPRETED BY SOFTWARE
--	-------	-------------------------

E5851

UNINDEXED (ORIGINAL OR COPY) DD

	1	RO											
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE											
50	46	42	38	34	30	26	22	18	14	10	6	2	
0	I	S		LENGTH					ASD REF				
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	PG	E											
48	44	40	36	32	28	24	20	16	12	8	4	0	

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
T	47:1	TOUCHED BIT (1 = TOUCHED)
C	46:1	COPY BIT (0 ORIGINAL, 1 COPY)
I	45:1	INDEXED BIT (0 UNINDEXED)
PG	44:1	PAGED BIT (0 NONPAGED, 1 PAGED)
RO	43:1	READ ONLY BIT (0 READ-WRITE, 1 READ ONLY)
ELEMENT SIZE	42:3	TYPE OF ARRAY ELEMENT (0 SINGLE PRECISION, 1 DOUBLE PRECISION, 2 HEX, 4 EBCDIC, (3,5,6,7) ARE INVALID).
LENGTH	39:20	NUMBER OF ELEMENTS IN THE ARRAY.
ASD REF	19:20	ASD REFERENCE FIELD: THE ASD NUMBER

E5852

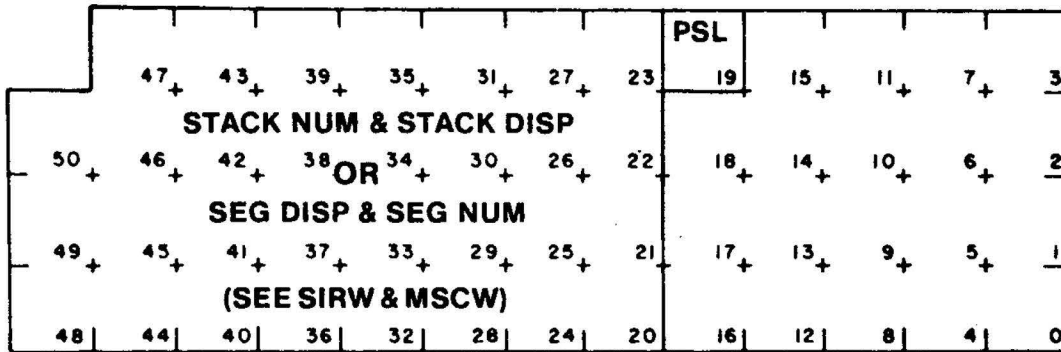
CODE SEGMENT DESCRIPTOR

	T		0	0									
	47	43	39	35	31	27	23	19	15	11	7	3	
0	C		0	0		SEG				ASD REF			
	50	46	42	38	34	30	26	22	18	14	10	6	2
1		SOFT	0	0		LENGTH							
	49	45	41	37	33	29	25	21	17	13	9	5	1
1			0										
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
T	47:1	TOUCHED BIT (1 = TOUCHED)
C	46:1	COPY BIT (0 = ORIGINAL, 1 = COPY)
	45:5	RESERVED FOR SOFTWARE
	40:1	UNDEFINED
	39:7	MUST BE ZERO
SEG LENGTH	32:13	NUMBER OF CODE WORDS IN THE SEGMENT.
ASD REF	19:20	ASD REFERENCE FIELD: THE ASD NUMBER

E5853

ENVIRONMENT LINK



FIELD	BITS	DESCRIPTION
ENV LINK	47:29	FIELD WITHIN SIRW AND MSCW WITH EITHER OF TWO FORMATS:
NORMAL ENVIRONMENT LINK		
STACK NUM	47:12	STACK NUMBER IDENTIFYING THE STACK CONTAINING THE REFERENCED LOCATION
STACK DISP	35:16	DISPLACEMENT FROM THE BASE OF THE STACK TO THE MSCW OF THE NORMAL ACTIVATION RECORD
PSEUDOLINK	19:1	0: DENOTES NORMAL ENV LINK.
PSEUDO ENVIRONMENT LINK		
SEG DISP	47:4	DISPLACEMENT FROM THE BASE OF THE SEGMENT TO THE MSCW OF THE PSEUDO ACTIVATION RECORD
SEG NUM	39:20	ASD NUMBER IDENTIFYING THE SEGMENT CONTAINING REFERENCED LOCATION
PSEUDOLINK	19:1	1: DENOTES PSEUDO ENV LINK.

E5854

STUFFED INDIRECT REFERENCE WORD

	47	43	39	35	31	27	23	19	15	11	7	3	
0				ENV LINK				ST 1		OFFSET			
	50	46	42	38	34	30	26	22	18	14	10	6	2
0													
	49	45	41	37	33	29	25	21	17	13	9	5	1
1													
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 1.
ENV LINK	47:29	DESIGNATES ACTIVATION RECORD IN WHICH REFERENCE OCCURS.
ST	18:1	STUFFED TYPE BIT, CONSTANT VALUE 1
	17:4	NOT USED
	15:1	RESERVED FOR SOFTWARE USE
OFFSET	12:13	OFFSET FROM THE BASE OF THE ACTIVATION RECORD TO THE REFERENCED LOCATION.

E5855

INDEXED DATA DESCRIPTOR

INDEXEDWORD DD (INDEXED WORD DATA DESCRIPTOR)

	1	RO											
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE											
50	46	42	38	34	30	26	22	18	14	10	6	2	
0	I	SIZE		INDEX					ASD REF				
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	PG												
48	44	40	36	32	28	24	20	16	12	8	4	0	

POINTER (INDEXED CHARACTER DATA DESCRIPTOR)

	1	RO	CHAR										
	47	43	39	35	31	27	23	19	15	11	7	3	
1	C	ELE		WORD									
50	46	42	38	34	30	26	22	18	14	10	6	2	
0	I	SIZE	INDEX		INDEX					ASD REF			
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	PG												
48	44	40	36	32	28	24	20	16	12	8	4	0	

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 5.
T	47:1	TOUCHED BIT (1 = TOUCHED)
C	46:1	COPY BIT (1:INDEXED)COPY)
I	45:1	INDEXED BIT (1:INDEXED)
	44:1	MUST BE ZERO
RO	43:1	READ ONLY BIT (0 READ, WRITE, 1 READ ONLY)
ELEMENT SIZE	42:3	TYPE OF ARRAY ELEMENT (0 SINGLE PRECISION, 1 DOUBLE PRECISION, 2 HEX, 4 EBCDIC, AND (3,5,6,7) ARE INVALID VALUES)
INDEX	39:20	USED IF ELEMENT SIZE IS SINGLE OR DOUBLE PRECISION. THE WORD INDEX FROM THE BASE OF THE ARRAY TO THE REFERENCED WORD.
CHAR INDEX	39:4	USED IF ELEMENT SIZE IS EBCDIC OR HEX. THE INDEX WITHIN THE WORD OF THE REFERENCED CHARACTER
WORD INDEX	35:16	USED IF ELEMENT SIZE IS EBCDIC OR HEX. THE INDEX FROM THE BASE OF THE ARRAY TO THE WORD CONTAINING THE REFERENCED CHARACTER
ASD REF	19:20	ASD REFERENCE FIELD. THE ASD NUMBER.

E5856

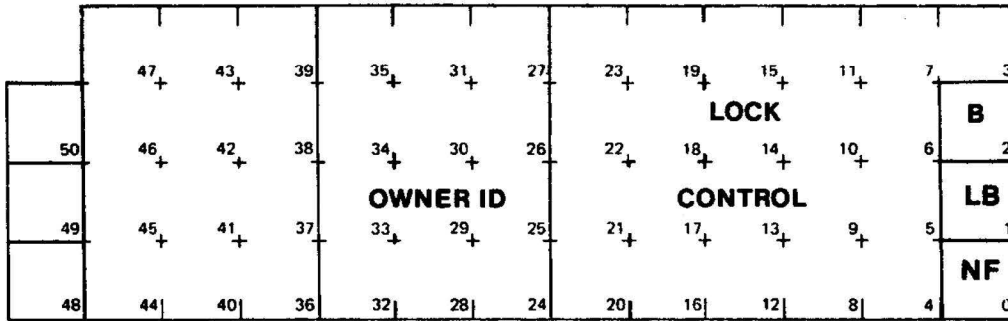
MARK STACK CONTROL WORD

									LL				
	47	43	39	35	31	27	23	19	15	11	7	3	
0					ENV LINK			E	LL	HISTORY			
	50	46	42	38	34	30	26	22	18	14	10	6	2
1									LL		LINK		
	49	45	41	37	33	29	25	21	17	13	9	5	1
1									LL				
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
ENV LINK	47:29	IDENTIFIES THE IMMEDIATE GLOBAL ACTIVATION RECORD (IF LEX LEVEL = 0)
E	18:1	ENTERED BIT (0 = INACTIVE, 1 = ENTERED).
LL	17:4	LEXICAL LEVEL AT WHICH THE ACTIVATION RECORD RUNS.
HISTORY LINK	13:14	DISPLACEMENT DOWN THE CONTAINING STACK FROM THE MSCW TO THE PRIOR (INITIATING) MSCW. THE FIRST ENTERED MSCW ON THIS CHAIN DEFINES THE PRIOR TOPMOST (INITIATING) ACTIVATION RECORD.

E5857

INTERLOCK WORD



FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. ACCEPTED: 0 OR 3, CREATED: 3
OWNER ID	35:12	STACK NUMBER OF LOCK OWNER (OR BUSY CONTENDER)
LOCK CONTROL	23:21	RESERVED FOR SOFTWARE USE.
B	2:1	BROKEN BIT, 1: STATE IS BROKEN
LB	1:1	LOCK BIT 0: STATE IS NOT LOCKED UNCONTENDED 1: STATE IS LOCKED UNCONTENDED
NF	0:1	NOT FREE BIT 0: STATE IS FREE 1: STATE IS NOT FREE

E6109

FOR ASN AND ASD OPERATING SYSTEMS NORMAL INDIRECT REFERENCE WORD

		47	43	39	35	31	27	23	19	15	11	7	3
0									0				
	50	46	42	38	34	30	26	22	18	14	10	6	2
0											ADDRESS		
	49	45	41	37	33	29	25	21	17	13	9	5	1
1											COUPLE		
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 1.
	47:29	NOT USED
ST	18:1	STUFFED TYPE BIT, CONSTANT VALUE 0
ADDRESS COUPLE	15:16	FIXED-FENCE ADDRESS COUPLE OF THE REFERENCED LOCATION IN THE CURRENT ADDRESSING ENVIRONMENT.
LAMBDA	15:4	LEX LEVEL
DELTA	11:12	OFFSET

F5858

PROGRAM CONTROL WORD

				P				CS	LL				
	47	43	39	35	31	27	23	19	15	11	7	3	
1	STACK			S				O	LL		SDI		
	50	46	42	38	34	30	26	22	18	14	10	6	2
1	NUMBER			I		PWI		LL	SDLL				
	49	45	41	37	33	29	25	21	17	13	9	5	1
1								LL					
	48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 7.
STACK NUMBER	47:12	THIS FIELD IS SUPPLIED BY THE MPCW OPERATOR FOR COMPATIBILITY WITH SOFTWARE, BUT IS NOT REQUIRED FOR ANY FUNCTIONAL OPERATION. (FOR ASD OPERATING SYSTEM, THE PCW DOES NOT CONTAIN THE STACK NUMBER.)
PSI	35:3	PROGRAM SYLLABLE INDEX CODE STREAM POINTER COMPONENT
PWI	32:13	PROGRAM WORD INDEX CODE STREAM POINTER COMPONENT
CS	19:1	INITIAL VALUE OF THE CONTROL STATE BOOLEAN (0 - NORMAL STATE, 1 - CONTROL STATE).
INVALID LL	18:1	CONSTANT VALUE 0
LL	17:4	LEXICAL LEVEL AT WHICH THE ACTIVATION RECORD RUNS.
SDLL	13:1	SEGMENT DICTIONARY LEXICAL LEVEL CODE STREAM POINTER COMPONENT
SDI	12:13	SEGMENT DICTIONARY INDEX CODE STREAM POINTER COMPONENT

E5859

RETURN CONTROL WORD

	EX 47	RS 43	EO 39	P 35	31	27	23	CS 19	LL 15	11	7	3
0	OF 50			S 34	30	26	22		LL 14	10	6	2
1	TF 49	BE 45		I 33	29	PWI 25	21	LL 17	SDLL 13	9	SDI 5	1
1	FL 48	EO 44			32	28	24	LL 16		12	8	4
												0

FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
EX	47:1	EXTERNAL SIGN FLIP-FLOP (EXTF)
OF	46:1	OVERFLOW FLIP-FLOP (OFFF)
TF	45:1	TRUE FALSE FLIP-FLOP (TFFF)
FL	44:1	FLOAT FLIP-FLOP (FLTF)
RS	43:1	RESTART INDICATOR (0 = INITIAL, 1 = RESTART STATE)
BE	41:1	ARMS BLOCK EXIT INTERRUPT FROM EXIT OR RETN (0 = DISARMED, 1 = ARMED)
EO	40:2	EXIT OPT BITS, THESE BITS ARE USED FOR OPTIMIZATION OF EXIT BY THE HARDWARE

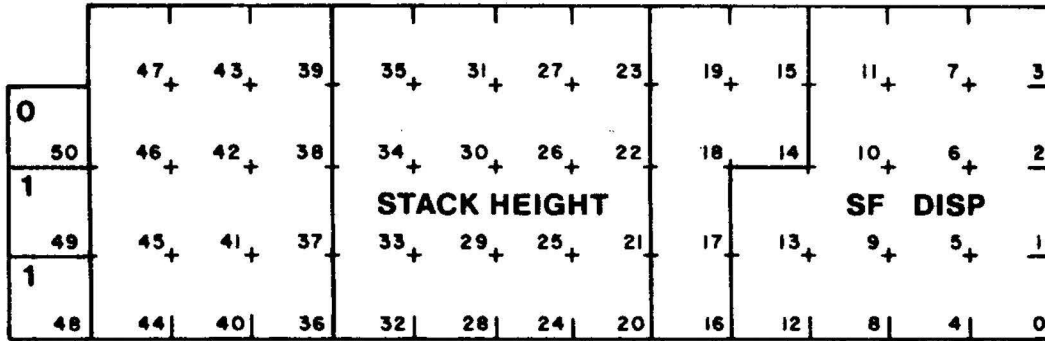
40 39

- 0 0 NO SHORT CUT ON EXIT. DESTROY ALL CURRENT OPTIMIZATIONS AND PERFORM FULL DISPLAY UPDATE.
- 0 1 FETCH CODE DESCRIPTOR USING PREVIOUS SET OF DISPLAYS AND DISTRIBUTE ITS CONTENTS.
- 1 0 FETCH CODE DESCRIPTOR USING CURRENT SET OF DISPLAYS AND DISTRIBUTE ITS CONTENTS.

	38:3	NOT USED
PSI	35:3	PROGRAM SYLLABLE INDEX CODE STREAM POINTER COMPONENT.
PWI	32:13	PROGRAM WORD INDEX CODE STREAM POINTER COMPONENT.
CS	19:1	CONTROL STATE BOOLEAN
INVALID LL	18:1	CONSTANT VALUE 0
LL	17:4	LEXICAL LEVEL OF THE FIRST ACTIVATION RECORD ON THE HISTORICAL CHAIN DEFINED BY MSCW HISTORY LINK.
SDLL	13:1	SEGMENT DICTIONARY LEXICAL LEVEL CODE STREAM POINTER COMPONENT.
SDI	12:13	SEGMENT DICTIONARY INDEX CODE STREAM POINTER COMPONENT.

E3330

TOP OF STACK CONTROL WORD



FIELD	BITS	DESCRIPTION
TAG	50:3	TAG FIELD. VALUE EQUALS 3.
STACK HEIGHT	35:16	DISPLACEMENT FROM THE BASE OF THE STACK TO THE TOP OF THE EXPRESSION STACK.
SF DISP	13:14	DISPLACEMENT FROM THE TOP OF THE EXPRESSION STACK DOWN TO THE HEAD OF THE HISTORICAL CHAIN.

E3331

ID PARAMETER BIT ASSIGNMENTS FOR OPERATOR DEPENDENT INTERRUPTS

Field/Bits	Description
SUBTYPE/ 15:4	The subtype of ODI is defined as required for each value of ODI type.
INT TYPE/ 11:12	0 = Presence Bit 1 = Paged Array
	[12:1] 1 = page referenced by P2 was being written
	[13:1] 1 = length is word count 0 = length is character count
	[14:1] 1 = length is at F-2 0 = length is at F-1
	[15:1] 1 = operator was skip reverse
	([14:2] is only valid if [12:1] = 1)
	2 = Stack Overflow
	3 = Invalid Operator
	4 = Undefined Operator
	5 = Invalid Stack Argument
	6 = Invalid Argument Value
	7 = Invalid Code Parameter
	8 = Invalid Reference
	9 = Invalid Reference Chain
(Hex)	12:1 = 1: operator was ENTR
A	10 = Invalid Index
B	11 = Memory Protect
C	12 = Divide by Zero
D	13 = Exponent Underflow
E	14 = Exponent Overflow
F	15 = Integer Overflow
10	16 = Stack Underflow
11	17 = Not used
12	18 = Stack Structure Error
13	19 = Code Segment Error
14	20 = Invalid Program Word
15	21 = Not used
16	22 = Invalid Object
17	23 = Page Structure Error
18	24 = Block Exit
19	25 = Binding Request
	12:1 = 1: operator was ENTR
1A	26 = Precision Loss
1B	27 = False Assertion
1C	28 = Locking
1D	29 = Unlocking
SUBTYPE/ 15:4	This field is used to extend the definition of certain interrupt types (shown above).

ID PARAMETER BIT ASSIGNMENTS FOR ALARM INTERRUPTS

Field/Bit	Description
15:11	Reserved
INT TYPE/ 4:5	Types of Alarm interrupts are:
[4:1]	1 = Invalid Address
[3:1]	1 = Uncorrectable Memory Error
[1:1]	1 = Hardware Error
[0:1]	1 = Loop Timer

Invalid Address Interrupt

The invalid address interrupt indicates that an attempt was made to address a nonexistent word in the memory system.

P2 identifies the origin of the invalid address interrupt. These origins are listed as P2 bit assignments of 0E, 0F, 11, 28, 45, and 60.

Uncorrectable Memory Error Interrupt

P2 identifies the origin of the uncorrectable memory error interrupt. These origins are listed in "P2 Parameter Bit Assignments for Hardware Errors" later in this section.

ID PARAMETER BIT ASSIGNMENTS FOR EXTERNAL INTERRUPTS

Field/Bits	Description
15:11	Reserved
INT TYPE/ Types of external interrupt are:	
4:5	
[4:1]	1 = Running Timeout
[3:1]	1 = Unmasked Attention
[2:1]	1 = I/O Finished
[1:1]	1 = Attention
[0:1]	1 = Interval Timer

External interrupts are masked by the CS (control state) flip-flop, except for unmasked attention and running timeout. External interrupt cannot occur between an enter-single-edit operator and the subsequent edit-mode operator.

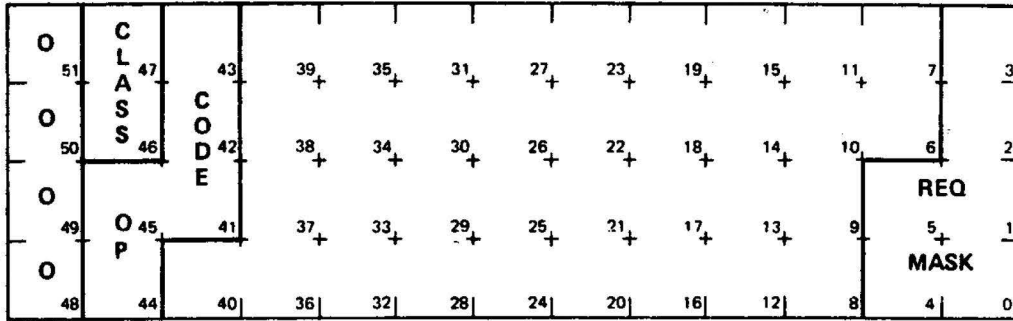
P2 PARAMETER BIT ASSIGNMENTS FOR HARDWARE ERRORS

Field/Bit	Description
	[6.7]
00	Loop time out
01	RU RCM cat parity error
02	RU RCD parity error
03	WU hardware error
04	MID parity error
05	MAU invalid CW or MSM error
06	DU parity error
07	PCU JIE cat parity error
08	PCU PO job no. parity error
09	RU RW job no. parity error
0A	RU RW cache address parity
0B	RU RWD parity error
0C	RU RRJ reg parity error
0D	RU RCM reg parity error
0E	RU invalid address time out
0F	RU address residue time out
10	MAU multiple copy error
11	Invalid address on non-cache job
20	RWR parity error
21	RWD parity error
22	RWD data error
23	Cache address parity error
24	RCM reg parity error
25	RCM cat parity slot 16
26	RCM cat parity slot 11
27	RCD parity error
28	Bad RET or address overflow
29	Interrupt logic failure
2A	RRP and RRX parity error
2B	RRC and RRX/RRP reg parity
2C	RRC reg parity error
2D	RRP reg parity error
2E	RRX reg parity error
2F	RRR reg parity error
30	RED parity error
31	REL parity error
32	RED residue error
33	REL residue error
34	REA residue error
35	RAM cat parity error slot 14
36	RRC cat parity error slot 14
37	RRM cat/reg parity error
38	REM cat parity error
39	RAM cat parity error slot 09
3A	RRC cat parity error slot 09

P2 Parameter Bit Assignments for Hardware Errors (cont.)

Field [6:7]	Description
3B	REC cat parity error
3C	RRC cat parity error slot 08
3D	uCODE error ROM=0*ROMV=1
3E	uCODE error RRC=0*RRMV=1
3F	RU local residue error
40	ELM reg parity error
41	EL cat parity error slot 03
42	EL cat parity error slot 02
43	EL cat/ECV reg parity
44	CER reg parity error
45	Invalid address
46	EPTR bus residue error EC
47	EBCI reg parity error
48	BAR cntl reg res error EU
49	BAR cntl reg res error RU
4A	BAR cntl reg res error PCU
4B	EDI reg parity error
4C	ED cntl parity error
4D	EC cat/CER par slots 01, 02
4E	EC cat slots 03, 04, 05
4F	EO cat parity slots 02, 03
50	EO cat parity error slot 05
51	EA cat parity error
52	ALU mult cntl parity error
53	EAS reg parity error
54	EPTR bus residue error EA
55	EARC reg residue error
56	EWD reg parity error
57	EWJ reg parity error
58	EWD exp residue error
59	EWR reg parity error
5A	EWD mant residue error SAU
5B	EWD mant residue error ALU
60	Bad or invalid address
61	Code error
62	PSCAN cat parity error
63	POL register parity error
64	POM register parity error
65	POM cat error slots 20, 23
66	PO cat error slots 21, 22

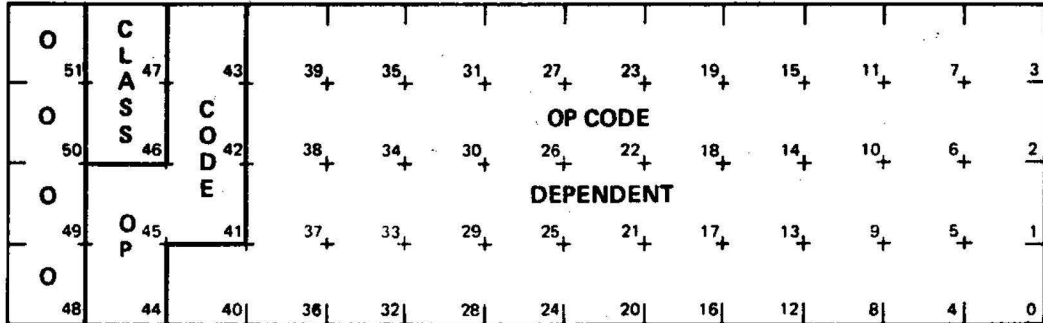
CPM-MC MESSAGE REQUEST CONTROL WORD



CLASS (47:2): 10
OP CODE (45:5): 00100
REQ MASK (5:6) MASK OF DESTINATION REQUESTORS
(ONLY BITS 0 AND 1 USED IN A 12)

E5861

CPM-MC MEMORY CONTROL REQUEST CONTROL WORD



CLASS (47:2) : 00

- OP CODE (45:5) :
- 01001 = READ REQUESTOR STATUS
 - 01010 = READ MEMORY CONFIGURATION
 - 01011 = READ MEMORY ENABLE MASK
 - 01100 = READ SU SAVED MASK
 - 01101 = READ STATUS
 - 01110 = READ TIME-OF-DAY CLOCK
 - 10000 = READY REQUESTOR
 - 10010 = FREE REQUESTOR FROM MAINTENANCE
 - 10100 = READY STORAGE UNIT
 - 10101 = HALT/LOAD
 - 10110 = DISABLE MAINTENANCE BUS
 - 11001 = SAVE REQUESTOR
 - 11011 = RESERVE REQUESTOR FOR MAINTENANCE
 - 11101 = SAVE STORAGE UNIT
 - 11110 = SET TIME-OF-DAY CLOCK
 - 11111 = ENABLE MAINTENANCE BUS

E6489

CPM-MC Memory Control Request Word (Cont.)

OP Code (Hex)	Description
9	Read Requestor Status: The current content of the requestor enable mask is returned in bits 5:6 for A 15 System (bits 1:2 for A 12 System), the requestor maintenance mode mask in bits 15:6 for A 15 System (bits 9:2 for A 12 System), and the requestor present mask in bits 23:6 for A 15 System (bits 17:2 for A 12 System).
A	Read Memory Configuration: The mask of SUs physically present is returned in bits 31:32 of the data word for A 15 System (bits 5:6 for A 12 System).
B	Read Memory Enable Mask: The current content of the SU enable mask is returned in bits 31:32 of the data word for A 15 System (bits 5:6 for A 12 System).
C	Read SU Saved Mask: A bit vector is returned in bits 31:32 of the data word for A 15 System (bits 5:6 for A 12 System). These bits contain a mask of SUs that have been marked to be saved when the next halt/load is performed.
D	Read Status: This OP code rearms the system running timer and returns the following information: [3:4] Box Type (Memory Subsystem = 5 for A 15 System, C for A 12 System) [7:4] Model Number (A 15 Memory Subsystem = 1, A 12 Memory Subsystem = 2). [8:1] Scrub Memory (1 = enabled). [9:1] Maintenance Bus Enable (MBE) 1 = enable [10:1] Scheduler Status (always 0) [16:6] Engineering Release Level (ERL) [22:6] Halt/Load Reason:

CPM-MC Memory Control Request Word (Cont.)

**Hex
Value**

Meaning

01	RIM removed due to requestor fault
02	RIM removed due to RIM fault
03	SIM removed
04	Scheduler module removed
05	SU removed

Note: For A 12 System, values 01 thru 05 are not used.

06	Halt/load request from maintenance console
07	Halt/load request from maintenance console and memory not remapped
08	Reserved for software: loaded thru from halt/load command
3F	control word

[23:2]	Power Fault
[24:1]	Temperature fault
[25:1]	TOD register status (0 = valid)
[26:1]	Subsystem ID (0 = subsystem 0, 1 = subsystem 1)
[29:3]	Reserved for maintenance
[31:2]	Maintenance bus mode: 01 - Bus enabled 10 - Bus disabled 11 - Bus controlled by MBE
[35:4]	SIM status (mask of present SIMs; for A 12 System, bit 32 = 1)

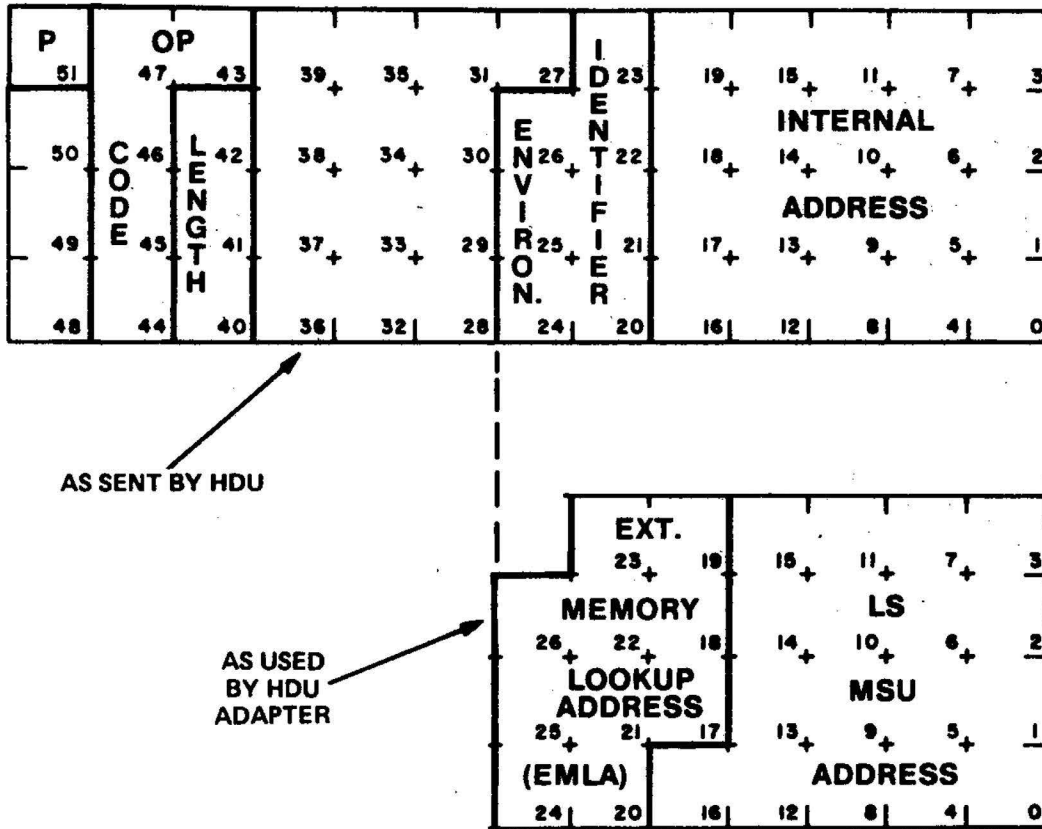
- E** Read Time-of-Day Clock: The returned data word contains the current value of the time-of-day clock in bits 35:36.
- 10** Ready Requestor: The number of the requestor to be readied is encoded in bits 2:3 of the control word for A 15 System (bit 0 for A 12 System). This OP is used only in halt/load operations.
- 12** Free Requestor from Maintenance: The requestor encoded in bits 2:3 of the control word is taken out of the maintenance mode. (Not used in A 12 System.)

CPM-MC Memory Control Request Word (Cont.)

**OP Code
(Hex)**

- | | |
|----|---|
| 14 | Ready Storage Unit: The number of the SU to be readied is encoded in bits 4:5 of the control word for A 15 System (bits 2:3 for A 12 System). |
| 15 | Halt/Load: This command causes the system to halt/load with the current configuration. |
| 16 | Disable Maintenance Bus |
| 19 | Save Requestor: The number of the requestor to be saved is encoded in bits 2:3 of the control word for A 15 System (bit 0 for A 12 System). |
| 1B | Reserve Requestor for Maintenance: The requestor specified by the number encoded in bits 2:3 of the control word is placed in maintenance mode. (Not used in A 12 System.) |
| 1D | Save Storage Unit: The number of the SU to be saved is encoded in bits 4:5 of the control word for A 15 System (bits 2:3 for A 12 System). The SU is saved when the next halt/load is performed. |
| 1E | Set Time of Day Clock: The time-of-day clock is set to the value contained in bits 35:36 of the control word. In addition, bit 25:1 of the Read Status word is made 0 to signify that the TOD register status is valid. |
| 1F | Enable Maintenance Bus: This command causes the maintenance bus to be enabled to the MC. |

HDU-MEMORY STORAGE CONTROL WORD



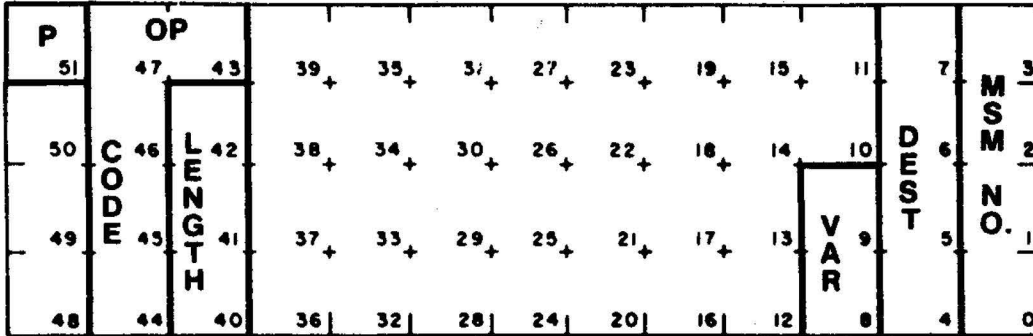
P (51:1) = OVERALL ODD PARITY
 OP CODE (47:5) 0 1001 = READ MODULO 8
 0 1100 = WRITE MODULO 8
 0 1101 = WRITE WITH FLASHBACK
 0 1110 = PROTECTED WRITE MODULO 8

LENGTH (42:3) = 000 THRU 111 (WHERE 000 = 8)

NOTE: ENVIRON. IDENTIFIER NOT USED IN A12 SYSTEM;
 BITS 26:27 = ADDRESS.

E5862

HDU WRITE HARDWARE INTERRUPT CONTROL WORD

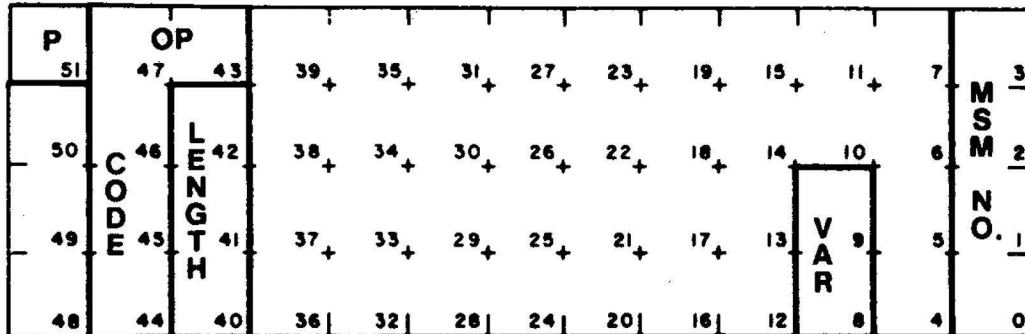


P (51:1) = OVERALL ODD PARITY
OP CODE (47:5) = 0 1000
LENGTH (42:3) : NOT USED
VAR (9:2) = 1
DEST (7:4) = REQUESTOR TO BE INTERRUPTED
(BIT 7 IS SPARE; ONLY BIT 4 USED IN A12 SYSTEM)
MSM NO. (3:4) : NOT USED

NOTE: DATA WORD THAT FOLLOWS CONTROL WORD IS NOT EXAMINED BY HDU ADAPTER (ONLY VALID HARDWARE INTERRUPT BIT IS ETIS).

E5863

HDU READ HARDWARE INTERRUPT CONTROL WORD



P (51:1) = OVERALL ODD PARITY
 OP CODE (47:5) = 0 0111
 LENGTH (42:3) : NOT USED
 VAR (9:2) = 1
 MSM NO. (3:4) : NOT USED

E6097

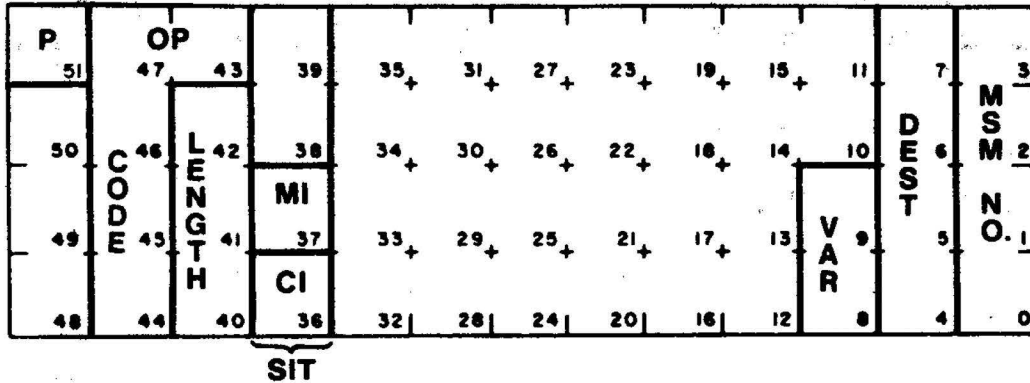
HDU READ HARDWARE INTERRUPT (RETURNED DATA)

P	47+	43+	39+	35+	31+	27+	23+	19+	15+	11+	7	LD	3
O	46+	42+	38+	34+	30+	26+	22+	18+	14+	10+	6	ST	2
O	45+	41+	37+	33+	29+	25+	21+	17+	13+	9+	5	HLT	1
O	44	40	36	32	28	24	20	16	12	8	4	ETIS	0

- P (51:1) = OVERALL ODD PARITY
- LD (3:1) = LOAD
- ST (2:1) = START
- HLT (1:1) = HALT
- ETIS (0:1) = EXECUTE TO INITIAL STATE

E6098

HDU WRITE SOFTWARE INTERRUPT/MESSAGE INTERRUPT CONTROL WORD



P (51:1) = OVERALL ODD PARITY
OP CODE (47:5) = 0 1000
LENGTH (42:3) : NOT USED
SIT (39:4) = SOFTWARE INTERRUPT TYPE:
 (37:1) = MESSAGE INTERRUPT
 (36:1) = CHANNEL INTERRUPT
VAR (9:2) = 0
DEST (7:4) = REQUESTOR TO BE INTERRUPTED (BIT 7 IS SPARE; ONLY BIT 4 USED IN A12 SYSTEM)
MSM NO. (3:4) : NOT USED

NOTE:

1. FOR SOFTWARE INTERRUPT, DATA WORD CONTAINS ALL 0s AND CORRECT PARITY.
2. FOR MESSAGE INTERRUPT, DATA WORD CONTAINS MESSAGE DATA.

E5884

HDU READ SOFTWARE INTERRUPT (RETURNED DATA)

P	51	47 ₊	43 ₊	39 ₊	35 ₊	31 ₊	27 ₊	23	19 ₊	15	11 ₊	7	3
	O	50	46 ₊	42 ₊	38 ₊	34 ₊	30 ₊	26 ₊	22	18 ₊	14	10 ₊	6
O		49	45 ₊	41 ₊	37 ₊	33 ₊	29 ₊	25 ₊	21	MIS		CIS	
	48	44	40	36	32	28	24	20	16	12	8	4	0

} SIP

- P (51:1) = OVERALL ODD PARITY
- MIS (19:8) = MESSAGE INTERRUPT SOURCE
(REQUESTOR BIT MASK; ONLY BIT 13 USED IN A12 SYSTEM)
- CIS (11:8) = CHANNEL INTERRUPT SOURCE
(REQUESTOR BIT MASK; ONLY BIT 5 USED IN A12 SYSTEM)
- SIP (3:4) = SOFTWARE INTERRUPT PRESENT:
(0:1) = CHANNEL OR MESSAGE INTERRUPT

E5866

HDU READ MESSAGE INTERRUPT (RETURNED DATA)

P	V											S	
51	47	43 ₊	39 ₊	35 ₊	31 ₊	27 ₊	23 ₊	19 ₊	15 ₊	11		7 ₊	3
O												R	
50	46	42 ₊	38 ₊	34 ₊	30 ₊	26 ₊	22 ₊	18 ₊	14 ₊	10		6 ₊	2
O	L											C	
49	45	41 ₊	37 ₊	33 ₊	29 ₊	25 ₊	21 ₊	17 ₊	13 ₊	9		5 ₊	1
O												E	
48	44	40	36	32	28	24	20	16	12	8		4	0

P (51:1) = OVERALL ODD PARITY

V (47:1) = MESSAGE VALID

L (45:1) = MESSAGE LOST (OVERWRITTEN)

SRCE (7:8) = REQUESTOR FROM WHICH WRITE MESSAGE
INTERRUPT ORIGINATED (NOT USED IN A12 SYSTEM)

NOTE: MESSAGE WORD FOLLOWS RETURNED DATA.

E5867

RIM OR HDUADPTR-SCHEDULER PRIMARY CONTROL WORD FOR STORAGE RESULTS

				ADD. RES. 27							
		39	35	J O B 31	23 +	19 +	15 +	11 +	7 +	3	
V 42	C O D E	38	34	N O. 30	26 +	22 +	18 +	14 +	10 +	6 +	2
CLU 41			CP 33	29	25 +	21 +	17 +	13 +	9 +	5 +	1
OP 40			ND 32	ADD. RES. 28	24	20	16	12	8	4	0

V (42:1): CONTROL WORD VALID BIT
CLU (41:1): CACHE LOOKUP (=1)
OP CODE (40:5): 00101 = FETCH
00001 = STORE
CP (33:1): COPY PAGE
ND (32:1): NO FETCH DATA REQUIRED
JOB NO. (31:3): 000 THRU 111
ADD. RES. (28:2): ADDRESS RESIDUE

E5868

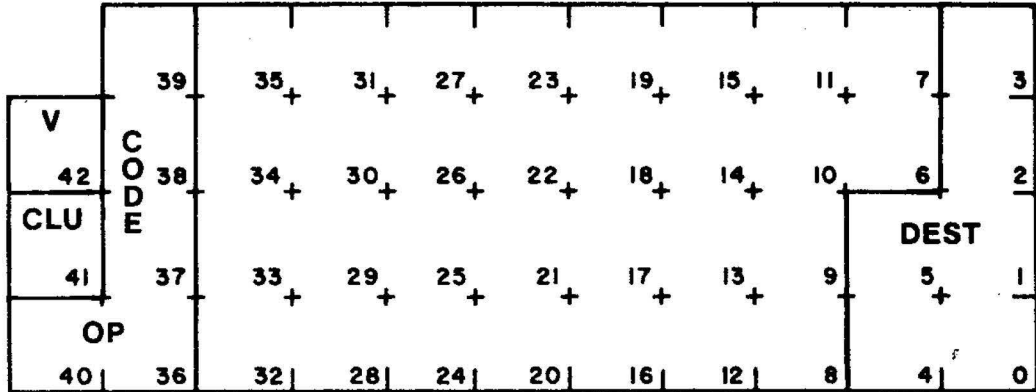
RIM Or HDUADPTR Scheduler Primary Control Word for Storage Requests (Cont.)

Bit/Field	Description
V (42:1)	Indicates that the control word is valid; if this bit is not set, the Scheduler module aborts the operation.
CLU (41:1)	Not significant to the Scheduler module, but indicates cache lookup must be performed by other RIMs (for A 15 System; by RIM logic of other requestor for A 12 System). For store (overwrite) operations, this bit is set and cache purge is performed in other RIMs that have the data (for A 15 System; if RIM has that data in A 12 System).
OP Code (40:5)	Fetch 00101: Four words are read from memory, starting at the address specified in the address field. Used for the fetch portion of a replace operation or for a fast fetch to an HDU. Store (0001): Four data words are stored in memory, starting at the address specified in the address field. Used only for overwrite operations from an HDU.
CP (33:1)	Set when a fetch is performed to provide a requestor with a copy of a four-word page.
ND (32:1)	Set when a fetch is performed to change the status of data from copy to original. (Since the requestor already has a copy, no data is sent from memory; only the status of the existing data is changed.)
Job No. (31:3)	Assigned by requestor to provide job reference for fetched data.
Add. Res. (28:2)	Provides check field for physical memory address; address is invalid if address residue field checks bad. A valid address is signified by good address residue and a valid SU number (contained in address translation table)

RIM-Or HDUADPTR Scheduler Secondary Control Word (Cont.)

Bit/Field	Description
V (42:1)	Indicates that the control word is valid; if this bit is not set, the Scheduler module aborts the operation.
CLU (41:1)	Not significant to the Scheduler module; is reset in the secondary control word to indicate that cache lookup is not required.
OP Code (40:5)	Store (00000): Four words of data are returned to memory. Forward (00110): Four words of data are forwarded to the destination RIM logic.
DEST (34:3)	The RIM or HDUADPTR to which data is to be forwarded if the operation is a Forward or Store and Forward
Job. No. (31:3)	Assigned by requestor to provide job reference for fetched data; used to address pointer queue and update deferred queue on Scheduler module.
Add.Res. (28:2)	Provides check field for physical memory address; address is invalid if address residue field checks bad. A fatal memory error occurs if bad residue exists in a Secondary control word.

RIM OR HDUADPTR-SCHEDULER PRIMARY CONTROL WORD FOR MESSAGE REQUESTS

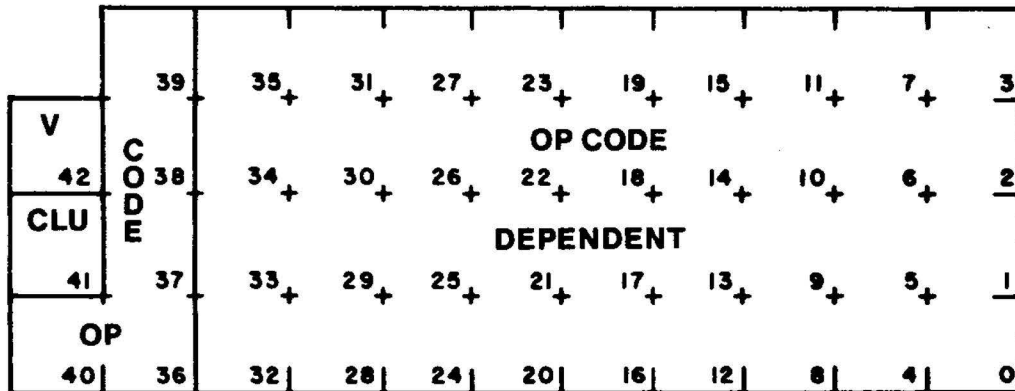


V (42:1): CONTROL WORD VALID BIT
 CLU (41:1): CACHE LOOKUP (=0)
 OP CODE (40:5): 00010 = MESSAGE
 DEST (5:6): MASK OF DESTINATION REQUESTORS
 (ONLY BITS 0 AND 1 USED IN A12 SYSTEM)

E5870

Bit/Field	Description
V (42:1)	Indicates that the control word is valid; if this bit is not set, the Scheduler module aborts the operation.
CLU (41:1)	Not significant to the Scheduler module; is reset in the message control word to indicate that cache lookup is not required.
DEST (5:6)	The bit set in this field indicates that the RIM or HDUADPTR is to receive the message.

RIM OR HDUADPTR-SCHEDULER PRIMARY CONTROL WORD FOR MEMORY CONTROL REQUESTS



V (42:1): CONTROL WORD VALID BIT

CLU (41:1): CACHE LOOKUP (=0)

OP CODE (40:5): 01001 = READ REQUESTOR STATUS

01010 = READ MEMORY CONFIGURATION

01011 = READ MEMORY ENABLE MASK

01100 = READ SU SAVED MASK

01101 = READ STATUS

01110 = READ TIME-OF-DAY CLOCK

10000 = READY REQUESTOR

10010 = FREE REQUESTOR FROM MAINTENANCE

10100 = READY STORAGE UNIT

10101 = HALT/LOAD

10110 = DISABLE MAINTENANCE BUS

11001 = SAVE REQUESTOR

11011 = RESERVE REQUESTOR FOR MAINTENANCE

11101 = SAVE STORAGE UNIT

11110 = SET TIME-OF-DAY CLOCK

11111 = ENABLE MAINTENANCE BUS

E6130

RIM-Or HDUADPTR Scheduler Primary Control Word for Memory Control Requests (Cont.)

OP Code (Hex)	Description
9	Read Requestor Status: The current content of the requestor enable mask is returned in bits 5:6 for A 15 System (bits 1:2 for A 12 System), the requestor maintenance mode mask in bits 15:6 for A 15 System (bits 9:2 for A 12 System), and the requestor present mask in bits 23:6 for A 15 System (bits 17:2 for A 12 System).
A	Read Memory Configuration: The mask of SUs physically present is returned in bits 31:32 of the data word for A 15 System (Bits 5:6 for A 12 System).
B	Read Memory Enable Mask: The current content of the SU enable mask is returned in bits 31:32 of the data word for A 15 System (bits 5:6 for A 12 System).
C	Read SU Saved Mask: A bit vector is returned in bits 31:32 of the data word for A 15 System (bits 5:6 for A 12 System). These bits contain a mask of SUs that have been marked to be saved when the next halt/load is performed.
D	Read Status: This Op code rearms the system running timer and returns the following information: <ul style="list-style-type: none"> [3:4] Box Type (Memory Subsystem = 5 for A 15 System, C for A 12 System) [7:4] Model Number (A 15 Memory Subsystem = 1; A 12 Memory Subsystem = 2) [8:1] Scrub Memory (1 = enabled) [9:1] Maintenance Bus Enable (MBE) 1 = enable [10:1] Scheduler Status (always 0) [16:6] Engineering Release Level (ERL) [22:6] Halt/Load Reason:

RIM-Or HDUADPTR Scheduler Primary Control Word for Memory Control Requests (Cont.)

Hex Value	Meaning
01	RIM removed due to requestor fault
02	RIM removed due to RIM fault
03	SIM removed
04	Scheduler module removed
05	SU removed

Note: For A 12 System, values 01 thru 05 are not used.

06	Halt/load request from maintenance console
07	Halt/load request from maintenance console and memory not remapped
08	Reserved for software: loaded thru from halt/load command
3F	control word

[23:1] Power fault

[24:1] Temperature fault

[25:1] TOD register status (0 = valid)

[26:1] Subsystem ID (0 = subsystem 0, 1 = subsystem 1)

[29:3] Reserved for maintenance

[31:1] Maintenance bus mode:
 01 - Bus enabled
 10 - Bus disabled
 11 - Bus controlled by MBE

[35:4] SIM status (mask of present SIMs; for A 12 System, bit 32 = 1)

- E Read Time-of-Day Clock: The returned data word contains the current value of the time-of-day clock in bits 35:36
- 10 Ready Requestor: The number of the requestor to be readied is encoded in bits 2:3 of the control word for A 15 System (bit 0 for A 12 System). This OP is used only in halt/load operations.
- 12 Free Requestor from Maintenance: The requestor encoded in bits 2:3 of the control word is taken out of maintenance mode. (Not used in A 12 System.)

RIM-Or HDUADPTR Scheduler Primary Control Word for Memory Control Requests (Cont.)

- 14 Ready Storage Unit: The number of the SU to be readied is encoded in bits 4:5 of the control word for A 15 System (bits 2:3 for A 12 System).
- 15 Halt/Load: This command causes the system to halt/load with the current configuration.
- 16 Disable Maintenance Bus
- 19 Save Requestor: the number of the requestor to be saved is encoded in bits 2:3 of the control word for A 15 System (bit 0 for A 12 System).
- 1B Reserve Requestor for Maintenance: The requestor specified by the number encoded in bits 2:3 of the control word is placed in maintenance mode. (Not used in A 12 System).
- 1D Save Storage Unit: The number of the SU to be saved is encoded in bits 4:5 of the control word for A 15 System (bits 2:3 for A 12 System). The SU is saved when the next halt/load is performed.
- 1E Set Time-of-Day Clock: The time-of-day clock is set to the value contained in bits 35:36 of the control word. In addition, bit 25:1 of the Read Status word is made 0 to signify that the TOD register status is valid
- 1F Enable Maintenance Bus: This command causes the maintenance bus to be enabled to the MC

SCHEDULER-SIM CONTROL WORD FOR STORAGE REQUESTS

P	JOB NO.	SRCE	OP CODE	SU NO.	19+	15+	11+	7+	3
43	39	35	31	27	23	19+	15+	11+	7+
SO	DEST	SRCE	OP CODE	SU NO.	18+	14+	10+	6+	2
42									
JOB NO.	DEST	SRCE	OP CODE	SU NO.	ADDRESS				
41					37	33	29	25	21+
NO.	DEST	SRCE	OP CODE	SU NO.	16	12	8	4	0
40									

- P (43:1): OVERALL ODD PARITY
- SO (42:1): SPECIAL OPERATION BIT (=0)
- JOB NO. (41:3): 000 THRU 111
- DEST (38:3): DESTINATION REQUESTOR (ONLY BIT 36 USED IN A12 SYSTEM)
- SRCE (35:3): SOURCE REQUESTOR (ONLY BIT 33 USED IN A12 SYSTEM)
- OP CODE (32:3): 000 = FETCH
 - 001 = CLEAR SU
 - 010 = STORE
 - 011 = STORE ABORT
 - 100 = FORWARD
 - 101 = STORE & FORWARD
 - 111 = SCRUB
- SU NO. (24:3): 000 THRU 111 (FOR A12 SYSTEM, 000 THRU 101)
- ADDRESS (21:22): (21:2) - RESERVED FOR EXPANSION } FOR A15 SYSTEM
 (19:20) - PHYSICAL SU ADDRESS }
 FOR A12 SYSTEM, 21:22 = PHYSICAL SU ADDRESS

E5871

Scheduler-SIM Control Word for Storage Requests (Cont.)

Bit/Field	Description
SO (42:1)	The special operation bit is always 0 in this control word.
Job No. (41:3)	This field is significant only for fetch (read), Forward, and Store and Forward operations. It is sent back to the HDUADPTR card but is transparent to the SIM.
DEST (38:3)	This field defines the RIM to which data is to be sent in fetch, forward, and store and forward operation.
SRCE (35:3)	This field defines the requestor from which data is received in store, store abort, and store and forward operations.
OP Code (32:3)	<p>Fetch (000): Four data words are read from memory, starting at the address specified in the address field, and not crossing a page boundary.</p> <p>Clear SU (001): When an SU is readied into the memory subsystem, each location within the SU is written with zeros.</p> <p>Store (010): Four data words are written to memory, starting at the address specified in the address field. The word number must be set to 0.</p> <p>Store Abort (011): The requestor associated with this operation is in maintenance mode; therefore, no data is to be stored in the memory.</p> <p>Forward (100): the data received from the requestor is to be forwarded to the requestor defined by the DEST field.</p> <p>Store and Forward (101): The data received from the requestor is stored at the specified address and is forwarded to the requestor defined by the DEST field.</p> <p>Scrub (111): Four words of data (starting at the address specified in the address field) are read from memory and the Error Check Code (ECC) for each word is checked. If necessary, the data or ECC is corrected and then written back into memory; however, if no correction is required, data is not written back to memory.</p>
SU No. (24:3)	This field specifies the number of the SU involved in the operation
Address (21:22)	<p>For A 15 System, bits 21:2 of this field are reserved for expansion; the remaining bits (19:20) define the physical starting address within the SU.</p> <p>For the A 12 System, this field defines the physical starting address within the SU.</p>

SCHEDULER-SIM CONTROL WORD FOR MESSAGE REQUESTS

P			OP								
43	39	35	31	27	23	19	15	11	7	3	
SO		SRCE	CODE								
42	38	34	30	26	22	18	14	10	6	2	
									DEST		
41	37	33	29	25	21	17	13	9	5	1	
		OP									
40	36	32	28	24	20	16	12	8	4	0	

P (43:1): OVERALL ODD PARITY
SO (42:1): SPECIAL OPERATION BIT (=0)
SRCE (35:3): SOURCE REQUESTOR (ONLY BIT 33 USED IN A12 SYSTEM)
OP COPE (32:3): 110
DEST (5:5): MASK OF DESTINATION REQUESTORS (ONLY BITS 0 AND 1 USED IN A 12 SYSTEM)

E5872

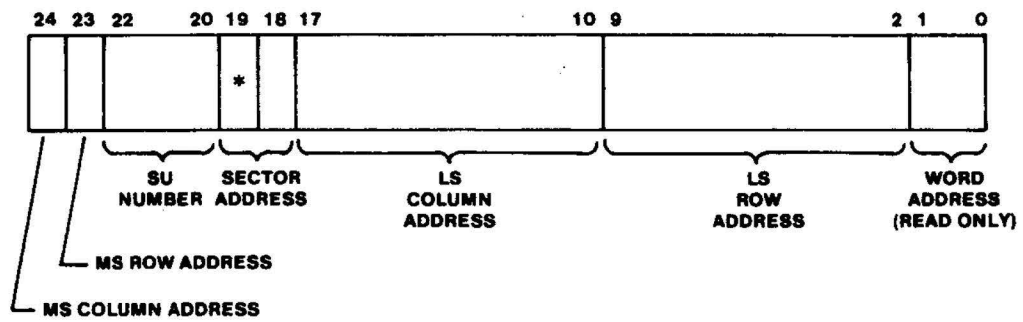
MEMORY CONTROL READ REQUEST

P	JOB NO.									
43	39	35 ₊	31 ₊	27 ₊	23 ₊	19 ₊	15 ₊	11 ₊	7 ₊	3
SO										
42	38	34 ₊	30 ₊	26 ₊	22 ₊	18 ₊	14 ₊	10 ₊	6 ₊	2
JOB	DEST	INFORMATION								
41		37	33 ₊	29 ₊	25 ₊	21 ₊	17 ₊	13 ₊	9 ₊	5 ₊
N O.										
40	36	32	28	24	20	16	12	8	4	0

P (43:1): OVERALL ODD PARITY
SO (42:1): SPECIAL OPERATION BIT (=1)
JOB NO. (41:3): 000 THRU 111
DEST (38:3): DESTINATION REQUESTOR
(ONLY BIT 36 USED IN A12 SYSTEM)

E5873

STORAGE ADDRESSING (SIM TO MSU)



*FOR A15 SYSTEM, BIT 19 IS NOT USED IN THE STORAGE UNITS.
 FOR A12 SYSTEM, BOTH BITS 18 AND 19 ARE USED.

E5874

SIM OUTPUT DATA BUS BIT ASSIGNMENTS

Data Line	Bit Number	
	Phase 0	Phase 1
0	0	4
1	1	5
2	2	6
3	3	7
4	8	12
5	9	13
6	10	14
7	11	15
8	16	20
9	17	21
10	18	22
11	19	23
12	24	28
13	25	29
14	26	30
15	27	31
16	32	36
17	33	37
18	34	38
19	35	39
20	40	44
21	41	45
22	42	46
23	43	47
24	48	50
25	49	51

SIM OUTPUT DATA CONTROL BIT ASSIGNMENTS

Output Data Line	Phase 0	Phase 1
26	Message Bit	Job Bit 2
27	Job Bit 0	Job Bit 1
28	Word Bit 0	Word Bit 1

SECTION 3

HOST DATA UNIT

HCB CONTROL WORD

HCB Control Word (cont.)

Field	Bits	Description
OW	4:1	Overwrite: If set, the HDP ignores memory tags during data transfer. If reset, HDP aborts data transfer if an attempt is made to read a word from memory with odd tags. If reset during a write to memory (read from DLP), the Memory Subsystem detects and sends back a memory protect error, and the HDP aborts the operation.
IN	5:1	Input: If set, the requested operation is a read from the DLP. If the DLP goes to other than a read status and this bit is set, the HDP reports a DLP status error and prevents the data transfer.
OUT	6:1	Output: If set, the requested operation is a write to the DLP. If the DLP goes to other than a write status and this bit is set, the HDP reports a DLP status error and prevents the data transfer.
OZ	7:1	Output Zeros: Used for erase operations to tape.
TAG CNTL	10:3	Tag Control (allowed only in word mode): The values of this field define how the tag is handled during data transfer.

010 Transfer double byte tag.

Tags are handled as two additional bytes of data. On output, the 3 bits of tag are placed in the 3 LSBs of the most significant byte; the other 13 bits are set to 0. On input, the 3 LSBs of the most significant byte are placed in the tag bits of the word; the other 13 bits are ignored.

100 Force tags to single (0).

Tags are not handled as data to be transferred. On input, the tag of each word is skipped.

110 Force tags to double (2).

Valid on input only; performs as force tags to single, except that the tag of each word is set to double (2).

111 Force tags to code (3).

Valid on input only; the tag of each word is set to code (3).

HCB Control Word (cont.)

Field	Bits	Description
WM	11:1	Word/Character Mode Transfer: If set, the HDP buffer descriptor must be a word data descriptor and the HDP buffer length is in words. If reset, the HDP buffer descriptor and HDP buffer Length are in characters.
REV	12:1	Reverse (allowed only in character mode input): If set, the HDP transfers the data into memory in reverse order. If this bit is set, and the output bit (6:1) is also set, an invalid control field error is reported.
CCT	13:1	Continue Count (allowed only in input): If set, the HDP continues to count the data received after the length count in the HDP has reached zero. It is used for tape operations.
ILCE	14:1	Ignore Length Count Error: If set, the queue manager does not set count error in the HDU result if the HDP buffer length is not zero at the end of the operation.
CQI	15:1	Command Queue Immediate: This operation is initiated regardless of the active count in the control word of the addressed command queue header. If bit 15:1 is set, QM does not increment the active count on initiation or on job termination. Also, QM ignores the state of the suspended bit of the C queue header.
	16:1	Not used.
DQI	17:1	DLP Queue Immediate: This operation is initiated regardless of the active count in the control word of the addressed DLP queue header. If bit 17:1 is set, QM does not increment the count on initiation or decrement it on job termination. Also, QM ignores the state of the suspended bit of the C queue header.

HCB Control Word (cont.)

Field	Bits	Description
LOC	18:1	Local/Global Allocation: If set, the queue manager attempts to capture the HCB locally when the operation is sent to the UIO subsystem.
NOTE		
If local memory of the queue manager is full, then queue manager changes Local to Global and executes it as a Global job.		
MAIN	19:1	Maintenance Operation: This bit is used only by software.
Stack Number		The number of the stack containing the process which requested the I/O operation (available for software use).
HCB Mark	47:16	Used by the HDU to verify that this is actually the first word of an HCB.

COMMAND QUEUE HEADER POINTER WORD

	PR	RO												
		47	43	39+	35+	31+	27+	23	19+	15+	11+	7+	3	
1	C	46	42	WORD				MEMORY						
50				38+	34+	30+	26+	22	18+	14+	10+	6+	2	
0	I	45	41	INDEX				ADDRESS						
49				37+	33+	29+	25+	21	17+	13+	9+	5+	1	
1														
48		44	40	36	32	28	24	20	16	12	8	4	0	

E4807

DLP COMMAND/RESULT LENGTHS

		47+	43+	39+	35+	31+	27	23+	19+	15+	11+	7+	3
0		COMMAND				RESULT							
50		46+	42+	38+	34+	30+	26	22+	18+	14+	10+	6+	2
0		LENGTH				LENGTH							
49		45+	41+	37+	33+	29+	25	21+	17+	13+	9+	5+	1
0		(BYTES)				(BYTES)							
48		44	40	36	32	28	24	20	16	12	8	4	0

E4808

DLP I/O COMMAND POINTER

	PR	RO																	
			39	35	31	27	23	19	15	11	7	3							
1	C	O	WORD					I/O DESCRIPTOR											
			38	34	30	26	22	18	14	10	6	2							
O	I		INDEX					ADDRESS											
			37	33	29	25	21	17	13	9	5	1							
1																			
			48	44	40	36	32	28	24	20	16	12	8	4	0				

E4809

DLP I/O RESULT POINTER WORD

	PR	RO																	
			39	35	31	27	23	19	15	11	7	3							
1	C	O	WORD					RESULT											
			38	34	30	26	22	18	14	10	6	2							
O	I		INDEX					DESCRIPTOR											
			37	33	29	25	21	17	13	9	5	1							
1																			
			48	44	40	36	32	28	24	20	16	12	8	4	0				

E4810

RESULT MASK WORD

		47+	43+	39+	35+	31+	27+	23+	19+	15+	11+	7+	3
0	50	RESULT											
		46+	42+	38+	34+	30+	26+	22+	18+	14+	10+	6+	2
0	49	MASK											
		45+	41+	37+	33+	29+	25+	21+	17+	13+	9+	5+	1
0	48	44	40	36	32	28	24	20	16	12	8	4	0

E4411

FOR ASN OPERATING SYSTEM

HDP BUFFER DESCRIPTOR

		PR	RO										
		47	43	39+	35+	31+	27+	23	19+	15+	11+	7+	3
1	C	O	INDEX					ADDRESS					
		46	42	38+	34+	30+	26+	22	18+	14+	10+	6+	2
0	I	O											
		45	41	37+	33+	29+	25+	21	17+	13+	9+	5+	1
1		O											
		44	40	36	32	28	24	20	16	12	8	4	0

Indexed Word Data Descriptor

		PR	RO	C										
		47	43	H	39	35+	31+	27+	23	19+	15+	11+	7+	
1	C	1	WORD				ADDRESS							
		46	42	A	38	34+	30+	26+	22	18+	14+	10+	6+	
0	I	O	INDEX											
		45	41	R	37	33+	29+	25+	21	17+	13+	9+	5+	
1		O												
		44	40	I	36	32	28	24	20	16	12	8	4	
				N									0	

E4412

Indexed Character Data Descriptor

HDP Buffer Descriptor (cont.)

Field/Bit	Description
Address/19:20	Address interpretations are: <ol style="list-style-type: none">1. Present: the memory address of the base word of the array.2. Absent: the memory address of the associated original data descriptor.
Word Index/35:16	The index from the base of the array to the word containing the reference character.
Character Index/39:4	The index within the word of the reference character.
Index/39:20	The word index from the base of the array to the referenced word.
Element Size/42:3	Type of array: 0 = single precision; 4 = EBCDIC
RO 43:1	Read Only Bit: 0 = read, write; 1 = read only.
I 45:1	Index bit: 1
C 46:1	Copy bit: 1
PR 47:1	Present bit: 0 = absent 1 = present
TAG 50:3	Tag field value equals 5.

FOR ASD OPERATING SYSTEM

UNINDEXED (ORIGINAL OR COPY) DD

∅	1	RO													
51	47	43	39+	35+	31+	27+	23	19+	15+	11+	7+	3			
1	C														
50	46	42	38+	34+	30+	26+	22	18+	14+	10+	6+	2			
∅	∅	ES	LENGTH					ASD REF							
49	45	41	37+	33+	29+	25+	21	17+	13+	9+	5+	1			
1	1														
48	44	40	36	32	28	24	20	16	12	8	4	0			

FIELD	BITS	DESCRIPTION
ASD REF	19:20	ASD NUMBER
LENGTH	39:20	THE NUMBER OF ELEMENTS IN THE ARRAY
ELEMENT SIZE	42:3	THE TYPE OF ARRAY ELEMENT 0 = SINGLE PRECISION 1 = DOUBLE PRECISION 2 = HEXADECIMAL (4 BITS) 4 = EBCDIC (8 BITS) 3,5,6,7 = INVALID
READ ONLY BIT	43:1	RESET FOR STORE ACCESS BY HDU
PAGED BIT	44:1	PAGED BIT (0 = UNPAGED, 1 = PAGED) - THIS BIT IS NOT USED BY THE HDU.
INDEXED BIT	45:1	0 DENOTES UNINDEXED DD
COPY BIT	46:1	COPY BIT(0 = ORIGINAL, 1 = COPY) - THIS BIT IS NOT REFERENCED BY THE HDU.
TOUCHED BIT	47:1	1 DENOTES TOUCHED DD - THIS BIT IS SET FOR ALL DDs REFERENCED BY THE HDU.
TAG	50:3	TAG FIELD VALUE EQUALS 5.

INDEXED DD

0	1	RO											
51	47	43	39	35	31	27	23	19	15	11	7	3	
1	1		38	34	30	26	22	18	14	10	6	2	
0	1	ES	INDEX				ASD REF						
49	45	41	37	33	29	25	21	17	13	9	5	1	
1	0		36	32	28	24	20	16	12	8	4	0	
48	44	40											

FIELD	BITS	DESCRIPTION
ASD REF	19:20	ASD NUMBER
INDEX	39:20	THE INDEX FROM THE BASE OF THE ARRAY TO THE REFERENCED ITEM.
ELEMENT SIZE	42:3	THE TYPE OF ARRAY ELEMENT. 0 = SINGLE PRECISION 1 = DOUBLE PRECISION 2 = HEXADECIMAL (4 BITS) 4 = EBCDIC (8 BITS) 3,5,6,7 = INVALID
READ ONLY BIT	43:1	RESET FOR STORE ACCESS BY THE HDU.
PAGED BIT	44:1	PAGED BIT (0 = UNPAGED, 1 = PAGED) -THIS BIT IS NOT USED BY HDU.
INDEXED BIT	45:1	0 DENOTES UNINDEXED DD.
COPY BIT	46:1	COPY BIT (0 = ORIGINAL, 1 = COPY) -THIS BIT IS NOT REFERENCED BY THE HDU.
TOUCHED BIT	47:1	1 DENOTES TOUCHED DD - THIS BIT IS SET FOR ALL DDs REFERENCED BY THE HDU.
TAG	50:3	TAG FIELD VALUE EQUALS 5.

E5876

ACTUAL SEGMENT DESCRIPTOR, FIRST WORD

0	0	UA																	
51	47	43	39+	35	31+	27+	23+	19+	15+	11+	7+	3							
1	1	1																	
50	46	42	38+	34	30+	26+	22+	18+	14+	10+	6+	2							
0	PP	PI	S/W				ADDRESS												
49	45	41	37+	33	29+	25+	21+	17+	13+	9+	5+	1							
1	0	NP																	
48	44	40	36	32	28	24	20	16	12	8	4	0							

FIELD	BITS	DESCRIPTION
ADDRESS	31:32	THE BASE ADDRESS OF THE ACTUAL SEGMENT.
SOFT	39:4	RESERVED FOR SOFTWARE USE.
NOT PAGE	40:1	PAGE INDICATOR (0 - PAGE, 1 - NOT PAGE) - THIS BIT IS NOT REFERENCED BY THE HDU.
PRESENT FOR I/O	41:1	SEGMENT IS PRESENT INDICATOR (0 - SEGMENT IS ABSENT, 1 - SEGMENT IS PRESENT) - THIS BIT IS SET FOR ANY USE OF THE ACTUAL SEGMENT AS THE SOURCE OR DESTINATION FOR I/O TRANSFER.
NOT STACK	42:1	STACK INDICATOR (0 - STACK, 1 - NOT STACK) - THIS BIT IS SET FOR ANY ASD REFERENCED BY THE HDU.
UNALTERED	43:1	ALTERED DATA INDICATOR (0 - ALTERED, 1 - UNALTERED) - THIS BIT IS NOT REFERENCED BY A12 REQUESTORS
	44:1	0 DENOTES ASD1

ACTUAL SEGMENT DESCRIPTOR, FIRST WORD (Cont.)

PRESENT TO PROC	45:1	SEGMENT IS PRESENT INDICATOR (0 - SEGMENT IS ABSENT; 1 - SEGMENT IS PRESENT) - THIS BIT IS SET FOR ANY USE OF THE ACTUAL SEGMENT AS THE I/O CONTROL STRUCTURE (IOCBs AND QUEUE HEADERS).
	47:2	ALL ABSOLUTE CONTAINER WORDS HAVE THE BINARY VALUE 01 IN FIELD [47:2]
TAG	50:3	TAG FIELD EQUALS 5.

NOTE

THE ASD2 (ACTUAL SEGMENT DESCRIPTOR, SECOND WORD), WHICH IS ASSOCIATED WITH THE ASD1 AND IS USED TO SPECIFY THE LENGTH IN WORDS OF THE ACTUAL SEGMENT, IS NOT USED BY THE HDU. ALSO, THE ASD3 (ACTUAL SEGMENT DESCRIPTOR, THIRD WORD), WHICH IS USED AS A REFERENCE WORD, IS NOT USED BY THE HDU.

E5877

HDP BUFFER LENGTH WORD

	47	43	39	35	31	27	23	19	15	11	7	3
O	SIGN											
50	46	42	38	34	30	26	22	18	14	10	6	2
O												
49	45	41	37	33	29	25	21	17	13	9	5	1
O												
48	44	40	36	32	28	24	20	16	12	8	4	0

E4613

HDP QUEUE MANAGER CONTROL WORD

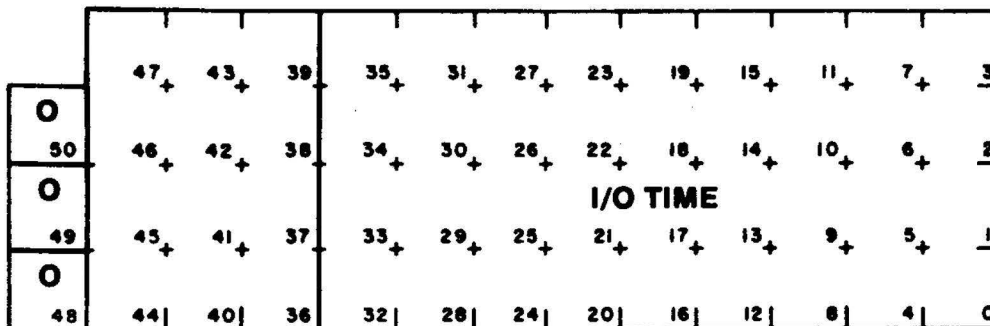
	O	WM	OZ				LOC					
	47	43	39	35	31	27	23	19	15	11	7	3
O	O	T	OUT									
50	46	A	38	34	30	26	22	18	14	10	6	2
O	CCT	G	IN									
49	45	C	37	33	29	25	21	17	13	9	5	1
O	REV	N	MP									
48	44	T	36	32	28	24	20	16	12	8	4	0
		L										

E4614

HDP Queue Manager Control Word (cont.)

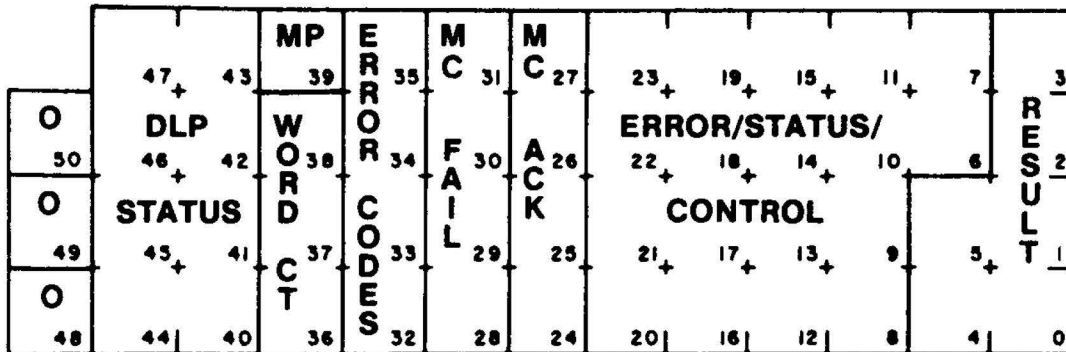
Field	Bits	Description
HCb address	22:23	Address of the HCB that initialized the UIO job. If HCB is captured locally (LOC bit set), the HCB address represents the local memory address (bits 11:12). If HCB is not captured locally, the HCB address represents the main memory address (bits 19:20).
LOC	23:1	LOC bit: 1 = HCB [CW] local; 0 = HCB [CW] in main memory.
HRF	31:8	Host Return Field: This field contains the information necessary for the UIO to make the connection back to the host system. HRF is copied from the DLP address word (QDLP) of the C queue header.
	45:10	This field is copied from HCB control word. The description of bits 45:10 is the same as bits 13:10 of the HCB control word.

I/O TIME WORD



E4015

HDU RESULT AND STATE WORD



E5334

Field	Bits	Description
QM Result	Bits 5:6	Exception: This bit is set under the following conditions
		<ol style="list-style-type: none"> Unanticipated non-zero residue data transfer count. An unmasked bit set in first 48 bits of DLP result. Attention was requested by MCP in the HCB control word (bit 2:1). A memory error was reported during data transfer to the HDP. An MLI error occurred during data transfer.
	1:1	Attention: This bit is set if the attention bit (bit 2:1) is set in the HDU control word.
	2:1	DLP Error: This bit is set if the result of the logical "AND" of the first 48 bits of the DLP result descriptor and the ones complement of the HCB mask word is not zero.

HDU Result and State Word (cont.)

Field	Bits	Description
	3:1	HDP/MLI Error: This bit is set if any error is reported in the error/status/control field.
	4:1	Spare
	5:1	MBC-Detected error reported to HDP. This bit is set if any error is detected by the MCB or reported to the MCB during the memory operation from the MSM.

Error/Status Control Bits 23:14

	6:1	Memory Protect Error: This bit is set if the HDP accesses a word with an odd tag, and memory overwrite is not set in the HDU control field. It is unconditionally set if the HDU accesses a word with an odd tag while writing the DLP result.
	7:1	Count Error: This bit is set if the HDP buffer length is not equal to zero when the I/O completes, and the ignore count error bit is not set.
	8:1	HDP Delayed Write Strobe: This bit is a hold bit used in the HDP to allow output data to settle before issuing a send/acknowledge (AG+SIO) to the MLI.
	9:1	Burst Mode Inhibit Delay: This bit is set during burst mode write operation. When this bit is not true, a clock delay is added to the inhibit to allow data to settle in the HDP. (Used in maintenance only.)
	10:1	Burst Mode Inhibit: This bit is set after the send/acknowledge is issued to the MLI. It inhibits further asynchronous transfers between I/O subsystem and HDP until it is reset by the microsequencer. (Used in maintenance only.)
	11:1	MLI Write Data Enable: This bit is set when the HDP is ready to send data over the MLI. (Used in maintenance only.)
	12:1	DLP Address Parity Error: Parity error detected on DLP address word during poll test.
	13:1	Memory Address Overflow: This bit is set if main memory address exceeded hex FFFF during the input operation.

HDU Result and State Word (cont.)

Field	Bits	Description
Error Codes	35:4	This field contains the error detected by MBC or reported to the MBC by the MC or both, as shown in table 1-1.
MP	39:1	Memory Protect: This bit is set if an attempt is made to write into a protected memory location.
Word CT	38:3	Indicates word in error for either requestor or MBUS data word parity error.
DLP Status	47:8	This field contains the current [47:4] and past [43:4] DLP status encountered by the HDP.

DEFINITION OF ERROR CODE FIELD IN THE HDU RESULT AND STATE WORD

Error Code Field 35:4	Definition
0	MC-detected error.
1	No-Access-To-Memory: Indicates that a particular operation for longer than the maximum MC busy time was tried by the MBC; indicates no other errors or acknowledges have occurred.
2	Invalid Read: Too many or too few data words were sent by the MC during a read operation.
3	Time-Out Waiting for MC: While in a read operation, no valid data signal was received from the MC; or no requestor operation complete signal was received during a protected write. The MC is reported in the MC fail field [31:4] of HDU result and state word.

**Definition of Error Code in the
HDU Result and State Word (cont.)**

**Error Code
Field 35:4**

Definition

- 4 Parity error on read data from MC: Indicates that at least one data word sent by the MC has a parity error. The first word with an error is reported in the word count field [39:3] of the HDU result and state word. The MC is reported in the fail field [31:4] of the HDU result and state word.
- 5 Spare
- 6 MBC detected MC protocol error: Indicates that a control signal from the MC is incorrect. The MC is reported in the MC fail field [31:4] of the HDU result and state word.
- 7 MBUS DW parity error: Indicates a data word the requestor was attempting to write to memory contained a parity error. The first data word with bad parity is recorded in the word count field [39:3] of the HDU result and state word.
- 8 MBC detected invalid CW: Indicates that the CW sent to the MBC by the requestor had an invalid length field or an illegal OP code.
- 9 MBUS CW parity error: Indicates that the CW received from the MBUS had bad parity.

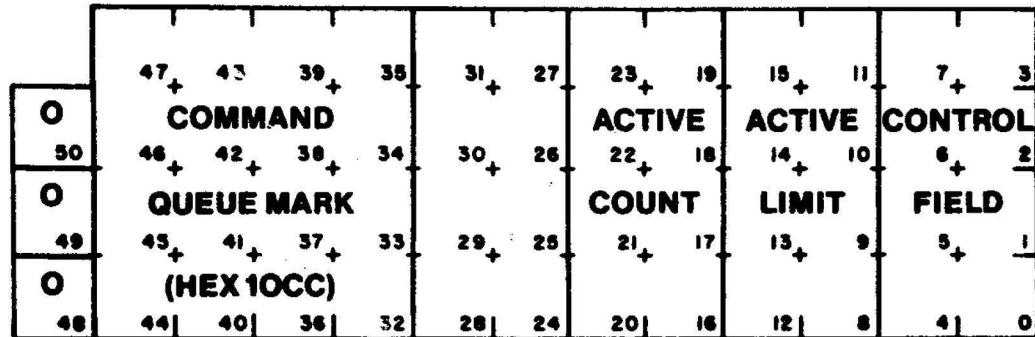
VALID DLP STATUS STATES

Status Mnemonic	Status State Count	Usage or Meaning
Cleared	STC = 0	Entered by the DLP when it is cleared. This status is also shown if the DLP is not present, it has PROM parity error, or it has been taken off line by the maintenance card (MC).
Disconnect	STC = 1	Used by the DLP to indicate that no more transfers are possible during the connection, or to indicate that the DLP is unable to accept a new I/O descriptor.
Reserved	STC = 2	Reserved for expansion. Detection of this status results in an error.
Idle	STC = 3	Indicates that the DLP can accept a new I/O descriptor, or that a DLP receiving this new descriptor requires additional descriptor words.
Read	STC = 4	Indicates that data is being transferred to the host system by the DLP.
Send Descriptor Link	STC = 5	Indicates that the descriptor link is being sent to the host system.
Receiver Descriptor Link	STC = 6	Indicates that the DLP needs to receive, or is receiving the descriptor link.
Result Descriptor	STC = 7	Indicates that the result descriptor is being sent to the host system.
Write	STC = 8	Indicates that the DLP needs data from the host system.

Valid DLP Status States (cont.)

Status Mnemonic	Status State Count	Usage or Meaning
Encoded Status	STC = 9	Indicates that the DLP is sending special status information on the data lines.
Port Busy	STC = 10	The host is waiting on port busy, but the LEM (line expansion module) has a request from another DLP.
I/O Descriptor LPW	SCT = 11	Indicates that the DLP requires the I/O descriptor LPW (longitudinal parity word).
Break	STC = 12	Indicates the end of a data message and the DLP now wants an LPW.
Break Enable	STC = 13	Indicates the desire by the DLP to translate another message to the host system. The host system may accept or refuse this request.
Character Transfer	STC = 14	Used by certain DLPs to resolve the contents of the last data word that has been received from the host system.
Result Descriptor LPW	STC = 15	Indicates that the final word of the result descriptor is being sent to the host system and is followed by the appropriate LPW.

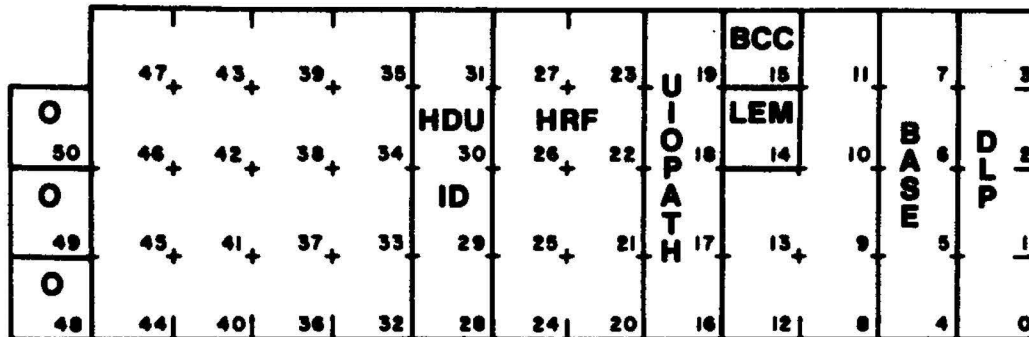
CONTROL WORD OF C QUEUE HEADER



E4817

Field	Bits	Description
Control Field	0:1	Suspended bit: QM can not issue any more initiate poll test commands to the HDP.
	1:1	Waiting bit: This bit is maintained by the HDU. C queue has been linked into an H queue.
	2:1	DLP queue present: HCBs from this queue are executed by a higher level queue (D queue). This queue is a C queue.
	3:1	Reserved for maintenance.
	4:1	Interrupt on complete: QM interrupts CPM when queue identified by HCB command queue header pointer word is empty and completion of operation causes active count to go to zero.
	5:1	Ignore: Suspend All Queues Flag.
	6:1	Hold on terminate: Hold DLP upon completion of any I/O job so that additional jobs can be started with the same DLP.
	7:1	Spare
Active Limit	15:8	Set by MCP during system initialization. Represents a non-zero count of the maximum number of HCBs which can be active from the queue.
Active Count	23:8	Maintained by the HDU: Represents the number of HCBs which are currently active from the queue.

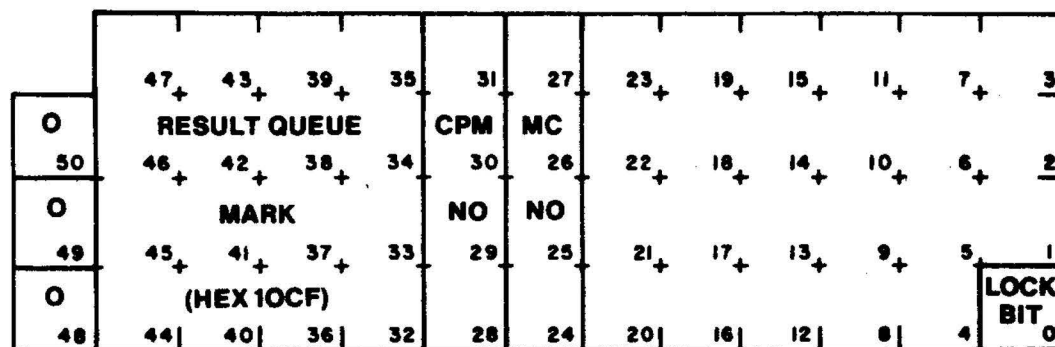
DLP ADDRESS (QDLP) WORD



24018

Field	Bits	Description
DLP	3:4	Identifies the DLP within the addressed UIO base.
Base	7:4	Identifies a UIO base connected to the MLI port.
LEM	14:1	Indicates that the command is for the line expansion module.
BCC		Indicates that the command is for base control card within the addressed UIO base.
DLP Address	19:4	UIO path: 19:2 MLI port to be used (0,1). 17:2 HDP Number to be used (0,1,2).
HRF	27:8	Host Return Field: This field contains the information necessary for the UIO to make the connection back to the host system.
HDU ID	31:4	Requestor number: (Used by software.)

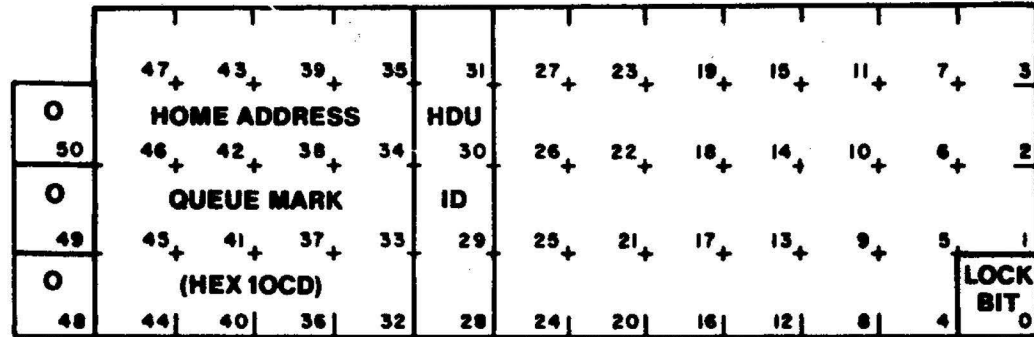
CONTROL WORD OF RQ HEADER



E5328

Field	Bits	Description
Lock Bit	0:1	0 = indicates that QM has the RQ header 1 = indicates that the RQ header is unavailable
MC No	27:4	Not used. (There is only one MC in a non-partitioned system.)
CPM No	31:4	Specifies the CPM to be interrupted by the HDU.
Result Queue Mark (hex 10CF)		Used by the HDU to verify that the fetched word is the RQ header control word.

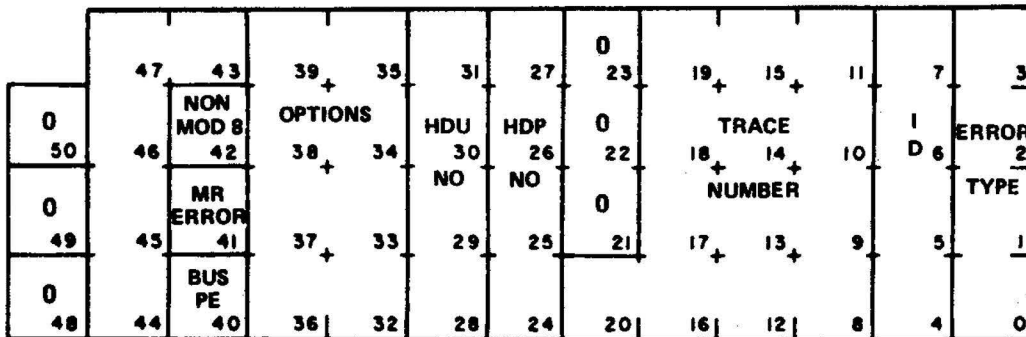
CONTROL WORD OF HAQ HEADER



E4622

Field	Bits	Description
Lock bit	0:1	0: indicates that QM has the HAQ header 1: indicates that the HAQ header is unavailable
HDU ID	31:4	Requestor number (used by software)
Home Address Queue Mark (Hex IOCD)	47:16	Used by the HDU to verify that the fetched word is the HAQ header control word

EIOCB (ERROR TYPE) WORD



E5283

Field	Bits	Description
	47:8	Bit-oriented indications
	47:5	Spare
	42:1	Non mod (8) memory operations
	41:1	MR error
	40:1	Parity error
		Multiple error/indicator bits (more than one of the above bits may be set.)
	42:1	If set, indicates non mod 8 main memory operation. EIOCB template may not be valid as defined within the Templates. However, the length of the MSMCW in the EIOCB [DATA0] may always be used to identify the valid words in the EIOCB involved in the failure.
	41:1	If set, indicates MR ERR (MSM or MBC detected error). EIOCB [DATA1] MR field defines the error(s).
	40:1	If set, indicates parity error on the bus defined in the trace field of the EIOCB [ERTYP] word.

NOTE

The EIOCB is decoded as part of the HDU DUMP or more specifically within IDA procedure OMP. ERRORID.

EIOCB (Error Type) Word (cont.)

Field	Bits	Description
Options	39:8	<p>An option value is contained in each trace field entry of the QM Fault Handler listing (p/o Hardware Test Guide for HDU). For example:</p> <pre>EIOCB; EIOCB[ERTYP].OPTIONS=1'10000001'</pre> <p>where '10000001'=bits 39, 38, 37 . . . of the option field.</p> <p>39:1 Data is valid for this trace number. If set, then data in this EIOCB is for this trace number.</p> <p>38:1 Spare</p> <p>37:1 Spare</p> <p>36:1 Halt HDP. If set and error is detected, then all or one HDP is halted, as indicated in the Halt typebit [35].</p> <p>35:1 HDP Halt Type</p> <p>0 = HDP [N] only 1 = All HDPs</p> <p>34:1 Halt HQ. If set and error is detected, then all or one HQ is halted as indicated in the Halt Type bit [33].</p> <p>33:1 HQ Halt Type.</p> <p>0 = HQ[N] only 1 = All HQs</p> <p>32:1 Halt HAQ. If set and error is detected, then HAQ is to be halted.</p>
HDU	31:4	<p>1 = HDU 0 2 = HDU 1 3 = HDU 2 4 = HDU 3</p>

EIOCB (Error Type) Word (cont.)

Field	Bits	Description
HDP	27:4	24:1 = HDP 0 25:1 = HDP 1
	23:3	Spare
Trace Number	20:13	Each trace field entry in the QM fault handler listing is identified by a trace number, identifier field (ID) and error type, as shown below:

TRACE
NUMBER

```
TF=4'092033'  ERROR TYPE
              ID
920 RQ[CW].MARK IS CHECKED.....
    QM HAS NOT FETCHED AN RQ.
    SAME AS FOR *TEXT* TRACE (900).
    EIOCB[ERTYP].OPTIONS=1'10000000'
    (12,1,MARK:1,0,0)
```

ID 7:4 Identifier field definitions:

0	not used
1	Software Interrupt
2	IODB
3	RQ
4	HAQ
5	CQ
6	DQ
7	'Q'
8	'Q' Address
9	IOCB Address
A	Release HDP command
B	HL Buffer
C	Hardware Interrupt
D	Spare
E	Spare
F	Spare

EIOCB (Error Type) Word (cont.)

Field	Bits	Description
Error Type	3:4	Error type definitions:
		0 M.M. Fetch
		1 M.M. Store
		2 M.M. Lock Fetch
		3 Mark
		4 Write Command to HDP
		5 Read Command from HDP (DBUS PARITY ERROR)
		6 Unexpected Status from HDP
		7 Operator Mismatch
		8 spare
		9 Global Priority and/or DL bad
		A QM timeout
		B ECQ Empty
		C spare
		D spare
		E spare
		F not used

HDU COMMAND WORD

	1	0	0										
	47	43	39	35	31+	27+	23+	19+	15+	11+	7+	3	
0	1	0	0										
50	46	42	38	34	30+	26+	22+	18+	14+	10+	6+	2	
0	1	0	OP CODE										
49	45	41	37+	33	29+	25+	21+	17+	13+	9+	5+	1	
0	1	0											
48	44	40	36	32	28	24	20	16	12	8	4	0	

E4630

HDU COMMANDS AND CORRESPONDING OP CODES

OP Code (hex)	HDU Commands
00	Spare
01	Spare
02	Write Error Command Queue Pointer
03	Read Error Command Queue Pointer
04	Set Suspend All Queues Flag
05	Reset Suspend All Queues Flag
06	Return Queue
07	Activate Queue
08	Suspend Queue
09	Spare
0A	Spare
0B	Set Queue Path Address
0C	Write Halt/Load Buffer
0D	Read Halt/Load Buffer
0E	Spare
0F	Spare
10	Write Box ID
11	Read Box ID
12	Spare
13	Spare
14	Spare
15	Spare
16	Spare

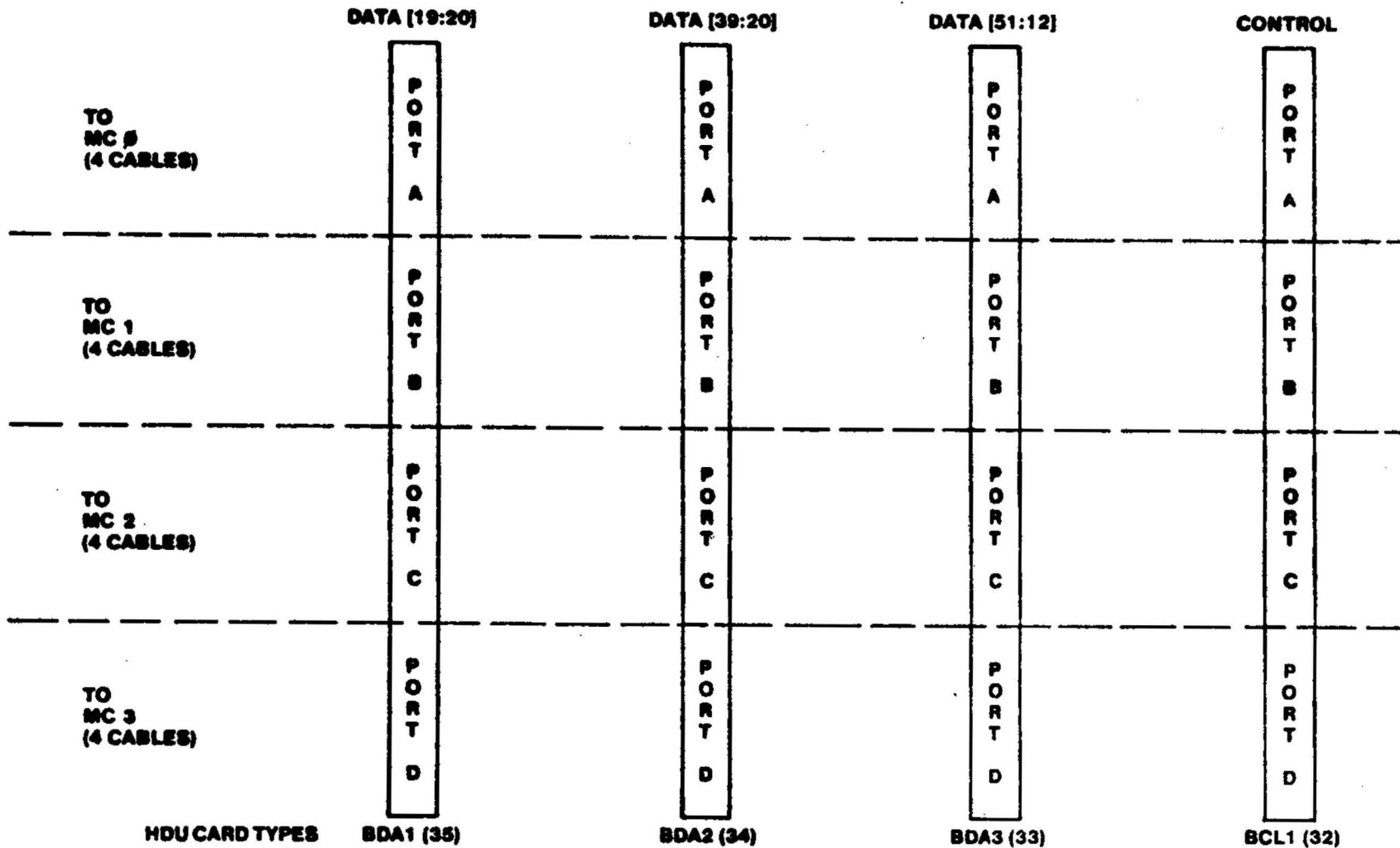
HDU Commands and Corresponding OP Codes (Cont.)

17	Set Queue Pointer
18	Write QM HDP Mask Register
19	Read QM HDP Mask Register
20	General Clear
21	Set Interrupt on Queue Empty Flag
22-29	Spares
30	Clear DLP [n]
31	Spare
32	Spare
33	Write HDP [n] MLI Port Mask
34	Read HDP [n] Port Mask
35	Master Clear Port/s

Box ID Register Format (Cont.)

MBL	31:2	<p>The maintenance bus mode is set up by a three position switch. The switch is used to control maintenance access to the HDU. The maintenance bus modes are:</p> <table border="0" style="margin-left: 40px;"> <tr> <td style="text-align: center;">MBM [31:2]</td> <td style="text-align: left;">S1 Position</td> </tr> <tr> <td style="text-align: center;">1</td> <td>ENABLED</td> </tr> <tr> <td style="text-align: center;">2</td> <td>DISABLED</td> </tr> <tr> <td style="text-align: center;">3</td> <td>NOR (normal)</td> </tr> </table> <p>In normal mode, access to the maintenance bus is determined by the state of the MBE bit [36:1] in the Box ID register. Software has read-only access to the S1 switch positions</p> <p>MBM Switch Location:</p> <ul style="list-style-type: none"> A 12 Cabinet Power Control Panel A 15 TRMH Card in the HDU Backplane 	MBM [31:2]	S1 Position	1	ENABLED	2	DISABLED	3	NOR (normal)
MBM [31:2]	S1 Position									
1	ENABLED									
2	DISABLED									
3	NOR (normal)									
ASD Initialized Bit	32:1	<p>Indicates that SYCON has loaded the QM with ASD or ASN microcode.</p> <ul style="list-style-type: none"> 1 = ASD microcode 0 = ASN microcode (Not used in the A 12 System) 								
S	33:1	Software running light on.								
H	34:1	HDU is halted.								
	35:1	Halt/Load HDU. Used by software only. This bit is used to identify which HDU of a partition is to be used for system initialization.								
MBE	36:1	<p>The maintenance bus is enabled to the mainframe if MBM = 1, or MBM = 3 and MBE = 1</p> <ul style="list-style-type: none"> 1 = enabled 2 = disabled 								
PID	39:3	<p>Partition ID (Used by software only.)</p> <ul style="list-style-type: none"> 0 = Power up, but not initialized by system or maintenance software. 1-4 = Assigned to partition 1-4 (a member of a partition 1, 2 and so on). 5 = Maintenance (owned by a maintenance process). 6 = Inhibited: available for use by a maintenance process (but not for inclusion in a running partition). 7 = Available for inclusion in partition. 								
MC Enable	43:4	Not used. (There is only one MC in a non-partitioned system.)								
HDU Numbers	47:4	<ul style="list-style-type: none"> 1 = HDU 0 2 = HDU 1 4 = HDU 2 8 = HDU 8 								

A 15 MC INTERFACE TO HDU CARD PORT LOCATIONS



NOTE: THERE IS ONLY ONE MC IN A NON-PARTITIONED SYSTEM.

E5332

SECTION 4

GENERAL SYSTEM INFORMATION

SYSTEM DATA COLLATING SEQUENCE

<u>EBCDIC Graphic</u>	<u>Decimal Value</u>	<u>EBCDIC Internal</u>	<u>Hex. Graphic</u>	<u>EBCDIC Card Code</u>	<u>Octal</u>
BLANK	64	0100 0000	40	No Punches	60
[74	0100 1010	4A	12 8 2	33
.	75	0100 1011	4B	12 8 3	32
<	76	0100 1100	4C	12 8 4	36
(77	0100 1101	4D	12 8 5	35
+	78	0100 1110	4E	12 8 6	
	79	0100 1111	4F	12 8 7	37
&	80	0101 0000	50	12	34
]	90	0101 1010	5A	11 8 2	76
S	91	0101 1011	5B	11 8 3	52
*	92	0101 1100	5C	11 8 4	53
)	93	0101 1101	5D	11 8 5	55
:	94	0101 1110	5E	11 8 6	56
	95	0101 1111	5F	11 8 7	57
.	96	0110 0000	60	11	54
/	97	0110 0001	61	0 1	61
.	107	0110 1011	6B	0 8 3	72
%	108	0110 1100	6C	0 8 4	73
-	109	0110 1101	6D	0 8 5	74
>	110	0110 1110	6E	0 8 6	16
?	111	0110 1111	6F	0 8 7	14
:	122	0111 1010	7A	8 2	15
*	123	0111 1011	7B	8 3	12
@	124	0111 1100	7C	8 4	13
.	125	0111 1101	7D	8 5	17
=	126	0111 1110	7E	8 6	75
"	127	0111 1111	7F	8 7	77
(+)PZ	192	1100 0000	C0	12 0	20
A	193	1100 0001	C1	12 1	21
B	194	1100 0010	C2	12 2	22
C	195	1100 0011	C3	12 3	23
D	196	1100 0100	C4	12 4	24
E	197	1100 0101	C5	12 5	25
F	198	1100 0110	C6	12 6	26
G	199	1100 0111	C7	12 7	27
H	200	1100 1000	C8	12 8	30
I	201	1100 1001	C9	12 9	31
(!)MZ	208	1101 0000	D0	11 0	40
J	209	1101 0001	D1	11 1	41

FOR A 12 SYSTEM CPMC CIRCUIT CARD LOCATIONS

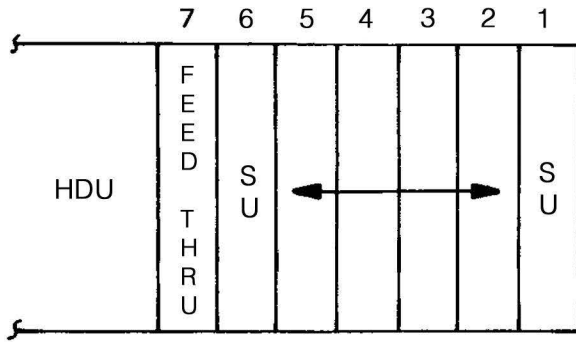
HMC BOARDS	HMCSCMBD	30
	HMCMICRO	29
MC BOARD	HDUADPTR	28
MAINT BD	CCOMPARE	27
MC BOARDS (NOTE)	MSMRIMIN	26
	MCMSCHED	25
	MSMIISIM	24
CPM	CPJOWRIT	23
	CPUSTACK	22
	CPSCANER	21
	CPBUFLIT	20
	CPADDINX	19
	CMAUOUT3	18
	CMAUINN	17
	CRCACONT	16
	CRUCACHE	15
	CREVDATA	14
	CCDBLEST	13
	CCDBMIDL	12
	CCDBMOST	11
	CRUPIPEC	10
	CRUPCONT	9
	CRMISCON	8
CLOCK BOARD	HMODBUFR	7
CPM	CEUMAJ01	6
	CEUMJCTL	5
	CEUSAUEW	4
	CEMINOR2	3
	CEUMICRO	2
	CECDBCTL	1

NOTE: FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO CPCM CARD LOCATOR CONTAINED IN VOLUME 4 OF A 12 T&F DOCUMENTATION.
 MCMSCHED2 IS USED IN SLOT 25 INSTEAD OF MCMSCHED IN ALL A 12E SYSTEMS.

ES879

MEMORY STORAGE CIRCUIT CARD LOCATIONS

(CARDS INSERTED FROM THIS SIDE)



E5880

MHDU CIRCUIT CARD LOCATIONS

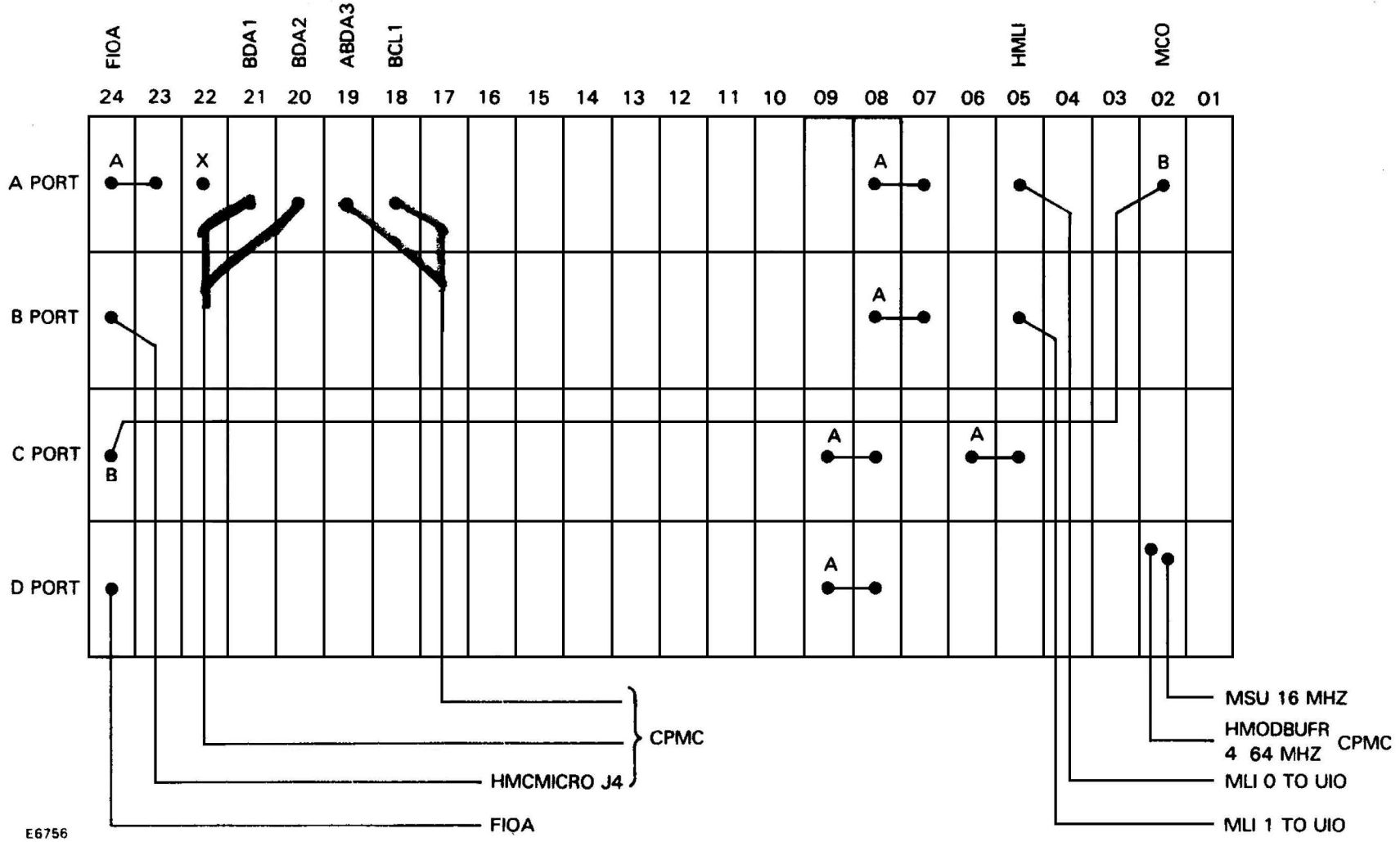
	24
FIOA	24
HMCH	23
ATRMH	22
BDA1	21
BDA2	20
BDA3	19
BCL1	18
QCL2	17
QCL1	16
QDM3	15
QDM2	14
QDM1	13
HCKA	12
HCKB	11
AHMIN	10
HPM2	9
HCNT	8
HPM1	7
HUSQ	6
HMLI	5
TRNH	4
	3
MASTER CLOCK	2
	1

HDP 0

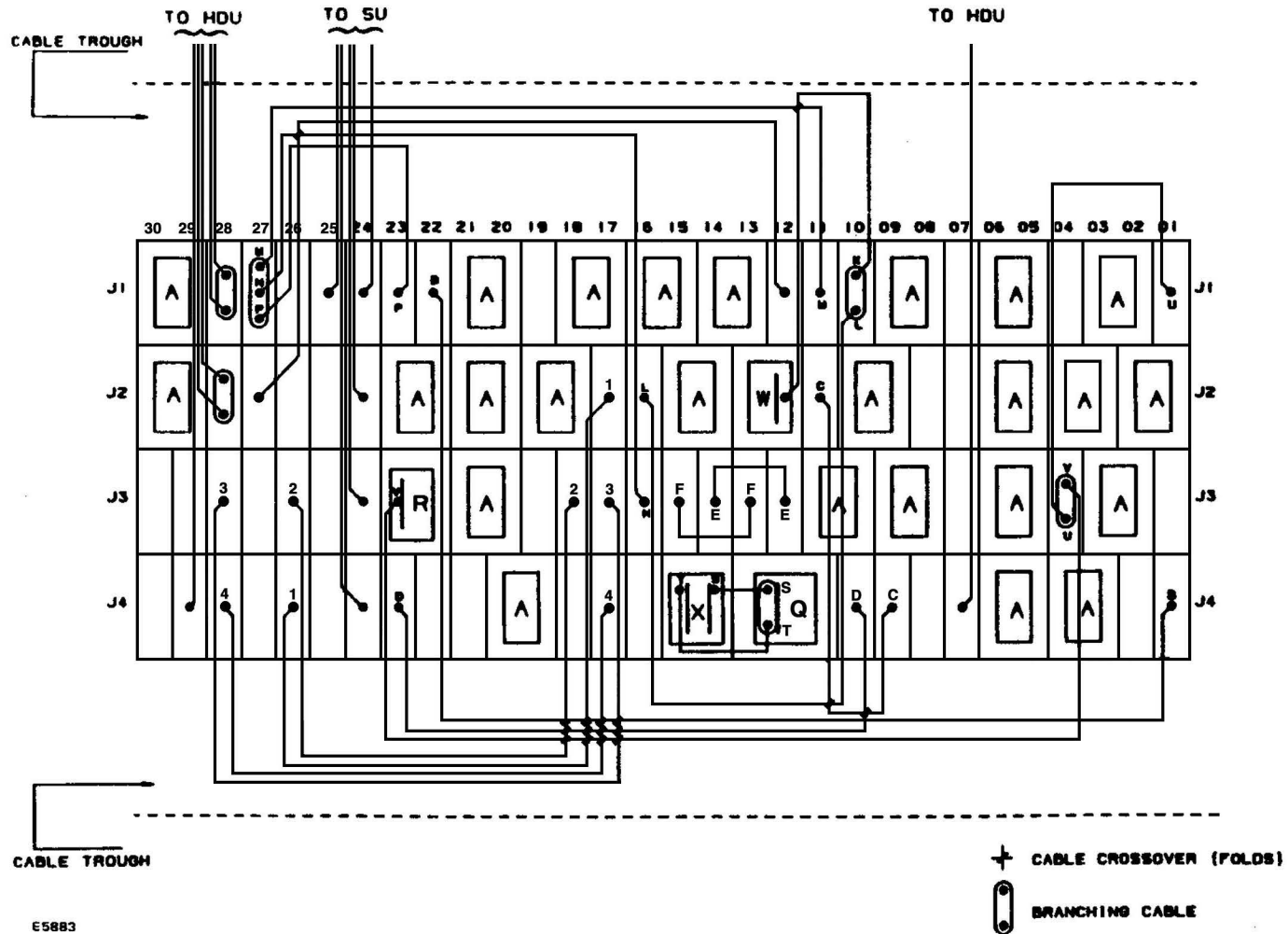
NOTE: FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO MHDU CARD LOCATOR CONTAINED IN VOLUME 4 OF A12 T & F DOCUMENTATION.

E5881

CPMC CARD PORT LOCATION ASSIGNMENTS



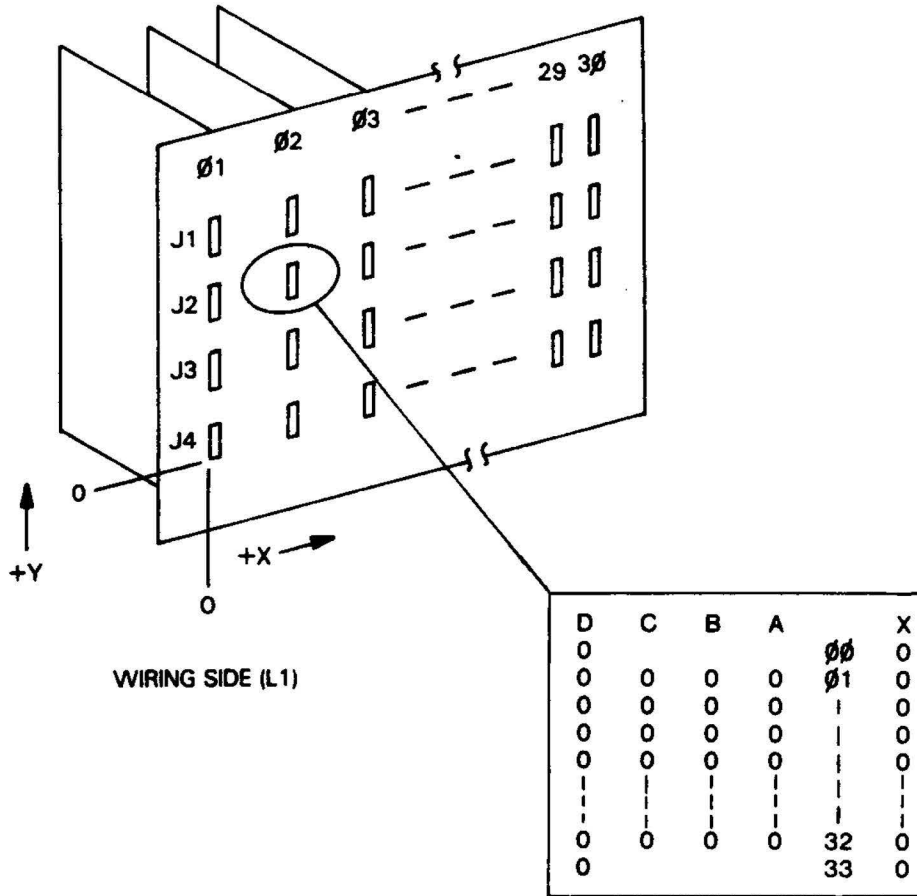
CPMC CARD PORT LOCATION ASSIGNMENTS



1192432

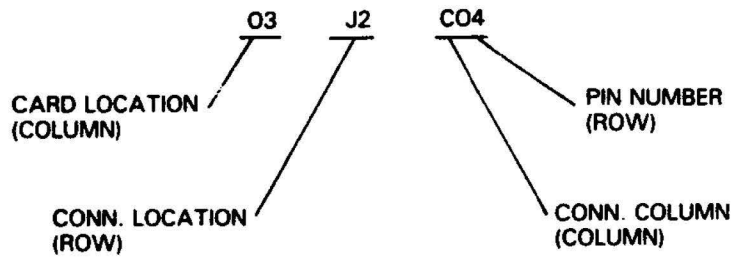
4-7

BACKPLANE LOCATION CODING



FOR DA INPUTS, EXCLUDE THE "J" (6 CHARACTERS MAX.)

EXAMPLE:



E5884

FOR A 15 SYSTEM

CPM CIRCUIT CARD LOCATIONS

CARD INSERTION SIDE

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CARD TYPE	CMODBUF2	HMCBMBD	HMCMICRO	CCOMPARE	CPARTIT2	CPARTIT1	CPARTIT1	CPJOWRIT	CPUSTACK	CPSCANER	CPBUFLIT	CPADDINX	CMAUOUTS	CMAUINN	CRCACONT	CRUCACHE	CREVDATA	CCDBLEST	CCDBMIDL	CCDBMOST	CRUPIPEC	CRUPCONT	CRIBSCON	(SPARE)	CEUMAJOI	CEUMJCTL	CEUBAUEW	CEMINOR2	CEUMICRO	CECDSECTL
CLASSIFICATION	C	K	HMC	MEMORY PARTITIONING			PCU					MAU		CDB			RU			WU				WU						

NOTE: FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO CPM CARD LOCATOR CONTAINED IN VOLUME 4 OF A15 T & F DOCUMENTATION.

E6562

MC CIRCUIT CARD LOCATIONS

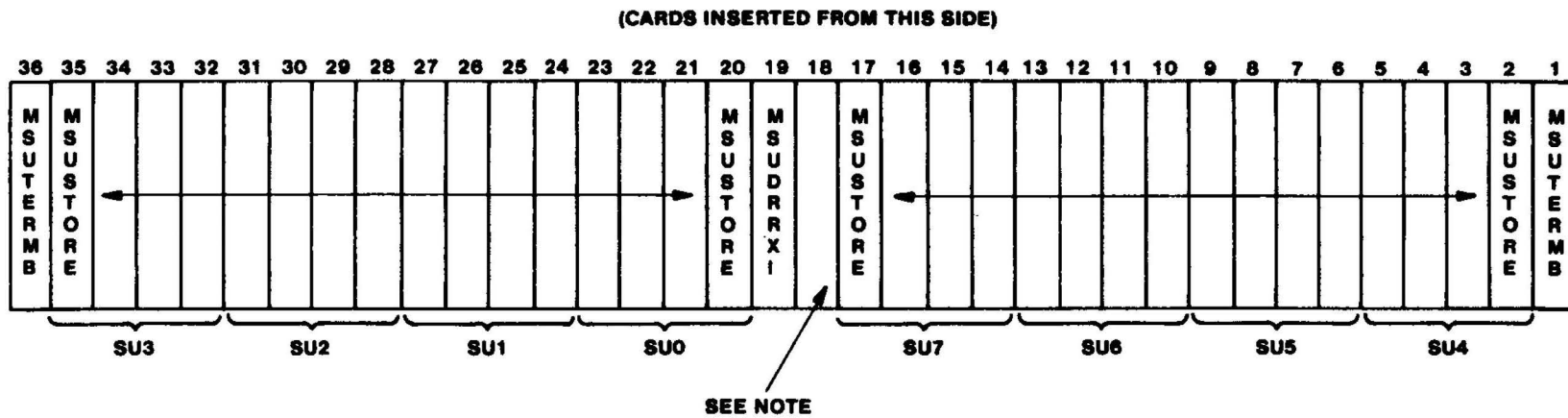
(CARDS INSERTED FROM THIS SIDE)

30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
M M O D B U F 2	H M C S C M B D	H M C M I C R O		M C R I M O U T 5	M C R I M O U T 4	M C R I M O U T 3	M C R I M O U T 2	M C R I M O U T 1	M C R I M O U T 0	M S M I I S I M 3	M S M I I S I M 2	M S M I I S I M 1	M S M I I S I M 0	M C M S C H E D 1	M C M S C H E D 0	M S M R I M I N 5	M S M R I M I N 4	M S M R I M I N 3	M S M R I M I N 2	M S M R I M I N 1	M S M R I M I N 0	M A D A P T R B 3	M A D A P T R B 3	M A D A P T R B 2	M A D A P T R B 2	M A D A P T R B 1	M A D A P T R B 1	M A D A P T R B 0	M A D A P T R B 0

NOTE: FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO MC CARD LOCATOR CONTAINED IN VOLUME 6 OF A15 T & F DOCUMENTATION.

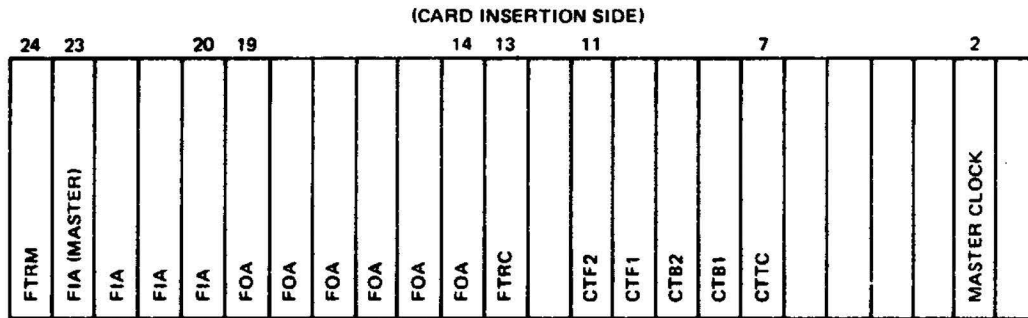
E6104

MEMORY STORAGE CIRCUIT CARD LOCATIONS



- NOTE:**
1. IF ALL EIGHT MSUs INTERFACE A SINGLE SIM, MSU DRRXU IS USED IN SLOT 18. IF SUs INTERFACE TWO SIMs, MSU DRRXI IS USED IN SLOT 18.
 2. FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO MEM STORAGE CARD LOCATOR CONTAINED IN VOLUME 6 OF A15 T & F DOCUMENTATION.

SCC CIRCUIT CARD LOCATIONS



NOTE: FOR CARD ASSEMBLY ORDER PL NUMBERS, REFER TO
 SCC CARD LOCATOR CONTAINED IN VOLUME 13 OF
 A15 T & F DOCUMENTATION.

E4368

MEX PORT ID ASSIGNMENTS

STYLE	BOX	MEX ID	MEX TYPE	REQUESTOR NO.
ALL A 15 Styles:				
Mex Loads:	SMP	7	FOA1	none
	MCO	10	FOA1	none
	Card tester	16	FOA2	none
Mex Sources:	SMP		FIA1	none
	MIPs		FIA2	none
A 15-F	MCM	8	FOA3	none
	CPM	5	FOA3	5
	HDU	0	FOA1	0
A 15-H	MCM	8	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	HDU	0	FOA1	0
A 15-I	MCM	8	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	HDU	0	FOA1	0
	HDU	1	FOA1	1
A 15-J	MCM	8	FOA3	none
	MCM	9	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	HDU	0	FOA1	0
	HDU	1	FOA1	1
A 15-K	MCM	8	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	CPM	3	FOA3	3
	HDU	0	FOA1	0
	HDU	1	FOA1	1
A 15-L	MCM	8	FOA3	none
	MCM	9	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	CPM	3	FOA3	3
	HDU	0	FOA1	0
	HDU	1	FOA1	1
A 15-M	MCM	8	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	CPM	3	FOA3	3
	CPM	2	FOA3	2
	HDU	0	FOA1	0
	HDU	1	FOA1	1
A 15-N	MCM	8	FOA3	none
	MCM	9	FOA3	none
	CPM	5	FOA3	5
	CPM	4	FOA3	4
	CPM	3	FOA3	3
	CPM	2	FOA3	2
	HDU	0	FOA1	0
	HDU	1	FOA1	1

E6588

CPM CONFIDENCE LOCATIONS

NOTE: Absolute addresses are shown assuming confidence is loaded at zero. If the load-address is other than zero, absolute addresses must be offset accordingly.

Absolute	DO-Relative	DESCRIPTION (IDA name in braces) * May be modified when CPM is halted.
0	-	PBR and F setting to start confidence (entrance to driver's initialization)
1C0	C0	* Testcase Index (TCI)
1C1	C1	* TCI-Stop (TS)
1C2	C2	* Cycle
1C3	C3	* Cycle-Limit (CL)
1C4	C4	* Option-Word: (Bit) - meaning - default (0:1) - Loop-On-Error (LOE) - reset (2:1) - Stop-On-Error (SOE) - set (3:1) - Delete-On-Error (DOE) - reset (4:1) - Freeze-TC-Index (FTI) - reset (5:1) - Recycle (RCL) - set (38:1) - Stop-Before-Test (SBT) - reset
1C8	C8	testcase base (PBR setting)
1C9	C9	address of testcase descriptor (TCI+400)
1CA	CA	testcase ID
1E0-1EF	E0-EF	Error Word Array - usual meaning:
1E0	E0	0 - Error Header Word
1E1	E1	1 - Argument Address or Iteration Count
-	-	2 - Actual Result (first word if D.P.)
-	-	3 - 2nd word of D.P. Actual Result
-	-	4, 5 - Expected Result
-	-	6, 7 - Top-of-Stack Operand
-	-	8, 9 - TOS-1 Operand
-	-	A, B - Tos-2 Operand
-	-	C, D - TOS-3 Operand
1EE	EE	E - Miscellaneous
1EF	EF	F - F Setting for Unexpected Interrupt
400	-	Testcase descriptor list, containing: number of testcases in this test
401	-	Descriptor for Testcase #1 (TCI=1)
402	-	Descriptor for Testcase #2 (TCI=2)
-	-	Etc.
E6589		

NORMAL STACK REGISTER CONTENTS

BOSR - FE
DO - 100
F - 100
S - 307
LOSR - 300

STOPS IN THE DRIVER (SDI:PWI:PSI)

0020:0003:2 - stop at beginning of testcase
0020:0004:2 - stop on error
0020:0005:2 - stop at end of cycle (normal stop)

STACK CONTENTS

Absolute	DO-Relative	Description
100	0	DO MSCW
101	1	DO RCW
102	2	stack vector descriptor
103	3	PCW for interrupt handler
104	4	descriptor for all memory
105	5	segment descriptor for current testcase
10A	A	initialization flag
10B	B	flag for intrinsic 1A2 called
110	10	descriptor for stack#0
11B	1B	base address of test (normally 0)
11F	1F	highest address used in test
120	20	segment descriptor for driver
121	21	PCW for testcase return to driver
122	22	PCW for driver entry to testcase
123	23	PCW for driver's interrupt handler
124	24	MSCW used in stack cutback
125	25	RCW used in stack cutback
126	26	Copy of stack vector descriptor
128	28	dummy RCW
129	29	dummy segment descriptor
12A	2A	dummy data descriptor
12B	2B	mask for unpredicted interrupts
12D	2D	comm-handler return address
12E	2E	error handler call flag
130	30	PCW for call on error handler
133	33	PCW for testcase interrupt handler
134	34	normal setting of S-register
13A	3A	error handler return address
140	40	interrupt : MSCW
141	41	Parameters : RCW
142	42	returned : P1
143	43	to testcase : P2
14A	4A	testcase interrupt handler address
160-167	60-67	MSM array
168	68	page counter (for 1A2)
16A	6A	MSM requestor mask
16B	6B	MSM status word
1A0	A0	PCW for intrinsic 1A0
1A2	A2	PCW for intrinsic 1A2
1B0	B0	segment descriptor for 1A0
1B2	B2	segment descriptor for 1A2
1C0	C0	testcase index (TCI)
1C1	C1	TCI-Stop (TS)
1C2	C2	cycle
1C3	C3	cycle-limit (CL)
1C4	C4	option word
1C8	C8	testcase base address (PBR)
1C9	C9	address of testcase descriptor
1CA	CA	testcase ID
1D0	D0	normal setting of D0
1E0-1EF	E0-EF	error word array
200-2FF	100-1FF	testcase D0 work area

TESTCASE DESCRIPTOR FORMAT

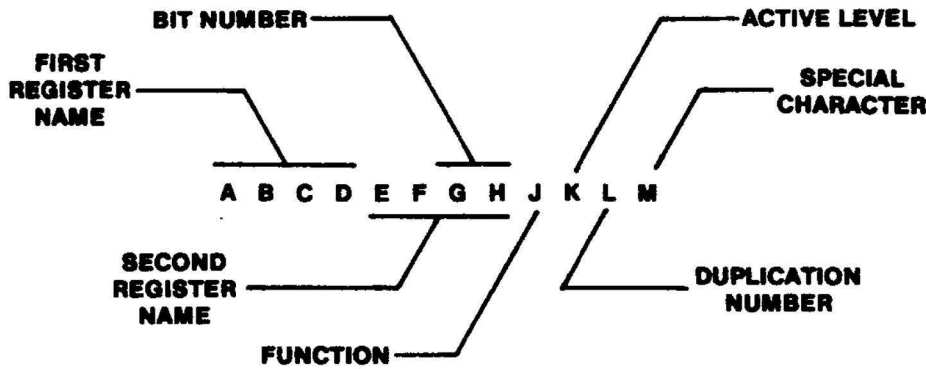
Each descriptor is a single-precision word (tag 0) with the following fields:

- [19:20] - Testcase ID (hex)
- [35:16] - Base Address of Testcase (PBR)
- [46:11] - Length of Testcase in words
- [47: 1] - Presence-bit (set by default, if reset then the testcase will not be run)

E6586

SIGNAL NAMING CONVENTIONS

A 15 signal names consist of 12 characters, as follows:



The first 11 characters of the 12-digit signal name are letters, numerals, periods, or dashes; the last can be any character. The first letter of a register name generally indicates the source of the signal (by functional unit) or its primary usage, as follows:

- C - Central Data Buffer
- D - Deallocation Control
- E - Execution Unit
- I - Interrupt Unit
- J - Job Number Control
- M - Memory Access Unit
- P - Program Control Unit
- R - Reference Unit
- X - Processor State Information
- Y - Maintenance Information

The second letter of a register name indicates the level of a pipelined unit or area of a parallel unit. The function character (ninth character) indicates any of the following signal functions:

Signal Naming Conventions (cont.)

Function	Meaning	First Reg. Name	Second Reg. Name	Bit No.
A	Load Register	Any Register	Any Signal	Optional
B	Backup or Partial	Any Signal	Any Signal	Optional
C	Decrement Register	Any Signal	Any Signal	Not Used
E	Enable (Latch, MUX)	Register or Field	Any Signal	Optional
G	Complement if Greater	REgister or Field	Dest. Reg. or Value	Not Used
I	Increment Register	Any Register	Not Used	Not Used
L	Less Than Comparison	Any Register	Dest. Reg. or Value	Not Used
N	FF Data Input	Any Register	Dest. Reg. or Value	Specific Binary
O	Older Comparison	Any Register	Dest. Reg. or Value	Not Used
Q	Equal Comparison	Any Register	Dest. Reg. or Value	Not Used
R	FF Input Reset	Any Register	Dest. Reg. or Value	Specific Binary
S	FF Set Input	Any Register	Dest. Reg. or Value	Specific Binary
T	Transfer	Source Reg. or Value	Dest. Reg.	Optional
W	Write into Storage	Storage Name	Not Used	Optional

The special character (last character of a signal name) has the following meanings and effects:

Character	Meaning/Effect
S	Output to a backplane bus (critical).
C	Critical input signal to card, no terminator.
P	Critical input signal to card, possible terminator.
F	Source or terminated load of a foreplane signal.
B	Source of a backplane signal.
T	Terminated backplane input signal to a card.
M	Signal exists in foreplane and backplane.
N	Terminated backplane signal to card (treated as critical signal for routing purposes).
. or -	Terminated signal; exists only on card.
Z	Unterminated signal; exists only on card.

E6590

Signal Naming Conventions (cont.)

The duplication number (next-to-last character in the signal name) indicates multiple copies of the same logical signal. This character can be a numeral from 0 through 9 or a letter from A through Z.

PROCESSOR STATE NAMING CONVENTION

First Letter (Unit) :

- R - Reference
- E - Execution
- P - Program Control
- S - Store Data
- M - Memory Access
- C - Central Data Buffer
- X - Stack Control, Lex Level
- W - Write
- J - Job Control
- T - Maintenance

Second Letter
(Level in Unit) :

- A - (R) Address Couple; (E) ALU
- C - (R) Cache; (E) CDB
- D - (R) Deferred Reference Queue;
(E) CDB Destination
- E - (R) Evaluate
- I - (R) Interrupt from Evaluate Level;
(E) Interrupt
- M - (R) MAU Interface
- O - Operator
- P - (R) Parameter Queue
- R - (R) Routine
- S - (R) SAL Output
- T - (R) Top of Stack Queue
- W - (R) Write
- F - (R) Interrupt from Write Level (Fault)
- L - (R) Look Ahead
- U - Unfinished Micro-operator Queue
- Z - No specific Level (Used across levels)

Third Letter
(Common Functions
between Units) :

- J - Job Number
- A - (R), (P) Address; (E) Accumulator
- D - Data
- R - Result CDB Location
- X - (R) X Input to CDB
- M - Micro-operator
- E - Exception Code
- V - Variant Bits
- L - LIT Data

Four-Letter Names:

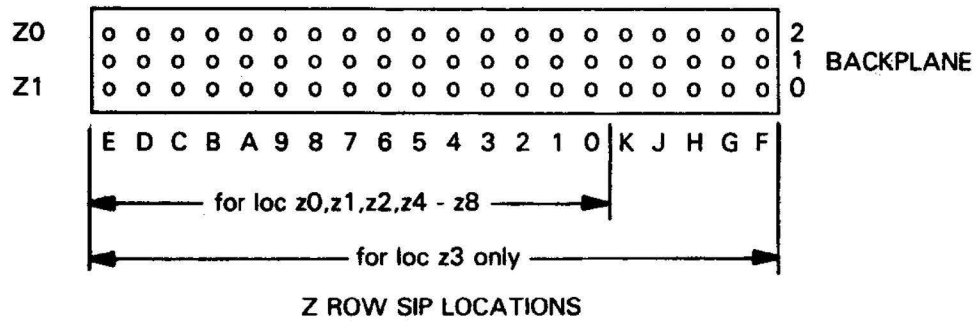
Third Letter	Fourth Letter	
A	C	(R) Address Couple
S	A,B,C,D	Stack Positions

CARD ARRAY LOCATIONS

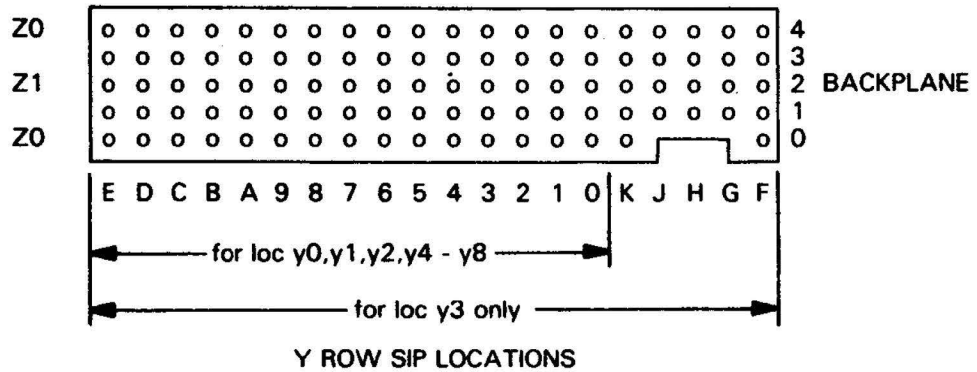
FORE PLANE	J1	Y0	Y1	Y2	Y3	Y4		Y5	Y6	Y7	Y8	P1
		A0	A1	A2	A3	A4		A5	A6	A7	A8	
		B0	B1	B2	B3	B4		B5	B6	B7	B8	
	J2	C0	C1	C2	C3	C4		C5	C6	C7	C8	P2
		D0	D1	D2	D3	D4		D5	D6	D7	D8	
	J3	E0	E1	E2	E3	E4		E5	E6	E7	E8	P3
		F0	F1	F2	F3	F4		F5	F6	F7	F8	
		G0	G1	G2	G3	G4		G5	G6	G7	G8	
	J4	H0	H1	H2	H3	H4		H5	H6	H7	H8	P4
		I0	I1	I2	I3	I4		I5	I6	I7	I8	
		Z0	Z1	Z2	Z3	Z4		Z5	Z6	Z7	Z8	

E7427

ARRAY LOCATIONS A 4 THROUGH 14

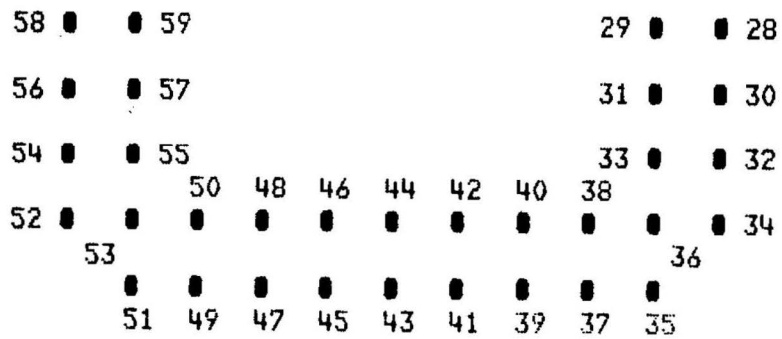
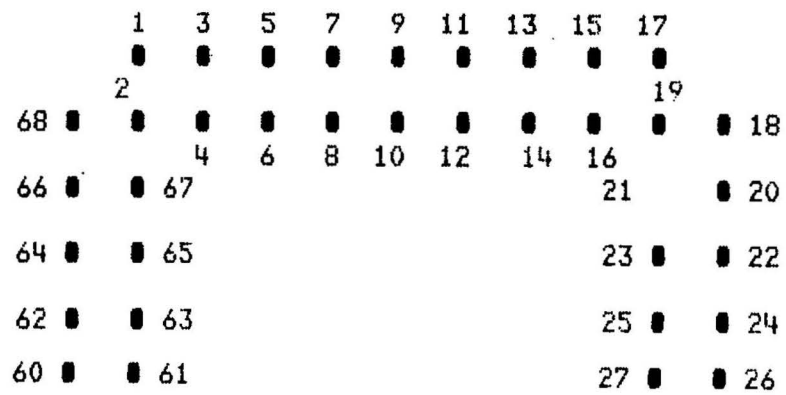


E7430



E7431

PIN DESIGNATIONS WITHIN ARRAY LOCATION



CONNECTOR TYPE PIN USAGE

FCON	HCON	TCON	CONN	BCON
ABCDEF	ABCDEF	FEDCBA	FEDCBA	FEDCBA
32 OGO...	32 OG 1	...GOG 1	...GOG 1
31 GOG...	31 *O 2	...O*O 2	...O*O 2
30 OGO...	30 OG 3	...GOG 3	...GOG 3
29 GOG...	29 #O 4	...O#O 4	...O#O 4
28 OGO...	29 OG 5	...GOG 5	...GOG 5
27 GOG...	27 *O 6	...O*O 6	...O*O 6
26 OGO...	26 OG 7	...GOG 7	...GOG 7
25 GOG...	25 GO....	... *O 8	...O*O 8	...O*O 8
24 OGO...	24 GO....	...GOG 9	...GOG 9	...GOG 9
23 GOG...	23 GO....	...O#O 10	...O#O 10	...O#O 10
22 OGO...	22 GO....	...GOG 11	...GOG 11	...GOG 11
21 GOG...	21 GO....	...O*O 12	...O*O 12	...O*O 12
20 OGO...	20 GO....	...GOG 13	...GOG 13	...GOG 13
19 GOG...	19 GO....	...O*O 14	...O*O 14	...O*O 14
18 OGO...	18 GO....	...GOG 15	...GOG 15	...GOG 15
17 GOG...	17 GO....	...O#O 16	...O#O 16	...O#O 16
16 OGO...	16 GO....	...GOG 17	...GOG 17	...GOG 17
15 GOG...	15 GO....	...O*O 18	...O*O 18	...O*O 18
14 OGO...	14 GO....	...GOG 19	...GOG 19	...GOG 19
13 GOG...	13 GO....	...O*O 20	...O*O 20	...O*O 20
12 OGO...	12 GO....	...GOG 21	...GOG 21	... OG 21
11 GOG...	11 GO....	...O#O 22	...O#O 22	... #O 22
10 OGO...	10 GO....	...GOG 23	...GOG 23	... OG 23
9 GOG...	9 GO....	...O*O 24	...O*O 24	... *O 24
8 OGO...	8 GO....	...GOG 25	...GOG 25	... OG 25
7 GOG...	7 GO....	...O*O 26	...O*O 26	... *O 26
6 OGO...	6 GO....	...GOG 27	...GOG 27	... OG 27
5 GOG...	5 GO....	...O#O 28	...O#O 28	... #O 28
4 OGO...	4 GO....	...GOG 29	...GOG 29	...GOG 29
3 GOG...	3 GO....	...O*O 30	...O*O 30	...O*O 30
3 OGO...	2 GO....	...GOG 31	...GOG 31	...GOG 31
1 GOG...	1 GO....	...O*O 32	...O*O 32	...O*O 32

PIN LEGEND

G = GROUND
 # = -2.0 VOLTS
 * = -5.2 VOLTS
 = +5.2 VOLTS
 O = SIGNAL

FCON

Foreplane connector area for J1, J2, J3, and J4.

HCON

Foreplane connector area for B 7900 style cables.

TCON

Backplane connector area for P1, +5 volts only.

CONN

Backplane connector area for P1, P2, P3, and P4 (standard card).

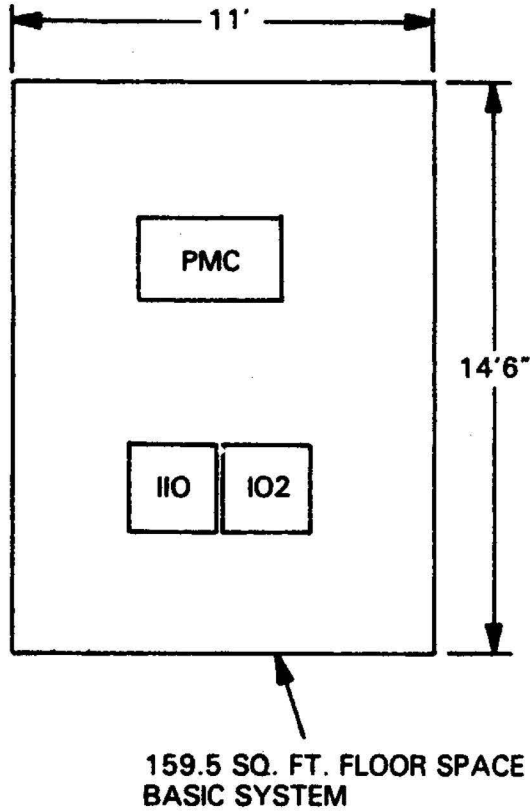
BCON

Backplane connector area for P4, +5 volts only.

E6585

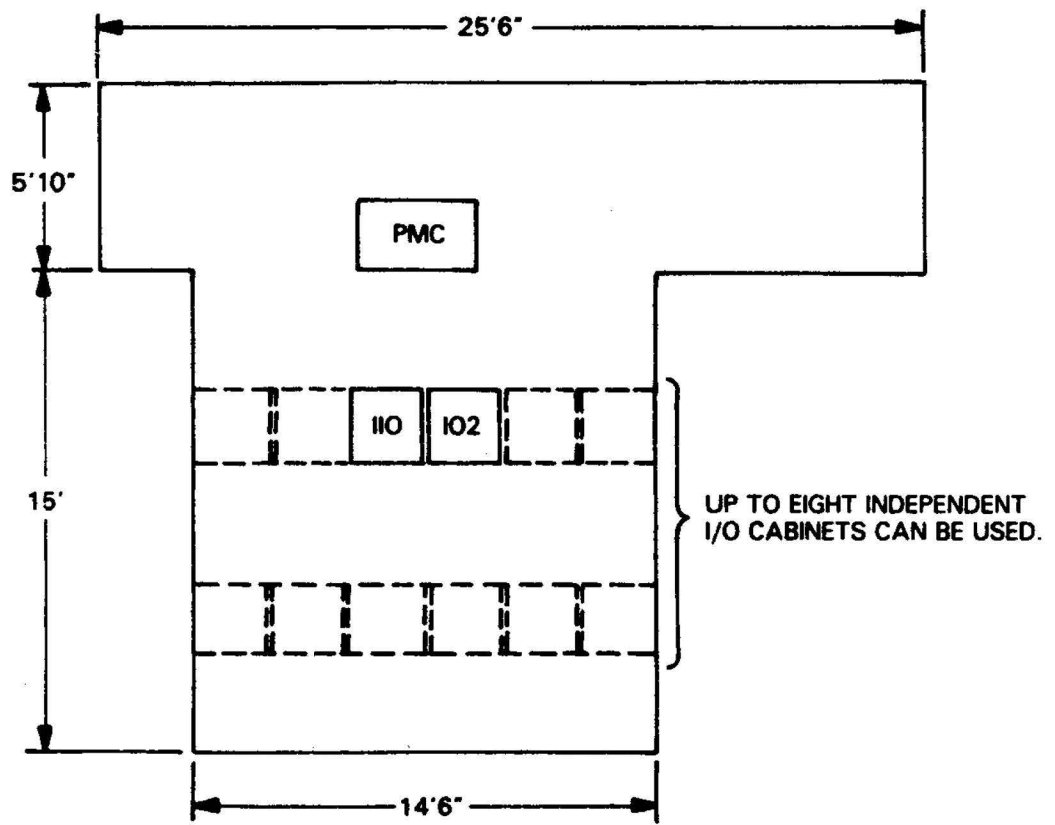
SECTION 5 SYSTEM LAYOUTS

BASIC A 12 SYSTEM



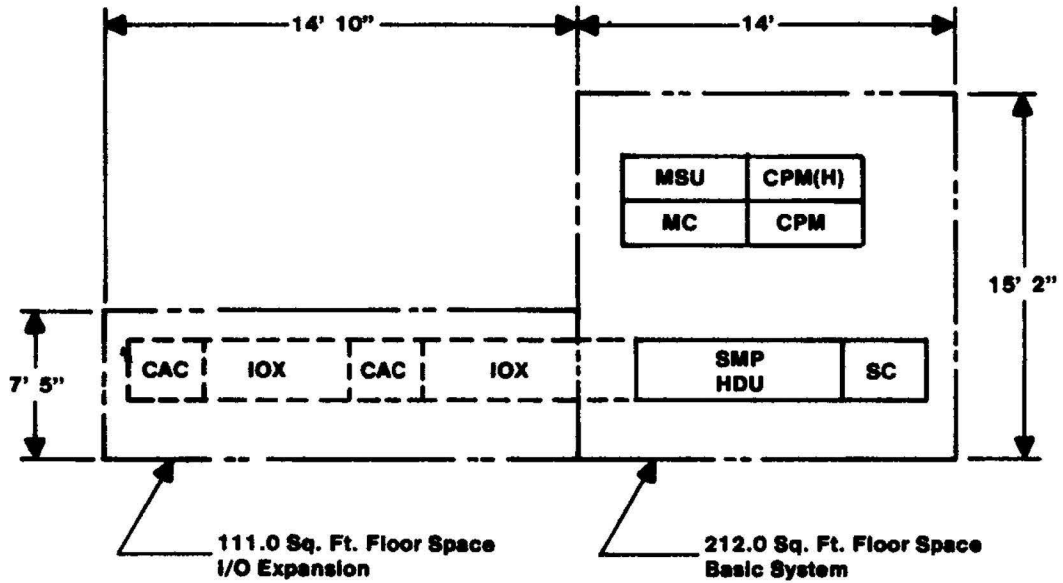
E5885

A 12 SYSTEM WITH EXPANSION ALLOWANCE



E5886

A 15-F, A 15-H

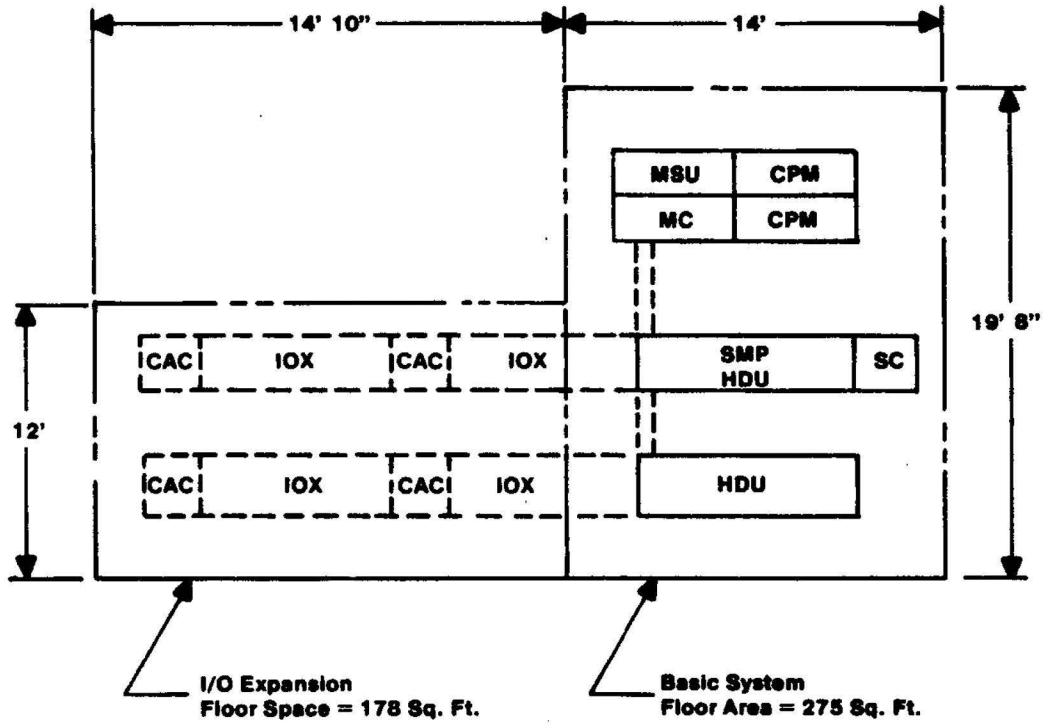


MAX SYSTEM FLOOR AREA = 323 SQ. FT.

NOTE: System Maintenance Station (SMS) and Operator Table also included with each System.

E6575

A 15-1

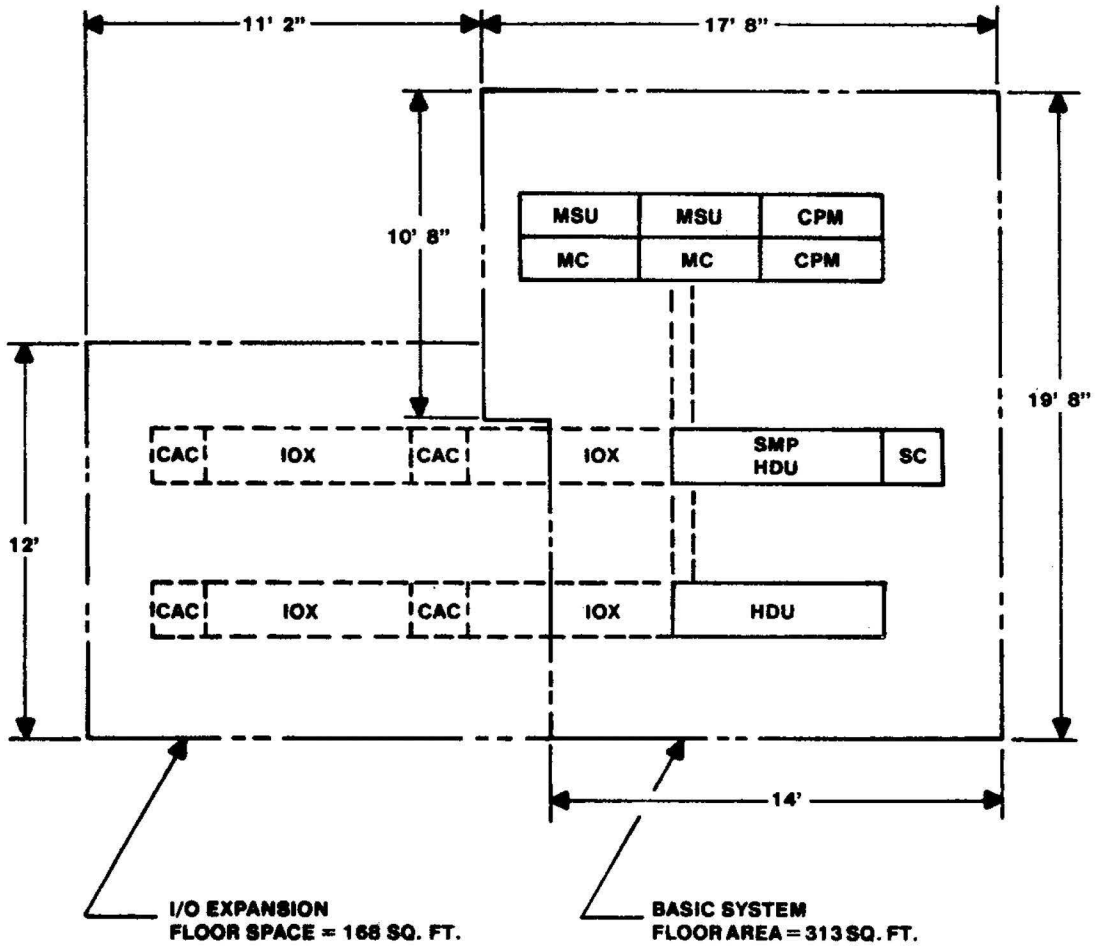


Maximum System Floor Area = 453 Sq. Ft.

NOTE: System Maintenance Station (SMS) and Operator Table also included with each System.

E6576

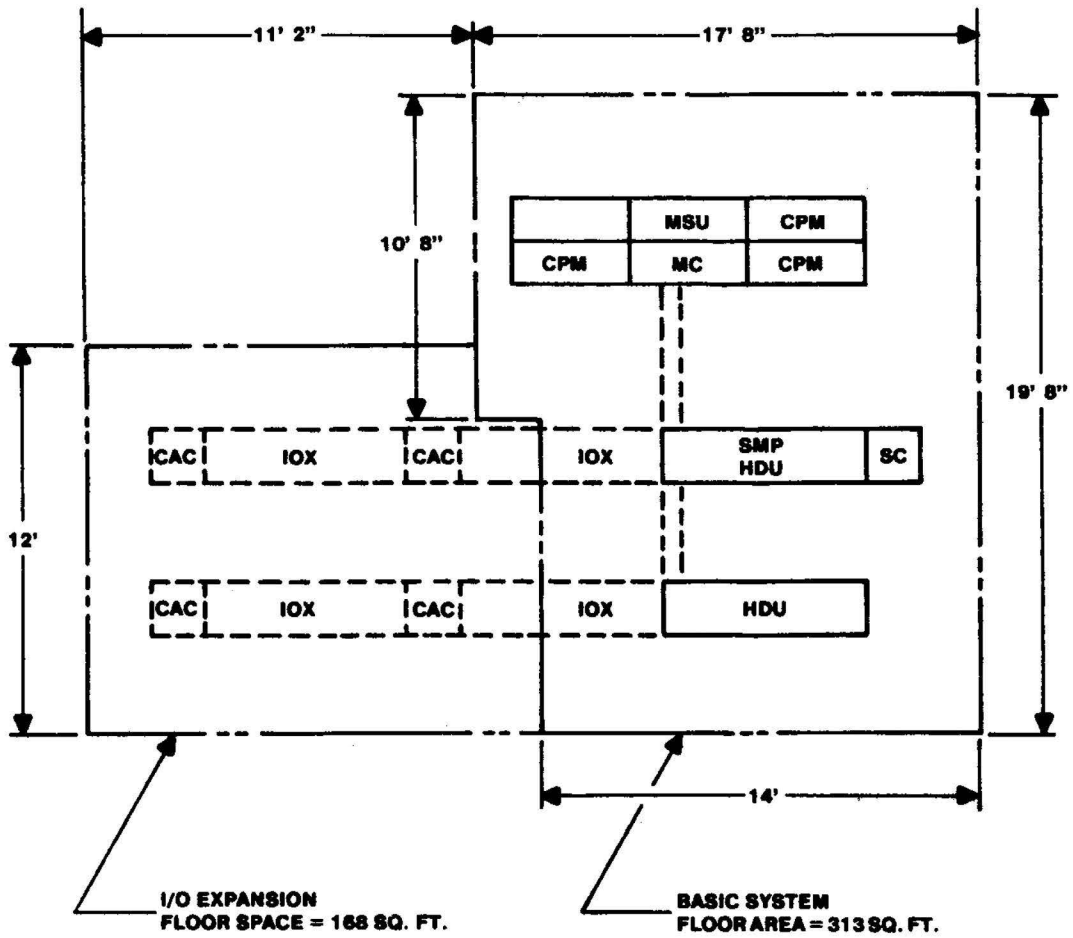
A 15-J



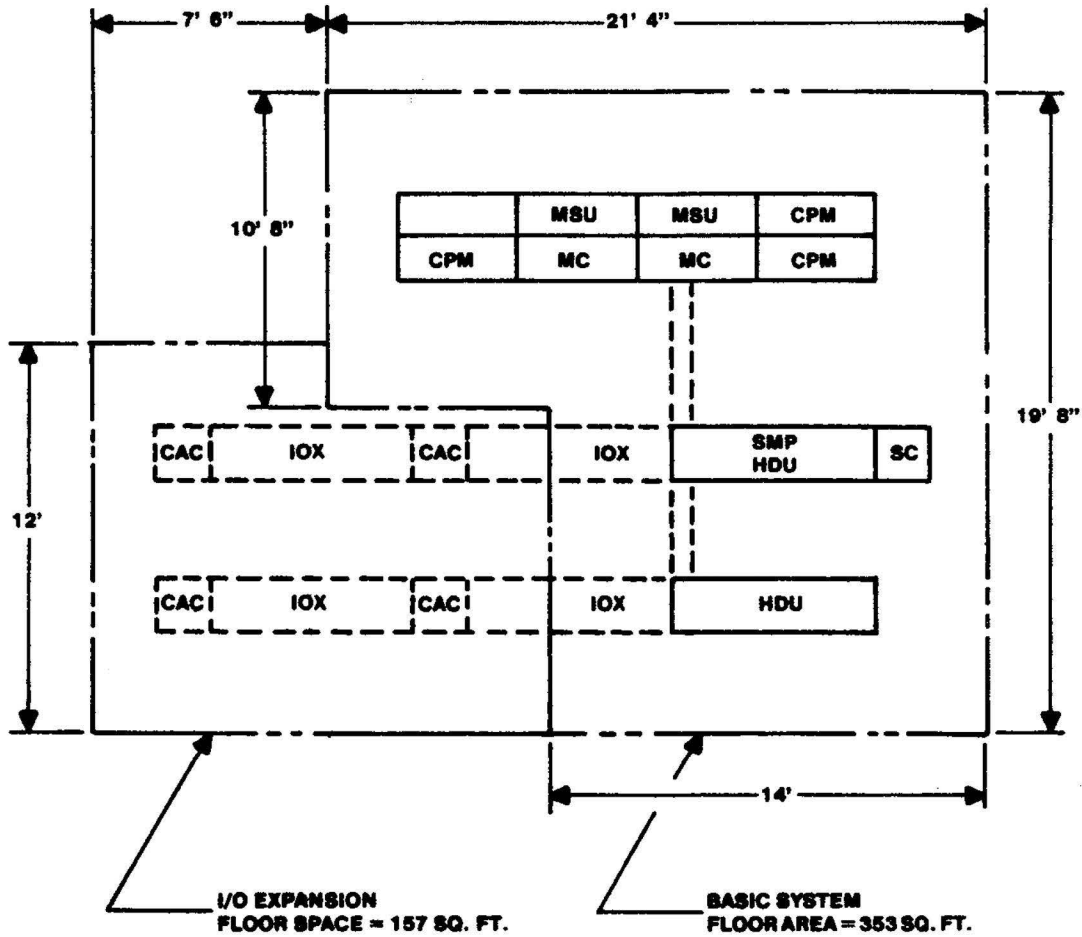
NOTE: System Maintenance Station (SMS) and two operator tables also included with each system.

E6578

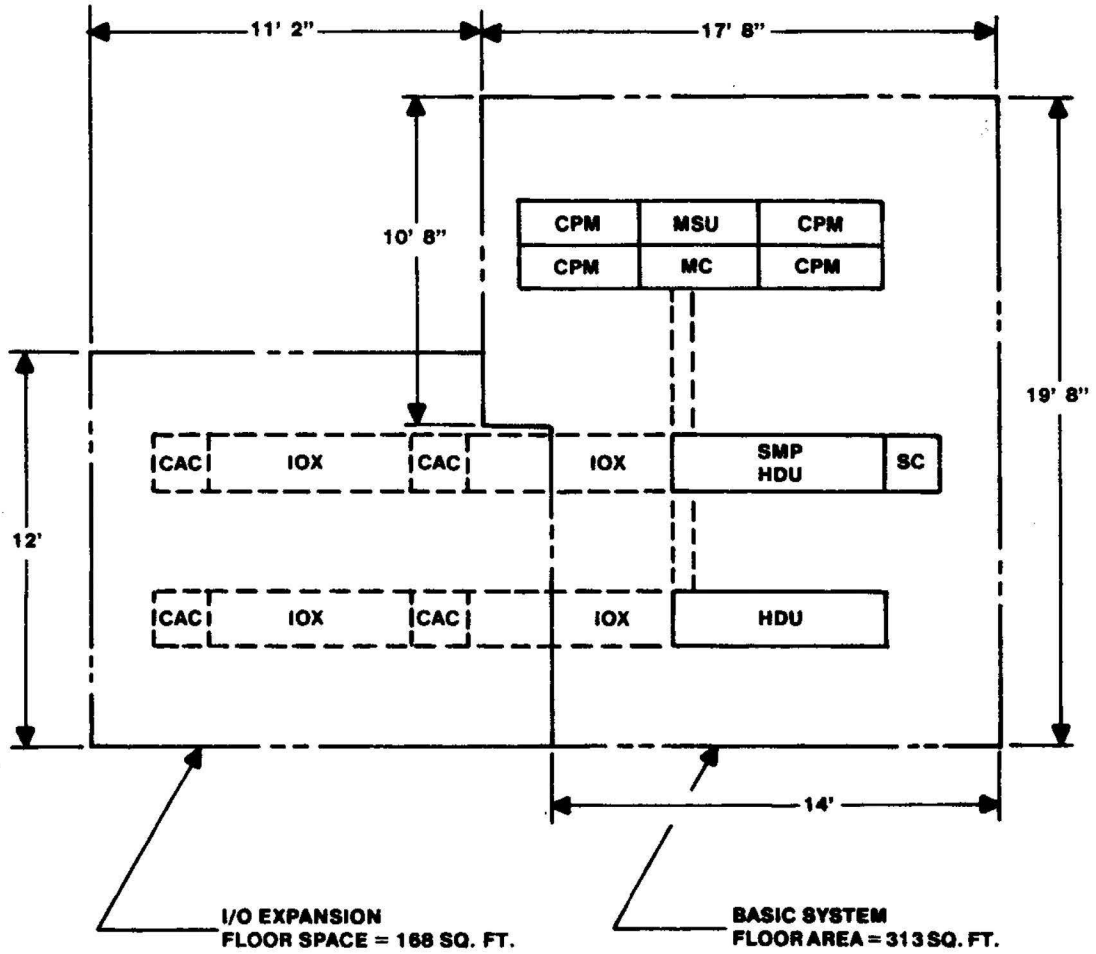
A 15-K



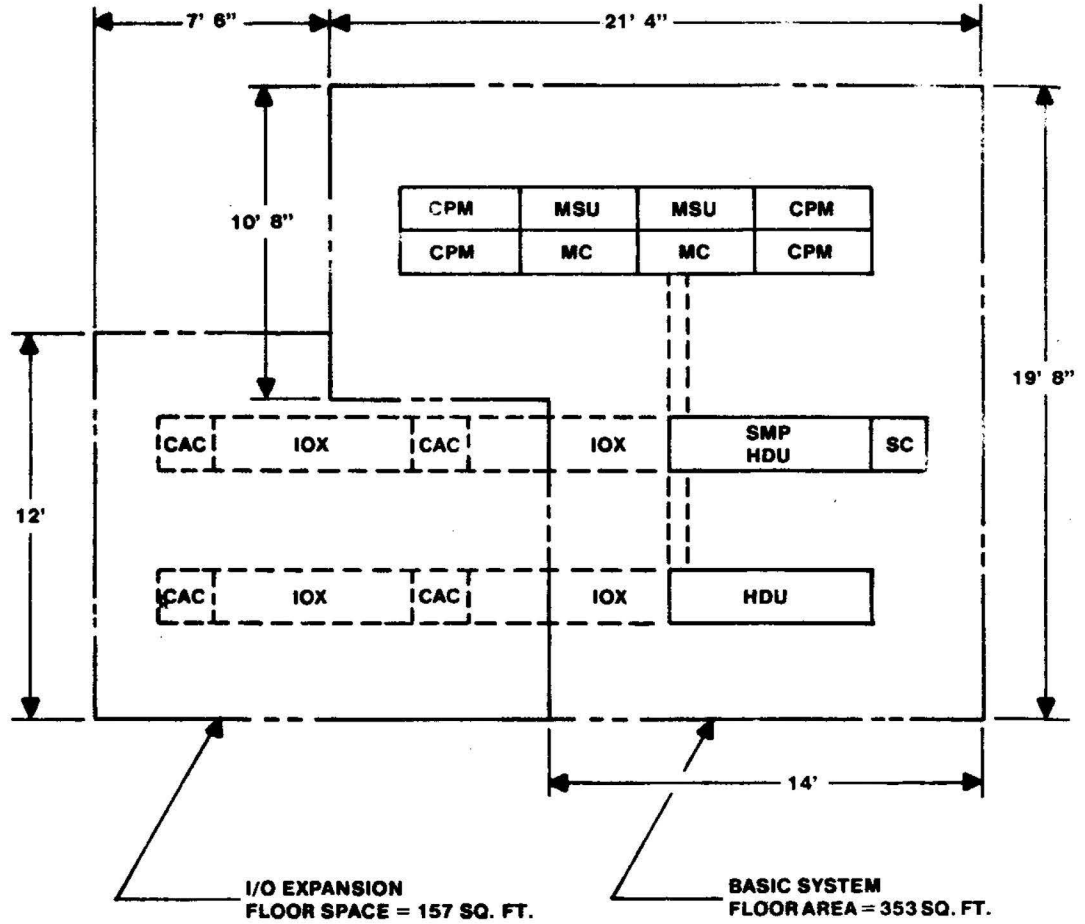
A 15-L



A 15-M



A 15-N

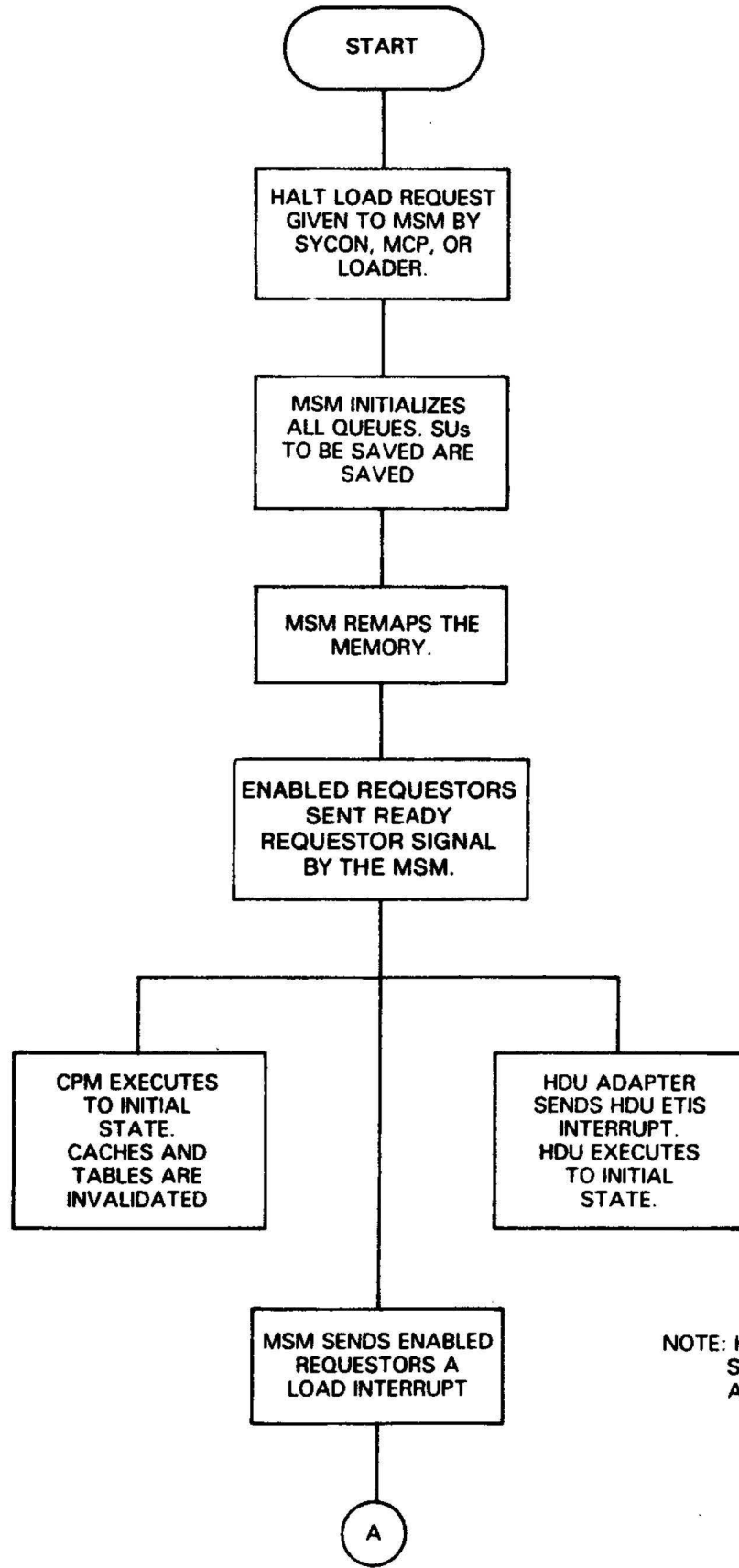


NOTE: System Maintenance Station (SMS) and two operator tables also included with each system.

E6581

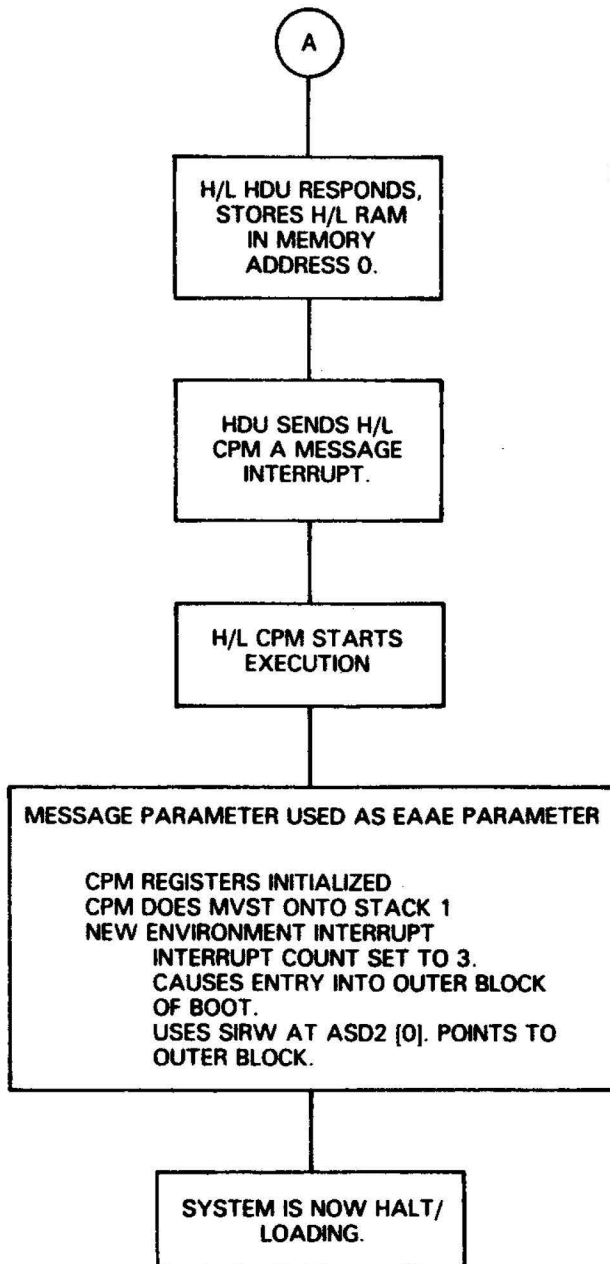
SECTION 6 A 12 SYSTEM MAINTENANCE

HALT/LOAD FLOW (SHEET 1)



NOTE: HOME ADDRESS QUEUE SET TO 0 NOT TO 16 AS ON OTHER SYSTEMS

HALT/LOAD FLOW (SHEET 2)



NOTE: THE A 12 SYSTEM IS AN ASD SYSTEM. IF ASN MICROCODE IS LOADED TO THE CPM AND IT RECEIVES A MESSAGE INTERRUPT, IT WILL SUPERHALT. THE HDU WITH ASN MICROCODE WILL FAULT.

E7432b

CPMC CABLES AND JUMPERS

J4	J3	J2	J1	
OPEN	OPEN	JUMPER	JUMPER	30
C FIOA J2	OPEN			29
C 17J4	C 17J3	C 18A,19A,HDU	C 20A,21A,HDU	28
OPEN	OPEN	C 12J1	C23J1,11J1,16J3	27
C 17J2	C 18J3	OPEN	OPEN	26
OPEN	OPEN	OPEN	C 7J4 MEM	25
C 7J4 MEM	C 7J3 MEM	C 7J2 MEM	C 7J1 MEM	24
C 10J4	C 4J3 JUMPER	JUMPER	C 27J1	23
OPEN			C 1J4	22
OPEN	JUMPER	JUMPER	JUMPER	21
JUMPER	OPEN	JUMPER	OPEN	20
OPEN	C 26J3	JUMPER	OPEN	19
C 28J4	C 28J3	C 26J4	JUMPER	18
OPEN	C 27J1	C 10J1	JUMPER	17
C 13J4 JUMPER C 13J4	C 13J3	JUMPER	JUMPER	16
	C12J3	JUMPER	JUMPER	15
C 15J4,14J4 JUMPER	C 15J3	JUMPER C 10J1	JUMPER	14
JUMPER	C 14J3	C 9J4	C 27J2	13
C 23J4	JUMPER	JUMPER	C 27J1	12
C 11J2	JUMPER	OPEN	C 12J2,16J2	11
OPEN	OPEN	OPEN	JUMPER	10
C CLOCK	JUMPER	JUMPER	JUMPER	09
JUMPER	JUMPER	JUMPER	JUMPER	08
JUMPER	C 1J1,23J3	JUMPER	OPEN	07
OPEN	JUMPER	JUMPER	JUMPER	06
C 22J1	OPEN	JUMPER	JUMPER	05
			JUMPER	04
			JUMPER	03
			JUMPER	02
			C 4J3	01

C CABLE; DESTINATION SHOWN

E7433

HDU CABLES AND JUMPERS

D	C	B	A	
C MIP	C CLOCK CARD	C CPMC 29J4	JUMPER	24
				23
			C RED & BLACK	22
			C CPMC 28J1	21
			C CPMC 28J1	20
			C CPMC 28J2	19
			C CPMC 28J2	18
				17
				16
				15
				14
				13
				12
				11
				10
JUMPER	JUMPER			09
		JUMPER	JUMPER	08
				07
	JUMPER			06
		C MLI 1	C MLI 0	05
				04
				03
				02
C CLOCK	C CLOCK	C CLOCK	C 24J3 FIOA	02
				01

C - CABLE; DESTINATION SHOWN

E7434

MSU CABLES

C 25J1,24J4	C 24J3 CPMC	C 24J2 CPMC	C 24J1 CPMC	07
SU 0				06
SU 1				05
SU 2				04
SU 3				03
				02
				01

C - CABLE; DESTINATION SHOWN

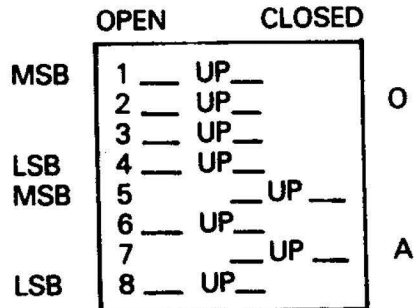
E7435

DIP SWITCHES

Power Net

CPMC

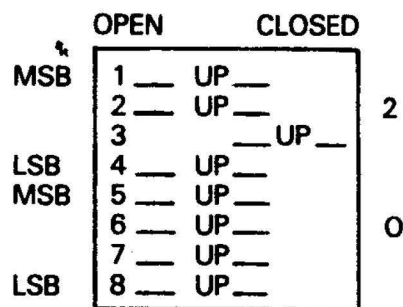
ADDRESS 0A



E7436

IIO

ADDRESS 20 - 2F



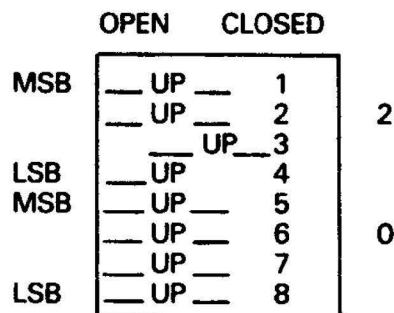
*LAST CABINET IN NET MUST HAVE TERMINATOR JUMPER ON JJ4. PINS 1 TO 3

E7437

Power Net Master

(IN MAINTENANCE STATION)

LOCATION C 132



E7438

DIP SWITCHES (CONT.)

LOCATION H518	OPEN	CLOSED	
MSB	___ UP ___	1	0
	___ UP ___	2	
	___ UP ___	3	
LSB	___ UP ___	4	0
MSB	___ UP ___	5	
	___ UP ___	6	
LSB	___ UP ___	7	
	___ UP ___	8	

*NOTE: TERMINATOR AT JJ5 WILL GO ON 1 PIN TO EITHER SIDE. BE SURE THAT IT IS CENTERED

E7439

MIP

	CLOSED	OPEN	
X	___ UP ___	8	9
X	___ UP ___	7	
X	___ UP ___	6	
MSB	___ UP ___	5	
	___ UP ___	4	
LSB	___ UP ___	3	
	___ UP ___	2	
X	___ UP ___	1	

*NOTE: TERMINATOR AT JJ5 WILL GO ON 1 PIN TO EITHER SIDE. BE SURE THAT IT IS CENTERED.

E7440

Maint Disk Control

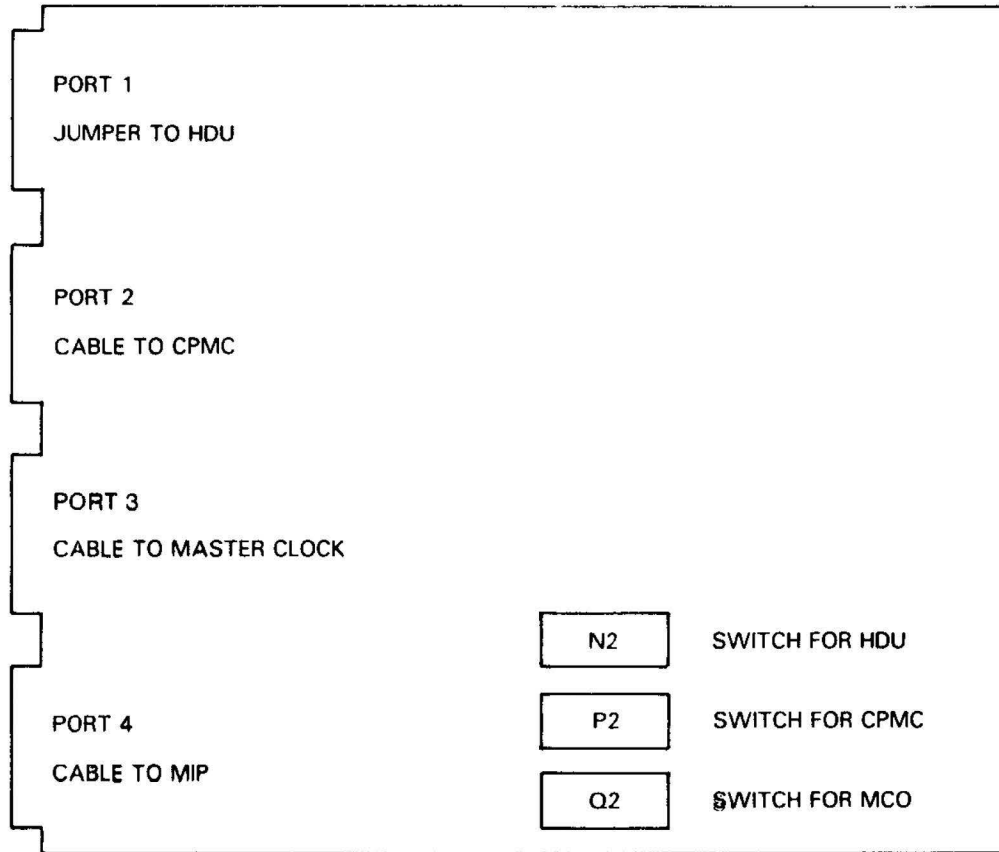
THE DCC SHOULD BE JUMPERED AS FOLLOWS

WO	0	1	2	3	4	5	6	7
							
							
W1	_____						
W2	_____						
W5							
W6							
W7							
W8	_____							
W4							
W3	_____							

1192432-001

DIP SWITCHES (CONT.)

FIOA CARD



SWITCH LAY OUT:
RED DOT UP OR
1 "ON"

ON	ON	ON	ON	ON	ON	ON	ON
1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

RED DOT DOWN OR
0 "OFF"

SWITCHES AT N2, P2 AND Q2

1	2	3	4	5	6	7	8	MODULE
OFF	OFF	OFF	ON	ON	OFF	ON	OFF	HDU
ON	OFF	ON	OFF	ON	ON	ON	OFF	CPMC
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	MCO

E7441

MAINTENANCE SOFTWARE

PART NUMBER	MEDIA	NAME	CONTENTS
3573-2254	FLOPPY	A12EXECNN	SHELL FILECON POWER NET SYCON MONITOR REMOTE SUPPORT TEST BUS
3573-2207	FLOPPY	A12MACCODENN	SYCON PROCS STATE ACCESS PROCS JIE TEXT
3573-2288	FLOPPY(3)	A12CPMCMCODE01 A12CPMCMCODE02 A12CPMCMCODE03	CPMC MICRO CODE
3573-2312	FLOPPY	A12UTILADERNN	SYSTEM TRBOOT SYSTEM UTILADER SYSTEM DEADSTOPS
35732292	FLOPPY	A12HDUASDMCODE	HDU MICRO CODE
35732262	STREAMER TAPE	A12MAINTNN	CPMC & HDU TEST: CPM CACHE CONF CPMC CONF CPM/MSU CONF CPMC MODULE DDRIVE CPMC RAM TEST CPMC STATE ACCESS PNLS. CPMC STATE DUMP HDU RECORDED TEST HDU QM MEM CONF HDU RECORDED CONF HDU STATE DUMP ECT.

NN - REVISION LEVEL; INITIALLY AA.

BOXTYPE FIELD ENCODING

BOXTYPE CHIP A8 0 = OFF, 1 = ON

SWITCH #	5	6	7	8	DESCRIPTION
	0	0	1	0	CPMC

MODEL NUMBER: CHIP A8

SWITCH #	1	2	3	4	DESCRIPTION
SETTING	0	0	1	0	CPMC

ERL FIELD ENCODING: CHIP A7

SWITCH #	3	4	5	6	7	8	DESCRIPTION
	0	0	0	0	0	0	ERL 0
	0	0	0	0	0	1	ERL 1
	0	0	0	0	1	0	ERL 2
	0	0	0	0	1	1	ERL 3

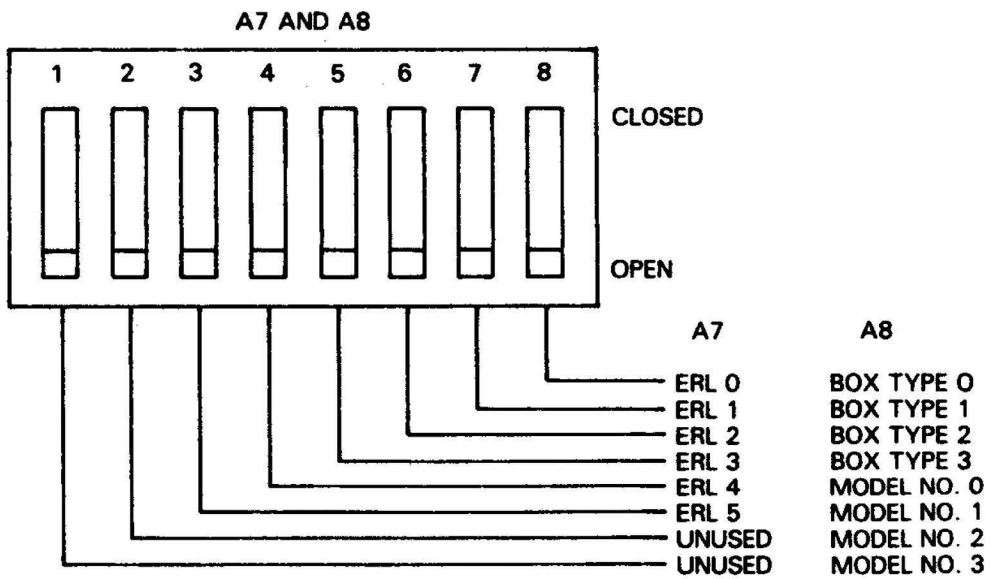
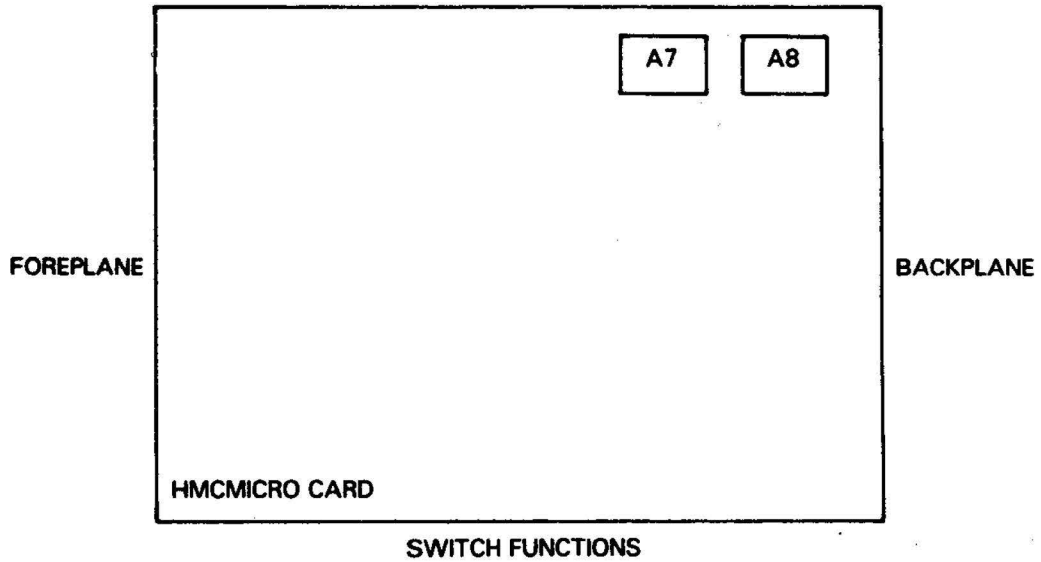
0	0	1	0	0	1	ERL 9
0	0	1	0	1	0	ERL 10
0	0	1	0	1	1	ERL 11

0	0	1	1	1	1	ERL 15
0	1	0	0	0	0	ERL 16

0	1	1	1	1	1	ERL 31
1	0	0	0	0	0	ERL 32

1	1	1	1	1	0	ERL 62
1	1	1	1	1	1	ERL 63

BOX ID SWITCH DEFINITIONS

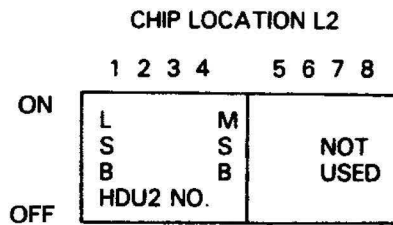


E7444

HDU ID SWITCHES

SWITCH FUNCTION	SWITCH CHIP LOCATION	SWITCH NUMBERS	ASSIGNMENTS
TYPE	LO	1 TO 4	HDU2 - 8
MOD	LO	5 TO 8	HDU2 - 1
CLS	JO	1 TO 3	DEFINED BY PROGRAMMING
ERL	JO DO	4 TO 8 1	DEFINED BY ENGINEERING
FRL	DO	2 TO 6	DEFINED BY PROGRAMMING

SET UP HDU2 NO. AT CHIP LOCATION L2 TO REFLECT ASSIGNED HDU2 ID NO.

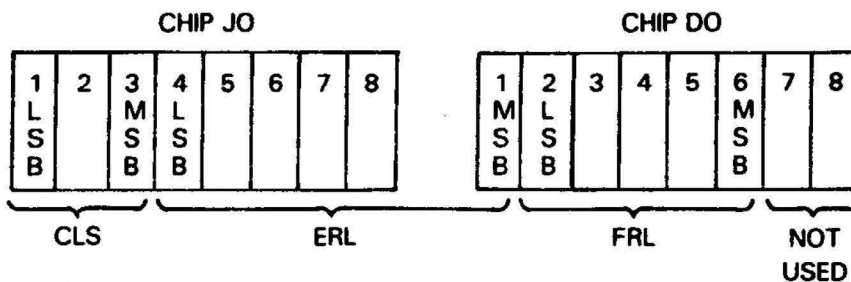
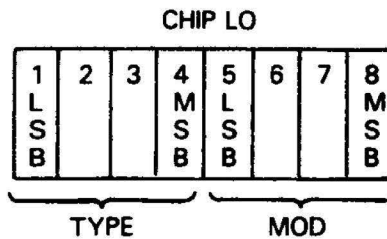


E7445

Switch Settings

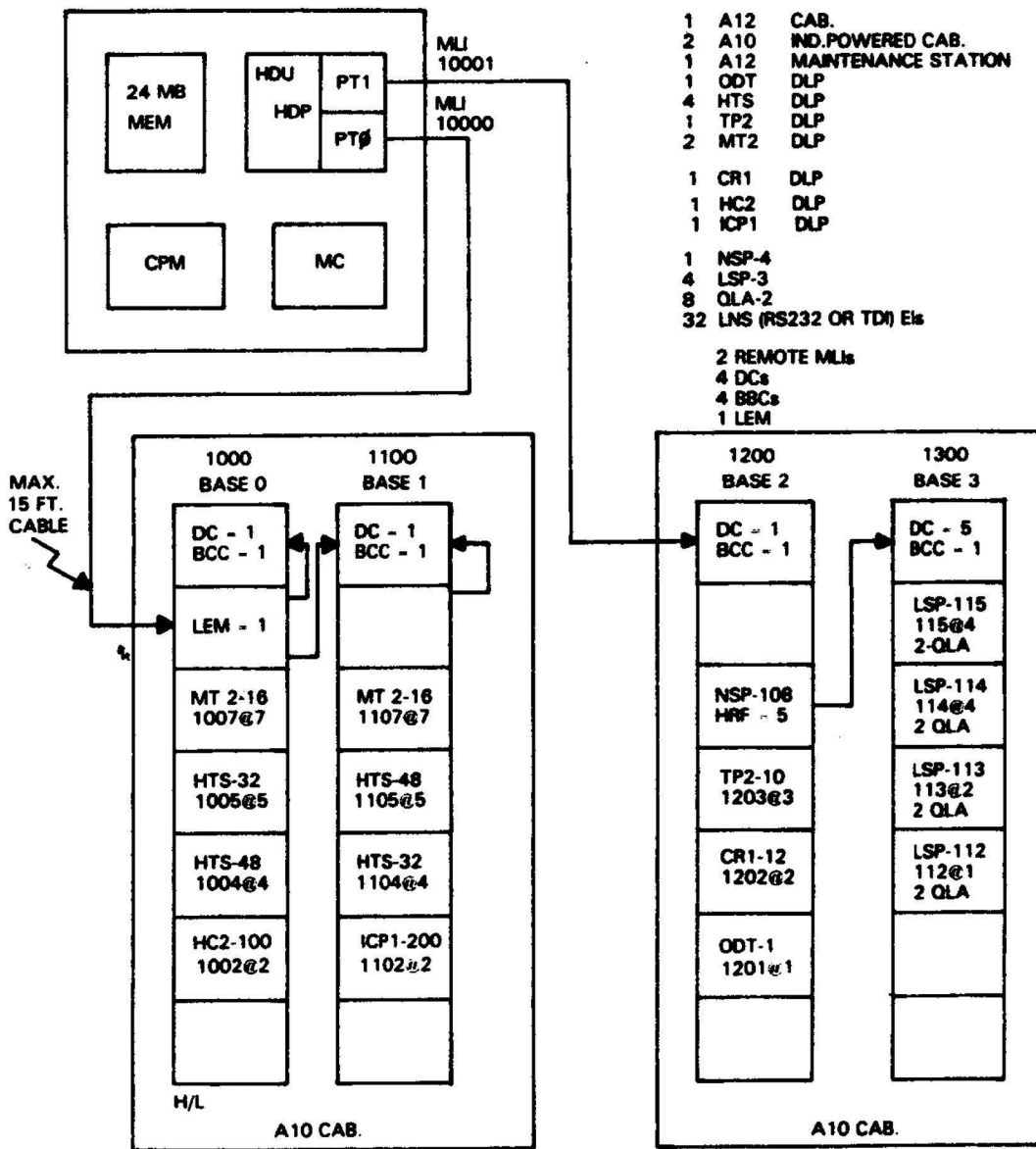
SWITCHES ARE ON CARD ATRMH SLOT # 22 OF HDU.

ON = 1, OFF = 0,



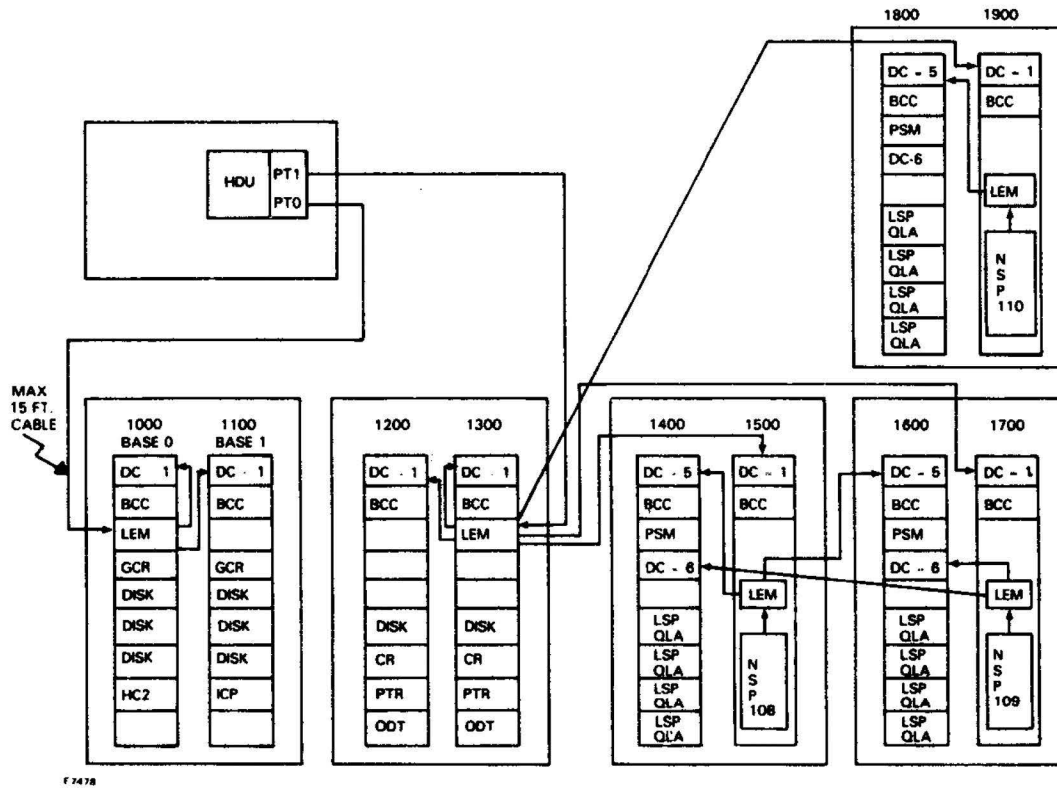
E7446

MINIMUM I/O CONFIGURATION

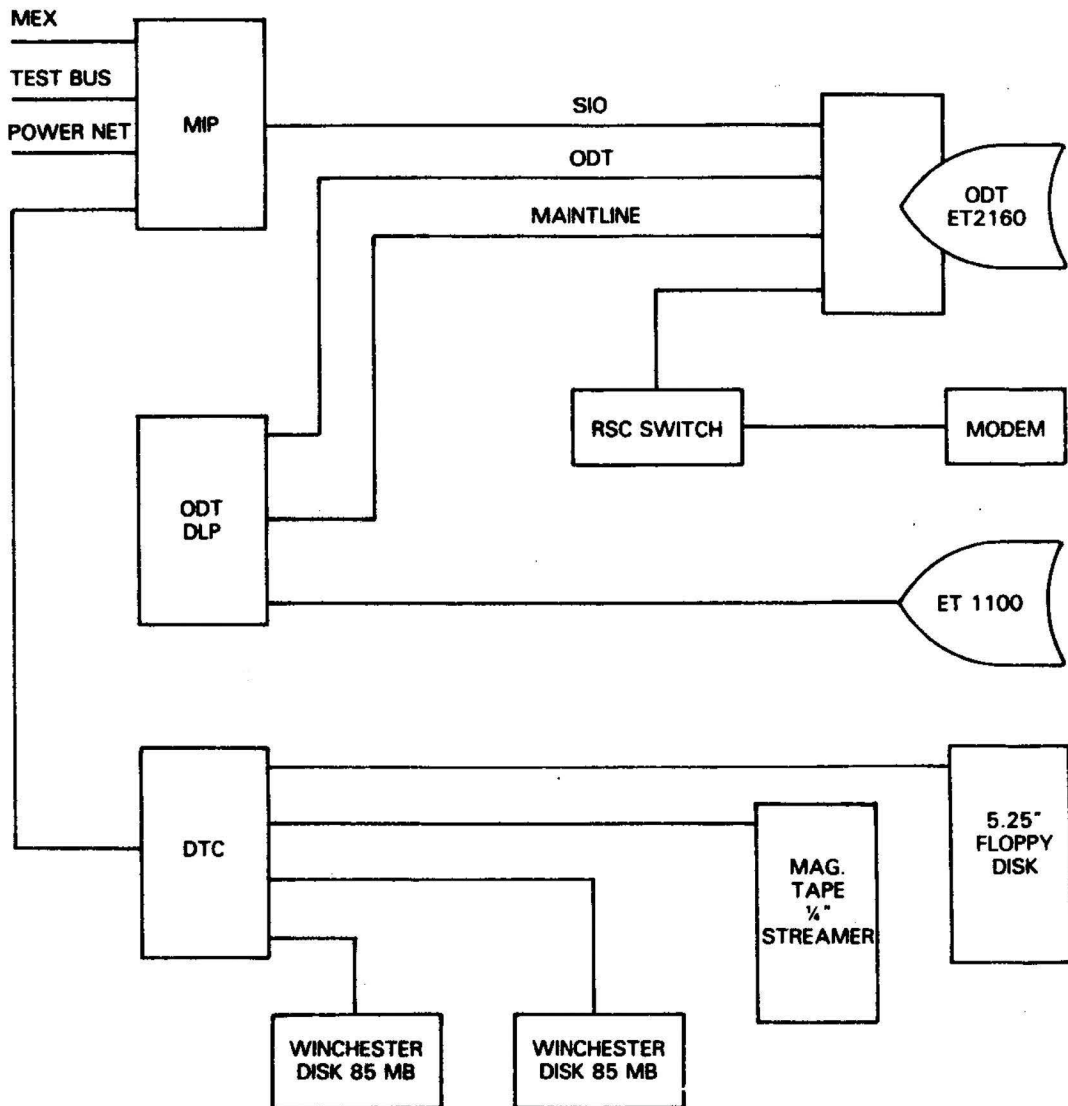


E7447

LARGE I/O CONFIGURATION



MAINTENANCE HARDWARE



E7449

MCP/AS SYSTEM SOFTWARE MAINTENANCE LINK

CONFIGURATION FILE SYNTAX

EXAMPLE:

```
DLP 2001      :TYPE = ODT1;  
              ID      = 1;  
              OUTBOARD = (1 @ 0  
                          ,2 (MAINLINE) @ 1  
                          );
```

**MAINLINEIR Will Grab The Highest Numbered Ready ODT With
'MAINLINE' Qualifier**

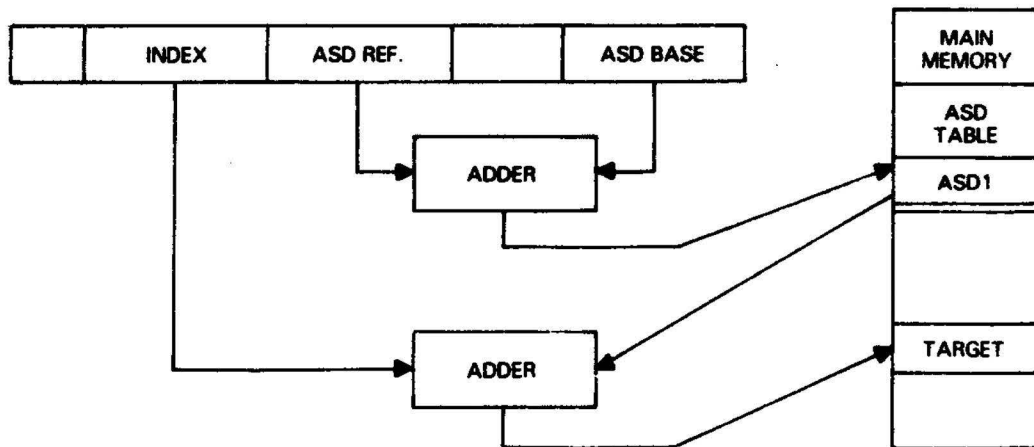
**Cannot Save A MAINLINE 'ODT', But Can UR/UR-

**If Maintline Is Accidentally Cabled To Regular ODT It Can Be Used As
Operator Terminator -- But Proper Linkage Is Important For
Normal System Maintenance**

ASD DESCRIPTORS - MCP/AS

	51	47	43	39	35	31	27	23	19	15	11	7	3
T	CONTROL			LENGTH				A S D					
	50	46	42	38	34	30	26	22	18	14	10	6	2
A													
	49	45	41	37	33	29	25	21	17	13	9	5	1
G													
	48	44	40	36	32	28	24	20	16	12	8	4	0

ASD # IS A REFERENCE THAT IS ADDED TO THE ASD TABLE BASE. THIS POINTS TO THE ASD1 WORD THAT WILL BE INDEXED BY THE LENGTH FIELD.



E7450

CPM BOX ID INFORMATION

51	47	43	39	35	31	27	23	19	15	11	7	3
50	46	42	38	34	30	26	22	18	14	10	6	2
49	45	41	37	33	29	25	21	17	13	9	5	1
48	44	40	36	32	28	24	20	16	12	8	4	0

FIELD	BITS	DESCRIPTION
MODEL	[7:4]	- 1
CLASS	[10:3]	- ACCESS TYPE
MBM	[31:2]	- MAINTENANCE BUS MODE SWITCH
H/L	[35:1]	- HALT/LOAD
E	[36:1]	- MAINTENANCE BUS ENABLE
FF	[45:1]	- FAN FAULT
TF	[46:1]	- TEMPERATURE FAULT
PF	[47:1]	- POWER FAULT (REGULATOR)

E7451

MSM STATUS REGISTER

51	47	43	39	35	31	27	23	19	15	11	7	3							
50	46	42	38	34	30	26	22	18	14	10	6	2							
49	45	41	37	33	29	25	21	17	13	9	5	1							
48	44	40	36	32	28	24	20	16	12	8	4	0							
				SIMS				HLR				ERL				MOD. TYPE			

FIELD	BITS	DESCRIPTION
TYPE	[3:4]	BOX TYPE (MSM II TYPE = 7)
MOD	[7:4]	MODEL NUMBER 2 - 4 MILLION WORDS/SU
SME	[8:1]	SCRUB MEMORY ENABLE
MBE	[9:1]	MAINTENANCE BUS ENABLE
	[10:1]	ALWAYS 0
ERL	[16:6]	ERL
HRL	[22:6]	HALT/LOAD REASON
TODV	[25:1]	TIME-OF-DAY VALID
ID	[26:1]	MSM ID (0 OR 1)
RES	[29:02]	RESERVED FOR MAINTENANCE SYSTEM USE
MBM	[31:2]	MAINTENANCE BUS MODE
SIMS	[35:4]	SIM STATUS MASK

E7452

SYSTEM LOG

1.0 CPM ERROR REPORTING
NOTIFY CSC OF ANY CPM ERRORS
APPROPRIATE ACTIONS WILL BE DISCUSSED

2.0 MSM ERROR REPORTING

2.1 RIMIN ERRORS :
2.2 HDUADPTR ERRORS : --- REFER TO A12TESTGUIDE
2.3 SCHEDULER ERRORS :
2.4 MCSIM ERRORS

ECC ERROR CODE DECODE

0 NO ERROR
1 NO ERROR
2 INVALID
3 INVALID
4 SINGLE DATA BIT CORRECTED ON READ (0-51)
5 SINGLE ECC BIT CORRECTED ON READ (52-59)
6 ADDRESS ERROR ON READ
7 MULTIPLE BIT ERROR ON READ

IF ECC ERROR CODE - 4 OR 5 CHECK ADDR 24:3 THIS IS THE SU NUMBER ALL 60 BITS ARE ON 1 CARD THEREFORE CHIP AND BIT VALUE CAN BE DISREGARDED IF SU REPLACEMENT DOES NOT FIX PROBLEM, CHANGE CABLES FROM SIM TO FEEDTHRU.

IF ECC CODE - 6 CHIP AND BIT REFERENCE WHICH ADDRESS BIT FAILED. FIX THIS PROBLEM BY FIRST REPLACING THE FOREPLANE CABLES, THEN THE SIM BOARD.

IF ECC CODE - 7 CHECK ADDR 24:3 FOR WHICH SU FAILED. REPLACE FOREPLANE CABLES, THEN SU, AND FINALLY SIM.

3.C HDU ERROR REPORTING

3.1 HDU ERROR TRACES
3.2 NOTIFY CSC WITH INFORMATION FROM LOG

B9494-12 ERRORS
TAKE A LOG OF PACK BY : LOG MAINT PK XX DUMPEX

OPERATOR DEPENDENT INTERRUPTS (LEVEL BETA)

Interrupt Class = 1 (26:3) - ODI

Subtype (15:4)

Interrupt Type (11:12)

ODE Halt	Hex	Dec	Interrupt
P	0	0	Presence Bit
N	1	1	<unused>
P	2	2	Stack Overflow
N	3	3	Invalid Operator
N	4	4	Undefined Operator
Y	5	5	Invalid Stack Argument
Y	6	6	Invalid Argument Value
Y	7	7	Invalid Code Parameter
Y	8	8	Invalid Reference
Y	9	9	Invalid Reference Chain [12:1] = 1: operator was ENTR
P	A	10	Invalid Index
Y	B	11	Memory Protect
P	C	12	Divide By Zero
P	D	13	Exponent Underflow
P	E	14	Exponent Overflow
P	F	15	Integer Overflow
Y	10	16	Stack Overflow
N	11	17	<unused>
Y	12	18	Stack Structure Error
Y	13	19	Code Segment Error
Y	14	20	Invalid Program Word
N	15	21	<unused>
Y	16	22	Invalid Object
Y	17	23	Page Structure Error
P	18	24	Block Exit
N	19	25	Binding Request [12:1] = 1: Operator was ENTR
N	1A	26	Precision Loss
N	1B	27	False Assertion
N	1C	28	Locking
N	1D	29	Unlocking
N	1E	30	undefined
N	1F	31	Activate Object [15:4] = 1: object is Interlock
P	20	32	Touch [12:1] = 1: touch was by load or on final target of NXLN
N	21	33	Sequence Boundary [12:1] = 1: P2 references the page being written, and: [14:1] Length Location: 0 F-1; 1 F-2 [13:1] Length count units: 0 characters; 1 words ([14:2] is valid only if [12:1] = 1)
Y	22	34	Invalid ASD Reference
Y	23	35	ASD Structure Error
N	24	36	New Environment

ALARM INTERRUPTS (LEVEL BETA)

INTERRUPT CLASS - 2 (26:3) - ALARM

[15:10] RESERVED

INTERRUPT TYPE (5:6)

[5:1]	1 =LINK ERROR ON A-SERIES MLIP SYSTEMS
[4:1]	1 =INVALID ADDRESS
[3:1]	1 =UNCORRECTABLE MEMORY ERROR
[1:1]	1 =HARDWARE ERROR
[0:1]	1 =LOOP TIMER

EXTERNAL INTERRUPTS (LEVEL BETA)

INTERRUPT CLASS - 4 (26:3) - EXTERNAL

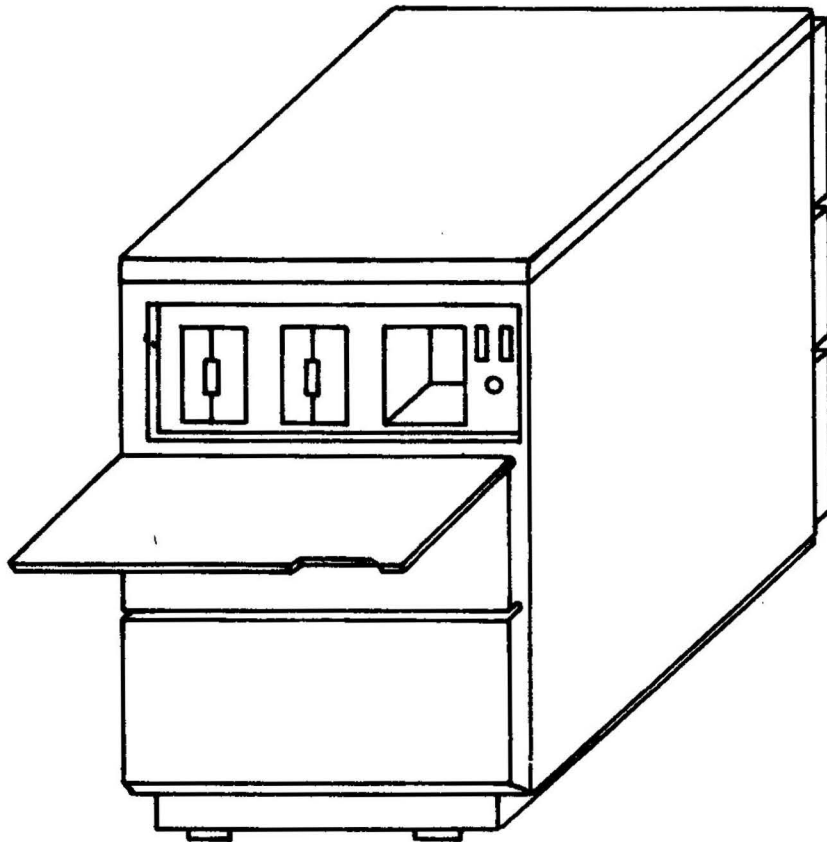
[15:11] RESERVED

INTERRUPT TYPE (4:5)

[4:1]	1 =RUNNING TIMEOUT
[3:1]	1 =UNMASKED ATTENTION
[2:1]	1 =I/O FINISHED
[1:1]	1 =ATTENTION
[0:1]	1 =INTERVAL TIMER

SECTION 7
A 15 SYSTEM MAINTENANCE

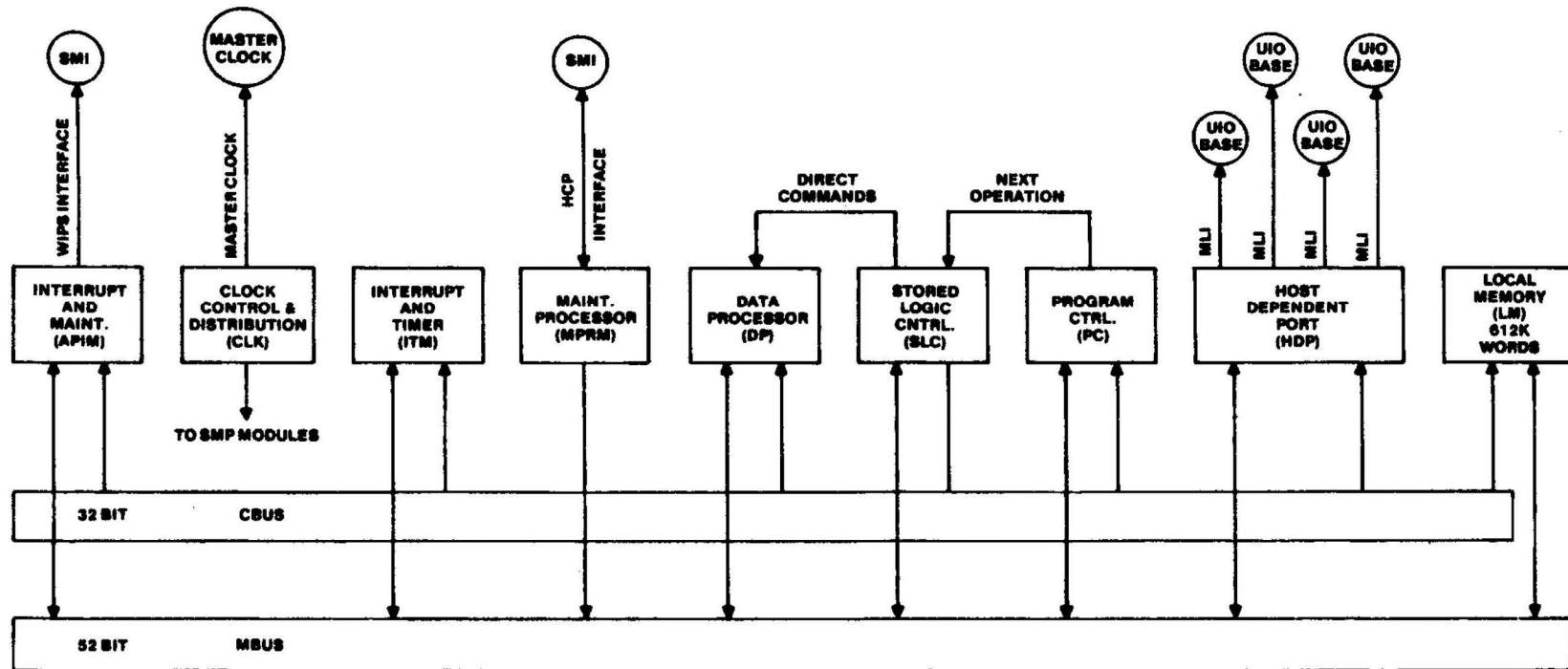
SYSTEM MAINTENANCE STATION (SMS)



FLOOR AREA	-	9 SQ. FT.
AIR FLOW	-	150 CPM
HEAT DISSIPATION	-	1350 BTU/HR
POWER	-	20A/2ϕ

E5829

SYSTEM MAINTENANCE PROCESSOR (SMP)



E5830

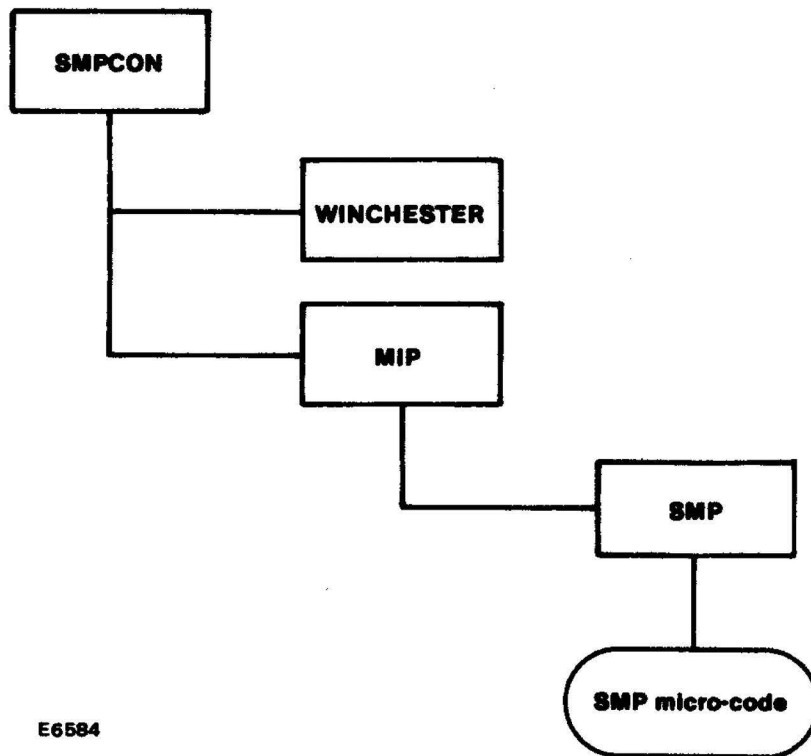
FEATURES OF SMP VS. AMP

- * Streaming Operators:
 - AMP: 1) connect
 - 2) transfer data
 - 3) disconnect

 - SMP: 1) connect
 - 2) transfer up to 10 commands
max of 256 bytes.
 - 3) disconnect
- * Special Code:
 - Perform Maintenance
 - Monitor the system

 - * Use FILECON to load Winchester
from Floppy.

 - * Call SMPCON to execute:
 - execute Power Up
 - execute Boot Loader
 - execute UTILoader for Halt/Load

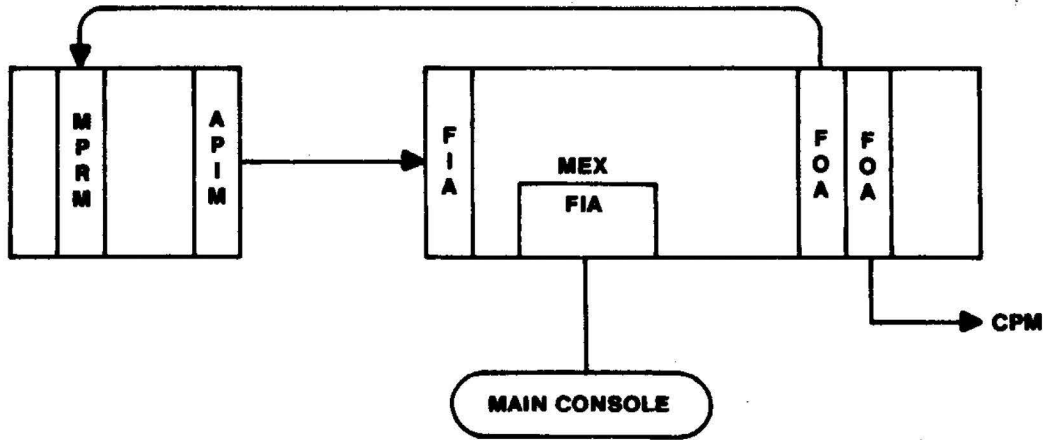


E6584

SHELL FEATURES

- * Initiated by MTSII BY ET 2150.
- * Menu driven screen.
- * Dynamic test:
 - SMPCONF
 - LMCONF
 - APIM tests

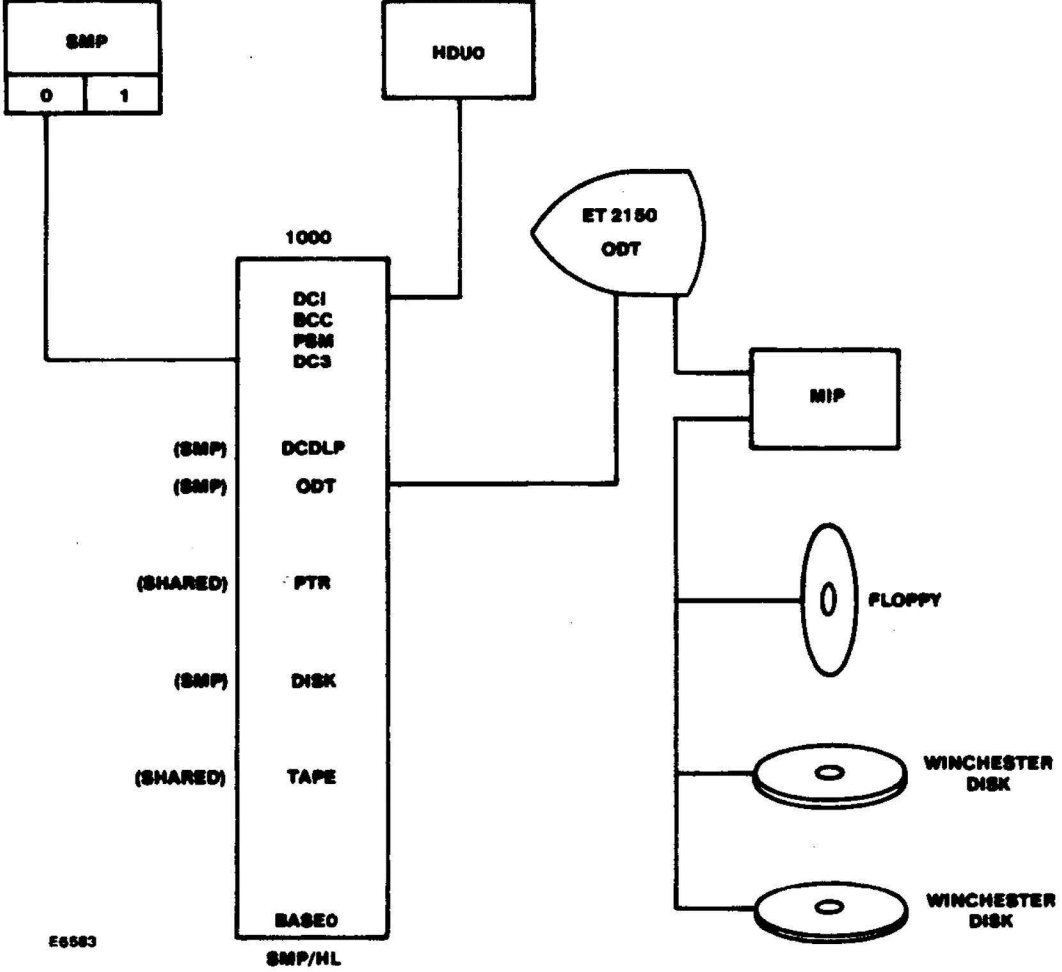
MAINTENANCE EXCHANGE INTERFACE



- MPRM - MAIN PROC. READ MODULE
- APIM - INTERRUPT AND MAINT. MODULE
- FIA - FAN IN ADAPTOR
- FOA - FAN OUT ADAPTOR
- MEX - MAINTENANCE EXCHANGE

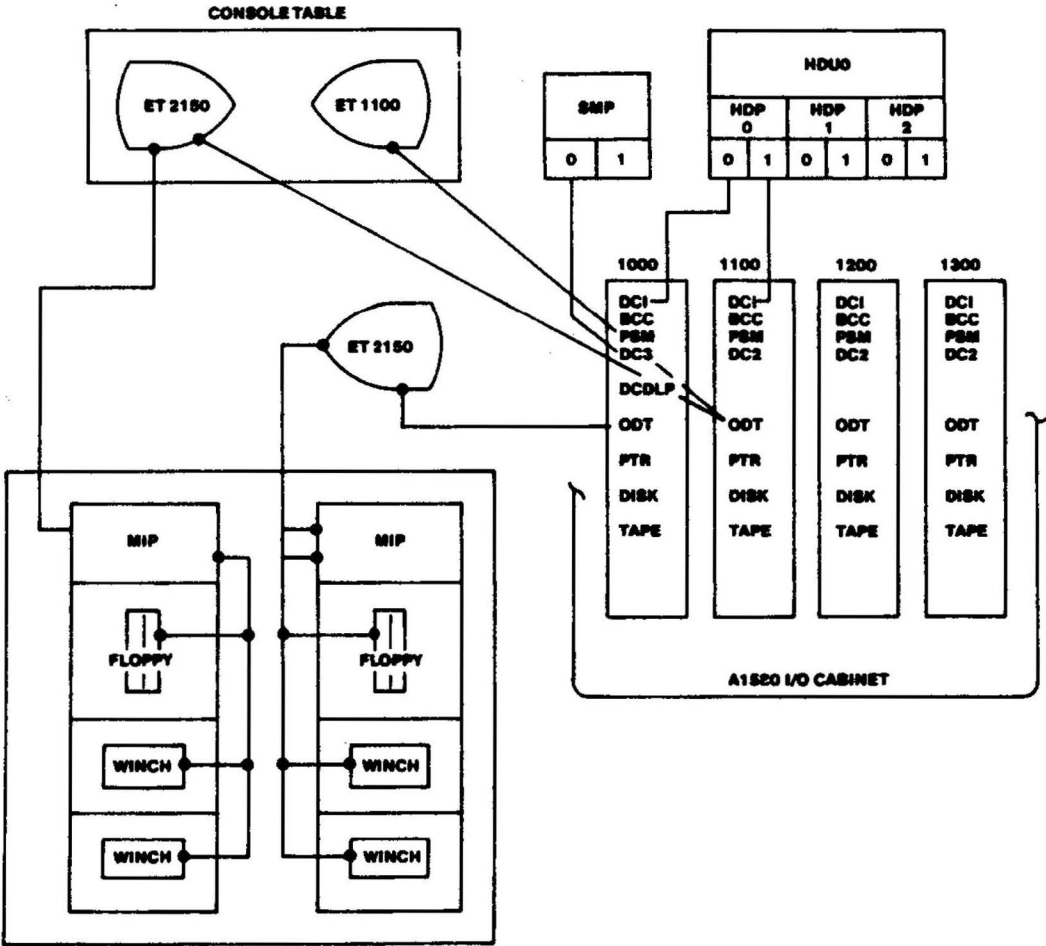
E5831

MAINTENANCE HARDWARE



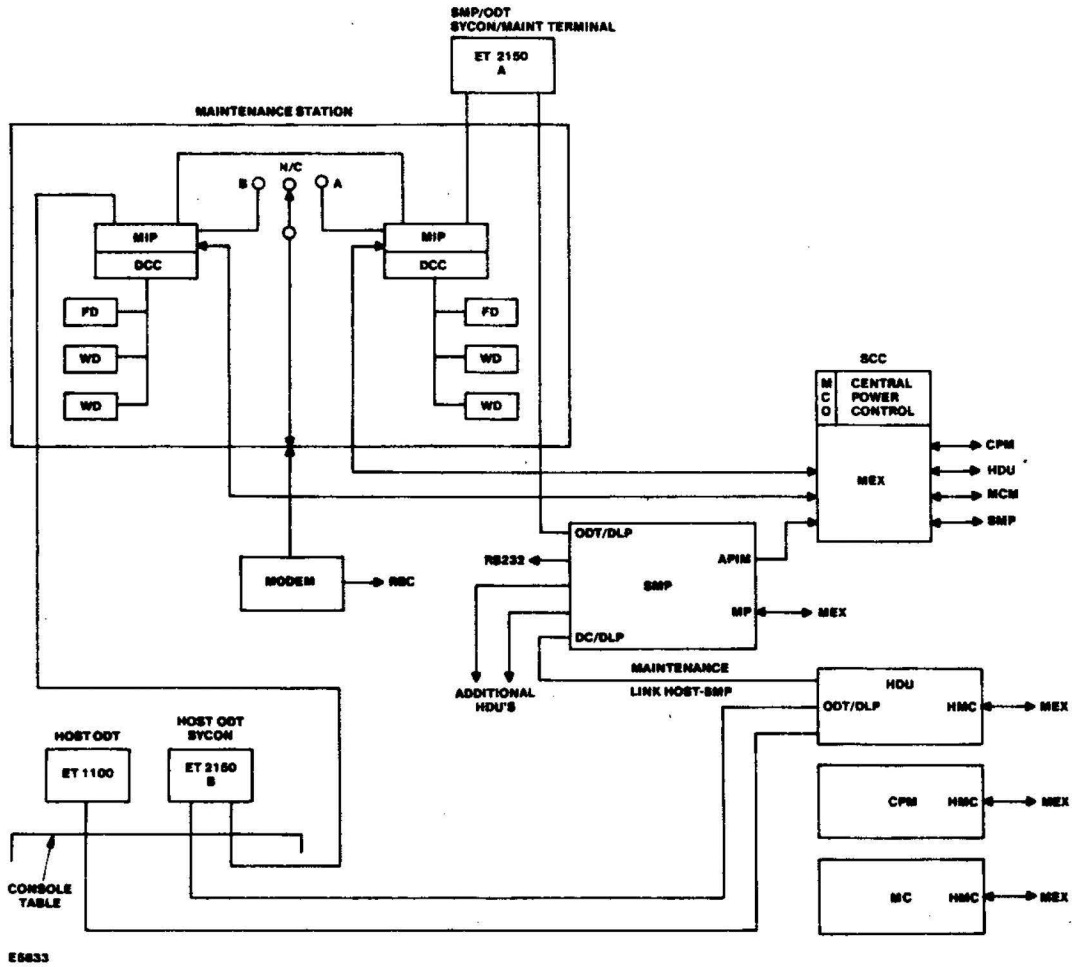
E6683

HALT/LOAD HARDWARE



E5832

MAINTENANCE SYSTEM CONFIGURATION



OPERATOR CONSOLE

MAINTENANCE STATION

- Dual Configuration
- MIP/DCC (A 9 components)
- Floppy Drive for console updates
- Winchester disks
- ET 2150 intelligent system
- RS232 interface for remote support (phase II)
- BDI interface for U10 testbus
- switchable remote interface

CONSOLE TABLE

ET 2150

- ODT
- maintenance/system console

RS232 INTERFACE

- line switchable to MIP A/MIP B/N.C.
- ring line disable
- software controlled access

SMP FEATURES

SMP is B 7900 amp (modified B 5900)

Maintains A 15 mainframe units

Maintained by system console

Independent System

- necessary to diagnose (maintain A 15)

- not required to halt/load, run A 15

shares base 0 with HDU

shares tape, printer with host A 15 only when needed

dedicated disk drives (2), ODT, datacomm

SMP - A 15 communications link via SMP datacomm to A 15 ODT

SMP MAINTENANCE SOFTWARE

Maintenance Executive

- Drive Tests**
- RAM Tests**
- Confidence Tests (CPM, HDU, MSM)**
- HDU Tests**
- State Dumps**
- State Formatter**
- CPM Monitor Control**
- IDA**

SMP - A 15 file transfer via ODT/MCS

Logging of MSM errors

SYSTEM MAINTENANCE SOFTWARE

- SMP**
- All functions are menu driven.
 - **D DRIVE TESTS** - Tests algorithmically generated from the logic design database with coverage 90%+
 - CPM
 - MCM
 - Static Tests
 - **RAM TESTS** - Pattern Tests designed to detect addressing and bit failure within RAMs.
 - CPM
 - MCM
 - Static Tests
 - **INTERACTIVE DIAGNOSTIC ACCESS (IDA)** - An interactive Maintenance tool used to read/write pulse-selected state.
 - CPM
 - MCM
 - HDU
 - **OFF-LINE CONFIDENCE** - CPM V Cache Confidence
 - MSM II Memory Confidence
 - Dynamic Test
 - **ON-LINE CONFIDENCE** - Confidence Routines run in a demi-partition - Dynamic Tests
 - **PANEL DUMP** - Used to dump all or selected state from the CPM, MSM, and HDU.
 - **PANEL FORMATTER/ANALYZER** - Used to print the dump and perform some analysis comparisons.
 - **BOARD ISOLATION PROBE** - Used in Conjunction with DRIVE to isolate failure to a board.
- HMC**
- Self Test
- MONITOR BOARD**
- Dynamic testing of single or multiple CPMs.
- HDU AND SMP TESTS**
- Same as B 7900.

E6587

SMP DESCRIPTION

- * SMP is AMP minus eight cache memory cards.
- * MSM-0 must be resident.
- * Floppy Micro-code; same as B 7900; located on Winchester disk.
- * SMP base - share with A 15 H/L proc.

*

SHELL:

- uses SMPCON box id
- menu includes:
 - hardware
 - software
 - operations
 - maintenance processor
- Two modes of data interface:
 - S.L.C. - Stored Logic Mode
 - for dynamic testing
 - run at full clock
 - Two Phases
 - 1) load
 - 2) run

Single Pulse Testing:

- Basic DP
- Basic LM
- Basic HDP

BOX IDENTIFICATION

Each box has ID register, accessible over the maintenance BUS whether or not BUS is disabled.

Box ID:

partition ID

halted indicator (requestors)

BUS enabled indicator

Partition ID and MEX used by software to identify state of box:

not physically present

powered off

uninitialized (is powered up)

reserved for maintenance

inhibited by SYCON

inhibited by MCP

available for inclusion in a partition

in partition

halted/not running/running

BOX STATE TRANSITIONS

TO FROM	POWER OFF	UNIN- ITIAL	MAINT	SYCON INHIB	MCP INHIB	AVAIL	PARTITION		
							H	NR	R
POWERED OFF	-	B							
Uninitialized	A	D*	C	D/E		F			
Maintenance	A		-	E					
SYCON Inhibited	A	D*	C	D		F			
MCP Inhibited	A		C	E	-				
Available	A			E		-	G		M
Partition 1/2/3/4									
Halted	A			E		H			I
Not Running	A			E				J	
Running	A				N	L	J	O	

- | | |
|--------------------------------|---|
| A. Physical Loss of Power | I. SYCON Load, Boot Load,
Force Dump, Continue |
| B. Physical Detection of Power | J. SYCON Halt & Diag. Halt |
| C. SYCON Panel Maintenance | L. MCP Free |
| D. SYCON Initialize | M. MCP Acquire |
| E. SYCON Inhibit | N. MCP Inhibit |
| F. SYCON Available | O. Running Light Goes Out |
| G. SYCON Acquire | |
| H. SYCON Free | |

* Indicates requested action failed.

CONSOLE TASKS AND SOFTWARE

ET 2000 MCP AND firmware

SHELL

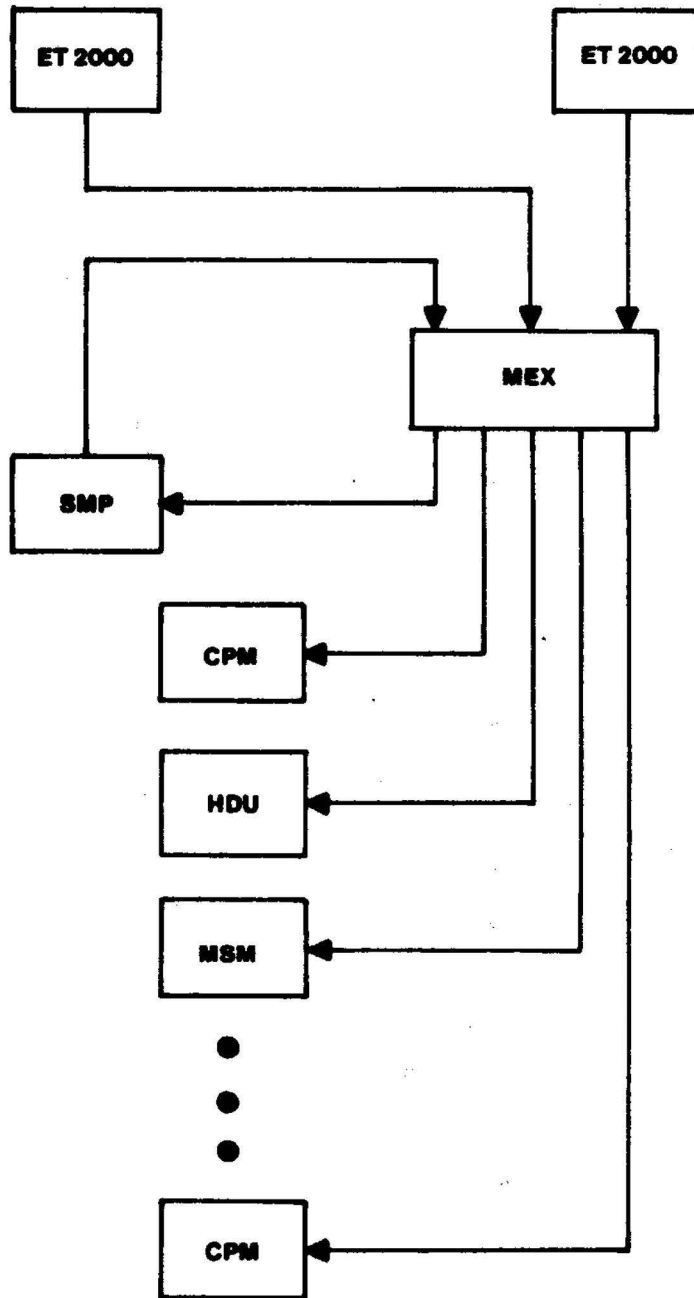
For A 15 system

partition configuration, system startup	SYCON
monitor	SHELL
ODT/terminal	SHELL

For SMP

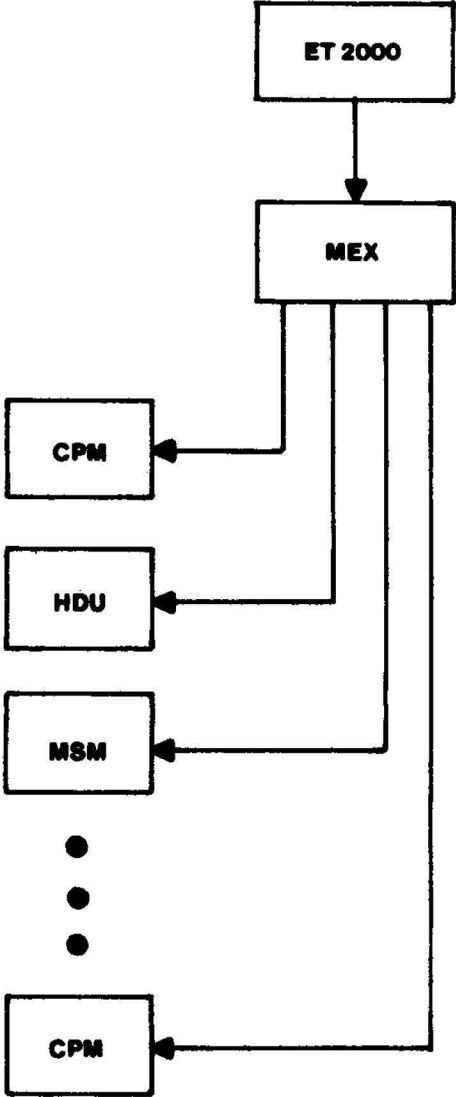
SMP startup	SMPCON
SMP maintenance	SMPCON/BEAM
SMP ODT/terminal	SHELL
low-level DLP diagnostics	TESTBUS
host - console file transfer	FILECON
remote support (phase 2)	

GENERAL MAINTENANCE BUS CONNECTIVITY



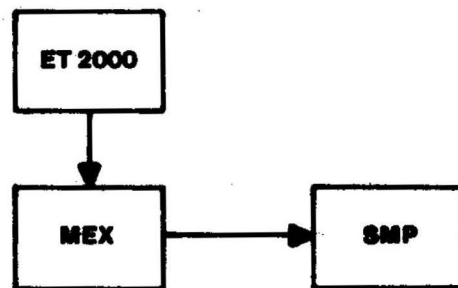
E5834

TYPICAL SYCON, MONITOR BUS CONNECTIVITY



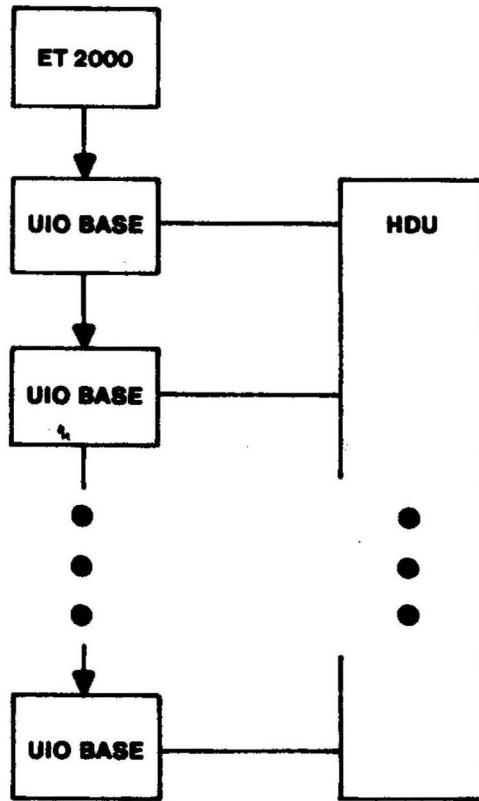
E5835

TYPICAL SMPCON, SMP MAINTENANCE BUS CONNECTIVITY



E5836

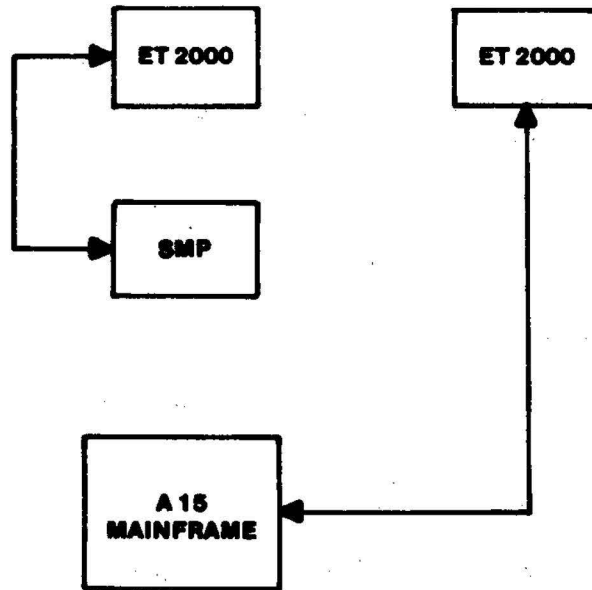
DLP DIAGNOSTICS (TESTBUS)



E5837

ODT CONNECTIONS VIA ODT DLPs

ODT Emulation, Host - Console File Transfer



E5838

CONSOLE HARDWARE

ET 2000

512KB RAM

Standard two Flemington PROMs (Confidence tests)

Additional four Tredyffrin PROMs (loader)

MIP

As on A 9 system (ICMD replaced with SASI disk interface)

Disk

DCC as on A 9 system

two hard disks

one double-sided double density floppy

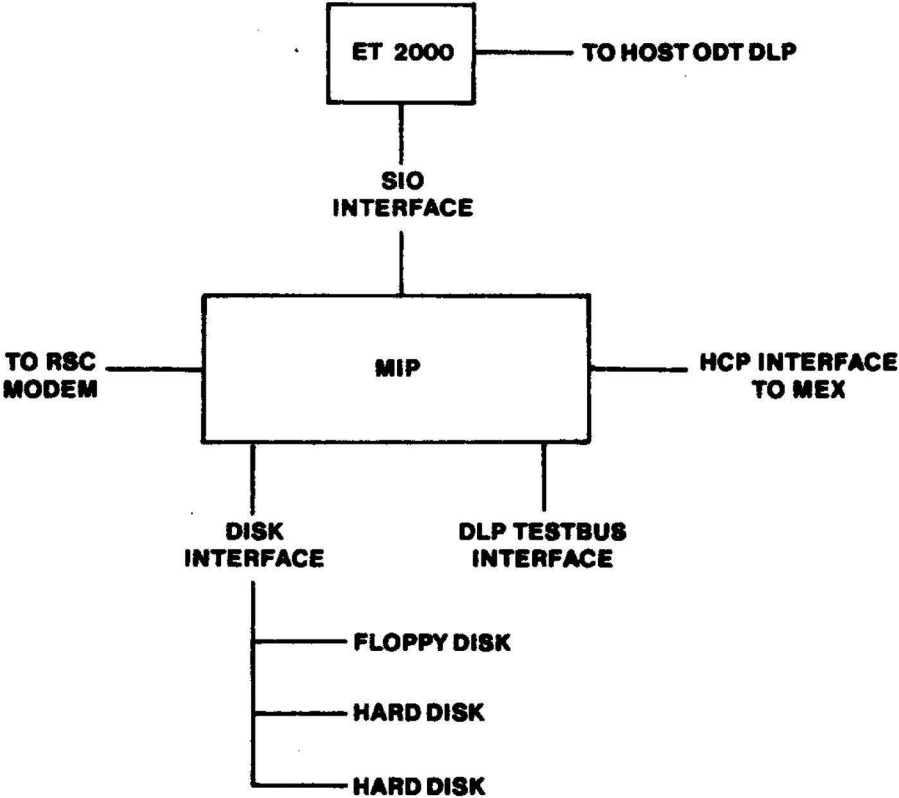
Two MIP/Disk subsystems housed in maintenance cabinet

ET 2000 on maintenance cabinet cabled as ODT to SMP

ET 2000 on table cabled as ODT to A 15

software is mostly TSL2

MAINTENANCE INTERFACE PROCESSOR (MIP)



E5839

SHELL

"MCP" and firmware for ET 2000

File directory

SHELL modules

monitor

always running, even if an executive or ODT

monitors A 15 status for change from running to not running

used special display line on ET 2000 screen for change message

keyboard command to switch to monitor menu

MCP deadstop analysis on monitor menu

uses file on hard disk to give description of deadstop

ODT

provides ODT emulation to either SMP or A 15 terminal, via ODT MCS (MCP 3.5)

RSC connection

Load and Initiate Executives

Shell modules may be involved directly, or from within an executive (at end of module, return to executive).

POWER UP CONSOLE

Power up ET 2000 with standard ET 2000 switch

Power up MIP/disk with switch on front of maintenance cabinet

Software Console Power Up Sequence:

ET 2000 confidence test

MIP test

auto load SHELL/SVM2 from hard disk

SHELL checks connectivity:

If direct connect to SMP then auto load SMPCON

If connected to MEX then auto load SYCON

SYCON

Configure and initiate A 15 partitions

limited box panel displays

Menus:

MASTER: start partition, get partition status,
other menu select

CONFIGURE: establish partition membership

H/L information: set parameters for H/L (minimum
peripheral configuration) in an HDU assigned to
partition.

CPM: panel displays for CPM

HDU: panel displays for HDU

MSM: panel displays for MSM

SMPCON

Console software for running/testing SMP

Menus:

operator: initialize and start the SMP

software: display and manipulate SMP "virtual" state

hardware: display and manipulate SMP "real" state; also invoke hardware tests.

MP: issue basic SMP maintenance commands

BEAM

Command driven executive for running beam tests against SMP hardware (D-Drive).

TESTBUS

Command driven executive for running low-level DLP diagnostics against I/O subsystem hardware.

FILECON

File maintenance for console disk (remove, change, etc.)

File Transfer

Between floppy and hard disk

Between console and host (SMP OR A 15),
via ODT line

Between console and remote support center
(phase 2)

RUNNING PARTITION

With MBM switch in system position, console cannot interfere with running partition: cannot halt it, change membership, etc.

MCP in a running partition can:

Self H/L

Free/acquire individual boxes

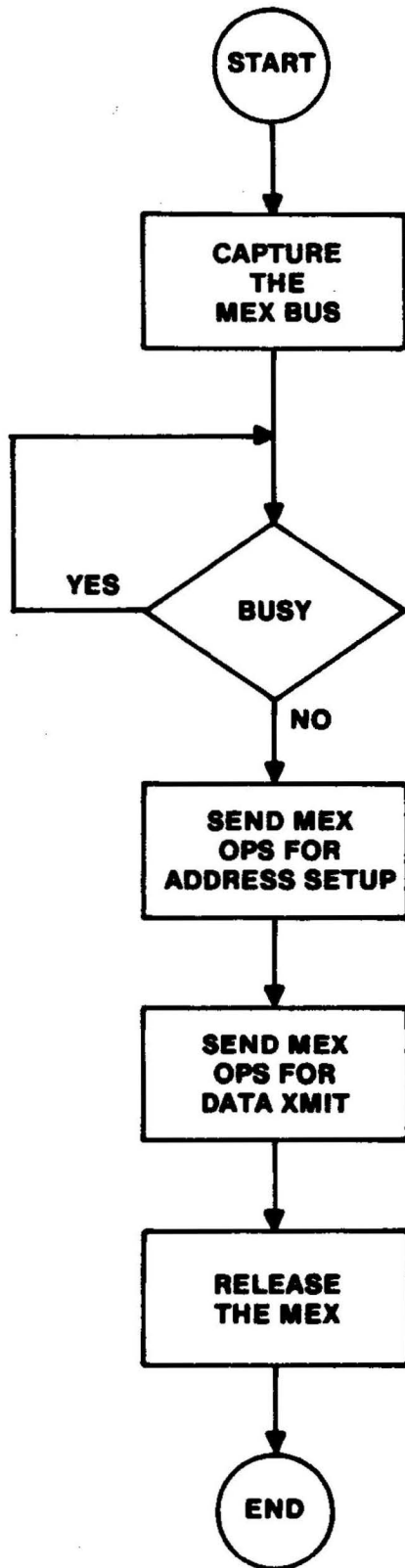
Halt

Timer enable BUS if:

Halt

Loop

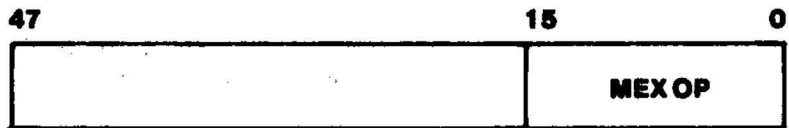
GENERAL MEX SEQUENCE



E5840

WIPS/RIPS OPERATORS

WIPS: OP CODE 9599



STATUS ID(6) = WRITE MAINT BUS INTERFACE

RIPS: OP CODE 9598



STATUS ID(6) = READ MAINT BUS INTERFACE

E5841

STATUS CODES

Hex Code	Meaning	Origin
3	FIA2 detected bad read parity	FIA2 (MIP only)
6	FIA2 detected bad command parity	FIA2 (MIP only)
7	FIA2 detected bad write data parity	FIA2 (MIP only)
D	FOA detected bad command or write data parity	FOA3
8	HMC detected bad command parity	HMC
9	HMC detected bad write data parity	HMC
A	HMC detected undefined command	HMC
B	HMC command error	HMC
C	HMC protect violation	HMC

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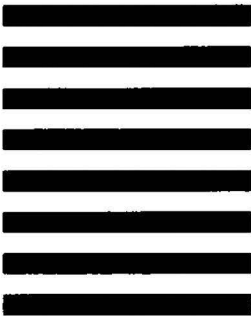
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