Direct Memory Access

DMA-Ø2 Logic Description

DMA-Ø5 Technical Reference

DMA-1Ø Assembly Drawings

DMA-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
B*	RELEASE FOR PRODUCTION	8-30-74	
C	ECN 0070	9-3-74	
D	ECN 0099	10-17-74	
E	ECN 0136	3-12-75	
F	ECN 0219	7-21-75	

DMA

* RELEASE AT B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER MFL

APP'D FOR REL MFL 7/11/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

DMA LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		DMA-02

SCALE	REV	SHEET
	F	1 OF 5

DMA LOGIC DESCRIPTION

Address Recognition

The DMA recognizes a block of eight words. The high order 6 bits must be ones, and the next 10 bits are determined by switches on the device interface (DI). Lines from these switches (ADS04-ADS13) are EX-ORed with address lines 4-13 and the results wire-ANDed to form SWMAT+. STRB+ is delayed by passing it through similar gating to form STRBD+. The latter is ANDed with HOLD- (to inhibit address recognition until the fall of HOLD) to form CLKAD which strobes the state of ADMAT into ME. The ME flop is operated inverted; ME+ is asserted when the Q output is true.

The rise of ME starts a 420 ns delay (MEPLS) before issuing a 50 ns DONE pulse (DONET). ME is cleared by the fall of undelayed STRB+.

The three low order address bits (not counting the byte bit, which is ignored) are sent to two demultiplexers (9334) to derive individual signals for writing and reading each of the individual registers. The data inputs are both senses of RITE, so one 9334 responds only to WRITEs and the other only to READs. The WRITE 9334 operates as a strict demultiplexer, enabled by MEPLS. The READ 9334 also demultiplexes but latches its state until the fall of ME+; thus its outputs are valid until the fall of STRB+.

Outputs from the 9334 are named:

{R (read) / W (write)} {
  {DEVT (device type) / DDP (device dependent)}
  {R (recv.) / X (xmit.)} {BEG (begin ptr.) / END (end ptr.) / ST (status)}
}

Several of these signals are passed directly to the DI as the appropriate control lines. For example, writing the begin pointer (WRBEG, WXBEG) pulses the RSTRT lines. Writing the end pointer (WREND, EXEND) pulses the START lines. Writing or reading the status (WRST, WXST, RRST, RXST) causes the appropriate GVST or STBST line to be asserted. If data bit 8 is set when writing the status (signifying a programmed reset) RSTRS or XSTRS will be asserted. These are ORed with MRES to form RRES and XRES. Accesses of the device dependent register (RDDP, WDDP)

and reads of the begin pointer (RRBEG, RXBEG) are sent to the DI and otherwise are ignored by the DMA.

Pointers

The pointers for receive and transmit sides are handled similarly. In the following, the receive half will be discussed; transmit is identical -- signal names are obtained by substituting an X for an R.

The "current" pointer, which holds the word address of the location either previously or just being accessed by that half of the CMA, is stored in a 19-bit synchronous counter (RC01-RC19). The carry input to stage 13 is disabled; therefore the high order seven bits of the counter (13-19) act only as a latch and do not change when the counter is toggled. This counter is parallel-loaded when the BEGIN pointer is written (WRBEG). The high order 16 bits come directly from the data bus (DB01-DB12). The low order 3 bits are specified by the low order 3 bits of the status word and are latched as RLC01-RLC03 by WRST. The counter is set for count-up operation.

The 12 bits of end pointer information are latched from the data bus by WREND. The outputs from the end pointer (RE01-RE12) are compared with the low order 12 bits of the current pointer (RC01-RC12). The output of the equals detect are wire-ANDed together to form the EOB signal.

Control

Bus access is controlled by two DBALs; one each for receive and transmit. In each DBAL, the A half controls data access and the B half handles pseudo-interrupt requests. The command inputs are connected directly to the DI's READY and DOINT lines, which signify that it wants a data or interrupt request, respectively. The answering signal to READY, NOW, is given for the transmit side coincident with ACLK telling the DI to strobe-in the data which the DMA has read for it; on the receive side, NOW follows AONL, telling the DI to output its data to the bus for the write cycle the DMA is performing. Receive NOW is delayed until the fall of the current PCDA so that a quick fall of READY in response to NOW will not allow a little PCDA to leak out. The response to DOINT, INTDN, is given at BCLK time. The DBALs are connected to the bus in the usual way, in parallel. QUIT and DONE are buffered to provide the necessary fanout to drive two DBALs. The precedence pulse (PCDA-PCDAB-PCDB) is chained

serially through the DBALs. The DBAL is reset either by the reset signal for that half (RRES/XRES), or when the begin pointer is written. If the latter occurs in the normal course of events, viz., after an interrupt has occurred and the program is setting up for the next buffer, no bus transactions will be in progress and reset will do nothing. However, if the begin pointer (to perform the restart function) is written while the device is active, the desirable feature of stopping any transaction in progress is accomplished.

The QUIT latches (RQUTL/XQUTL) remember that a QUIT has occurred during an access. They are reset by reset or the writing of the begin pointer for the next buffer.

Writing the begin pointer also sets the corresponding "first" flop (RFRST/XFRST), thus preventing the first access from toggling RCLK/XCLK. At its conclusion (the trailing edge of NOW/DOIT), the flop is reset and CLK follows READY.

RITE is latched from the bus by STRB. RITE is asserted on the bus by the DMA (RITET) when on-line for either a receive access (RONLN) or an interrupt access (DOINT).

The Data Bus

The DMA contains a 16-line, open collector, negatively asserted bus (DAB00-DAB15). These wires are passed to the DI (ST00-ST15) and are used to pass non-data information to the DMA, e.g., device type, interrupt levels, status. The other primary source is the pointer multiplexer, which multiplexes the two current pointers and converts to open collector form. The multiplexer is enabled onto the DAB lines either when on-line for a data transfer (DATOL) or when reading either end pointer (RDEND) (only the low order 12 bits). In the former case we are broadcasting the address to be used for the data transfer. The DAB lines in this case go through the address multiplexer to the address BDRs. (Note that bits 16-19 go directly to the multiplexer since they are not used elsewhere.) If the end pointers are being read, the data BDRs are enabled (DDREN from SLVRD) and the address BDRs (ONLN) are not -- thus the information goes on the data lines. A situation similar to the latter occurs when reading status or device type, except that the DI provides the source. During an interrupt access (DOINT), the address multiplexer switches so that the prewired (except for two bits from the DI) PID address is connected to the address BDRs. The DI supplies the PI level via the DAB lines which are broadcast on the data lines, since DOINT is a term in DDREN.

Special Status Bits

The error bits (RERR/XERR) are passed from the DI. The sense of the QUIT latch is ORed in and when the end pointer is read (RREND/RXEND) it is connected to bit 0. The last packet bit (LASTP) is also passed from the DI. If there is no QUIT on the receive side (RQUTL), completion will be reported (bit 15 set) when the end pointer is read. The sense of the QUIT latches is reported as bit 8 when the status words are read (RRST/RXST). The signal GVPI asking for the DI to present the appropriate PI levels on the ST lines is asserted when status is read (RRST/RXST), or when an interrupt access is on-line (RBONL/XBONL).

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8-30-74	

DMA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER MFK

APP'D FOR REL MFK 12/11/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

DMA TECHNICAL REF

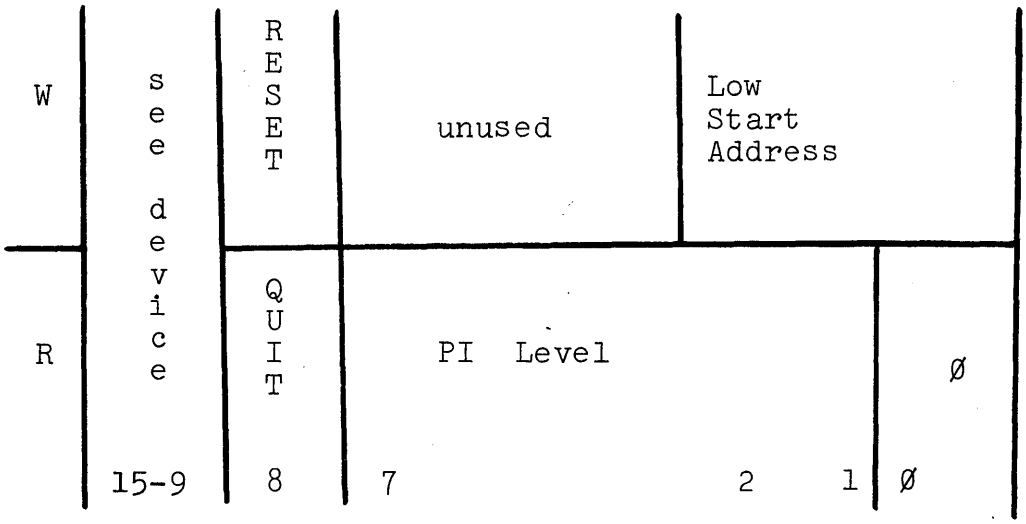
SIZE	CODE IDENT NO.	DRAWING NO.
A		DMA-05

SCALE	REV	SHEET
	A	1 OF 2

DMA - Direct Memory Access BBN

see also individual devices

Status - address FXXX6(receive), FXXXC(transmit) DMA

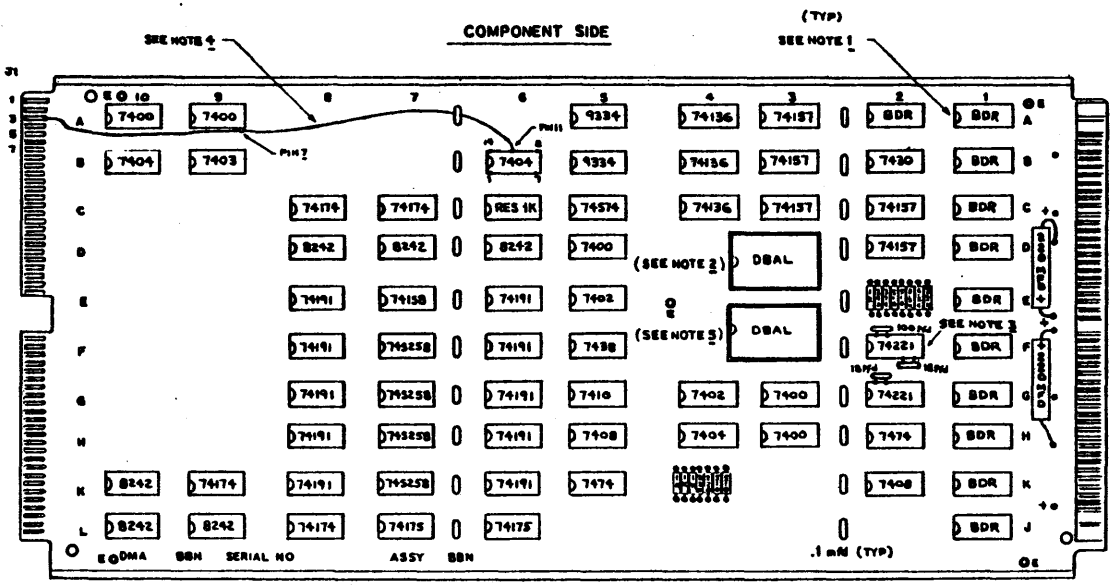


Switches - none

Jumpers - none

DMA-1Ø ASSEMBLY DRAWING

APPD	REVISION SYM	DESCR	DATE
MFK	A	REL for PROD	9-9-73
MFK	B	ECN #0013	11-26-73
MFK	C	ECN #0099 ECN 0100	12-28-74
MFK	D	ECN 0102	12-3-74
MFK	E	ECN 0136	3-18-75
MFK	F	ECN 0162	9-16-75
	G	ECN 0288	9-28-78
	H	ECN 0296	5-2-78



COMPONENT VALUES

20 CAPACITORS (TYP) = .1 mfd CERAMIC DISC

2 CAPACITORS = 220 mfd-10 VOLT ELECTROLYTIC

5 BINDING POST (E) = CAMBION #1457-1-01 (GROUND TURRETS)

ALL RESISTORS ARE ¼ WATT, 10 %

NOTES

1 – NOTCH SHOWN IN BUG INDICATES INSERTION DIRECTION.

2 – MOUNT DBAL'S ON SOCKETS, ALL OTHER COMPONENTS MOUNT DIRECTLY ON CARD.

3 – CAPACITORS, 18 (2) ℄ 100 pfd ARE SOLDERED DIRECTLY TO PINS OF F2 ℄ G2 (SEE DMA-00-MW)

4 – SOLDER A 30 AWG W.W. WIRE FROM J1:3 INTO THE HOLE USED BY THE IC LEAD AT B6:11, ROUTE AS SHOWN (UNDER A9 IC, PIN 7 LEAD ℄ UNDER .1 mfd CAP)

5 – CUT WIRE BETWEEN B6:11 ℄ F4:22, MAKE CUT AS SHALLOW AS POSSIBLE, REMOVE A SMALL PORTION OF THE WIRE, MAKE CUT IN THE MOST OPEN PLACE

COMPUTER SYSTEMS DIVISION
EDP PERIPHERALS INC
CAMBRIDGE MASS 02138

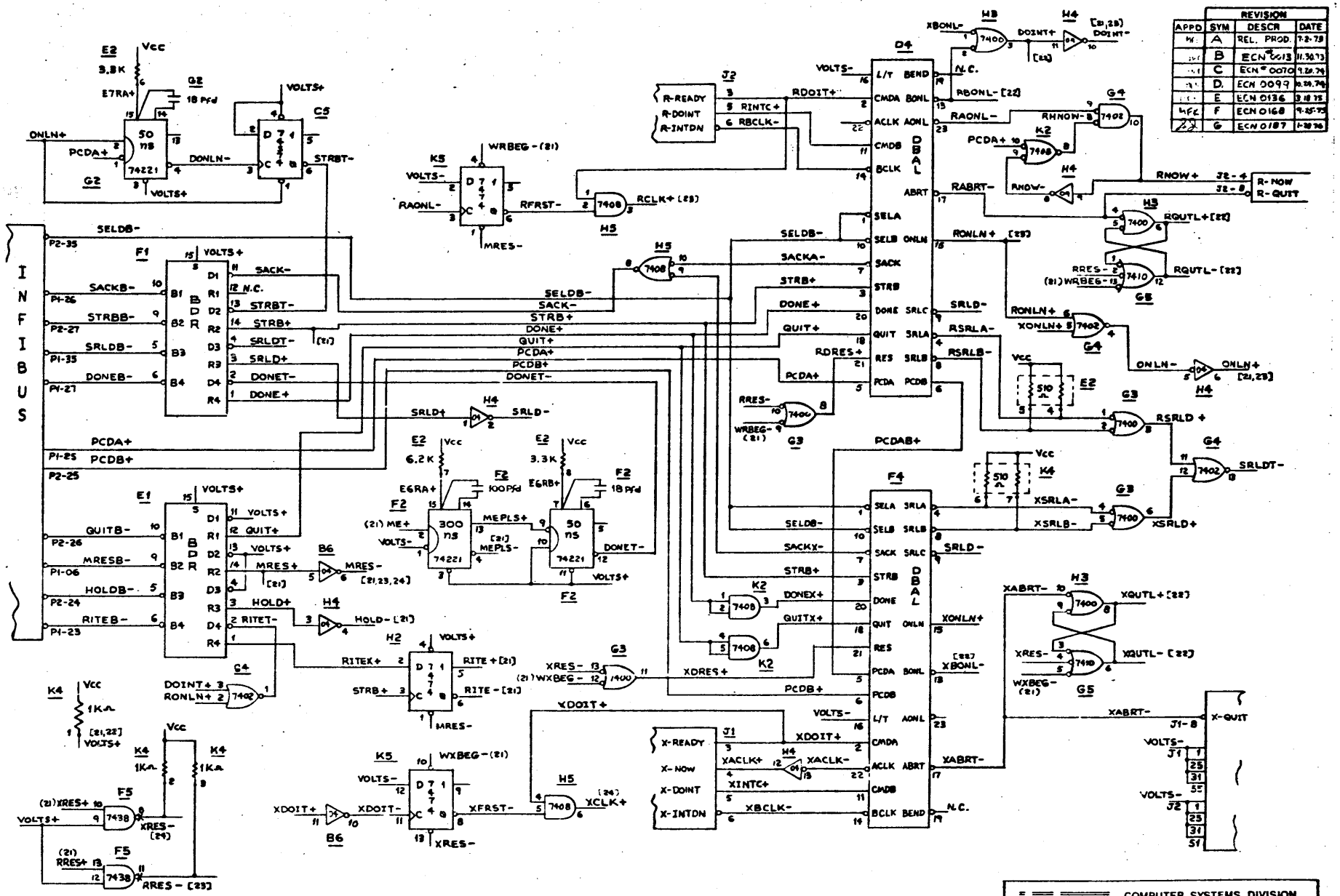
		DATE
DRAWN	DRF	9/22
CHECKED	DRF	9/28
APPROVED	MFK	9/29/73

INTEGRATED CIRCUIT ASSEMBLY

HSMIMP DMA-10-MW H

DMA

DMA-2Ø SCHEMATICS

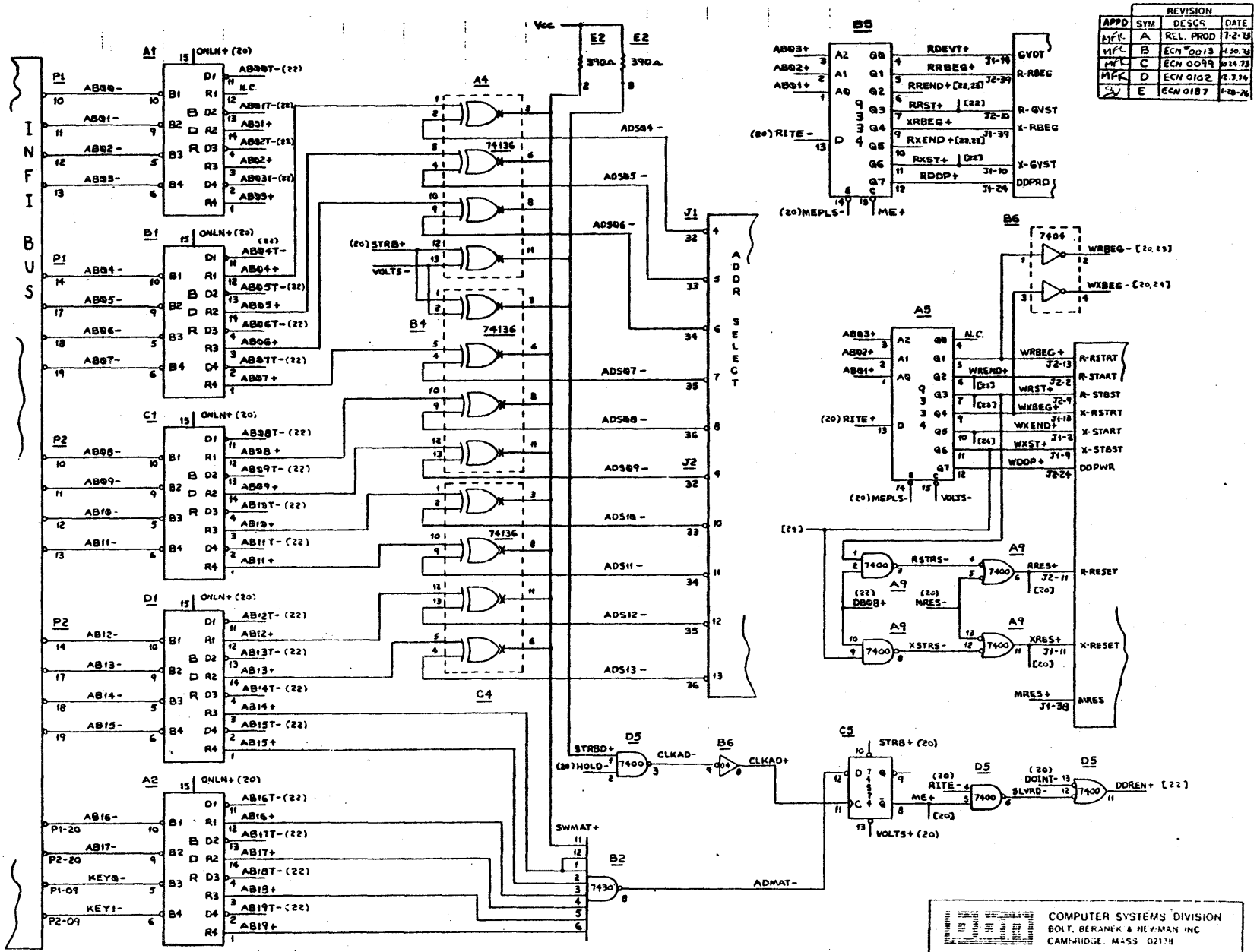


REVISION			
APPD	SYM	DESCR	DATE
	A	REL. PROD.	7-2-73
	B	ECN 0013	11.30.73
	C	ECN 0070	9.26.74
	D	ECN 0099	10.29.74
	E	ECN 0136	3.10.75
	F	ECN 0168	9-25-75
	G	ECN 0187	1-30-76

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	3/4/73	TITLE: DMA CONTROL
CHECKED	DRF	7.2.73	CUSTOMER NO.: HSMIMP
APPROVED	[illegible]	4/1/75	DWG NO.: DMA-20-MW
			REV: G

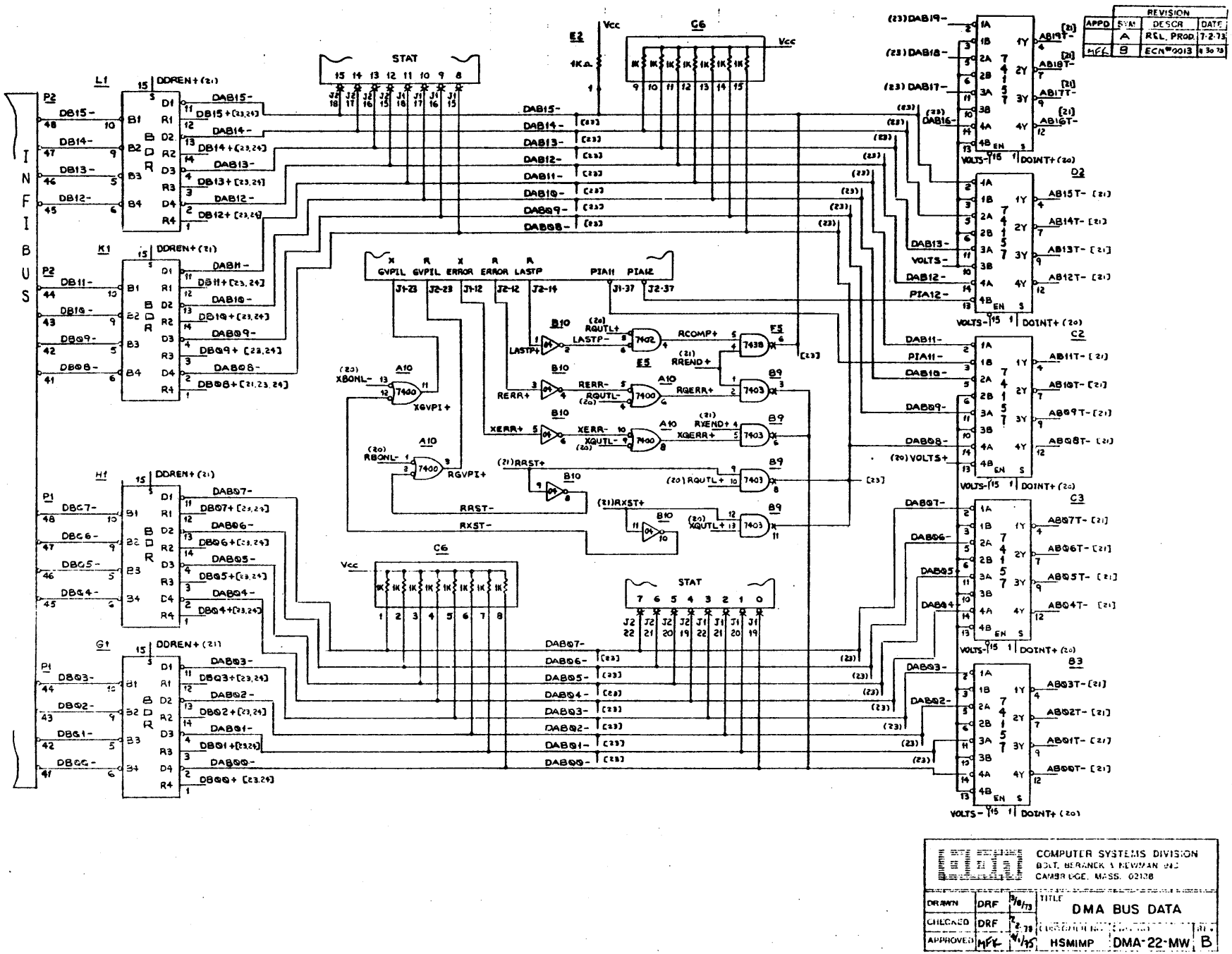
DMA



	REVISION		
APPD	SYM	DESCR	DATE
MFK	A	REL. PROD	7-2-73
MFK	B	ECN #0013	4-30-74
MFK	C	ECN 0099	9-24-75
MFK	D	ECN 0102	12-3-74
SW	E	ECN 0187	1-28-76

BBN COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	8/11/73	TITLE: DMA ADDRESS RECOGNITION & DECODE
CHECKED	DRF	9/2/73	
APPROVED	MFK	9/11/75	CUSTOMER NO. HSMIMP; DWG. NO. DMA-21-MW; REV. E

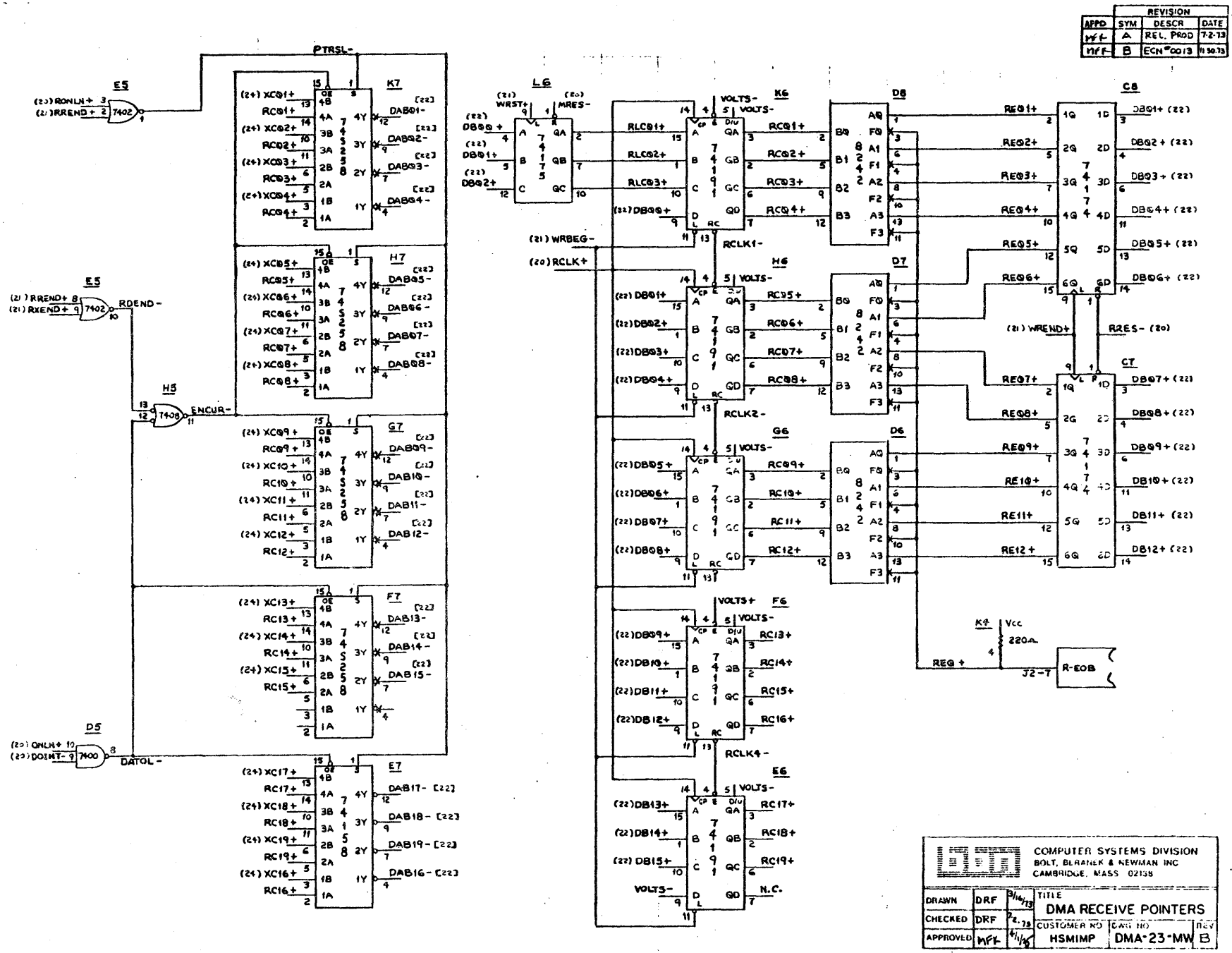


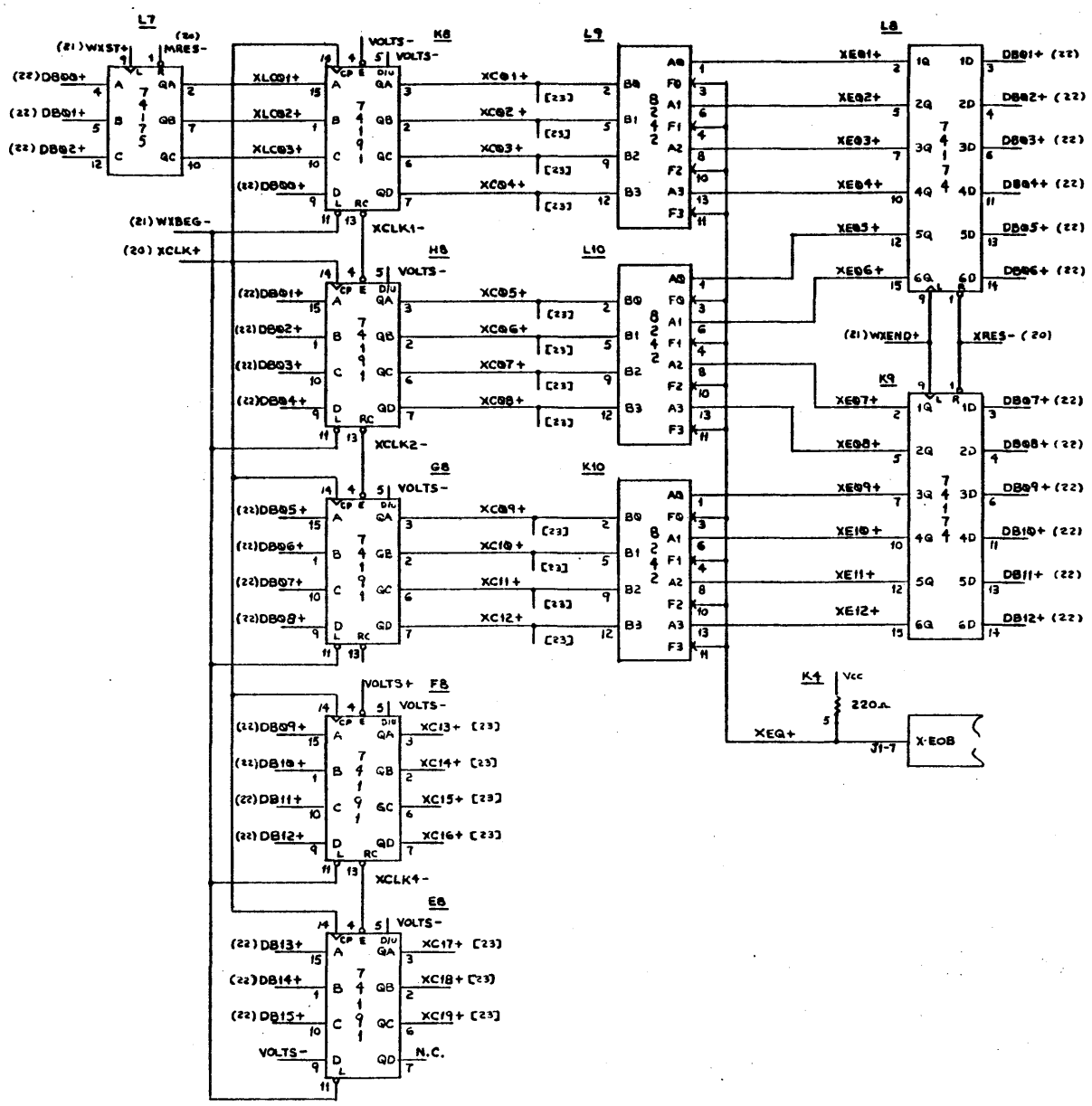
REVISION			
APPD	SYM	DESCR	DATE
	A	REL. PROD	7-2-73
MFK	B	ECN#0013	8 30 73

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/16/73	TITLE: DMA BUS DATA
CHECKED	DRF	8-29-73	
APPROVED	MFK	9/1/73	HSMIMP DMA-22-MW B

DMA


REVISION
APPD SYM DESCR DATE
MFF A REL. PROD 7-2-73
MFF B ECN#0013 11-30-73
PTRSL-
E5
(23) RONLN+ 3
(21) RREND+ 2
7402
K7
(24) XC01+
RC01+
(24) XC02+
RC02+
(24) XC03+
RC03+
(24) XC04+
RC04+
DAB01- [22]
DAB02- [22]
DAB03- [22]
DAB04- [22]
H7
(24) XC05+
RC05+
(24) XC06+
RC06+
(24) XC07+
RC07+
(24) XC08+
RC08+
DAB05- [22]
DAB06- [22]
DAB07- [22]
DAB08- [22]
E5
(21) RREND+ 8
(21) RXEND+ 9
7402
RDEND-
H5
7408
ENCUR-
G7
(24) XC09+
RC09+
(24) XC10+
RC10+
(24) XC11+
RC11+
(24) XC12+
RC12+
DAB09- [22]
DAB10- [22]
DAB11- [22]
DAB12- [22]
F7
(24) XC13+
RC13+
(24) XC14+
RC14+
(24) XC15+
RC15+
DAB13- [22]
DAB14- [22]
DAB15- [22]
D5
(23) ONLN+ 10
(23) DOINT- 9
7400
DATOL-
E7
(24) XC17+
RC17+
(24) XC18+
RC18+
(24) XC19+
RC19+
(24) XC16+
RC16+
DAB17- [22]
DAB18- [22]
DAB19- [22]
DAB16- [22]
L6
(21) WRST+
(20) MRES-
(22) DB00+
(22) DB01+
(22) DB02+
(21) WRBEG-
(20) RCLK+
K6
VOLTS-
RLC01+
RLC02+
RLC03+
(22) DB00+
RCLK1-
RC01+
RC02+
RC03+
RC04+
H6
(22) DB01+
(22) DB02+
(22) DB03+
(22) DB04+
RCLK2-
RC05+
RC06+
RC07+
RC08+
G6
(22) DB05+
(22) DB06+
(22) DB07+
(22) DB08+
RCLK4-
RC09+
RC10+
RC11+
RC12+
F6
VOLTS+
(22) DB09+
(22) DB10+
(22) DB11+
(22) DB12+
RCLK4-
RC13+
RC14+
RC15+
RC16+
E6
(22) DB13+
(22) DB14+
(22) DB15+
VOLTS-
N.C.
RC17+
RC18+
RC19+
D8
D7
D6
C6
C7
REQ1+
REQ2+
REQ3+
REQ4+
REQ5+
REQ6+
REQ7+
REQ8+
REQ9+
RE10+
RE11+
RE12+
DB01+ (22)
DB02+ (22)
DB03+ (22)
DB04+ (22)
DB05+ (22)
DB06+ (22)
DB07+ (22)
DB08+ (22)
DB09+ (22)
DB10+ (22)
DB11+ (22)
DB12+ (22)
(21) WREND+
RRES- (20)
K4
Vcc
220Ω
REQ+
J2-7
R-EOB
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN DRF 3/16/73
CHECKED DRF 7.2.73
APPROVED MFF 4/1/73
TITLE
DMA RECEIVE POINTERS
CUSTOMER NO HSMIMP
DWG NO DMA-23-MW
REV B



	REVISION		
APPD	SYM	DESCR	DATE
MFL	A	REL. PROD	7-2-73
MFL	B	ECN#0013	8-30-78

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	5/16/73	TITLE: DMA TRANSMIT POINTERS
CHECKED	DRF	7-2-73	CUSTOMER NO: HSMIMP
APPROVED	MFL	4/1/75	DWG NO: DMA-24-MW
			REV: B

DMA

8K Memory Magnetics X and Y

EXY-Ø2 Logic Description

EXY-Ø5 Technical Reference

EXY-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

EXY

SEE TAG-02

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL 12/20/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

EXY LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		EXY-02

SCALE	REV	SHEET 1 OF 1

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	

EXY

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

EXY TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		EXY-05

SCALE	REV	SHEET
	A	1 OF 1

EXY - 8K Core - Magnetics X and Y Lockheed

Status - address none

Switches - none

Jumpers - Interleave Mode

Remove	J 2-1	to	J 2-2
ADD	J 3-1	to	J 3-2

EXY-2Ø SCHEMATICS

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

EXY

SEE TAG-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN 12/8/75	DRAWING TITLE: EXY SCHEMATIC
	CHECKER	
	ENGINEER	
	APP'D FOR REL	SIZE: A; CODE IDENT NO.; DRAWING NO.: EXY-2Ø
	APP'D (CUSTOMER)	SCALE; REV; SHEET 1 OF 1

Compatible Local Host

HLC-Ø2 Logic Description

HLC-Ø5 Technical Reference

HLC-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	4-25-73	
B	ECN 0009	11-27-73	
C	ECN 0046	3-30-74	
D	ECN 0218	[illegible]	

HLC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL 7/5/07

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

HLC LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		HLC-02

SCALE	REV	SHEET
	D	1 OF 10

HLC LOGIC DESCRIPTION

The Compatible Local Host interface (HLC) is a single card module interconnecting a local Special Host Interface as detailed in BBN Report #1822, "Specifications for the Interconnection of a Host and an IMP." The functional specification for this module outlines operational aspects, while the present document describes the logic in detail. The following descriptions assume that the interface has been cleared, the Host and IMP are in the ready state, and the interface is unlooped. Signals signed + are true when at a TTL high and signals signed - are true when low.

Output Section (HLC20)

An output transfer is initiated when the buffer end pointer is written to the DMA, which in turn asserts START (STRTT+, 100-150 ns). On its rising edge, the high order data bit on the INFIBUS DBR15 is sampled to see if this is the start of the last packet. If so, EOMTX is set. The inverted version of STRTT assures that LIBTF is cleared, clears the 74161 bit counter, sets BUSYT to an active condition and sets RDYTF+. Since BUSYT is true, REDYT+ is true. This appears at the DMA as READY, the data service request line. When the DMA gains bus access and the data is present on the bus, the DMA asserts NOW (NOWTX+, 40-60 ns). This signal direct loads the 16-bit output shift register from the bus receivers and direct clears RDYTF. On the trailing edge of NOWTX, BTAVL is set to indicate that the high order bit of the shift register is available on the data line to the Host, IMDTA+.

When the Host is ready to receive, he will assert READY FOR NEXT BIT (RFNIB+). Since the interface is unlooped and the Host is ready, BNABL is true and TYIMB+ (THERE'S YOUR IMP BIT) appears on the cable to the Host, signifying that the bit is now available on the data line IMDTA. Note that it makes no difference whether RFNIB comes true before or after BTAVL.

Upon accepting the data bit, the Host shuts off RFNIB, firing SHIFT (100 ns). The leading edge shifts a new bit into position while the trailing edge increments the bit counter on the rising edge of SHIFT-. Also, SHIFT direct clears BTAVL, removing TYIMB in conjunction with the disappearance of RFNIB. Since DONET is not true, TDELY (adjustable for desired IMP-to-Host transmission rate) fires on the trailing edge of SHIFT. The trailing edge of TDELY sets BTAVL to indicate that a new bit is available.

This sequence repeats until DONET, an all 1's detector, comes true after the 15th SHIFT. On the 16th SHIFT, since DONET is true, TDELY does not fire. Instead, because EOBTX is false, the trailing edge of SHIFT sets RDYTF, raising REDYT. When NOWTX is returned by the DMA, this new word and succeeding words are transferred as above.

When the last word of the buffer is requested, the DMA raises EOB (EOBTX+) sometime after it sees REDYT, but before it raises NOWTX. This time when DONET comes true, if EOMTX was true (last packet), LIBTF is set. This appears at the Host as LIBIT+ (LAST IMP BIT), indicating that the next bit will be the last bit of the message. If EOMTX was not true, LIBTF will not be set. In either case, on the trailing edge of the next shift, which follows transmission of the sixteenth bit, BUSYT is shut off. The fall of BUSYT sets RINTT (DOINT at the DMA). The DMA acknowledges this interrupt request by raising INTDN (CLRIT-, 40-60 ns), which direct clears RINTT. The interface is ready now for another START pulse.

In the event that a data word access fails and QUIT appears on the bus, the DMA asserts QUIT (QUITT-, 80-100 ns). This is used to direct clear BUSYT, which holds BTAVL clear. It also direct clears RINTT, preventing the fall of BUSYT from setting RINTT. At the same time, since BUSYT was true, the rise of QUITT sets QUINT, raising DOINT to the DMA. When the DMA returns CLRIT, the interface is quiet once again. If the interrupt access should fail, QUITT will come true while DOINT is true. This will direct clear RINTT if it is set. However, if QUINT is true, the leading edge of QUITT will clear QUINT since BUSYT is false. In either case, QUITT will shut off DOINT, once again leaving the interface quiet.

There are four ways to generate the clear signals used in this section of the interface (see HLC22). A bus MASTER RESET is passed to the interface from the DMA as MRES (MRESX+, 500 microseconds) and as RESET (RESETT+, 500 microseconds) which appears as RESTT in the transmit section. These signals clear all but one of the flops, and reset all delays to render the transmit section quiescent. RESET can be generated under program control also and passed from the DMA (100-150 nsec). In this case the interface is cleared as above, except that RINTT is not directly altered. If the interface has been active, the fall of BUSYT sets RINTT. When the DMA responds, the interface is left quiet.

Writing a begin pointer causes the DMA to assert RSTRT (RSTRT+, 100-150 ns). The effect is identical to the assertion of RSETT. Also identical is the effect of looping or unlooping the interface. An active interface in either case will raise DOINT.

In the case of a looped interface, signals to and from the IMP are shut off (BNABL false and LOOPX true) and corresponding signals from the receive section are gated on when IMRDY is true (LPRDY true). Operation is otherwise identical.

Input Section (HLC21)

When the receive end pointer is written, the DMA asserts START (STRTR+, 100-150 ns). This signal direct sets BUSYR to indicate that the interface is active, direct clears the 74161 bit counter, insures that RDYRF is cleared, and since neither LASTR, LASTP, or DONER is true, its trailing edge fires RDELY (adjustable for desired Host-to-IMP transmission rate). Since TYBTN is false and neither RDYRF nor NOWRX are true, the trailing edge of REDLY sets RFNBF, and, since the interface is unlooped, this appears at the Host as RFNHB+ (READY FOR NEXT HOST BIT).

When the Host asserts TYHBX+ (THERE'S YOUR HOST BIT) to indicate that a bit is available on the Host Data line (HSDTA+), the leading edge of TYHBX sets TYNHB. Any subsequent transitions will have no effect until the next bit is available. This prevents uncontrolled transitions on TYHBX from causing excessive interface activity. The rise of TYNHB fires SHIFR (100 ns) which direct clears RFNBF. The leading edge of SHIFR shifts the data into the low order bit of the shift register and the trailing edge increments the bit counter. Since DONER, LASTR and LASTP still are not true, the trailing edge of SHIFR also fires RDELY when TYBIN is false and RDELY has run out, RFNBF is set again and the above sequence is repeated.

On the trailing edge of the 15th SHIFR, DONER comes true, indicating all 1's in the bit counter. On the next SHIFR accompanying the 16th bit, RDYRF is set on the leading edge and REDYR+ (READY) is raised to the DMA to indicate that a word is available for a data access. When the DMA responds by raising NOWR (NOWRX+, 40-60 ns) the data drivers to the INFIBUS (HLC22) are enabled and the data word is stored. NOWRX also direct clears RDYRF and since EOBLP is false, its trailing edge fires RDELY to start input of the next word. However, the fall of RDELY or TYBIN cannot set RFNBF while a memory access is in progress since RDYRF and NOWRX must be false to set RFNBF.

When a word access will fill a buffer, the DMA asserts EOB (EOBRX+) to indicate this condition sometime after the interface has raised REDYR but before the DMA issues NOWRX. The result is that since EOBRX is true, the trailing edge of NOWRX clears BUSYR, indicating that the interface is no longer active. The fall of BUSYR sets RINTR (DOINT at the DMA) to request the DMA to issue an interrupt. The DMA responds to the interrupt by asserting INTDN (CLRIR-, 40-60 ms) which direct clears RINTR, leaving the interface ready to accept the next STRTR pulse.

When the Host raises TYHBX with the last bit of a given message, he also raises LAST HOST BIT (LHBIT+). If the card is jumpered to pad with a 1 followed by zeros, the leading edge of the resultant SHIFR sets LASTR. What happens next depends on the relationship of the last bit to the HSMIMP word boundary. Under all circumstances, the interface must append a marking one bit after the last bit followed by enough zeros (0 to 15) to fill up the current word. The interesting cases occur when the last bit falls between the 1st to 14th bit of the word, at the 15th bit, or at the 16th bit. Since LASTR is set by SHIFR following the last bit, but DONER is false, the trailing edge of SHIFR fires PADLY (100 ns), whose trailing edge sets PADFF. The leading edge of PADFF fires SHIFR, but since LASTR is true, the register shifts a one into its low order bit. Note that because of the bus drivers the shift register is operating inverted. The leading edge of SHIFR also sets LASTP, which direct clears LASTR. Since LASTP is now true, the trailing edge of SHIFR once again fires PADLY which sets PADFF, firing SHIFR. This time the bit shifted into the register is zero since LASTR is now false and LASTP is true. The clock input to LASTP is disabled, however, since it is now set. This sequence is repeated until DONER comes true as above. Since LASTP is true, the trailing edge of NOWRX clears BUSYR, setting DOINR. As before, the operation is terminated by CLRIR. The DMA reads LASTP to determine that this is the last packet of the message. This line (LASTM) is true only at the DMA, however, when ERORF, indicating a receiver error, is false.

Should the last bit of the message be the 15th bit of the word, everything proceeds as above, but since DONER is true following the 15th bit, the 16th SHIFT captures a one and causes RDYRF to be set. Since the last SHIFR was able to set LASTP, the trailing edge of NOWRX clears BUSYR, and DOINR is set as above.

In the case where the last bit of the message falls on the 16th bit, RDYRF is set in the usual way, but NOWRX will find

LASTR set and its trailing edge will fire PADLY. As above, first a one, then 15 zeros, will be shifted into the register. Since LASTR is true, the final data access will be followed by DOINT being set. In the event that the word containing the last bit fills the buffer, the presence of EOBRX will cause NOWRX to clear BUSYR, setting DOINR. When the next input is begun with STRTR, PADLY fires on its trailing edge and, as before, the marking bit and padding bits are shifted into the register followed by a data access and interrupt.

On the other hand, if the card is jumpered to pad only zeros, the leading edge of the SHIFR after LHBIT sets LASTP. The padding sequence is essentially identical to that described above, with the exception that LASTR never comes true, and LASTP comes true one bit earlier. For instance, if the last bit falls at the 16th bit of a word, no padding will take place, since LASTP will be true when NOWRX comes true following the data access.

Response to a QUIT is identical to that for transmit. QUIT passed from the DMA (QUITR-, 80-100 ns) direct clears BUSYR, if it has been set, and direct clears RINTR. If BUSYR has been set, QUINR will be set on the leading edge of QUITR, raising DOINT to the DMA. Similarly if DOINT has been true previously, RINTR will either be direct cleared, or cleared on the leading edge of QUITR since BUSYT is true.

Operation of the various reset options is identical to that for transmit. Refer to the previous section and drawing HLC22. As for transmit, looping the interface substitutes transmit side signals for Host signals, but operation is otherwise the same.

Status and Interconnection (HLC22)

Three main functions are contained in this logic: Host and IMP ready and error, interface loop, and status as read. The remainder is miscellaneous inversion of DMA control signals, generation of the reset signals, bus drivers, receiver modules, and the various external interconnections.

When writing transmit status, the DMA asserts STBST (RDSTT+, 100-150 ns). On its leading edge, data bit 12 (DBR12) is sampled to indicate whether IMRFF should be set or clear. If clear, IMRDY will be held off, disabling the drivers to the Host. If set, IMRDY will be true when retriggered at the prescribed interval by writing to the transmit or receive status words causing the DMA to assert STBST (RDSTT or RDSTR, 100-150 ns).

If the card is jumpered to use the ready line and if IMRDY is set and the interface is unlooped (LOOPX false), a relay closes, shorting XMTOT and XMTXN to indicate to the Host that the IMP is ready. When the Host is also ready HMRDY is at ground and when the interface is unlooped HNABL and BNABL are true, allowing gating of certain external signals when both the IMP and Host are in a ready condition. HNABL indicates that the Host is ready and the interface is unlooped.

If the card is jumpered to ignore the ready lines, the relay will not close and HMRDY is always at ground.

HERRF is set to indicate a receive error. This can be accomplished when HMRDY goes false, direct setting HERRF, when the interface is not looped. Whenever IMRDY goes false, this also direct sets HERRF. The error condition is cleared by starting a new input when STRTR direct clears HERRF.

In the looped interface, HRDYX follows IMRDY, while in the unlooped state it follows HMRDY. In either case the ERROR line to the DMA (ERORR) is true when HERRF is true.

For both receive and transmit, the ERROR line to the DMA is asserted if an interrupt request is caused by other than a normal end of message. It is cleared by either a Master Reset or a START from the DMA. For transmit, the fall of BUSYT sets ERORT if RESTT is true. Once set, the clock input is disabled and ERORT can be direct cleared only by MRESX or by START. If QUITT is asserted, ERORT will be direct set. ERORT+ occurs at the DMA as ERORT.

The receive error logic is essentially identical, but HERRF direct sets ERORR. The two error status bits, HREOM and HERRX respectively, are true when there has been a Host error with and without an end of message indication.

Transmit and receive ERROR is true while the transmit and receive sections are active (BUSY T and BUSY R true).

Looping is accomplished in the following way. Receive STBST (RDSTR, 100-150 ns) samples data bit 14 on the INFIBUS (DBR14) into GOLUP. The trailing edge of RDSTR samples GOLUP into LOOPX. If the contents of LOOPX ever are different from DBR14 during RDSTR, LPRST will be asserted. This signal is a component of RESTT and RESTR, so as looping or unlooping takes place, both sides of the interface are cleared, and if they were active,

interrupts will result. MASTER RESET on the INFIBUS will cause the DMA to issue MRES (MRESX+, 500 microseconds) which forces the interface into the unlooped state.

When status is read from the DMA, it asserts GVST for either transmit or receive (STSTX+ or STSRX+, 100-150 ns). These signals are used to gate various status conditions onto the open collector bus to the DMA. GOLUP is read for either transmit or receive; BUSYT and IMRDY are read for transmit; BUSYR, HRDYX, HERRX and HREOM are read for receive. The device-type number, 2, is put on the open collector bus when the DMA asserts GVDT (STSDX+, 100-150 ns).

As can be seen, the two reset signals, RESTT and RESTR, are formed of the components discussed earlier. Other signals from the DMA are inverted to achieve the proper sense for use in the control logic.

Switches (HLC23)

Device-type data, and transmit and receive PI codes are made available to the DMA by driving open collector inverters onto those lines to the DMA where the switches have been installed. This delivers the proper code to the DMA at the proper time. The other switches are straightforward and all switch functions are described in the HLC functional specification.

Drivers and Receivers

IMP drivers are discrete component current drivers allowing interconnection of a number of IMP interfaces to the same Host. When IMRDY is either cleared or timed out, the drivers are disabled, allowing the drivers in another interface to drive the lines to the Host. IMP receivers are high impedance Schmitt trigger inverters. These lines terminate in 68 ohm resistors at the driver to achieve a typical signal level of about 5 volts at the receiver. When connecting more than one interface in parallel to the same Host, the termination resistors must be removed from all but the last interface card in the string. The driver is described below in detail.

The 26-pin connector on the interface board is laid out to provide a ground line between each adjacent signal wire in a flat ribbon cable to avoid cross talk. Alternatively, the return line of each twisted pair will be grounded using flat woven cable.

Drivers and receivers to and from the DMA are standard TTL gates employed as described in the functional specifications for the DMA and the Compatible Local Host. Bus drivers and receivers are the standard CMI integrated circuits.

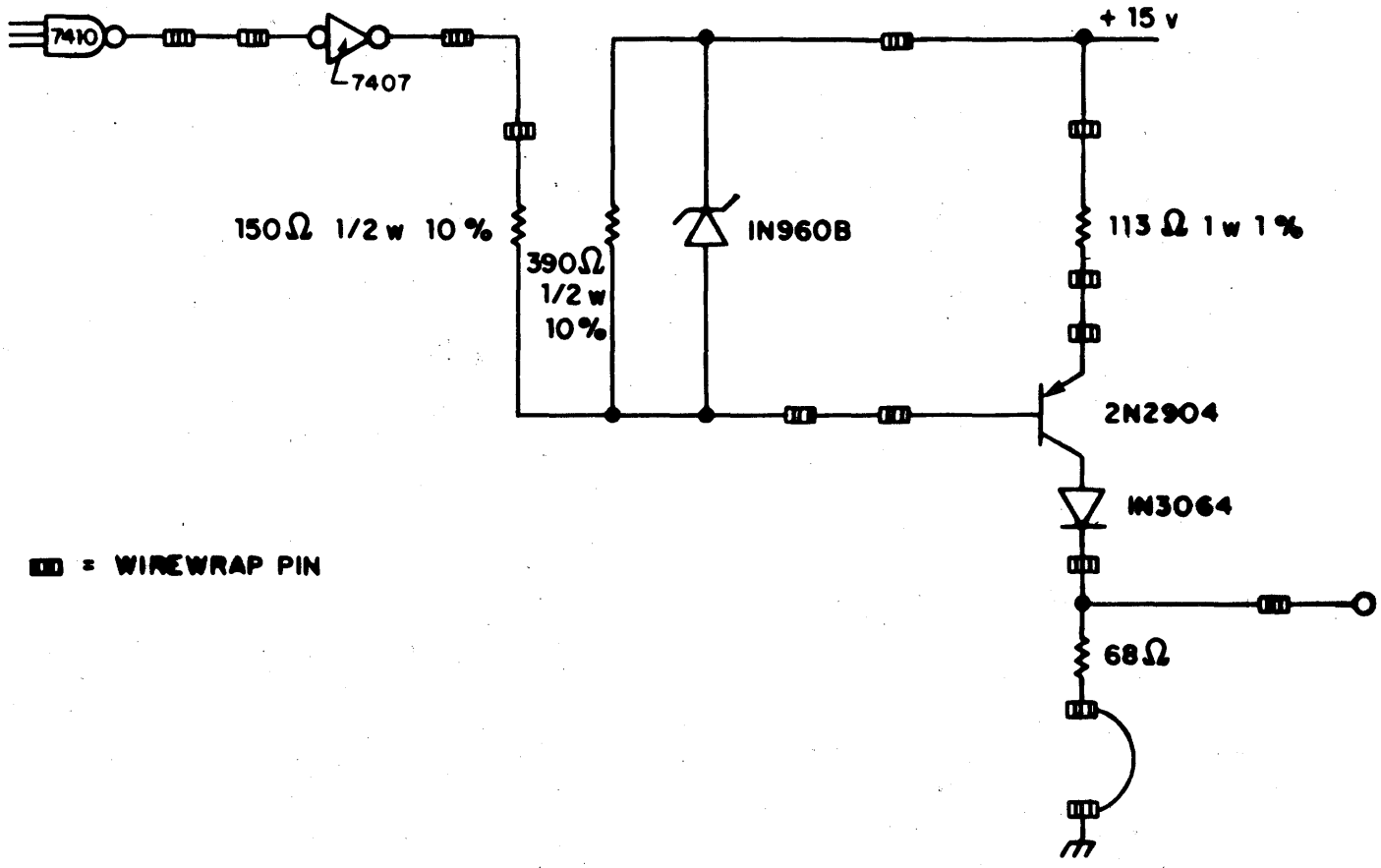


Figure 1 Typical Driver

In the "1" state, the output of the 7407 is at ground, causing the 9.1 volt Zener diode to conduct. The transistor base is then at 5.9 volts, with current through the Zener diode at about 20 ma. The transistor will now conduct, with the emitter at about 6.6 volts. The collector current will then be about 75 ma causing a 5 volt drop across the 68 ohm load resistor.

When the input is in the "0" state, the open collector output of the 7407 will be pulled up to +15 volts shutting off the transistor. Therefore, since no voltage is developed across the load resistor, line voltage is zero.

The diode in the collector lead is to cause an inactive driver to present a high impedance to the line, even when no power is applied to that driver.

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION	8-30-74	

HLC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER	
APP'D FOR REL	7511 07
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

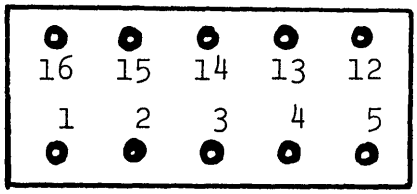
DRAWING TITLE

HLC TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		HLC-05

SCALE	REV	SHEET
	A	1 OF 3

JUMPERS



READY LINE

Type	Connect	
	From	To
ENABLE	3	14
	4	13
	5	12
DISABLE	13	14

PADDING

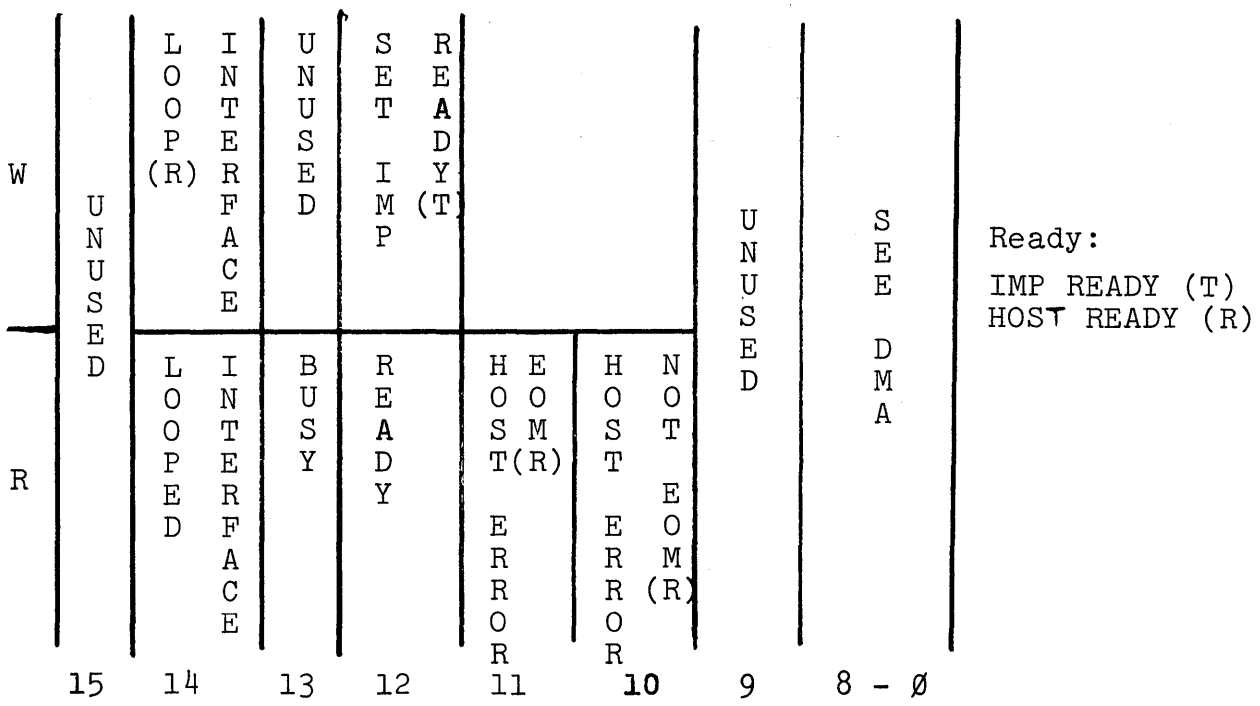
Type	Connect	
	From	To
ONE	1	16
	2	15
NO ONE	1	2
	15	16

SOCKET

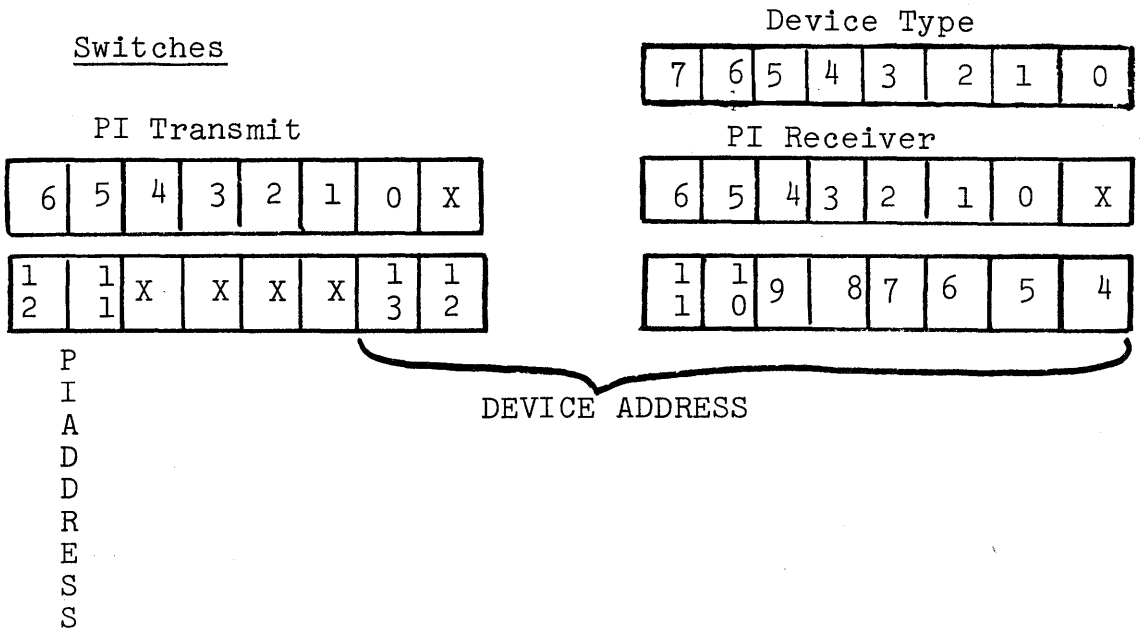
1 Ready for next IMP Bit
2 There's your IMP Bit
3 Last IMP Bit
4 IMP Data
5 Ready for next Host Bit
6 There's your Host Bit
7 Last Host Bit
8 Host Data
9 IMP Master Ready
10 IMP Ready Test
11 Host Master Ready
12 Host Ready Test
13 Unused
14-26 Ground

see also DMA

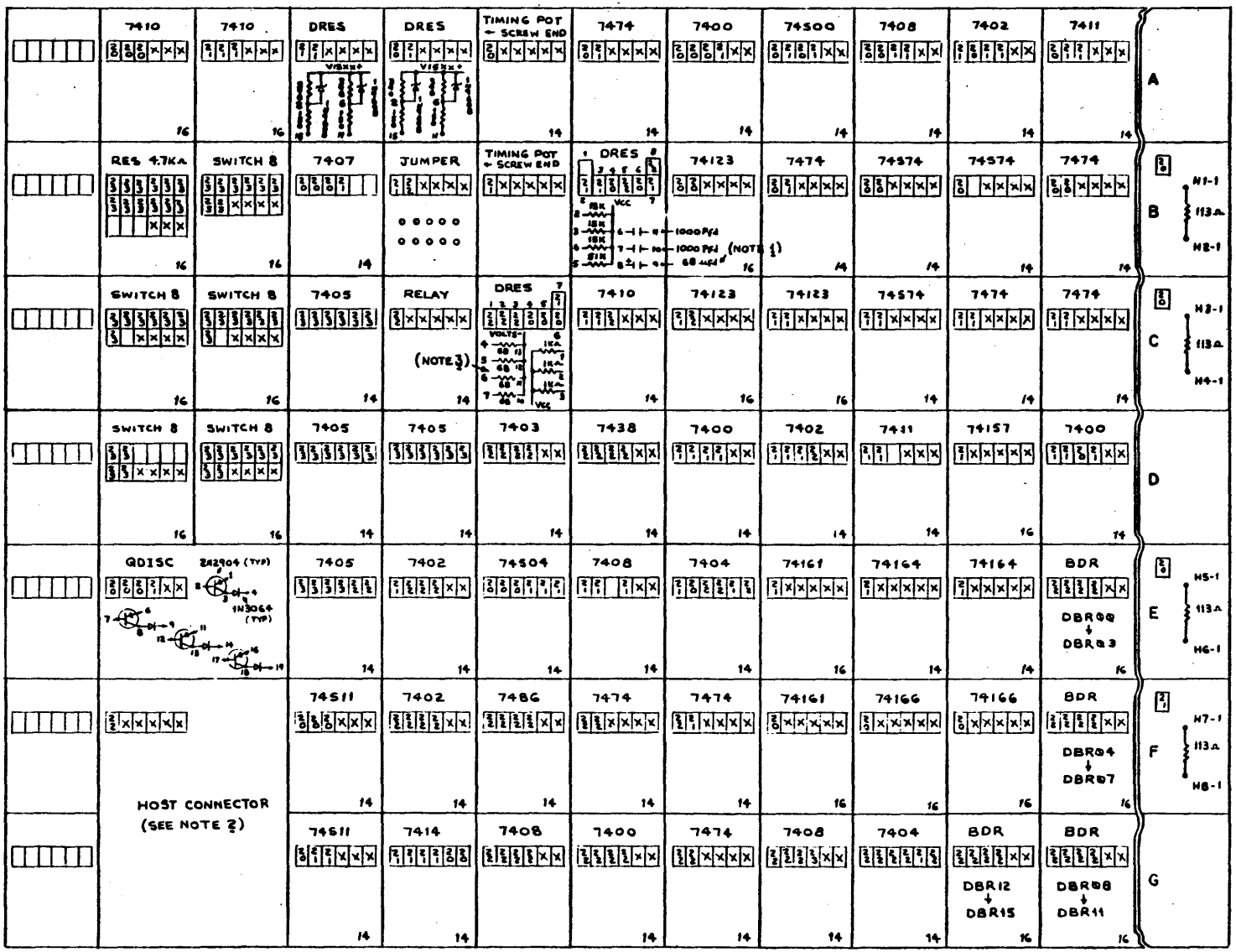
Status - address FXXX6(receive), FXXXC(transmit)



Note: Writing to either status address pokes watchdog timer



HLC-2Ø SCHEMATICS



APPD	REVISION SYM	DESCR	DATE
	A	REL. PROD	5.11.73
	B	ECN #0009	6.27.73
	C	ECN #0046	6.9.74
	D	ECN #0133	3.9.75
	E	ECN #0181	7.22.75
	F	ECN #0159	9/11/75
	G	ECN 0175	11.18.75
	H	ECN 0283	6.2.78

NOTES

1- 68 MFD 6 VOLT SPRAGUE, 196D SERIES.

2- CONNECTOR MFG, SCOTCHFLEX, P-NO. 3429-1002

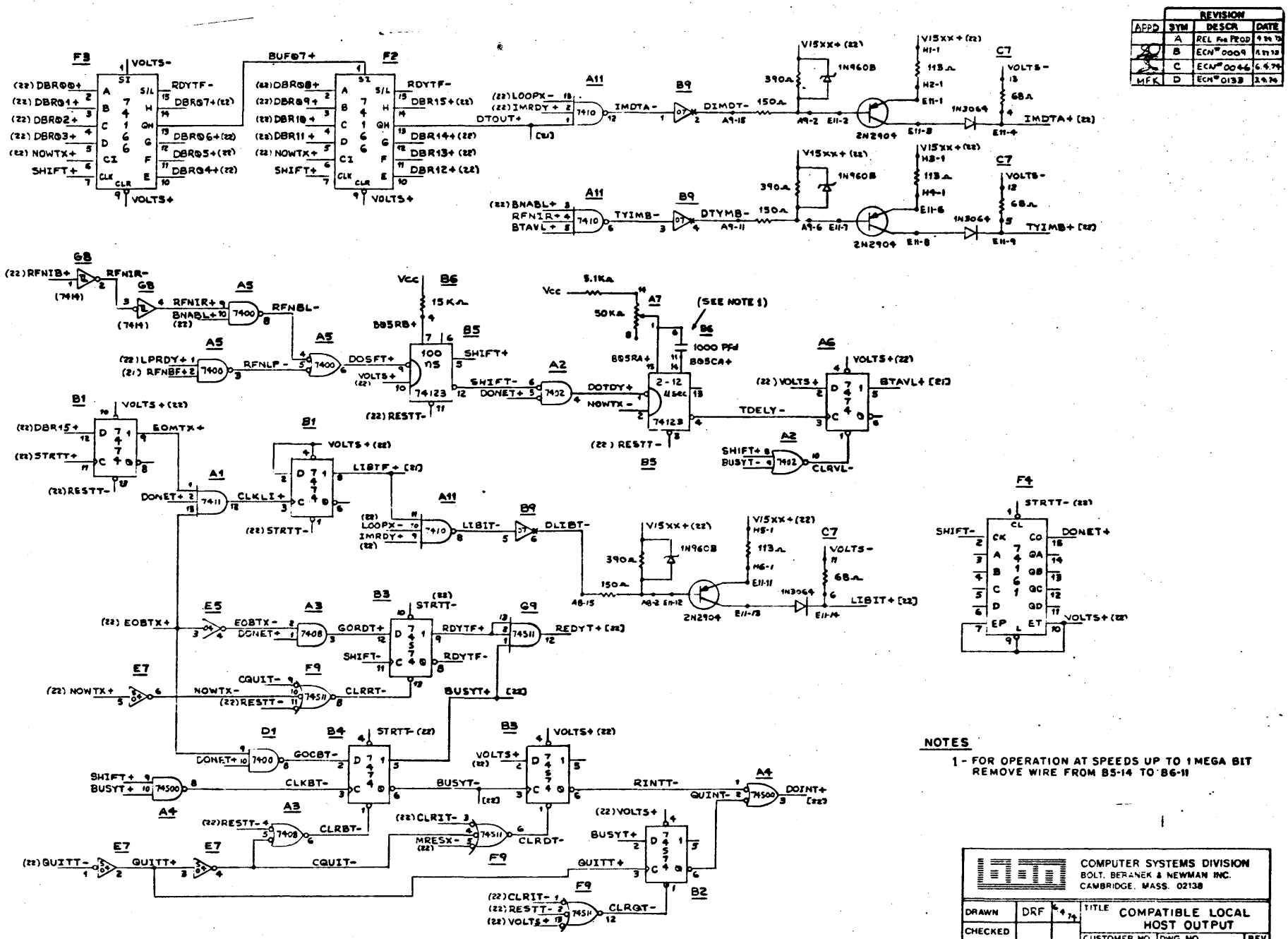
3- IF CARD IS NOT AT END OF DEVICE CABLE, REMOVE VOLTS - FROM ALL 68Ω RESISTORS

TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	6/12/74	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED	DRF	7/12/74	CUSTOMER/NO.	DWG NO. / REV
APPROVED	MJT	8/26/74	HSMIMP	HLC-00-WW / H

HLC



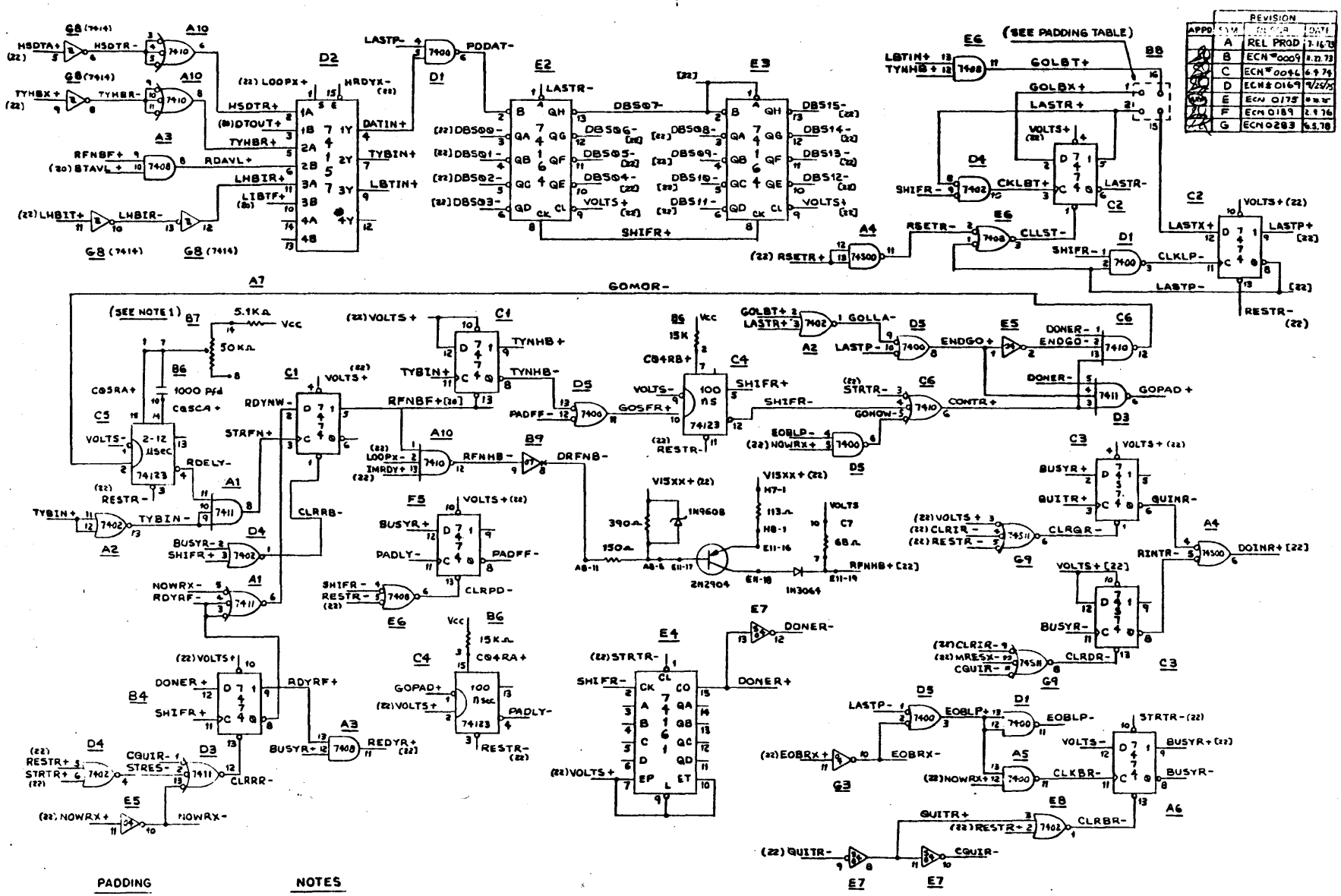
	REVISION		
APPD	SYM	DESCR	DATE
	A	REL FOR PROD	4 29 75
	B	ECN# 0009	6 27 75
	C	ECN# 0046	6.4.76
MFK	D	ECN# 0133	2.9.76

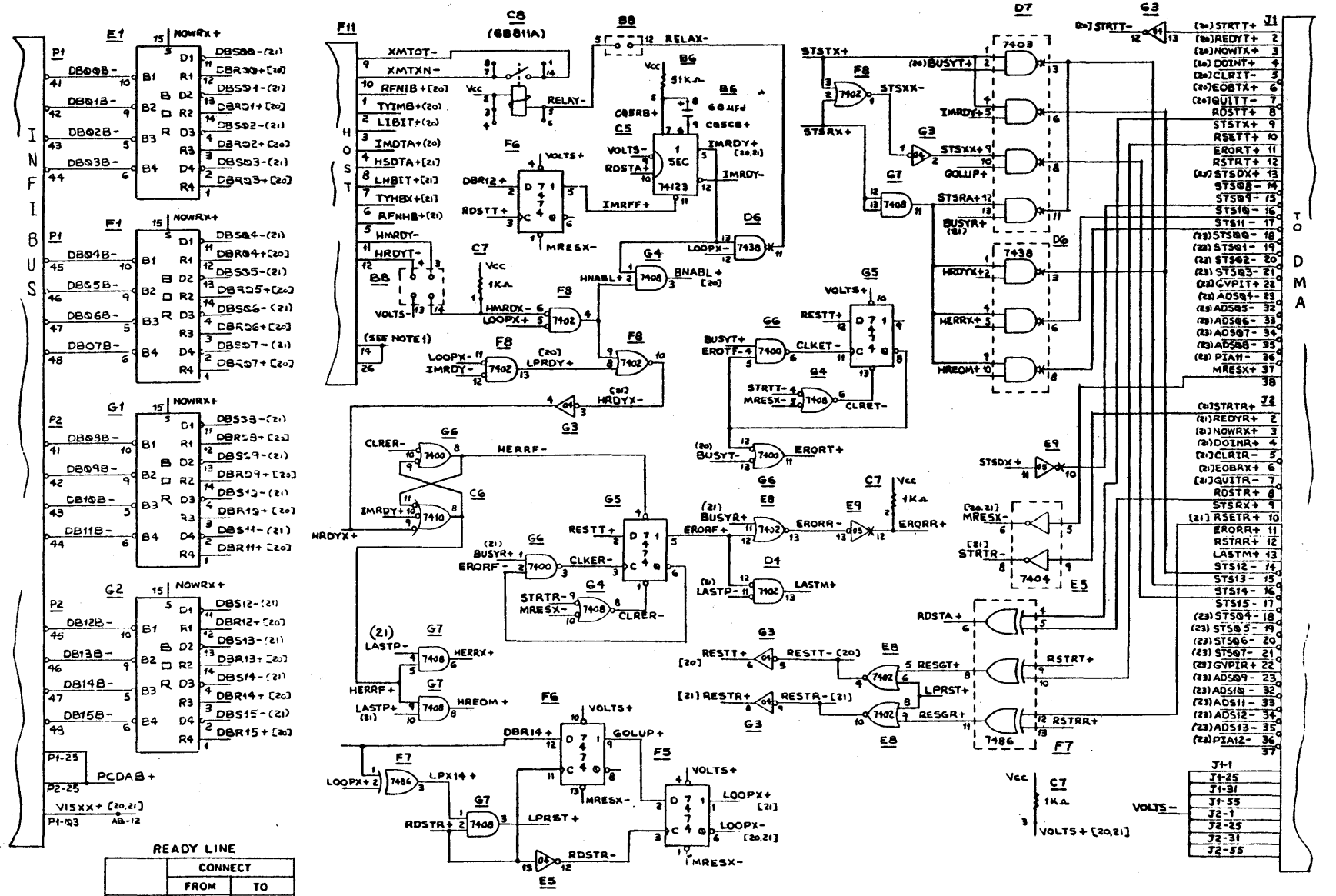
NOTES

1 - FOR OPERATION AT SPEEDS UP TO 1 MEGA BIT REMOVE WIRE FROM B5-14 TO B6-11

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	TITLE	COMPATIBLE LOCAL HOST OUTPUT
CHECKED		CUSTOMER NO.	DWG NO. / REV
APPROVED	MJT	HSMIMP	HLC-20-WW / D


REVISION
APPD
LTR
DESCR
DATE
A REL PROD 7.16.73
B ECN 0009 8.22.73
C ECN 0046 6.9.74
D ECN & 0169 9/25/74
E ECN 0175
F ECN 0189 2.9.76
G ECN 0283 6.3.76
(SEE PADDING TABLE)
GOMOR-
(SEE NOTE 1)
5.1K Ω
50K Ω
1000 pfd
2-12 μSec
74123
100 n S
15K
15K Ω
390 Ω
150 Ω
113 Ω
68 Ω
1N9608
2N2904
1N3064
PADDING
TYPE
CONNECTION
FROM
TO
ONE
B8-1
B8-2
B8-16
B8-15
NO ONE
B8-1
B8-15
B8-2
B8-16
NOTES
1-FOR OPERATION AT SPEEDS UP TO 1 MEGA-BIT REMOVE WIRE FROM C5-14 TO B6-10
DRAWN DRF
CHECKED DRF
APPROVED MT
INPUT
COMPATIBLE LOCAL HOST
HSMIMP HLC-21-WW G
HLC



READY LINE

	CONNECT	
	FROM	TO
ENABLE	88-3	88-14
	88-4	88-13
	88-5	88-12
DISABLE	88-13	88-14

NOTES

1 - NO.14 THRU NO. 26 TIED TO GROUND

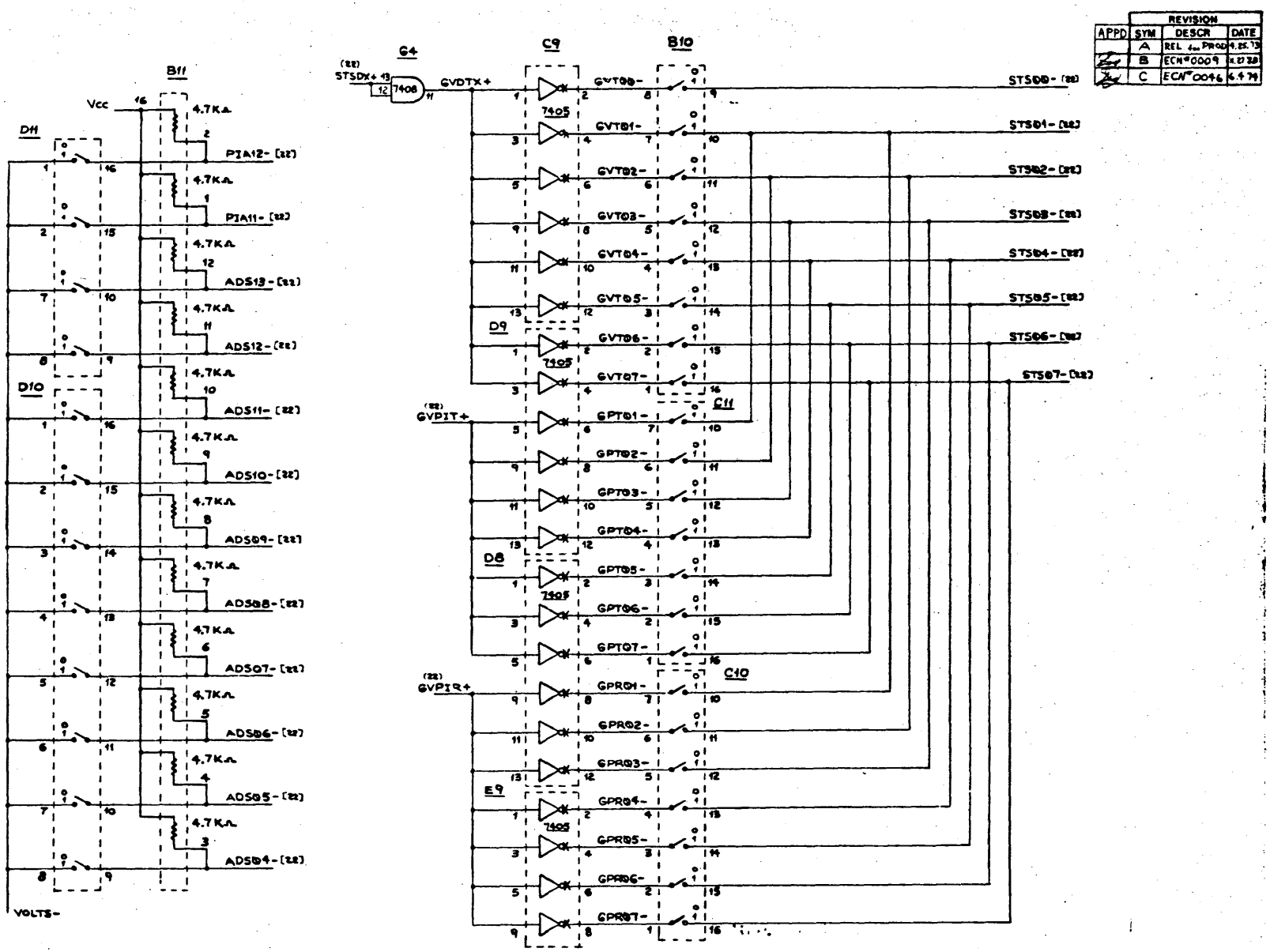
APPD	SYM	DESCRIPTION	DATE
	F	ECN 0189	2.9.76
MFK	E	ECN #0157	7.31.75
	D	ECN #0151	7.15.75
	C	ECN 0046	6.4.74
	B	ECN #0009	8.27.73
	A	REL. PROD	8.16.73

REVISION

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138

DRAWN	DRF	5/10/73
CHECKED	DRF	7/30/73
APPROVED	MJT	8/22/73

TITLE: COMPATIBLE LOCAL HOST STATUS & INTERCONNECTION
DRAWING NO. HSMIMP HLC-22-WW REV F



REVISION			
APPD	SYM	DESCR	DATE
	A	REL 4th PROD	4.25.79
	B	ECN#0009	4.27.79
	C	ECN#0046	6.4.79

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4/25/79	TITLE	SWITCHES COMPATIBLE LOCAL HOST
CHECKED	DRF	5/30/79	CUSTOMER NO.	DWG NO. / REV
APPROVED	HJT	6/28/79	HSMIMP	HLC-23-WW / C

HLC

Host

HST-Ø5 Technical Reference

HST-1Ø Assembly Drawings

HST-15 Standard Mod

HST-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRELIMINARY	7/25/77	
B	ECN 0387	6/11/79	

HST

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN [illegible] 7/25/77

CHECKER

ENGINEER [illegible] 7/25/77

APP'D FOR REL [illegible] 7/25/77

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

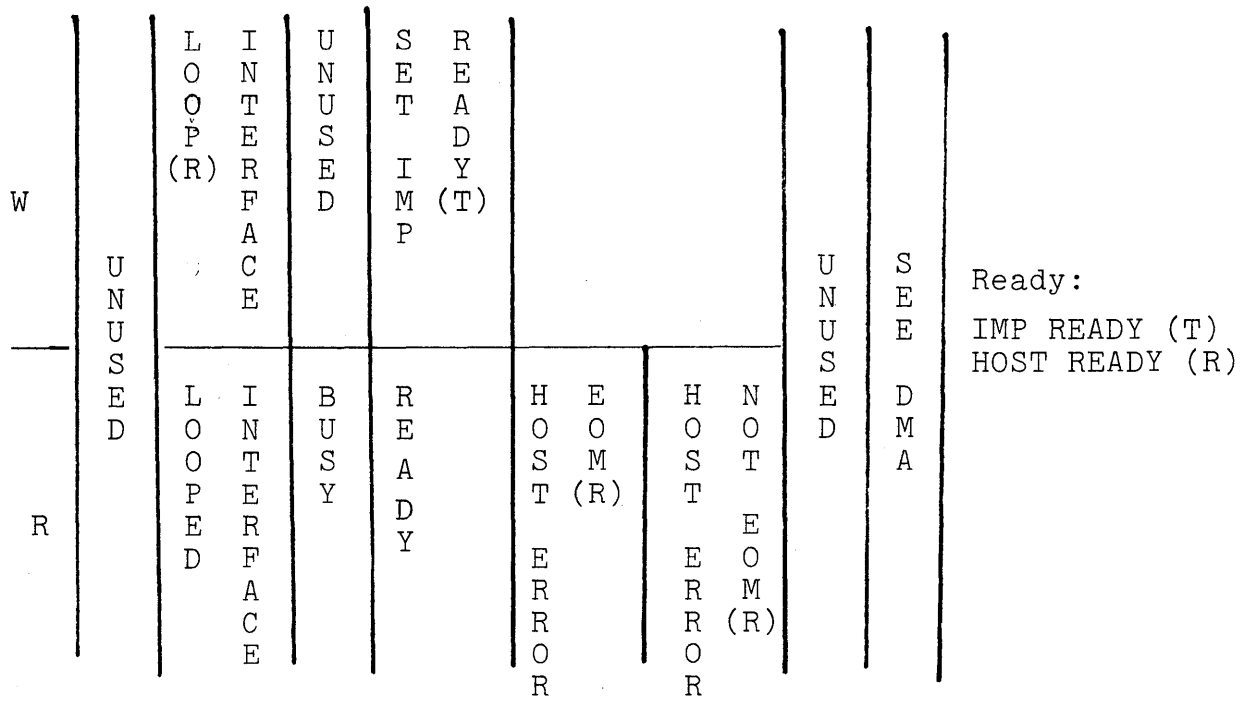
DRAWING TITLE

HST TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		HST-05

see also DMA

Status - address FXXX6(receive), FXXXC(transmit)



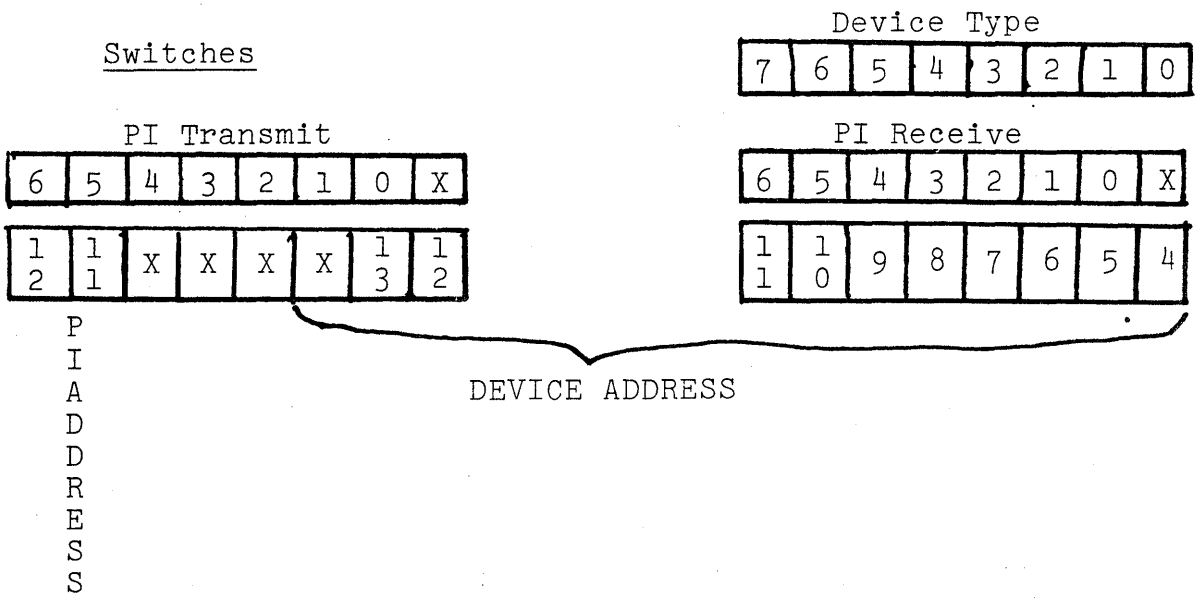
Ready:

IMP READY (T)
HOST READY (R)

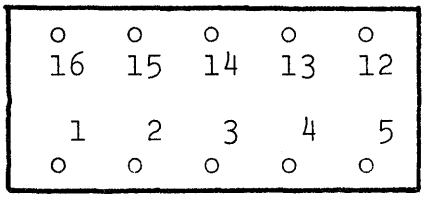
HST

Note: Writing to either status address pokes watchdog timer

Switches



JUMPERS



READY LINE

Type	Connect	
	From	To
ENABLE	3	14
	4	13
	5	12
DISABLE	13	14

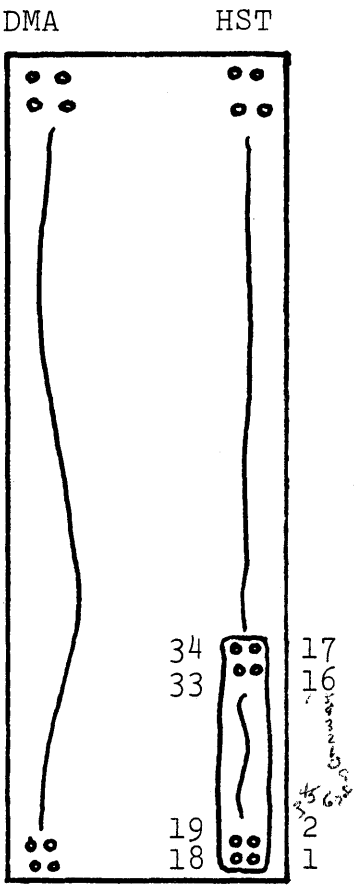
PADDING

Type	Connect	
	From	To
ONE	1	16
	2	15
NO ONE	1	2
	15	16

SPEED (SPEED=)

	High Speed (H)	Low Speed (L)
TRANSMIT	remove .001 µfd capacitor between C10-6 and C10-11	add .001 µfd capacitor between C10-6 and C10-11
RECEIVE	remove .001 µfd capacitor between C10-7 and C10-10	add .001 µfd capacitor between C10-7 and C10-10

LOCAL/DISTANT SOCKET



IDM-H

pin No.

34. IMP ready
31. IMP ready return
13. Host ready
30. Host ready return
12. Ready for next host bit +
29. Ready for next host bit -
11. There's your IMP bit +
28. There's your IMP bit -
10. IMP data +
27. IMP data -
9. Last IMP bit +
26. Last IMP bit -
8. Ready for next IMP bit +
25. Ready for next IMP bit -
7. There's your Host bit +
24. There's your Host bit -
6. Host data +
23. Host data -
5. Last host bit +
22. Last host bit -
4. There's your IMP bit/Local
21. GND
3. Ready for next Host bit/Local
20. GND
2. IMP data/Local
19. GND
1. Last IMP bit/Local
18. GND

HST

RECEIVER OPTION (RCV=) (choose only 1)

LOCAL RECEIVERS (LR)

FROM	TO
J21B	J21C
J22B	J22C
J23B	J23C
J24B	J24C
J21D	J2-51
J22D	J2-52
J23D	J2-53
J24D	J2-54

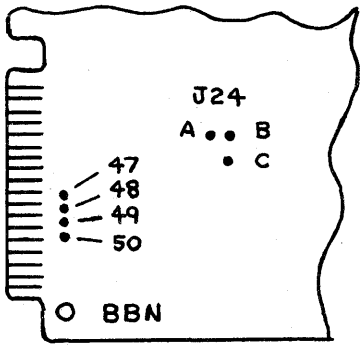
DISTANT RECEIVERS (DR) (*)

FROM	TO
J21B	J21D
J22B	J22D
J23B	J23D
J24B	J24D

* FOR PROTOTYPE BOARDS (6 EXIST)

J21D= 49
J22D= 48
J23D= 50
J24D= 47

} WIRE WRAP PINS ON CARD EDGE



TERMINATION OPTIONS (TERM=)

DISTANT DRIVERS (DD)

FROM	TO
J9A	J9B
J10A	J10B
J11A	J11B
J12A	J12B
J13A	J13B
J14A	J14B
J15A	J15B
J16A	J16B

DISTANT RECEIVERS (DR)

FROM	TO
J5A	J5B
J6A	J6B
J7A	J7B
J8A	J8B
J21A	J21B
J22A	J22B
J23A	J23B
J24A	J24B

LOCAL DRIVERS (LD)

FROM	TO
J17A	J17B
J18A	J18B
J19A	J19B
J20A	J20B

LOCAL RECEIVERS (LR)

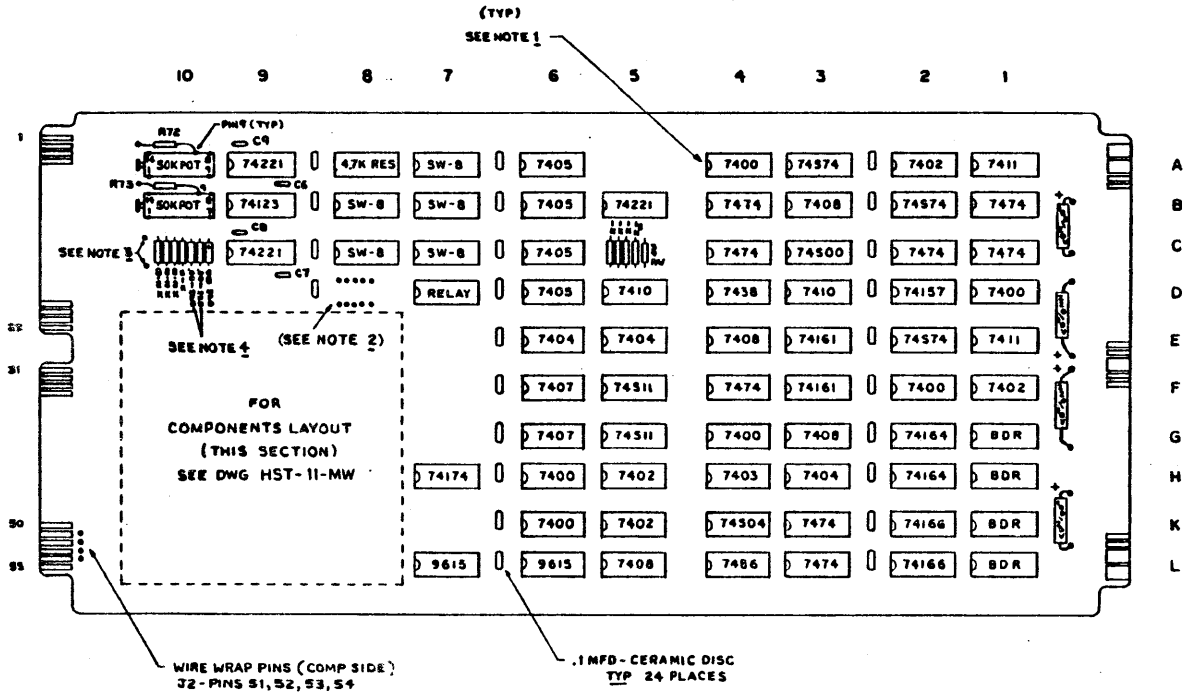
FROM	TO
J5A	J5B
J6A	J6B
J7A	J7B
J8A	J8B

Notes:

1. For 1822 local and distant levels only terminate drivers.
2. For V.35 option terminate both distant drivers and receivers.
3. In all cases, if two HSTs are paired for redundancy, only terminate at most one set of drivers and/or receivers.
4. Local receiver and distant receiver strappings are mutually exclusive.

HST-1Ø ASSEMBLY DRAWINGS

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	9.9.77	
B	ECN 255	1.26.77	MAW
C	ECN 275	4.28.78	"
D	ECN 282	4.28.78	
E	ECN 292	4.27.78	



COMPONENT VALUES

R72 = 3.3 KΩ - 1/4 W
R73 = 5.1 KΩ - 1/4 W
C6,7,8,9 = 18 Pfd

NOTES

1 — NOTCH SHOWN IN BUGS INDICATES INSERTION DIRECTION
2 — WIRE WRAP PINS
3 — LEFT MOST PAIR OF PINS UNUSED
4 — FOR ASSY EASE, MOUNT THESE 2 CAPACITORS DURING BOARD CHECKOUT

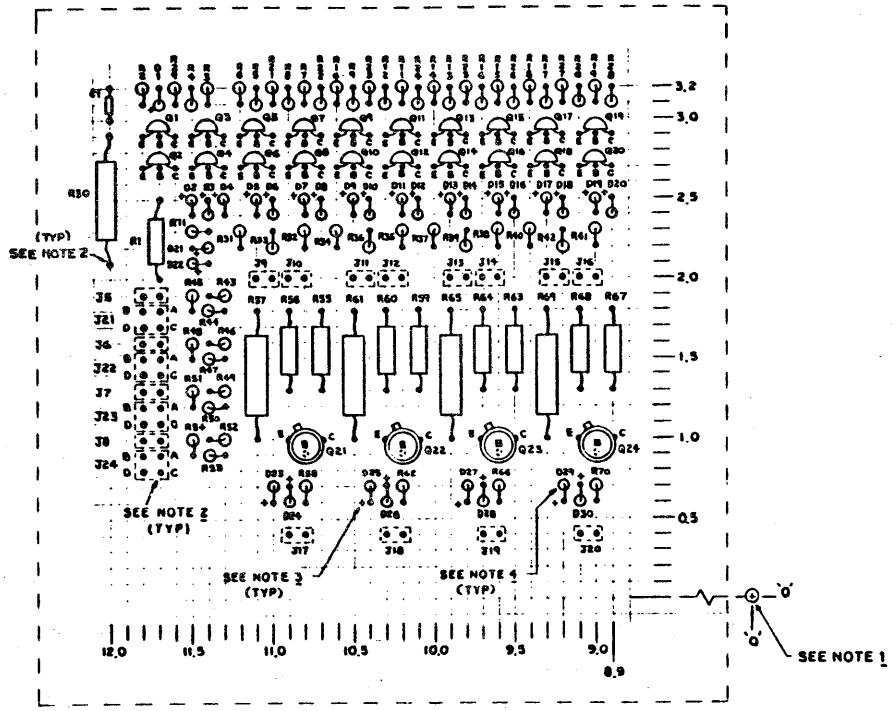
				SIZE
	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC CAMBRIDGE, MASS. 02138			
DRAWN	DRF	9.7.76	TITLE HST MULTI-WIRE LAYOUT	
CHECKED				
ENG APPD	MAW	5/4/77	CODE IDENT NO. DWG NO. HST-10-MW	REV E

HST

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.4.77	
B	ECN 255	7.22.77	
C	ECN 318	8.6.78	

HST CARD LOCATIONS (APPX)

10 9 8



HST DISCRETE COMPONENTS

C1 = 1 MFD

R1 = 3.9KΩ-1/2 W
R2-4,6,8,10,12,14,16,18,20 = 549Ω UNLESS OTHERWISE NOTED
R5,7,9,11,13,15,17,19,21-28 = 274Ω ALL RESISTOR = 1/4 W
R29 = 3.9KΩ
R30 = 390Ω - 1W
R31,32,34,35,37,38,40,41,43,44, 46,47,49,50,52,53 = 300Ω
R33,36,39,42,45,48,51,54 = 121Ω
R55,59,63,67 = 150Ω - 1/2 W
R56,60,64,68 = 390Ω - 1/2 W
R57,61,65,69 = 115 Ω - 1 W
R58,62,66,70 = 68Ω
R71 = 1KΩ

D1 = IN5235B
D2-22,24,26,28,30 = IN3064
D23,25,27,29 = IN960B

Q1,2,4,6,8,10,12,14,16,18,20 = 2N3904
Q3,5,7,9,11,13,15,17,19 = 2N3906
Q21-24 = 2N2904

NOTES

1 - ALL DIMENSIONS ARE IN INCHES, DATUM LINES SCALED FROM ℄ OF TOOLING HOLE (LOCATED IN LOWER RT SIDE OF HST CARD)

2 - WIRE WRAP PINS SYMBOL

3 - DIODES (+) SYMBOL INDICATES: BOTTOM END OR TOPEND AS PER DIODE SYMBOL

4 - MOUNT ALL VERTICALLY MTD DIODES & RESISTORS 1/32" UP OFF BOARD

TOLERANCES UNLESS OTHERWISE SPECIFIED			SIZE
DECIMAL : XX ± .010 .XXX ± .005	BOLT, BERANEK & NEWMAN INC. CAMBRIDGE MASS 02138		
FRACTIONS : ± 1/64			
ANGLES : ± 1°			
MATERIAL :	DRAWN	DRF	5-7-76
	CHECKED		
FINISH :	ENG APPD	MAW	5/4/77

TITLE: COMPONENT SECTION HST MULTI-WIRE LAYOUT

CODE IDENT NO. | DWG NO HST-11-MW | REV C

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED PRODUCTION	5/4/77	
B	ECN 247	5/6/77	MAW
C	ECN 255	7/25/77	MAW
D	ECN 256	8/2/77	MAW
E	ECN 275	11/24/78	[illegible]
F	ECN 282	4/18/78	E.C

HST

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN DRF 5/4/77

CHECKER

ENGINEER MAW

APP'D FOR REL MAW 5/4/77

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

HST STANDARD MOD

SIZE	CODE IDENT NO.	DRAWING NO.
A		HST-15-MW

SCALE	REV F	SHEET 1 OF 5

1. This applies to HST Multiwire Boards whose multiwiring plots (HST-08) are REV. A.

2. Make the following cuts and adds:
(Cuts should be made as shallow as possible, with a small portion of the cut wire removed. Adds should be made on the component side of the board and should be routed under components to secure them. Adds should be terminated by soldering into holes shared by IC leads. See attached diagrams.)

   a. Cuts on component side (before insertion of components):

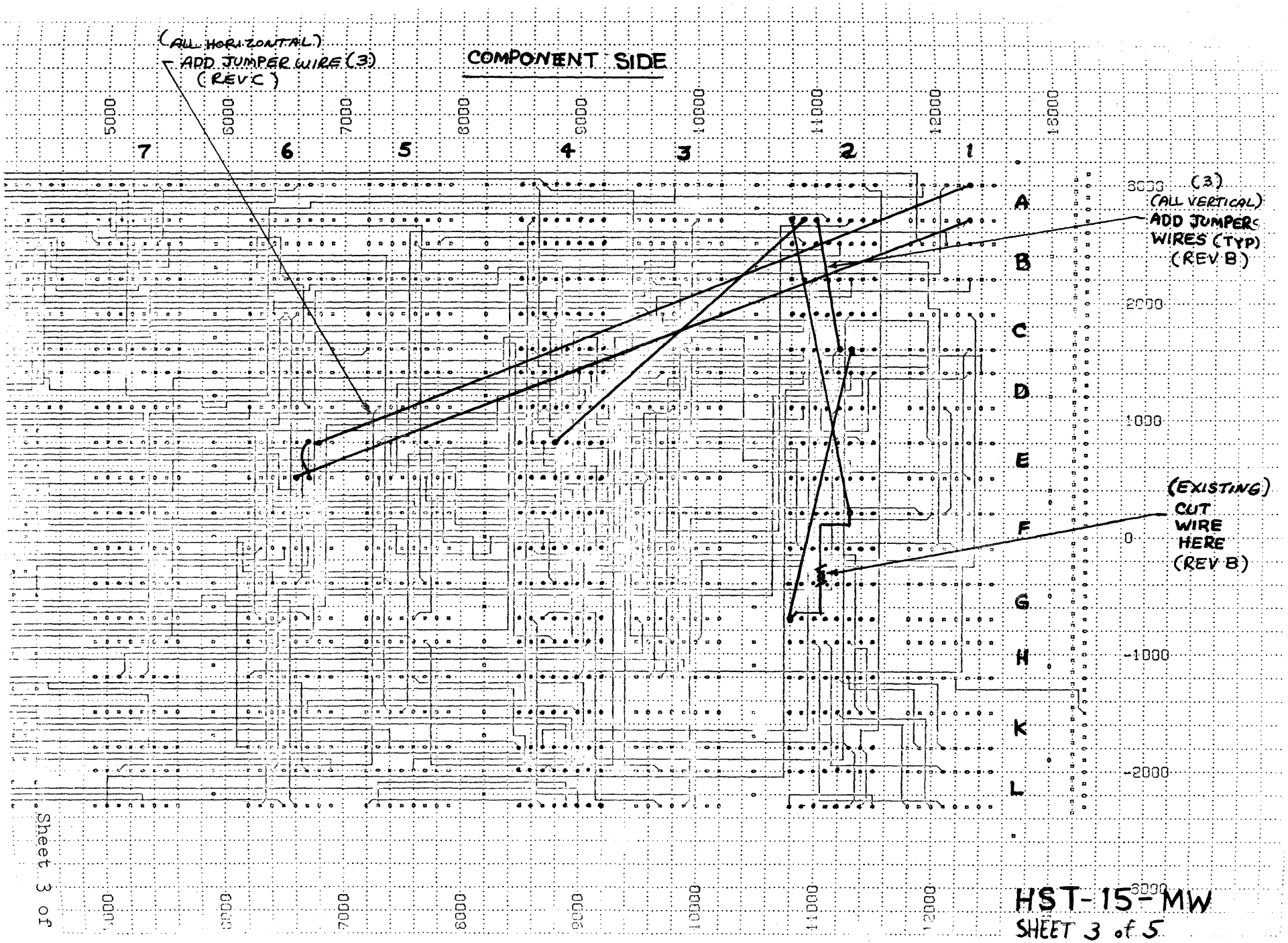
      1) F2:9 → G2:1
      2) L4:6 → B9:10

   b. Cuts on solder side (after soldering):

      1) F2:9 → C2:6
      2) A1:6 → A1:9

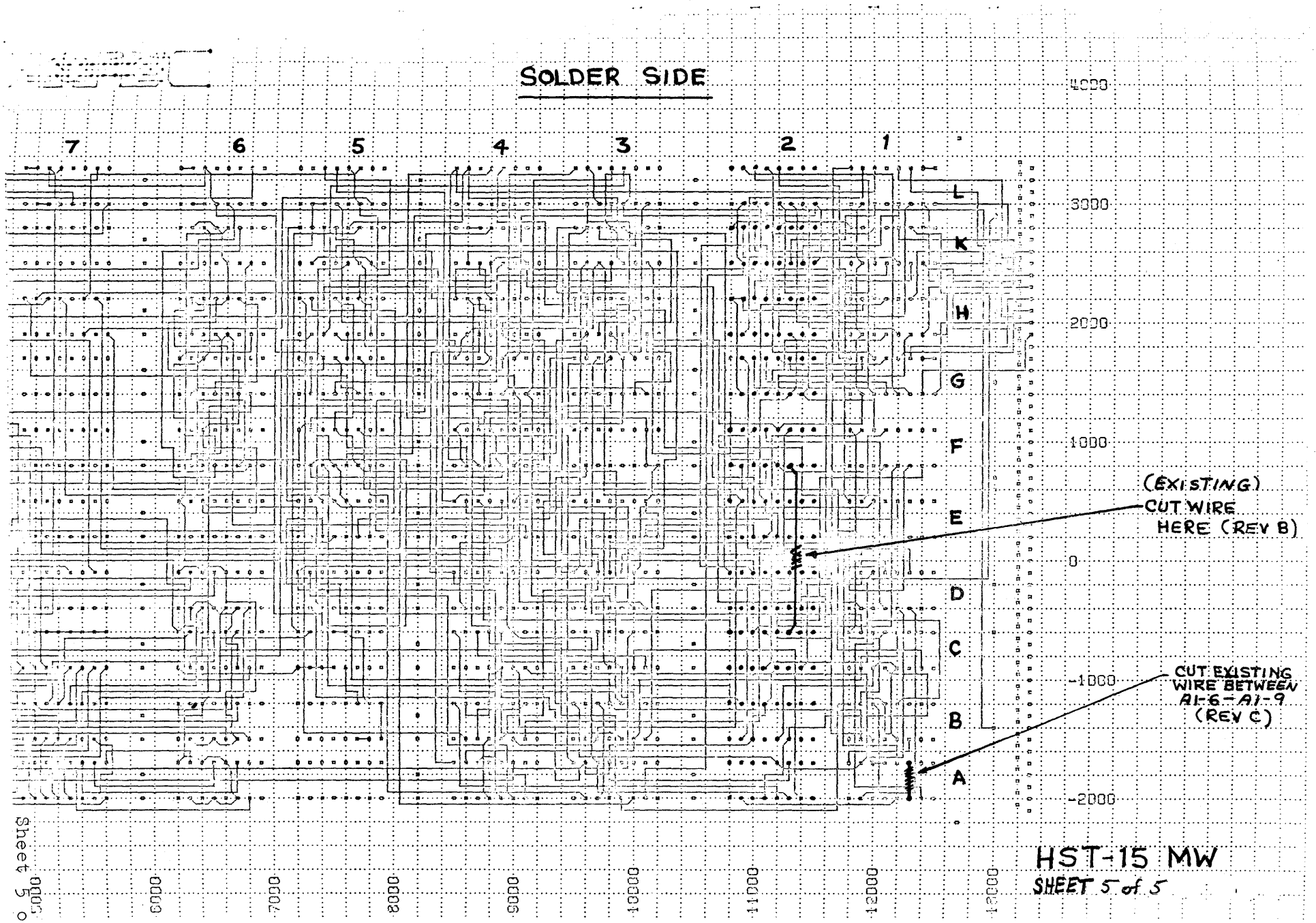
   c. Adds (after soldering):

      1) C2:6 → G2:1
      2) C2:5 → A2:3
      3) A2:1 → F2:9
      4) E4:11 → A2:2
      5) A1:6 → E6:5
      6) E6:6 → E6:9
      7) E6:8 → A1:9
      8) L4:4 → B9:10
      9) A10:9 → A10:14
     10) B10:9 → B10:14

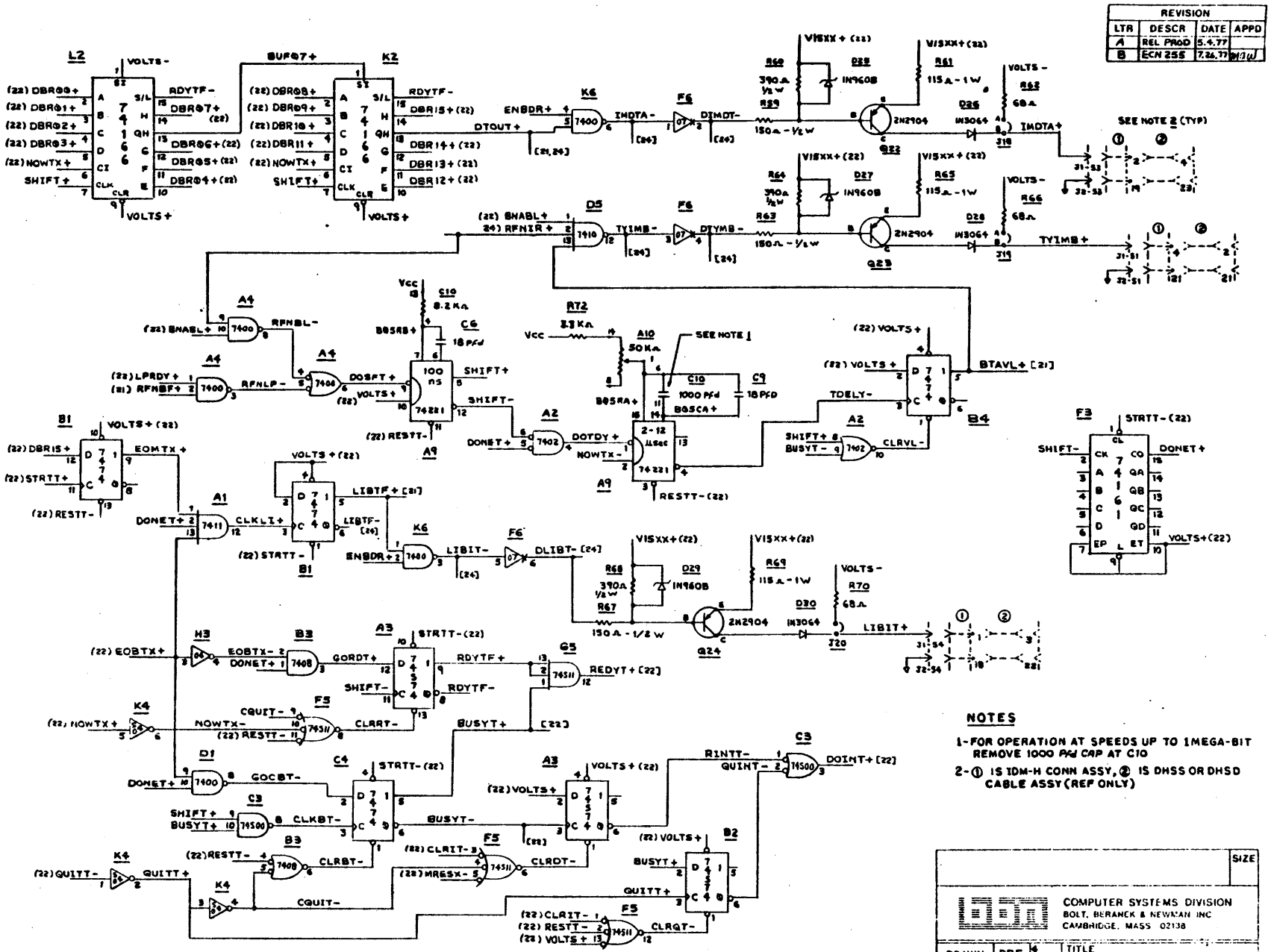

(ALL HORIZONTAL)
ADD JUMPER WIRE (3)
(REV C)
COMPONENT SIDE
5000
6000
7000
8000
9000
10000
11000
12000
13000
7
6
5
4
3
2
1
A
B
C
D
E
F
G
H
K
L
8000
2000
1000
0
-1000
-2000
(3)
(ALL VERTICAL)
ADD JUMPER WIRES (TYP)
(REV B)
(EXISTING)
CUT
WIRE
HERE
(REV B)
HST-15-MW
SHEET 3 of 5

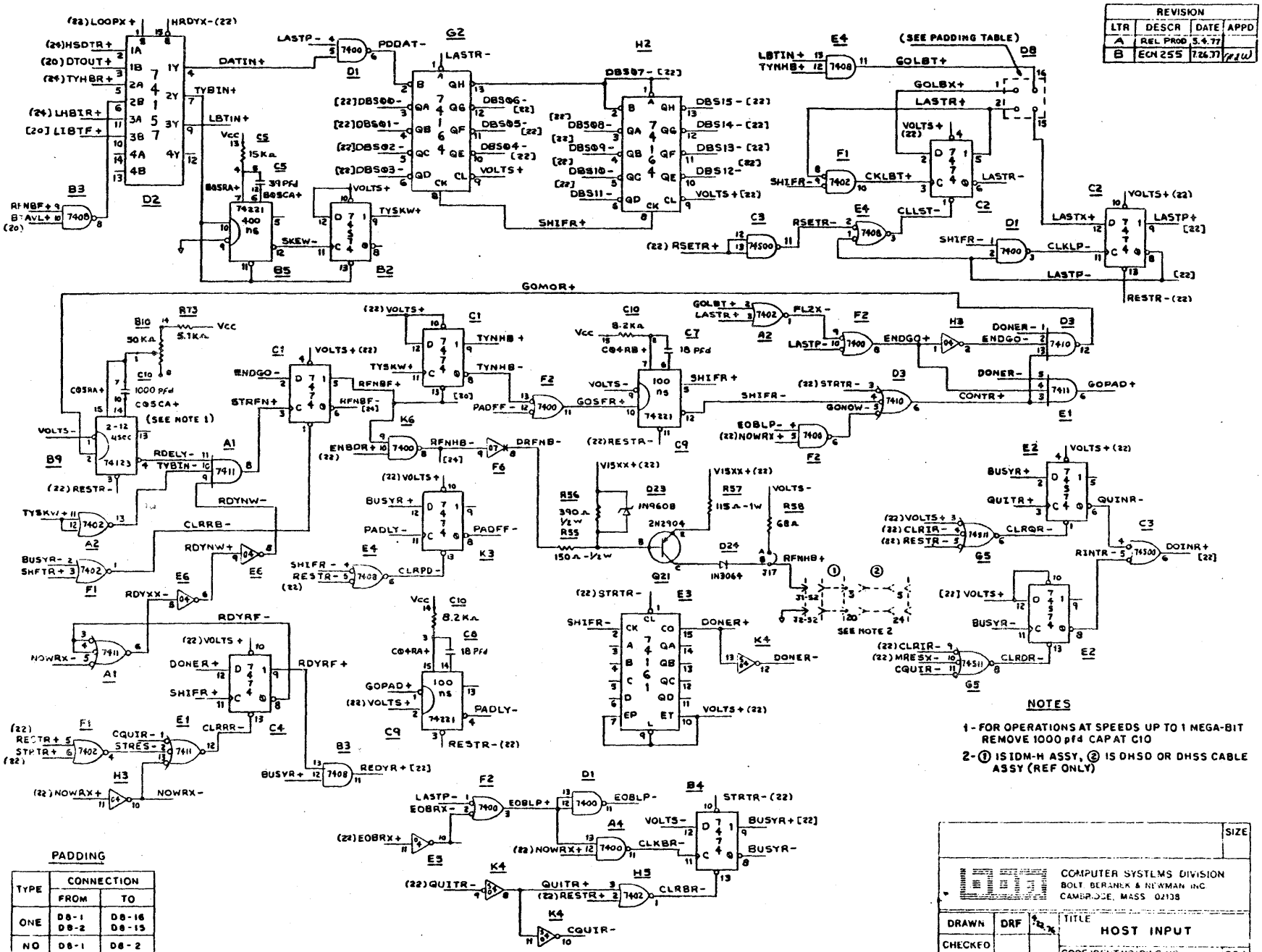
HST-15-MW
SHEET 4 of 5
(COMPONENT SIDE)
ADD JUMPER WIRES (2)
CUT WIRE HERE
ADD JUMPER WIRE
A
B
C
D
E
F
G
H
K
L
1
2
3
4
5
6
7
8
9
10
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

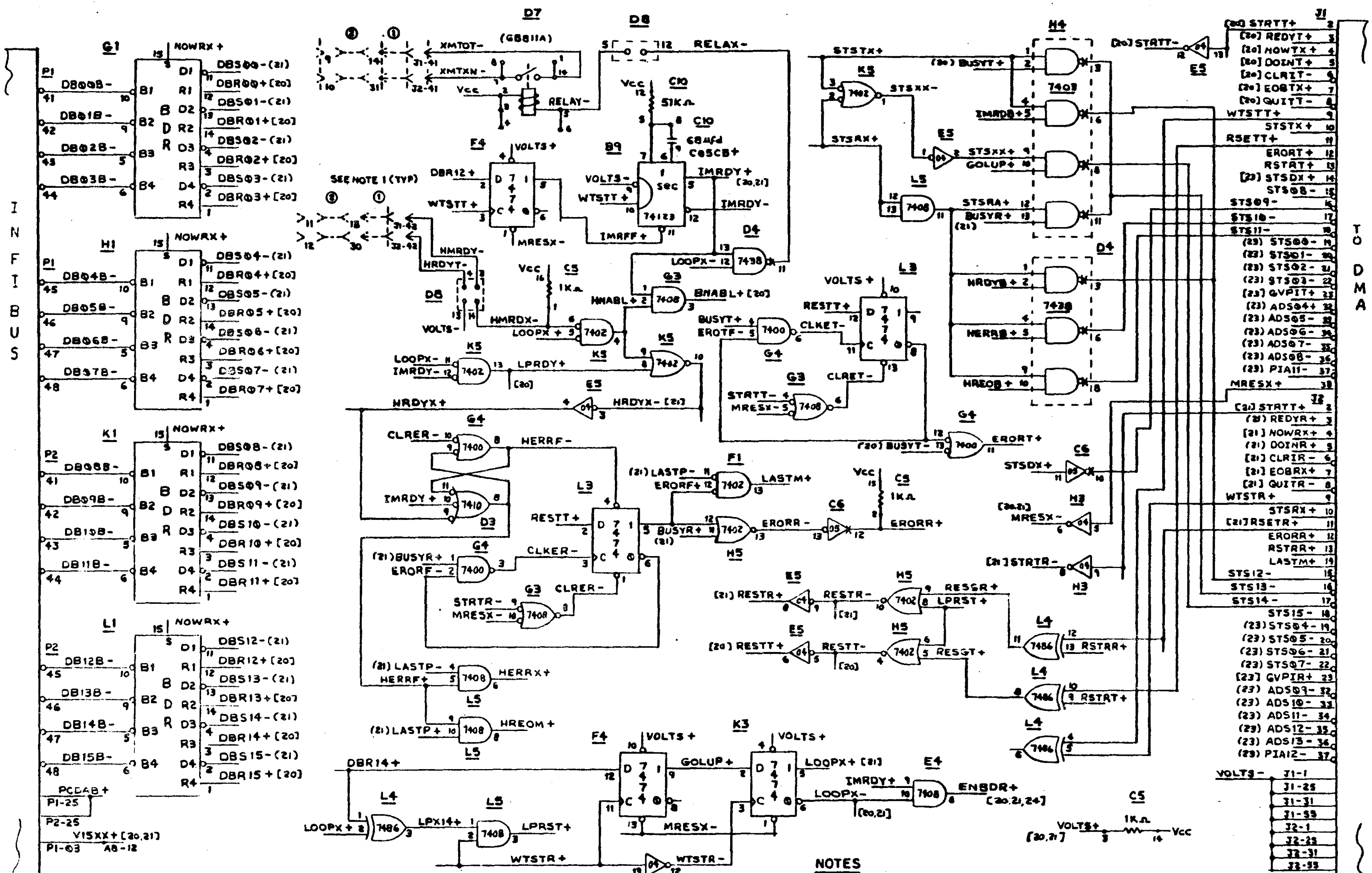
HST


SOLDER SIDE
7
6
5
4
3
2
1
L
K
H
G
F
E
D
C
B
A
4000
3000
2000
1000
0
-1000
-2000
(EXISTING)
CUT WIRE
HERE (REV B)
CUT EXISTING
WIRE BETWEEN
A1-6 - A1-9
(REV C)
6000
7000
8000
9000
10000
11000
12000
13000
HST-15 MW
SHEET 5 of 5

HST-2Ø SCHEMATICS

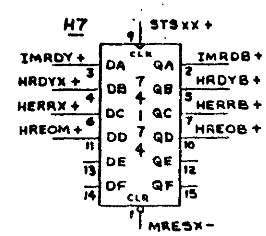

REVISION
LTR | DESCR | DATE | APPD
A | REL PROD | 5.4.77 |
B | ECN 255 | 7.26.77 MAW
NOTES
1-FOR OPERATION AT SPEEDS UP TO 1MEGA-BIT REMOVE 1000 Pfd CAP AT C10
2-① IS 10M-H CONN ASSY, ② IS DHSS OR DHSD CABLE ASSY (REF ONLY)
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN DRF 4.19.76
CHECKED
ENG APPD MAW 5/4/77
TITLE
HOST OUTPUT
CODE IDENT NO
DWG NO. HST-20-MW, B
REV
SIZE
HST


REVISION
LTR | DESCR | DATE | APPD
A | REL PROD | 5.4.77 |
B | ECN 255 | 7.26.77 | RFW
(SEE PADDING TABLE)
GOMOR+
NOTES
1 - FOR OPERATIONS AT SPEEDS UP TO 1 MEGA-BIT REMOVE 1000 pfd CAP AT C10
2 - ① IS IDM-H ASSY, ② IS DHSD OR DHSS CABLE ASSY (REF ONLY)
PADDING
TYPE | CONNECTION | FROM | TO
ONE | D8-1 | D8-16
D8-2 | D8-15
NO ONE | D8-1 | D8-2
D8-15 | D8-16
SIZE
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN | DRF | 5/4/77
CHECKED
ENG APPD | MAW | 5/4/77
TITLE
HOST INPUT
CODE IDENT NO. DWG NO. REV
HST-21-MW B



NOTES

1- ① IS IDM-H CONN ASSY, ② IS DHSD OR DHSS CABLE ASSY (REF ONLY)



READY LINE

	CONNECT FROM	CONNECT TO
ENABLE	D8-3	D8-14
	D8-4	D8-13
	D8-5	D8-12
DISABLE	D8-13	D8-14

LTR	DESCR	DATE	APPD
B	ECN 256	8/1/77	
A	REL PROD	5.4.77	

REVISION

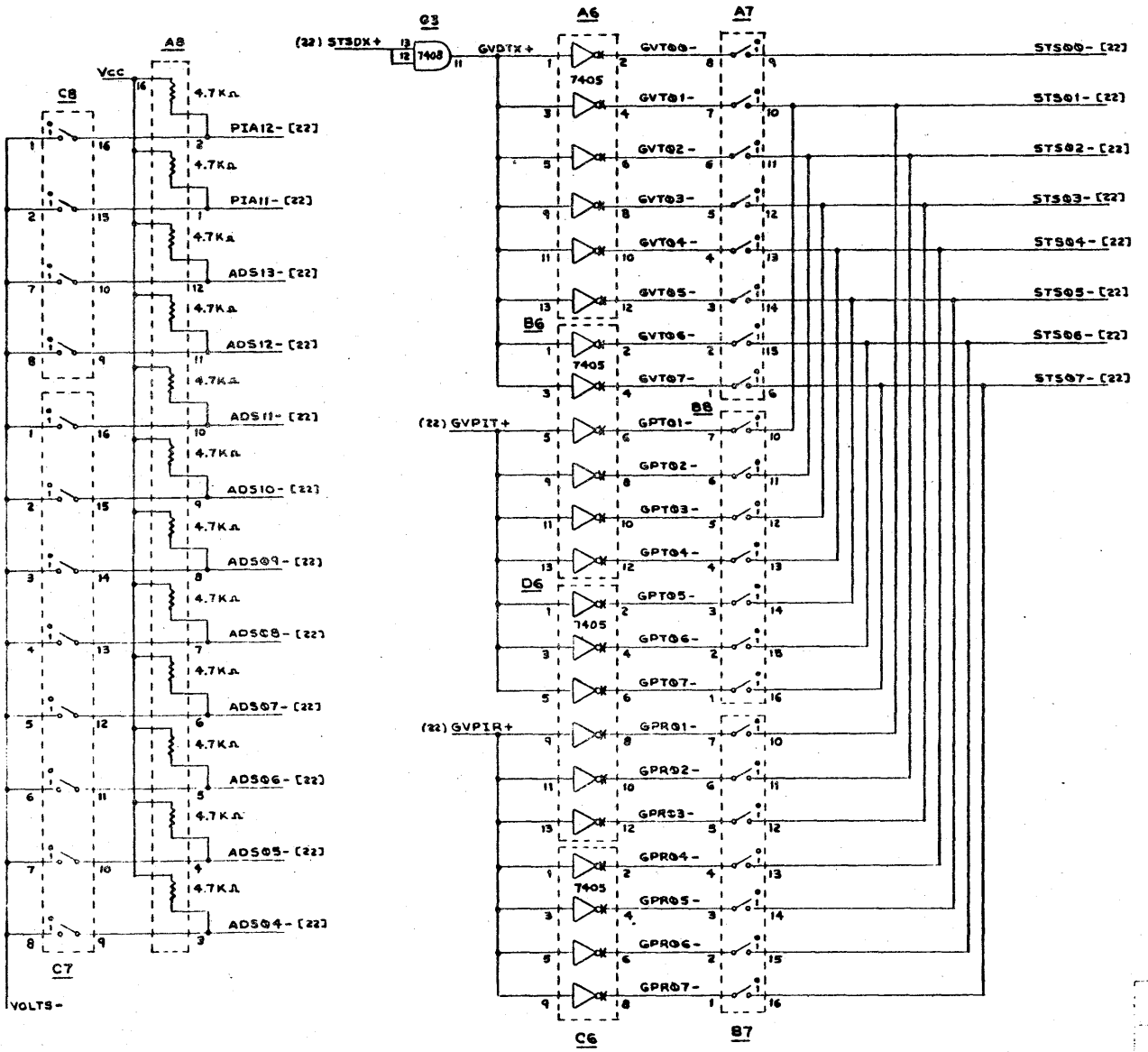
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	4.27.76	TITLE HOST STATUS & INTERCONNECTION
CHECKED			
ENG APPD	MAW	5/4/77	CODE IDENT NO. DWG NO HST-22-MW REV B

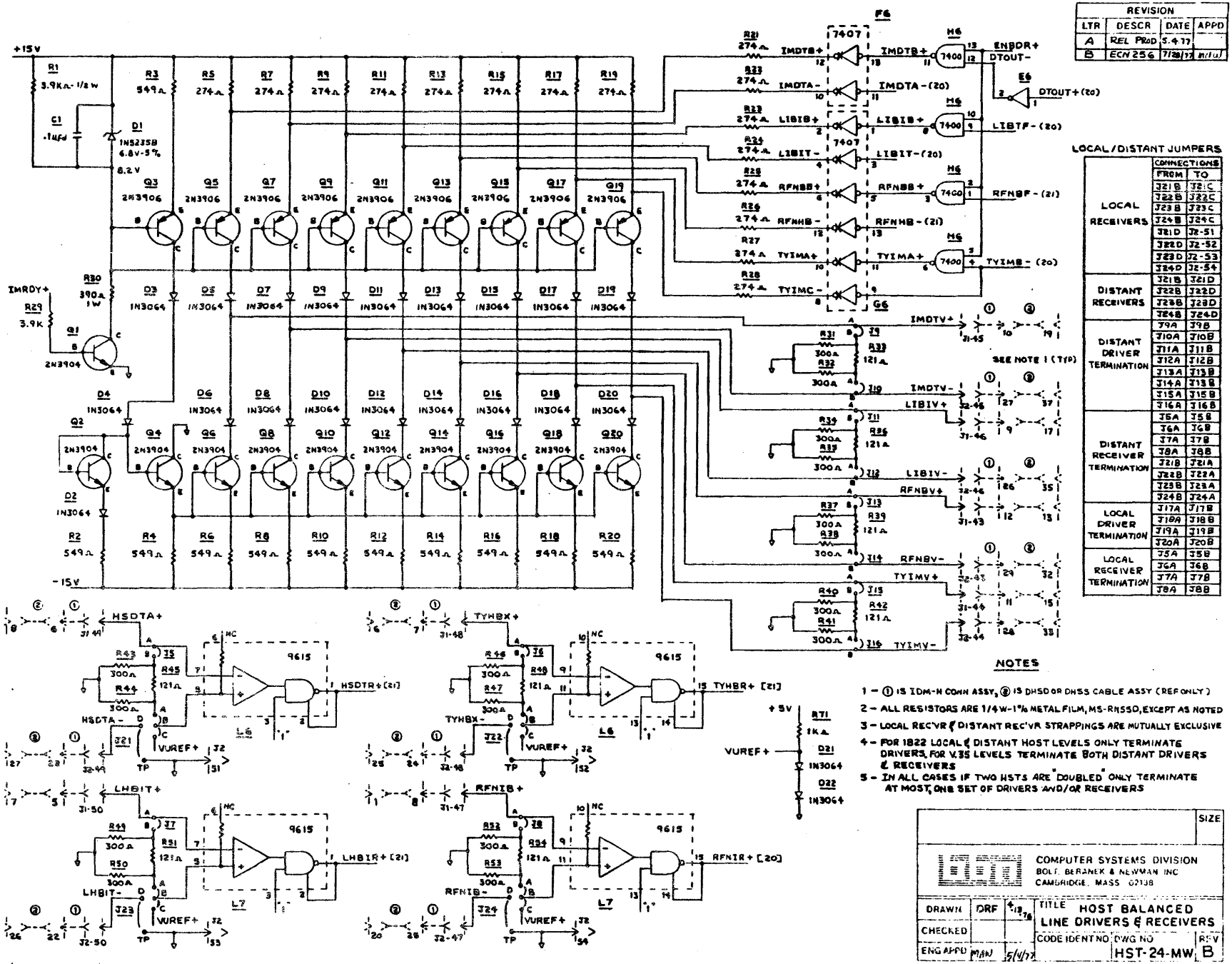
SIZE

HST

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.4.77	



			SIZE
COMPUTER SYSTEMS DIVISION BOLT BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	2/16	TITLE: HOST SWITCHES
CHECKED			
ENG APPD	MAJ	5/4/77	CODE IDENT NO. DWG NO. HST-23-MW REV A



LOCAL/DISTANT JUMPERS

	CONNECTIONS FROM	TO
LOCAL RECEIVERS	J21B	J21C
	J22B	J22C
	J23B	J23C
	J24B	J24C
	J21D	J2-51
	J22D	J2-52
	J23D	J2-53
	J24D	J2-54
DISTANT RECEIVERS	J21B	J21D
	J22B	J22D
	J23B	J23D
	J24B	J24D
DISTANT DRIVER TERMINATION	J9A	J9B
	J10A	J10B
	J11A	J11B
	J12A	J12B
	J13A	J13B
	J14A	J14B
	J15A	J15B
	J16A	J16B
DISTANT RECEIVER TERMINATION	J5A	J5B
	J6A	J6B
	J7A	J7B
	J8A	J8B
	J21B	J21A
	J22B	J22A
	J23B	J23A
	J24B	J24A
LOCAL DRIVER TERMINATION	J17A	J17B
	J18A	J18B
	J19A	J19B
	J20A	J20B
LOCAL RECEIVER TERMINATION	J5A	J5B
	J6A	J6B
	J7A	J7B
	J8A	J8B

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5-4-77	
B	ECN 256	7/28/77	mlw

NOTES

1 – ① IS IDM-H CONN ASSY, ② IS DHSD OR DHSS CABLE ASSY (REF ONLY)
2 – ALL RESISTORS ARE 1/4W-1% METAL FILM, MS-RN55D, EXCEPT AS NOTED
3 – LOCAL REC'VR & DISTANT REC'VR STRAPPINGS ARE MUTUALLY EXCLUSIVE
4 – FOR 1822 LOCAL & DISTANT HOST LEVELS ONLY TERMINATE DRIVERS, FOR V.35 LEVELS TERMINATE BOTH DISTANT DRIVERS & RECEIVERS
5 – IN ALL CASES IF TWO HSTS ARE "DOUBLED" ONLY TERMINATE AT MOST, ONE SET OF DRIVERS AND/OR RECEIVERS

			SIZE
BBN	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC CAMBRIDGE, MASS 02138		
DRAWN	DRF	4/18/76	TITLE HOST BALANCED LINE DRIVERS & RECEIVERS
CHECKED			CODE IDENT NO DWG NO HST-24-MW REV B
ENG APPD	MAW	5/4/77	

HST

Interface Level Converters

ILC-Ø2 Logic Description

ILC-2Ø Schematics & Assembly Drawings

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	9/15/77	JAT
B	ECN 268	5/18/78	JAT

ILC

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN LJF

CHECKER AT 8/15/77

ENGINEER AT 9/15/77

APP'D FOR REL Frank 11/15/77

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

ILC LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		ILC-02

SCALE | REV B | SHEET 1 OF 4

INTERFACE LEVEL CONVERTERS

The Interface Level Converters change output and input voltage levels from the Pluribus MLR card (Pluribus Modem Interface) to various electrical protocols. The level converters are designed to be connected in parallel as part of the Pluribus philosophy of redundant abilities.

This document is a detailed description of the operation of the ILC.

OPERATION OF THE ILC

The ILC receives two signals from the MLR card (TData and TLoop) and sends three signals to the MLR card (TClk, RData, and RClk). We shall examine the received signals first.

TDATA- This signal is received on the ILC card by an 8T14 line receiver integrated circuit. The output of the chip feeds a 74123 retriggerable monostable multivibrator (a watchdog timer for the card) and a 75452 dual peripheral driver integrated circuit. The watchdog timer has a time period of about 0.3 seconds during which it must be retriggered by arriving data or syn characters. If no characters arrive, it will shut off the outputs of the ILC.

During the normal case, the data going into the 75452 is inverted on one channel, introducing a worst case 22 nanosecond skew- a negligible amount on a worst case data bit of 667 nanoseconds at a transmission rate of 1.5 megabits per second.

Data then enters the discrete current driver section of the ILC. The current driver can be examined for a typical case by following data flow from one half of the 75452 with the card configured for the MIL-188-100 case. A positive signal at an input of the 75452 turns on its internal transistor causing the two resistors between the collector and +15 volts to become a voltage divider. The drop in voltage to +8.6 volts at the base of the 2N2905 transistor forces it on. This causes a 10 milliamp current through the emitter and places +9.3 volts at the base of the second 2N2905 and -8.6 volts at the base of the 2N2219 transistor. Both of these transistors turn on, forcing a 50 milliamp current through the 100 ohm load and establishing a 5 volt potential across it. By removing transistors or using different values for resistors, several different electrical protocols can be generated.

When the data entering the 75452 is a low signal, the first gate is turned off and the second half of the ILC is activated. This causes a reversal of current flow and the opposite potential to form at the load.

TLOOP-This received signal goes through an identical circuit to TDATA except that it does not poke the watchdog timer.

TCLK, RCLK, and RDATA- These signals are all sent to the MLR card from the ILC via 8T13 drivers. The 75107B receivers and the 8T16 receivers can be configured to meet different protocols in conjunction with the optional termination resistors on the card.

OUTPUT CONNECTORS

The output connector on the front panel of the ILC will vary according to different customer's needs. Currently documented are an ITT CANNON GK-12-32SL for NSA and a CINCH DB-25P for the RS-232 protocol.

SINGLE ILC

In the case of a nonredundant Pluribus system, a single ILC would be used for level conversion. All the termination resistors would then be mounted on the circuit card in the forked turrets provided.

DOUBLE ILC

Two ILC's can be connected in parallel for redundancy. To accomplish this while maintaining the integrity of the transmission line required two features. First, the differential drivers were chosen to be current drivers to present a high-impedance load on the transmission line when not active or powered down.

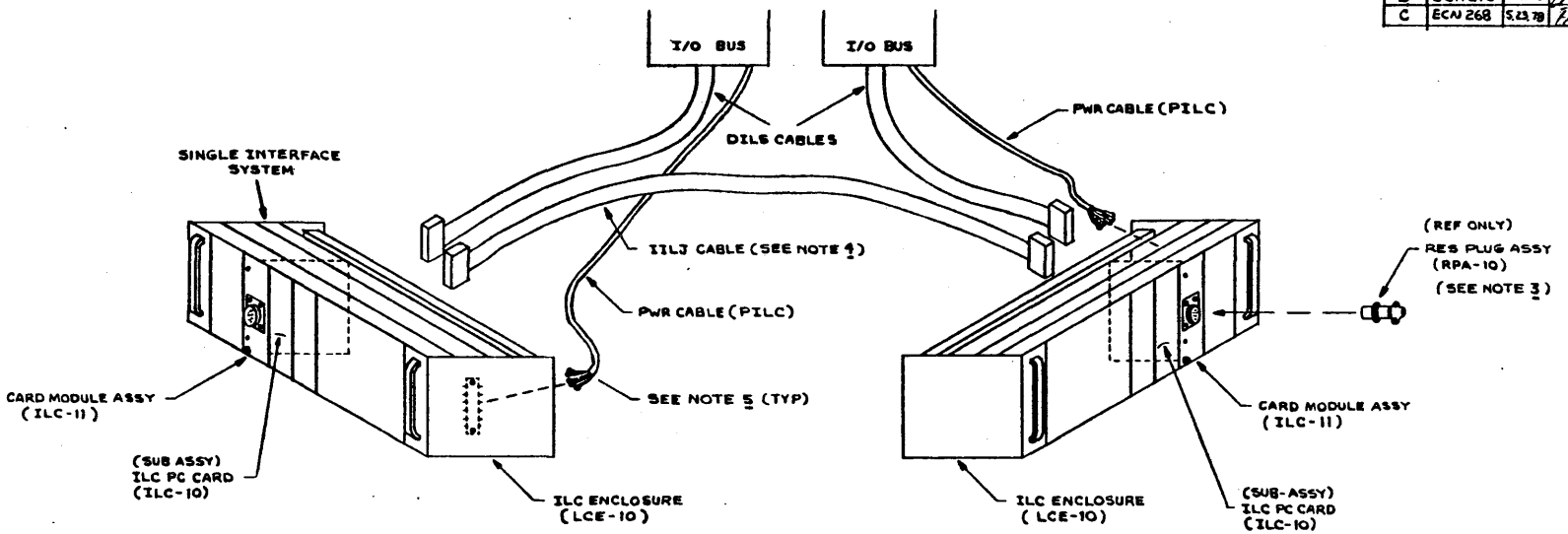
Second, the driver and receiver terminating resistors were placed on a moveable resistor plug to force termination at the end of the transmission line.

All differential signals passing through the Cannon plug are present on both ILC cards at all times. The choice of which ILC is active is handled by the Pluribus computer by which I/O interface is being used.

ILC

ILC-2Ø Schematics & Assembly Drawings

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	8.18.77	
B	ECN 273	4.9.78	
C	ECN 268	5.23.78	



DOUBLE INTERFACES SYSTEM

NOTES

1 - A DOUBLE INTERFACES SYSTEM CONSISTS OF; 2-ILC ENCLOSURES (LCE-10) 2-PWR CABLES(PILC), 1-IILJ CABLE & 2-DILS CABLES [FOR EACH TWO CARD MODULE ASSY (ILC-11) USED]

2 - A ILC ENCLOSURE (LCE-10) CAN ACCOMODATE 1-8 CARD MODULE ASSY. CARD MODULE ASSY'S LOCATIONS (LESS THEN 8) OPTIONAL

3 - ON DOUBLE INTERFACES SYSTEM, INSERT RESISTOR PLUG ASSY(RPA-10 ; INTO CARD MODULULE ASSY(S) NOT USED AS OUTPUT(S) [ONLY ONE OF TWO PARALLELED OUTPUT PLUGS MAY BE USED FOR OUTPUT ON DOUBLE INTERFACES SYSTEM, OTHERS MUST HAVE RESISTOR PLUG ASSY]

4 - DILS CABLE PLUGS INTO TOP & IILJ CABLE PLUGS INTO BOTTOM OF EACH CARD MODULE'S EDGE CONN USED. (SEE DWG LCE-10)

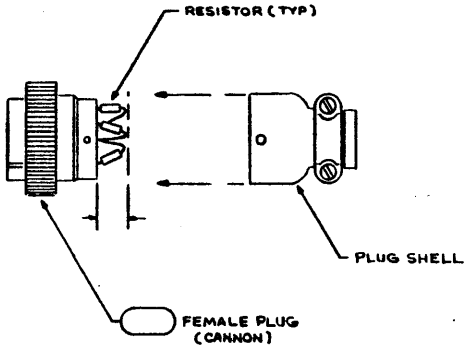
5 - POWER CABLE (S) RING LUGS , CONNECT TO TERMINAL BKT, MOUNTED ON INSIDE OF ILC ENCLOSURE END PLATE

INTERFACE LEVEL CONVERTER			SIZE
COMPUTER SYSTEMS DIVISION BOLT BERANEK & NEWMAN INC CAMBRIDGE, MASS 02138			
DRAWN	DRF	7/5/77	TITLE: DOUBLE SYSTEM LAYOUT
CHECKED	AT	8/10/77	
ENG APPD	AT	8/12/77	CODE IDENT NO. / DWG NO. DLC-09 / REV C

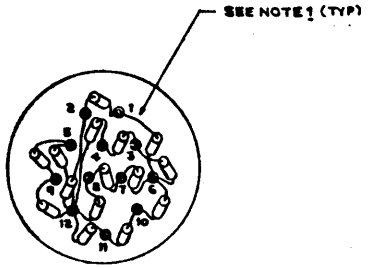
ILC

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	8.18.77	
B	ECN 268	5.25.78	

SCALE = 1:1



PLUG, BACK VIEW
(UNASSEMBLED)



NOT TO SCALE

WIRING TABLE				
RES	PIN		PIN	BBN NO
110Ω	1		2	1127
270Ω	1		6	856
270Ω	2		12	856
110Ω	3		4	1127
270Ω	3		6	856
270Ω	4		12	856
120Ω	5		9	344
270Ω	5		12	856
270Ω	6		7	856
270Ω	6		10	856
120Ω	7		8	344
270Ω	8		12	856
270Ω	9		12	856
120Ω	10		11	344
270Ω	11		12	856

NOTES

1 - RESISTOR LEADS MUST NOT TOUCH CONNECTOR SHELL OR OTHER RESISTOR LEADS.

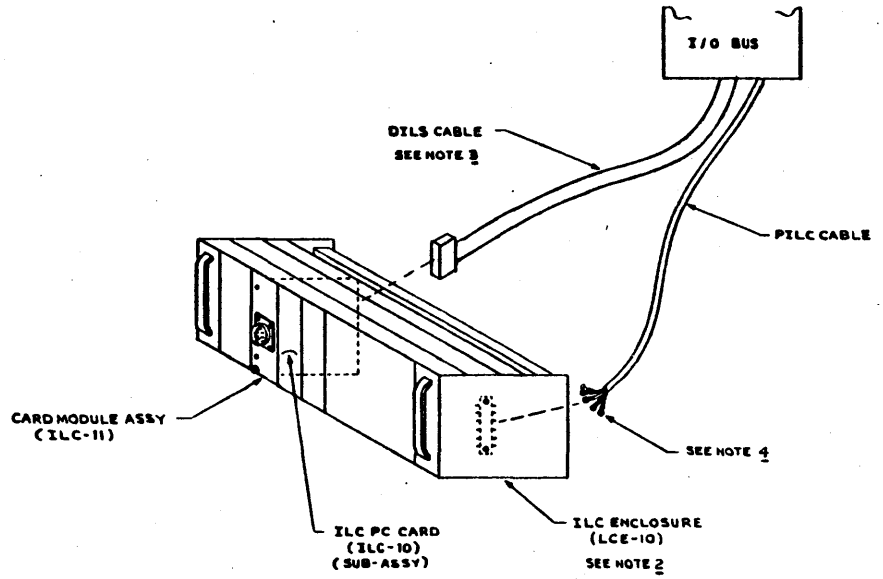
INTERFACE LEVEL CONVERTER

SIZE

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8.8.77	TITLE: RESISTOR PLUG ASSY
CHECKED	AT	8.8.77	
ENG APPD	AT	8.8.77	CODE IDENT NO. / DWG NO. RPA-10 / REV B

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.17.78	



NOTES

1 - A SINGLE INTERFACE SYSTEM CONSISTS OF; 1 ILC ENCLOSURE (LCE-10), 1 PWR CABLE(PILC), 1 DILS CABLE [FOR EACH CARD MODULE ASSY (ILC-11) USED]

2 - A ILC ENCLOSURE (LCE-10) CAN ACCOMODATE FROM 1 TO 8 CARD MODULE ASSY'S CARD MODULE ASSY'S LOCATIONS (IF LESS THEN 8) OPTIONAL

3 - DILS CABLE(S) PLUGS INTO TOP HALF OF EACH CARD MODULES EDGE CONN USED (SEE LCE-10)

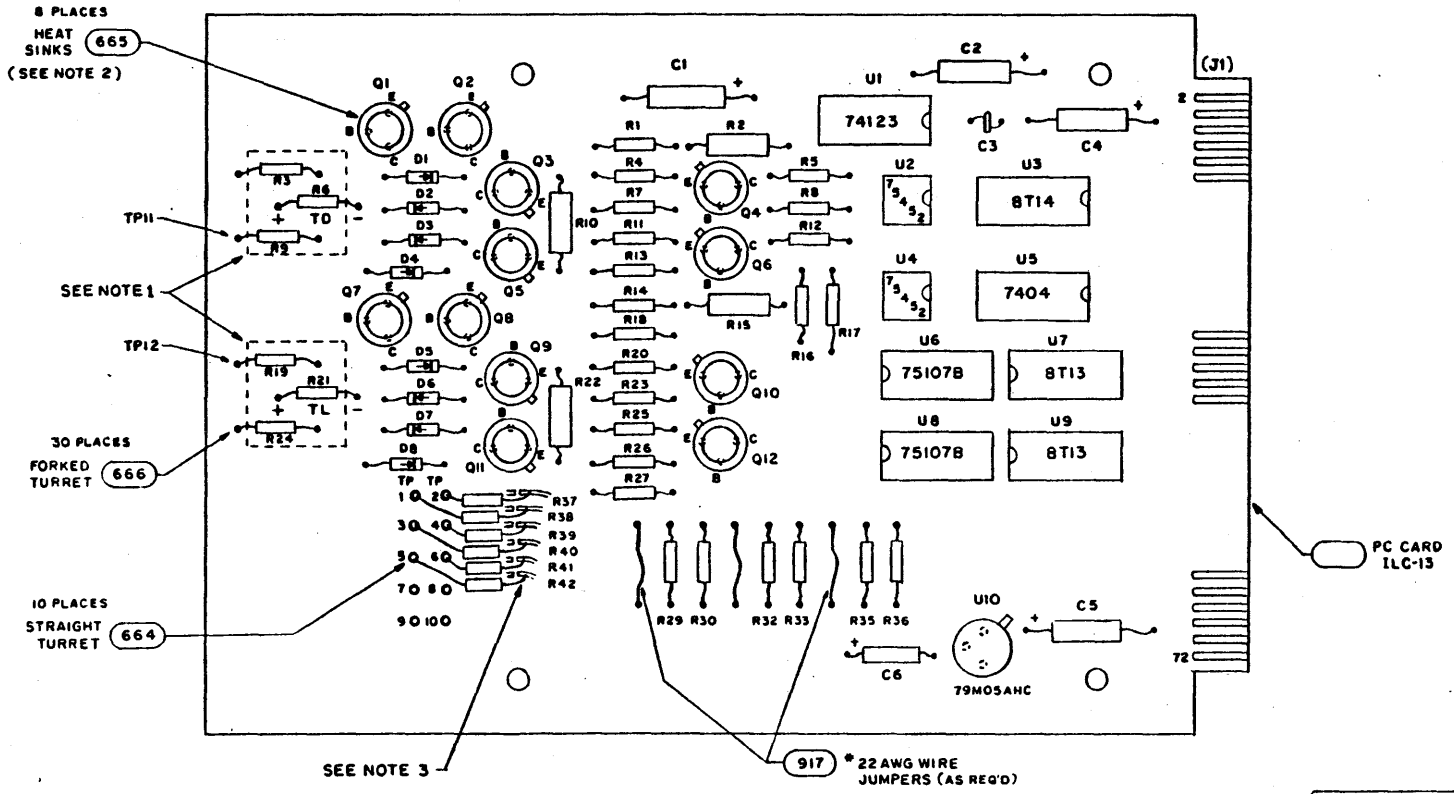
4 - POWER CABLE (PILC) RING LUG'S CONNECT TO TERMINAL BKT, MOUNTED ON INSIDE OF ILC ENCLOSURE END PLATE (SEE LCE-10)

INTERFACE LEVEL CONVERTER			SIZE
COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE MASS 02138			
DRAWN	DRF	5/15/78	TITLE: SINGLE SYSTEM LAYOUT
CHECKED	JHT	5/17/78	CODE IDENT NO. / DWG NO. SLC-09
ENG APPD	JHT	5/17/78	REV A

ILC

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	3/9/78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10 MFD
C2,4,5,6 = 2.2 MFD
C3 = .1 MFD

R1,4,11,14,18,20,25,27 = 610Ω - 1/4W
R2,10,15,22 = 100Ω - 1/2W
R3,9,19,24 = 270Ω - 1/4W
R5 = 90KΩ
R6,21 = 110Ω
R7,13,23,26 = 510Ω
R8,12,16,17 = 680Ω
R29,30,32,33,35,36 = 680Ω - 1/4W
R37,38,39,40,41,42 = 4.7KΩ - 1/4W

Q1,2,7,8 = 2N2219A
Q3-6,9-12 = 2N2905A

D1-8 = IN4003

NOTES

1 - RESISTORS INSIDE DOTTED LINES ARE NOT INSTALLED ON DOUBLE INTERFACES SYSTEMS (SEE ILC-09)

2 - PRESS HEAT SINKS ONTO Q1,2,3,5,7,8,9,11

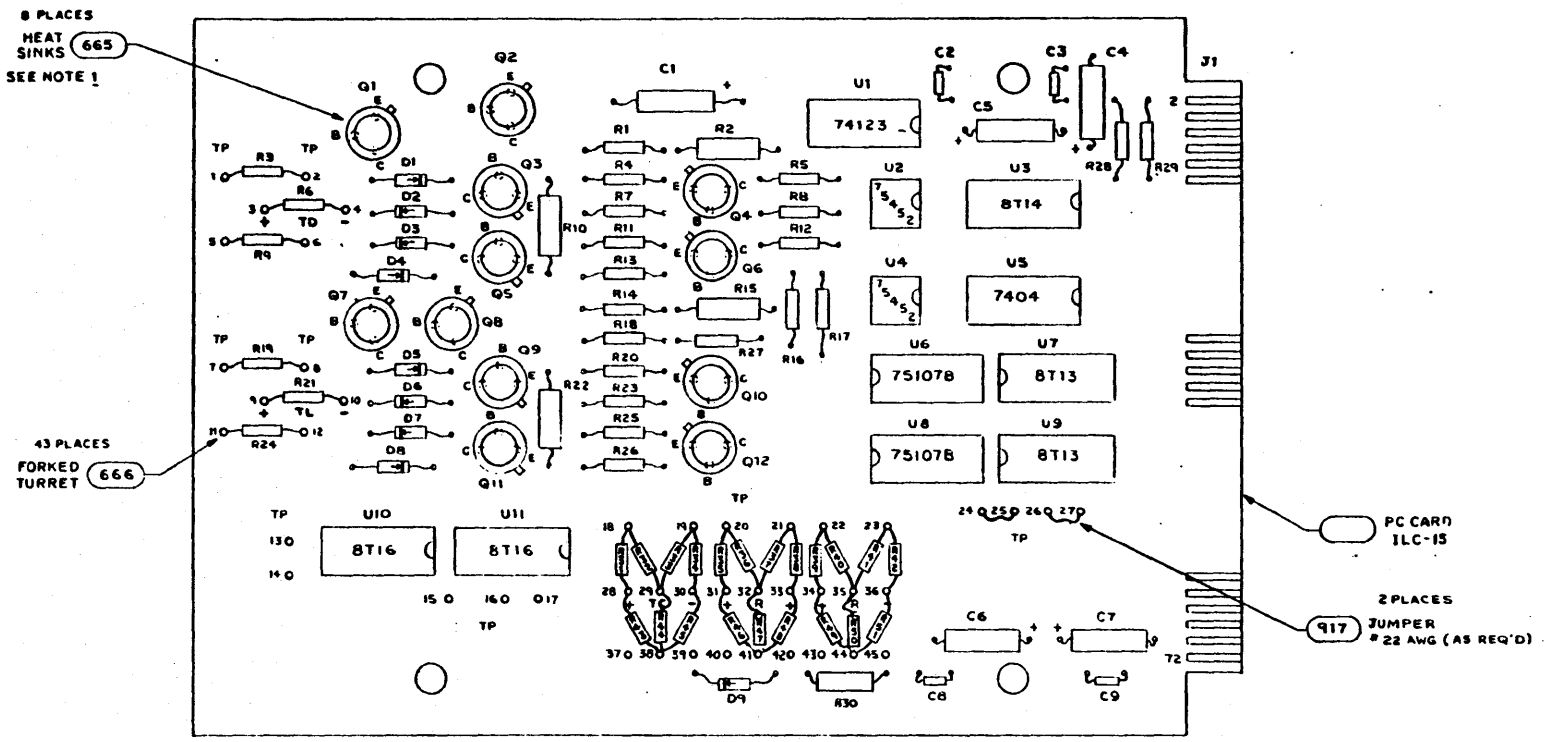
3 - SOLDER RESISTOR (R37-42) LEADS TO PC LINES AS SHOWN

THIS CARD ASSY MOD FOR NSA SYSTEM CARDS ONLY, S/N1-25

					SIZE
		BBN	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC CAMBRIDGE, MASS 02138		
	PSE-CU3				
	PSE-CU2	DRAWN	DRF	3/9/78	TITLE INTERFACE LEVEL CONVERTER ASSEMBLY
LCE-10	PSE-CU1	CHECKED	AT	3/9/78	
NEXT ASSY	USED ON	ENG APPD	AT	3/9/78	CODE IDENT NO DWG NO ILC-10A REV A
APPLICATION					

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.11.78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10MFD
C2,3,8,9 = .1 MFD
C4,5,6,7 = 2.2 MFD

R1,4,11,14,18,20,25,27, = 620Ω - 1/4 W
R2,10,15,22 = 100Ω - 1/2 W
R3,9,19,24 = 270Ω - 1/4 W
R5 = 91KΩ - 1/4 W
R6,21 = 110Ω - 1/4 W
R7,13,23,26 = 510Ω - 1/4 W
R8,12,16,17 = 680Ω - 1/4 W
R28,29 = 100Ω - 1/4 W
R30 = 390Ω - 1/2 W
R31,34,35,38,39,42 = 6.2KΩ - 1/4 W
R32,33,36,37,40,41 = 3KΩ - 1/4 W
R43,45,46,48,49,51 = 51Ω - 1/4 W
R44,47,50 = 120Ω - 1/4 W

Q1,2,7,8 = 2N2219A
Q3-6,9-12 = 2N2905A

D1-8 = IN4003
D9 = IN5230

NOTES

1 - PRESS HEAT SINKS ONTO Q1,2,3,5,7,8,9,11

2 - REMOVE R3,6,9,19,21,24,43,44,45,46,47,48, 49,50,51 WHEN CARD IS USED ON DOUBLE INTERFACE SYSTEMS, SEE SPECIFIC WORK REQUEST

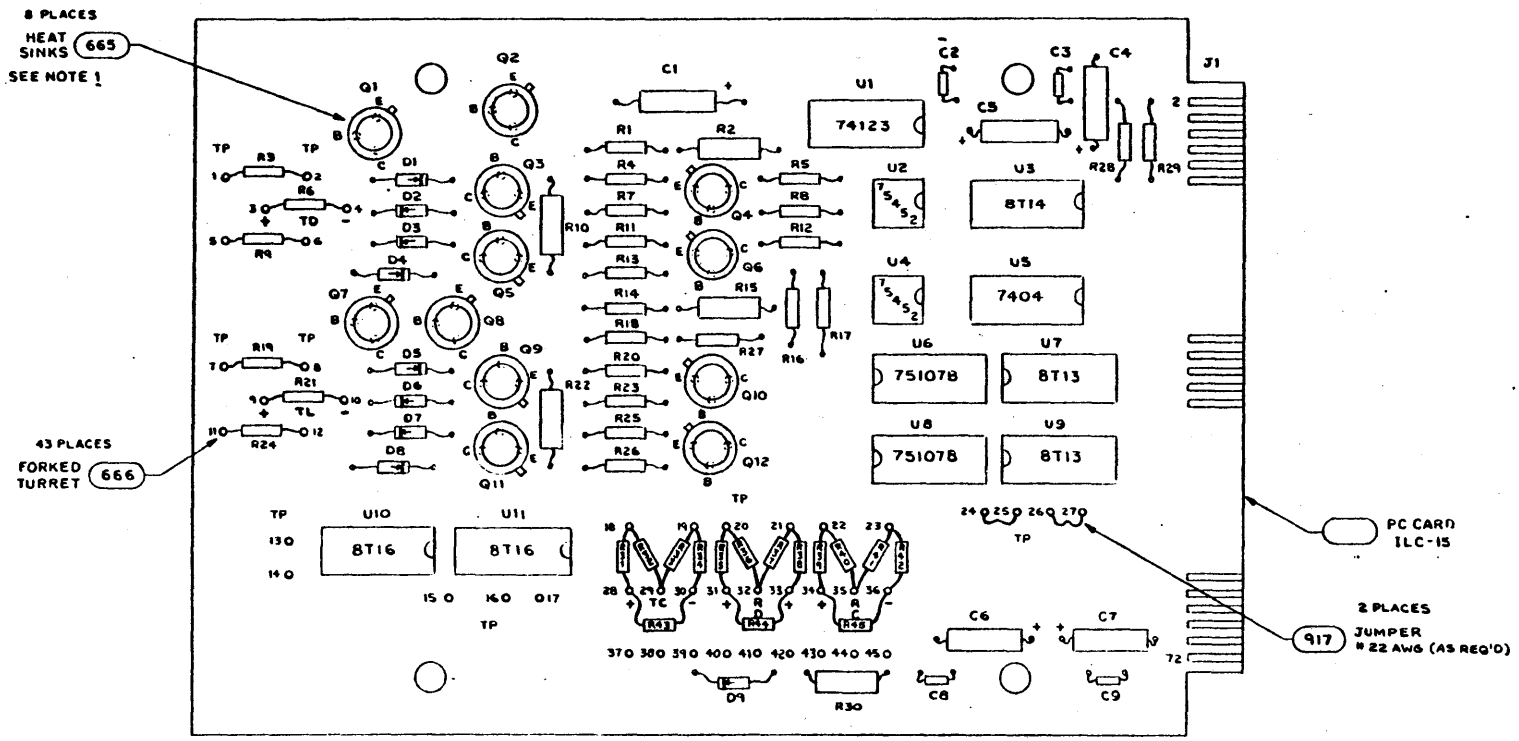
FOR PARTS LIST, SEE ILC-068

		PROTOCOL, MIL-188-100	SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138	
		DRAWN DRF 3.9.78	TITLE INTERFACE LEVEL CONVERTER PC CARD ASSY
		CHECKED JAT 3.9.78	
NEXT ASSY	USED ON	ENG APPD JAT 3.9.78	CODE IDENT NO. DWG NO. ILC-10-B REV A
APPLICATION			

ILC

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.11.78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10 MFD
C2,3,8,9 = .1 MFD
C4,5,6,7 = 2.2 MFD

R1,4,11,14,18,20,25,27 = 620Ω - 1/4 W
R2,10,15,22 = 100Ω - 1/2 W
R3,9,19,24 = 270Ω - 1/4 W
R5 = 91 KΩ - 1/4 W
R6,21,43,44,45 = 110Ω - 1/4 W
R7,13,23,26 = 510Ω - 1/4 W
R8,12,16,17 = 680Ω - 1/4 W
R28,29 = 100Ω - 1/4 W
R30 = 390Ω - 1/2 W
R31,34,35,38,39,42 = 4.7KΩ - 1/4 W
R32,33,36,37,40,41 = 820Ω - 1/4 W

Q1,2,7,8 = 2N2219A
Q3-6,9-12 = 2N2905A

D1-8 = 1N4003
D9 = 1N5230

NOTES

1 - PRESS HEAT SINKS ONTO Q1,2,3,5,7,8,9,11

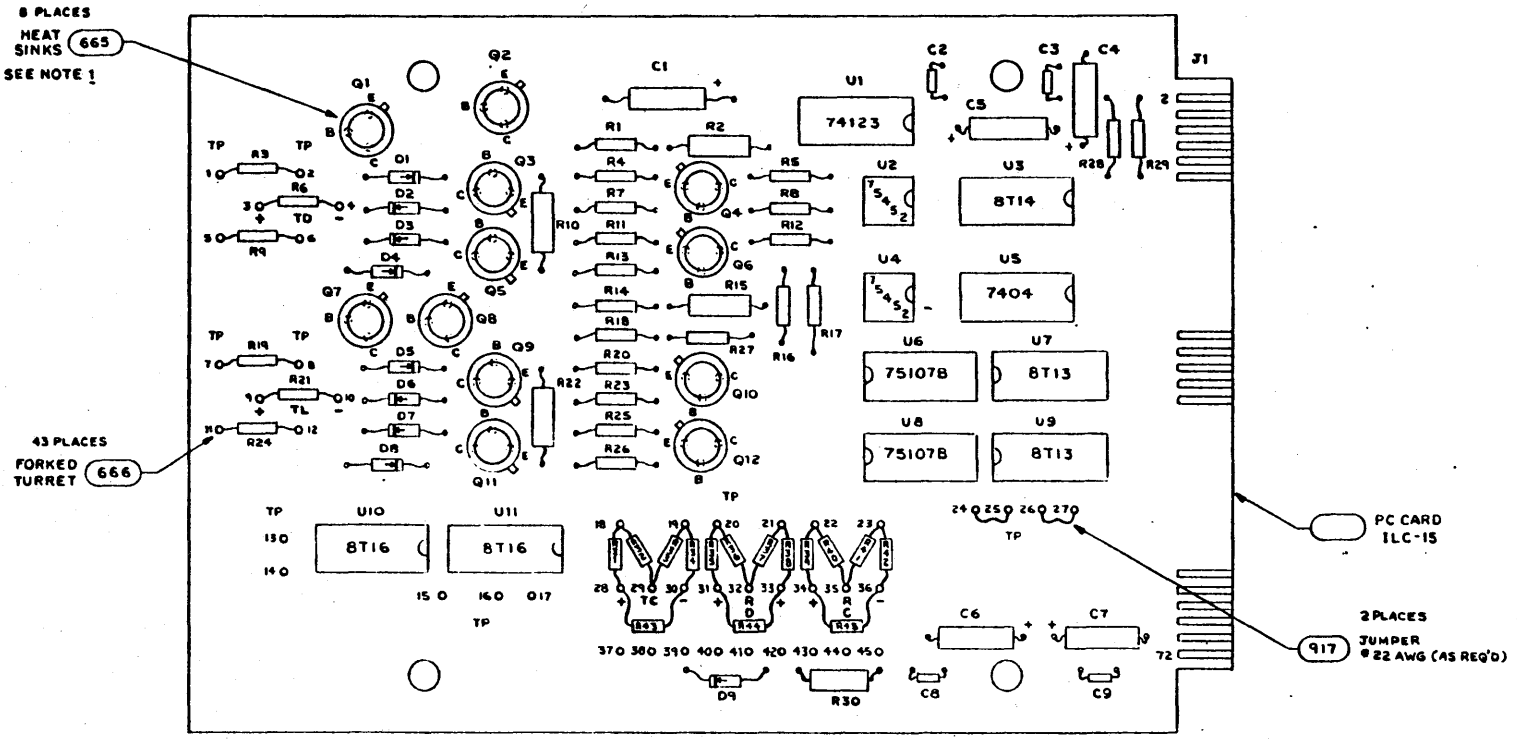
2 - REMOVE R3,6,9,19,21,24,43,44,45 WHEN CARD IS USED ON DOUBLE INTERFACE SYSTEMS, SEE SPECIFIC WORK REQUEST

FOR PARTS LIST, SEE ILC-06C

		PROTOCOL, MIL-188-114 / RS-422	SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138	
		DRAWN DRF 3/10/78	TITLE INTERFACE LEVEL CONVERTER PC CARD ASSY
		CHECKED 3/9/79	
NEXT ASSY	USED ON	ENG APPD 3-9-79	CODE IDENT NO. DWG NO. ILC-10-C REV A
APPLICATION			

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	9.11.78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10 MFD
C2,3,8,9 = .1 MFD
C4,5,6,7 = 2.2 MFD

R1,4,11,14,18,20,25,27 = 620Ω - 1/4W
R2,10,15,22 = 390Ω - 1/2W
R3,9,19,24 = 270Ω - 1/4W
R5 = 91 KΩ - 1/4W
R6,21,43,44,45 = 110Ω - 1/4W
R7,13,23,26 = 510Ω - 1/4W
R8,12,16,17 = 680Ω - 1/4W
R28,29 = 100Ω - 1/4W
R30 = 390Ω - 1/2W
R31,34,35,38,39,42 = 5.1 KΩ - 1/4W
R32,33,36,37,40,41 = 240Ω - 1/4W

Q1,2,7,8 = 2N2219A
Q3-6,9-12 = 2N2905A

D1-8 = 1N4003
D9 = 1N5230

NOTES

1 - PRESS HEAT SINKS ONTO Q1,2,3,5,7,8,9,11

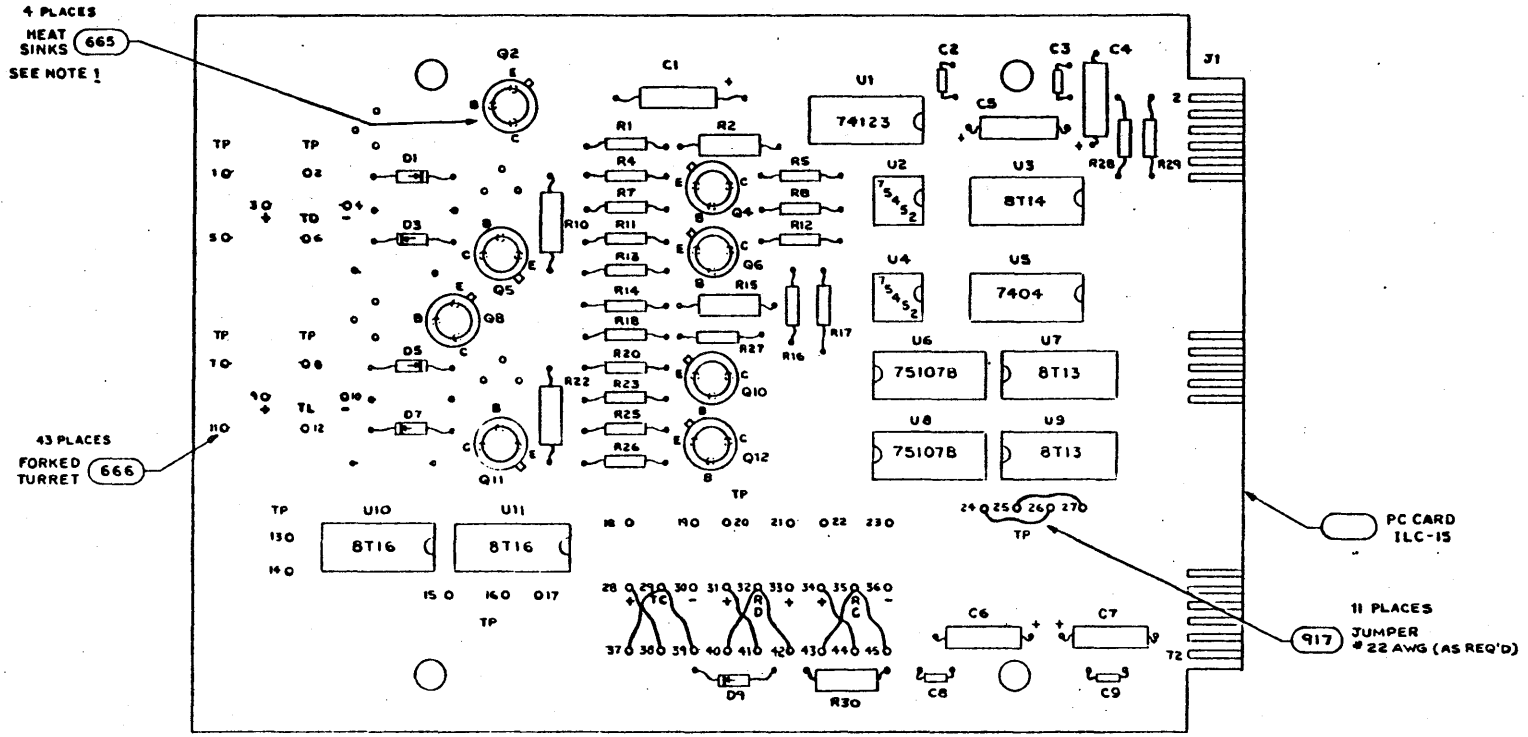
2 - REMOVE R3,6,9,19,21,24,43,44,45 WHEN CARD IS USED ON DOUBLE INTERFACE SYSTEM, SEE SPECIFIC WORK REQUEST

FOR PARTS LIST, SEE ILC-06D

		PROTOCOL, WE306 or V-35	SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138	
		DRAWN DRF 3-19-78	TITLE INTERFACE LEVEL CONVERTER PC CARD ASSY
		CHECKED JAT 3-1-78	
NEXT ASSY	USED ON	ENG APPD JAT 3-1-78	CODE IDENT NO. DWG NO. ILC-10-D REV A
APPLICATION			

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.11.78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10MFD
C2,3,8,9 = .1 MFD
C4,5,6,7 = 2.2 MFD

R1,4,11,14,18,20,25,27 = 620Ω - 1/4 W
R2,10,15,22 = 620Ω - 1/2 W
R5 = 91KΩ - 1/4 W
R7,13,23,26 = 270Ω - 1/4 W
R8,12,16,17 = 1.2KΩ - 1/4 W
R28,29 = 100Ω - 1/4 W
R30 = 390Ω - 1/2 W

Q2,8 = 2N2219A
Q4,5,6,10,11,12 = 2N2905A

D1,3,5,7 = 1N4003
D9 = 1N5230

NOTES

1 - PRESS HEAT SINKS ONTO Q2,5,8,11

FOR PARTS LIST, SEE ILC-06E

NEXT ASSY	USED ON		
APPLICATION			

PROTOCOL, RS-232C — SIZE

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

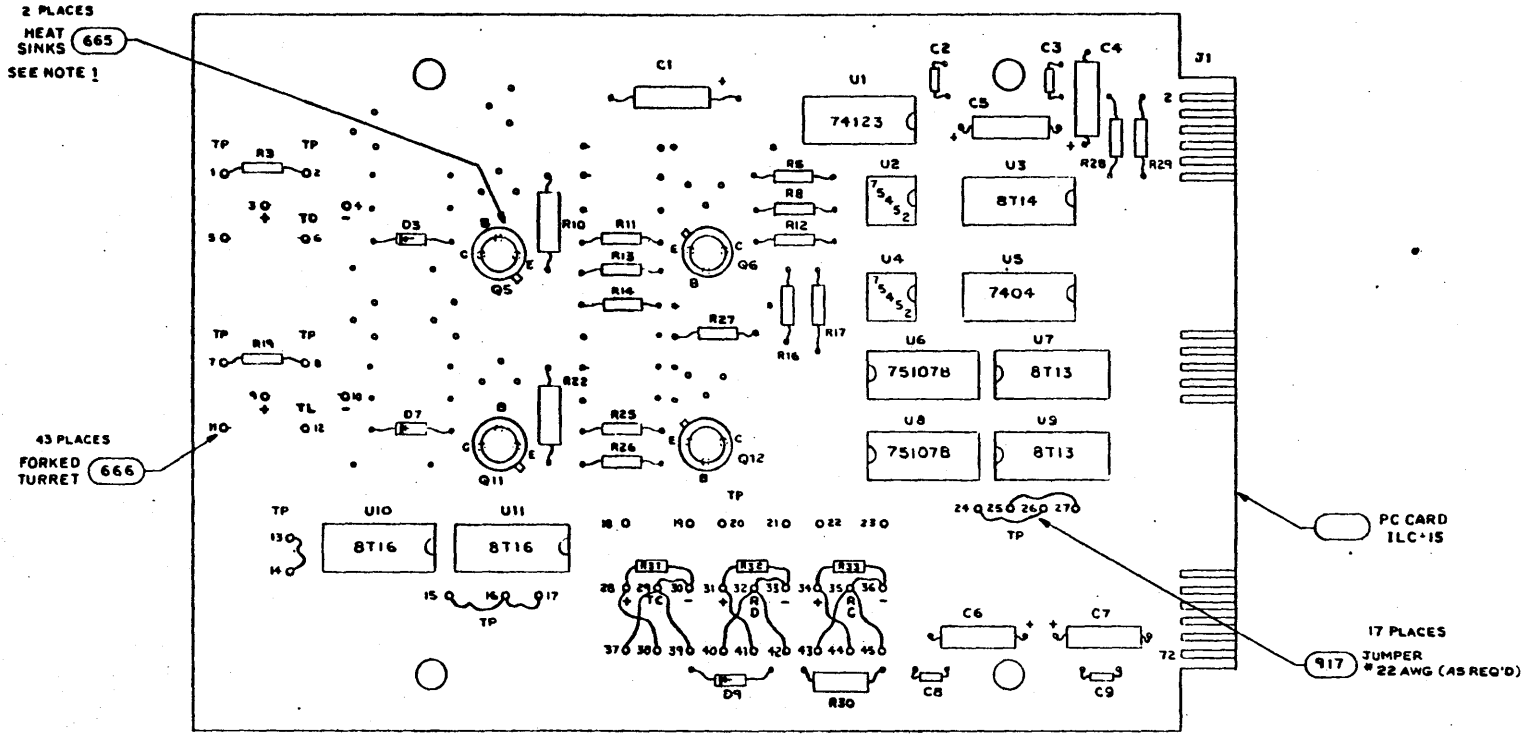
DRAWN	DRF	3.10.78
CHECKED	[illegible]	3-1-78
ENG APPD	[illegible]	3-1-78

TITLE: INTERFACE LEVEL CONVERTER PC CARD ASSY

CODE IDENT NO. | DWG NO. ILC-10-E | REV A

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.8.78	

COMPONENT SIDE



COMPONENT VALUES

C1 = 10 MFD
C2,3,8,9 = .1 MFD
C4,5,6,7 = 2.2 MFD

R3,19,28,29 = 100Ω - 1/4 W
R5 = 91 KΩ - 1/4 W
R8,12,16,17 = 680Ω - 1/4 W
R10,22 = 100Ω - 1/2 W
R11,25 = 620Ω - 1/4 W
R13,14,26,27 = 510Ω - 1/4 W
R30 = 390Ω - 1/2 W
R31,32,33 = 110Ω - 1/4 W

Q5,6,11,12 = 2N2905A

D3,7 = IN4003
D9 = 1N5230

NOTES

1 - PRESS HEAT SINKS ONTO Q5,11

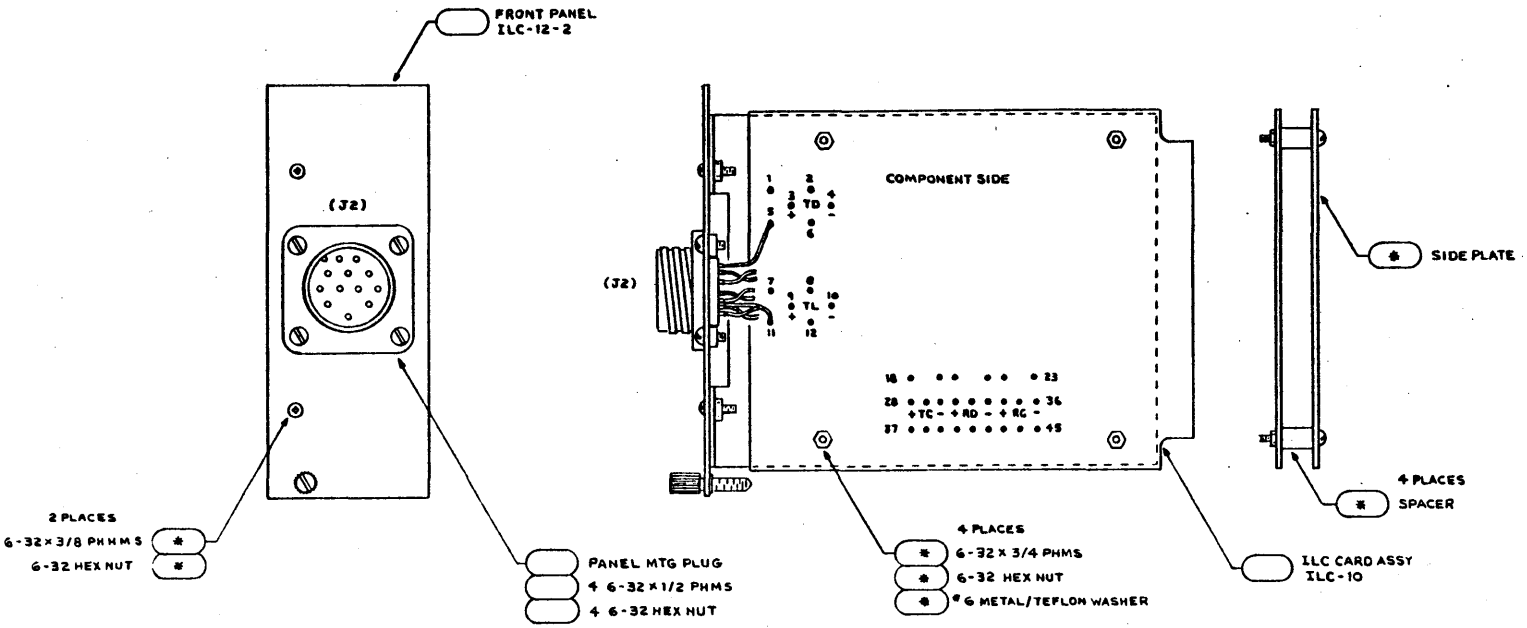
2 - REMOVE R3, 19 WHEN CARD IS USED ON DOUBLE INTERFACE SYSTEMS SEE SPECIFIC WORK REQUEST

FOR PARTS LIST, SEE ILC-06F

		PROTOCOL, BELL - 303	SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138	
		DRAWN DRF 3-19-78	TITLE INTERFACE LEVEL CONVERTER PC CARD ASSY
		CHECKED JAT 4-10-78	CODE IDENT NO. DWG NO. ILC-10-F REV A
NEXT ASSY	USED ON	ENG APPD JAT 4-12-78	
APPLICATION			

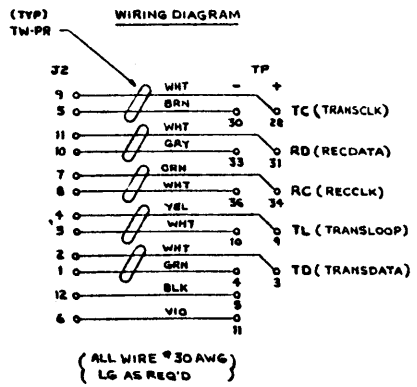
ILC

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.17.78	
B	ECN 0334	8.27.78	



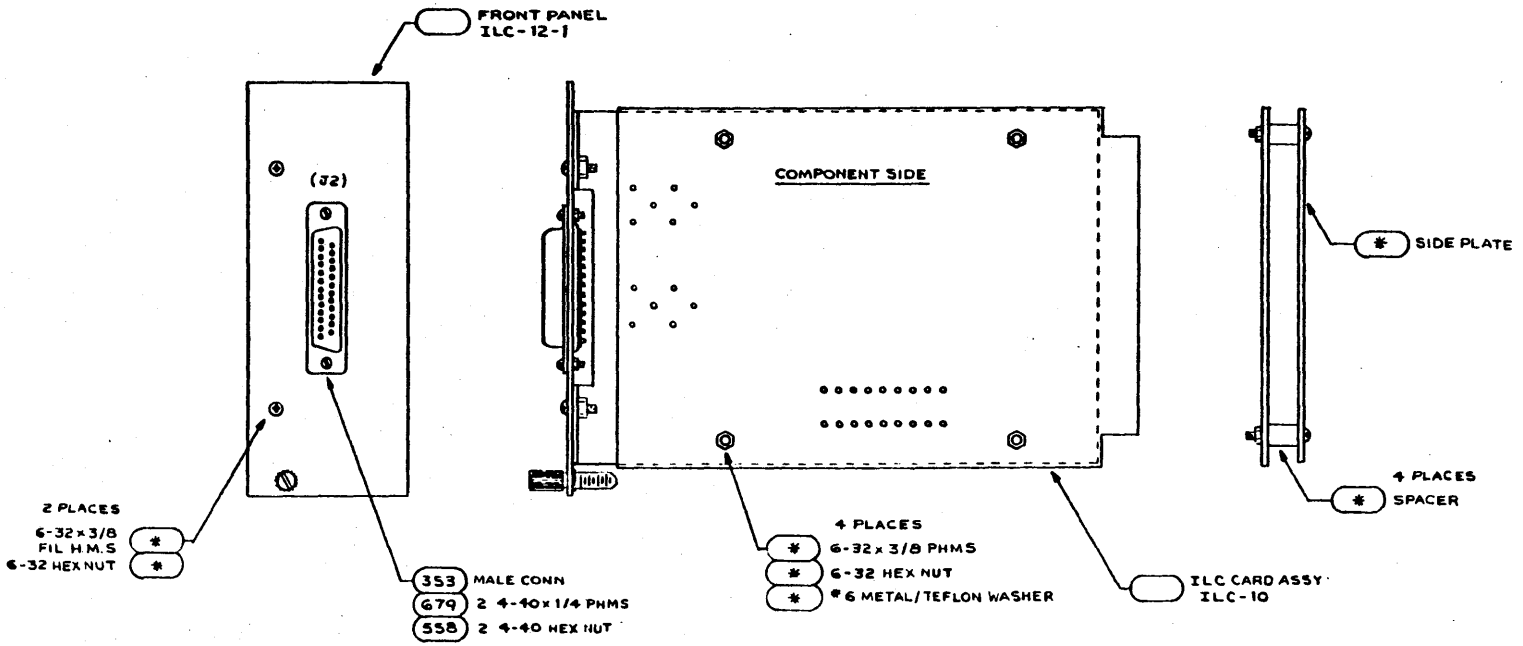
NOTES

1 - (*) DENOTES SUPPLIED WITH VECTOR-PAK CARD MODULE [CM45-65-2]



		INTERFACE LEVEL CONVERTER	SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC CAMBRIDGE, MASS. 02138	
		DRAWN DRF 5/17/78	TITLE ILC CARD/MODULE ASSY
		CHECKED JAT 5/18/78	CODE IDENT NO. DWG NO. ILC-11-C REV B
NEXT ASSY	USED ON	ENG APPD JAT 5/16/78	
APPLICATION			

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	5.18.78	



NOTES

1 - * INDICATES SUPPLIED WITH VECTOR-PAK CARD MODULE (CM45-65-2)

PLUG WIRING DIAGRAM

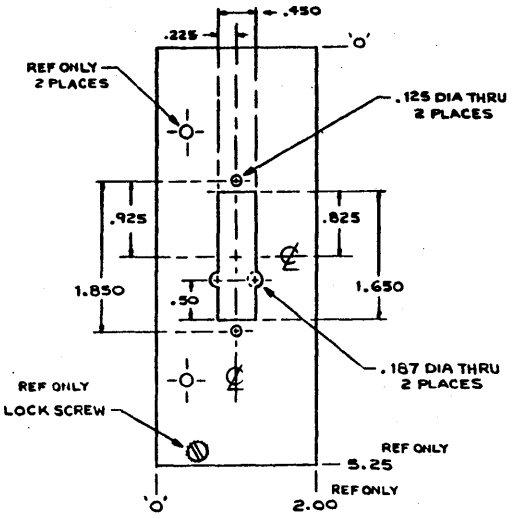
J2		TP
1	o———	o 1 (GND)
2	o———	o 3 (TRANSDATA+)
3	o———	o 31 (REC DATA+)
7	o———	o 11 (GND)
15	o———	o 28 (TRANSCLK+)
17	o———	o 34 (RECCLK+)

				SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138		
		DRAWN	DRF	1/13/78
		CHECKED	JAT	5/16/78
NEXT ASSY	USED ON	ENG APPD	JAT	5/18/78
APPLICATION				

TITLE		
ILC CARD & MODULE ASSY		
CODE IDENT NO	DWG NO.	REV
	ILC-11-E	A

ILC

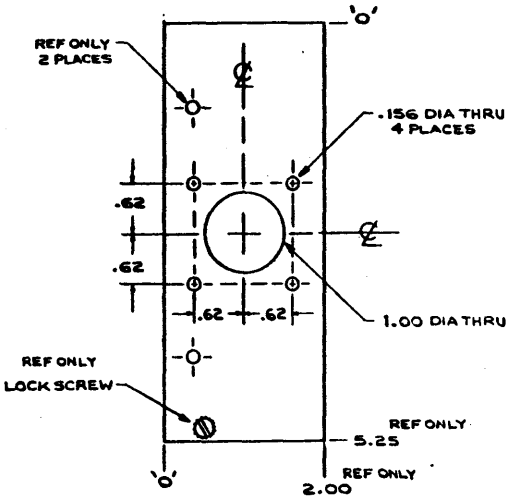
REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	9.18.77	
B	ECN 268	5-25-78	



FRONT PANEL
(VIEW UNASSEMBLED)

SCALE = 1:1

ILC-12-1

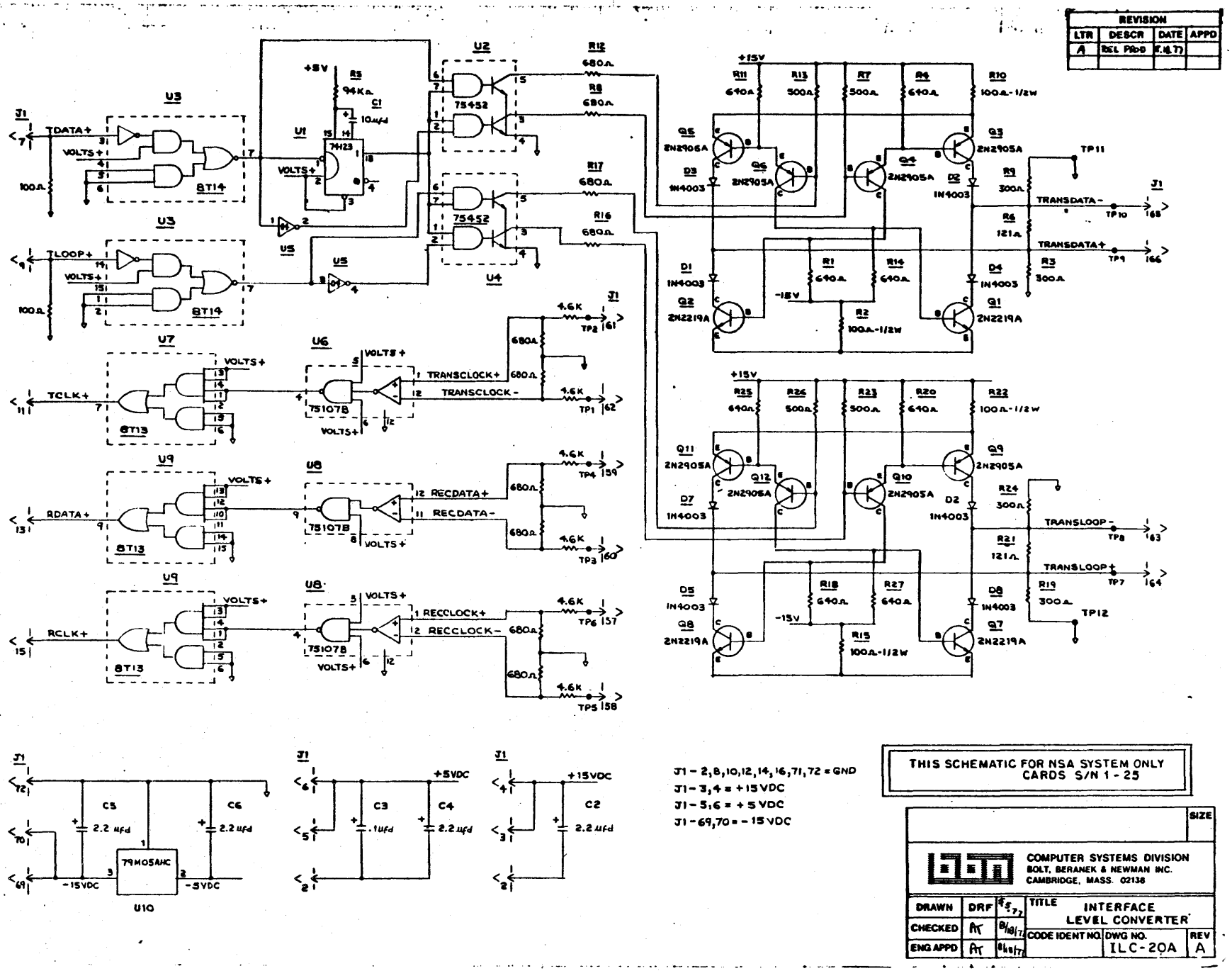


FRONT PANEL
(VIEW UNASSEMBLED)

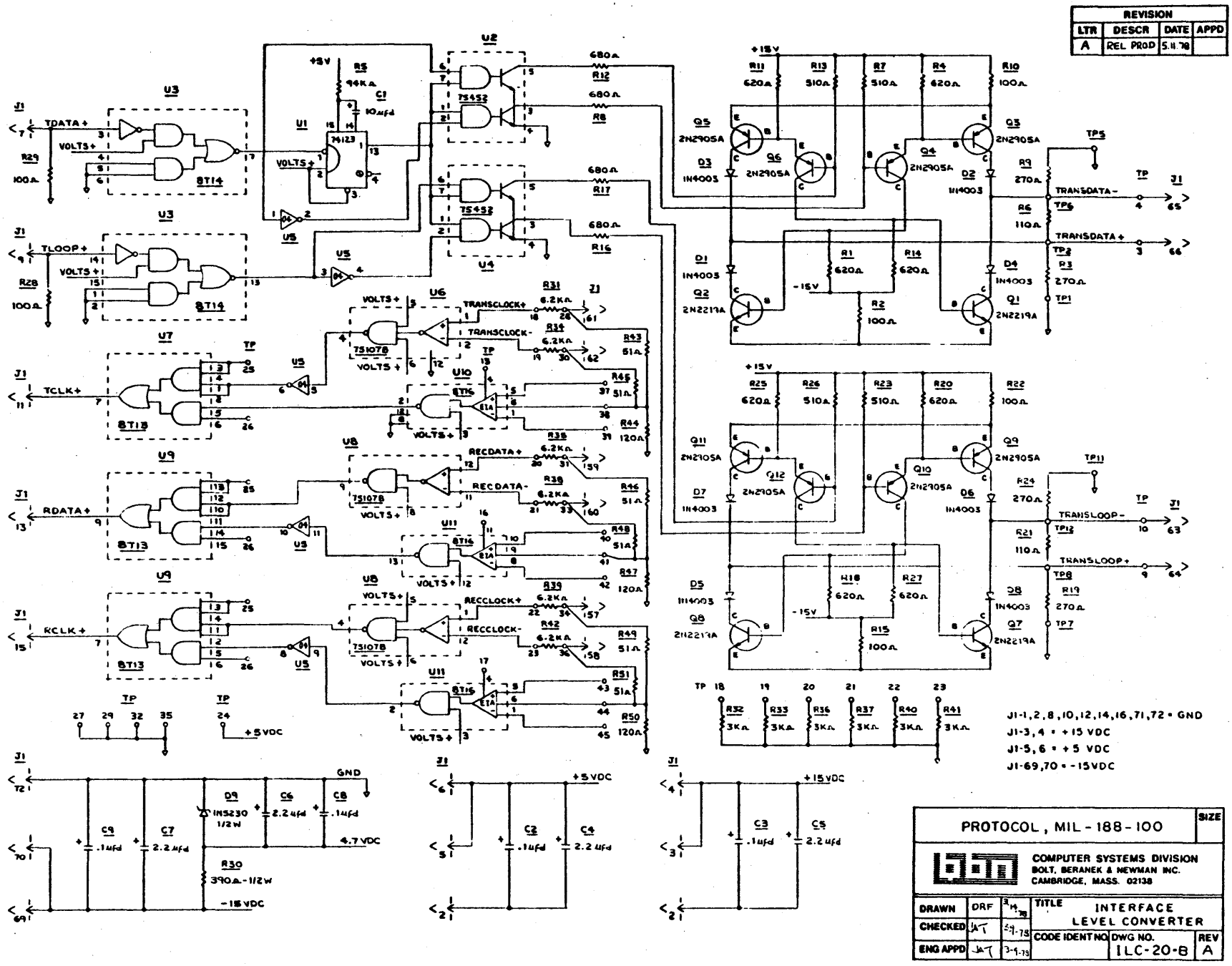
SCALE = 1:1

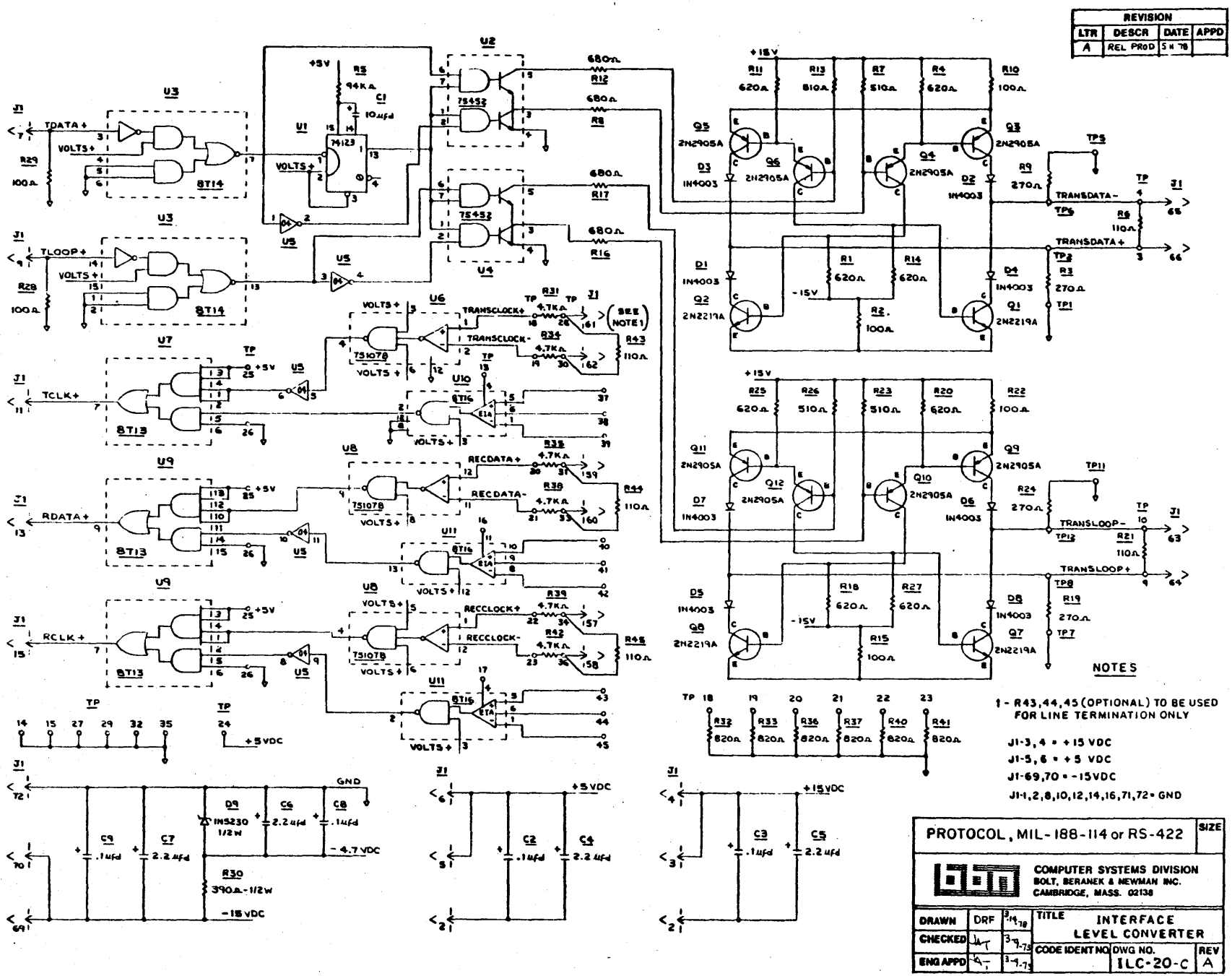
ILC-12-2

		TOLERANCES UNLESS OTHERWISE SPECIFIED	SIZE
		DECIMAL : .XX ± .010 .XXX ± .005	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138
		FRACTIONS : ± 1/64	
		ANGLES : ± 1°	
		MATERIAL : CM45-65-2 VECTOR-PAK CARD MTG ASSY	DRAWN DRF 9/14/77 — TITLE: FRONT PNL MOD OPTIONS VECTOR-PAK CARD MODULE
		FINISH :	CHECKED AT 9/14/77 — CODE IDENT NO. — DWG NO. ILC-12 — REV B
NEXT ASSY	USED ON		ENG APPD AT 9/14/77
APPLICATION			


REVISION
LTR DESCR DATE APPD
A REL PROD 7.18.77
+5V
+15V
-15V
-5VDC
+5VDC
+15VDC
-15VDC
TDATA+
TLOOP+
TCLK+
RDATA+
RCLK+
VOLTS+
TRANSCLOCK+
TRANSCLOCK-
RECDATA+
RECDATA-
RECCLOCK+
RECCLOCK-
TRANSDATA+
TRANSDATA-
TRANSLOOP+
TRANSLOOP-
U1 74123
U2 75452
U3 8T14
U4 75452
U5 8T14
U6 75107B
U7 8T13
U8 75107B
U9 8T13
U9 8T13
U10 79MOSAHC
Q1 2N2219A
Q2 2N2219A
Q3 2N2905A
Q4 2N2905A
Q5 2N2905A
Q6 2N2905A
Q7 2N2219A
Q8 2N2219A
Q9 2N2905A
Q10 2N2905A
Q11 2N2905A
Q12 2N2905A
D1 IN4003
D2 IN4003
D3 IN4003
D4 IN4003
D5 IN4003
D6 IN4003
D7 IN4003
D8 IN4003
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
J1 - 2,8,10,12,14,16,71,72 = GND
J1 - 3,4 = +15 VDC
J1 - 5,6 = +5 VDC
J1 - 69,70 = -15 VDC
THIS SCHEMATIC FOR NSA SYSTEM ONLY
CARDS S/N 1 - 25
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
SIZE
DRAWN DRF
CHECKED
ENG APPD
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO.
DWG NO. ILC-20A
REV A

ILC


REVISION
LTR DESCR DATE APPD
A REL PROD 5.11.78
+5V
R5 4.4KΩ
C1 10μfd
U1 74123
U2 75452
U4 75452
680Ω R12
680Ω R8
680Ω R17
680Ω R16
U5 O4
U3 8T14
J1
TDATA+
VOLTS+
R29 100Ω
TLOOP+
R28 100Ω
U6 75107B
TRANSCLOCK+
TRANSCLOCK-
R31 6.2KΩ
R34 6.2KΩ
R43 51Ω
U7 8T13
TCLK+
U10 8T16
R45 51Ω
R44 120Ω
U8 75107B
RECDATA+
RECDATA-
R35 6.2KΩ
R39 6.2KΩ
R46 51Ω
U9 8T13
RDATA+
U11 8T16
R48 51Ω
R47 120Ω
RCLK+
RECCLOCK+
RECCLOCK-
R42 6.2KΩ
R49 51Ω
R51 51Ω
R50 120Ω
TP 27 29 32 35
TP 24 +5VDC
+15V
R11 620Ω
R13 510Ω
R7 510Ω
R4 620Ω
R10 100Ω
Q5 2N2905A
Q6 2N2905A
Q3 2N2905A
Q4 2N2905A
D3 IN4003
D2 IN4003
R9 270Ω
R6 110Ω
TRANSDATA-
TRANSDATA+
TP5
TP6
TP2
TP1
R3 270Ω
D1 IN4003
Q2 2N2219A
R1 620Ω
R14 620Ω
-15V
R2 100Ω
D4 IN4003
Q1 2N2219A
+15V
R25 620Ω
R26 510Ω
R23 510Ω
R20 620Ω
R22 100Ω
Q11 2N2905A
Q12 2N2905A
Q9 2N2905A
Q10 2N2905A
D7 IN4003
D6 IN4003
R24 270Ω
TRANSLOOP-
TRANSLOOP+
TP11
TP12
TP8
TP7
R21 110Ω
R19 270Ω
D5 IN4003
Q8 2N2219A
R18 620Ω
R27 620Ω
-15V
R15 100Ω
D8 IN4003
Q7 2N2219A
TP 18 19 20 21 22 23
R32 3KΩ
R33 3KΩ
R36 3KΩ
R37 3KΩ
R40 3KΩ
R41 3KΩ
J1-1,2,8,10,12,14,16,71,72 = GND
J1-3,4 = +15 VDC
J1-5,6 = +5 VDC
J1-69,70 = -15VDC
GND
C9 .1μfd
C7 2.2μfd
D9 IN5230 1/2W
C6 2.2μfd
C8 .1μfd
4.7 VDC
R30 390Ω-1/2W
-15 VDC
+5VDC
C2 .1μfd
C4 2.2μfd
+15VDC
C3 .1μfd
C5 2.2μfd
PROTOCOL, MIL-188-100
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 3-1-78
CHECKED JAT 3-1-78
ENG APPD JAT 3-1-78
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO
DWG NO. ILC-20-B
REV A


REVISION
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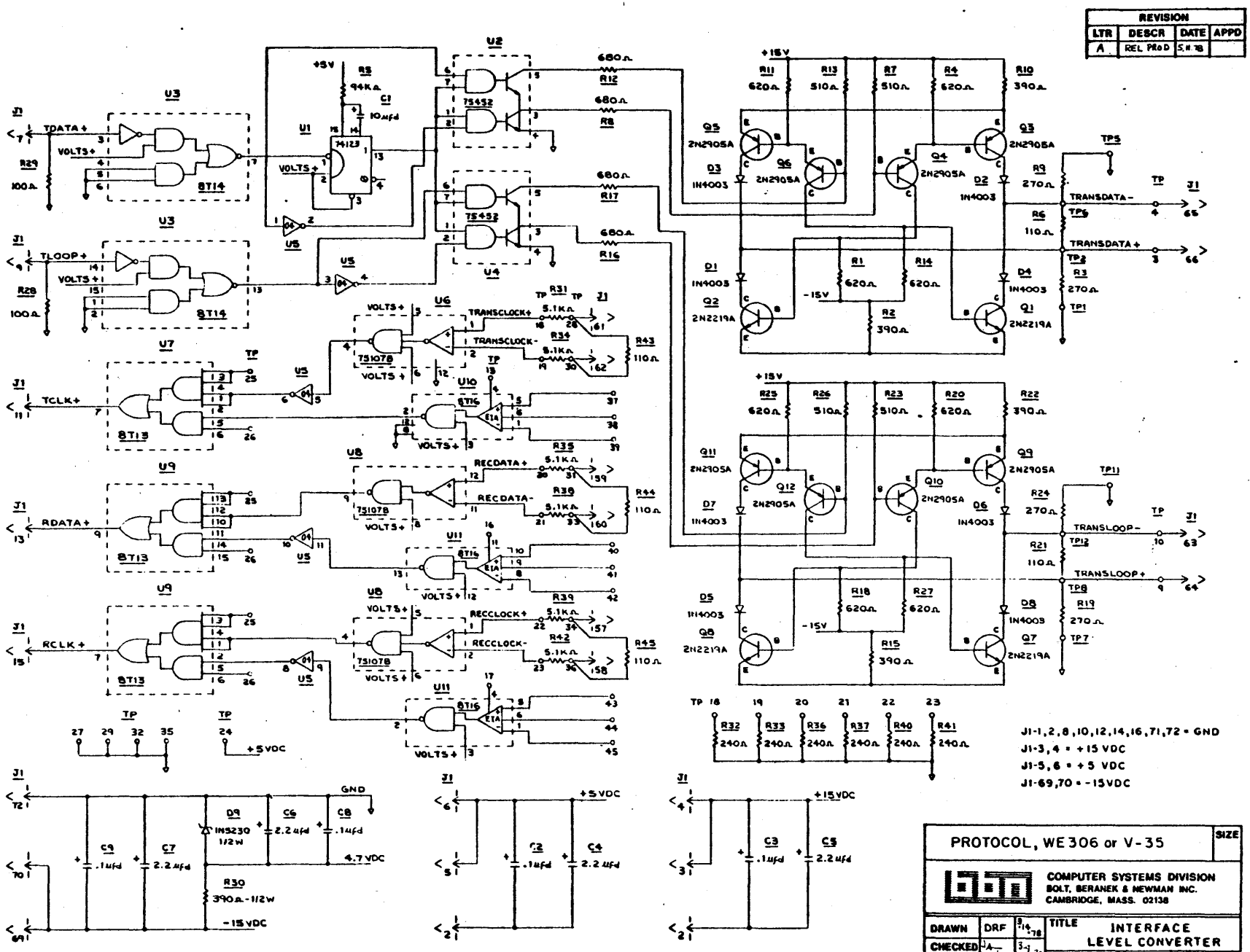
A REL PROD 5-4-78
TDATA+
TLOOP+
TCLK+
RDATA+
RCLK+
VOLTS+
TRANSDATA+
TRANSDATA-
TRANSLOOP+
TRANSLOOP-
TRANSCLOCK+
TRANSCLOCK-
RECDATA+
RECDATA-
RECCLOCK+
RECCLOCK-
+5V
-15V
+15V
GND
-4.7 VDC
-15 VDC
+5 VDC
+15 VDC
74123
75452
75107B
8T14
8T13
8T16
1N5230 1/2W
2N2905A
2N2219A
1N4003
NOTES
1 - R43,44,45 (OPTIONAL) TO BE USED FOR LINE TERMINATION ONLY
J1-3,4 = +15 VDC
J1-5,6 = +5 VDC
J1-69,70 = -15VDC
J1-1,2,8,10,12,14,16,71,72 = GND
PROTOCOL, MIL-188-114 or RS-422
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 3-14-78
CHECKED 3-9-78
ENG APPD 3-9-78
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO
DWG NO. ILC-20-C
REV A


REVISION
LTR DESCR DATE APPD
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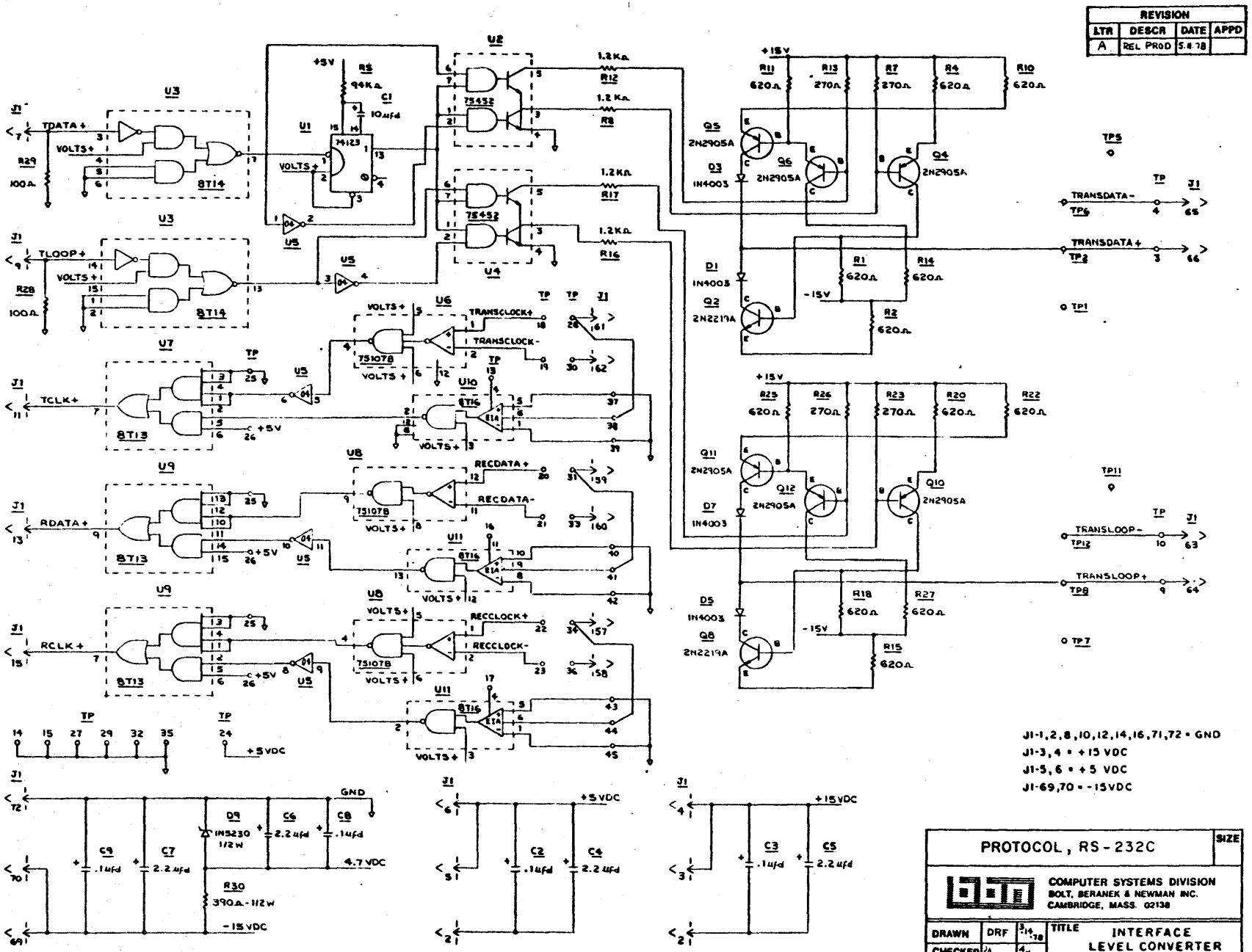
VOLTS+
TLOOP+
TCLK+
RDATA+
RCLK+
TRANSCLOCK+
TRANSCLOCK-
RECDATA+
RECDATA-
RECCLOCK+
RECCLOCK-
TRANSDATA-
TRANSDATA+
TRANSLOOP-
TRANSLOOP+
+5V
+15V
-15V
GND
+5VDC
+15VDC
-15VDC
J1-1,2,8,10,12,14,16,71,72 = GND
J1-3,4 = +15 VDC
J1-5,6 = +5 VDC
J1-69,70 = -15VDC
PROTOCOL, WE306 or V-35
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 3/14/78
CHECKED 3-1-79
ENG APPD 3-9-79
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO.
DWG NO. 1LC-20-D
REV A


REVISION
LTR DESCR DATE APPD
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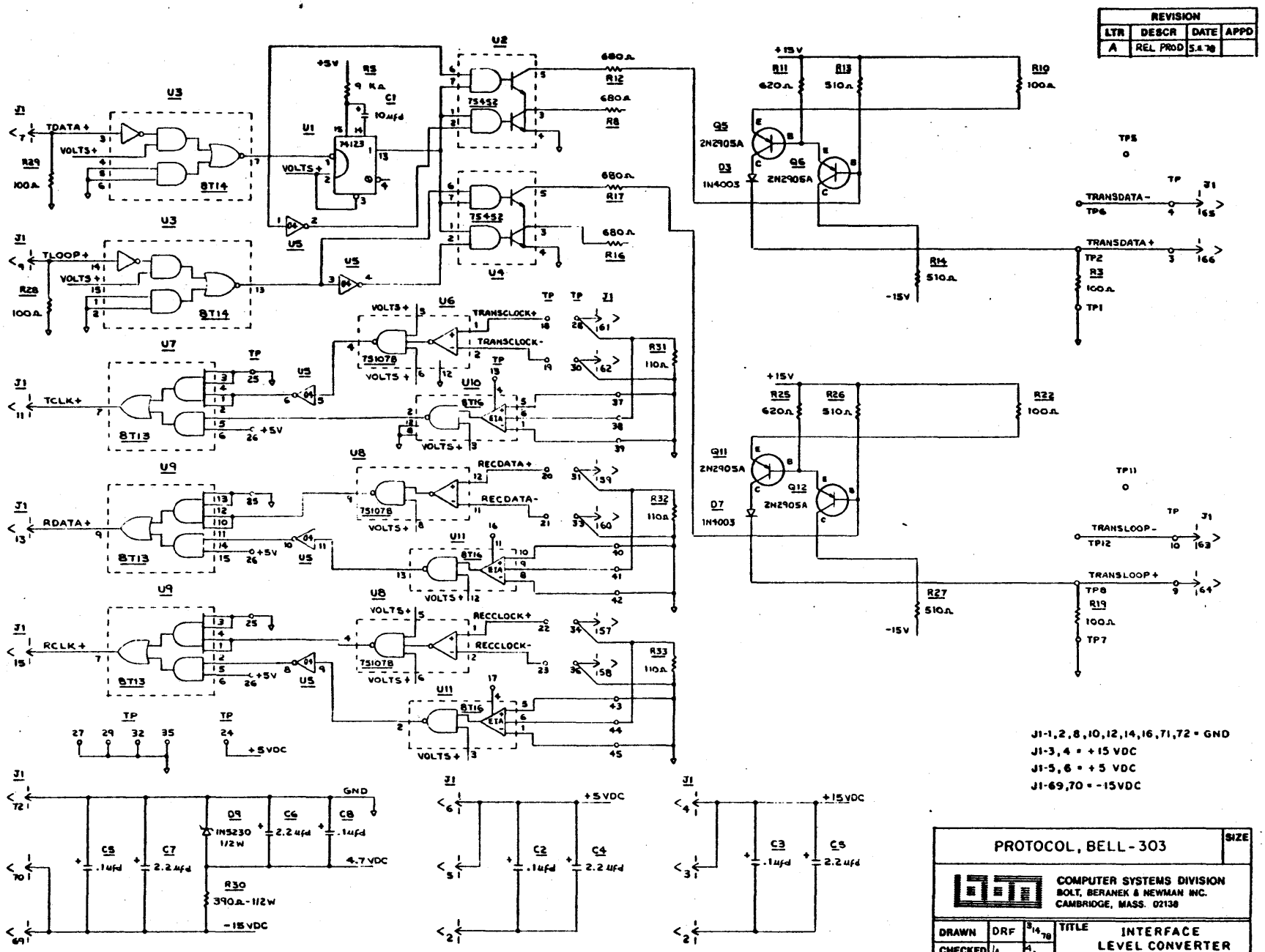
+5V
+15V
-15V
U1 74123
U2 75452
U3 8T14
U4 75452
U5 04
U6 75107B
U7 8T13
U8 75107B
U9 8T13
U10 8T16
U11 8T16
TDATA+
TLOOP+
TCLK+
RDATA+
RCLK+
VOLTS+
TRANSCLOCK+
TRANSCLOCK-
RECDATA+
RECDATA-
RECCLOCK+
RECCLOCK-
TRANSDATA+
TRANSDATA-
TRANSLOOP+
TRANSLOOP-
+5VDC
GND
+15VDC
-15VDC
4.7VDC
J1-1,2,8,10,12,14,16,71,72 = GND
J1-3,4 = +15 VDC
J1-5,6 = +5 VDC
J1-69,70 = -15VDC
PROTOCOL, RS-232C
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 3.14.78
CHECKED 4.16.78
ENG APPD 4.16.78
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO.
DWG NO. ILC-20-E
REV A

ILC


REVISION
LTR | DESCR | DATE | APPD
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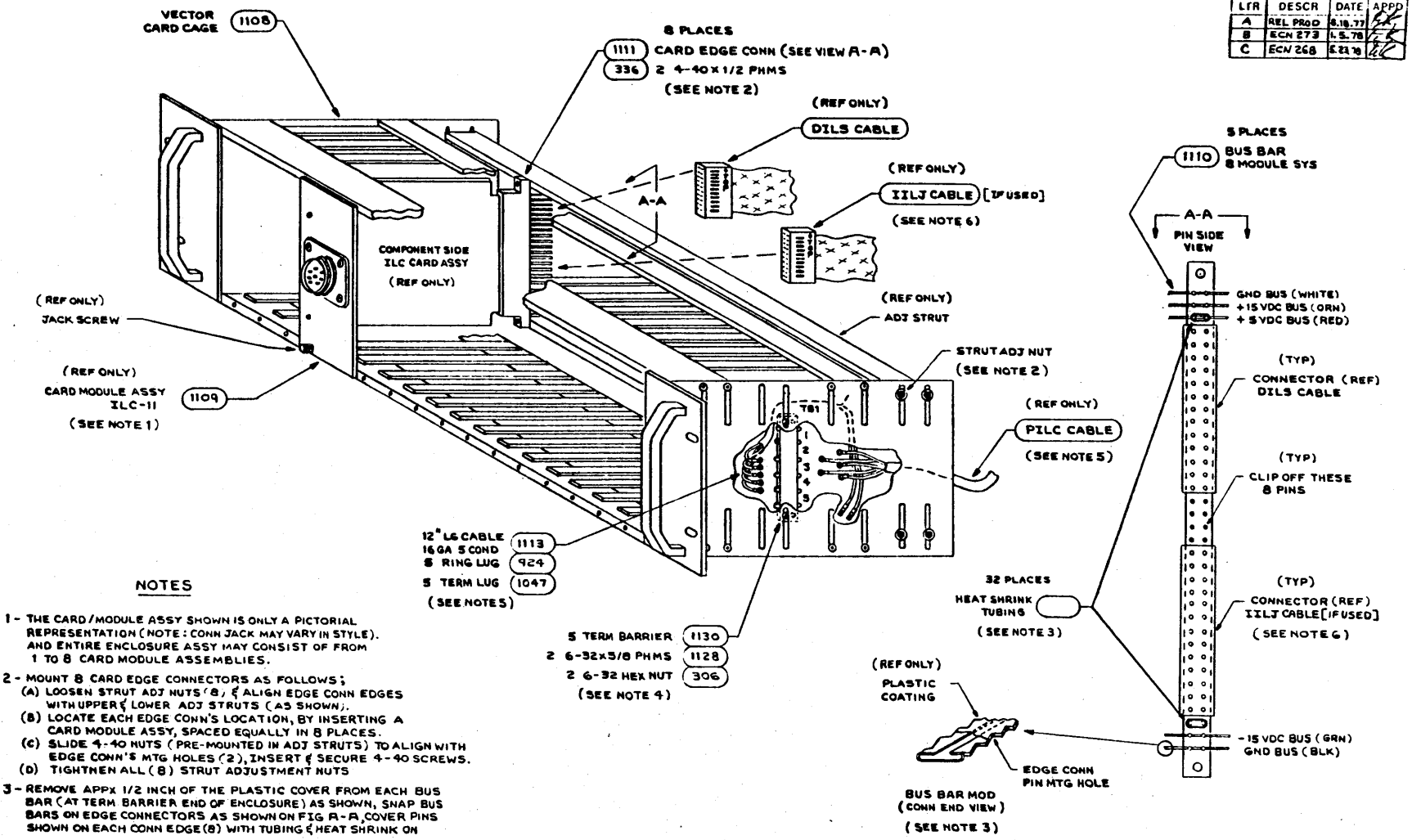
+5V
+15V
-15V
TDATA+
VOLTS+
TLOOP+
TCLK+
RDATA+
RCLK+
TRANSDATA+
TRANSDATA-
TRANSLOOP+
TRANSLOOP-
TRANSCLOCK+
TRANSCLOCK-
RECDATA+
RECDATA-
RECCLOCK+
RECCLOCK-
74123
75452
75107B
8T13
8T14
8T16
2N2905A
1N4003
J1-1,2,8,10,12,14,16,71,72 = GND
J1-3,4 = +15 VDC
J1-5,6 = +5 VDC
J1-69,70 = -15VDC
PROTOCOL, BELL-303
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 3/14/78
CHECKED
ENG APPD
TITLE INTERFACE LEVEL CONVERTER
CODE IDENT NO. DWG NO. ILC-20-F REV A

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	8.18.77	
B	ECN 273	4.5.78	
C	ECN 288	8.23.78	



NOTES

1 - THE CARD/MODULE ASSY SHOWN IS ONLY A PICTORIAL REPRESENTATION (NOTE: CONN JACK MAY VARY IN STYLE). AND ENTIRE ENCLOSURE ASSY MAY CONSIST OF FROM 1 TO 8 CARD MODULE ASSEMBLIES.

2 - MOUNT 8 CARD EDGE CONNECTORS AS FOLLOWS;
- (A) LOOSEN STRUT ADJ NUTS (8), & ALIGN EDGE CONN EDGES WITH UPPER & LOWER ADJ STRUTS (AS SHOWN).
- (B) LOCATE EACH EDGE CONN'S LOCATION, BY INSERTING A CARD MODULE ASSY, SPACED EQUALLY IN 8 PLACES.
- (C) SLIDE 4-40 NUTS (PRE-MOUNTED IN ADJ STRUTS) TO ALIGN WITH EDGE CONN'S MTG HOLES (2), INSERT & SECURE 4-40 SCREWS.
- (D) TIGHTNEN ALL (8) STRUT ADJUSTMENT NUTS

3 - REMOVE APPX 1/2 INCH OF THE PLASTIC COVER FROM EACH BUS BAR (AT TERM BARRIER END OF ENCLOSURE) AS SHOWN, SNAP BUS BARS ON EDGE CONNECTORS AS SHOWN ON FIG A-A, COVER PINS SHOWN ON EACH CONN EDGE (8) WITH TUBING & HEAT SHRINK ON

4 - MOUNT TERMINAL BARRIER (5 TERM) ON INSIDE ENCLOSURE END PIECE. CENTER AND BOLT THRU EXISTING SLOTTED HOLES AS SHOWN.

5 - CONNECT PILC & INTERNAL CABLE WIRES TO TERM BARRIER & BUS BARS AS FOLLOWS

WIRE COLOR	TB1	BUS BAR (FIG A-A)
WHITE	1	GND
ORANGE	2	+15 VDC
RED	3	+5 VDC
GREEN	4	-15 VDC
BLACK	5	GND

6 - IILJ CABLE(S) USED ONLY WITH DOUBLE INTERFACE SYSTEMS

		INTERFACE LEVEL CONVERTER			SIZE
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138			
		DRAWN	DRF	6-28-77	TITLE INTERFACE LEVEL CONVERTER ENCLOSURE
NEXT ASSY	USED ON	CHECKED	AT	8/8/77	
APPLICATION		ENG APPD	AT	8/8/77	CODE IDENT NO. DWG NO. LCE-10 REV C

ILC

Key Generator Interface

KGB-Ø2 Logic Description

KGB-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	REL FOR PROD	4/27/78	

KGB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN D. FRANCIS 4/12/78

CHECKER

ENGINEER

APP'D FOR REL D. L. Tock 5/1/78

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

KGB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		KGB-02

SCALE	REV	SHEET
	A	1 OF

KGB Interface
Logic Description

Revised March 21, 1978 by A. Lake

The KGB card allows the connection of the Black side of a Series 30 Key Generator (KG) to a Private Line Interface (PLI). Understanding of this logic description requires a knowledge of the KGR and KGB Functional Specifications, in addition to the data sheets on the COM-2601 USRT integrated circuit (Universal Synchronous Receiver Transmitter), the 3341 FIFO memory chip, and the ISO-108 optical isolator. A detailed understanding of the KG unit itself is not required, but familiarity with it (through the PLI Maintenance Guide) will be useful. Figure 1 is a block diagram of the KGB logic, showing the interface registers and control structure.

Drawing KGB-20: MISC CONTROL & RED-TO-BLACK RECEIVER

Drawing 20 contains the logic and buffering for various Infibus control signals, and the Red-to-Black word data receivers. The 7414 Schmitt-triggers in the upper right corner are used to buffer the incoming R-B data path which originates on KGR-20 and passes through feed-thru capacitors in the PLI bulkhead. The eight data bits (RBW0-7) go to the Infibus data multiplexers on drawing KGB-22. The Red-to-Black-Bus-Reset signal (RBBR+) is asserted by the Red PLI to cause a complete hardware reset in the Black PLI. The signal passes

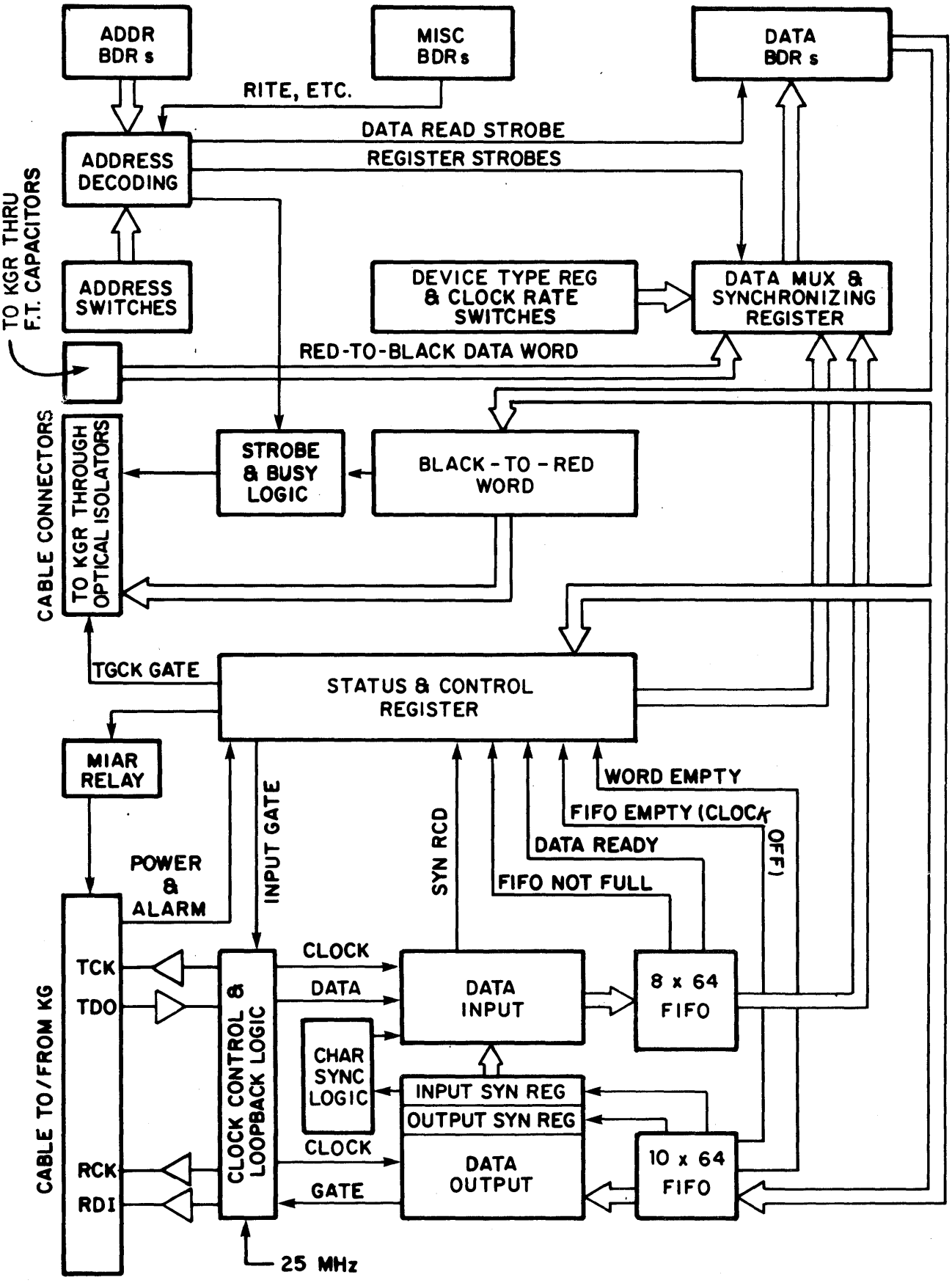


Figure 1 KGB Block Diagram

from the 7414 to dual 7438 buffer gates in the upper center of the drawing, which then drive the Infibus PSTAT line, assertion of which causes a bus reset and power restore interrupt of the Black PLI.

In the upper left, the discontinous Infibus signals are carried from one side of the Infibus connector to the other, including the precedence pulse PCDAB+. The remaining four Infibus signals used actively in the KGB card are the: Strobe, Done Pulse, Master Reset, and Rite signals. These are interfaced in the BDR D1. The status of the Rite signal during a particular memory reference is held in a flip-flop whose outputs are RITE+ and RITE-.

KGB-21: ADDRESS DECODING

Drawing 21 shows the interface address decoding for this card. The logic is straightforward and conventional. At the left are 5 BDRs providing a direct interface to the INFIBUS. Their inputs are unused (left floating but gated off by grounding the strobes), and their outputs are used as part of the address selection logic. The switches on the card are used to select the address to be recognized by an individual card. To the right of center is a 13-input AND-gate, whose output ADCOM- indicates that the address specified on the bus matches the switch settings on the card. Its inputs include bits 16-19 ungated, and bits 4-13 as selected by switches shown at the bottom of the drawing. Also included is AB03-, as the KGB device registers only occupy the lower 8 bytes of the 16 byte address space specified by AB04 thru AB19.

KGB Interface
Logic Description

The 7486 and 74136 bugs are exclusive-OR circuits used for address comparison. Note 1 on the drawing indicates that a switch closure is used to specify recognition of a 1 in the corresponding address bit. It does this by grounding the 1 input of the exclusive-or circuit associated with it. For example, with ASL11- grounded by the lowest switch in the leftmost switch of A3, a positive gate output ABS11+ will occur when the second gate input AB11+ is high. This will occur when the associated BDR input is low, indicating assertion of AB11B- on the INFIBUS. The output of the 10 gates in C3, B2, and B3 is a wired-AND configuration going high only when bits 4-13 compare correctly.

At the bottom of the drawing, an additional de-skewing gate is used to delay the strobe pulse STRB+ by an amount equivalent to the delay in the individual data bits before triggering the flip-flop whose output is ME+. A gate is also provided to inhibit ADSTR+ from clocking the flip-flop if the bus HOLD signal is present. Note that until the address selection cycle is started, the STRB+ pulse keeps the flip-flop in the "1" state. ME+ is a synchronized address selection signal used for all subsequent address dependent functions. Following this flip-flop is a 150 ns delay whose output ultimately generates a 60 ns DONE pulse. Below this circuit is a single AND-gate whose output DRSTR+ is used to strobe the data BDRs during a read operation.

In the upper right corner of the drawing is an octal decoder, which is used to strobe the appropriate interface registers. Its inputs are the RITE signal, and the low order address bits 1 and 2, all strobed by MEPLS+.

KGB-22: DATA BDR's and MUX

Drawing 22 contains the data multiplexer and BDRs used to interface with the data portion of the INFIBUS. The 4 BDRs are shown at the right of the drawing; their non-bus outputs in all cases go to other drawings. Each of their inputs comes from a flip-flop used to synchronize the data information with the INFIBUS reading cycle. The flip-flops themselves are contained on three circuits near the top center of the drawing. In all three cases the strobe used to latch the data is the data-read strobe DRSTR+. Note that this is the same signal used to strobe the BDRs themselves. This does not prohibit change of the signals on the INFIBUS at the beginning of the cycle, but the 150 ns duration of DRSTR+ is sufficient to ensure stabilization of outputs by the time DONE is assented, when the signals are used on the bus.

The remaining logic is part of the data multiplexer. The low order 2 bits of the address decoding are brought in at the bottom of each bug, and the data bits to be decoded are brought in at the left. The KGB Functional Specification's bit assignment chart will be of considerable help in understanding the origin of these signals.

KGB-23, OPT ISOLATORS and KG CONTROL

Logic for communicating over the Black-to-Red path through the optical isolators is shown on KGB-23 and KGR-23. Storing a word into the B-R word results in assertion of WBR which will set the BR Buffer Full flop. Flow control over the B-R path is accomplished by the

Black-to-Red-Word-Empty line (B2RWE). When the B-R word has been received by the Red program the B2RWE line will be asserted, clearing the BR Buffer Full flop.

The B-R word written is held in a 12 bit buffer whose outputs drive 7405 inverters which, in turn, drive the isolator input diodes. The 330 ohm pull-up resistors provide 15mA of current which is switched into the isolator diodes or sinked by the 7405s. The output voltage will therefore be only 0.8 volts max. At the isolator outputs, rise and fall times (isolators produce logical inversion) will be about 80- and 15-microseconds respectively.

At the same time the data bits change, the BR-Buffer-Full signal is generated and transmitted over optical isolator path #15. In the KGR card this signal is filtered and used to deskew and strobe the incoming B-R word. Isolator path #14 is presently unused. Isolator path #11 is independent of the status of Black's B-R word, controlled instead by a flip-flop (bottom center of #23) which is set by SC10 and cleared by SC11. Two bits are used for its control so that the program could change other control functions without affecting this flip-flop. This line is used on the KGR card to gate on the Transmitter Gated Clock (TGCK), and is monitored on the KGB card via SC10.

Isolator path #10 is used to reset Red's bus by asserting Red PWTST. An inverter is provided on the output of the 74174 buffer to allow the DBRS cable to be disconnected without causing constant assertion of ISO10.

KGB Interface
Logic Description

The connector for low speed KG signals is shown at the left side of KGB-23. KG-Power and -Alarm status are sensed by schmitt triggers, conveyed to the KGB as status bits SC06 and SC07, and passed through isolators 12 and 13 to the KGR card, independent of Black program activity.

The MIAR signal (see KG specs) is a relay closure to ground produced by a 7mS oneshot triggered by SC bit 01. The duration is sufficient to meet KG requirements, and the state of the oneshot may be sensed as SC bit 01.

Shown for reference is the remaining signal (TPREP) entering the FKGA cable even though it bypasses the KGB card. Both TPREP and KMIAR will show distortion and lousy edge speeds due to the effects of the KG's TEMPEST filters.

KGB-24: USRT Receiver

The normal sequence of events controlling this portion of the logic is as follows: During initialization the program will have stored a Receive-Sync character in the USRT. Further, either Master Reset or the program will have gated on the Input-Clock-flipflop (GICON) shown at the bottom center of the drawing. A random serial data stream will arrive on the KTDO line from the KG and will appear at pin 22 of the USRT since the program has not specified looptest (LOOP negated). When appropriate to get in message sync (analogous to Modem sync) a Receiver Reset is issued by setting bit 00 of the SC word. In the lower left of the drawing, this asserts IRES and RSET and

fires a oneshot that provides the pulse required by the USRT. This places the USRT into "SYN-search" mode, and the USRT scans the serial data for eight bits that match the pre-specified Receiver-sync character.

When a SYN is received, pin 17 is raised (RD14) priming the 1SYN flipflop just before assertion of the Input Data Available (IDA) signal from the USRT pin 26. Two or more adjacent SYNs are required for valid message sync, so if the second byte received is not SYN the four inputs of the NOISE gate (bottom center) are high and the IRESP oneshot is pulsed again, reinitializing SYN-search. The 33pf capacitor stretches the NOISE signal enough to prevent a runt pulse on the oneshot input.

If the byte following the SYN is a second SYN the 2SYN flipflop will be set by the following IDA pulse, and one input of the NSYN-gate will be asserted. This state will remain for as long as additional SYNs are received. However, when the first non-SYN is received NSYN is asserted and the DATA flipflop is set, concluding the SYN-search mode. The four-input NOISE gate is disabled so that further SYNs in the data stream will be ignored until the program initiates SYN-search mode again.

In the data mode, as long as the input rank of the FIFOs is empty, (IIR signals), the presentation of a new byte at the USRT outputs (IDA asserted) will trigger the 400nS oneshot. This produces Input Data Available Reset (IDAR) which strobes the data from the USRT to the FIFO (U2FST) and clears the RDA signal, although the sluggishness of the USRT makes the RDA pulse last about 100 nS in what would otherwise be a runt situation.

In the event that the FIFO memory is full, IFIR at the oneshot input will be negated, and no IDAR will be generated by the IDA signal which now will remain asserted. It will, however, trigger the ICKON flipflop in the upper left corner of =24, and this will gate off the input clock counter, halting clock pulses to both the KG and the USRT receiver. This situation will remain until the FIFO ceases to be full, at which time the IDAR oneshot will fire and the input clock will again be turned on (ICKON). Note that prior to data mode, since the FIFOs will have been cleared by IRESP, an IDAR will always follow IDA and keep the clock going even though no bytes will be strobed into the FIFOs.

The GICON flipflop at the bottom of the drawing allows the program to exercise further control over the clock, but as the Functional Specs state, it should only turn the clock off while it is already off, due to its asynchronous nature.

When the FIFO input byte percolates to the FIFO outputs, the Transmitter FIFO Output=Ready (TFOR) signal is asserted. This is synchronized with the Infibus STRB signal and presents a Data Ready signal to the program as bit 15 of the Read Data word. The program will periodically read the data word and ignore it unless it is negative (bit 15 is set). When it does read a negative data word, the combination of DAS15 and RDAT produces TSO which clears both the Data Ready flipflop and the output rank of the FIFOs.

At the left center of the drawing, the 74158 decoder provides the necessary gating to effect a loopback test mode. The LOOP signal,

originating on KGB-25, causes the USRT clock signal ICP to be derived from the output clock OCLK rather than the normal ICLK signal. Similarly, the serial data into the USRT is derived from its own serial output data OTSO rather than the KG's Transmit-Data-Out (KTDO) signal. Provision is made on KGB-25 for the test clock to be gated off in loopback by either the full state of the input FIFOs or the empty state of the output FIFOs. The USRT is thus prevented from automatically inserting SYN characters even in loopback.

KGB-25: USRT Transmitter

Drawing 25 shows the serial output portion of the KGB, which interfaces the Black side of the KG Receiver. The MIL-188 drivers (9616) are shown to the left of the USRT. Their outputs, if unterminated, would be + or - 6 volts, but proper termination at the KG inputs reduces this to about + or - 0.8 volts. The drivers are gated off during LOOP test.

Bits 0-9 of the Data Bus are buffered in the three FIFO memory chips. When the input rank of the FIFOs is empty, a three input gate asserts SC15 signifying that the Transmitter Buffer is Empty. The program, sensing this Status/Control bit, can store a new data byte into the FIFO.

The write data signal WDAT will shift the data bus bits into the FIFOs, dropping the Empty signal until the first rank is empty again.

When the 10-bit byte reaches the output rank of the FIFOs, OFOR (Output FIFO Output Ready) will fire the 400 nS oneshot if the USRT's

Transmitter Buffer Empty (OBMT) signal is high, or wait for it to go high. When both conditions are satisfied the FIFO-to-USRT Strobe (F2UST) transfers the FIFO byte into the USRT. As outlined in the Functional Specs, if bits 8 or 9 are set, the remaining 8 bits are transferred to the SYN-character holding registers inside the USRT. If neither 8 nor 9 is present (NOB89) bits 0-7 will enter the USRT data register. In addition, if the output clock had been gated off by the ORUN flipflop, the arrival of a new data byte at the FIFO outputs would have set ORUN again.

The ORUN flipflop will be reset only if the USRT empties its buffer (OBMT) requesting a new byte at a time when no byte is available at the FIFO outputs. Until a new byte percolates to the FIFO outputs, the clock pulses to the KG and the USRT transmitter will be gated off, thus avoiding the automatic insertion of a Transmitter Sync character into the data stream by the USRT (see USRT data sheet).

KGB-26: SERIAL DATA CLOCK COUNTERS

The Input Clock and Output Clock pulses (ICLK and OCLK) are derived from the 25 MHz Infibus clock signal. Three DIP switches are provided to allow the selection of one of eight basic clock speeds ranging from 24.4 to 97.6 KBaud as tabulated on the drawing. The switches determine the "preset" count of the second- thru-fourth stages of the first counter. The second counter simply divides by sixteen.

Gating of the Output clock has the added complication that, since ICLK is not used during loopback, OCLK must be controlled by both OCGO

and ICKON. The gate structure is such that when LOOP is negated, INLOP+ is high and only OCGO affects the output clock. OCGO will be asserted whenever the output is running (ORUN) and the Red Receiver Fifo is ready (RRFR).

KGB-Ø2 LOGIC DESCRIPTION - APPENDIX 1

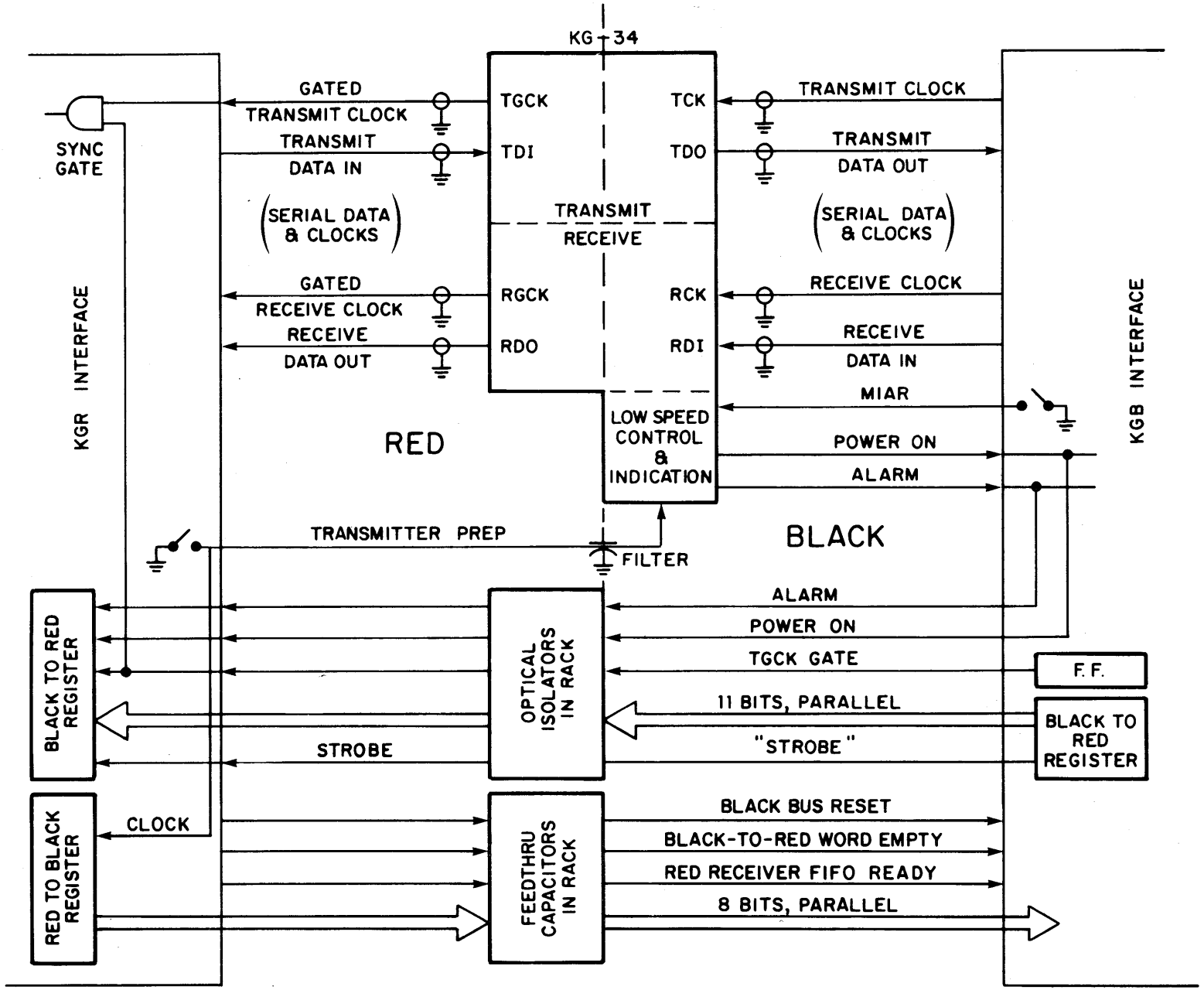
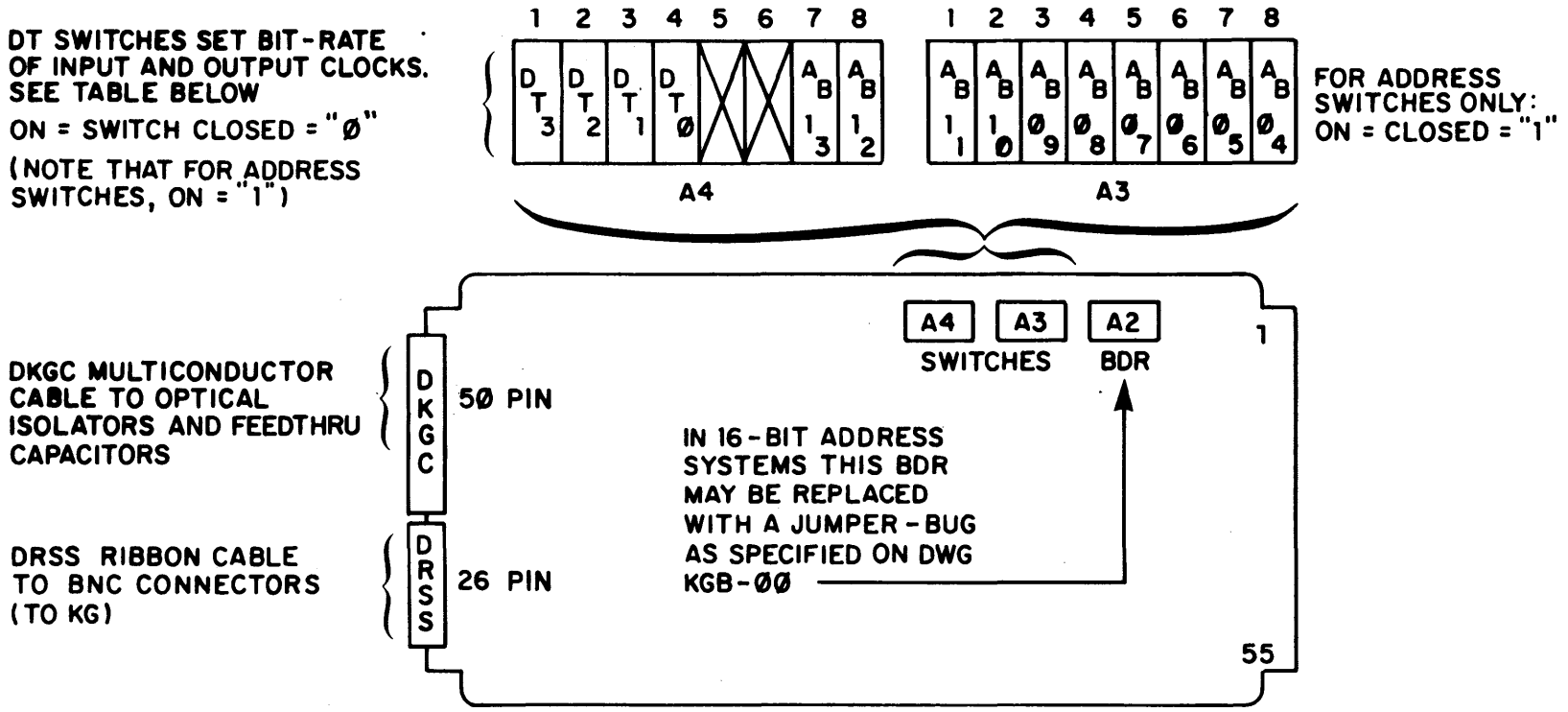


Figure 1-1 KGR-KG-KGB System Diagram and Nomenclature



SWITCH SETTING TABLE

NOMINAL BIT RATE	A4 -2	A4 -3	A4 -4	D.T. REG BITS 2-1-Ø	
(4ØØ)				111	← PROHIBITED
2ØØ			ON	11Ø	
133		ON		1Ø1	
1ØØ		ON	ON	1ØØ	
8Ø	ON			Ø11	
66	ON		ON	Ø1Ø	
58	ON	ON		ØØ1	
5Ø	ON	ON	ON	ØØØ	

NOTE: A4-1 MAY BE SET TO EITHER POSITION AND DOES NOT INFLUENCE CLOCK RATE

Figure 1-2 KGB Switches and Connectors

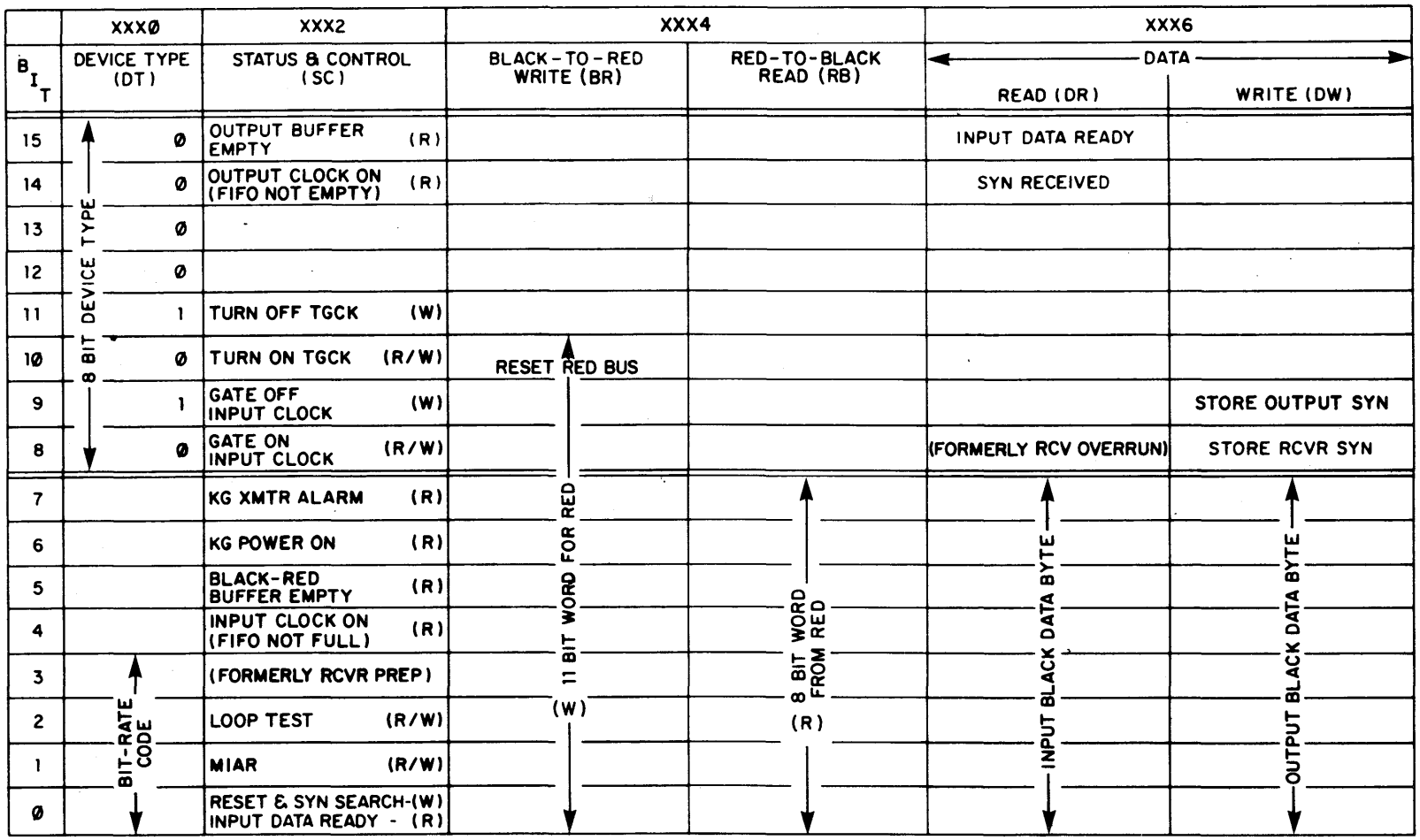
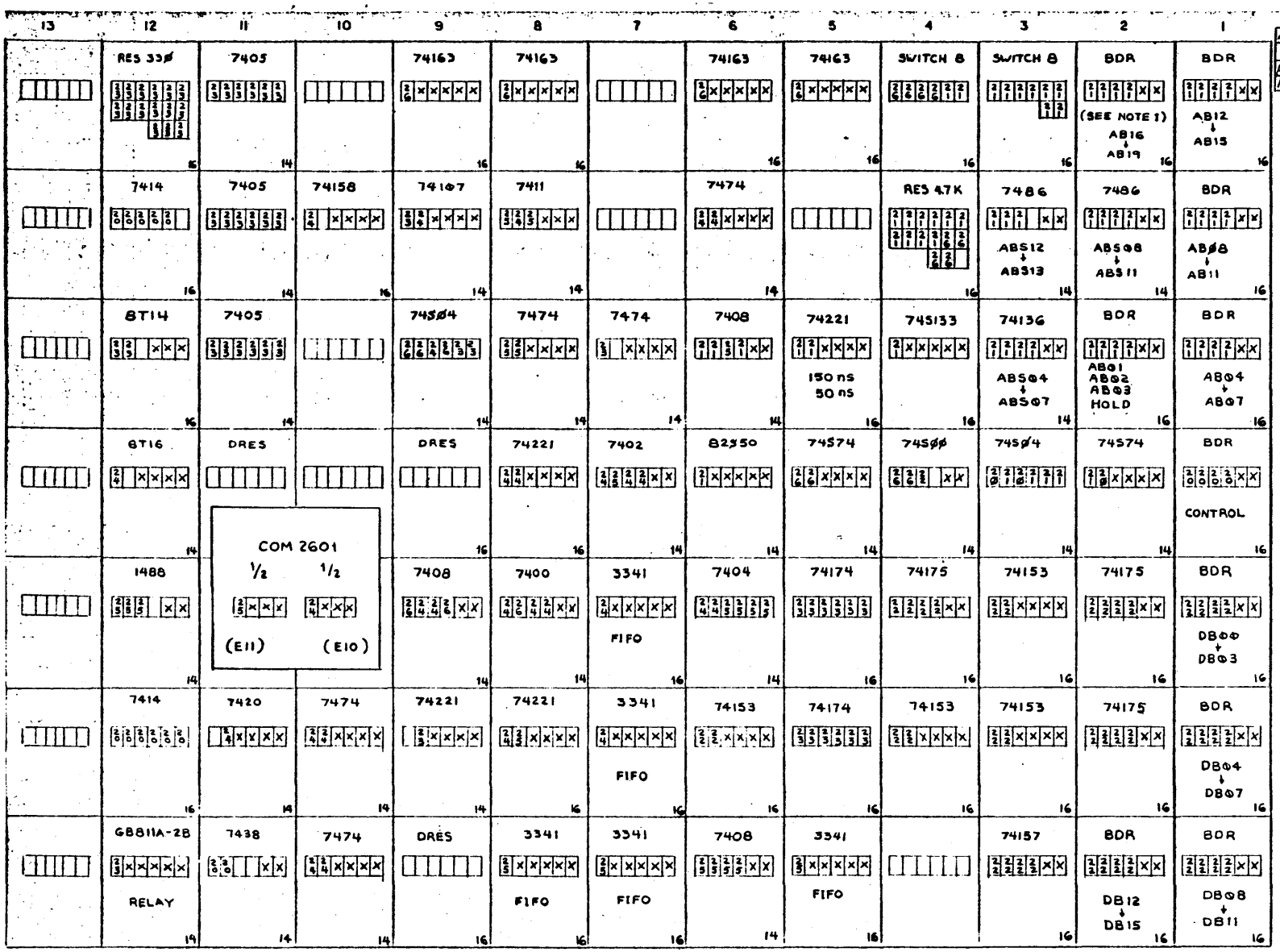


Figure 1-3 KGB Bit Assignments

KGB-2Ø SCHEMATICS



TOP VIEW

NOTES:

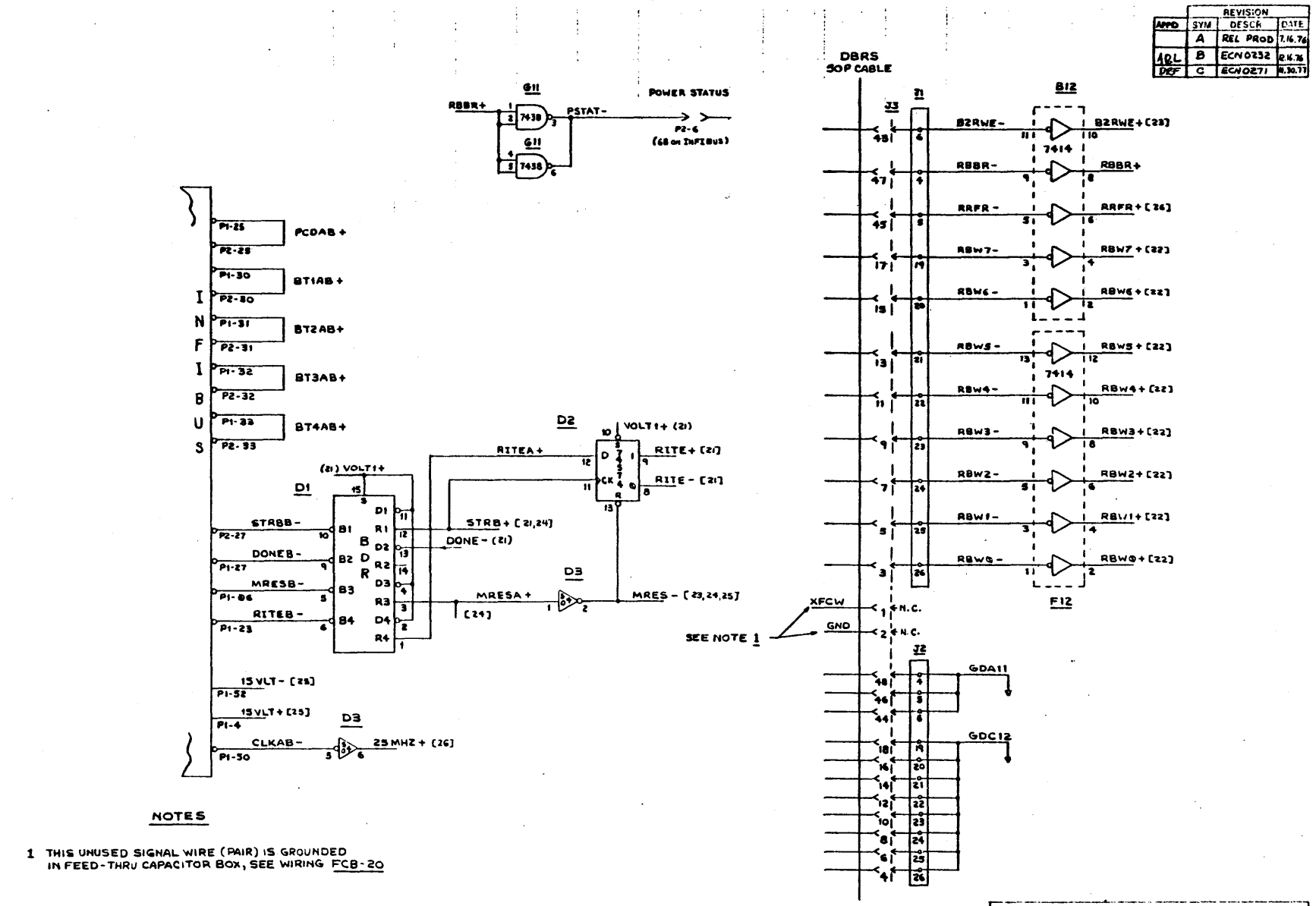
1 - IN 16 BIT ADDRESS SYSTEM, REPLACE A2 WITH COMPONENT BUG, CONNECTING PINS 1,3,12 & 14 TO PIN 16 THROUGH A 1K-1/4 RESISTOR

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.6.76
AVL	B	ECN0232	12.16.76
PEL	C	ECN0241	2.3a.77

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	SET	8.2.75	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED	DCF	1.5.76	
APPROVED	JM	7/16/76	CUSTOMER/NO. PLI-1 · DWG NO. KGB-00-WW · REV C

KGB

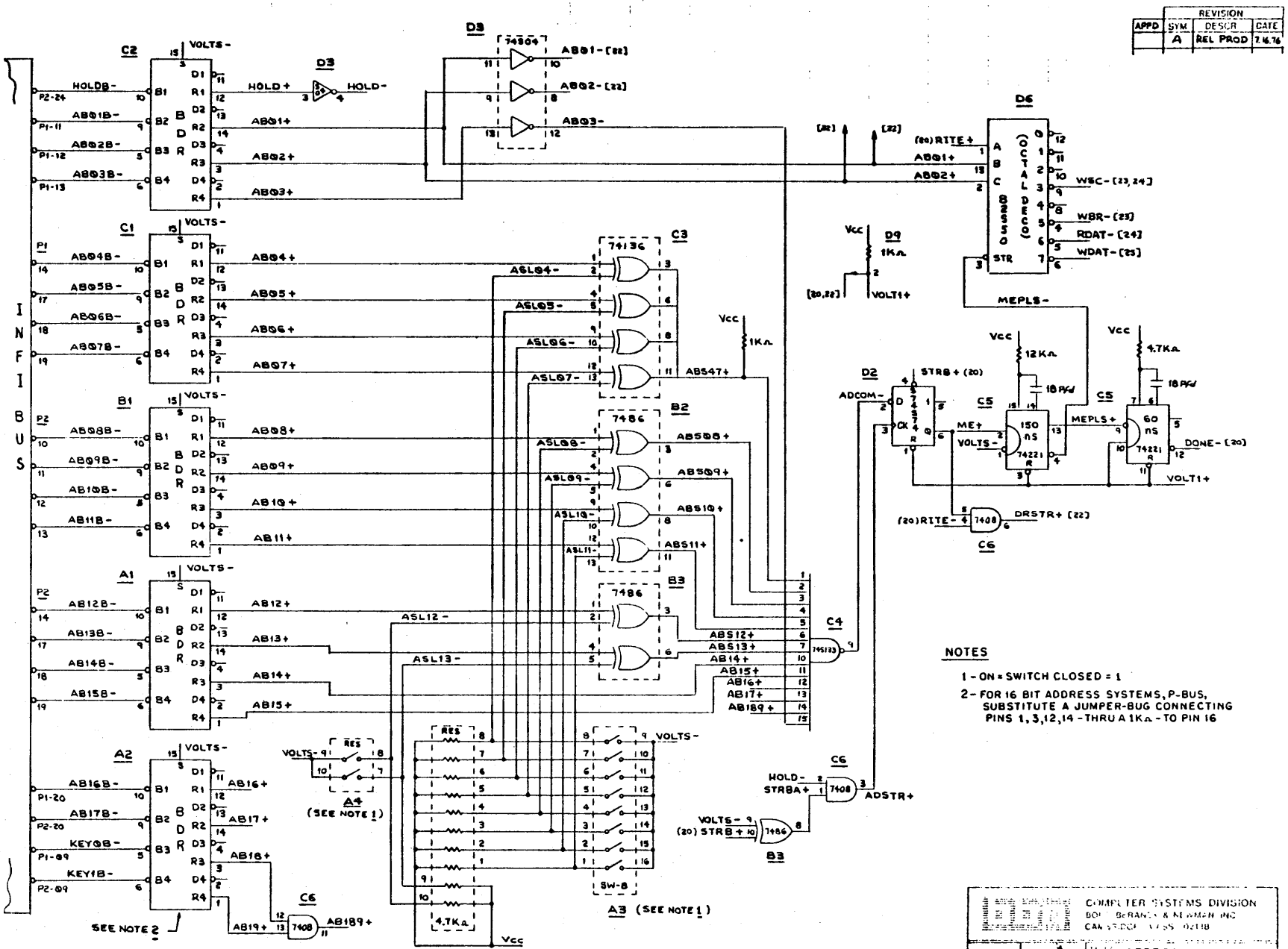


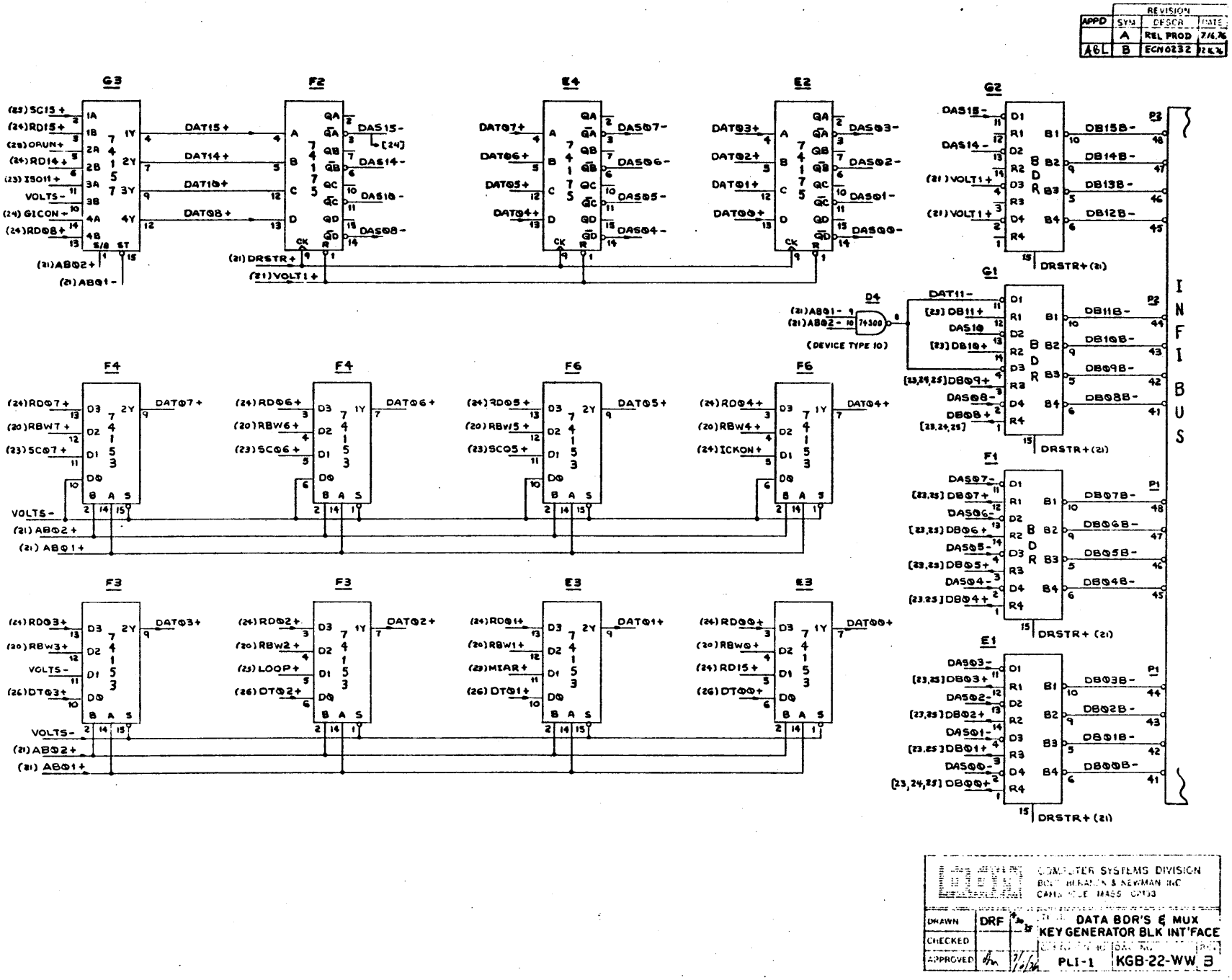
NOTES

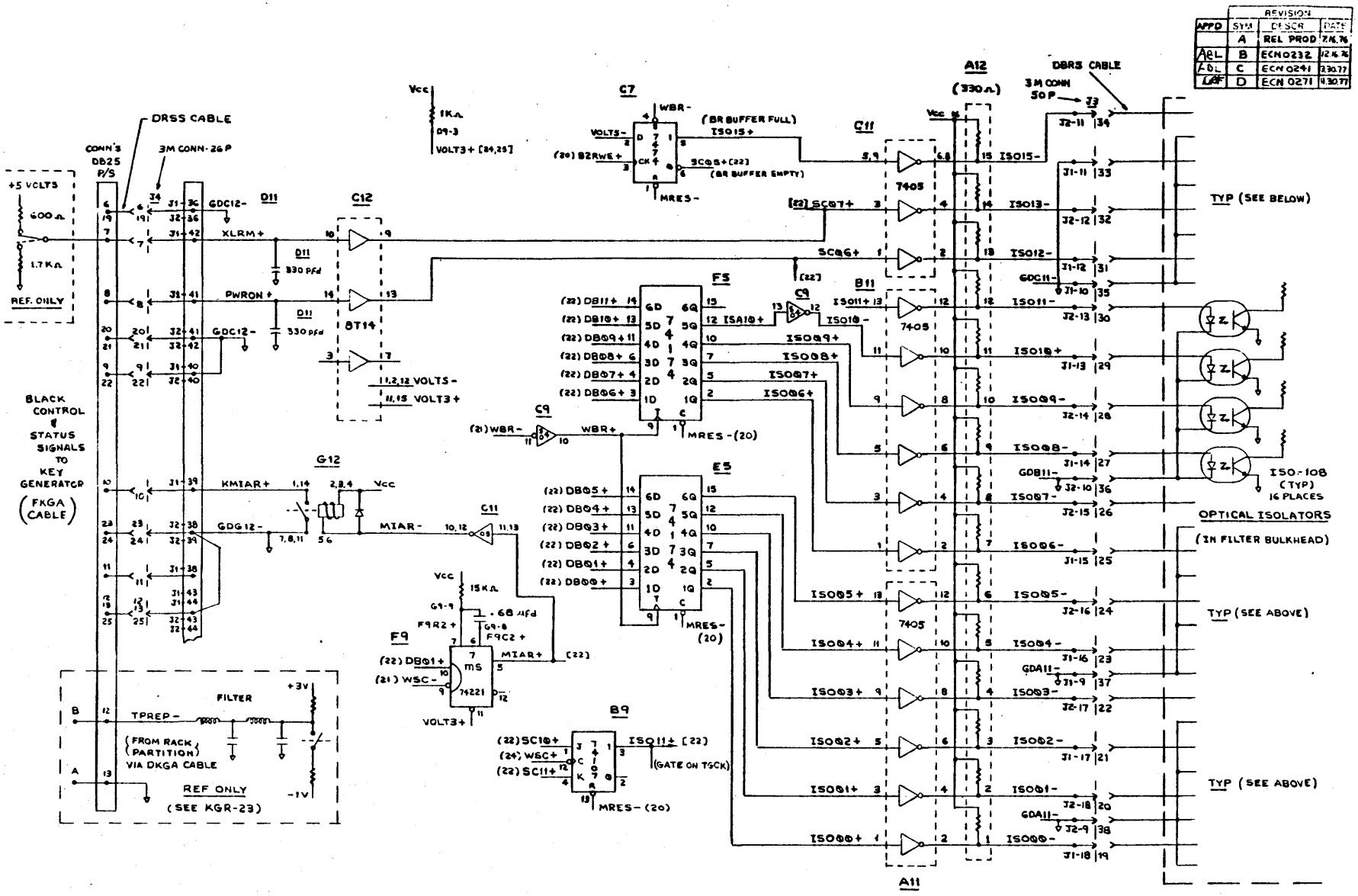
1 THIS UNUSED SIGNAL WIRE (PAIR) IS GROUNDED IN FEED-THRU CAPACITOR BOX, SEE WIRING FCB-20

BBN COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138

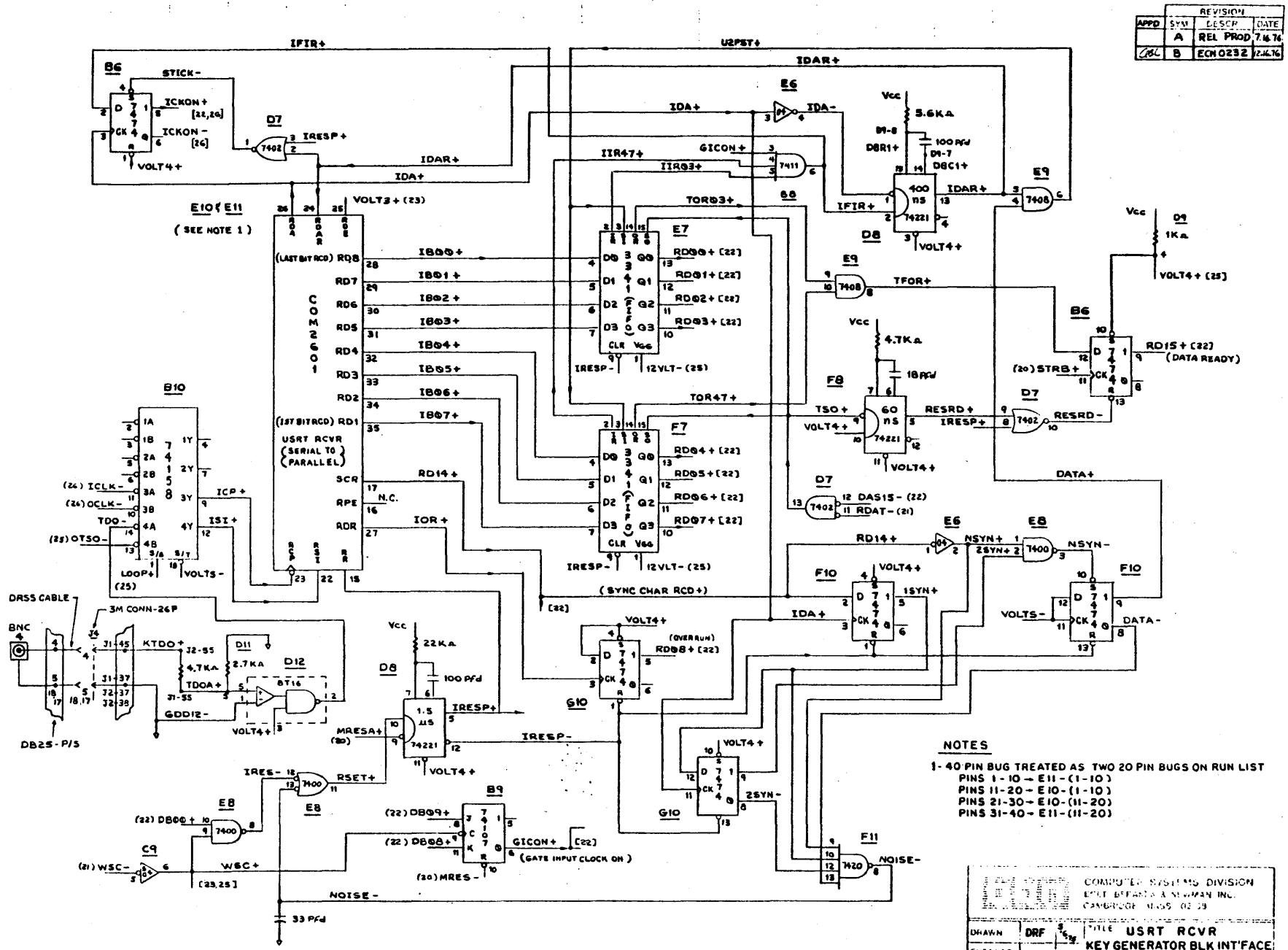
DRAWN	DRF	TITLE	MISC CONT & RB RCVR KEY GENERATOR BLK INT'FACE
CHECKED		COS CONTRACT NO.	DWG NO. / REV
APPROVED		PLI-1	KGB-20-WW C

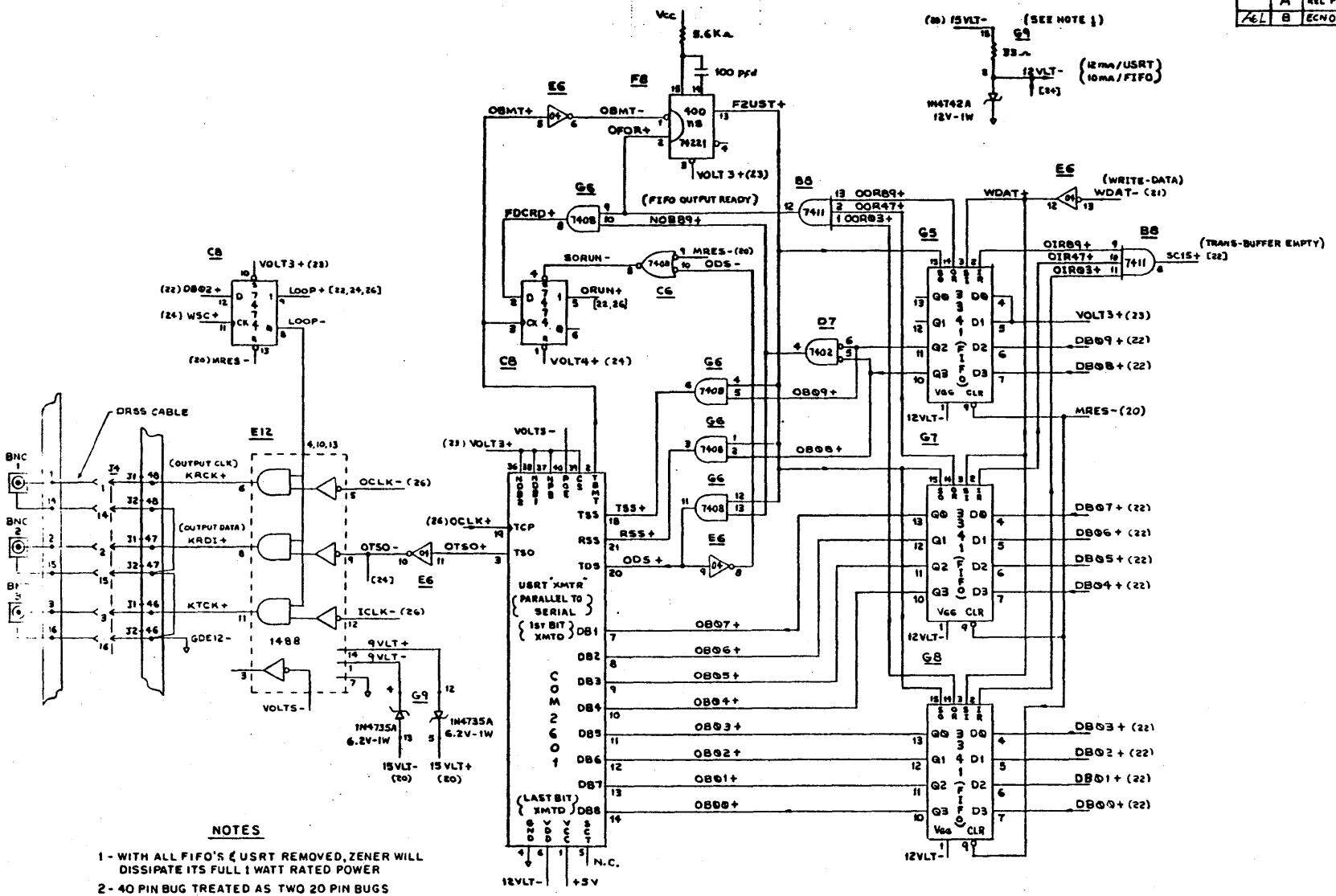

REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7.16.76
INFI BUS
C2
C1
B1
A1
A2
VOLTS-
BDR
HOLDB-
HOLD+
HOLD-
ABS1B-
ABS2B-
ABS3B-
ABS1+
ABS2+
ABS3+
ABS4B-
ABS5B-
ABS6B-
ABS7B-
ABS4+
ABS5+
ABS6+
ABS7+
ABS8B-
ABS9B-
AB10B-
AB11B-
ABS8+
ABS9+
AB10+
AB11+
AB12B-
AB13B-
AB14B-
AB15B-
AB12+
AB13+
AB14+
AB15+
AB16B-
AB17B-
KEY0B-
KEY1B-
AB16+
AB17+
AB18+
AB19+
AB189+
SEE NOTE 2
D3
D8
74804
ABS1-[22]
ABS2-[22]
ABS3-
C3
74136
ASL04-
ASL05-
ASL06-
ASL07-
ABS4+
B2
7486
ASL08-
ASL09-
ASL10-
ASL11-
ABS8+
ABS9+
ABS10+
ABS11+
B3
ASL12-
ASL13-
ABS12+
ABS13+
AB14+
AB15+
AB16+
AB17+
AB189+
C4
74S133
A4
(SEE NOTE 1)
RES
SW-8
A3 (SEE NOTE 1)
B4
4.7KΩ
Vcc
C6
7408
HOLD-
STRBA+
ADSTR+
(20) STRB+
B3
D6
(80) RITE+
ABS1+
ABS2+
WSC-[23,24]
WBR-[23]
RDAT-[24]
WDAT-[23]
STR
MEPLS-
D9
1KΩ
VOLT1+
D2
ADCOM-
STRB+ (20)
C5
ME+
150 nS
74221
MEPLS+
60 nS
DONE-[20]
12KΩ
4.7KΩ
18PFd
(20) RITE-
DRSTR+ [22]
NOTES
1 - ON = SWITCH CLOSED = 1
2 - FOR 16 BIT ADDRESS SYSTEMS, P-BUS, SUBSTITUTE A JUMPER-BUG CONNECTING PINS 1,3,12,14 - THRU A 1KΩ - TO PIN 16
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF 3/25/75
CHECKED
APPROVED
ADDRESS DECODING
KEY GENERATOR BLK INT'FACE
PLI-1 KGB-21-WW A
KGB


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7/6/76
A&L | B | ECN0232 | 12/6/76
G3
F2
E4
E2
G2
G1
F1
E1
F4
F6
F3
E3
D4
74S00
(DEVICE TYPE 10)
DRSTR+(21)
INFIBUS
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF
CHECKED
APPROVED
DATA BDR'S & MUX
KEY GENERATOR BLK INT'FACE
PLI-1
KGB-22-WW B


REVISION
WPD SYM DESCR DATE
A REL PROD 2/6/76
AEL B ECN 0232 2/24/76
ADL C ECN 0241 3/30/77
CAF D ECN 0271 4/30/77
DRSS CABLE
3M CONN-26 P
CONN'S DB25 P/S
+5 VOLTS
600 Ω
1.7 KΩ
REF. ONLY
BLACK CONTROL & STATUS SIGNALS TO KEY GENERATOR (FKGA CABLE)
GDC12-
XLRM+
PWRON+
KMIAR+
GDG12-
MIAR-
330 pfd
8T14
11,12 VOLTS-
11,15 VOLT3+
Vcc
1KΩ
09-3
VOLT3+ [24,25]
C7
WBR-
(BR BUFFER FULL) ISO15+
SCQ5+ [22]
(BR BUFFER EMPTY)
MRES-
(20) B2RWE+
VOLTS-
C11
A12
(330Ω)
DBRS CABLE
3M CONN 50P
J3
7405
SCQ7+ [22]
SCQ6+ [22]
C12
C9
B11
F5
E5
WBR+
MRES-(20)
ISA10+
ISO11+
ISO10-
ISO09+
ISO08+
ISO07+
ISO06+
(22) DB11+
(22) DB10+
(22) DB09+
(22) DB08+
(22) DB07+
(22) DB06+
(22) DB05+
(22) DB04+
(22) DB03+
(22) DB02+
(22) DB01+
(22) DB00+
G12
C11
15KΩ
.68 μfd
F9
F9R2+
F9C2+
(22) DB01+
(21) WSC-
74221
VOLT3+
B9
(22) SC10+
(24) WSC+
(22) SC11+
ISO11+ [22]
(GATE ON TSCK)
MRES-(20)
FILTER
+3V
-1V
TPREP-
(FROM RACK (PARTITION) VIA DKGA CABLE
REF ONLY
(SEE KGR-23)
ISO15-
ISO13-
ISO12-
GDC11-
ISO11-
ISO10+
ISO09-
ISO08-
GDB11-
ISO07-
ISO06-
ISO05+
ISO05-
ISO04+
ISO04-
GDA11-
ISO03+
ISO03-
ISO02+
ISO02-
ISO01+
ISO01-
GDA11-
ISO00+
ISO00-
J2-11 34
J1-11 33
J2-12 32
J1-12 31
J1-10 35
J2-13 30
J1-13 29
J2-14 28
J1-14 27
J2-10 36
J2-15 26
J1-15 25
J2-16 24
J1-16 23
J1-9 37
J2-17 22
J1-17 21
J1-18 20
J2-9 38
J1-18 19
TYP (SEE BELOW)
TYP (SEE ABOVE)
TYP (SEE ABOVE)
ISO-108 (TYP) 16 PLACES
OPTICAL ISOLATORS
(IN FILTER BULKHEAD)
A11
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE MASS. 02138
DRAWN DRF
CHECKED
APPROVED
5-1-78
TITLE OPT. ISOLATORS, KG CONT
KEY GENERATOR BLK INT'FACE
PLI-1
KGB-23-WW D
REV

KGB


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7.16.76
B | ECN 0232 | 12.16.76
IFIR+
U2PST+
IDAR+
B6
STICK-
ICKON+ [22,24]
ICKON- [24]
VOLT4+
D7
7402
IRESP+
IDA+
E6
IDA-
Vcc
5.6KΩ
100 PFd
D8-8
D8R1+
D8-7
D8C1+
400 NS
74221
E9
7408
IDAR+
IFIR+
D8
VOLT4+
IIR47+
IIR03+
GICON+
7411
TOR03+
TOR47+
E10 & E11
(SEE NOTE 1)
VOLT3+ (23)
COM2601
(LAST BIT RCD) RD8
RD7
RD6
RD5
RD4
RD3
RD2
(1ST BIT RCD) RD1
USRT RCVR (SERIAL TO PARALLEL)
SCR
RPE
N.C.
RDR
IBB0+
IBB1+
IBB2+
IBB3+
IBB4+
IBB5+
IBB6+
IBB7+
RD14+
IOR+
E7
FIFO
D0 D1 D2 D3
Q0 Q1 Q2 Q3
CLR Vcc
IRESP-
12VLT- (25)
RDB0+ [22]
RDB1+ [22]
RDB2+ [22]
RDB3+ [22]
RDB4+ [22]
RDB5+ [22]
RDB6+ [22]
RDB7+ [22]
F7
F8
4.7KΩ
18 PFd
60 NS
74221
TSO+
VOLT4+
RESRD+
IRESP+
7402
RESRD-
D7
12 DAS15- (22)
11 RDAT- (21)
D9
1KΩ
VOLT4+ (25)
B6
RD15+ [22]
(DATA READY)
(20) STRB+
DATA+
B10
7415 8
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
(24) ICLK-
(24) OCLK-
TDO-
(23) OTSO-
LOOP+ (25)
VOLTS-
ICP+
ISI+
E6
E8
RD14+
NSYN+
2SYN+
7400
NSYN-
F10
VOLT4+
1SYN+
VOLTS-
DATA-
(SYNC CHAR RCD+) [22]
IDA+
G10
(OVERRUN) RDB8+ [22]
DRSS CABLE
3M CONN-26P
J4
BNC
DB25-P/S
J1-45
J2-55
J1-37
J2-37
J2-38
KTDO+
4.7KΩ
TDOA+
J1-55
GDD12-
D11
2.7KΩ
D12
8T16
VOLT4+
D8
22KΩ
100 PFd
1.5 µS
74221
IRESP+
IRESP-
MRESA+ (20)
VOLT4+
IRES-
7400
RSET+
E8
B9
(22) DB00+
(22) DB01+
(20) MRES-
GICON+ [22]
(GATE INPUT CLOCK ON)
C9
(21) WSC-
WSC+
[23,25]
NOISE-
33 PFd
F11
7420
NOISE-
2SYN-
G10
NOTES
1- 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST
PINS 1-10 → E11-(1-10)
PINS 11-20 → E10-(1-10)
PINS 21-30 → E10-(11-20)
PINS 31-40 → E11-(11-20)
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE MASS 02139
DRAWN DRF
CHECKED
APPROVED
TITLE USRT RCVR
KEY GENERATOR BLK INT'FACE
CUSTOMER PLI-1
KGB-24-WW B
REV



NOTES

1 - WITH ALL FIFO'S & USRT REMOVED, ZENER WILL DISSIPATE ITS FULL 1 WATT RATED POWER

2 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST AS FOLLOWS

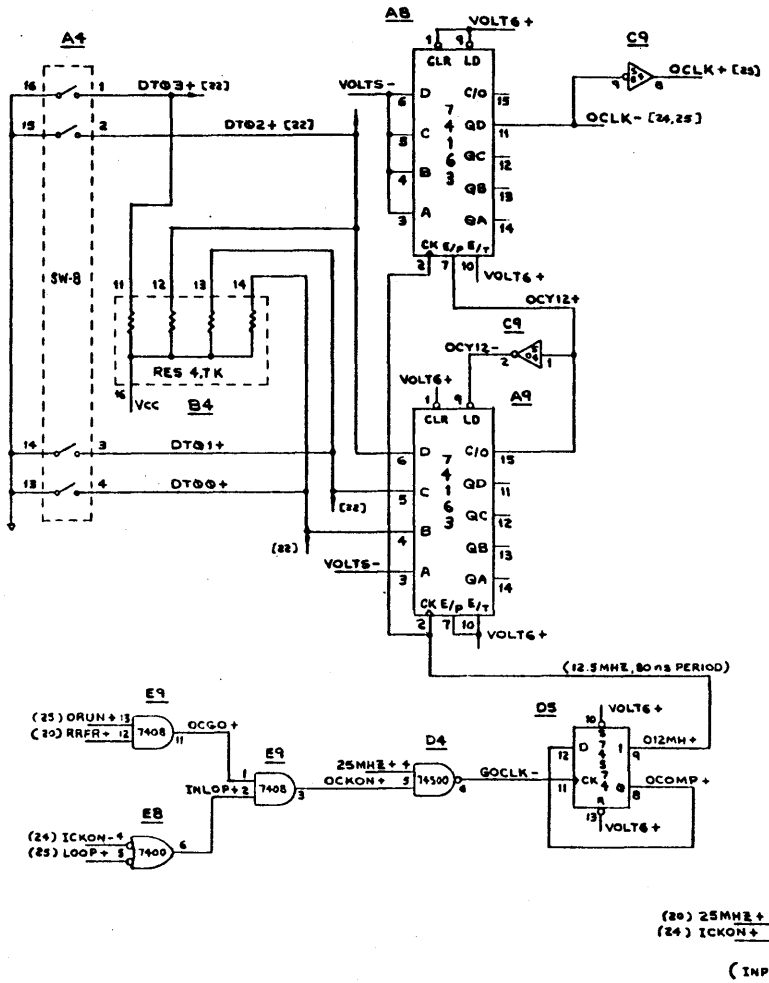
PINS 1-10 → E11 (1-10)
PINS 11-20 → E10 (1-10)
PINS 21-30 → E10 (11-20)
PINS 31-40 → E11 (11-20)

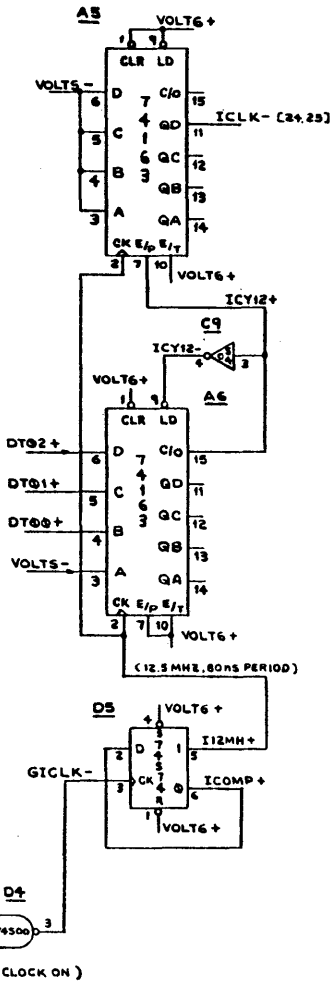
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138

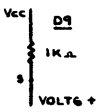
DRAWN	DRF	USRT XMTR KEY GENERATOR BLK INT'FACE
CHECKED		
APPROVED		PLI-1 KGB-25-WW B

KGB

REVISION			
APPD	STR	DESCR	DATE
	A	REL PROD	2.16.76
MCL	B	ECN 0232	12.16.76







NOTE: SWITCH A4-1 = EITHER STATE

SWITCH SETTING TABLE				
NOM. BAUD RT K bits	A4 -2	A4 -3	A4 -4	DATA TYPE BITS
PROHIBITED- (400)				111
200			ON	110
133		ON		101
100		ON	ON	100
80	ON			011
66	ON		ON	010
58	ON	ON		001
50	ON	ON	ON	000

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138

DRAWN	DRF	SIZE B	SERIAL DATA CLK CTRS KEY GENERATOR BLK INT'FACE
CHECKED			
APPROVED		PLI-1	KGB-26-WW B

Key Generator Interface

KGR-Ø2 Logic Description

KGR-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	REL FOR PROD	4/27/78	

KGR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN D. FRANCIS 4/12/78

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

KGR LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		KGR-02

SCALE	REV	SHEET
	A	1 OF 14

KGR Interface
Logic Description

Revised February 6, 1979 by A. Lake

The KGR card allows the connection of the Red side of a Series 30 Key Generator (KG) to a Private Line Interface (PLI). Understanding of this logic description requires a knowledge of the KGR and KGB Functional Specifications, in addition to the data sheets on the COM-2601 USRT integrated circuit (Universal Synchronous Receiver Transmitter), the 3341 FIFO memory chip, and the ISO-108 optical isolator. A detailed understanding of the KG unit itself is not required, but familiarity with it (through the PLI Maintenance Guide) will be useful. Signals signed + are true when at a TTL high, and signals signed - are true when low.

KGR

Drawing KGR-20: MISC CONTROL & RED-TO-BLACK BUFFER

Drawing 20 contains the buffering for various Infibus control signals, and the Red-to-Black word data register. The Red-to-Black word data bits (RBW0 through RBW7) are strobed from the Infibus into the holding register by the assertion of Transmitter Prep (SC 03). Because TPREP is generated by a 6 milli-second oneshot (see KGR-23), the Red-to-Black word is bandwidth limited to approximately 180 words per second for security reasons. The Red-to-Black Bus Reset (RBBR) signal is also strobed by TPREP and therefore bandwidth limited for the

same security reasons. In actual operation the TPREP and RBBR signals cause such noticeable and significant effects in the Black PLI that the real clear-path bandwidth available between Red and Black will be orders of magnitude lower.

The inverters shown in the upper right hand corner are used to drive the cable going to the KGB card. The Black-to-Red-Word Empty (B2RWE) flow control line shown on this drawing and the RRFR control signal on KGR-24 join the aforementioned RBBR and RBW0-7 to form the eleven Red-to-Black signals which are filtered in the PLI Feedthrough Capacitor Assembly, and ultimately terminate on drawing KGB-20. (12 capacitors are actually installed in the PLI bulkhead to provide for future expansion.)

In the upper left, the discontinous Infibus signals are carried from one side of the Infibus connector to the other, including the precedence pulse PCDAB+. The remaining four Infibus signals used actively in the KGR card are the: Strobe, Done Pulse, Master Reset, and Rite signals. These are interfaced in the BDR D1. The status of the Rite signal during a particular memory reference is held in a flip-flop whose outputs are RITE+ and RITE-. In addition, there are 4 single-pole switches and their associated pull-up resistors used to generate signals in the Card-Type word (DT00 through DT03). These presently perform no active logic function but may be used to indicate baud rates or identify individual cards in a system.

KGR-21: ADDRESS DECODING

Drawing 21 shows the interface address decoding for this card. The logic is straightforward and conventional. At the left are 5 BDRs providing a direct interface to the INFIBUS. Their inputs are unused (left floating but gated off by grounding the strobes), and their outputs are used as part of the address selection logic. The switches on the card are used to select the address to be recognized by an individual card. To the right of center is a 13-input NAND-gate, whose output ADCOM- indicates that the address specified on the bus matches the switch settings on the card. Its inputs include bits 16-19 ungated, and bits 4-13 as selected by switches shown at the bottom of the drawing. Also included is AB03-, as the KGB device registers only occupy the lower 8 bytes of the 16 byte address space specified by AB04 thru AB19.

The 7486 and 74136 bugs are exclusive-OR circuits used for address comparison. Note 1 on the drawing indicates that a switch closure is used to specify recognition of a 1 in the corresponding address bit. It does this by grounding the 1 input of the exclusive-or circuit associated with it. For example, with ASL11- grounded by the lowest switch in the leftmost switch of A3, a positive gate output ABS11+ will occur when the second gate input AB11+ is high. This will occur when the associated BDR input is low, indicating assertion of AB11B- on the INFIBUS. The output of the 10 gates in C3, B2, and B3 is a wired-AND configuration going high only when bits 4-13 compare correctly.

At the bottom of the drawing, an additional de-skewing gate is used to delay the strobe pulse STRB+ by an amount equivalent to the delay in the individual data bits before triggering the flip-flop whose output is ME+. A gate is also provided to inhibit ADSTR+ from clocking the flip-flop if the bus HOLD signal is present. Note that until the address selection cycle is started, the STRB+ pulse keeps the flip-flop in the "1" state. ME+ is a synchronized address selection signal used for all subsequent address dependent functions. Following this flip-flop is a 150 ns delay whose output ultimately generates a 60 ns DONE pulse. Below this circuit is a single AND-gate whose output DRSTR+ is used to strobe the data BDRs during a read operation.

In the upper right corner of the drawing is an octal decoder used for strobing or reading the appropriate interface registers. Its inputs are the RITE signal, and the low order address bits 1 and 2, all strobed by MEPLS+.

KGR-22: DATA BDR's and MUX

Drawing 22 contains the data multiplexer and BDRs used to interface with the data portion of the INFIBUS. The 4 BDRs are shown at the right of the drawing; their non-bus outputs in all cases go to other drawings. Each of their inputs comes from a flip-flop used to synchronize the data information with the INFIBUS reading cycle. The flip-flops themselves are contained on three circuits near the top center of the drawing. In all three cases the strobe used to latch the data is the data-read strobe DRSTR+. Note that this is the same signal

used to strobe the BDRs themselves. This does not prohibit change of the signals on the INFIBUS at the beginning of the cycle, but the 150 ns duration of DRSTR+ is sufficient to ensure stabilization of outputs by the end of the cycle, when the signals are used on the bus.

The remaining logic is part of the data multiplexer. The low order 2 bits of the address decoding are brought in at the bottom of each bug, and the data bits to be decoded are brought in at the left. The KGR Functional Specification's bit assignment chart will be of considerable help in understanding the origin of these signals.

KGR-23. OPT ISOLATORS and KG CONTROL

Logic for communicating over the Black-to-Red path through the optical isolators is shown on KGB-23 and KGR-23. A new B-R word is sensed by the assertion of the IS015 line which, after appropriate filtering and deskewing, causes the 12 data bits to be clocked into the B-R register (A10 and B10 in the center of the drawing.) The 189 micro-second oneshot at the top center of the drawing is used to both deskew the incoming data bits and also insure that noise on the IS015 line does not cause false detection of spurious B-R words. Two gate delays after the oneshot times out, the Word Ready flipflop is clocked and, if IS015 is still asserted the Red PLI program is informed of a new B-R word via bit BR15. The delay of ISOWA clocking the Word Ready flipflop is necessary to insure the validity of the B-R word register when BR15 is asserted, but also produces an undesirable "runt" pulse on the B2RWE flow control line. This spurious pulse is of approximately 30 nanoseconds in duration and is therefore completely filtered out by the feedthrough capacitors in the B2RWE line to the KGR card.

Bits BR00 through BR09 form the Black-software-to-Red-software data path, while BR10 and BR11 are reserved for hardware functions. BR10 is used by Black to reset Red's bus, as shown in upper right corner of the drawing. Dual 7438 buffers are used to drive the PWTST line on the Infibus, assertion of which initiates a Master Reset and software restart sequence in the Red PLI. BR11 is used on KGR-25 to gate on the transmitter clock, and may also be read by the Red PLI software.

The 6 milli-second oneshot in the lower right hand corner is used to generate the TPREP pulse and strobe the Red-to-Black word (see KGR-20) whenever SC03 is written with a "1". The discrete network surrounding the TPREP relay has survived for historical reasons and continues to defy circuit analysis. The neighboring 60 ns oneshot is used to clear the Word Ready flipflop when the B-R word is read and it contains a new word.

KGR-24: USRT Receiver

The normal sequence of events controlling this portion of the logic is as follows: During initialization the program will have stored a Receive-Sync character in the USRT. A random serial data stream will arrive on the ISI + line from the multiplexer shown on KGR-25 and will appear at pin 22 of the USRT. When appropriate to get in message sync (analogous to Modem sync) a Receiver Reset is issued by setting bit 00 of the SC word. In the lower left of the drawing, this asserts IRES and RSET and fires a oneshot that provides the pulse required by the USRT. This places the USRT into "SYN-search" mode, and

the USRT scans the serial data for eight bits that match the pre-specified Receiver-sync character.

When a SYN is received, pin 17 is raised (RD14) priming the 1SYN flipflop just before assertion of the Input Data Available (IDA) signal from the USRT pin 26. Two or more adjacent SYNs are required for valid message sync, so if the second byte received is not SYN the four inputs of the NOISE gate (bottom center) are high and the IRESP oneshot is pulsed again, reinitializing SYN-search. The 33pf capacitor stretches the NOISE signal enough to prevent a runt pulse on the oneshot input.

If the byte following the SYN is a second SYN the 2SYN flipflop will be set by the following IDA pulse, and one input of the NSYN-gate will be asserted. This state will remain for as long as additional SYNs are received. However, when the first non-SYN is received NSYN is asserted and the DATA flipflop is set, concluding the SYN-search mode. The four-input NOISE gate is disabled so that further SYNs in the data stream will be ignored until the program initiates SYN-search mode again.

In the data mode, as long as the input rank of the FIFOs is empty, (IIR signals), the presentation of a new byte at the USRT outputs (IDA asserted) will trigger the 400nS oneshot. This produces Input Data Available Reset (IDAR) which strobes the data from the USRT to the FIFO (U2FST) and clears the RDA signal, although the sluggishness of the USRT makes the RDA pulse last about 100 nS in what would otherwise be a runt situation.

In the event that the FIFO memory is full, IFIR at the oneshot input will be negated, and no IDAR will be generated by the IDA signal which now will remain asserted. This situation will remain until the FIFO ceases to be full, at which time the IDAR oneshot will fire and the RRFR + signed will again be asserted to the BPLI. Note that prior to data mode, since the FIFOs will have been cleared by IRESP, an IDAR will alaways follow IDA and keep the clock going even though no bytes will be strobed into the FIFOs.

When the FIFO input byte percolates to the FIFO outputs, the Transmitter FIFO Output-Ready (TFOR) signal is asserted. This is synchronized with the Infibus STRB signal and presents a Data Ready signal to the program as bit 15 of the Read Data word. The program will periodically read the data word and ignore it unless it is negative (bit 15 is set). When it does read a negative data word, the combination of DAS15 and RDAT produces TSD which clears both the Data Ready flipflop (via the GOns oneshot in the right center of the drawing)and the output rank of the FIFOs.

KGR-25: USRT Transmitter

Drawing 25 shows the serial output portion of the KGR, which interfaces the Red side of the KG Receiver. The MIL-188 data driver (9616) is shown to the left of the USRT. The output, is about + or - 6 volts, and is source terminated. The driver is gated off during LOOP test.

Bits 0-9 of the Data Bus are buffered in the three FIFO memory chips. When the input rank of the FIFOs is empty, a three input gate asserts SC15 signifying that the Transmitter Buffer is Empty. The program, sensing this Status/Control bit, can store a new data byte into the FIFO.

The write data signal WDAT will shift the data bus bits into the FIFOs, dropping the Empty signal until the first rank is empty again.

When the 10-bit byte reaches the output rank of the FIFOs, OFOR (Output FIFO Output Ready) will fire the 400 nS oneshot if the USRT's Transmitter Buffer Empty (OBMT) signal is high, or wait for it to go high. When both conditions are satisfied the FIFO-to-USRT Strobe (F2UST) transfers the FIFO byte into the USRT. As outlined in the Functional Specs, if bits 8 or 9 are set, the remaining 8 bits are transferred to the SYN-character holding registers inside the USRT. If neither 8 nor 9 is present (NOB89) bits 0-7 will enter the USRT data register.

KGR-Ø2 LOGIC DESCRIPTION - APPENDIX 1

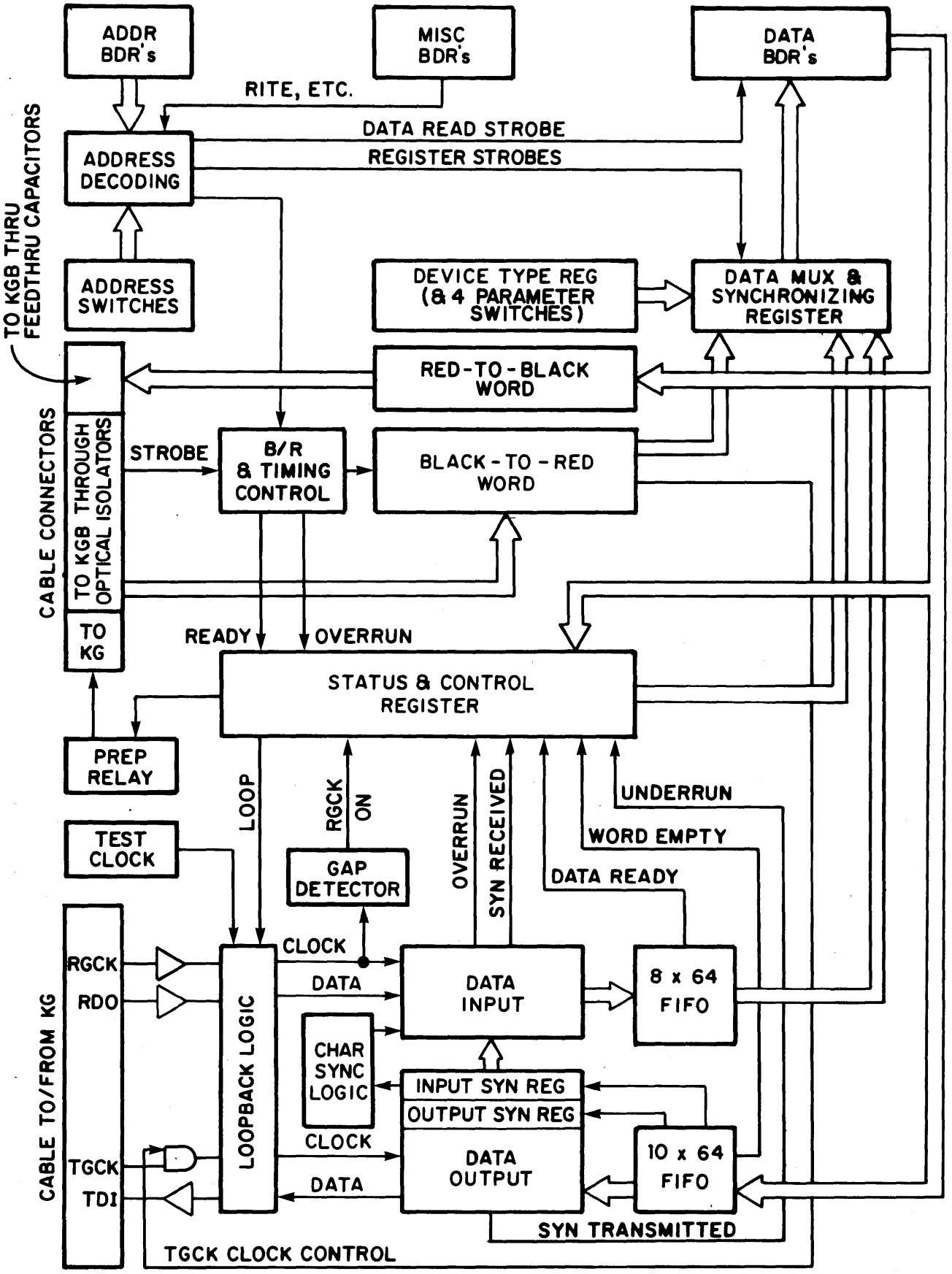


Figure 1-1 KGR Block Diagram

KGR

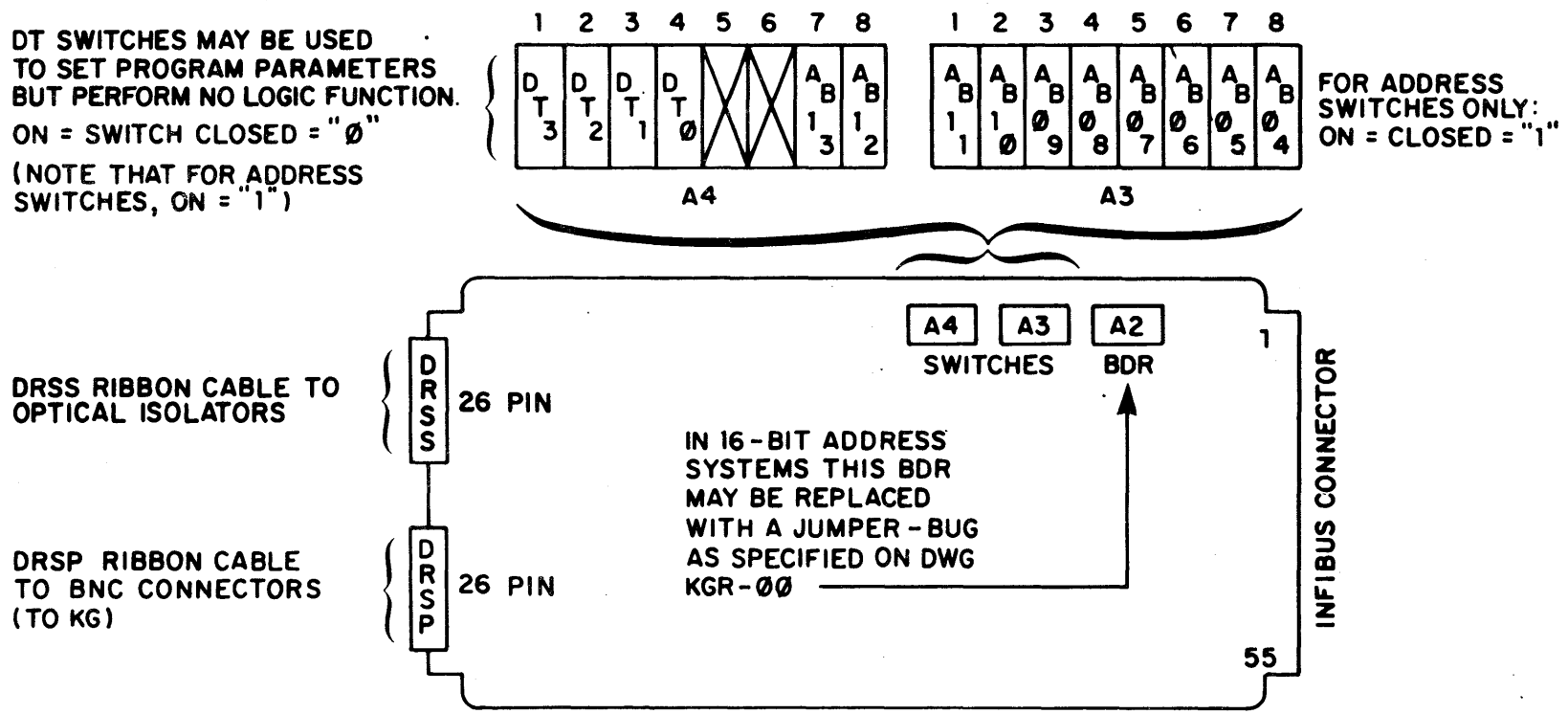


Figure 1-2 KGR Switches and Connectors

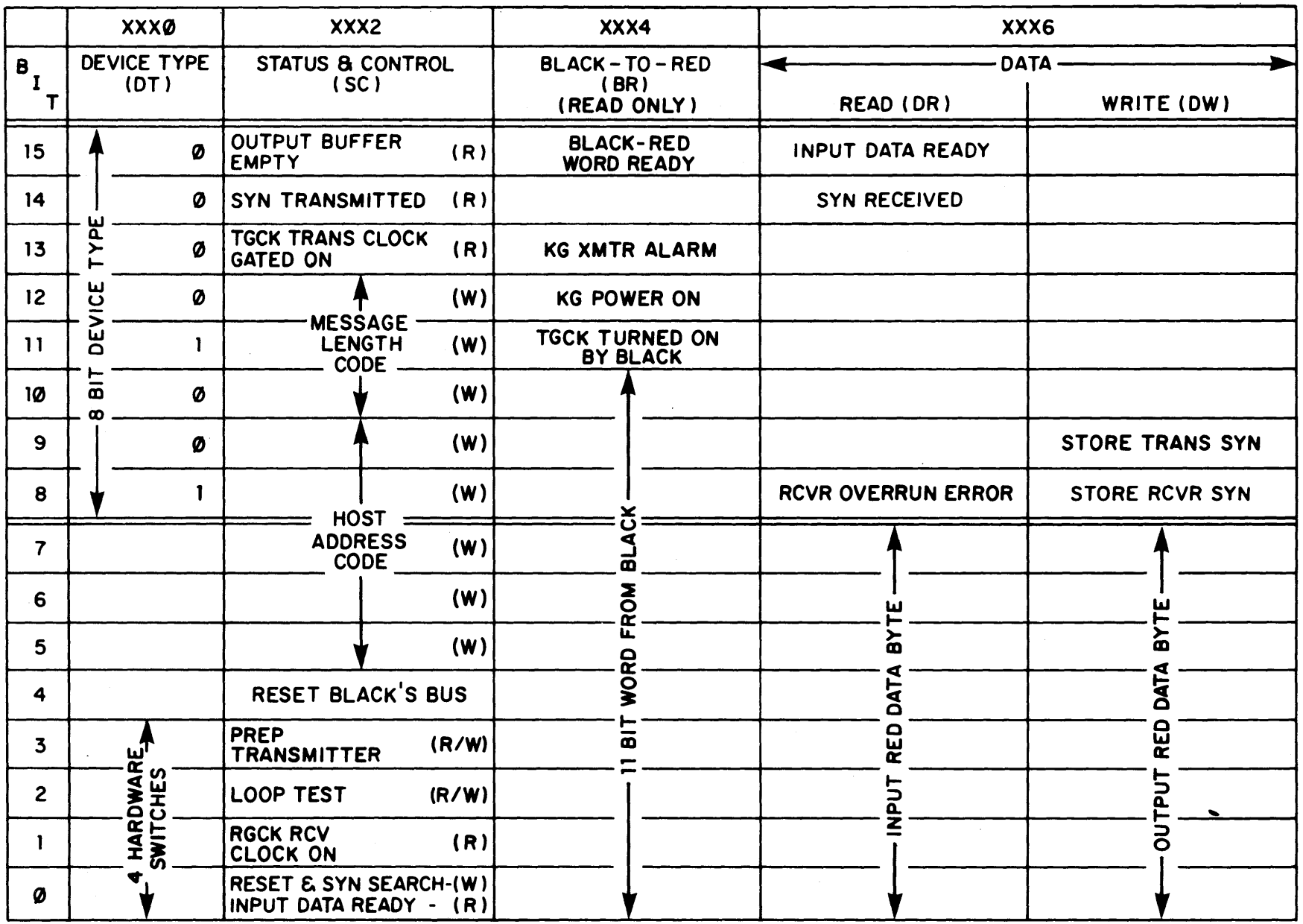
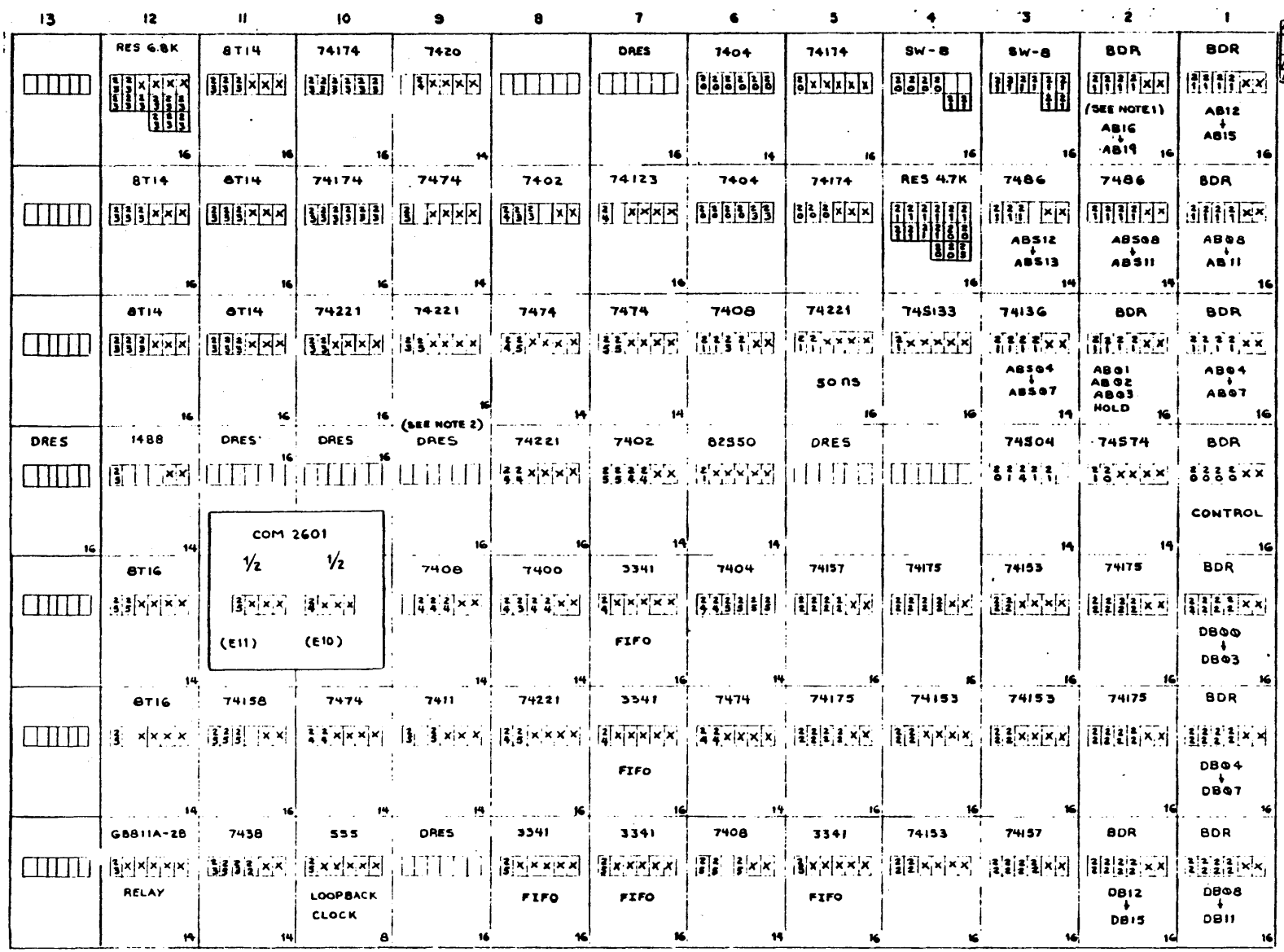


Figure 1-3 KGR Bit Assignments

KGR-2Ø SCHEMATICS

KGR



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7/6/76
APD	B	ECN0233	12-6-76
APD	C	ECN0242	2-24-77

TOP VIEW

NOTES:

1 - IN 16 BIT ADDRESS SYSTEM, REPLACE A2 WITH COMPONENT-BUG, CONNECTING PINS 1, 3, 12 & 14 TO PIN 16 THRU A 1K-1/4 W RESISTOR

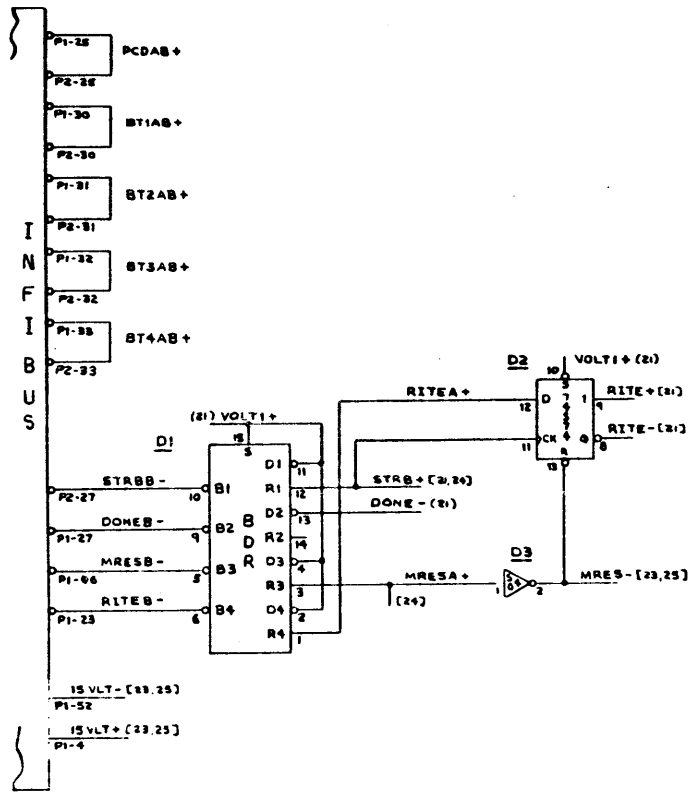
2 - POSITION H-9 IS LOCATED BETWEEN C-9 & D-9 SEE ASSY DWG KGR-10

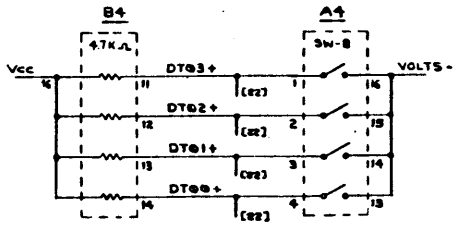
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

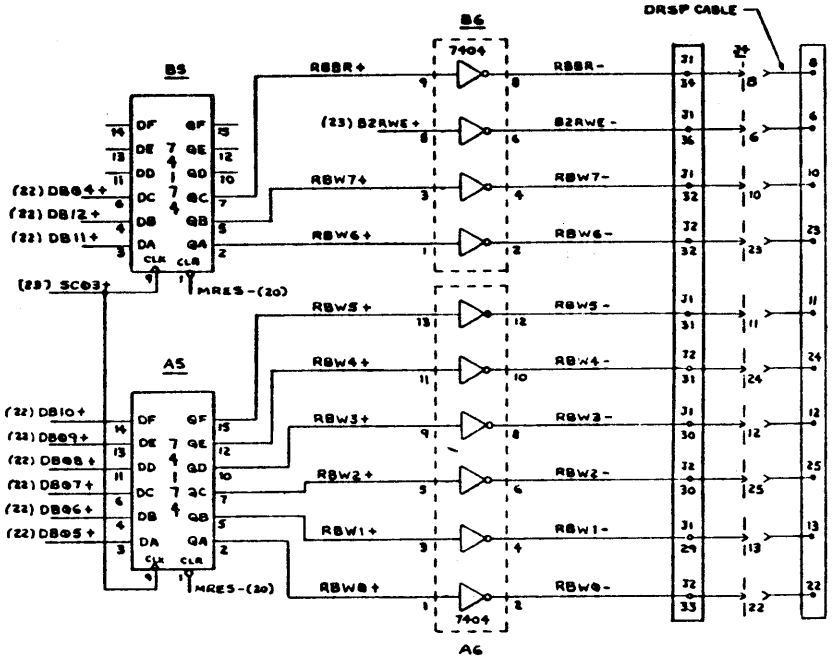
DRAWN	S.E.T.	4-11-75	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED				
APPROVED		7/6/76	CUSTOMER/NO. PLI-1	DWG NO. KGR-00-WW REV C

KGR

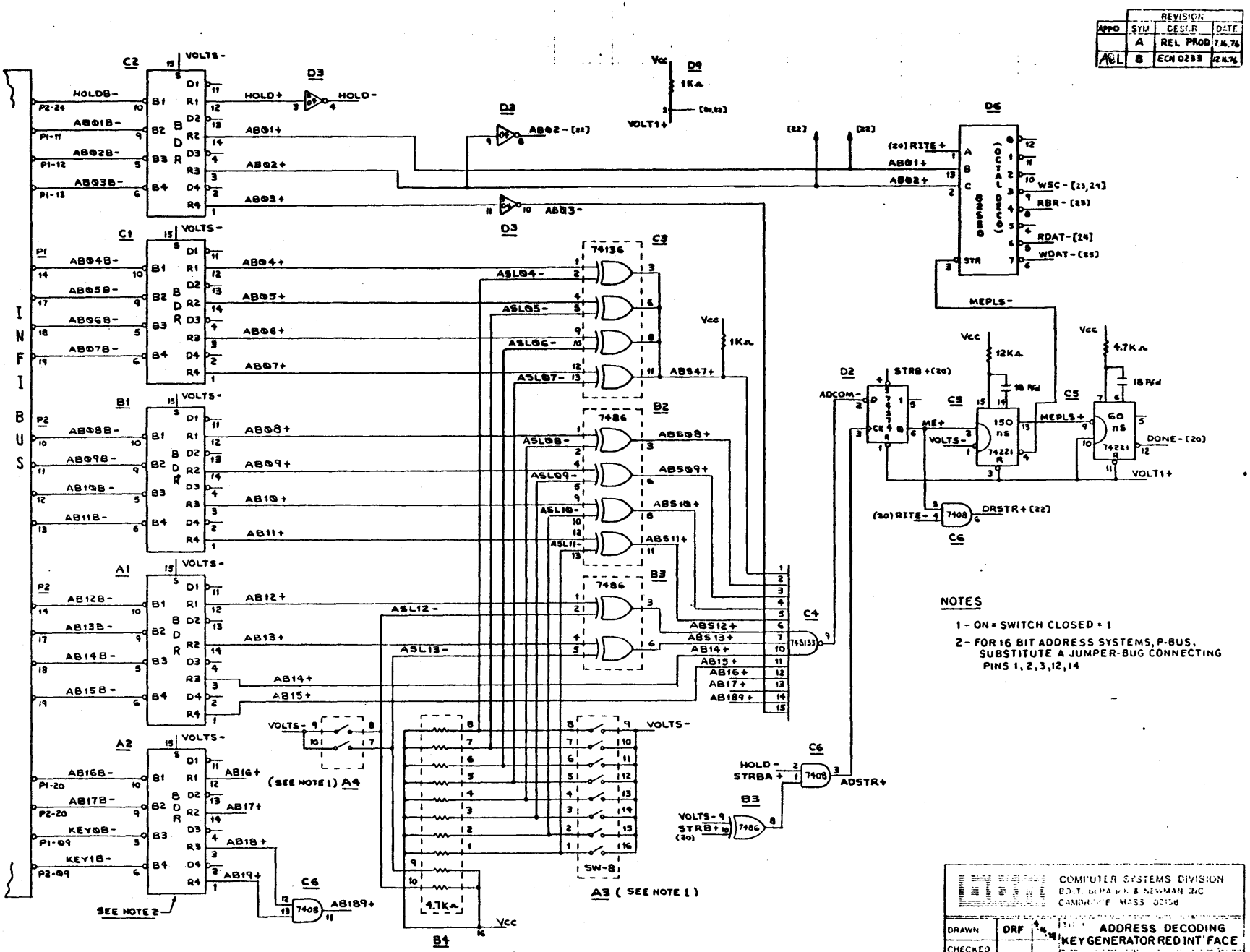
REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	7/11/75	
B	ECN 0233	8/19/75	ARL

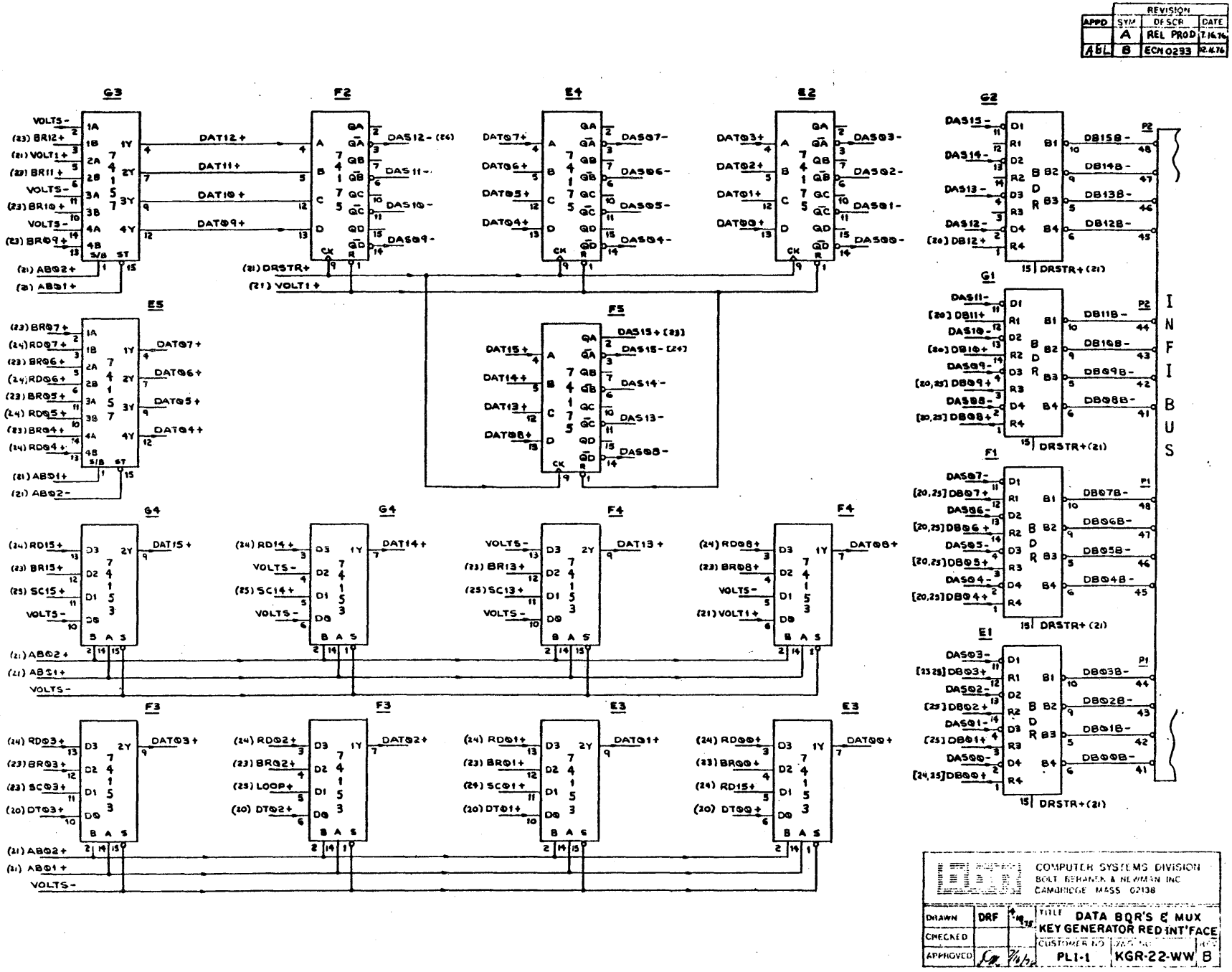






			SIZE
COMPUTER SYSTEMS DIVISION BOLT BERANEK & NEWMAN INC CAMBRIDGE MASS 02138			
DRAWN	DRF	TITLE	MISC CONT & RB BUFFER KEY GENERATOR RED INT FACE
CHECKED		CODE IDENT NO	DWG NO / REV
ENG APPD			KGR-20-WW, B


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7.16.76
AEL | B | ECN 0233 | 12.16.76
INFIBUS
C2
C1
B1
A1
A2
BDR
VOLTS-
HOLDB-
AB01B-
AB02B-
AB03B-
AB04B-
AB05B-
AB06B-
AB07B-
AB08B-
AB09B-
AB10B-
AB11B-
AB12B-
AB13B-
AB14B-
AB15B-
AB16B-
AB17B-
KEY0B-
KEY1B-
HOLD+
HOLD-
AB01+
AB02+
AB03+
AB04+
AB05+
AB06+
AB07+
AB08+
AB09+
AB10+
AB11+
AB12+
AB13+
AB14+
AB15+
AB16+
AB17+
AB18+
AB19+
AB189+
SEE NOTE 2
D3
D9
1Kᴀ
VOLT1+
D6
OCTAL DECODER
RITE+
WSC-[23,24]
RBR-[23]
RDAT-[24]
WDAT-[25]
STR
MEPLS-
D2
STRB+[20]
ADCOM-
C3
12Kᴀ
18 Pfd
150 ns
74221
C5
4.7Kᴀ
60 ns
DONE-[20]
VOLT1+
ME+
MEPLS+
C6
7408
DRSTR+[22]
NOTES
1 - ON = SWITCH CLOSED = 1
2 - FOR 16 BIT ADDRESS SYSTEMS, P-BUS, SUBSTITUTE A JUMPER-BUG CONNECTING PINS 1,2,3,12,14
C9
74136
ASL04-
ASL05-
ASL06-
ASL07-
AB04+
AB05+
AB06+
AB07+
AB04T+
B2
7486
ASL08-
ASL09-
ASL10-
ASL11-
AB08+
AB09+
AB10+
AB11+
AB08T+
AB09T+
AB10T+
AB11T+
B3
7486
ASL12-
ASL13-
AB12+
AB13+
AB14+
AB15+
C4
74S133
AB12T+
AB13T+
AB14+
AB15+
AB16+
AB17+
AB189+
A4
(SEE NOTE 1)
A3 (SEE NOTE 1)
SW-8
4.7Kᴀ
B4
Vcc
HOLD-
STRBA+
ADSTR+
STRB+
(20)
COMPUTER SYSTEMS DIVISION
B.B.N. BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF
CHECKED
APPROVED
ADDRESS DECODING
KEY GENERATOR RED INT'FACE
PLI-1
KGR-21-WW B
KGR


REVISION
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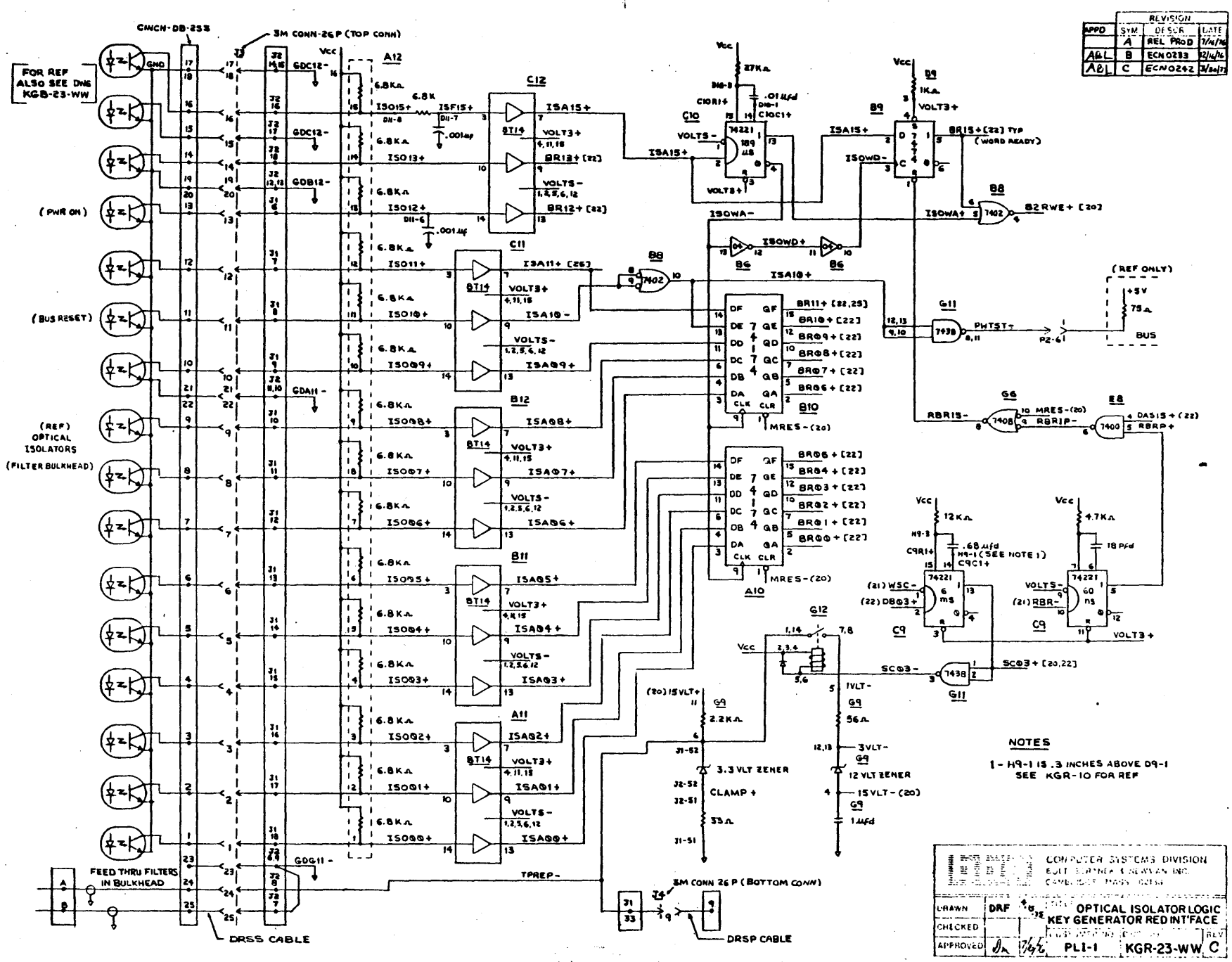
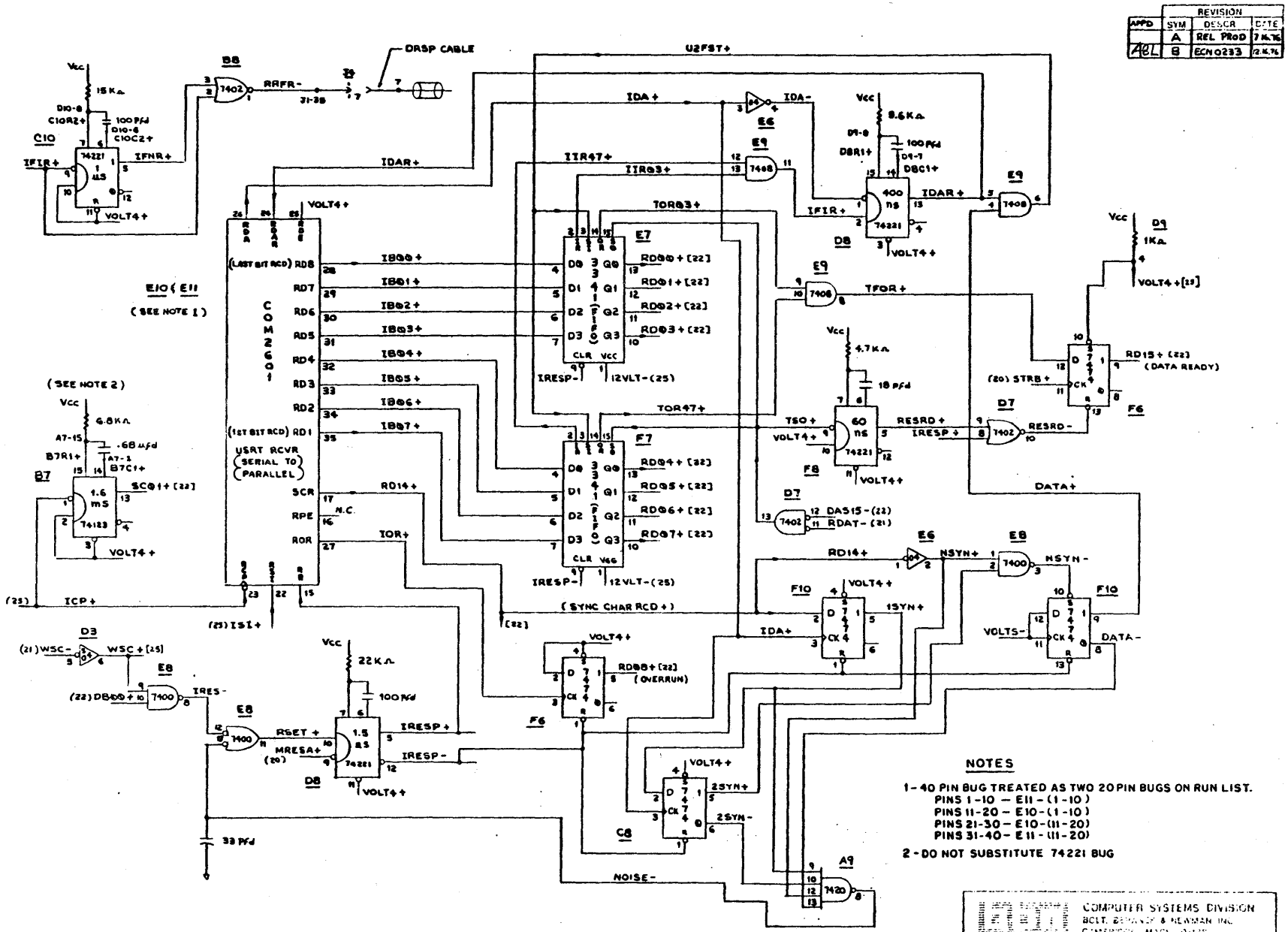
ABL | B | ECN 0293 | 12.4.76
G3
F2
E4
E2
G2
G1
F1
E1
E5
F5
G4
F4
F3
E3
INFIBUS
VOLTS-
DAT12+
DAT11+
DAT10+
DAT09+
DAS12-
DAS11-
DAS10-
DAS09-
DRSTR+
VOLT1+
DAT07+
DAT06+
DAT05+
DAT04+
DAS07-
DAS06-
DAS05-
DAS04-
DAT03+
DAT02+
DAT01+
DAT00+
DAS03-
DAS02-
DAS01-
DAS00-
DAS15-
DAS14-
DAS13-
DAS12-
DB15B-
DB14B-
DB13B-
DB12B-
DAS11-
DAS10-
DAS09-
DAS08-
DB11B-
DB10B-
DB09B-
DB08B-
DAS07-
DAS06-
DAS05-
DAS04-
DB07B-
DB06B-
DB05B-
DB04B-
DAS03-
DAS02-
DAS01-
DAS00-
DB03B-
DB02B-
DB01B-
DB00B-
DAT15+
DAT14+
DAT13+
DAT08+
DAS15-
DAS14-
DAS13-
DAS08-
DAT15+
DAT14+
DAT13+
DAT08+
DAT03+
DAT02+
DAT01+
DAT00+
ABS02+
ABS01+
VOLTS-
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF
CHECKED
APPROVED
TITLE DATA BQR'S & MUX KEY GENERATOR RED INT'FACE
CUSTOMER NO PLI-1
KGR-22-WW B


CINCH-DB-25S
3M CONN-26P (TOP CONN)
FOR REF ALSO SEE DWG KGB-23-WW
(PWR ON)
(BUS RESET)
(REF) OPTICAL ISOLATORS (FILTER BULKHEAD)
FEED THRU FILTERS IN BULKHEAD
DRSS CABLE
3M CONN 26P (BOTTOM CONN)
DRSP CABLE
A12
C12
C11
B12
A11
A10
B10
B9
B8
B6
C10
C9
G11
G12
G9
G6
E8
ISA15+
ISA11+ [26]
ISA10+
ISA09+
ISA08+
ISA07+
ISA06+
ISA05+
ISA04+
ISA03+
ISA02+
ISA01+
ISA00+
ISO15+
ISO13+
ISO12+
ISO11+
ISO10+
ISO09+
ISO08+
ISO07+
ISO06+
ISO05+
ISO04+
ISO03+
ISO02+
ISO01+
ISO00+
ISOWA-
ISOWD-
ISOWA+
ISOWD+
B2RWE+ [20]
BR15+ [22] TYP (WORD READY)
BR13+ [22]
BR12+ [22]
BR11+ [22,25]
BR10+ [22]
BR09+ [22]
BR08+ [22]
BR07+ [22]
BR06+ [22]
BR04+ [22]
BR03+ [22]
BR02+ [22]
BR01+ [22]
BR00+ [22]
MRES-(20)
PHTST+
P2-61
BUS
+5V
RBR15-
RBRP-
DAS15+ (22)
RBRP+
(21) WSC-
(22) DB03+
(21) RBR-
SC03+ [20,22]
SC03-
(20) 15VLT+
3.3 VLT ZENER
CLAMP +
12 VLT ZENER
15VLT-(20)
3VLT-
VOLT3+
VOLTS-
TPREP-
GDC12-
GDB12-
GDA11-
GDG11-
VCC
GND
(REF ONLY)
NOTES
1 - H9-1 IS .3 INCHES ABOVE D9-1
SEE KGR-10 FOR REF
REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7/4/16
A&L | B | ECN0233 | 12/4/16
A&L | C | ECN0242 | 3/20/17
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DAF
CHECKED
APPROVED
OPTICAL ISOLATOR LOGIC
KEY GENERATOR RED INT'FACE
PLI-1
KGR-23-WW
REV C

KGR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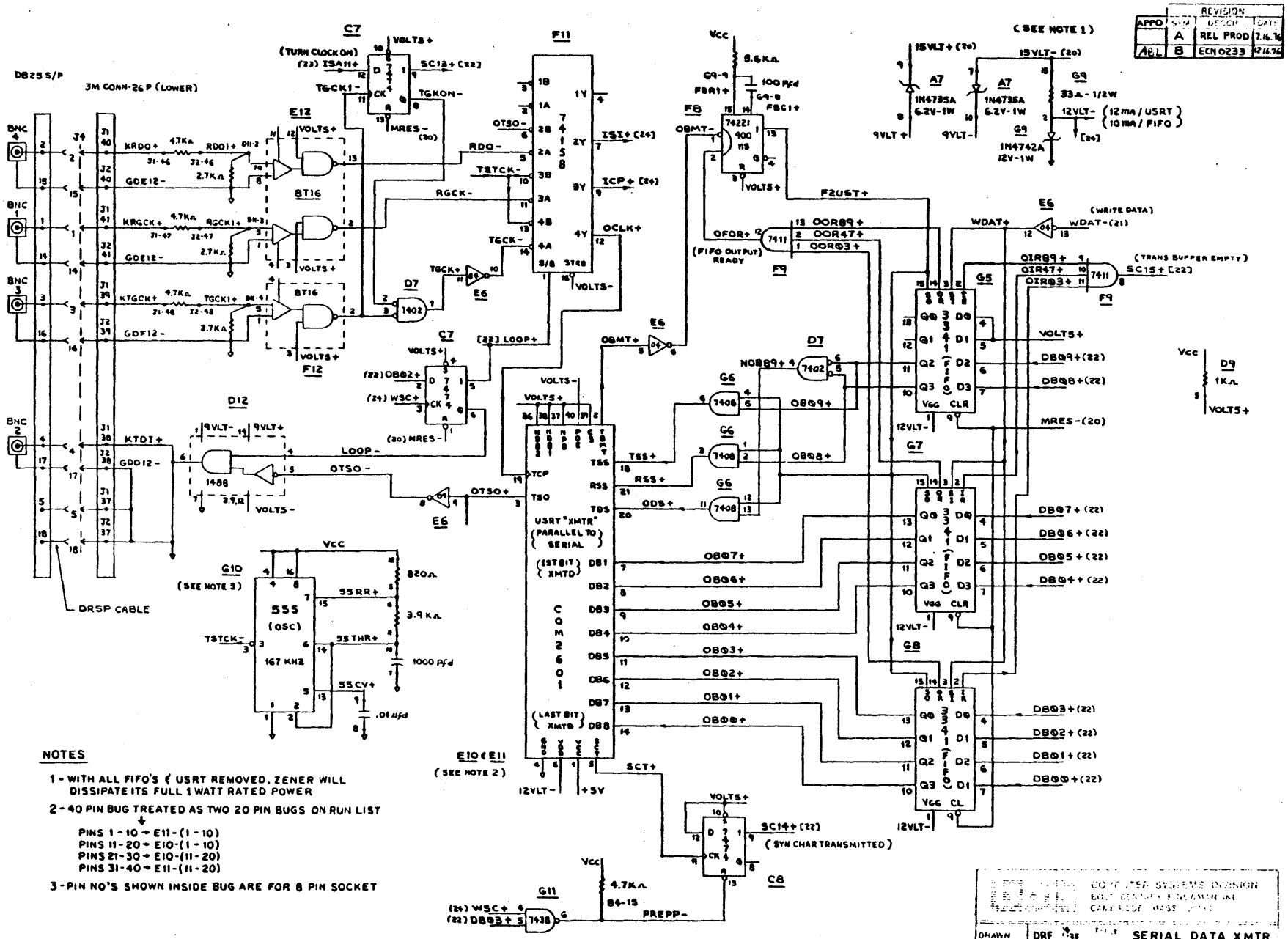
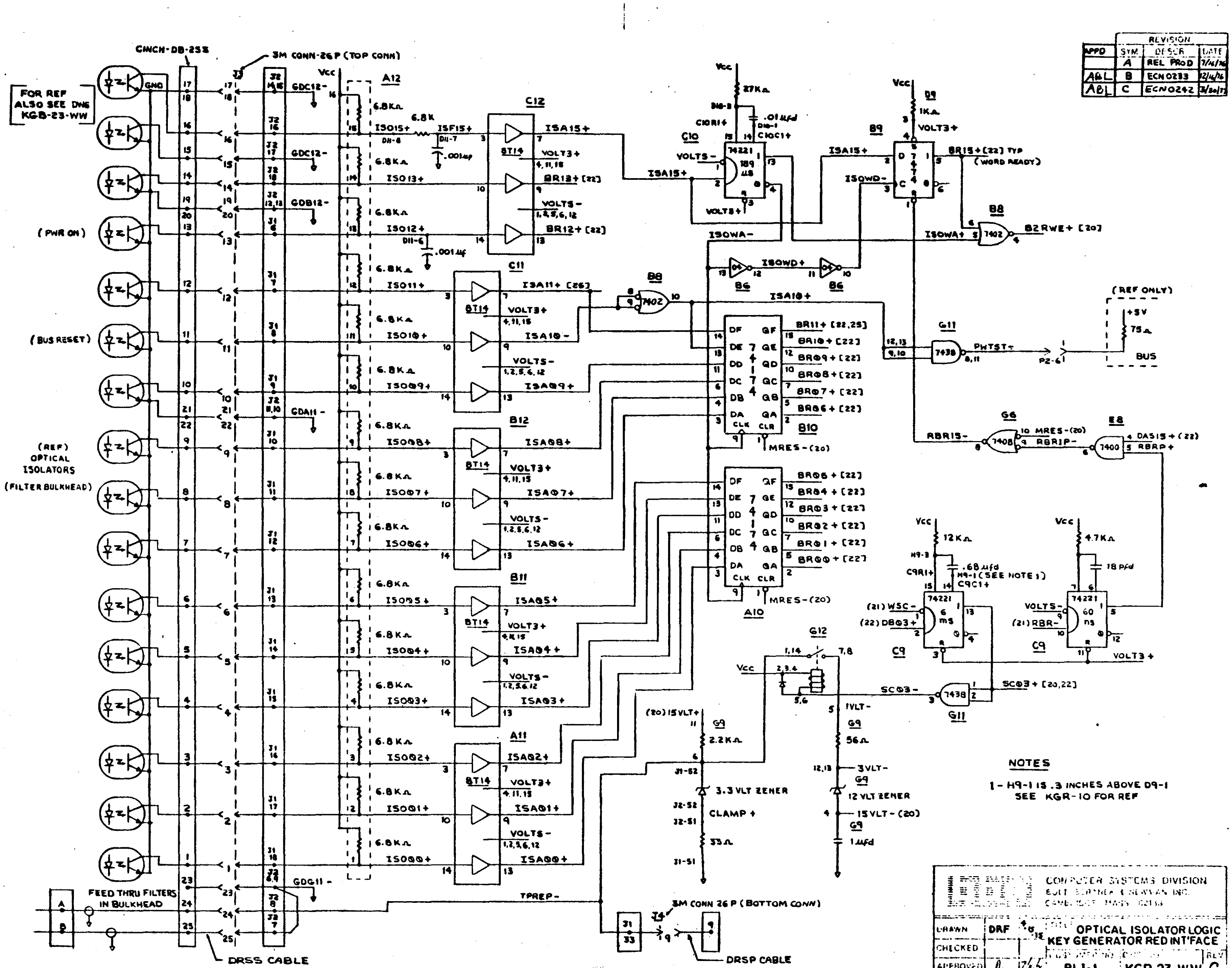
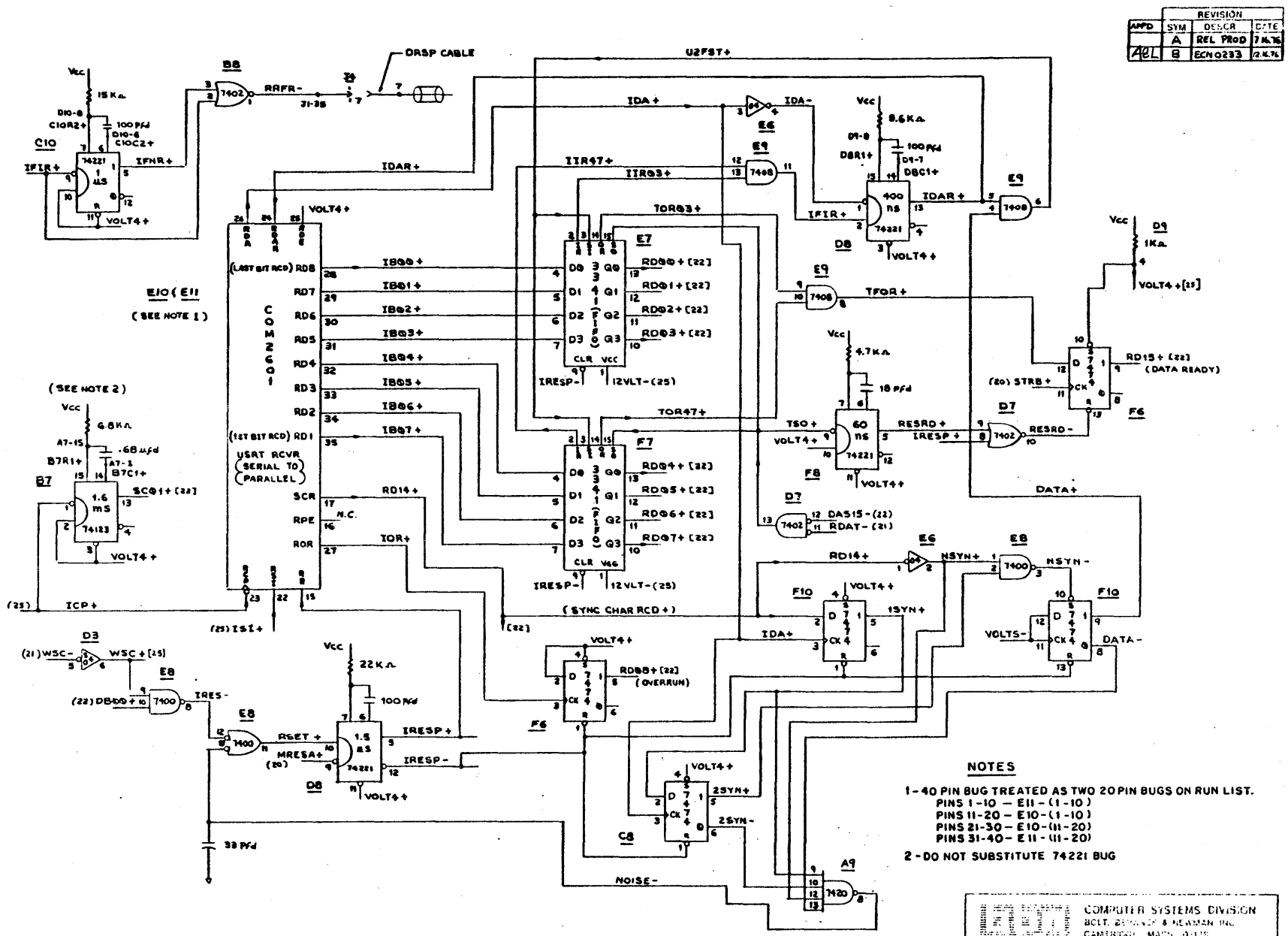
DRSP CABLE
U2FST+
IDA+
IDA-
IDAR+
IIR47+
IIR03+
TOR03+
TOR47+
TFOR+
IFIR+
IFNR+
RRFR-
VOLT4+
12VLT-(25)
IRESP-
IRESP+
RSET+
MRESA+
IRES-
RESRD+
RESRD-
TSO+
IBD0+
IBD1+
IBD2+
IBD3+
IBD4+
IBD5+
IBD6+
IBD7+
RD14+
IOR+
ICP+
ISI+
SCO1+ [22]
WSC+ [25]
WSC- (21)
DB00+ (22)
RDAT- (21)
DAS15- (22)
STRB+ (20)
RD15+ (22) (DATA READY)
DATA+
DATA-
NSYN+
NSYN-
1SYN+
2SYN+
2SYN-
VOLTS-
SYNC CHAR RCD+ (22)
RDD0+ [22] (OVERRUN)
NOISE-
RDD0+ [22]
RDD1+ [22]
RDD2+ [22]
RDD3+ [22]
RDD4+ [22]
RDD5+ [22]
RDD6+ [22]
RDD7+ [22]
(SEE NOTE 1)
(SEE NOTE 2)
C10
B8
B7
D3
D7
D8
D9
E6
E7
E8
E9
E10 (E11
F6
F7
F8
F10
C8
A9
15 KΩ
100 pfd
6.8 KΩ
.68 µfd
1.6 mS
22 KΩ
1.5 µS
33 pfd
9.6 KΩ
400 ns
1 KΩ
4.7 KΩ
18 pfd
60 ns
74221
7402
7408
7400
7420
74123
USRT RCVR (SERIAL TO PARALLEL)
COM2601
NOTES
1 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST.
PINS 1-10 — E11 - (1-10)
PINS 11-20 — E10 - (1-10)
PINS 21-30 — E10 - (11-20)
PINS 31-40 — E11 - (11-20)
2 - DO NOT SUBSTITUTE 74221 BUG
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF
CHECKED
APPROVED
SERIAL DATA RECEIVER
KEY GENERATOR RED INT'FACE
SIZE PLI-1
DWG NO KGR-24-WW B
REV B

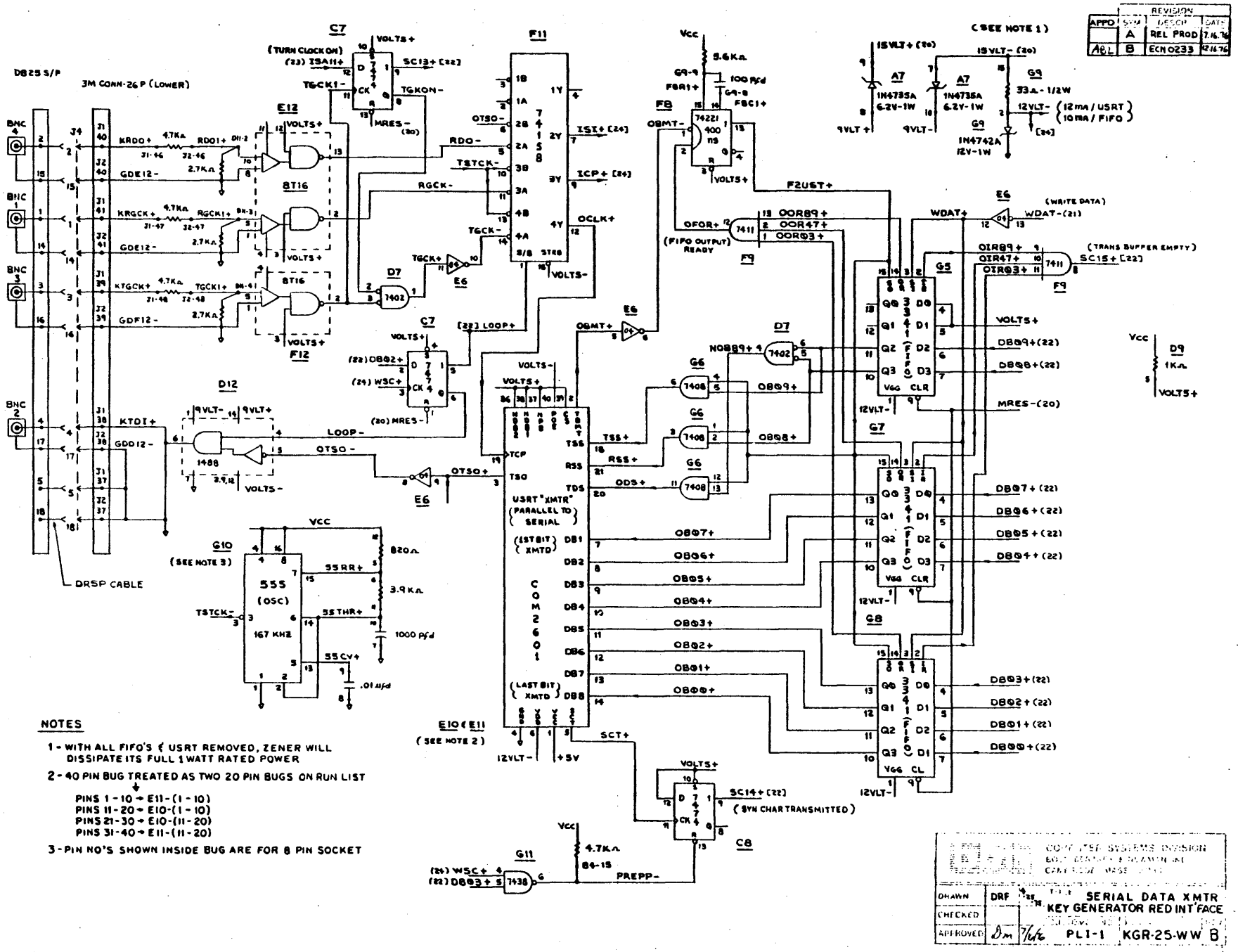

DB25 S/P
3M CONN-26 P (LOWER)
DRSP CABLE
NOTES
1 - WITH ALL FIFO'S & USRT REMOVED, ZENER WILL DISSIPATE ITS FULL 1 WATT RATED POWER
2 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST
PINS 1-10 → E11-(1-10)
PINS 11-20 → E10-(1-10)
PINS 21-30 → E10-(11-20)
PINS 31-40 → E11-(11-20)
3 - PIN NO'S SHOWN INSIDE BUG ARE FOR 8 PIN SOCKET
(SEE NOTE 1)
(SEE NOTE 2)
(SEE NOTE 3)
USRT "XMTR" (PARALLEL TO SERIAL)
COM2601
555 (OSC)
167 KHZ
(FIFO OUTPUT READY)
(TRANS BUFFER EMPTY)
(WRITE DATA)
(SYN CHAR TRANSMITTED)
REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7/16/76
B | ECN 0233 | 12/16/76
COMPUTER SYSTEMS DIVISION
SERIAL DATA XMTR KEY GENERATOR REDINTFACE
DRAWN DRF
CHECKED
APPROVED
PL1-1 KGR-25-WW B

KGR


REVISION
APPD | SYM | DESCR | DATE
| A | REL PROD | 7/16/76
A&L | B | ECN 0233 | 12/14/76
A&L | C | ECN 0242 | 3/30/77
CINCH-DB-25S
3M CONN-26P (TOP CONN)
FOR REF ALSO SEE DWG KGB-23-WW
(PWR ON)
(BUS RESET)
(REF) OPTICAL ISOLATORS (FILTER BULKHEAD)
FEED THRU FILTERS IN BULKHEAD
DRSS CABLE
3M CONN 26 P (BOTTOM CONN)
DRSP CABLE
TPREP-
(REF ONLY)
+5V
75Ω
BUS
PWTST-
P2-6
B2RWE+ [20]
BR15+ [22] TYP (WORD READY)
MRES-(20)
DAS15+ (22)
RBRP+
SC03+ [20,22]
3.3 VLT ZENER
CLAMP +
12 VLT ZENER
-15VLT-(20)
NOTES
1- H9-1 IS .3 INCHES ABOVE D9-1
SEE KGR-10 FOR REF
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN | DRF
CHECKED
APPROVED
OPTICAL ISOLATOR LOGIC
KEY GENERATOR RED INT'FACE
PL1-1
KGR-23-WW
REV C

KGR


REVISION
APPD | SYM | DESCR | DATE
AEL | A | REL PROD | 7 JUL 76
B | ECN 0233 | 12 JUL 76
DRSP CABLE
U2FST+
IDA+
IDA-
IDAR+
IIR47+
IIR03+
TOR03+
TOR47+
TFOR+
IFIR+
IFNR+
RRFR-
VOLT4+
IBD0+
IBD1+
IBD2+
IBD3+
IBD4+
IBD5+
IBD6+
IBD7+
RD14+
IOR+
ICP+
ISI+
RSET+
MRESA+
IRES-
IRESP+
IRESP-
NOISE-
RESRD+
RESRD-
TSO+
DATA+
DATA-
NSYN+
NSYN-
1SYN+
2SYN+
2SYN-
VOLTS-
RD15+ [22] (DATA READY)
RD08+ [22] (OVERRUN)
(SYNC CHAR RCD+)
(LAST BIT RCD) RD8
(1ST BIT RCD) RD1
USRT RCVR (SERIAL TO PARALLEL)
COM2601
SCR
RPE
ROR
N.C.
(SEE NOTE 1)
(SEE NOTE 2)
C10
B8
B7
D3
E6
E7
E8
E9
E10 (E11
D7
D8
D9
F6
F7
F8
F10
A9
C8
7402
7408
7400
74221
74123
74174
7420
15 KΩ
100 pfd
1.6 mS
1.5 µS
400 nS
60 ns
22 KΩ
8.6 KΩ
4.7 KΩ
1 KΩ
6.8 KΩ
.68 µfd
18 pfd
33 pfd
NOTES
1 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST.
PINS 1-10 — E11 - (1-10)
PINS 11-20 — E10 - (1-10)
PINS 21-30 — E10 - (11-20)
PINS 31-40 — E11 - (11-20)
2 - DO NOT SUBSTITUTE 74221 BUG
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 7/76
CHECKED
APPROVED 7/14/76
SERIAL DATA RECEIVER KEY GENERATOR RED INT'FACE
CUSTOMER PLI-1
CAGE NO KGR-24-WW
SIZE B



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7/16/76
ADL	B	ECN 0233	12/16/76

NOTES

1 - WITH ALL FIFO'S & USRT REMOVED, ZENER WILL DISSIPATE ITS FULL 1 WATT RATED POWER

2 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST

PINS 1-10 → E11-(1-10)
PINS 11-20 → E10-(1-10)
PINS 21-30 → E10-(11-20)
PINS 31-40 → E11-(11-20)

3 - PIN NO'S SHOWN INSIDE BUG ARE FOR 8 PIN SOCKET

COMPUTER SYSTEMS DIVISION
MAYNARD, MASSACHUSETTS

DRAWN	DRF	SERIAL DATA XMTR KEY GENERATOR RED INT FACE
CHECKED		
APPROVED	Dm 7/16	PL1-1 KGR-25-WW B

KGR

Low Speed Modem Interface Receive

MLR-Ø2 Logic Description

MLR-Ø5 Technical Reference

MLR-1Ø Assembly Drawing

MLR-15 Standard Modification

MLR-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8/27/73	

MLR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL 9/20/73

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

MLR LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		MLR-02

SCALE	REV	SHEET 1 OF 21

MLR LOGIC DESCRIPTION

The receive side of the modem is the MLR card, a block diagram of which is given in Figure 1. There are three drawings associated with MLR: MLR 20, 21, and 22. MLR 20 shows the input shift register, control character detection logic, and the input finite state machine. Drawing MLR21 shows the FIFOs and the DMA interface. Drawing MLR22 shows the data buffers, the bus driver/receivers, the input check register, the line interface drivers, receivers and associated logic, the crosspatch clock, and the status bit drivers. We begin with Drawing MLR20.

MLR20 In the lower left-hand corner is the input shift register, which assembles a character, and inverters for the control character detecters. The upper left-hand corner of the drawing shows the control character detecters, which are 7430 8-input nand gates, and are driven off the appropriate sets of uninverted and inverted bits. To the right of these is a 74163 bit counter, a modulo 8 counter implemented from a 4-bit counter with a synchronous parallel load of 8, producing an output which is true for 1-bit time out of each character time. The synchronous load is made to happen any time the count reaches 15, or any time the device is in SYN state, in which it is searching for character SYNC.

MLR

To the right of the bit counter is the finite state counter, decoder, and associated logic. A state diagram of this machine is given in Figure 2. The states are named according to the character which is being received. For instance, while in SYN state a SYN character is expected; the machine is actually searching for character SYNC. In DLE state, a SYN character has

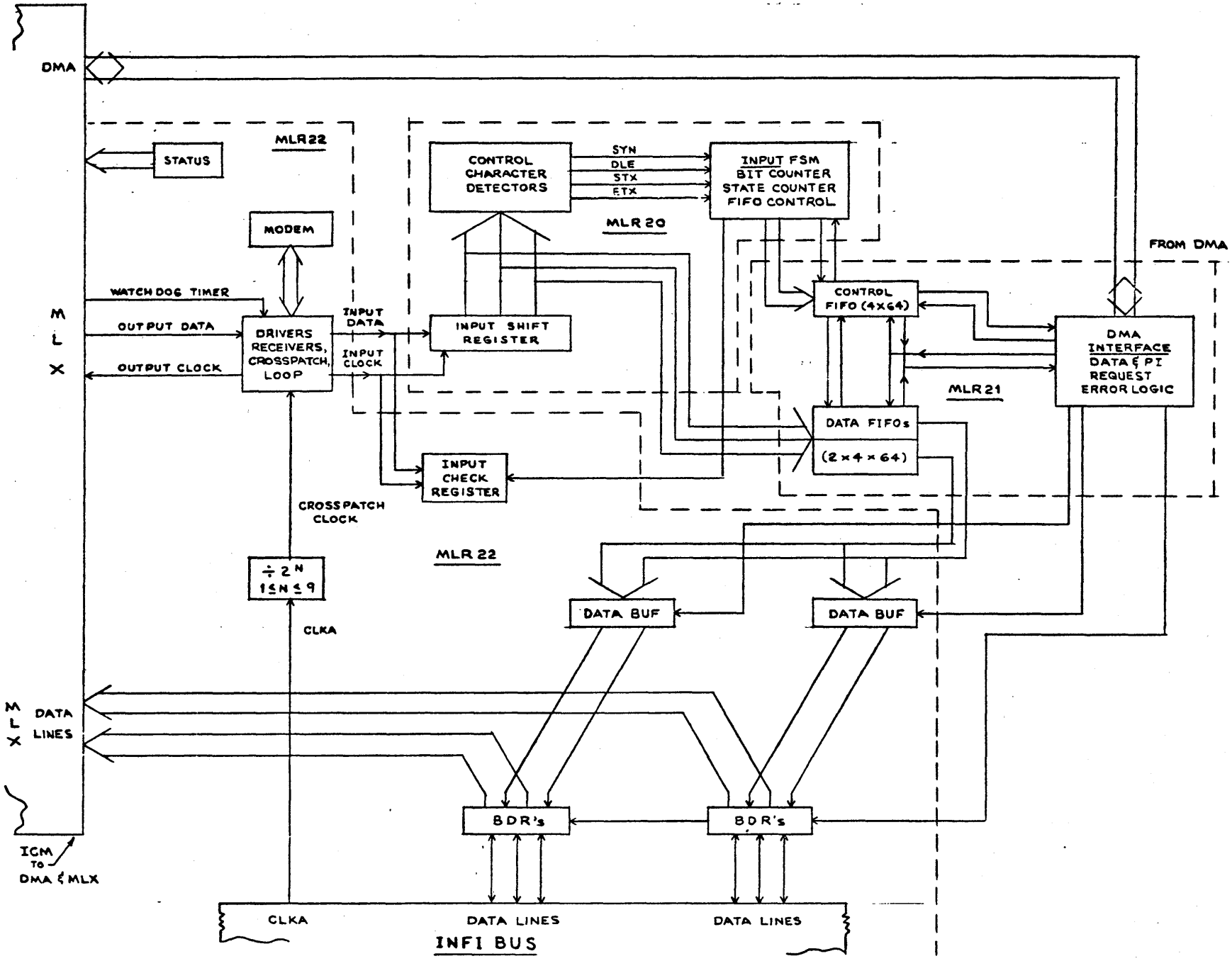


Figure 1 MLR BLOCK DIAGRAM

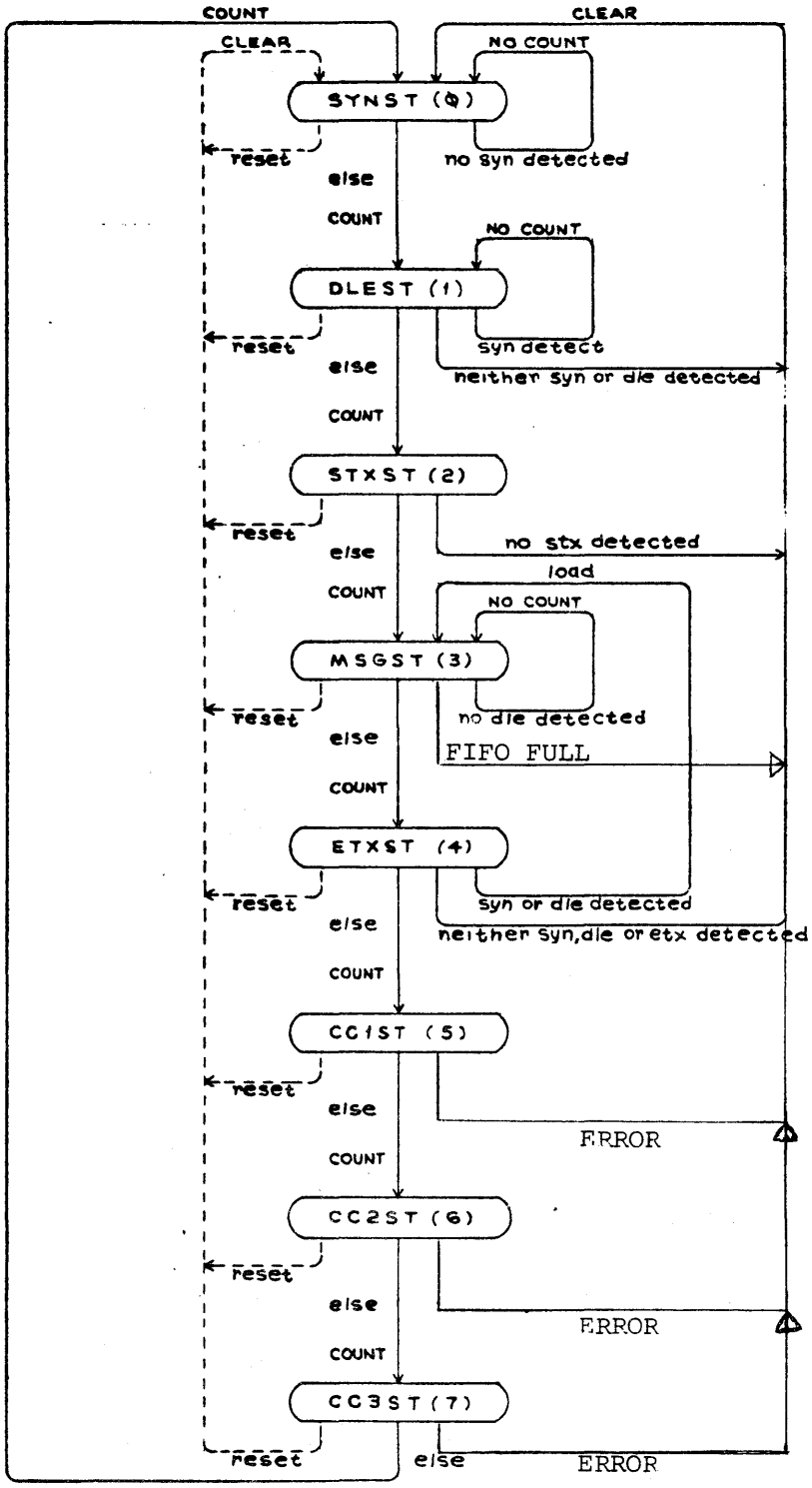


Figure 2 MLR FSM STATE DIAGRAM

MLR

been received, and a DLE is expected. The state counter itself is a 4-bit synchronous counter with a synchronous clear and a synchronous load. The inputs are hard-wired to be a 3, which means that a load puts the machine into message state. A clear causes the machine to go back into SYN state and search for character SYNC. Other state transitions are accomplished by incrementing the state counter, by bringing true IDXRF (index receive finite state machine) at the appropriate bit time. This is done either when in SYN state and a SYN character has been detected, or at NXTST (next state) time. This latter happens every eighth bit time (RBIT8), unless 1) we are in message state and no DLE has been detected, so that we want to remain in message state, or 2) we are in DLE state and a SYN has been detected, in which case we wish to remain in DLE state.

The state counter is loaded with a 3 to put us into message state at the eighth bit time of ETX state, if either a DLE or a SYN was detected, the DLE being a doubled DLE, the SYN being a protocol idle sequence. The state counter will be reset if at RBIT8 time any one of 4 error conditions is found to hold: 1) a receive reset command, at least 1 bit time earlier, 2) neither a DLE nor a SYN detected while in DLE state, 3) no STX detected while in STX state, or 4) neither of the three acceptable characters, DLE, ETX, or SYN, detected while in ETX state. All remaining state transitions are accomplished by incrementing the state counter.

The 7476 in the middle of the left-hand side of MLR20 is used to capture and synchronize the receive reset signal. Receive reset sets the first flip-flop (RRESS, receive reset synchronized). The next leading edge of the input clock (CLKIN) causes RFSMR (receive finite state machine reset) to come true.

The next leading edge of CLKIN will clear RRESS. RFSMR will remain true until the first leading edge of CLKIN while in SYN state, the state to which RFSMR will force the finite state machine.

The control FIFO carries two control bits from the finite state machine to the DMA interface. These are finite state machine error and end of message. End of message is derived in the middle of the lower half of MLR20. REOM is the OR of being in check character 3 state, or receiving an illegal character following a DLE in the text stream (signal DLCRP). The logic which makes up receive finite state machine error (RFSER), at the lower right-hand side of MLR20, is somewhat more complex. The error conditions include the FIFO not being ready to accept data when the finite state machine presented a byte, a bad checksum detected, or any of the conditions which caused the finite state machine to be reset (RRFSM). The error condition "receive FIFO full" (RFFUL) becomes set if, at the leading edge of a command to the FIFO to shift (RSI), the FIFO level "receive input ready" (RIR) was not high, indicating the FIFO was not yet ready to accept that data. The other condition for setting RFSER is if at clock time, either RRFSM (receive reset finite state machine) was true, or CKBAD (bad checksum) is true. This latter is true if during either check character 1 state, check character 2 state, or check character 3 state, the check register's feedback line (CKN1) is non-zero.

MLR

The remaining logic at the bottom of drawing MLR20, is the receive shift input logic (RSI). RSI is brought true indicating to the FIFO that there is a data byte to be taken, if, during the second half of an RBIT8 time (to allow for settling), either 1) we are in message state and no DLE character has been detected

(MSNDL), or 2) we have come to the end of message (REOM), in which case the data to be shifted is in control, or 3) we are in ETX state and a DLE is detected. This must be a doubled DLE, since the first DLE has been discarded, this DLE is presented as data to the FIFO.

MLR21 On the left-hand side of MLR21, the FIFOs are shown. The FIFO handshake logic (receive shift input, receive shift output, receive input ready, receive output ready) is identical to that for MLX. The pseudo-interrupt request logic in the upper right-hand portion of MLR21 is just like that in MLX except that now the signal REONN is ORed into the logic to clear the active flip-flop, if the control FIFO is indicating end of message at receive now time (RNOW).

The receive byte 2 flip-flop (RBYT2) is used to select which half-word of the data buffer will be loaded with the byte now being presented by the data FIFOs. This flip-flop is cleared by RACTV being false, so that the first data byte of each buffer will go into the right half-word, and is toggled each time a data byte is taken from the FIFO (each RSO, if not a control byte REOMF). The signals RLLBB (receive load left byte buffer) and RLRBB (receive load right byte buffer) cause the appropriate half-word to be loaded at the leading edge of RSO (receive shift out-out). As the left byte buffer is loaded, ROKSF is set, bringing down RSO, and inhibiting further RSOs. When the FIFO again has data to be presented, receive output ready ROR comes true. Since ROKSF is true at this time, the receive ready flop gets set and if RACTV is true, RREDY, the receive request line to the DMA, is brought true. On the leading edge of RNOW, indicating that the DMA is taking the data, the receive ready flop is cleared. On the trailing edge of RNOW, ROKSF is cleared, enabling RSO to the FIFOs. The setting of RREDF is delayed until the FIFO is again ready with data because if this is last data

word of the buffer, and an interrupt is generated, the program needs to be able to read the "end of message" and "error" lines from the FIFO, which will be guaranteed to be valid, since ROR is true.

MLR22 On the right side of MLR22 are the receive data latches and the bus driver/receivers, which interface to the INFIBUS itself. The receive data lines from the bus driver/receivers are driven across to the ICM and over to MLX. This is the path whereby MLX gets its data from memory. The BDR drivers are enabled by RNOW. Both half words of the data buffer are loaded from the FIFO data RFDB0 through RFDB7. The loading of the buffers is accomplished with the RLLBB and RLRBB signals.

The lower central portion of MLR22 shows the receive check register. This is similar to the transmit check register, but does not include the switching, since all data, text, control, and check characters are passed through the check register in the same fashion. The check register simulator results given in Appendix 1 apply equally well to this, as to the transmit check registers.

MLR

The logic at the top central part of MLR22 is the cross-patch clock. CLKA, the 25 megacycle infibus clock, is received through a 7404, and driven into a 7474 toggle, to the output of which drives two 74163 synchronous 4-bit counters, providing a factor of 512 speed reduction, to produce a roughly 50-KB clock. If a faster clock is desired, MICLK (modem internal clock) can be shifted to one of the other bits in the counter chain.

The lower left-hand portion of the MLR22 shows the logic which drives the status bits to the DMA, as described in the DMA functional spec and in the modem functional spec.

The logic at the upper left hand portion of MLR22 is the line interface drivers and receivers. At the extreme upper left-hand corner is the external crosspatch flip-flop (EXPCH), which, when true, drives the modem loop line (MLPLD) to the 303, causing the 303 to loop internally. The driving of this line is conditioned with WDTOK (watchdog timer OK) from MLX, to prevent driving this line if this particular interface is not in use. The data line to the 303 (MXDLD) is driven from the MLX output data line OUDAT, if the watchdog timer is OK, and the interface is not internally crosspatched (IXCPH-). These are the only two lines driven to the 303. IXPCH is a flip flop loaded by writing bit 14 to the receive status word.

The receive data line from the 303 is ANDed with the interface not being internally crosspatched (IXPCH-), and ORed with the output data ANDed with the interface being internally crosspatched. This selected data is then applied to the input of a 7474 to make BINDT the buffered input data signal, which, 1-bit time later, to allow for settling, is shifted into the input shift register and to the input check register. The two modem clocks, MRCLR, the receive clock, and MXCLR, the transmit clock, are similarly received, ANDed with "not internally crosspatched" and then ORed with the internal modem clock (MICLK) ANDed with "internally crosspatched", to provide CLKIN and CLKO, the logic level signals derived from these clocks. All three of these input lines from the 303 are terminated in 100 ohm resistors. These resistors can be optionally removed to provide a high impedance input if interfaces are to be paralleled and the termination resistors to be installed externally.

DATA 020 002 000 000 000 000 020 203

020

0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
1	1	00000000	00000000	00000000
0	0	10000000	00000000	00000000
0	1	01000000	00000000	00000000
0	0	10100000	00000000	00000000

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

000

0	1	10001111	01010000	00000000
0	0	11000111	10101000	00000000
0	0	01100011	11010100	00000000
0	1	00110001	11101010	00000000
0	1	10011000	11110101	00000000
0	0	11001100	01111010	10000000
0	1	01100110	00111101	01000000
0	0	10110011	00011110	10100000

000

0	0	01011001	10001111	01010000
0	1	00101100	11000111	10101000
0	0	10010110	01100011	11010100
0	0	01001011	00110001	11101010
0	0	00100101	10011000	11110101

MLR

0	0	00010010	1100$\bar{1}$100	0$\bar{1}$111010
0	0	00010001	01$\bar{1}$00110	00111101
0	1	00000100	10$\bar{1}$10011	00011110

000

0	0	10000010	0101$\bar{1}$001	10001111
0	1	01000001	00$\bar{1}$01$\bar{1}$00	11000111
0	1	10100000	10010110	01100011
0	1	11010000	01001011	00110001
0	0	11101000	00$\bar{1}$00101	10011000
0	0	01110100	00010010	11001100
0	1	00111010	00001$\bar{1}$01	01100110
0	1	10011101	00000100	10110011

000

0	0	11001110	10000010	01011001
0	0	01100111	01000001	00101100
0	1	00110011	10$\bar{1}$00000	10010110
0	0	10011001	$\bar{1}$1010000	01001011
0	0	01001100	11$\bar{1}$01000	00100101
0	0	00100110	01$\bar{1}$10100	00010010
0	0	00010011	00$\bar{1}$11010	00001001
0	1	00001001	10011101	00000100

023

0	0	10000100	1100$\bar{1}$110	10000010
0	0	01000010	01$\bar{1}$00111	01000001
0	1	00100001	00$\bar{1}$10011	10100000
0	0	10010000	10011$\bar{0}$01	11010000
1	1	01001000	01001$\bar{1}$00	11101000
0	0	10100100	00$\bar{1}$00110	0$\bar{1}$110100
0	0	01010010	00010011	00$\bar{1}$11010
0	0	00101001	00001$\bar{0}$01	10011101

203

1	0	00010100	10000100	11001110
1	1	00001010	01000010	01100111
0	0	10000101	00$\bar{1}$00001	00110011
0	1	01000010	10010000	10011001
0	1	10100001	01001000	01001100
0	0	11010000	10$\bar{1}$00100	00100110

0	0	01101000	01010010	00010011
1	1	00110100	00101001	00001001

0	0	10011010	00010100	10000100
0	0	01001101	00001010	01000010
0	0	00100110	10000101	00100001
0	1	00010011	01000010	10010000
0	0	00001001	10100001	01001000
0	1	00000100	11010000	10100100
0	1	00000010	01101000	01010010
0	1	00000001	00110100	00101001

0	0	00000000	10011010	00010100
0	1	00000000	01001101	00001010
0	1	00000000	00100110	10000101
0	1	00000000	00010011	01000010
0	0	00000000	00001001	10100001
0	1	00000000	00000100	11010000
0	0	00000000	00000010	01101000
0	1	00000000	00000001	00110100

MLR

0	1	00000000	00000000	10011010
0	1	00000000	00000000	01001101
0	1	00000000	00000000	00100110
0	0	00000000	00000000	00010011
0	0	00000000	00000000	00001001
0	1	00000000	00000000	00000100
0	0	00000000	00000000	00000010
0	1	00000000	00000000	00000001

DATA 020 002 223 371 375 000 020 203

020

0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
1	1	00000000	00000000	00000000
0	0	10000000	00000000	00000000
0	1	01000000	00000000	00000000
0	0	10100000	00000000	00000000

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

223

1	0	10001111	01010000	00000000
1	1	01000111	10101000	00000000
0	1	10100011	11010100	00000000
0	0	11010001	11101010	00000000
1	1	01101000	11110101	00000000
0	1	10110100	01111010	10000000
0	1	11011010	00111101	01000000
1	0	11101101	00011110	10100000

371

1	0	01110110	10001111	01010000
0	1	00111011	01000111	10101000
0	1	10011101	10100011	11010100
1	0	11001110	11010001	11101010
1	1	01100111	01101000	11110101
1	1	10110011	10110100	01111010
1	0	11011001	11011010	00111101
1	0	01101100	11101101	00011110

375

1	1	00110110	01$\bar{1}$10110	10001111
0	1	10011011	00$\bar{1}$11011	01000111
1	0	11031101	10011$\bar{1}$01	10100011
1	0	01100110	$\bar{1}$100$\bar{1}$110	11010001
1	1	00110011	01$\bar{1}$00111	01101000
1	1	10011001	10$\bar{1}$10011	10110100
1	0	11001100	$\bar{1}$101$\bar{1}$001	11011010
1	1	01100110	01$\bar{1}$01$\bar{1}$00	11101101

000

0	0	10110011	00$\bar{1}$10110	01110110
0	0	01011001	10011011	00111011
0	0	00101100	11001$\bar{1}$01	10001101
0	0	00010110	01$\bar{1}$00110	1$\bar{1}$001110
0	0	00001011	00$\bar{1}$10011	01100111
0	0	00000101	10011001	10110011
0	0	00000010	$\bar{1}$1001$\bar{1}$00	11011001
0	0	00000001	01100110	01101100

020

0	0	00000000	10$\bar{1}$10011	00110110
0	0	00000000	01011001	10011011
0	0	00000000	00$\bar{1}$01$\bar{1}$00	11001101
0	0	00000000	00010110	01100110
1	0	00000000	00001011	00110011
0	0	00000000	00000101	10011001
0	0	00000000	00000010	11001100
0	0	00000000	00000001	01100110

203

1	0	00000000	00000000	10110011
1	0	00000000	00000000	01011001
0	0	00000000	00000000	00101100
0	0	00000000	00000000	00010110
0	0	00000000	00000000	00001011
0	0	00000000	00000000	00000101
0	0	00000000	00000000	00000010
1	0	00000000	00000000	00000001

0	0	00000000	00000000	00000000

MLR

```
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
```

```
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
```

```
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
```

```
DATA   020  002  221  024  342  000  020  203

  020

0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
0  0      00000000   00000000   00000000
```

1	1	00000000	00000000	00000000
0	0	10000000	00000000	00000000
0	1	01000000	00000000	00000000
0	0	10100000	00000000	00000000

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	10111101	01000000	00000000
0	1	00011110	10100000	00000000

221

1	0	10001111	01010000	00000000
0	0	01000111	10101000	00000000
0	1	00100011	11010100	00000000
0	1	10010001	11101010	00000000
1	1	11001000	11110101	00000000
0	0	11100100	01111010	10000000
0	1	01110010	00111101	01000000
1	1	10111001	00011110	10100000

024

0	1	11011100	10001111	01010000
0	1	11101110	01000111	10101000
1	0	11110111	00100011	11010100
0	1	01111011	10010001	11101010
1	1	10111101	11001000	11110101
0	0	11011110	11100100	01111010
0	1	01101111	01110010	00111101
0	0	10110111	10111001	00011110

342

0	1	01011011	11011100	10001111
1	1	10101101	11101110	01000111
0	0	11010110	11110111	00100011
0	0	01101011	01111011	10010001
0	0	00110101	10111101	11001000

MLR

1	1	00011010	1101$\bar{1}$110	11100100
1	0	10001101	01$\bar{1}$01111	01110010
1	1	01000110	10$\bar{1}$10111	10111001

000

0	0	10100011	0101$\bar{1}$011	11011100
0	1	01010001	$\bar{1}$01$\bar{1}$1101	11101110
0	1	10101003	11010110	11110111
0	0	11010103	01$\bar{1}$01011	01111011
0	1	01101010	00$\bar{1}$10101	10111101
0	0	10110101	00011010	11011110
0	0	01011013	10001101	01101111
0	0	00101101	01000110	10110111

020

0	0	00010110	10$\bar{1}$00011	01011011
0	0	00001011	01010001	10101101
0	0	00000101	$\bar{1}$01$\bar{1}$0000	11010110
0	0	00000010	11010103	01101011
1	0	00000001	01$\bar{1}$01010	00110101
0	0	00000000	10110101	00011010
0	0	00000000	01011010	10001101
0	0	00000000	00101$\bar{1}$01	01000110

203

1	0	00000000	00010110	10100011
1	0	00000000	00001011	01010001
0	0	00000000	00000101	10101000
0	0	00000000	00000010	11010100
0	0	00000000	00000001	01101010
0	0	00000000	00000000	10110101
0	0	00000000	00000000	01011010
1	0	00000000	00000000	00101101

0	0	00000000	00000000	00010110
0	0	00000000	00000000	00001011
0	0	00000000	00000000	00000101
0	0	00000000	00000000	10000010
0	1	00000000	00000000	00100001
0	0	00000000	00000000	10000000

```
0  0     00200000   00000000   00000000
0  0     00000000   00000000   00000000


0  0     00000000   00000000   00000000
0  0     00200000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000


0  0     00000000   00000000   00000000
0  0     00200000   00000002   00000000
0  0     00200000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00200000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
```

MLR

```
DATA   020  002  363  346  154  000  020  203


  020

0  0     00200000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
0  0     00000000   00000000   00000000
1  1     00000000   00000000   00000000
0  0     10000000   00000000   00000000
0  1     00000000   00000000   00000000
0  0     10100000   00000000   00000000
```

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

363

1	0	10001111	01010000	00000000
1	1	01000111	10101000	00000000
0	1	10100011	11010100	00000000
0	0	11010001	11101010	00000000
1	1	01101000	11110101	00000000
1	0	10110100	01111010	10000000
1	0	01011010	00111101	01000000
1	1	00101101	00011110	10100000

346

0	0	10010110	10001111	01010000
1	1	01001011	01000111	10101000
1	0	10100101	10100011	11010100
0	1	01010010	11010001	11101010
0	1	10101001	01101000	11110101
1	1	11010100	10110100	01111010
1	0	11101010	01011010	00111101
1	1	01110101	00101101	00011110

154

0	0	10111010	10010110	10001111
0	0	01011101	01001011	01000111
1	0	00101110	10100101	10100011
1	0	00010111	01010010	11010001
0	1	00001011	10101001	01101000
1	1	10000101	11010100	10110100
1	0	11000010	11101010	01011010
0	1	01100001	01110101	00101101

000

0	1	10110000	1011̄1̄010	10010110
0	0	11011000	0101̄1̄101	01001011
0	1	01101100	0010̄1̄110	10100101
0	1	10110110	0001̄0̄111	01010010
0	0	11011011	0000̄1̄011	10101001
0	0	01101101	1000̄0̄101	11010100
0	1	00110110	1100̄0̄010	11101010
0	0	10011011	0̄1̄100001	01110101

020

0	1	01001101	10̄1̄10000	10111010
0	0	10100110	1̄1̄01̄1̄000	01011101
0	1	01010011	0̄1̄1̄01̄100	00101110
0	0	10101001	1̄0̄1̄10̄110	00010111
1	0	01010100	1̄1̄01̄1̄011	00001011
0	1	00101010	0̄1̄1̄01̄101	10000101
0	1	10010101	0̄0̄1̄1̄0̄110	11000010
0	1	11001010	1̄0̄0̄1̄1̄011	01100001

203

1	1	11100101	0̄1̄0̄0̄1̄101	10110000
1	0	11110010	1̄0̄1̄0̄0̄110	11011000
0	0	01111001	0̄1̄0̄1̄0̄011	01101100
0	0	00111100	1̄0̄1̄0̄1̄001	10110110
0	1	00011110	0̄1̄0̄1̄0̄100	11011011
0	0	10001111	0̄0̄1̄0̄1̄0̄1̄0	01101101
0	0	01000111	1̄0̄0̄1̄0̄101	00110110
1	0	00100011	1̄1̄0̄0̄1̄0̄1̄0	10011011

0	0	00010001	1̄1̄1̄00̄101	01001101
0	0	00001000	1̄1̄1̄1̄0̄0̄1̄0	10100110
0	0	00010100	0̄1̄1̄1̄1̄001	01010011
0	0	00000010	0̄0̄1̄1̄1̄1̄00	10101001
0	1	00000001	0000̄1̄1̄10	01010100
0	0	00000000	1000̄1̄111	00101010
0	0	00000000	0̄1̄0̄0̄0̄111	10010101
0	0	00000000	0̄0̄1̄0̄0̄0̄1̄1	11001010

0	1	00000000	00010001	11100101

MLR

0	1	00000000	00001000	11110010
0	0	00000000	00000100	01111001
0	0	00000000	00000010	00111100
0	0	00000000	00000001	00011110
0	0	00000000	00000000	10001111
0	0	00000000	00000000	01000111
0	1	00000000	00000000	00100011

0	0	00000000	00000000	00010001
0	1	00000000	00000000	00001000
0	1	00000000	00000000	00000100
0	0	00000000	00000000	00000010
0	1	00000000	00000000	00000001
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/7/73	
B	ECN 216	7/16/76	

MLR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

MLR TECHNICAL REF

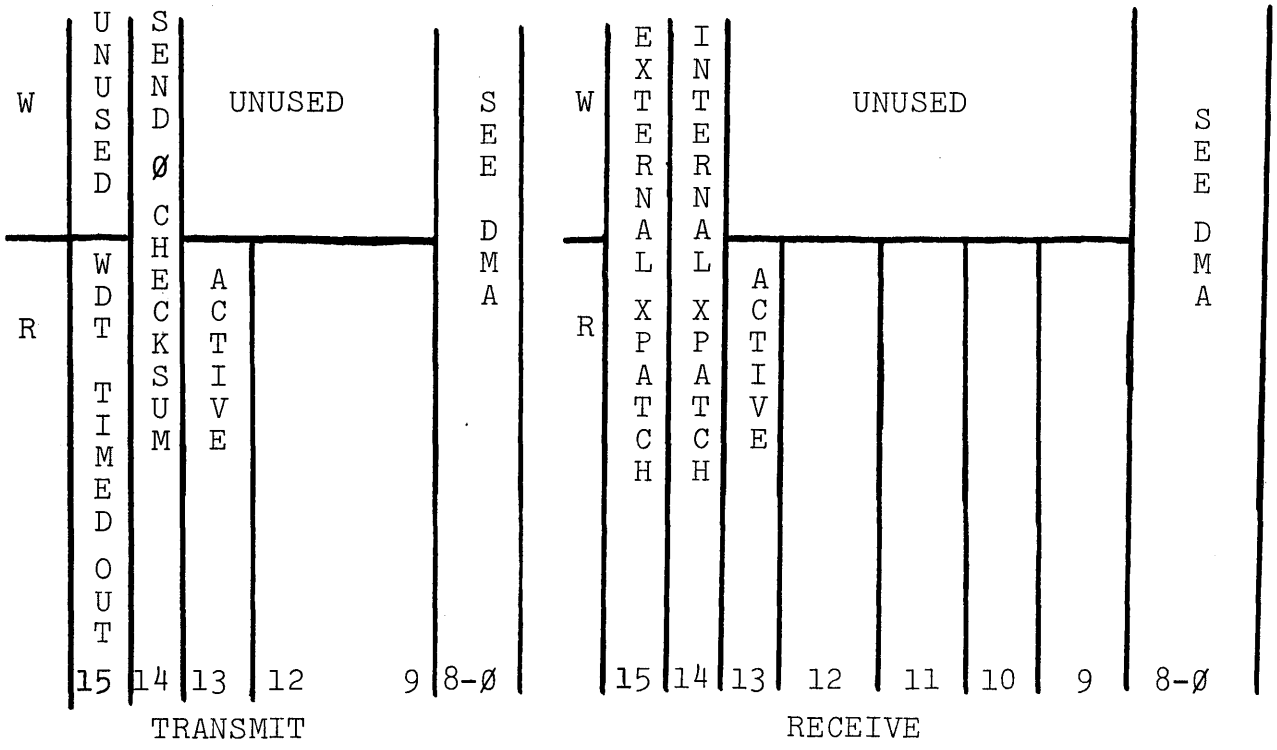
SIZE	CODE IDENT NO.	DRAWING NO.
A		MLR-05

SCALE	REV	SHEET
	B	1 OF 3

MLR - Low Speed Modem Receiver BBN

see DMA, MLX

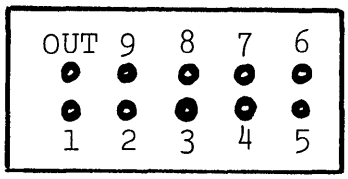
Status - address FXXX6(receive), FXXXC(transmit)



MLR

Switches - none, see MLX

Jumpers - Crosspatch clock speed PC only



Connect OUT to one of these pins for desired speed.

PIN	SPEED
1	12.5 MHz
2	6.25 MHz
3	3.125 MHz
4	1.563 MHz
5	781 KHz
6	391 KHz
7	195 KHz
8	98 KHz
9	44 KHz

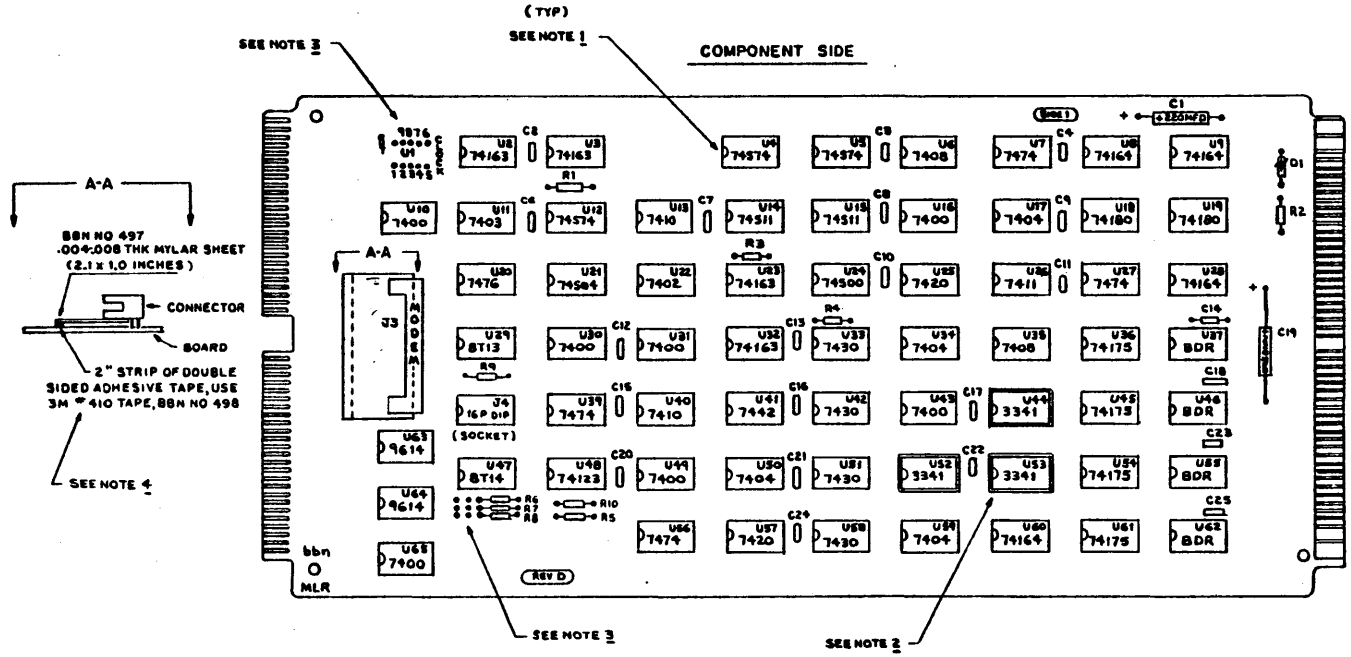
Line Terminator Resisters
Jumper when this MLR is at the end of the device cable.
Located to left of R6, R7, R8 at lower left of board (PLC).

Socket

3	Transmit Data
4	Crosspatch
5	Transmit Clock
6	Receive Data
7	Receive Clock

MLR-1Ø ASSEMBLY DRAWING

APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	8-27-73
	B	ECN #0055	6.18.74
	C	ECN #0075	9.11.74
	D	ECN 0080	9.25.74
	E	ECN 0091	10.28.74
	F	ECN 0122	1.10.75
	G	ECN 0134	3.5.75
	H	ECN 0179	8.11.75
	I	ECN 0289	4.20.78



COMPONENT VALUES

C2-C4, C6-C18, C20-C25 = .1 mfd CERAMIC DISC
C1-C19 = 220 mfd-10 VOLT ELECTROLYTIC
R1, R3, R4, R9 = 1K Ω - 1/4 W-10 %
R2, R6, R7, R8 = 100 Ω
R5 = 33K
R10 = 15K
D1 = ZENER DIODE, 1N5242
J3 = 26 PIN CONN, 3429-1002
J4 = 16 PIN DIP SOCKET

NOTES

1 – NOTCH SHOWN IN BUG INDICATES INSERTION DIRECTION.
2 – U35, U43, U44, BUGS (3341) ARE MOUNTED IN SOCKETS.
3 – WIRE-WRAP JUMPER PINS (16 PLACES).
4 – WITH TAPE ATTACHED TO MYLAR AS SHOWN, SLIDE MYLAR UNDER CONN UNTIL IT TOUCHES PINS (CONN), THEN PRESS TAPE EDGE AGAINST BOARD.

DRAWN	DRF	8-27-73	MLR PC LAYOUT
CHECKED	DK	9/16/74	
APPROVED		9/16/74	HSMIMP MLR-10-PC I

MLR

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	
B	ECN 281	4/12/78	EC

MLR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

MLR MODIFICATION STND

SIZE	CODE IDENT NO.	DRAWING NO.
A		MLR-15

SCALE	REV	SHEET
	B	1 OF 4

MLR-15-PC (STANDARD MOD)

1) Refer to Fig. 1 (component side, view of MLR) to identify the P.C. area effected.

2) Refer to Fig. 2 (Solder side, view of MLR) to identify the P.C. area effected (all soldering to be done on this side).

3) The ground pins for the BDRs are pins 7 and 8. These are connected to the P.C. lands adjacent to the Board's System Logic Ground. The BDRs grounds should be connected by bridging the gap which separates the two lands (as shown in Fig. 2).

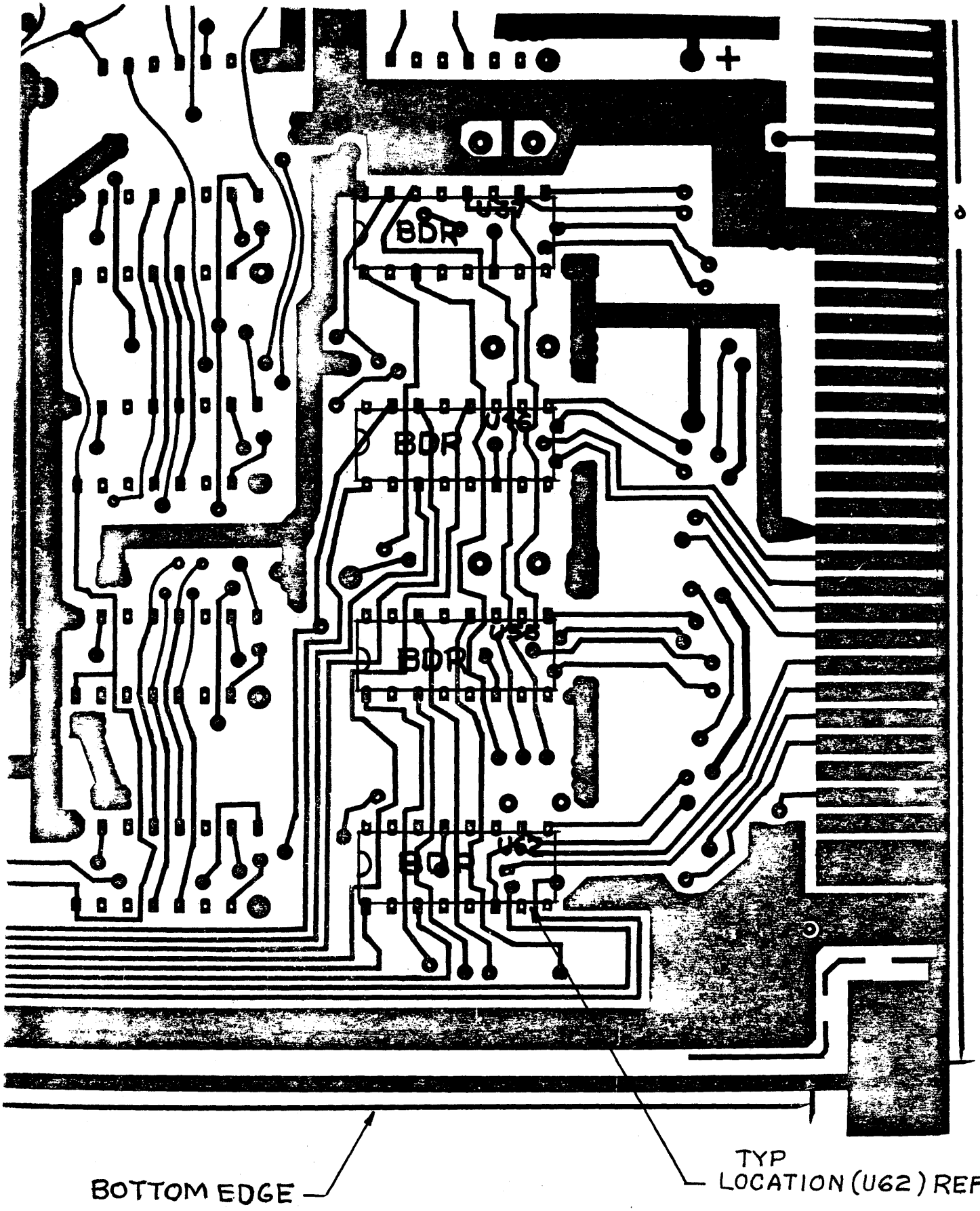


FIG 1
(COMPONENT SIDE)

MLR-15-PC
SHT 3 of 4

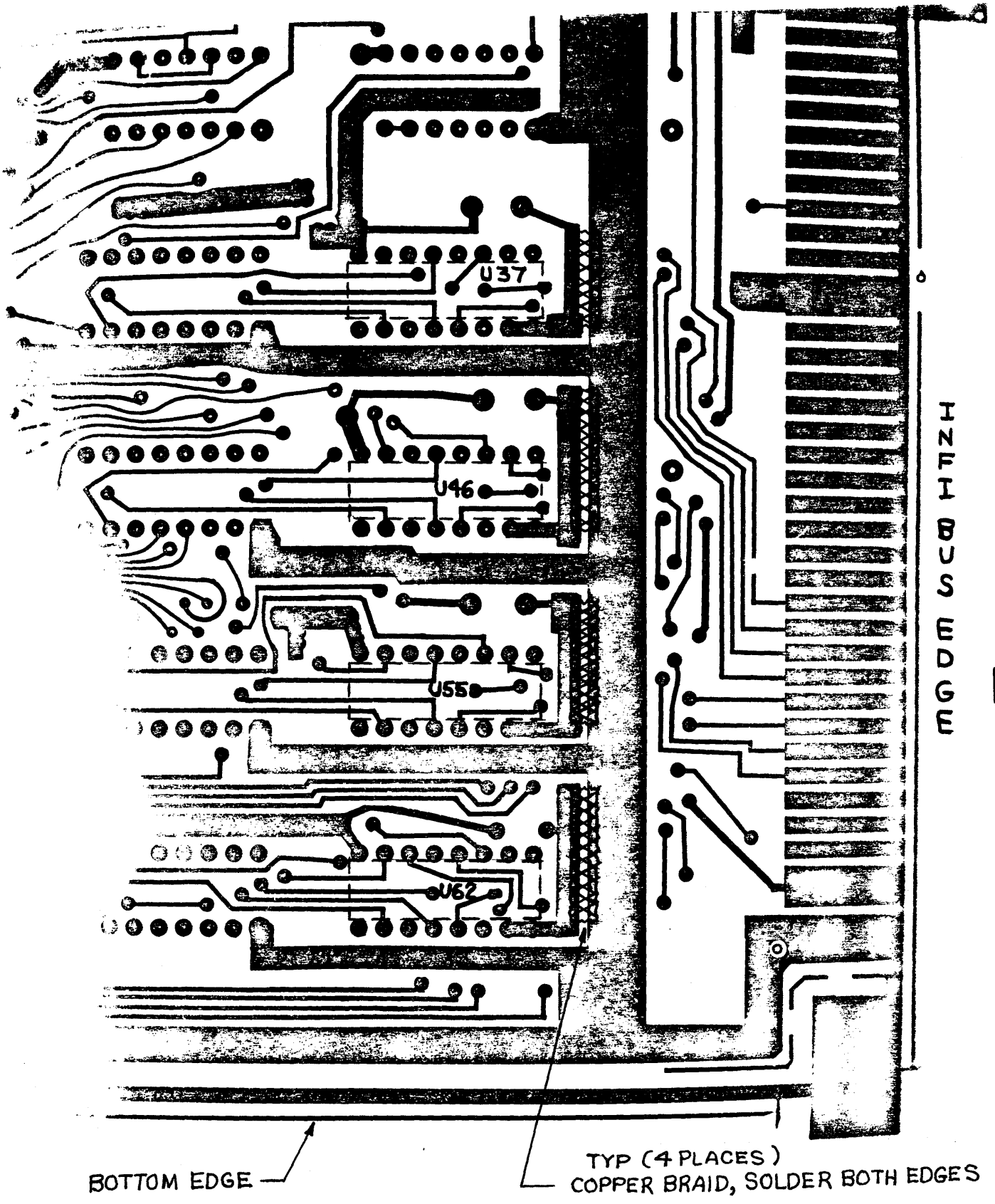
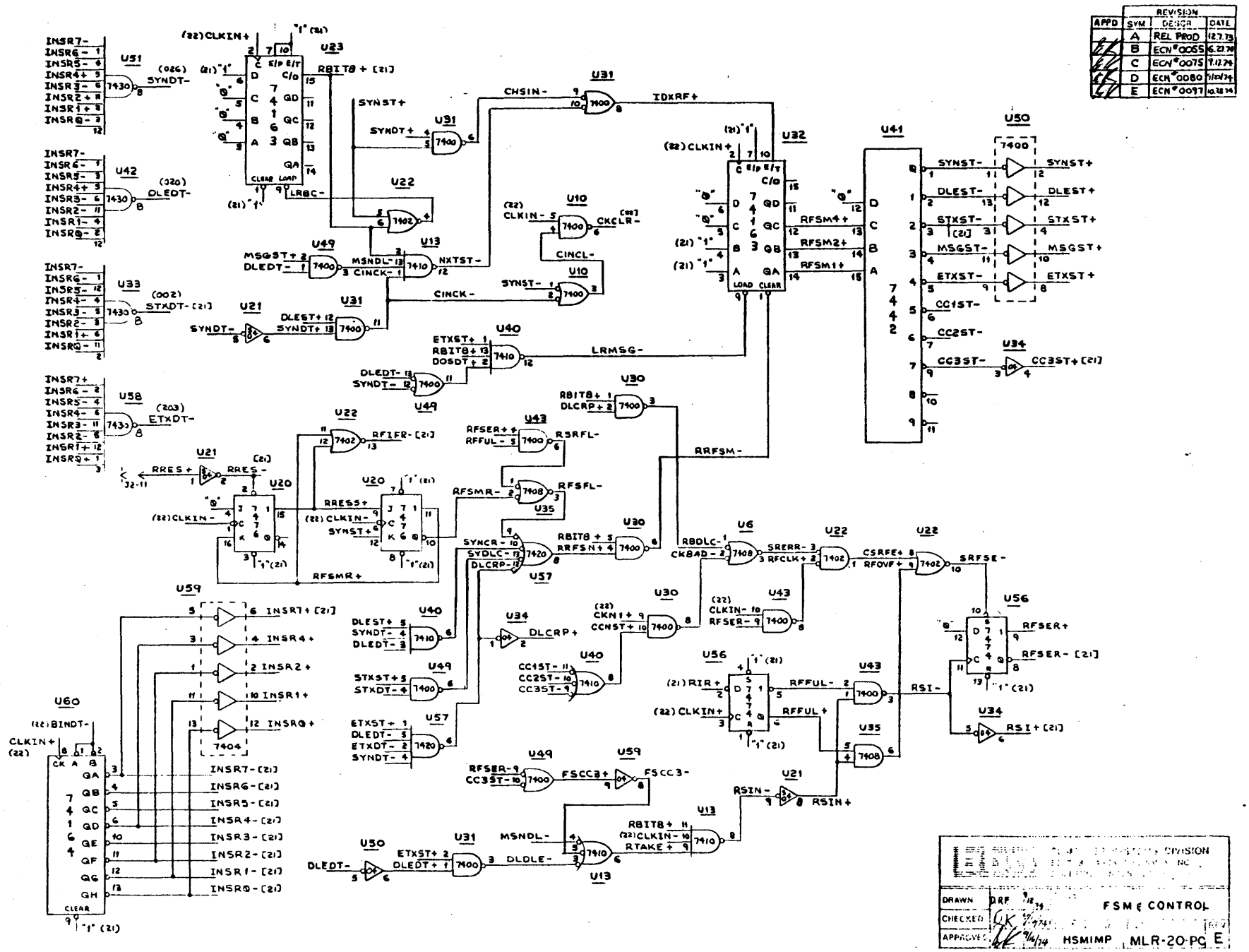
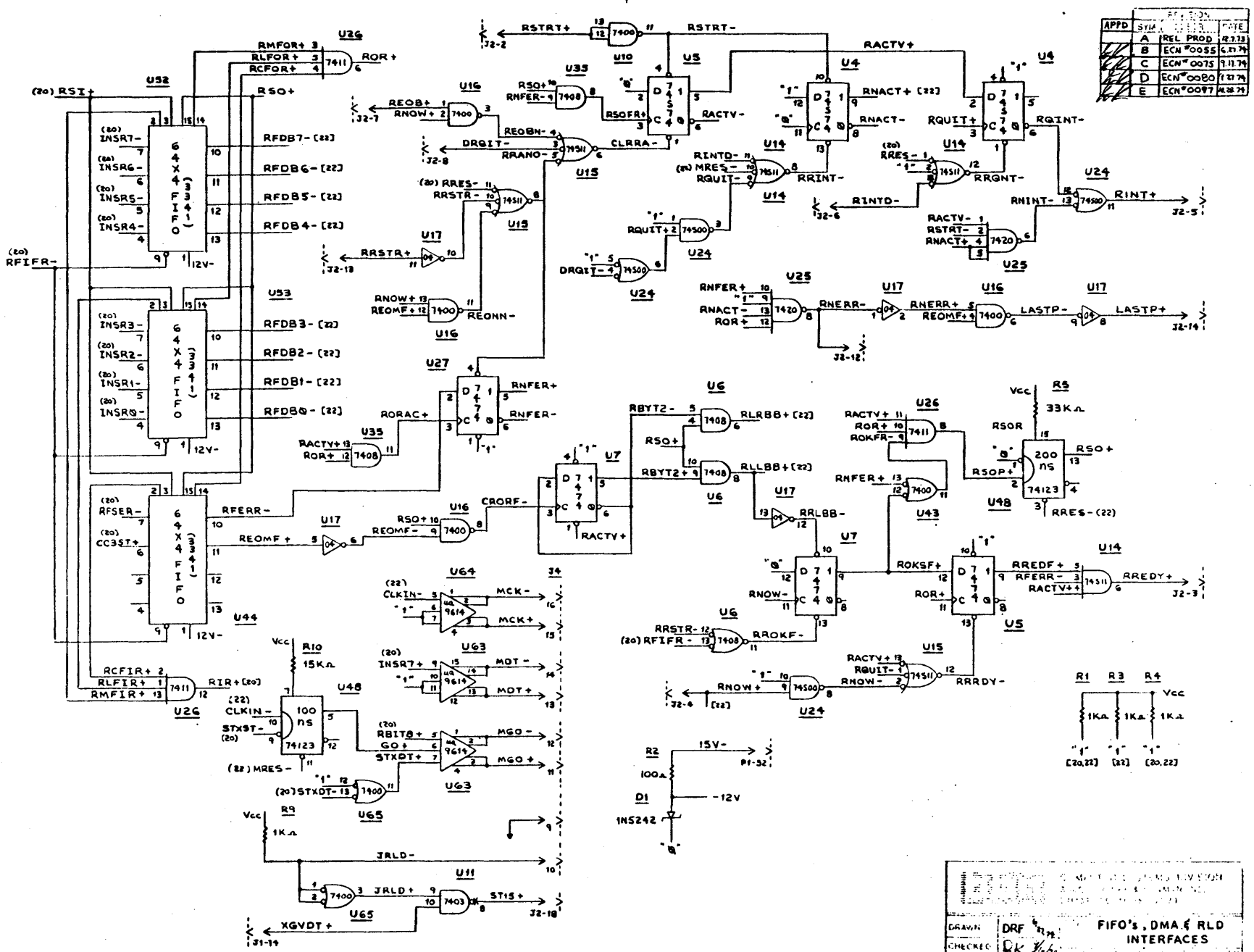


FIG 2
(SOLDER SIDE)

MLR-15-PC
SHT 4 of 4

MLR-2Ø SCHEMATICS

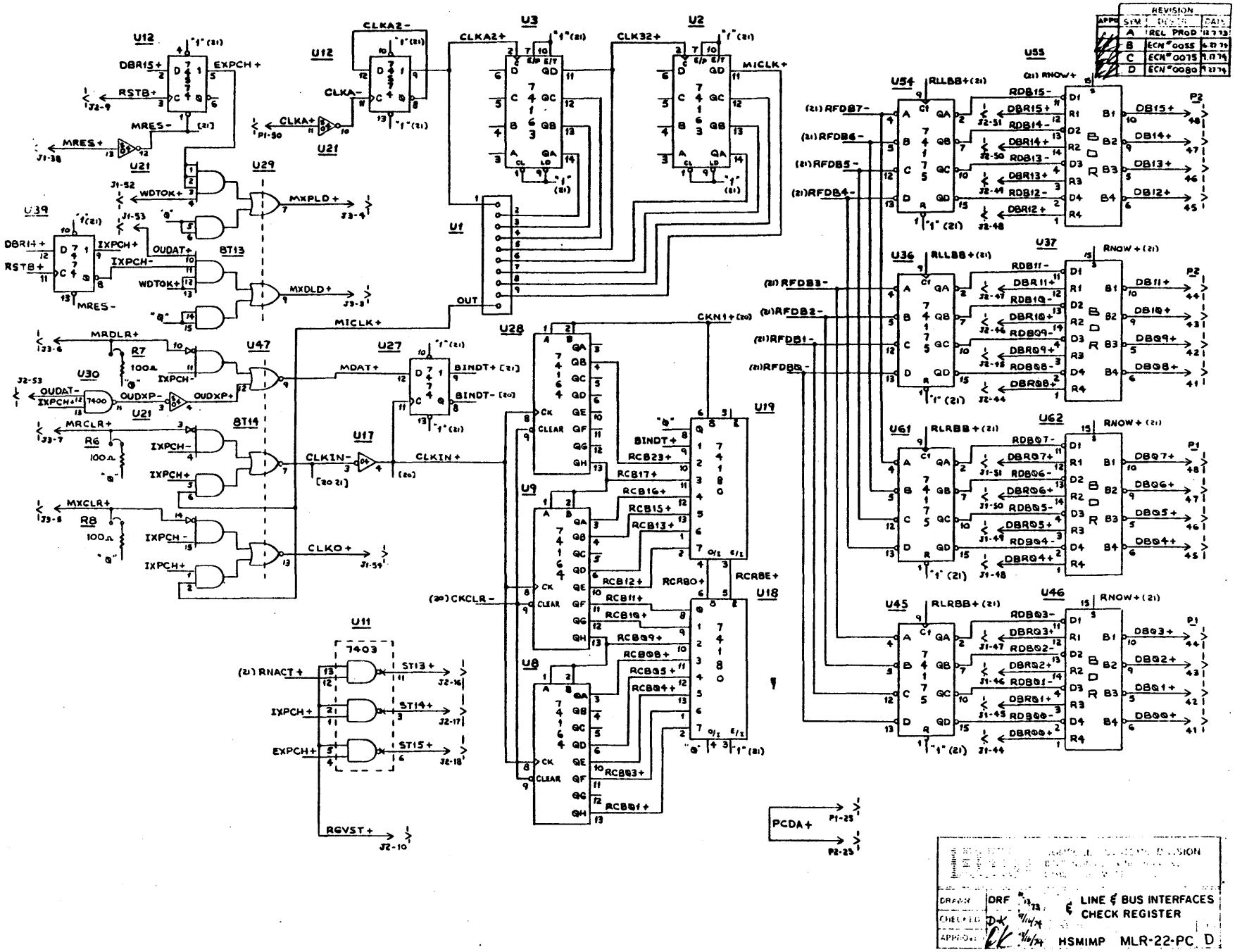

REVISION
APPD SYM DESCR DATE
A REL PROD 12.7.73
B ECN 0055 6.27.74
C ECN 0075 9.12.74
D ECN 0080 11/21/74
E ECN 0097 10.28.75
DRAWN DRF 12/18/75
CHECKED OK 12/19/75
APPROVED 12/19/75
FSM & CONTROL
HSMIMP MLR-20-PC E
MLR



DRAWN	DRF 12/74
CHECKED	DK 12/5/74
APPROVED	GL 12/4/74

FIFO's, DMA & RLD INTERFACES

HSMIMP MLR-21-PC E


REVISION
APPD
SYM
DESCR
DATE
A
REL PROD
B
ECN #0055
C
ECN #0075
D
ECN #0080
U12
U3
U2
U55
U54
U37
U36
U62
U61
U46
U45
U1
U21
U29
U39
U47
U30
U27
U28
U19
U9
U8
U18
U17
U11
7403
DBR15+
EXPCH+
RSTB+
MRES-
MRES+
CLKA2-
CLKA+
CLKA-
CLKA2+
CLK32+
MICLK+
WDTOK+
MXPLD+
MXDLD+
DBR14+
IXPCH+
IXPCH-
OUDAT+
BT13
MRDLR+
R7
100Ω
OUDAT-
OUDXP-
OUDXP+
MDAT+
BINDT+ (21)
BINDT- (20)
MRCLR+
R6
BT14
CLKIN-
CLKIN+
MXCLR+
R8
CLKO+
OUT
CKN1+(20)
(20) CKCLR-
RCB23+
RCB17+
RCB16+
RCB15+
RCB13+
RCB12+
RCB11+
RCB10+
RCB09+
RCB08+
RCB05+
RCB04+
RCB03+
RCB01+
RCR80+
RCR8E+
BINDT+
(21) RNACT+
ST13+
ST14+
ST15+
RGVST+
PCDA+
P1-25
P2-25
(21) RFDB7-
(21) RFDB6-
(21) RFDB5-
(21) RFDB4-
(21) RFDB3-
(21) RFDB2-
(21) RFDB1-
(21) RFDB0-
RLLBB+(21)
RLRBB+(21)
RNOW+(21)
RDB15-
RDB14-
RDB13-
RDB12-
RDB11-
RDB10-
RDB09-
RDB08-
RDB07-
RDB06-
RDB05-
RDB04-
RDB03-
RDB02-
RDB01-
RDB00-
DB15+
DB14+
DB13+
DB12+
DB11+
DB10+
DB09+
DB08+
DB07+
DB06+
DB05+
DB04+
DB03+
DB02+
DB01+
DB00+
P2
P1
LINE & BUS INTERFACES
CHECK REGISTER
DRAWN
ORF
CHECKED
APPROVED
HSMIMP
MLR-22-PC
D

MLR

Low Speed Modem Interface Transmit

MLX-Ø2 Logic Description

MLX-Ø5 Technical Reference

MLX-1Ø Assembly Drawing

MLX-2Ø Schematics

[redacted]

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR [illegible]	11/7/78	DK

MLX

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN DK Francis 11/7/78

CHECKER

ENGINEER [illegible] 11/9/78

APP'D FOR REL [illegible] 11/9/78

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

MLX LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		MLX-02

SCALE	REV	SHEET
	A	1 OF 26

TECHNICAL DESCRIPTION OF THE LOW-SPEED MODEM INTERFACE

The low-speed modem interface is designed to communicate with the 303 modem at speeds of up to 250 Kb per second. A functional description is given elsewhere and should be read and understood before attempting to read this document. The low-speed modem interface is made up of two cards: MLX, the transmit side, and MLR, the receive side. We will deal with the transmit side first.

A block diagram of MLX is given in Figure 1 and shows which pieces are covered by each of the drawings in the MLX series. On the left of this drawing is the ICM connector which connects to the DMA and to the MLR. All communications with MLX go through this connector. The only connections to the INFIBUS are the PCD pins which are simply used to jumper the precedence pulse through, and the negative 15-volt supply pin, in addition, of course, to the ground and +5 volt supplies. The data from the INFIBUS to be transmitted is received in BDRs on the MLR card and passed across the ICM to the MLX.

MLX

MLX24

The data is received on the MLX in three 6-bit latches, type 74174, as shown on MLX24. Also latches in one of these 74174s is the end of block signal XEOBC, which is the transmit end of block (XEOB) from the DMA, and XLAST. XLAST is the output of a flip-flop which stores the last packet indicator (the least significant bit of the transmit start pointer).

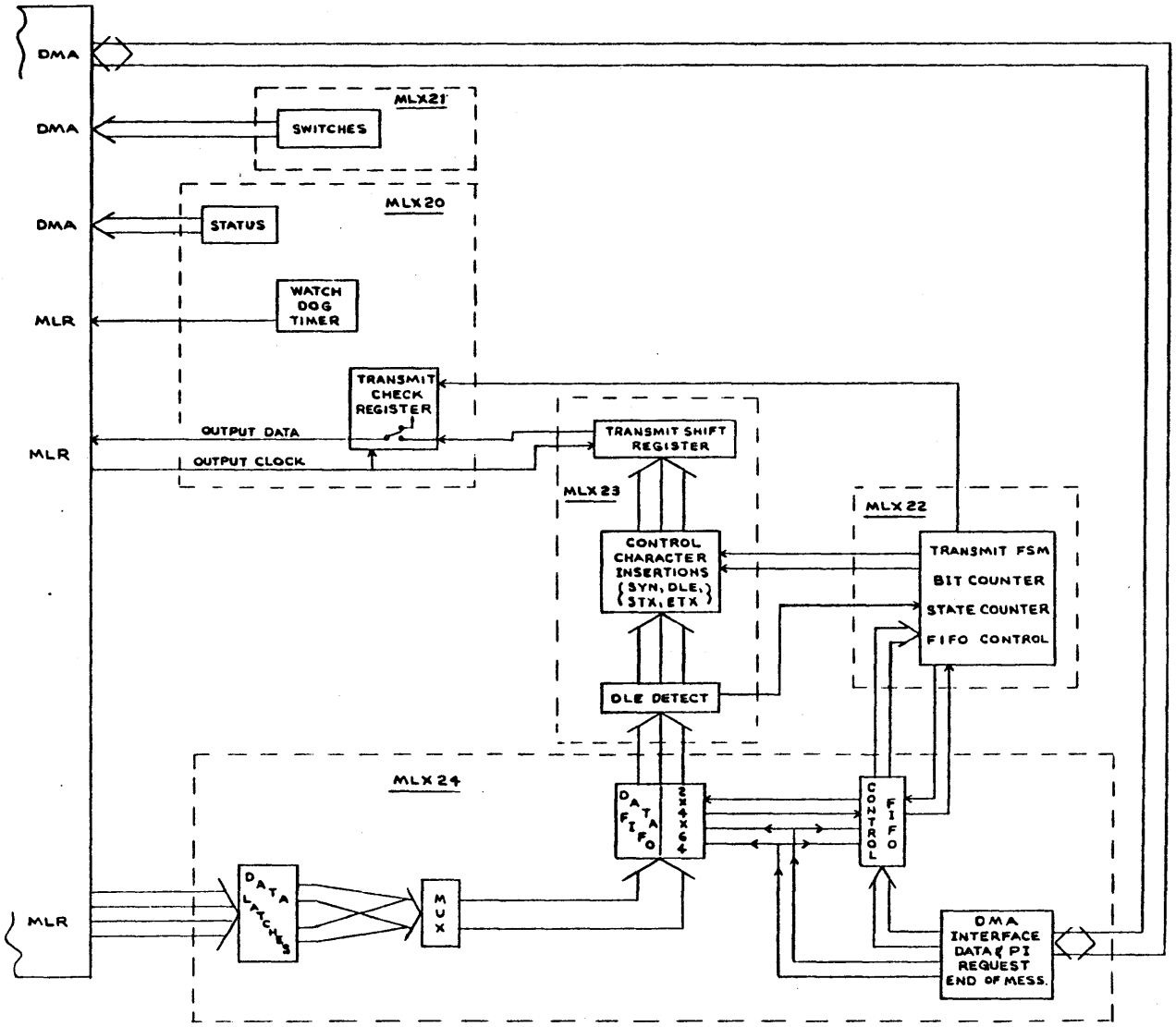


FIG1

MLX BLOCK DIAGRAM

MLX-02-SHT 2a

The 16 data bits from these latches are then fed to two 74157 multiplexers, which select the left or right half-word to be fed to the 3341 FIFO buffers. The latched end of buffer indicator, XEOBB, is ANDed with XBYT2, a signal which is true when the second byte is being loaded, to make XEOB2, a last byte of packet indicator, which is presented to the control FIFO.

The FIFOs are controlled by two sets of two control lines, one set for FIFO input and one set for FIFO output. Each set consists of a READY line from the FIFO, indicating that the FIFO is ready for the next transfer, and a SHIFT line driven to the FIFO, which commands the FIFO to shift in or out the next nibble. The three FIFOs (two data FIFOs and one control FIFO) are driven in parallel, to make, in effect, one 12-bit wide, 64-bit long FIFO. To accomplish this, the ready lines are ANDed together to make an overall ready line: XIR for transmit input ready, XOR for transmit output ready. The three shift lines are driven in parallel from the same signal: XSI for transmit shift input, and XSO for transmit shift output.

MLX

The two flip-flops and two AND gates at the top of MLX 24 form the DMA data control machine. Transmit reset XRES causes the flop XREDF (transmit ready flop) to be set, indicating, as soon as transmit active comes true, that the transmit side is ready for data from the bus. When the data appears, as signified by the truth of XNOW, XREDF is cleared, and the data is loaded into the 74174 latches. Assuming the FIFOs are prepared to accept the data, the truth of XIR, combined with the falsity of transmit ready flop, causes XSI to come true, shifting the first data byte into the FIFOs. As the FIFOs take this byte, XIR will become false. The trailing edge of XIR will cause XBYT2 to toggle, causing the 74157 multiplexers to switch to selecting the most

significant half-word. The trailing edge of XIR also causes the status of XBYT2 to be strobed in to the transmit ready flop. However, since XBYT2 was false, having been cleared by transmit reset, the transmit ready flop remains clear.

As soon as this first data byte has vacated the first level of the FIFO, so that the FIFO is once again ready to accept data, XIR again comes true. Since transmit ready flop is still false, XSI also becomes true, shifting in to the FIFO the most significant half-word of the first word. As soon as the FIFO has accepted this byte, XIR again goes false. This strobes XBYT2 into XREDF, setting XREDF, indicating that the buffers are ready for the next data word. It also simultaneously clears XBYT2. When the next word arrives, as indicated by XNOW, XREDF is cleared, and the cycle repeats. This data control cycle will continue indefinitely, being stopped only by transmit active going false.

The pseudo interruption control logic shown on the right side of MLX24 is prototypical of that in any DMA controlled device. Transmit active (XACTV) is set on the leading edge of the transmit start pulse, and is cleared by either a transmit reset, a transmit quit signal from the DMA, a transmit restart signal (being the writing of the transmit begin pointer), or a normal completion, being a transmit end of block signal from the DMA at XNOW time.

When transmit active goes false, it causes transmit normal interrupt XNINT to go true, requesting a transmit pseudo interrupt. This flop is cleared by either master reset, transmit interrupt done, or transmit quit. It is explicitly not cleared by transmit reset, so that a program generated reset, if written while transmit is active, will cause a pseudo interrupt. This is to assure that one pseudo interrupt is returned for each buffer that the program gives the interface.

The quit interrupt flip-flop XQINT, at the lower right-hand corner of MLX24, is to provide a pseudo interrupt if a quit was encountered during a data cycle. If XACTV was true when XQUIT happened, the quit must have come on a data cycle, and the transmit quit interrupt flip-flop is set. The flop is cleared by either the transmit interrupt done or a transmit reset. Note that the quit in any case clears transmit active so that if a pseudo interrupt request is quit upon, X active will no longer be true, so that XQINT will not be set again.

The one remaining flip-flop on MLX24 is the transmit error flip-flop in the upper left corner. This logic defines reading the pointer while transmit is active, or between a reset command and the following transmit start command as an error or exception condition.

MLX23 Drawing MLX23 contains the transmit shift register, the control character insertion logic, and the DLE detection logic.

The transmit shift register is made up of the two 4-bit shift registers, type 7495, at F2 and G2 shown on the right-hand side of MLX23. Data is loaded into these shift registers in parallel each eighth bit time as indicated by the signal XBIT8 being true, and on successive bit times is shifted out the shift out data line SODAT. The data loaded into the shift register may either be the text data from the FIFO on lines XFDB0 through XFDB7, for transmit FIFO data bit 0 through 7, or any one of the four control characters SYN DLE, STX, or ETX. The signal CXFSM for Clear Transmit Finite State Machine, indicates that the byte to go out on the line next, is a text byte, and therefore causes the FIFO data to be loaded into the shift register.

DLETX state means that the next character to be sent is an ETX and therefore causes the 200 bit, the 2 bit, and the 1 bit to be set, and the other bits cleared, at load time. SYNXM- is a signal which means that a SYN character is to be transmitted next. This signal is true when the FSM is in check character 3 state (CC3XM), in which case the first SYN character is transmitted next, or from being in SYN1X state, in which case the second SYN character is to be transmitted next, or being in DLSYN state, in which case the protocol idle SYN character is to be transmitted next, or being in SYN2X state, and having no data available, as indicated by XORS (transmit output ready synchronized) being false. This signal explicitly causes the 4-bit and the 2-bits to be loaded as one and by not explicitly disabling the loading of the 20-bit also causes this bit to be loaded as one producing a SYN character code 26.

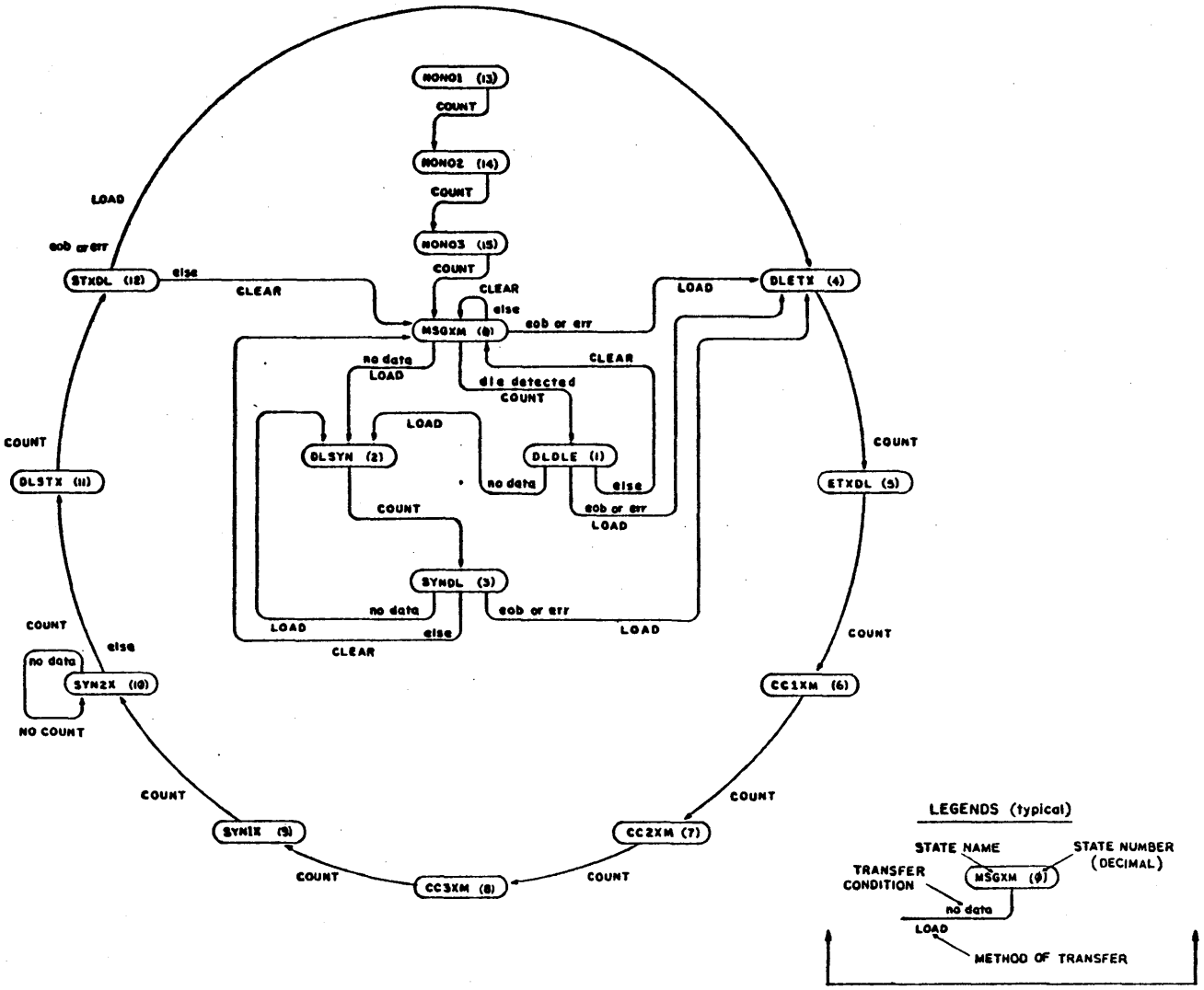
DLSTX state indicates that an STX (character code 2) is to be sent next, and therefore causes the 2 bit to be loaded as one, and the other bits as zero. The loading of the 20 bit is a special case, due to the fact that most of the funny control states cause either a DLE or a SYN to be transmitted, and both of these characters require the 20-bit to be set. The logic on the 20-bit therefore causes the 20-bit to be set unless CXFSM is true, indicating that a text byte is to be transmitted, or DLETX is true, in which case ETX is to be transmitted next, or DLSTX is true, indicating that an STX is to be transmitted next, or NONO3 is true. This last is an error condition, indicating that the finite state machine got into one of the three illegal states. In this case, after clearing the transmit check register to assure that an invalid checksum will be sent, a zero data byte is transmitted, followed by a standard end of packet sequence, followed by the now invalid checksum. The NONO3 term on this gate is to permit transmission of the zero data byte.

The four gates in the lower left of drawing MLX 23 are the data DLE detector, simply watching the text bytes for data bit 4 to be 1 while all the others are at zero. This condition causes DLEXD to come true.

MLX22 Drawing MLX22 shows transmit finite state machine and control logic. A state diagram of this machine is given in Figure 2.

The 74163 at the upper left corner of MLX22, is a modulo 8 counter, implemented as a 4-bit counter synchronously parallel loaded with an 8 whenever the count gets to 15. This makes the signal XBIT8 come true for 1-bit time out of every 8. XBIT8 ANDed with CLKO gives XSCLK-, a clock pulse one-half bit time wide every character time, which is used as the clock on the state counter 74163 in D5. At clock time, this counter can be either loaded, cleared, counted, or not counted.

The not count condition is used in SYN2X state if no data is ready from the FIFO, to remain in SYN2X state, transmitting SYN characters. The state counter is synchronously cleared to enter or remain in message state, transmitting text characters. The conditions for this are that data be available from the FIFO, as indicated by XORS (transmit output ready synchronized), that there be no error or end of block condition, indicated by ERB-, and that we be in one of the states after which it is permissible to transmit a text character. These states are STXDL, the normal entrance to message state at the beginning of the message, DLDLE, indicating that the second DLE is being sent after discovering a DLE in the text string, SYNDL, indicating that the SYN character of a protocol idle sequence has been sent, or message state, but only if a text DLE character has not just been discovered. The



MLX STATE DIAGRAM

FIG 2

MLX-02-SHT 7a

OR of these state conditions, CORLX (clear or load transmit Finite State Machine) causes the transmit finite state machine to be either cleared or loaded. If there has been no error or end of block indicator, and there is data available, as indicated by XORS, then the state counter is cleared and the text character is transmitted. Otherwise the state counter is loaded with either a 2 or a 4. The 4 is loaded on error or end of block, causing the machine to step into DLETX state, preparatory for the end of packet sequence. A 2 is loaded if error or end of block is not true, but no data is available, causing the machine to step into DLSYN state, for the protocol idle sequence. The only condition under which the finite state machine is neither cleared nor loaded while in message state, is the case where a DLE has been discovered in the text string. In this case the machine counts to state 1, DLDLE state, to insert the doubling DLE. The 74154 in E3 is a 4-bit decoder, and decodes the state of the machine.

The 7474 in F5, drawn in the lower left hand area of MLX22, is used to capture and synchronize the state of the XOR, indicating whether or not the FIFO's have text available for transmission. These flip-flops are clocked by the transmit clock signal CLKO. The first flop samples the XOR line on the leading edge of CLKO. The second samples that 1-bit time later, having allowed it time to settle. If this flip-flop is true at XBIT8 time, and the finite state machine is prepared to send a text byte, as indicated by CSFSM, XSO (transmit shift output) is brought true to the FIFOs for 1-bit time, during which time the byte is loaded into the transmit shift register. At the same time, the end of block bit from the control FIFO is strobed into the 7474 in F6, giving XEOBB (transmit end of block buffered). This flop remains true until entering check character 1 state.

MLX

XEOBB is then ORed with synchronized error signal to form ERB, the error or end of block signal used in controlling the finite state machine. The synchronized error signal, XERS, comes from a 7476, which is set by the trailing edge of a CLKO of XRESB (transmit reset buffered) is set. It will remain set until the transmit finite state machine enters SYN2 state, the idle state.

There is a potential race here, in that XRESB may come true just as entering or leaving SYN2 state. This is irrelevant however, since ERB is not used for many bit times thereafter, and will therefore be stable by the time it is used. It does not matter whether it stabilizes true or false, since the transmit reset is quite entitled to discard a packet, which is all that will occur if XERS is set. XRESB comes from the other half of the 7476, which is simply used to latch the fact that a transmit reset has occurred. This latch also is cleared by being in SYN2 state.

The flip-flop at the extreme lower left-hand corner of MLX22 is used to latch the DLE detection signal at the time a data byte is loaded into the transmit shift register, to cause the transmit finite state machine to step into the DLE doubling state DLDLE at the next byte time.

The reset logic at the lower right-hand corner of MLX22 is used to clear the FIFO, the transmit check register and the transmit finite state machine. The FIFO requires a 400 nanosecond pulse to be cleared reliably; the one shot (74123) is used to generate this pulse. This one shot is fired by MXRES (my transmit reset) which is generated either on a transmit reset, or being in NONO3, the third illegal state. The output check register is cleared on either of these conditions, or on being in SYN2 state, i.e., just before the beginning of the packet.

MLX21 is a most uninteresting drawing which shows the switches required by the DMA. These switches are used to select PI address, device address, device characteristics, and transmit and receive PI levels. To the extent that the print is not self-explanatory, the modem functional spec and DMA functional spec should answer any questions.

MLX20 shows the transmit check register and status bits, and the watchdog timer. The check register computes a 24-bit CRC checksum compatible with that used in the 316/516 series modem interfaces. The three 74164s form a 24-bit straight shift register. The two 74180 parity chips compute the exclusive OR of selected bits in these shift registers and the bit being transmitted. This exclusive OR bit is then fed back in to be the input to the shift registers.

The output of a simulator of this check register is given in Appendix A. It shows the state of each of the 24 bits of the check register at each bit time during the transmission of a number of different 2-word messages. This might prove handy in debugging hard check register failures, but hopefully a problem could be localized to the check register by merely noting that the transmitted checksum was bad despite the transmitted data being correct, in which case trail replacement of the few bugs involved in the check register would probably be the easiest way to diagnose the failure.

MLX

When the checksum is not actually being transmitted, as indicated by the level SNDCK- being true, a data bit presented at the input to the exclusive OR gate is in fact the inverse to the data bit being shifted out, due to the fact that the 7400 which produces XDNSC (transmit data not send check) inverts the

data presented to it. To overcome this problem, SNDCK- itself is presented at another input to the exclusive OR network. This has the effect of inverting the sense of the exclusive OR when this signal is true, that is when data is being shifted out, but not inverting it when the checksum itself is being transmitted.

The remaining logic at the top of MLX20 is used to select either the shift-out data or the checksum itself, to be presented to the MLR through the ICM as OUDAT, the output data. The flip-flop at the upper left of MLX20, XZRCK, is used to record the MLX as being in a "send 0 checksum" state, in which case the check register is always held to zero, and by sending appropriate data, the receive check register can be tested.

Appendix B lists various two-word patterns which will produce a single bit in error in the receive checksum, when the transmitted checksum is zero, as well as a pattern which will produce a correct checksum when the transmitted checksum is zero.

The logic on the left-hand side of MLX20 is used to present the various status bits to the DMA, as described in the modem functional spec and the DMA functional spec. The 74123 at the extreme right-hand side of MLX20 is the watchdog timer. With its 30K resistor and its 100 microfared capacitor, it renders the signal WDTOK true if the transmit status word has been written any time within the last second. This retriggerable one-shot is fired by XSTB, the transmit write status line from the DMA. This concludes the discussion of MLX.

MLX-Ø2 LOGIC DESCRIPTION - APPENDIX A

DATA	Ø23	Ø02	Ø00	Ø00	Ø00	Ø00	Ø20	203

Ø2Ø

Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
1	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ

Ø02

Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
1	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ

ØØØ

Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ

ØØØ

Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	1	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ
Ø	Ø	ØØØØØØØØ	ØØØØØØØØ	ØØØØØØØØ

MLX

0	0	00010010	1100$\bar{1}$100	0$\bar{1}$111010
0	0	00010001	01$\bar{1}$00110	00111101
0	1	00000100	10$\bar{1}$10011	00011110

000

0	0	10000010	0101$\bar{1}$001	10001111
0	1	01000001	00$\bar{1}$01100	11000111
0	1	10100000	1001$\bar{1}$110	01100011
0	1	11010000	0100$\bar{1}$011	00110001
0	0	11101000	00$\bar{1}$00101	10011000
0	0	01110100	0001$\bar{1}$010	11001100
0	1	00111010	0000$\bar{1}$001	01100110
0	1	10011101	00000100	10110011

000

0	0	11001110	$\bar{1}$0000010	01011001
0	0	01100111	0$\bar{1}$000001	00101100
0	1	00110011	$\bar{1}$0$\bar{1}$00000	10010110
0	0	10011001	$\bar{1}$10$\bar{1}$0000	01001011
0	0	01001100	11$\bar{1}$01000	00100101
0	0	00100110	01$\bar{1}$10100	00010010
0	0	00010011	00$\bar{1}$11010	00001001
0	1	00001001	10011101	00000100

020

0	0	10000100	1100$\bar{1}$110	10000010
0	0	01000010	01$\bar{1}$00111	01000001
0	1	00100001	00$\bar{1}$10011	10100000
0	0	10010000	1001$\bar{1}$001	11010000
1	1	01001000	0100$\bar{1}$100	11101000
0	0	10100100	00$\bar{1}$00110	01110100
0	0	01010010	0001001$\bar{1}$	00111010
0	0	00101001	0000$\bar{1}$001	10011101

203

1	0	00010100	10000100	11001110
1	1	00001010	01000010	01100111
0	0	10000101	00$\bar{1}$00001	00110011
0	1	01000010	1001$\bar{0}$000	10011001
0	1	10100001	01001000	01001100
0	0	11010000	$\bar{1}$0$\bar{1}$00100	00100110

```
Ø   Ø      Ø1101ØØØ   Ø1Ø1ØØ1Ø   ØØØ1ØØ11
1   1      ØØ11Ø1ØØ   ØØ1Ø1ØØ1   ØØØØ1ØØ1


Ø   Ø      1ØØ11Ø1Ø   ØØØ1Ø1ØØ   1ØØØØ1ØØ
Ø   Ø      Ø1ØØ11Ø1   ØØØØ1Ø1Ø   Ø1ØØØØ1Ø
Ø   Ø      ØØ1ØØ11Ø   1ØØØØ1Ø1   ØØ1ØØØØ1
Ø   1      ØØØ1ØØ11   Ø1ØØØØ1Ø   1ØØ1ØØØØ
Ø   Ø      ØØØØ1ØØ1   1Ø1ØØØØ1   Ø1ØØ1ØØØ
Ø   1      1ØØØØ1ØØ   11Ø1ØØØØ   1Ø1ØØ1ØØ
Ø   1      ØØØØØ1Ø1   Ø11Ø1ØØØ   Ø1Ø11ØØ1Ø
Ø   1      ØØØØØØ1Ø   ØØ11Ø1ØØ   ØØ1Ø1ØØ1


Ø   Ø      ØØØØØØØØ   1ØØ1Ø1Ø1Ø   ØØØ1Ø1ØØ
Ø   1      ØØØØØØØØ   Ø1ØØ1Ø1Ø   ØØØØ1Ø1Ø
Ø   1      ØØØØØØØØ   ØØ1ØØ11Ø   1ØØØØ1Ø1
Ø   1      ØØØØØØØØ   ØØØ1ØØ11   Ø1ØØØØ1Ø
Ø   Ø      ØØØØØØØØ   ØØØØ1ØØ1   1Ø1ØØØØ1
Ø   1      ØØØØØØØØ   ØØØØØ1ØØ   11Ø1ØØØØ
Ø   Ø      ØØØØØØØØ   ØØØØØ2Ø1Ø   Ø11Ø1ØØØ
Ø   1      ØØØØØØØØ   ØØØØØØØ1   ØØ11Ø1ØØ


Ø   1      ØØØØØØØØ   ØØØØØØØØ   1ØØ11Ø1Ø
Ø   1      ØØØØØØØØ   ØØØØØØØØ   Ø1ØØ11Ø1
Ø   1      ØØØØØØØØ   ØØØØØØØØ   ØØ1ØØ11Ø
Ø   Ø      ØØØØØØØØ   ØØØØØØØØ   ØØØ1ØØ11
Ø   Ø      ØØØØØØØØ   ØØØØØØØØ   ØØØØ1ØØ1
Ø   1      ØØØØØØØØ   ØØØØØØØØ   ØØØØØ1ØØ
Ø   Ø      ØØØØØØØØ   ØØØØØØØØ   ØØØØØØ1Ø
Ø   1      ØØØØØØØØ   ØØØØØØØØ   ØØØØØØØ1
```

MLX

DATA 020 002 223 371 375 000 020 203

020

0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
1	1	00000000	00000000	00000000
0	0	10000000	00000000	00000000
0	1	01000000	00000000	00000000
0	0	10100000	00000000	00000000

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

223

1	0	10001111	01010000	00000000
1	1	01000111	10101000	00000000
0	1	10100011	11010100	00000000
0	0	11010001	11101010	00000000
1	1	01101000	11110101	00000000
0	1	10110100	01111010	10000000
0	1	11011010	00111101	01000000
1	0	11101101	00011110	10100000

371

1	0	01110110	10001111	01010000
0	1	00111011	01000111	10101000
0	1	10011101	10100011	11010100
1	0	11001110	11010001	11101010
1	1	01100111	01101000	11110101
1	1	10110011	10110100	01111010
1	0	11011001	11011010	00111101
1	0	01101100	11101101	00011110

375

1	1	00110110	01$\bar{1}$10110	10001111
0	1	10011011	00$\bar{1}$11011	01000111
1	0	11001101	$\bar{1}$001$\bar{1}$101	10100011
1	0	01100110	$\bar{1}$100$\bar{1}$110	11010001
1	1	00110011	01$\bar{1}$00111	01101000
1	1	10011001	$\bar{1}$0$\bar{1}$10011	10110100
1	0	11001100	$\bar{1}$101$\bar{1}$001	11011010
1	1	01100110	01$\bar{1}$01$\bar{1}$00	11101101

000

0	0	10110011	00$\bar{1}$10110	01110110
0	0	01011001	10011011	00111011
0	0	00101100	$\bar{1}$100$\bar{1}$101	10011101
0	0	00010110	01$\bar{1}$00110	$\bar{1}$1001110
0	0	00001011	00$\bar{1}$10011	01100111
0	0	00000101	$\bar{1}$001$\bar{1}$001	10110011
0	0	00000010	$\bar{1}$1001$\bar{1}$00	11011001
0	0	00000001	01100110	01101100

020

0	0	00000000	$\bar{1}$0$\bar{1}$10011	00110110
0	0	00000000	01011001	10011011
0	0	00000000	00$\bar{1}$01$\bar{1}$00	$\bar{1}$1001101
0	0	00000000	0001011$\bar{0}$	01100110
1	0	00000000	00001011	00110011
0	0	00000000	00000101	10011001
0	0	00000000	00000010	11001100
0	0	00000000	00000001	01100110

203

1	0	00000000	00000000	10110011
1	0	00000000	00000000	01011001
0	0	00000000	00000000	00101100
0	0	00000000	00000000	00010110
0	0	00000000	00000000	00001011
0	0	00000000	00000000	00000101
0	0	00000000	00000000	00000010
1	0	00000000	00000000	00000001

0	0	00000000	00000000	00000000

MLX

```
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
```

```
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
```

```
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
```

DATA 020 002 221 024 342 000 020 203

020

```
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
0   0       00000000    00000000    00000000
```

1	1	00200003	00000000	00000000
0	0	10000000	00030000	00000000
0	1	01000000	00000000	00000000
0	0	10100003	00000000	00000000

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

221

1	0	10001111	01010000	00000000
0	0	01000111	10101000	00000000
0	1	00100011	11010100	00000000
0	1	10010001	11101010	00000000
1	1	11001000	11110101	00000000
0	0	11100100	01111010	10000000
0	1	01110010	00111101	01000000
1	1	10111001	00011110	10100000

MLX

024

0	1	11011100	10001111	01010000
0	1	11101110	01000111	10101000
1	0	11110111	00100011	11010100
0	1	01111011	10010001	11101010
1	1	10111101	11001000	11110101
0	0	11011110	11100100	01111010
0	1	01101111	01110010	00111101
0	0	10110111	10111001	00011110

342

0	1	01011011	11011100	10001111
1	1	10101101	11101110	01000111
0	0	11010110	11110111	00100011
0	0	01101011	01111011	10010001
0	0	00110101	10111101	11001000

1	1	00011010	1101$\bar{1}$110	11100100
1	0	10001101	01$\bar{1}$01111	01110010
1	1	01000110	10$\bar{1}$10111	10$\bar{1}$11001

000

0	0	10100011	0101$\bar{1}$011	$\bar{1}$1011100
0	1	01010001	$\bar{1}$01$\bar{1}$1101	11101110
0	1	10101003	11010110	11110111
0	0	11010100	01$\bar{1}$01011	01111011
0	1	01101010	00$\bar{1}$10101	10111101
0	0	10110101	00011$\bar{1}$010	11011110
0	0	01011013	10001$\bar{1}$101	01101111
0	0	00101101	01000110	10110111

020

0	0	00010110	10$\bar{1}$00011	01011011
0	0	00001011	01010001	10101101
0	0	00000101	$\bar{1}$01$\bar{1}$01000	11010110
0	0	00000010	11010103	01101011
1	0	00000001	01$\bar{1}$01010	00110101
0	0	00000000	10110101	00011010
0	0	00000000	01011$\bar{1}$010	10001101
0	0	00000000	00101$\bar{1}$101	01000110

203

1	0	00000000	00010110	10100011
1	0	00000000	00001011	01010001
0	0	00000000	00000101	10101000
0	0	00000000	00000010	11010100
0	0	00000000	00000001	01101010
0	0	00000000	00000000	10110101
0	0	00000000	00000000	01011010
1	0	00000000	00000000	00101101

0	0	00000000	00000000	00010110
0	0	00000000	00000000	00001011
0	0	00000000	00000000	00000101
0	0	00000000	00000000	00000010
0	1	00000000	00000000	00000001
0	0	00000000	00000000	00000000

```
0   0      00200000    00000000    00000000
0   0      00000000    00000000    00000000



0   0      00000000    00000000    00000000
0   0      00200000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000



0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00200000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00200000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
```

MLX

```
DATA   020  002  363  346  154  000  020  203
```

020

```
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
0   0      00000000    00000000    00000000
1   1      00000000    00000000    00000000
0   0      10000000    00000000    00000000
0   1      00000000    00000000    00000000
0   0      10100000    00000000    00000000
```

002

0	1	01010000	00000000	00000000
1	1	10101000	00000000	00000000
0	1	11010100	00000000	00000000
0	1	11101010	00000000	00000000
0	0	11110101	00000000	00000000
0	0	01111010	10000000	00000000
0	0	00111101	01000000	00000000
0	1	00011110	10100000	00000000

363

1	0	10001111	01010000	00000000
1	1	01000111	10101000	00000000
0	1	10100011	11010100	00000000
0	0	11010001	11101010	00000000
1	1	01101000	11110101	00000000
1	0	10110100	01111010	10000000
1	0	01011010	00111101	01000000
1	1	00101101	00011110	10100000

346

0	0	10010110	10001111	01010000
1	1	01001011	01000111	10101000
1	0	10100101	10100011	11010100
0	1	01010010	11010001	11101010
0	1	10101001	01101000	11110101
1	1	11010100	10110100	01111010
1	0	11101010	01011010	00111101
1	1	01110101	00101101	00011110

154

0	0	10111010	10010110	10001111
0	0	01011101	01001011	01000111
1	0	00101110	10100101	10100011
1	0	00010111	01010010	11010001
0	1	00001011	10101001	01101000
1	1	10000101	11010100	10110100
1	0	11000010	11101010	01011010
0	1	01100001	01110101	00101101

000

0	1	10110003	10111010	10010110
0	0	11011003	01011101	01001011
0	1	01101100	00101110	10100101
0	1	10110110	00010111	01010010
0	0	11011011	00001011	10101001
0	0	01101101	10000101	11010100
0	1	00110110	11000010	11101010
0	0	10011011	01100001	01110101

020

0	1	01001101	10110000	10111010
0	0	10100110	11011000	01011101
0	1	01010011	01101100	00101110
0	0	10101001	10110110	00010111
1	0	01010100	11011011	00001011
0	1	00101010	01101101	10000101
0	1	10010101	00110110	11000010
0	1	11001010	10011011	01100001

203

1	1	11100101	01001101	10110000
1	0	11110010	10100110	11011000
0	0	01111001	01010011	01101100
0	0	00111100	10101001	10110110
0	1	00011110	01010100	11011011
0	0	10001111	00101010	01101101
0	0	01000111	10010101	00110110
1	0	00100011	11001010	10011011

0	0	00010001	11100101	01001101
0	0	00001000	11110010	10100110
0	0	00000100	01111001	01010011
0	0	00000010	00111100	10101001
0	1	00000001	00011110	01010100
0	0	00000000	10001111	00101010
0	0	00000000	01000111	10010101
0	0	00000000	00100011	11001010

0	1	00000000	00010001	11100101

MLX

0	1	00000000	0000?000	11110010
0	0	00?00000	00000100	01111001
0	0	0?000000	00000010	00111100
0	0	00000000	00000001	00011110
0	0	00?00000	00?00000	10001111
0	0	00?00000	00?00000	01000111
0	1	00?00000	00000000	00100011

0	0	00?00000	00000000	00010001
0	1	0?000000	00000000	00001000
0	1	00000000	00000000	00000100
0	0	00?00000	00?00000	00000010
0	1	00000000	00000000	00000001
0	0	00000000	00000000	00000000
0	0	00000000	00000000	00000000
0	0	00000000	00?00000	00000000

MLX-Ø2 LOGIC DESCRIPTION - APPENDIX B

40000000	10011101011010111000011	271	326	301	D6B9	00C1
20000000	01100000011101111100111	006	356	343	EE06	00E3
10000000	10001111011001001110110	361	046	167	26F1	0077
04000000	01000100011010019011101	042	226	270	9622	00B8
02000000	10010011101011010110011O	311	265	146	B5C9	0066
01000000	01111101111111010000011O1	276	137	260	5FBE	00B0
00400000	11100000100010110100011O	007	321	142	D107	0062
00200000	10011011101101100100110I	331	155	262	6DD9	00B2
00100000	00111001001110000110011I	234	034	346	1C9C	00E6
00040000	00111101111111011101011O	274	337	165	DFBC	0075
00020000	00110100011111100001111OO	054	076	074	3E2C	003C
00010000	01110011100001110010010O	316	341	044	E1CE	0024
00004000	10101000100001010010100O	025	241	024	A115	0014
00002000	01011111010111101010110I	372	172	265	7AFA	00B5
00001000	11110001001101100011101O	217	154	134	6C8F	005C
00000400	11101100001110001000100I	067	034	221	1C37	0091
00000200	11010110001001011110111I	153	244	367	A46B	00F7
00000100	10100010000111110010001I	105	370	304	F845	00C4
00000040	00011110100111101000011I	170	171	341	7978	00E1
00000020	00100110010000100101001O	144	102	112	4264	004A
00000010	00000011000011111100010O	300	360	043	F0C0	0023
00000004	01001001100101001110100O	222	051	027	2992	0017
00000002	11011100101000101011000O	073	105	015	453B	000D
00000001	11100011111001011010000I	307	247	205	A7C7	0085
00000000	11001001100111111011111I	223	371	375	F993	00FD

MLX

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PUBLICATION	8-30-74	

MLX

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

MLX TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		MLX-05

SCALE	REV	SHEET
	A	1 OF –

A

See DMA, MLR

Status - address FXXX6 (receive), FXXXC (transmit)

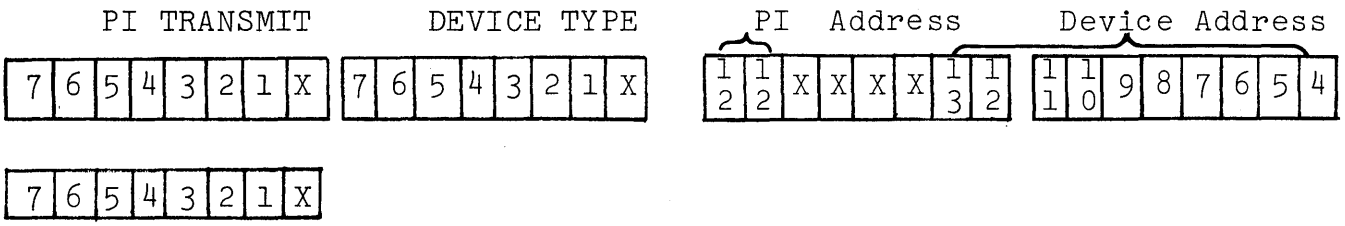
W

R

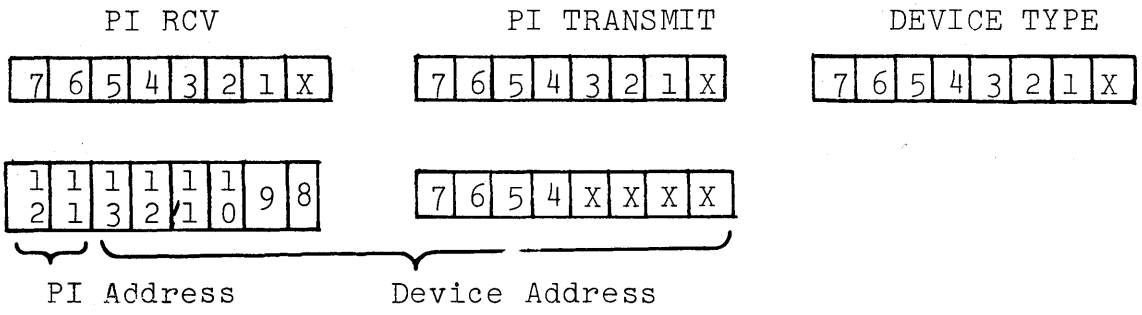
See MLR

Switches

WIRE WRAP



PC



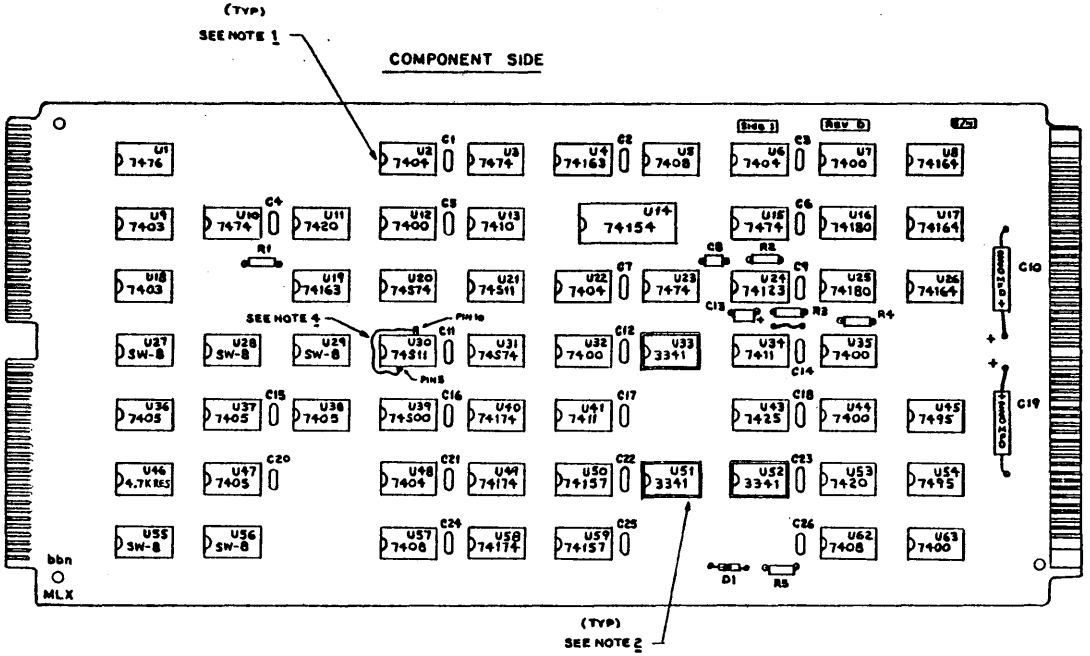
MLX

Jumpers - see MLR

Socket - see MLR

MLX-10 Assembly Drawing

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	4-25-78
MFL	B	ECN # 0157	7/31/78
	C	ECN # 289	8-10-78
	D	ECN 300	8.6.78



COMPONENT VALUES

C1-C7, C9, C11, C12, C14-C18, C20-C26 = .1 mfd CERAMIC DISC
C10, C19 = 220 mfd-10 VOLT ELECTROLYTIC
C8 = 100 pfd
C13 = 68 mfd - 6 VOLT ELECTROLYTIC
R1, R4 = 1 K Ω - 1/4 W-10 %
R2 = 13 K Ω
R3 = 39 K Ω
R5 = 100 Ω
D1 = ZENER DIODE (1N5242)

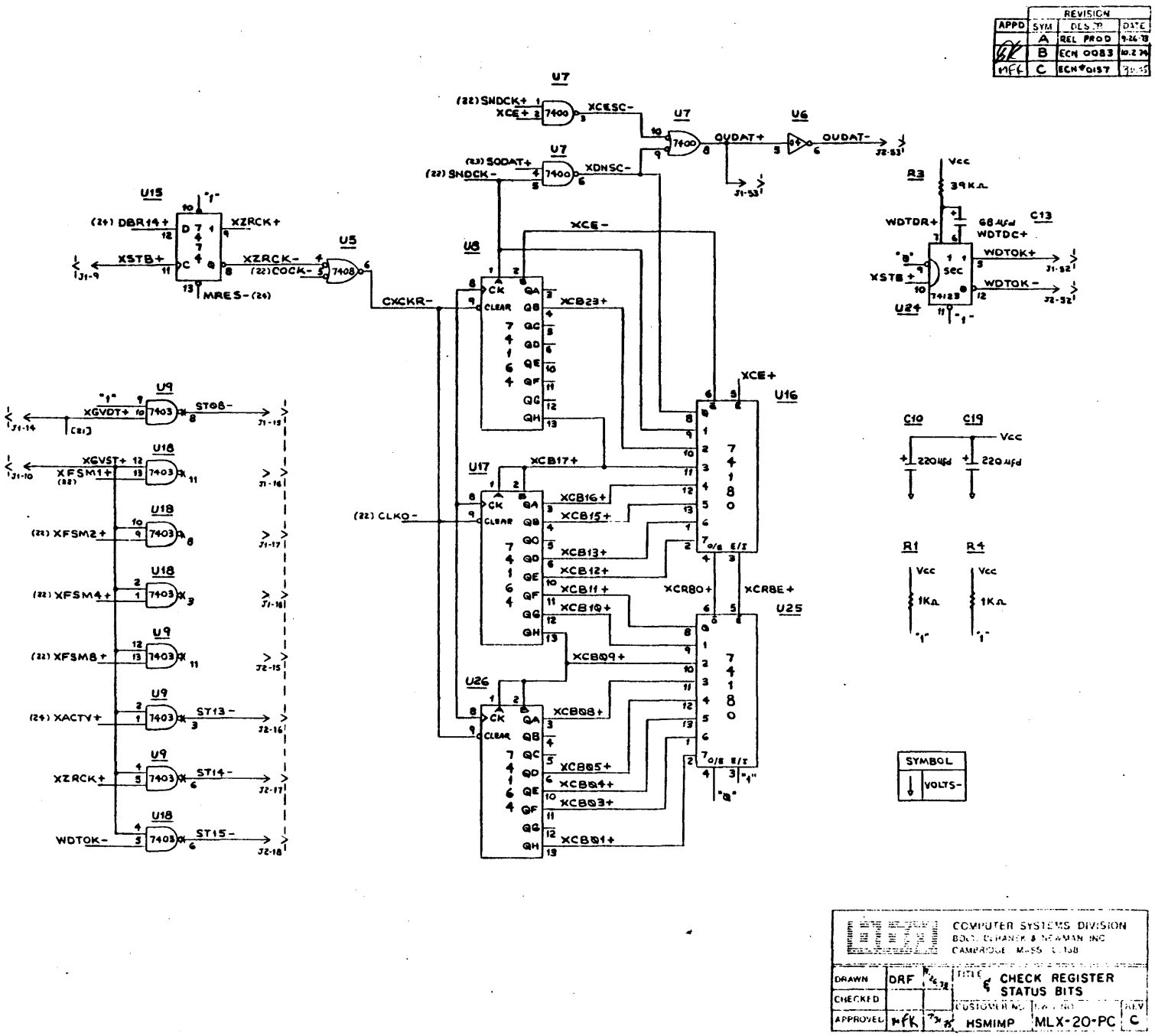
NOTES

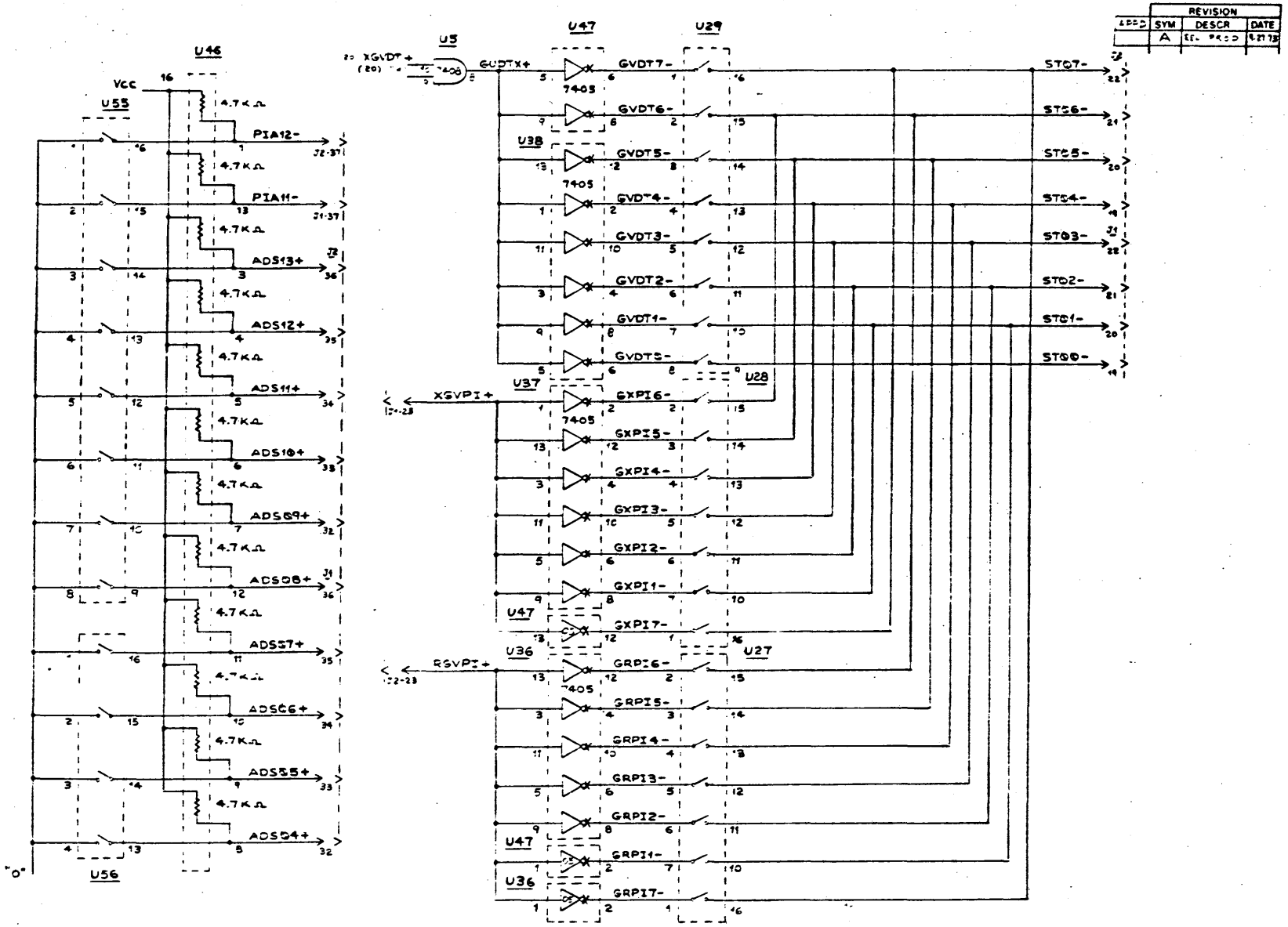
1 – NOTCH SHOWN IN BUG INDICATES INSERTION DIRECTION.
2 – U33, U51, U52, BUGS (3341) ARE MOUNTED IN SOCKETS
3 – JUMPER DIODE HOLES, ABOVE U34 WITH INSULATED WIRE
4 – CLIP THE IC LEAD (U30:10) AT BOARD LEVEL, LIFT IC LEAD AWAY FROM BOARD. SOLDER A 30 AWG W.W. WIRE FROM LIFTED LEAD TO U30:3 IC LEAD

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138

DRAWN	DRF	7/31/78	MLX PC LAYOUT	
CHECKED	DRF	7/31/78	SIZE / DWG NO	REV
APPROVED	MFK	7/31/78	HSMIMP MLX-10-PC	D

MLX-2Ø SCHEMATICS

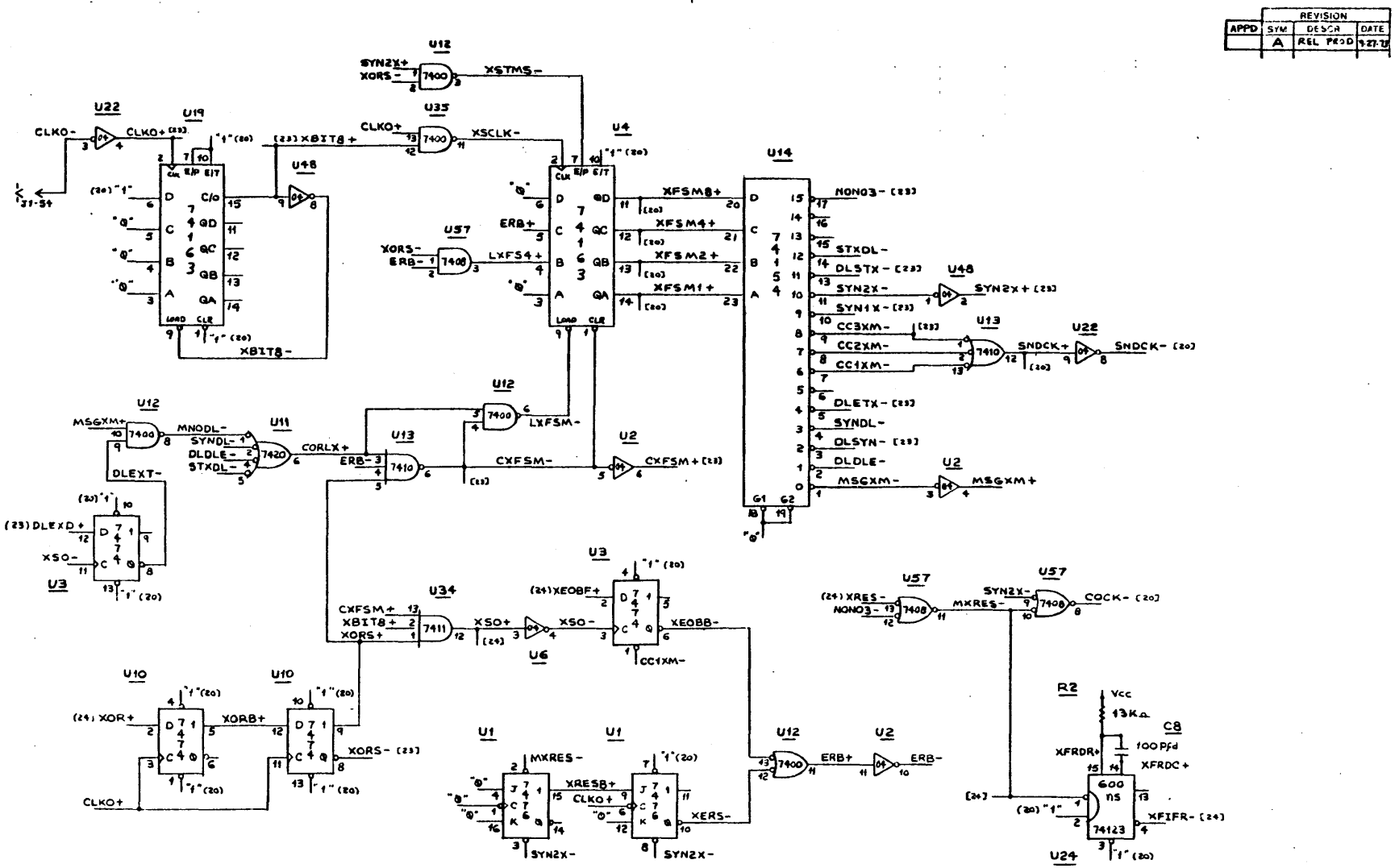

REVISION
APPD | SYM | DESCRIPTION | DATE
A | REL PROD
B | ECN 0083
C | ECN 0157
U7
U6
U15
U5
U8
U9
U16
U17
U18
U25
U26
U24
R3
R1
R4
C10
C19
C13
SYMBOL
VOLTS-
XCE-
XCE+
XCXCKR-
XCB23+
XCB17+
XCB16+
XCB15+
XCB13+
XCB12+
XCB11+
XCB10+
XCB09+
XCB08+
XCB05+
XCB04+
XCB03+
XCB01+
XCR80+
XCRBE+
XZRCK+
XZRCK-
XSTB+
MRES-(24)
CXCKR-
CLKO-(22)
SNDCK+(22)
SNDCK-(22)
SODAT+(23)
XCESC-
XDNSC-
OUDAT+
OUDAT-
WDTDR+
WDTDC+
WDTOK+
WDTOK-
XSTB+
XGVDT+
XGVST+
XFSM1+
XFSM2+
XFSM4+
XFSM8+
XACTY+
WDTOK-
ST08-
ST13-
ST14-
ST15-
Vcc
39KΩ
68μfd
220μfd
1KΩ
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS
DRAWN DRF
CHECKED
APPROVED MFK
TITLE CHECK REGISTER STATUS BITS
CUSTOMER NO. HSMIMP
MLX-20-PC
REV C



REVISION			
LTR'D	SYM	DESCR	DATE
	A	ECL PROD	5/21/73

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

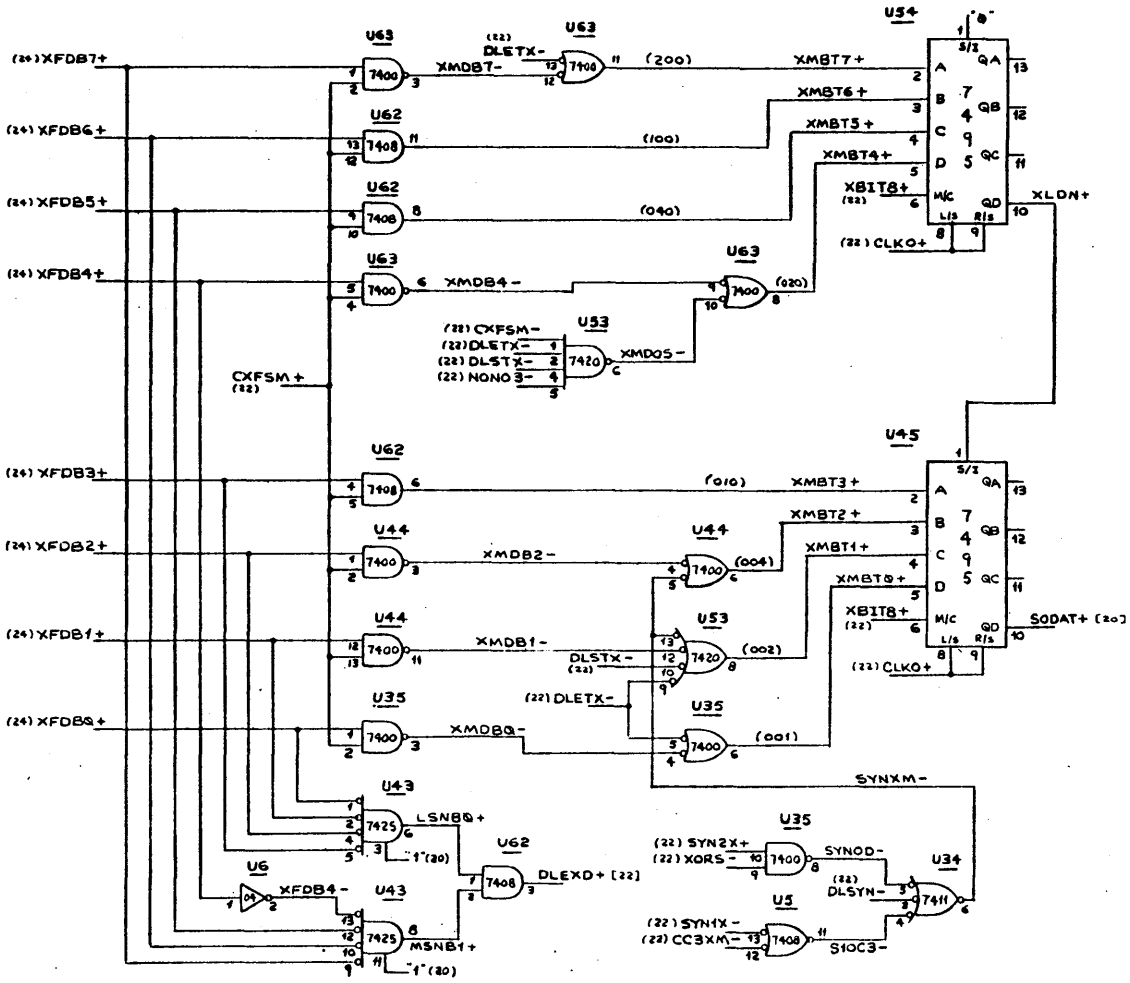
DRAWN	DRF	5/18/73	TITLE: MLX SWITCHING
CHECKED			
APPROVED			CUSTOMER NO: HSMIMP; DWG NO: MLX-21-PC; REV: A



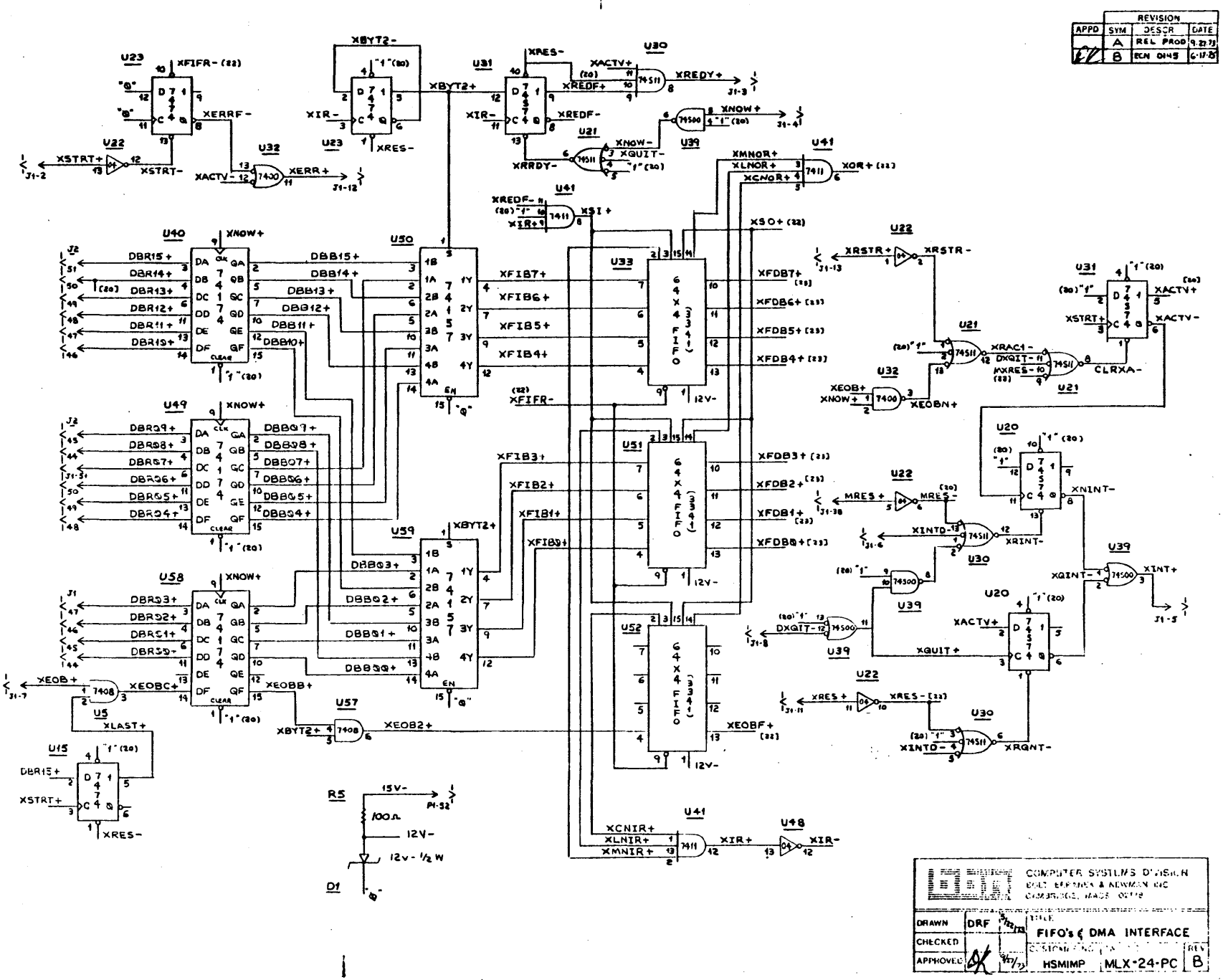
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	5/21/73	TITLE	F S M & CONTROL
CHECKED				
APPROVED		7/11/73	CUSTOMER NO HSMIMP	DWG NO MLX-22-PC REV A

APPD	REVISION		
	SYM	DESCR	DATE
	A	REL PROD	9-27-73



COMPUTER SYSTEMS DIVISION BOLT BERANEK & NEWMAN INC CAMBRIDGE MASS 02138			
DRAWN	DRF	9/19/73	TITLE: SHIFT REGISTER & CHARACTER LOADING
CHECKED			
APPROVED		9/27/73	CUSTOMER NO: HSMIMP — DWG NO: MLX-23-PC — REV: A


REVISION
APPD SYM DESCR DATE
A REL PROD 9-22-77
B ECN 0145 6-17-85
XBYT2-
XRES-
XACTV+
XREDY+
XREDF+
XREDF-
XIR-
XRRDY-
XNOW+
XNOW-
XQUIT-
XFIFR-
XERRF-
XSTRT+
XSTRT-
XACTV-
XERR+
XBYT2+
XIR+
XSI+
XMNOR+
XLNOR+
XCNOR+
XOR+
XSO+
XRSTR+
XRSTR-
XFDBT+
XFDB6+
XFDB5+
XFDB4+
XFDB3+
XFDB2+
XFDB1+
XFDB0+
XFIB7+
XFIB6+
XFIB5+
XFIB4+
XFIB3+
XFIB2+
XFIB1+
XFIB0+
DBR15+
DBR14+
DBR13+
DBR12+
DBR11+
DBR10+
DBR09+
DBR08+
DBR07+
DBR06+
DBR05+
DBR04+
DBR03+
DBR02+
DBR01+
DBR00+
DBB15+
DBB14+
DBB13+
DBB12+
DBB11+
DBB10+
DBB09+
DBB08+
DBB07+
DBB06+
DBB05+
DBB04+
DBB03+
DBB02+
DBB01+
DBB00+
XEOB+
XEOBC+
XEOBB+
XEOB2+
XEOBF+
XLAST+
XCNIR+
XLNIR+
XMNIR+
XIR+
XIR-
XRES+
XRES-
XRAC1-
DXQIT-
MXRES-
CLRXA-
XEOBN+
MRES+
MRES-
XINTO-
XRINT-
XINT+
XQINT-
XRQNT-
R5
100Ω
15V-
12V-
12v - ½ W
D1
U5
U15
U20
U21
U22
U23
U30
U31
U32
U33
U39
U40
U41
U48
U49
U50
U51
U52
U57
U58
U59
J1
J2
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN DRF
CHECKED
APPROVED
TITLE
FIFO's & DMA INTERFACE
SYSTEM NO. HSMIMP
DRAWING NO. MLX-24-PC
REV B

I/O Parity

PAR-Ø2 Logic Description

PAR-Ø5 Technical Reference

PAR-15 Standard Modification

PAR-2Ø Schematics

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8-30-74	
B	ECN 0118	12-17-74	
C	ECN 0218	7-21-76	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 1|16|76 (AMW)

APP'D FOR REL 1|16|76 (AMW)

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PAR LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PAR-02

SCALE	REV	SHEET
	C	1 OF 5

PAR

PAR LOGIC DESCRIPTION

The I/O Parity (PAR) card generates address-XOR-data parity for references to the I/O bus; operation is straightforward as described below. The following discussion assumes jumpering for recognition of I/O addresses only.

Parity Generation (PAR21)

The parity network is constantly calculating proper parity based on the current state of address lines 0 through 19, data lines 0 through 15 and the BYTE control line on the bus. When the address is FC000 or higher, this network drives the PBHI and PBLO bus lines. The nine-wide 74S280 parity tree is used in such a way that the slower 74180 can be substituted directly with the appropriate jumper configuration in the control circuitry. This is done by using the 74180 cascade input as the ninth data input. Since the value of address bit 0 for the high order byte is zero, the sense of the high order parity is inverted. Data parity also includes address bit 1. Low order data parity is XORed with the inverted value of bit 0 in byte mode to reflect the fact that byte data appears in the low order (bits 0-7) byte position and high order (bits 8-15) position -- data and parity are ignored. Where word data would have address bit 0 equal to one, data for only the low order byte will have this value in byte mode, so the inverted ADR00 is gated with BYTER (BYTE from the INFIBUS) to preserve consistency.

The two address components (bits 2 through 19) are XORed together and the result XORed with the high order data parity and the low order data parity modified as described above. The two resulting outputs, PBHID- and PBLOD-, input directly to the bus drivers for PBHI and PBLO. The parity networks are configured to produce even parity for the parity line, the data byte, address bits 1 through 19 and the explicit (in byte mode) or implied (in word mode) value of address bit 0.

PAR

Control (PAR20)

There are two different implementations of parity: 1) the data source always <u>generates</u> parity (write source generate-classical), 2) the data source always <u>checks</u> parity (write source check-feedback).

In the first case it is sufficient to always calculate parity and drive the I/O bus parity lines as appropriate to the observed data. In this case, no control function is needed, since the source bus coupler can use or not use the available parity signals as required. Parity is available at the bus coupler sometime after data, due to calculation propagation delays.

The second case, parity for read data, available at the bus coupler after calculation propagation delay, presents no particular problem. However, write data parity must be calculated before it can be passed to the source bus coupler for checking; this requires suspension of write to the I/O bus, using the HOLD line, to allow for the calculation delay. On reads from the I/O bus and reads or writes originating on the I/O bus, the control delay should be minimized to shorten cycle time as much as possible. The control circuitry used to achieve this is described below.

There are three possible causes for STRB to be asserted on the I/O bus: 1) read or write initiated to a different bus by a device on the I/O bus, 2) read from the I/O bus, 3) write to the I/O bus. In all cases, the assertion of MRES or the negation of STRB (STRB+) direct set HOLDD, a cross coupled Schottky flop for maximum speed.

For a reference initiated on the I/O bus to an address off the bus, address lines 14 through 19 on the bus will not all be true, so ADRIT is false, STRAD direct clears HOLDD. This negates HOLD on the bus, allowing the reference to proceed.

Prior to a read from the I/O bus, address lines 14 through 19 will be true on the bus, but the RITE line on the bus will be false. This will cause ADRIT to be false and, when STRB is asserted on the bus the state of STRBE, ADRIT, and HOLDD allows STRAD to direct clear HOLDD. This negates HOLD on the bus, allowing the I/O device to be referenced. After the data is presented, as signaled by DONE, good parity will be available on the bus when the parity network propagation time has elapsed.

Shortly before STRB is asserted on the bus from a write to the bus, the RITE line and address lines 14 through 19 on the bus will be asserted. ADRIT is then true when STRBR comes true. The assertion of STRAD is blocked by ADRIT and HOLDD remains set, causing the HOLD line on the bus to be asserted. When STRBD comes true a gate delay later, WRADS is asserted, firing DELAY

(45ns). The delays in this path allow for propagation through the parity networks. For the Schottky 74S280, two gate delays (SHDLY, CLHLZ) are sufficient, but for the 74180 the longer delay introduced by an additional 74123 (CLHLX-) is required. In the first case, CLHLZ is tied to CLHLD to direct clear HOLDD, shutting off HOLD on the bus. In the second case, the trailing edge of DELAY fires CLHLX which, tied to CLHLD, clears HOLDD. Since bus HOLD is now false, the addressed device accepts the data and returns DONE.

A separate 6-bit address recognizer enables the parity bits on the bus only in the presence of an I/O bus address. This allows combined memory on I/O buses.

Control jumpering and timing are summarized below.

Switches (PAR20)

Four switches drive any of the high order address lines directly for test purposes and for single bus machines.

Jumpers (PAR20)

For write source checking, the HOLD function is enabled by connecting jumper pins 1 and 16.

When using the non Schottky 74180 parity tree, the proper delay path is enabled by connecting jumper pins 2 and 3 and 14 and 15. Using the Schottky 74S280, the proper path is enabled by connecting pins 3 and 4 and 13 and 14.

Jumpering to recognize all addresses allows use of this card for test purposes. Normal jumpering for I/O addresses drives the parity BDR strobe on recognition of an I/O address (G4-5 to G4-12) and fires the write delay chain when an I/O write is recognized (G4-6 to G4-11). Test jumpering sends parity to the bus continuously and fires the write delay chain on all writes (G4-6 to G4-10).

The jumpering option to generate always, except on memory reads, sends parity to the bus on all accesses, except memory reads (G4-5 to G4-7), and fires the write delay chain on all writes (G4-6 to G4-10).

Table 1 - Parity Card Propagation Delays

	Standard	Schottky
1. WRITE (write source check only)		
control path delay typical	196.0 ns	141 ns
parity path delay maximum	166.5 ns	112 ns
safety margin typical minimum	29.5 ns	29 ns
This margin may be increased by increasing delay.		
2. READ		
parity path delay maximum	156.5 ns	102 ns
DONE driver-receiver pair delay minimum	25.0 ns	25 ns
required bus coupler delay minimum	131.5 ns	77 ns
3. Reference from the I/O bus (write source check only)		
Control path delay maximum	85 ns	85 ns

Times are based on inputs to drivers and outputs from receivers and assume one gate access time for the I/O slave.

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8-30-74	
B	ECN 0119	12-17-75	MPL

PAR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN BT / BT

CHECKER

ENGINEER 1/16/76 (AXM)

APP'D FOR REL 1/16/76 (AXM)

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PAR TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		PAR-05

SCALE	REV	SHEET
	B	1 OF 2

PAR - I/O BUS PARITY BBN

Status - address none

Switches - Set Bus Address Lines

19	18	17	16	X	X	X	X

Jumpers - Parity Tree Type (B2, B3, E2, F2)

FROM	G4-3	G4-14
TYPE	TO	TO
74180	G4-2	G4-15
74S280	G4-4	G4-13

Write Source Check (Feedback)

Connect G4-1 to G4-16

PAR

Address Recognition

From	G4-5	G4-6
	to	to
I/O only	G4-12	G4-11
ALL	--	G4-10
ALL EXCEPT MEMORY READ	G4-7	G4-10

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8-30-74	
B	ECN 0118	12-17-74	MFK
C	ECN 281	4-12-78	EC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER 1/16/76 (AXW)	
APP'D FOR, REL 1/16/76 (AXW)	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PAR STANDARD MODIFICATION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PAR-15

SCALE	REV	SHEET
	C	1 OF 2

PAR

Card Type PAR Modification Standard

Card Function: I/O Parity

Modification Description:

Configure card with Schottky parity trees, I/O address recognition, address switches off.

Implementation:

1 Turn off all switches at the left of the board.

2 Confirm that 74S280 is plugged in at locations B2, B3, E2, F2

Jumper with 30 ga wrapped wire as follows:

G4-3 to G4-4
G4-13 to G4-14

3 Jumper with 30 ga wrapped wire as follows:

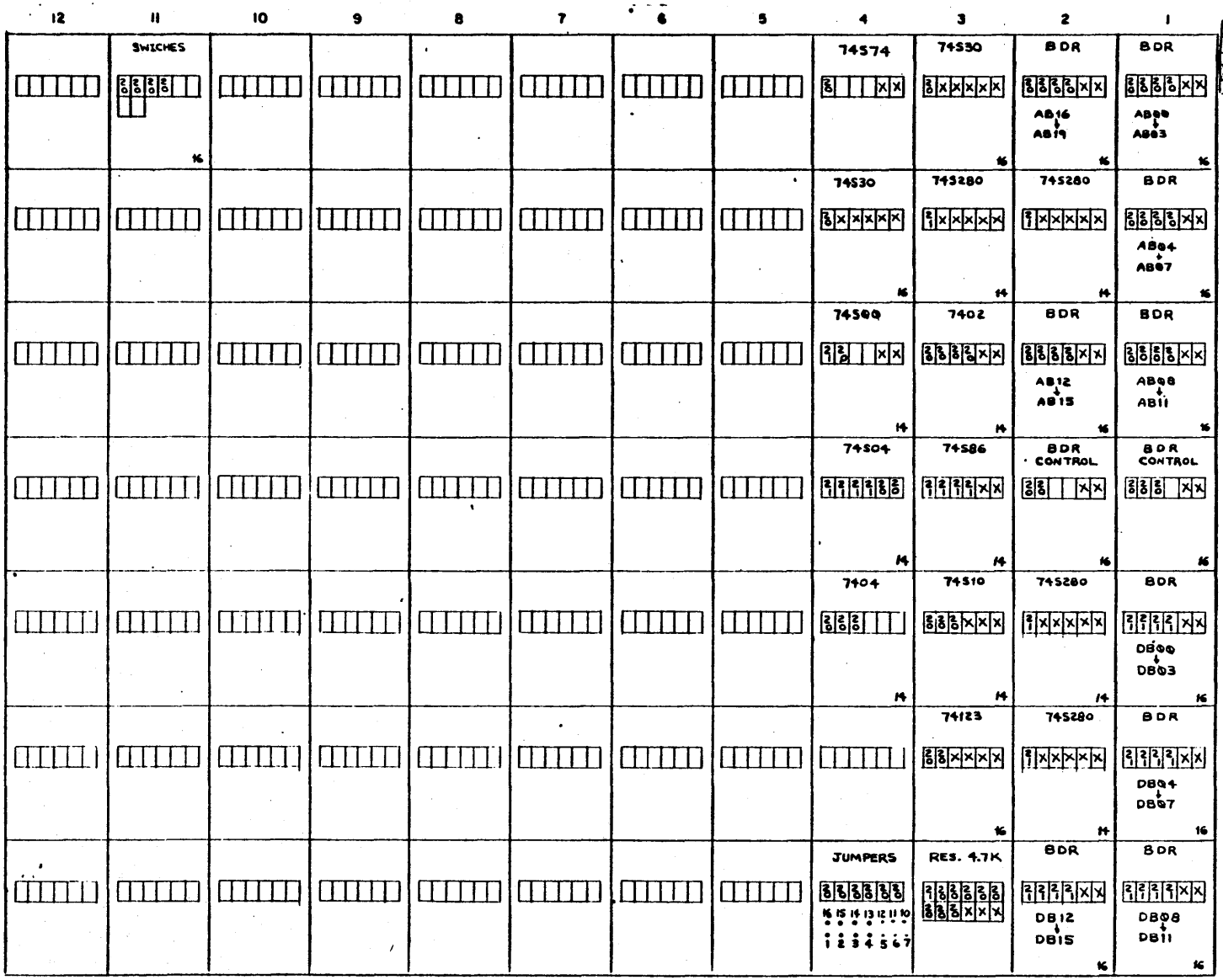
G4-5 to G4-12
G4-6 to G4-11

All jumpers should be installed on the pins at each pad having no other wire connected

Module designations are detailed below

Module	Row	Column (from top right)
B2	2	2
B3	2	3
E2	5	2
F2	6	2
G4	7	4

PAR-2Ø SCHEMATICS



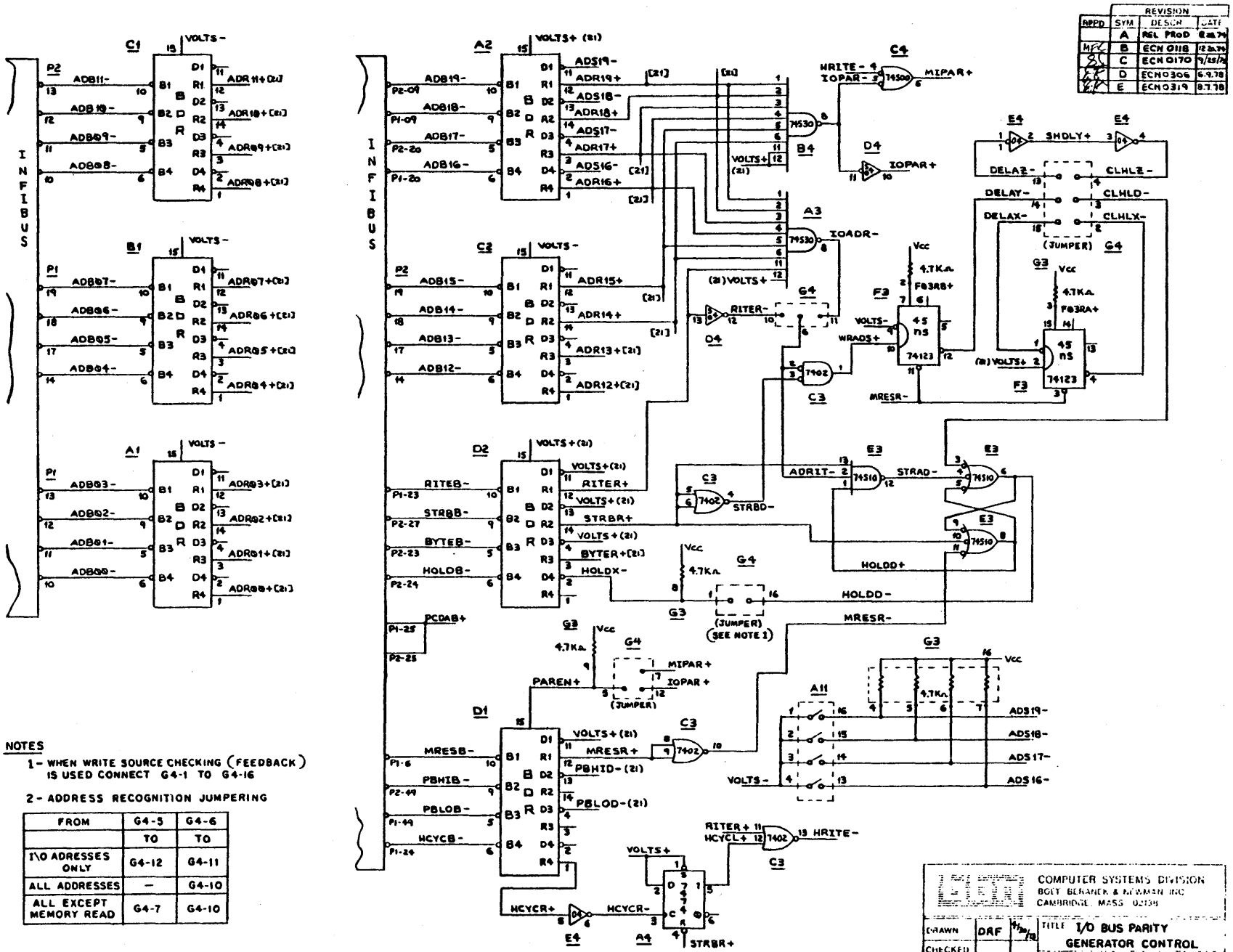
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	9.28.79
	B	ECN 0118	12.28.78
	C	ECN 0306	6.12.78
	D	ECN 0319	8.7.78

TOP VIEW

NOTES :

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	9/29/79	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED				
APPROVED		9/26/79	CUSTOMER/NO. HSMIMP	DWG NO. PAR-QQ-WW REV D

PAR



REVISION			
APPD	SYM	DESCN	DATE
	A	REL PROD	8 MAY 74
MC	B	ECN 0118	12 JUN 74
	C	ECN 0170	9/25/75
	D	ECN 0306	6.9.78
	E	ECN 0319	8.7.78

NOTES

1- WHEN WRITE SOURCE CHECKING (FEEDBACK) IS USED CONNECT G4-1 TO G4-16

2- ADDRESS RECOGNITION JUMPERING

FROM	G4-5	G4-6
	TO	TO
I\O ADRESSES ONLY	G4-12	G4-11
ALL ADDRESSES	—	G4-10
ALL EXCEPT MEMORY READ	G4-7	G4-10

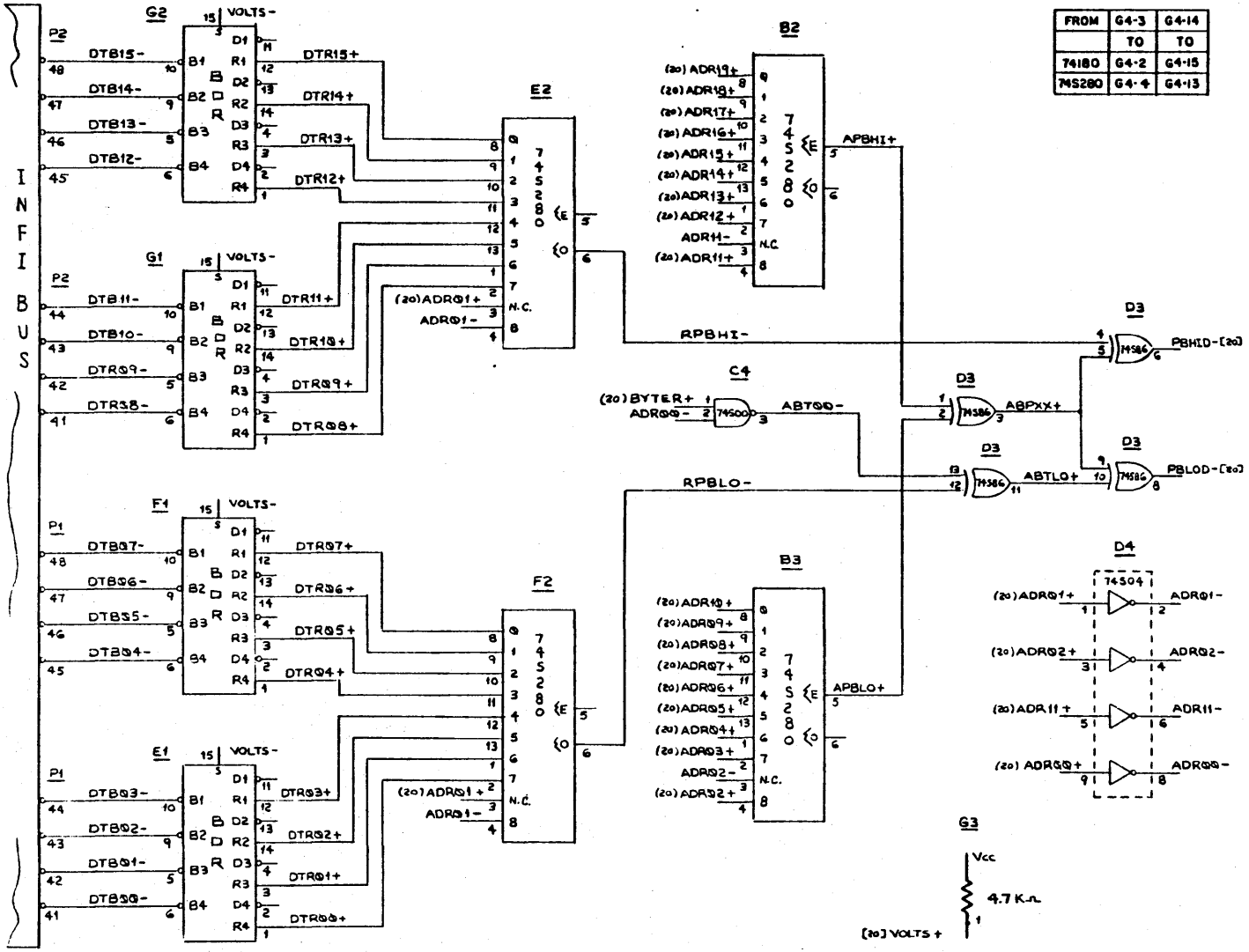
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	11/20/78	TITLE I/O BUS PARITY GENERATOR CONTROL
CHECKED			CUSTOMER NO. DWG NO. REV
APPROVED	TJT	11/20/78	HSMIMP PAR-20-WW E

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	8 28 79

NOTE 1: 74S280 IS PIN COMPATIBLE WITH 74180
JUMPER AS FOLLOWS

FROM	G4-3	G4-14
	TO	TO
74180	G4-2	G4-15
74S280	G4-4	G4-13



COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/30/79	TITLE I/O BUS PARITY GENERATOR DATA
CHECKED			CUSTOMER NO.
APPROVED	MJT	8/28/79	HSMIMP PAR-21-WW REV A

PAR

Control Panel Bus Interface

PBI-Ø2 Logic Description

PBI-Ø5 Technical Reference

PBI-15 Standard Modification

PBI-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/1/77	

PBI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PBI LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PBI - Ø2

SCALE	REV	SHEET	OF
	A		

SUE 2220 PROGRAM/MAINTENANCE CONTROL PANEL

MAINTENANCE BULLETIN M2220

PBI

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PBI

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LIST OF ILLUSTRATIONS

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PBI

PREFACE

This Maintenance Bulletin contains a detailed description of the SUE 2220 Program Maintenance Control Panel. Information in this bulletin is written primarily for system user and maintenance personnel with backgrounds in digital systems. Read Reference Bulletin R2220 for a general description of this module and SUE General System Bulletins for background information.

SUE 2220 PROGRAM/MAINTENANCE CONTROL PANEL

MAINTENANCE BULLETIN M2220

INTRODUCTION

SUE 2220 Program/Maintenance Control Panel provides a means of manual access to all processor internal registers for program debugging, maintenance and troubleshooting SUE hardware. SUE 2220 can be used with or without one of the optional SUE Power Control Panels, 2201 or 2202. This bulletin contains a detailed explanation of Program/Maintenance Control Panel theory and use based on four illustration types located at the end of this document. Figure 1 is a block diagram keyed to three logic diagram sets: Switch Panel Board (SWB), Panel Bus Interface (PBI), and Control Panel Board (PCB). Figure 2 is a flow chart, figure 3 the panel states diagram, and figure 4 the switch-debounce timing diagram.

PROGRAM/MAINTENANCE PANEL BLOCK DIAGRAM

Figure 1, the block diagram, shows the INFIBUS interface on the left, the Switch Panel right. At top left in each block are noted applicable pages of the PBI/PCB logic diagrams. Connecting paths between and among blocks carry respective four-letter signal mnemonics.

PBI

Mnemonics starting with F signify flip-flop signals, O one-shot signals, and S touch-switch signals; mnemonics ending in L are signals relating to light emitting diode (LED) drivers — the enable signal (ENBL) is the one exception.

FLOW CHART

Figure 2, the flow chart (two sheets), is a detailed plan of all important functions performed by the logic. (Slave mode operation is not included, except for flagged statement number 6.) Because many blocks in the block diagram

encompass large amounts of logic, the flow chart is adapted more for use with the logic diagrams. The block diagram serves as the logic diagram index.

LOGIC DIAGRAMS

PBI and PCB cards contain all active logic; SWB logic comprises LEDs and switch closures. Signal paths on the PBI and PCB logics carry many mnemonic definitions, and timing sketches are shown where pertinent.

PANEL STATES WITH SYNCHRONOUS MICROOPERATIONS DIAGRAM

Panel control states and all microoperations performed in synchronism are shown in figure 3. State transitions on the trailing edge (TE) of clock phase 0 (CF0A) and delays between individual states are shown. State-transition gatings are symbolic; for actual transition logic see sheet 3 of the logic diagram.

DATA BUS DRIVERS/RECEIVERS

Data Bus Driver/Receiver signals DB15-DB00 are connected between the INFIBUS and the PCB logic shown on sheet 5. DB15-DB00 signals are strobed out by DOUT (gate data to INFIBUS); Inputs are driven by D15N-D00N signals from the Data Input selection logic. D15A-D00A signals are connected to the parallel inputs of the Data and Address Registers (sheets 6 and 7).

DATA INPUT SELECTION

Data input selection logic (PCB sheet 5) is used to gate the following items to the data bus driver inputs one at a time:

a. Address register outputs A15S-A00S
b. Data register outputs D15S-D00S
c. Run command 0002_{16}
d. Halt command 0001_{16}
e. Step command 0003_{16}
f. Control panel address
g. 0000_{16}.

ADDRESS SELECTION

Address register outputs are gated to the data bus driver inputs for the condition $\overline{DRDB}.\overline{RNDB}.\overline{VADB}.\overline{HTDB}$, because for this condition the output of HRVB (Force Zero Output From Data Multiplexers) is low. DxxM = AxxS because of $\overline{DRDB}$.

DATA SELECTION

Data Register outputs are gated to the data bus driver inputs for the condition $DRDB.\overline{RNDB}.\overline{VADB}.\overline{HTDB}$, because for this condition the output of HRVB is low. When DRDB is active DxxM = DxxS.

RUN COMMAND SELECTION

0002_{16} is forced to the data bus driver inputs for the condition $RNDB.\overline{VADB}$. When RNDB is active, the output of D0lN is true and DxxM = 0.

HALT COMMAND SELECTION

0001_{16} is forced to the data bus driver inputs for the condition $HTDB,\overline{VADB}$. Whenever HTDB is active, the output of D00N is true and DxxM = 0.

STEP COMMAND SELECTION

0003_{16} is forced to the data bus driver inputs for the condition $RNDB.HTDB.\overline{VADB}$. Due to RNDB.HTDB, D0lN = D00N = 1 and DxxM = 0.

PB1

CONTROL PANEL ADDRESS

$FF8Y_{16}$ is forced to the inputs of the data bus drivers for the condition VADB; Y can be 0_{16}, 4_{16}, 8_{16}, or C_{16} -- depending on the jumpering tabulated on sheet 5 of the PCB logic (PB0l and PB00). Note that an active VADB causes DxxM = 0.

ZERO ADDRESS

All the inputs of the data bus drivers are forced to zero for the condition FMRA. $\overline{RNDB}.\ \overline{HDTB}.\overline{VADB}$.

ADDRESS BUS DRIVERS/RECEIVERS

Address bus driver/receiver signals AB15-AB00 are connected between the INFIBUS and the PCB logic shown on page 8. AB15-AB00 signals are strobed by the AOUT signal. Driver inputs are driven by A15M-A00M, A04-A01N, and A00M that signals all come from the Address Input Selection logic. Receiver outputs A15A-A00A drive the logic in the Slave Recognition and Address Comparison blocks.

ADDRESS INPUT SELECTION

Address input selection logic (PCB sheet 8) is used to gate the following items to the inputs of the address bus drivers, one at a time:

a. Address register outputs A15S-A00S

b. Selected processor register address

c. Selected processor control register address.

ADDRESS SELECTION

Address register outputs A15S-A00S are gated to the inputs of the address bus drivers for the condition ARAB.CRAB. Note that multiplexers A15M through A00M are always enabled because the S1 inputs are terminated at 0 volts.

PROCESSOR REGISTER ADDRESS SELECTION

The fully encoded processor register address is driven from the multiplexer outputs A15N through A05N, A04N through A01N, and A00N to the inputs of the address bus drivers for the condition $\overline{\text{ARAB}}.\overline{\text{CRAB}}$. For this condition A15N through A08N are all ONEs (low), because the B_3 through B_0 inputs of U46 and U56 are all grounded at 0 volts. Bits A07N and A00N are zero-valued (high) because the appropriate B_3 input of U66 and B_0 input of U76 are pulled up to a high level. Therefore, the processor register address is

/1, 1, 1, 1, /1, 1, 1, 1, /0, CPU1, CPU0, RA04, /RA03, RA02, RA01, 0/.

The processor number is determined by the CPU1 and CPU0 bits per Table 1 that normally are controlled by the SUE 2202 Power Distribution Unit inputs to

the SWB card. However, jumpers can be used on the SWB card to control the CPUl and CPU0 signals.

Table 1. Processor Number Selection

CPU1-N	CPU0-N	Either Jumper on SWB . . .		Or set selector of SUE 2202 to position (if available)	Processor Number
		E3 to E4	E5 to E6		
High	High	Missing	Missing	1	1 (CPU) Standard Production
High	Low	Missing	Installed	2	2
Low	High	Installed	Missing	3	3
Low	Low	Installed	Installed	4	4

RA04 through RA0l are the outputs of the Register Selection Storage logic (U62 on Sheet 2 of the PCB logic diagram).

PROCESSOR CONTROL REGISTER SELECTION

The fully encoded processor control register address is driven from the multiplexer outputs A15N through A05N, A04N through A01N, A00N to the inputs of the address bus drivers/receivers for the condition $\overline{\text{ARAB}}$.CRAB. The full address is

1,1,1,1,/1,1,1,/0,CPUl,CPU0,1/1,1,1,0/.

PBI

SWITCH PANEL

The switch panel block represents the SWB logic diagram. The SWB card contains all the touch switches. Each touch switch has an associated LED indicator. The SWB card is connected to the free-edge connectors of the PCB and PBI cards by three flat cables. These cables convey the switch closures from the SWB card to the PCB and PBI cards and connect the LED drivers to their respective LEDs on the SWB. Three control signals also are fed back to SWB: ENBL, ENDA, ENAD; ±5 power also is supplied through these cables.

PANEL ENABLE

The SWB card must be enabled either by a jumper from E1 to E2 or by the power distribution unit. Signal ENBL is true when the control panel is enabled.

PROCESSOR SELECTION

The processor usually is selected by a selection switch located on the power distribution unit; in its absence, processor 1 (CPU) is selected automatically unless jumpers are field-installed on the SWB card per Table 1.

TOUCH SWITCH CLOSURES

Refer to the SWB logic diagram. Switch-closure signals are identified by four letter mnemonics the same as any logic signal. For example, RS15 (sheet 2 of the SWB logic) is the signal generated by closing **register** selection switch 15. All touch-switch closures, except the **register** selection switch closures, produce a 0 volt signal only when enabled. The **register** selection switch closures unconditionally produce a +5 volt signal.

Note that the **address** and **data** switch closures are shorted to a single connector pin per bit position (SWB logic sheets 3 and 4). By enabling either the **address** switches with ENAD or the **data** switches by ENDA, one or the other switch can be sensed properly. Except for these two switch rows and the **register** selection switches, all other touch switches are enabled by ENBL.

INTERRUPT INHIBIT SWITCHES

The power fail/recovery interrupt lines (PFIN-N, PRAL-N, PRIN-N) and the line frequency interrupt line (LFIN-N) on the INFIBUS, can be controlled by switches S70, S71, and S72 (sheet 6, SWB logic diagram). The switches can be replaced by jumpers. Setting a switch or placing a jumper causes the respective interrupt line to be high or low as indicated in Table 2. From the J3 cable connection, the switch or jumper closures are passed through the PBI circuit card (sheet 10, PBI logic diagram) to the INFIBUS where they are monitored by the Bus Control Unit (BCU). On systems containing multiple panels, the switches or jumpers must be configured identically on all of the panels, or removed from all but one of the panels.

Table 2. Switch or Jumper-Controlled INFIBUS Lines

Interrupt	Switch or Jumper Position	INFIBUS LINES			
		LFIN	PRAL	PRIN	PFIN
PWR FAIL	OFF	-	-	-	Low
PWR FAIL	ON	-	-	-	High
PWR RCVRY	OFF	-	High	Low	-
PWR RCVRY	IN (Interrupt)	-	High	High	-
PWR RCVRY	AL (Auto Load)	-	Low	High	-
LINE FREQ	OFF	Low	-	-	-
LINE FREQ	ON	High	-	-	-

OPTIONAL SWITCH/JUMPER CONTROLS

Four optional switches or jumpers, intended for SUE servicing aids, are shown on sheet 6 of the SWB logic diagram. The switches can be installed in the field, or a jumper can be substituted for these closures. If switches are used, they are type T8001 (Singer Controls). Use of these closures is shown in the Figure 2 flowchart and figure 3.

The BYTE closure allows reading or writing at byte addresses; address increments in this case are by one instead of two.

The WRITE INCR closure enables automatic address incrementing with the **write** touch switch.

PBI

The remaining two closures, CONT R⊕W and INCR CONT R⊕W, allow continuous reading or writing from the panel, either at the specified address or the incremented address by a single push of the **read** or **write** switch. During this mode, the panel does not handle any other functions. The CONT R⊕W closure must first be placed to the OFF position to get the panel out of this operational mode. Both figure 2 and 3 show how these closures influence the logic. For example, note that to write the same information at every memory address, all the following closures must have been ON prior to touching the **write** (at address) switch:

INCR CONT R⊕W

CONT. R⊕W

WRITE INCR

SWITCH BOUNCE LOCKOUT TIMING AND SHIFT CONTROL

Logic on PCB sheets 3 and 4 has the following diverse functions:

a. Generation of a single debounced sampling pulse (OACS) for a single switch closure

b. Identification of any **data** switch closure versus any **address** switch closure

c. Generation of sixteen shift pulses for serially loading either the address or the data register with the latest information as a function of the **address** or **data** switch closure(s)

d. Serial incrementing the address register by one or two.

DEBOUNCED SAMPLING PULSE

At the top of PCB logic sheet 4 are shown oneshots and a flip-flop. The sequence described here is summarized in the figure 4 timing diagram. Initially all oneshots are in quiescent states and FLS is being cleared continually by OLTS, which in turn insures that OSB and OAC are not being cleared. The last leading edge of TOSB-N retriggers Debounce Oneshot OSB to time out in about 1.9 milliseconds. Thus, by the time OSB has timed out, no leading switch bounce can exit. Lockout Timing oneshot OLT is retriggered every 640 nanoseconds for an additional 24 milliseconds (approximate) during the relatively long time (tenths of a second or more) that TOSB remains low. From the time OLTS-P switched high, FLS is no longer being cleared. The trailing edge of OSBR-N triggers OACS-P on for approximately 3.4 microseconds. The trailing edge of OACS sets FLS, which means that FLSR-N keeps both OSB and OAC reset. Approximately 24 milliseconds after TOSB goes inactive (high), OLTS goes low to clear FLS. At that time, FLSR is high and the oneshots are ready for the next switch closure.

ADDRESS/DATA SWITCH IDENTIFICATION

Refer to the PCB logic at the top of sheet 3. When OAD and ODA are quiescent, and if ENBL is low, both 10AD and 10DA are ready to sink current through inductors L2 and L1 respectively, in the event of a switch closure on the **address** or **data** switch rows. Assume that one of the **address** switches, bit 15, is touched. Current begins to flow from R8 (PCB logic sheet 2) through the closed switch and cable conductors into J1-13 (ENDA). The voltage at J1-13 rises instantly to +5 volts and then decays to 0 volts in less than one microsecond because of inductor L2. This differentiated voltage spike is fed through TOAD and through a second differentiating network to trigger OAD with its leading edge. (This double differentiation is necessary to prevent oscillations between OAD and ODA after OAD or ODA is initially triggered because of the T123s characteristics. As soon as OAD is triggered on, the switch closure is declared to be an **address** switch closure for a minimum period of 3.55 millisecond. OADS meanwhile forces ODA to remain cleared and forces ENDA high to prevent data switch closure sensing during the

PBI

duration of OADS-P. An initial **data** switch closure works similarly except that ODA is triggered on and ENAD is forced high for the duration of ODAS-P. FBAS (Block Action F-F) clears both OAD and ODA while set.

ADDRESS/DATA REGISTER CLOCKS

Refer to the middle of PCB logic sheet 4. Assuming that **address** bit switch 15 was just closed, OADS is high for a minimum of 3.55 milliseconds, and the output of SFSA goes low for the duration of OACS (minimum of 2.41 microseconds). The very next negative-going (trailing) edge of TFSD (Trigger Shift F-Fs) sets FSA. With FSAS high, ASCC advances the SCxx (Shift Counter) with each trailing edge of TFSD every 640 nanoseconds. After the sixteenth ASCA-N (Address Register Clock) is gated through, FSA is reset to prevent anymore ASCAs from being generated. The FSAA-N (Synchronized Shift Address Register) and ASCA-N signals are used to shift the contents of the address register around. Had the detected switch closure been a **data** switch closure, the same SCxx shift counter would have generated 16 DSCA-N pulses as FSD would have been set. The DSCA-N pulses, along with the FSDA-N signal, would have been used to shift the contents of the data register around sixteen times.

ADDRESS REGISTER INCREMENTATION

Refer to the bottom of sheet 4 PCB logic and figure 3. FNC is the flip-flop that may have been set with 1FNC-N during STATE A. Also, at the leading edge of STATE A, FSAT-N sets FSH. Sixteen shift pulses (ASCA-N) are generated with FSAA after the Synchronized Shift Address flip-flop sets. Because the exclusive-or gate feeding the address register represents a half adder, incrementation takes place. If the BYSW (Byte Switch) signal is low, FNCS is gated through with the first shift count (zero) and thereafter until AR00-N goes false. If the BYSW-N signal is high, incrementation is skipped during the first shift count (zero); however, incrementation can take place during the fifteen following shift counts. Shifting the carry-in over by one is the same as adding two instead of one.

DATA ADDRESS MULTIPLEXER

Refer to PCB logic sheets 2 and 4. SMUX is the sequentially-scanned output of BS00 during shift count 0, BS01 during shift count 1, until finally it is BS15 during shift count 15. (During no shifting, SMUX = BS00). BSxx is either from an address touch switch closure or from a data touch switch closure due to action of the ADDRESS/DATA SWITCH IDENTIFICATION logic. Based upon whether or not OADS or ODAS is active, either INAX = SMUX or DMUX=SMUX respectively.

DATA REGISTER

Sheet 6 of the PCB logic shows the sixteen-bit data register, the outputs of which drive the data LEDs on the SWB and other blocks as shown in figure 1. The SCLD-N signal comes directly from the **clear** (data) touch switch. Loading the register takes place either in parallel from the data bus receivers or serially from DMUX⊕D00S when FSDA-N is true. Timing of the required control signals for either kind of loading is shown at the bottom of sheet 6. Capacitors on the outputs of D13L, D12L, D09L, and D08L prevent excessive noise pickup on the ENDA and ENAD lines (see top of sheet 3 PCB logic).

ADDRESS REGISTER

The sixteen-bit address register (PCB logic sheet 7) functions similarly to the data register. For timing and control signals refer to the bottom of PCB sheet 6. Signal 1F1R sets the 1st Read and 1st Write flip-flops anytime the address is altered from the panel.

PBI

PROCESSOR REGISTER SELECTION WITH LED DRIVERS

Processor register selection logic is shown at the top of PCB diagram sheet 2. RS15-RS00 switch closures are encoded into a straight (four-bit weighted) binary code by U52. This four-bit code (SRA4-SRA1) is loaded into the Processor Register Selection Storage for the condition ENBL. OACS. STROBE. $\overline{\text{ROLLOVER}}$. The outputs of the Processor Register Selection Storage (RA04-RA01) are decoded into sixteen separate LED drivers by U72.

SWITCH FLIP-FLOPS AND SINGLE ACTION DISCRIMINATOR

Seven action switch closures require a DDC bus access: **run**, **halt**, **step**, **read** (at address), **write** (at address), **read** (register), and **write** register. (Touching any one causes its LED to be lit directly on the SWB card assy). The Single Action Discriminator logic (PBI diagram sheet 2) prevents setting FBA, the Block Action F-F, if more than one action touch switch is closed at the trailing edge of OACS. However, for a single action closure, FBA is set and is not cleared till after the action has been carried out via the INFIBUS.

The leading edge of OSTS (Start Oneshot) loads the output of the action switch inverters into the switch flip-flops shown at the top of PBI logic sheet 3. For example, READ is thus loaded into FRD.

The AUTO LOAD gate is shown on PBI logic sheet 4. On the same sheet appear the INHIBIT INTERRUPT (FIT) and ADDRESS HALT (FAH) flip-flops, both of which have toggle action activated by the trailing edge of OACS (debounced switch sampling pulse), both with respective LED drivers.

The ATTENTION F-F (FTT) also is shown on PBI logic sheet 4. FTT does its own debouncing being set by the first leading edge/bounce of SATN (attn switch) and then getting reset only on the trailing edge of OLTS (Switch Lockout Oneshot). The trailing edge of FTTR-N sets the LEVEL 1 SERVICE NEED F-F (FN1) on PBI logic sheet 9.

CLOCK GENERATION, STATE GENERATION, AND CONTROL FLIP-FLOPS

Grouped together within this block (figure 1) are three different logic areas taken from PBI logic sheets 2, 3, 4, 5, and 9, and PCB logic sheet 7.

CLOCK GENERATION

At the bottom of PBI logic diagram sheet 5 the 25 MHz CLKA is shown driving a four-bit binary counter (U55). Clocks CLKI and CLQD are obtained from the most significant stage of the counter. FPH is the Phase Flip-Flop that controls the generation of CF0A-P (Clock Phase 0) and CF1A (Clock Phase 1). The timing diagram next to gates CF0A and CF1A shows all inter-relationships.

The phased clocks are exclusively for generating states and micro-operations. The other two clocks are for sampling signals into oneshots and for driving the Switch Bounce Lockout Timing and Shift Control logic on the PCB card.

STATE GENERATION LOGIC

Refer to the lower half of PBI logic sheet 3, where, for any action U34 is shown generating FSA (STATE A), FSB(STATEB), FSC(STATE C), and occasionally FSD (STATE D). State transitions in figure 3 afford a concise, yet detailed explanation of what this logic performs. The timing diagram at the lower right-hand corner of PBI sheet 3 is a helpful reference.

MISCELLANEOUS CONTROL FLIP-FLOPS

Refer to figure 2 and 3, during the following discussion.

The Block Action F-F (FBA shown on PBI logic sheet 2) is set by a single action at the trailing edge of OACS, the debounced switch sampling pulse, and is not reset until the last DONE or QUIT is received for a specific action. (For an optional continuous read or continuous write, it is not reset until the CONT R⊕W toggle switch is placed to OFF). The leading edge of FBAS triggers the Start Oneshot (OST) that times out in about 3.4 microseconds.

The START F-F, FST, (shown on PBI logic sheet 3) is set by the trailing edge of the Start Oneshot (OSTS) output, and causes STATE A to be generated next.

PBI

The SHIFTING DONE F-F, FDS, (PBI logic sheet 3) is set by the trailing edge of FSHR-N. This implies the address register has just been shifted around for possible incrementation and causes STATE B to be generated next.

The WAIT 2 F-F, FW2, (PBI logic sheet 3) is set during STATE C, only for a step so that setting STATE C can be delayed until a DONE or QUIT has been received.

The WAIT 2 F-F (FW2 , PBI logic sheet 3) is set during STATE C only for step switch closure so that STATE D can be generated after QUIT or DONE is

received. The Single Step F-F, FSP, (PBI logic sheet 5) hold the condition that the Run and Halt F-Fs had been set prior to 0A1G, which set the read flip-flop and cleared all other action flip-flops.

The Address Match F-F, FAM, (PBI logic sheet 5) is set when the content of the address register equals the address on the INFIBUS while the control panel is not accessing the INFIBUS, and only if the Address Halt flip-flop is set.

The (Synchronized) Address Comparison F-F, FCP, (PBI logic sheet 5) synchornizes the recognition time of an address match condition.

The Service Address Comparison F-F, FAC, (PBI logic sheet 5) sets only when States B and C issue the halt Command to the addressed processor because of an existing synchronized address comparison.

The Panel Busy (with state transitions) F-F (also PBI logic sheet 5) insures that State B always can be reset after being on for 320 nanoseconds.

The DDC DONE F-F and DDC ABORT F-F (PBI logic sheet 5) holds these conditions for subsequent logical decisions because the bus access logic does not.

The functions of Master Read F-F (FMR), the Level 1 Service Need F-F (FN1), the DDC Service Need F-F (FND) and the Last Service Request on DDC Level F-F (FLD) (PBI logic sheet 9) are self-explanatory by titles.

The 1st Read and 1st Write F-Fs (bottom of PBI logic sheet 2) cause the address register to increment before use on the INFIBUS for a READ (optionally for a WRITE) operation.

The Arm Auto Load Flip-Flop (top of PBI logic sheet 4) enables the issuing ATLD signal after being set by master reset, causing the load light on the panel to be lit whenever set or armed.

MICRO-OPERATIONS .

Those micro-operations synchronous to the control states, are shown on sheets 6 and 9 of the PBI logic diagram. They are described in figure 3.

Micro-operations that are partially, or totally, dependent on: Bus Access Logic; INFIBUS signals such as DONE or QUIT; or the Slave Address

Recognition Logic are grouped together on sheet 7 of the PBI logic diagrams. The function of each is described next to its respective signal line. These micro-operations are also implied in the flowchart of Figure 2.

SYSTEM STATUS LOGIC

System Status Logic monitors the processor Service Request Line, SRLC, and the processor Run Line, RUNN, directly on the INFIBUS and displays the condition on the **run**, **idle**, or **halt** LEDS. The logic controls the signals to the **done** and **busy** LEDS.

HALT LED

Refer to sheet 4 of the PBI logic. The **halt** LED is lit approximately 0.12 seconds after the trailing edge of RUNN. This is done by the Run Oneshot (ORN) which is retriggered every 160 nanoseconds, as long as RUNN is true. (The worst-case variations of trailing edge or ORNR-N are indicated). Thus, ORN discriminates against conditions where short run periods are interspersed with short halt periods in a SUE system, and causes ORNL-P to be true and the **halt** LED to be turned off. That is, once the **halt** LED is turned on, the SUE system is known to have been halted and is no longer running.

RUN LED

Refer to sheet 4 of the PBI logic. The **run** LED remains turned on, as long as there are SRLC signals on the INFIBUS. Note that the output of gate SRCN can rise to only 1.5v (approximate) in 11 microseconds, as indicated on the logic. This ensures that FITL has a steady low level as long as at least two SRLC pulses occur within about 10 microseconds.

IDLE LED

Refer to sheet 4 of the PBI logic. The **idle** LED is driven by the IDLL gate and turned on for the condition RUNN.$\overline{\text{SRLC}}$. For this instance the output of gate SRCO goes low only after the SRCN output has risen above +1.5v.

DONE LED

On sheet 4 of the PBI logic, is shown the Bus Access Done F-F (FAD) which drives the **done** LED with the BADL driver. This flip-flop is controlled only for DDC accesses.

BUSY LED

Refer to sheet 3 of the PCB logic diagram. The **busy** LED remains lit as long as OSD is triggered by any strobe at least once every .088 seconds.

SLAVE ADDRESS RECOGNITION LOGIC

Slave Address Recognition logic is shown at the top of PCB logic sheet 9, and the output signal is called SARO-N. The input to gate SARO goes high during STRB. HCYC when signals on the address bus become FF8x, (where x_{16} ⇒ PB01, PB00, 0, 0). Note that the rise time to +1.5v of the tied outputs of U69, U49, and U59 has been slowed down by C32 to prevent false slave address recognition. On PBI logic sheet 9, the Slave To Be Read F-F (FSRS) is set by the condition SARP.$\overline{\text{RITE}}$, and is reset either at the trailing edge of STRC or by the leading edge of FDNA-N delayed 50 nsec. Oneshot ORG (Load Reg Pulse Read Reg Delay) is triggered either by the leading edge of FSRR-N or by the condition SARP.RITE. Using this oneshot assures that the data has been loaded safely into the address register by ASCB-N, or into the data register by DSCB-N before DOND-N Internal Done is generated. The oneshot also allows time for the proper register address to ripple through all cascaded logic elements for a read register operation. Note that loading the address or data registers is inhibited by OLTS-P (Switch Lockout Timing) even though DONE is returned to the bus controller.

ADDRESS COMPARISON LOGIC

The Address Comparison Logic is shown on the bottom of PCB logic sheet 9. Output EQA4-P is true when the address register contents equal the address bus receiver outputs during STRB.

BUS ACCESS LOGIC

The bus access Logic is shown on PBI logic sheet 8. This logic is similar to the DBAL integrated circuit logic and is not explained in detail here. Refer to SPECIAL COMPONENTS in General System Bulletin G4 for a description of this logic. The top-half of the bus access logic is used both for DDT level bus access (**run**, **halt**), or for Level 1 bus access (**attn**), but never at the same time.

CONTROL BUS DRIVERS/RECEIVERS

The Control Bus Drivers/Receivers interface the following signals between the INFIBUS and the PBI circuit card on PBI logic sheet 10: AB01, SRLD, SRL1, SACK, STRB, DONE, RITE, BYTE, AB16, AB17, ATLD, and MRES.
On PCB logic sheet 3, the Control Bus Drivers/Receivers interface the following signals: STRB, HCYC, and MRES.

MASTER STROBE LOGIC

The Master Strobe Logic is shown on PBI logic sheet 10, and consists of gates STRE, STRF, and a 50-nanosecond delay line. STRF is issued to the Control Bus Drivers/Receivers Block at least 50 nanoseconds after the leading edge of FOLR-N.

SERVICE HINTS

Signal SYNC-N has been brought out to TP1 (Test Point 1) of the PBI circuit card, and is issued whenever the Address Bus = Address Register during the strobe.

PBI

Also, an extra-long jumper cable to go between J4 of the PBI card and J4 of the PCB card is useful so that one card can be extended past the other during servicing. The part number is CA-D24P05-261-AA-024 manufactured by:

Circuit Assembly Corp.
3025 So. Kilson Drive
Santa Ana, California 92707
(714) 540-5490

Both the PBI and PCB cards can be extended at the same time with the extra-long jumper cable by using two SUE extender cards in tandem for one card, and a single extender for the other.

DRAWINGS AND PARTS LISTS

This ia a list of the drawings and parts lists included in this bulletin.

Title	Mnemonic	Drawing Number	Sheets
Control Panel Circuit Card	PCB	2001002177-1	1
Control Panel Logic Diagram	PCB	LD2001002177-1	9
Switch Panel Circuit Card	SWB	2001002178-1	1
Switch Panel Logic Diagram	SWB	LD2001002178-1	6
Panel Bus Interface Circuit Card	PBI	2001002165-1	1
Panel Bus Interface Logic Diagram	PBI	LD2001002165-1	10
Control Panel Parts List	PCB	PL2001002177-1	2,3,4
Switch Panel Parts List	SWB	PL2001002178-1	2,5
Panel Bus Interface Parts List	PBI	PL2001002165-1	2,3,4

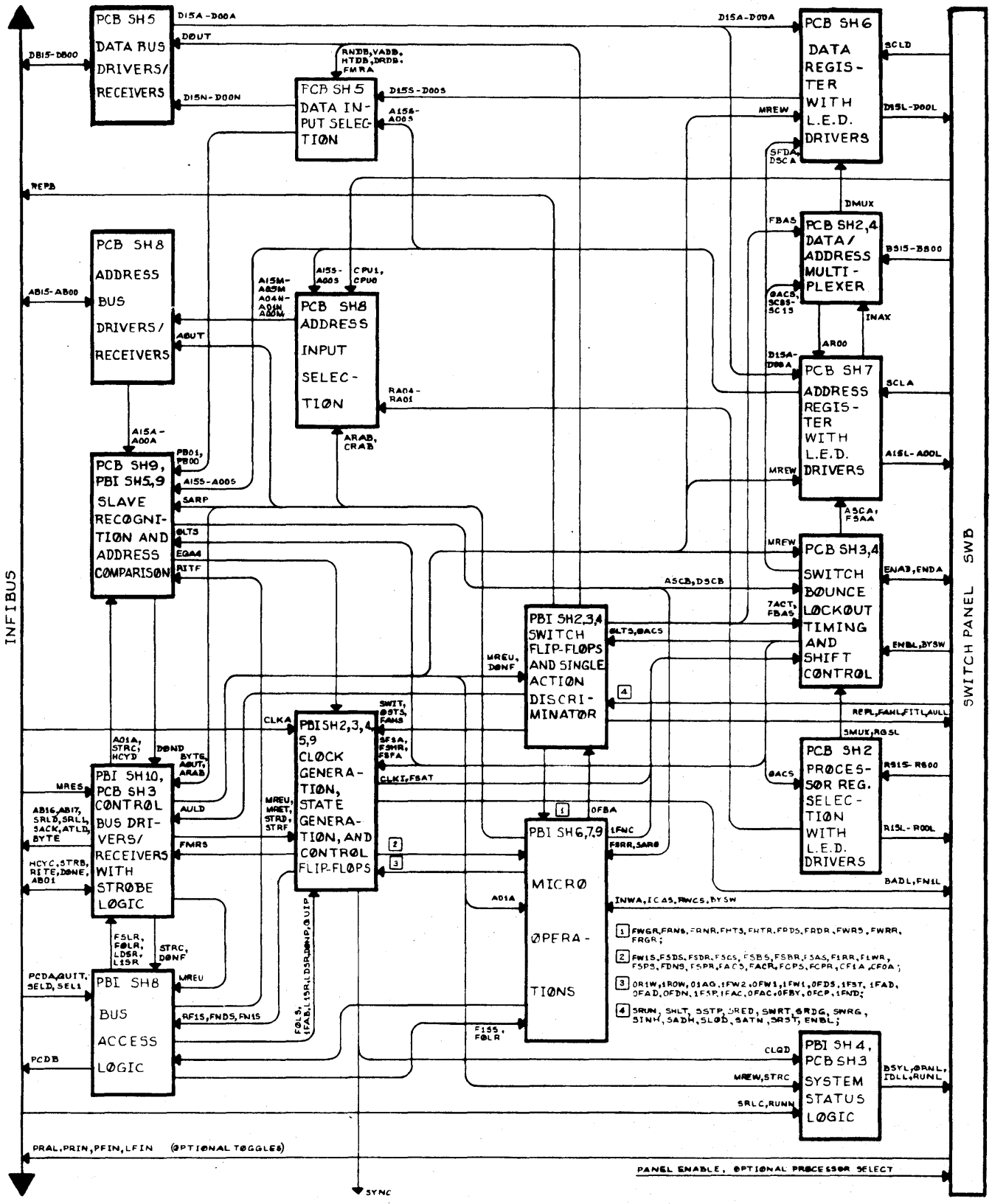
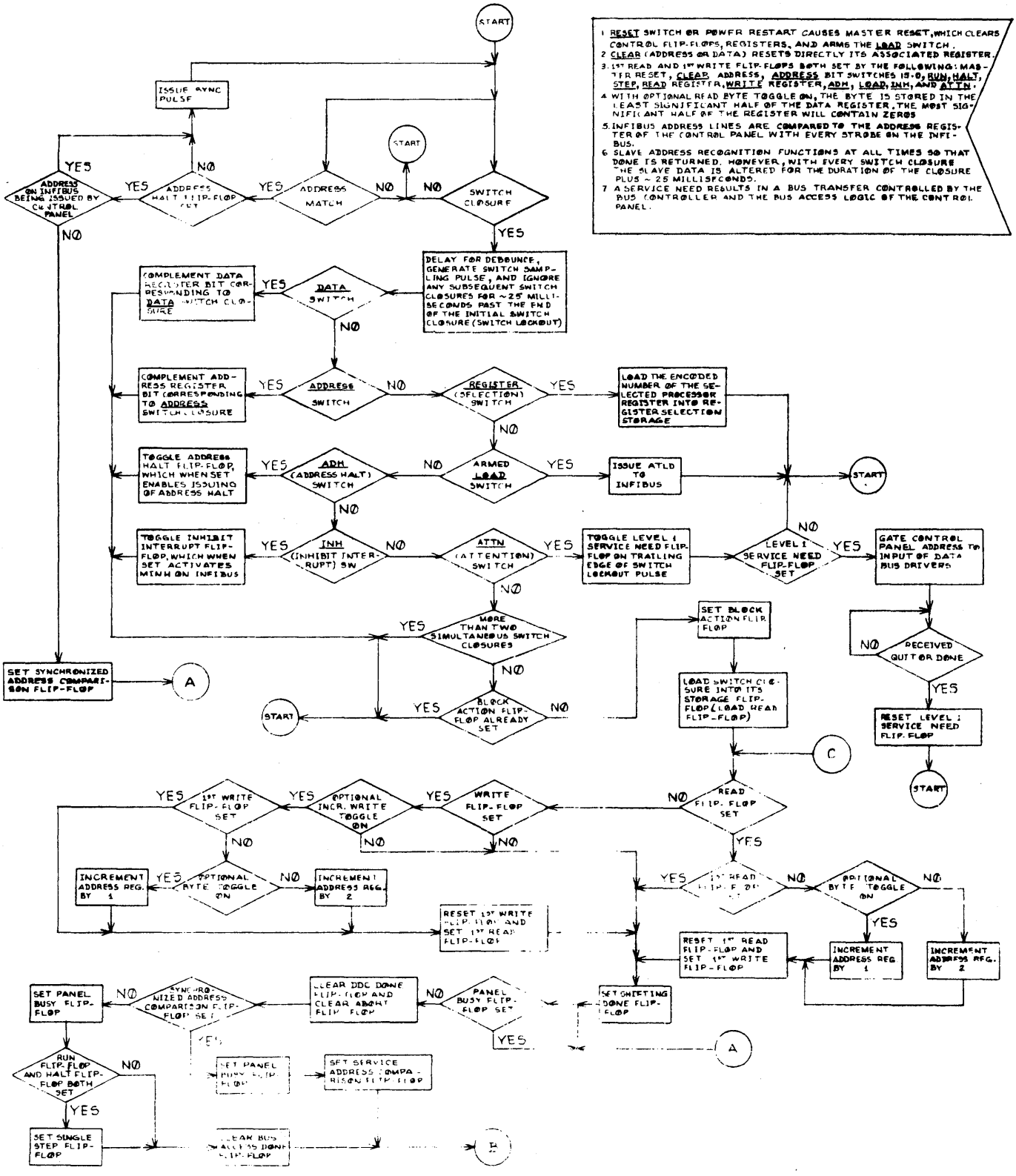


FIGURE 1. PROGRAM/MAINTENANCE PANEL BLOCK DIAGRAM.



1. RESET SWITCH OR POWER RESTART CAUSES MASTER RESET, WHICH CLEARS CONTROL FLIP-FLOPS, REGISTERS, AND ARMS THE LOAD SWITCH.
2. CLEAR (ADDRESS OR DATA) RESETS DIRECTLY ITS ASSOCIATED REGISTER.
3. 1ST READ AND 1ST WRITE FLIP-FLOPS BOTH SET BY THE FOLLOWING: MASTER RESET, CLEAR, ADDRESS, ADDRESS BIT SWITCHES 15-0, RUN, HALT, STEP, READ REGISTER, WRITE REGISTER, ADH, LOAD, INH, AND ATTN.
4. WITH OPTIONAL READ BYTE TOGGLE ON, THE BYTE IS STORED IN THE LEAST SIGNIFICANT HALF OF THE DATA REGISTER, THE MOST SIGNIFICANT HALF OF THE REGISTER WILL CONTAIN ZEROS
5. INFIBUS ADDRESS LINES ARE COMPARED TO THE ADDRESS REGISTER OF THE CONTROL PANEL WITH EVERY STROBE ON THE INFIBUS.
6. SLAVE ADDRESS RECOGNITION FUNCTIONS AT ALL TIMES SO THAT DONE IS RETURNED. HOWEVER, WITH EVERY SWITCH CLOSURE THE SLAVE DATA IS ALTERED FOR THE DURATION OF THE CLOSURE PLUS ~ 25 MILLISECONDS.
7. A SERVICE NEED RESULTS IN A BUS TRANSFER CONTROLLED BY THE BUS CONTROLLER AND THE BUS ACCESS LOGIC OF THE CONTROL PANEL.

FIGURE 2. PROGRAM MAINTENANCE PANEL FLOWCHART

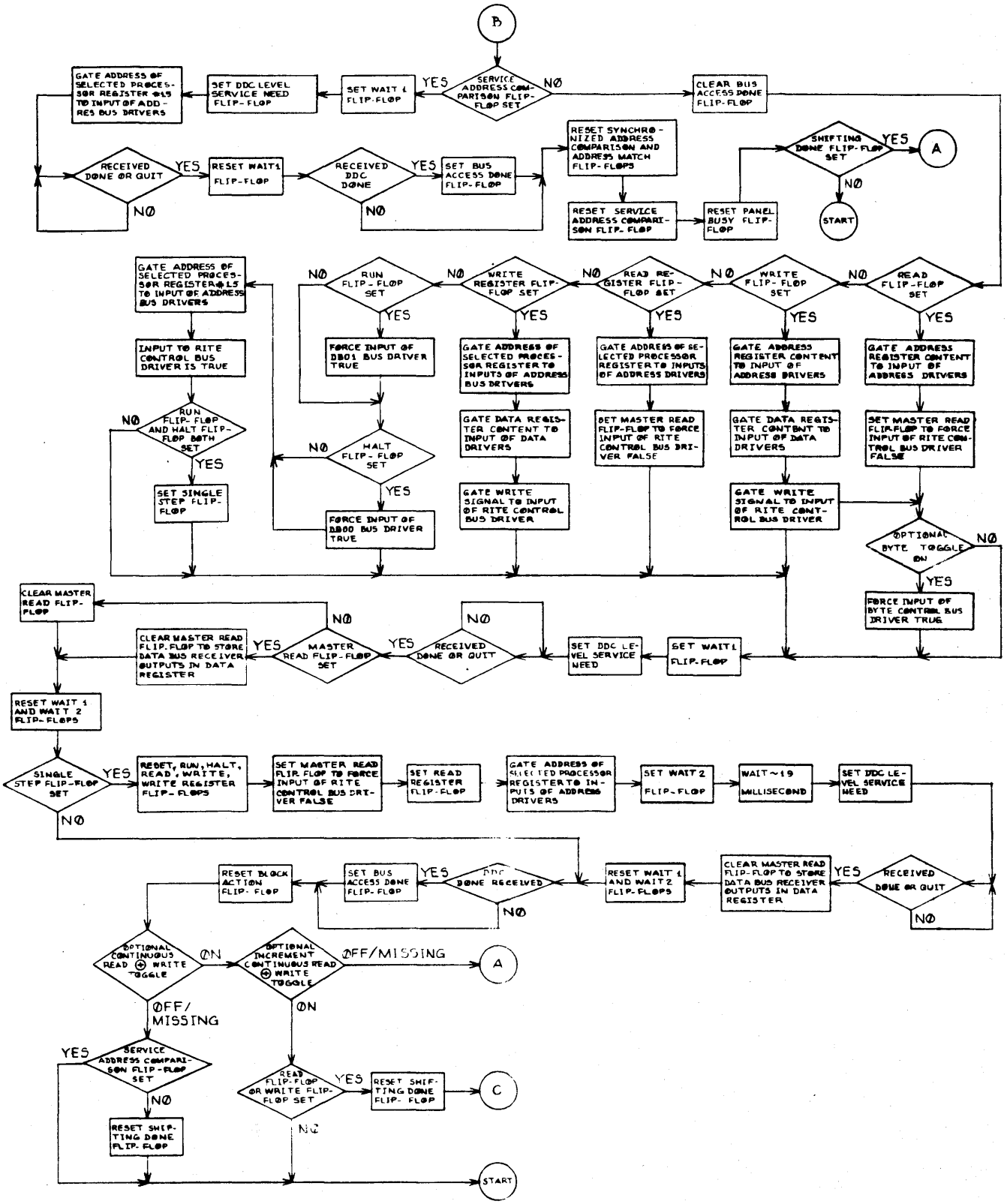
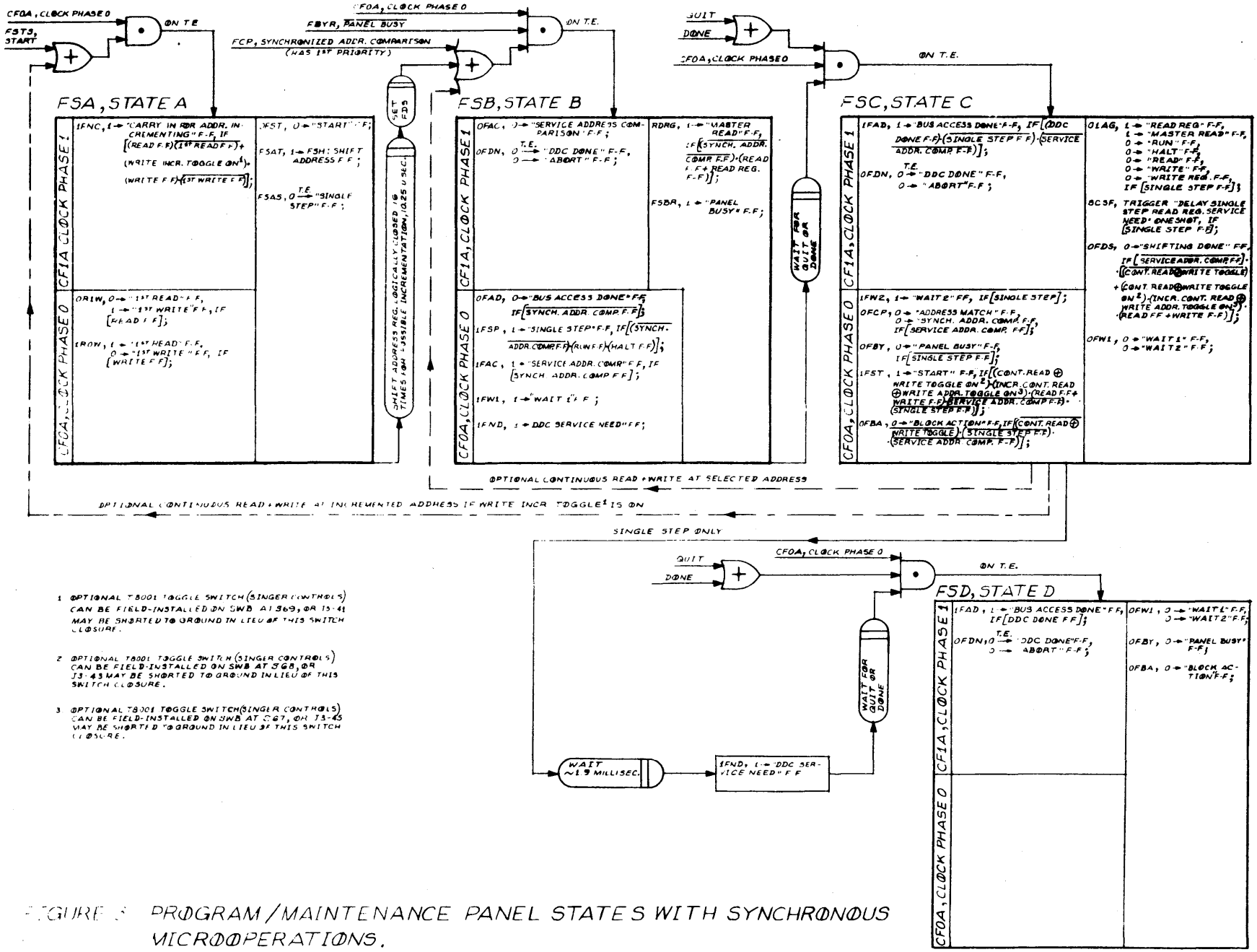


FIGURE 2 (CONTINUED). PROGRAM/MAINTENANCE PANEL FLOWCHART



1 OPTIONAL T8001 TOGGLE SWITCH (SINGER CONTROLS) CAN BE FIELD-INSTALLED ON SWB AT J3-69, OR J3-41 MAY BE SHORTED TO GROUND IN LIEU OF THIS SWITCH CLOSURE.

2 OPTIONAL T8001 TOGGLE SWITCH (SINGER CONTROLS) CAN BE FIELD-INSTALLED ON SWB AT J3-68, OR J3-43 MAY BE SHORTED TO GROUND IN LIEU OF THIS SWITCH CLOSURE.

3 OPTIONAL T8001 TOGGLE SWITCH (SINGER CONTROLS) CAN BE FIELD-INSTALLED ON SWB AT J3-67, OR J3-45 MAY BE SHORTED TO GROUND IN LIEU OF THIS SWITCH CLOSURE.

FIGURE 3 PROGRAM/MAINTENANCE PANEL STATES WITH SYNCHRONOUS MICROOPERATIONS.

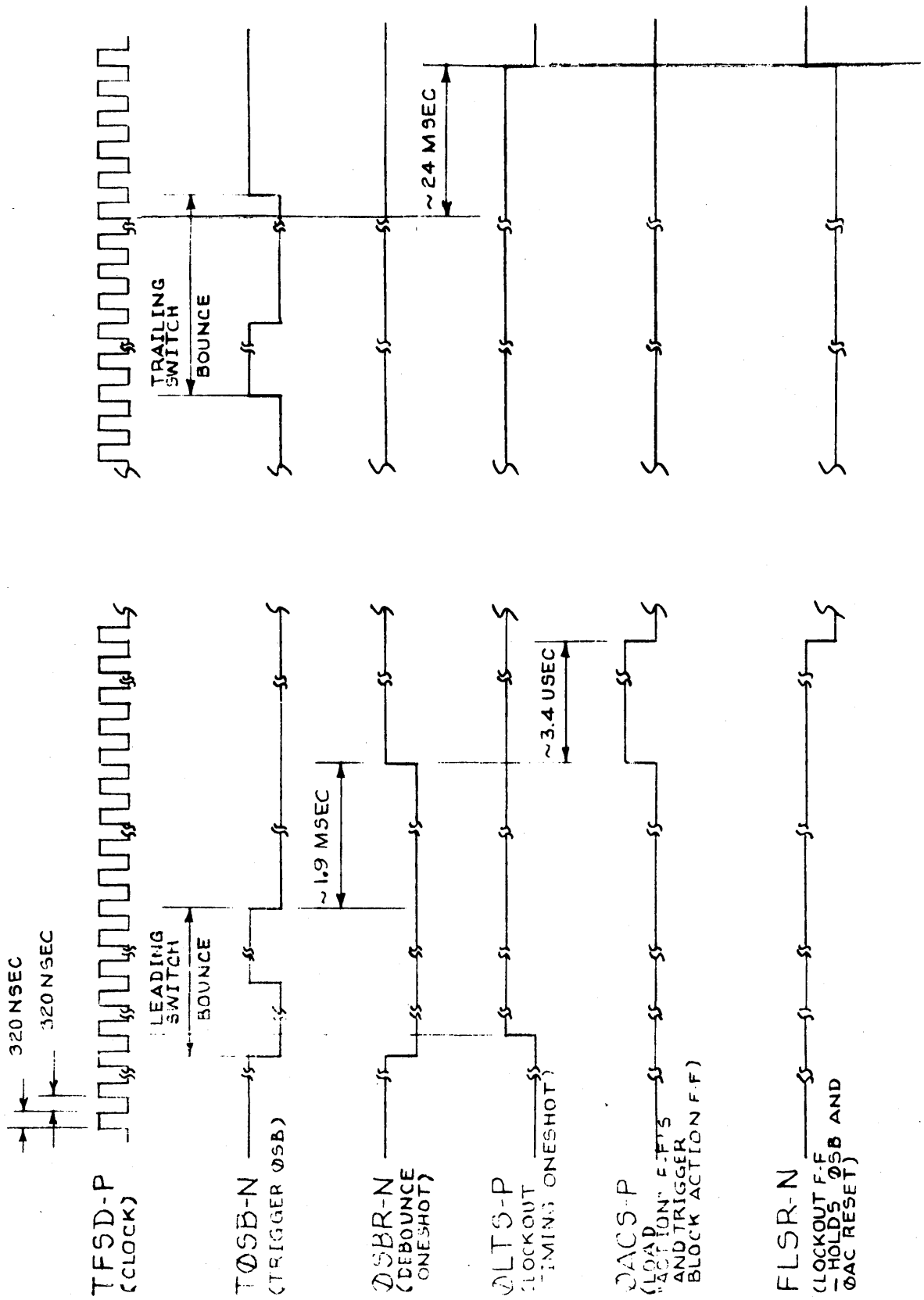
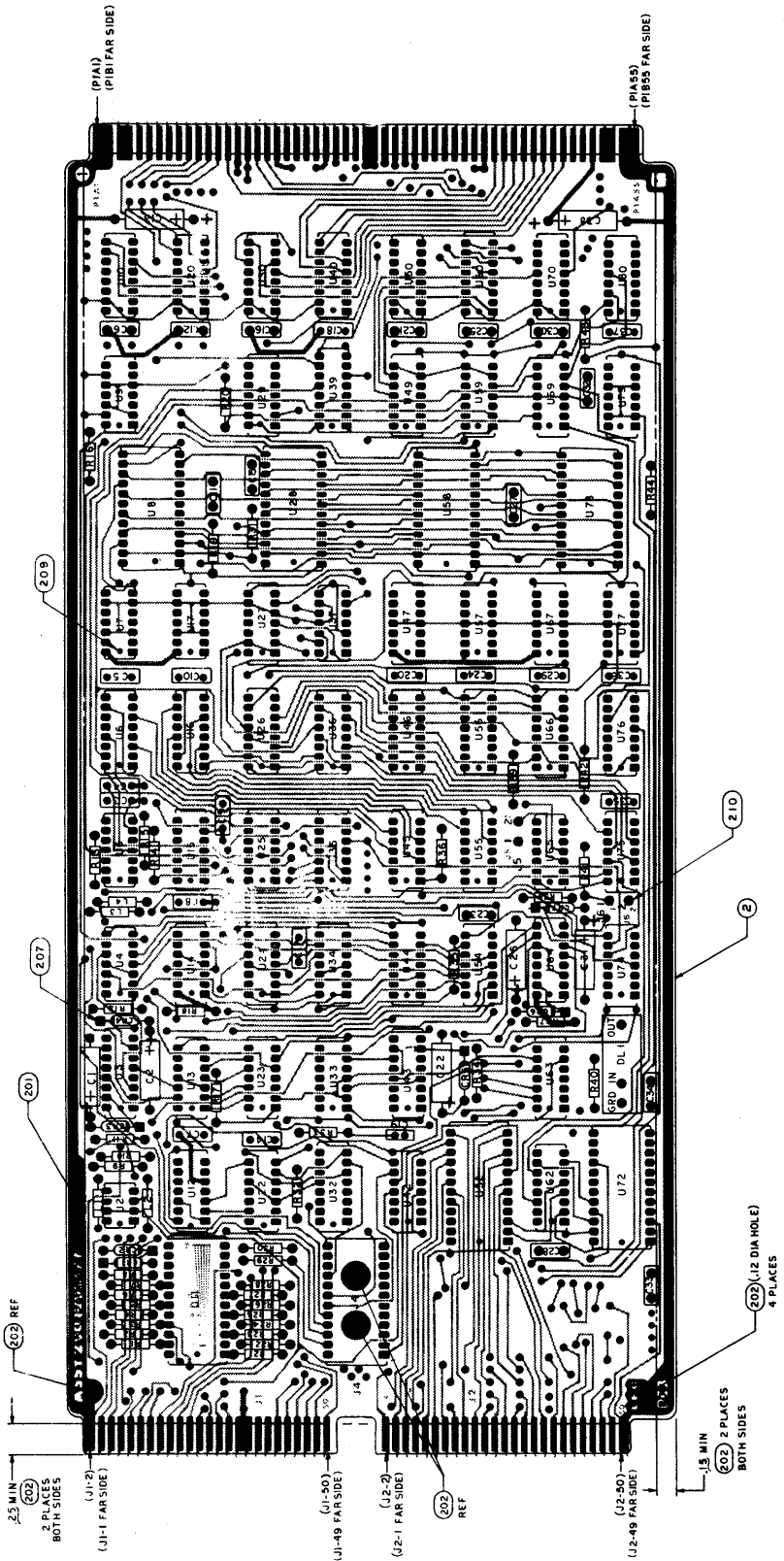


FIGURE 4. Switch Debounce and Lockout Timing Diagram

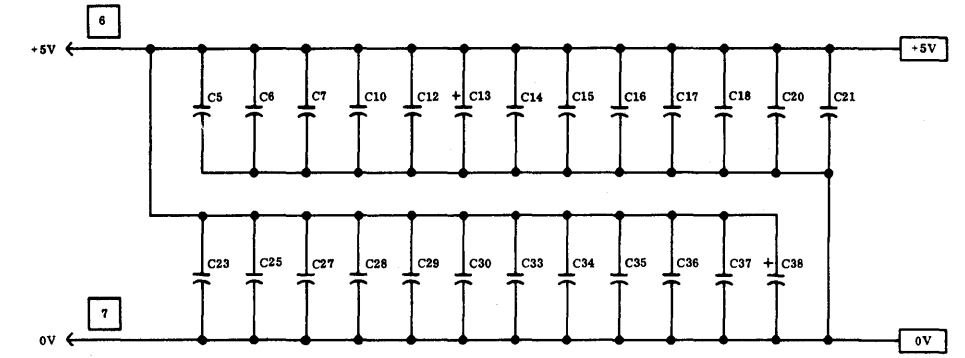
PBI

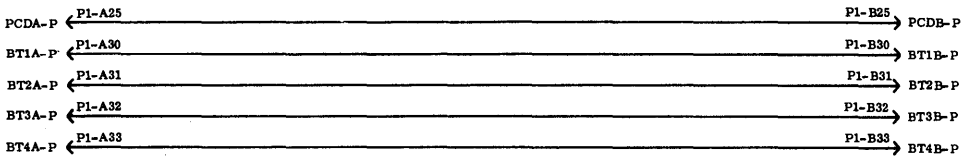


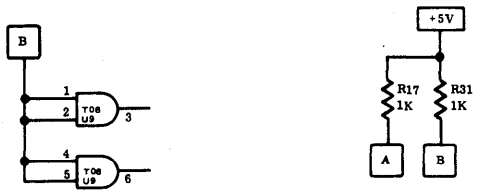
Control Panel Circuit Card (PCB)
2001002177-1, Rev. D (Sheet 1)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT T73 PIN 4 +5V, PIN 11 0V, T93 PIN 5 +5V, PIN 10 0V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR PIN 7 AND 8 0V, PIN 16 +5V T76 PIN 5 +5V, PIN 13 0V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V, EXCEPT R165 PIN 1 +5V, PIN 23 0V.
6. +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51; J1-32, 34; J2-33, 35.
7. 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J2-49.
8. ALL DIODES ARE 8001100001-1.



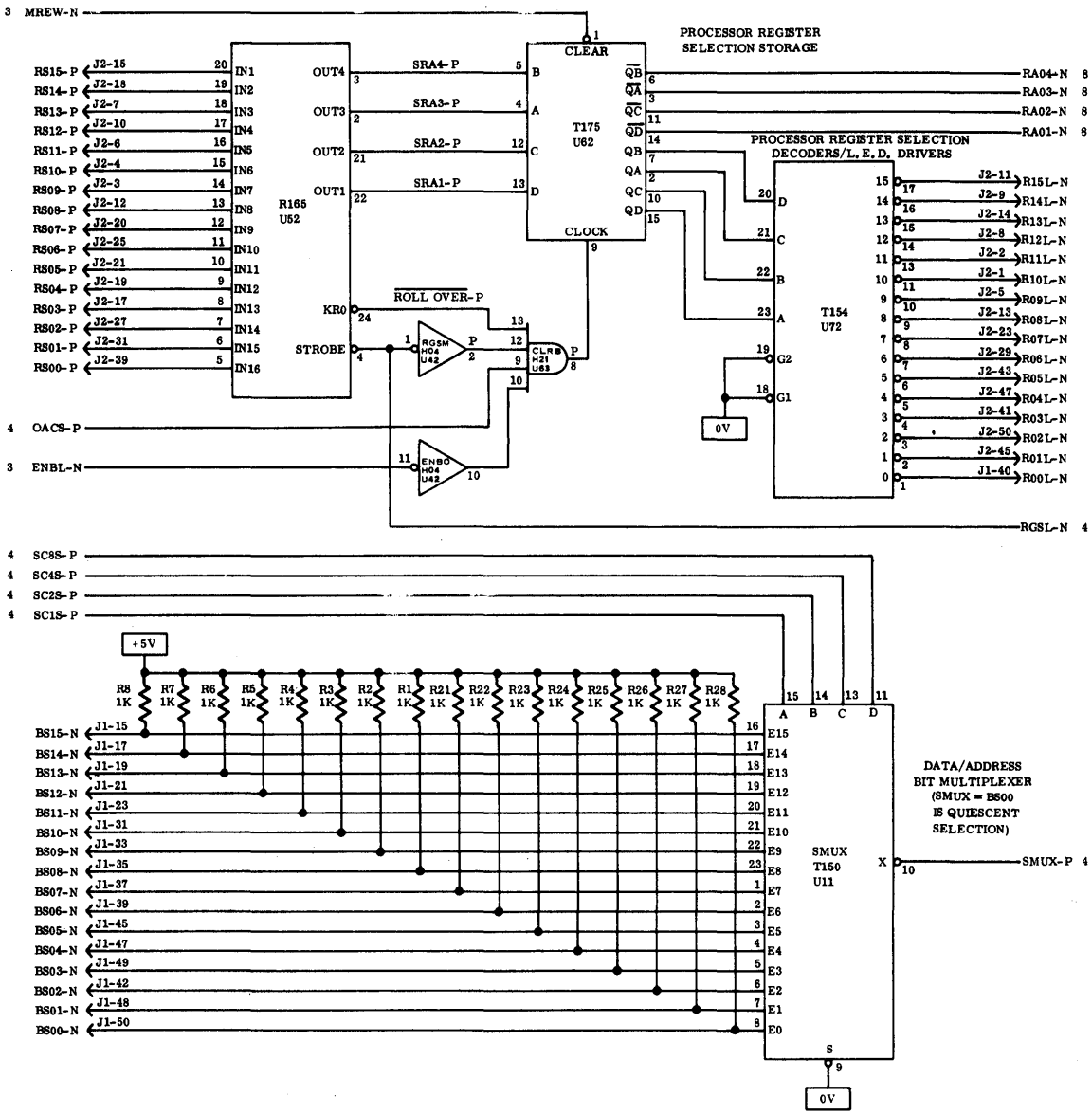




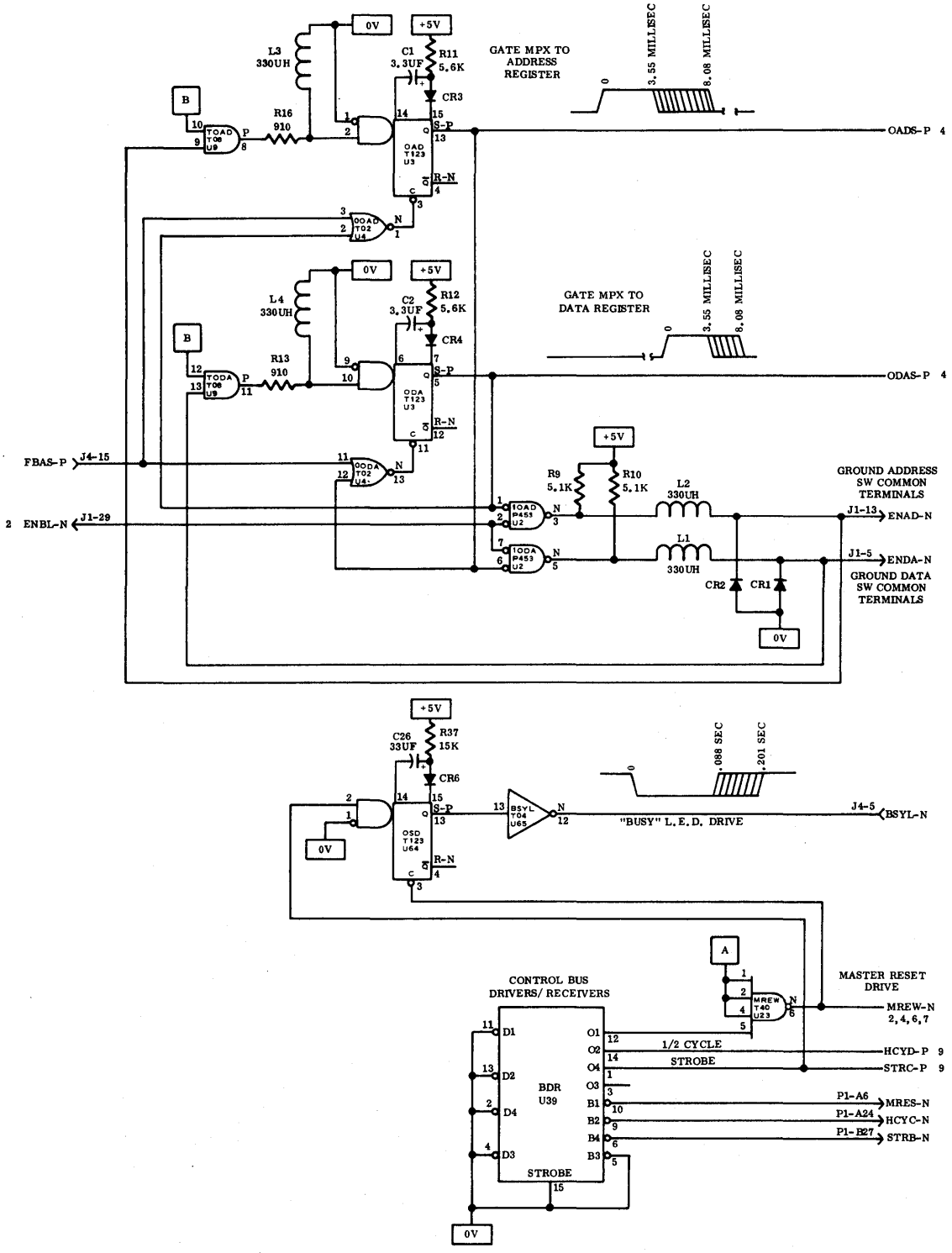
UNUSED GATES

PB1

Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 1 of 9)

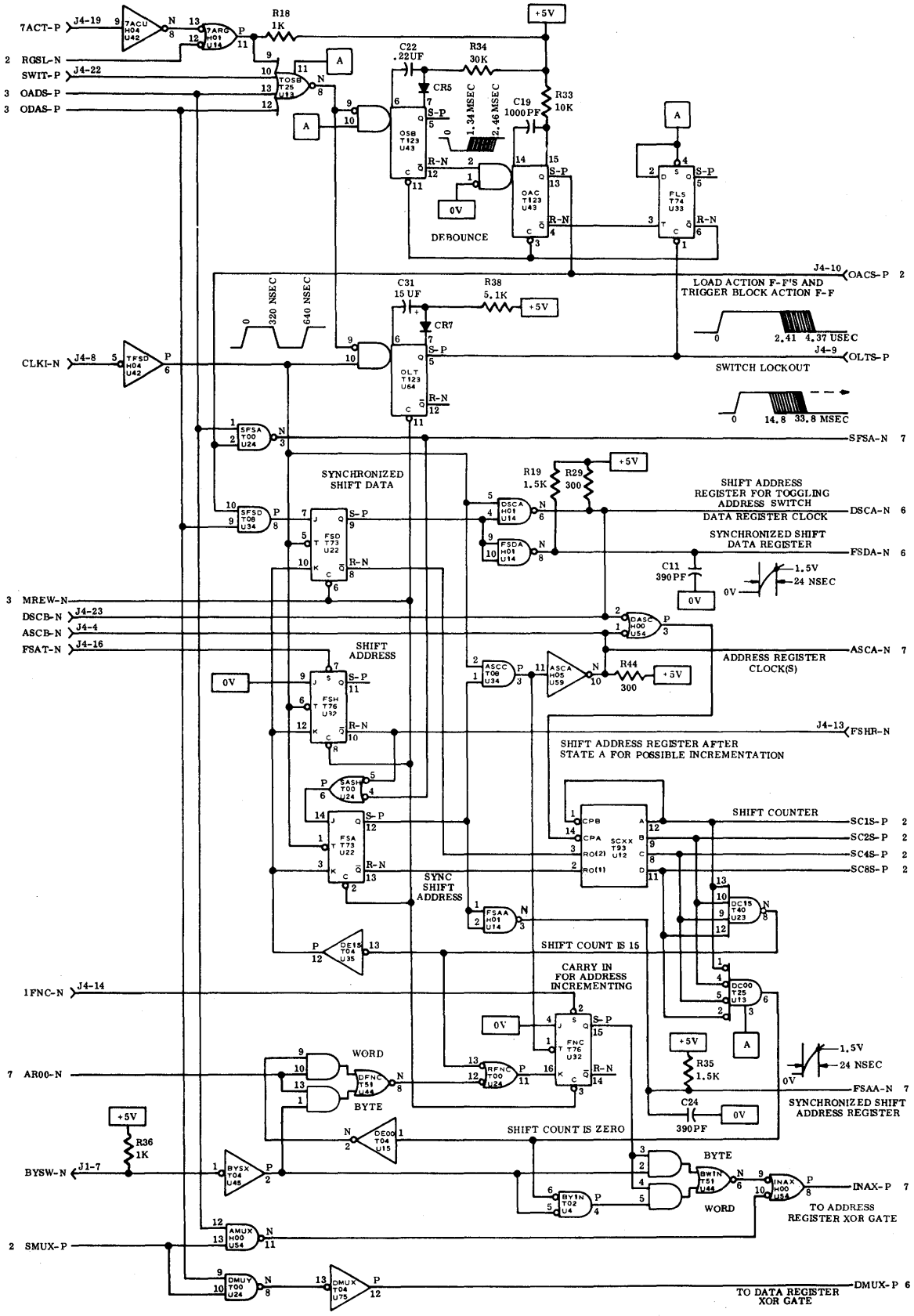


Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 2 of 9)

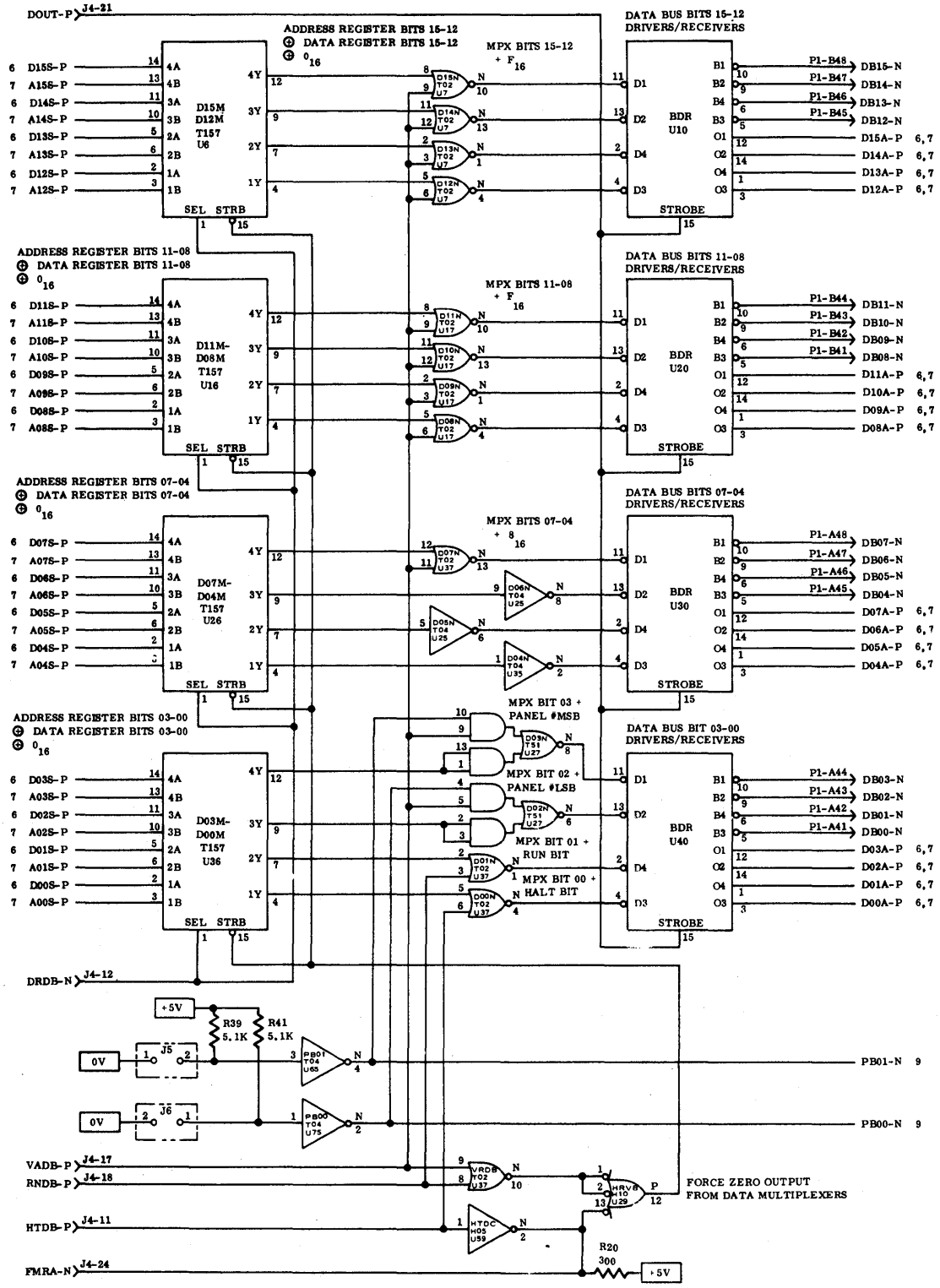


PB1

Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 3 of 9)



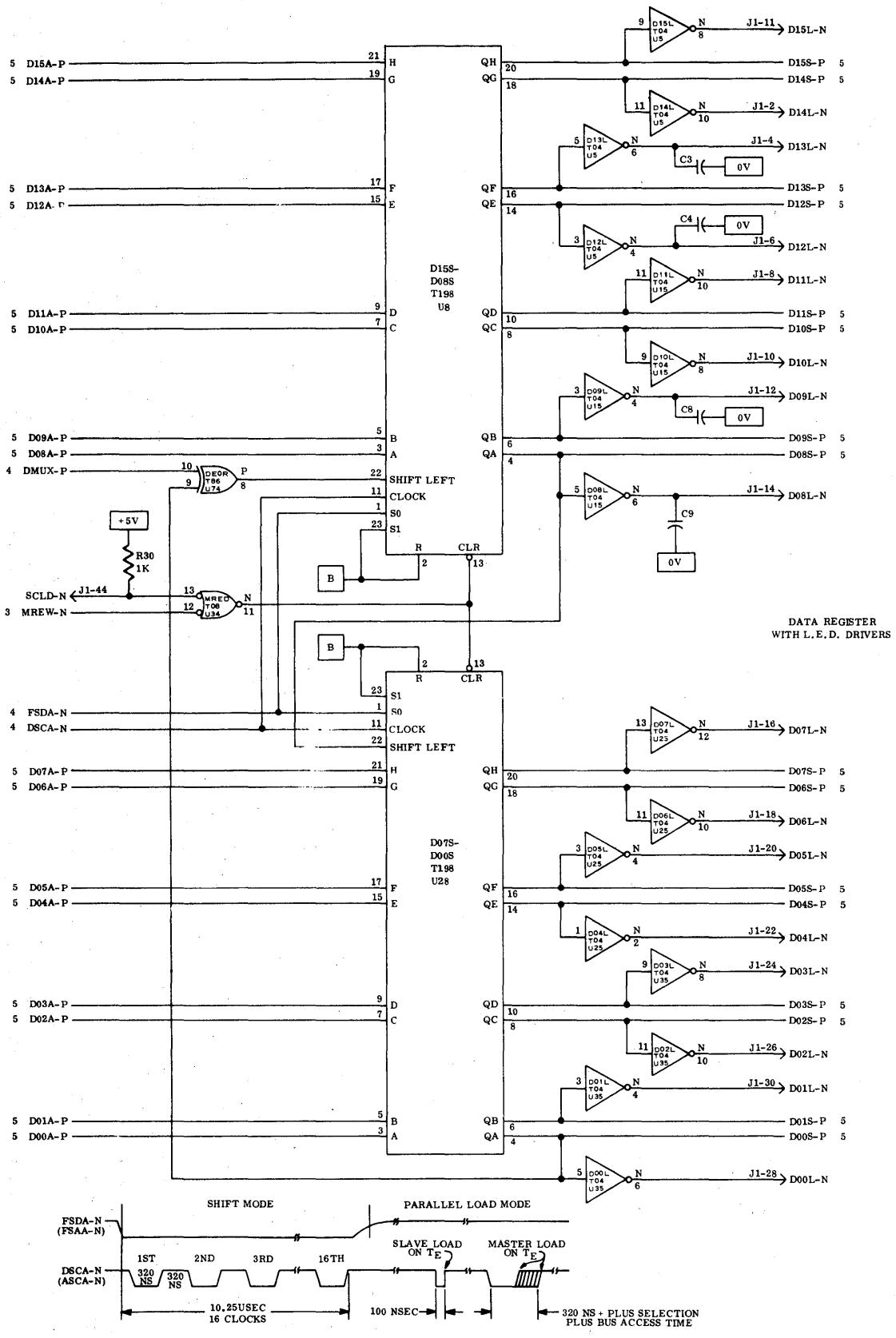
Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 4 of 9)



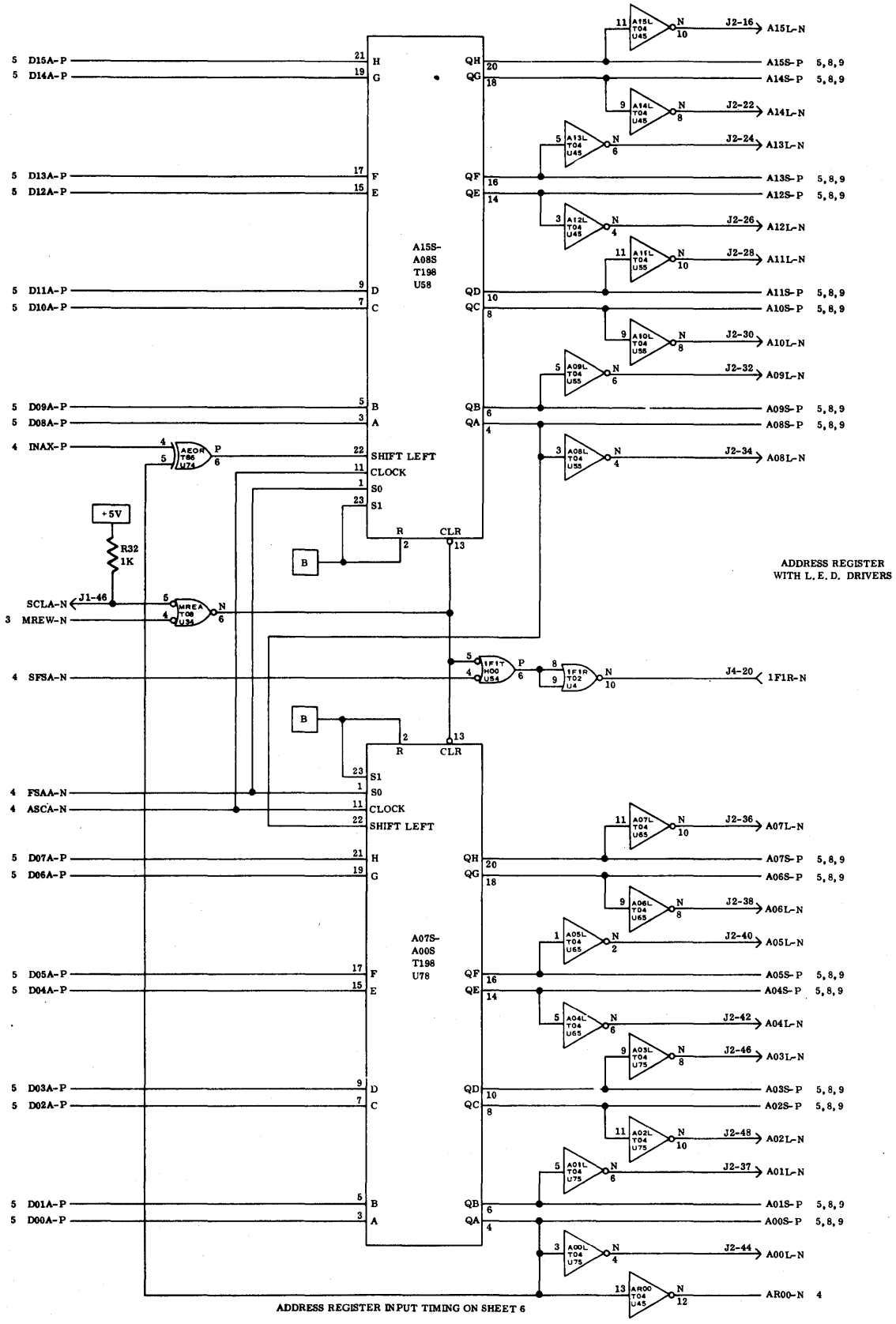
J5	J6	CONTROL PANEL
NONE	NONE	#1 (STANDARD PRODUCTION)
NONE	JUMPERED	#2
JUMPERED	NONE	#3
JUMPERED	JUMPERED	#4

PB1

Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 5 of 9)

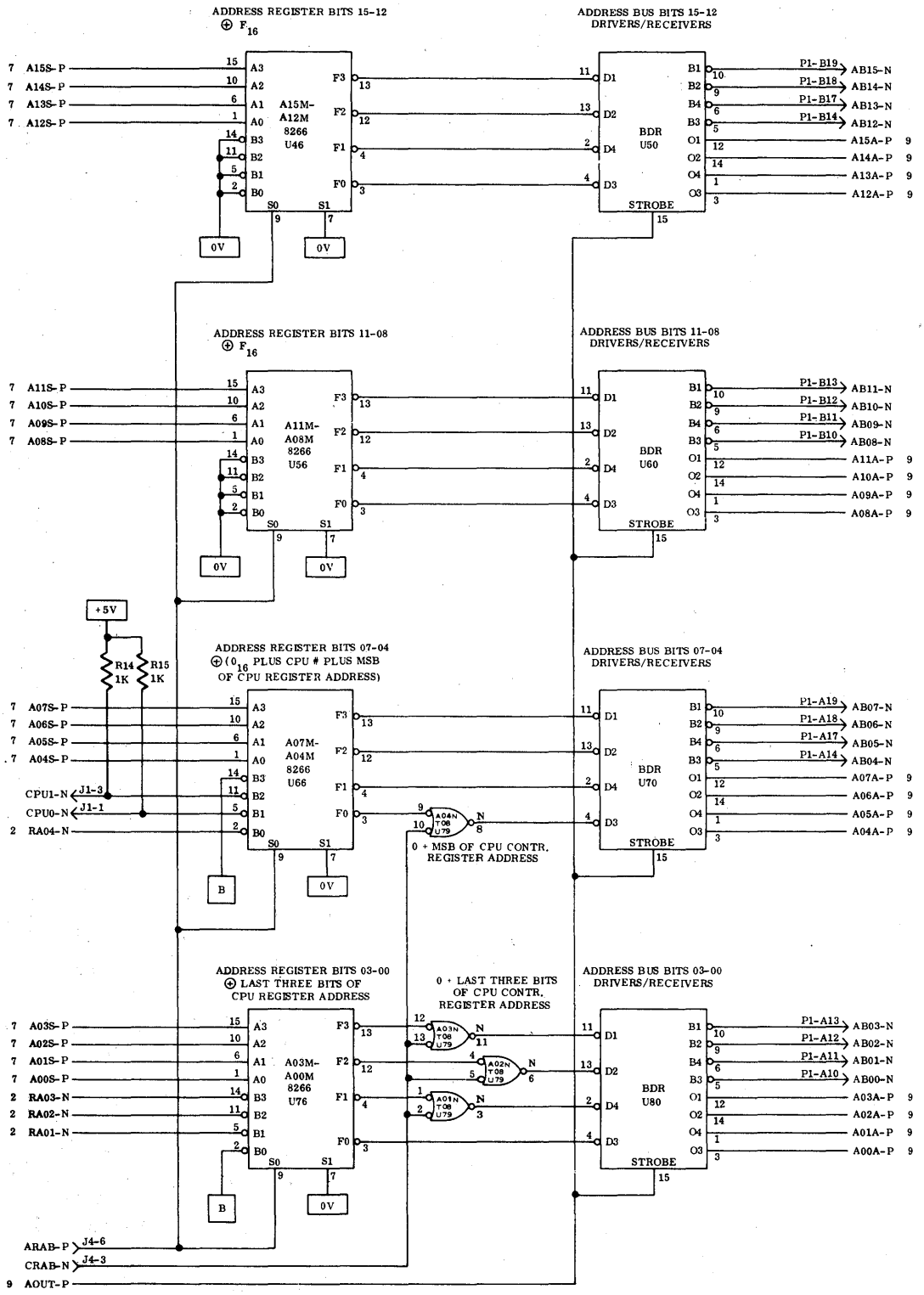


Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 6 of 9)

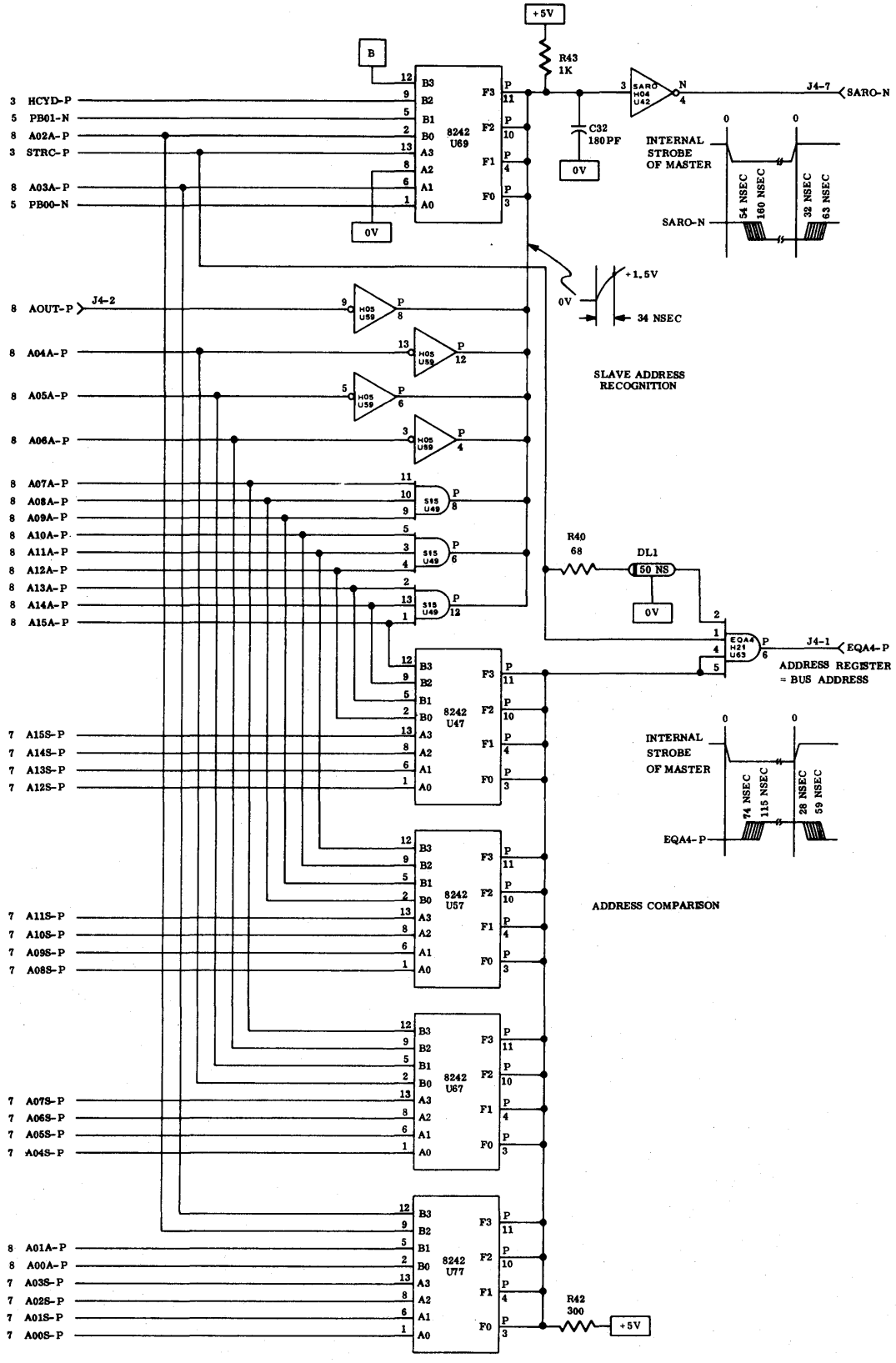


Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 7 of 9)

PBI

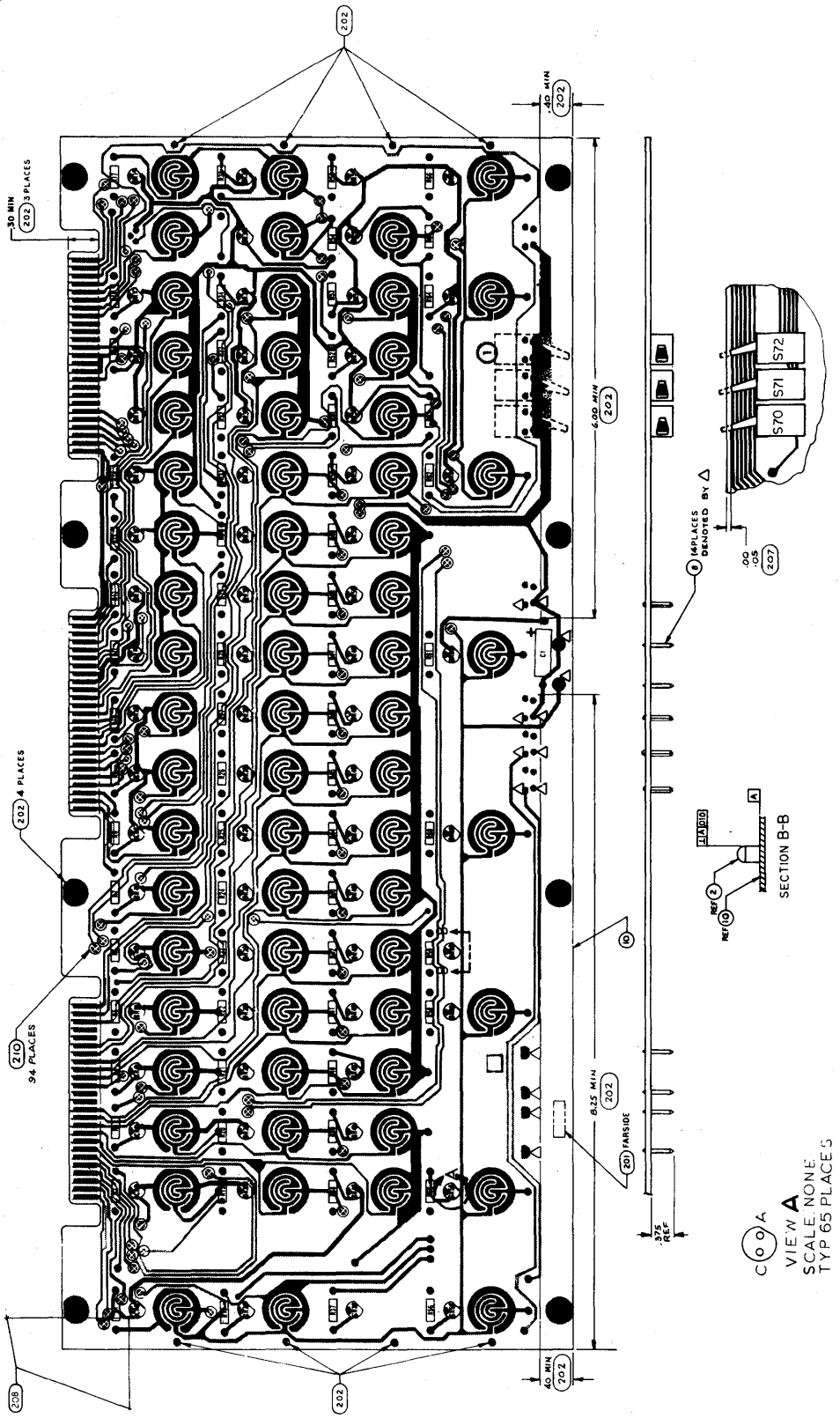


Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 8 of 9)



PBI

Control Panel Logic Diagram (PCB)
LD2001002177-1, Rev. C (Sheet 9 of 9)



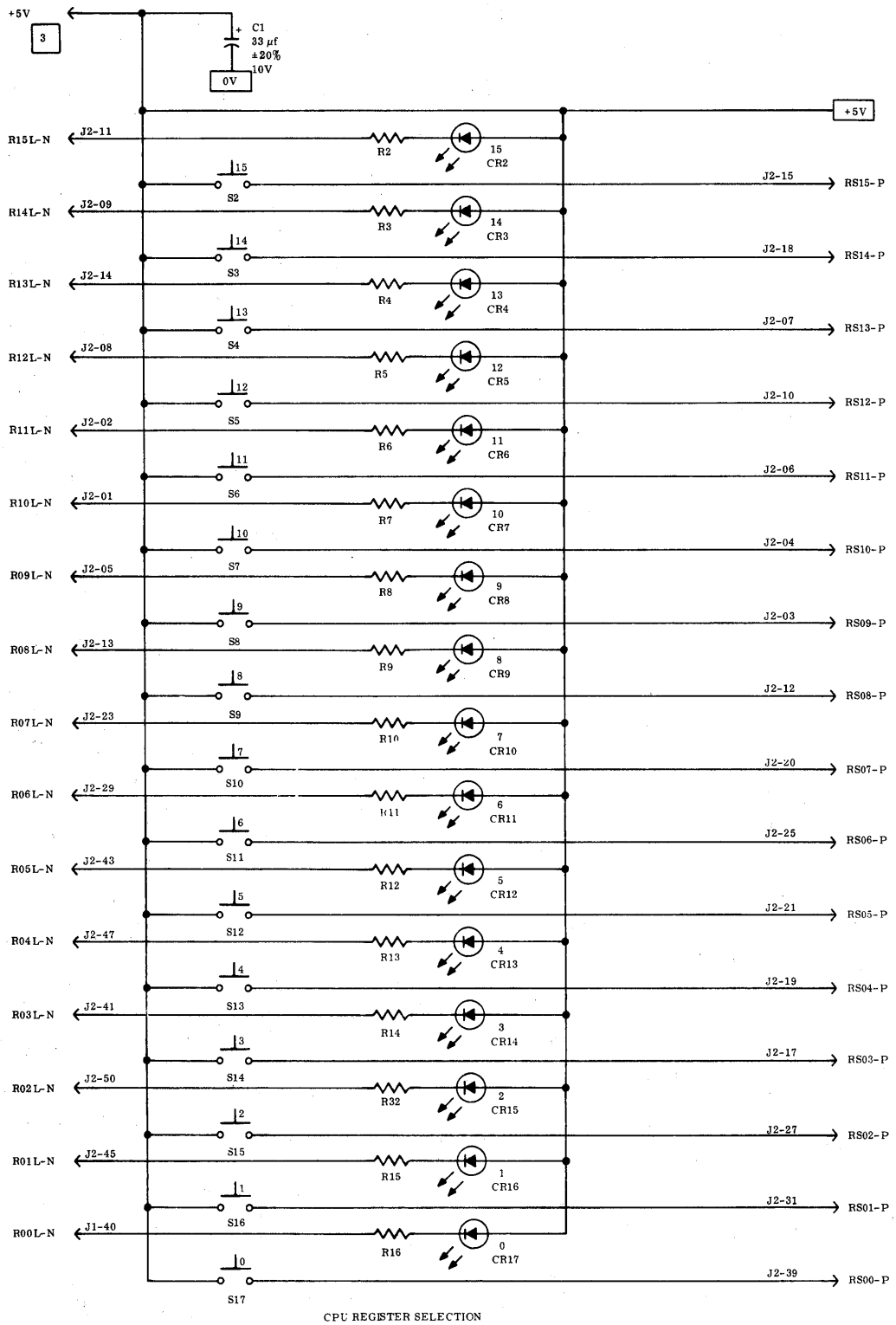
Switch Panel Circuit Card (SWB)
2001002178-1, Rev. H (Sheet 1)

NOTES:

1. ALL RESISTOR VALUES ARE 270 OHMS, ±2%, 1/4W.
2. CONFIGURATION MAY BE USED WITHOUT SWITCHES. IF USED WITHOUT SWITCHES JUMPER S66 THRU S69, S73 TO "ON" POSITION, S70 AND S72 TO "OFF" POSITION AS SHOWN, S71 MAY BE JUMPERED AS REQUIRED.
3. +5V CONNECTOR PINS ARE: J1-32, 34, J2-33, 35, J3-21, 23 AND 25.
4. 0V CONNECTOR PINS ARE: J2-45, J3-1 AND 2.
5. ALL LIGHT-EMITTING DIODES ARE 1005000837-1.

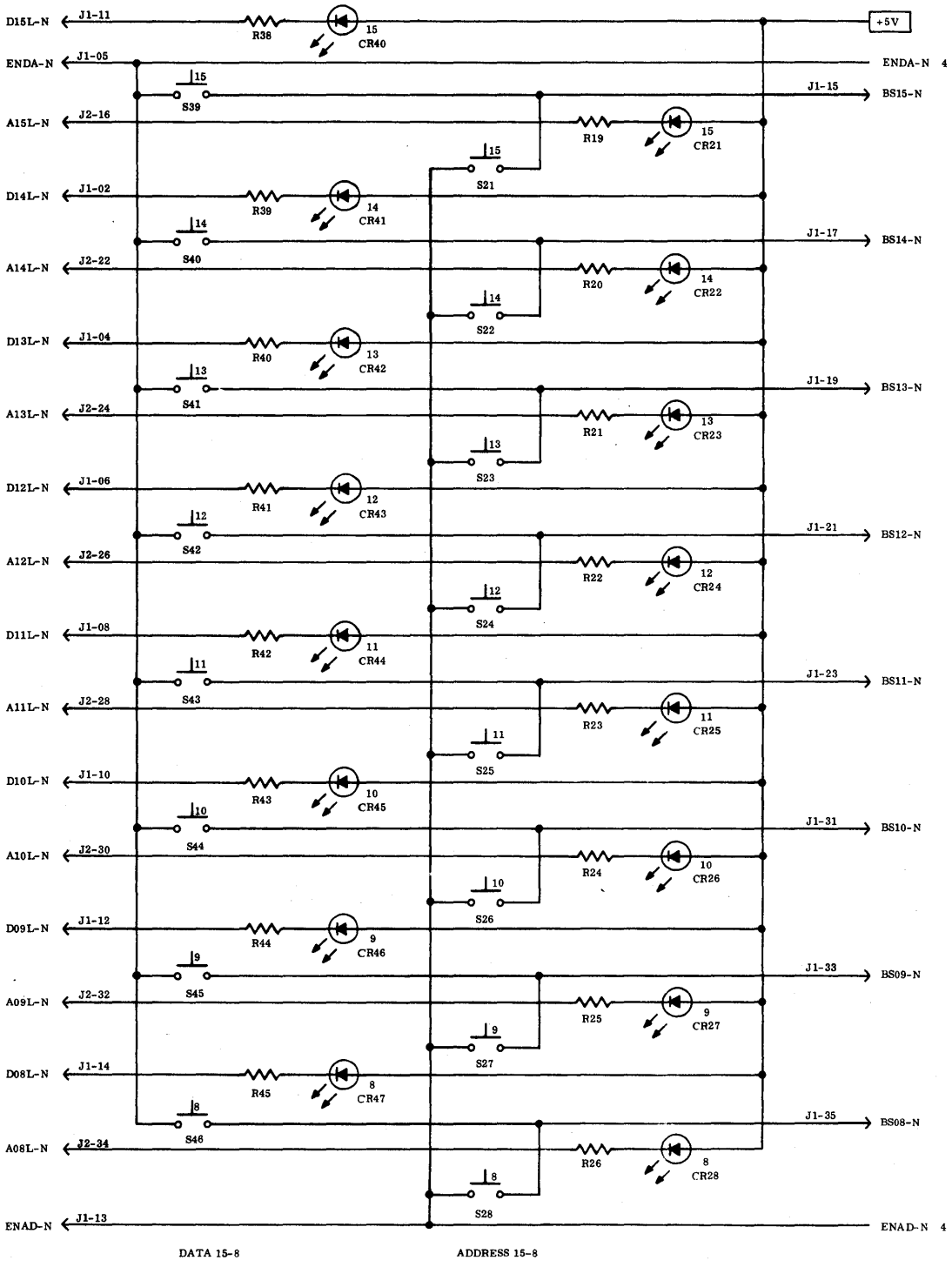
PBI

Switch Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 1 of 6)



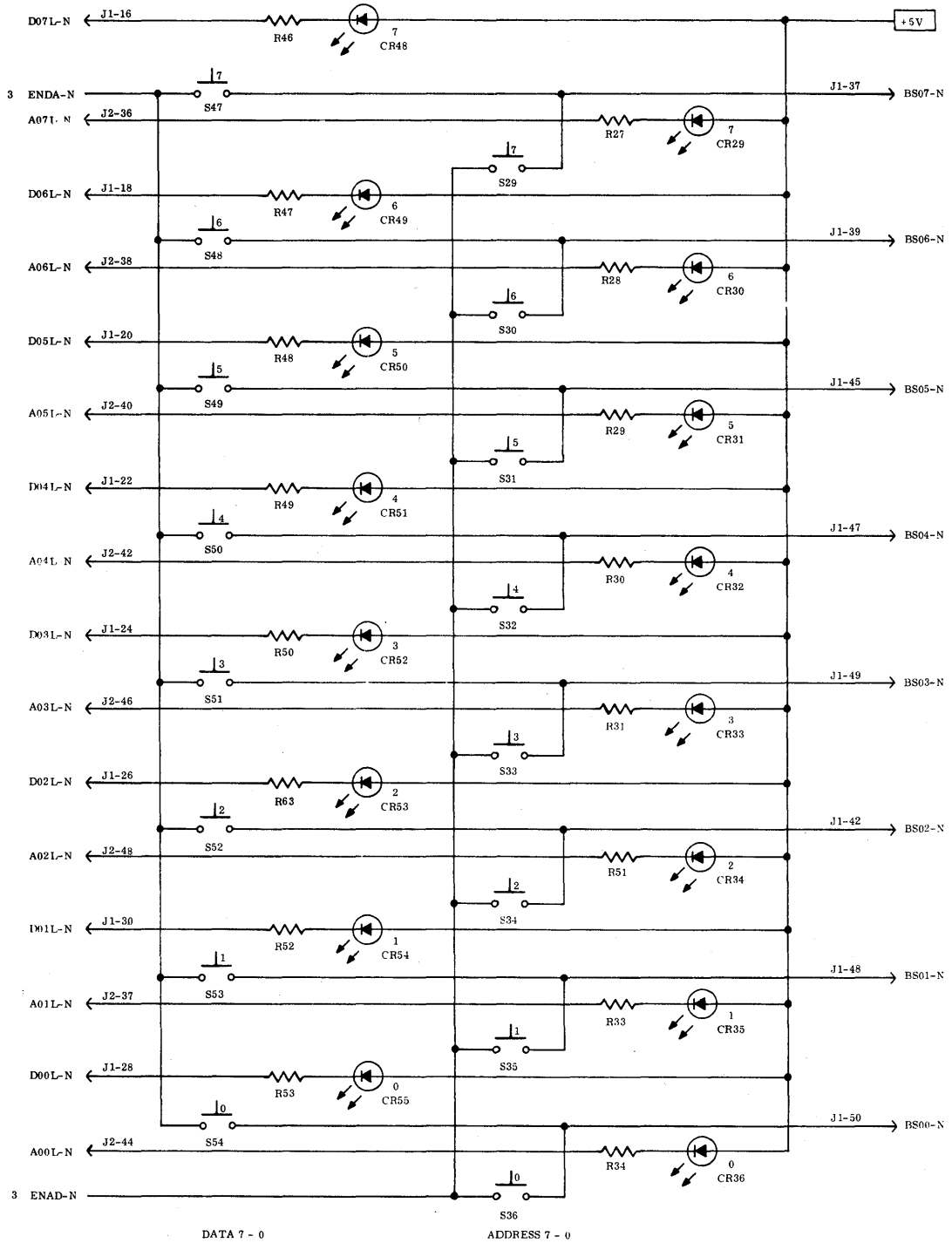
CPU REGISTER SELECTION

Switch Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 2 of 6)

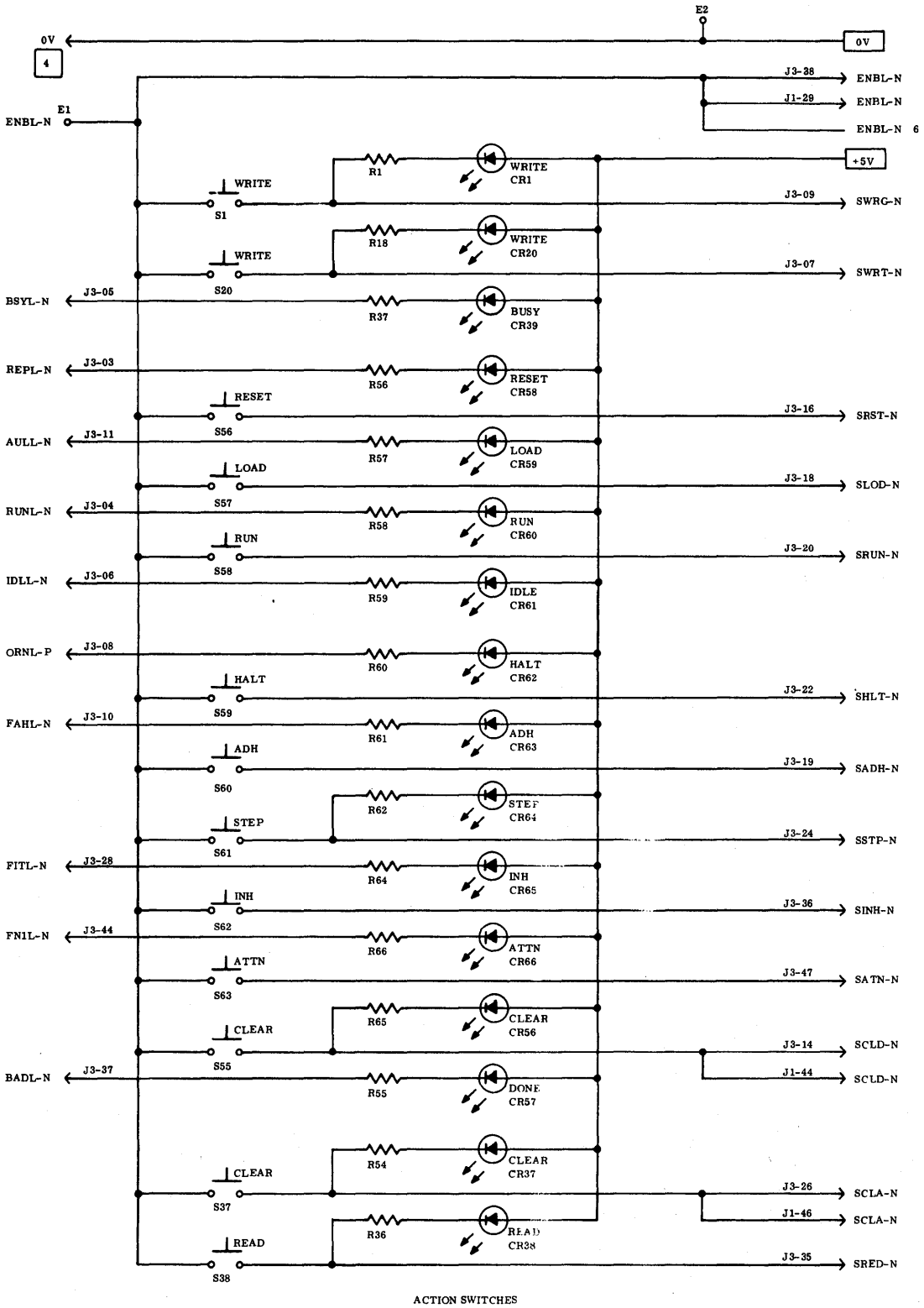


PBI

Switch Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 3 of 6)

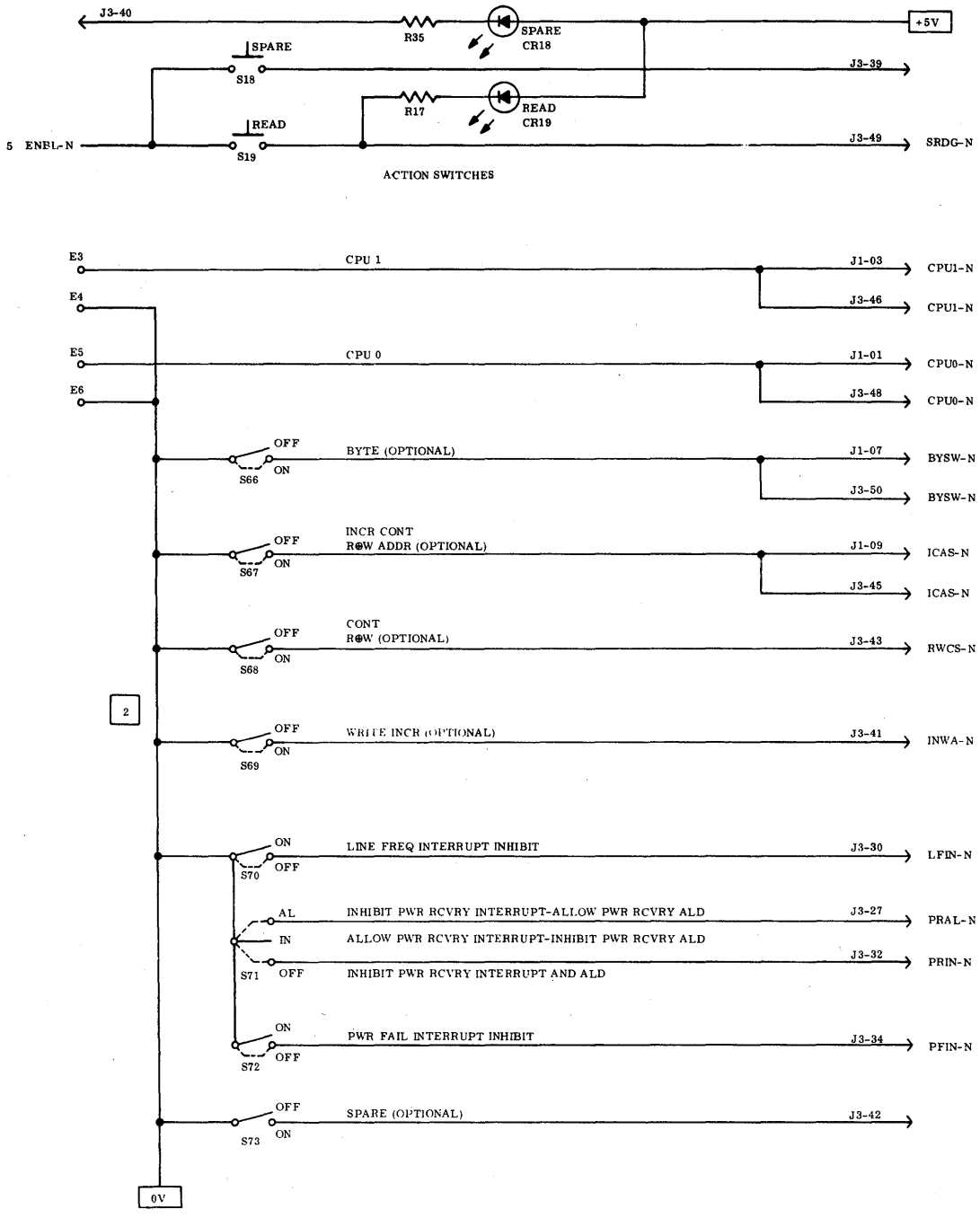


Switch Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 4 of 6)

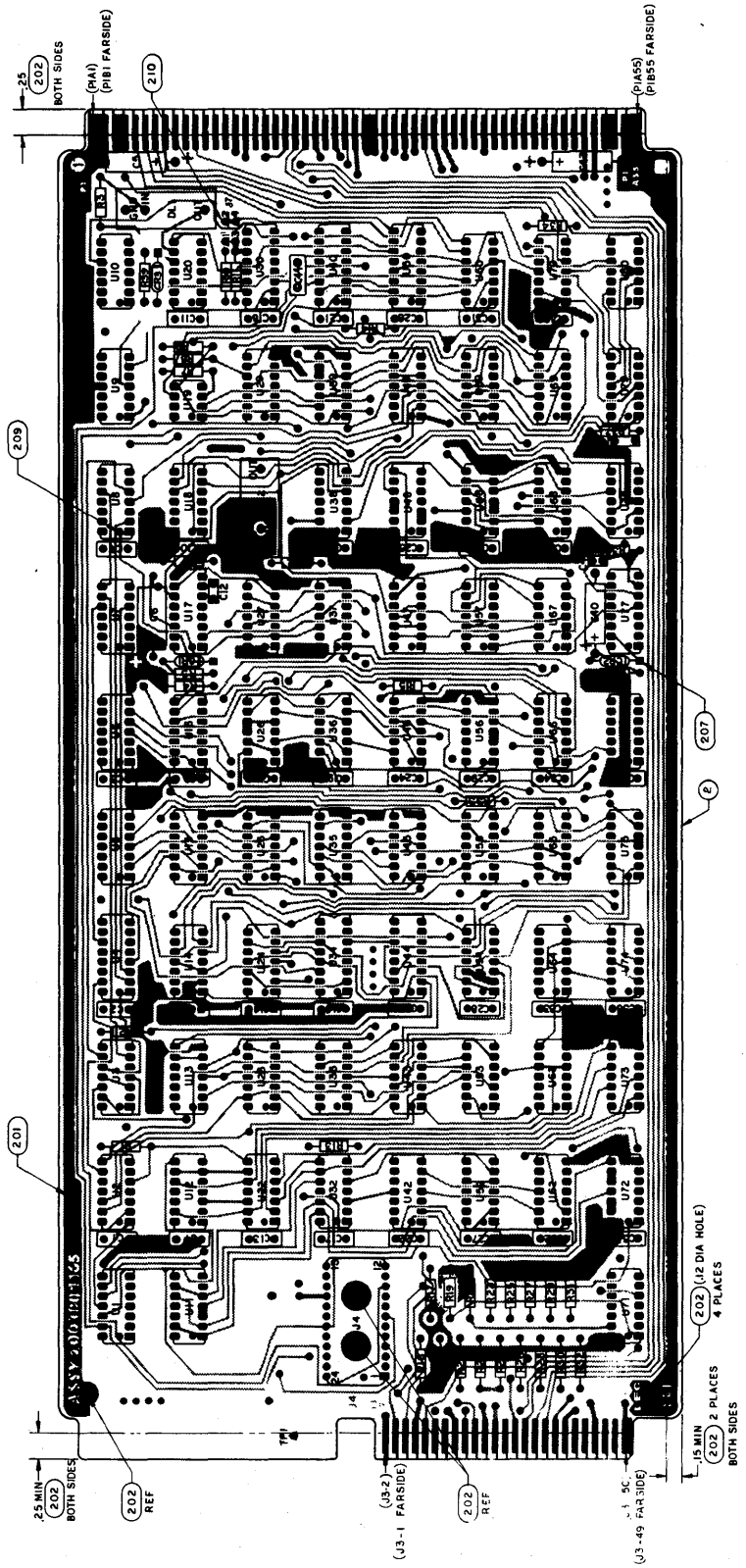


PBI

Switch Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 5 of 6)



Swithc Panel Logic Diagram (SWB)
LD2001002178-1, Rev. D (Sheet 6 of 6)



PBI

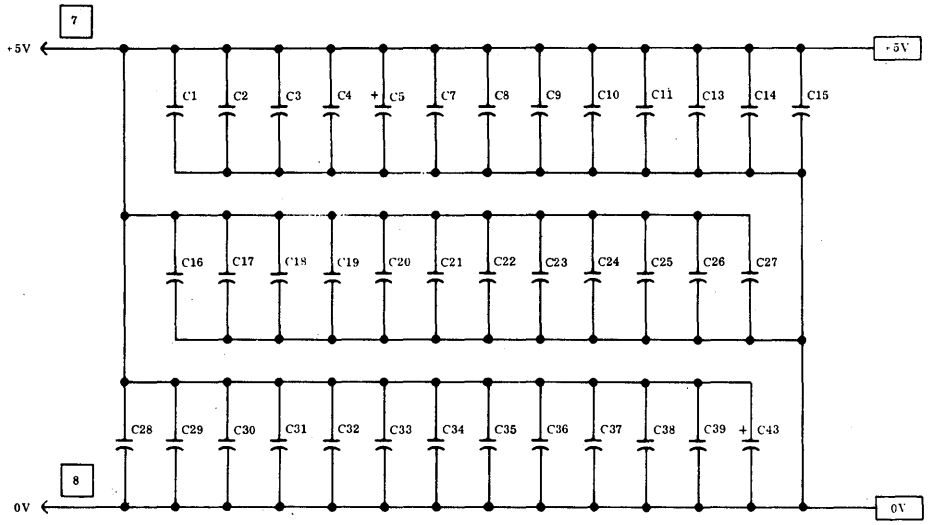
Panel Bus Interface Circuit Card (PBI)
2001002165-1, Rev. D (Sheet 1)

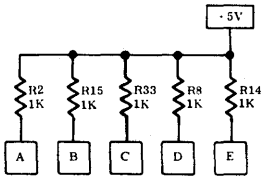
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
4. ALL DIODES ARE 8001100001.
5. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
6. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT T73 PIN 4 +5V, PIN 11 0V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR PIN 7 AND 8 0V, PIN 16 +5V, T76 PIN 5 +5V, PIN 13 0V.

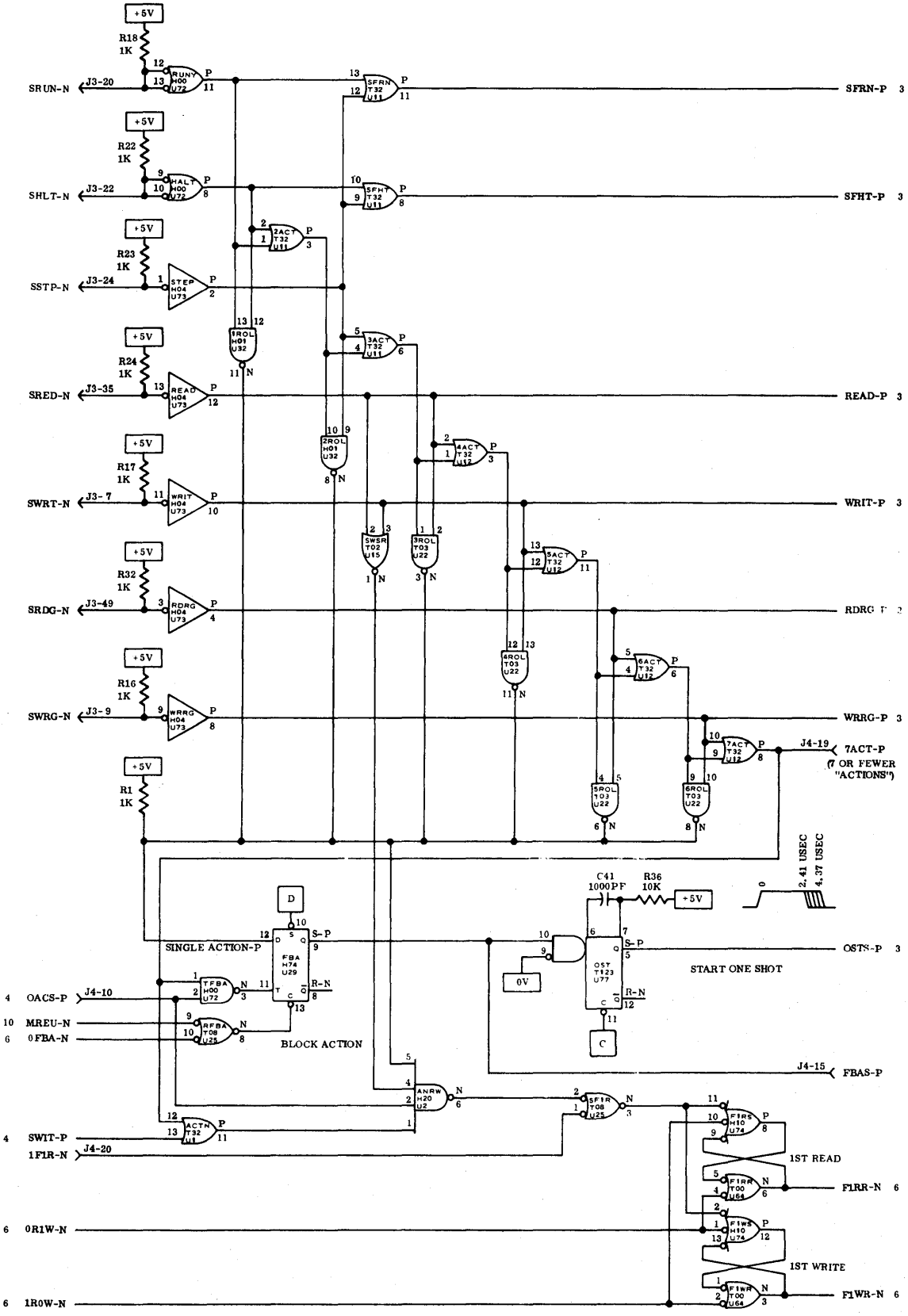
7 +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51; J3-21, 23, 25.

8 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J3-1,2.



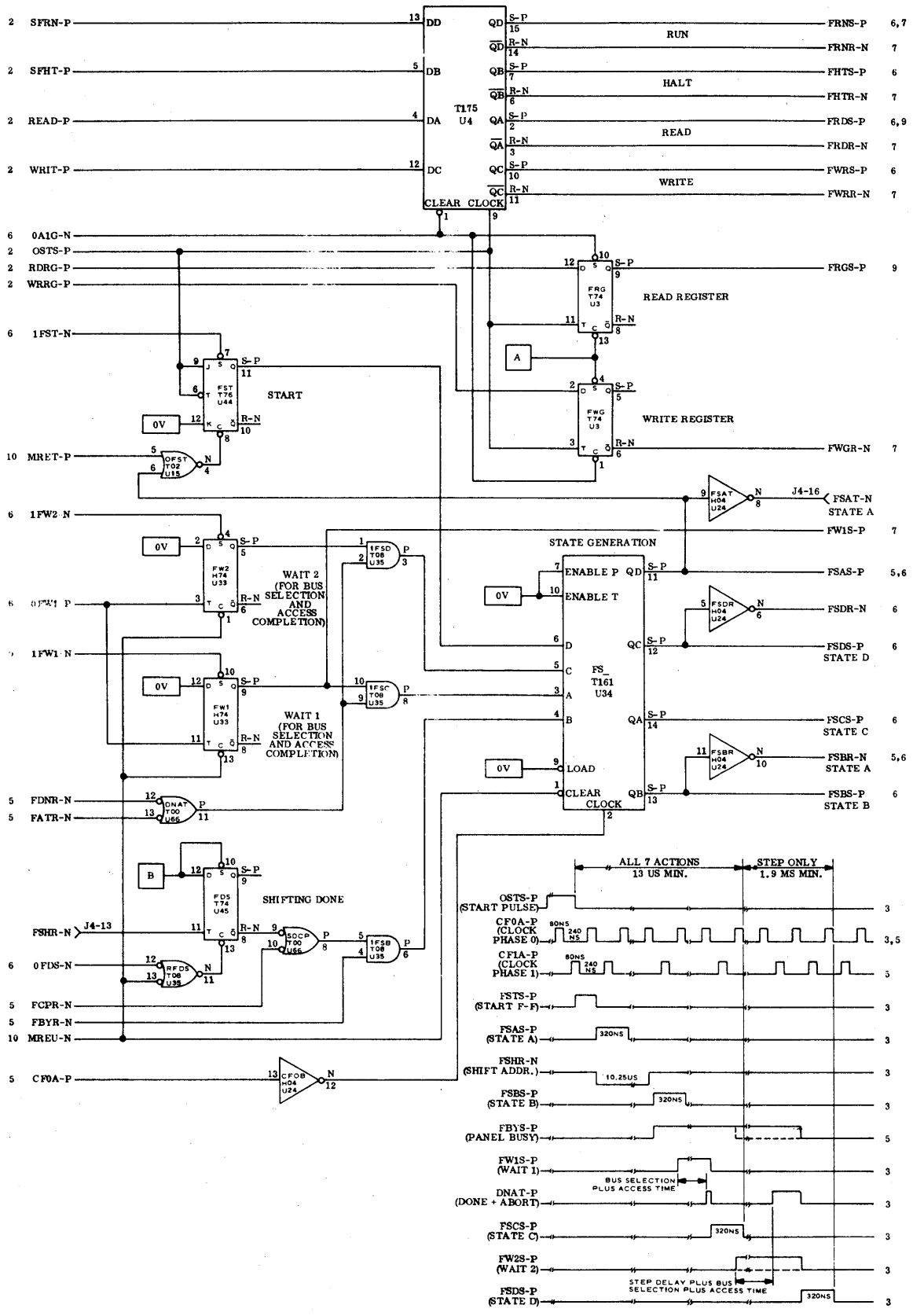


Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 1 of 10)

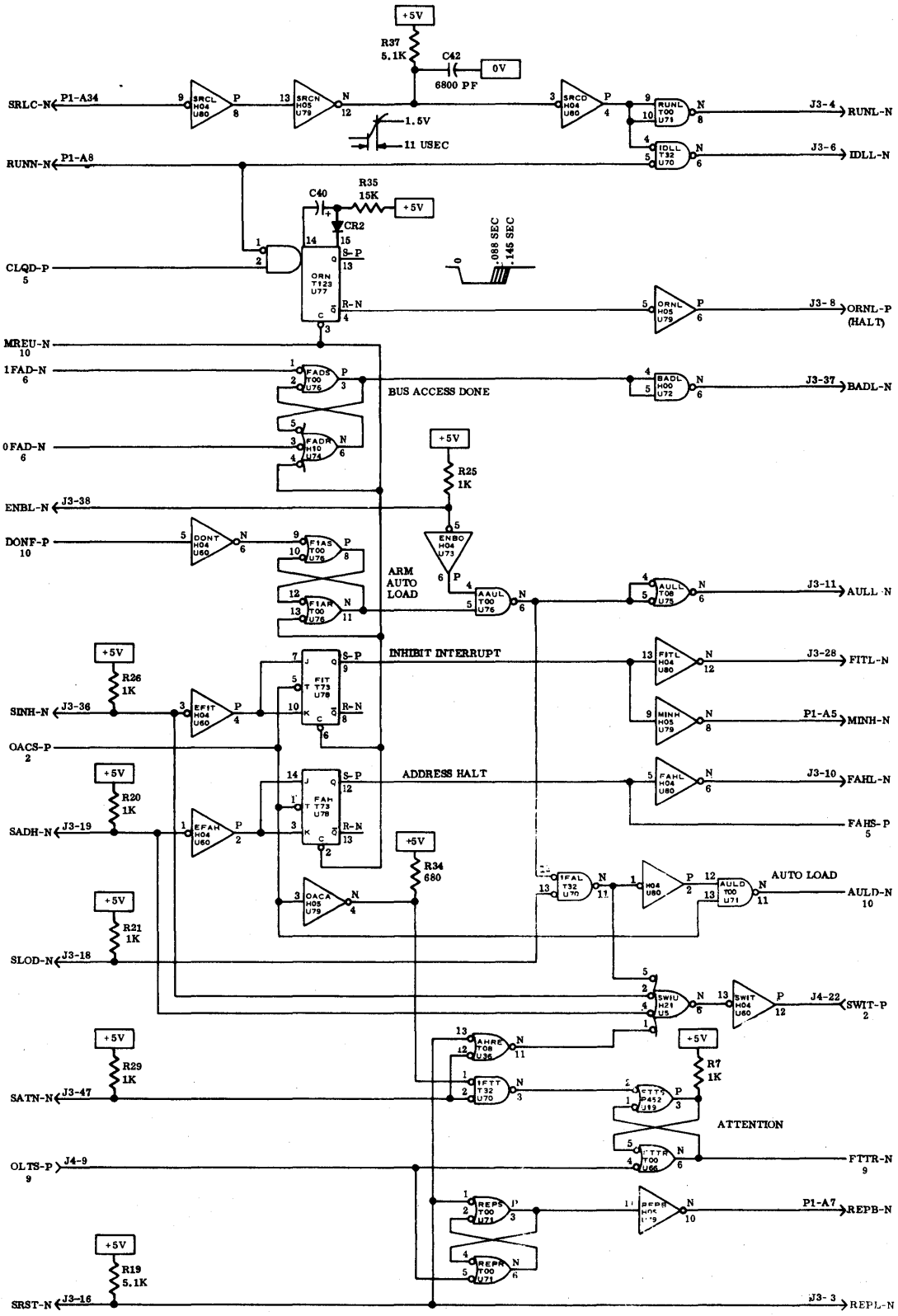


Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 2 of 10)

PBI

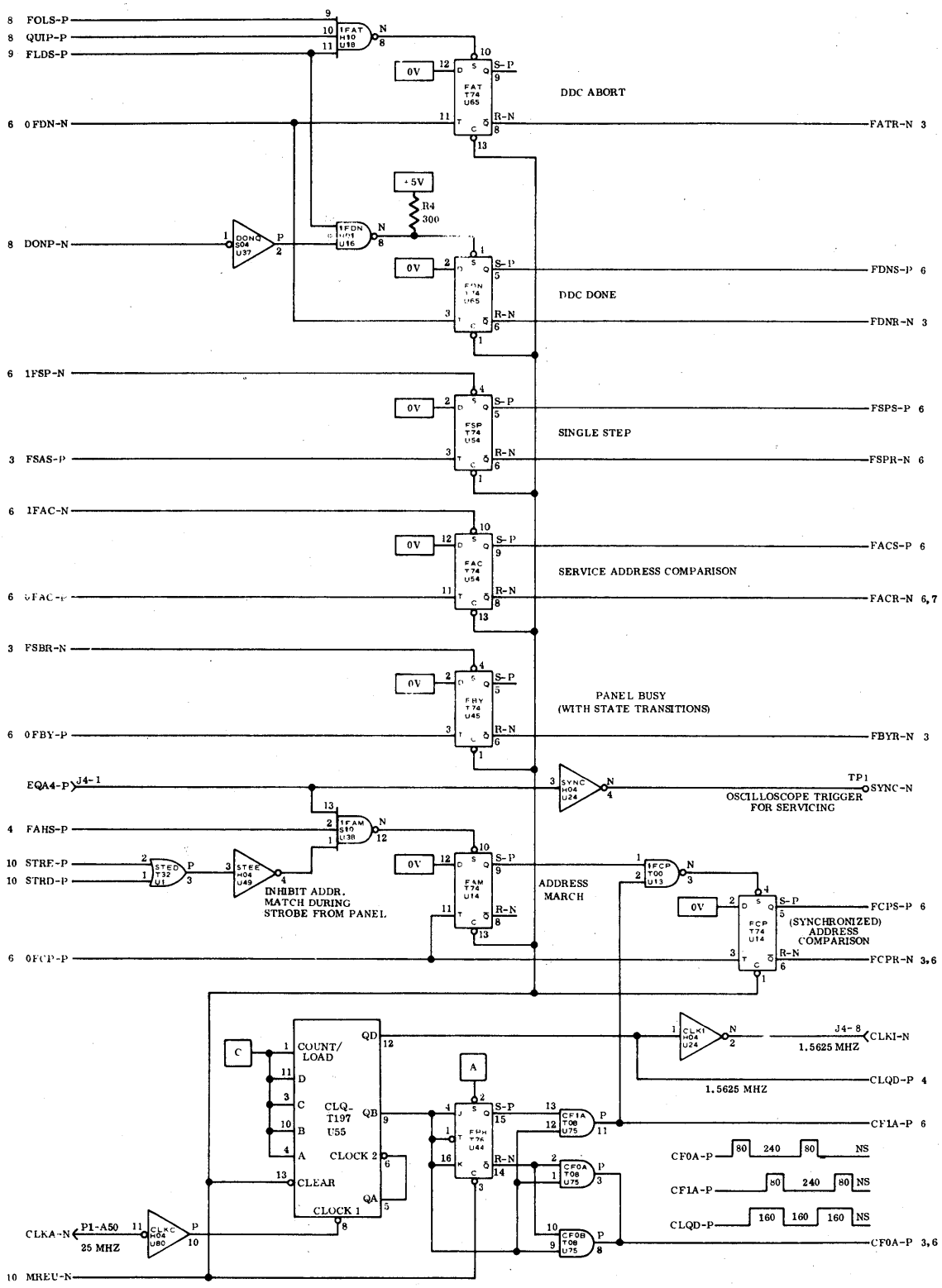


Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 3 of 10)

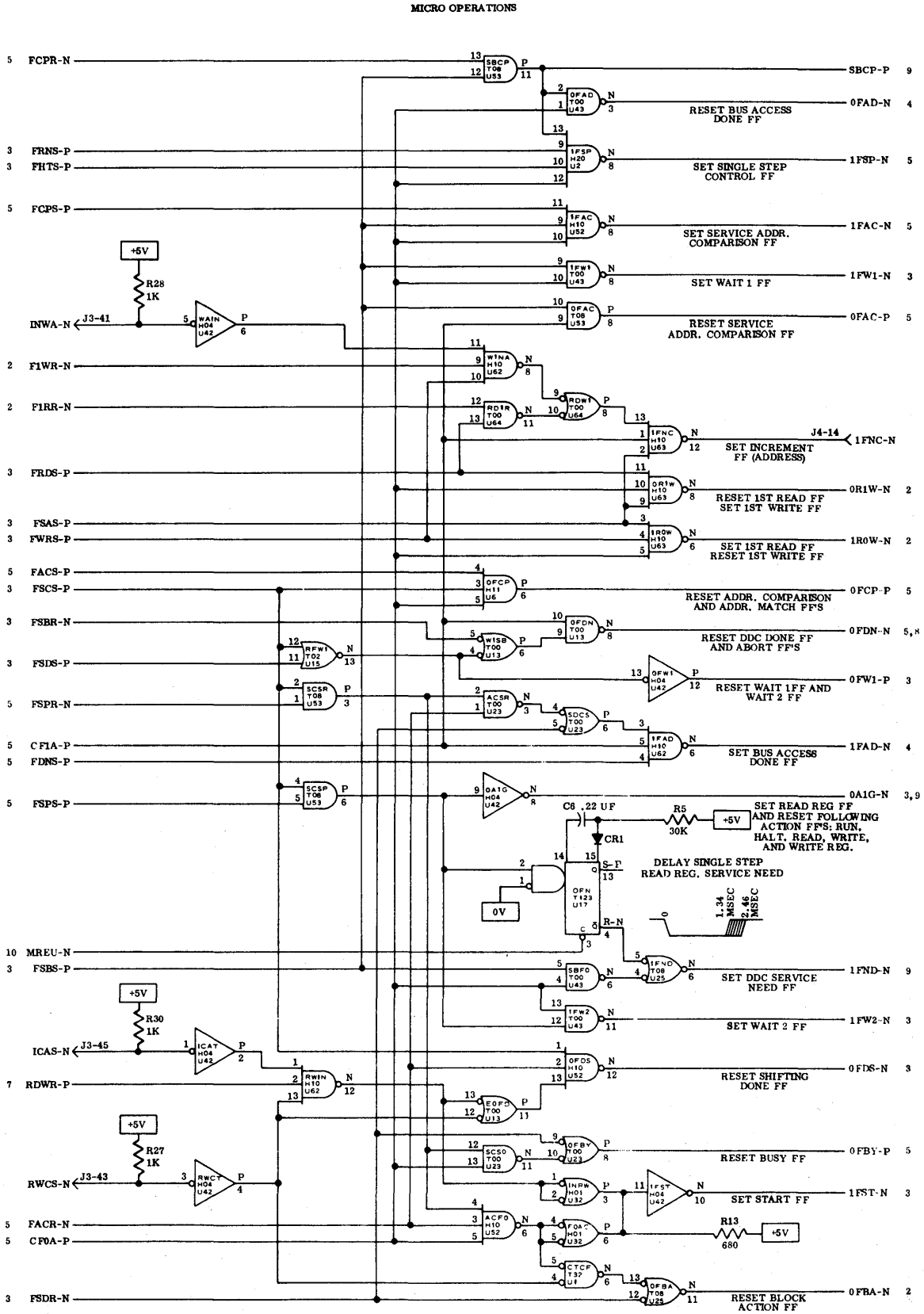


PBI

Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 4 of 10)

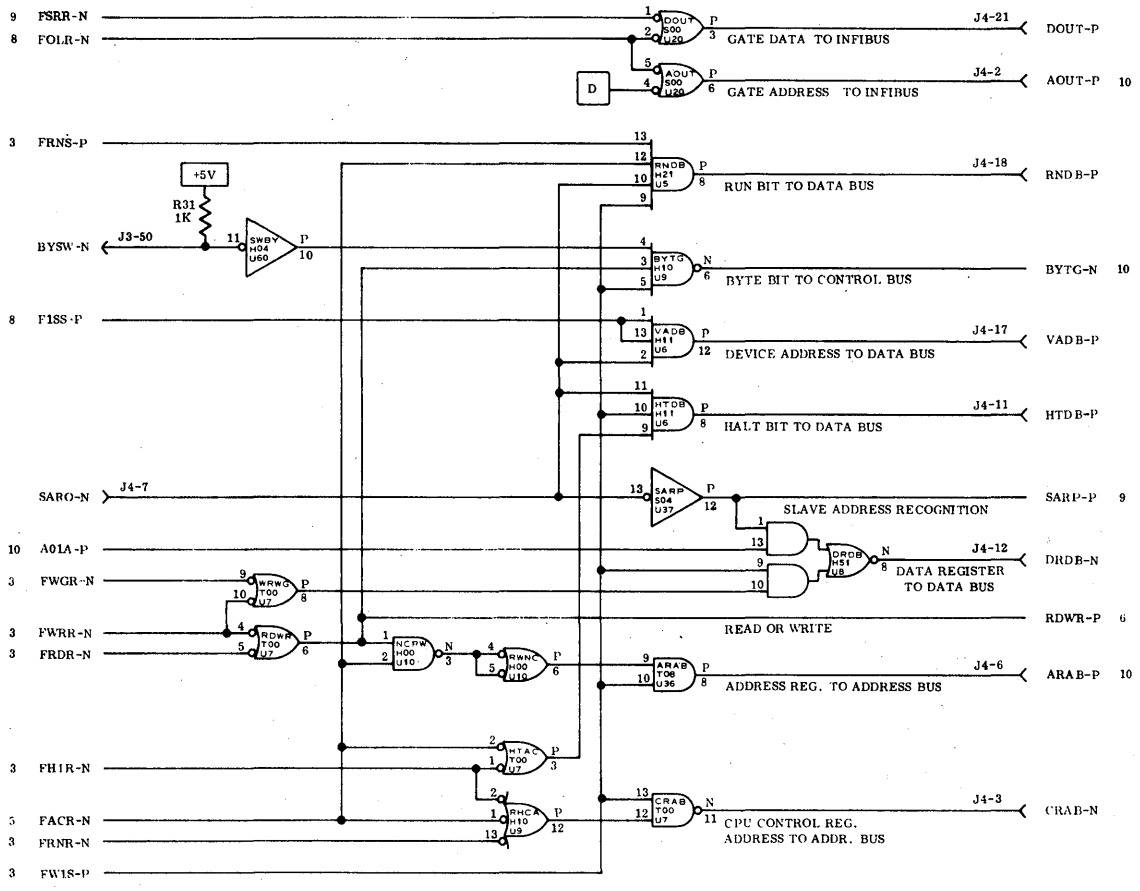


Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 5 of 10)



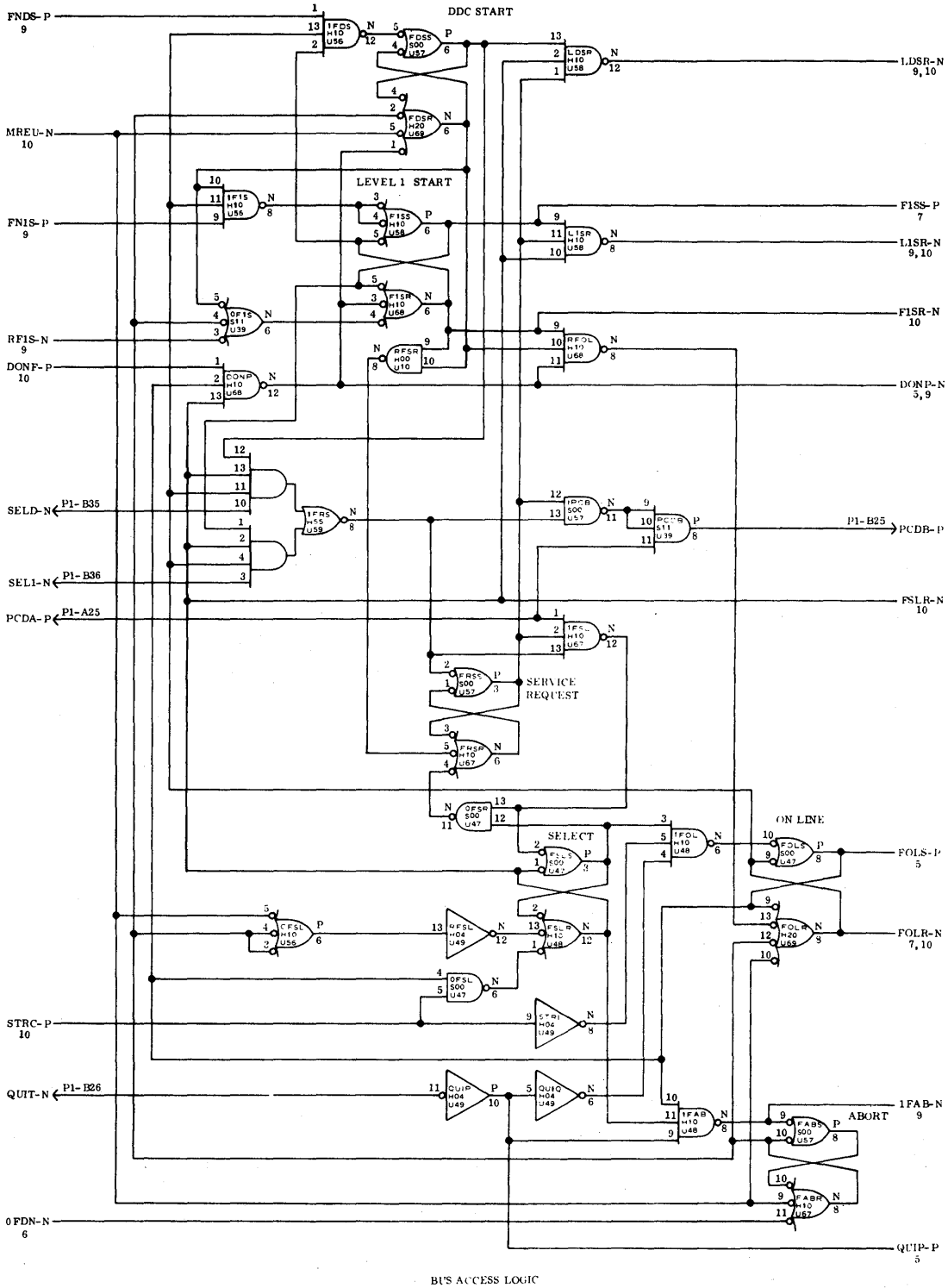
Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 6 of 10)

PBI



MICRO OPERATIONS

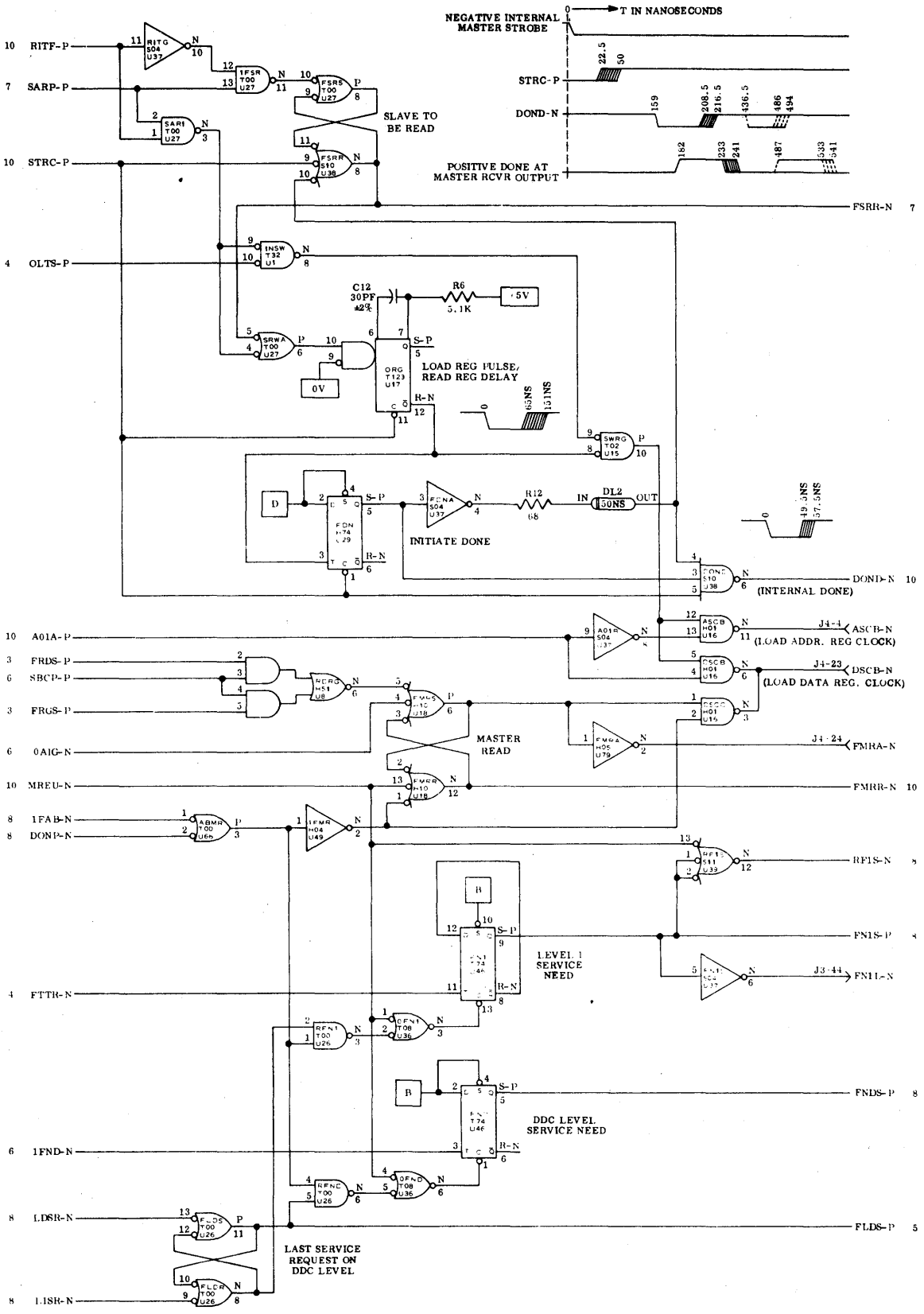
Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 7 of 10)



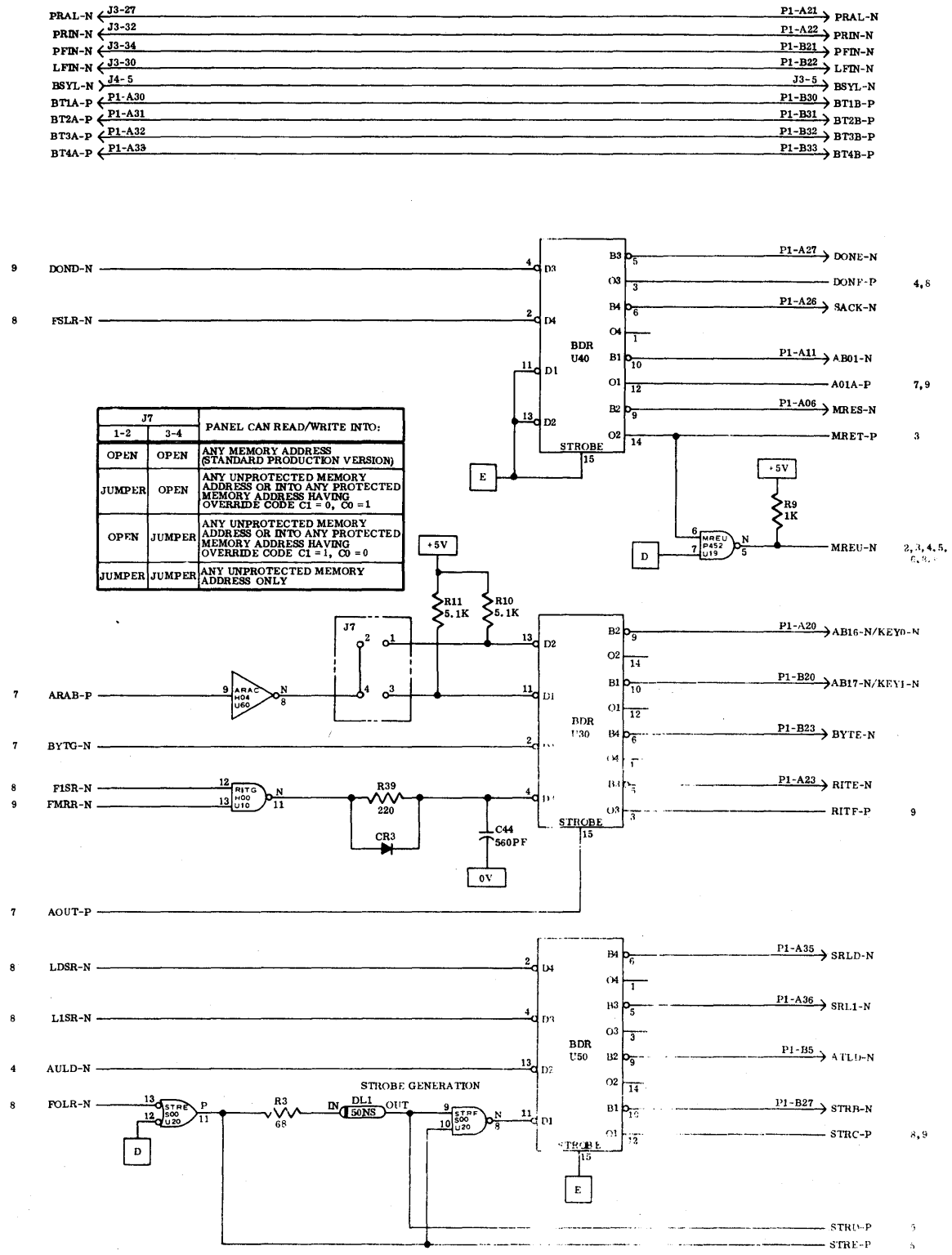
BUS ACCESS LOGIC

PBI

Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 8 of 10)



Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 9 of 10)



Panel Bus Interface Logic Diagram (PBI)
LD2001002165-1, Rev. C (Sheet 10 of 10)

PBI

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTE:			200
201		A/R	0001		LECP1049-17		MARK DASH NUMBER, REVISION LETTER AND SERIALIZE USING A FOUR DIGIT NUMBER STARTING WITH 0001 PRECEDED BY M (M0001).			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206		REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207		REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
210		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTE:			200
201		A/R	0001		LECP1049-17		MARK DASH NUMBER, REVISION LETTER AND SERIALIZE USING A FOUR DIGIT NUMBER STARTING WITH 0001 PRECEDED BY M (M0001).			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206		REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207		REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
210		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210

PB1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002178-1		SWB-CKT CARD ASSY		USED ON SUE 2220	1
002	F	065	0001		1005000837-1		LIGHT EMITTING DIODE		CR1 THRU CR17, CR19 THRU CR66	2
003		065	0001		RL07S271G		RESISTOR	MIL-R-22684/1	R1 THRU R34, R36 THRU R66 .5 IS	3
004		002	0001		T8201	86140	SWITCH, TOGGLE	CONTROL SWITCH	S70, 72	4
005		001	0001		T8206	81640	SWITCH, TOGGLE	CONTROL SWITCH	S71	5
6		000								6
007		001	0001		8001300311-2		CAPACITOR		C1 .8 IS	7
008		014	0001		1005000764-1		PIN, TERMINAL			8
009		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		9
010		001	0001		1001004842-1		PRINTED WRG BD, SWB			10

Parts List, Switch Panel (SWB)
PL2001002178-1, Rev. H (Sheet 2)

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTE:			200
201		A/R	0001		LECP1049-17		MARK DASH NUMBER, REVISION LETTER AND SERIALIZE USING A FOUR DIGIT NUMBER STARTING WITH 0001 PRECEDED BY M (M0001).			201
202		REF	0001				AREA TO BE FREE OF SOLDER AS SHOWN. (BOTH SIDES)			202
203		REF	0001				PRINTED CIRCUITRY SHOWN IS PHYSICALLY ON COMPONENT SIDE.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT .300.			205
206		REF	0001				LEAD PROTRUSION .075 MAXIMUM. (BOTH SIDES)			206
207		REF	0001				MODIFY SWITCH LEVER AS SHOWN.			207
208		REF	0001				LEDS (FIND NO. 2) TO BE IN LINE WITHIN .030.			208
209		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED FACE OF DRAWING, FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			209
210		REF	0001				HOLES NOTED ● SHALL HAVE NO SOLDER PROTRUSION ON COMPONENT SIDE.			210

Parts List, Switch Panel (SWB)
PL2001002178-1, Rev. H (Sheet 5)

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002177-1		PCB-CKT CARD ASSY		USED ON SUE 2220	1
002		001	0001		1001004841-1		PRINTED WRG BD, PCB			2
003	F	001	0001		8001800044-1		ICP		U42 (74H04)	3
004	F	001	0001		8001800049-1		ICP		U63 (74H21)	4
005	F	001	0001		8001800046-1		ICP		U29 (74H10)	5
006	F	001	0001		8001800072-1		ICP		U24 (7400)	6
007	F	004	0001		8001800074-1		ICP		U4,17,7,37 (7402)	7
008	F	001	0001		8001800043-1		ICP		U14 (74H01)	8
009	F	008	0001		8001800076-1		ICP		U5,15,25,35,45, 55,65,75 (7404)	9
010		000								10
011	F	001	0001		8001800045-1		ICP		U59 (74H05)	11
012	F	002	0001		8001800092-1		ICP		U27,44 (7451)	12
013	F	001	0001		8001800098-1		ICP		U22 (7473)	13
014	F	001	0001		8001800099-1		ICP		U33 (7474)	14
015	F	001	0001		8001800101-1		ICP		U32 (7476)	15
016	F	001	0001		8001800110-1		ICP		U12 (7493)	16
017	F	001	0001		8001800117-1		ICP		U11 (74150)	17
018	F	001	0001		8001800042-1		ICP		U54 (74H00)	18
019	F	001	0001		8001800081-1		ICP		U23 (7440)	19
020		009	0001		8001800123-1		ICP		U10,20,30,40,50, 60,70,80,39(BDR)	20
021	F	004	0001		1005000764-1		PIN, TERMINAL		NOTE 210	21
022	F	001	0001		8001803166-1		ICP		U72 (74154)	22
023	F	003	0001		8001803126-1		ICP		U9,34,79 (7408)	23
024	F	001	0001		8001803134-1		ICP		U13 (7425)	24
025		000								25
026	F	001	0001		8001803143-1		ICP		U74 (7486)	26
027	F	004	0001		8001803169-1		ICP		U6,16,26,36 (74157)	27
028	F	001	0001		8001803181-1		ICP		U62 (74175)	28
029	F	004	0001		8001803195-1		ICP		U8,28,58,78 (74198)	29
030		000								30
031		001	0001		SN75453P	01295	ICP	TEXAS INSTR INC	U2	31
032		000								32
033	F	003	0001		8001803155-1		ICP		U3,43,64 (74123)	33
034		004	0001		N8266B	18324	ICP	SIGNETICS	U46,56,66,76	34
035		001	0001		HD1-0165-5	34371	ICP	HARRIS SEMICOND	U52	35
036		005	0001		N8242A	18324	ICP	SIGNETICS	U47,57,67,69,77	36
037	F	001	0001		8001803204-1		ICP		U49 (74S15)	37

PB1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
038	E	007	0001		8001100001-1		DIODE		CR3,4,2,1,6,5,7 .5 IS	38
039		001	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R40 .5 IS	39
040		002	0001		RL07S562G		RESISTOR	MIL-R-22684/1	R11,12 .5 IS	40
041		004	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R20,29,42,44 .5 IS	41
042		005	0001		RL07S512G		RESISTOR	MIL-R-22684/1	R9,10,38,39,41 .5 IS	42
043		002	0001		RL07S911G		RESISTOR	MIL-R-22684/1	R13,16 .5 IS	43
044		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R33 .5 IS	44
045		001	0001		RL07S303G		RESISTOR	MIL-R-22684/1	R34 .5 IS	45
046		002	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R19,35 .5 IS	46
047		000								47
048		025	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R1,2,3,4,5,6,7, 8,14,15,17,18, 21,22,23,24,25, 26,27,28,30,31, 32,36,43 .5 IS	48
049		001	0001		RL07S153G		RESISTOR	MIL-R-22684/1	R37 .5 IS	49
050		001	0001		C932402	01295	SOCKET, RCPT	TEXAS INSTR INC	J4 (24 PIN)	50
051		000								51
052	F	027	0001		8001300101-1		CAPACITOR		C5,6,7,10,12,14, 15,16,17,18,20, 21,23,25,27,28, 29,30,33,34,35, 36,37,3,4,8,9 .25 IS	52
053		000								53
054		000								54
055		000								55
056		003	0001		8001300311-2		CAPACITOR		C13,38,26 .8IS	56
057		002	0001		8001300412-1		CAPACITOR		C1,2 .8 IS	57
058	F	001	0001		8001300015-1		CAPACITOR		C19 .1 IS	58
059		001	0001		192P2249R8	56289	CAPACITOR	SPRAGUE	C22 .8 IS	59
060		001	0001		DM-15-181J	72136	CAPACITOR	EL MENCO	C32 .25 IS	60
061		004	0001		DD-330	43543	INDUCTOR	NYTRONICS	L1,2,3,4 .5 IS	61
062	F	001	0001		8001600008-1		DELAY LINE, FIXED		DL1	62
063		001	0001		8001300333-2		CAPACITOR		C31 .8 IS	63
064		002	0001		CM05FD391J03		CAPACITOR	MIL-C-5/18	C11,24 .25 IS	64
065		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
066		REF	0001		LD2001002177-1		LOGIC DIAGRAM			66

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002165-1		PBI-CKT CARD ASSY		USED ON SUE 2220	1
002		001	0001		1001004807-1		PRINTED WRG BD, PBI			2
003		000								3
004	F	036	0001		8001300101-1		CAPACITOR		C1,2,3,4,C7 THRU C11,C13 THRU C39 .25 IS	4
005		003	0001		8001300311-2		CAPACITOR		C5,40,43 .8 IS	5
006		001	0001		CM05ED300G03		CAPACITOR	MIL-C-5/18	C12 .25 IS	6
007	F	001	0001		8001300015-1		CAPACITOR		C41 .1 IS	7
008	F	001	0001		8001300020-1		CAPACITOR		C42 .2 IS	8
009		001	0001		192P2249R8	56289	CAPACITOR	SPRAGUE	C6 .8 IS	9
010		001	0001		8001300065-1		CAPACITOR		C44 .25 IS	10
011		000								11
012		005	0001		RL07S512G		RESISTOR	MIL-R-22684/1	R6,10,11,19,37 .5 IS	12
013		002	0001		RL07S681G		RESISTOR	MIL-R-22684/1	R13,34 .5 IS	13
014		024	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R1,2,7,8,9,R14 THRU R18,R20 THRU R33 .5 IS	14
015		001	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R4 .5 IS	15
016		001	0001		RL07S153G		RESISTOR	MIL-R-22684/1	R35 .5 IS	16
017		001	0001		RL07S303G		RESISTOR	MIL-R-22684/1	R5 .5 IS	17
018		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R36 .5 IS	18
019		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R3,12 .5 IS	19
020		001	0001		RL07S221G		RESISTOR	MIL-R-22684/1	R39 .5 IS	20
021	F	002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	21
022		000								22
023		003	0001		8001100001-1		DIODE		CR1,2,3 .5 IS	23
024		000								24
025		010	0001		8001800072-1		ICP		U7,13,23,26,27,43,64,66,71,76 (74L00)	25
026	F	002	0001		8001800042-1		ICP		U10,72 (74H00)	26
027	F	001	0001		8001800074-1		ICP		U15 (7402)	27
028	F	001	0001		8001800075-1		ICP		U22 (7403)	28
029	F	006	0001		8001800044-1		ICP		U24,42,49,60,73,80 (74H04)	29
030	F	001	0001		8001800045-1		ICP		U79 (74H05)	30
031	F	011	0001		8001800046-1		ICP		U9,18,48,52,56,58,62,63,67,68,74 (74H10)	31
032	F	001	0001		8001800047-1		ICP		U6 (74H11)	32
033	F	002	0001		8001800048-1		ICP		U2,69 (74H20)	33

PBI

Parts List, Panel Bus Interface (PBI)
PL2001002165-1, Rev. D (Sheet 2)

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
034	F	001	0001		8001800049-1		ICP		U5 (74H21)	34
035	F	001	0001		8001800054-1		ICP		U8 (74H51)	35
036	F	001	0001		8001800058-1		ICP		U59 (74H55)	36
037	F	001	0001		8001800098-1		ICP		U78 (7473)	37
038	F	006	0001		8001800099-1		ICP		U3,14,45,46,54, 65 (7474)	38
039	F	003	0001		8001800123-1		ICP		U30,40,50 (BDR)	39
040	F	002	0001		8001800043-1		ICP		U16,32 (74H01)	40
041	F	001	0001		8001800101-1		ICP		U44 (7476)	41
042	F	003	0001		8001803198-1		ICP		U20,47,57(74S00)	42
043	F	005	0001		8001803126-1		ICP		U25,35,36,53,75 (7408)	43
044	F	001	0001		8001803202-1		ICP		U38 (74S10)	44
045	F	001	0001		8001803203-1		ICP		U39 (74S11)	45
046		004	0001		8001803137-1		ICP		U1,11,12,70 (7432)	46
047	F	002	0001		8001803121-1		ICP		U29,33 (74H74)	47
048	F	001	0001		8001803171-1		ICP		U34 (74161)	48
049	F	001	0001		8001803194-1		ICP		U55 (74197)	49
050		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U19	50
051	F	002	0001		8001803155-1		ICP		U17,77 (74123)	51
052	F	001	0001		8001803181-1		ICP		U4 (74175)	52
053	F	001	0001		8001803200-1		ICP		U37 (74S04)	53
054		000								54
055		001	0001		C932402	01295	SOCKET, RCPT	TEXAS INSTR INC	J4 (24 PIN)	55
056		000								56
057		000								57
058	F	005	0001		1005000764-1		PIN, TERMINAL		NOTE 210	58
059		000								59
060		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		60
061		REF	0001		LD2001002165-1		LOGIC DIAGRAM			61

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR PRODUCTION	2/6/73	

PBI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PBI TECHNICAL REF

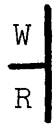
SIZE	CODE IDENT NO.	DRAWING NO.
A		PBI-05

SCALE	REV	SHEET
	A	1 OF 2

PBI - CONTROL PANEL-PANEL BUS INTERFACE Lockheed

see also PCB-Ø5, SWB-Ø5

Status - address none



Switches - none

Jumpers

Memory Protect Access (Assert Key Bits)

These jumpers will assert address lines 16 and 17 as tabulated below, during a control panel reference to memory space.

BIT	FROM	CONNECT TO 1	CONNECT TO Ø
16	J7-1	J7-2	-
17	J7-3	J7-4	-

PBI

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR PRODUCTION		
		B	ECN 294	4/26/78	E.L.

PBI

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PBI MODIFICATION STND

SIZE	CODE IDENT NO.	DRAWING NO.
A		PBI-15

SCALE	REV	SHEET
	B	1 OF 4

1. This applies to LEC PBI's of all revision levels.

2. Parts needed:

BBN #	QTY	ITEM
5	1	24-pin DIP socket (Augat)
130	1	CIT-10 TAG
181	1	6-32 X 1/4 nylon screw

3. Install plastic tag with board type and serial number.

4. Replace 24-pin DIP socket (J4) at notched end of the board with the 24-pin Augat socket. (See Figure 1)

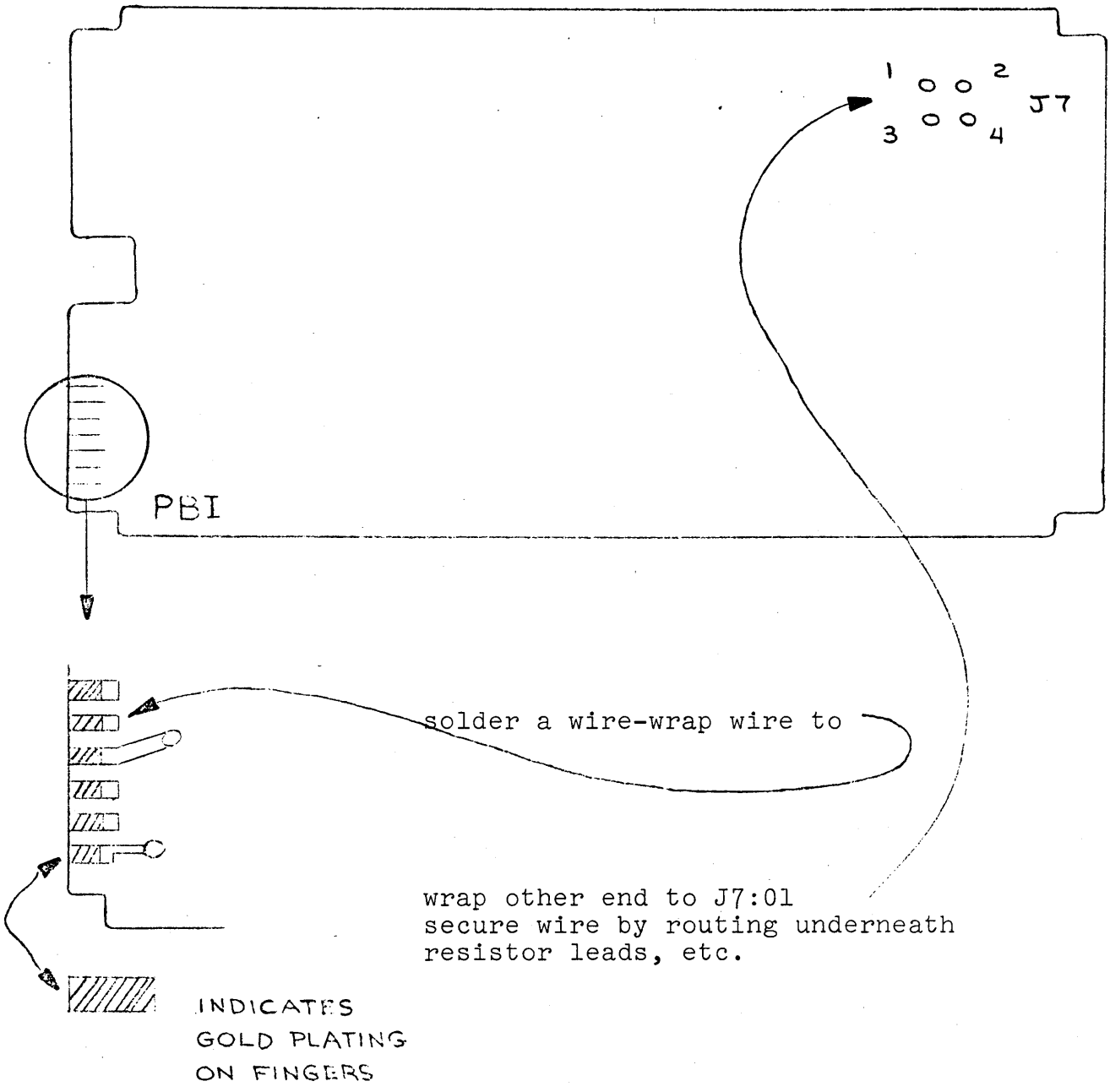
5. Solder a wirewrap wire to the right of the gold plating on the finger shown in Figure 1. Wirewrap the other end to J7:01 as shown.

6. The added wire allows selection of key bits for console references.

DETAIL

(see page 4 for Figure 1)

Fix to Console (1) on PBI cards



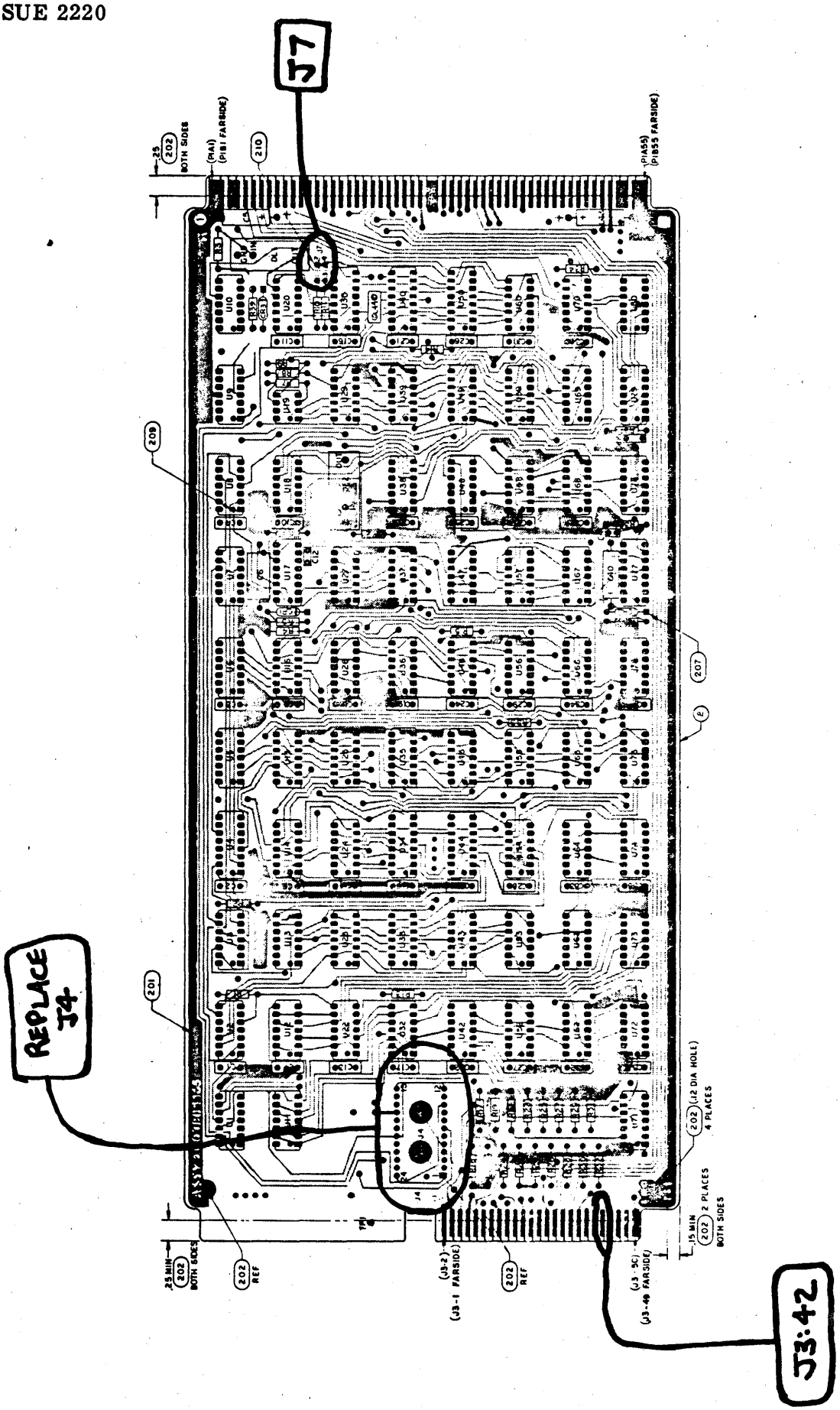
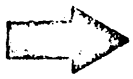


FIGURE 1

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		



SEE PBI-Ø2

PBI

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 11/8/75

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PBI SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		PBI-2Ø

SCALE	REV	SHEET 1 OF 1

Control Panel Board

PCB-Ø2 Logic Description

PCB-Ø5 Technical Reference

PCB-15 Assembly (Modification)

PCB-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE PBI-Ø2

PCB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL 12/12/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PCB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PCB - Ø2

SCALE	REV	SHEET 1 OF 1

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/6/75	

PCB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PCB TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		PCB-05

SCALE	REV	SHEET
	A	1 OF 2

PCB - CONTROL PANEL--CONTROL PANEL BOARD Lockheed

see also PCB-Ø5, SWB-Ø5

Status - Address none

W
R

Switches - none

Jumpers

Control Panel Address

Panel Number	Connector J5	Connector J6
1	--	--
2	--	1 to 2
3	1 to 2	--
4	1 to 2	1 to 2

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PROD. - ECN 294	4/26/78	

PCB

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN E. Cox

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE PCB ASSEMBLY (MODIFICATION)

SIZE	CODE IDENT NO.	DRAWING NO.
A		PCB-15

SCALE	REV	SHEET	OF
	A	1	3

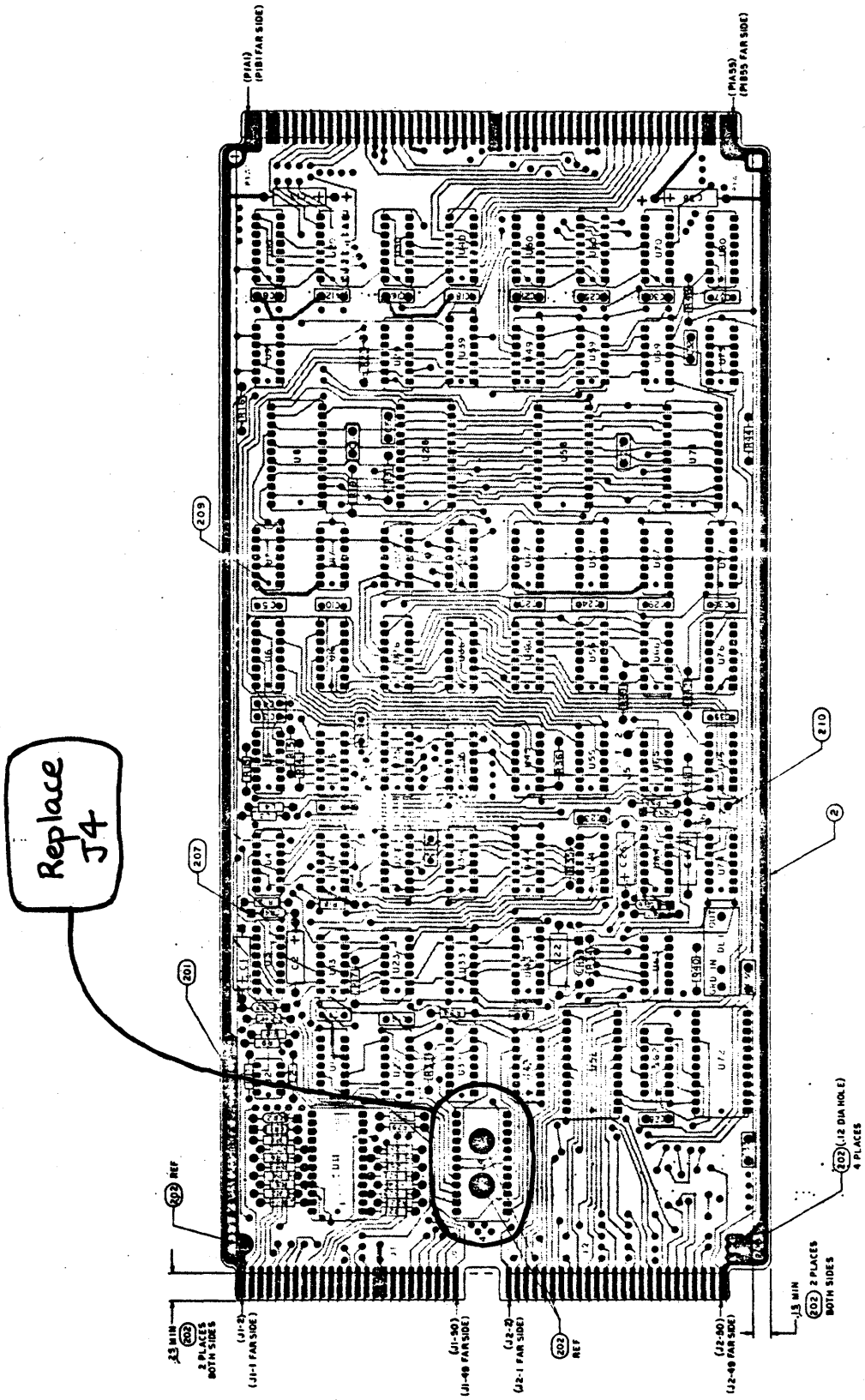
1. This applies to LEC PCB's of all revision levels.

2. Parts needed:

BBN #	QTY	ITEM
5	1	24-pin DIP socket (Augat)
130	1	CIT-10 TAG
181	1	6-32 X 1/4 nylon screw

3. Install plastic tag with board type and serial number.

4. Replace 24-pin DIP socket (J4) at notched end of the board with the 24-pin Augat socket. (See Figure 1)


Replace J4
(P1A1) (P1B1 FAR SIDE)
(P1A35) (P1B35 FAR SIDE)
209
207
201
210
2
202 REF
202 .12 DIA HOLE 4 PLACES
.13 MIN
202 2 PLACES BOTH SIDES
(J1-2) (J1-1 FAR SIDE)
(J1-50) (J1-49 FAR SIDE)
(J2-2) (J2-1 FAR SIDE)
202 REF
(J2-50) (J2-49 FAR SIDE)
.13 MIN
202 2 PLACES BOTH SIDES

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE PBI-Ø2

PCB

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL 12/15/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PCB SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		PCB-2Ø

SCALE	REV	SHEET 1 OF 1

Pseudo Interrupt Device

PID-Ø2 Logic Description

PID-Ø5 Technical Reference

PID-1Ø Assembly Drawing

PID-2Ø Schematics

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
B*	RELEASE FOR PRODUCTION	1-19-73	
C	ECN 0012	9-5-74	MFK
D	ECN 0218	7-21-76	

* PID-02 - PC RELEASED AT B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

PID

CONTRACT NO:

DRAFTSMAN JF

CHECKER

ENGINEER MFK

APP'D FOR REL MFK 12/11/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PID LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PID-02

SCALE	REV	SHEET
	D	1 OF 5

A

PID LOGIC DESCRIPTION

Address Recognition and Decode

The PID recognizes the following addresses:

FXY0Z where XY = E0, E8, F0, F8

and Z = 0 (R/W)

2 (R only)

4 (R/W)

The 20 address wires are received from the INFIBUS by BDRs. The low-order bit is ignored. ADC1 prevents recognition of Z=6. ADC6 prevents recognition of writing to Z=2. PIA11 and PIA12 are the switch-selected levels to choose X and Y. These are EX-ORed with AB11 and AB12 to produce ADC4 and ADC5. Thus ADCOM- is low when a satisfactory address is received.

STRB+ is delayed by an EX-OR gate (to allow for address decoding gating) and ANDed with HOLD- (i.e., prevent recognition until the fall of HOLD) to form CLKAD+ which clocks the ME flop. This flop is operated in an inverted manner; ME+ is true when the $\overline{Q}$ output is asserted, etc. ME+ is cleared by the fall of undelayed STRB+.

Since the priority tree takes some time to settle, a subsequent access to the PID must be delayed until the outputs are stable; thus, a timer (BUSY) is included. When ME+ comes true and BUSY is not true, a 60 ns timer (DODON) is started. This delays the beginning of DONET until the data on a READ has come back through the BDRs to the input logic (see Overview below). A 50 ns DONE pulse, whose trailing edge starts the BUSY timer (300 ns), is then produced.

Since processors cannot assert address bits 18 and 19, single-bus IMPs have a problem -- a processor must directly reference a device without an intervening bus coupler. Because devices expect these two bits to be true, they are never addressed, and therefore, the PID (which we posit to be always present, even in the smallest IMP) includes a switch (Single/Multiple Bus Control) to force these lines always true (low). Because the PID is always a slave, it need never

broadcast an address, hence the ENABLEs of the other BDRs are low.

Memory, Priority Tree, and Output

The 127 levels are stored in 16 Fairchild 9334 addressable latches, 8 bits to a latch (level 0 is always true). The outputs of these latches are numbered, e.g., F093 means ninth package, third level. Larger numbers are higher priority. The latches are operated inverted; a level is asserted if its output is low.

Associated with each latch is a 9318 priority tree which outputs the 3-bit number of the highest level asserted within that group (e.g., R124 means group 12, 14 bit). The Group Select output is asserted if any level within that group is true.

The Group Select outputs are in turn input to another pair of 9318s to determine the number of the highest priority group with a true level. If the Group Select of the high order 9318 is true, the desired level number is in groups 8-15 and the high order bit (bit 7) should be a one; therefore DB07X is taken directly from the GS output. The sense of this signal also determines the second level 9318s from which to take the rest of the group number;* therefore, DB07X switches the multiplexer which outputs DB04X-DB06X. These 4 bits of the group number are used by three multiplexers to select the 3 bits output by the priority tree of that group. These 3 bits are then used as the low order 3 bits of the output level.

The seven lines DB01X-DB07X contain the number of the highest priority level that is set. These are latched by the two 74175s at the trailing edge of BUSY, i.e., after any change has had a chance to propagate through the tree (CKLAT also latches the lines after a reset cycle, see below). The outputs of the latches go to the driver inputs of the data BDRs and to seven LEDs mounted on the rear edge of the board which displays the highest priority level set at any time.

*Since level 000 is forced true, we are assured that there is always a true level in the lower half.

Input

This section performs two functions: to address the correct latch in the memory and to provide the correct sense of the data to be inserted in that latch. The four high-order data bits drive a demultiplexer that enables the correct latch. The address within that latch is determined by data bits 1-3 which become PIL0-PIL2.

The data input to the latches is LDAT, which, driving normal accesses, is determined by SETPI. SETPI= (RITE • AB02) + AB01, giving the following truth table:

Z	R	W	
0	1	1	[write address]
2	0	no done	[read address]
4	1	0	[clear address]

Thus a READ to the read address or a WRITE to the clear address clears that latch; a WRITE to the write address sets it. A READ to either of the addresses which are normally WRITten to causes LDAT to be true, i.e., reset the highest set level (don't change anything). These addresses must be recognized to allow for the early processors' prefetch before a MOVE to memory.

LDAT and the PILs are buffered (e.g., PIL0- becomes PIL0A+ and PIL0B+) to drive the necessary load.

PID

Reset

Since the latches are operated inverted, the proper reset condition (no levels on) is with all latches set; thus the usual CLEAR inputs will not suffice. Instead, the occurrence of MRES sets the RES flop to begin a reset cycle. RES switches the multiplexers which determine the PILs and LDAT from bus data to a counter driven by CLKA, the 25 MHz bus clock. LDAT is held to zero and the enable demultiplexer is always enabled; thus the PILs will cycle through all values, setting each latch to logical zero. When the counter overflows, RSDON clears RES.*

Overview

On a WRITE operation to the write address, the address is recognized and ME is set. While the DODON delay is running, the data bits (i.e., the level to be set) are propagating to the enable demultiplexer and the address inputs on the latches. LDAT also is being set properly. When DONET fires, the proper latch is enabled and LDAT is strobed in. The receipt of DONE by the originating master will cause him to remove the data bits from the bus and lower STRB, which resets ME. BUSY prevents any subsequent access until the worst-case new information can propagate through the priority tree and be captured in the output latches.

On a READ operation to the read address, the address is recognized and ME is set. Since RITE is false, DREN will be true while ME is true. Thus the highest level set (captured in the output latches on the previous access) is output to the bus. While DODON is running, the transmitted data is being received by the BDRs and routed to the demultiplexer and address inputs on the latches. When DONET pulses, indicating to the originating master that the data on the bus is valid, the demultiplexer is enabled, causing that latch to be cleared (LDAT=0). The cycle ends and BUSY works in the same way as for a WRITE.

A WRITE operation to the clear address works just as it would to the write address, except that LDAT=0, so the addressed latch is cleared rather than set.

---

*In fact, since RES is long (50 ms.) about 500 RES cycles will take place.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	1-19-73	
B	ECN 0387	6/11/79	

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

PID

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER MFL

APP'D FOR REL MFK 12/4/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PID TECHNICAL REF

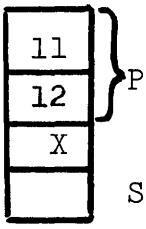
SIZE	CODE IDENT NO.	DRAWING NO.
A		PID-05

SCALE	REV	SHEET
	B	1 OF 3

PID - PRIORITY INTERRUPT DEVICE BBN

Status - address none

Switches



PID address

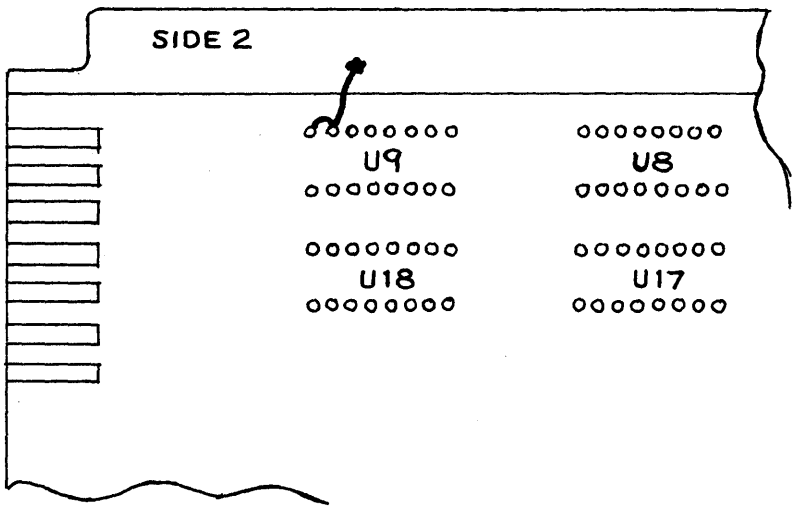
Single/Multiple BUS Set=Single

Jumpers - none

PID

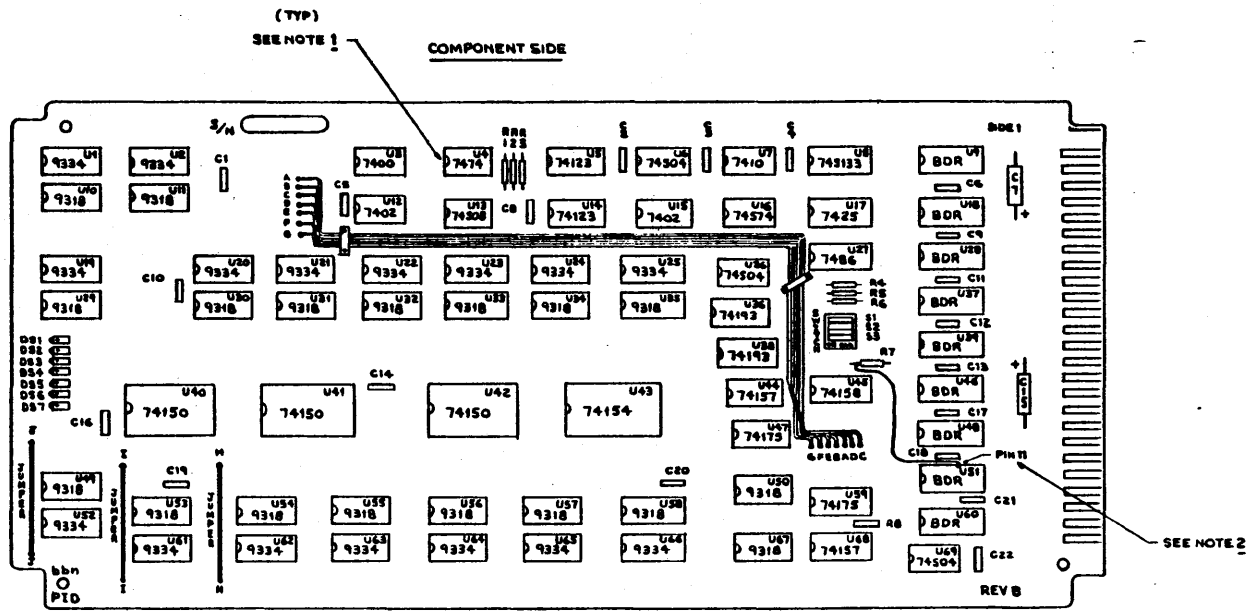
"F" STICKING PROCEDURES, FOR SINGLE BUS MACHINES

Solder wire to ground (FOIL PATH THAT HAS "SIDE 2" ETCHED IN IT), then to pins 9 & 10 of bug. Bug coordinates (FROM FRONT-SIDE---BUG SIDE---OF CARD): U 9.



PID-1Ø ASSEMBLY DRAWING

REVISION			
APPD	SYM	DESCR	DATE
MFK	B	REL. PROD	6/22/76
MFK	C	ECN #0012	8.24.76
DRF	D	ECN #0237	1.22.77
ER	E	ECN #286	9.19.78



COMPONENT VALUES

C1-C6, C8-C14, C16-C22 = .1mfd CERAMIC DISC
C7, C15 = 220 mfd - 10 VOLT ELECTROLYTIC
R1 = 7.5 K Ω — 1/4 W - 10%
R2, R4, R5, R6 = 5.1 K Ω
R3 = 51 K Ω
R7, R8 = 1.0 K Ω
DS1 - DS7 = DIALCO # 555-2007

NOTES

1 - NOTCH SHOWN IN BUGS, INDICATES INSERTION DIRECTION.

2 - SOLDER 30 AWG W.W. WIRE FROM THE LEFT END OF R7 INTO THE HOLE USED BY THE IC LEAD AT U55:11

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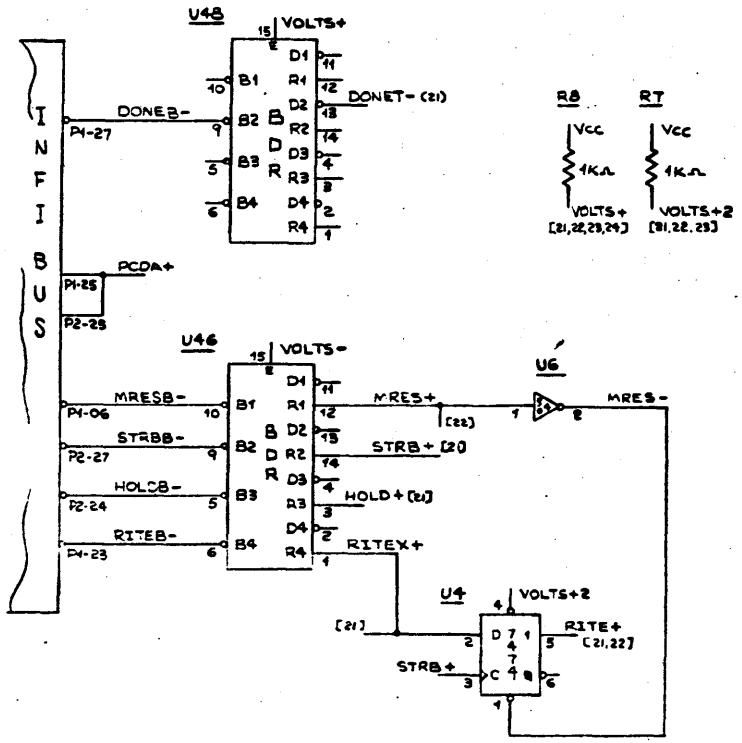
CAMBRIDGE MASS 02138

DRAWN	DRF	6/78	TITLE: PID PC LAYOUT	
CHECKED	DRF	6/78	CUSTOMER NO. HSMIMP	DWG NO. PID-10-PC	REV. E
APPROVED	MFK	6/78		

PID

PID-2Ø SCHEMATICS

	REVISION		
APPD	SYM	DESCR	DATE
	B	REL PROD	6-25-73
	C	ECN# 0012	9.30.73



COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
DRAWN	DRF	5/30/73	TITLE	PID CONTROL	
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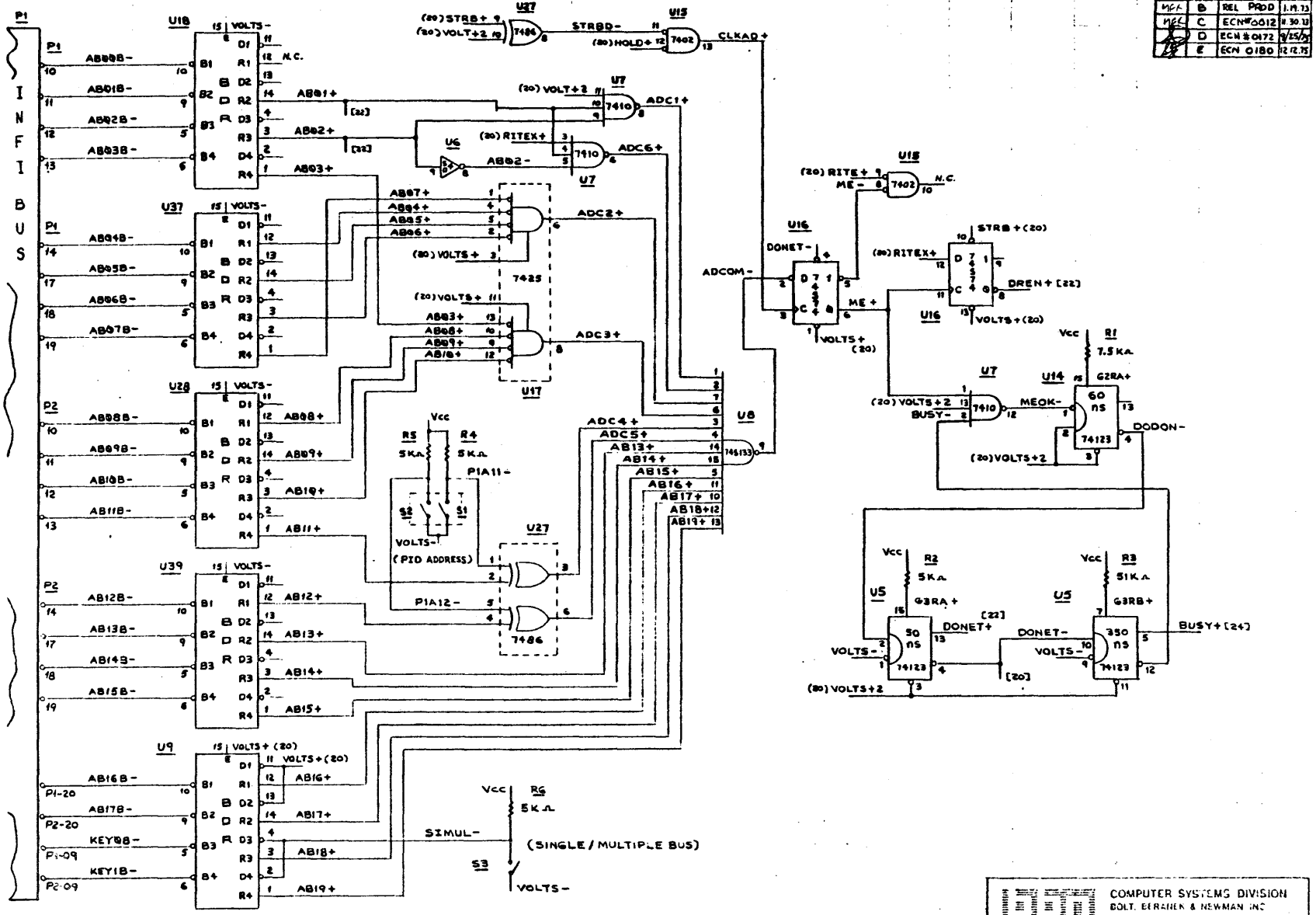
APPROVED		6/2/73	HSMIMP	PID-20-PC	C

PID



REVISION			
APPD	SYM	DESCR	DATE
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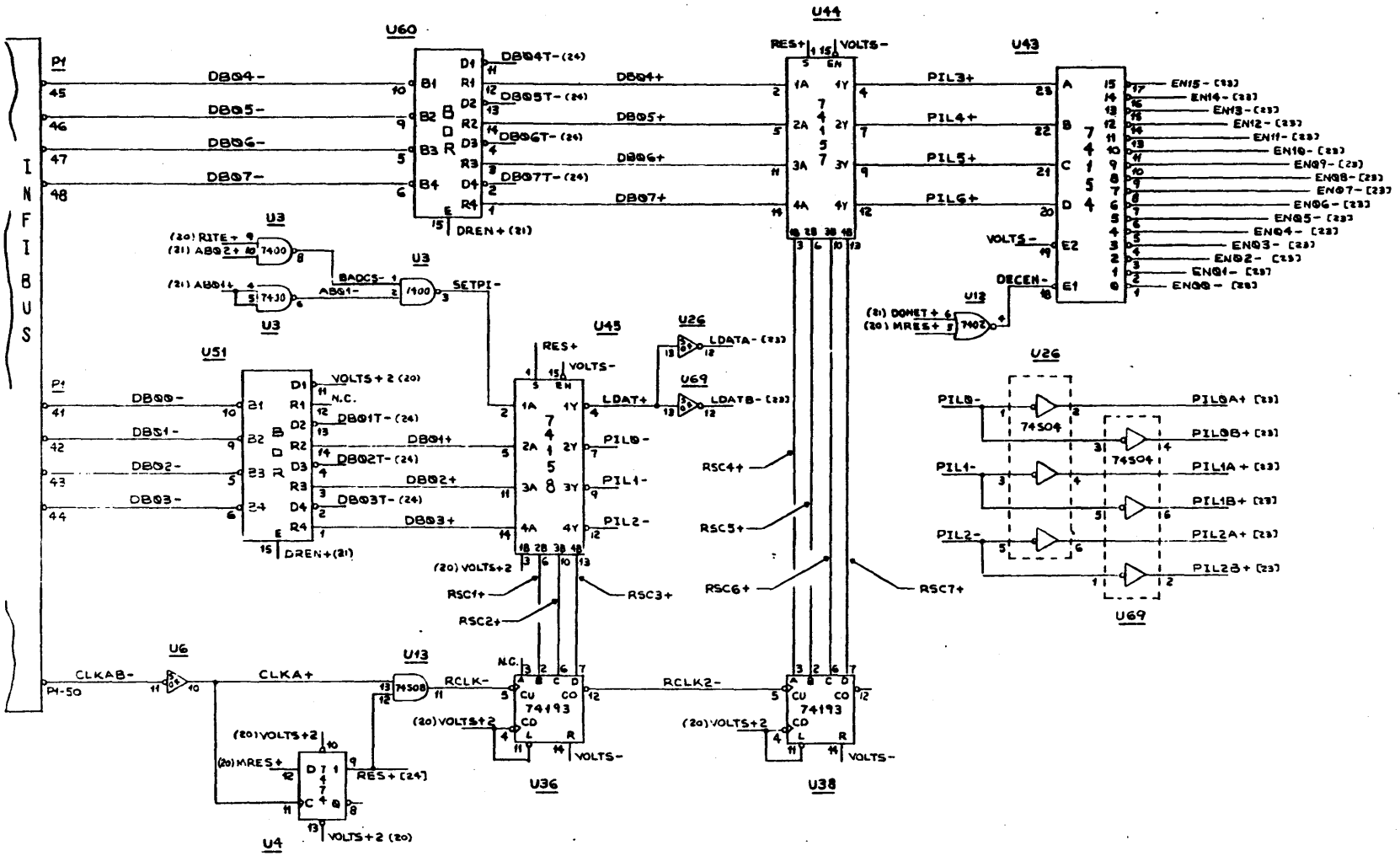
MFK	C	ECN#0012	11-30-73
	D	ECN #0172	9/25/74
	E	ECN 0180	12-12-75

BBN COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	D.R.F.	1-19-73	TITLE: PID ADDRESS & DECODE
CHECKED	DRF	1-19-73	CUSTOMER NO: HSMIMP
APPROVED	MFK	1/28/73	DWG NO: PID-21-PC
			REV: E

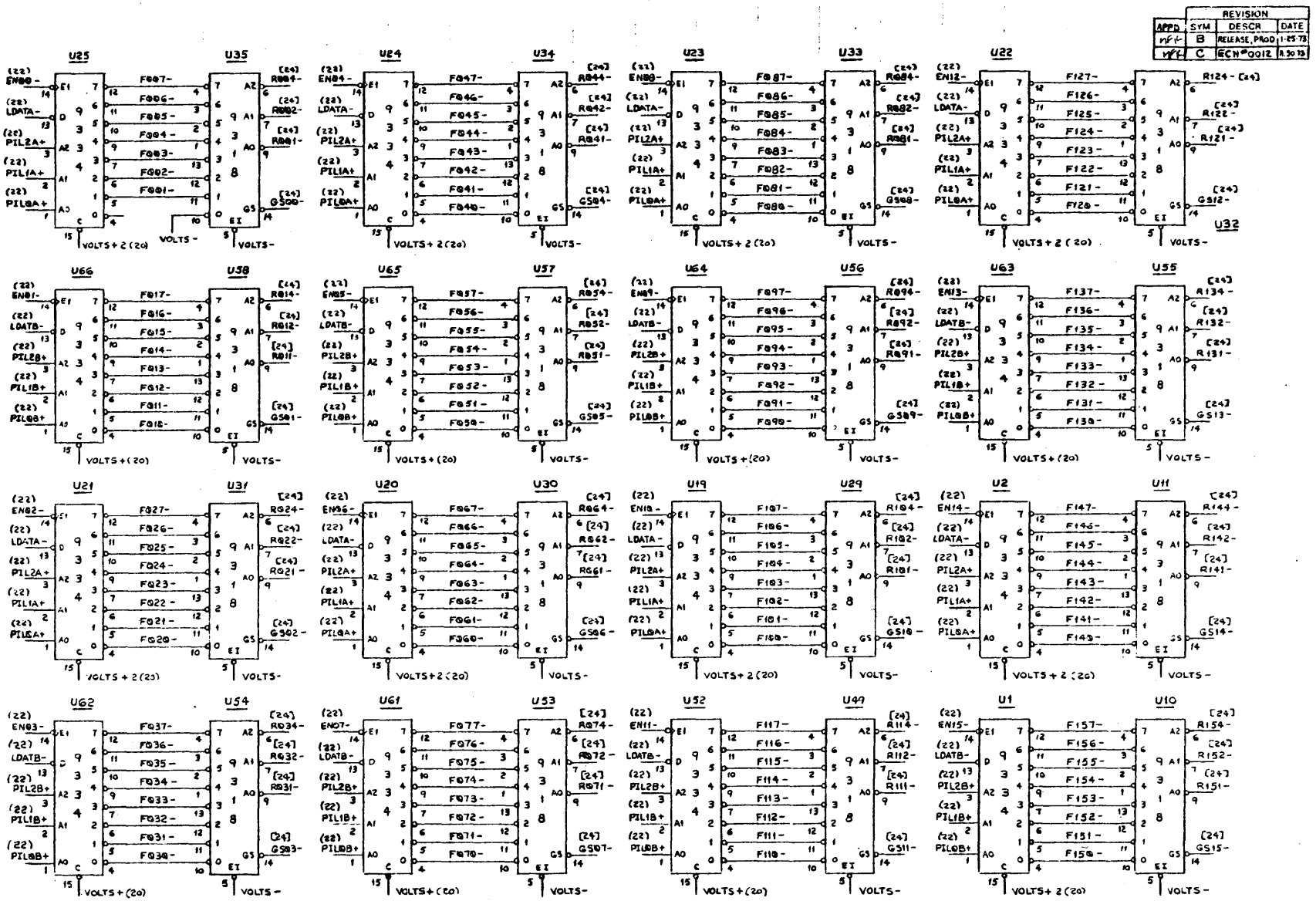


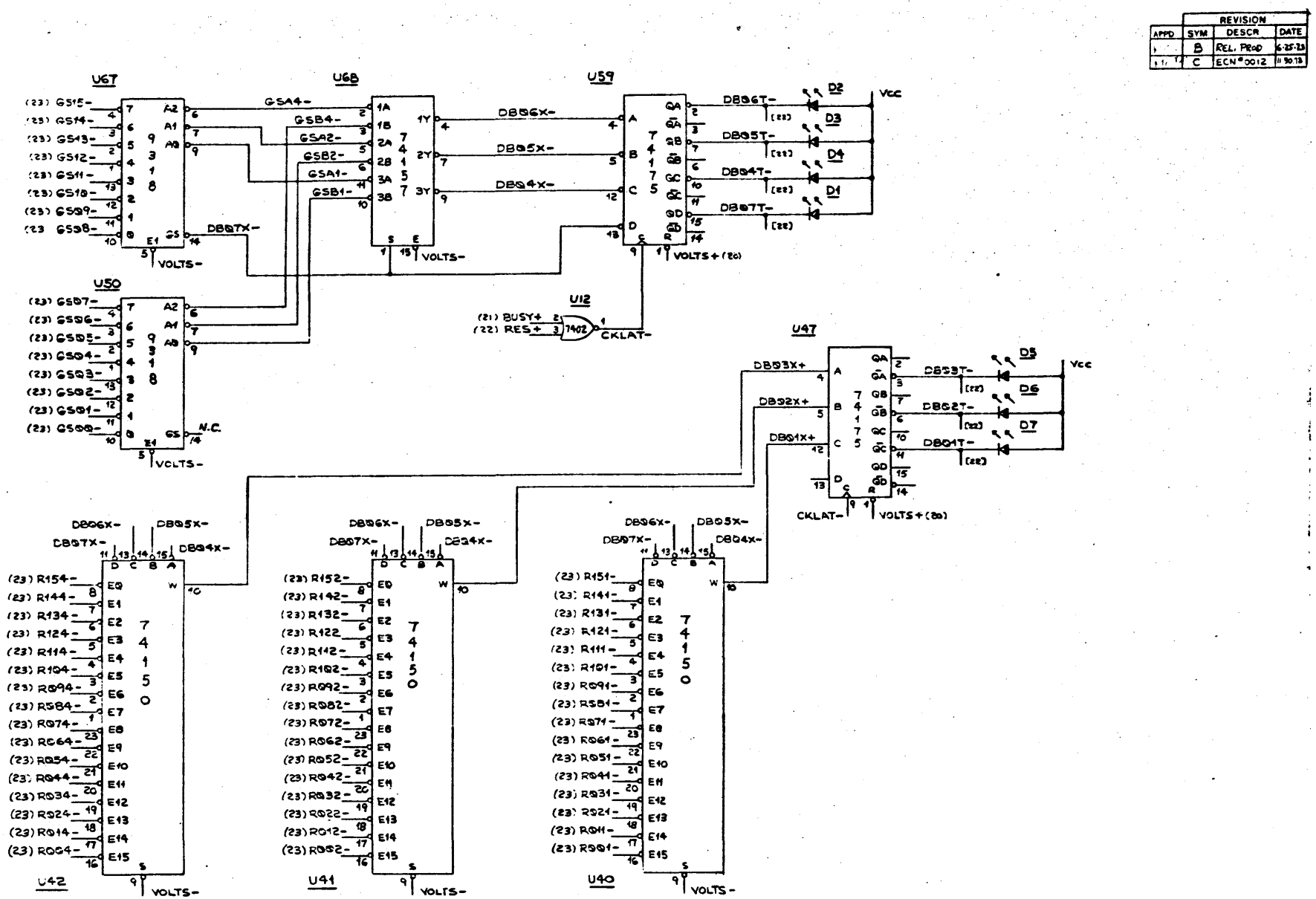
	REVISION		
APPD	SYM	DESCR	DATE
MFK	B	REL. PROD	4.25.73
MFK	C	ECN #0012	4.30.73
[illegible]	D	ECN #0043 ECN #0152	7.31.73
[illegible]	E	ECN 0180	12.12.73

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	5/24/73	TITLE: PID INPUT & RESET
CHECKED	DRF	5/29/73	
APPROVED	MFK	5/29/73	CUSTOMER NO: HSMIMP; DWG NO: PID-22-PC; REV: E

PID


REVISION
APPD | SYM | DESCR | DATE
MFK | B | RELEASE, PROD | 1-25-73
MFK | C | ECN #0012 | 1-30-73
U25 U35 U24 U34 U23 U33 U22 U32
U66 U38 U65 U37 U64 U36 U63 U55
U21 U31 U20 U30 U19 U29 U2 U11
U62 U54 U61 U53 U52 U49 U1 U10
VOLTS+2(20)
VOLTS-
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN DRF 1/25/73
CHECKED DRF 1/25/73
APPROVED MFK 1/31/73
TITLE
PID MEMORY
CUSTOMER NO HSMIMP
DWG NO PID-23-PC
REV C


REVISION
APPD | SYM | DESCR | DATE
B | REL. PROD | 6-25-73
C | ECN #0012 | 11-30-73
U67
U68
U59
U50
U12
U47
U42
U41
U40
(23) GS15-
(23) GS14-
(23) GS13-
(23) GS12-
(23) GS11-
(23) GS10-
(23) GS09-
(23) GS08-
GSA4-
GSB4-
GSA2-
GSB2-
GSA1-
GSB1-
DB07X-
DB06X-
DB05X-
DB04X-
DB03X+
DB02X+
DB01X+
DB06T-
DB05T-
DB04T-
DB07T-
DB03T-
DB02T-
DB01T-
D2
D3
D4
D1
D5
D6
D7
Vcc
VOLTS-
VOLTS+ (20)
(21) BUSY+
(22) RES+
7402
CKLAT-
N.C.
(23) GS07-
(23) GS06-
(23) GS05-
(23) GS04-
(23) GS03-
(23) GS02-
(23) GS01-
(23) GS00-
(23) R154-
(23) R144-
(23) R134-
(23) R124-
(23) R114-
(23) R104-
(23) R094-
(23) R084-
(23) R074-
(23) R064-
(23) R054-
(23) R044-
(23) R034-
(23) R024-
(23) R014-
(23) R004-
(23) R152-
(23) R142-
(23) R132-
(23) R122-
(23) R112-
(23) R102-
(23) R092-
(23) R082-
(23) R072-
(23) R062-
(23) R052-
(23) R042-
(23) R032-
(23) R022-
(23) R012-
(23) R002-
(23) R151-
(23) R141-
(23) R131-
(23) R121-
(23) R111-
(23) R101-
(23) R091-
(23) R081-
(23) R071-
(23) R061-
(23) R051-
(23) R041-
(23) R031-
(23) R021-
(23) R011-
(23) R001-
7 4 1 5 0
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 5/29/73
CHECKED DRF 5/24/73
APPROVED MFK 6/25/73
TITLE P I D OUTPUT
CUSTOMER NO HSMIMP
DWG NO. PID-24-PC
REV C

PID

Peripheral Parallel Buffer

PPB-Ø2 Logic Description

PPB-Ø5 Technical Reference

PPB-14 Special Modification

PPB-15 Standard Modification

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/19/75

CHECKER

ENGINEER 7 5 12 '9

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PPB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PPB - Ø2

SCALE	REV A	SHEET OF

PPB

SUE 4601 INPUT/OUTPUT HIGH SPEED PAPER TAPE CONTROLLER MAINTENANCE BULLETIN M4601

PPB

CONTENTS

LIST OF ILLUSTRATIONS

PPB

LIST OF TABLES

PREFACE

This Maintenance bulletin contains a detailed description of the SUE 4601 Input/Output High-Speed Paper Tape Controller. Information in this bulletin is written primarily for system user and maintenance personnel with backgrounds in digital systems. Read Reference bulletin R4601 for a general description of this module and SUE General System Bulletins for background information.

SUE 4601 INPUT/OUTPUT HIGH SPEED PAPER TAPE CONTROLLER MAINTENANCE BULLETIN M4601

INTRODUCTION

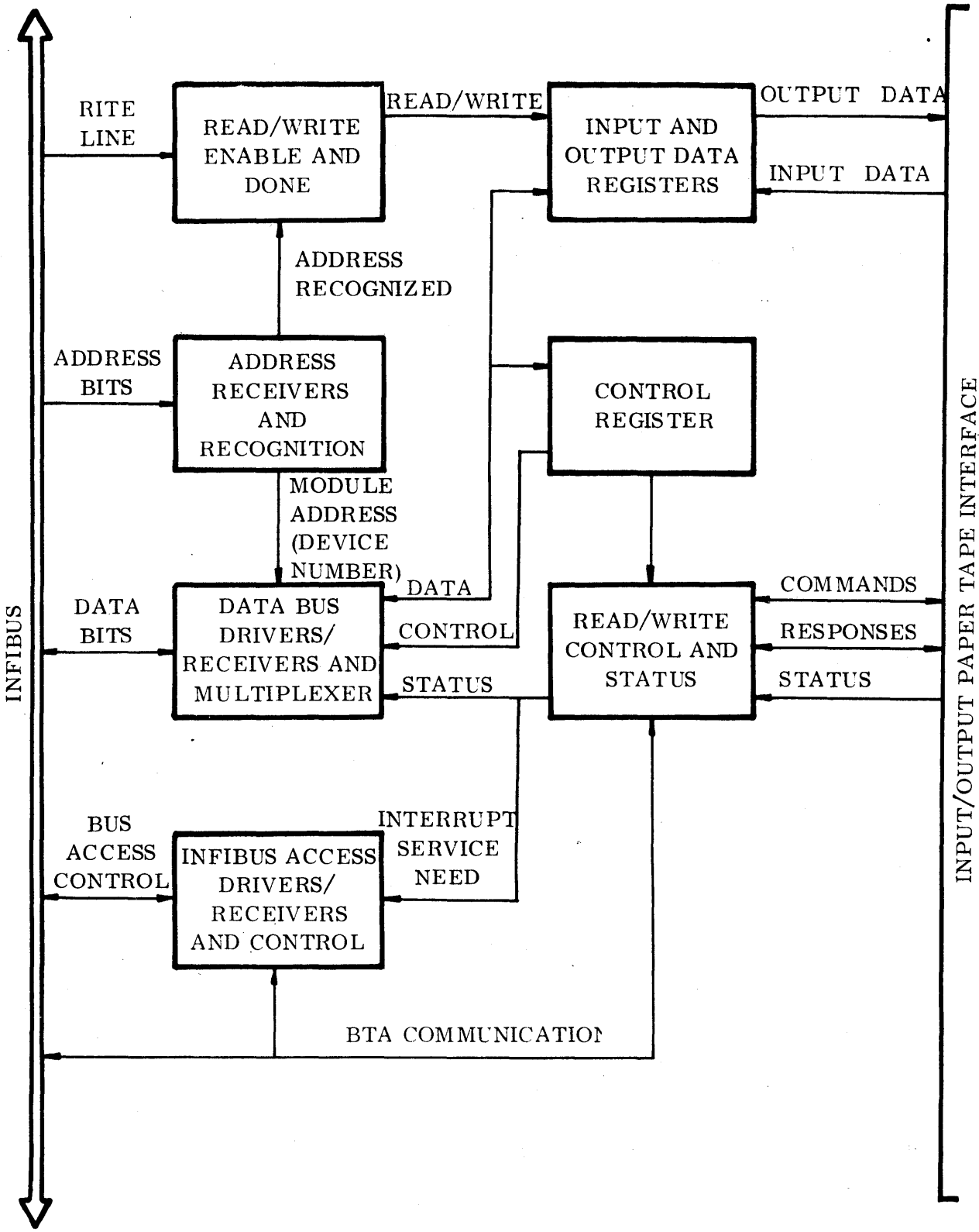
SUE 4601 Input/Output (I/O) High Speed Paper Tape (HSPT) Controller interfaces with HSPT devices using TTL high-true logic for both input and output data, and is capable of half-duplex operation. Using the basic SUE 4501 controller module, SUE 4601 is configured by jumpers to interface with one paper tape reader and/or one paper tape punch of the following equipment:

SUE Peripheral Device Model Number	Corresponding SUE Maintenance Bulletins
6714 High-Speed Paper Tape Reader with Spoolers	M4601, M6714/6715
6715 High-Speed Paper Tape Reader without Spoolers	M4601, M6714/6715
6716 High-Speed Paper Tape Punch	M4601, M6716
6719 High-Speed Paper Tape Reader-Punch	M4601, M6719

Maintenance bulletins in the 6700 series contain descriptions unique to each peripheral device.

Figure 1 is a general block diagram of the SUE 4601 HSPT Controller. The seven blocks in the diagram represent functional logic groups that operate to receive and transmit input and output data between the INFIBUS and HSPT equipment. Paragraphs following define each functional logic group.

PPB



4601-M01-72

Figure 1. SUE 4601 High Speed Paper Tape Controller, General Block Diagram

DATA BUS DRIVERS/RECEIVERS AND MULTIPLEXER

Interfaced with the INFIBUS data lines, the data bus drivers/receivers transmit and receive I/O data bi-directionally. Data received for output is applied directly to the output data register. Data for input is selectable by the data bus multiplexer for transmission on the INFIBUS data lines. One of four information types can be selected for input: read data from the device, control register contents, device and controller status, and controller address (same as device number).

INPUT AND OUTPUT DATA REGISTERS

Two data registers are contained in the controller: one for input, the other for output. Each register temporarily holds eight I/O data bits for transmission between the INFIBUS and the I/O device. Both registers are addressed indentically; therefore, the input data register cannot be written by a master module, and the output data register cannot be read.

CONTROL REGISTER

The control register can hold up to six control bits loaded from the six least-significant bits of the data bus. Three control bits are decoded and used to activate read/write/interrupt control functions. The control register contents can be input through the data bus multiplexer by a Read Control Register operation.

READ/WRITE CONTROL AND STATUS

The read/write control logic sends I/O commands to the device, receives device responses, and handles read or write control functions in the controller. One status bit is used for Read timing error or no ata read after 300 milliseconds. One device-not-ready status bit is used for each paper tape read or write device. Device-not-ready status bits are not stored in the controller but are d-c signals that indicate operational condition. All status is available for input by a Read Status Register operation.

PPB

INFIBUS ACCESS DRIVERS/RECEIVERS AND CONTROL

The INFIBUS access drivers/receivers transmit and receive the INFIBUS control signals commonly used in the SUE system to control system module communication. Controller bus access logic, the type implemented in most SUE modules, initiates interrupt service requests when a service need is indicated, and communicates with the bus controller during selection for bus access.

ADDRESS RECEIVERS AND RECOGNITION

The address receivers and recognition logic are implemented to receive and recognize the controller register addresses from the INFIBUS address lines. Recognizing one of the controller register addresses initiates either a read or write operation according to the logic state of the RITE line at the time of recognition. Part of the recognition logic is used to encode the controller address that is placed on the data bus during a bus service cycle. The address placed on the data bus is used to identify the controller during the subsequent system interrupt.

READ/WRITE ENABLE AND DONE

Read/write enable logic activates either the read or write mode according to the logic state of the INFIBUS RITE line. A delay line associated with this logic ensures that data is transferred after the data lines have settled. The delay line terminates in the Done logic to signal the end of a read or write operation.

INSTALLATION CONSIDERATIONS

SUE 4601 Paper Tape Controller can be installed from the insertion side of the chassis in any slot to the left of the bus controller, considering priority for bus access. Module priority relative to bus access is described in General System Bulletin G4.

To use a SUE 4690 Block Transfer Adapter with a SUE parallel controller, the BTA must be located in the adjacent slot immeidately to the right of the parallel controller that it modifies.

SUE 4601 CONFIGURATION

SUE 4601 is configured to operate with a paper tape reader or punch by factory installed jumpers at pre-designated terminal points on the printed circuit card. Two jumper classes are used: program and function jumpers. Program jumpers define the module address, interrupt request/select lines, and operating mode. Function jumpers effect the logical interface between the controller and the specific device. All jumpers are wrapped on 0.025-inch wire-wrap posts using number 30 AWG wire. Wire-wrap posts are pre-installed in jumper connection pads. A maximum of two wires can be wrapped on a wire-wrap post.

PROGRAM JUMPERS. - Logic diagram sheet 1 contains a list of the SUE 4601 program jumpers. J3 is used to encode the module address; J4, the interrupt request/select lines; and J5 the Program Data Transfer (PDT) or Direct Data Transfer (DDT) mode.

Program jumpers are identified by an alphanumeric designation such as J3-1A where J3 defines the functional group (i.e. addressing) and -1A defines the connection location. The same designation type is used to identify I/O connectors J1 and J2 and their pin locations.

Address Encoding (J3)

Each address bit, A04 through A11, is encoded by connecting a jumper as indicated in the Program Plug Data for J3 on LD sheet 1. J3 is represented schematically on LD sheet 10. Each of the eight bits must be connected to either a binary 1 terminal or a binary 0 terminal to encode the address.

PPB

Interrupt Line Connections (J4)

The interrupt request/select line jumper terminals are represented schematically on LD sheet 3. Only one pair of the four SRL(x)/SEL(x) terminal points should be connected. In LEC SUE standard practice, line 2 is assigned to most peripheral controllers. Where system requirements demand another pair of lines because of priority or design, any one of the four pairs can be connected. Interrupt line priorities and operation are described in General System Bulletin G4.

Mode Selection (J5)

Program plug J5 contains terminals for one jumper and is shown schematically on LD sheet 3. To operate the controller without a SUE 4590 Block Transfer Adapter (PDT mode), this jumper must be connected so that bus access can be initiated for a program data transfer. To operate with a SUE 4590 Block Transfer Adapter (BTA mode), this jumper must be disconnected.

FUNCTION JUMPERS. - Function jumper pads are identified by an alphanumeric designation such as E1, E2, E3 etc., where E is a fixed prefix and the number set is sequential beginning with 1. SUE 4601 contains 79 terminal points for function jumpers, but only 27 are used to configure the controller to operate paper tape devices. All function jumper terminals are listed in table 1; those used to configure a 4601 are listed at the beginning of table 1. Each program and function jumper terminal identification is etched on the controller circuit card. The terminal points can be located physically by referring to the circuit card assembly drawing facing the first logic diagram.

Table 1. SUE 4601 Function Jumper Terminals and Configurations

Jumper Terminal	Logic Diagram Location	Function
E1	7D2	J1-A1
E2	6C2	J1-A13
E3	6C2	J1-A14
E4	6C2	J1-A15
E5	6C2	J1-A16
E6	6C2	J1-A17
E7	6C2	J1-A18
E8	6C2	J1-A19
E9	6C2	J1-A20
E10	9A3	SIST-P
E11	9A3	0 V
E12	9A3	1K Pull-up to +5.0 v
E13	6B2	J2-A18
E14	6B2	J2-A19
E15	6B2	J2-A20
E16	6B2	J2-A21
E17	6B2	J2-A22
E18	6B2	J2-A23
E19	6B2	J2-A24
E20	6B2	J2-A25
E21	6D2	ID08-P Input Data
E22	6D2	ID09-P Input Data
E23	8D4	ID10-P Input Data
E24	8D4	ID11-P Input Data
E25	8D4	ID12-P Input Data
E26	8D3	ID13-P Input Data

Jumper Configuration SUE 4601

From	To
E9	E50
E11	E30
E11	E28
E13	E49
E21	E22
E22	E23
E23	E24
E24	E25
E25	E26
E26	E27
E27	E28
E30	E31
E31	E32
E32	E33
E35	E36
E47	E52
E48	E53
E55	E60
E58	E59
E65	E66

PPB

Table 1. SUE 4601 Function Jumper Terminals and Configuration (Continued)

Jumper Terminal	Logic Diagram Location	Function
E27	8D3	ID14-I Input Data
E28	8D3	ID15-P Input Data
E29	4D2	STS3-N Auxiliary Status
E30	8D3	STS6-P Auxiliary Status
E31	8D3	STS8-P Auxiliary Status
E32	8D3	STS7-P Auxiliary Status
E33	8D3	STS5-P Auxiliary Status
E34	4D2	STS4-N Auxiliary Status
E35	7D3	Character/Block Control
E36	5B4	CRQS-P Read Start
E37	4D3	STS2-N Auxiliary Status
E38	5A1	OD08-P Output Data
E39	8A2	OD11-P Output Data
E40	8A2	OD10-P Output Data
E41	8A2	OD12-P Output Data
E42	8A2	OD13-P Output Data
E43	8A2	OD14-P Output Data
E44	8A2	OD15-P Output Data
E45	5A1	OD09-P Output Data
E46	7C4	J2A3 WDDC Write Device Data Call
E47	7B4	Pin 13 WDGR Write Device Run Gate
E48	7C4	Pin 9 WDDA Write Data Call Gate
E49	7D2	Pin 5 WDNA Write Device Not Ready Gate
E50	7C2	Pin 2 RDNA Read Device Not Ready Gate
E51	7C2	[illegible] Write Device Not Ready
E52	7B4	[illegible]

Table 1. SUE 4601 Function Jumper Terminals and Configuration (Continued)

Jumper Terminal	Logic Diagram Location	Function
E53	7D4	0 v
E54	7D2	0 v
E55	7C2	0 v
E56	9B4	CMD2-N Auxiliary Command to Device
E57	9B4	CMD1-N Write Command to Device
E58	6D4	J1A2 Input Data Strobe
E59	6D4	SOS-P Strobe One-Shot Input
E60	6D4	SOS-N Strobe One-Shot Input
E61	7A4	J2A7 WDGA-N Write Device Run
E62	7D1	Auxiliary I/O Control Driver Input
E63	7D1	Auxiliary I/O Control Driver Input
E64	7A4	EDST-P External Device Strobe
E65	6D4	RDS-P Read Data Strobe Input
E66	6D4	SOS-N Strobe One-Shot Output
E67	6D4	SOS-P Strobe One-Shot Output
E68	9B4	J2A5 CMD2-N
E69	9B4	J2A6 CMD1-N
E70	-	Not Used
E71	-	Not Used
E72	5A3	CR01-N Write Start
E73	5B3	CR5S-P Control Register Bit 5
E74	5A3	CR05-N Control Register Bit 5 Inverted
E75	5A4	GRSA-N Reset or Write Status Register
E76	5A4	GRSC-P General Reset Inverted
E77	5A3	CR0S-N Control Register Bit 3 Inverted
E78	5A2	CR04-N Control Register Bit 4 Inverted
E79	5B3	CR4S-P Control Register Bit 4

PPB

CONTROLLER-DEVICE INTERFACE

Two connectors, J1 and J2, interface the input and output cables to the device. J1 interfaces input devices; J2 interfaces output devices. Both connectors are edge-mounted on the controller module as shown on the circuit card assembly drawing. Part numbers of the I/O connectors and mating plugs follow:

I/O Connector	I/O Connector Part Number	Mating Plug Part Number
J1	3M Company (40-Pin) 3432-1002	ITT Cannon (20/40 Position) 121-7365-000
J2	3M Company (50-Pin) 3433-1002	ITT Cannon (25/50 Position) 121-7365-002

Input and output connector pin functions are listed in tables 2 and 3, respectively. Pin assignments are shown in table 4.

LOGIC DESCRIPTION

Figure 2 is a detailed block diagram of SUE 4601 that corresponds directly with the logic diagrams. The number in the upper left-hand corner of each block refers to the logic diagram sheet number where the corresponding logic is located. Logic descriptions and key source logic definitions are contained on the sheet preceding each logic diagram.

ASSEMBLY, LOGIC, AND PARTS

The SUE 4601 assembly drawing, logic diagrams, and parts list contained on the pages following, are listed below:

SUE 4601 Paper Tape Controller Circuit Card Assembly (PPB) 2001002137, Revision D (Sheet 1)

SUE 4601 Paper Tape Controller (PPB) LD2001002137-10 Revision B (Sheets 1 through 10)

Parts List, Assembly Model 4601 PL2001002137-1, Revision D (Sheets 1 and 2 of 2)

A description of the reference designators, signal locations, and procedures for using these items is contained in the SUE DOCUMENT INDEX, General System Bulletin G1.

Table 2. SUE 4601/6714/6715 and /6719 High Speed Paper Tape Readers Interconnections

Controller	Logic Diagram Location	Function	P1	Device Cable SUE 6714/15 P01	Device Cable SUE 6719 P03
J1-A1	7D2	Reader Not Ready Status	P1-A1	13	13
J1-A2	6D4	(E58) Input Data Strobe (Sprocket)	P1-A2	12	9
J1-A3	7A3	RDRC-N Drive Right	P1-A3	-	12
J1-A4	7A3	RDRH-P Read Command	P1-A4	8	-
J1-A5	6D3	ID00-P Input Data Channel 1	P1-A5	1	1
J1-A6	6D3	ID01-P Input Data Channel 2	P1-A6	2	2
J1-A7	6D3	ID02-P Input Data Channel 3	P1-A7	6	3
J1-A8	6D3	ID03-P Input Data Channel 4	P1-A8	10	4
J1-A9	6D3	ID04-P Input Data Channel 5	P1-A9	4	5
J1-A10	6D3	ID05-P Input Data Channel 6	P1-A10	9	6
J1-A11	6D2	ID06-P Input Data Channel 7	P1-A11	3	7
J1-A12	6D2	ID07-P Input Data Channel 8	P1-A12	7	8
J1-A13	6D2	Reader Not Ready Status Return	P1-A13	17	10
J1-A14	6D2		Not used	-	-
J1-A15	6D2		Not used	-	-
J1-A16	6D2		Not used	-	-
J1-A17	6D2		Not used	-	-
J1-A18	6D2		Not used	-	-
J1-A19	6D2		Not used	-	-
J1-A20	6D2	SUE 6714/15 XOR GRD (E50)	⑤P1-A20	-	-

Notes:

1. Signal returns to ground on J1 are on corresponding B pins.
2. All wires in device cable are twisted pairs except the jumpers.
3. Pins 5, 11, 14, 15, 16, 17 are jumpered to signal ground in P01.
4. Device cable signals P1-A1 and P1-A13 are twisted pair with P1-A13 as return to reader ground.

⑤ SUE 6714/15 cable only, jumper to GRD, P1-B20.

6. All signal returns are connected to ground at P03 pin 10 for SUE 6719.

PPB

Table 3. SUE 4601/6716 and/6719 High Speed Paper Tape Punch Interconnections

Controller	Logic Diagram Location	Function	Device Cable P2	Device Cable SUE 6716 P01	Device Cable SUE 6719 P01
J2-A1	9D4	STS1-N Auxiliary Device Status	Not used	-	-
J2-A2	9D4	Auxiliary Device Control Input	Not used	-	-
J2-A3	7D4	WDDC Punch Data Call	P2-A3	12	12
J2-A4	7D2	Punch Not Ready Status	P2-A4	20	20
J2-A5	9A4	CMD2-N Auxiliary Command to Device	Not used	-	-
J2-A6	9A4	CMD1-N Write Command to Device	Not used	-	-
J2-A7	7A4	WDGA-N Start Punch Cycle	P2-A7	11	11
J2-A8	7A1	Auxiliary I/O Control Driver 2	Not used	-	-
J2-A9	7A1	Auxiliary I/O Control Driver 1	Not used	-	-
J2-A10	5A2	OD07-P Output Data Channel 8	P2-A10	8	8
J2-A11	5A2	OD06-P Output Data Channel 7	P2-A11	7	7
J2-A12	5A2	OD05-P Output Data Channel 6	P2-A12	6	6
J2-A13	5A2	OD04-P Output Data Channel 5	P2-A13	5	5
J2-A14	5A2	OD03-P Output Data Channel 4	P2-A14	4	4
J2-A15	5A2	OD02-P Output Data Channel 3	P2-A15	3	3
J2-A16	5A2	OD01-P Output Data Channel 2	P2-A16	2	2
J2-A17	5A2	OD00-P Output Data Channel 1	P2-A17	1	1
J2-A18	6A2	E13 Function Jumper (Status Polarity)	P2-A18	-	-
J2-A19	6A2	E14 Function Jumper	Not used	-	-
J2-A20	6A2	E15 Function Jumper	Not used	-	-
J2-A21	6A2	E16 Function Jumper	Not used	-	-
J2-A22	6A2	E17 Function Jumper	Not used	-	-
J2-A23	6A2	E18 Function Jumper	Not used	-	-
J2-A24	6A2	E19 Function Jumper	Not used	-	-
J2-A25	6A2	E20 Function Jumper	Not used	-	-

Notes:

1. Signal returns to ground on J2 are on corresponding B pins.
2. All wires in device cable are twisted pairs except the jumpers.
3. P01-9 and P01-24 jumpered for +6 v Bias to Feed Hole for SUE 6716 only.
4. P2-A18 jumpered to P2-B18.

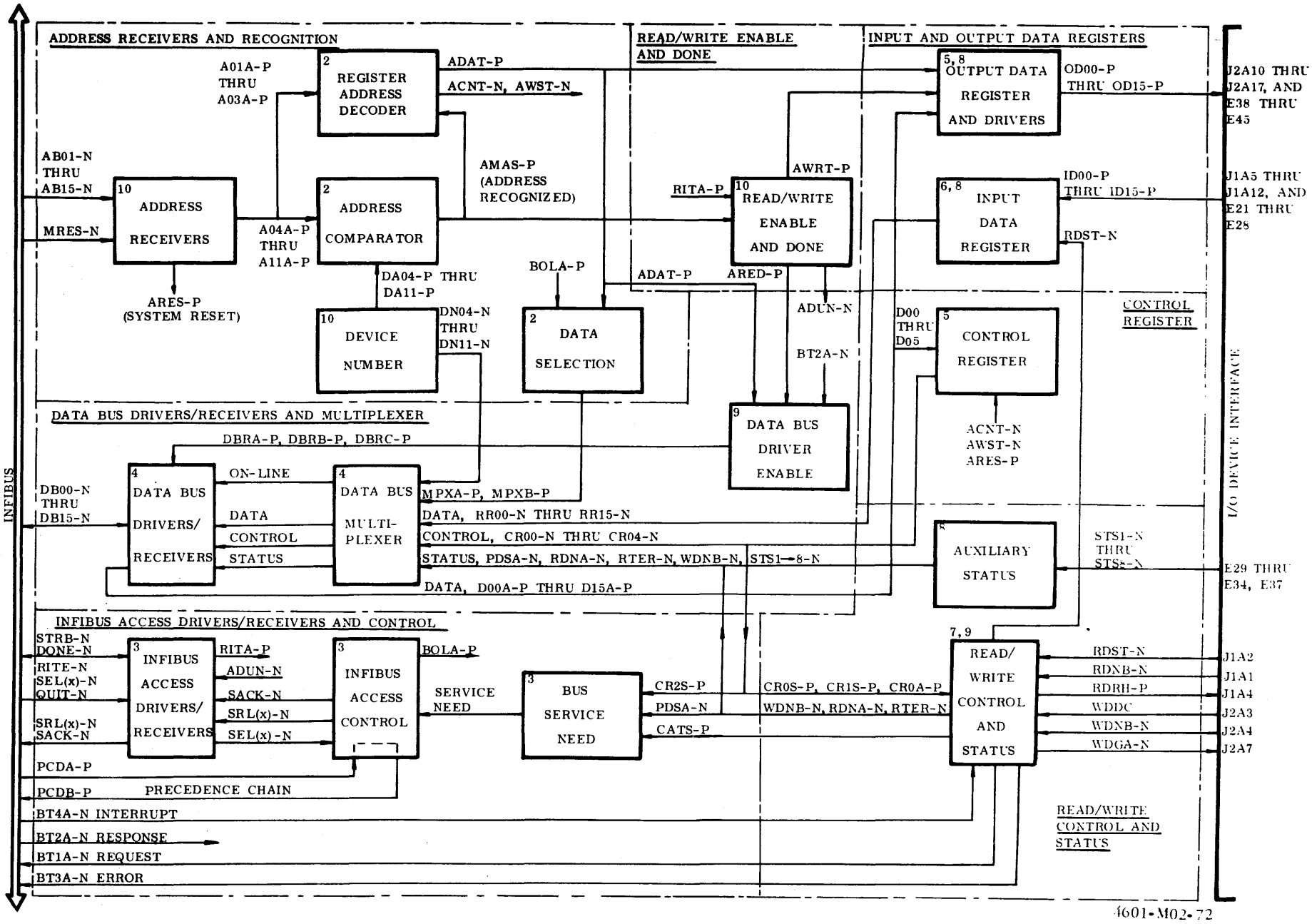
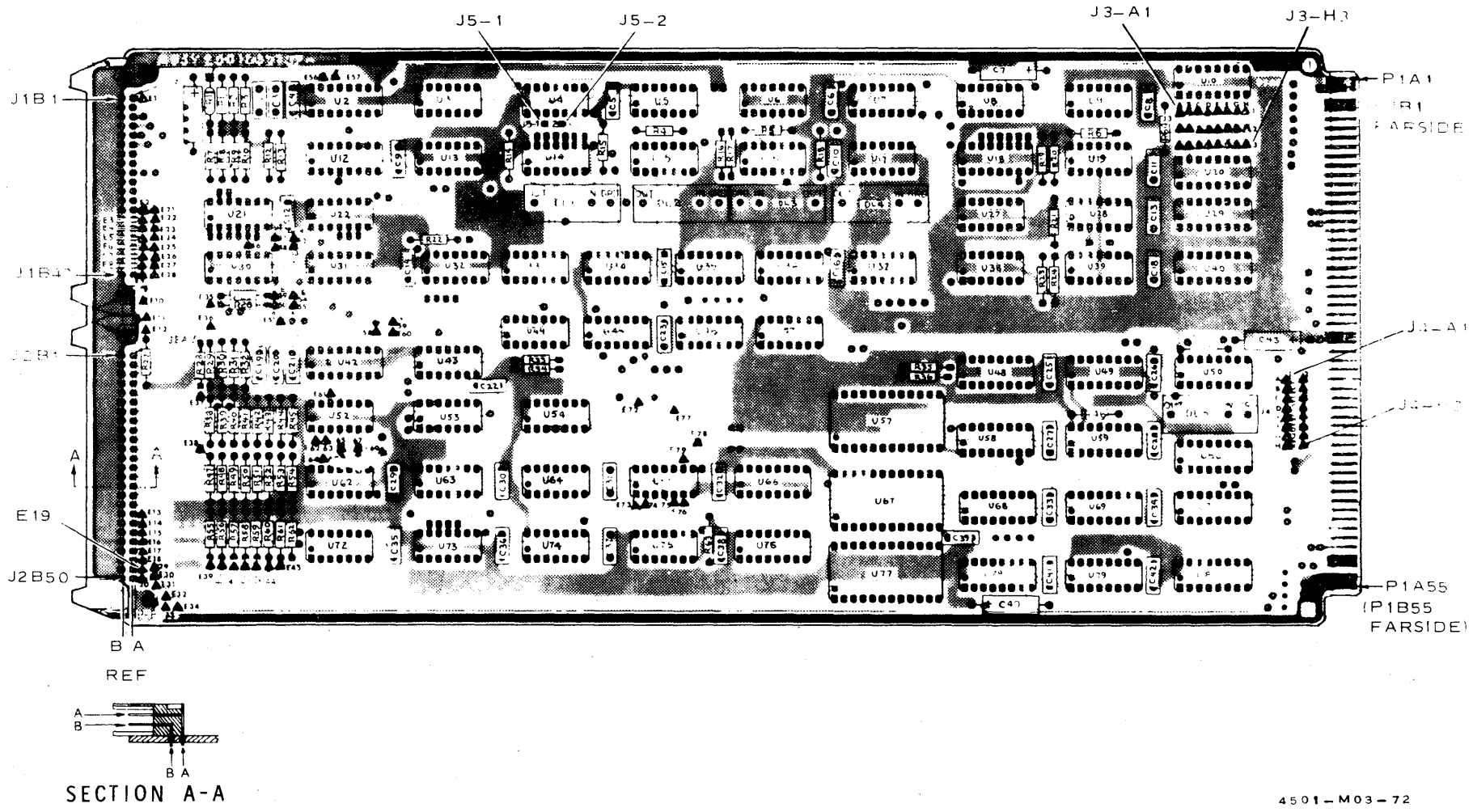


Figure 2. SUE 4601 High Speed Paper Tape Controller, Detailed Block Diagram

PPB



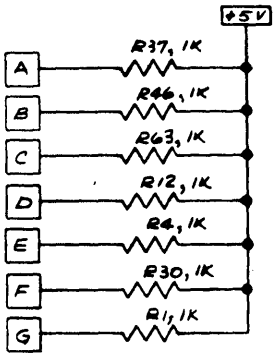
SUE 4601 Parallel I/O Controller Circuit Card
Assembly (PPB) 2001002137 Revision D

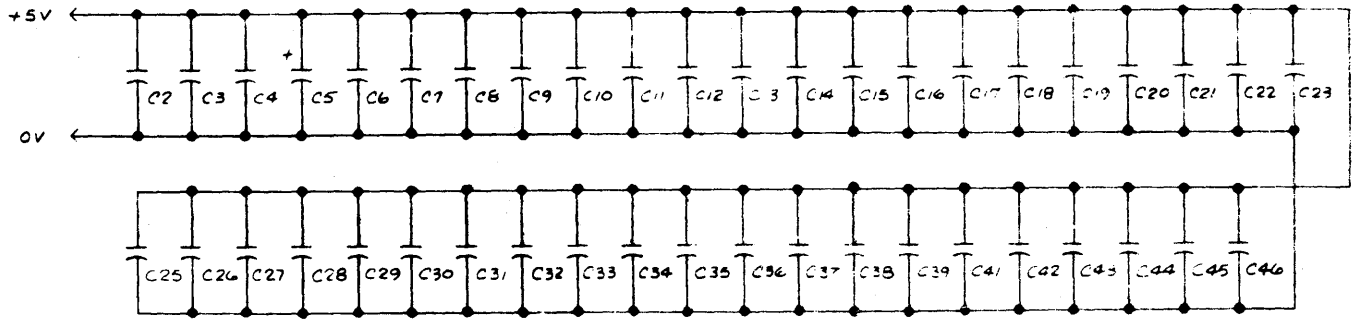
A B C D

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS ± 2%, 1/4W.
2. ALL DIODES ARE 8001100001.
3. ALL NON-POLARIZED CAPACITORS ARE 8001300101.
4. ALL POLARIZED CAPACITORS ARE 33 μF, +80%-20%, 50V.
5. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE 8001800200.
6. J1-B1 THRU J1-B20 AND J2-B1 THRU J2-B25 ARE CIRCUIT RETURNS (0V).

PROGRAM PLUG DATA		
FUNCTION	LOCATION	MATCH LOCATION
ADDRESS BIT 4	J3-2H	J3-1H (BINARY 0), J3-3H (BINARY 1)
5	J3-2G	J3-1G, J3-3G
6	J3-2F	J3-1F, J3-3F
7	J3-2E	J3-1E, J3-3E
8	J3-2D	J3-1D, J3-3D
9	J3-2C	J3-1C, J3-3C
10	J3-2B	J3-1B, J3-3B
ADDRESS BIT 11	J3-2A	J3-1A (BINARY 0), J3-3A (BINARY 1)
SERVICE REQ. LEVEL 1	J4-1A	J4-2A (SEL 1)
	J4-1E	J4-2E (SRL 1)
SERVICE REQ. LEVEL 2	J4-1B	J4-2B (SEL 2)
	J4-1F	J4-2F (SRL 2)
SERVICE REQ. LEVEL 3	J4-1C	J4-2C (SEL 3)
	J4-1G	J4-2G (SRL 3)
SERVICE REQ. LEVEL 4	J4-1D	J4-2D (SEL 4)
	J4-1H	J4-2H (SRL 4)
STAND ALONE PDT MODE	J5-1	J5-2 (PDT INTERRUPT)





PPB

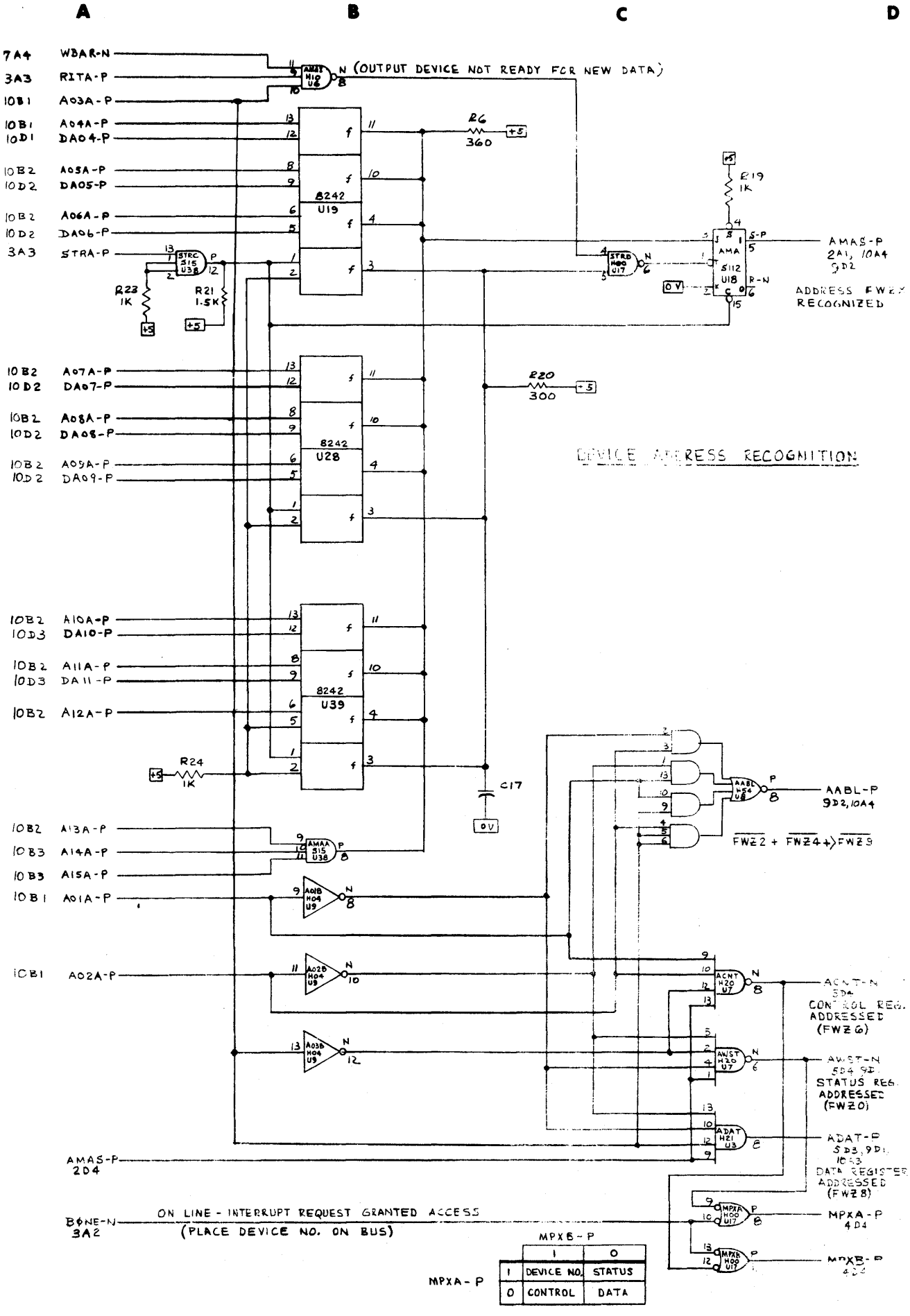
DEVICE ADDRESS RECOGNITION (LD Sheet 2)

Address Comparators U19, U28, and U39 are four-bit quad exclusive NOR gates that compare the incoming address with the jumper-encoded device address. The strobe received from the INFIBUS triggers flip-flop AMA when the two addresses match. During output operations, AMA cannot set if the output device is not ready to accept new data.

Decodes of bits A01A-P, A02A-P, and A03A-P, address the control, status, and data registers, and specify through AABL-P that the present register address is valid.

KEY SOURCE LOGIC DEFINITIONS

AABL-P	Address valid, asserted only for register addresses 0, 1, 6, 7, 8, and 9.
ACNT-N	Address control, enables accessing the control register with a read or write command.
ADAT-P	Address data, enables loading the output data register or reading the input data register, and conditions data bus driver enabling signals DBRB-P and DBRC-P.
AMAS-P	Address recognized, asserted when address bits A04A-P through A11A-P match the device number encoded in DA04-P through DA11-P. Inhibited during output operations if device cannot accept new data.
AWST-N	Address status, clears the controller when the status register is addressed (FWZ0) concurrent with a write command. Input and output data registers are not cleared. Enables reading the status register with a read command.
MPXA-P, MPXB-P	A decode of these signals allows the multiplexer to select one of four sets of information for input. See the table at bottom of LD sheet 2.



SUE 4601 Paper Tape Controller (PPB), LD2001002137-1 Rev. B, Sheet 2

INFIBUS ACCESS DRIVERS/RECEIVERS AND CONTROL (LD Sheet 3)

Bus access drivers/receivers and initiating logic is shown above the dashed line on LD sheet 3.

Bus access control logic, represented below the dashed line, is equivalent to one-half of a Dual Bus Access Logic (DBAL) chip described in General System Bulletin G4 under SPECIAL COMPONENTS.

Operating in the PDT mode, connection J5-2 is jumpered to J5-1; in the BTA mode this jumper is absent. Jumper connections on J4 connect one of four interrupt request/select lines. In most SUE systems, SRL2-N and SEL2-N are used for peripheral device controllers.

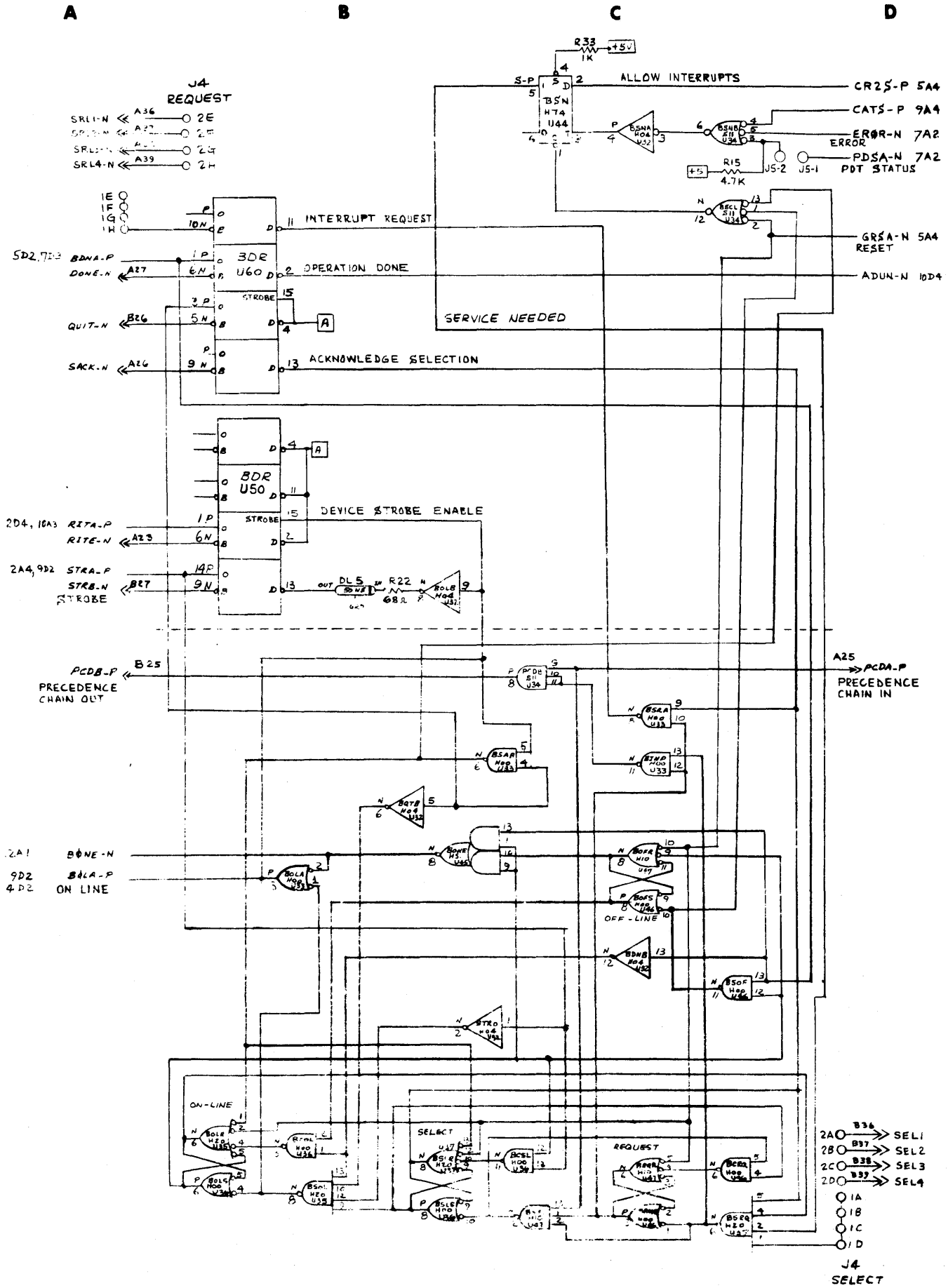
If interrupts are allowed (CR2S-P), Bus Service Need flip-flop (BSN) initiates the access control logic for any one of three conditions:

a. a BTA interrupt (CATS-P)
b. an error (EROR-N)
c. a PDT status (PDSA-N).

Reset clears BSN unconditionally. An abort or done condition clears BSN if the on-line latch is set.

KEY SOURCE LOGIC DEFINITIONS

BOLA-P, BONE-N	Bus On-Line signals generated when the controller has obtained bus access. These signals are used to enable the data bus multiplexer and drivers to transmit the device number on the data bus.
DONE-N, PCDA-P, PCDB-P, QUIT-N, SACK-N, SEL(x)-N, SRL(x)-N, STRB-N	INFIBUS control signals commonly used in SUE systems to control system module communication. See INFIBUS interface, General System Bulletin G4, for signal function descriptions.
RITE-N, RITA-P	RITE-N is the INFIBUS write command. RITA-P in the controller is the output of the RITE receiver. Asserted, RITA-P conditions the write mode; negated, conditions the read mode.



SUE 4601 Paper Tape Controller (PPB), LD2001002137-1 Rev. B, Sheet 3

DATA BUS DRIVERS/RECEIVERS AND MULTIPLEXER (LD Sheet 4)

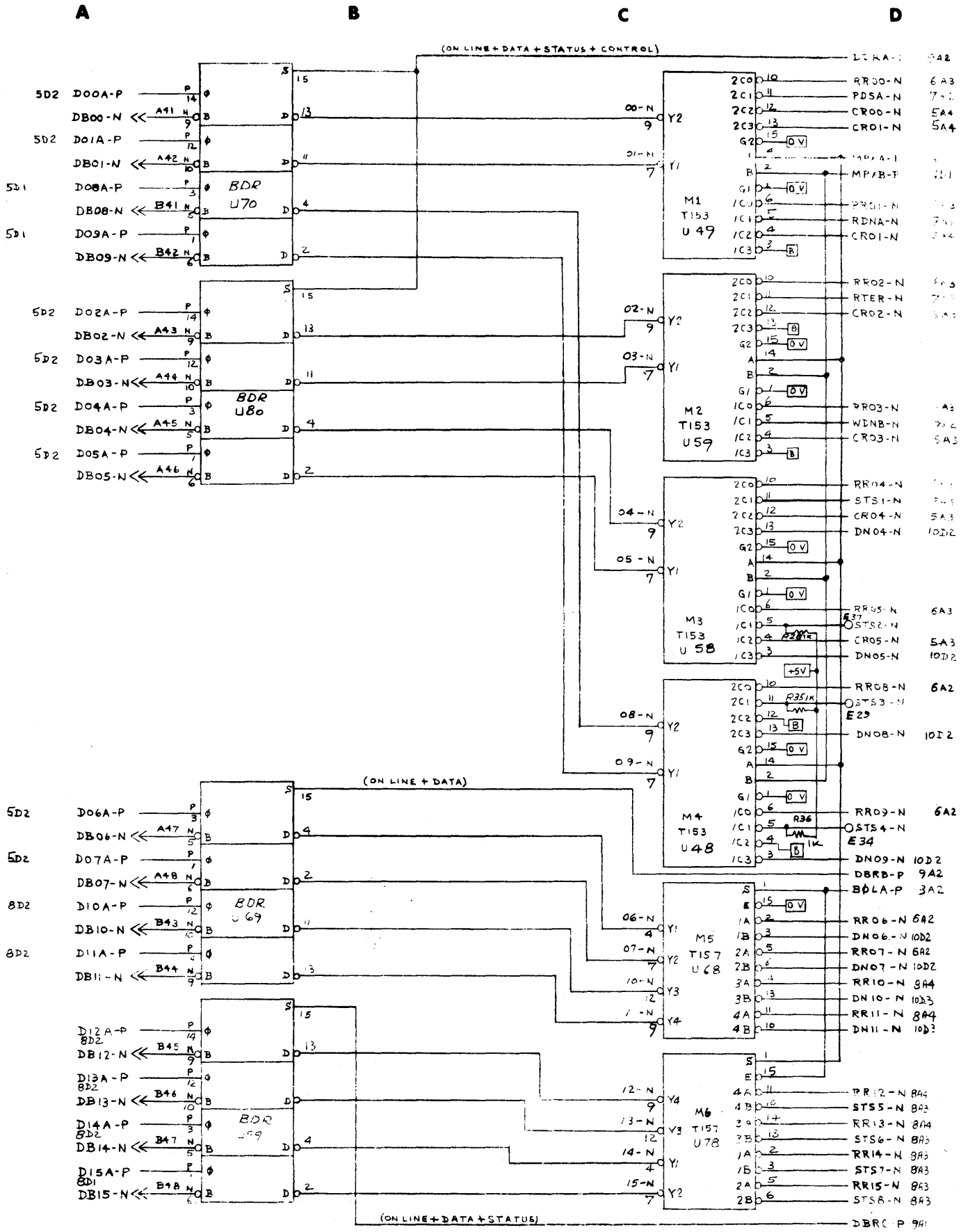
In the data bus drivers/receivers (U69, U70, U79 and U80) the receivers are always enabled; the drivers are off unless a positive strobe is present at the S input. With positive strobes DBRA-P, DBRB-P and DBRC-P, multiplexer outputs are transmitted on the data bus.

Multiplexer components U48, U49, U58, and U59 are four-line to one-line selectors activated by a decode of MPXA-P and MPXB-P. Components U68 and U78 are two-line to one-line selectors activated by the logic state at the select (S) and enable (E) inputs. S asserted selects B inputs; S negated, A inputs. U78 performs an additional function. E asserted forces outputs Y1, Y2, Y3, and Y4 low. Therefore, device number bits DN12-N through DN15-N are always transmitted as binary ONEs (hexadecimal F) to be consistent with LEC SUE standard practice for controller addresses.

To minimize propagation delay for device inputs, RR00-N through RR15-N are always selected (MPXA-P, MPXB-P both ZERO) when no other selection is active.

KEY SOURCE LOGIC DEFINITIONS

DB00-N thru DB15-N	Data bus interfaced to the data bus drivers/receivers.
D00A-P thru D15A-P	Data bits received from the data bus and applied to the output data register. Bits D00A-P thru D05A-P also are used to load the control register during Write Control Register operations.


A
B
C
D
(ON LINE + DATA + STATUS + CONTROL)
(ON LINE + DATA)
(ON LINE + DATA + STATUS)
BDR U70
BDR U80
BDR U69
BDR U79
M1 T153 U49
M2 T153 U59
M3 T153 U58
M4 T153 U48
M5 T157 U68
M6 T157 U78
DATA BUS MULTIPLEXER

CONTROL REGISTER CR00-N THROUGH CR05-N (LD Sheet 5)

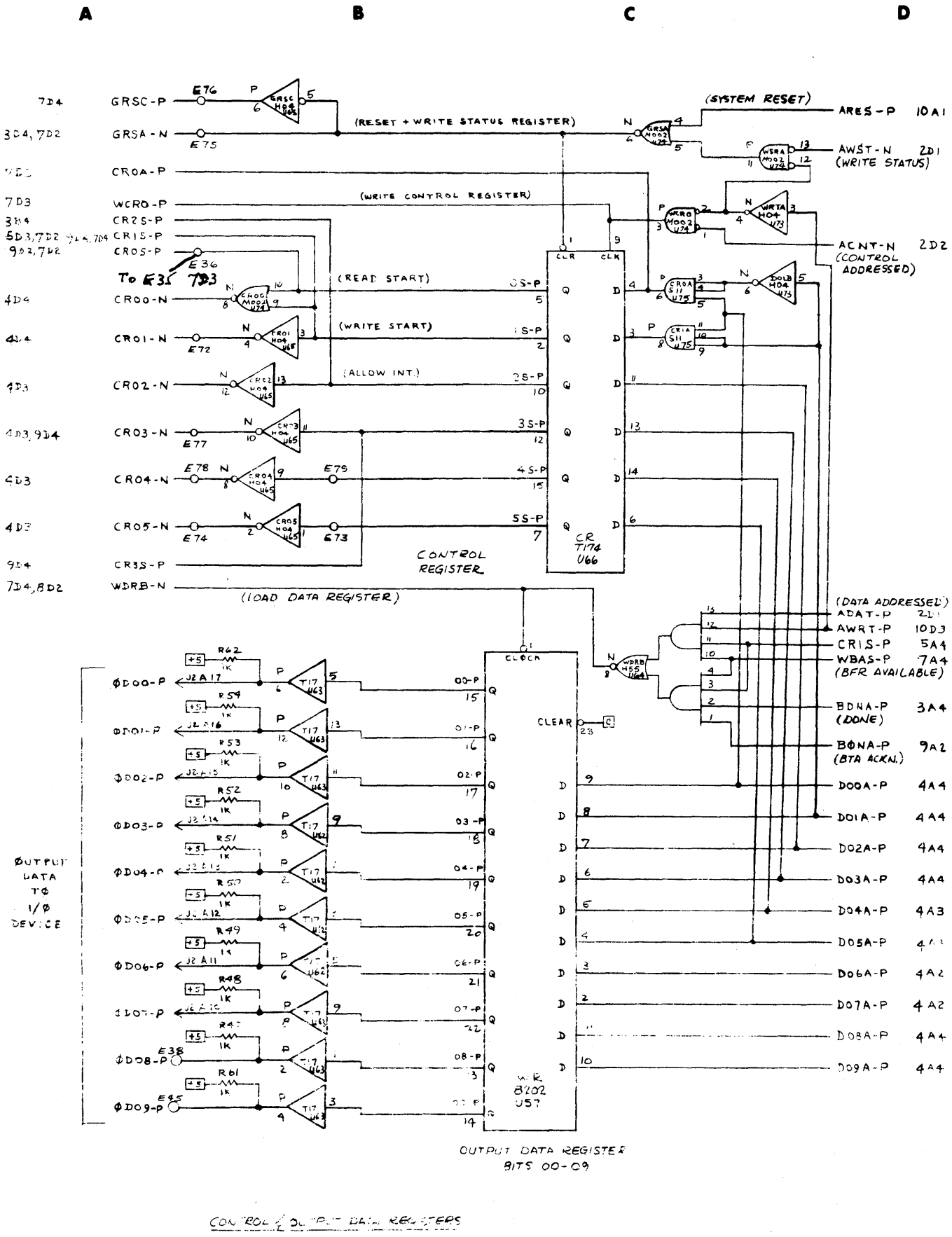
Control register U66 is loaded from data receivers D00A-P through D05A-P, by a positive-going transition of the clock input. Either a Write Status or a system reset clears the control register.

OUTPUT DATA REGISTER WR00-P THROUGH WR09-P (LD Sheet 5)

Output data register U57 is clocked by a negative-going transition at the clock input. Neither a Write Status nor a system reset clears U57; data is retained as entered by the last clock pulse. The output data register is continued on LD sheet 8.

KEY SOURCE LOGIC DEFINITIONS

CR00-N thru CR05-N	Inverted outputs of the control register selectable for input by the data bus multiplexer.
CR0S-P	Control bit 0, asserted, enables the input mode.
CR1S-P	Control bit 1, asserted, enables the output mode.
CR0A-P	Read command input to control register bit 0, used to direct-set the read-device-run flip-flop.
CR2S-P	Control bit 2, asserted, indicates that interrupts are allowed. Enables the INFIBUS access logic.
CR3S-P	Control bit 3 used to enable an auxiliary write command.
D00A-P thru D09A-P	Part of data received from the data bus and sent to the output data register. D00A-P through D05A-P also set control bits CR00 through CR05 when the control register is addressed.
GRSA-N, GRSC-P	Resets the controller as a result of a system reset or a Write Status operation.
OD00-P thru OD09-P	Part of output data from the output data drivers to the write device.
WCR0-P	Clocks a read or write command into the control register and used to direct-set read-device-run flip-flop.
WDRB-N	Clocks data into the output data register and resets the WBA flip-flop.


A
B
C
D
GRSC-P
GRSA-N
CR0A-P
WCR0-P
CR2S-P
CR1S-P
CR0S-P
CR00-N
CR01-N
CR02-N
CR03-N
CR04-N
CR05-N
CR3S-P
WDRB-N
(RESET + WRITE STATUS REGISTER)
(SYSTEM RESET)
ARES-P
AWST-N
(WRITE STATUS)
(WRITE CONTROL REGISTER)
ACNT-N
(CONTROL ADDRESSED)
(READ START)
(WRITE START)
(ALLOW INT.)
CONTROL REGISTER
(LOAD DATA REGISTER)
(DATA ADDRESSED)
ADAT-P
AWRT-P
CR1S-P
WBAS-P
(BFR AVAILABLE)
BDNA-P
(DONE)
BØNA-P
(BTA ACKN.)
D00A-P
D01A-P
D02A-P
D03A-P
D04A-P
D05A-P
D06A-P
D07A-P
D08A-P
D09A-P
ØD00-P
ØD01-P
ØD02-P
ØD03-P
ØD04-P
ØD05-P
ØD06-P
ØD07-P
ØD08-P
ØD09-P
ØUTPUT DATA TØ I/Ø DEVICE
CLEAR
CLOCK
OUTPUT DATA REGISTER BITS 00-09
CONTROL & OUTPUT DATA REGISTERS

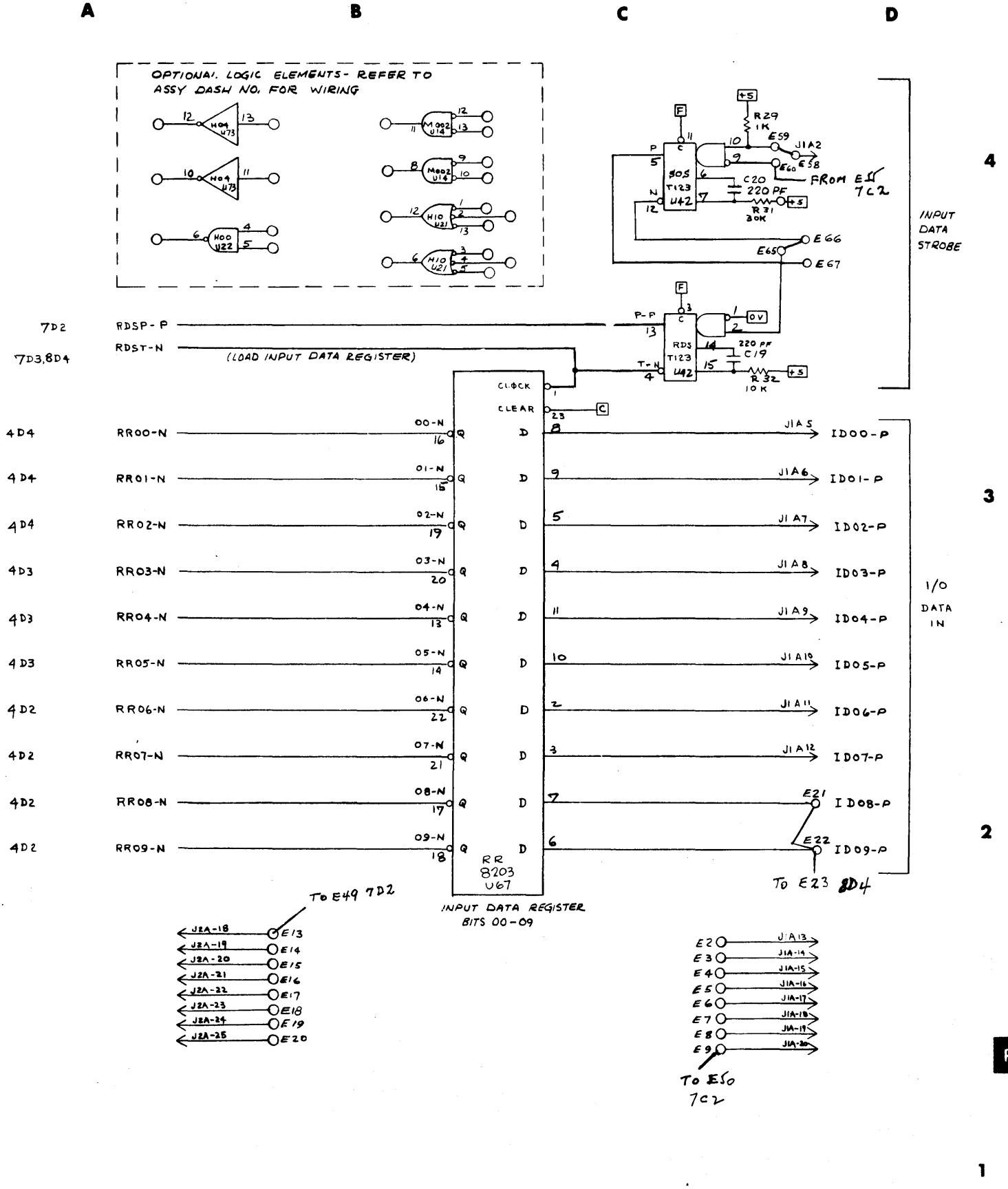
INPUT DATA REGISTER, RR00-N THROUGH RR09-N (LD Sheet 6)

A positive-going transition of the read data strobe (sprocket signal) sent by the reader triggers one-shot SOS. SOS times out in 2.8 microseconds, triggering one-shot RDS whose negative-going transition clocks input data register U67, loading reader data into the register. RDST-N and complement RDSP-P also control timing in the read control logic.

Neither a Write Status nor a system reset clears the input data register. Data is retained as entered by the last clock pulse. The input data register is continued on LD sheet 8.

KEY SOURCE LOGIC DEFINITIONS

ID00-P thru ID09-P	Input data bits applied to the input data register from the read device.
RDSP-P	Positive read device strobe that terminates the read start pulse and triggers flip-flop RTE.
RDST-N	Negative read device strobe that clocks data into the input data register, and triggers the read-buffer-available flip-flop.
RR00-N thru RR09-N	Data from the input data register selectable at the data bus multiplexer for transmission on the INFIBUS.



INPUT DATA REGISTER

WRITE CONTROL (LD Sheet 7)

Punch start pulse WDGA-N is issued when the output data register has been loaded (WBAR-N is high) and a data request (WDDC) satisfies gate WDGC. Dropping the data request terminates the start pulse and triggers WBAT which direct-sets WBA. As a result, WBAS-P:

a. sets PDT status bit PDSA-N
b. primes gate WDRB to clock new data into the output data register.

READ CONTROL (LD Sheet 7)

Flip-flop RDR issues a start pulse to the reader whenever a read command is clocked into the control register (WCRO-P, CROA-P). For character read devices, where E35 is connected to E36 (LD sheet 5), another run pulse is issued after each input data transfer (DRBB-N or gate RDRA-N). A strobe (RDST-N and RDSP-P) from the read device:

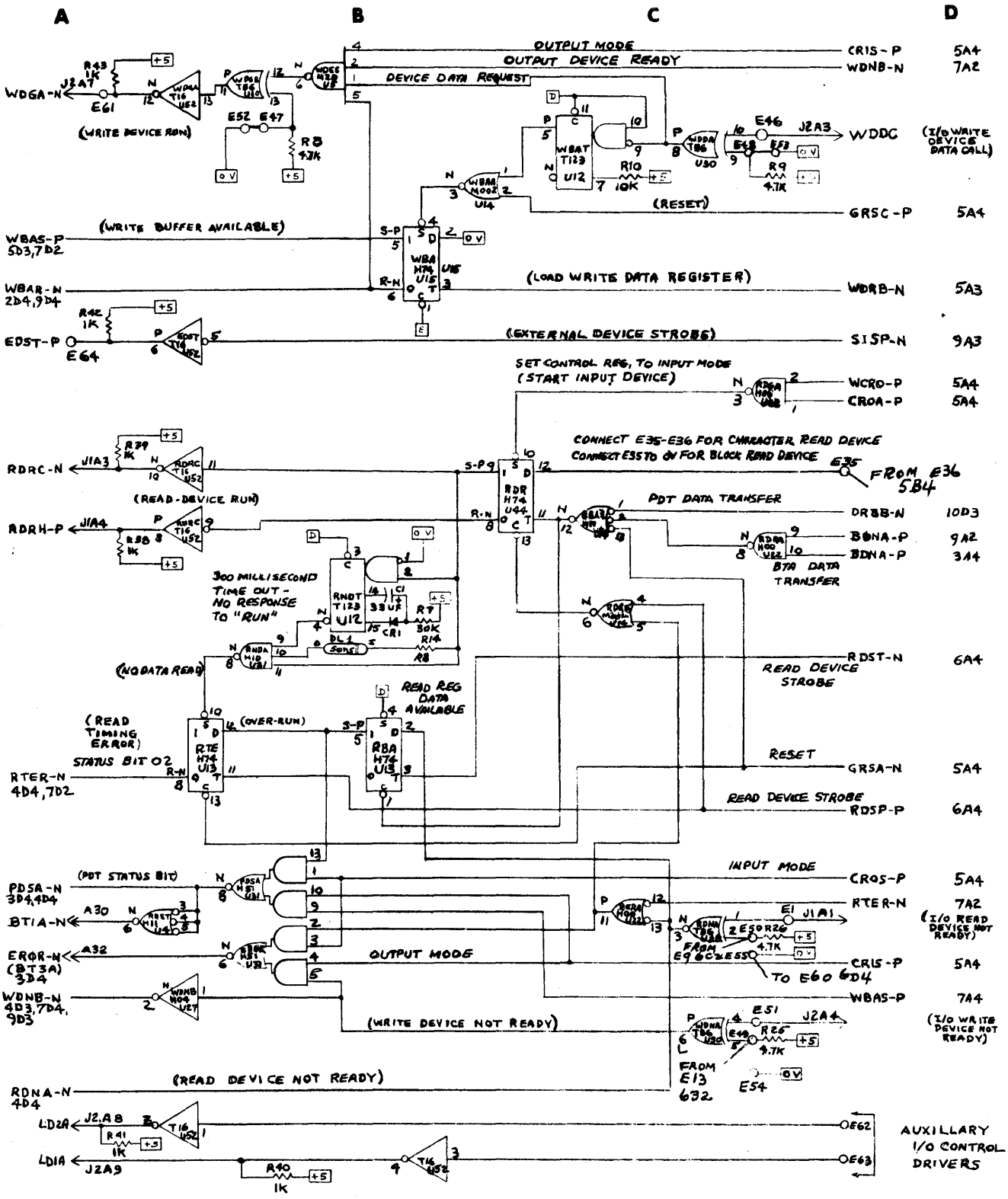
a. clocks the input data register
b. terminates the start pulse by resetting RDR
c. triggers flip-flop RBA (which sets PDT status, PDSA)
d. triggers flip-flop RTE.

READ TIMING ERROR

Either an overrun or a 300-millisecond time-out sets flip-flop RTE. An overrun occurs if flip-flop RBA is not cleared by a data transfer (gate RBAZ-N) before the next read device strobe is received. A time-out occurs if the read device does not respond to the run pulse within 300 milliseconds, nominal. Time-out is a function of one-shot RNDT which is retriggered with every run pulse.

KEY SOURCE LOGIC DEFINITIONS

BT1A-N	Request bit asserted by the same conditions that activate PDSA-N, notifies the BTA that a data transfer is required.
BT3A-N	Error signal EROR-N to the BTA that specifies either a read timing error has occurred or the I/O device is not ready.
PDSA-N	Program data transfer status - asserted during input when read data is strobed into the input data register; asserted during output when the output data register is ready to be loaded with the next write data.
RDNA-N	Read-device-not-ready status.
RDRC-N, RDRH-P	Read-device-run signals to start the input device.
RTER-N	Read timing error status generated if an overrun condition occurs or the read device does not respond within a time limit.
WBAR-N, WBAS-P	Write-Buffer-Available flip-flop set, indicates output data register is available to receive output data.
WDDC-N	Write device data call received from the output device when ready to receive another data output.
WDGA-N	Write-device-run signal to start the output device.
WDNB-N	Write-device-not-ready status.



I/O READ-WRITE CONTROL/STATUS

INPUT DATA REGISTER, RR10-N THROUGH RR15-N (LD Sheet 8)

Input data register, U77, is a continuation of U67 shown on LD sheet 6, but not used actively in the 4601 configuration.

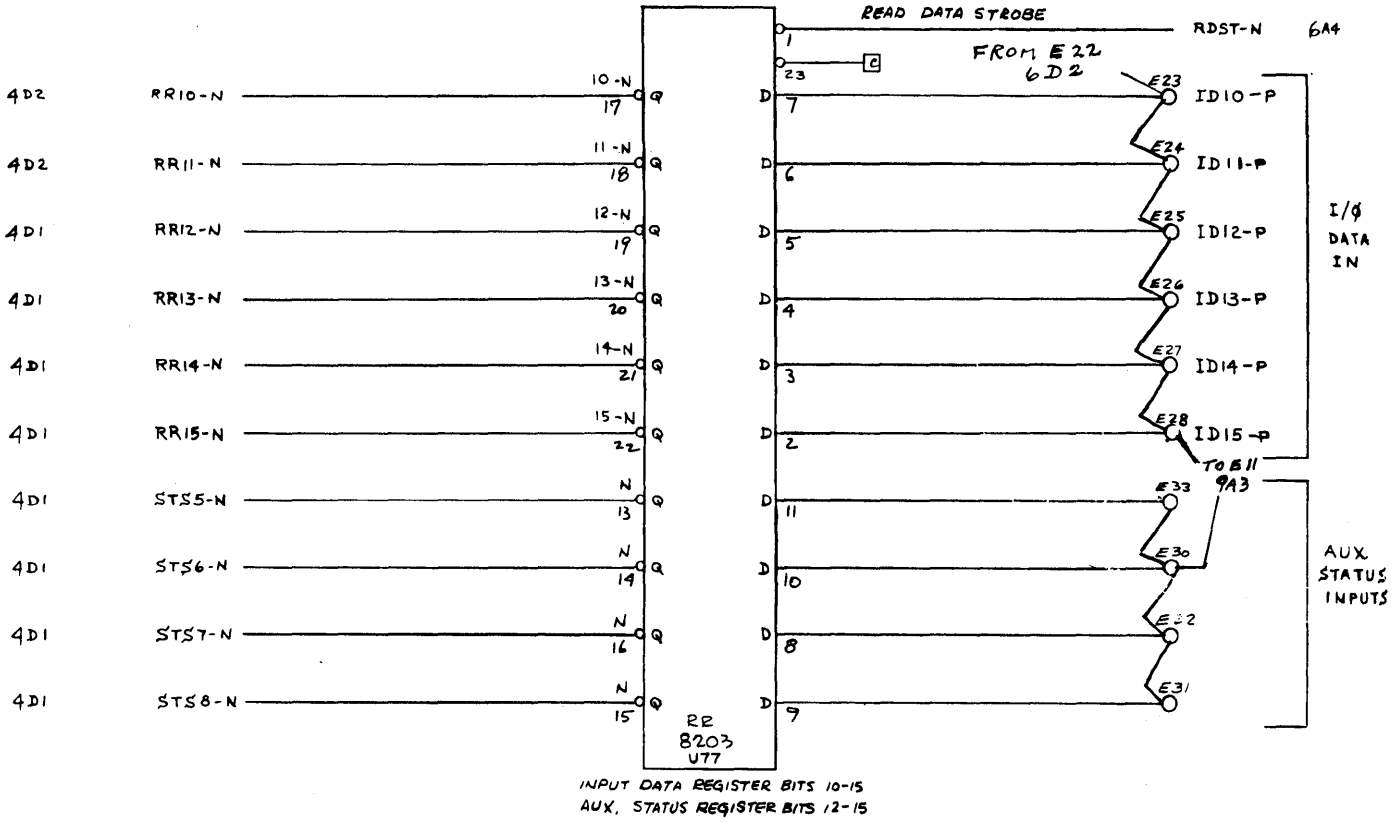
OUTPUT DATA REGISTER, WR10-P THROUGH WR15-P

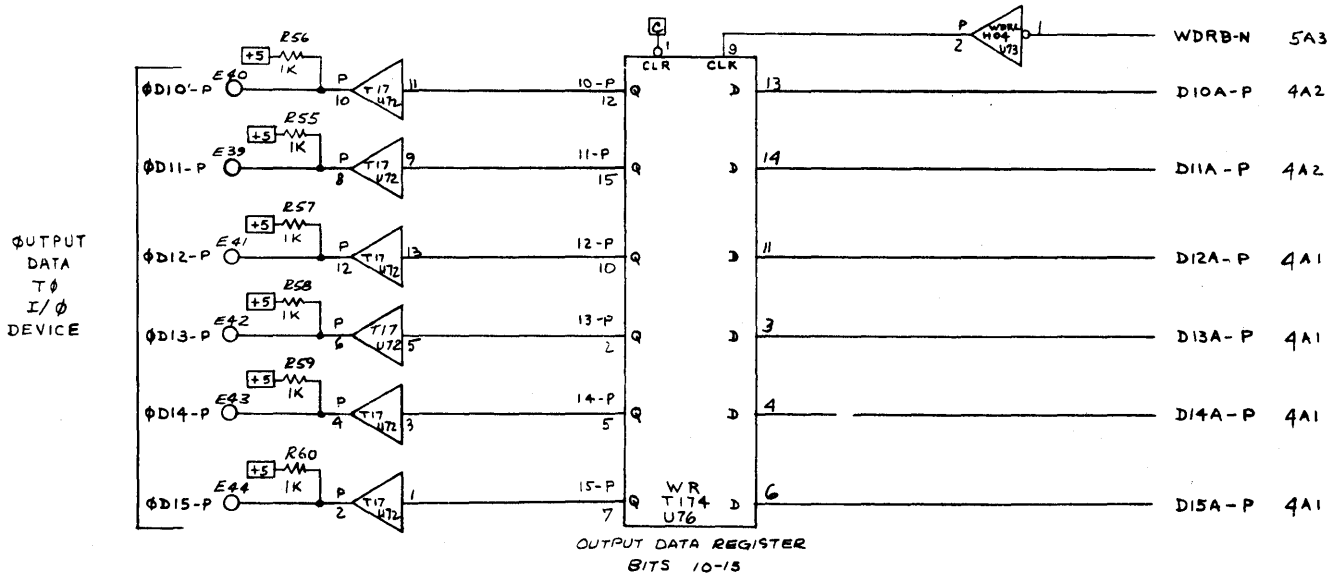
Output data register U76 is a continuation of U57 shown on LD sheet 5, but not used actively in the 4601 configuration.

KEY SOURCE LOGIC DEFINITIONS

*D10A-P thru D15A-P
*ID10-P thru ID15-P
*OD10-P thru OD15-P
*RR10-N thru RR15-N
*STS5-N thru STS8-N

*Not used for paper tape devices.





INPUT/ΦUTPUT BITS 10 THRU 15 DATA REGISTERS

PPB

AUXILIARY WRITE CONTROL (LD Sheet 9)

Write command lines CMD1-N, CMD2-N, and the associated logic components allow the controller to communicate with devices that multiplex both data and control information on the output data lines. CMD1-N indicates data; CMD2-N control. Either one or the other command line is activated according to the logic state of control bit CR03.

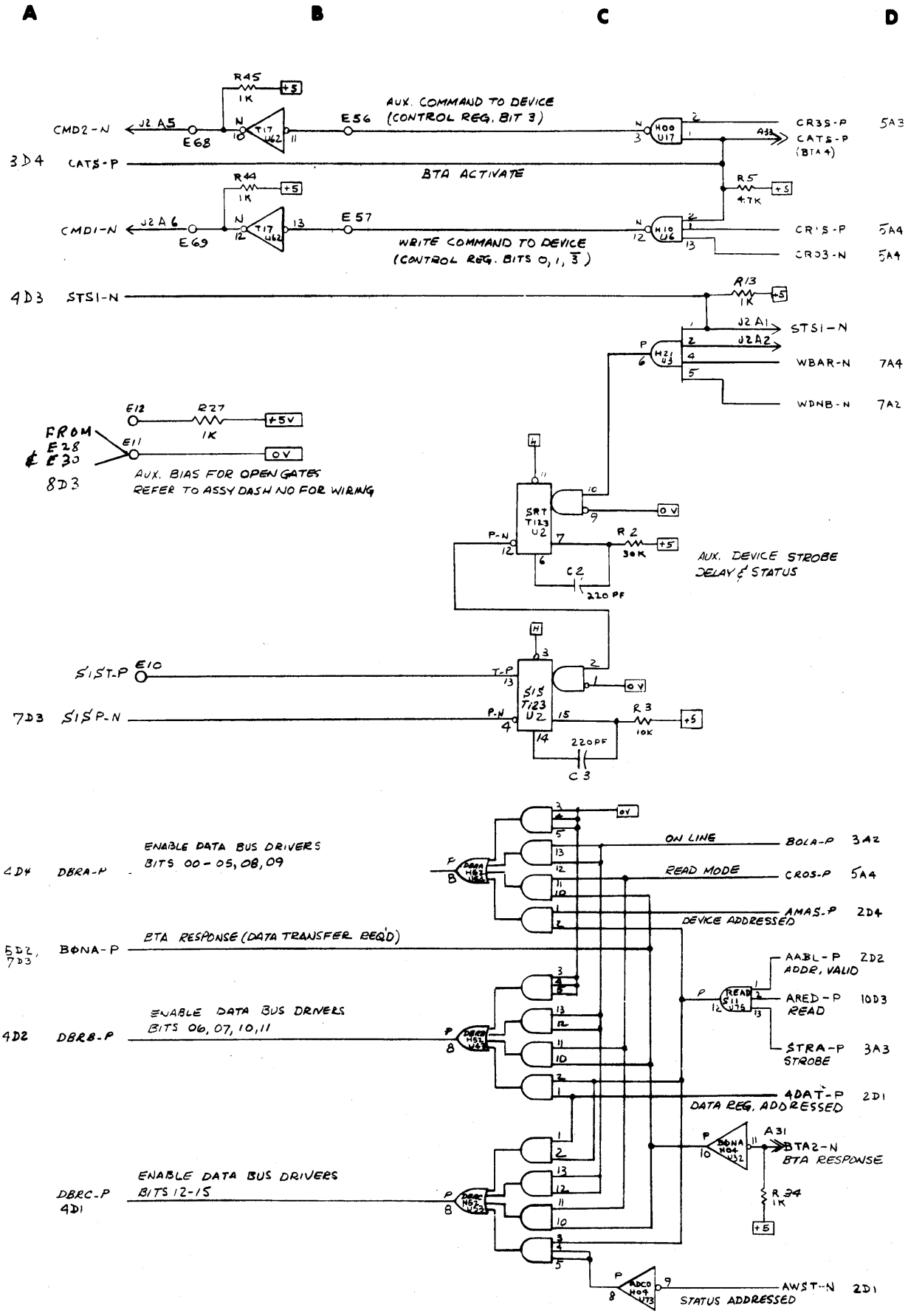
One-shots SRT and SIS allow the controller to operate with output devices that do not send a data call. For such devices, pseudo command SIST-P (or SISP-N) is applied to E48 (LD sheet 7) to initiate the write control logic. One-shot SRT is triggered when the output device can accept another output as indicated by auxiliary device status at J2-A1 and J2-A2.

DATA BUS DRIVER ENABLE

Conditioning logic to assert the data bus driver enabling signals is shown in the lower portion of LD sheet 9.

KEY SOURCE LOGIC DEFINITIONS

BT2A-N, BONA-P	Response from the BTA used by the controller during a block transfer to enable loading the output data register during output; trigger the read-device-run flip-flop and issue data bus driver enabling signals to place read data on the data bus during input.
BT4A-N	The interrupt initiate signal from the BTA becomes CATS-P initiates the controller bus access control logic, and enables auxiliary write command lines CMD1-N and CMD2-N.
CATS-P	Inverted signal BT4A-N.
CMD1-N	Auxiliary write command to device indicating output data lines contain data.
CMD2-N	Auxiliary write command to device indicating output data lines contain control information.
DBRA-P, DBRB-P, DBRC-P	Data bus driver enabling signals, asserted during input mode to transmit information on the data bus.
SISP-N, SIST-P	Pseudo data call to initiate write control logic for devices that do not send a data call.
STS1-N	Auxiliary status from write device indicates device is ready to accept another output.



SUE 4601 Paper Tape Controller (PPB), LD2001002137-1 Rev. B, Sheet 9

READ/WRITE ENABLE AND DONE (LD Sheet 10)

The three 50-nanosecond delay lines in series with five inverters provide a total delay of less than 200 nanoseconds after address recognition. The delay allows time for the data lines to settle (deskew) before data is strobed into the receiving elements. The delay line terminates in the Done logic. Flip-flop ADN prevents a false DONE signal if the address is not valid (AABL-P).

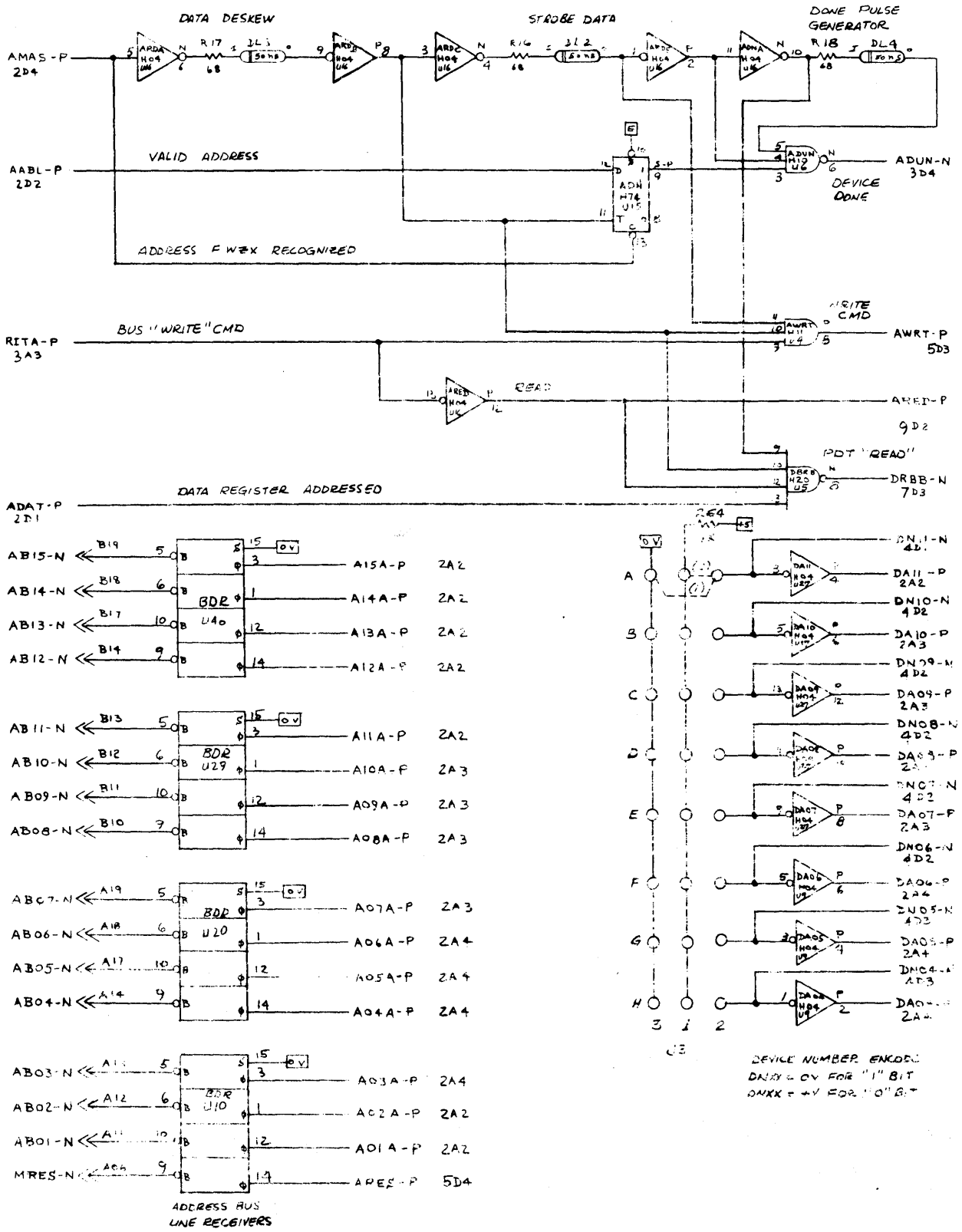
ADDRESS BUS DRIVER/RECEIVERS AND RECOGNITION (LD Sheet 10)

In the address bus drivers/receivers (U10, U20, U29, and U40) only the receivers are used; the drivers are inhibited because the controller never asserts its address on the address bus. The receiver normally assigned to address bit AB00-N, receives master reset pulse MRES-N. AB00-N is not decoded in the controller.

Program plug J3 is used to encode the controller device number for address recognition.

KEY SOURCE LOGIC DEFINITIONS

A01A-P thru A15A-P	Bits from the address receivers used for controller address recognition logic.
AB01-N thru AB15-N	Address bus interfaced to the controller address receivers.
ADUN-N	Address done, generated by the controller at the end of each operation. For a device-write operation ADUN-N indicates that data has been taken from the lines and that lines can be released by the master module. For a read operation ADUN-N indicates that input data on the data lines is valid.
ARED-P	Inverse of the RITE-N signal, ARED-P initiates data bus driver enabling signals during an input operation.
ARES-P	Clears the controller when system reset pulse MRES-N is asserted.
AWRT-P	Derived from RITE-N, the bus write command, AWRT-P enables the output data register during a device output operation.
DA04-P thru DA11-P	Inverse of device number encoded in the controller by jumpers and compared with bits A04A-P through A11A-P, respectively, to accomplish address recognition.
DN04-N thru DN11-N	Device number bits encoded with the controller address and placed on the data bus when the controller goes on line.
DRBB-N	Triggers the read-device-run flip-flop to send run pulse to the read device during PDT mode.
MRES-N	Master reset pulse from the INFIELDS that initiates reset logic in the controller.


DATA DESKEW
STROBE DATA
DONE PULSE GENERATOR
AMAS-P 2D4
VALID ADDRESS
AABL-P 2D2
ADDRESS F W&X RECOGNIZED
ADUN-N 3D4
DEVICE DONE
BUS "WRITE" CMD
RITA-P 3A3
AWRT-P 5D3
READ
AREP-P 9D2
PDT "READ"
DRBB-N 7D3
DATA REGISTER ADDRESSED
ADAT-P 2D1
AB15-N
AB14-N
AB13-N
AB12-N
A15A-P 2A2
A14A-P 2A2
A13A-P 2A2
A12A-P 2A2
AB11-N
AB10-N
AB09-N
AB08-N
A11A-P 2A2
A10A-P 2A3
A09A-P 2A3
A08A-P 2A3
AB07-N
AB06-N
AB05-N
AB04-N
A07A-P 2A3
A06A-P 2A4
A05A-P 2A4
A04A-P 2A4
AB03-N
AB02-N
AB01-N
MRES-N
A03A-P 2A4
A02A-P 2A2
A01A-P 2A2
AREF-P 5D4
ADDRESS BUS LINE RECEIVERS
DA11-P 2A2
DA10-P 2A3
DA09-P 2A3
DA08-P 2A3
DA07-P 2A3
DA06-P 2A4
DA05-P 2A4
DEVICE NUMBER ENCODE
DNXX = 0V FOR "1" BIT
DNXX = +V FOR "0" BIT

Parts List, Assembly Model 4601
PL2001002137-1, Revision D (Sheet 1 of 2)

QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)
000	0001		2001002137-1		ASSY, MODEL 4501		
001	0001		1001004751-1		PRINTED WRG BD, PPP		
000							
043	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R1,4,12,13,19, 23,24,R27 THRU R30,R33 THRU R64 .5 IS
005	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R14,16,17,18,22 .5 IS
001	0001		RL07S361G		RESISTOR	MIL-R-22684/1	R6 .5 IS
001	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R20 .5 IS
003	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R3,10,32 .5 IS
001	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R21 .5 IS
003	0001		RL07S303G		RESISTOR	MIL-R-22684/1	R2,7,31 .5 IS
006	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R5,8,9,15,25,26 .5 IS
033	0001		8001300101		CAPACITOR		C4,5,6,C8 THRU C16,C18,C21 THRU C23,C25 THRU C39,C41,42 .25IS
004	0001		M39003/01-2018		CAPACITOR	MIL-C-39003/1	C1,7,40,43 .8 IS
004	0001		CM05DD221J03		CAPACITOR	MIL-C-5/18A	C2,3,19,20 .25 IS
000							
000							
000							
000							
000							
000							
000							
001	0001		8001100001		DIODE		CR1 .5 IS
005	0001		8001800042		ICP		U17,22,33,36,46 (74H00)
003	0001		8001800046		ICP		U6,21,47 (74H10)
001	0001		8001800047		ICP		U4 (74H11)
004	0001		8001800048		ICP		U5,7,35,37 (74H20)
000							
006	0001		8001800044		ICP		U9,16,27,32,65, 73 (74H04)
003	0001		SN74H74N	01295	ICP	TEXAS INSTR INC	U13,15,44
002	0001		SN74S11N	01295	ICP	TEXAS INSTR INC	U34,75
002	0001		N8203N	18324	ICP	SIGNETICS	U6,72
001	0001		SN7486N	01295	ICP	TEXAS INSTR INC	U7

Parts List, Assembly Model 4601
PL2001002137-1, Revision D (Sheet 2 of 2)

QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)
001	0001		SN7416N	01295	ICP	TEXAS INSTR INC	U52
000							
003	0001		SN74123N	01295	ICP	TEXAS INSTR INC	U2,12,42
002	0001		SN74157N	01295	ICP	TEXAS INSTR INC	U68,78
004	0001		SN74153N	01295	ICP	TEXAS INSTR INC	U48,49,58,59
000							
001	0001		8001800049		ICP		U3 (74H21)
010	0001		8001800120		ICP, DRIVER/RECEIVER		U10,20,29,40,50, 60,69,70,79,80
005	0001		8001600008		DELAY LINE, FIXED		DL1,2,3,4,5
003	0001		SN7417N	01295	ICP	TEXAS INSTR INC	U62,63,72
001	0001		8001800054		ICP		U45 (74H51)
001	0001		8001800057		ICP		U8 (74H54)
001	0001		8001800058		ICP		U64 (74H55)
001	0001		8001800092		ICP		U31 (7451)
000							
002	0001		SN74174N	01295	ICP	TEXAS INSTR INC	U66,76
000							
002	0001		MC3002P	04713	ICP	MOTOROLA	U14,74
003	0001		SN74H52N	01295	ICP	TEXAS INSTR INC	U43,53,54
001	0001		SN74S15N	01295	ICP	TEXAS INSTR INC	U38
001	0001		SN74S112N	01295	ICP	TEXAS INSTR INC	U18
003	0001		N8242A	18324	ICP	SIGNETICS	U19,28,39
001	0001		N8202N	18324	ICP	SIGNETICS	U57
001	0001		3432-1002	26066	CONNECTOR, 40 PIN	3M COMPANY	J1
001	0001		3433-1002	26066	CONNECTOR, 50 PIN	3M COMPANY	J2
119	0001		10050000764-1		PIN, TERMINAL		NOTE 210
REF	0001		LD2001002137-1		LOGIC DIAGRAM, PPB		- - -

PPB

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	REL FOR PROD	5/7/74	
		B	ECN # 0131	2/20/75	
		C	ECN 309	7/13/78	E.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PPB TECHNICAL REFERENCE

SIZE	CODE IDENT NO.	DRAWING NO.
A		PPB-Ø5

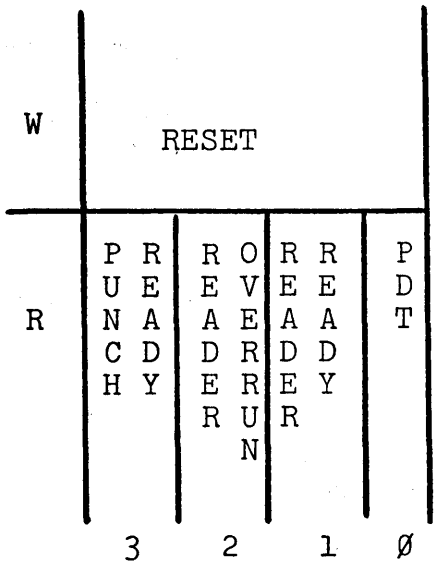
SCALE	REV	SHEET
	C	1 OF 3

PPB

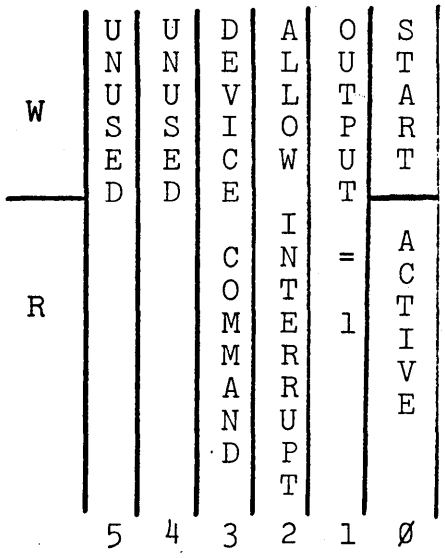
Paper Tape Reader Interface

Status - address FXX0

Control - address FXX6



STATUS



CONTROL

Device Command inhibits Write Command

Switches - none

Jumpers

Address Selection

ADDRESS BIT	FROM	CONNECT TO	
		Ø	1
4	J3-2H	J3-1H	J3-3H
5	J3-2G	J3-1G	J3-3G
6	J3-2F	J3-1F	J3-3F
7	J3-2E	J3-1E	J3-3E
8	J3-2D	J3-1D	J3-3D
9	J3-2C	J3-1C	J3-3C
10	J3-2B	J3-1B	J3-3B
11	J3-2A	J3-1A	J3-3A
12	U39-05	J3-3A	J3-1A

A12 MODIFICATION
'ALLED" (See PSB-Ø5)

PPB

PPB

Bus Service Level

Level	Connect J4	
	From	To
1	1A	2A
	1E	2E
2	1B	2B
	1F	2F
3	1C	2C
	1G	2G
4	1D	2D
	1H	2H

BTA not used with PPB

Connect J5-1 to J5-2

Socket - See PPB prints

Paper Tape Reader -

For use with REMEX reader RR-105/305RA, jumper the bottom-most pair of pins (pins 1 and 2) of the Cannon connector (Connector A) on the IPTR cable.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	REL FOR PROD		
B	ECN. 0131	2/20/75	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE
PPB MODIFICATION, SPECIAL

SIZE	CODE IDENT NO.	DRAWING NO.
A		PPB-14

SCALE	REV	SHEET
	B	1 OF 4

PPB

Card Type PPB **Modification** A12

Card Function:

parallel interface

Modification Description:

allow choice of sense of address bit 12 recognized
either NO, Ø, or 1 must be chosen
for A12=NO do not modify card
for A12=Ø or A12=1 proceed as below

Implementation:

lift leg U39:05 - solder a wire to the leg and wire to pin in J3 row 3 for A12=Ø or a pin in J3 row 1 for A12=1

Card Type PPB **Modification** BUS

Card Function:

parallel interface

Modification Description:

recognize 20 bit addresses

either P or I must be chosen
for BUS = P do not modify card
for BUS = I proceed as below

Implementation:

1. Mount two IC sockets with attached legs (P/N 264) on pieces of foam tape immediately below U38 and U39. Call these locations U38A and U39B.
2. Insert a BDR in U39A and a 74S15 in U38A
3. Drill a 1/16" hole thru the board 3/16" to the left of the left end of the finger at P1:20. Check for shorts between +5 and ground.
4. Wire as follows:

P2:20-U39A:10 }
P2:09-U39A:09 } route through hole drilled in step 3.
P1:20-U39A:05
P1:09-U39A:06
U39A:07-U39A:08-U39A:15-U39:07
U39A:12-U38A:01
U39A:14-U38A:02
U39A:03-U38A:13
U39A:01-U38A:09-U38A:10-U38A:11
U38A:08-U38A:12-U39:11
U39A:16-U39:14
U38A:14-U38:14
U38A:07-U38:07

Card Type PPB - Modification ADDR

Card Function:

parallel interface

Modification Description:

set address recognition

Implementation:

jumper J3 according to * and -

* means jumper from row 2 to row 3
- means jumper from row 2 to row 1

PPB

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	REL FOR PROD	5/7/74	
B	ECN # 0131	2/20/75	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PPB MODIFICATION, STANDARD

SIZE	CODE IDENT NO.	DRAWING NO.
A		PPB-15

SCALE	REV	SHEET
	B	1 OF 3

PPB

Card Type PPB Modification Standard

Card Function: Peripheral Parallel Interface

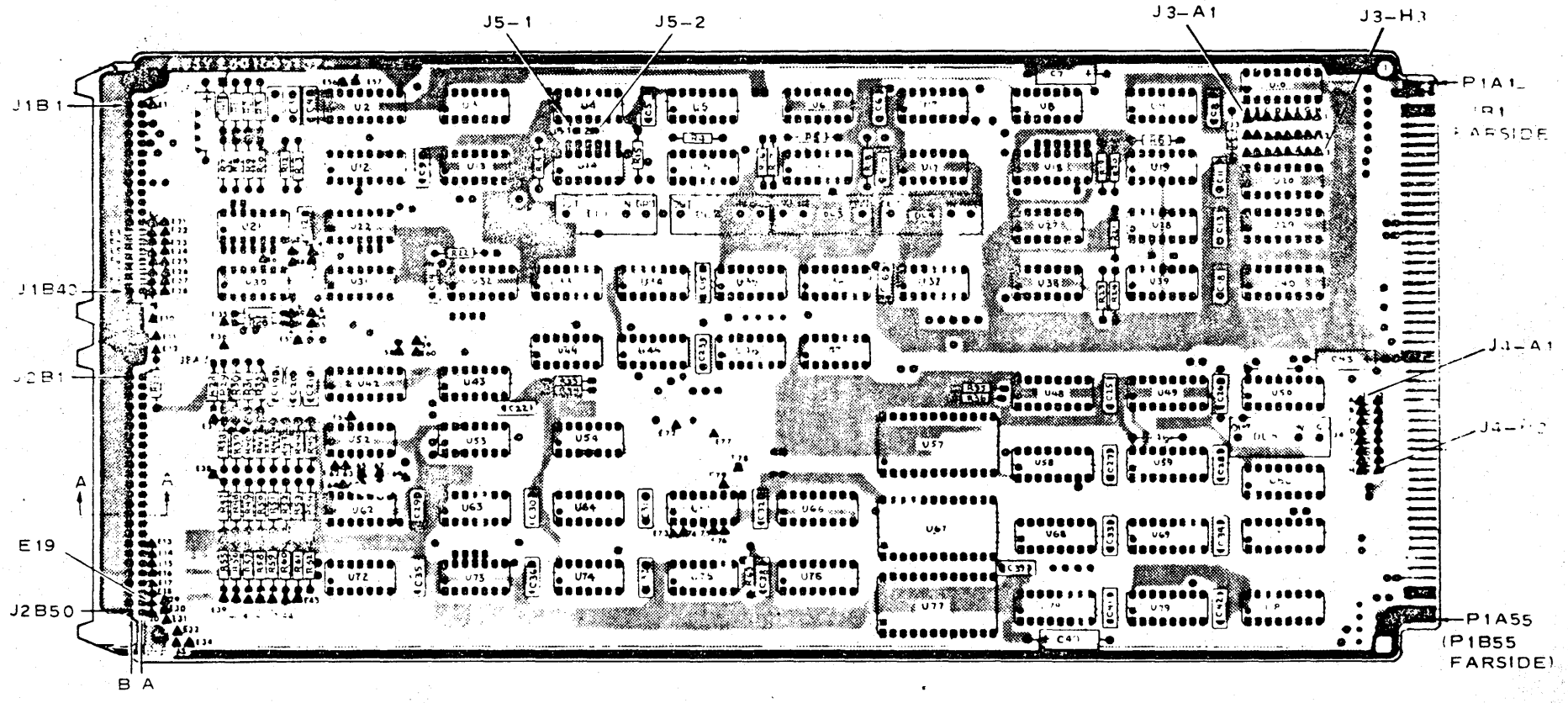
Modification Description:

Configure card to operate without BTA.

Implementation:

Jumper with wrapped 30 ga wire as follows:

J5-1 to J5-2


J5-1
J5-2
J3-A1
J3-H1
P1A1
(P1B1
FARSIDE)
J1B1
J1B40
J2B1
J2B50
E19
A
A
B A
REF
P1A55
(P1B55
FARSIDE)
J1-A1
A
B
B A
SECTION A-A

4501-M03-72