APPLICATION		G01	REVISION		
NEXT ASSEMBLY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		PA	Release per ECO #		

PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES ANGLES ±

FRACTIONS ±

3 PLACE DECIMALS ±

2 PLACE DECIMALS ±

1 PLACE DECIMALS ±

MATERIAL:

CONTR NO.

DR K McGrattan 11/07/90

CHK

APPD

APPROVED

BY DIRECTION OF

BBN Manufacturing Corporation

Billerica, MA

Drawing Title

TC/CTI TCS Slave: Functional Specification

Size		Drawing No.
A	63942	FS19693G01
Scale		Sheet 1 of 30

TC/CTI TCS Slave Processor Firmware Specification

1.1 Introduction

The TC/CTI card is the integrated TCS master and master clock generator for the TC2000. It is equipped with a TC2000 Test and Control System (TCS) Slave Processor, a Motorola 68HC11 single chip microcomputer. The programmed device impements Master/Slave communication and circuit board control defined in the *Butterfly 2 Technical Reference Guide*.

This document defines the TCS Bus commands defined for a TC/CTI Slave Processor, BBN programmed part number 4619693G01.

1.2 TCS Messages

There are three types of TCS message defined for the TC/CTI:

- Register Access Request
- Read Time Interval (Memory Read Request)
- Set Up PLL Programming Data (Memory Write Request)

The read and write memory messages are implemented in the TC/CTI TCS slave processor even though the TC/CTI has no memory. The memory message format is used to exchange 16 bit time information with the TCS master processor, and to program the board's Phase Lock Loop (PLL) frequency synthesizer.

1.2.1 Slave Addressing

The TC/CTI Level 1 slave is always in in Bay 0 with MS_SLOT_ID = 0x00 and LS_SLOT_ID = 0x0A. The TC/CTI Level 2 slave has an associated Bay number from 0 to 7. Its LS_SLOT_ID is 0x1A and its MS_SLOT_ID = 0000 1 BAY_ID<2..0>.

The TC/CLK slave is initialized to broadcast group 0x02. The slave carries out requests broadcast to this group, but does not respond. An EEPROM register defines the slave's group. It may be modified using EEPROM write commands.

1.2.2 Register Access Messages

There are five types of register access message:

Action Registers — Action registers perform a sequence of actions on the target circuit card that hide board specific, and 68HC11 details.

EEPROM Registers — EEPROM registers store board specific information in slave processor non-volatile memory.

Gate Array Registers — The TC/CTI's gate array message programs the phase lock loop used to generate clock. (The TC/CTI gate array register message is different from the that of other cards.)

Hardware Registers — Hardware write registers load board control registers. Hardware read registers monitor board status signals and data bits.

Shadow Registers -- These include the Hardware Write registers RAM shadow copy and an additional nine RAM locations that can be used by TEX for general purpose storage.

1.2.3 TC/CTI Memory Messages

Memory Access Set-Up — Not Implemented. Returns Format NACK.

Read Time Interval (Memory Read) — In the TC/CTI the memory read message is actually a *Time Interval Read*. It returns a two byte time value, of 4 micro-seconds per tick. There are 5 different memory read messages distinguished between with the command modifier field of the TCS memory message. One version of the memory read command reads back the programming information set up by a PLL programming set up message (see below).

Set Up PLL Programming Data (Memory Write) — Stores four bytes of programming information in slave processor RAM. These values are loaded into the phase lock loop's control registers in response to a "read time to lock" message.

1.3 Message Formats

There are three message types defined by the TC/CTI Slave. These are described below.

1.3.1 Register Access Message

The register command accesses the four different kinds of Slave register: Action Registers, Gate Array Registers, Hardware Registers, and EEPROM Registers. Each of these four kinds use the following message format. (The P in the following message format diagrams is message parity. This parity is calculated as the exclusive XNOR over the entire message.)

Register Access Request

bit: 8	7	6	5	4	3	2	1	0
1	P	0						
0	LS_SLOT_ID							
0	CMD MOD				CMD TYPE			
0	ADDRESS							
0	DATA							

Positive Reply

1	MASTER ADDRESS							
0	P	ACK CODE						
0	DATA							

Negative Reply

1	MASTER ADDRESS							
0	NACK CODE							

Register Access Message Format
Figure 1-1

1.3.2 Phase Lock Loop Gate Array Access Message

The phase lock loop programming message programs either of the two registers within the device. The message uses the gate array register command type, and redefines the message's fourth byte to be address and data rather than just data.

Bit<7> of the fourth byte selects between register 0 and register 1, each of which define 15 data bits.

Register Access Request

bit:	8	7	6	5	4	3	2	1	0
1	P	0							
0	LS_SLOT_ID								
0	Don't Care					1	0	0	1
0	Add Bit	Prog Data <14..8>							
0	Prog Data<7..0>								

Positive Reply

1	MASTER ADDRESS	
0	P	0x0B
0	0x00	

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

Phase Lock Loop Programming Message
Figure 1-2

1.3.3 Read Time Interval (Memory Read Request)

The read time interval message returns one of four different time values or PLL programming information. The four different values, or registers, are selected using the command modifier field (CMD MOD) of the TCS message.

All time values are returned in units of 4 micro-seconds per tick.

CMD MOD	Description
0	Read the time between the next two transitions on the PLL test pin.
1	Read the time between the next two transitions on the External 65 mS clock.
2	Read the time between the next two transitions on the Internal 65 mS clock.
3	Initializes the PLL with the data previously written with a PLL program setup message, and returns the time it takes for the device to achieve lock.
4	Returns the four bytes of PLL programming information sent by the last PLL programming set up message.
5	Read the time between the next two transitions on the External Hold clock.
6	Read the time between the next two transitions on the Internal Hold clock.

Time Interval Read Request

bit: 8 7 6 5 4 3 2 1 0

1	P	0
0	LS_SLOT_ID	
0	CMD MOD	0 0 0 0

Positive Reply

1	MASTER ADDRESS	
0	P	ACK CODE
0	0	
0	0	*PLL Data 0 <14..8>*
0	*PLL Data 0 <7..0>*	
0	Time Data<15..8>	
0	Time Data<7..0>	

These byte are non-zero only for CMD MOD = 4.

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

Time Interval Read Message Format
Figure 1-3

1.3.4 Set Up PLL Programming Data (Memory Write Message)

The memory write message loads phase lock loop programming information into the Slave processor RAM for future use by the "program PLL and read time to lock" message.

The most significant bit of each of the two sixteen bit PLL programming words must be set as shown in Figure 1-4.

Set Up PLL Programming Data Request
(Memory Write Request)

bit:	8	7	6	5	4	3	2	1	0
1	P	0							
0	LS_SLOT_ID								
0	Don't Care				0	0	0	1	
0	0	PLL Data 0 <14..8>							
0	PLL Data 0 <7..0>								
0	1	PLL Data 1 <14..8>							
0	PLL Data 1 <7..0>								

Positive Reply

1	MASTER ADDRESS	
0	P	0x09
0	0x00	

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

Set up PLL Programming Data Message Format
Figure 1-4

1.4 Command Byte Decoding

Cmd Type, Cmd Mod		Description
Memory Read Messages		
0	0	Measure Time Between Transitions on PLL Test Pin
	1	Measure Time Between Transitions on External 65 mS Clock
	2	Measure Time Between Transitions on Internal 65 mS Clock
	3	Program PLL and Measure time to lock
	4	Read back the last PLL programming information set up
	5	Measure Time Between Transitions on External Hold Clock
	6	Measure Time Between Transitions on Internal Hold Clock
	7-15	Illegal Commands
Memory Write Messages		
1	Don't Care	Load PLL Programming Information into Slave RAM
Memory Set-Up Message		
2,3	Don't Care	Illegal Commands
Register Access Messages		
Action Registers		
4	Don't Care	Action Register Read (See List of Action Registers)
5	Don't Care	Action Register Write (See List of Action Registers)
EEPROM Registers		
6	Don't Care	EEPROM Register Read (See EEPROM Register List)
7	Don't Care	EEPROM Register Write (See EEPROM Register List)
Gate Array Registers		
8,9	Don't Care	Program the Phase Lock Loop (See special description)
Hardware Registers		
10	0	Read Hardware Register 0
	1	Read Hardware Register 1
	2	Read Hardware Register 2
	3	Read Hardware Register 3
	4	Read Hardware Register 4
	5	Read Hardware Register 5
	6	Read Hardware Register 6
	7	Read Hardware Register 7
	8	Read Hardware Register 8
	9	Read Hardware Register 9
	10-15	Not Implemented
11	0	Write Hardware Register 0
	1	Write Hardware Register 1
	2	Write Hardware Register 2
	3	Write Hardware Register 3
	4	Write Hardware Register 4
	5	Write Hardware Register 5
	6	Write Hardware Register 6
	7-15	Not Implemented
Shadow Registers		
12	0	Read Hardware Shadow Register 0
	1	Read Hardware Shadow Register 1
	2	Read Hardware Shadow Register 2
	3	Read Hardware Shadow Register 3

	4	Read Hardware Shadow Register 4
	5	Read Hardware Shadow Register 5
	6	Read Hardware Shadow Register 6
	7	Read Shadow Register 7
	8	Read Shadow Register 8
	9	Read Shadow Register 9
	10	Read Shadow Register 10
	11	Read Shadow Register 11
	12	Read Shadow Register 12
	13	Read Shadow Register 13
	14	Read Shadow Register 14
	15	Read Shadow Register 15
13	0	Write Hardware Shadow Register 0
	1	Write Hardware Shadow Register 1
	2	Write Hardware Shadow Register 2
	3	Write Hardware Shadow Register 3
	4	Write Hardware Shadow Register 4
	5	Write Hardware Shadow Register 5
	6	Write Hardware Shadow Register 6
	7	Write Shadow Register 7
	8	Write Shadow Register 8
	9	Write Shadow Register 9
	10	Write Shadow Register 10
	11	Write Shadow Register 11
	12	Write Shadow Register 12
	13	Write Shadow Register 13
	14	Write Shadow Register 14
	15	Write Shadow Register 15

1.5 Action Register List

The TCS message's address byte selects which register is accessed.

The TCS message's data byte is unused in the read message, and conveys write data in the write message.

Reg. Number		Description	Read/Write
0	(0x00)	Board Status Register	(read only)
1	(0x01)	Slave Ready Control Register	(write only)
2	(0x02)	Power Control Register	(write only)
3	(0x03)	Previous ACK/NACK	(read only)
4	(0x04)	Clock Activity Check Register	(read only)
5	(0x05)	EEPROM Write Enable	(write only)
6	(0x06)	Board Ambient Temperature	(read only)
7	(0x07)	Read/Write RAM register	(read/write)
8	(0x08)	Slave Address Re-Read Command	(write only)
9	(0x09)	Illegal Command	(n/a)
10	(0x0A)	5 VDC Voltage Level	(read only)
11	(0x0B)	-4.5 VDC Voltage Level	(read only)
12	(0x0C)	-2 VDC Voltage Level	(read only)
13	(0x0D)	LED Control	(write only)
14	(0x0E)	8 VDC Voltage Level	(read only)
15	(0x0F)	-5.2 VDC Voltage Level	(read only)
16	(0x10)	Illegal Command	(n/a)
17	(0x11)	Illegal Command	(n/a)
18	(0x12)	Phase Lock Loop Control Voltage	(read only)
19	(0x13)	Aligned Hardware Register 0	(read only)
20	(0x14)	Aligned Hardware Register 1	(read only)
21	(0x15)	Aligned Hardware Register 2	(read only)
22	(0x16)	Aligned Hardware Register 3	(read only)

1.6 EEPROM Register List

Reg. Number		Description	Read/Write
0	(0x00)	Card Type	(read/write)
1-16	(0x01-10)	Serial Number	(read/write)
17,18	(0x11,12)	Artwork Revision Level	(read/write)
19,20	(0x13,14)	Electrical Revision Level	(read/write)
21,22	(0x15,16)	TCS Slave Code Revision Level	(read/write)
23	(0x17)	Temperature Alarm Setpoint	(read/write)
24	(0x18)	Vcc Nominal A/D Reading	(read/write)
25	(0x19)	Vcc Alarm Magnitude	(read/write)
26	(0x1A)	Vtt Nominal A/D Reading	(read/write)
27	(0x1B)	Vtt Alarm Magnitude	(read/write)
28	(0x1C)	Vee Nominal A/D Reading (10K)	(read/write)
29	(0x1D)	Vee Alarm Magnitude (10K)	(read/write)
30	(0x1E)	Board Group Identifier	(read/write)

1.7 Gate Array Register List

There is only one form of gate array access message. It programs either of the two registers within the phase lock loop.

Reg. Number	Description	Read/Write
Don't Care	Program Phase Lock Loop	(write only)

1.8 Hardware Register List

Hardware registers are selected using the command byte. The address byte is not used.

Reg. Number		Description	Read/Write
Write Registers			
0	(0x00)	TCS Bus Enable<7..0>	(write only)
1	(0x01)	LED, Internal/External 65 msec/Hold Mux Select, S/R Net Fan I/O	(write only)
2	(0x02)	65 msec Prescale, 65 msec Test Mode Select	(write only)
3	(0x03)	Hold Time Control	(write only)
4	(0x04)	Voltage Margin, Crystal/PLL Select, Margin Enable, PDU Control <9..8>, Relay Control	(write only)
5	(0x05)	PDU Control <7..0>	(write only)
6	(0x06)	Fan-In Control <7..0>	(write only)
Read Hardware Registers			
1-9	(0x01-0x09)	*See Hardware Register Definitions*	(read/write)

1.9 Hardware Shadow Register List

Hardware Shadow registers are selected using the TCS message command modifier field. The TCS message address byte is not used by Hardware Shadow Register accesses. Hardware Shadow Register access is read/write.

Note that the Hardware Shadow Registers can be written independently of the actual Hardware Registers. If this is done it can lead to inconsistencies between the state of the actual TC/CTI board and the slaves knowledge of the TC/CTI board. As the actual Hardware Reg-

isters do not have readback capability, this can be fatal. Program these registers with caution!

Reg. Number		Description	Read/Write
Write Registers			
0	(0x00)	TCS Bus Enable<7..0>	(read/write)
1	(0x01)	LED, Internal/External 65 msec/Hold Mux Select, S/R Net Fan I/O	(read/write)
2	(0x02)	65 msec Prescale, 65 msec Test Mode Select	(read/write)
3	(0x03)	Hold Time Control	(write only)
4	(0x04)	Voltage Margin, Crystal/PLL Select, Margin Enable, PDU Control <9..8>, Relay Control	(read/write)
5	(0x05)	PDU Control <7..0>	(read/write)
6	(0x06)	Fan-In Control <7..0>	(read/write)
7	(0x07)	Reserved for TEX	(read/write)
8	(0x08)	Reserved for TEX	(read/write)
9	(0x09)	Reserved for TEX	(read/write)
10	(0x0A)	Reserved for TEX	(read/write)
11	(0x0B)	Reserved for TEX	(read/write)
12	(0x0C)	Reserved for TEX	(read/write)
13	(0x0D)	Reserved for TEX	(read/write)
14	(0x0E)	Reserved for TEX	(read/write)
15	(0x0F)	Reserved for TEX	(read/write)

1.9 Action Register Definitions

Action Register 0. Board Status (read only)

Temp Okay	PLL Test	Power Okay	Spare	Broad-cast Error	Zero	Serial Comm. Error	Slave Proc. Error

Temp Okay
: Temperature okay. Indicates that the board's temperature is below the value set in the slave's EEPROM temperature alarm register. Note: The slave sets the LED to blink at a fast rate if the temperature ever exceeds the alarm value. If the temperature has returned to normal since the event, the register read returns the error value (zero) and resets the bit to one.

PLL Test
: Indicates the state of the PLL's test pin. When the PLL is programmed appropriately, this pin indicates that the phase lock loop has achieved lock (1 = lock).

Power Okay
: Indicates that board power supply voltage levels are within the limits specified in the slave's EEPROM registers. Specificaly monitors the +5V, -5.2V, and -2V power supplies. This provides maximum power system coverage.

Broadcast Error
: Indicates that a broadcast message to this slave has resulted in a negative acknowledgement since the last time the status register was read. This bit is cleared by reading the status register.

Serial Comm. Error
: Indicates that a receiver serial communications error was detected by the slave's serial communication hardware since the last read of the status register. This bit is cleared by a read of the status register.

Slave Processor Error
: Indicates that the slave processor software entered an illegal state since the last time the status register was read. If this bit is set frequently either the slave processor must be replaced, or there is a bug in the slave software.

Action Register 1. Slave Ready (write only)

Spare	Spare	Spare	Spare	Spare	Spare	Spare	Slave Ready

Slave Ready
: Sets and clears the SLAVE READY bit on the TC/TCI slave. This signal is set to one at the end of slave initialization by default.

Action Register 2, Power Control Register (write only)

Spare	Spare	Spare	Spare	Power Margin Level<1>	Power Margin Level<0>	Power Margin Enable	Spare

Power Margin Level<1..0>
Selects the voltage level that the board's power supplies are set to when margining is enabled.

00 = -10%
01 = -5%
10 = +5%
11 = +10%

Power Margin Enable
Sets the board's power supplies to the voltage level selected by the power margin level bits.

Power On
Turns the board power supplies on. Note: The slave only turns power on in response to an individually addressed message; never a broadcast message.

Action Register 3, Previous Message Ack/Nack (read only)

This register always contains the Ack/Nack byte of the previous TCS message. Reading this register clears it.

Spare	Ack Nack Code<5>	Ack Nack Code<4>	Ack Nack Code<3>	Ack Nack Code<2>	Ack Nack Code<1>	Ack Nack Code<0>	Ack Bit

Ack/Nack Code<5..0>
This is an acknowledgment code for TCS messages. It is either a positive or negative acknowledgment depending on the sense of the Ack bit in this register.

Nack codes

0 - Null Description
1 - Timeout
2 - Parity Error
3 - Serial Communication Error
4 - Spare
5 - TCS Message Format Error

Ack Codes

0 - Action Register Acknowledge
1 - EEPROM Register Acknowledge
2 - Setup Message Acknowledge
3 - Memory Read Message Acknowledge
4 - Memory Write Message Acknowledge
5 - Gate Array Register Acknowledge
6 - Hardware Register Acknowledge

Ack Bit
This bit indicates that the code is an acknowledgment.

Action Register 4. Clock Check (read only)

Indicates whether transitions were detected on signals during a monitoring period. A one indicates that the Slave detects transitions on the corresponding signal. One by one the slave watches the clock signals for rising edges. Each clock is watched for up to 150 msec. If none are detected, the signal's bit position is reset to zero.

Note: If both signals are quiescent, this register takes 300 msec to respond.

Spare	Spare	Spare	Spare	Ext Hold	Ext 65mS	Local Hold	Local 65mS

Action Register 5. EEPROM Access Enable (write only)

Writing this register with any data enables an EEPROM register write on the next access. This register must be written before each EEPROM write, otherwise a format nack is returned.

Action Register 6. Board Ambient Temperature (read only)

This register returns the board's ambient temperature at 0.977 °F per tick.

Action Register 7. RAM Test, PLL Programming Temporary Register (read/write)

This register is a one byte piece of read/write RAM for testing communication with the TCS Master. Anything may be written into it.

This register is also used as a temporary holding register for PLL programming information. See the section on reading TC/CLK time intervals in this document.

Action Register 8. Slave Address Re-Read (write only)

Writing this register causes the slave to re-read its address from the rack and cabinet pins of the midplane and reinitialize itself based on what it finds. The write data is ignored, and the response message returns a zero in the data field.

Action Register 9. NOT IMPLEMENTED

Fromerly TCS Vcc Voltage Sensor (read only)

Action Register 10. Vcc Voltage Sensor (read only)

This register returns the voltage detected on the board's +5 VDC supply at 24.5 mV per tick. The voltage is calculated with the following formula:

Millivolts = (register value)*(24.4 mv/tick)

Action Register 11. Vee Voltage Sensor (read only)

This register returns the voltage detected at the board's -4.5 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(36.7 mv/tick) - 6863 mv

Action Register 12. Vtt Voltage Sensor (read only)

Bulk Vtt termination power supply voltage sensing register.

This register returns the voltage detected at the board's -2 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(22.8 mv/tick) - 3325 mv

Action Register 13. LED Control (write only)

This register controls the indicator LED. The LED is turned on by a power on reset and is left on until instructed otherwise. Writing the following values to the LED control register results in the called out LED state.

0 - LED off
1 - LED flash at 1 Hz
2 - LED flash at 2 Hz
3 - LED constant on
4-255 - Not Defined

Action Register 14. 8 VDC Voltage Sensor (read only)

This register returns the voltage detected on the 8 VDC supply 40 mv per tick. The voltage is calculated with the following formula:

Millivolts = (register value)*(40 mv/tick)

Action Register 15. -5.2 VDC Voltage Sensor (read only)

This register returns the voltage detected on the -5.2 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(41.5 mv/tick) - 8099 mv

Action Register 16. NOT IMPLEMENTED

Formerly +24 VDC Voltage Sensor (read only)

Action Register 17. NOT IMPLEMENTED

Formerly -24 VDC Voltage Sensor (read only)

Action Register 18. Phase Lock Loop Control Voltage Sensor (read only)

This register returns the voltage detected at the phase lock loop's control voltage pin at 36.3 mv per tick. The value is calculated with the following formula:

Millivolts = (register value)*(36.3 mv/tick)

Action Register 19. Collected Hardware Register 0 (read only)

This register returns values that are also available via the hardware read registers. This and the following three registers read back two associated nibbles from the four readback mutliplexers and assemble the data into a single one byte value.

Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0

Action Register 20. Collected Hardware Register 1 (read only)

PDU ACK 7	PDU ACK 6	PDU ACK 5	PDU ACK 4	PDU ACK 3	PDU ACK 2	PDU ACK 1	PDU ACK 0

Action Register 21. Collected Hardware Register 2 (read only)

PDU ACK 9	S Phase B	M Phase B	R Phase B	PDU ACK 8	S Phase A	M Phase A	R Phase A

Action Register 22. Collected Hardware Register 3 (read only)

Termination Jumper Position Chan 7	Termination Jumper Position Chan 6	Termination Jumper Position Chan 5	Termination Jumper Position Chan 4	Termination Jumper Position Chan 3	Termination Jumper Position Chan 2	Termination Jumper Position Chan 1	Termination Jumper Position Chan 0

Termination Jumper Position<7..0>

This bit returns the position of the corresponding channel's termination jumper.

0 = Channel unterminated
1 = Channed terminated

1.10 EEPROM Register Definitions

Slave EEPROM writes take about 20 ms to complete. The Master processor must take into account the long time it takes for the Slave to acknowledge these messages.

The TCS message address byte is the EEPROM register number. The data byte is unused in the Read message, and conveys data to be written in the write message.

All EEPROM registers are read/write.

EEPROM Register 0, Card Type

One byte register allocated for storing the card type. The card type is an ASCII character.

EEPROM Registers 1-16, Board Serial Number

Board serial number registers. This is a block of 16 bytes allocated for storing the BBN board serial number in ASCII format. The least significant character is in register 1.

EEPROM Registers 17 and 18, Artwork Revision Level

Revision level of the printed circuit board part of the board assembly. These registers hold two ASCII characters that represent the revision level of the circuit card. The least significant character is in register 17.

EEPROM Registers 19 and 20, Electrical Revision Level

The revision level of the circuitry of the circuit board. This is used to keep track of the implementation of Engineering Change Orders (ECOs) on the circuit card. These registers hold two ASCII characters that represent the electrical revision level of the circuit card. The least significant character is in register 19.

EEPROM Registers 21 and 22, Slave Software Revision Level

Revision level of the firmware in the 68HC11. This is a two character alphanumeric value. The least significant character is in register 21.

EEPROM Register 23, Temperature Alarm Setpoint

This register contains the analog to digital converter reading at which the slave considers the board too hot. At this value the slave flashes the LED at the fastest rate and flags temperature error in the board status register. The units of this register are the same as for the temperature sensor action register: 0.977 °F per tick.

EEPROM Register 24, A/D Converter Vcc Nominal Reading

This register stores the analog to digital converter reading that results when the Vcc power supply is at 5.00 VDC. This register is programmed at the factory, and is referenced by the TCS master processor when reading the Vcc voltage sensing register. This calibrates the results for analog component tolerances. The register's units are the same as those of the Vcc voltage sensing action register: 24.4 mV per tick.

EEPROM Register 25, Vcc Voltage Alarm Magnitude

This register contains the maximum deviation from nominal, tolerable on Vcc before a voltage alarm is signaled in the board status register. The register's units are the same as those of the Vcc voltage sensing action register: 24.4 mV per tick.

EEPROM Register 26, A/D Converter Vtt Nominal Reading

Stores the nominal reading of Vtt (-2.0V)

EEPROM Register 27, Vtt Voltage Alarm Magnitude

Stores the maximum allowable Vtt voltage deviation from nominal before a voltage alarm is signalled in the status register.

EEPROM Register 28, A/D Converter 10K Vee Nominal Reading

Stores nominal reading of the 10K ECL Vee (-5.2V).

EEPROM Register 29, 10K Vee Voltage Alarm Magnitude

Stores the maximum allowable 10K Vee voltage deviation from nominal before a voltage alarm is signalled in the status register.

EEPROM Register 30. Board Group ID

Stores the board's broadcast group identifier. When the slave receives a broadcast message it compares the LS_SLOT_ID to this register to determine whether the message is meant for this board's broadcast group.

1.11 Hardware Register Definitions

The hardware registers are the raw registers the slave has access to.

The command modifier field of the TCS message command byte specifies which parallel register to read or write. The address byte is unused. The data byte specifies write data, if any.

1.11.1 Hardware Write Registers

Write Register 0, TCS Bus Enable Register (write only)

TCS from Cable J7	TCS from Cable J6	TCS from Cable J5	TCS from Cable J4	TCS from Cable J3	TCS from Cable J2	TCS from Cable J1	TCS from Cable J0

TCS from Cable J<7..0>
Enables communication from the clock cable plugged into the corresponding connector on the TC/CLK.
0 = Disable communication
1 = Enable communication

Write Register 1, Fan-in/Fan-out Control, Clock Source Select, LED Control (write only)

This register performs some miscellaneous control.

Reset Net Fan-out	Set Net Fan-out	Reset Net Fan-in	Set Net Fan-in	65 mS Hold-Sel<1>	65 mS Hold Sel<0>	LED Control	Spare

Reset Net Fan-out

Set Net Fan-out

Reset Net Fan-in

Set Net Fan-in

65 mS/Hold Sensor Select<1..0>
Controls which of the four Internal/External 65mS/Hold signals is fed into the Pulse Accumulator and Input Capture Port 3 of the slave.
0 = Local 65mS
1 = Local Hold
2 = External 65mS
3 = External Hold

LED Control
Controls the boards yellow indicator LED
0 = On
1 = Off

Write Register 2. 65mS Test Mode Control. 65 msec Clock Prescale

This register selects the normal or 65mS test mode. This register also controls the timing of the 65 msec clock signal.

Test 65 mS Mode	Spare>	Spare	65 msec scale<4>	65 msec scale<3>	65 msec scale<2>	65 msec scale<1>	65 msec scale<0>

Test 65 mS Mode
Selects either the normal 65 mS clock or high speed version for oscilloscope visibility.

0 = Normal 65 mS clock
1 = High speed (undivided) 65 mS clock

65 Msec Scale<4..0>
Controls the frequency of the 65 msec clock signal relative to system clock (requestor and server clock). These bits are programmed with the value:

((system frequency)/2e6) - 1

Write Register 3. Hold Time Control

This register controls the frequency of the hold time signal relative to system clock.

Hold Time Control<7..0>

Hold Time Control<7..0>
The value written to this register sets the ratio of system clock frequency to hold time frequency.

R Clock freq./Hold Time freq. = 32 + (16*(Hold Time Control<7..0>))

Write Register 4, Relay Control, PDU Control, Voltage Margin Enable, Clock Source Select, Voltage Margin Select

This register selects where the board's clock originates. It can be sourced by either a crystal oscillator or a programmable phase locked loop. This register also selects the board's voltage margin level. Voltage margining is enabled in hardware write register 1.

Note: PLL cannot function when the crystal is selected as the clock source. This means that the "PLL test" pin is stuck.

Relay 2 On	Relay 1 On	PDU CTL 9	PDU CTL 8	Voltage Margin Enable	Select Crystal	Voltage Margin Sel<1>	Voltage Margin Sel<0>

Relay Control <2..1>
Turns on the relays used to control standard PDU via contact closure.
0 = Relay OPEN
1 = Relay CLOSED

PDU Control <9..8>
Turns on the corresponding PDU in new hierarchical power control scheme (not currently implemented).

Voltage Margin Enable
Turns on voltagre margining for the board power supplies that have this capability (+5.2 volts and -2 volts)
0 = Maintain the nominal voltage
1 = Margin the voltage

Select Crystal
Setting this bit makes a crystal oscillator the main clock source for the TC/CLK. Clearing it makes the programmable phase locked loop the main clock source.

Voltage Margin Select Values <1..0>
These bits select the magnitude voltage change that occurs in the board power supplies in response to clearing "voltage margin disable" in write register 1. Note: A positive margin value moves the voltage farther from ground. The resulting voltage deviations are:

00 = -10%
01 = -5%
10 = +5%
11 = +10%

Write Register 5, PDU Control <7..0)

PDU Control <7..0>
Turns on the corresponding PDU in new hierarchical power control scheme (not currently implemented).

PDU CTL 7	PDU CTL 6	PDU CTL 5	PDU CTL 4	PDU CTL 3	PDU CTL 2	PDU CTL 1	PDU CTL 0

Write Register 6. Fan-in Control <7..0>

Fan-in Control <7..0>
Passes Fan-in Control signals down to TC/CS to select path that is connected back to TCS.

0 = Fan-in path disabled
1 = Fan-in path enabled

Fan-in CTL 7	Fan-in CTL 6	Fan-in CTL 5	Fan-in CTL 4	Fan-in CTL 3	Fan-in CTL 2	Fan-in CTL 1	Fan-in CTL 0

1.11.2 Hardware Read Register List

Read Register 0 (read only)

No Connect	No Connect	No Connect	No Connect	Termination Jumper Position Chan 3	Termination Jumper Position Chan 2	Termination Jumper Position Chan 1	Termination Jumper Position Chan 0

Termination Jumper Position Channel<3..0>
This bit returns the position of the channel <3..0> termination jumper.

0 = Channel terminated
1 = Channed unterminated

Read Register 1 (read only)

No Connect	No Connect	No Connect	No Connect	Termination Jumper Position Chan 7	Termination Jumper Position Chan 6	Termination Jumper Position Chan 5	Termination Jumper Position Chan 4

Termination Jumper Position Channel<7..4>
This bit returns the position of the channel <7..4> termination jumper.
0 = Channel terminated
1 = Channed unterminated

Read Register 2 (read only)

No Connect	No Connect	No Connect	No Connect	Phase Chan 3	Phase Chan 2	Phase Chan 1	Phase Chan 0

Phase Channel<3..0>
This bit returns the level of the channel <3..0> phase signal.
0 = Signal connected
1 = Open circuit pull-up

Read Register 3 (read only)

No Connect	No Connect	No Connect	No Connect	Phase Chan 7	Phase Chan 6	Phase Chan 5	Phase Chan 4

Phase Channel<7..4>
This bit returns the level of the channel <7..4> phase signal.
0 = Signal connected
1 = Open circuit pull-up

Read Register 4 (read only)

No Connect	No Connect	No Connect	No Connect	PDU ACK Chan 3	PDU ACK Chan 2	PDU ACK Chan 1	PDU ACK Chan 0

PDU Acknowledge Channel<3..0>
This bit returns the level of the channel <3..0> PDU-ACK signal.
0 = Signal connected
1 = Open circuit pull-up

Read Register 5 (read only)

No Connect	No Connect	No Connect	No Connect	PDU ACK Chan 7	PDU ACK Chan 6	PDU ACK Chan 5	PDU ACK Chan 4

PDU Acknowledge<7..4>
This bit returns the level of the channel <7..4> PDU-ACK signal.
0 = Signal connected
1 = Open circuit pull-up

Read Register 6 (read only)

No Connect	No Connect	No Connect	No Connect	PDU ACK Chan 8	S-Clock Phase Jumper Position A Clk	M-Clock Phase Jumper Position A Clk	R-Clock Phase Jumper Position A Clk

PDU Acknowledge<8>
This bit returns the level of the channel <8> PDU-ACK signal.
0 = Signal connected
1 = Open circuit pull-up

A/S-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal S-Clock for the A clock.
0 = Jumper installed
1 = Open circuit pull-up

A/M-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal M-Clock for the A clock.
0 = Jumper installed
1 = Open circuit pull-up

A/R-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal M-Clock for the A clock.
0 = Jumper installed
1 = Open circuit pull-up

Read Register 7 (read only)

No Connect	No Connect	No Connect	No Connect	PDU ACK Chan 9	S-Clock Phase Jumper Position B Clk	M-Clock Phase Jumper Position B Clk	R-Clock Phase Jumper Position B Clk

PDU Acknowledge<9>
This bit returns the level of the channel <9> PDU-ACK signal.
0 = Signal connected
1 = Open circuit pull-up

B/S-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal S-Clock for the A clock.
0 = Jumper installed
1 = Open circuit pull-up

B/M-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal M-Clock for the A clock.

0 = Jumper installed
1 = Open circuit pull-up

B/R-Clock Phase Jumper Position
Returns the position of the phase jumper that affects the signal M-Clock for the A clock.

0 = Jumper installed
1 = Open circuit pull-up

Read Register 8 (read only)

No Connect	No Connect	No Connect	No Connect	0	0	Net Fan-Out	Net Fan-In

Always readback = 0

Net Fan-out signal

Net Fan-in signal

Read Register 9 (read only)

No Connect	No Connect	No Connect	No Connect	L1 / L2 Clock Select Jumper	BAY_ID <2>	BAY_ID <1>	BAY_ID <0>

Level 1/Level 2 Clock jumper position
0 = Level 1 clock configuration
1 = Level 2 clock configuration

BAY_ID<2..0>
Returns the setting of the BAY_ID dip switch settings
000 = Bay 0
001 = Bay 1
010 = Bay 2
011 = Bay 3
100 = Bay 4
101 = Bay 5
110 = Bay 6
111 = Bay 7

(Level 1 clocks always return BAY_ID = 0)