RasterOps 8XL/GSXL

Specification

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1.0 Introduction

This document establishes the physical and electrical characteristics for the RasterOps 8XL/GSXL Graphics Display System. The RasterOps 8XL/GSXL, referred to as 8XL throughout the rest of this document, is a very high resolution, very high speed, graphics display system for the Macintosh II family of computers. The 8XL occupies 1 Nubus slot. It is capable of five pixel depths and several resolutions. A block diagram of the 8XL is shown in Figure 1-1. This document is the property of RasterOps Corporation and is confidential. Reproduction of this document is prohibited.

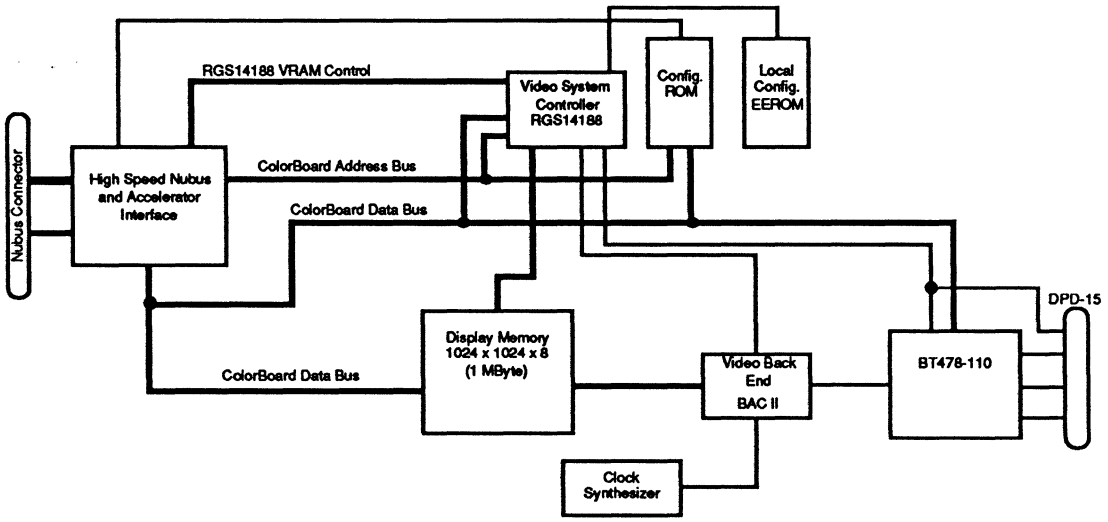

Figure 1-1 8XL Block Diagram

2.0 Hardware Description

2.1 Features

Switchable Resolutions of (Software Selectable)
- 1152 x 870 (72 Hz Vertical Refresh)
- 1024 x 768 (75 Hz Vertical Refresh)
- 1024 x 768 (60 Hz Vertical Refresh)
- 800 x 600
- 640 x 870
- 640 x 480 (66 Hz Non-interlaced)

- 640 x 480 (30 Hz Interlaced)

Pixel Depths of 1, 2, 4, and 8-bits

Macintosh II "FAT" and "Skinny" NuBus Compatible

16.7 Million Color Palette

100, 80, 64, 57, 50, and 30.24, 12.2727 MHz Video Rate

Single NuBus Slot

Current Consumption of 1.5 Amps at 5 Volts

Full Block Mode Support In All Bit-depths

RS-343 Compatible

15-Pin D-Submininature Connector (Same as Apple)

Hardware Zoom of 1x, 2x, 4x, and 8x

Hardware Pan

Extended Desktop

State of the Art Surface Mount Technology Including three ASICs

Supports the RasterOps Accelerator

2.2 Overview

The 8XL is a stand alone frame buffer. This means one can plug this card into a NuBus Slot on a Macintosh and display up to 8-bits per pixel in one of several resolutions. As an added feature the 8XL also supports a direct interface, through the NuBus, to the RasterOps Accelerator. This card provides QuickDraw acceleration capabilities making the 8XL much faster when manipulating images in any bit-depth.

3.0 Technical Data

3.1. Absolute Maximum Ratings

Supply Voltage, VCC	5.25 Volts
Operating Ambient Temperature Range	0 °C to 60 °C
Storage Temperature	-65 °C to 150 °C
ICC (Supply Current)	1.5 A @ 5.25 V

3.2 Reference Drawings

The following items should be referenced for information on the 8XL.

8XL Top Assembly LM	8XL
8XL Assembly Drawing	0002-0224
8XL Schematics	0002-0223
8XL PCB Fab	0002-0225
8XL L/M	0002-0226
8XL Manual	0700-0069

3.3 Video Specifications

3.3.1 Resolution 1152 x 870 75 Hz

1 Pixel = 10 nS = 100.0 MHz
1 VidClk = 160.0 nS = 6.25 MHz
1152 Pixels Horizontal Visible
1456 Pixels Horizontal Total
32 Pixels Horizontal Front Porch
128 Pixels Horizontal Sync
144 Pixels Horizontal Back Porch
870 Lines Vertical Visible
915 Lines Vertical Total
3 Lines Vertical Front Porch
3 Lines Vertical Sync
39 Lines Vertical Back Porch
Horizontal Frequency = 68.68 KHz
Vertical Frequency = 75.08 Hz

3.3.2 Resolution 1024 x 768 75 Hz

1 Pixel = 12.50 nS = 80.0 MHz
1 VidClk = 200.0 nS = 5.0 MHz
1024 Pixels Horizontal Visible
1328 Pixels Horizontal Total
32 Pixels Horizontal Front Porch
128 Pixels Horizontal Sync
144 Pixels Horizontal Back Porch
768 Lines Vertical Visible
802 Lines Vertical Total
3 Lines Vertical Front Porch
2 Lines Vertical Sync
29 Lines Vertical Back Porch
Horizontal Frequency = 60.24 KHz
Vertical Frequency = 75.10 Hz

3.3.3 Resolution 1024 x 768 60 Hz

1 Pixel = 15.625 nS = 64.0 MHz
1 VidClk = 250.0 nS = 4.0 MHz
1024 Pixels Horizontal Visible
1312 Pixels Horizontal Total
64 Pixels Horizontal Front Porch
96 Pixels Horizontal Sync
128 Pixels Horizontal Back Porch
768 Lines Vertical Visible
813 Lines Vertical Total
6 Lines Vertical Front Porch
6 Lines Vertical Sync
33 Lines Vertical Back Porch
Horizontal Frequency = 48.80 KHz
Vertical Frequency = 60.00 Hz

3.3.4 Resolution 800 x 600 67 Hz

1 Pixel = 20.0 nS = 50.0 MHz
1 VidClk = 320.0 nS = 3.125 MHz
800 Pixels Horizontal Visible

1024 Pixels Horizontal Total
64 Pixels Horizontal Front Porch
64 Pixels Horizontal Sync
96 Pixels Horizontal Back Porch
600 Lines Vertical Visible
730 Lines Vertical Total
48 Lines Vertical Front Porch
6 Lines Vertical Sync
79 Lines Vertical Back Porch
Horizontal Frequency = 48.80 Khz
Vertical Frequency = 66.66 Hz

3.3.5 Resolution 640 x 480 67 Hz

1 Pixel = 33.06878 nS = 30.24 MHz
1 VidClk = 529.1005 nS = 1.89 MHz
640 Pixels Horizontal Visible
864 Pixels Horizontal Total
64 Pixels Horizontal Front Porch
64 Pixels Horizontal Sync
96 Pixels Horizontal Back Porch
480 Lines Vertical Visible
525 Lines Vertical Total
3 Lines Vertical Front Porch
3 Lines Vertical Sync
39 Lines Vertical Back Porch
Horizontal Frequency = 35.0000 KHz
Vertical Frequency = 66.6666 Hz

4.0 Addressing

The 8XL needs over 1 MByte of addressable space to run in and will run under Apple's 32-bit and 24-bit versions of QuickDraw. The 16 Megabyte memory map is provided in Figure 4-1. In Figure 4-1 "Fat Slot Mode" indicates the address map when 32-bit QuickDraw is running and "Skinny Slot Mode" indicates the address map when 24-bit QuickDraw is running. There are also two modes of address decode as indicated in Figure 4-1. Both address mode give special decodes that the 8XL does not understand. The "Skinny Slot" map in Figure 4-1 shows all the accessible areas for the 8XL design. The board can be run in fat slot mode but things like the PIP and G-World RAM would obviously not function.

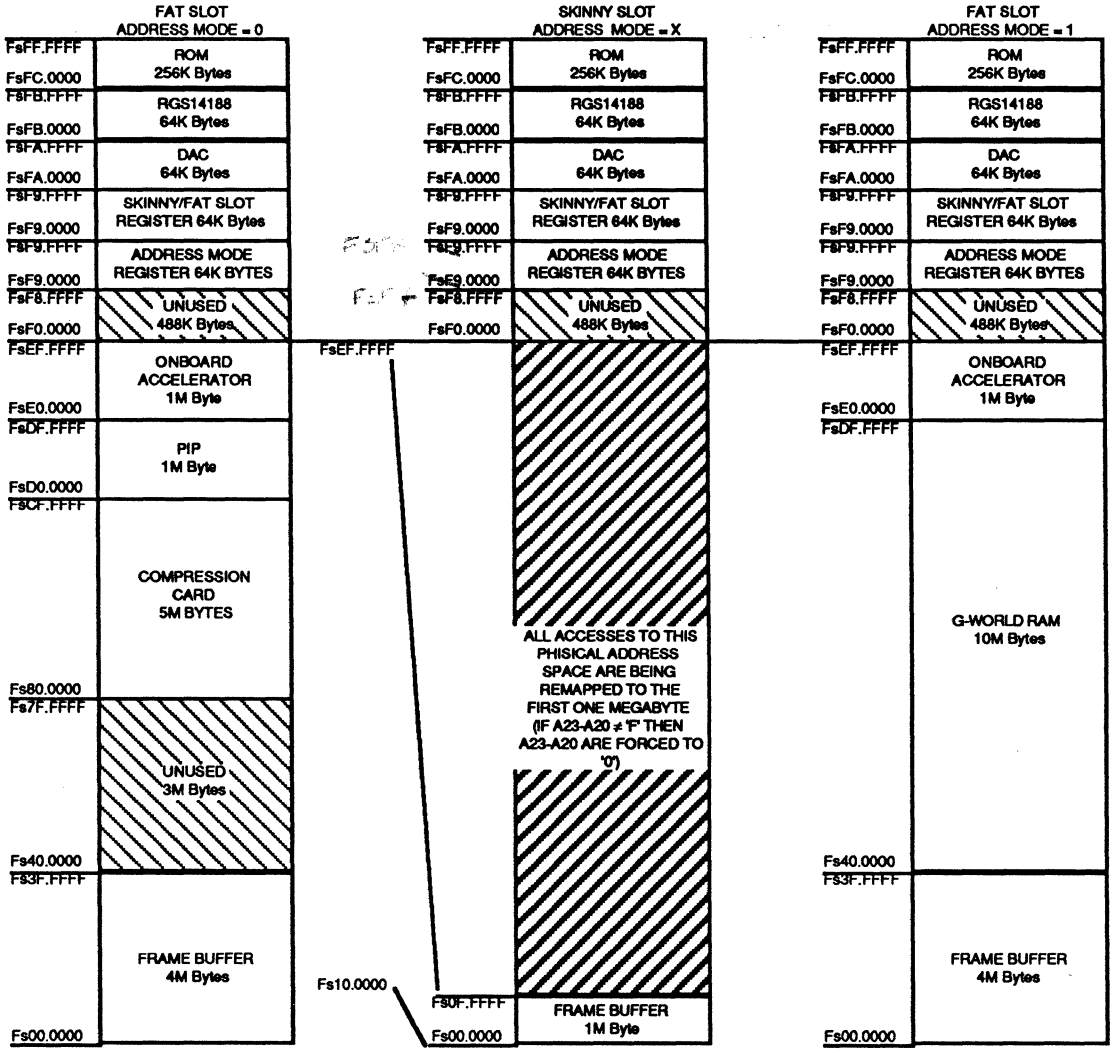

Figure 4-1 Address Map

4.1 Video System Controller - RGS14188

The RGS14188 is used to control the video display and dynamic memory of the 8XL. A brief description of the pertinent registers is given in the following sections. For more information on the RGS14188 refer to the RasterOps RGS14188 User's Guide given in Appendix A.

4.1.1 Interface Control Registers

These registers are used to control the interface and internal configuration of the RGS14188.

Register	Byte	Address	Function
Control 1		FsFB.0000	RAM Size, Arbitration etc.
Control 2		FsFB.0004	Page Mode Ctrl. General I/o Funct.
Control 3		FsFB.0008	Video Timing Interface Control
Control 4		FsFB.000C	Interrupt and Ready Control
Status		FsFB.0010	Interrupt, CRT Control Status

Table 4-1 - Interface Control Registers

4.1.2 Refresh Control

This register sets the internal refresh request interval. It should be set to approximately '9C' hex.

Register	Byte	Address	Function
Refresh Interval		FsFB.0014	Refresh Interval Duration

Table 4-2 - Refresh Control

4.1.3 Screen Update Control Registers

These registers are used to control how the actual display is updated. They provide panning capability and other important functions for screen update operation.

Register	Byte	Address	Function
Display Start	Low	FsFB.002C	Upper Left Corner of Display
	Middle	FsFB.0028	
	High	FsFB.0024	
Half Row Increment	Low	FsFB.003C	Half Row Address for VRAM
	Middle	FsFB.0038	
	High	FsFB.0034	
Display Pitch	Low	FsFB.004C	Difference between Vertially Adj. Pixels
	Middle	FsFB.0048	
	High	FsFB.0044	
Column-address Mask		FsFB.0050	Logical Column-address Mask for MLs
Horizonal Latency		FsFB.0054	Holdoff Time for Transfer Cycles

Table 4-3 - Screen Update Control

4.1.4 Horizontal Timing Control

These registers are used to control all the horizontal screen timing parameters for interlaced and non-interlaced screens.

Register	Byte	Address	Function
Horizontal End Sync	Low	FsFB.005C	Sync Duration
	High	FsFB.0058	
Horizontal End Blank	Low	FsFB.0064	Sync + Back Porch
	High	FsFB.0060	
Horizontal Start Blank	Low	FsFB.006C	Sync + Back Porch + Visible
	High	FsFB.0068	
Horizontal Total	Low	FsFB.0074	Total Visible
	High	FsFB.0070	
Horizontal Half Line	Low	FsFB.007C	Duration for Half a Line
	High	FsFB.0078	
Horizontal Count	Low	FsFB.0084	
	High	FsFB.0080	

Table 4-4 - Horizontal Timing Control

4.1.5 Vertical Timing Control

These registers are used to control all the vertical screen timing parameters for interlaced and non-interlaced screens.

Register	Byte	Address	Function
Vertical End Sync		FsFB.0088	Sync Duration
Vertical End Blank		FsFB.008C	Sync + Back Porch
Vertocal Start Blank	Low	FsFB.0094	Sync + Back Porch + Visible
	High	FsFB.0090	
Vertical Total	Low	FsFB.009C	Total Visible
	High	FsFB.0098	
Vertical Count	Low	FsFB.00A4	Start Value for Vertical Counter
	High	FsFB.00A0	
Vertical Interrupt Line	Low	FsFB.00AC	Interrupt Line
	High	FsFB.00A8	
Y-Zoom		FsFB.00B8	Y-Zoom Factor 1-256X

Table 4-5 - Vertical Timing Control

4.1.6 General Purpose Registers

These registers are used to control the general input/output functions of the RGS14188. Figure 4-2 shows exactly how each bit is defined for the 8XL system.

Register	Byte	Address	Function
General I/O Configuration	Low	FsFB.00B4	Configs. the Low Byte 0 = Input
	High	FsFB.00B0	Configs. the High Byte 0 = Input
General I/O	Low	FsFB.001C	Actual Input/Output Pins
	High	FsFB.0018	
Software Register		FsFB.00BC	General Purpose Register

Table 4-6 - General Purpose Registers

High Byte

GIO15	GIO14	GIO13	GIO12	GIO11	GIO10	GIO9	GIO8
-EE CS	EE SCLK	EE DATA IN	EE DATA OUT	VCLK1	VCLK0	Zoom1	Zoom0

Low Byte

GIO7	GIO6	GIO5	GIO4	GIO3	GIO2	GIO1	GIO0
+Gate Enable	Unused	SPD1	SPD0	CS3	CS2	CS1	CS0

Figure 4-2 General I/O Definitions

-EE CS - EEROM Chip Select
This active low bit is used to select the EEROM.

EE SCLK - EEROM Shift Clock
This bit is pulsed high then low to clock data in or out of the EEROM.

EE Data In - EEROM Data Input
This bit is tied directly to the Data In input on the EEROM.

EE Data Out - EEROM Data Output
This bit is tied directly to the Data Out output on the EEROM.

VCLK[1:0] - VIDCLK Frequency Select[1:0]
The combination of these two bits determines the VIDCLK frequency as a function of the pixel clock. Table 4-7 shows the encoding.

VCLK1	VCLK1	Output Frequency
0	0	Pixel ÷ 16
0	1	Pixel ÷ 4
1	0	Pixel ÷ 32
1	1	Pixel ÷ 8

Table 4-7 Video Clock Frequency Selections

Zoom[1:0] - Zoom Multiplier[1:0]
The combination of these two bits determines the zoom multiplier for the X direction. Table 4-8 shows the encoding.

Zoom1	Zoom0	Zoom Value
0	0	1 X (No Zoom)
0	1	2X
1	0	4X
1	1	8X

Table 4-8 Zoom Selections

+Gate Enable - Gate Enable
This bit is used to enable circuitry that will remove the first SHIFT CLOCK pulse after each horizontal blanking interval. This bit should be set to a 1 if midline transfer cycles are being used.

SPD[1:0] -Sub-pixel Depth[1:0]
The combination of these two bits determines the pixel depth when running in 1, 2, 4, or 8-bits per pixel mode. When 16 or 24-bits per pixel is used these two bits should be set to a '11' selecting a sub-pixel depth of 8-bits per pixel. Table 4-9 shows the encoding.

SPD1	SPD0	Sub-Pixel Depth
0	0	1-Bit per Pixel
0	1	2-Bit per Pixel
1	0	4-Bit per Pixel
1	1	8-Bit per Pixel

Table 4-9 Sub-pixel Depth Selections

CS[3:0] -Clock Select[1:0]
The combination of these five bits determines the pixel clock frequency and the pixel clock source. Table 4-12 shows the encoding.

CS3	CS2	CS1	CS0	Pixel Depth
0	0	0	0	12.2727 MHz
0	0	0	1	14.750 MHz
0	0	1	0	25.172 MHz
0	0	1	1	30.244 MHz
0	1	0	0	50.00 MHz
0	1	0	1	57.273 MHz
0	1	1	0	64.00 MHz
0	1	1	1	80.00 MHz
1	0	0	0	86.00 MHz
1	0	0	1	100.00 MHz
1	0	1	0	107.50 MHz
1	0	1	1	119.843 MHz
1	1	0	0	92.9405 MHz
1	1	0	1	24.5454 MHz
1	1	1	0	29.50 MHz
1	1	1	1	40.00 MHz

Table 4-12 Pixel Clock Frequency Selections

4.2 DAC

The Digital to Analog Converter is the BT478. The BT478 has a palette of 16.7 million colors. Any access (byte, word, long) is allowed but the data must always be in 68020 byte lane 3 (data bits D7 - D0). For more information on DAC addressing and functions refer to the BT478 Data Sheets. 68020 addresses A4, A3, and A2 are connected to BT478 pins RS2, RS1, and RS0 respectively.

4.2.1 Sync Sources

By installing a shunt on JP1601 "Syncs" will appear on the RED, GREEN, and BLUE analog outputs of the BT478. Removing the shunt will cause the BT478 to produce no sync pulses. This is useful for monitors that require only external TTL level syncs. For more information refer to the RasterOps 8XL users Manual. A pinout for the Video Output Connector is provided in Figure 4-3.

15-PIN DSUB CONNECTOR	
Pin 1	GROUND
Pin 2	RED
Pin 3	Composite Sync (Output Only, Active Low)
Pin 4	NO CONNECT
Pin 5	GREEN
Pin 6	GROUND
Pin 7	NO CONNECT
Pin 8	NO CONNECT
Pin 9	BLUE
Pin 10	NO CONNECT
Pin 11	NO CONNECT
Pin 12	Ext. Vertical Sync. (Output Only, Active Low)
Pin 13	GROUND
Pin 14	NO CONNECT
Pin 15	Ext. Horizontal Sync. (Output Only, Active Low)

Figure 4-3 Video Output Connector Pinout

4.3 Configuration ROM

The Configuration ROM consists of a 27C256-20 EPROM IC physically wired to the 68020 byte lane 3 (data bits D7-D0). The Configuration ROM must have a value of 78 (hex) at location FsFF.FFFF. In addition other header information must be included in the Configuration ROM for the slot manager to function properly. See chapter 8 of the Macintosh II Specification for more details on this topic.

The Configuration ROM is 8-bits wide (one byte), the data always appears in 68020 byte number 3 and any type of read access is allowed (byte, word, long).

The configuration ROM contains both a primary and secondary initialization, Apple compatible video driver, slot manager and video resources for 1, 2, 4, 8-bit mode, multiple resolution system. The primary initialization, when executed by the slot manager, initializes the DAC control registers, RGS14188 registers,

and grays the screen.

4.3.1 ROM Size Alternatives

The 8XL board is capable of supporting a 27C512 (64 KBytes instead of 32 KBytes) and directly addressing all 64 KBytes.

4.3.2 Apple Board Identification

The 8XL board is registered with Apple and has been assigned the following identifiers, which are reflected in the appropriate slot manager resources.

Board ID for RasterOps 8XL is $xxxx

Functional sResource ID for RasterOps 8XL is $xxx.

4.3.3 Video Driver

The video driver supports open, close, control, and status calls. The open routine allocates private storage, stores a handle to private storage in the dCtlStorage field of the device control entry, initializes local variables, installs an interrupt handler, and enables VBL interrupts. The close routine disables VBL interrupts from the RGS14188, removes the interrupt handler, and releases private storage. A list of supported driver calls follows.

Supported Video Driver Control Calls:

csCode	Routine
0	initialization
1	Kill I/O
2	SetMode
3	SetEntries
4	SetGamma
5	GrayScreen
6	SetGray
7	SetInterrupt

Supported Video Driver Status Calls:

csCode	Routine
0	Error

1 Error
2 GetMode
3 GetEntries
4 GetPages
5 GetBaseAddr
6 GetGray
7 GetInterrupt
8 GetGamma

5.0 Frame Buffer

The frame buffer is designed to be accessible as a Extended Desktop. This means that as the pixel bit depths and screen size decrease there is more memory available which can be used to store more pixels. The frame buffer is 1024 x 1024 in 8-bit mode. The maximum screen resolution is 1152 x 900. If smaller resolutions are selected, the user could be able to pan into the unused region of RAM that would normally not be displayable If the bit depth is reduced to 4-bit, 2-bit or 1-bit even more RAM is available for extended desktop.

Appendix 1 - RGS14188 Specification

Appendix 2 - RGS4932 Specification